

COMTEN

3650

COMMUNICATIONS CONTROL MODULE

**REFERENCE
GUIDE**

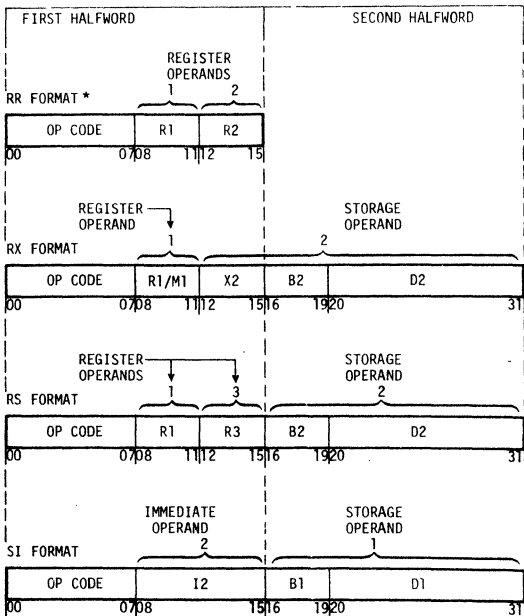
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BASIC INSTRUCTION FORMATS



*Op Code 0A hex. (SVC) uses R1, R2 fields as an Immediate Operand designated I1.

MEMORIC CODES

| | | | | | |
|-------|---------------------------------|----|------|---------------------------|----|
| A | Add | 5A | STC | Store Character | 42 |
| AH | Add Halfword | 4A | STH | Store Halfword | 40 |
| AI | Add Immediate | 9A | STPR | Set Table Pointer | 00 |
| AL | Add Logic | 5E | SVC | Supervisor Call | 0A |
| ALR | Add Logic | 1E | SWAP | Swap | 81 |
| API | Allow Pending Interrupts | 0C | TM | Test Undermask | 91 |
| AR | Add Register | 1A | TP | Test Parity | 9F |
| BAL | Branch And Link | 45 | X | Exclusive Or | 57 |
| BALR | Branch And Link | 05 | XI | Exclusive Or Immediate | 97 |
| BC | Branch on Condition | 47 | XR | Exclusive Or | 17 |
| BCR | Branch on Condition | 07 | ZIC | Zero and Insert Character | 40 |
| BCT | Branch on Count | 46 | | | |
| BCTR | Branch on Count | 06 | | | |
| BPI | Branch on I/O Interrupt Pending | 51 | | | |
| C | Compare | 59 | | | |
| CH | Compare Halfword | 49 | | | |
| CL | Compare Logical | 55 | | | |
| CLI | Compare Logical Immediate | 95 | | | |
| CLR | Compare Logical | 15 | | | |
| CR | Compare | 19 | | | |
| EIIIO | Emergency Halt I/O | 9E | | | |
| IC | Insert Character | 43 | | | |
| ITPR | Insert Table Pointer | 08 | | | |
| L | Load | 58 | | | |
| LA | Load Address | 41 | | | |
| LCR | Load Compliment | 13 | | | |
| LH | Load Halfword | 48 | | | |
| LNR | Load Negative | 11 | | | |
| LPR | Load Positive | 10 | | | |
| LPSW | Load Psw | 82 | | | |
| LR | Load | 18 | | | |
| LTR | Load and Test | 12 | | | |
| MVI | Move Immediate | 92 | | | |
| N | And | 54 | | | |
| NI | And Immediate | 94 | | | |
| NR | And | 14 | | | |
| O | Or | 56 | | | |
| OI | Or Immediate | 96 | | | |
| OR | Or | 16 | | | |
| S | Subtract | 5B | | | |
| SH | Subtract Halfword | 4B | | | |
| SIO | Start I/O | 9C | | | |
| SL | Subtract Logical | 5F | | | |
| SLA | Shift Left Arithmetic | 8B | | | |
| SLL | Shift Left Logical | 89 | | | |
| SLR | Subtract Logical | 1F | | | |
| SR | Subtract | 1B | | | |
| SRA | Shift Right Arithmetic | 8A | | | |
| SRL | Shift Right Logical | 88 | | | |
| SSM | Set System Mask | 80 | | | |
| ST | Store | 50 | | | |

INSTRUCTION LOGICAL EFFECT

| CODE | MNEMONIC | NAME | EFFECT |
|-------------------------|----------|---------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| SHIFTS | | | |
| 8B | SLA ① | Shift Left Single Arithmetic | (R1,0) no shift. (R1,1-31)L end off. Zero fill. $K=(B1)+D1$. CC. |
| 89 | SLL ① | Shift Left Single Logical | (R1,0-31)L end off. Zero fill. $K=(B1)+D1$. |
| 8A | SRA ① | Shift Right Single Arithmetic | (R1,0-31)R end off. Sign ext. $K=(B1)+D1$. CC. |
| 88 | SRL ① | Shift Right Single Logical | (R1,0-31)R end off. Zero fill. $K=(B1)+D1$. |
| BRANCHES | | | |
| 45 | BAL ② | Branch and Link | (PSW,32-63)·R1. (STO,8-31)·PSW,40-63. |
| 05 | BALR ③ | Branch and Link Register | (PSW,32-63)·R1. (R2,8-31)·PSW,40-63. |
| 47 | BC ④ | Branch on Condition | $(D2+(X2)+(B2))$ ·PSW,45-63 if M1=CC. |
| 07 | BCR ⑤ | Branch on Condition, Via Register | $(R2,13-31)+PSW,45-63$ if M1=CC. |
| 46 | BCT ② | Branch on Count | (R1) minus 1 → R1. New(R1)=0, no branch. New(R1)≠0, $(D2+(X2)+(B2))$ ·PSW,45-63 |
| 06 | BCTR ③ | Branch on Count, Via Register | (R1) minus 1 → R1. New(R1)=0, no branch. New(R1)≠0, $(R2,13-31)+PSW,45-63$. |
| 51 | BPI ⑥ | Branch on Pending I/O Interrupt | None pending: no branch. Pending: $(D2+(X2)+(B2))$ → PSW,45-63. |
| STATUS SWITCHERS | | | |
| 0C | API ⑦ | Allow pending Interrupts | None pending: no-op. Pending: (STO)·PSW,0-15; 0·PSW,16-31; (STO+4)·PSW,32-63; (STO+8)·GR14; (STO+12)·GR15. |
| 0B | ITPR ③ | Insert Table Pointer Register (See page 18) | •P2=0: CIA FAR address in GR0, 20-31. Then (CIA Address FAR) → R1, 19; (CIA Scan FAR) → R1, 20-23; (CIA Priority FAR) → R1, |

⊗ SPECIFICATION FORMATS AT HEAD OF TABLE.

INSTRUCTION LOGICAL EFFECT, CONT'D

| CODE | MNEMONIC | NAME | EFFECT |
|------|----------|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 82 | LPSW ⑦ | Load Program Status Word | 24-31. ●R2=1: CIA FAR address in GR1, 20-31. Then (CIA Address FAR)→ R1,19; (CIA Scan FAR)→ R1,20-23;(CIA Priority FAR)→R1,24-31. ● R2=2: (CHAN 2-5,E and F FAR)→ R1,19-29; 0→ Unused R1 bits. Clear interrupt request F/F. ●R2=4: (Chan 0 Interrupt + FAR) → R1,14-29; 0→ Unused R1 bits Clear interrupt request F/F. ●R2=5:(Chan 1 Interrupt FAR)→R1,14-29; 0→ Unused R1 bits Clear interrupt request F/F. ●R2=6: Chan 2-5 status → R1,24-31; 0→ Unused R1 bits. (ST0)+PSW,0-15; 0→PSW,16-31; (ST0+4)→PSW,32-63; (ST0+8)→GR10; (ST0+12)→GR11; (ST0+16)→GR12; (ST0+20)→GR13; (ST0+24)→GR14; (ST0+28)→GR15; Code I2=0. |
| 80 | SSM ⑦ | Set System Mask | (D1+(B1))→PSW,0-7. Code field I2=0. |
| 0D | STPR ③ | Set Table Pointer Register (See page 18) | ●R2=0: CIA FAR address in GR0, 20-31. Then (R1,20-23)→Scan FAR if (R1,16)=1; (R1,24-31)→Priority FAR if (R1,17)=1; (R1,19)→Address FAR when (R1,16&17)=0 or (R1,18)=1. ●R2=1: CIA FAR address in GR1,20-31. Then (R1,20-23)→Scan FAR if (R1,16)=1; (R1,24-31)→ Priority FAR if (R1,17)=1; (R1,19)→Address FAR when (R1,16&17)=0 or (R1,18)=1. ●R2=2: 180016-Chan 2-D, E&F FAR. ●R2=4: (R1,14-29)→Chan 0 Interrupt FAR, Unused R1 bits ignored. ●R2=5: (R1,14-29)→Chan 1 Interrupt FAR, Unused R1 bits ignored. ●R2=7: (R1,20-31)→Control Timer register & Timer activated. ●R2=F: CPU reset & initial load from ROM to main storage. No effect if ROM not installed. |

⊗ SPECIFICATION FORMATS AT END OF TABLE.

INSTRUCTION LOGICAL EFFECT, CONT'D

| CODE | MNEMONIC | NAME | EFFECT |
|----------|---------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0A | SVC 10 | Supervisor Call | SVC Interrupt and PSW GR swap with fixed memory addresses (hex.) as follows: PSW, 0-15; 60; 0-62; I1-63; PSW, 32-63; 64; (GR10)-68; (GR11)-6C; (GR12)-70; (GR13)-74; (GR14)-78; (GR15)-7C; (E0)-PSW, 0-15; 0-PSW, 16-31; (E4)-PSW 32-63; (E8)-GR14; (EC)-GR15. |
| LOGICALS | | | |
| 55 | CL 2 | Compare Logical | (R1) compare with (D2+(X2) (B2)). CC. |
| 15 | CLR 3 | Compare Logical Register | (R1) compare with (R2). CC. |
| 95 | CLI 9 | Compare Logical Immediate | (D1+(B1)) compare with I2. CC. |
| 43 | IC 2 | Insert Character | (D2+(X2)+(B2))·R1, 24-31. R1, 0-23 no change. |
| 41 | LA 2 | Load Address | D2+(X2)+(B2)·R1, 8-31.* 0·R1, 0-7. |
| 54 | N 2 | And | (R1)∧(D2+(X2)+(B2))·R1. CC. |
| 14 | NR 3 | And Register | (R1)∧(R2)·R1. CC. |
| 94 | NI 9 | And Immediate | (D1+(B1))∧I2·D1+(B1). CC. |
| 56 | O 2 | Or | (R1)∨(D2+(X2)+(B2))·R1. CC. |
| 16 | OR 3 | Or Register | (R1)∨(R2)·R1. CC. |
| 96 | OI 9 | Or Immediate | (D1+(B1))∨I2·D1+(B1). CC. |
| 42 | STC 2 | Store Character | (R1, 24-31)·D2+(X2)+(B2). |
| 9F | TP 2 | Test Parity | (D2+(X2)+(B2))byte odd parity test. (D2+(X2)+(B2))byte Ex-∨ (R1, 24-31)·R1. R1, 0-23 no change. CC. |
| 57 | X 2 | Exclusive Or | (R1)Ex-∨(D2+(X2)+(B2))·R1. CC. |
| 17 | XR 3 | Exclusive Or Register | (R1)Ex-∨(R2)·R1. CC. |
| 97 | XI 9 | Exclusive-Or Immediate | (D1+(B1))Ex-∨I2·D1+(B1). CC. |
| 40 | ZIC 2 | Zero and Insert Char | (D2+(X2)+(B2))byte, odd parity test. (D2+(X2)+(B2))byte·R1, 24-31. 0·R1, 0-23. CC. |
| 91 | TM 3 | Test Under Mask | (D+(B1)) compare with I2. CC. |
| 92 | MVI 3 | Move Immediate | I2·D1+(B1). |

*SUM OF D2 + (X2) + (B2), NOT THE CONTENTS OF STORAGE.
SPECIFICATION FORMATS AT END OF TABLE.

INSTRUCTION LOGICAL EFFECT, CONT'D

| CODE | MNEMONIC | NAME | EFFECT |
|------------|----------|---------------------------|---------------------------------------------------------------------------------------------|
| ARITHMETIC | | | |
| 5A | A ② | Add | $(D2+(X2)+(B2))+(R1) \rightarrow R1$. CC. |
| 1A | AR ③ | Add Register | $(R1)+(R2) \rightarrow R1$. CC. |
| 4A | AH ② | Add Halfword | $(D2+(X2)+(B2))$ halfword sign-extended to fullword $\rightarrow (R1) \rightarrow R1$. CC. |
| 9A | AI ② | Add Immediate | $(D1+(B1))$ byte $\rightarrow I2 \rightarrow D1+(B1)$. CC. |
| 5E | AL ② | Add Logical | $(D2+(X2)+(B2))+(R1) \rightarrow R1$. CC. |
| 1E | ALR ③ | Add Logical Register | $(R1)+(R1) \rightarrow R1$. CC. |
| 59 | C ② | Compare | $(D2+(X2)+(B2))$ compare with $(R1)$. CC. |
| 49 | CH ② | Compare Halfword | $(D2+(X2)+(B2))$ halfword sign-extended to fullword and compared with $(R1)$. CC. |
| 19 | CR ③ | Compare Register | $(R1)$ compare with $(R2)$. CC. |
| 58 | L ② | Load | $(D2+(X2)+(B2)) \rightarrow R1$. |
| 13 | LCR ② | Load Complement Register | $(\overline{R2}) \rightarrow R1$. CC. |
| 48 | LH ② | Load Halfword | $(D2+(X2)+(B2))$ halfword sign-extended to fullword $\rightarrow R1$. |
| 11 | LNR ③ | Load Negative Register | $ \overline{(R2)} \rightarrow R1$. CC. |
| 10 | LPR ③ | Load Positive Register | $ (R2) \rightarrow R1$. CC. |
| 18 | LR ③ | Load Register | $(R2) \rightarrow R1$. |
| 12 | LTR ③ | Load and Test Register | $(R2) \rightarrow R1$. CC. |
| 5B | S ① | Subtract | $(R1)$ minus $(D2+(X2)+(B2)) \rightarrow R1$. CC. |
| 4B | SH ② | Subtract Halfword | $(R1)$ minus $(D2+(X2)+(B2))$ halfword sign-extended $\rightarrow R1$. CC. |
| 5F | SL ② | Subtract Logical | $(R1)$ minus $(D2+(X2)+(B2)) \rightarrow R1$. CC. |
| 1F | SLR ③ | Subtract Logical Register | $(R1)$ minus $(R2) \rightarrow R1$. CC. |
| 1B | SR ③ | Subtract Register | $(R1)$ minus $(R2) \rightarrow R1$. CC. |
| 50 | ST ② | Store | $(R1) \rightarrow D2+(X2)+(B2)$. |
| 40 | STH ② | Store Halfword | $(R1, 16-31) \rightarrow D2+(X2)+(B2)$. |
| 81 | SWAP ② | Swap | $(R1) \rightarrow D2+(X2)+(B2)$. $(D2+(X2)+(B2)) \rightarrow R1$. Simultaneous. CC. |

⊗ SPECIFICATION FORMATS AT END OF TABLE.

INSTRUCTION LOGICAL EFFECT, CONT'D

| CODE | MNEMONIC | NAME | EFFECT |
|------|----------------|-----------------------------|-------------|
| 9C | SIO 11 | Start Input/Output | See Page13. |
| 9E | EHIO 11 | Emergency Halt Input Output | See Page13. |

SYMBOL

DEFINITIONS

| | |
|------------|-------------------|
| CC | Condition Code |
| K | Shift Count |
| L | Left |
| R | Right |
| STO or | D1+(B1) |
| STO | D1+(X2)+(B2) |
| () | Contents of |
| = | Equals |
| ≠ | Not Equal |
| ≡ | Equivalent to |
| - | Through |
| + | Plus |
| Λ | AND |
| V | OR |
| In-V | Inclusive-OR |
| Ex-V | Exclusive-OR |
| (overline) | Complement of |
| | Absolute Value of |
| + | Transfer to |

TRUTH TABLE: Operand A 1 1 0 0
 Operand B 1 0 1 0

| | | | | |
|------|---|---|---|---|
| A | 1 | 0 | 0 | 0 |
| In-V | 1 | 1 | 1 | 0 |
| Ex-V | 0 | 1 | 1 | 0 |

SPECIFICATION FORMATS

| | |
|-----------|----------------|
| 1 | R1, D2, B2 |
| 2 | R1, D2, X2, B2 |
| 3 | R1, R2 |
| 4 | M1, D2, X2, B2 |
| 5 | M1, R2 |
| 6 | D2, X2, B2 |
| 7 | D1, B1 |
| 8 | R2, D2, X2, B2 |
| 9 | I2, D1, B1 |
| 10 | I1 |
| 11 | C, CC, B1, L* |

*C = Channel Number

L = Line Number (if applicable)

CC = Channel Code (if applicable)

EXTENDED MNEMONICS

| CODE | MNEMONIC | SPECIFICATION | CONDITION |
|-------------------------|----------|---------------|----------------------------------|
| GENERAL | | | |
| 47F | B | D2,X2,B2 | Branch Unconditionally |
| Ø7F | BR | R2 | Branch Unconditionally |
| 47Ø | NOP | _____ | No Operation |
| Ø7Ø | NOPR | _____ | No Operation |
| AFTER COMPARE | | | |
| 472 | BH | D2,X2,B2 | Branch On First Operand High |
| Ø72 | BHR | R2 | Branch On First Operand High |
| 474 | BL | D2,X2,B2 | Branch On First Operand Low |
| Ø74 | BLR | R2 | Branch On First Operand Low |
| 477 | BNE | D2,X2,B2 | Branch On Operands Not Equal |
| Ø77 | BNER | R2 | Branch On Operands Not Equal |
| 478 | BE | D2,X2,B2 | Branch On Operands Equal |
| Ø78 | BER | R2 | Branch On Operands Equal |
| 47B | BNL | D2,X2,B2 | Branch On First Operand Not Low |
| Ø7B | BNLR | R2 | Branch On First Operand Not Low |
| 47D | BNH | D2,X2,B2 | Branch On First Operand Not High |
| Ø7D | BNHR | R2 | Branch On First Operand Not High |
| AFTER ARITHMETIC | | | |
| 4/1 | BO | D2,X2,B2 | Branch On Overflow |
| Ø71 | BOR | R2 | Branch On Overflow |
| 472 | BP | D2,X2,B2 | Branch On Positive |
| Ø72 | BPR | R2 | Branch On Positive |
| 474 | BM | D2,X2,B2 | Branch On Minus |
| Ø74 | BMR | R2 | Branch On Minus |
| 477 | BNZ | D2,X2,B2 | Branch On Not Zero |
| Ø77 | BNZR | R2 | Branch On Not Zero |
| 478 | BZ | D2,X2,B2 | Branch On Zero |
| Ø78 | BZR | R2 | Branch On Zero |

EXTENDED MNEMONICS, CONT'D

| CODE | MNEMONIC | SPECIFICATION | CONDITION |
|-------------------------------------|----------|---------------|-------------------------|
| AFTER ARITHMETIC (cont'd) | | | |
| 47B | BNM | D2,X2,B2 | Branch On Not Minus |
| 07B | BNMR | R2 | Branch On Not Minus |
| 47D | BNP | D2,X2,B2 | Branch On Not Positive |
| 07D | BNPR | R2 | Branch On Not Positive |
| 47E | BNOV | D2,X2,B2 | Branch On Not Overflow |
| 07E | BNOVR | R2 | Branch On Not Overflow |
| AFTER TEST UNDER MASK | | | |
| 471 | BO | D2,X2,B2 | Branch If All Ones |
| 071 | BOR | R2 | Branch If All Ones |
| 474 | BM | D2,X2,B2 | Branch If Mixed |
| 074 | BMR | R2 | Branch If Mixed |
| 477 | BNZ | U2,X2,B2 | Branch If Not All Zeros |
| 077 | BNZR | R2 | Branch If Not All Zeros |
| 478 | BZ | D2,X2,B2 | Branch If All Zeros |
| 078 | BZR | R2 | Branch If All Zeros |
| 47E | BNOV | D2,X2,B2 | Branch If Not All Ones |
| 07E | BNOVR | R2 | Branch If Not All Ones |
| AFTER PARITY CONDITION CODE SETTING | | | |
| 471 | BOD | D2,X2,B2 | Branch If Odd |
| 071 | BODR | R2 | Branch If Odd |
| 47C | BEV | D2,X2,B2 | Branch If Even |
| 07C | BEVR | R2 | Branch If Even |

CONDITION CODE SETTINGS

| MASK BITS | | | | 8 | 4 | 2 | 1 | | |
|----------------|----------|--------------------------|------|--------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------|------------|-----------------------|
| CONDITION CODE | | | | 0 | 1 | 2 | 3 | | |
| CODE | MNEMONIC | NAME | TYPE | RESULT = ZERO, NO CARRY ITPR NORMAL/RESULT = ZERO OPERANDS ARE EQUAL EVEN PARITY, BYTE = ZERO | RESULT # ZERO, NO CARRY RESULT LESS THAN ZERO FIRST OPERAND LOW | RESULT = ZERO, CARRY RESULT GREATER THAN ZERO FIRST OPERAND HIGH | RESULT # ZERO, CARRY OVERFLOW | ODD PARITY | CYCLES: 1 = 650 nsec. |
| 05 | BALR | Branch and Link | RR | | | | | | 4 |
| 06 | BCTR | Branch on Count | RR | | | | | | 4 |
| 07 | BCR | Branch on Condition | RR | | | | | | 3 |
| 0A | SVC | Supervisor Call | RR | | | | | | 27 |
| 0B | ITPR | Insert Table Pointer | RR | X* | | | | X* | 3 ϕ |
| 0C | API | Allow Pending Interrupts | RR | | | | | | 10 Δ |
| 0D | STPR | Set Table Pointer | RR | | | | | | 2 |
| 10 | LPR | Load Positive | RR | X | | X | X | X | 3 |
| 11 | LNR | Load Negative | RR | X | X | | | | 3 |
| 12 | LTR | Load and Test | RR | X | X | X | | | 3 |
| 13 | LCR | Load Complement | RR | X | X | X | X | | 3 |
| 14 | NR | And | RR | X | X | | | | 3 |
| 15 | CLR | Compare Logical | RR | X | X | X | | | 3 |
| 16 | OR | Or | RR | X | X | | | | 3 |
| 17 | XR | Exclusive Or | RR | X | X | | | | 3 |
| 18 | LR | Load | RR | | | | | | 3 |
| 19 | CR | Compare | RR | X | X | X | | | 3 |
| 1A | AR | Add Register | RR | X | X | X | X | | 3 |
| 1B | SR | Subtract | RR | X | X | X | X | | 3 |

NOTES:

* Set only if R2= 2-D

ϕ 3 if R2= 2-D
3 + I/O if R2=0,1,4,
C,D,E, or F and INT.

Δ 2 if no pending INT,
10 if pending INT.

CONDITION CODE SETTINGS, CONT'D

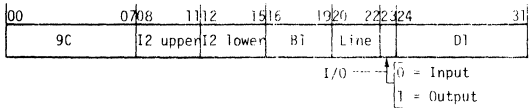
| MASK BITS | | | | 8 | 4 | 2 | 1 | | | | | | | | | | | | |
|----------------|-----------|---------------------------------|------|-------------------------|---------------------------|--------------------|--------------------------|-------------------------|-----------------------|-------------------|--------------------------|----------------------|--------------------------|--------------------|----------------------|----------|------------|-----------------------|------------|
| CONDITION CODE | | | | 0 | 1 | 2 | 3 | | | | | | | | | | | | |
| CODE | MNEUMONIC | NAME | TYPE | RESULT = ZERO, NO CARRY | ITPR NORMAL/RESULT = ZERO | OPERANDS ARE EQUAL | EVEN PARITY, BYTE = ZERO | RESULT ≠ ZERO, NO CARRY | RESULT LESS THAN ZERO | FIRST OPERAND LOW | EVEN PARITY, BYTE ≠ ZERO | RESULT = ZERO, CARRY | RESULT GREATER THAN ZERO | FIRST OPERAND HIGH | RESULT ≠ ZERO, CARRY | OVERFLOW | ODD PARITY | CYCLES: 1 = 650 nsec. | EXCEPTIONS |
| | | | | 1E | ALR | Add Logical | RR | X | | | X | | | | X | | | X | |
| 1F | SLR | Subtract Logical | RR | | | | X | | | | X | | | X | | | | 3 | |
| 40 | STH | Store Halfword | RX | | | | | | | | | | | | | | | 3 | SPC |
| 41 | LA | Load Address | RX | | | | | | | | | | | | | | | 5 | |
| 42 | STC | Store Character | RX | | | | | | | | | | | | | | | 3 | |
| 43 | IC | Insert Character | RX | | | | | | | | | | | | | | | 3 | |
| 45 | BAL | Branch and Link | RX | | | | | | | | | | | | | | | 5 | |
| 46 | BCT | Branch on Count | RX | | | | | | | | | | | | | | | 5 | |
| 47 | BC | Branch on Cond. | RX | | | | | | | | | | | | | | | 3 | |
| 48 | LH | Load Halfword | RX | | | | | | | | | | | | | | | 4 | SPC |
| 49 | CH | Compare Halfword | RX | | X | | | X | | | | X | | | | | | 4 | SPC |
| 4A | AH | Add Halfword | RX | X | | | X | | | | X | | X | | | | | 4 | SPC |
| 4B | SH | Subtract Halfword | RX | X | | | X | | | | X | | X | | | | | 4 | SPC |
| 4D | ZIC | Zero & Insert Character | RX | | | X | | | X | | | | | | X | | | 4 | |
| 50 | ST | Store | RX | | | | | | | | | | | | | | | 4 | SPC |
| 51 | BPI | Branch on I/O Interrupt Pending | RX | | | | | | | | | | | | | | | 3 | |
| 54 | N | And | RX | X | | | X | | | | | | | | | | | 4 | SPC |
| 55 | CL | Compare Logical | RX | | X | | | X | | | | X | | | | | | 4 | SPC |
| 56 | O | Or | RX | X | | | X | | | | | | | | | | | 4 | SPC |
| 57 | X | Exclusive Or | RX | X | | | X | | | | | | | | | | | 4 | SPC |
| 58 | L | Load | RX | | | | | | | | | | | | | | | 4 | SPC |

CONDITION CODE SETTINGS, CONT'D

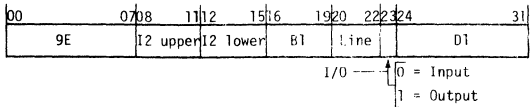
| MASK BITS | | | | 8 | 4 | 2 | 1 | |
|----------------|----------|---------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|--------|
| CONDITION CODE | | | | 0 | 1 | 2 | 3 | |
| CODE | MNEMONIC | NAME | TYPE | RESULT = ZERO, NO CARRY ITPR NORMAL/RESULT = ZERO OPERANDS ARE EQUAL EVEN PARITY, BYTE = ZERO SELECTED BITS ALL-ZERO; MASK IS ALL-0 RESULT ≠ ZERO, NO CARRY RESULT LESS THAN ZERO FIRST OPERAND LOW EVEN PARITY, BYTE ≠ ZERO SELECTED BITS MIXED ZERO AND ONE RESULT = ZERO, CARRY RESULT GREATER THAN ZERO FIRST OPERAND HIGH RESULT ≠ ZERO, CARRY OVERFLOW ODD PARITY SELECTED BITS ALL-ONE | | | | |
| 59 | C | Compare | RX | X | X | X | | 4 SPC |
| 5A | A | Add | RX | X | X | X | X | 4 SPC |
| 5B | S | Subtract | RX | X | X | X | X | 4 SPC |
| 5E | AL | Add Logical | RX | X | X | X | X | 4 SPC |
| 5F | SL | Subtract Logical | RX | | X | X | X | 4 SPC |
| 80 | SSM | Set System Mask | SI | | | | | 3 |
| 81 | SWAP | Swap | RX | X | X | X | | 6 SPC |
| 82 | LPSW | Load PSW | SI | | | | | 20 SPC |
| 88 | SRL | Shift Right Logical | RS | | | | | 6 |
| 89 | SLL | Shift Left Logical | RS | | | | | 6 |
| 8A | SRA | Shift Right Arith. | RS | X | X | X | | 6 |
| 8B | SLA | Shift Left Arith. | RS | X | X | X | X | 6 |
| 91 | TM | Test Undermask | SI | | X | X | | 4 |
| 92 | MVI | Move Immediate | SI | | | | X | 4 |
| 94 | NI | And Immediate | SI | X | X | | | 4 |
| 95 | CLI | Compare Logical Immediate | SI | X | X | X | | 4 |
| 96 | OI | Or Immediate | SI | X | X | | | 4 |
| 97 | XI | Exclusive Or Immediate | SI | X | X | | | 4 |
| 9A | AI | Add Immediate | SI | X | X | X | X | 4 |
| 9C | SIO | Start I/O | SI | | | | | 3 |
| 9E | EHIO | Emergency Halt I/O | SI | | | | | 3 |
| 9F | TP | Test Parity | RX | X | X | | X | 4 |

START AND EMERGENCY HALT I/O INSTRUCTIONS

SIO

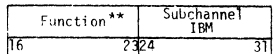


EHIO

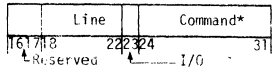


SIO and EHIO effect: (B1) + D1 + external device on channel designated by I2.

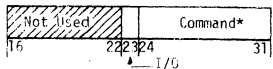
I2u = 0,1; then (B1) + D1 =



I2u = 2-5; then (B1) + D1 =



I2u = E,F; then (B1) + D1 =



* Command only with SIO. See pages 15 through 17.

** See CIA Functions on page 14.

I2 FIELD DEFINITIONS

| HEX I2 upper | CODE I2 lower | SELECTION |
|-----------------|------------------|-----------------------------|
| 2 | 0 | MIM's and 1, Lines 0-31 |
| 3 | 0 | MIM's 2 and 3, Lines 32-63 |
| 4 | 0 | MIM's 4 and 5, Lines 64-95 |
| 5 | 0 | MIM's 6 and 7, Lines 96-127 |
| E | 0 | Cassette |
| F | 0 | Console |
| 0 | 4 | CPU Interface 0 |
| 1 | 5 | CPU Interface 1 |

FUNCTIONS FOR CIA ATTACHED TO CPU INTERFACE

| HEX CODE | FUNCTION |
|----------|--------------------------------------------|
| 04 | Direct-Input Data Transfer (IBM Write) |
| 05 | Direct-Output Data Transfer (IBM Read) |
| 06 | BCW-Input Data Transfer (IBM Write) |
| 07 | BCW-Output Data Transfer (IBM Read) |
| 08 | Status Transfer Request |
| 18 | Queue Special Status Transfer Request |
| 20 | Clear Reset/Disconnect |
| 28 | Clear Reset/Disconnect and Transfer Status |
| 40 | Prepare to Go Off-Line |
| 50 | Go Off-Line |
| 70 | Go On-Line |
| 80 | Command Test Sequence |
| 84-87 | Data Transfer Tests |
| 88 | Status Transfer Test |

COMMANDS FOR 16-LINE, A-MIM T2016-00,01

| | | | | | | | | |
|----|----|----|----|----|----|----|----|---------------------------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Command Byte Bit Position |
| L | | S | | | B | | | Command Byte |
| 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | SIO Bit Position |

| | | | |
|---|---|---|-------------|
| 0 | 0 | 0 | Baud Rate 0 |
| 0 | 0 | 1 | Baud Rate 1 |
| 0 | 1 | 0 | Baud Rate 2 |
| 0 | 1 | 1 | Baud Rate 3 |
| 1 | 0 | 0 | Baud Rate 4 |
| 1 | 0 | 1 | Baud Rate 5 |
| 1 | 1 | 0 | Baud Rate 6 |
| 1 | 1 | 1 | Baud Rate 7 |

| | | | |
|---|---|---|---------------------------|
| 0 | 0 | 0 | 1 Stop Bit |
| 0 | 0 | 1 | 2 Stop Bit* |
| 0 | 1 | 0 | Break (Output) |
| 0 | 1 | 1 | Busy Out (Output) |
| 1 | 0 | 0 | Comcheck And 1 Stop-Bit |
| 1 | 0 | 1 | Comcheck And 2 Stop-Bit** |
| 1 | 1 | 0 | Send Marks |
| 1 | 1 | 1 | Sample Mode (Input) ABRD |

| | | |
|---|---|--------------|
| 0 | 0 | 8-Level Code |
| 0 | 1 | 7-Level Code |
| 1 | 0 | 6-Level Code |
| 1 | 1 | 5-Level Code |

* 1-1/2 or 2 stop bits (Strap option)

** Supervisory Xmit (0H) T2016-02.

COMMANDS FOR MIM's (except 16 Line A-MIM)

| HEX CODE | MIM TYPE | COMMAND |
|----------|------------------|---------------------------------------------|
| 00 | A11 | Start Input (bit 23=0) or Output (bit 23=1) |
| 01 | ADS,S,BSC | Pass Raw Data |
| 02 | A11 but BSC | Probe for Status |
| 04 | S,ADS,BSC,and IS | New Sync/(Transparent Mode in IS-MIM) |
| 08 | A11 | Comm-Check |
| 10 | ADS,ADA,BSC | Dial Out |
| 20 | A,ADA | Send Break |
| 21 | A,ADA | Start Supervisory Transmit |
| 41 | A,ADA | Stop Supervisory Transmit |
| 80 | 16 L- BSC | SIO DTR on |
| 02 | BSC | Inhibit I1B |
| 20 | BSC | Inhibit Data Transfer |
| 40 | ECA | Send Break |

COMMANDS FOR TAPE CASSETTE

| HEX CODE | SI or SO | COMMAND |
|----------|----------|-----------------------|
| 01 | SO | Write on Tape |
| 02 | SO | Erase Tape |
| 03 | SO | Write with Read Check |
| 07 | SI | Read |
| 05 | SI | Backspace |
| 06 | SI | Rewind |
| 04 | SI | Bootstrap |

INSERT AND SET TABLE POINTER INSTRUCTIONS

| | | | | |
|-------|----|------|------|----|
| | 00 | 0708 | 1112 | 15 |
| ITPR* | OB | R1 | R2 | |
| STPR | OD | R1 | R2 | |

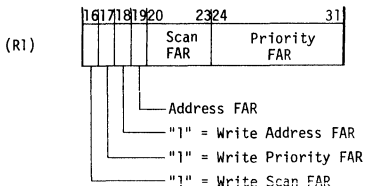
*ITPR is the only means of clearing an Interrupt Table's Interrupt Request ff.

| R2 Code (Hex) | Accesses | | | | | | | | | |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|------|----|---------|------|--|-----|-------|--|
| 4 (Chan 0) | 19-Bit Channel 0/1 Interrupt Table Pointer FAR. | | | | | | | | | |
| 5 (Chan 1) | | | | | | | | | | |
| 2 | 8-Bit Channel 2-5, E&F Interrupt Table Pointer FAR. If overflow in detected, CC=3. | | | | | | | | | |
| 0 (Chan 0) | GRO contains CIA FAR address, bits**20-31. | | | | | | | | | |
| 1 (Chan 1) | GR1 contains CIA FAR address. | | | | | | | | | |
| 6 (ITPR only) | Comm Line Instant Status to R1, bits 24-31. When R2=6, (R6) = <table border="1" style="display: inline-table; vertical-align: middle; text-align: center;"> <tr> <td style="border: none;">23</td> <td style="border: none;">2627</td> <td style="border: none;">31</td> </tr> <tr> <td style="border: none;">Channel</td> <td style="border: none;">Line</td> <td style="border: none;"></td> </tr> <tr> <td style="border: none;">2-5</td> <td style="border: none;">00-1F</td> <td style="border: none;"></td> </tr> </table> | 23 | 2627 | 31 | Channel | Line | | 2-5 | 00-1F | |
| 23 | 2627 | 31 | | | | | | | | |
| Channel | Line | | | | | | | | | |
| 2-5 | 00-1F | | | | | | | | | |
| 7 | (R1,20-31)→Control Timer Register & Activate Timer | | | | | | | | | |
| 8-E | Not Used | | | | | | | | | |
| F | Specifies Initial load from ROM (STPR only) | | | | | | | | | |

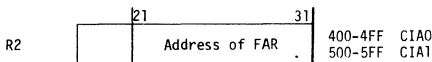
*See FAR Address Map in Hardware General Reference Manual for addresses.

LOADING and TESTING ADDRESS FAR, SCAN FAR and PRIORITY FAR

The Set Table Pointer (STPR) instruction (ODR_1R_2) must have the R_2 field coded as zero for communication with a CIA attached to channel zero and coded as one for a CIA attached to channel one. General register zero or one is then used to address the Scan FAR, Priority FAR and/or the Address FAR (400_{16} to $4FF_{16}$ or 500_{16} to $5FF_{16}$). The General Register specified by the R_1 field contains the data to be written. Bits 20 to 23 are used to load the Scan FAR. The Scan register will only be written when bit 16 is a one. The CIA uses bits 24 to 31 to load the Priority FAR. The Priority FAR will only be loaded when bit 17 is a one. The Address FAR is loaded with the value of bit 19 when both bits 16 and 17 are zeros or when bit 18 is a one.



NOTE: If (R1) bits 16, 17 and 18 are all zero, write bit 19 into Address FAR

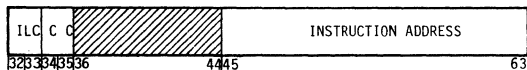
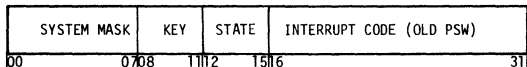


The Insert Table Pointer (ITPR) instruction (OBR_1R_2) uses the R_2 field identically to the STPR instruction. The contents of the Address FAR, Scan FAR and Priority FAR are loaded into bits 19, 20 to 23 and 24 to 31 respectively of the General Register specified by R_1 . The Scan FAR, Priority FAR and Address FAR are accessed simultaneously by the ITPR instruction.

The CIA will accept an STPR instruction only when off-line. It can accept an ITPR instruction at any time, but the value of the Address FAR location (bit 19) and the Priority FAR (bits 24-31) will only be valid when the CIA is off-line.

PROCESSOR HARDWARE FORMATS

PROGRAM STATUS WORD



System Mask, Bits 0-7 0-3

Bits 0-3 are simply carried with the old and new PSWs. COMTEN software conventions treat this field as either a 4 bit program number or a system performance measurement. Of the sixteen states available only seven are currently defined as follows:

PSW bits 0-3

Measurement Meaning

| | |
|----------|-----------------------------------------------------------------------------|
| 0 - 0000 | Wait state. |
| 1 - 0001 | Communications channel interrupt handling state with interrupts locked out. |
| 2 - 0010 | Channel 0 interrupt handling state with interrupts locked out. |
| 3 - 0011 | Channel 1 interrupt handling state with interrupts locked out. |
| 4 - 0100 | Non-interruptable task and time task state, |
| 5 - 0101 | Low priority interruptable task state. |
| 6 - 0110 | Low priority non-interruptable task state. |
| 7 - 0111 | Reserved for future use by NCP and DSS. |
| F - 1111 | |

- 4 Machine Fault: 1=Allow Storage Parity Error Interrupts
- 5 I/O Lockout: 1=disable all I/O Data and Status Transfers and tabling of Interrupts.
- 6 Timer: 1=allow Timer Interrupts.
- 7 I/O Interrupts: 0=disable Immediate I/O Interrupts but allow tabling.

| | | |
|-------------------------|----------------|-----------------------------------------------------------------|
| Protection Key | 8-11 | hardware-ignored. |
| State | 12,14,15 13 | hardware-ignored 1=Interrupt State. Set by execution of API. |
| Instruction Length Code | 32,33 | 01=RR; 10=RX, RS or SI. |
| Condition Code | 34,35 | (see previous pages 10, 11, and 12) |
| Unused | 36-44 | |
| Instruction Address | 45-63 | Next instruction's Address |

STORAGE ASSIGNMENTS

| BYTE STORAGE LOCATION | | USE |
|-----------------------|-------------|------------------------------------------------------|
| DECIMAL | HEXIDECIMAL | |
| 0-63 | 0-3F | Storage for software |
| 64-239 | 40-EF | Old and New PSWs (See Figure 1.1) |
| 242-243 | F2-F3 | Timer |
| 244-255 | F4-FF | Day Clock (software) |
| 256-287 | 100-11F | Channel E Cassette Control Packet |
| 288-319 | 120-13F | Channel F Console Control Packet. |
| 320-327 | 140-147 | 45/65 Control Packet Address |
| 328-343 | 148-157 | Interrupt Storage 360/370 Subchannel |
| 344-511 | 158-1FF | Reserved for future use |
| 512-1023 | 200-3FF | Storage for software |
| 1024-3071 | 400-BFF | Communications Line Control Packets, Lines 0-63 |
| 3072-4095 | C00-FFF | Storage for software |
| 4096-6143 | 1000-17FF | Communications Line Control Packets, Lines 64-127 |
| 6144-7167 | 1800-1BFF | Communications Interrupt Table |
| 7168-7679 | 1C00-1DFF | 360/370 CIA 0 Subchannel Control Packet Address |
| 7680-8191 | 1E00-1FFF | 360/370 CIA 1 Subchannel Control Packet Address |
| 8192-262,143 | 2000-3FFFF | Storage for software |

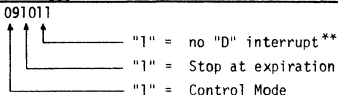
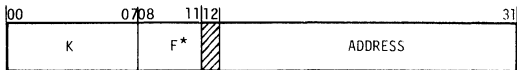
Program Status Word Table

| BYTE DECIMAL | ADDRESSES HEXADECIMAL | ASSIGNMENT | INTERRUPT TYPES |
|-----------------------------------------|----------------------------------|---------------------------------------------------|-----------------------------------------------------------------|
| 64-71 72-79 80-87 88-95 | 40-47 48-4F 50-57 58-5F | Old PSW GR10, GR11 GR12, GR13 GR14, GR15 | Machine Fault and Program Error Inter- rupts |
| 96-103 104-111 112-119 120-127 | 60-67 68-6F 70-77 78-7F | Old PSW GR10, GR11 GR12, GR13 GR14, GR15 | I/O Interrupts, Timer Interrupts, Supervisor Call Interrupts |
| 128-135 136-143 | 80-87 88-8F | New PSW GR14, GR15 | Machine Fault Interrupt |
| 144-151 152-159 | 90-97 98-9F | New PSW GR14, GR15 | Program Error Interrupt |
| 160-167 168-175 | A0-A7 A8-AF* | New PSW GR14, GR15 | Channel 0 Interrupts |
| 176-183 184-191 | B0-B7 B8-BF** | New PSW GR14, GR15 | Communications Interrupts |
| 192-199 200-207 | C0-C7 C8-CF*** | New PSW GR14, GR15 | Channel 1 Interrupts |
| 208-215 216-223 | D0-D7 D8-DF | Not Used Not Used | Not Used Not Used |
| 224-231 232-239 | E0-E7 E8-EF | New PSW GR14, GR15 | SVC, Timer Interrupts |

*A8 - Address of next Channel 0 Interrupt
 **B8 - Address of next Comm-Line Interrupt
 ***C8 - Address of next Channel 1 Interrupt

} FIRMWARE
 } POINTERS

BUFFER CONTROL WORD *



K = Count (count field = 0 specifies 256 bytes)

F = Function

- F = 0 (Transfer, Continue, "D" Interrupt)
- F = 1 (Transfer, Continue, No "D" Interrupt)
- F = 2 (Transfer, Stop, "D" Interrupt)
- F = 3 (Transfer, Stop, No "D" Interrupt)
- F = 4 (Control, Continue, "D" Interrupt)
- F = 5 (Control, Continue, No "D" Interrupt)
- F = 6 (Control, Stop, "D" Interrupt)
- F = 7 (Control, Stop, No "D" Interrupt)
- F = F (Unconditional Stop)

* Notes: Function field is not used with CIA.

**Buffer Expiration

CHANNEL IPL ROM STRAPPING - FEATURE 1034-00

| | | | | | |
|-----------------------------|-----------------------------|-------------|-------|----------|----------|
| 0 | 78 | 11 12 13 14 | 15 16 | 23 24 | 31 |
| HOST 1 IPL SUBCHANNEL | HOST 2 IPL SUBCHANNEL | | | Reserved | Reserved |
| MEMORY SIZE | CPU TYPE | * | ** | R R | RESERVED |

* CHANNEL 0 INTERRUPT TABLE SIZE — Interface Status ***

** CHANNEL 1 INTERRUPT TABLE SIZE

*** 0 = interface not available

1 = interface available

VARIABLE DATA VALUES:

SUBCHANNELS - HEXIDECIMAL VALUE OF THE IPL SUBCHANNEL FOR THAT HOST

MEMORY SIZE - EACH INCREMENT REPRESENTS 16K. A MACHINE WITH 16K
WOULD HAVE A VALUE OF 1 STRAPPED

CPU TYPE - 0 - 3670-00
1 - 3670-01
2 - 3650
3-15 - RESERVED

INTERRUPT TABLE SIZE - 0 - 256 bytes (64 words)
1 - 512 bytes (128 words)
2 - 1024 bytes (256 words)
3 - Reserved

Memory locations 20 to 27 are loaded from the 8 bytes of variable data.

Communications Line Control Packet Format

| | | | | | | | |
|-----|----------------------------------------------|---------------------------------------|--------|-----------------|----------------|----|--------------------|
| | 00 | 0708 | 111213 | 16 | 2324 | 31 | |
| +0 | COUNT | FUNCTION | | | BUFFER ADDRESS | | INPUT ACTIVE BCW |
| +4 | COUNT | FUNCTION | | | BUFFER ADDRESS | | INPUT STANDBY BCW |
| +8 | INPUT INT PTG OFFSET | ACTIVITY FLAG 1 | | ACTIVITY FLAG 2 | EMULATOR INDEX | | |
| +C | INPUT MULTIPLEXER SUBCHANNEL PACKET ADDRESS | | | | INPUT TIMER | | |
| +10 | COUNT | FUNCTION | | | BUFFER ADDRESS | | OUTPUT ACTIVE BCW |
| +14 | COUNT | FUNCTION | | | BUFFER ADDRESS | | OUTPUT STANDBY BCW |
| +18 | OUTPUT INT PTG OFFSET | SECONDARY LINE CONTROL PACKET ADDRESS | | | | | |
| +1C | OUTPUT MULTIPLEXER SUBCHANNEL PACKET ADDRESS | | | | OUTPUT TIMER | | |

SECONDARY LINE CONTROL PACKET

| | | | | | | |
|-----|-------------------------------|--------------------|------------------|-------------------------------------|----|-------------------------|
| | 00 | 0708 | 1516 | 2324 | 31 | |
| +0 | I/O MODE | CHANNEL NUMBER 2-D | LINE NUMBER 0-31 | FUNCTION | | START I/O CONTROL WORD |
| +4 | CURRENT COMMAND | LAST COMMAND | | | | |
| +8 | EMU OPTION 1 | EMU OPTION 2 | LINE OPTION 3 | LINE OPTION 4 | | EMULATOR LINE OPERATORS |
| +C | AUTO-CALL ADAPTER LINE NUMBER | | | AUTO-CALL UNIT RELATIVE PORT NUMBER | | |
| +10 | FOR FIRMWARE USE | | | | | |
| | CHARACTER 0 | CHARACTER 1 | CHARACTER 2 | CHARACTER 3 | | INPUT BUFFER NO. 1 |
| | CHARACTER 0 | CHARACTER 1 | CHARACTER 2 | CHARACTER 3 | | INPUT BUFFER NO. 2 |
| | CHARACTER 0 | CHARACTER 1 | CHARACTER 2 | CHARACTER 3 | | OUTPUT BUFFER NO. 1 |
| | CHARACTER 0 | CHARACTER 1 | CHARACTER 2 | CHARACTER 3 | | OUTPUT BUFFER NO. 2 |
| | CHARACTER 0 | CHARACTER 1 | CHARACTER 2 | CHARACTER 3 | | |

Communications Line Control Packet Table

| PACKET 1st BYTE | | LCP | | PACKET 1st BYTE | | LCP | | PACKET 1st BYTE | | LCP | |
|------------------------|-----|------|-----|-----------------|------|------|-----|-----------------|------|------|-----|
| DEC | HEX | LINE | MIM | DEC | HEX | LINE | MIM | DEC | HEX | LINE | MIM |
| LCP FORMAT | | | | 2080 | 820 | 33 | 2 | 4576 | 11E0 | 79 | 4 |
| Input Active BCW | | | | 2112 | 840 | 34 | 2 | | | | |
| Input Standby BCW | | | | 2144 | 860 | 35 | 2 | 4608 | 1200 | 80 | 5 |
| Reserved (program use) | | | | 2176 | 880 | 36 | 2 | 4640 | 1220 | 81 | 5 |
| Reserved (program use) | | | | 2208 | 8A0 | 37 | 2 | 4672 | 1240 | 82 | 5 |
| Output Active BCW | | | | 2240 | 8C0 | 38 | 2 | 4704 | 1260 | 83 | 5 |
| Output Standby BCW | | | | 2272 | 8E0 | 39 | 2 | 4736 | 1280 | 84 | 5 |
| Reserved (program use) | | | | 2304 | 900 | 40 | 2 | 4768 | 12A0 | 85 | 5 |
| Reserved (program use) | | | | 2236 | 920 | 41 | 2 | 4800 | 12C0 | 86 | 5 |
| Reserved (program use) | | | | 2368 | 940 | 42 | 2 | 4832 | 12E0 | 87 | 5 |
| 1024 | 400 | 0 | 0 | 2400 | 960 | 43 | 2 | 4864 | 1300 | 88 | 5 |
| 1056 | 420 | 1 | 0 | 2432 | 980 | 44 | 2 | 4896 | 1320 | 89 | 5 |
| 1088 | 440 | 2 | 0 | 2464 | 9A0 | 45 | 2 | 4928 | 1340 | 90 | 5 |
| 1120 | 460 | 3 | 0 | 2496 | 9C0 | 46 | 2 | 4960 | 1360 | 91 | 5 |
| 1152 | 480 | 4 | 0 | 2528 | 9E0 | 47 | 2 | 4992 | 1380 | 92 | 5 |
| 1184 | 4A0 | 5 | 0 | 2560 | A00 | 48 | 3 | 5024 | 13A0 | 93 | 5 |
| 1216 | 4C0 | 6 | 0 | 2592 | A20 | 49 | 3 | 5056 | 13C0 | 94 | 5 |
| 1248 | 4E0 | 7 | 0 | 2624 | A40 | 50 | 3 | 5088 | 13E0 | 95 | 5 |
| 1280 | 500 | 8 | 0 | 2656 | A60 | 51 | 3 | 5120 | 1400 | 96 | 6 |
| 1312 | 520 | 9 | 0 | 2688 | A80 | 52 | 3 | 5152 | 1420 | 97 | 6 |
| 1344 | 540 | 10 | 0 | 2720 | AA0 | 53 | 3 | 5184 | 1440 | 98 | 6 |
| 1376 | 560 | 11 | 0 | 2752 | AC0 | 54 | 3 | 5216 | 1460 | 99 | 6 |
| 1408 | 580 | 12 | 0 | 2784 | AE0 | 55 | 3 | 5248 | 1480 | 100 | 6 |
| 1440 | 5A0 | 13 | 0 | 2816 | B00 | 56 | 3 | 5280 | 14A0 | 101 | 6 |
| 1472 | 5C0 | 14 | 0 | 2848 | B20 | 57 | 3 | 5312 | 14C0 | 102 | 6 |
| 1504 | 5E0 | 15 | 0 | 2880 | B40 | 58 | 3 | 5344 | 14E0 | 103 | 6 |
| | | | | 2912 | B60 | 59 | 3 | 5376 | 1500 | 104 | 6 |
| 1536 | 600 | 16 | 1 | 2944 | B80 | 60 | 3 | 5408 | 1520 | 105 | 6 |
| 1568 | 620 | 17 | 1 | 2976 | BA0 | 61 | 3 | 5440 | 1540 | 106 | 6 |
| 1600 | 640 | 18 | 1 | 3008 | BC0 | 62 | 3 | 5472 | 1560 | 107 | 6 |
| 1632 | 660 | 19 | 1 | 3040 | BE0 | 63 | 3 | 5504 | 1580 | 108 | 6 |
| 1664 | 680 | 20 | 1 | | | | | 5536 | 15A0 | 109 | 6 |
| 1696 | 6A0 | 21 | 1 | 4096 | 1000 | 64 | 4 | 5568 | 15C0 | 110 | 6 |
| 1728 | 6C0 | 22 | 1 | 4128 | 1020 | 65 | 4 | 5600 | 15E0 | 111 | 6 |
| 1760 | 6E0 | 23 | 1 | 4168 | 1040 | 66 | 4 | | | | |
| 1792 | 700 | 24 | 1 | 4192 | 1060 | 67 | 4 | 5632 | 1600 | 112 | 7 |
| 1824 | 720 | 25 | 1 | 4224 | 1080 | 68 | 4 | 5664 | 1620 | 113 | 7 |
| 1856 | 740 | 26 | 1 | 4256 | 10A0 | 69 | 4 | 5696 | 1640 | 114 | 7 |
| 1888 | 760 | 27 | 1 | 4292 | 10C0 | 70 | 4 | 5728 | 1660 | 115 | 7 |
| 1920 | 780 | 28 | 1 | 4324 | 10E0 | 71 | 4 | 5760 | 1680 | 116 | 7 |
| 1952 | 7A0 | 29 | 1 | 4356 | 1100 | 72 | 4 | 5792 | 16A0 | 117 | 7 |
| 1984 | 7C0 | 30 | 1 | 4392 | 1120 | 73 | 4 | 5824 | 16C0 | 118 | 7 |
| 2016 | 7E0 | 31 | 1 | 4424 | 1140 | 74 | 4 | 5856 | 16E0 | 119 | 7 |
| | | | | 4448 | 1160 | 75 | 4 | 5888 | 1700 | 120 | 7 |
| 2048 | 800 | 32 | 2 | 4480 | 1180 | 76 | 4 | 5920 | 1720 | 121 | 7 |
| | | | | 4512 | 11A0 | 77 | 4 | 5952 | 1740 | 122 | 7 |
| | | | | 4544 | 11C0 | 78 | 4 | 5984 | 1760 | 123 | 7 |
| | | | | | | | | 6016 | 1780 | 124 | 7 |
| | | | | | | | | 6048 | 17A0 | 125 | 7 |
| | | | | | | | | 6080 | 17C0 | 126 | 7 |
| | | | | | | | | 6112 | 17E0 | 127 | 7 |

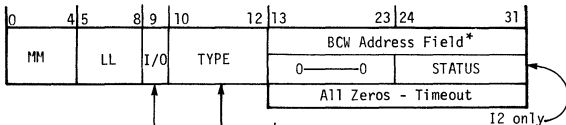
INTERRUPTS AND STATUS CODES

Three classes of Interrupts may occur: 1) Processor, 2) Channel 0,1 and 3) Channel 2-5.

Processor Interrupts

| TYPE | PRIORITY | OLD PSW BITS 16-31 | OLD PSW LOCATION (hex.) |
|--------------------------|----------|-----------------------|----------------------------|
| Machine Fault | | | 40-47 |
| CPU Parity | 1 | 0000 | |
| I/O Parity | 1 | 0001 | |
| Power-ON | 3 | 0004 | |
| Power-OFF | 3 | 0002 | |
| Program Error | | | 40-47 |
| Program Specification | 4 | 0006 | |
| Illegal OP Code | 4 | 0001 | |
| Memory size exceeded | 4 | 0004 | |
| Control timer | 4 | 0002 | |
| CHAN 0 Int Request | 5 | 0000 | 60-67 |
| CHAN 1 Int Request | 6 | 0000 | 60-67 |
| CHAN 2-5 Int Request | 7 | 0000 | 60-67 |
| Supervisor Call or Timer | | | 60-67 |
| SVC | 2 | 00NN* | |
| Timer | 3 | 0100 | |
| *NN = SVC I1 field | | | |

CHANNEL 2-5, E, and F INTERRUPT FORMATS and MIM STATUS



MM = 0-7₁₆-MIM NO.
 MM = 1C₁₆- Cassette
 MM = 1E₁₆- Console

LL = Line No.

I = Output
 0 = Input

- 000 Timeout (Firmware-generated)**
- 001 I2 (status)
- 010 D (Buffer expiration)
- 011 I1 (Control Code detected. Stored in Input Buffer)
- 100 Simultaneous I1 and D (I1D)
- 101 BID (Branch-control-code detected. Standby BCW to working location with K=1)

* address of last character stored.

** Does not appear in interrupt table.

NOTE: I2 with Bit 9=1 and Bits 13-31 all zeros = Output Completion

Comm-Channel Interrupt Trace Table

LL - System line number if line is at priority 2 or 3.
 System line number shifted right 1 bit if line is at priority 1.

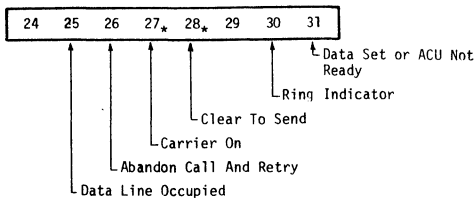
SS - Status byte from MIM or cassette.

AAAA - Ending buffer address.

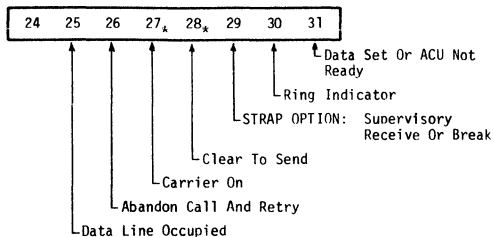
Format in Bits

| | | | | | | | | | |
|------|------|-------|-----|------|------|------|------|--------|-------------------|
| LLLL | LLLL | L0001 | 000 | 0000 | 0000 | SSSS | SSSS | Input | I2 |
| LLLL | LLLL | L0010 | AAA | AAAA | AAAA | AAAA | AAAA | Input | buffer expiration |
| LLLL | LLLL | L0011 | AAA | AAAA | AAAA | AAAA | AAAA | Input | I1 |
| LLLL | LLLL | L0100 | AAA | AAAA | AAAA | AAAA | AAAA | Input | I1D |
| LLLL | LLLL | L0101 | AAA | AAAA | AAAA | AAAA | AAAA | Input | BID |
| LLLL | LLLL | L1001 | 000 | 0000 | 0000 | 0000 | 0000 | Output | I2 |
| LLLL | LLLL | L1010 | AAA | AAAA | AAAA | AAAA | AAAA | Output | buffer expiration |

4 Line ADS-MIM STATUS

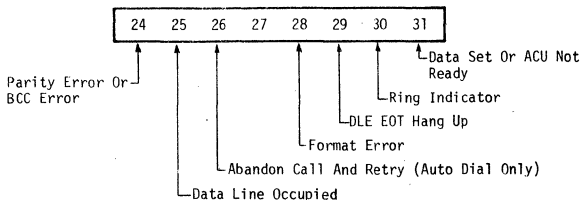


4 Line ADA-MIM STATUS



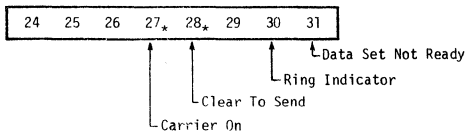
* must be probed but will accompany unsolicited status.

4 Line BSC-MIM STATUS



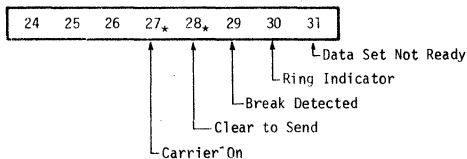
NOTE: No status bits present on end of input (BCC check) implies no error.

4 Line S-MIM STATUS



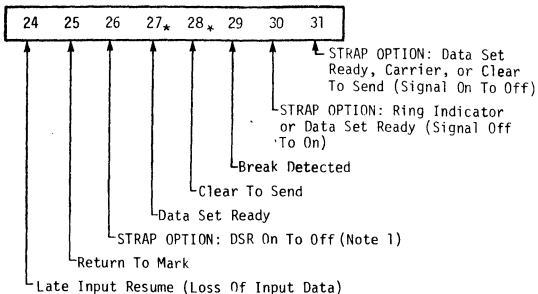
NOTE: No status bits present implies end of output, no error.

4 Line ECA-MIM STATUS



* must be probed but will accompany unsolicited status.

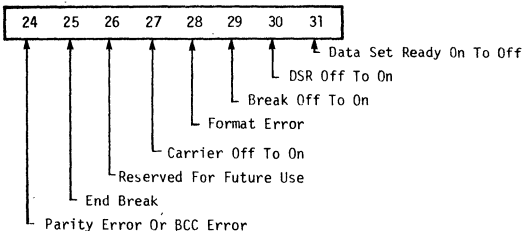
16-LINE, A-MIM STATUS (Normal Status) See page 33 for Instant Status (T2016-02)



* Does not generate interrupt and cannot be probed. They will accompany an unsolicited status.

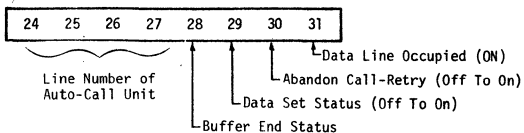
Note 1: Strap Option: Hi Suprec, Lo Suprec, RI, DSR, CTS, CO. Foiled to DSR (T2016-02)

*16-LINE, BSC-MIM STATUS (Normal Status) See page 33 for Instant Status

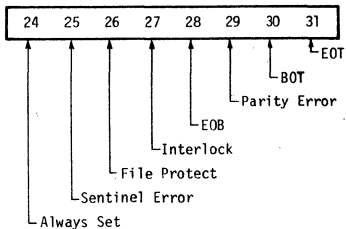


* Status byte of all zeros means CRC is ok.

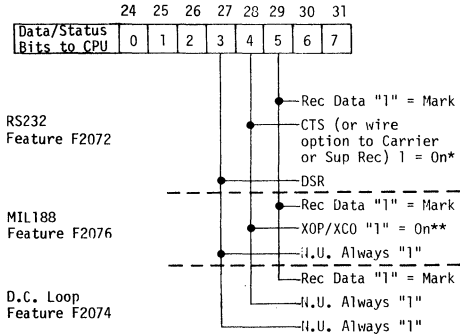
AUTOCALL ADAPTER STATUS



PROGRAM LOAD DEVICE (CASSETTE) STATUS

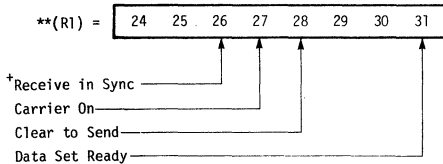


T2016-02 INSTANT STATUS
(16-line A-MIM)



- * foiled to strap option CTS
- ** foiled to be off all the time. Foil cut & strap addition will connect to XOP/XCO signal

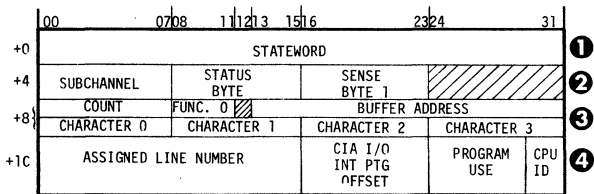
T2018 INSTANT STATUS
(16-Line BSC-MIM)



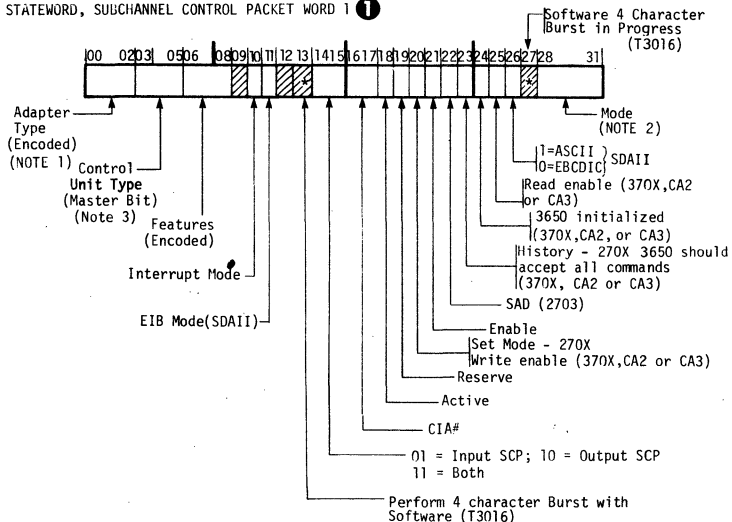
+ "Receive In Sync" is an Internal Logic Signal

CHANNEL 0 OR 1 HARDWARE FORMATS for T3019

Multiplexer Subchannel Control Packet Format



STATEWORD, SUBCHANNEL CONTROL PACKET WORD 1 ①



*Bit 13 must be set before Firmware will use bit 27. (T3016 only)
 Bit 13 not used by T3018 and T3019.

NOTE 1: Adapter Field tells which Emulator according to the following:

FULL EMULATOR LIST

| EMULATOR | CODE |
|----------|------|
| SDAI | 000 |
| SDAII | 001 |
| TGHI | 010 |
| TGHII | 011 |
| TAI | 100 |
| TAII | 101 |
| TAIII | 110 |
| WTTY | 111 |

If the list is partial the list compresses always with the Emulators in the same sequence such as:

EXAMPLE 1

| EMULATOR | CODE |
|----------|------|
| SDAII | 000 |
| TGHI | 001 |
| TAII | 010 |

EXAMPLE 2

| EMULATOR | CODE |
|----------|------|
| SDAI | 000 |
| SDAII | 001 |
| TAI | 010 |
| TAII | 011 |
| WTTY | 100 |

NOTE 2: SDAII Code Detection Effect on Stateword bits:

Bit 23 - Set by firmware if bit 30 set and DLE Stop received.

Bit 28 - Set if bit 23 set and Write Command received.

Bit 30 - Sets on DLE STX.

Bit 31 - Sets on DLE, Clears on next character.

Bit 28 & 30 - Both clear if bit 28 set and (1) LXI or DLE ITB or DLE ENQ or DLE ITB detected.

NOTE 3:

Bit 3 - 2701

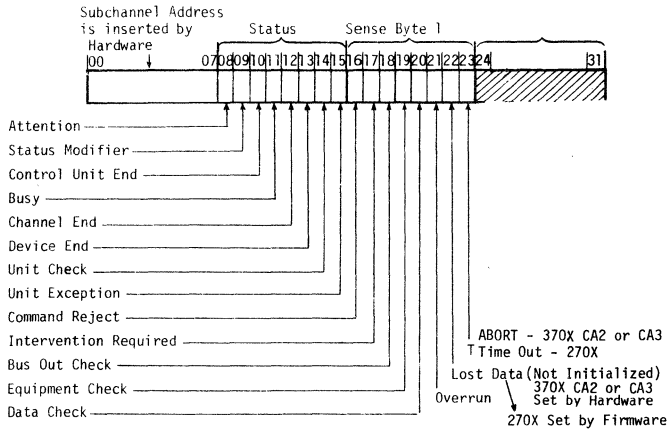
Bit 4 - 370X channel adapter type 2 or type 3

Bit 5 - 2703

TERMINAL ADAPTER

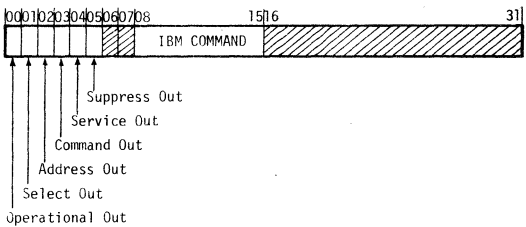
| | |
|--------|------------------------------------------------------|
| TA I | 2740; 2740-II; 2741; 1050; 1060; 1070 |
| TA II | 1030, 1032 |
| TA III | 2260; 2265 |
| TGH I | TTY 28; TTY 32 |
| TGH II | TTY 33; TTY 35; TTY 38 |
| SDA I | (STR); 1009; 1013; 7701; 7702; 7710; 7711; 7740; 360 |
| SDA II | (BSC); 2780; 1130; REMOTE 360 |

STATUS/SENSE, SUBCHANNEL CONTROL PACKET WORD 2 **2**



SUBCHANNEL CONTROL PACKET WORD 3: BCW Mode = BCW; Direct Transfer Mode = Data **3**

TESTWORD, SUBCHANNEL CONTROL PACKET WORD 4 **4**



360/370 SCAN FAR COMMANDS

| | INITIATED BY | SI/O FUNCTION | ACTION |
|----------------------------------------------------------------|--------------|------------------|--------------|
| 0 - Idle | | | NO |
| 1 - Stacked Special Status Pending | 360/370 | | YES |
| 2 - Input/Write | 360/370 | | NO |
| 3 - Output/Read | 360/370 | | NO |
| 4 - Direct Input | COMTEN | 04 | YES |
| 5 - Direct Output | COMTEN | 05 | YES |
| 6 - BCW Input | COMTEN | 06 | YES |
| 7 - BCW Output | COMTEN | 07 | YES |
| 8 - Normal Status | COMTEN | 08 | YES |
| 9 - Stacked Status | | | YES |
| A - Special Status | COMTEN | 18 | YES |
| B - Stacked Special Status | 360/370 | | YES |
| C - Command Request (Test Command) | COMTEN | 80 | YES-OFF LINE |
| D - Not Used | | | NO |
| E - Not Used | | | NO |
| F - IBM Disconnect (Selective Reset For A Given Subchannel) | 360/370 | | NO |

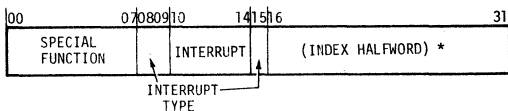
FUNCTIONS FOR CIA . ATTACHED TO BASE INTERFACE

| HEX CODE | FUNCTION |
|----------|--------------------------------------------|
| 04 | Direct-Input Data Transfer (IBM Write) |
| 05 | Direct-Output Data Transfer (IBM Read) |
| 06 | BCW-Input Data Transfer (IBM Write) |
| 07 | BCW-Output Data Transfer (IBM Read) |
| 08 | Status Transfer Request |
| 18 | Queue Special Status Transfer Request |
| 20 | Clear Reset/Disconnect |
| 28 | Clear Reset/Disconnect and Transfer Status |
| 40 | Prepare to Go Off-Line |
| 50 | Go Off-Line |
| 70 | Go On-Line |
| 80 | Command Test Sequence |
| 84-87 | Data Transfer Tests |
| 88 | Status Transfer Test |

CHANNEL 0 OR 1 INTERRUPTS

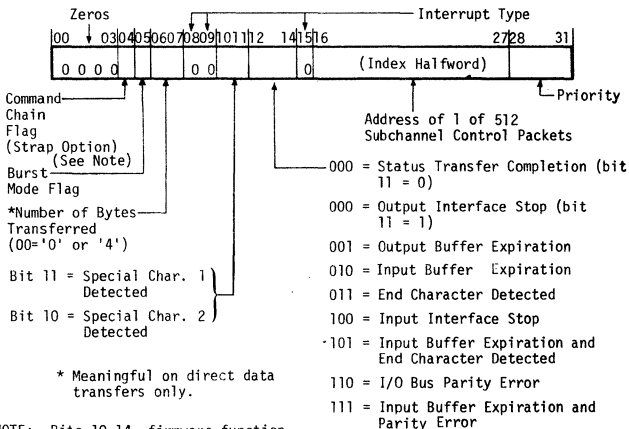
Channel 0 or 1 have Interrupt Types identified by bits 8,9 and 15 of the Interrupt Word. These seven types(000-110) originate from CIA; and appear in various formats. The basic interrupt format appears below. All channel 0 or 1 formats are variations of this.

■ Basic Format



*bits 16-27 = Control Packet Address, bits 28-31 = firmware priority

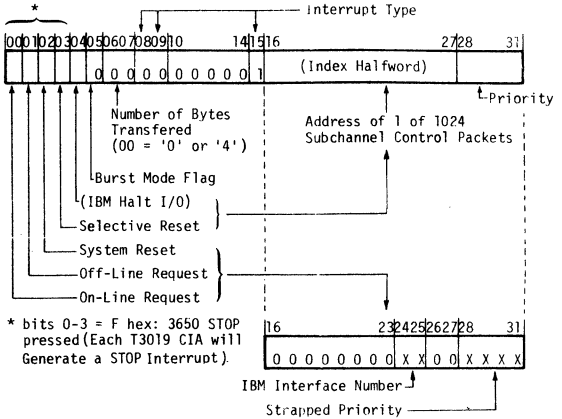
■ Interrupt Type: 000, Normal Status/Data Completion



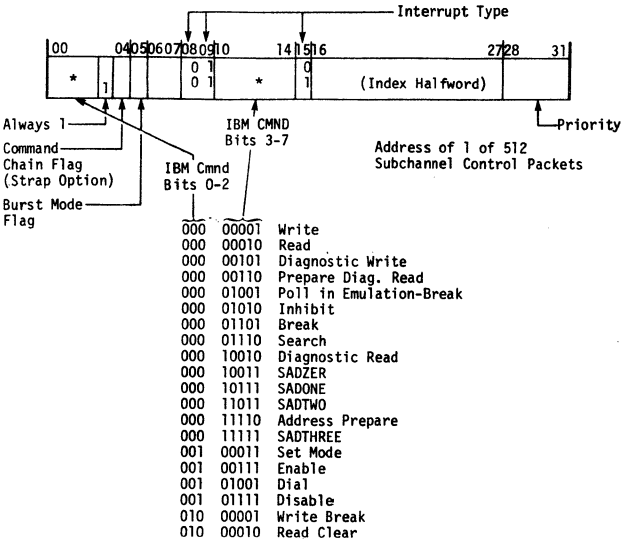
* Meaningful on direct data transfers only.

NOTE: Bits 10-14, firmware function
 1 = Command Chaining
 0 = No Command Chaining

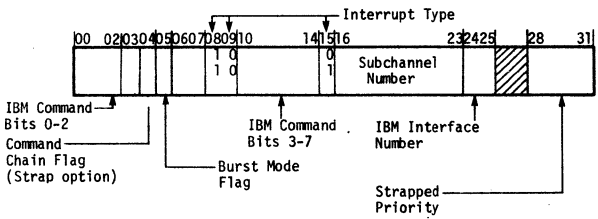
■ Interrupt Type: 001, Special Interrupt



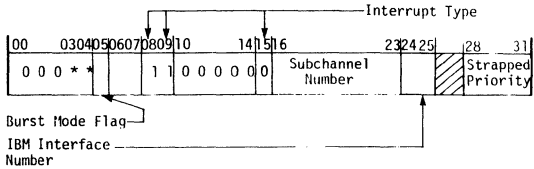
- Interrupt Types: 010, Normal Command
- 011, Stacked Command



- Interrupt Types: 100, Reserved Subchannel Command
- 101, Reserved Subchannel Stacked Command



■ Interrupt Type: 110, Special Status Completion



* Can also indicate Selective Reset or Disconnect received during transfer of Special Status, Command to reserved subchannel, i.e. bit 3 or 4 = 1.

INTERRUPT TABLE FORMATS

HARDWARE COMMAND INTERRUPTS

| | |
|----------|--------------------------------------------------------|
| 1Y42XXXX | Write |
| 1Y44XXXX | Read |
| 1Y4AXXXX | Diag. Write in Emulation-Write IPL Write IPL to NCP |
| 1Y4CXXXX | Prepare-Diag Read for TAI11 2701 |
| 1Y52XXXX | Poll in Emulation-Write Break for NCP |
| 1Y54XXXX | Inhibit |
| 1Y5AXXXX | Break |
| 1Y5CXXXX | Search |
| 1Y64XXXX | Diag Read |
| 1Y66XXXX | SADZER |
| 1Y6EXXXX | SADONE |
| 1Y76XXXX | SADTWO |
| 1Y7CXXXX | Address Prepare |
| 1Y7EXXXX | SADTHREE |
| 3Y46XXXX | Set Mode |
| 3Y4EXXXX | Enable |
| 3Y52XXXX | Dial |
| 3Y5EXXXX | Disable |
| 5Y42XXXX | Write Break |
| 5Y44XXXX | Read Clear |

XXXX - SCP Address
 Y - 8 = Command chain
 - 4 = Burst mode
 K - Count plus Y
 P - Interface number & priority

TERMINATION INTERRUPTS

| | |
|----------|-----------------------------------------------------|
| 0Y00XXXX | Status Transfer Complete |
| 0K10XXXX | Output Interface Stop |
| 0K02XXXX | Output Buffer Expiration |
| 0Y04XXXX | Input Buffer Expiration |
| 0K06XXXX | End Char Detected |
| 0K08XXXX | Input Interface Stop |
| 0Y0AXXXX | Input Buffer Expiration and End Char Detected |
| 0K0CXXXX | I/O Bus Parity Error |
| 0Y0EXXXX | I/O Bus Parity Error and Input Buffer Expiration |

FIRMWARE CONVERTED COMMAND INTERRUPTS**

| | |
|----------|-------------|
| 0040XXXX | Write |
| 0042XXXX | Read |
| 0044XXXX | D Write |
| 0046XXXX | Prepare |
| 0048XXXX | Enable |
| 004AXXXX | Disable |
| 004CXXXX | Inhibit |
| 004EXXXX | D Read |
| 0050XXXX | Poll |
| 0052XXXX | Break |
| 0054XXXX | Dial |
| 0056XXXX | Search |
| 0058XXXX | Add Prepare |
| 005AXXXX | Set Mode |

SPECIAL INTERRUPTS

| | |
|----------|-----------------|
| 0Y41XXXX | Stacked Status |
| 0801XXXX | IBM Halt I/O |
| 1001XXXX | Selective Reset |
| 2001000P | System Reset |
| 4001000P | Go Off-Line |
| 8001000P | Go On-Line |
| F001000P | 3650 Stop* |

FIRMWARE INTERRUPTS

| | |
|----------|----------------|
| 00400000 | Output Timeout |
| 00000000 | Input Timeout |

- * Each T3019 CIA will generate a STOP Interrupt.
 ** These Interrupts will be seen in the Interrupt Trace Table

•360/370 CHANNEL COMMANDS DECODED BY TERMINAL ADAPTER EMULATORS•

| COMMAND | COMMAND CODE (HEX) | TA I | | TA II | | TA III | | WTTA | | TGH I | | TGH II | | SDA II | | NCP |
|------------------|--------------------|------|------|-------|------|--------|------|------|------|-------|------|--------|------|--------|------|-----|
| | | 2701 | 2703 | 2701 | 2703 | 2701 | 2703 | 2701 | 2703 | 2701 | 2703 | 2701 | 2703 | 2701 | 2703 | CA2 |
| ENABLE | 27 | X | X | X | X | - | - | X | X | X | X | X | X | X | X | - |
| DISABLE | 2F | X | X | X | X | - | - | X | X | X | X | X | X | X | X | - |
| READ | 02 | X | X | X | X | X | - | X | X | X | X | X | X | X | X | X |
| WRITE | 01 | X | X | X | X | X | - | X | X | X | X | X | X | X | X | X |
| POLL | 09 | - | X | - | X | - | - | X | - | - | - | - | - | X | X | - |
| INHIBIT | 0A | X | X | X | X | - | - | X | X | X | X | X | X | - | - | - |
| PREPARE | 06 | X | X | X | X | - | - | X | X | X | X | X | X | X | X | - |
| SEARCH | 0E | - | - | - | - | - | - | ** | - | X | X | - | - | X | X | - |
| BREAK | 0D | - | X | - | - | - | - | X | X | X | X | X | X | - | - | - |
| DIAL | 29 | * | * | - | - | - | - | - | - | - | - | * | * | * | * | - |
| WRITE BREAK | 41 | - | - | - | - | X | - | - | - | - | - | - | - | - | - | - |
| READ CLEAR | 42 | - | - | - | - | X | - | - | - | - | - | - | - | - | - | - |
| SET MODE | 23 | - | - | - | - | - | - | - | - | - | - | - | - | X | X | - |
| ADDRESS PREPARE | 1E | - | - | - | - | - | - | - | - | - | - | - | - | X | X | - |
| DIAGNOSTIC READ | 06 | - | - | - | - | X | - | - | - | - | - | - | - | - | - | - |
| DIAGNOSTIC READ | 12 | X | - | X | - | - | - | X | - | X | - | X | - | - | - | - |
| DIAGNOSTIC WRITE | 05 | X | - | X | - | X | - | X | - | X | - | X | - | - | - | - |
| SADZER | 13 | - | *** | - | *** | - | - | - | *** | - | *** | - | *** | - | - | - |
| SADONE | 17 | - | *** | - | *** | - | - | - | *** | - | *** | - | *** | - | - | - |
| SADTWO | 1B | - | *** | - | *** | - | - | - | *** | - | *** | - | *** | - | - | - |
| SADTHREE | 1F | - | *** | - | *** | - | - | - | *** | - | *** | - | *** | - | - | - |
| WRITE IPL | 05 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | X |
| WRITE BREAK | 09 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | X |

* - REQUIRES DIALING EQUIPMENT

** - EXECUTED AS A READ

*** - EXECUTED AS AN I/O NOOP

•360/370 CHANNEL COMMANDS COMMON TO ALL EMULATORS•

(IMMEDIATE COMMANDS)

| COMMAND | COMMAND CODE (HEX) | 2701 | 2703 | CA2 |
|-----------|--------------------|------|------|-----|
| I/O NO-OP | 03 | X | X | X |
| TEST I/O | 00 | X | X | X |
| SENSE | 04 | X | X | X |
| RESERVE | F4 | - | X | - |
| RELEASE | D4 | - | X | - |

CONTROL CODE DETECT STRAPPING

| EMULATOR | CHANNEL 2-D | | | CHANNEL 0 | |
|-----------------------------------------------------------|-------------|--------|-----------|-----------|---------------|
| | CODE | HEX | INTERRUPT | CODE | INTERRUPT |
| TA I, TA II 2740,2741,1050, 1060,1070,1030, 1032 | NAK | 01 | 11 | 3D | End Character |
| | ACK | 37 | 11 | | |
| | EOB | 5E | B1D | | |
| | EOA | 34 | 11 | | |
| | EOT | 7C | 11 | | |
| TA III 2260, 2265 | ETX | 03 | B1D | 03 | End Character |
| | EOT | 84 | 11 | | |
| | ACK | 06 | 11 | | |
| | NAK | 95 | 11 | | |
| TGH I TTY 28, TTY 32 | ACK | 1E | 11 | | None |
| | EOA | 1C | 11 | | |
| | EOT | 14 | B1D | | |
| TGH II TTY 33, TTY 35, TTY 38 | WRU | 05 | B1D | | None |
| | WRU | 85 | B1D | | |
| | XON | 11 | B1D | | |
| | XON | 91 | B1D | | |
| | XOFF | 93 | B1D | | |
| | EOT | 84 | B1D | | |
| | ACK | 06 | B1D | | |
| | ACK | 86 | B1D | | |
| SDA II 2780,BSC, 1130, Remote 360 | EBCDIC | EBCDIC | | EBCDIC | |
| | SOH | 01 | 11 | 26 | End Character |
| | STX | 02 | 11 | 03 | End Character |
| | ETB | 26 | 11 | 1F | End Character |
| | ETX | 03 | 11 | 2D | End Character |

CONTROL CODE-DETECT STRAPPING, CONT'D

| EMULATOR | CHANNEL 2-D | | | CHANNEL 0 | |
|-------------------------------------------|-------------|-----|-----------|---------------|---------------|
| | CODE | HEX | INTERRUPT | CODE | INTERRUPT |
| SDA II 2780,BSC, 1130,Remote 360 | EOT | 37 | 11 | 1026 | End Character |
| | ENQ | 2D | 11 | 1003 | End Character |
| | NAK | 3D | 11 | 101F | End Character |
| | ITB | 1F | 11 | 102D | End Character |
| | ACK 0 | 70* | 11 | | |
| | ACK 1 | 61* | 11 | | |
| | WACK | 6B* | 11 | | |
| | RVI | 7C* | 11 | | |
| | WABT | 7F* | 11 | | |
| | ASCII | | | | |
| | SOH | 01 | 11 | 17 | End Character |
| | STX | 02 | 11 | 03 | End Character |
| | ETB | 17 | 11 | 1F | End Character |
| | ETX | 03 | 11 | 05 | End Character |
| EOT | 04 | 11 | 1017 | End Character | |
| ENQ | 05 | 11 | 1003 | End Character | |
| NAK | 15 | 11 | 101F | End Character | |
| ITB | 1F | 11 | 1005 | End Character | |
| ACK 0 | 30 | 11 | | | |
| ACK 1 | 31 | 11 | | | |
| WACK | 3B | 11 | | | |
| RVI | 3C | 11 | | | |
| WABT | 3F | 11 | | | |

* These codes are detected only when preceded by a DLE ('10')

CODE CHARTS

CODE CHART: TA I AND TA II (EBCD)

| SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR |
|-----------|----------|-----------|-----------|----------|-----------|-----------|----------|-----------|
| 00 | 00 | | 2C | 1A | : | 58 | 0D | '6 |
| 01 | 40 | - | 2D | 5A | | 59 | 4D | |
| 02 | 20 | @ | 2E | 3A | | 5D | 2D | |
| 03 | 60 | | 2F | 7A | HT | 5B | 6D | F |
| 04 | 10 | *8 | 30 | 06 | | 5C | 1D | |
| 05 | 50 | | 31 | 46 | L | 5D | 5D | BS |
| 06 | 30 | | 32 | 26 | T | 5E | 3D | EOB |
| 07 | 70 | H | 33 | 66 | | 5F | 7D | |
| 08 | 08 | :4 | 34 | 16 | # " | 60 | 03 | |
| 09 | 48 | | 35 | 56 | | 61 | 43 | J |
| 0A | 28 | | 36 | 36 | | 62 | 23 | ?/ |
| 0B | 68 | D | 37 | 76 | ┌ | 63 | 63 | |
| 0C | 18 | | 38 | 0E | >7 | 64 | 13 | (9 |
| 0D | 58 | * | 39 | 4E | | 65 | 53 | |
| 0E | 38 | | 3A | 2E | , | 66 | 33 | |
| 0F | 78 | | 3B | 6E | G | 67 | 73 | i |
| 10 | 04 | <2 | 3C | 1E | | 68 | 0B | %5 |
| 11 | 44 | | 3D | 5E | IDLE | 69 | 4B | |
| 12 | 24 | | 3E | 3E | | 6A | 2B | |
| 13 | 64 | B | 3F | 7E | | 6B | 6B | E |
| 14 | 14 | | 40 | 01 | SP | 6C | 1B | |
| 15 | 54 | | 41 | 41 | | 6D | 5B | NL |
| 16 | 34 | | 42 | 21 | | 6E | 3B | LF |
| 17 | 74 | | 43 | 61 | + & | 6F | 7B | |
| 18 | 0C | | 44 | 11 | | 70 | 07 | ;3 |
| 19 | 4C | O | 45 | 51 | Q | 71 | 47 | |
| 1A | 2C | W | 46 | 31 | Y | 72 | 27 | |
| 1B | 6C | | 47 | 71 | | 73 | 67 | C |
| 1C | 1C | >us | 48 | 09 | | 74 | 17 | |
| 1D | 5C | | 49 | 49 | M | 75 | 57 | !\$ |
| 1E | 3C | | 4A | 29 | U | 76 | 37 | , |
| 1F | 7C | DS | 4B | 69 | | 77 | 77 | |
| 20 | 02 | =1 | 4C | 19 | @ | 78 | 0F | |
| 21 | 42 | | 4D | 59 | | 79 | 4F | P |
| 22 | 22 | | 4E | 39 | | 7A | 2F | X |
| 23 | 62 | A | 4F | 79 | SUBT | 7B | 6F | EOT |
| 24 | 12 | | 50 | 05 | | 7C | 1F | |
| 25 | 52 | R | 51 | 45 | K | 7D | 5F | |
| 26 | 32 | Z | 52 | 25 | S | 7E | 3F | |
| 27 | 72 | | 53 | 65 | | 7F | 7F | DEL |
| 28 | 0A | | 54 | 15 |) Ø | | | |
| 29 | 4A | N | 55 | 55 | | | | |
| 2A | 2A | V | 56 | 35 | | | | |
| 2B | 6A | | 57 | 75 | RESTORE | | | |

NOTES:

- 1) When 2 characters are shown, the first is for upper case and the second is for lower case.
- 2) All hex is shown lower case. Upper case characters will have the most significant bit (BIT Ø) in SCP packet.

CODE CHART. TA III (ASCII)

| SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR |
|-----------|----------|-----------|-----------|----------|-----------|-----------|----------|-----------|
| 00 | 00 | | AC | 4C | - | D8 | B8 | X |
| 81 | 01 | SOH | 2D | 4D | - | 59 | B9 | Y |
| 82 | 02 | STX | 2E | 4E | . | 5A | BA | Z |
| 03 | 03 | ETX | AF | 4F | / | DB | BB | |
| 84 | 04 | EOT | 30 | 50 | Ø | 5C | BC | |
| 05 | 05 | | B1 | 51 | 1 | DD | BD | |
| 06 | 06 | ACK | B2 | 52 | 2 | DE | BE | |
| 87 | 07 | | 33 | 53 | 3 | 5F | BF | - |
| 88 | 08 | | B4 | 54 | 4 | 60 | E0 | @ |
| 09 | 09 | | 35 | 55 | 5 | E1 | E1 | a |
| 0A | 0A | LF | 36 | 56 | 6 | E2 | E2 | b |
| 88 | 0B | | B7 | 57 | 7 | 63 | E3 | c |
| 0C | 0C | | B8 | 58 | 8 | E4 | E4 | d |
| 8D | 0D | | 39 | 59 | 9 | 65 | E5 | e |
| 8E | 0E | | 3A | 5A | : | 66 | E6 | f |
| 0F | 0F | | BB | 5B | ; | E7 | E7 | g |
| 90 | 10 | | 3C | 5C | < | E8 | E8 | h |
| 11 | 11 | | BD | 5D | = | 69 | E9 | i |
| 12 | 12 | | BE | 5E | > | 6A | EA | j |
| 93 | 13 | | 3F | 5F | ? | EB | EB | k |
| 14 | 14 | | C0 | A0 | | 6C | EC | l |
| 95 | 15 | NAK | 41 | A1 | A | ED | ED | m |
| 96 | 16 | | 42 | A2 | B | EE | EE | n |
| 17 | 17 | | C3 | A3 | C | 6F | EF | o |
| 18 | 18 | CAN | 44 | A4 | D | F0 | F0 | p |
| 99 | 19 | | C5 | A5 | E | 71 | F1 | q |
| 9A | 1A | | C6 | A6 | F | 72 | F2 | r |
| 1B | 1B | | 47 | A7 | G | F3 | F3 | s |
| 9C | 1C | | 48 | A8 | H | 74 | F4 | t |
| 1D | 1D | | C9 | A9 | I | F5 | F5 | u |
| 1E | 1E | | CA | AA | J | F6 | F6 | v |
| 9F | 1F | | 4B | AB | K | 77 | F7 | w |
| A0 | 40 | SP | CC | AC | L | 78 | F8 | x |
| 21 | 41 | | 4D | AD | M | F9 | F9 | y |
| 22 | 42 | | 4E | AE | N | FA | FA | z |
| A3 | 43 | # | CF | AF | O | 7B | FB | |
| 24 | 44 | \$ | 50 | B0 | P | FC | FC | ~ |
| A5 | 45 | % | D1 | B1 | Q | 7D | FD | |
| A6 | 46 | & | D2 | B2 | R | 7E | FE | |
| 27 | 47 | ' | 53 | B3 | S | FF | FF | |
| 28 | 48 | (| D4 | B4 | T | | | |
| A9 | 49 |) | 55 | B5 | U | | | |
| AA | 4A | * | 56 | B6 | V | | | |
| 2B | 4B | + | D7 | B7 | W | | | |

NOTE: The lower case alphabetic characters are converted to upper case by the 2848. On a read operation, lower case characters will be transmitted and stored in upper case bit configuration.

CODE CHART: TGH I (BAUDOT)

| SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR |
|--------------|-------------|--------------|--------------|-------------|--------------|--------------|-------------|--------------|
| 00 | 00 | BLANK | 16 | 0D | P | 2C | 26 | ,7/8 |
| 01 | 10 | E | 17 | 1D | Q | 2D | 36 | :1/4 |
| 02 | 08 | LF | 18 | 03 | O | 2E | 2E | :1/8 |
| 03 | 18 | A | 19 | 13 | B | 2F | 3E | (1/2 |
| 04 | 04 | SP | 1A | 0B | G | 30 | 21 | 5 |
| 05 | 14 | S | 1B | 1B | FIGS | 31 | 31 | " |
| 06 | 0C | I | 1C | 07 | M | 32 | 29 |)3/4 |
| 07 | 1C | U | 1D | 17 | X | 33 | 39 | 2 |
| 08 | 02 | CR | 1E | 0F | V | 34 | 25 | #() |
| 09 | 12 | D | 1F | 1F | LTRS | 35 | 35 | 6 |
| 0A | 0A | R | 20 | 20 | BLANK | 36 | 2D | Ø |
| 0B | 1A | J | 21 | 30 | 3 | 37 | 3D | 1 |
| 0C | 06 | N | 22 | 28 | LF | 38 | 23 | 9 |
| 0D | 16 | F | 23 | 38 | - | 39 | 33 | ?5/8 |
| 0E | 0E | C | 24 | 24 | SP | 3A | 2B | & |
| 0F | 1E | K | 25 | 34 | ' | 3B | 3B | FIGS |
| 10 | 01 | T | 26 | 2C | 8 | 3C | 27 | . |
| 11 | 11 | Z | 27 | 3C | 7 | 3D | 37 | / |
| 12 | 09 | L | 28 | 22 | CR | 3E | 2F | ;3/8 |
| 13 | 19 | W | 29 | 32 | WRU | 3F | 3F | LTRS |
| 14 | 05 | H | 2A | 2A | 4 | | | |
| 15 | 15 | Y | 2B | 3A | BELL | | | |

NOTE: When two characters are shown, the first is for BAUDOT Arrangement and second for Arrangement C.

CODE CHART: TGH II (TWX)

| SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR | SLCP HEX. | SCP HEX. | CODE CHAR |
|-----------|----------|-----------|-----------|----------|-----------|-----------|-----------|-----------|
| *80 | 01 | NULL | A3 | C5 | # | C6 | 63 | F |
| 81 | 81 | SOM | *A4 | 25 | \$ | *C7 | E3 | G |
| 82 | 41 | EOA | A5 | A5 | % | *C8 | 13 | H |
| *83 | C1 | EOM | A6 | 65 | & | C9 | 93 | I |
| 84 | 21 | EOT | *A7 | E5 | , | CA | 53 | J |
| *85 | A1 | WRU | A8 | 15 | (| *CB | D3 | K |
| *86 | 61 | ACK | A9 | 95 |) | CC | 33 | L |
| 87 | E1 | BELL | AA | 55 | * | *CD | B3 | M |
| 88 | 11 | | *AB | D5 | + | *CE | 73 | N |
| *89 | 91 | HT | AC | 35 | - | CF | F3 | O |
| *8A | 51 | LF | *AD | B5 | . | *DO | 0B | P |
| 8B | D1 | VT | *AE | 75 | / | D1 | 8B | Q |
| *8C | 31 | FF | AF | F5 | / | D2 | 4B | R |
| 8D | B1 | CR | *B0 | 0D | Ø | *D3 | CB | S |
| 8E | 71 | SO | B1 | 8D | 1 | D4 | 2B | T |
| *8F | F1 | SI | B2 | 4D | 2 | *D5 | AB | U |
| 90 | 09 | | *B3 | CD | 3 | *D6 | 6B | V |
| *91 | 89 | X-ON | B4 | 2D | 4 | D7 | EB | W |
| 92 | 49 | | *B5 | AD | 5 | D8 | 1B | X |
| 93 | C9 | X-OFF | *B6 | 6D | 6 | *D9 | 9B | Y |
| 94 | 29 | | B7 | ED | 7 | *DA | 5B | Z |
| 95 | A9 | | B8 | 1D | 8 | DB | DB | [|
| 96 | 69 | | *B9 | 9D | 9 | *DC | 3B | \ |
| 97 | E9 | | *BA | 5D | : | DD | BB |] |
| 98 | 19 | | BB | DD | ; | DE | 7B | + |
| 99 | 99 | | *BC | 3D | < | *DF | FB | + |
| 9A | 59 | | BD | BD | = | <u>EO</u> | <u>07</u> | UNUSED |
| 9B | D9 | | BE | 7D | > | ~ | ~ | |
| 9C | 39 | | *BF | FD | ? | FA | 5F | PAD |
| 9D | B9 | | C0 | 03 | @ | FB | DF | |
| 9E | 79 | | *C1 | 83 | A | FC | 3F | |
| 9F | F9 | | *C2 | 43 | B | | | |
| A0 | 05 | SP | C3 | C3 | C | FD | BF | DELETE |
| *A1 | 85 | : | *C4 | 23 | D | FE | 7F | |
| *A2 | 45 | " | C5 | A3 | E | FF | FF | |

- NOTES: 1) Bit configurations shown are due to the parity bit being held in mark-hold state.
- 2) When the parity bit is not held in mark-hold, the most significant bit in the SLCP and the least significant bit in the SCP will be a zero for asterisked (*) codes, i.e., (The CHAR A will be '41' in the SLCP and 82 in the SCP when not in mark-hold state).

CODE CHART: SDA II

| HEX. | ASCII | EBCDIC | HEX. | ASCII | EBCDIC | HEX. | ASCII | EBCDIC |
|------|-------|---------|------|-------|--------|------|-------|--------|
| 00 | NUL | NUL | 30 | Ø | | 60 | \ | - |
| 01 | SOH | SOH | 31 | 1 | | 61 | a | / |
| 02 | STX | STX | 32 | 2 | SYN | 62 | b | |
| 03 | ETX | ETX | 33 | 3 | | 63 | c | |
| 04 | EOT | PF | 34 | 4 | PN | 64 | d | |
| 05 | ENQ | HT | 35 | 5 | RS | 65 | e | |
| 06 | ACK | LC | 36 | 6 | UC | 66 | f | |
| 07 | BEL | DEL | 37 | 7 | EOT | 67 | g | |
| 08 | BS | | 38 | 8 | | 68 | h | |
| 09 | HT | | 39 | 9 | | 69 | i | |
| 0A | LF | SMM | 3A | : | | 6A | j | : |
| 0B | VT | VT | 3B | ; | CU3 | 6B | k | , |
| 0C | FF | FF | 3C | < | DC4 | 6C | l | % |
| 0D | CR | CR | 3D | = | NAK | 6D | m | — |
| 0E | SO | SO | 3E | > | | 6E | n | > |
| 0F | SI | SI | 3F | ? | SUB | 6F | o | ?> |
| 10 | DLE | DLE | 40 | @ | SP | 70 | p | |
| 11 | DCL | DCI | 41 | A | | 71 | q | |
| 12 | DC2 | DC2 | 42 | B | | 72 | r | |
| 13 | DC3 | DC3 | 43 | C | | 73 | s | |
| 14 | DC4 | RES | 44 | D | | 74 | t | |
| 15 | NAK | NL | 45 | E | | 75 | u | |
| 16 | SYN | BS | 46 | F | | 76 | v | |
| 17 | ETB | IL | 47 | G | | 77 | w | |
| 18 | CAN | CAN | 48 | H | | 78 | x | |
| 19 | EM | EM | 49 | I | | 79 | y | . |
| 1A | SUB | CC | 4A | J | ¢ | 7A | z | : |
| 1B | ESC | CUI | 4B | K | < | 7B | { | # |
| 1C | FS | IFS | 4C | L | (| 7C | | |
| 1D | GS | IGS | 4D | M |) | 7D | ~ | ^ |
| 1E | RS | IRS | 4E | N | + | 7E | | = |
| 1F | US* | IUS* | 4F | O | | 7F | DEL | " |
| 20 | SP | DS | 50 | P | & | 80 | | |
| 21 | ! | SOS | 51 | Q | | 81 | | a |
| 22 | " | FS | 52 | R | | 82 | | b |
| 23 | # | | 53 | S | | 83 | | c |
| 24 | \$ | BYP | 54 | T | | 84 | | d |
| 25 | % | LF | 55 | U | | 85 | | e |
| 26 | & | ETB/EOB | 56 | V | | 86 | | f |
| 27 | ' | PRE/ESC | 57 | W | | 87 | | g |
| 28 |) | | 58 | X | | 88 | | h |
| 29 | * | | 59 | Y | | 89 | | i |
| 2A | + | SM | 5A | Z | ! | 8A | | |
| 2B | , | CU2 | 5B | [| \$ | 8B | | |
| 2C | - | | 5C | \ | * | 8C | | |
| 2D | . | ENQ | 5D |] |) | 8D | | |
| 2E | / | ACK | 5E | ^ | ; | 8E | | |
| 2F | | BEL | 5F | _ | ~ | 8F | | |

* Used as the III Control Character.

CODE CHART: SDA II, CONT'D

| HEX. | EBCDIC | HEX. | EBCDIC | HEX. | EBCDIC | HEX. | EBCDIC |
|------|--------|------|--------|------|--------|------|--------|
| 90 | | AC | | C8 | H | E4 | U |
| 91 | j | AD | | C9 | I | E5 | V |
| 92 | k | AE | | CA | | E6 | W |
| 93 | l | AF | | CB | | E7 | X |
| 94 | m | B0 | | CC | | E8 | Y |
| 95 | n | B1 | | CD | | E9 | Z |
| 96 | o | B2 | | CE | | EA | |
| 97 | p | B3 | | CF | | EB | |
| 98 | q | B4 | | D0 | | EC | |
| 99 | r | B5 | | D1 | J | ED | |
| 9A | | B6 | | D2 | K | EE | |
| 9B | | B7 | | D3 | L | EF | |
| 9C | | B8 | | D4 | M | FO | Ø |
| 9D | | B9 | | D5 | N | F1 | 1 |
| 9E | | BA | | D6 | O | F2 | 2 |
| 9F | | BB | | D7 | P | F3 | 3 |
| A0 | | BC | | D8 | Q | F4 | 4 |
| A1 | ~ | BD | | D9 | R | F5 | 5 |
| A2 | s | BE | | DA | | F6 | 6 |
| A3 | t | BF | | DB | | F7 | 7 |
| A4 | u | C0 | { | DC | | F8 | 8 |
| A5 | v | C1 | A | DD | | F9 | 9 |
| A6 | w | C2 | B | DE | | FA | |
| A7 | x | C3 | C | DF | | FB | |
| AB | y | C4 | D | E0 | | FC | |
| A9 | z | C5 | E | E1 | | FD | |
| AA | | C6 | F | E2 | S | FE | |
| AB | | C7 | G | E3 | T | FF | |

NOTES: 1) SDA II codes have the same bit configuration in the SLCP as in the SCP.

2) The following configurations when preceded by the DLE character (hex. 10) are defined as listed below;

EBCDIC

ASC II

'70' = ACK 0

'30' = ACK 0

'61' = ACK 1

'31' = ACK 1

'6B' = WACK

'3B' = WACK

'7C' = RVI

'3C' = RVI

'7F' = WABT

'3F' = WABT

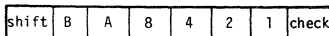
3) The bit configuration '1F' performs the intermediate block check (ITB) function.

CHARACTER CODE BIT TRANSPOSITIONS

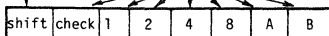
TAI, TAI1 TERMINAL ADAPTER EMULATORS

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

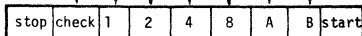
8-Bit Character in Channel "0" Buffer



8-Bit Character in Communications Buffer*



7-Bit Character Plus Start-Stop on Comm-Line

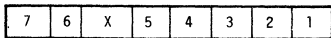


* The Emulator Will Strip Off the Shift Bit before Inserting in the Communication Buffer.

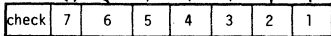
TA I11 TERMINAL ADAPTER EMULATOR

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

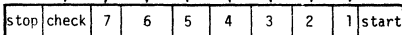
8-Bit Character in Channel "0" Buffer



8-Bit Character in Communications Buffer



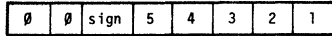
8-Bit Character Plus Start-Stop on Comm-Line



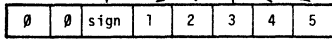
TGHI TERMINAL ADAPTER, WORLD-TRADE TTY EMULATORS

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

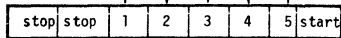
8-Bit Character in Channel
"0" Buffer



8-Bit Character in
Communications Buffer



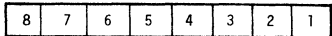
5-Bit Character Plus Start-Stop
on Comm-Line



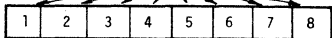
TGH II TERMINAL ADAPTER EMULATOR

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

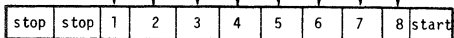
8-Bit Character in Channel
"0" Buffer



8-Bit Character in
Communications Buffer



8-Bit Character Plus
Start-Stop Bits on
Comm-Line

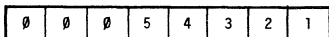


Between COMTEN Core and COMTEN 10 Low-Speed Line

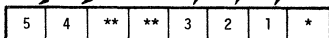
- 5-Level Conversion

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

5-Bit Character in COMTEN Core Byte



5-Bit Character Embedded in Byte for COMTEN 10



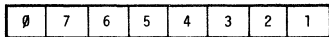
* Forced To "0"

** Forced To "1"

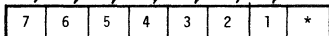
- 7-Level Conversion

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

7-Bit Character in COMTEN Core Byte



7-Bit Character Embedded in Byte for COMTEN 10



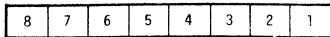
* Forced To "0"

- 8-Level Conversion (none necessary)

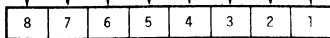
SDA II TERMINAL ADAPTER EMULATOR

| | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Power of 2 | 2^7 | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 |
| Bit Position | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

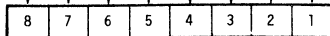
8-Bit Character in Channel
"0" Buffer



8-Bit Character in
Communications Buffer



8-Bit Character on
Comm-Line



HEXADECIMAL-DECIMAL CONVERSION

To find a decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find a Hex number, locate the next lower decimal and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

| BYTE | | | | BYTE | | | | BYTE | | | |
|------|------------|------|---------|------|--------|------|-------|------|-----|------|-----|
| 0123 | | 4567 | | 0123 | | 4567 | | 0123 | | 4567 | |
| HEX | DEC | HEX | DEC | HEX | DEC | HEX | DEC | HEX | DEC | HEX | DEC |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1,048,576 | 1 | 65,536 | 1 | 4,096 | 1 | 256 | 1 | 16 | 1 | 1 |
| 2 | 2,097,152 | 2 | 131,072 | 2 | 8,192 | 2 | 512 | 2 | 32 | 2 | 2 |
| 3 | 3,145,728 | 3 | 196,608 | 3 | 12,288 | 3 | 768 | 3 | 48 | 3 | 3 |
| 4 | 4,194,304 | 4 | 262,144 | 4 | 16,384 | 4 | 1,024 | 4 | 64 | 4 | 4 |
| 5 | 5,242,880 | 5 | 327,680 | 5 | 20,480 | 5 | 1,280 | 5 | 80 | 5 | 5 |
| 6 | 6,291,456 | 6 | 393,216 | 6 | 24,576 | 6 | 1,536 | 6 | 96 | 6 | 6 |
| 7 | 7,340,032 | 7 | 458,752 | 7 | 28,672 | 7 | 1,792 | 7 | 112 | 7 | 7 |
| 8 | 8,388,608 | 8 | 524,288 | 8 | 32,768 | 8 | 2,048 | 8 | 128 | 8 | 8 |
| 9 | 9,437,184 | 9 | 589,824 | 9 | 36,864 | 9 | 2,304 | 9 | 144 | 9 | 9 |
| A | 10,485,760 | A | 655,360 | A | 40,960 | A | 2,560 | A | 160 | A | 10 |
| B | 11,534,336 | B | 720,896 | B | 45,056 | B | 2,816 | B | 176 | B | 11 |
| C | 12,582,912 | C | 786,432 | C | 49,152 | C | 3,072 | C | 192 | C | 12 |
| D | 13,631,488 | D | 851,968 | D | 53,248 | D | 3,328 | D | 208 | D | 13 |
| E | 14,680,064 | E | 917,504 | E | 57,344 | E | 3,584 | E | 224 | E | 14 |
| F | 15,728,640 | F | 983,040 | F | 61,440 | F | 3,840 | F | 240 | F | 15 |
| 6 | | 5 | | 4 | | 3 | | 2 | | 1 | |

MAXIMUM STORAGE ADDRESS

STORAGE SIZE
(BYTES)

LAST BYTE
ADDRESS

STORAGE SIZE
(BYTES)

LAST BYTE
ADDRESS

| | | |
|------|--------|-------|
| 16K | | 03FFF |
| 32K | | 07FFF |
| 48K | | 0BFFF |
| 64K | | 0FFFF |
| 80K | | 13FFF |
| 96K | | 17FFF |
| 112K | K=1024 | 1BFFF |
| 128K | | 1FFFF |
| 144K | | 23FFF |
| 160K | | 27FFF |
| 176K | | 2BFFF |
| 192K | | 2FFFF |
| 208K | | 33FFF |
| 224K | | 37FFF |
| 240K | | 3BFFF |

| | | |
|------|--------|-------|
| 256K | | 3FFFF |
| 272K | | 43FFF |
| 288K | | 47FFF |
| 304K | | 4BFFF |
| 320K | | 4FFFF |
| 336K | | 53FFF |
| 352K | | 57FFF |
| 368K | K=1024 | 5BFFF |
| 384K | | 5FFFF |
| 400K | | 63FFF |
| 416K | | 67FFF |
| 432K | | 6BFFF |
| 448K | | 6FFFF |
| 464K | | 73FFF |
| 480K | | 77FFF |
| 496K | | 7BFFF |
| 512K | | 7FFFF |

• POWERS •

| POWERS OF 16 | | | | | POWERS OF 2 | | | | | | |
|--------------|-----|-----|-----|-----|-------------|-----|-----|-----|-----|-----|----|
| 16^n | | | n | | 2^n | n | | | | | |
| | | | 1 | 0 | | 512 | 9 | | | | |
| | | | 16 | 1 | 1 | 024 | 10 | | | | |
| | | | 256 | 2 | 2 | 048 | 11 | | | | |
| | | 4 | 096 | 3 | 4 | 096 | 12 | | | | |
| | | 65 | 536 | 4 | 8 | 192 | 13 | | | | |
| | 1 | 048 | 576 | 5 | 16 | 384 | 14 | | | | |
| | 16 | 777 | 216 | 6 | 32 | 768 | 15 | | | | |
| | 268 | 435 | 456 | 7 | 65 | 536 | 16 | | | | |
| | 4 | 294 | 967 | 296 | 8 | 131 | 072 | 17 | | | |
| | 68 | 719 | 476 | 736 | 9 | 262 | 144 | 18 | | | |
| 1 | 099 | 511 | 627 | 776 | 10 | 524 | 288 | 19 | | | |
| 17 | 592 | 186 | 044 | 416 | 11 | 1 | 048 | 576 | 20 | | |
| 281 | 474 | 976 | 710 | 656 | 12 | 2 | 097 | 152 | 21 | | |
| 4 | 503 | 599 | 627 | 370 | 496 | 13 | 4 | 194 | 304 | 22 | |
| 72 | 057 | 594 | 037 | 927 | 936 | 14 | 8 | 388 | 608 | 23 | |
| 1 | 152 | 921 | 504 | 606 | 846 | 976 | 15 | 16 | 777 | 216 | 24 |

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COMTEN

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