CIRRUS LOGIC

*PRELIMINARY DATA SHEET*
*June, 1987*

## FEATURES

- Buffer size from 256 to 64K bytes
- Automatic generation of external address latch enables
- Non multiplexed addressing of up to 16K bytes
- Interfaces directly with 16 MHz 8051
- DMA handshake logic – handles transfer rate up to 2.5 Mb/s
- Provides host transfer overrun control
- Dual port circular FIFO buffer control
- Port priority resolver
- SCSI arbitration logic
- Optimized for use with the CL–SH130 Winchester hard disk formatter
- Single +5V power supply
- 44-pin PLCC and 40-pin P-DIP packages
- 2-Micron double metal CMOS technology

*CL – SH 120*

# Buffer Storage Manager

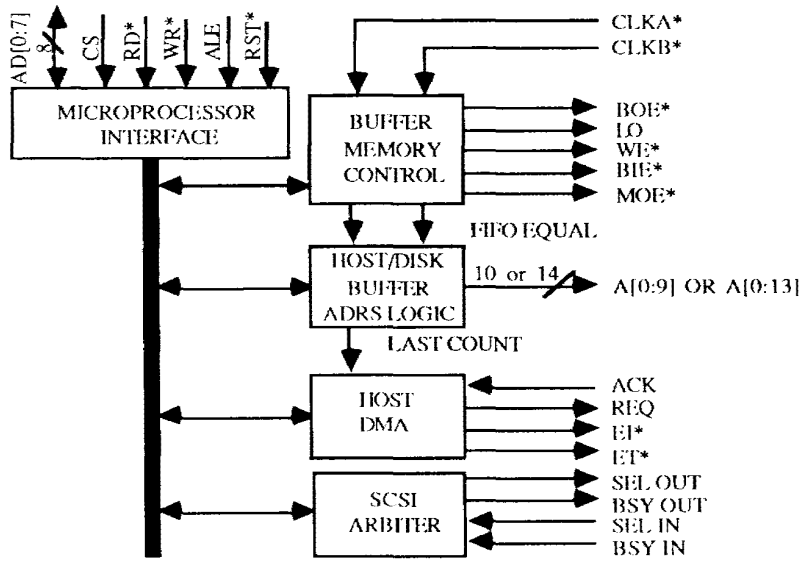
## OVERVIEW

The CL–SH120 is a VLSI component that provides the buffer management and SCSI port control for an intelligent Winchester disk controller. The CL–SH120 design eases the implementation of a SCSI interface, since the majority of the functionality needed for this is inherent in the overall architecture.

The CL–SH120 will control up to 64K bytes of dual-ported buffer memory, supporting both non-multiplexed/-multiplexed addressing modes with software-selectable switchover range. It supports synchronous data transfer to and from the drive at the data transfer frequency, and provides REQ/ACK handshake for asynchronous transfer with the host.

The CL–SH120 is designed to be software configurable via a multiplexed microprocessor I/O bus as provided by the Intel 8085 and 8051 microprocessor families and is easily adaptable to other microprocessor I/O techniques.

## FUNCTIONAL BLOCK DIAGRAM




71-02a-1M-5C

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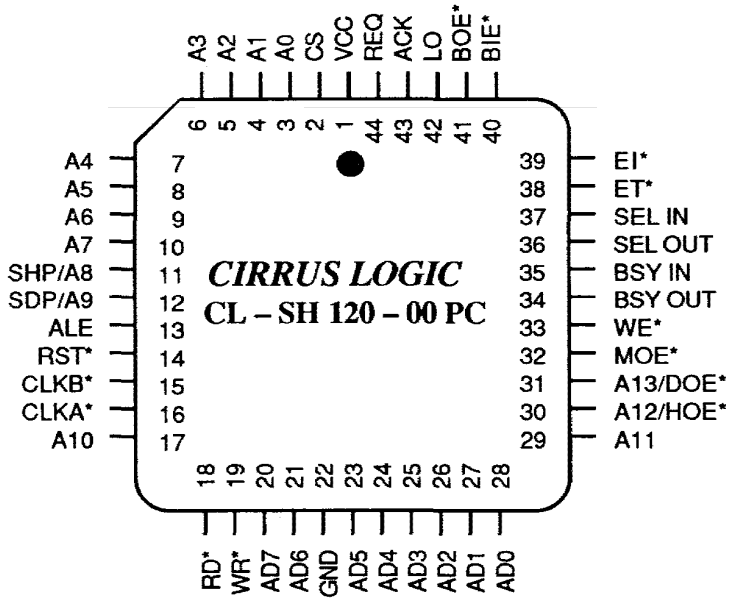
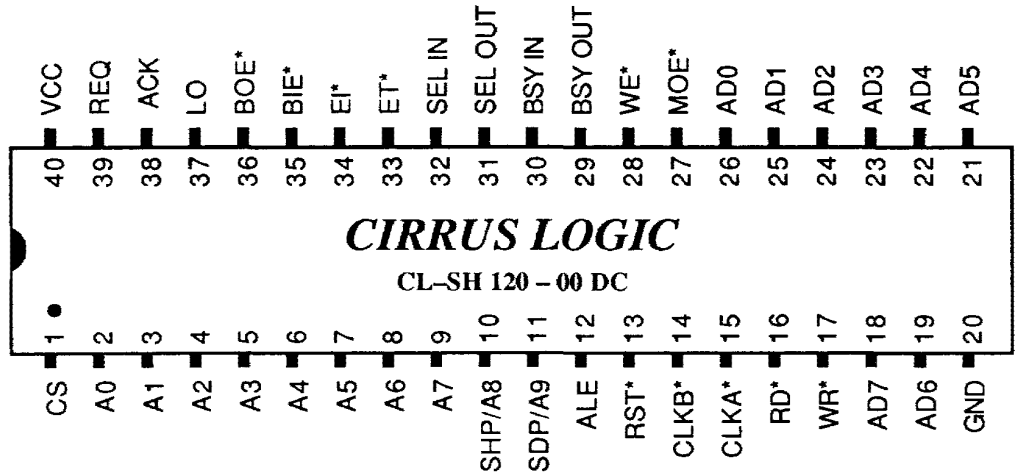
### 1.1 Pin Diagram For 44-Pin PLCC




* Denotes negative true signal.

### 1.2 Pin Diagram For 40-Pin P-DIP



## 1.3 Pin Assignments – 44-Pin PLCC

| SYMBOL | NUM. | TYPE | DESCRIPTION |
|---|---|---|---|
| VCC | 1 | I | POWER SUPPLY |
| CS | 2 | I | CHIP SELECT: Active during chip access by microprocessor |
| A0-A7 | 3-10 | O | BUFFER ADDRESS LINES: Bits 0-7 for addressing low order address in the Minimum Addressing Mode. They are the multiplexed low and high order addresses in the Maximum Addressing Mode. |
| SHP/A8 | 11 | O | STROBE HOST POINTER/A8: In the Maximum Addressing Mode, this pin is SHP. It strobes the high order address byte into the external host address latch during host data transfer. In the minimum and extended mini - mum addressing modes, this pin is Buffer Address bit A8. |
| SDP/A9 | 12 | O | STROBE DEVICE POINTER/A9: In the Maximum Addressing Mode, this pin is SDP. It strobes the high order address byte into the external device address latch during data transfer. In the minimum and extended minimum addressing modes, this pin is Buffer Address bit A9. |
| ALE | 13 | I | ADDRESS LATCH ENABLE: This control signal latches the address on the AD lines. |
| RST* | 14 | I | RESET: When asserted, all internal registers will be reset and bit 0 of Register 59H will be set. |
| CLKB* | 15 | I | CLKB: When asserted, a data transfer cycle will take place between the device and the buffer during the following negative going edge of the CLKA*. |
| CLKA* | 16 | I | CLKA: This is the primary clock for the CL–SH120. Its minimum period is 200 ns (5 MHz max frequency). |
| A10 | 17 | O | BUFFER ADDRESS LINE: Buffer address bit 10. |
| RD* | 18 | I | READ: RD* and CS active causes the data from the specified register to be read on to the AD lines. |
| WR* | 19 | I | WRITE: WR* and CS active causes the data on the AD lines to be written into the specified register. |
| AD6-AD7 | 20-21 | I/O | MULTIPLEXED ADDRESS/DATA: Bits 6 and 7 of the multiplexed tri-state Address/Data bus of the microprocessor interface. |
| GND | 22 | I | GROUND: The electrical ground connection. |
| AD0-5 | 23-28 | I/O | MULTIPLEXED ADDRESS/DATA: Bits 0 to 5 of the multiplexed tri-state Address Data bus of the microprocessor interface. |

(*) Denotes negative true signal.

| SYMBOL | NUM. | TYPE | DESCRIPTION (cont'd) |
|---|---|---|---|
| A11 | 29 | O | BUFFER ADDRESS LINE: Buffer address bit 11. |
| HOE*/A12 | 30 | O | HOST LATCH ENABLE: HOE* in the Maximum Addressing Mode. Enables the external host address latch on the buffer address bus during host data transfer. Buffer Address bit A12 in the Extended Minimum Addressing mode. HOE* in the Minimum Addressing Mode, but is not used. |
| DOE*/A13 | 31 | O | DEVICE LATCH ENABLE: In the Maximum Addressing Mode, this pin is DOE*. It enables the device address latch on the buffer address bus dur - ing device data transfer. In the Extended Minimum Addressing Mode, this pin is Buffer Address bit A13. In the Minimum Addressing Mode this pin is DOE*, but is not used. |
| MOE* | 32 | O | MEMORY SELECT: Asserted when a buffer RAM operation is active. Should be connected to the RAM output enable for high speed operation. |
| WE* | 33 | O | WRITE ENABLE: Asserted when a buffer write operation is active. |
| BSY OUT | 34 | O | BUSY OUT: Asserted when the microprocessor sets bit 7 of Register 52H. Also asserted by the arbitration logic during the arbitration phase. |
| BSY IN | 35 | I | BUSY IN: Active indicates BSY is being asserted on the SCSI bus. |
| SEL OUT | 36 | O | SELECT OUT: Set by the microprocessor as bit 6, Register 52H (Channel Control). |
| SEL IN | 37 | I | SELECT IN: Active indicates a bus select status and will reset the arbi - tration circuitry to be ready for Bus Free detection. |
| ET* | 38 | O | ENABLE TARGET: Microprocessor-settable signal to identify slave status. |
| EI* | 39 | O | ENABLE INITIATOR: Microprocessor-settable signal to identify master status. |
| BIE* | 40 | O | BUS INPUT ENABLE: Used to gate data from the host bus on to the buf - fer memory bus. This pin is asserted by DMA logic or by setting bit 2 in Register 52H. |
| BOE* | 41 | O | BUS OUTPUT ENABLE: Used to gate data from the external latch on to the host bus. This pin is asserted by DMA logic or by setting bit 3 in Register 52H. |
| LO | 42 | O | LATCH OUT: Used to latch the data into the external latch from the buf - fer memory bus. |
| ACK | 43 | I | PORT B ACKNOWLEDGE: When active, indicates that the host has acknowledged the data transfer. |
| REQ | 44 | O | PORT B REQUEST: Asserted to request the host for data transfer. |

(*) Denotes negative true signal.

## 2. REGISTER TABLES

### 2.1 Internal Registers

| REGISTER(S) | ACCESS | DESCRIPTION/FUNCTION |
|---|---|---|
| 52H | R/W | HOST INTERFACE CONTROL: Register for Host bus and Arbitration. |
| 53H | R/W | DMA CONTROL: Starts DMA operations, and defines data transfer direc - tion for both host and device. |
| 54H | R/W | BUFFER SIZE: Specifies the size of the buffer, hence determining whether the multiplexed-address mode is activated. |
| 55H | R/W | ADDRESS MODE CONTROL: Specifies the Extended Address Mode where the CL–SH120 can directly address up to 16Kbytes of buffer memory. |
| 59H | W | RESET CONTROL: Any write to this register will reset RAP, WAP, and SP registers. Sets bit 0 to reset all internal registers. |
| 5AH & 5BH | R/W | READ ADDRESS POINTER (RAP): Addresses buffer on read cycle. |
| 5CH & 5DH | R/W | WRITE ADDRESS POINTER (WAP): Addresses buffer on write cycle. |
| 5EH & 5FH | R/W | STOP POINTER (SP): Used to prevent the host from overrunning the device. The STOP POINTER is compared with the RAP/WAP (Registers 5AH-5DH). When they are equal, the DMA Done bit (Register 53H, Bit 5) is set, and the DMA REQ/ACK cycle is halted. If a new STOP POINTER is set, a new DMA cycle will begin again if the appropriate Read Latch or Write Latch bit is still active. |

### 2.2 External Registers

The external registers are not physical, but logical register addresses that allow the microprocessor to gain access to the host data bus and the buffer.

| REGISTER(S) | ACCESS | DESCRIPTION/FUNCTION |
|---|---|---|
| 50H | R/W | REGISTER 50H DECODE: Allows the processor to gain access to the host data bus. It is used in conjunction with Register 52H Bit 2 or 3 for Read or Write respectively. A write to Register 50H will assert LO. |
| 51H | R/W | REGISTER 51H DECODE: Allows the processor to gain access to the high order byte in the 16-bit host data bus application. It operates the same way as Register 50H. |
| 70H | R/W | REGISTER 70H DECODE: Allows the processor to gain access to the buffer. A Register 70H Read will cause MOE* to be active. A Register 70H Write will cause both MOE* and WE* to be active. |

## 3. FUNCTIONAL DESCRIPTION

The CL–SH120 consists of four major blocks:

- Microprocessor Interface,
- Buffer Memory Control,
- SCSI Arbitration Logic and
- Host DMA Control

### 3.1 Microprocessor Interface

The Microprocessor Interface block decodes addresses 50H to 5FH and 70H to provide various read/write strobes to access 11 internal registers and three external registers. The internal registers include the host bus access and arbitration control register, the DMA control register, the Buffer size register, the Reset register, the Read Address Pointer, the Write Address Pointer, the Stop Pointer and the Address Mode register. The three external registers are not physical registers but logical register addresses that allow the microprocessor to gain access to the host data bus and the buffer.

### 3.2 Buffer Memory Control

Buffer Memory Control provides MEMORY SELECT (MOE*) and READ/WRITE (WE*) signals that are used to read or write data from the RAM buffer. It also resolves the priority between buffer access requests from the disk or from the host. Since the disk transfer, also referred to as Port A transfer, is a synchronous transfer, it gets priority over host transfer (also referred to as Port B transfer). The CL–SH120 is capable of handling buffer sizes from 256 to 64K bytes of static RAM. The chip provides up to 16 buffer address signals necessary to do this, along with the MEMORY SELECT (MOE*) signal and a Read/Write (WE*) signal. All of the buffer addressing is done with 14 address lines (A0-A13), four of which are dual purpose (A8/SHP, A9/SDP, A12/HOE* and A13/DOE*).

### 3.3 SCSI Arbitration Logic

The SCSI Arbitration Logic handles all the arbitration timing to access the SCSI bus. It allows stacking a request for arbitration when the SCSI bus is in the busy state. It continuously searches for the SCSI Bus Free (BUSY IN and SELECT IN inactive for up to three CLKA* cycles) which then allows entering the arbitration phase after four more CLKA* cycles if the Arbitration Bit is enabled. The microprocessor is expected to evaluate the Bus ID byte to determine whether it has won the arbitration, and taken care of the Selection/Reselection process.

### 3.4 Host DMA Control

The Host DMA Control provides the logic circuitry for the REQ/ACK handshake signals for transferring data between the host and buffer memory. It also provides the logic to stop DMA transfer and prevent a host overrun situation.

## 4. FUNCTIONAL OPERATION

### 4.1 Addressing Modes

There are three addressing modes in which the chip can operate:

- Minimum Addressing Mode,
- Extended Minimum Addressing Mode and
- Maximum Addressing Mode.

The Minimum Addressing Mode enables buffer address lines A0 to A9. In the Extended Mini - mum Addressing Mode, Buffer address lines A0 to A13 are enabled. In the Maximum Addres - sing Mode, Address lines A0 to A7 are enabled, but there is an external latch which latches the first eight bits as the upper address byte. The Minimum and Extended Minimum Addressing Modes are invoked by programming bit 0 of register 55H. The Maximum Addressing Mode is invoked automatically when the Buffer Size register (Register 54H) is programmed for a buffer size greater than what the current addressing mode can directly address.

The chip will power up in the Minimum (10 bits) Addressing Mode. In this mode, the CL–SH120 will directly address buffer RAM of up to 1K bytes. If the buffer size register is set for more than 1K bytes, then the Maximum Addressing Mode will be invoked automat - ically. If the Extended Addressing Mode bit (Register 55H, Bit 0) is set, 14-bit addressing is available directly from pins A0 to A13 during read or write operation, allowing up to 16K bytes to be addressed directly only in the 44-pin PLCC configuration. If the Buffer Size Register is set for a size greater than 16K bytes, then the chip will operate in the Maximum (16-bit) Addressing Mode. Figures 4.1 and 4.2 show suggested system hookups for the Mini - mum and Extended Minimum Addressing Modes respectively.

In Maximum Addressing Mode, 16 address bits are used, allowing up to 64K bytes of buffer RAM in the Address-Multiplexed scheme whereby external latches are required to hold high order address bytes. This mode is invoked by setting the buffer size register for more than either 1K bytes or 16K bytes, depending on whether the Extended Address Mode Bit (Reg - ister 55H, Bit 0) is reset or set respectively.

The contents of the external latches are derived from internal registers 5BH or 5DH, depending upon the nature of the access. They are updated by the address strobes SHP and SDP on the CLKA* cycle following the update of the appropriate internal register if a CLKB* cycle is not required. If a CLKB* cycle is required, these latches will be updated in the following CLKA* cycle after the CLKB* cycle. Internal registers are updated either by a microprocessor write operation to those registers or by auto in - crementing the counters after a read or write cycle. **A word of caution: For proper operation of the CL–SH120 the microprocessor should not update these latches during a disk read or write operation.** In normal operation, these updates will occur after every 256 bytes trans- ferred by either port. Also in this mode, exter- nal latch output enables are provided by the HOE* and DOE* to minimize external compo - nents. Figure 4.3 shows a suggested system hookup for the Maximum Addressing Mode.

The CLKA* period determines the access time requirement for the buffer RAM, along with the valid address time for the CL–SH120. How - ever, it is recommended practice to use MEMORY SELECT (MOE*) as the RAM out - put enable to take advantage of utilizing slower speed RAM in high speed applications.

For properly interleaved CLKB* and Port B operation, the maximum rate at which CLKB* requests should occur is once every two CLKA* cycles. This allows Port B REQ/ACK cycles to occur at one half the CLKA* rate. CLKB* cycles always have priority over Port B cycles.

**Summary of different address modes.**

| Pin | Minimum Mode | Extended Minimum Mode | Maximum Mode |
|---|---|---|---|
| | R55H(0)=0 X≤1K | R55H(0)=1 X≤16K | R55H(0)=0, 1K<X≤64K, R55H(0)=1, 16K<X≤64K |
| 11 | A8 | A8 | SHP |
| 12 | A9 | A9 | SDP |
| 17 | Unused | A10 | A10 |
| 29 | Unused | A11 | A11 |
| 30 | HOE* | A12 | HOE* |
| 31 | DOE* | A13 | DOE* |

NOTES: (X) denotes buffer size in bytes.
Only minimum mode is available in 40-pin P-DIP parts.

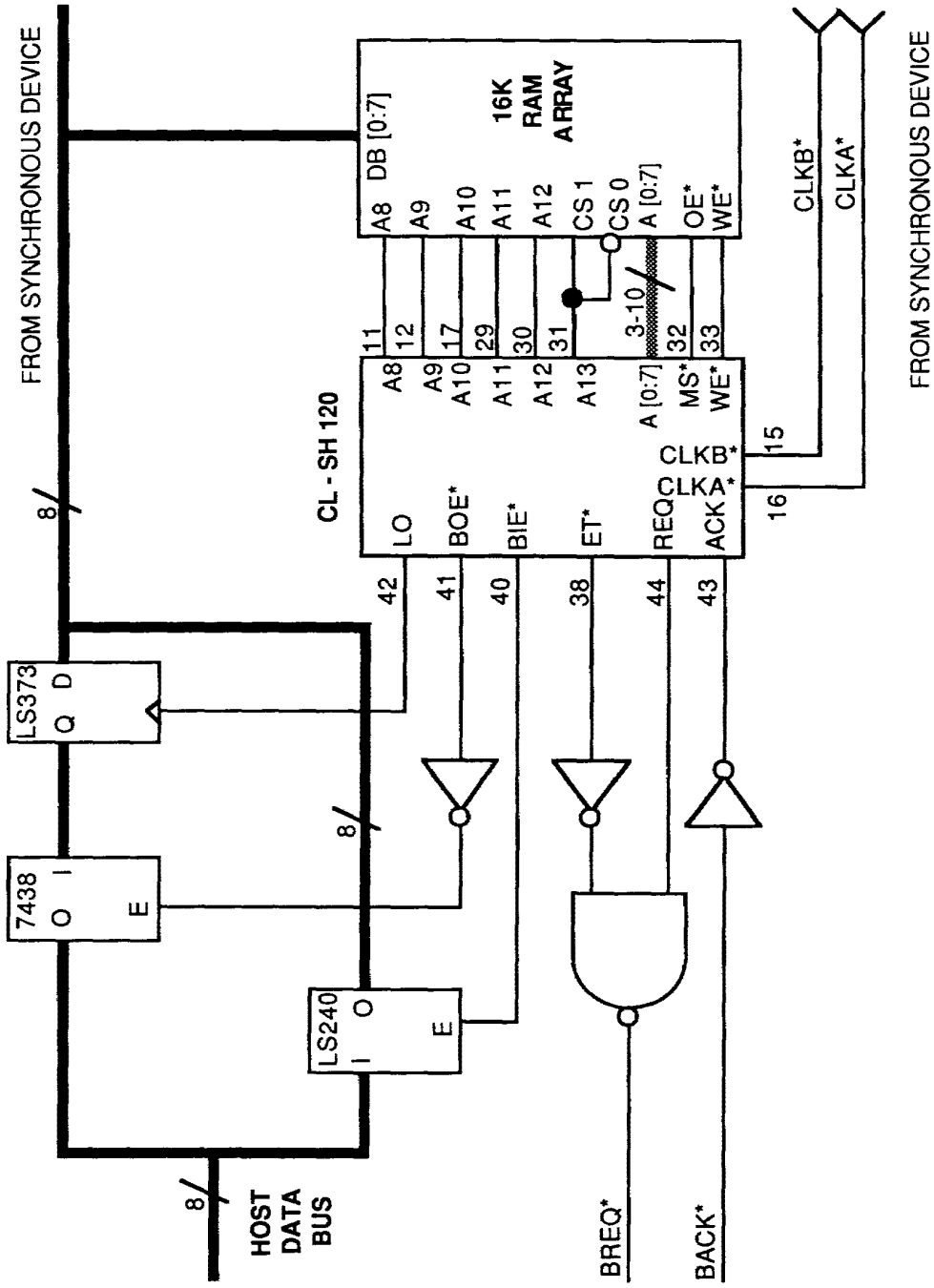



Figure 4.1 Minimum Addressing Mode

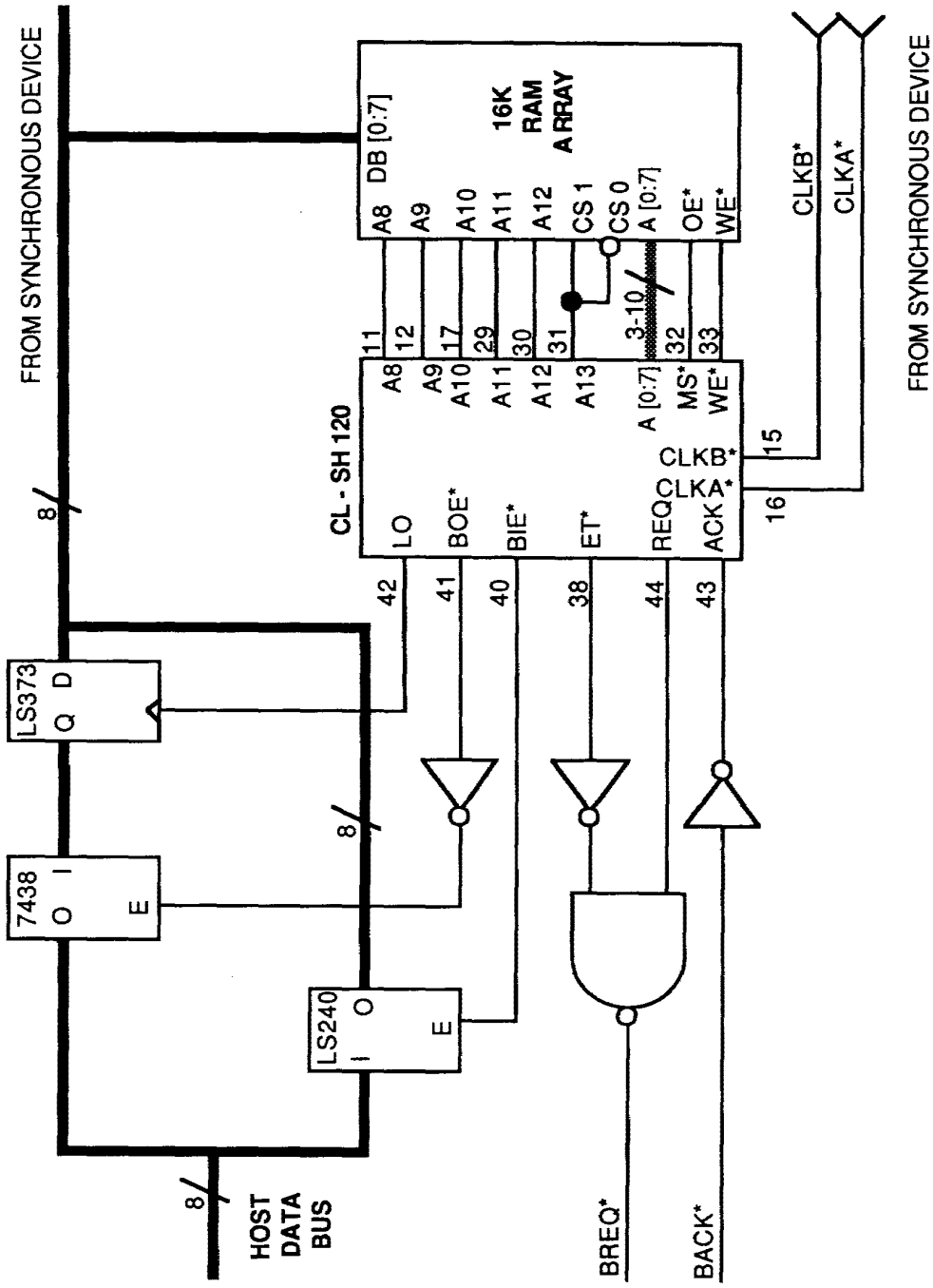



Figure 4.2 Extended Minimum Addressing Mode
(Not available in 40-pin P-DIP parts)

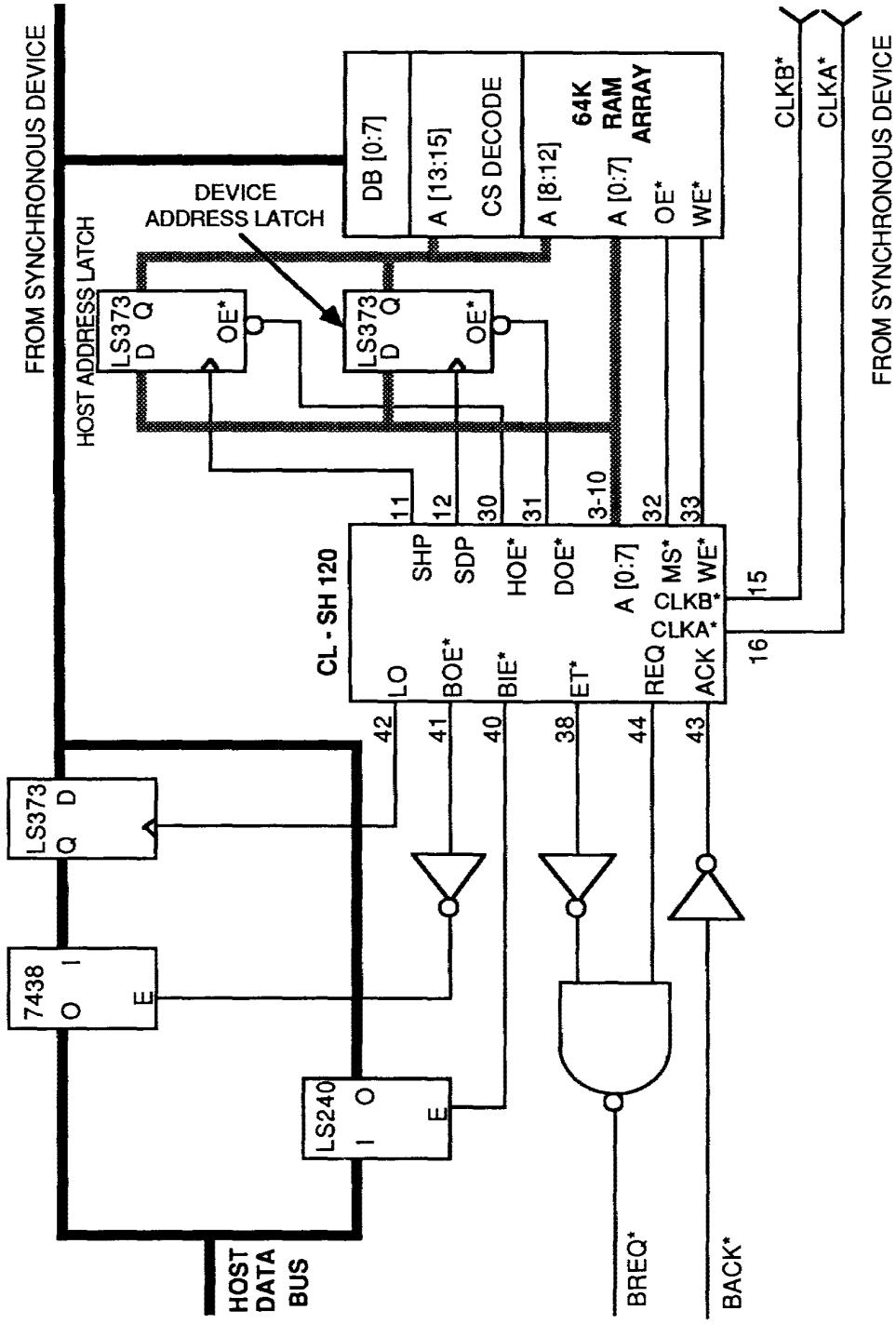



Figure 4.3 Maximum Addressing Mode
(Not available in 40-pin P-DIP parts)

## 4.2 Data Transfer Description

The CL–SH120 handles data transfer in two ways: (1) synchronously with the peripheral (CLKB* transfer) or (2) asynchronously with the host (Port B transfer).

### Synchronous Transfer

In case of CLKB* transfers, a byte is transferred each time after CLKB* is asserted. This line is sampled on the falling edge of the CLKA* signal, and the data transfer will take place on the next cycle after CLKB* is asserted.

The direction of the transfer is determined by the state of the ROP/WOP bit (Register 53H, Bit 4). If it is set, then a Disk Read Operation (ROP) is performed from the disk to the memory. The contents of the WAP Registers (5CH and 5DH) are used to select the buffer memory location, and MEMORY SELECT (MOE*) and WRITE ENABLE (WE*) are used to write the data to that buffer memory address.

If the ROP/WOP bit (Register 53H, Bit 4), is reset, a Disk Write Operation (WOP) from memory to the disk is performed. The RAP Registers (5AH and 5BH) are used to generate the buffer memory address, and the data is read when MEMORY SELECT (MOE*) is active. The CL–SH120 samples the data from the RAM at the falling edge of CLKA* signal following the CLKB*.

### Asynchronous Transfer

In case of Port B transfers, data is transferred under DMA control. Again the direction of transfer is determined by the state of the ROP/ - WOP bit (Register 53H, Bit 4), and either WRITE LATCH or READ LATCH Bit (Register 53H, Bit 1 or Bit 2, respectively). **NOTE: For correct operation of CL–SH120, the ROP/WOP Bit (Register 53H, Bit 4) MUST be set when the READ LATCH Bit (Register 53H, Bit 2) is set. Also, the ROP/ - WOP Bit (Register 53H, Bit 4) MUST be reset when the WRITE LATCH Bit (Register 53H, bit 1) is set.**

If the READ LATCH Bit (Register 53H, Bit 2) is set and the ROP/WOP bit is set (ROP), then the data is transferred from the buffer to the host. The contents of the RAP Registers (5AH and 5BH) are used to address the buffer memory. The data from the RAM is latched into an external latch by the LO signal. The data then is made available on the host data bus by assert - ing the BUS OUT ENABLE (BOE*) signal. A Port B REQ is sent to the host, and after accepting the data, the host completes the hand - shake by asserting the Port B ACK signal. After an acknowledgement has been received, both Port B REQ and BOE* are de-asserted and the RAP register is incremented.

If ROP/WOP (Register 53H, Bit 4) is reset (WOP), and Write Latch is on then data is transferred from the host into the buffer memory. The buffer memory address is provided by the contents of the WAP Registers (5CH and 5DH). The data from the host is ena - bled on to the buffer memory bus by asserting the BUS IN ENABLE (BIE*) signal to the external receiver.

During the host data transfer, the top buffer address that can be accessed is controlled by the STOP POINTER (Registers 5EH and 5FH). This STOP POINTER is compared with either the RAP or the WAP, masked by the contents of Register 54H, depending upon Read or Write Operation. When a match occurs, DMA DONE bit of Register 53H is set signifying the completion of the transfer to or from the host.

## 4.3 External Register Decode

In addition to the normal data transfer operations, the CL–SH120 also supports the processor access to both the host bus and the buffer by addressing the external Register 50H, 51H, and 70H respectively.

### Register 50H or 51H Decode

Register 50H or 51H decode is provided for the processor to directly access the host data bus via the buffer data bus. If used in conjunction with the CL–SH120, the buffer data bus and the processor data bus will be internally bridged accordingly.

A read to Register 50H or 51H will gate the host data into the processor data bus if the BUS IN ENABLE signal has been previously asserted by setting bit 2 of Register 52H. A write to Register 50H or 51H will activate LO signal to latch the data from the processor, then the BUS OUTPUT ENABLE signal is asserted by setting bit 3 of Register 52H to enable the processor data onto the host bus. Typical system configurations are illustrated in Figures 4.1, 4.2 and 4.3.

### Register 70H Decode

Register 70H decode is provided for the processor to gain access to the buffer. If used in conjunction with the CL–SH120, the buffer data bus and the processor data bus will be internally bridged accordingly.

In the minimum and extended minimum addressing mode, the address is generated by the CL–SH120 based upon the contents of the RAP if the ROP/WOP Bit (Register 53H, Bit 4) is reset (WOP) and on the contents of the WAP if the ROP/WOP Bit (Register 53H, Bit 4) is set (ROP). The RAP or WAP will not be incremented by Register 70H access. RAP registers are 5AH and 5BH. WAP registers are 5CH and 5DH.

In the maximum addressing mode, both RAP and WAP must be loaded with the same address, the ROP/WOP Bit (Register 53H, Bit 4) is set (ROP), and both READ LATCH Bit (Register 53H, Bit 3) and WRITE LATCH Bit (Register 53H, Bit 2) are reset.

## 4.4 SCSI Arbitration

The arbitration logic of the CL–SH120 complies with the SCSI arbitration and selection phase protocol and timing. Although the logic is designed to automatically arbitrate, the controlling processor is responsible for evaluating the arbitration byte and controlling the selection/reselection process.

The arbitration logic circuit continuously searches for the SCSI Bus Free phase (BUSY IN and SELECT IN inactive for a minimum of 600 nanoseconds). If the ARBITRATION REQUEST Bit (Register 52H, Bit 0) is set, the 'OK TO ARBITRATE' latch will be activated allowing the entering of the Arbitration phase. After a minimum of 800 nanoseconds, the arbitration will start and the BUSY OUT signal will be asserted automatically. If another SCSI device asserts 'SELECT IN' the internal 'OK TO ARBITRATE' latch will be immediately cleared and BUSY OUT will be deasserted. The CL–SH120 logic is still set up to find the next bus free phase and begin arbitration. Figure 4.4 illustrates the Arbitration logic circuit. The algorithm for arbitrating and selecting is as follows:

- The processor must write the arbitration bit to the external output buffer. This is done by writing to register 50H.
- The processor must set REQUEST ARBITRATION, bit 0 of register 52H.
- The processor must look for an Arbitration Status. This is done by reading bit 0 of register 52H. When this bit is active, arbitrating has begun.
- The processor must wait for at least 2.2 microseconds after first reading a positive Arbitrating Status. Then the arbitration byte should be read from register 50H. This byte must be evaluated for the arbitration results. If there is a higher priority requestor, that device's assertion of SELECT will immediately clear the internal 'OK TO ARBITRATE' signal and the Arbitrating Status. The CL–SH120 logic is still set up to find the next bus free phase and begin arbitration.
- If the arbitration has been won, assert the BUSY OUT, BUS OUTPUT ENABLE and SELECT LINES by setting bit 7, bit 3 and bit 6 of Register 52H. This will clear REQUEST ARBITRATION Bit and the Arbitration Status. Note that BUSY OUT and BUS OUTPUT ENABLE were already asserted by the internal arbitration logic. This assertion provides for correct selection phase protocol.
- The processor must wait at least 1.2 microseconds after asserting select. Then the processor should write the selection byte to register 50H. This will load the external output register. As a target reselecting an initiator, the I/O line on the SCSI bus should also be asserted at this time.
- The processor must deassert BUSY OUT. Now the processor must monitor the BUSY IN status by reading bit 5 of register 52H, this will indicate if the selected device has responded.
- If BUSY IN has not been asserted in the recommended 250 milliseconds, then the selection abort procedure should begin. First the data bus must be released by resetting bit 3 of register 52H. If there is still no response in 201 microseconds, then the SELECT OUT, bit 6 of register 52H, (also I/O if it has been asserted) should be de-asserted. This will totally release the SCSI bus.
- If the selection is successful, and the CL–SH120 is a target reselecting an initiator, then the processor should first reassert BUSY OUT (bit 7 of register 52H), second release both SELECT OUT and BUS OUT ENABLE (bits 3 and 7 of register 52H), and finally set I/O, MSG, and C/D lines on the SCSI bus appropriately to enter the Information Transfer phase. The REQ/ACK DMA circuitry will enable the input and output buffers as required.

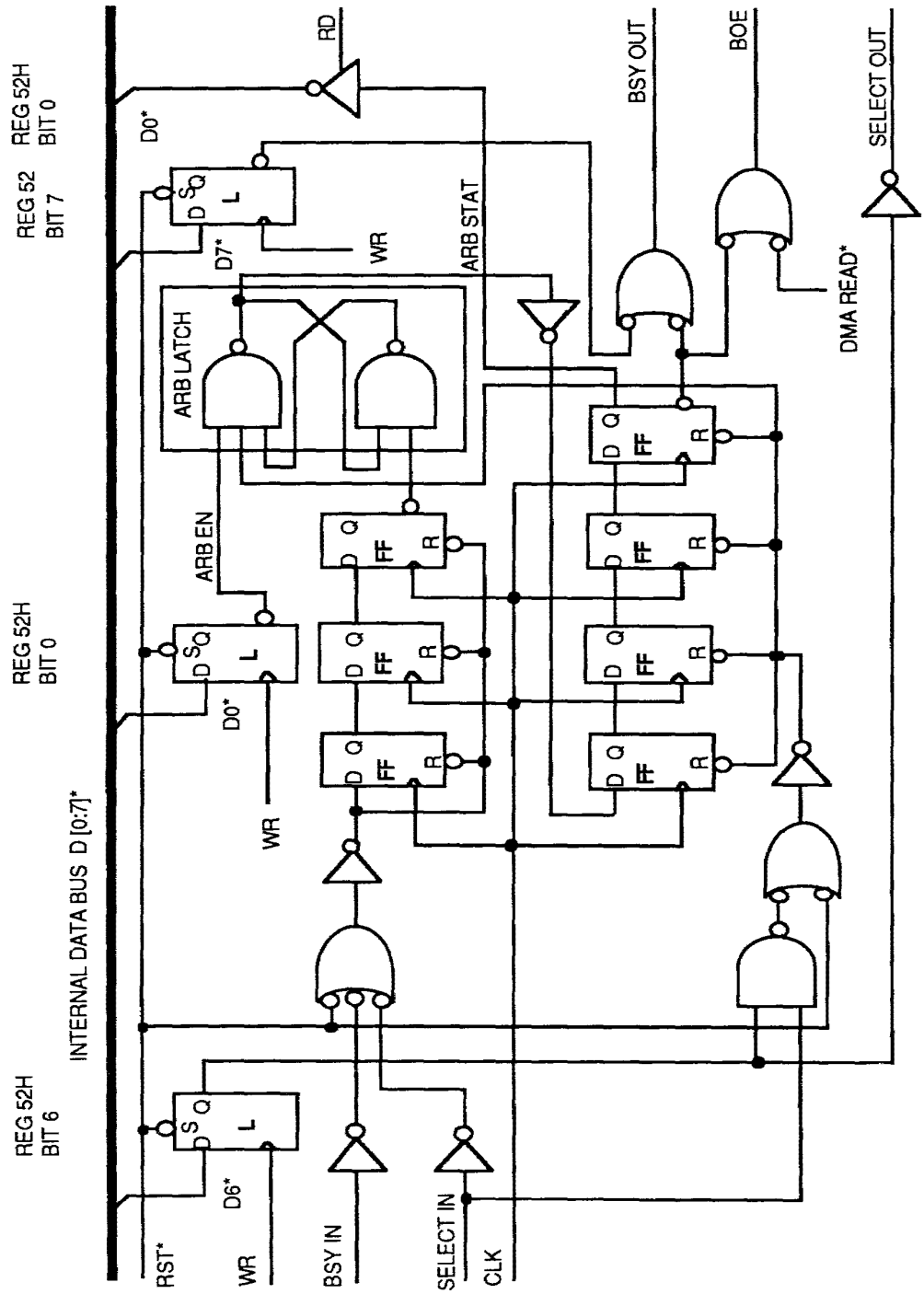



Figure 4.4 Arbitration Logic Circuit

## 5. DETAILED REGISTER DESCRIPTION

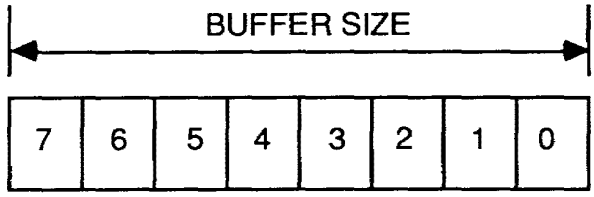
### 5.1 52H – Host Interface Control (Read/Write)

| | |
|---|---|
| Bit 0 | ARBITRATION: Setting this bit enables the arbitration logic circuit. The Arbitration Status can also be monitored by reading this bit. |
| Bit 1 | NOT USED: Status indeterminate. |
| Bit 2 | BUS IN ENABLE: Setting this bit will assert the BIE pin, allowing data from the host data bus onto the buffer memory bus. |
| Bit 3 | BUS OUT ENABLE: Setting this bit will assert the BOE pin, allowing data from the buffer memory bus onto the host data bus. |
| Bit 4 | SELECT IN: This bit indicates the status of the Select In signal ( READ ONLY ). |
| Bit 5 | BUSY IN: This bit indicates the status of the Busy In signal (READ ONLY). |
| Bit 6 | SELECT OUT: Set this bit after the arbitration has been won. |
| Bit 7 | BUSY OUT: Setting this bit will assert BUSY OUT pin. |

### 5.2 53H – DMA Control (Read/Write)

| | |
|---|---|
| Bit 0 | NOT USED: Status indeterminate. |
| Bit 1 | SCSI ACKNOWLEDGE STATUS: Indicates status of ACK (READ ONLY) pin. |
| Bit 2 | WRITE LATCH: Setting this bit will start DMA transfer from the host to the buffer. In addition, the ROP/WOP bit (Bit 4) must be reset when this bit is set. |
| Bit 3 | READ LATCH: Setting this bit will start DMA transfer from the buffer to the host. In addition, the ROP/WOP bit (Bit 4) must be set when this bit is set. |
| Bit 4 | ROP/WOP: Set this bit for a Read Operation: Assertion of CLKB* will cause data transfer from device to buffer. With READ LATCH bit set, DMA cycle will be activated to transfer data from buffer to host. Reset this bit for a Write Operation: Assertion of CLKB* will cause data transfer from buffer to device. With WRITE LATCH bit set, DMA cycle will be activated to transfer data from host to buffer. |
| Bit 5 | DMA DONE: When set, indicates a completion of DMA cycle (Stop Pointer equal to the appropriate address pointers). **NOTE**: READ ONLY. |
| Bit 6 | ENABLE INITIATOR: Set to assert EI* output. |
| Bit 7 | ENABLE TARGET: Set to assert ET* output. |

## 5.3 54H – Buffer Size (Read/Write)




00H = 256 BYTES BUFFER
01H = 512 BYTES BUFFER
03H = 1K BYTES BUFFER
07H = 2K BYTES BUFFER
0FH = 4K BYTES BUFFER
1FH = 8K BYTES BUFFER
3FH = 16K BYTES BUFFER
7FH = 32K BYTES BUFFER
FFH = 64K BYTES BUFFER

## 5.4 55H – Address Mode Control (Read/Write)

| | |
|---|---|
| Bit 0 | EXTENDED ADDRESS MODE: When set extends the direct address range to 16 K bytes by allowing A10-A13 to be brought out to pin 17, pin 29, pin 30, and pin 31 respectively. |
| Bits 1-7 | NOT USED: Status indeterminate. |

## 5.5 59H – Reset Control (Write Only)

| | |
|---|---|
| Bit 0 | RESET: When set, holds all registers in reset state until this bit is reset. Assertion of RST* pin will also set this bit. |
| Bits 1-7 | NOT USED: Status indeterminate. |

**NOTE**: Any Write to the Reset Control register will reset RAP, WAP, and SP registers. If external address latches are used, they will not be reset. Write 00H to the high order byte of the above mentioned RAP/WAP registers to reset the corresponding external latches.

## 5.6 5AH – Read Address Pointer (RAP) [0:7] (Read/Write)

| | |
|---|---|
| Bit 0-7 | ADDRESS: Low order byte of the Read Address Pointer. |

## 5.7 5BH – Read Address Pointer (RAP) [8:15] (Read/Write)

| | |
|---|---|
| Bit 8-15 | ADDRESS: High order byte of the Read Address Pointer. |

## 5.8 5CH – Write Address Pointer (WAP) [0:7] (Read/Write)

| | |
|---|---|
| Bit 0-7 | ADDRESS: Low order byte of the Write Address Pointer. |

## 5.9 5DH – Write Address Pointer (WAP) [8:15] (Read/Write)

| | |
|---|---|
| Bit 8-15 | ADDRESS: High order byte of the Write Address Pointer. |

## 5.10 5EH – Stop Pointer (SP) [0:7] (Read/Write)

| | |
|---|---|
| Bit 0-7 | ADDRESS: Low order byte of the Stop Pointer. |

## 5.11 5FH – Stop Pointer (SP) [8:15] (Read/Write)

| | |
|---|---|
| Bit 8-15 | ADDRESS: High order byte of the Stop Pointer. |

## 6. OP COMMAND SEQUENCES

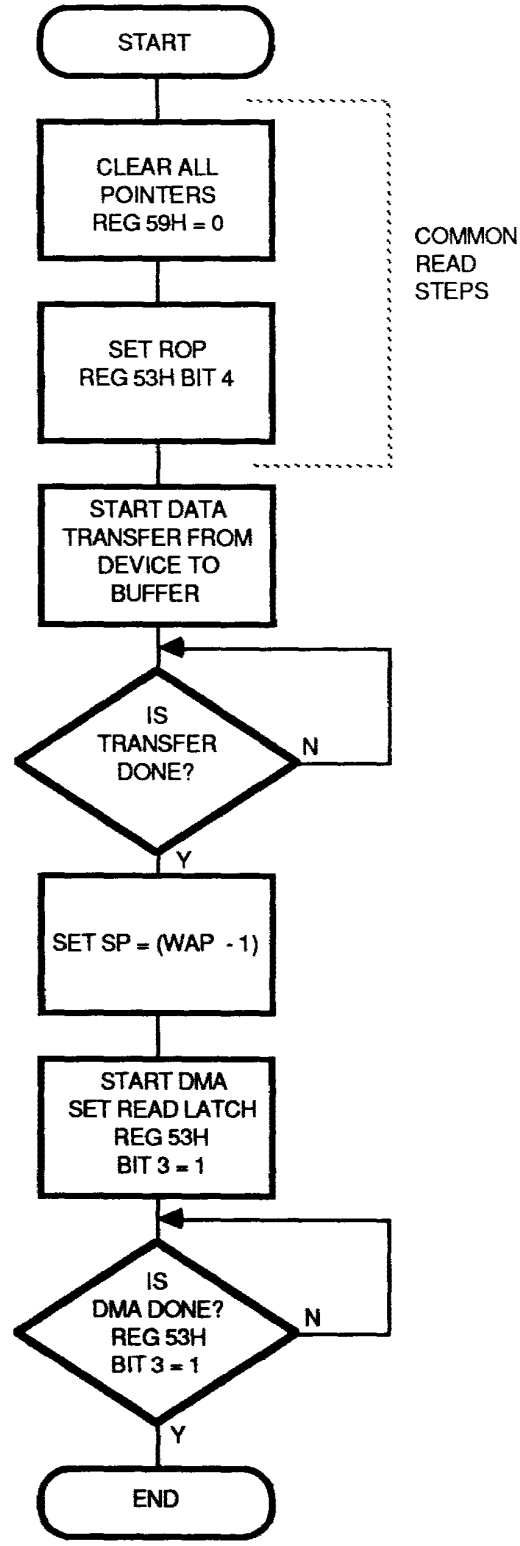
A detailed description of the data transfers in two fundamental CL–SH120 operations follows:

Read - Single Block and Multiple Block
Write - Single Block and Multiple Block

### 6.1 Single Block Read

- Clear all pointers (set Register 59H to 0). When in the Multiplex Address mode, write 0 to both Registers 5BH and 5DH to clear the external address latches.
- Initiate the read operation by setting the ROP bit (Register 53H, Bit 4).
- Transfer data from device to buffer (WAP will increment on each byte transfer).
- At the completion of the transfer from the device, set SP to (WAP-1) and set read latch for DMA operation (Register 53H, Bit 3). RAP will increment after the completion of each Req/Ack Handshake cycle.
- Monitor DMA Done bit (Register 53H, Bit 5) for the completion of the DMA transfer (RAP equals to SP).

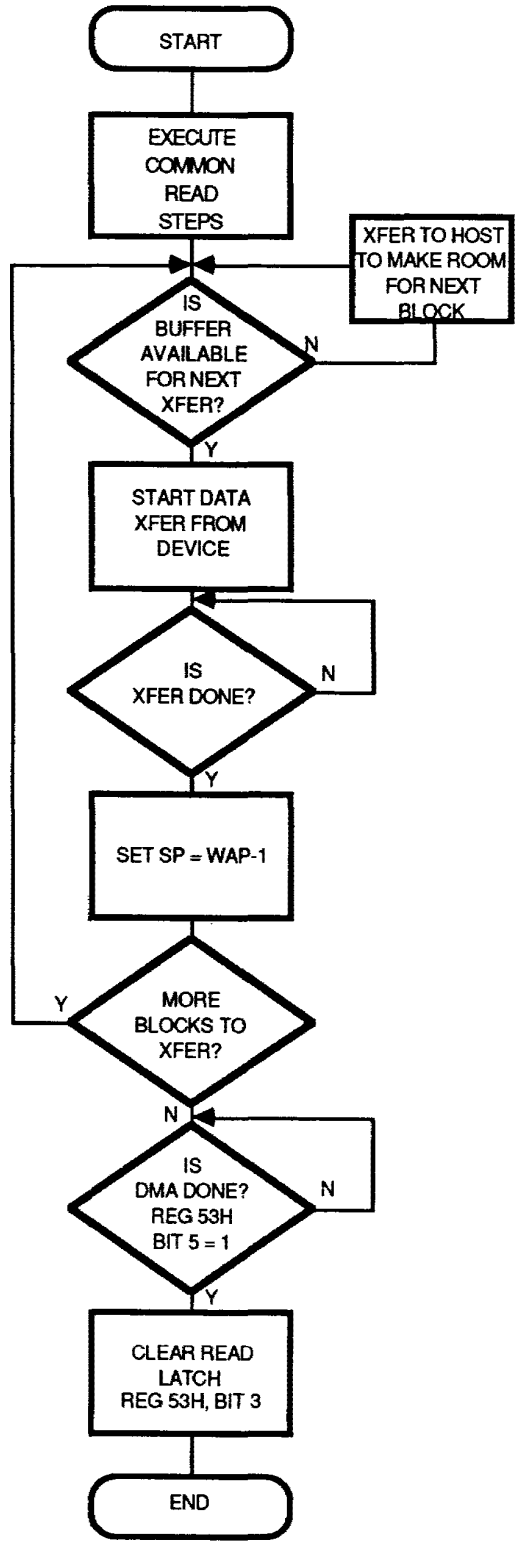
NOTE: In the multiplexed addressing mode the ROP/WOP bit (Register 53H, bit 4) must be set to a ONE prior to loading the RAP/WAP registers.



## 6.2 Multiple Block Read

- Repeat the first four of "Single Block Read."
- Read RAP to ensure that the next block may be transferred from the device without over - running the RAP.
- Begin transfer of next block to buffer (WAP will increment on each byte transfer).
- At end of transfer, set SP to new (WAP-1).
- A restart of the DMA transfer will occur as soon as the new SP address is set.
- Return to step two if more blocks are to be transferred.
- Wait for DMA Done bit (Register 53H, Bit 5) and clear Read Latch bit (Register 53H, Bit 3).

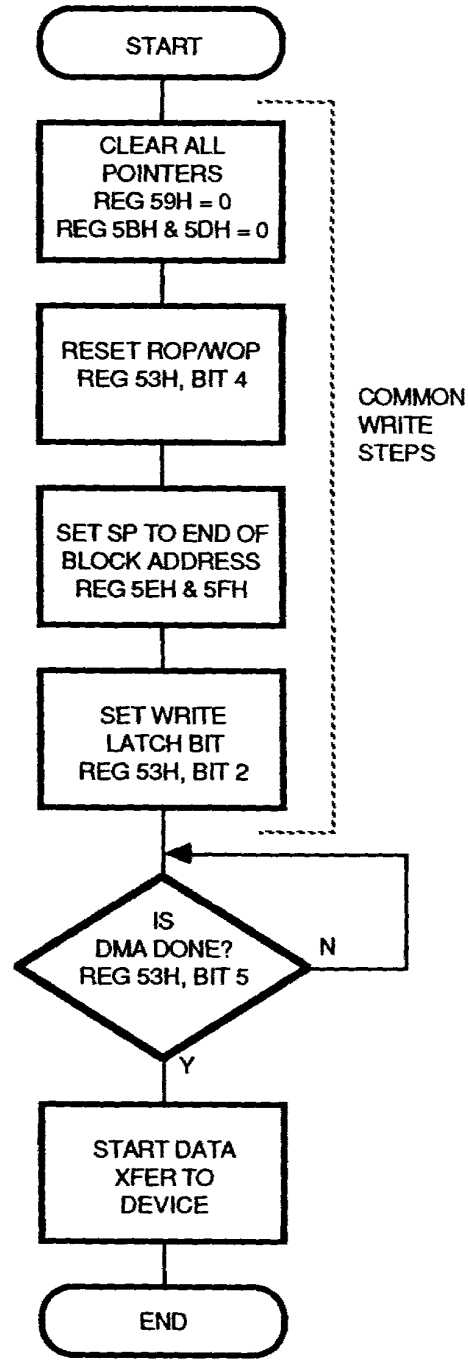
NOTE: In the multiplexed addressing mode the ROP/WOP bit (Register 53H, bit 4) must be set to a ONE prior to loading the RAP/WAP registers.



## 6.3 Single Block Write

- Clear all pointers (Register 59H to 0). In the Multiple Address mode, also write 0 to both Registers 5BH and 5DH to clear the external address latches.
- Reset ROP/WOP bit in DMA Control Register (Register 53H, Bit 4).
- Set SP to the address at the end of the block to be transferred.
- Set the Write Latch bit in DMA Control Register (Register 53H, Bit 2). This will cause the DMA cycle to begin.
- Monitor DMA done bit (Register 53H, Bit 5) to determine when DMA transfer is complete (WAP equals SP).
- Transfer to device can now proceed.

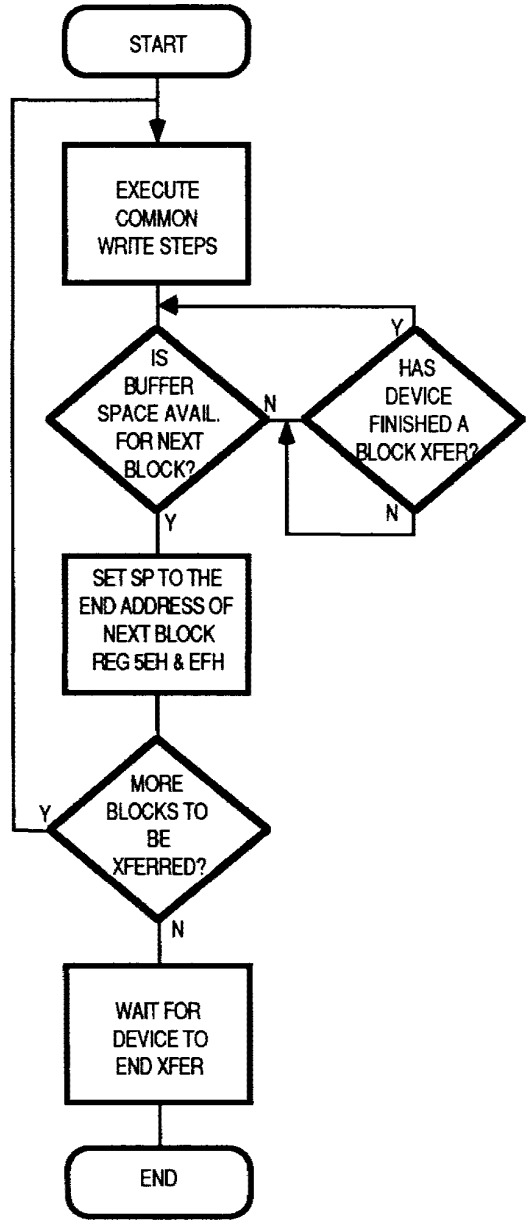
NOTE: In the multiplexed addressing mode the ROP/WOP bit (Register 53H, bit 4) must be reset to ZERO prior to loading the RAP/WAP registers.



## 6.4 Multiple Block Write

- Repeat the first five steps of a Single Block Write.
- Begin block transfer to device.
- Check if there is enough buffer for the next block without overrunning the RAP. If buffer space is available, set SP to end of next block address.
- This will clear the DMA Done Bit and renew DMA transfer.

NOTE: In the multiplexed addressing mode the ROP/WOP bit (Register 53H, bit 4) must be reset to ZERO prior to loading the RAP/WAP registers.



## 7. ELECTRICAL SPECIFICATIONS

### 7.1 Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... -65° C to 150° C
Voltage On Any Pin With Respect To Ground ..... GND-0.5 to VCC+0.5 Volts
Power Dissipation ..... 0.500 Watt
Power Supply Voltage ..... 7 Volts
Injection Current (Latch-up) ..... 100 mA

**NOTE**: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maxi - mum rating conditions for extended periods may affect device reliability.

### 7.2 D.C. Characteristics (VCC= 5V±5%, TA= 0° to 70° C, unless otherwise specified)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| VCC | Power Supply Voltage | 4.75 | 5.25 | V | Operating |
| VIL | Input Low Voltage | -0.5 | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | VCC+0.5 | V | |
| VOL | Output Low Voltage | | 0.4 | V | IOL=2mA |
| VOH | Output High Voltage | 2.4 | | V | IOH=400µA |
| ICCS | Standby Supply Current | | 200 | µA | All Inputs at GND or VCC |
| ICC | Operating Supply Current | | 50 | mA | @ 5.25V |
| IL | Input Leakage | -10 | 10 | µA | 0<VIN<VCC |
| CIN | Input Capacitance | | 10 | pf | |
| COUT | Output Capacitance | | 10 | pf | |

### 7.3 A.C. Characteristics

The following timings are operating under the assumption that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are conforming to the operating ranges of power supply voltage of 5V +/-5% and ambient temperature of 0C to 70C.

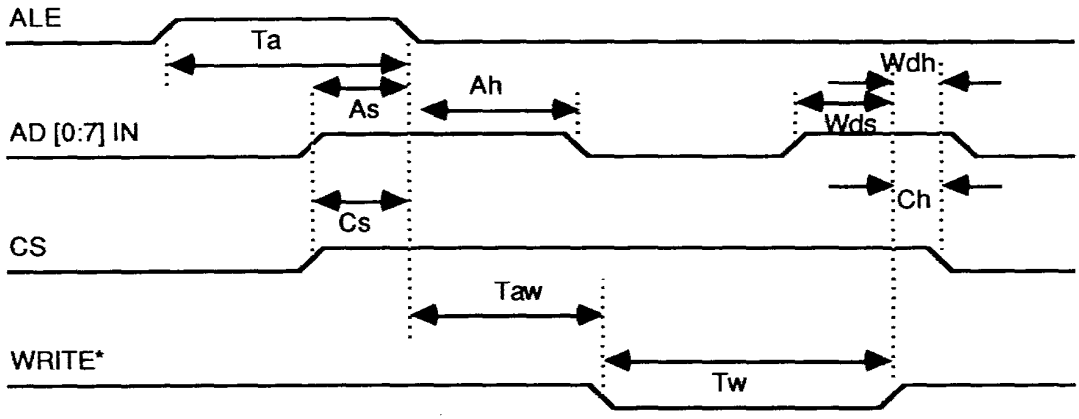
**CL – SH 120 Microprocessor Interface Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| Ta | ALE Width | 45 | | ns |
| Taw | ALE⬇ to WRITE* ⬇ | 25 | | ns |
| Tar | ALE⬇ to READ* ⬇ | 25 | | ns |
| Tw | WRITE* Width | 200 | | ns |
| Tr | READ* Width | 200 | | ns |
| As | Address valid to ALE⬇ | 7.5 | | ns |
| Ah | ALE⬇ to Address invalid | 20 | | ns |
| Cs | CHIP SELECT valid to ALE⬇ | 7.5 | | ns |
| Ch | READ*⬆ or WRITE*⬆ to CS⬇ | 0 | | ns |
| Wds | Write Data valid to WRITE*⬆ | 70 | | ns |
| Wdh | WRITE*⬆ to Write Data invalid | 10 | | ns |
| Tda | READ*⬇ to Read Data valid | | 145 | ns |
| Tdh | READ*⬆ to Read Data invalid | | 50 | ns |

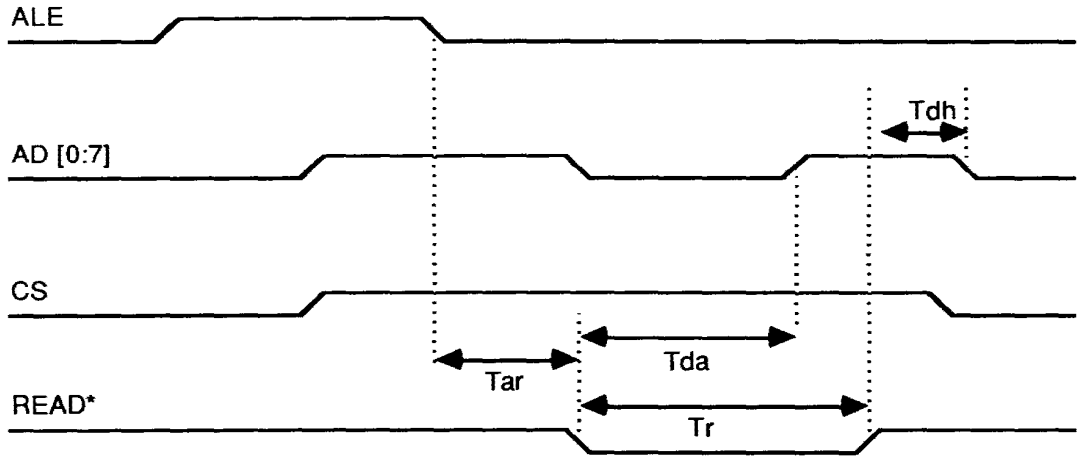
**NOTE:** ⬇ Indicates falling edge. ⬆ Indicates rising edge.

**CL – SH 120 Microprocessor Interface Timing**

**Register Write Timing**




**Register Read Timing**

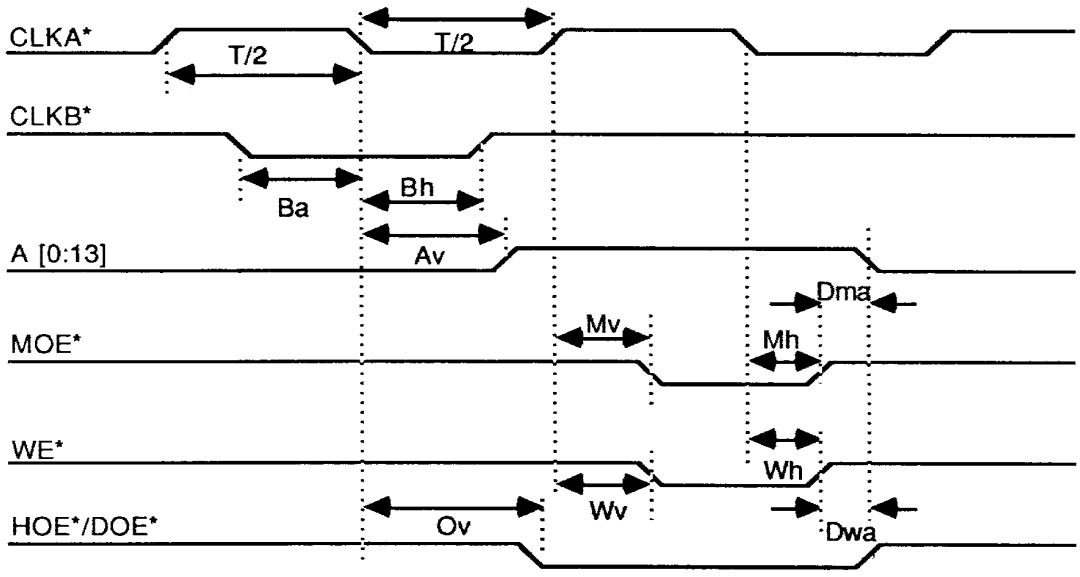


**CL – SH 120 Buffer RAM Interface Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| T/2 | CLKA* Half Cycle | 100 | | ns |
| Ba | CLKB*⬇ to CLKA* ⬇ Set Up | 30 | | ns |
| Bh | CLKA*⬇ to CLKB* ⬆ Hold | 30 | | ns |
| Av | CLKA*⬇ to Address Stable | | 100 | ns |
| Dwa | WE*⬆ to Address Hold | 10 | 40 | ns |
| Mv | CLKA*⬆ to Asserted MOE* | | 40 | ns |
| Mh | CLKA*⬇ to Deasserted MOE* | 10 | 40 | ns |
| Wv | CLKA*⬆ to Asserted WE* | | 40 | ns |
| Wh | CLKA*⬇ to Deasserted WE* | 10 | 40 | ns |
| Dma | Deasserted MOE* to Address Hold | 10 | 40 | ns |
| Ov | CLKA*⬇ to Asserted HOE*/DOE* | | 100 | ns |

**NOTE:** ⬇ Indicates falling edge. ⬆ Indicates rising edge.

**CL – SH 120 Buffer RAM Interface Timing**

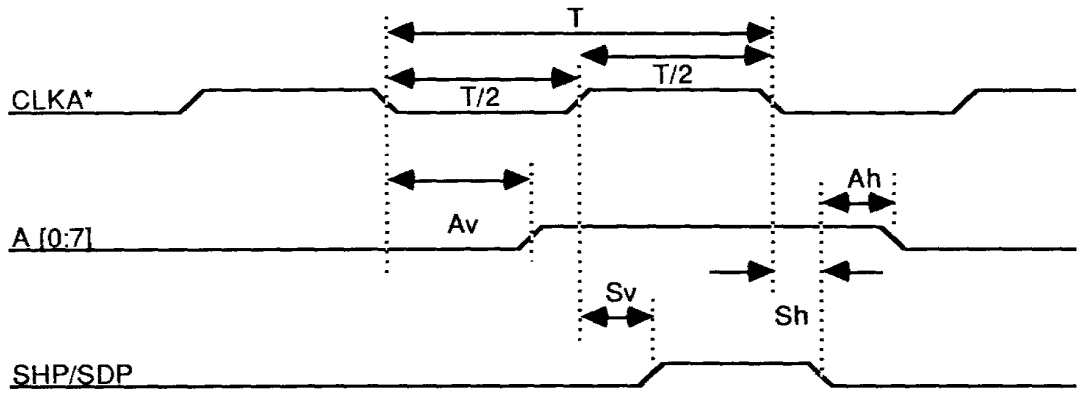


**CL – SH 120 Buffer RAM Multiplexed Address Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| T | CLKA* Period | 200 | | ns |
| T/2 | CLKA* Assert/Deassert | 95 | | ns |
| Av | CLKA*⬇ to Address valid | | 100 | ns |
| Sv | CLKA*⬆ to Asserted SHP/SDP | | 40 | ns |
| Sh | CLKA*⬇ to Deasserted SHP/SDP | | 40 | ns |
| Ah | Address Hold from SHP/SDP⬇ | 10 | 40 | ns |

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

**CL – SH 120 Buffer RAM Multiplexed Address Timing**

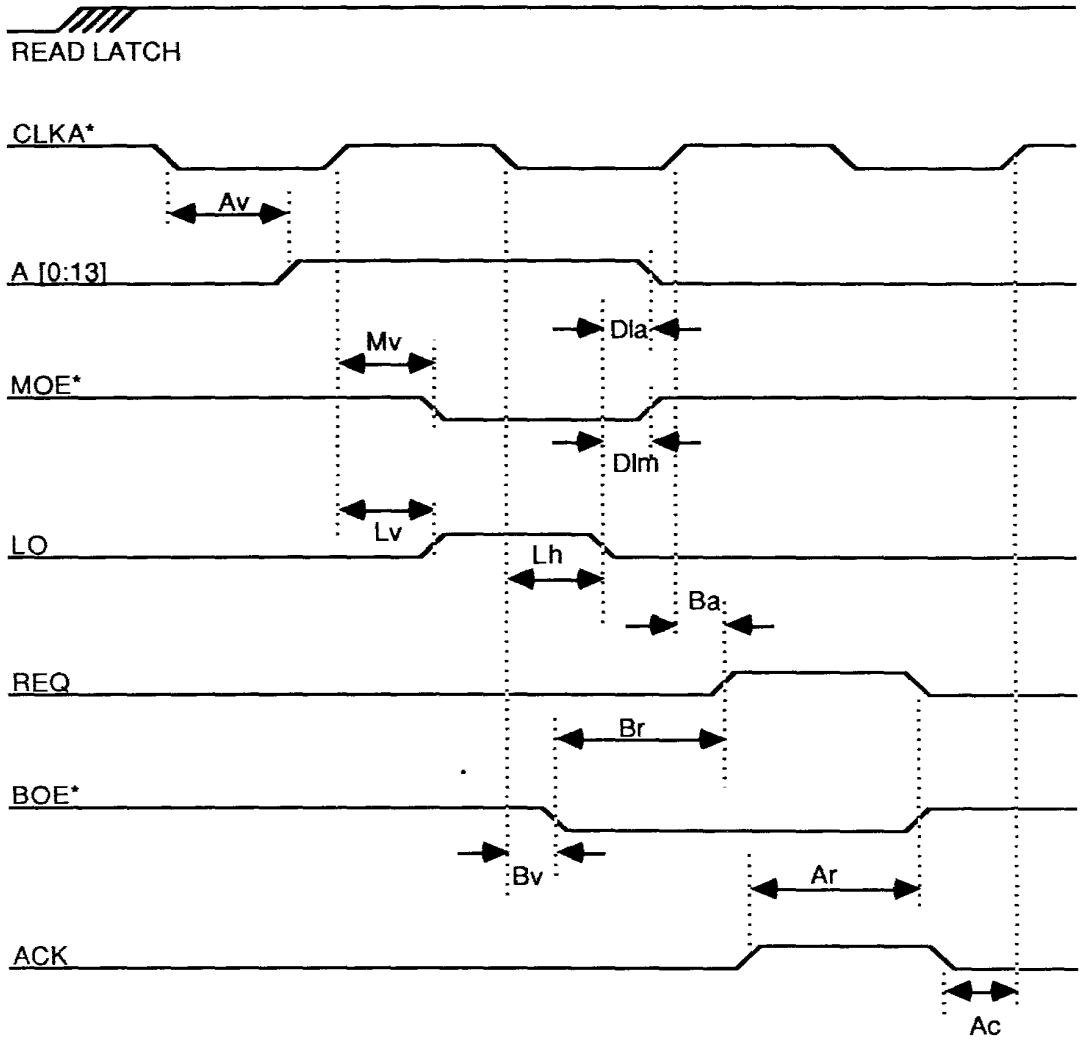


**CL – SH 120 Buffer-to-Host Interface Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| Av | CLKA*⬇ to Address Valid | | 100 | ns |
| Dla | LO⬇ to Address Hold | 10 | 40 | ns |
| Mv | CLKA*⬆ to Asserted MOE* | | 40 | ns |
| Dlm | LO⬇ to Deasserted MOE* | 10 | 40 | ns |
| Lv | CLKA*⬆ to Asserted LO | | 40 | ns |
| Lh | CLKA*⬇ to Deasserted LO | | 40 | ns |
| Bv | CLKA*⬇ to Asserted BOE* | | 40 | ns |
| Ba | CLKA*⬆ to Asserted Req | | 40 | ns |
| Br | BOE*⬇ to Asserted Req | 70 | | ns |
| Ar | ACK⬆ to Deasserted Req | | 40 | ns |
| Ac | ACK⬇ to CLKA* ⬆ Set Up | | 35 | ns |

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

**CL – SH 120 Buffer-to-Host Interface Timing**



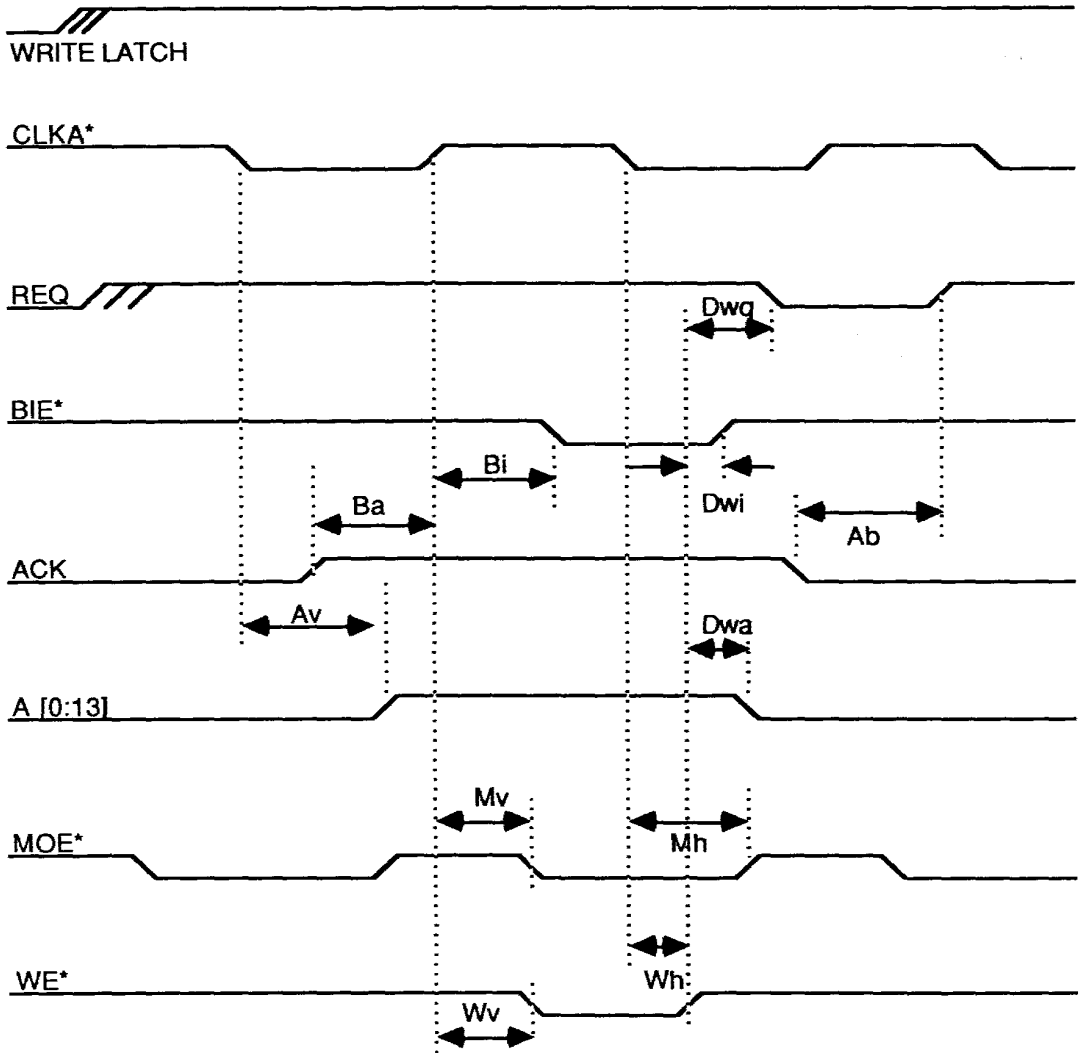

**NOTE:** MOE* will be continuously asserted every CLKA*⬆ while waiting for ACK⬆.

**CL – SH 120 Host-to-Buffer Interface Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| Av | CLKA*⬇ to Address valid | | 100 | ns |
| Bi | CLKA*⬆ to Asserted BIE* | | 40 | ns |
| Dwq | WE*⬆ to Deasserted REQ | 10 | 40 | ns |
| Ba | ACK⬆ to CLKA*⬆ Set Up | 40 | | ns |
| Dwa | WE*⬆ to Address Hold | 10 | 40 | ns |
| Mv | CLKA*⬆ to Asserted MOE* | | 40 | ns |
| Mh | CLKA*⬇ to Deasserted MOE* | | 40 | ns |
| Wv | CLKA*⬆ to Asserted WE* | | 40 | ns |
| Wh | CLKA*⬇ to Deasserted WE* | | 40 | ns |
| Ab | ACK⬇ to Asserted REQ | | 60 | ns |
| Dwi | WE*⬆ to Deasserted BIE* | 10 | 40 | ns |

NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

**CL – SH 120 Host-to-Buffer Interface Timing**




**NOTE:** MOE* and WE* will be continuously asserted every CLKA*⬆ while waiting for ACK⬆.

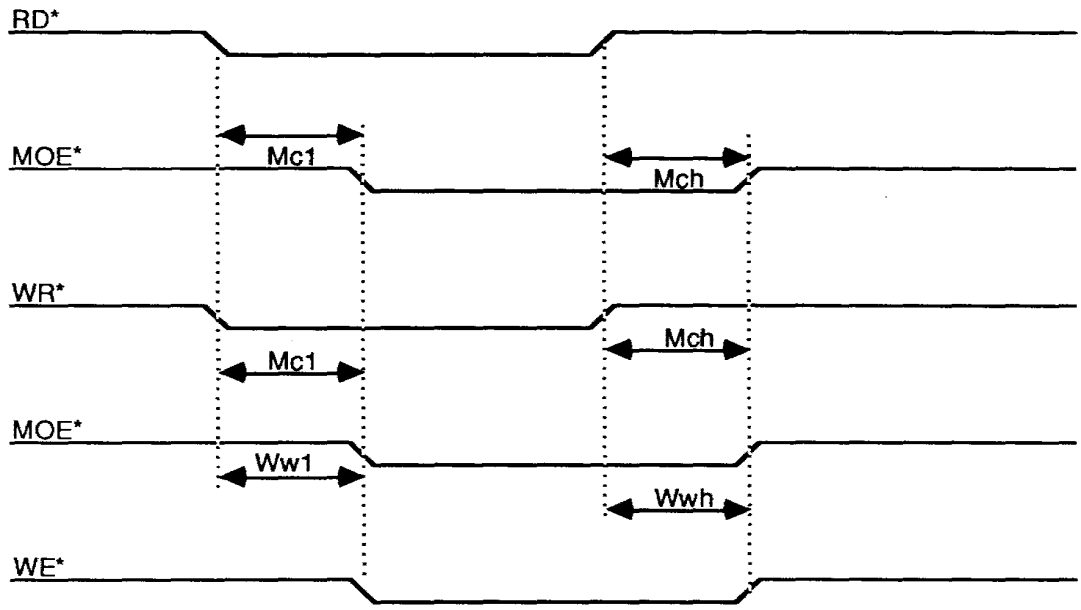
**CL – SH 120 Register 70H Timing Table**

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| Mcl | RD*⬇ or WR*⬇ to Asserted MOE* | | 40 | ns |
| Mch | RD*⬆ or WR*⬆ to Deasserted MOE* | | 40 | ns |
| Wwl | WR*⬇ to Asserted WE* | | 40 | ns |
| Wwh | WR*⬆ to Deasserted WE* | | 40 | ns |

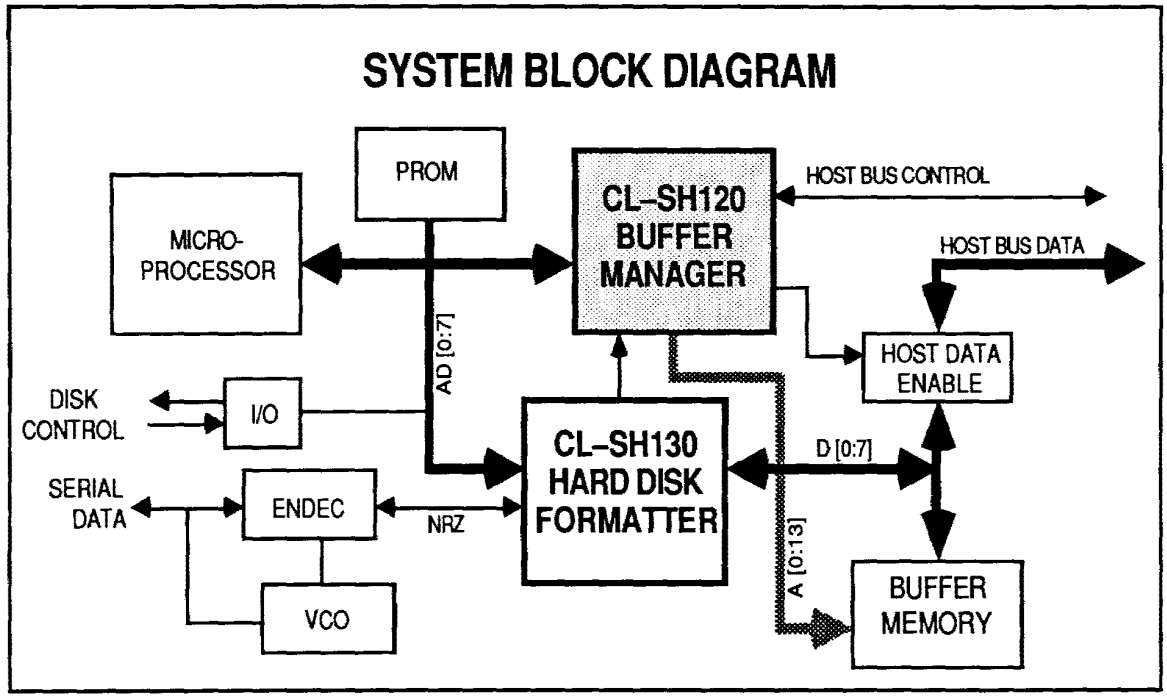
NOTE: ⬇ Indicates falling edge. ⬆ Indicates rising edge.

NOTE: Address [0:13] in the Extended Address Mode is valid according to ROP/WOP and the con - tents of RAP/WAP.

**CL – SH 120 Register 70H Timing**

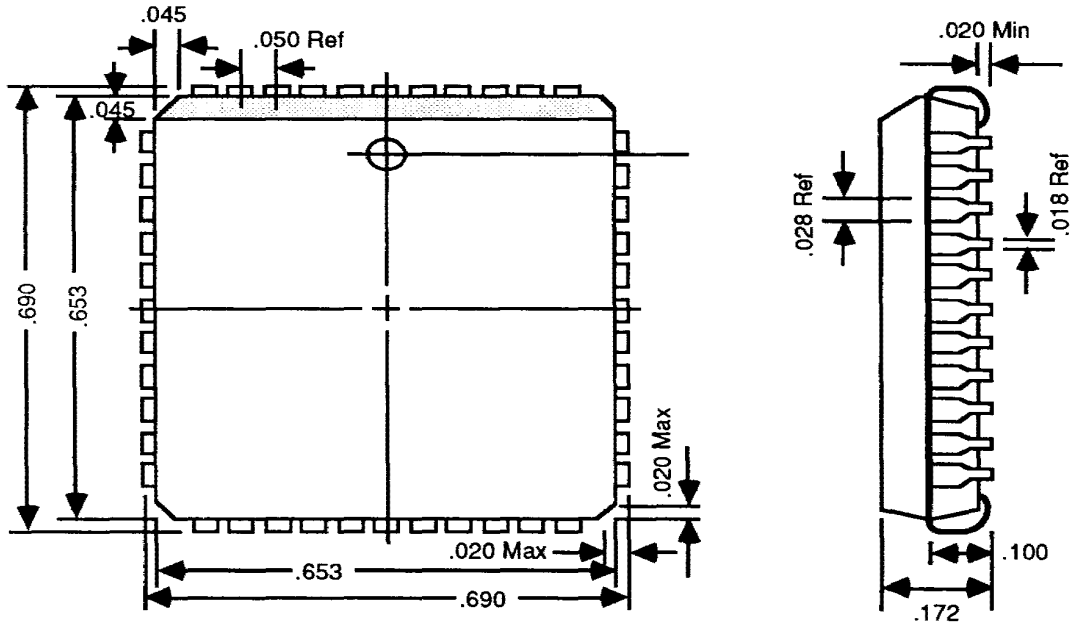


## 8. TYPICAL APPLICATION



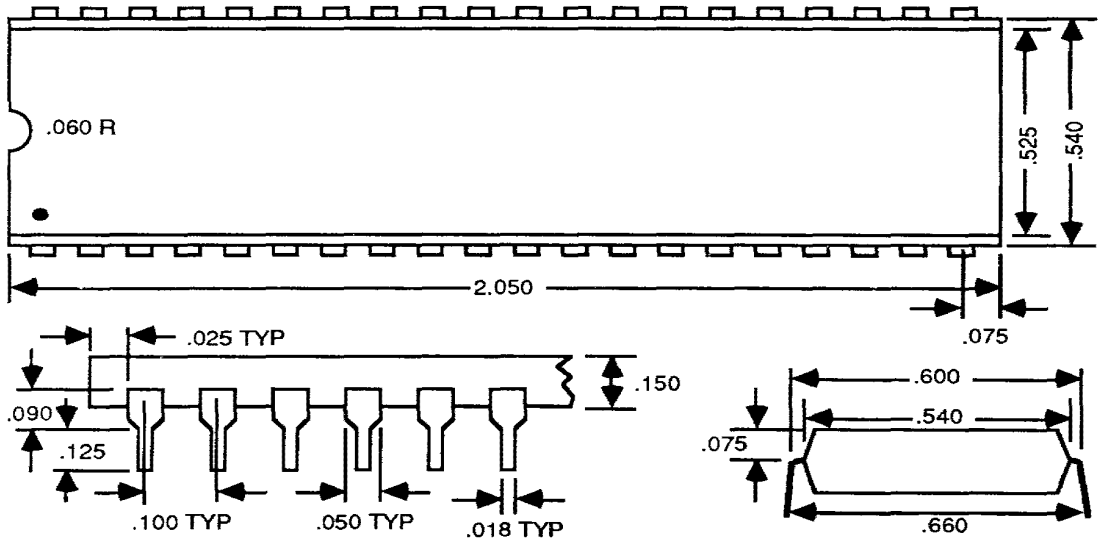
## 9. SAMPLE PACKAGES

### 9.1 44-Pin PLCC



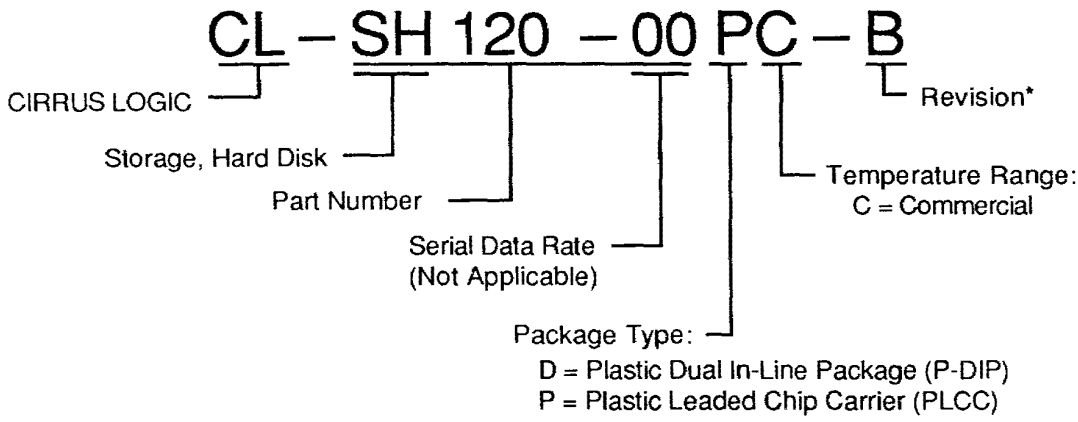

All dimensions are in inches and are nominal unless otherwise stated.

### 9.2 40-Pin P-DIP



## 10. ORDERING INFORMATION

### CIRRUS LOGIC Numbering Guide




* Contact CIRRUS LOGIC for up-to-date information on Revisions.

## ABOUT CIRRUS LOGIC

CIRRUS LOGIC makes proprietary VLSI circuits in three product lines. The CD line is Data Communications circuits, the SH line is Hard Disk Controllers, and the GD line is Graphics Display Controllers.

A variety of redefinable products are offered in each line. These are not "standard products." Through the Redefinable IC CIRRUS LOGIC provides a unique solution that is custom-tailored to your system requirements. You are invited to start with our Data Sheet, and consider changes you would like to see in order to provide an optimal component for your system product. CIRRUS LOGIC will supply you the exact IC that your system requires.

It is more than a "standard product." You will receive a VLSI circuit that is specific to your application. But you are relieved of the burden of specifying and designing the IC. If you can critique a data sheet, you can have a custom VLSI component.

Our own internally developed proprietary silicon compilation technology* makes it possible for us to offer this level of VLSI product for the first time.

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* U.S. Patent No. 4,293,783







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