9400 SERIES MACROLOGIC™

COMPOSITE DATA SHEET

GENERAL DESCRIPTION – Fairchild 9400 Series TTL MACROLOGIC utilizes advanced Schottky technology to provide high performance peripheral and processor oriented LSI. The design of 9400 ensures maximum deisgn flexibility with no performance loss. The MACROLOGIC elements may be used with any bit length, instruction set or organization. Devices may be expanded with little or no extra components. Where applicable, bus oriented, 3-state outputs are provided. A new slim 24-pin package reduces PC board real estate by a third.

- 150–250 GATE COMPLEXITY
- COMPATIBLE WITH ALL TTL FAMILIES
- PERFORMANCE EQUIVALENT TO SCHOTTKY IMPLEMENTATION
- 14, 16, 18, AND SLIM 24-PIN PACKAGES
- INPUTS ABOUT 1/4 NORMAL TTL LOAD, i.e., 360–400 μA
- OUTPUTS DRIVE 16 mA (10U.L.) OR 8mA (5U.L.) DEPENDING ON APPLICATION
- DESIGNED FOR MAXIMUM FLEXIBILITY
- OPERATES OVER COMMERCIAL OR MILITARY TEMPERATURE RANGE

ADVANCED SCHOTTKY PROCESS

The 9400 family uses an advanced Schottky TTL process to obtain the best speed/power product of any commercially available digital bipolar circuitry. Key characteristics are as follows:

- SHALLOW, LOW CAPACITANCE DIFFUSION TO PROVIDE TRANSISTOR f_T OF 2 GHz
- SCHOTTKY DIODES TO ELIMINATE STORAGE TIME
- INTERNAL GATES
  - –30 mils^2 (50 GATES PER mm^2)
  - –4 ns DELAY
  - –6.0 pJ DELAY POWER PRODUCT
- OUTPUT BUFFERS
  - –70 mils^2
  - –6 ns DELAY
  - –10 pJ DELAY POWER PRODUCT

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD SEMICONDUCTOR

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Manufactured under one or more of the following U.S. Patents: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; other patents pending.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	XM			XC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Ambient Temperature Range	−55	25	125	0	25	75	°C

D for Ceramic Dip, P for Plastic Dip.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC}
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IH} Input current HIGH – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} Input current LOW – The current flowing into an input when a specified LOW voltage is applied.

I_{OH} Output current HIGH – The current flowing into the output with a specified HIGH output voltage (V_{OH}) applied.

I_{OL} Output current LOW – The current flowing into the output with specified LOW output voltage (V_{OL}) applied.

I_{OS} Short circuit output current – The current flowing into an output when that output is short circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} Output off current HIGH – The current flowing into a disabled 3-state output with a specified HIGH output voltage (V_{OH}) applied.

I_{OZL} Output off current LOW – The current flowing into a disabled 3-state output with a specified LOW output voltage (V_{OL}) applied.

I_{CC} Supply current – The current flowing into the V_{CC} supply terminal of a circuit when the inputs are open.

VOLTAGES – All voltages are referenced to ground.

V_{IH} Input HIGH voltage – The range of input voltages that represents a logic HIGH in the system.

V_{IL} Input LOW voltage – The range of input voltages that represents a logic LOW in the system.

V_{IH}(MIN) Minimum input voltage HIGH – The minimum allowed input HIGH in a logic system.

V_{IL}(MAX) Maximum input voltage LOW – The maximum allowed input LOW in a system.

V_{OH} Output voltage HIGH – The range of voltages at an output terminal for specified output current I_{OH}. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} Output voltage LOW – The range of voltages at an output terminal for specified output current I_{OL}. Device inputs are conditioned to establish a LOW level at the output.

V_{CD} Input clamp diode voltage – The range of negative voltage applied to an input which will cause −18 mA to flow into the device.

V_{CC} Supply voltage – Typically 5 V.

AC SWITCHING PARAMETERS

f_{MAX}	Toggle frequency/operating frequency — The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.
t_{PLH}	Propagation delay time — The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW to the defined HIGH.
t_{PHL}	Propagation delay time — The time between the specified reference, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH to the defined LOW.
t_w	Pulse Width — The time between 1.3 V amplitude points on the leading and trailing edges of pulse.
t_h	Hold time — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_s	Set-up time — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{PHZ}	Output disable time (of a 3-state output) from HIGH level — The time between the 1.3 V levels on the input and output voltage waveforms with the 3-state output changing from the defined HIGH to a high-impedance (off) state.
t_{PLZ}	Output disable time (of a 3-state output) from LOW level — The time between the 1.3 V levels on the input and output voltage waveforms with the 3-state output changing from the defined LOW level to a high-impedance (off) state.
t_{PZH}	Output enable time (of a 3-state output) to a HIGH level — The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.
t_{PZL}	Output enable time (of a 3-state output) to a LOW level — The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.
t_{rec}	Recovery time — The time between the 1.3 V levels of inputs which will allow the device to operate correctly.

9401

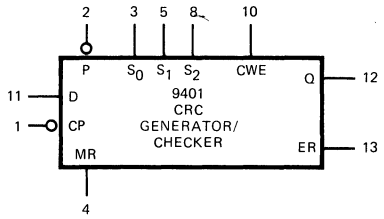
CRC GENERATOR/CHECKER

FAIRCHILD MACROLOGIC

DESCRIPTION – The 9401 Cyclic Redundancy Check (CRC) Generator/Checker provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Individual clear and preset inputs are provided for floppy disc and other applications. The Error Output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is a member of Fairchild's MACROLOGIC family and is fully compatible with all TTL families.

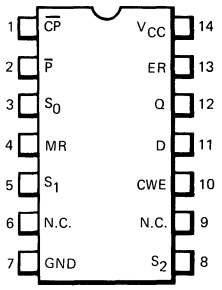
- **GUARANTEED 12 MHz DATA RATE**
- **EIGHT SELECTABLE POLYNOMIALS**
- **ERROR INDICATOR**
- **SEPARATE PRESET AND CLEAR CONTROLS**
- **AUTOMATIC RIGHT JUSTIFICATION**
- **FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES**
- **14-PIN PACKAGE**
- **TYPICAL APPLICATIONS:**
  - **FLOPPY AND OTHER DISC STORAGE SYSTEMS**
  - **DIGITAL CASSETTE AND CARTRIDGE SYSTEMS**
  - **DATA COMMUNICATION SYSTEMS**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

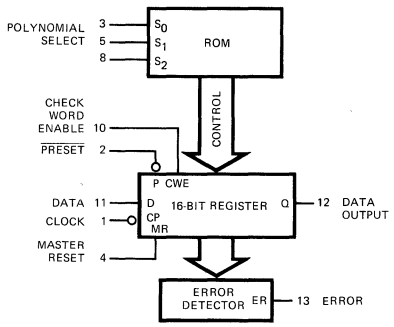
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{CC} = 14
GND = 7

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	0.5 U.L.	0.23 U.L.
D	Data Input	0.5 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH to LOW Transition) Input	0.5 U.L.	0.23 U.L.
CWE	Check Word Enable Input	0.5 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	0.5 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FUNCTIONAL DESCRIPTION – The 9401 Cyclic Redundancy Check (CRC) Generator/Checker is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the HIGH to LOW transition of the Clock Input ($\overline{CP}$). This data is gated with the most significant Output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWE Input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH to LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH. ER remains valid until the next HIGH to LOW transition of $\overline{CP}$ or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the register. A LOW on the Preset Input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage	XM & XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70	110	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 2)	MAX			
f_{max}	Maximum Clock Frequency	12	20		MHz	Fig. 3, 4, 5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation Delay, Preset to Data Output		40	60	ns		
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR or Preset to Error Output		40	60	ns		

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
$t_w\overline{CP}$ (L)	Clock Pulse Width (LOW)	35			ns	Fig. 2	C_L = 15 pF
t_sD	Set-up Time, Data to Clock		35	55	ns	Fig. 6	
t_sCWE	Set-up Time, CWE to Clock		35	55	ns		
t_h	Hold Time, Data and CWE to Clock		0		ns		
t_wP (L)	Preset Pulse Width (LOW)	35	25		ns	Fig. 4	
t_wMR (H)	Master Reset Pulse Width (HIGH)	35	25		ns	Fig. 6	
t_{rec}	Recovery Time, MR and Preset to Clock		25	35	ns	Fig. 4, 5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

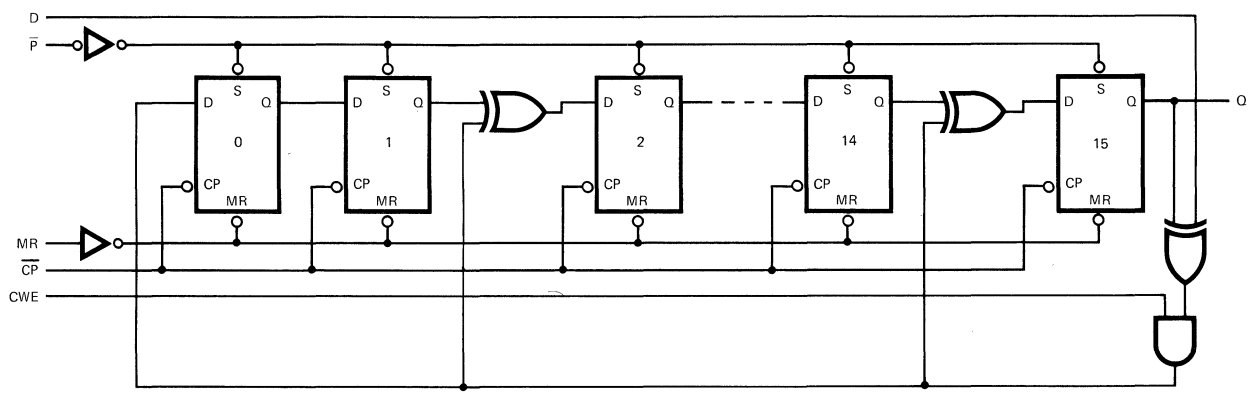
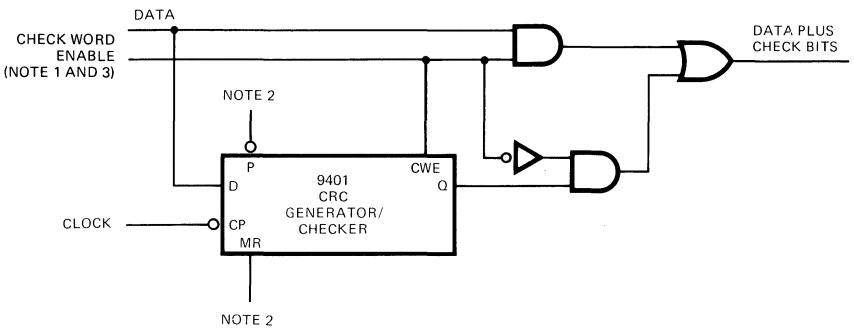


Fig. 1



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Fig. 2
CHECK WORD GENERATION

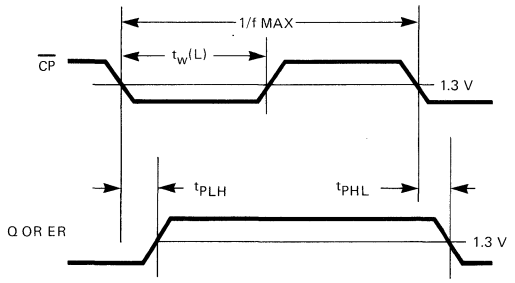


Fig. 3
PROPAGATION DELAYS,
$\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

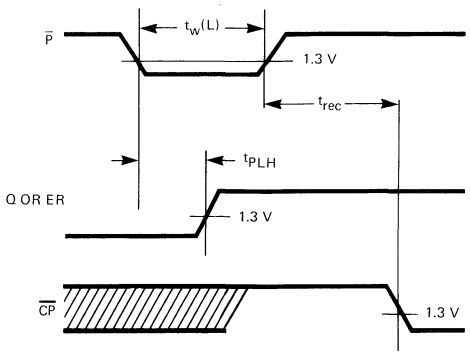


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER
PLUS RECOVERY TIME P TO $\overline{CP}$

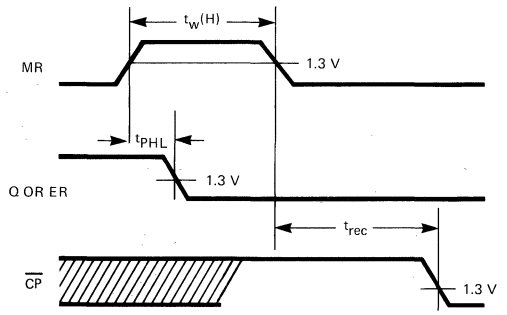


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER
PLUS RECOVERY TIME, MR TO $\overline{CP}$

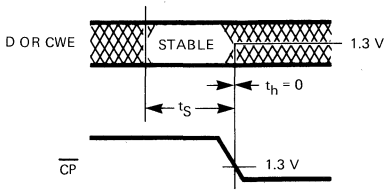


Fig. 6
SET-UP AND HOLD TIMES,
D TO $\overline{CP}$ AND CWE TO $\overline{CP}$

9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

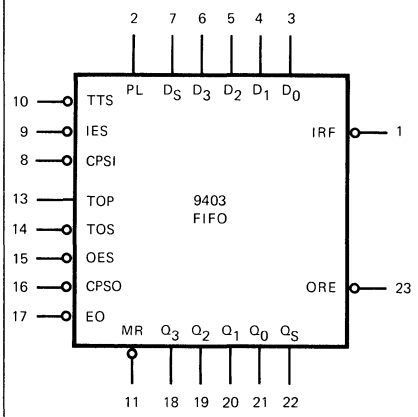
FAIRCHILD MACROLOGIC

DESCRIPTION — The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of 4). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility. It is a member of Fairchild's TTL MACROLOGIC family and is fully compatible with all TTL families.

- **14 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **24-PIN PACKAGE**

LOGIC SYMBOL



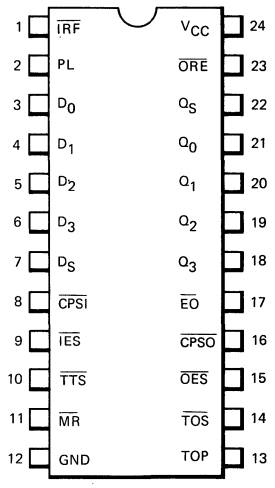
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$D_0 - D_3$	Parallel Data Inputs	0.5 U.L.	0.23 U.L.
D_S	Serial Data Input	0.5 U.L.	0.23 U.L.
PL	Parallel Load Input	0.5 U.L.	0.23 U.L.
$\overline{CPSI}$	Serial Input Clock (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$\overline{IES}$	Serial Input Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{TTS}$	Transfer to Stack Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{OES}$	Serial Output Enable Input (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)	0.5 U.L.	0.23 U.L.
TOP	Transfer Out Parallel Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CPSO}$	Serial Output Clock Input (Operates on Negative-Going Transition)	0.5 U.L.	0.23 U.L.
$Q_0 - Q_3$	Parallel Data Outputs (Note b)	130 U.L.	10 U.L.
Q_S	Serial Data Output (Note b)	10 U.L.	10 U.L.
$\overline{IRF}$	Input Register Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{ORE}$	Output Register Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

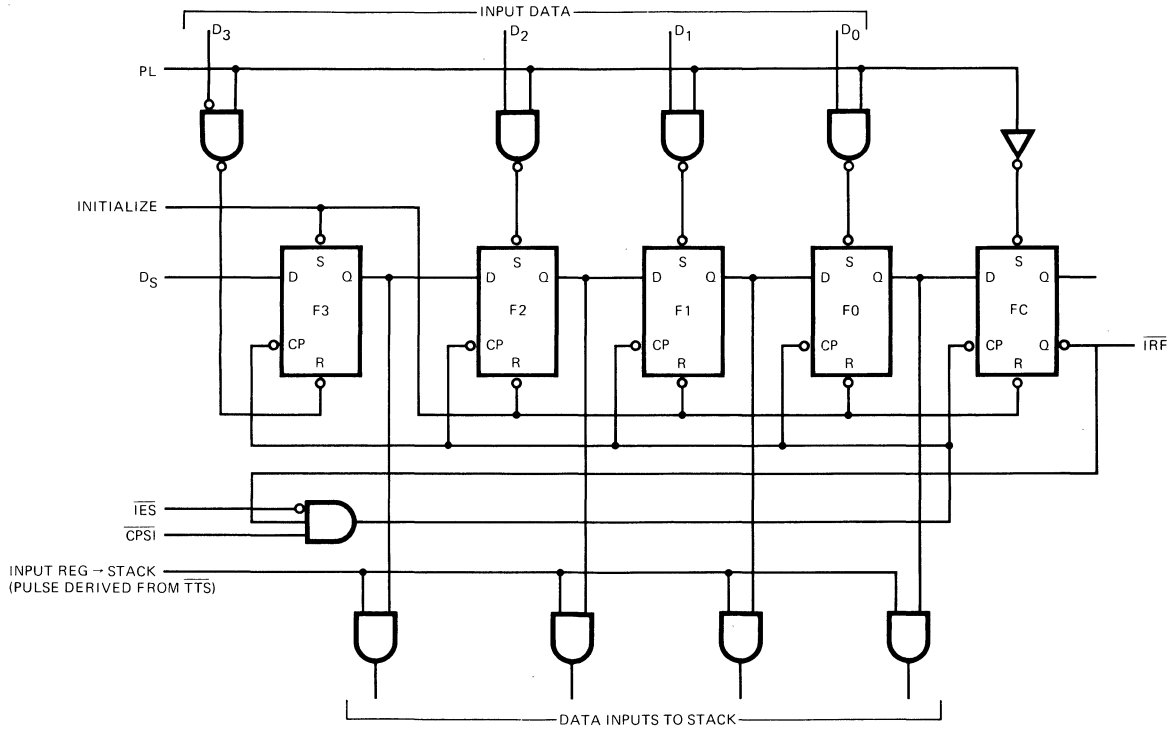


Fig. 1
CONCEPTUAL INPUT SECTION

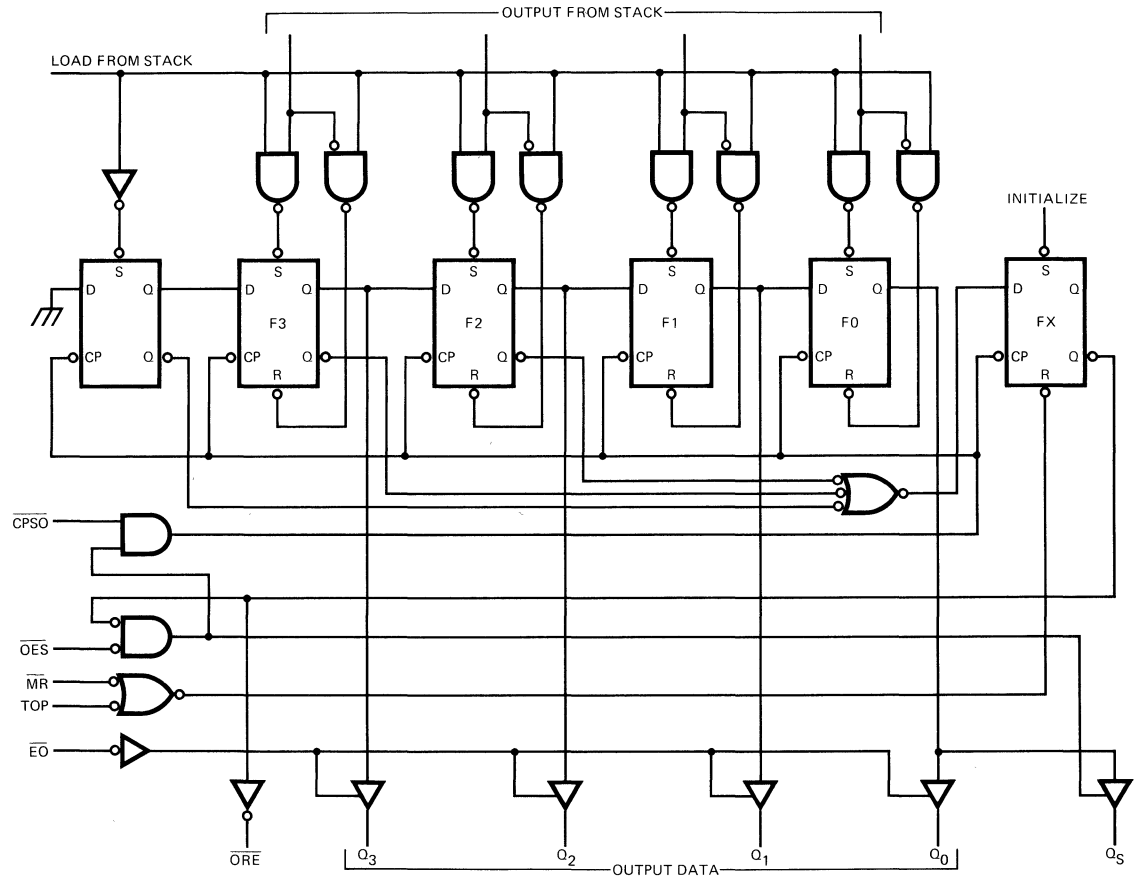
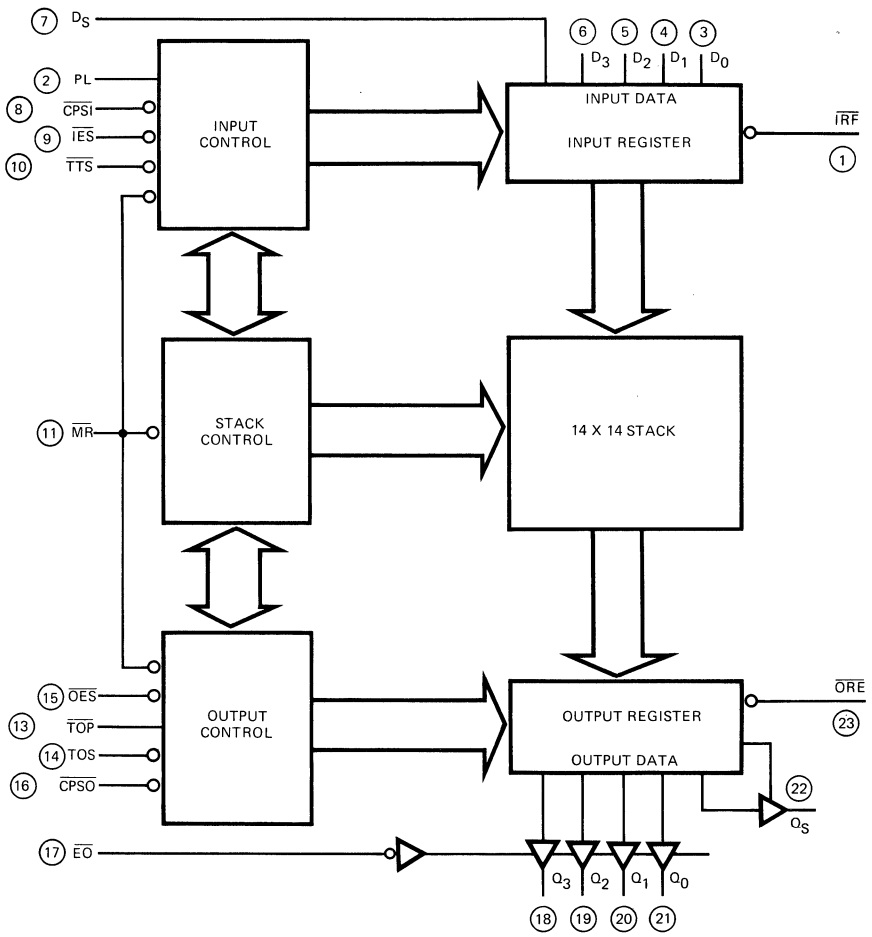


Fig. 2
CONCEPTUAL OUTPUT SECTION

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — As shown in the Block Diagram the 9403 consists of three parts:

1. An Input Register with Parallel and Serial Data Inputs as well as control inputs and outputs for input handshaking and expansion.

2. A 4-bit wide, 14-word deep Fall-Through Stack with self-contained control logic.

3. An Output Register with Parallel and Serial Data Outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):

The Input Register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the Fall-Through Stack and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 Flip-Flop and resetting the other flip-flops. The $\overline{Q}$ Output of the last Flip-Flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL Input loads the $D_0 - D_3$ Data Inputs into the F0 – F3 Flip-Flops and sets the FC Flip-Flop, which forces $\overline{IRF}$ LOW, indicating "Input Register Full". The D Inputs must be stable while PL is HIGH. During parallel entry, the $\overline{IES}$ Input should be LOW; the $\overline{CPSI}$ Input may be either HIGH or LOW.

SERIAL ENTRY:
Data on the DS Input is serially entered into the F3, F2, F1, F0, FC Shift Register on each HIGH-to-LOW transition of the $\overline{CPSI}$ Clock Input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC Flip-Flop is set, forcing $\overline{IRF}$ LOW (Input Register full) and internally inhibiting further $\overline{CPSI}$ clock pulses. Figure 3 illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B0 is the first bit, B63 the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of Flip-Flops F0 – F3 feed the Stack. A LOW level on the $\overline{TTS}$ Input attempts to initiate a "fall-through" action. If the top location of the Stack is empty, data is loaded into the Stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the Stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the Stack control section and does not clear the data.

OUTPUT REGISTER (DATA EXTRACTION):
The Output Register receives 4-bit data words from the bottom Stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

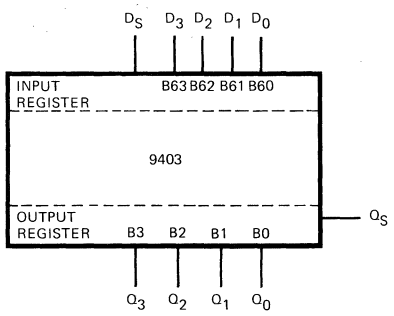


Fig. 3
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

PARALLEL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) Output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) Input is HIGH, and the $\overline{OES}$ Input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction, $\overline{TOS}$, $\overline{CPSO}$, and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:
When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom Stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial Data Output Q_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output Q_S. For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the Stack as soon as the previous one has been shifted out.

EXPANSION:

Vertical Expansion – The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does ot sacrifice any of the FIFO's flexibility for serial/parallel input and output.

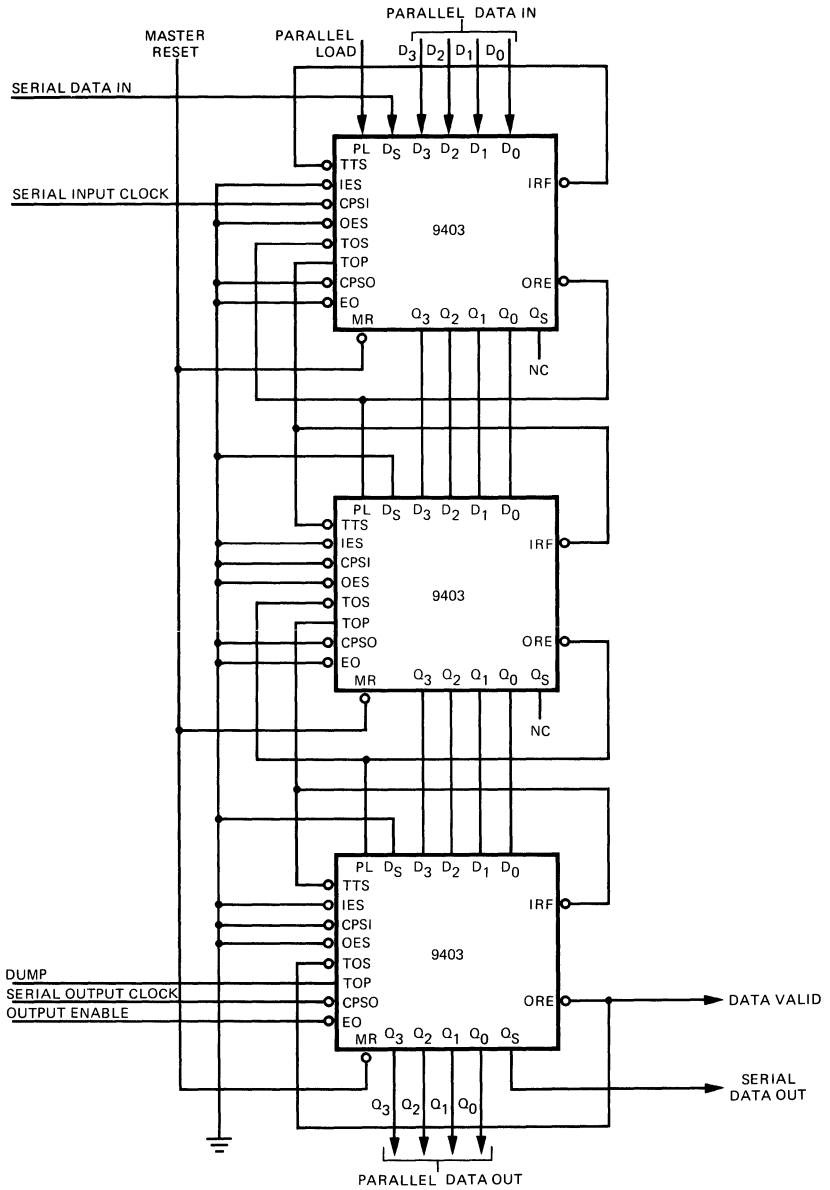


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 may also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 X n bits can be constructed. When expanding in the horizontal direction, it is usual to connect the $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$ outputs of the right most device (most significant device) to the $\overline{\text{TTS}}$ and $\overline{\text{TOS}}$ inputs respectively of all devices to the left (less significant devices) to guarantee that no operation is initiated before all devices are ready.

As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the FIFO's flexibility for serial/parallel input and output.

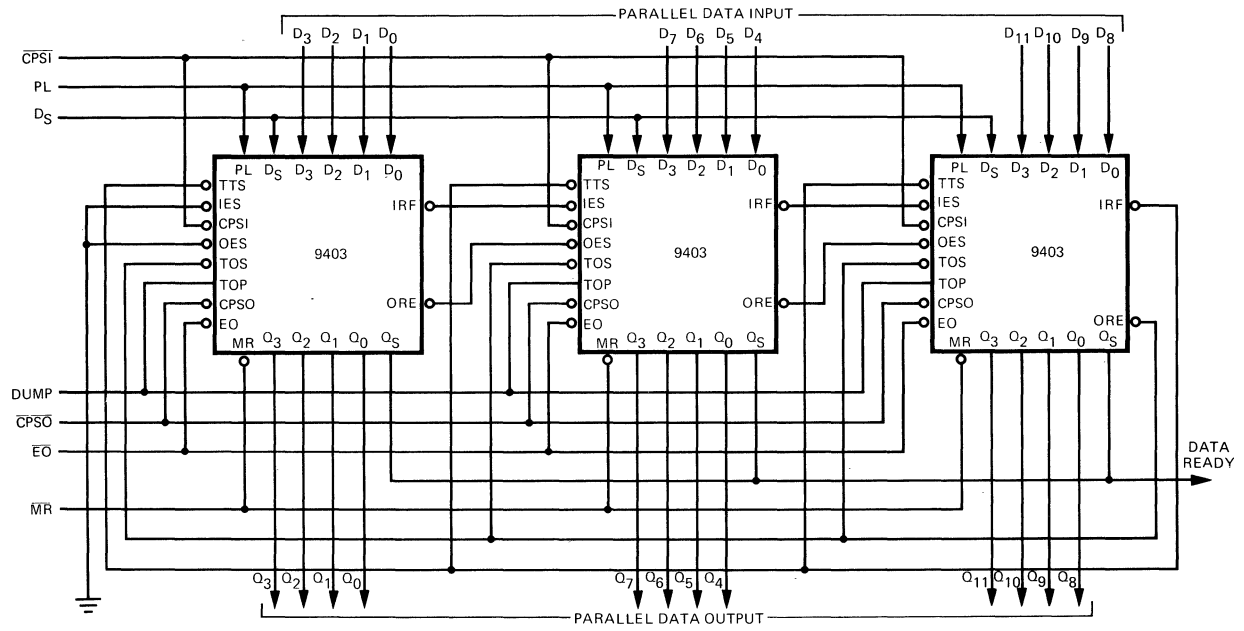


Fig. 5
A HORIZONTAL EXPANSION SCHEME

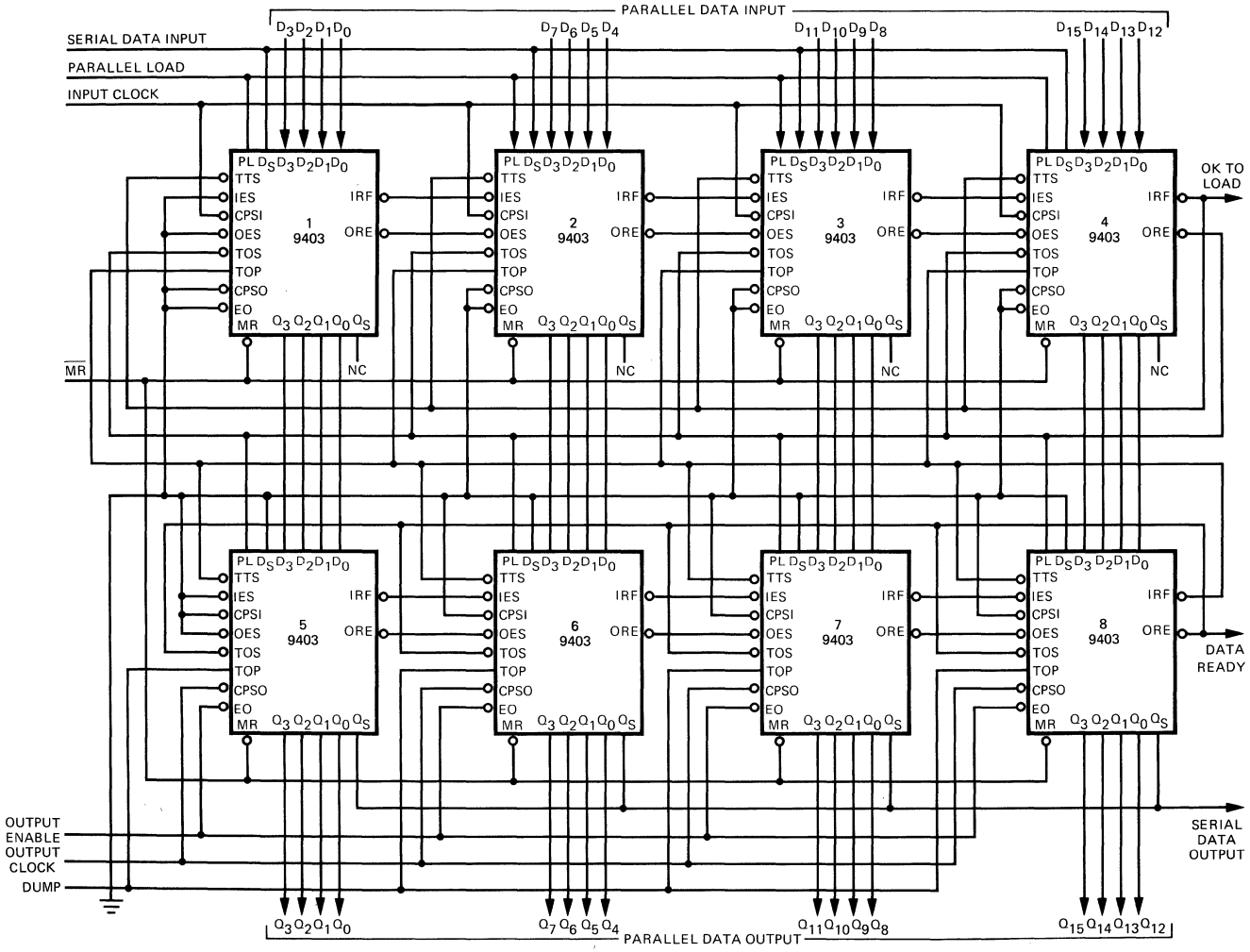


Fig. 6
A 31 X 16 FIFO ARRAY

Horizontal and Vertical Expansion – The 9403 can be expanded in both the horizontal and vertical direction without any external parts and without sacrificing any of the FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of $15n_1 + 1$ words by $4 \times n_2$ bits can be constructed.

Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

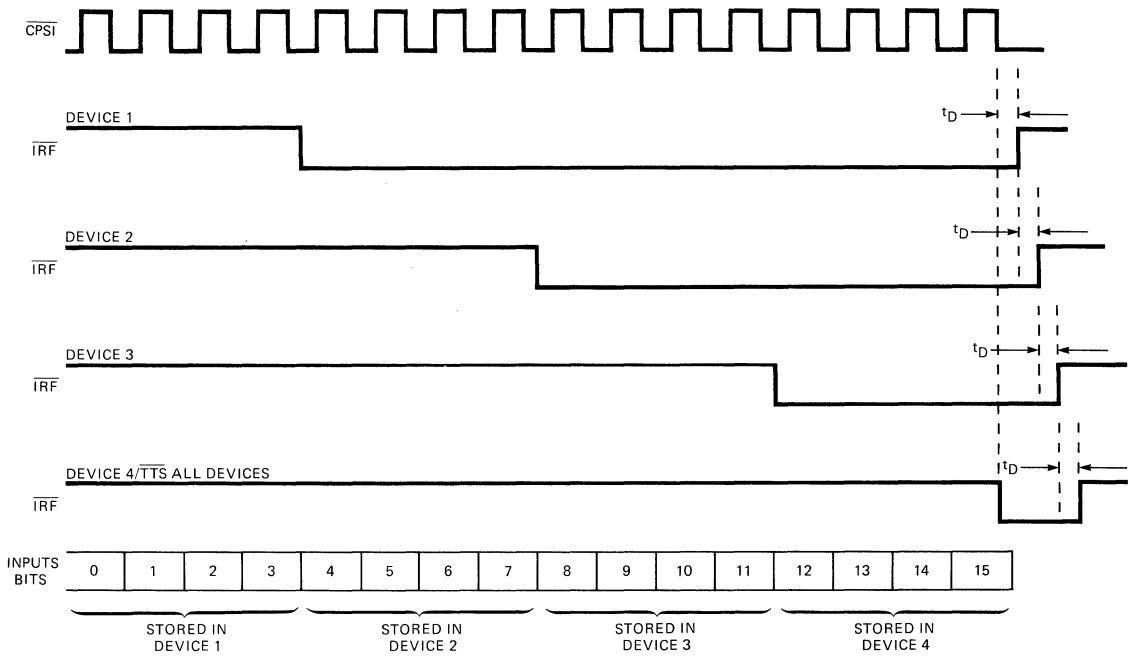


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

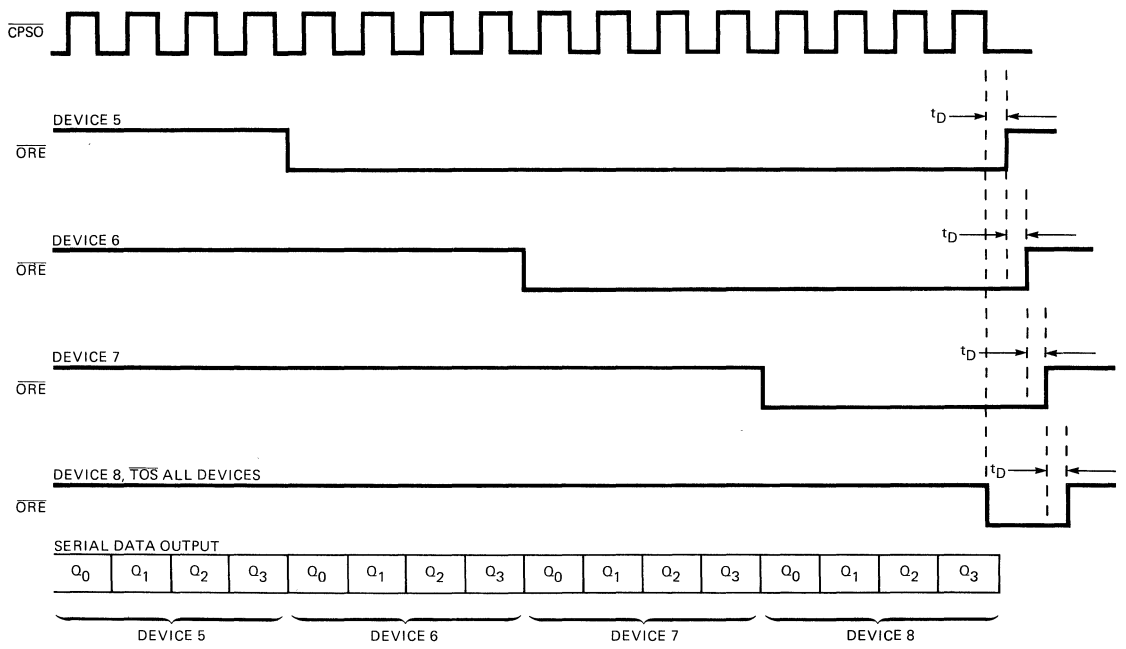


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

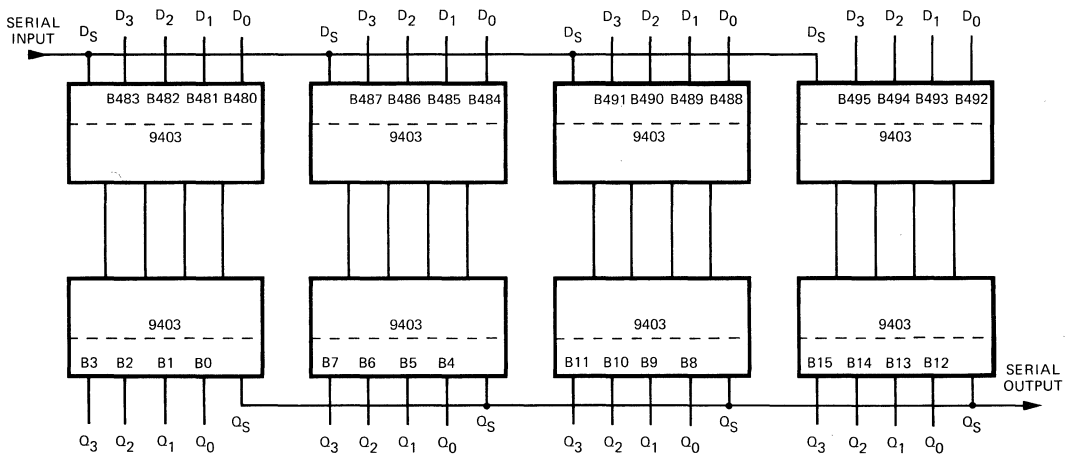


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

INTERLOCKING CIRCUITRY:

Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of Figure 6 devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ input has gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the master latch is set. Whenever $\overline{TTS}$ goes LOW the request initialization flip-flop will be set. If the master latch is HIGH, the input register will be immediately initialized and the request initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ request flip-flop. If the master latch is set, the last Output Register flip-flop is set and $\overline{ORE}$ goes HIGH. If the master latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

TABLE 1

OUTPUT CONDITION	INTERNAL STATE	
	Master Operation — IES LOW when Initialized	Slave Operation — IES HIGH when Initialized
IRF LOW	Input Register Full	Input Register Full and IES LOW
ORE LOW	Output Register not Full	Output Register not Full and OES LOW

Table 1 summarizes master/slave status outputs.

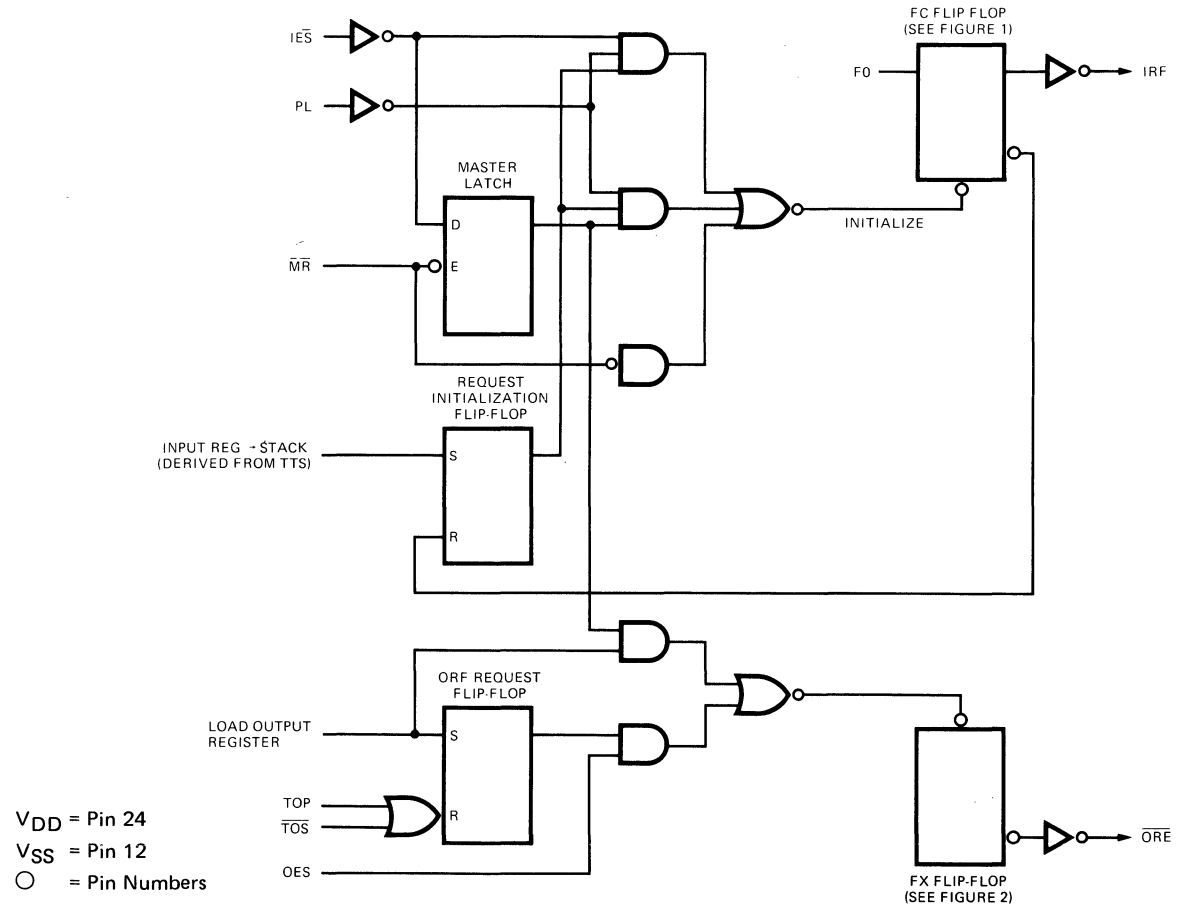


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage Q_S, QRE, OES	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA	
		XC	2.4	3.4				
V_{OH}	Output HIGH Voltage, Q_0–Q_3	XM	2.4	3.4		V	I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA	
V_{OL}	Output LOW Voltage, Q_0–Q_3, Q_S			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
				0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{OL}	Output LOW Voltage, ORE, OES			0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN
				0.35	0.5		I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH, Q_0–Q_3, Q_S				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V	
I_{OZL}	Output Off Current LOW, Q_0–Q_3, Q_S				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current, all except OES				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	OES				−0.86			
I_{OS}	Output Short Circuit Current, ORE, OES		−10		−42	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{OS}	Output Short Circuit Current, Q_0–Q_3, Q_S		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)	
I_{CC}	Supply Current			105	160	mA	V_{CC} = MAX, Inputs Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{CPSI}$ Pulse Width (HIGH)		25		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PWL}	$\overline{CPSI}$ Pulse Width (LOW)		12		ns	
t_{PWH}	PL Pulse Width (HIGH)		15		ns	Stack not full, Figures 17 & 18
t_{PWL}	$\overline{TTS}$ Pulse Width (LOW) Serial or Parallel Mode		6.0		ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{MR}$ Pulse Width (LOW)		15		ns	Figure 16
t_{PWH}	TOP Pulse Width (HIGH)		17		ns	$\overline{CPSO}$ LOW, Data available in stack, Figure 15
t_{PWL}	TOP Pulse Width (LOW)		25		ns	
t_{PWH}	$\overline{CPSO}$ Pulse Width (HIGH)		16		ns	TOP HIGH, Data in stack, Figures 13 & 14
t_{PWL}	$\overline{CPSO}$ Pulse Width (LOW)		20		ns	
t_s	Set-Up Time D_S to Negative $\overline{CPSI}$		20		ns	PL LOW, Figures 11 & 12
t_s	Set-Up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode		0		ns	Figures 11, 12, 17, 18
t_s	Set-Up Time Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$		0		ns	TOP HIGH, Figures 13 & 14
t_{rec}	Recovery Time $\overline{MR}$ to any Input		5.0		ns	Figure 16

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		18		ns	Stack not full, PL LOW, Figures 11 & 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		50		ns	
t_{PLH}	Propagation Delay, Negative-Going $\overline{CPSO}$		30		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH, Figures 13 & 14
t_{PHL}	to Q_S Output		20			
t_{PLH}	Propagation Delay, Positive-Going TOP		42		ns	$\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PHL}	to Outputs $Q_0 - Q_3$		32			
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		35		ns	Serial Output $\overline{OES}$ LOW, TOP HIGH, Figures 13 & 14
t_{PLH}	Propagation Delay, Positive-Going $\overline{TOS}$ to $\overline{ORE}$					
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$				ns	Parallel Output, $\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		45			
t_{ft}	Fall Through Time		450		ns	$\overline{TTS}$ connected to IRF TOS connected to $\overline{ORE}$ $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		48		ns	Data in stack, TOP HIGH, Figures 13 & 14
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going IRF		35		ns	Stack not full, Figures 17 & 18

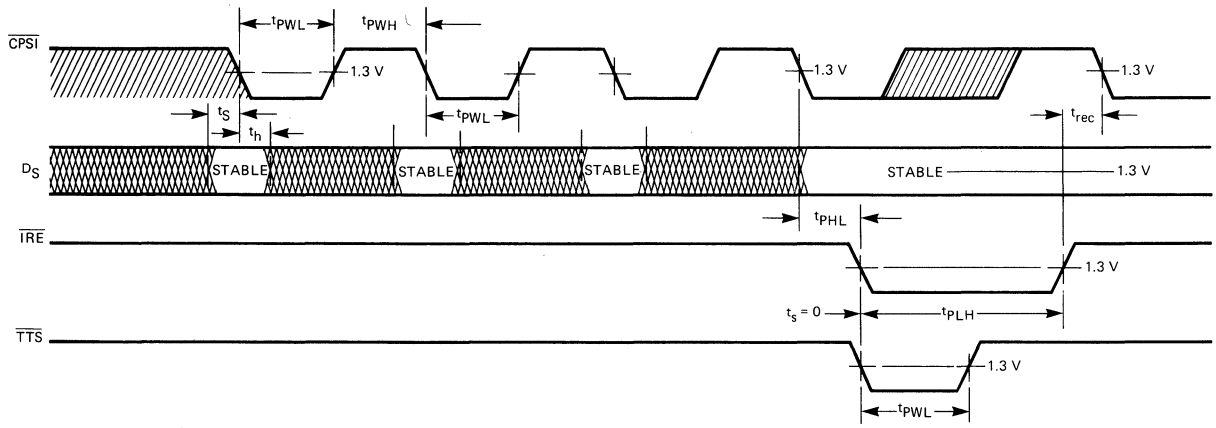


Fig. 11
SERIAL INPUT, UNEXPANDED OR MASTER OPERATION

Conditions: Stack not full, $\overline{IES}$, PL LOW

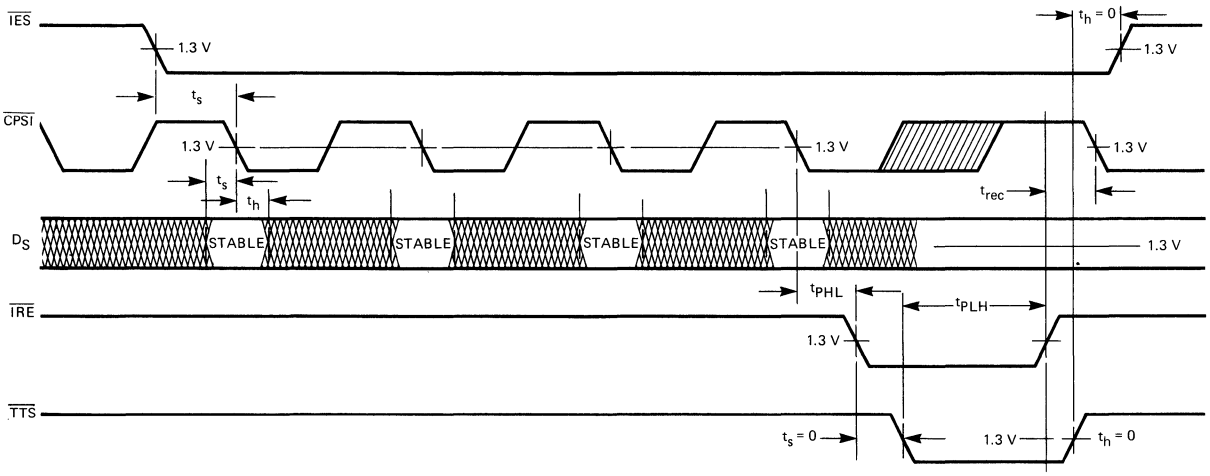


Fig. 12
SERIAL INPUT, EXPANDED SLAVE OPERATION

Conditions: Stack not full, $\overline{IES}$ HIGH when initialized, PL LOW

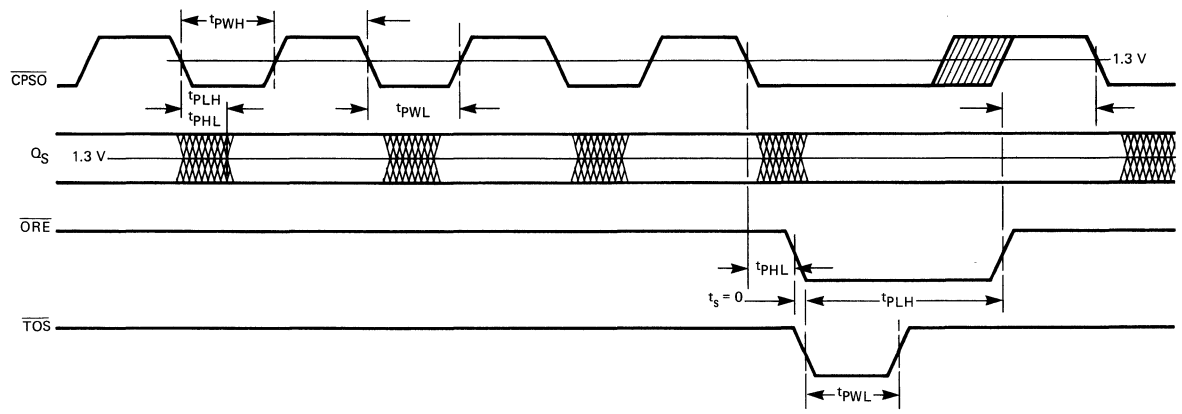


Fig. 13
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION

Conditions: Data in stack, TOP HIGH, $\overline{IES}$ LOW when initialized, $\overline{OES}$ LOW

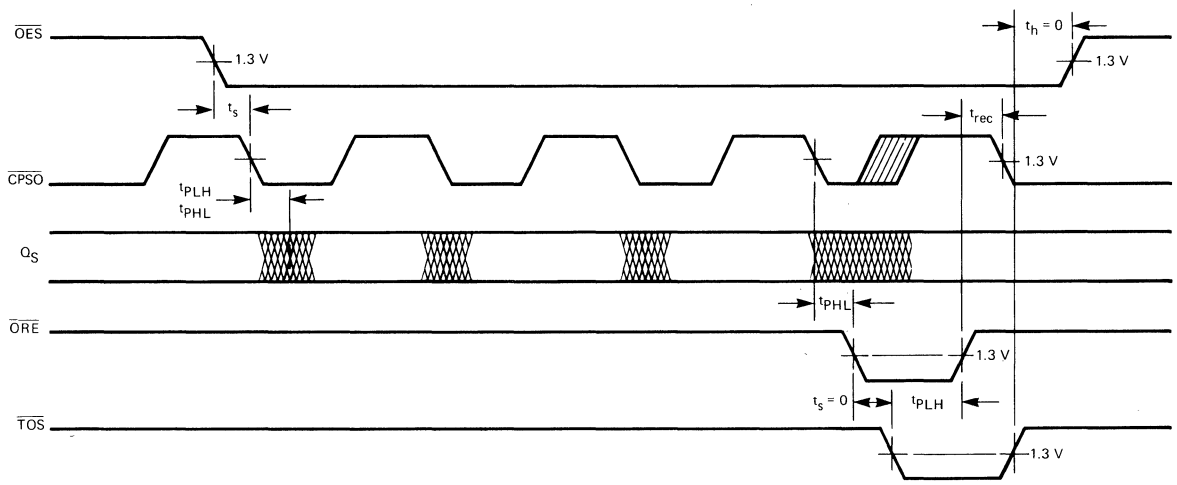


Fig. 14
SERIAL OUTPUT, SLAVE OPERATION

Conditions: Data in stack, TOP HIGH, $\overline{IES}$ HIGH when initialized

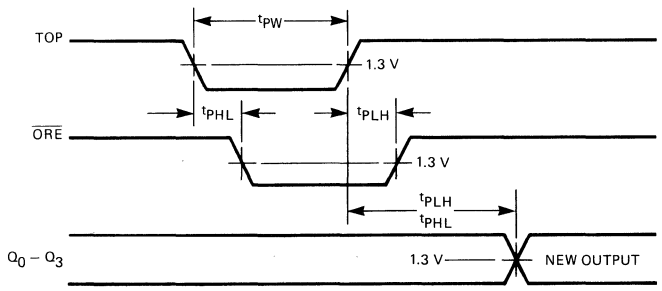


Fig. 15
PARALLEL OUTPUT, 4-BIT WORD OR MASTER IN PARALLEL EXPANSION

Conditions: $\overline{IES}$ LOW when initialized, $\overline{EO}$, $\overline{CPSO}$ LOW. Data available in stack

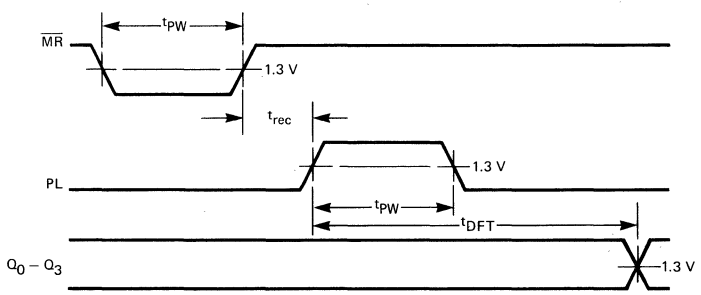
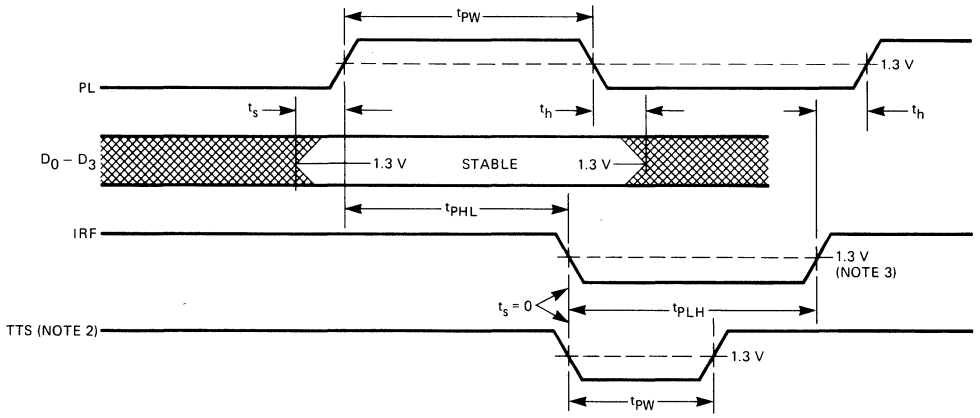


Fig. 16
FALL THROUGH TIME

Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH



NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, IRE will stay LOW.

Fig. 17
PARALLEL LOAD MODE, 4-BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

Conditions: Stack not full, $\overline{IES}$ LOW when initialized

---

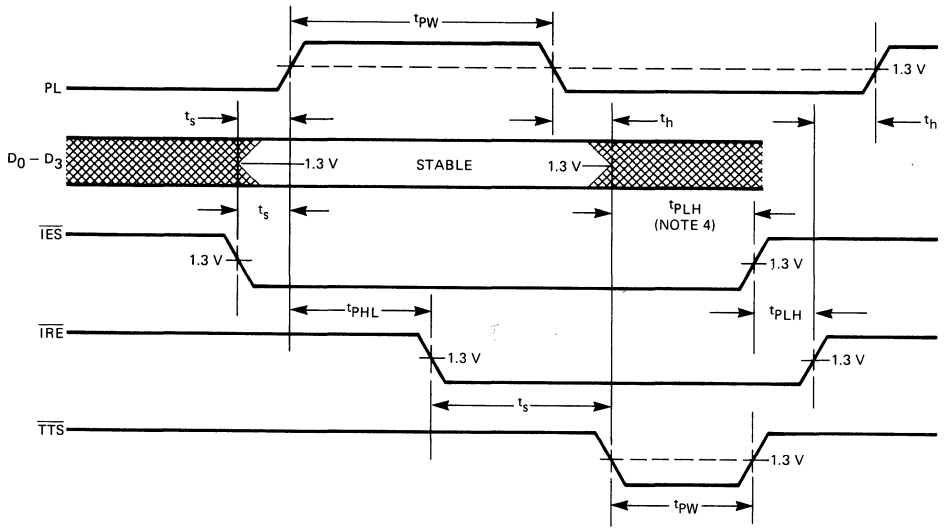


Fig. 18
PARALLEL LOAD, SLAVE MODE

Conditions: Stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

9404
DATA PATH SWITCH
FAIRCHILD MACROLOGIC

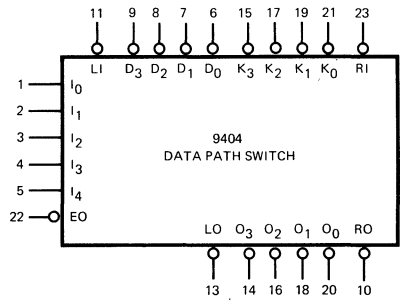
DESCRIPTION – The 9404 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the 9405 (Arithmetic Logic Register Stack). A total of 30 instructions (see Table 1) facilitate logic shifting, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction Word Inputs (I_0-I_4) selects one of the thirty instructions operating on two sets of 4-bit Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$). Left Input ($\overline{LI}$) and Left Output ($\overline{LO}$) and Right Input ($\overline{RI}$) and Right Output ($\overline{RO}$) are available for expansion in 4-bit increments. An active LOW Output Enable Input ($\overline{EO}$) provides 3-state control of the Data Outputs ($\overline{O}_0$-$\overline{O}_3$) for bus oriented applications.

The 9404 is a member of Fairchild's MACROLOGIC family and is fully compatible with all TTL families.

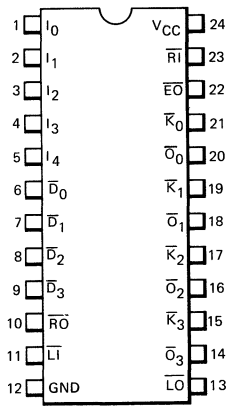
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **30 ns DELAY OVER 16-BIT WORD**
- **TWO 4-BIT DATA INPUT BUSSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **PURELY COMBINATORIAL – NO CLOCKS REQUIRED**
- **PACKAGED IN SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



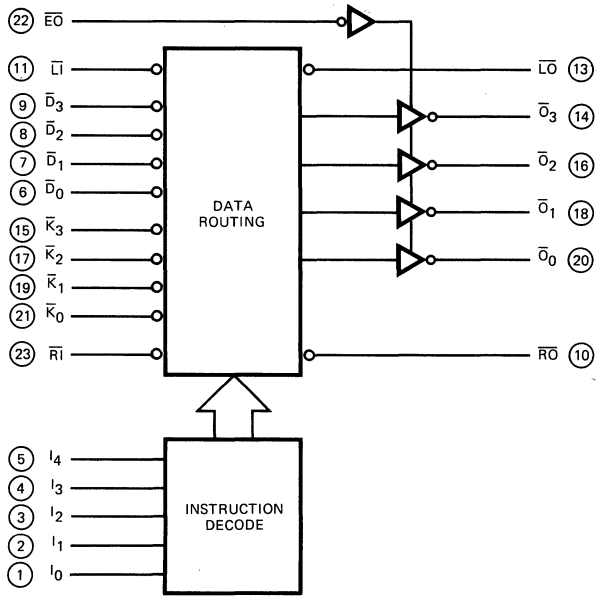
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0$-$\overline{D}_3$	D-Bus Inputs (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{K}_0$-$\overline{K}_3$	K-Bus Inputs (active LOW)	0.5 U.L.	0.23 U.L.
I_0-I_4	Instruction Word Input	0.5 U.L.	0.23 U.L.
$\overline{LI}$	Shift Left Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{LO}$	Shift Left Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
$\overline{RI}$	Shift Right Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{RO}$	Shift Right Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
$\overline{EO}$	Output Enable Input (active LOW)	0.5 U.L.	0.23 U.L.
$\overline{O}_0$-$\overline{O}_3$	Data Output (active LOW) (Note b)	130 U.L.	10 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V

BLOCK DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Number

TABLE 1
INSTRUCTION SET FOR THE 9404

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS					FUNCTION
I_4	I_3	I_2	I_1	I_0	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$		I_4	I_3	I_2	I_1	I_0	$\overline{LO}$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	$\overline{RO}$	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)	H	L	L	H	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)	H	L	L	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Sign Extend
L	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	$\overline{RI}$		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask D-Bus	H	L	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	$\overline{RI}$		K-Bus Shift Left
L	L	H	H	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	H	L		$\overline{LI}$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask D-Bus	H	L	H	H	H		$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right Arith(2)
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		$\overline{LI}$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right Arith(2)
L	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Byte Mask K-Bus	H	H	L	H	L		$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		Byte Mask K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask K-Bus
L	H	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

FUNCTIONAL DESCRIPTION – The 9404 Data Path Switch combines the functions of a dual 4-input multiplexer, a true/complement one/zero generator, and a shift left/shift right array.

As shown in Table 1, there are two shift right modes. The arithmetic right shift preserves the sign bit in the most significant position while the logic shift moves all positions. Right shift is defined as a 1-bit shift toward the least significant position.

For half-word arithmetic the 9404 provides instructions which extend the sign bit left through the more significant slices. Shift linkages are available as individual inputs and outputs for complete flexibility.

The 9404 may be used to generate constants +1, 0, −1 and −2 in 2s complement notation.

9404 ARRAYS – Arrays of larger than 4-bit word lengths are easily obtained. Figure 1 illustrates a 16-bit array constructed using four devices; device 1 is the least significant and device 4 is the most significant slice. Within each slice, inputs and outputs with '0' subscript are the least significant bits.

The I_1 through I_4 inputs of all devices are bussed. These four bus lines together with the I_0 inputs of the devices form an 8-bit instruction bus to control the array. In some applications, it may be possible to connect the I_0 inputs of devices 1 & 2 together and the I_0 Inputs of devices 3 & 4 together, so that only six bits are needed to control the arrays. Connecting the $\overline{LO}$ of device 1 to $\overline{RI}$ of device 2, $\overline{LO}$ of device 2 to RI of device 3, etc. provides left shift (i.e., shift towards most significant bit) and sign extension. From Table 1 it can be seen that "sign extend" consists of two adjacent instructions differing only in I_0; one of these instructions connects the most significant bit of the selected input bus (i.e., $\overline{D}_3$ or $\overline{K}_3$) to the $\overline{LO}$ output while the other instruction forces the output bus and $\overline{LO}$ to the $\overline{RI}$ input. In a similar fashion right shift operation is accomplished by connecting the $\overline{LI}$ input of a device to the $\overline{RO}$ of the next more significant device.

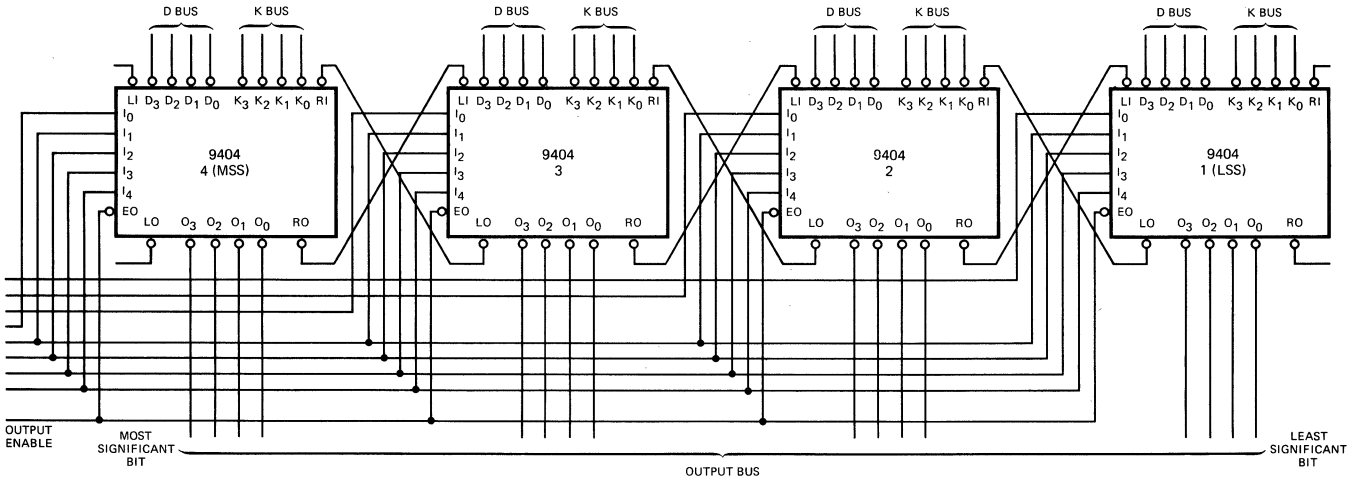


Fig. 1 16-BIT 9404 ARRAY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			–0.9	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage $\overline{LO}$, $\overline{RO}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = –400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $\overline{O}_0$-$\overline{O}_3$	XM	2.4	3.4		V	I_{OH} = –2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = –5.7 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{LO}$, $\overline{RO}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $\overline{O}_0$-$\overline{O}_3$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V
I_{OZL}	Output Off Current LOW				–100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		–30		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			76		mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$) to Output (O_0-O_3)		20		ns	$\overline{EO}$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$) to Shift Outputs ($\overline{LO}$, $\overline{RO}$)		18		ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{RI}$ to $\overline{LO}$		10		ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction Word (I_0-I_5) to Data Outputs ($\overline{O}_0$-$\overline{O}_3$)		22		ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction Word (I_0-I_5) to Shift Outputs ($\overline{RO}$, $\overline{LO}$)		22		ns	
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs ($\overline{O}_0$-$\overline{O}_3$)		10		ns	
t_{PLZ} t_{PHZ}	Disable Delay, EO to Outputs ($\overline{O}_0$-$\overline{O}_3$)		8		ns	

9405
ARITHMETIC LOGIC REGISTER STACK
FAIRCHILD MACROLOGIC

DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement general registers in high performance programmable digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0-A_2). The result of the operation is loaded into the same RAM location and simultaneously, is loaded into the output register making it available at the 3-state output data bus.

The 9405 operates on four bits of data but features are provided for expansion to longer word lengths. Carry Propagate and Carry Generate Outputs are provided for an external carry lookahead where maximum operating speed is required. In applications where high speed arithmetic is not needed, ripple expansion may also be implemented. The 9405 provides three status signals: Zero, Negative and Overflow. These qualify the result of an operation. The 9405 is a member of Fairchild's MACROLOGIC family and is fully compatible with all TTL families.

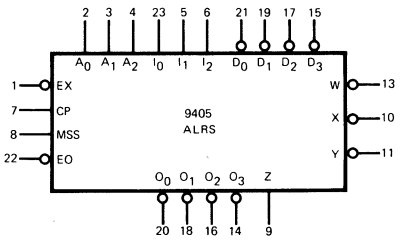
- **EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE**
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR LOOKAHEAD CARRY**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES STATUS – ZERO, NEGATIVE, AND OVERFLOW**
- **3-STATE OUTPUTS**
- **24-PIN PACKAGE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
A_0-A_2	Address Instruction Inputs	0.5 U.L.	0.23 U.L.
I_0-I_2	ALU Instruction Inputs (Note b)	0.5 U.L.	0.23 U.L.
MSS	Most Significant Slice Input (Active HIGH)	0.5 U.L.	0.23 U.L.
CP	Clock Input	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
O_0-O_3	Data Outputs (Active LOW)	130 U.L.	10 U.L.
$\overline{W}$	Ripple Carry Output (Active LOW) (Note c)	10 U.L.	5 U.L.
$\overline{X}$	Carry Propagate Output (Note d)	10 U.L.	5 U.L.
$\overline{Y}$	Carry Generate Output (Note e)	10 U.L.	10 U.L.
Z	Zero Status Output (Active HIGH, Open Collector) (Note f)		5 U.L.

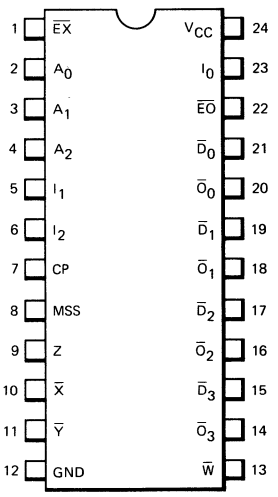
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW (0.5 V).
b) I_0 used also for Carry Input on lesser significant slices.
c) $\overline{W}$ Output also carries instruction information.
d) $\overline{X}$ Output provides Negative Status (active LOW) on most significant slice.
e) $\overline{Y}$ Output provides Overflow Status (active LOW) on most significant slice.
f) An external pull-up resistor is required to supply HIGH level drive capability.

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM

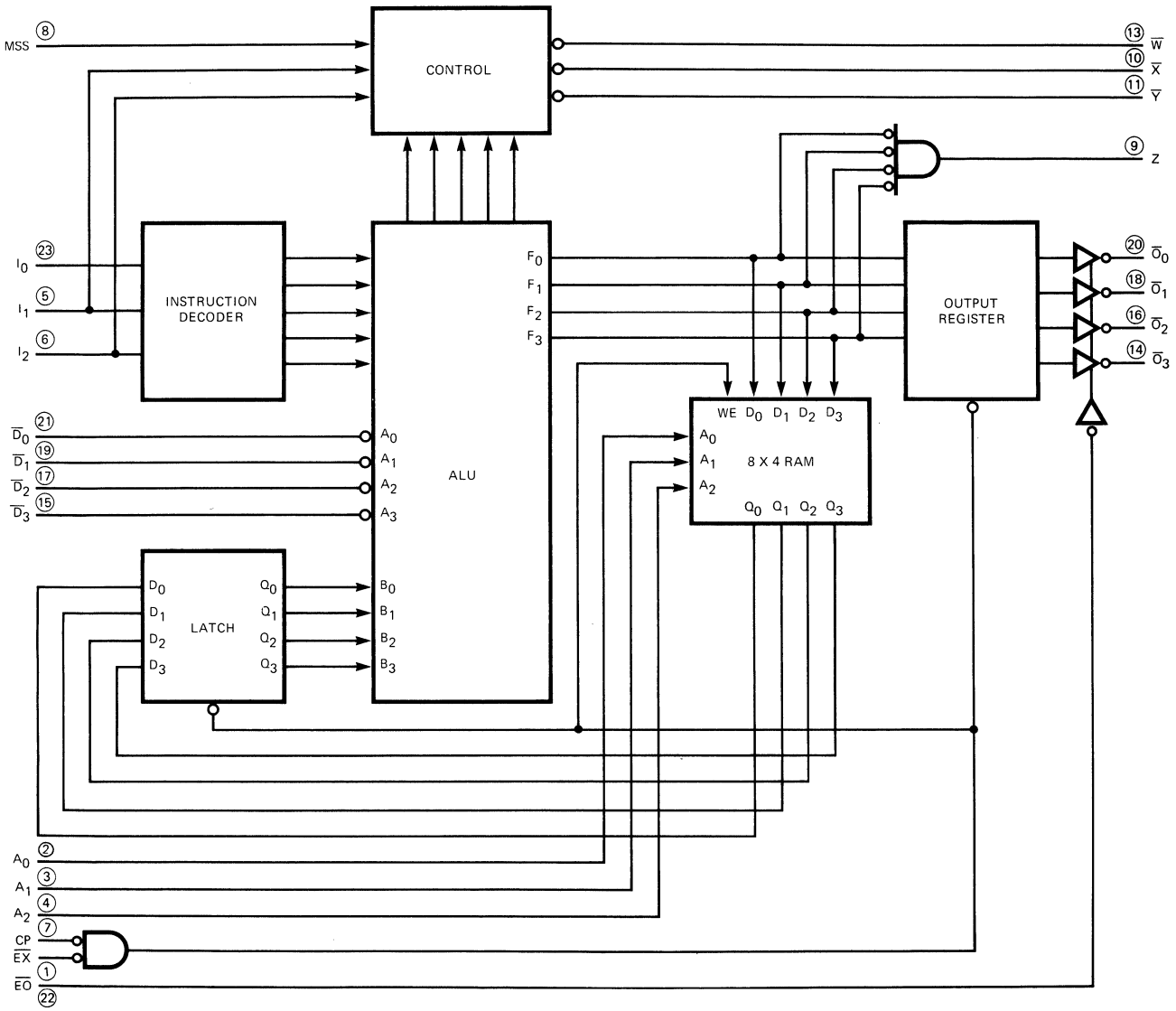


TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2	I_1	I_0	INTERNAL OPERATION
L	L	L	Rx plus D-Bus plus 1 → Rx
L	L	H	Rx plus D-Bus → Rx
L	H	H	Rx • D-Bus → Rx (Logic AND)
L	H	H	D-Bus → Rx
H	L	L	Rx → Output Register
H	L	H	Rx + D-Bus → (Logic OR)
H	H	L	Rx ⊕ D-Bus → Rx
H	H	H	$\overline{\text{D-Bus}}$ → Rx

NOTES:
1. Rx is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

FUNCTIONAL DESCRIPTION – As shown in the Block Diagram the 9405 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an instruction decode network, control logic and a 4-bit Output Register.

The ALU receives the active LOW input data ($\overline{D}_0$-$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and output register. The active LOW Output Data Bus ($\overline{O}_0$-$\overline{O}_3$) is obtained from the output register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level $\overline{EO}$ disables the buffers (high impedance state).

The instruction bus for the 9405 consists of two fields, A and I; A_0-A_2 specify the desired location of the RAM and I_0-I_2 specify the desired function to be performed. Table 1 lists Instruction Field Code assignments. Thus, the 9405 provides eight registers (R_0-R_7) and eight different operations may be performed on any of these registers. The I_0-I_2 Inputs are decoded by the instruction decode network to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: Carry Out, Carry Propagate, Carry Generate, Negative Status and Overflow Status. The control logic manipulates the status signals as a function of I_0-I_2 and a control input MSS. A HIGH on the MSS Input declares the most significant slice in a 9405 array (the diode-input on MSS allows it to be tied directly to V_{CC}). All devices, except the most significant 9405 should have a LOW level (ground) on the MSS Input. The control logic generates three device outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$ for arrayed operation. An all zero result from the ALU is decoded and presented at the open collector Zero Status (Z) Output.

The I_0 input serves a dual purpose. For arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 9405 expansion schemes.

OPERATION – The 9405 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input active LOW AND gate. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$-$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0-I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. The A lines must obviously be held stable during this time. On the LOW-to-HIGH CP transition, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A Inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

9405 ARRAYS – The 9405 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 9405 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 9405s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, $\overline{CP}$ and $\overline{EO}$ Inputs of all devices. The Z Output is open collector and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four 9405s. The MSS input is tied to V_{CC} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-Field and I-Field. A-Field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 Inputs forms the I-Field for the array. The I_0 Inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ Outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ Output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ Output is the carry output of that slice. In case of non-arithmetic instructions, it assumes the state of the I_0 input. Thus, in Figure 1, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ Output to I_0 Input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 Inputs together to form the I-Field for the array. The $\overline{W}$ Output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ Outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

Thus, $\overline{X}$ Output of device 4 is LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW level on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occured. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP. Figure 2 shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 93S42/74S182 in addition to the four 9405s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS Inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-Field for the array instruction bus is obtained by connecting corresponding A Inputs of all four devices. Bussed I_1 and I_2 Inputs together with the I_0 Input of device 1 form the I-Field for the array. The I_0 Inputs for devices 2, 3 and 4 are obtained from the 93S42/74S182 Carry Outputs (Cn+x, Cn+y, and Cn+z

respectively). Also the $\overline{P}$ and $\overline{G}$ Inputs of 93S42/74S182 are connected to $\overline{X}$ and $\overline{Y}$ Outputs of the 9405s as shown. The control logic in the 9405 (see Block Diagram) generates $\overline{X}$ and Y Outputs as a function of I_1, I_2 and MSS Inputs as well as the Carry Generate and Carry Propagate Outputs of the ALU. If the MSS Input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ Output reflects Carry Propagate and $\overline{Y}$ reflects Carry Generate Outputs from that slice. For an arithmetic instruction the I_0 Input is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ Outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ Output of device 4 is the carry output from the array. Also, note that the I_0 Input of device 1 is not only an instruction input but also provides the carry input to the array so the I_0 Input of device 1 must be connected to the appropriate 93S42/74S182 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 9405 forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ Outputs on all except the most significant slice. An examination of the 93S42/74S182 logic reveals that whenever $\overline{P}$ is LOW and $\overline{G}$ is HIGH the associated carry output is the same as the carry input. Thus, in Figure 2 devices 2, 3, and 4 will assume the logic level as that presented to the I_0 Input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion $\overline{X}$ and $\overline{Y}$ Outputs of device 4 represent Negative and Overflow from the array.

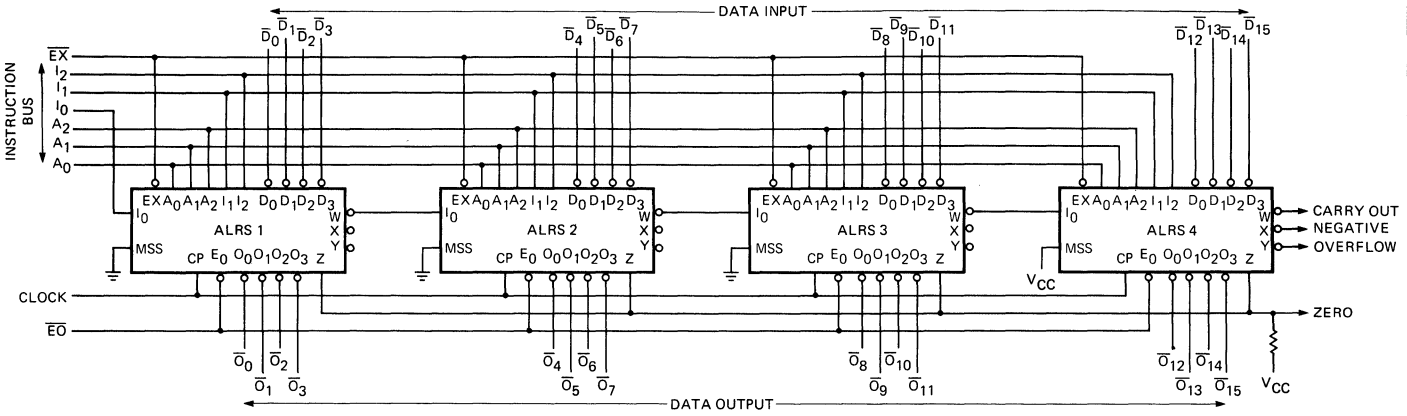


Fig. 1 RIPPLE CARRY EXPANSION

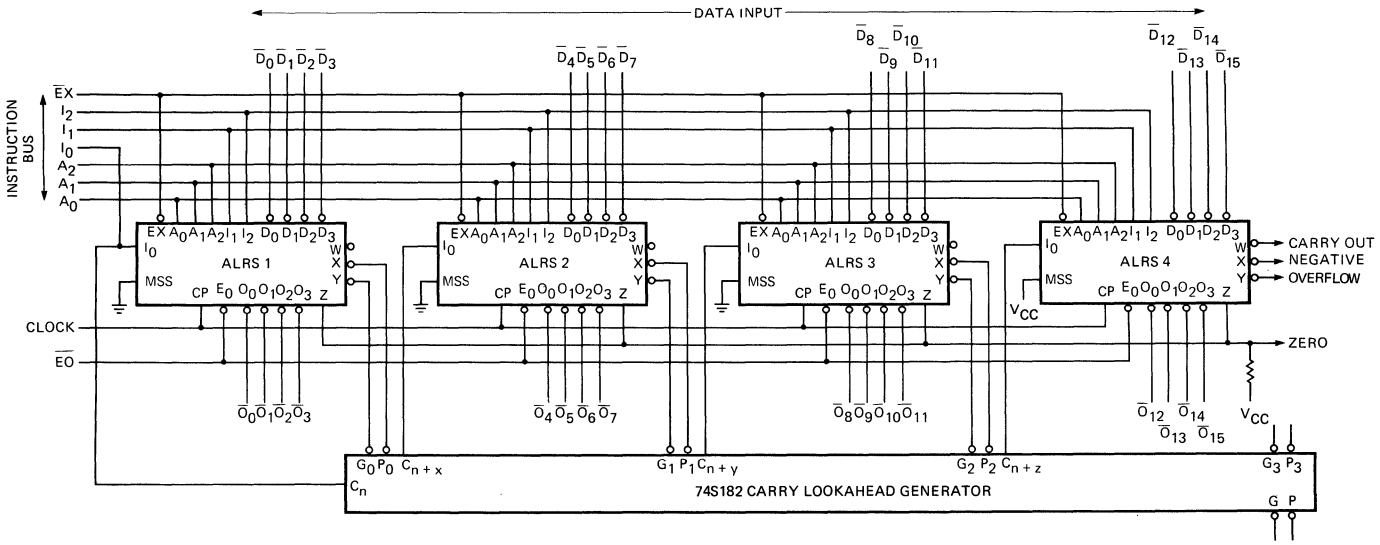


Fig 2. CARRY LOOKAHEAD EXPANSION

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{W}$, $\overline{X}$ Outputs	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA; V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA; V_{CC} = MIN
I_{OH}	Output HIGH Current Z Output				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{W}$, $\overline{X}$, Z			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3, \overline{Y}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			100	160	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

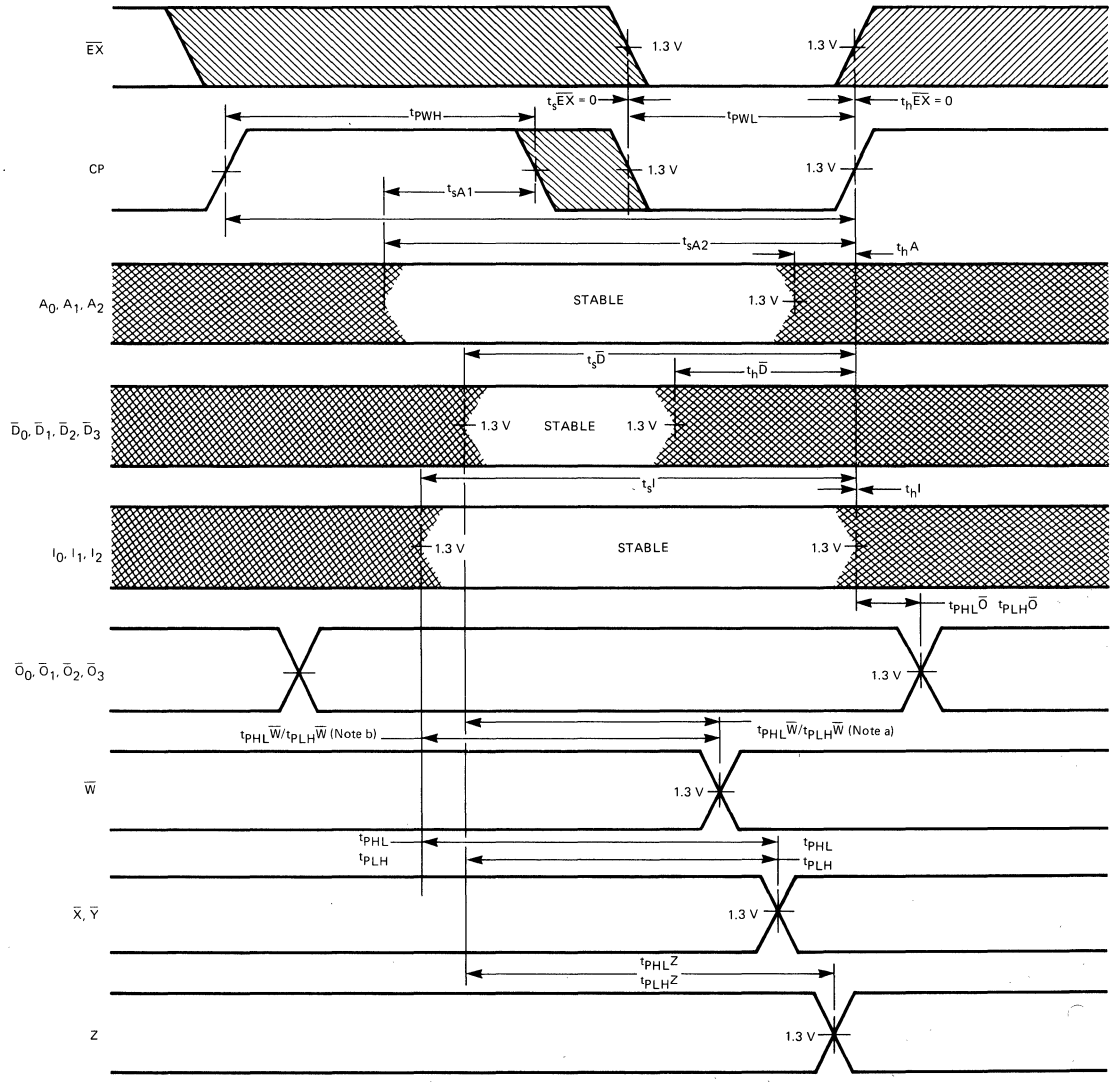
AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{CW}	Clock Period		75		ns	
t_{PWH}	Clock Pulse Width (HIGH)		30			
t_{PWL}	Clock Pulse Width (LOW)		20			
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0			
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0			
t_{sA1}	Set-Up Time, A_0, A_1, A_2 to Negative Going CP (Note 1)		25		ns	
t_{sA2}	Set-Up Time, A_0, A_1, A_2 to Positive Going CP (Note 1)		70		ns	$\overline{EX}$ LOW
t_hA	Hold Time, A_0, A_1, A_2 to Positive Going CP		5		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$ to Positive Going CP		45		ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$ to Positive Going Clock		−20		ns	
t_sI	Set-Up Time, I_0, I_1, I_2 to Positive Going Clock		50		ns	
t_hI	Hol dTime, I_0, I_1, I_2 to Positive Going Clock		0		ns	

NOTE:
1. Both set-up times must be met simultaneously.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Positive Going CP to $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$		25		ns	$\overline{EO}$, $\overline{EX}$ LOW
t_{PLH} t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		15		ns	I_1 or I_2 HIGH
t_{PLH} t_{PHL}	Propagation Delay, Data ($\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$) to $\overline{W}$		35		ns	I_1, I_2 LOW
t_{PLH} t_{PHL}	Propagation Delay, Data ($\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$) to $\overline{X}$, $\overline{Y}$		45		ns	MSS HIGH
			25		ns	MSS LOW
t_{PLH} t_{PHL}	Propagation Delay, I_1, I_2 to $\overline{X}$, $\overline{Y}$		22		ns	MSS LOW
t_{PLH} t_{PHL}	Propagation Delay, Data ($\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$) to Z		55		ns	1 kΩ External Load Resistor to V_{CC}
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$		12			
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}$ to $\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$		10			



NOTES:
a) Delay for logical operation (I_1 or I_2 HIGH)
b) Delay for arithmetic operation (I_1 = I_2 = LOW)

Fig. 3 ALRS TIMING DIAGRAM

9406

PROGRAM STACK

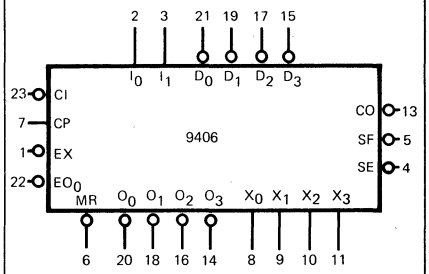
FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9406 is a 16-word by 4-bit "Push-Down Pop-Up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 9406 executes 4 instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, the Program Counter (PC) is in the top location of the Stack. As a new PC value is "pushed" into the Stack (Call Operation), all previous PC values effectively move down one level. The top location of the Stack is the current PC. Up to 16 PC values can be stored, which gives the 9406 a 15 level nesting capability. "Popping" the Stack (Return Operation) brings the most recent PC to the top of the Stack. The remaining two instructions affect only the top location of the Stack. In the Branch operation a new PC value is loaded into the top location of the Stack from the $\overline{D}_0 - \overline{D}_3$ Inputs. In the Fetch operation, the contents of the top Stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 9406 may be expanded to any word length without additional logic. 3-State output drivers are provided on the 4-bit Address Outputs ($X_0 - X_3$) and Data Outputs, ($\overline{O}_0 - \overline{O}_3$); the X-Bus Outputs are enabled internally during the Fetch instruction while the O-bus Outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 9406 is a member of Fairchild's 9400 MACROLOGIC family, and is fully compatible with all TTL families.

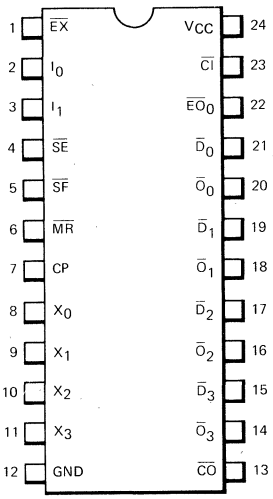
- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **10 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADS FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **24-PIN PACKAGE**
- **3-STATE OUTPUTS**

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
I_0, I_1	Instruction Inputs	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_0$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Output Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{CO}$	Carry Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SF}$	Stack Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SE}$	Stack Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

FUNCTIONAL DESCRIPTION – As shown in the Block Diagram, the 9406 consists of an input multiplexer, a 16 X 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 9406 is organized around three 4-bit busses; the Input Data Bus ($\overline{D}_0 - \overline{D}_3$), Output Data Bus ($\overline{O}_0 - \overline{O}_3$) and the Address Bus ($X_0 - X_3$). The 9406 implements four instructions as determined by Inputs I_0 and I_1. (See Table 1). The O-Bus is derived from the RAM output latches and enabled by the active LOW Output Enable ($\overline{EO}_0$) Input. The X-Bus is also derived from the output latches; it is enabled internally during the Fetch instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) Inputs.

FETCH OPERATION – The Fetch Operation places the content of the current Program Counter (PC) on the X-Bus. If the Carry In ($\overline{CI}$) is LOW, the current PC is incremented in preparation for the next Fetch. If $\overline{CI}$ is HIGH, the value of the current program is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The active level LOW Execute ($\overline{EX}$) is normally set up at this time as well. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the input multiplexer. The current PC value is loaded into the latches and is available on the O-Bus if $\overline{EO}_0$ is LOW. When CP is LOW the output latches are disabled from following the RAM output, when both CP and $\overline{EX}$ are LOW, buffers are enabled, applying the current PC to the X-Bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out (CO) is LOW when the contents of the current PC is at its maximum, e.e., all ones and the Carry In ($\overline{CI}$) is LOW. When CP or EX goes HIGH, writing into the RAM is inhibited and the Address Buffers ($X_0 - X_3$) are disabled.

BRANCH OPERATION – During a Branch Operation, the Data Inputs ($\overline{D}_0 - \overline{D}_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. The Stack Pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into the current PC. The X-Bus drivers are not enabled during a Branch Operation.

CALL OPERATION – During a Call Operation the content of the Data Bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The Instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the Stack Pointer value thus incrementing the RAM address. Since the output latches go to the nontransparent or store mode when CP is LOW, the O-Bus outputs will reflect the RAM output at the CP negative-going transition. If EX goes LOW considerably before CP goes LOW, the O-Bus will correspond to the previous contents of the incremented RAM address after CP goes LOW. If CP goes LOW a very short time after EX, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

When CP is LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into this new RAM location. On the LOW-to-HIGH CP transition, the incremented Stack Pointer value is loaded into the Stack Pointer Register and the O-Bus Outputs reflect the newly entered data. When the RAM address is "1111" the Stack Full Output ($\overline{SF}$) is LOW, indicating that no further Call operations should be initiated. If an additional Call Operation is performed SP is incremented to (0000), the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-Bus drivers are not enabled during a Call operation.

RETURN OPERATION – During the Return operation the previous PC is "popped" to become the current PC.

The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the Stack Pointer value, thus decrementing the RAM address. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the new value after $\overline{EX}$ goes LOW. If CP goes LOW a short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

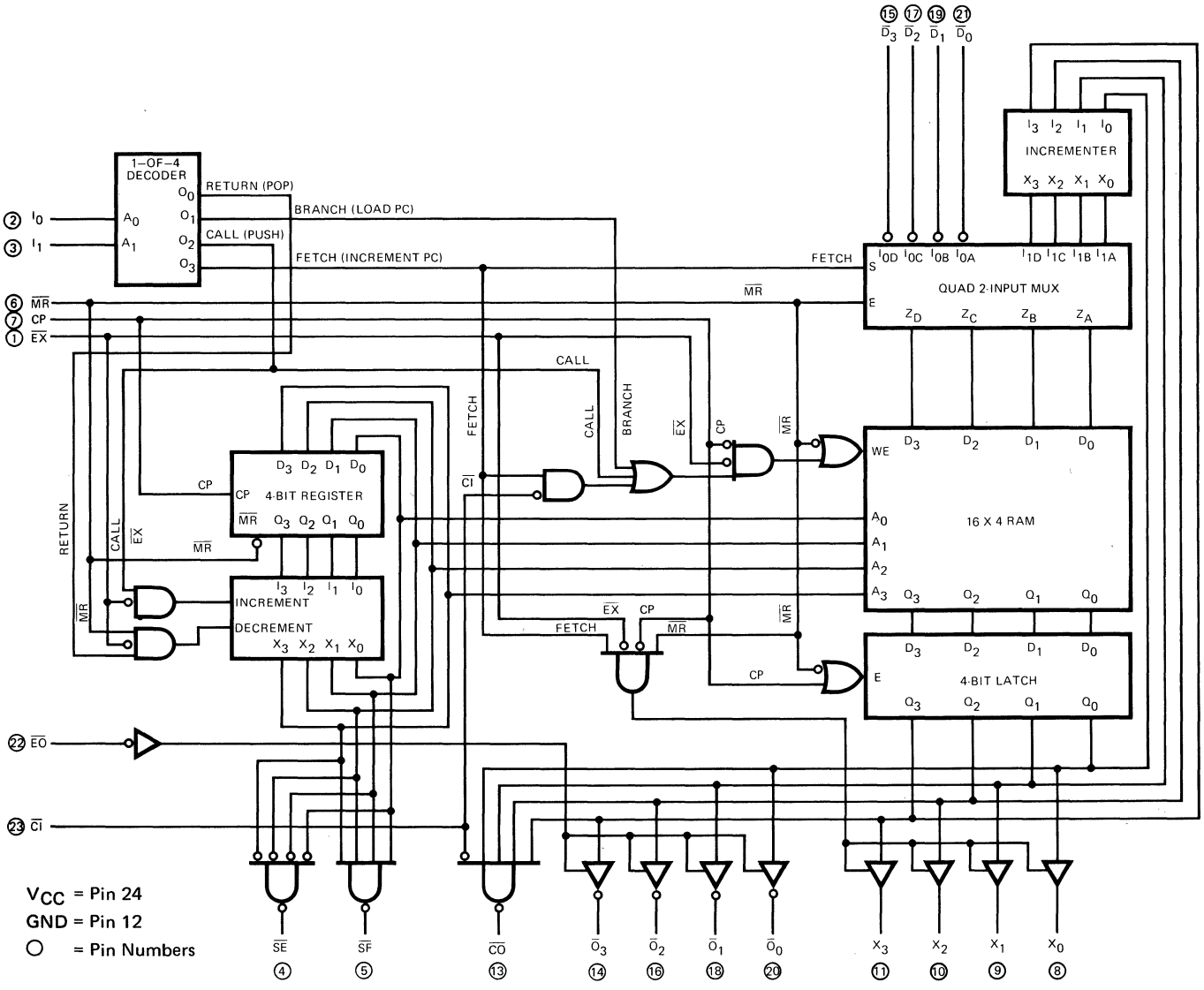
On the LOW-to-HIGH CP transition the decremented Stack Pointer value is loaded into the Stack Pointer Register and the O-Bus Outputs correspond to the new "popped" value.

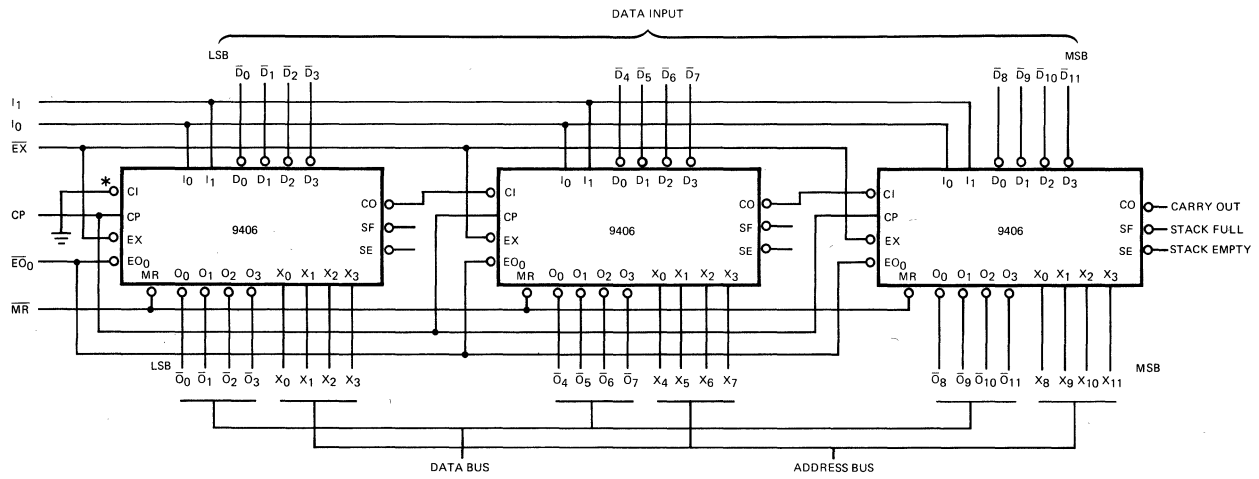
The X-Bus drivers are not enabled during a return operation. When the RAM address is "0000", the Stack Empty Output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full Output ($\overline{SF}$) will go LOW. Operation of the active LOW Master Reset ($\overline{MR}$) causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

MULTIPLE 9406 OPERATION – The 9406 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in Figure 1. Carry In ($\overline{CI}$) and Carry Out (CO) are connected to provide automatic increment of the current program counter during Fetch. The $\overline{CI}$ Input of the least significant 9406 is tied LOW to ground.

If automatic increment during Fetch is not desired, the $\overline{CI}$ Input of the least significant 9406 is held HIGH.

BLOCK DIAGRAM





*Tie to V_{CC} to disable automatic increment.

Fig. 1
9406 EXPANSION A 16 BY 12 PROGRAM STACK

TABLE 1
INSTRUCTION SET FOR THE 9406

I_1 I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH EO_0 LOW)
L L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of EX and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L H	Branch (Load PC)	Load D-Bus into Current Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H L	Call (Push)	Increment Stack Pointer and Load D-Bus into New Program Counter Location	Disabled	Depending on the relative timing of EX and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Figure 9 for details.
H H	Fetch (Increment PC)	Increment Current Program Counter if CI is LOW	Current Program Counter while both CP and EX are LOW, disabled while CP or EX is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level
L = LOW Level

DC CHARACTERISTICS OVER OPERATION TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{CO}$, $\overline{SE}$, $\overline{SF}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
V_{OL}	Output LOW Voltage $\overline{CO}$, $\overline{SE}$, $\overline{SF}$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.35	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.35	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V
I_{IH}	Input HICH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CCH}	Supply Current			100	160	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS – ALL MODES OF OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{CW}	Clock Period		80		ns	
t_{PWH}	Clock Pulse Width (HIGH)		40		ns	
t_{PWL}	Clock Pulse Width (LOW)		30		ns	
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0		ns	Figure 2
t_sI	Set-Up Time, I_0, I_1 to Negative-Going Clock		20		ns	
t_hI	Hold Time, I_0, I_1 to Positive-Going Clock		0		ns	
$t_s\overline{CI}$	Set-Up Time, $\overline{CI}$ to Negative-Going Clock		5		ns	
$t_h\overline{CI}$	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	
t_sD	Set-Up Time, D_0–D_3 to Positive-Going Clock		20		ns	
t_hD	Hold Time, D_0 – D_3 to Positive-Going Clock		0		ns	
$t_{PWL}\overline{MR}$	$\overline{MR}$ Pulse Width (LOW)		40		ns	Figure 3
t_{rec}	MR to Negative-Going Clock		30		ns	

REFER TO INDIVIDUAL TIMING DIAGRAMS FOR EACH OPERATION TO DETERMINE OUTPUT RESPONSE

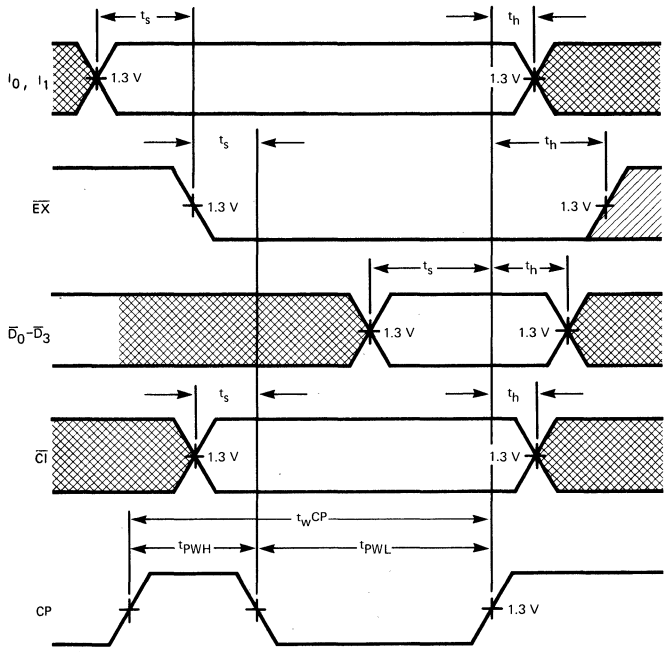


Fig. 2
WAVEFORMS FOR ALL OPERATIONS

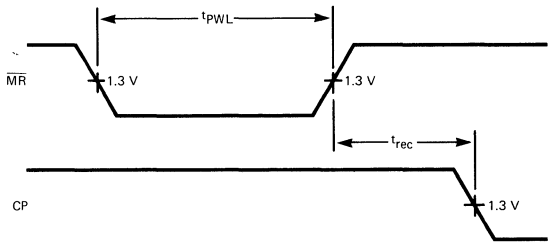


Fig. 3
RESET OPERATION

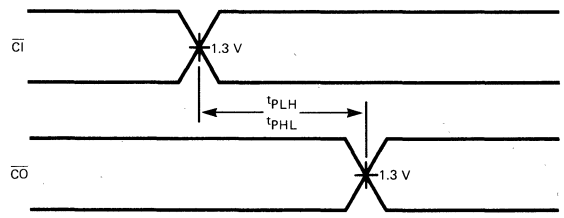


Fig. 4
CARRY-IN TO CARRY-OUT

AC CHARACTERISTICS – ALL MODES OF OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Carry In ($\overline{CI}$) to Carry Out ($\overline{CO}$)		14 10		ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Carry Out ($\overline{CO}$)		34 38		ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Carry Out ($\overline{CO}$)		34 38		ns	Figure 6

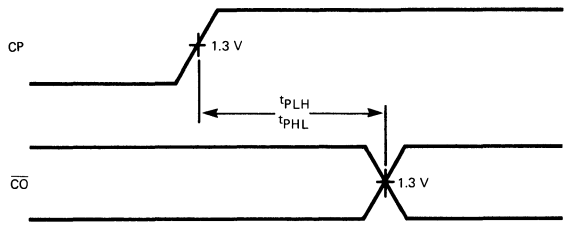


Fig. 5
CLOCK TO CARRY-OUT

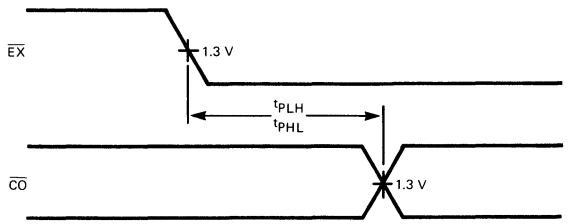


Fig. 6
EXECUTE TO CARRY-OUT

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE BRANCH (LOAD PC) OPERATION:
V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Outputs ($\overline{O}_0 - \overline{O}_3$)		28 36		ns	Figures 7 and 8
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$		20		ns	
t_h	Hold Time I_0, I_1 to Positive-Going $\overline{EX}$		0		ns	$\overline{EX}$ goes HIGH before CP, Figure 8
t_h	Hold Time, I_0, I_1 to Positive-Going CP		0		ns	CP goes HIGH before $\overline{EX}$, Figure 7
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		16		ns	Figures 7 and 8
t_h	Hold Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		0		ns	
t_{PWL}	$\overline{EX}$ Pulse Width		30		ns	$\overline{EX}$ Goes HIGH Before CP, Figure 8

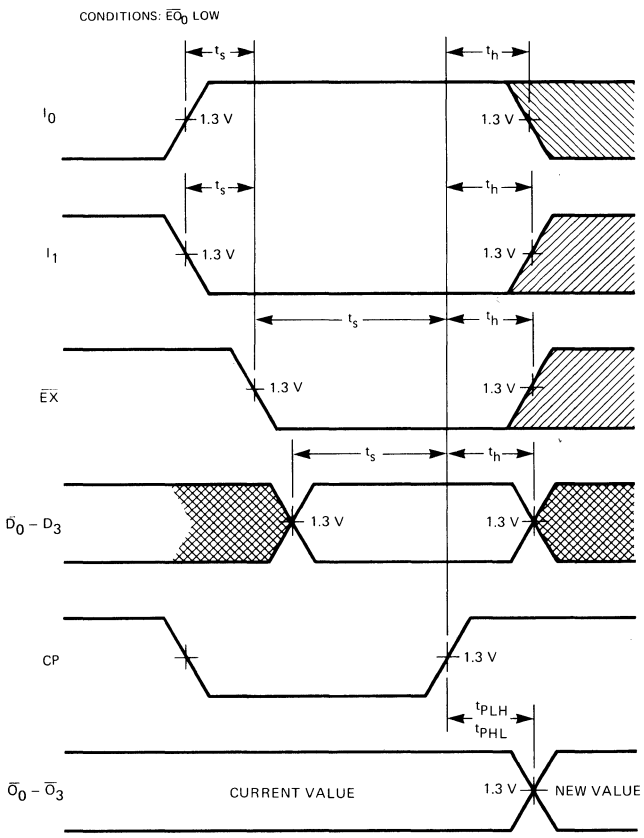


Fig. 7
BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

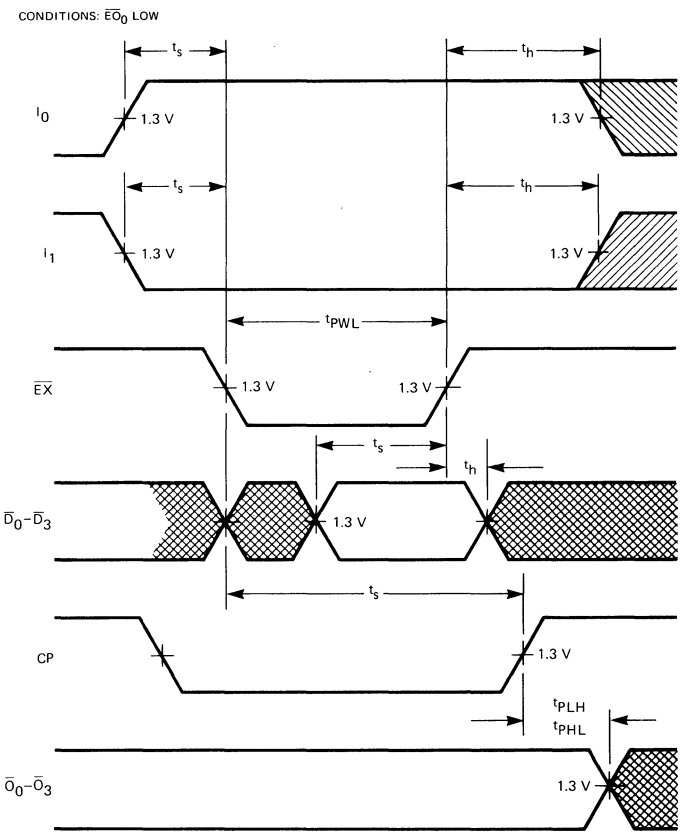


Fig. 8
BRANCH OPERATION, EX GOES HIGH BEFORE CP

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE CALL (PUSH) OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 9)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		35 55		ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Intermediate Value of $\overline{O}_0 - \overline{O}_3$		30 45		ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		20 40		ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1		20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1		0		ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees Intermediate Data on $\overline{O}_0 - \overline{O}_3$ while CP is LOW		45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees no Change in $\overline{O}_0 - \overline{O}_3$ While CP is LOW		0		ns	
$t_h\overline{EX}$	Hold Time, Positive-Going CP to Positive-Going $\overline{EX}$		0		ns	
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP		20		ns	
t_h	Hold Time, Positive-Going CP to $\overline{D}_0 - \overline{D}_3$		0		ns	

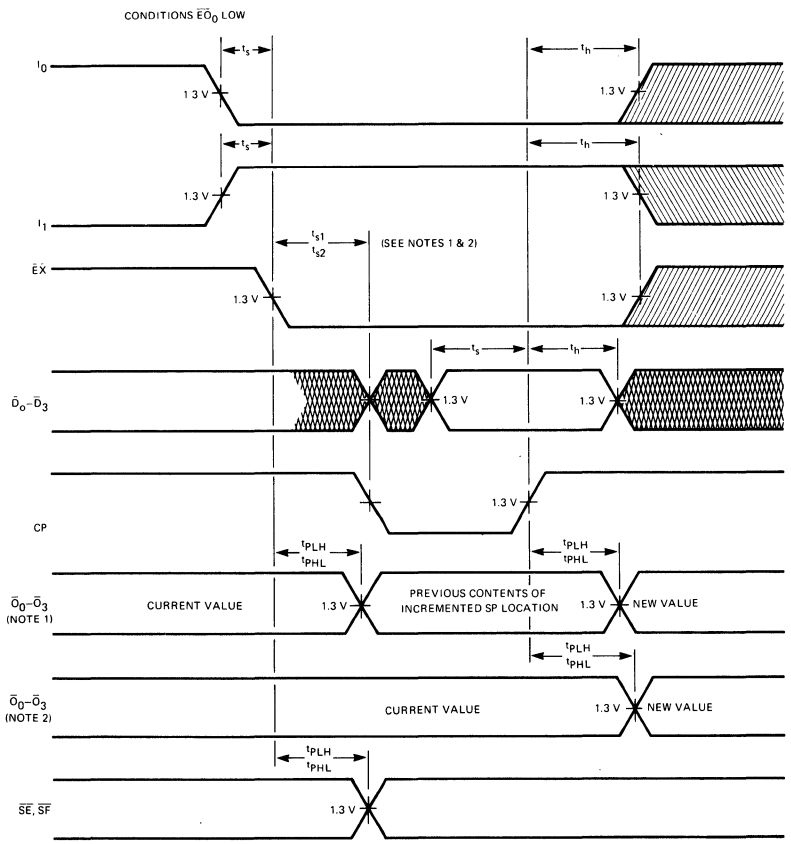


Fig. 9
CALL (PUSH) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW ($t_{S2}\overline{EX}$ is met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE RETURN (POP) OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 10)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Delay to New Value of $\overline{O}_0 - \overline{O}_3$		28 55		ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to New Value of $\overline{O}_0 - \overline{O}_3$		30 45		ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		20 40		ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1		20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1		0		ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees the New Value on $\overline{O}_0 - \overline{O}_3$ While CP is LOW		45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP. Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ must be met for Proper Operation		0		ns	
$t_{s3}\overline{EX}$	Set-Up Time, EX to Positive-Going CP. Either $t_{s3}\overline{EX}$ or $t_{s2}\overline{EX}$ (Above) must be met for Proper Operation.		30		ns	

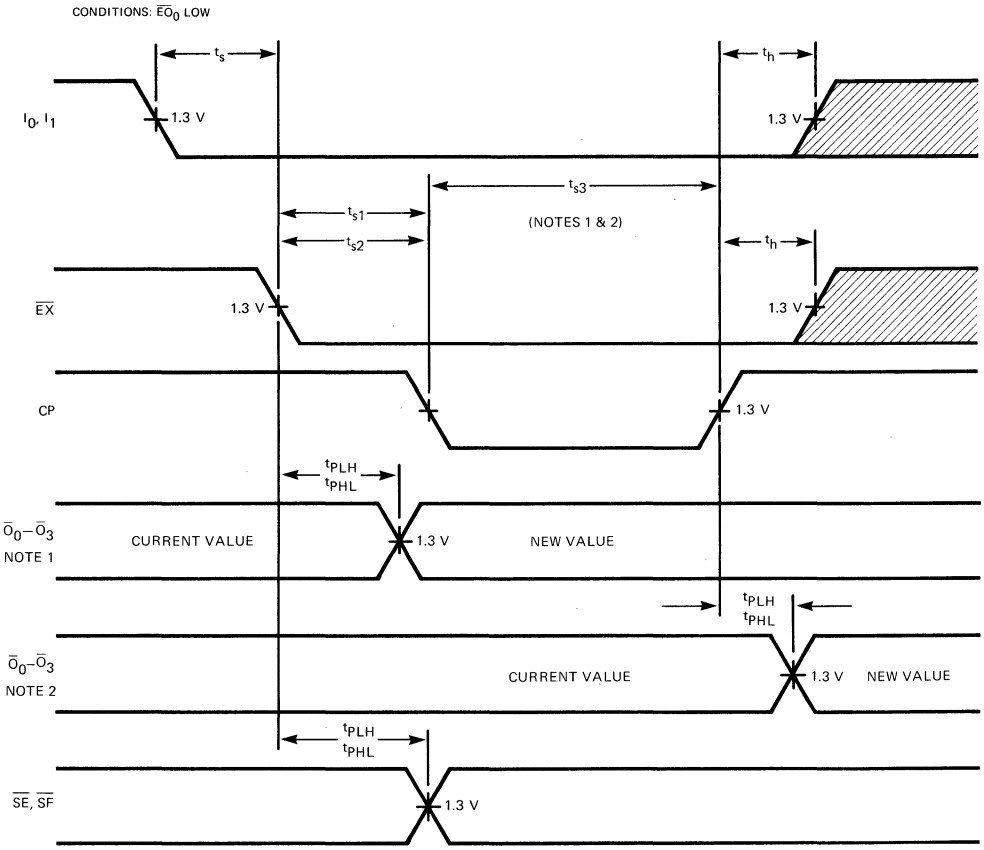


Fig. 10
RETURN (POP) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (either $t_{s2}EX$ or $t_{s3}\overline{EX}$ are met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS FOR THE FETCH OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay Positive-Going CP to Incremented Value of $\overline{O}_0 - \overline{O}_3$		29 38		ns	$\overline{EO}_0$, $\overline{CI}$ LOW, Figures 13 and 14
t_{PZL} t_{PZH}	Turn-On Delay, from CP or $\overline{EX}$ Whichever goes LOW last to $X_0 - X_3$		15 12		ns	$\overline{EO}_X$ LOW, Figures 11, 12, 13 and 14
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$		20		ns	Figures 11, 12, 13 and 14
t_h	Hold Time , I_0, I_1 to CP or $\overline{EX}$ whichever goes HIGH first		0		ns	
t_s	Set-Up Time, Negative Going $\overline{EX}$ to Positive-Going CP		25		ns	
t_s	Negative-Going $\overline{CI}$ to Positive-Going CP		20		ns	Fetch with Increment, Figures 13 and 14
t_h	Positive-Going $\overline{CI}$ to Negative-Going $\overline{EX}$		0			Iterative Fetch, Figures 11 and 12

CONDITIONS $\overline{EO}_0$ LOW, CP goes HIGH before $\overline{EX}$

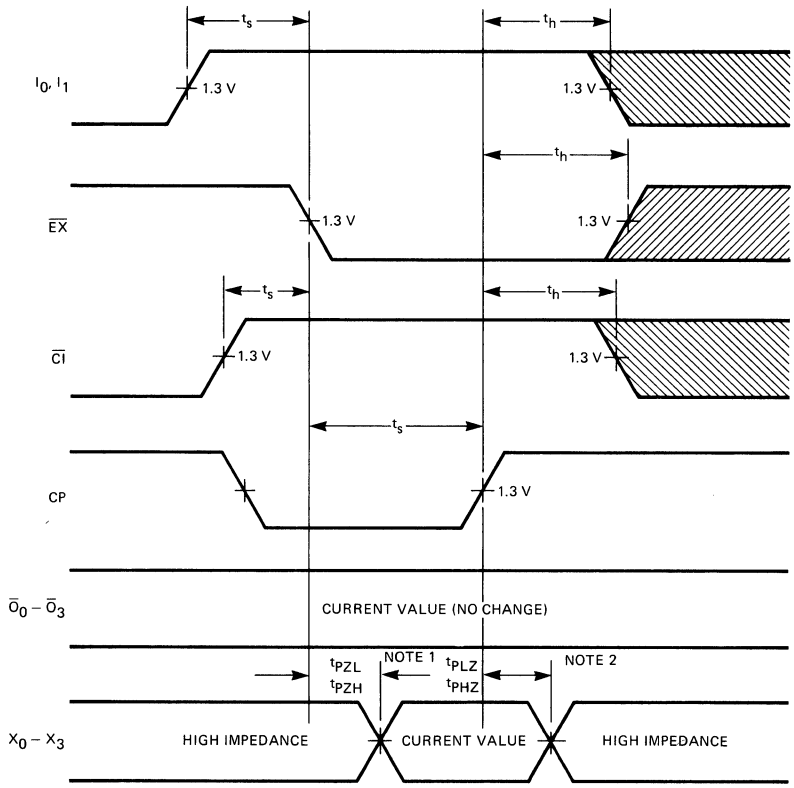


Fig. 11
ITERATIVE FETCH

CONDITIONS $\overline{EO}_0$ LOW, $\overline{EX}$ goes HIGH before CP

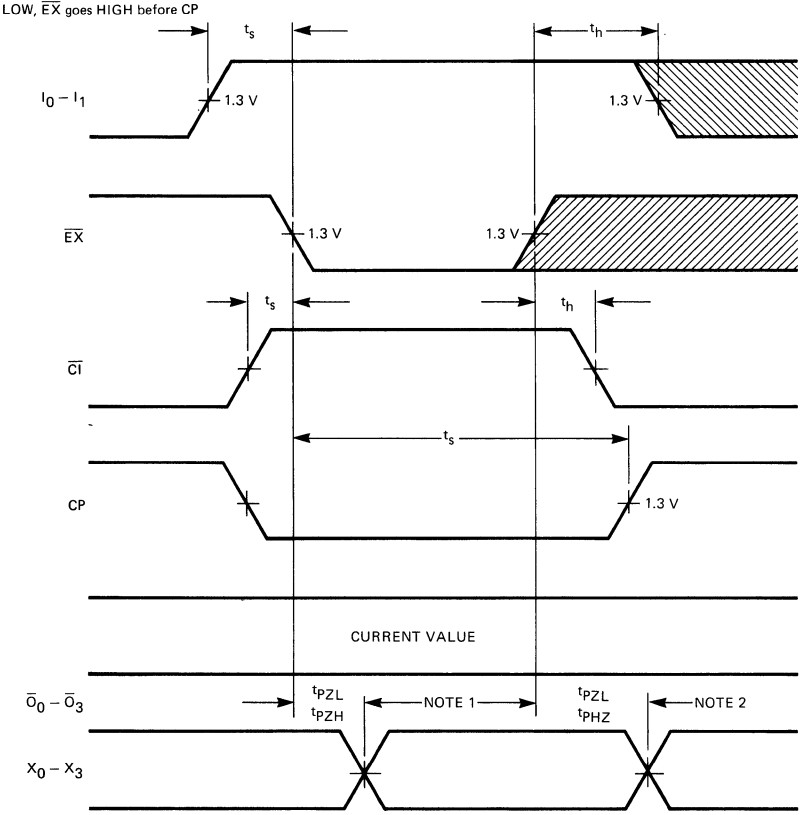


Fig. 12
ITERATIVE FETCH

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

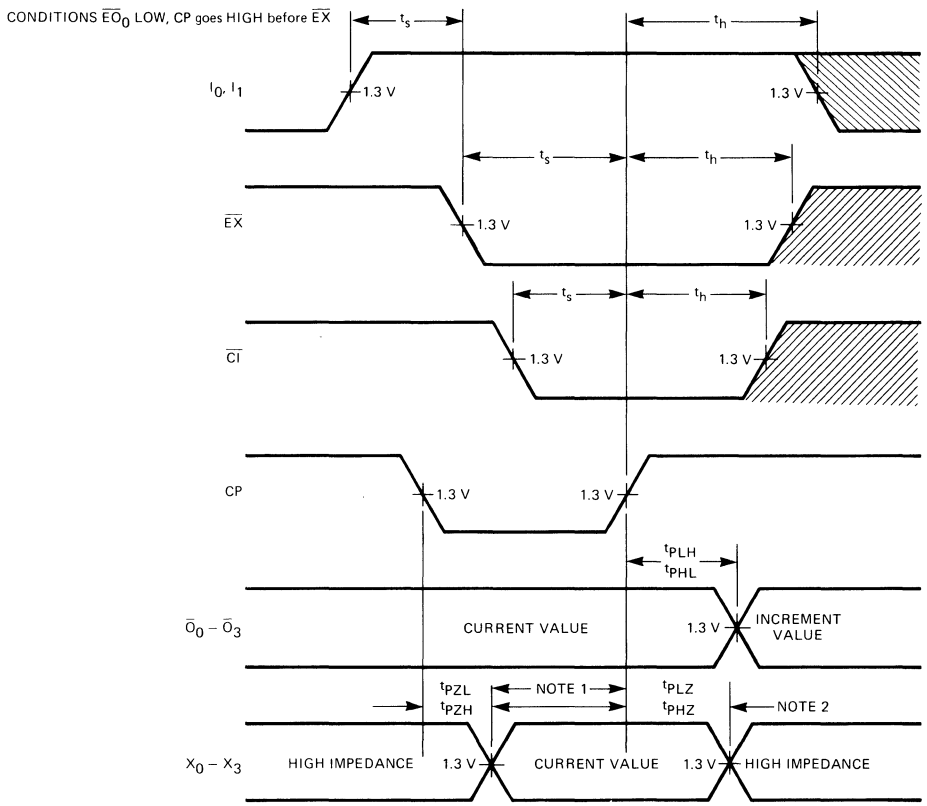


Fig. 13
FETCH WITH INCREMENT PC

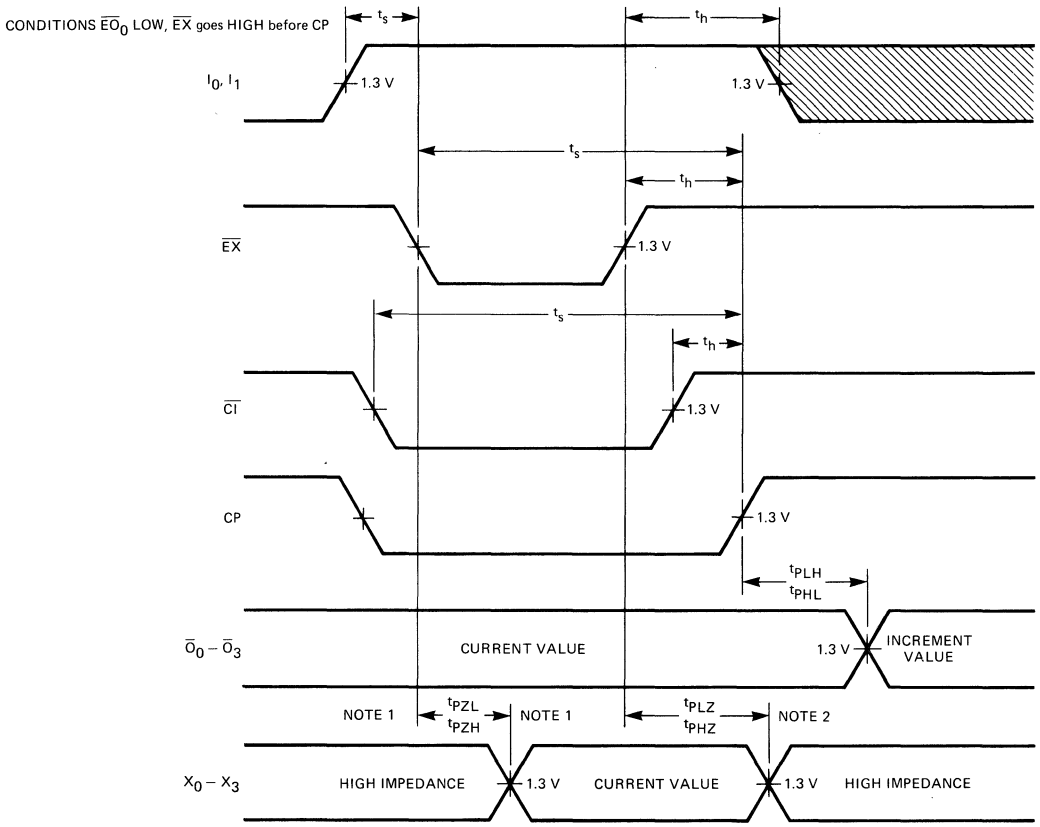


Fig. 14
FETCH OPERATION WITH INCREMENT PC

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

9407

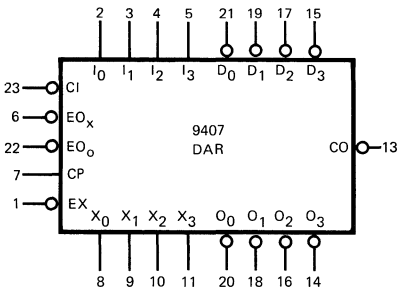
DATA ACCESS REGISTER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1), and Operand Address (R_2). The 9407 implements 16 instructions (see Table 1) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 10 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The 9407 is a member of Fairchild's MACROLOGIC family and is fully compatible with all TTL families.

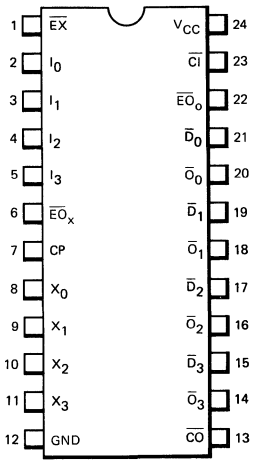
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **THREE 4-BIT REGISTERS**
- **16 INSTRUCTIONS FOR REGISTER MANIPULATION**
- **TWO SEPARATE OUTPUT PORTS, ONE TRANSPARENT**
- **RELATIVE ADDRESSING CAPABILITY**
- **3-STATE OUTPUTS**
- **OPTIONAL PRE OR POST ARITHMETIC**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



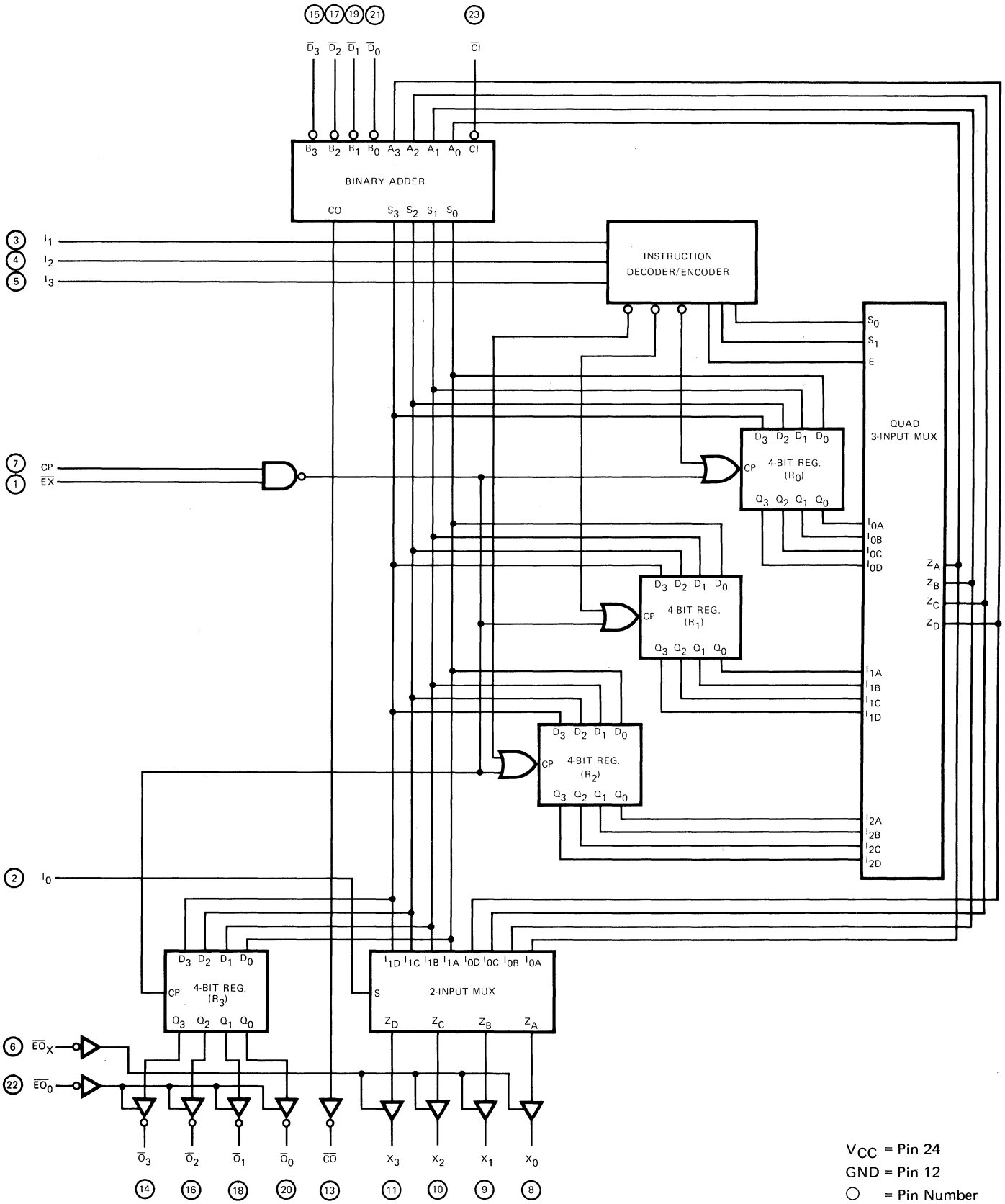
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
$I_0 - I_3$	Instruction Word Inputs	0.5 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW) (Note b)	0.5 U.L.	0.23 U.L.
$\overline{CO}$	Carry Output (Active LOW)	10 U.L.	5 U.L.
CP	Clock Input (L → H Edge-Triggered)	0.5 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_X$	Address Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}_0$	Data Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output Current measured at V_{OUT} = 0.5 V.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 9407 contains a 4-bit slice of three Registers (R_0–R_2), a 4-Bit Adder, a 3-state Address Output Buffer (X_0–X_3), and a separate Output Register with 3-state buffers ($\overline{O}_0$–$\overline{O}_3$), allowing output of the register contents on the data bus (refer to the Block Diagram). The DAR performs 16 instructions, selected by I_0–I_3, as listed in Table 1.

OPERATION – The 9407 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input, active LOW AND gate. For normal operation $\overline{EX}$ is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data Inputs $\overline{D}_0$–$\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines (I_1,I_2,I_3) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH CP transition writes the result from the Adder into a register (R_0–R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the 3-state Buffer controlling the address bus (X_0–X_3) independent of EX and CP. If I_0 is LOW, the multiplexer routes the output of the selected register directly into the 3-State Buffer controlling the Address Bus (X_0–X_3), independent of $\overline{EX}$ and CP.

34707 ARRAYS – The 9407 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – In a typical application, the register utilization in the DAR may be as follows: R_0 is the program counter (PC), R_1 is the stack pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction Fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC, and loaded into R_2 during the next microcycle.

TABLE 1
INSTRUCTION SET FOR THE 9407

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

L = LOW Level
H = HIGH Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, $\overline{CO}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
	$X_0 - X_3$, $\overline{O}_0 - \overline{O}_1$	XC	2.4	3.1			I_{OH} = −5.7 mA
V_{OL}	Output LOW Voltage, $\overline{CO}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
	$X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$			0.4	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			90	145	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{CW}	Clock Period (Note)		80		ns	
t_{PWH}	Clock Pulse Width (HIGH) (Note)		50			
t_{PWL}	Clock Pulse Width (LOW) (Note)	20				
t_s	Set-Up Time, $I_0 - I_3$ to Negative-Going Clock	20			ns	
t_h	Hold Time, $I_0 - I_3$ to Positive-Going Clock	0			ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	20			ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	0			ns	
t_sI	Set-Up Time, $\overline{CI}$ to Positive-Going Clock	5			ns	
t_hI	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to $\overline{O}_0 - \overline{O}_3$ (Note)		32 24 22		ns	$\overline{EO}_0$ LOW, Figure 3
t_{PLH} t_{PHL}	Instruction Code – $I_1 - I_3$ to $X_0 - X_3$		26 22		ns	$\overline{EO}_X$ LOW, I_0 LOW, Figure 1
t_{PLH} t_{PHL}	Instruction Code – $I_1 - I_3$ to $X_0 - X_3$		50 45		ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 1
t_{PLH} t_{PHL}	Positive-Going Internal Clock to $X_0 - X_3$		40 35		ns	$\overline{EO}_X$ LOW, I_0,
t_{PLH} t_{PHL}	Positive-Going Internal Clock to $X_0 - X_3$		65 55		ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 2
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to $X_0 - X_3$		30 30		ns	I_0 HIGH, $I_1 - I_3$ Stable $\overline{EO}_0$ LOW, Figure 4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CI}$ to $X_0 - X_3$		24 20		ns	$\overline{EO}_X$ LOW, Figure 5
t_{PLH} t_{PHL}	Propagation Delay I_0 to $X_0 - X_3$		24 32		ns	$\overline{EO}_X$ LOW, Figure 2
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Internal Clock to $\overline{CO}$		45 58		ns	Figure 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$		13 15 22		ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs $\overline{D}_0 - \overline{D}_3$ to $\overline{CO}$		13 24		ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Instruction Inputs $I_1 - I_3$ to $\overline{CO}$		30 32		ns	Figure 1
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs $\overline{O}_0 - \overline{O}_3$, $\overline{EO}_X$ to $X_0 - X_3$		13 18		ns	
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}_0$ to $\overline{O}_0$, $\overline{O}$ $\overline{EO}_X$ to $X_0 - X_3$		13 13		ns	

TIMING DIAGRAM

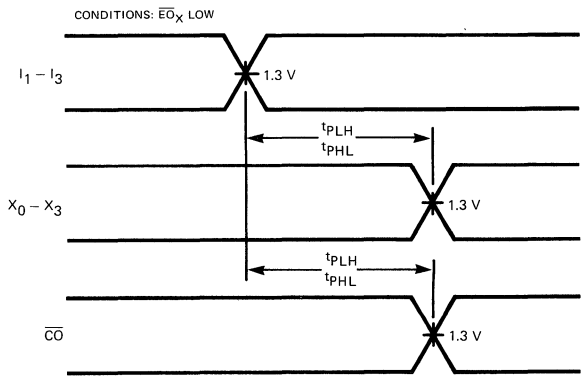


Fig. 1

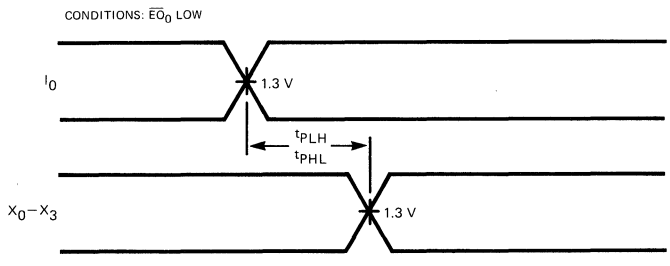


Fig. 2

NOTE:
The internal clock is generated from CP and $\overline{EX}$. The internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW.

TIMING DIAGRAM

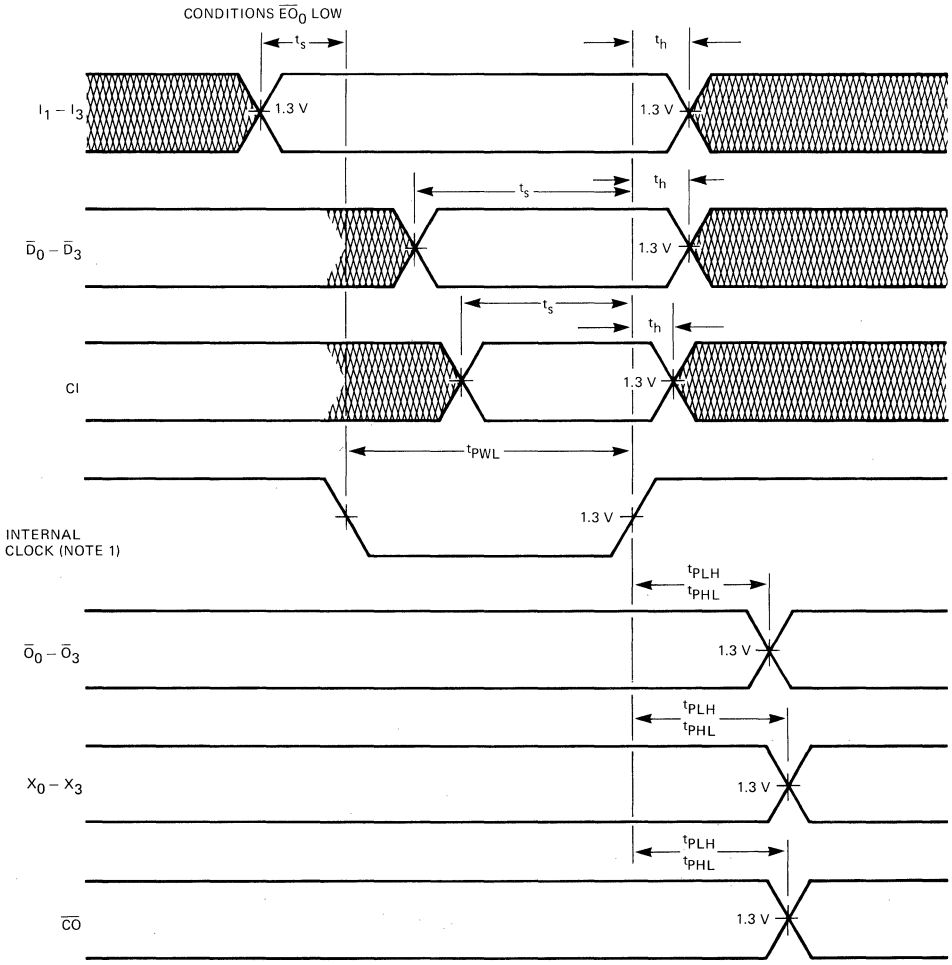


Fig. 3

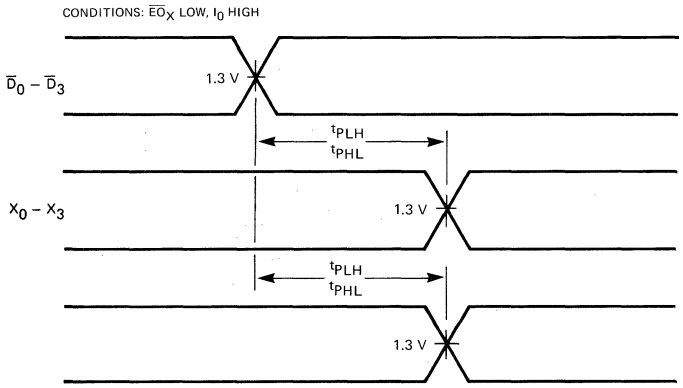


Fig. 4

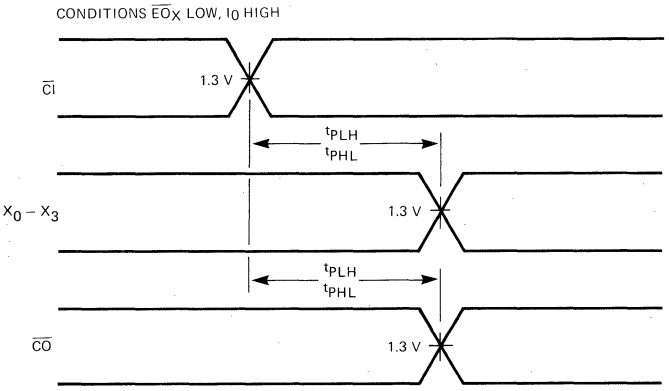


Fig. 5

9410

16 × 4 CLOCKED RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD MACROLOGIC

DESCRIPTION – The 9410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 9410 is a member of Fairchild's 9400 TTL MACROLOGIC family and is fully compatible with all TTL families.

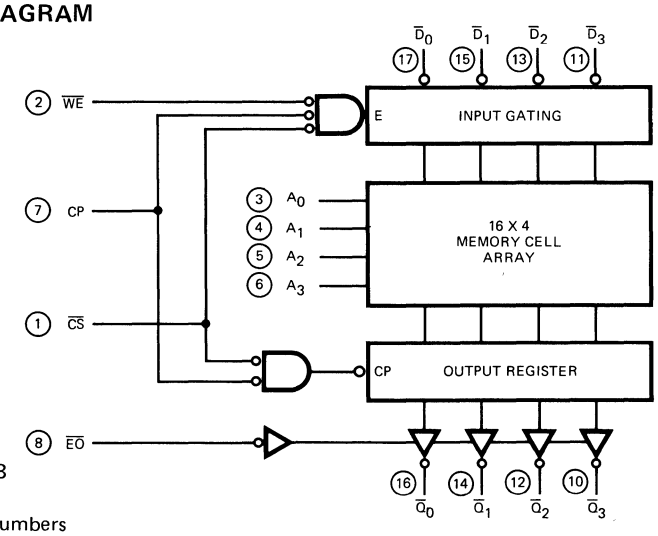
- **EDGE TRIGGERED OUTPUT REGISTER**
- **TYPICAL ACCESS TIME OF 35 ns**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **TYPICAL POWER OF 375 mW**
- **18-PIN PACKAGE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0-A_3	Address Inputs	0.5 U.L.	0.23 U.L.
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{CS}$	Chip Select Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
$\overline{WE}$	Write Enable Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Input (Outputs Change on LOW to HIGH Transition)	0.5 U.L.	0.23 U.L.
$\overline{Q}_0$-$\overline{Q}_3$	Outputs (Active LOW)	130 U.L.	10 U.L. (Note b)

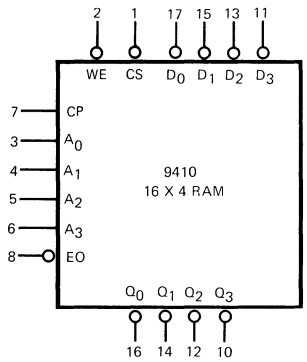
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) 10 LOW Unit Loads measured at 0.5 V.

BLOCK DIAGRAM



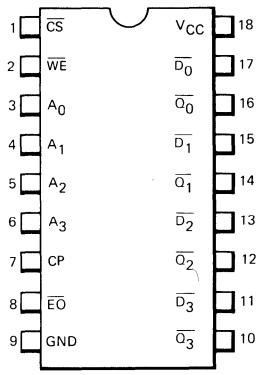
V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION

Write Operation – When the three Control Inputs: Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the Data Inputs ($\overline{D}_0$-$\overline{D}_3$) is written into the memory location selected by the Address Inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

Read Operation – Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the Address Inputs (A_0-A_3) is edge-triggered into the Output Register.

A 3-State Output Enable ($\overline{EO}$) controls the Output Buffers. When $\overline{EO}$ is HIGH the four Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the Outputs are determined by the state of the output register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			–0.9	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = –2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = –5.2 mA	
V_{OL}	Output LOW Voltage	XM & XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 0.8 V	
I_{OZL}	Output Off Current LOW				–100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 0.8 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		–30		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)	
I_{CCH}	Supply Current			75	110	mA	V_{CC} = MAX, Inputs Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25^\circ C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
READ MODE						
t_{PZH}	Enable Delay, Output Enable to Output		9	14	ns	Figure 2
t_{PZL}			9	14	ns	
t_{PHZ}	Disable Time, Output Enable to Output		5	8	ns	Figure 2
t_{PLZ}			5	8	ns	
t_{PLH}	Propagation Delay, Clock to Output		10	19	ns	Figure 3
t_{PHL}			11	19	ns	
t_sAR	Set-up Time to Read from Address to Clock	45	35		ns	Figure 3
t_hAR	Hold Time to Read from Address to Clock	0		0	ns	Figure 3
WRITE MODE						
t_W	Write Enable, Chip Select, or Clock Pulse Width Required to Write (Note a)	35	20		ns	Figure 4
t_sAW	Set-up Time Address to Write Enable (Note b)	5			ns	Figure 4
t_hAW	Hold Time Address to Write Enable (Note b)	0			ns	Figure 4
t_sDW	Set-up Time Data to Write Enable (Note b)	35	25		ns	Figure 4
t_hDW	Hold Time Data to Write Enable	0			ns	Figure 4

NOTES:

a) Writing occurs when $\overline{WE}$, $\overline{CE}$ and CP are LOW.
b) Assuming $\overline{WE}$ is utilized as Writing Strobe.

READ MODE AC PARAMETERS

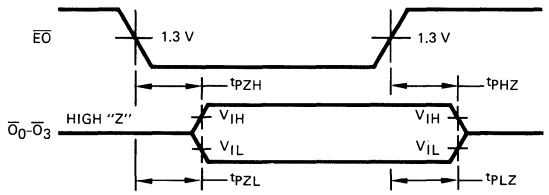
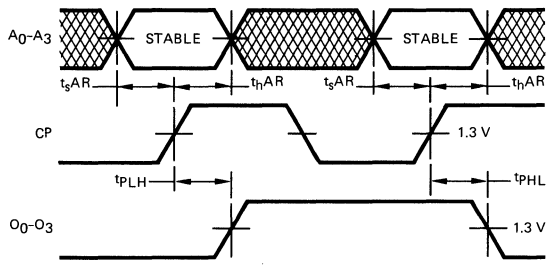


Fig. 2

PROPAGATION DELAY OUTPUT ENABLE TO DATA OUTPUTS

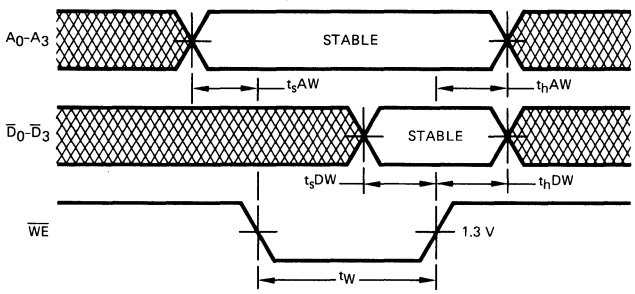


Other Conditions: $\overline{CS} = \overline{OE}$ = LOW

Fig. 3

PROPAGATION DELAY CLOCK TO DATA OUTPUTS, AND SET-UP AND HOLD TIMES ADDRESS TO CLOCK TO READ

WRITE MODE AC PARAMETERS



Other Conditions: $\overline{CS}$ = CP = LOW

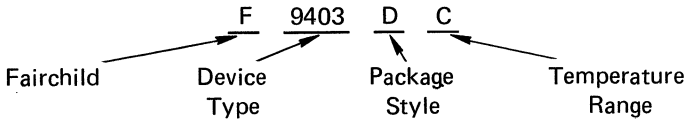
Fig. 4

WRITE ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES ADDRESS AND DATA TO WRITE ENABLE

ORDER AND PACKAGE INFORMATION

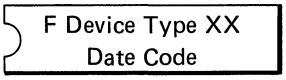
Fairchild digital integrated circuits may be ordered using a simplified purchasing code where the package style and temperature range are defined as follows:

PACKAGE STYLE
D = Dual In-Line – Ceramic (Hermetic)
P = Dual In-Line – Plastic



Temperature Range
Two Basic temperature grades are in common use: C = Commercial-Industrial, 0°C to +75°C; M = Military, –55°C to +125°C. Exact values and conditions are indicated on the data sheets.

Device Identification/Marking
All Fairchild standard catalog digital circuits will be marked as follows:

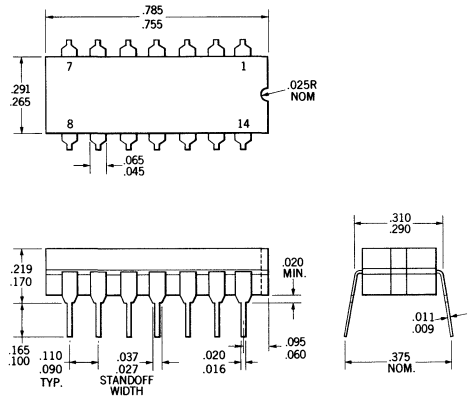


PACKAGE OUTLINES

CERAMIC PACKAGES – USED ON ALL DC AND DM DEVICES

7A

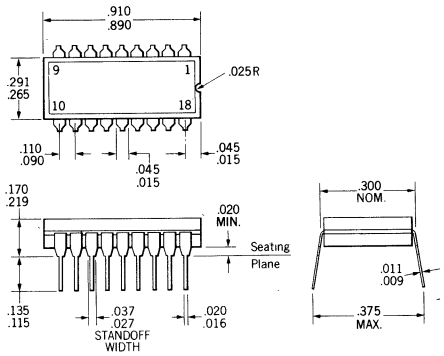
14-Pin Ceramic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

7D

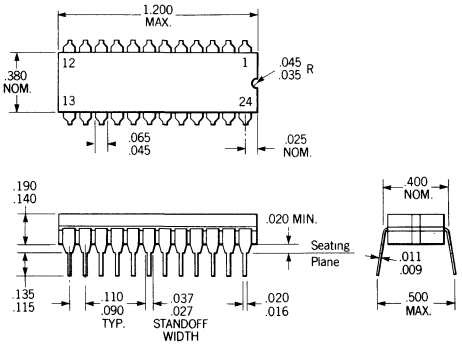
18-Pin Ceramic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

6Q

24-Pin Ceramic Dual In-Line



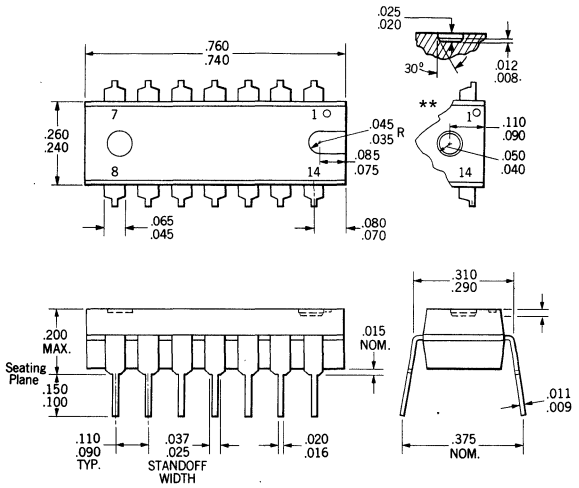
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

PACKAGE OUTLINES

PLASTIC PACKAGES – USED ON ALL PC DEVICES

9A

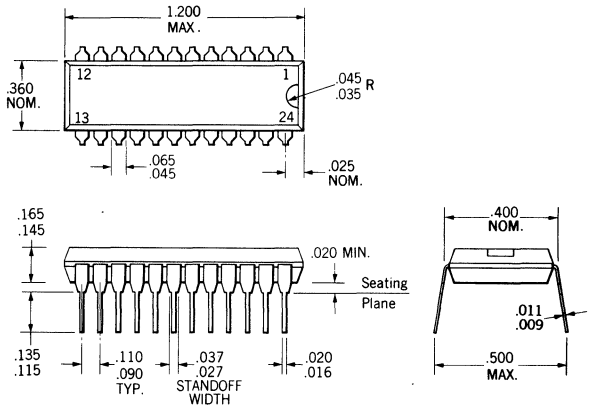
14-Pin Plastic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
Package material is silicone

9U

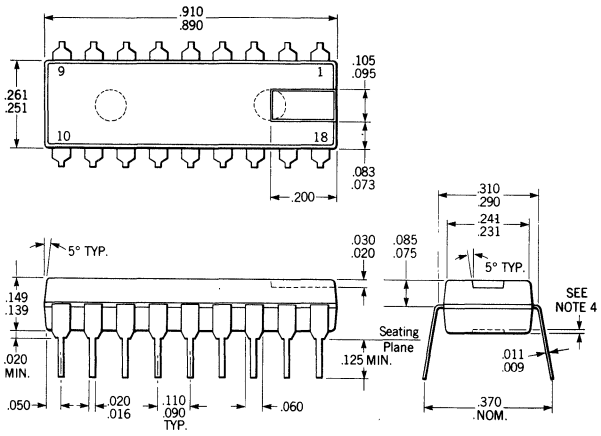
24-Pin Plastic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

9M

18-Pin Plastic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar

PLASTIC (PC) PRICING

DEVICE	1-24	25-99	100-999	Sample Availability
9401	12.75	10.85	8.75	NOW
9403	17.75	15.00	12.20	JUNE 18
9404	TBD			AUGUST
9405	24.00	20.25	15.95	JUNE 30
9406	16.95	14.30	11.65	JUNE 30
9407	TBD			AUGUST
9410	8.00	6.78	5.50	NOW