FAIRCHILD
A Schlumberger Company

F6854/F68A54/F68B54 Advanced Data Link Controller (ADLC)

Microprocessor Product

Description

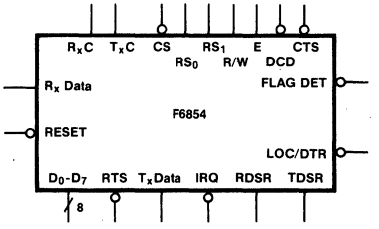
The F6854/F68A54/F68B54 Advanced Data Link Controllers (ADLC) perform the complex MPU/data communication link function for the Advanced Data Communication Control Procedure (ADCCP), High-level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling and loop configurations.

- **F6800 Compatible**
- **Protocol Features**
  - **Automatic Flag Detection and Synchronization**
  - **Zero Insertion and Deletion**
  - **Automatic Address Field Extension (Optional)**
  - **Extended Control Field (Optional)**
  - **Auto Extendable Logic Control Field (Optional)**
  - **Variable Word Length Information Field 5-, 6-, 7-, or 8-Bit**
  - **Automatic Frame Check Sequence Generation and Check**
  - **Abort Detection and Transmission**
  - **Idle Detection and Transmission**
- **Modem/Data Channel Control Lines**
- **Loop Mode**
- **Single 5 V Power Supply**
- **Enhanced Speed Options**
  F6854—1.0 MHz
  F68A54—1.5 MHz
  F68B54—2.0 MHz

Pin Names

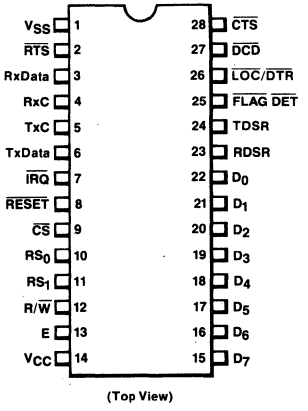
RxData	Receiver Serial Data Input
RxC	Receiver Data Timing Clock Input
TxC	Transmitter Data Timing Clock Input
$\overline{\text{RESET}}$	Chip Master Reset Input
$\overline{\text{CS}}$	Chip Select Input
RS_0, RS_1	Register Addressing Select Inputs
R/$\overline{\text{W}}$	Read/Write Input
E	System Control Clock Input
$\overline{\text{DCD}}$	Data Carrier Detect Input
$\overline{\text{CTS}}$	Clear-to-Send Input
D_0 - D_7	Bidirectional Data I/O Lines
$\overline{\text{RTS}}$	Request-to-Send Output
TxData	Transmitter Serial Data Output
$\overline{\text{IRQ}}$	Interrupt Request Output
RDSR	Receiver Data Service Request Output
TDSR	Transmitter Data Service Request Output
$\overline{\text{FLAG}}$ $\overline{\text{DET}}$	Flag Detect Output
$\overline{\text{LOC}}$/$\overline{\text{DTR}}$	Loop On-line Control/Data Terminal Ready Output
V_{SS}	Ground
V_{CC}	+5 V Power Supply

Logic Symbol



V_{CC} = Pin 14
V_{SS} = Pin 1

Connection Diagram
28-Pin DIP



(Top View)

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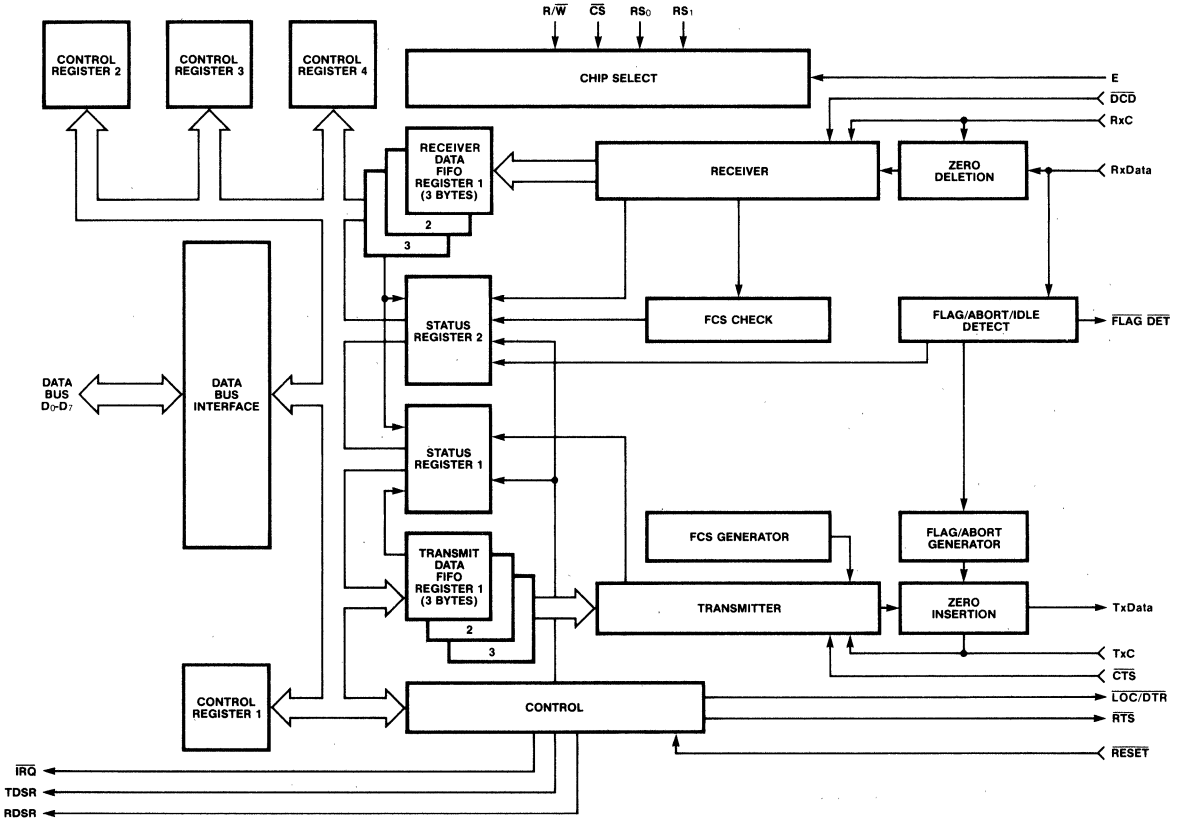
Block Diagram



Operation

Initialization

During a power-on sequence, the ADLC is reset via the Reset ($\overline{\text{RESET}}$) input and internally latched in a reset condition to prevent erroneous output transitions. The four Control Registers must be programmed prior to the release of the reset condition. The release of the reset condition is performed via software by writing a LOW into the Receiver Reset (RxRS) control bit and/or Transmitter Reset (TxRS) control bit. The release of the reset condition will be done after $\overline{\text{RESET}}$ has gone HIGH.

At any time during operation, writing a HIGH into the RxRS control bit or TxRS control bit causes the reset condition of the receiver or transmitter section.

Transmitter Operation

The Transmitter Data FIFO Register (Tx FIFO) cannot be pre-loaded when the transmitter section is in a reset state. After the reset release, the Flag/Mark Idle Select control bit (F/M Idle) selects either the mark idle state (inactive idle) or the flag time fill (active idle) state. This active or inactive mark idle state will continue until data is loaded into the Tx FIFO.

The availability of the Tx FIFO is indicated by the Transmitter Data Available/Frame Complete (TDRA/FC) status bit under the control of the 2-Byte/1-Byte Transfer (2/1-Byte) control bit. TDRA status is inhibited by the TxRS control bit or Clear-to-Send ($\overline{\text{CTS}}$) input being HIGH. When the 1-byte mode is selected, one byte of the Tx FIFO is available for data transfer when TDRA/FC goes

HIGH. When the 2-byte mode is selected, two successive bytes can be transferred when TDRA/FC goes HIGH.

The first byte (address field) should be written into the Tx FIFO at the frame-continue address. Then the transmission of a frame automatically starts. If the Transmitter is in a mark idle state, the transfer of an address causes an opening flag within two or three transmitter clock cycles. If the Transmitter has been in a time fill state, the current time fill flag being transmitted is assumed as an opening flag and the address field will follow it.

A frame continues as long as data is written into the Tx FIFO at the frame-continue address. The ADLC internally keeps track of the field sequence in the frame. The frame format is described in the Frame Format section.

The frame is terminated by one of two methods. The most efficient way to terminate the frame from a software standpoint is to write the last data character into the Tx FIFO frame-terminate address (RS_1, RS_0 = HH) rather than the Tx FIFO frame-continue address (RS_1, RS_0 = HL). An alternate method is to follow the last write of data in the Tx FIFO frame-continue address with the setting of the Transmit Last Data (Tx Last) control bit. Either method causes the last character to be transmitted and the Frame Check Sequence (FCS) field to be appended automatically along with a closing flag. Data for a new frame can be loaded into the Tx FIFO immediately after the old frame data if TDRA/FC is HIGH. The closing flag can serve as the opening flag of the next frame, or separate opening and closing flags may be transmitted. If a new frame is not ready to be transmitted, the ADLC will automatically transmit the active (flag) or inactive (mark) idle condition.

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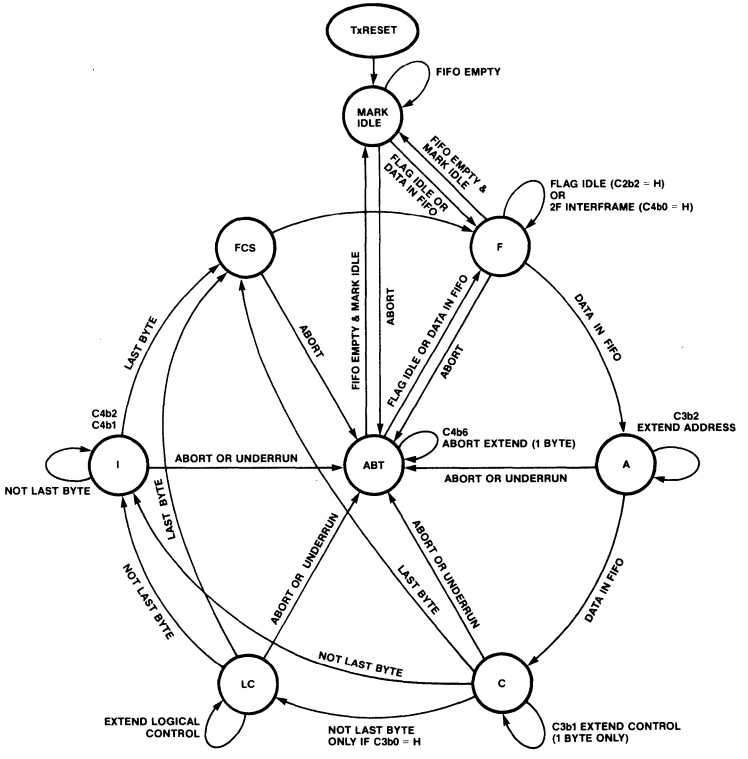
ADLC Transmitter State Diagram
(Cibi refers to Control Register bit)



Data Being Transmitted:
F = flag
A = address
C = (link) control

LC = logical control (optional)
I = information
FCS = frame check sequence
ABT = abort

If the Tx FIFO becomes empty at any time during frame transmission (the Tx FIFO has no data to transfer into the transmitter shift register during transmission of the last half of the next-to-last bit of a word), an underrun will occur and the Transmitter automatically terminates the frame by transmitting an abort. The underrun state is indicated by the Transmitter Underrun (TxU) status bit.

Any time the Transmit Abort (ABT) control bit is set, the Transmitter immediately aborts the frame (transmits at least eight consecutive 1s) and clears the Tx FIFO. If the Abort Extend (ABT_{EX}) control bit is set at the time, an idle (at least 16 consecutive 1s) is transmitted. An abort or idle in an out-of-frame condition can be useful to gain eight or 16 bits of delay. (For an example see Programming Considerations.)

The $\overline{CTS}$ input and Request-to-Send ($\overline{RTS}$) output are provided for a modem or other hardware interface.

The TDRA/FC status bit (when selected to be frame-complete status) can cause an interrupt upon frame completion (i.e., a flag or abort completion).

Details regarding the pin functions, Tx FIFO operation, and control and status registers are described in their respective sections.

Receiver Operation

Data and a pre-synchronized clock are provided to the ADLC receiver section by means of the Receiver Serial Data (RxData) and Receiver Data Timing Clock (RxC) inputs. The data is a continuous stream of binary bits with the characteristic that a maximum of five 1s can occur in succession unless abort, flag, or idling conditions occur. The Receiver continuously (on a bit-by-bit basis) searches for flags and aborts.

When a flag is detected, the Receiver establishes frame synchronization to the flag timing. If a series of flags is received, the Receiver resynchronizes to each flag.

If the frame is terminated before the internal buffer time expires (the frame data is less than 25 bits after an opening flag), the frame is simply ignored. Noise on RxData during time fill can cause this kind of invalid frame.

Once synchronization has been achieved and the internal buffer time (24 bit-times) expires, data will automatically transfer to the Receiver Data FIFO Register (RxFIFO). The Rx FIFO is clocked by System Control Clock (E) input to cause received data to move through the Rx FIFO to the last empty register location. The Receiver Data Available (RDA) status bit indicates when data is present in the last register (Register 3) for the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two Rx FIFO register locations (Registers 2 and 3) are full. If the data character present in the Rx FIFO is an address octet, Status Register 1 will exhibit an address present status condition. Data being available in the Rx FIFO causes an interrupt to be initiated (assuming the Receiver Interrupt Enable (RIE) control bit is enabled, RIE="1"). The MPU will read the ADLC status registers as a result of the interrupt or in its turn in a polling sequence. The Receiver Data Available (RDA) or Address Present (AP) status bits will indicate that receiver data is available and the MPU should subsequently read the Rx FIFO. The Interrupt Request (IRQ) and RDA status bits will then be reset automatically. If more than one character is received and is resident in the Rx FIFO, subsequent E clocks will cause the Rx FIFO to update and the RDA and IRQ status bits will again be set. In the 2-byte transfer mode both data bytes may be read on consecutive E cycles. The AP status bit provides for 1-byte transfers only.

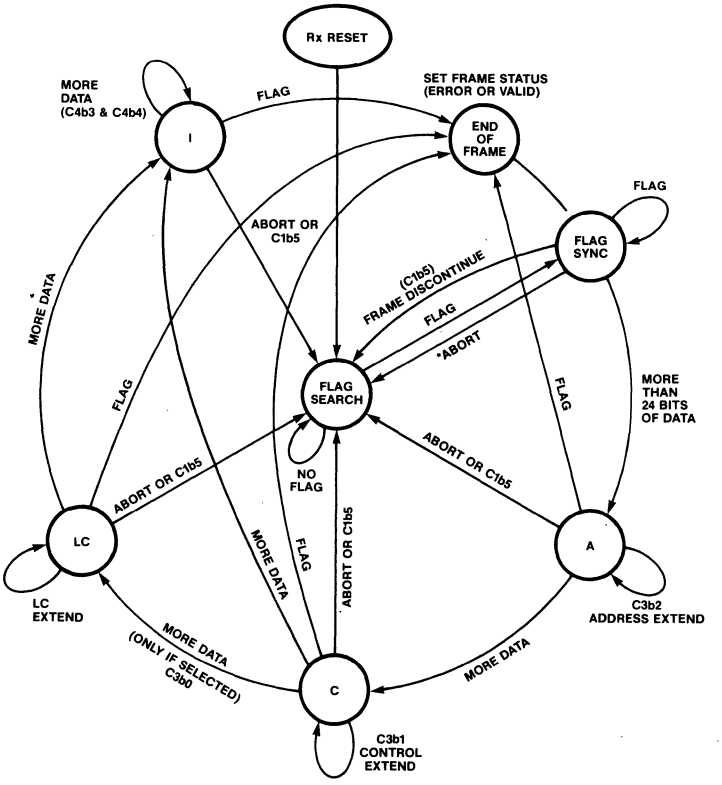
The sequence of each field in the received frame is automatically handled by the ADLC. The frame format is described in the Frame Format section.

When a closing flag is received, the frame is terminated. The 16 bits preceding the closing flag are regarded as the FCS and are not transferred to the MPU. Whatever data is present in the most significant byte portion of the receiver buffer register is right justified and transferred to the Rx FIFO. The frame boundary pointer, explained in the Rx FIFO Register section, is set simultaneously in the Rx FIFO. The frame boundary pointer sets the Frame Valid (FV) status bit (when the frame was completed with no error) or the Frame Check Sequence/Invalid Frame Error (ERR) status bit (when the frame was completed with error) when the last byte of the frame appears at the last location of the Rx FIFO. As long as the FV or ERR status bit is set, the data transfer from the second location of the Rx FIFO to the last location of the Rx FIFO is inhibited.

Any time the Rx Frame Discontinue (DISCONTINUE) control bit is set, the ADLC discards the current frame data in the ADLC without dropping flag synchronization. This feature can be used to ignore a frame which is addressed to another station.

The reception of an abort or idle is explained in the Frame Format section. The details regarding the pin functions, Rx FIFO operation, and control and status registers are described in their respective sections.

ADLC Receiver State Diagram

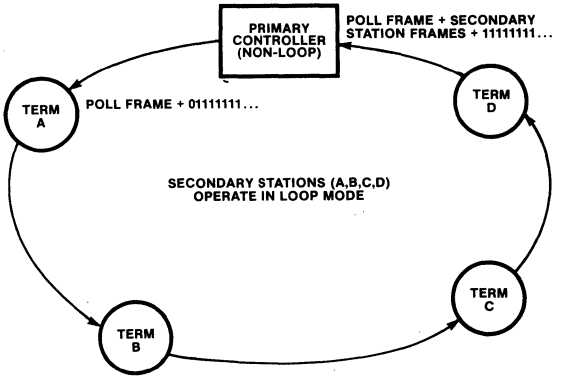


*Out-of-frame Abort (No IRQ)

Loop Mode Operation

In the loop mode the ADLC not only transmits and receives data frames in the manner previously described, but also has additional features for gaining and relinquishing loop control. In *Figure 1*, a configuration is shown which depicts loop mode operation. The system configuration shows a primary station and several secondary stations. The loop is always under control of the primary station. When the primary wants to receive data, it transmits a poll sequence and allows frame transmission to secondary stations on the loop. Each secondary is in series and adds one bit of delay to the loop. Secondary A in the figure receives data from the primary via the RxData input, delays the data one bit, and transmits it to secondary B via the Transmitter Serial Data (TxData) output. Secondaries B, C, and D operate in a similar manner. Therefore, data passes through each secondary and is received back by the primary controller.

Fig. 1 Typical Loop Configuration



Certain protocol rules must be followed that establish the manner by which the secondary station places itself on-loop (connects TxData to the loop), goes active on the loop (starts transmitting data on the loop), and goes off the loop (disconnects TxData). Otherwise, loop data to other stations down-loop would be interrupted. The data stream always flows the same way; the order in which secondary terminals are serviced is determined by the hardware configuration. The primary controller times the delay through the loop. Should it exceed n + 1 bit-times, where n is the number of secondary terminals on the loop, it will indicate a loop failure. Control is transferred to a secondary by transmitting a go-ahead signal following the closing flag of a polling frame (request for a response from the secondary) from the primary station. The go-ahead from the primary is a 0 and seven 1s followed by mark idling. The primary can abort its response request by interrupting its idle with flags. The secondary should immediately stop transmission and return control to the primary. When the secondary completes its frame, a closing flag is transmitted followed by all 1s. The primary detects the final 01111111 (go-ahead to the primary) and resumes control. Note that if a down-loop secondary (e.g., station D) needs to insert information following an up-loop station (e.g., station A), the go-ahead to station D is the last 0 of the closing flag from station A followed by 1s.

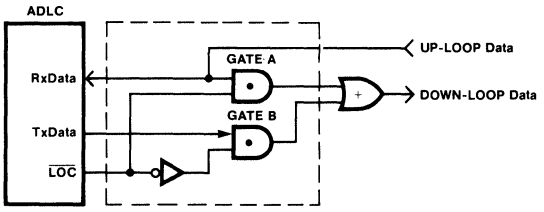
The ADLC in the primary station should operate in a non-loop, full-duplex mode. The ADLC in the secondaries should operate in a loop mode, monitoring up-loop data on RxData. The ADLC can recognize the necessary sequences in the data stream to automatically go on/off the loop and to insert its own station data. This procedure is summarized in *Table 1.*

1. Go On-loop — When the ADLC powers up, the terminal station will be off line. The first task is to become an active terminal on the loop. The ADLC must be connected to a loop link via an external switch as shown in *Figure 2.* After a hardware reset, the ADLC Loop On-line Control/Data Terminal Ready ($\overline{LOC}/\overline{DTR}$) output will be in the HIGH state and the up-loop receive data repeated through gate A to the down-loop stations. Any up-loop transmission will be received by the ADLC. The Loop/Non-Loop Mode (LOOP) control bit must be set to place the ADLC in the loop mode. The ADLC now monitors its RxData input for a string of seven consecutive 1s which will allow a station to go on line. The loop operation may be monitored by use of the Loop Status (LOOP) status bit. After power-up and reset, this bit is a LOW. When seven consecutive 1s are received by the ADLC, the $\overline{LOC}/\overline{DTR}$ output will go to a LOW level, disabling gate A (refer to *Figure 2),* enabling gate B and connecting the ADLC TxData output to the down-loop stations. The up-loop data is now repeated to the down-loop stations via the ADLC. A 1-bit delay is inserted in the data (in NRZI mode, there will be a 2-bit delay) as it circulates through the ADLC. The ADLC is now on-line and the LOOP status bit will be at a HIGH.

Table 1 Summary of Loop Mode Operation

State	Receiver (Rx) Section	Transmitter (Tx) Section	LOOP Status Bit
Off-loop	Rx section receives data from loop and searches for seven 1s (when the LOC/DTR control bit set) to go on-loop.	Inactive 1. NRZ Mode TxData output is maintained HIGH (mark). 2. NRZI Mode TxData output reflects the RxData input state delayed by one bit-time. (Not normally connected to loop.) The NRZI data is internally decoded to provide error-free transitions to on-loop mode.	L
On-loop	1. When GAP/TST control bit is set, Rx section searches for 01111111 pattern (the EOP or go-ahead) to become the active terminal on the loop. 2. When the LOC/DTR control bit is reset, Rx section searches for eight 1s to go off-loop.	Inactive 1. NRZ Mode TxData output reflects RxData input state delayed one bit-time. 2. NRZI Mode TxData output reflects RxData input state delayed two bit-times.	H
Active	Rx section searches for flag (an interrupt from the loop controller) at RxData input. Received flag causes FLAG DET output to go LOW. IRQ is generated if the RIE and FDSE control bits are set.	TxData originates within ADLC until GAP/TST control bit is reset and a flag or abort is completed, then returns to on-loop state.	L

Fig. 2 External Loop Logic



2. Go Active after Poll — The receiver section will monitor the up-link data for a general or addressed poll command; the Tx FIFO should be loaded with data so that when the go-ahead sequence of a 0 followed by seven 1s (01111111--) is detected, transmission can be initiated immediately. When the polling frame is detected, the Go Active On Poll/Test (GAP/TST) control bit must be set. A minimum of seven bit-times are available to set this control bit after the closing flag of the poll. When the go-ahead is detected by the Receiver, the ADLC will automatically change the seventh 1 to a 0 so that the repeated sequence out gate B in *Figure 2* is now an opening flag sequence (01111110). Transmission now continues from the Tx FIFO with data (address, control, etc.) as previously described. When the ADLC has gone active-on-poll, the LOOP status bit will go to a LOW. The Receiver searches for a flag, which indicates that the primary station is interrupting the current operation.

3. Go Inactive when On-loop — The GAP/TST control bit may be reset at any time during transmission. When the frame is complete (the closing flag or abort is transmitted), the loop is automatically released and the station reverts back to being just a 1-bit delay in the loop, repeating up-link data. If the GAP/TST control bit is not reset by software and the final frame is transmitted (F/M Idle control bit = LOW), then the Transmitter will mark idle and will not release the loop to up-loop data. A transmitter abort command would have to be used in this case in order to go inactive when on the loop. Also, if the Tx FIFO was not preloaded with data (address, control, etc.) prior to changing the go-ahead character to a flag, the ADLC will either transmit flags (active idle character) until data is loaded (when the F/M Idle control bit is HIGH) or will go into an underrun condition and transmit an abort (when the F/M Idle control bit is LOW). When an abort is transmitted, the GAP/TST control bit is reset automatically and the ADLC reverts to its repeating mode (TxData = delayed RxData). When the ADLC Transmitter lets go of the loop, the LOOP status bit will return to a HIGH, indicating normal on-loop retransmission of up-loop data.

4. Go Off-loop — The ADLC can drop off the loop (go off-line) similar to the way it went on-line. When the Loop On-line Control/DTR Control (LOC/DTR) control bit is reset, the ADLC receiver section looks for eight successive "1s" before allowing the $\overline{LOC}/\overline{DTR}$ output to return HIGH (the inactive state). Gate A in *Figure 2* will be enabled and gate B disabled allowing the loop to maintain continuity without disturbance. The LOOP status bit will show an off-line condition (logic HIGH).

Pin Functions

All inputs of the ADLC are high-impedance and TTL-level compatible. All outputs of the ADLC are compatible with standard TTL. Interrupt Request ($\overline{IRQ}$), however, is an open-drain output (no internal pull-up).

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Interface for MPU

Bidirectional Data I/O Lines (D_0-D_7)
These data bus I/O ports allow the data transfer between ADLC and system bus. The data bus drivers are 3-state devices that remain in the high-impedance (OFF) state except when the MPU performs an ADLC Read operation.

System Control Clock (E)
E activates the address inputs ($\overline{CS}$, RS_0 and RS_1) and Read/Write input ($R/\overline{W}$) and enables the data transfer on the data bus. E also moves data through the Tx FIFO and Rx FIFO. E should be a free-running clock, such as the F6800 MPU system clock.

Chip Select ($\overline{CS}$)
An ADLC Read or Write operation is enabled only when the $\overline{CS}$ input is LOW and the E input is HIGH ($E{\cdot}\overline{CS}$).

Register Addressing Select (RS_0, RS_1)
When the RS_0, RS_1 inputs are enabled by ($E{\cdot}\overline{CS}$), they select internal registers in conjunction with the $R/\overline{W}$ input and Address Control (AC) control bit. Register addressing is defined in *Table 2*.

Read/Write ($R/\overline{W}$)
The $R/\overline{W}$ input controls the direction of data flow on the data bus when it is enabled by ($E{\cdot}\overline{CS}$). The bidirectional Data Bus Interface acts as an output driver when $R/\overline{W}$ is HIGH, and as an input buffer when LOW. It also selects the read-only and write-only registers within the ADLC.

Chip Master Reset ($\overline{RESET}$)
The $\overline{RESET}$ input provides a means of resetting the ADLC from a hardware source. In the LOW state, the $\overline{RESET}$ input causes the following:

1. RxRS and TxRS are set, causing both the receiver and transmitter sections to be held in a reset condition.

2. Resets the following control bits: ABT, Request-to-Send Control (RTS), LOOP, and LOC/DTR.
3. Clears all stored status condition of the status registers.
4. The $\overline{RTS}$ and $\overline{LOC/DTR}$ ouputs go HIGH; TxData goes to the mark state (1s are transmitted).

When $\overline{RESET}$ returns HIGH (the inactive state), the transmitter and receiver sections will remain in the reset state until TxRS and RxRS are cleared via the data bus under software control. The control register bits affected by $\overline{RESET}$ cannot be changed when $\overline{RESET}$ is LOW.

Interrupt Request Output ($\overline{IRQ}$)
$\overline{IRQ}$ will be LOW if an interrupt situation exists and the appropriate interrupt enable has been set. The interrupt remains as long as the cause for the interrupt is present and E is set.

Clock and Data of Transmitter and Receiver
Transmitter Data Timing Clock (TxC)
The Transmitter shifts data on the negative transition of the TxC input. When the loop mode or test mode is selected, TxC should be the same frequency and phase as the RxC input. The data rate of the Transmitter should not exceed the E frequency.

Receiver Data Timing Clock (RxC)
The Receiver samples the data on the positive transition of the TxC input. RxC should be synchronized with RxData externally.

Transmitter Serial Data (TxData)
The serial data from the Transmitter is coded in NRZ or NRZI (zero complement) data format.

Receiver Serial Data (RxData)
The serial data to be received by the ADLC can be coded in NRZ or NRZI (zero complement) data format. The data rate of the Receiver should not exceed the E frequency. If a partial byte reception is possible at the end of a frame, the maximum data rate of the Receiver is indicated by the following relationship:

$$f_{RxC} \leq \frac{1}{2t_E + 300\ ns}$$

where t_E is the period of E.

Peripheral/Modem Control
Request-to-Send ($\overline{RTS}$)
The Request-to-Send output is controlled by the RTS control bit in conjunction with the state of the transmitter section. When the RTS control bit goes HIGH, the $\overline{RTS}$ output is forced LOW. When the RTS control bit returns LOW, the $\overline{RTS}$ output remains LOW until the end of the frame and there is no further data in the Tx FIFO for a new frame. The positive transition of $\overline{RTS}$ occurs after the completion of a flag, an abort, or when the RTS control bit is reset during a mark idling state. When the $\overline{RESET}$ input is LOW, the $\overline{RTS}$ output goes HIGH.

Clear-to-Send ($\overline{CTS}$)
The $\overline{CTS}$ input provides a real-time inhibit to the TDRA/FC status bit and its associated interrupt. The positive transition of $\overline{CTS}$ is stored within the ADLC to insure its occurrence will be acknowledged by the system. The stored CTS information and its associated IRQ status bit (if enabled) are cleared by writing a HIGH in the Clear Transmitter Status (CLR TxST) or the TxRS status bit.

Data Carrier Detect ($\overline{DCD}$)
The $\overline{DCD}$ input provides a real-time inhibit to the receiver section. A HIGH level on the $\overline{DCD}$ input resets and inhibits the receiver register, but data in the Rx FIFO from a previous frame is not disturbed. The positive transition of $\overline{DCD}$ is stored within the ADLC to insure that its occurrence will be acknowledged by the system. The stored DCD information and its associated IRQ status bit (if enabled) are cleared by means of the Clear Receiver Status (CLR RxST) or by the RxRS control bit.

Loop On-line Control/Data Terminal Ready ($\overline{LOC/DTR}$)
The $\overline{LOC/DTR}$ output serves as a $\overline{DTR}$ output in the non-loop mode or as an $\overline{LOC}$ output in the loop mode. When the $\overline{LOC/DTR}$ output performs the $\overline{DTR}$ function, it is turned on and off by means of the LOC/DTR control bit.

When the LOC/DTR control bit is HIGH, the $\overline{DTR}$ output will be LOW. In the loop mode the $\overline{LOC/DTR}$ output provides the means of controlling the external loop interface hardware to go on-line or off-line. When the LOC/DTR control bit is set and the loop has idled for seven bit-times or more (RxData = 01111111...), the $\overline{LOC/DTR}$ output will go LOW (on-line). When the LOC/DTR control bit is LOW and the loop has idled for eight bit-times or more, the $\overline{LOC/DTR}$ output will return HIGH (off-line). The $\overline{RESET}$ input being LOW will cause the $\overline{LOC/DTR}$ output to be HIGH.

Flag Detect ($\overline{FLAG\ DET}$)
The $\overline{FLAG\ DET}$ output indicates the reception of a flag and initiates an external time-out counter for the loop mode operation. The $\overline{FLAG\ DET}$ output goes LOW for one bit-time beginning at the last bit of the flag character, as sampled by RxC.

DMA Interface
Receiver Data Service Request (RDSR)
The RDSR output is provided primarily for use in DMA mode operation and indicates (when HIGH) that the Rx FIFO requests service (RSDR output reflects the RDA

status bit). If the prioritized status mode is selected, RDSR will be inhibited when any other receiver status conditions are present. RDSR goes LOW when the Rx FIFO is read.

Transmitter Data Service Request (TDSR)
The TDSR output is provided for DMA mode operation and indicates (when HIGH) that the Tx FIFO requests service. TDSR goes LOW when the Tx FIFO is loaded. TDSR is inhibited by the TxRS control bit being set, $\overline{RESET}$ being LOW, or $\overline{CTS}$ being HIGH. If the prioritized status mode is used, the TxU status bit also inhibits TDSR. TDSR reflects the TDRA/FC status bit except in the frame-complete mode.

ADLC Registers

Eight registers in the ADLC can be accessed via D_0-D_7 and RS_0, RS_1. The registers are defined as read-only or write-only according to the direction of information flow. The addresses of these registers are defined in *Table 2*. The Tx FIFO can be accessed by two different addresses, the frame-terminate address and the frame-continue address.

Table 2 Register Addressing

Register Selected	R/$\overline{W}$	RS_1	RS_0	Address Control Bit (C1b0)
Control Register 1	L	L	L	X
Control Register 2	L	L	H	L
Control Register 3	L	L	H	H
Transmitter Data FIFO Register (Frame Continue)	L	H	L	X
Transmitter Data FIFO Register (Frame Terminate)	L	H	H	L
Control Register 4	L	H	H	H
Status Register 1	H	L	L	X
Status Register 2	H	L	H	X
Receiver Data FIFO Register	H	H	X	X

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Receiver Data First-In First-Out Register (Rx FIFO)
The Rx FIFO consists of three 8-bit registers which are used for the buffer storage of received data. Data bytes are always transferred from a full register to an adjacent empty register; both phases of the E input clock are used for the data transfer. Each register has pointer bits which point the frame boundary. When these pointers appear at the last Rx FIFO location, they update the AP, FV or ERR status bits.

The RDA status bit indicates the state of the Rx FIFO. When RDA status bit is HIGH, the Rx FIFO is ready to be read. The RDA status is controlled by the 2/1-Byte control bit. When overrun occurs, the data in the first byte of the Rx FIFO are no longer valid.

Both the RxRS control and $\overline{RESET}$ input clear the Rx FIFO. Abort (in frame) and a HIGH level of $\overline{DCD}$ input also clear the Rx FIFO, but the last bytes of the previous frame, which are separated by the frame boundary pointer, are not disturbed.

Transmitter Data First-In First-Out Register (Tx FIFO)
The Tx FIFO consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Data is always transferred from a full register to an empty adjacent register; the transfer occurs on both phases of the E input clock. The Tx FIFO can be addressed by two different register addresses, the frame-continue address and the frame-terminate address. Each register has pointer bits which point to the frame boundary. When a data byte is written at the frame-continue address, the pointer of the first FIFO register is set. When a data byte is written at the frame-terminate address, the pointer of the first FIFO register is reset. The RxRS or ABT control bit resets all pointers. The pointer will shift through the Tx FIFO. When a positive transition is detected at the third FIFO register, the Transmitter initiates a frame with an open flag. When the negative transition is detected at the third FIFO register, the Transmitter closes a frame, appending the FCS and closing flag to the last byte.

The Tx Last control bit can be used instead of using the frame-terminate address. When the Tx Last control bit is set with a HIGH, the logic searches the last byte location in the Tx FIFO and resets the pointer.

The status of Tx FIFO is indicated by the TDRA/FC status bit. When TDRA/FC is HIGH, the Tx FIFO is available for loading data. The TDRA/FC status is controlled by the 2/1-Byte control bit. The Tx FIFO is reset by both TxRS and the $\overline{RESET}$ input. During this reset condition or when $\overline{CTS}$ input is HIGH, the TDRA/FC status bit is suppressed and data loading is inhibited.

ADLC Internal Register Structure

		RS_1, RS_0 = LL	RS_1, RS_0 = LH	RS_1, RS_0 = HL	RS_1, RS_0 = HH
	Bit No.	Status Register 1	Status Register 2	Receiver Data FIFO Register	Unused
Read-Only Registers	0	Receive Data Available (RDA)	Address Present (AP)	Bit 0	Same as RS_1, RS_0 = HL
	1	Status Register 2 Read Request (S2RQ)	Frame Valid (FV)	Bit 1	
	2	Loop Status (LOOP)	Inactive Idle Received (RxIdle)	Bit 2	
	3	Flag Detected (FD)	Abort Received (Rx ABT)	Bit 3	
	4	Clear-to-Send (CTS)	Frame Check Sequence/Invalid Frame Error (ERR)	Bit 4	
	5	Transmitter Underrun (TxU)	Data Carrier Detect (DCD)	Bit 5	
	6	Transmitter Data Register Available/ Frame Complete (TDRA/FC)	Receiver Overrun (OVRN)	Bit 6	
	7	Interrupt Request (IRQ)	Received Data Available (RDA)	Bit 7	

					Transmitter Data FIFO Register		
	Bit No.	Control Register 1	Control Register 2 (C1b0 = L)	Control Register 3 (C1b0 = H)	Frame Continue	Frame Terminate (C1b0 = L)	Control Register 4 (C1b0 = H)
Write-Only Registers	0	Address Control (AC)	Prioritized Status Enable (PSE)	Logic Control Field Select (LCF)	Bit 0	Bit 0	Double Flag/Single Flag Interframe Control ("FF"/"F")
	1	Receiver Interrupt Enable (RIE)	2-Byte/1-Byte Transfer (2/1-Byte)	Extended Control Field Select (C_{EX})	Bit 1	Bit 1	Transmitter 1 Word Length Select ($TxWLS_1$)
	2	Transmitter Interrupt Enable (TIE)	Flag/Mark Idle Select (F/M Idle)	Auto/Address Extend Mode (A_{EX})	Bit 2	Bit 2	Transmitter 2 Word Length Select ($TxWLS_2$)
	3	Receiver Data Service Request Mode (RDSR Mode)	Frame Complete/ TDRA Select (FC/TDRA Select)	01/11 Idle (01/11 Idle)	Bit 3	Bit 3	Receiver 1 Word Length Select ($RxWLS_1$)
	4	Transmitter Data Service Request Mode (TDSR Mode)	Transmit Last Data (Tx Last)	Flag Detect Status Enable (FDSE)	Bit 4	Bit 4	Receiver 2 Word Length Select ($RxWLS_2$)
	5	Rx Frame Discontinue (DISCONTINUE)	Clear Receiver Status (CLR RxST)	Loop/Non-Loop Mode (LOOP)	Bit 5	Bit 5	Transmit Abort (ABT)
	6	Receiver Reset (RxRS)	Clear Transmitter Status (CLR TxST)	Go Active on Poll/Test (GAP/TST)	Bit 6	Bit 6	Abort Extend (ABT_{EX})
	7	Transmitter Reset (TxRS)	Request-to-Send Control (RTS)	Loop On-Line Control/DTR Control (LOC/DTR)	Bit 7	Bit 7	NRZI (Zero Complement)/NRZ Select (NRZI/NRZ)

Control Register 1 (CR1)

RS_1	RS_0	R/$\overline{W}$	AC	7	6	5	4	3	2	1	0
L	L	L	X	TxRS	RxRS	DISCONTINUE	TDSR Mode	RDSR Mode	TIE	RIE	AC

b0 Address Control (AC) — AC provides another register select signal internally. The AC bit is used in conjunction with the RS_0, RS_1 and R/$\overline{W}$ inputs to select particular registers, as shown in *Table 2.*

b1 Receiver Interrupt Enable (RIE) — RIE enables/disables the interrupt request caused by the receiver section (HIGH = enable, LOW = disable).

b2 Transmitter Interrupt Enable (TIE) — TIE enables/disables the interrupt request caused by the Transmitter (HIGH = enable, LOW = disable).

b3 Receiver Data Service Request Mode (RDSR Mode) RDSR Mode provides the capability of operation with a bus system in the DMA mode when used in conjunction with the prioritized status mode. When RDSR Mode is set, an interrupt request caused by the RDA status bit is inhibited, and the ADLC does not request data transfer via the $\overline{IRQ}$ output.

b4 Transmitter Data Service Request Mode (TDSR Mode) — TDSR Mode provides the capability of operation with a bus system in the DMA mode when used in conjunction with the prioritized status mode. When TDSR Mode is set, an interrupt request caused by the TDRA/FC status bit is inhibited, and the ADLC does not request a data transfer via the $\overline{IRQ}$ output.

b5 Rx Frame Discontinue (DISCONTINUE) — When DISCONTINUE is set, the currently received frame is ignored and the ADLC discards the data of the current frame. DISCONTINUE is automatically reset when the last byte of the frame is discarded or when the ignored frame is aborted by receiving an abort or $\overline{DCD}$ failure.

b6 Receiver Reset (RxRS) — When RxRS is HIGH, the receiver section stays in the reset condition. All receiver sections, including the Rx FIFO and the receiver status bits in both status registers, are reset. (During reset, the stored DCD status is reset but the DCD status bit follows the $\overline{DCD}$ input.) RxRS is set by forcing a LOW level on the $\overline{RESET}$ input or by writing a HIGH into RxRS from the data bus. RxRS will be reset by writing a LOW from the data bus after $\overline{RESET}$ has gone HIGH.

b7 Transmitter Reset (TxRS) — When TxRS is HIGH, the transmitter section stays in the reset condition and transmits marks (1s). All transmitter sections, including the Tx FIFO and the transmitter status bits, are reset (Tx FIFO cannot be loaded). During reset, the stored $\overline{CTS}$ status is reset but the CTS status bit follows the $\overline{CTS}$ input. TxRS is set by forcing a LOW level on the $\overline{RESET}$ input or by writing a HIGH from the data bus. It will be reset by writing a LOW after $\overline{RESET}$ has gone HIGH.

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Control Register 2 (CR2)

RS_1	RS_0	R/$\overline{W}$	AC	7	6	5	4	3	2	1	0
L	H (C1b0 = L)	L	L	RTS	CLR TxST	CLR RxST	Tx Last	FC/TDRA Select	F/M Idle	2/1 Byte	PSE

b0 Prioritized Status Enable (PSE) — When PSE is set, the status bits in both status registers are prioritized as defined in the Status Register section. When PSE is LOW, the status bits indicate current status without bit suppression by other status bits. The exception to this rule is the CTS status bit which always suppresses the TDRA/FC status bit.

b1 2-Byte/1-Byte Transfer (2/1-Byte) — When 2/1-Byte is reset, the TDRA/FC and RDA status bits then will indicate the availability of their respective data FIFO registers for a single-byte data transfer. Similarly, if 2/1-Byte is set, the TDRA/FC and RDA status bits indicate when two bytes of data can be moved without a second status read.

b2 Flag/Mark Idle Select (F/M Idle) — F/M Idle Select selects flag characters or bit-by-bit mark idle for the time fill or the idle state of the Transmitter. When mark idle is selected, go-ahead code can be generated for loop operation in conjunction with the 01/11 Idle control bit (HIGH = flag time fill, LOW = mark idle).

b3 Frame Complete/TDRA Select (FC/TDRA Select) — FC/TDRA Select selects TDRA status or FC status for the TDRA/FC status bit indication (HIGH = FC status, LOW = TDRA status).

b4 Transmit Last Data (Tx Last) — Tx Last provides another method to terminate a frame. When the Tx Last is set just after loading a data byte, the ADLC assumes the byte is the last byte and terminates the frame by appending Cyclic Redundancy Check Character (CRCC) and a closing flag. This control bit is useful for DMA operation. Tx Last automatically returns to the LOW state.

b5 Clear Receiver Status (CLR RxST) — When a HIGH is written into CLR RxST, a reset signal is generated for the receiver status bits in Status Registers 1 and 2 (except AP and RDA bits). The reset signal is enabled only for the bits which have been present during the last read status operation. CLR RxST automatically returns to the LOW state.

b6 Clear Transmitter Status (CLR TxST) — When a HIGH is written into CLR TxST, a reset signal is generated for the transmitter status bits in Status Register 1 (except TDRA/FC). The reset signal is enabled for the bits which have been present during the last read status operation. CLR TxST automatically returns to the LOW state.

b7 Request-to-Send Control (RTS) — RTS, when HIGH, causes the $\overline{RTS}$ output to be LOW (the active state). When the RTS bit returns LOW and data is being transmitted, the $\overline{RTS}$ output remains LOW until the last character of the frame (the closing flag or abort) has been completed and the Tx FIFO is empty. If the Transmitter is idling when the RTS bit returns LOW, the $\overline{RTS}$ ouput will go HIGH (the inactive state) within two bit-times.

Control Register 3 (CR3)

RS_1 L RS_0 H $R/\overline{W}$ L AC H (C1b0 = H)

7	6	5	4	3	2	1	0
LOC/DTR	GAP/TST	LOOP	FDSE	01/11 Idle	A_{EX}	C_{EX}	LCF

b0 Logic Control Field Select (LCF) — LCF causes the first byte(s) of data belonging to the information field to remain 8-bit characters until the logic control field is complete. The logic control field (when selected) is an automatically extendable field which is extended when bit 7 of a logic control character is HIGH. When LCF is reset, the ADLC assumes no logic control field is present for either the transmitted or received data channels. When the logic control field is terminated, the word length of the information data is then defined by Rx or Tx WLS_1 and WLS_2.

b1 Extended Control Field Select (C_{EX}) — When the C_{EX} bit is HIGH, the control field is extended and assumed to be 16 bits. When C_{EX} is LOW, the control field is assumed to be eight bits.

b2 Auto/address Extend Mode (A_{EX}) — A_{EX}, when LOW, allows a full eight bits of the address octet to be utilized for addressing, because address extension is inhibited. When A_{EX} is HIGH, bit 0 of address octet equal to 0 causes the address field to be extended by one octet. The exception to this automatic address field extension is when the first address octet is all 0s (the null address).

b3 01/11 Idle (01/11 Idle) — The 01/11 Idle control bit determines whether the inactive (mark) idle condition begins with a 0 or not. If 01/11 Idle is set, the closing flag (or abort) will be followed by a 011111... pattern. This is required of the controller for the go-ahead character in the loop mode. When 01/11 Idle is reset, the idling condition will be all 1s.

b4 Flag Detect Status Enable (FDSE) — FDSE enables the Flag Detected (FD) status bit in Status Register 1 to indicate the occurrence of a received flag character. The status indication will be accompanied by an interrupt if the RIE control bit is set. Flag detection will cause the $\overline{FLAG}$ $\overline{DET}$ output to go LOW for one bit-time regardless of the state of FDSE.

b5 Loop/Non-Loop Mode (LOOP) — When LOOP is set, loop mode operation is selected and the GAP/TST control bit, LOC/DTR control bit and $\overline{LOC}/\overline{DTR}$ output are selected to perform the loop control functions. When LOOP is reset, the ADLC operates in the point-to-point data communications mode.

b6 Go Active on Poll/Test (GAP/TST) — In the loop mode GAP/TST is used to respond to the poll sequence and to begin transmission. When GAP/TST is set, the Receiver searches for the go-ahead (or end-of-poll, EOP). The Receiver go-ahead is converted to an opening flag and the ADLC starts its own transmission. When GAP/TST is reset during the transmission, the end of the frame (the completion of flag or abort) causes the termination of the go-active-on-poll operation and the RxData to TxData link is reestablished. The ADLC then returns to the loop-on-line state.

In the non-loop mode GAP/TST is used for self-test purposes. If GAP/TST is set, the TxData output is connected to the RxData input internally, and provides a loop-back feature. For normal operation, the GAP/TST bit should be reset.

b7 Loop On-line Control/DTR Control (LOC/DTR) — In the loop mode LOC/DTR is used to go on-line or to go off-line. When LOC/DTR is set, the ADLC goes to the on-line state after seven consecutive 1s occur at the RxData input. When LOC/DTR is reset, the ADLC goes to the off-line state after eight consecutive 1s occur at the RxData input.

In the non-loop mode the LOC/DTR bit directly controls the $\overline{LOC}/\overline{DTR}$ output state (HIGH = $\overline{DTR}$ output goes to LOW level, LOW = $\overline{DTR}$ output goes to HIGH level).

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Control Register 4 (CR4)

RS_1	RS_0	$R/\overline{W}$	AC	7	6	5	4	3	2	1	0
H	H (C1b0 = H)	L	H	NRZI/NRZ	ABT_{EX}	ABT	$RxWLS_2$	$RxWLS_1$	$TxWLS_2$	$TxWLS_1$	"FF"/"F"

b0 Double Flag/Single Flag Interframe Control ("FF"/"F") — "FF"/"F" determines whether the Transmitter will transmit separate closing and opening flags when frames are transmitted successively. When the "FF"/"F" control bit is LOW, the closing flag of the first frame will serve as the opening flag of the second frame; when HIGH, independent opening and closing flags will be transmitted.

b1, b2 Transmitter Word Length Select ($TxWLS_1$, $TxWLS_2$)- $TxWLS_1$ and $TxWLS_2$ are used to select the word length of the Transmitter information field. The encoding format is shown in *Table 3.*

b3, b4 Receiver Word Length Select ($RxWLS_1$, $RxWSL_2$) — $RxWLS_1$ and $RxWLS_2$ are used to select the word length of the Receiver information field. The encoding format is shown in *Table 3.*

b5 Transmit Abort (ABT) — ABT causes an abort (at least eight bits of 1 in succession) to be transmitted. The abort is initiated and the Tx FIFO is cleared when ABT goes HIGH. Once abort begins, the ABT bit assumes the LOW state.

b6 Abort Extended (ABT_{EX}) — If ABT_{EX} is set, the abort code initiated by ABT is extended at least 16 bits of consecutive 1s, the mark idle state.

b7 NRZI (Zero Complement)/NRZ Select (NRZI/NRZ) NRZI/NRZ selects the transmit/receive data format to be NRZI or NRZ in both loop mode or non-loop mode operation. When the NRZI mode is selected, a 1-bit delay is added to the transmitted data (TxData) to allow for NRZI encoding (HIGH = NRZI, LOW = NRZ).

Note
NRZI coding — The serial data remains in the same state to send a binary 1 and switches to the opposite state to send a binary 0.

Table 3 I-Field Character Length Select

WLS_1	WLS_2	I-Field Character Length
L	L	5 bits
H	L	6 bits
L	H	7 bits
H	H	8 bits

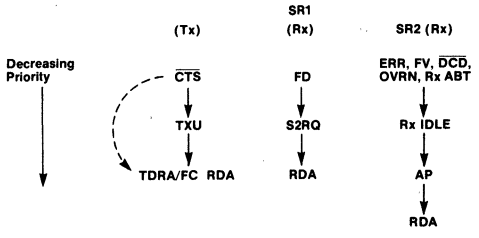
Status Registers
Status Register 1 is the main status register. The $\overline{IRQ}$ bit indicates whether the ADLC requests service or not. The S2RQ bit indicates whether any bits in Status Register 2 request service. TDRA/FC and RDA, because they are most often used, are located in bit positions that are more convenient to test. RDA reflects the state of the RDA bit in Status Register 2.

Status Register 2 provides the detailed status information contained in the S2RQ bit, and these bits reflect receiver status.

The prioritized status mode provides maximum efficiency in searching the status bits and indicates only the most important action required to service the ADLC. The priority trees of both status registers are provided in *Figure 3.*

Reading the status register is a non-destructive process. The method of clearing status depends upon the bit function and is discussed for each bit in the register.

Fig. 3 Status Register Priority Tree (PSE = 1)



* Prioritized even when PSE = 0

Note
Status bit above will inhibit one below it.

Status Register 1 (SR1)

RS_1	RS_0	R/$\overline{W}$	AC	7	6	5	4	3	2	1	0
L	L	H	X	IRQ	TDRA/FC	TXU	CTS	FD	LOOP	S2RQ	RDA

b0 Receiver Data Available (RDA) — The RDA status bit reflects the state of the RDA status bit in status Register 2. It provides the means of achieving data transfers of received data in the full-duplex mode without having to read both status registers.

b1 Status Register 2 Read Request (S2RQ) — All the status bits (stored conditions) of Status Register 2 (except RDA) are logically ORed and indicated by the S2RQ status bit. Therefore S2RQ indicates when Status Register 2 needs to be read. When S2RQ is LOW, it is not necessary to read Status Register 2. The bit is cleared when the appropriate bits in Status Register 2 are cleared or when RxRS is used.

b2 Loop Status (LOOP) — The LOOP status bit is used to monitor the loop operation of the ADLC. This bit does not cause an IRQ. When non-loop mode is selected, LOOP stays LOW; when loop mode is selected, the LOOP goes to HIGH during on-loop condition. When ADLC is in an off-loop condition or go-active-on-poll condition, the LOOP status bit is LOW.

b3 Flag Detected (FD) — The FD status bit indicates that a flag has been received if the Flag Detect Status Enable control bit has been set. FD goes HIGH at the last bit of the flag character received (when the $\overline{FLAG}$ $\overline{DET}$ output goes LOW) and is stored until cleared by clear RxST or RxRs.

b4 Clear-To-Send (CTS) — The $\overline{CTS}$ input positive transition is stored in Status Register 1 and causes an IRQ (if enabled). The stored CTS condition and its IRQ are cleared by CLR TxST or TxRS control bit. After the stored status is reset, the CTS status bit reflects the state of the $\overline{CTS}$ input.

b5 Transmitter Underrun (TxU) — When the transmitter runs out of data during a frame transmission, an underrun occurs and the frame is automatically terminated by transmitting an abort. The underrun condition is indicated by the TxU status bit. TxU can be cleared by means of the CLK TxST control bit or by TxRS.

b6 Transmitter Data Register Available/Frame Complete (TDRA/FC) — The TDRA/FC status bit serves two purposes, depending upon the state of the FC/TDRA Select control bit. When TDRA/FC serves as a TDRA status bit, it indicates that data (to be transmitted) can be loaded into the Tx FIFO. The first register (Register 1) of the Tx FIFO being empty (TDRA = HIGH) will be indicated by the TDRA/FC status bit in the 1-byte transfer mode. The first two registers (Registers 1 and 2) must be empty for TDRA to be HIGH when in the 2-byte transfer mode. TDRA/FC is inhibited by TxRS or $\overline{CTS}$ being HIGH.

When the frame-complete mode of operation is selected, the TDRA/FC status bit goes HIGH when an abort is transmitted or when a flag is transmitted with no data in the Tx FIFO. The bit remains HIGH until cleared by resetting the FC/TDRA Select or setting the TxRS control bit.

b7 Interrupt Request (IRQ) — The Interrupt Request status bit indicates when the $\overline{IRQ}$ output is in the active state ($\overline{IRQ}$ output = LOW). The IRQ status bit is subject to the same interrupt enables (RIE, TIE) as the $\overline{IRQ}$ output. The IRQ status bit simplifies status inquiries for polling systems by providing single-bit indication of service requests.

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Status Register 2 (SR2)

RS_1	RS_0	R/$\overline{W}$	AC
L	H	L	X

7	6	5	4	3	2	1	0
RDA	OVRN	DCD	ERR	RxABT	Rx Idle	FV	AP

b0 Address Present (AP) — The AP status bit provides the frame boundary and indicates an address octet is available in the Rx FIFO. In the extended addressing mode, the AP bit continues to indicate addresses until the address field is complete. The AP status bit is cleared by reading data or by RxRS.

b1 Frame Valid (FV) — The FV status bit provides the frame boundary indication to the MPU and also indicates that a frame is complete with no error. The FV status bit is set when the last data byte of a frame is transferred into the last location of the Rx FIFO (available to be read by MPU). Once FV status is set, the ADLC stops further data transfer into the last location of the Rx FIFO (in order to prevent the mixing of two frames) until the status bit is cleared by the CLR RxST or RxRS control bit.

b2 Inactive Idle Received (Rx Idle) — The Rx Idle status bit indicates that a minimum of 15 consecutive 1s have been received. The event is stored within the status register and can cause an interrupt. The interrupt and stored condition are cleared by the CLR RxST control bit. Rx Idle is the logical OR of the receiver idling detector (which continues to reflect idling until a LOW is received) and the stored inactive idle condition.

b3 Abort Received (RxABT) — The RxABT status bit indicates that seven or more consecutive 1s have been received. Abort has no meaning under out-of-frame conditions; therefore, no interrupt or storing of the status will occur unless a flag has been detected prior to the abort. An abort received when in-frame is stored in the status register and causes an $\overline{IRQ}$. The RxABT is the logical OR of the stored conditions and the receiver abort detect logic, which is cleared after 15 consecutive 1s have occurred. The stored abort condition is cleared by the CLR RxST or RxRS control bit.

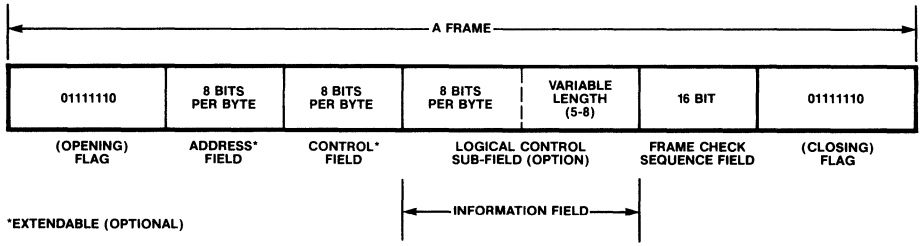
b4 Frame Check Sequence/Invalid Frame Error (ERR) When a frame is complete with a cyclic redundancy check (CRC) error or a short frame error (the frame does not have complete address and control fields), the ERR status bit is set instead of the Frame Valid status bit. Other functions, frame boundary indication and control function, are exactly the same as for the Frame Valid status bit. Refer to the FV status bit.

b5 Data Carrier Detect (DCD) — A positive transition on the $\overline{DCD}$ input is stored in the status register and causes an IRQ (if enabled). The stored DCD condition and its IRQ are cleared by the CLR RxST control bit or RxRS. After stored status is reset, the DCD status bit follows the state of the $\overline{DCD}$ input. Both the stored DCD condition and the $\overline{DCD}$ input cause the reset of the receiver section when they are HIGH.

b6 Receiver Overrun (OVRN) — The OVRN status bit indicates that receiver data has been transferred into the Rx FIFO when it is full, resulting in data loss. The OVRN status bit is cleared by the CLR RxST or RxRS control bit. Continued overrunning only destroys data in the first FIFO register.

b7 Receiver Data Available (RDA) — The Receiver Data Available status bit indicates when receiver data can be read from the Rx FIFO. When the prioritized status mode is used, the RDA bit indicates that non-address and non-last data are available in the Rx FIFO. The receiver data being present in the last register of the FIFO causes RDA to be HIGH for the 1-byte transfer mode. The RDA bit being HIGH indicates that the last two registers are full when in the 2-byte transfer mode. The RDA status bit is reset automatically when data is not available.

Frame Format



The ADLC transmits and receives data (information or control) in a format called a frame. All frames start with an opening flag (F) and end with a closing flag (F). Between the opening flag and closing flag, a frame contains an address field, control field, information field, and frame check sequence field.

Flag (F)
The flag is the unique binary pattern 01111110. It provides the frame boundary and a reference for the position of each field of the frame.

The ADLC Transmitter generates a flag pattern internally and the opening flag and closing flags are appended to a frame automatically. Two successive frames can share one flag for a closing flag of the first frame and for the opening flag of the next frame, if the "FF/F" control bit in Control Register 4 is reset.

The Receiver searches for a flag on a bit-by-bit basis and recognizes a flag at any time. The Receiver establishes the frame synchronization with every flag. The flags mark the frame boundary and reference for each field but they are not transferred to the Rx FIFO. The detection of a flag is indicated by the $\overline{\text{FLAG}}$ $\overline{\text{DET}}$ output and by the FD Status bit.

Order of Bit Transmission
Address, control and information field bytes are transferred between the MPU and the ADLC in parallel by means of the data bus. The bit on D_0 (data bus bit 0, pin 22) is serially transmitted first, and the first serially received bit is transferred to the MPU on D_0. The FCS field is transmitted and received MSB first.

Address (A) Field
The eight bits following the opening flag are the address (A) field. The A-field can be extendable if the auto-address extend mode is selected in Control Register 3. In the address extend mode, the first bit (bit 0) in every address octet becomes the C_{EX} control bit. When the bit is LOW, the ADLC assumes another address octet will follow; when the bit is HIGH, the address extension is terminated. A "null" address (all LOW) does not extend. In the Receiver, the AP status bit distinguishes the address field from other fields. When an address byte is available to be read in the Rx FIFO, the AP status bit is set and causes an interrupt (if enabled). The AP status bit is set for every addresss octet when the address extend mode is used.

Control (C) Field
The eight bits following the address field are the control (link control) field. When the C_{EX} control bit in Control Register 3 is selected, the C-field is extended to 16 bits.

Information (I) Field
The I-field follows the C-field and precedes the FCS field. The I-field contains data to be transferred but is not always necessarily contained in every frame. The word length of the I-field can be selected from five to eight bits per byte by control bits in Control Register 4. The I-field will continue until it is terminated by the FCS and closing flag. The Receiver has the capability to handle a partial last byte. The last information byte can be any word length between one and eight bits. If the last byte in the I-field is less than the selected word length, the Receiver will right justify the received bits, fill the remaining bits of the receiver shift register with zeros, and transfer a full byte to the Rx FIFO. Regardless of selected byte length, the ADLC will transfer eight bits of data to the data bus. Unused bits for word lengths of five, six, and seven will be zeroed.

Logic Control (LC) Field
When the LCF control bit in Control Register 3 is selected, the ADLC separates the I-field into two sub-fields. The first sub-field is the logic control field and the following sub-field is the data portion of the I-field. The logic control field is eight bits and follows the C-field, which is extendable by

octets, if it is selected. The last bit (bit 7) is the C_{EX} bit, and if it is HIGH, the LC-field is extended one octet.

Note

Hereafter, the term information field, or I-field, is used as the data portion of the information field and excludes the logic control field. This is done in order to keep the consistency of the meaning of information field as specified in SDLC, HDLC, and ADCCP standards.

Frame Check Sequence (FCS) Field

The 16 bits preceding the closing flag are the FCS field. The FCS is the cyclic redundancy check character (CRCC). The polynomial $x^{16} + x^{12} + x^5 + 1$ is used both for the Transmitter and Receiver. Both the transmitter and receiver polynomial registers are initialized to all 1s prior to calculation of the FCS. The Transmitter calculates the FCS on all bits of the address, control, logic control (if selected), and information fields, and transmits the complement of the resulting remainder as FCS. The Receiver performs a similar computation on all bits of the address, control, logic control (if selected), information, and received FCS fields and compares the result to FOB8 (hexadecimal). When the result matches FOB8, the FV status bit is set in Status Register 2. If the result does not match, the ERR status bit is set. The FCS generation, transmission, and checking are performed automatically by the ADLC Transmitter and Receiver. The FCS field is not transferred to the Rx FIFO.

Invalid Frame

Any valid frames should have at least the A-field, C-field and FCS field between the opening flag and the closing flag. When invalid frames are received, the ADLC handles them as follows:

1. A short frame which has less than 25 between flags—The ADLC ignores the short frame and its reception is not reported to the MPU.
2. A frame less than 32 bits between the flags, or a frame 32 bits or more with an extended A-field or C-field that is not completed is transferred into the Rx FIFO. The ERR status bit indicates the reception of the invalid frame at the end of the frame.
3. Aborted frame—The frame which is aborted by receiving an abort or $\overline{DCD}$ failure is also an invalid frame. Refer to ABT and DCD status bits.

Zero Insertion and Zero Deletion

The zero insertion and deletion that allows the content of the frame to be transparent is performed by the ADLC automatically. A binary 0 is inserted by the Transmitter after any succession of five 1s within a frame (A, C, LC, I, and FCS field). The Receiver deletes a binary 0 that follows five successive 1s within a frame.

Abort

The function of prematurely terminating a data link is called abort. The Transmitter aborts a frame by sending at least eight consecutive 1s immediately after the ABT control bit in Control Register 4 is set to HIGH. (Tx FIFO is also cleared by the ABT control bit at the same time.) The abort can be extended to at least 16 consecutive 1s, if the ABT_{EX} control bit in the Control Register 4 is set when an abort is sent. This feature is useful to force mark idle transmission. Reception of seven or more consecutive 1s is interpreted as an abort by the Receiver. The Receiver responds to a received abort as follows:

1. An abort in an out-of-frame condition—An abort during the idle or time fill has no meaning. The abort reception is indicated in the Status Register as long as the abort condition continues, but neither an interrupt nor a stored condition occurs. The abort indication disappears after 15 or more consecutive 1s are received (Rx Idle status bit is set).
2. An abort in frame, when less than 26 bits have been received after an opening flag, has not transferred any field to the MPU. The ADLC clears the aborted frame data in the Rx FIFO and clears flag synchronization. Neither an interrupt nor a stored status occurs. The status indication is the same as (1) above.
3. An abort in-frame, when 26 bits or more have been received after an opening flag, might have transferred some fields of the aborted frame onto the data bus. The abort status is stored in Status Register 2 and the data of the aborted frame in the ADLC is cleared. The synchronization is also cleared.

Idle and Time Fill

When the Transmitter is in an out-of-frame condition (the Transmitter is not transmitting a frame), it is in an idle state. Either a series of contiguous flags (time fill) or a mark idle (consecutive 1s on a bit-by-bit basis) is selected for the transmission in an idle state by the F/M Idle control bit. When the Receiver receives 15 or more consecutive 1s, the Rx Idle status bit is set and causes an interrupt. The flags and mark idle are not transferred to the Rx FIFO.

Programming Considerations

1. **Status Priority** — When the prioritized status mode is used, it is best to test for the lowest priority conditions first. The lowest priority conditions typically occur more frequently and are the most likely conditions to exist when the processor is interrupted.

2. **Stored vs. Present Status** — Certain status bits (DCD, CTS, RxABT, and Rx Idle) indicate a status which is the logic OR of a stored and a present condition. It is the stored status that causes an interrupt and which is

cleared by the CLR RxST or CLR TxST control bit. After being cleared, the status register will reflect the present condition of an input or a receiver input sequence.

3. **Clearing Status Registers** — In order to clear an interrupt with the two status clear control bits, a particular status condition must be read before it can be cleared. In the prioritized mode, clearing a higher priority condition might result in another $\overline{IRQ}$ caused by a lower priority condition whose status was suppressed when a status register was first read. This guarantees that a status condition is never inadvertently cleared.

4. **Clearing the Rx FIFO** — An RxRS will effectively clear the contents of all three Rx FIFO bytes. However, the Rx FIFO may contain data from two different frames when abort or DCD failure occurs. When this happens, the data from a previously closed frame (a frame whose closing flag has been received) will not be destroyed.

5. **Servicing the Rx FIFO in a 2-Byte Mode** — The procedure for reading the last bytes of data is the same, regardless of whether the frame contains an even or an odd number of bytes. Continue to read two bytes until an interrupt occurs that is caused by an end-of-frame status (FV or ERR). When this occurs, indicating that the last byte either has been read or is ready to be read, switch temporarily to the 1-byte mode with no prioritized status (Control Register 2). Test RDA to indicate whether a 1-byte read should be performed. Then clear the frame end status.

6. **Frame Complete Status and RTS Release** — In many cases, a modem will require a delay for releasing $\overline{RTS}$. An 8-bit or 16-bit delay can be added to the ADLC $\overline{RTS}$ output by using an abort. At the end of a transmission, frame-complete status will indicate the frame completion. After the TDRA/FC status bit goes HIGH, write 1 into the ABT control bit (and ABT_{EX} bit if a 16-bit delay is required). After the ABT control bit is set, write 0 into the RTS control bit. The Transmitter will transmit eight or 16 1s and the $\overline{RTS}$ output will then go HIGH (inactive).

7. **Note to users not using the F6800** — (a) Care should be taken when performing a write followed by a read on successive E pulses at a high frequency rate. Time must be allowed for status changes to occur. If this is done, the time that E is LOW between successive write/read E pulses should be at least 500 ns. (b) The ADLC is a completely static part. However, the E frequency should be high enough to move data through the FIFO registers and to service the peripheral requirements. Also, the period between successive E pulses should be less than the period of RxC or TxC in order to maintain synchronization between the data bus and the peripherals.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	-0.3V, +7.0V
Input Voltage, V_{IN}	-0.3V, +7.0V
Operating Temperature, T_A	
F6854P/S, F68A54P/S, F68B54P/S	0° C, +70° C
F6854CP/CS, F68A54CP/CS	-40° C, +85° C
F6854DL	-55° C, +85° C
F6854DM	-55° C, +125° C
Storage Temperature, T_{STG}	-65° C, +150° C

Thermal Resistance, θ_{JA}	
Plastic	115° C/W
Ceramic	60° C/W

These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC Characteristics V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = over operating temperature range, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input HIGH Voltage	V_{SS} + 2.0			V	
V_{IL}	Input LOW Voltage			V_{SS} + 0.8	V	
V_{OH}	Output HIGH Voltage D_0-D_7 All Others	 V_{SS} + 2.4 V_{SS} + 2.4			V	 I_{Load} = -205 μA I_{Load} = -100 μA
V_{OL}	Output LOW Voltage			V_{SS} + 0.4	V	I_{Load} = 1.6 mA
I_{IN}	Input Leakage Current All Inputs Except D_0-D_7		1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	Three-State (Off State) Input Current D_0-D_7		2.0	10	μA	V_{IN} = 0.4 to 2.4 V V_{CC} = 5.25 V
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μA	V_{OH} = 2.4 V
P_D	Power Dissipation			850	mW	V_{CC} = 5.25 V
C_{IN}	Input Capacitance D_0-D_7 All Other Inputs			 12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0 MHz
C_{OUT}	Output Capacitance $\overline{IRQ}$ All Others			 5.0 10	pF	

AC Characteristics

Symbol	Characteristic	F6854 Min	F6854 Max	F68A54 Min	F68A54 Max	F68B54 Min	F68B54 Max	Unit
PW_{CL}	Minimum Clock Pulse Width, LOW	700		450		280		ns
PW_{CH}	Minimum Clock Pulse Width, HIGH	700		450		280		ns
f_{max}	Clock Frequency		0.66		1.0		1.5	MHz
t_{RDSU}	Receive Data Set-up Time	250		200		120		ns
t_{RDH}	Receive Data Hold Time	120		100		60		ns
t_{RTS}	Request-to-Send Delay Time		680		460		340	ns
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320		250	ns
t_{FD}	Flag Detect Delay Time		680		460		340	ns
t_{DTR}	DTR Delay Time		680		460		340	ns
t_{LOC}	Loop On-line Control Delay Time		680		460		340	ns
t_{RDSR}	RDSR Delay Time		540		400		340	ns
t_{TDSR}	TDSR Delay Time		540		400		340	ns
t_{IR}	Interrupt Request Release Time		1.2		0.9		0.7	μs
t_{RES}	RESET Minimum Pulse Width	1.0		0.65		0.40		μs
t_r, t_f	Input Rise and Fall Times (Except Enable) 0.8 V to 2.0 V		1.0*		1.0*		1.0*	μs

* 1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = over operating temperature range, unless otherwise noted

Symbol	Characteristic	F6854		F68A54		F68B54		Unit
		Min	Max	Min	Max	Min	Max	
Read								
PW_{EH}	Enable Pulse Width, HIGH	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, LOW	0.43		0.28		0.21		μs
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
t_{AS}	Set-up Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
PW_{EH}	Enable Pulse Width, HIGH	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, LOW	0.43		0.28		0.21		μs
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
t_{AS}	Set Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Set-up Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Fig. 4 Bus Timing Test Loads

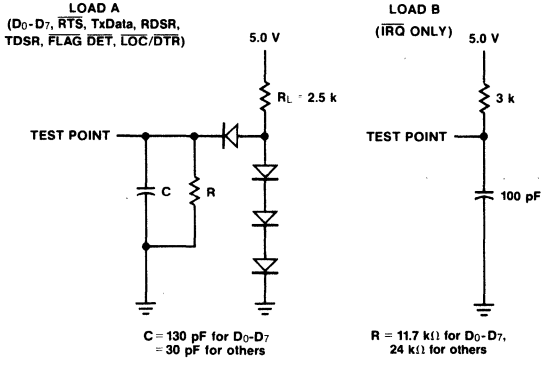


Fig. 5 Receiver Data Set-up/Hold, Flag Detect and Loop On-line Control Delay Timing

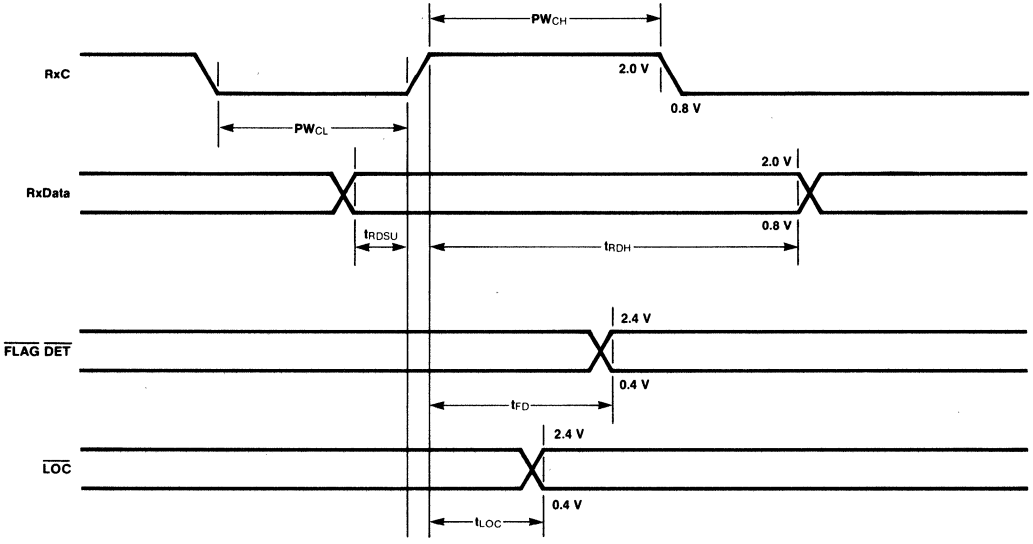


Fig. 6 Transmit Data Output Delay and Request-to-Send Delay Timing

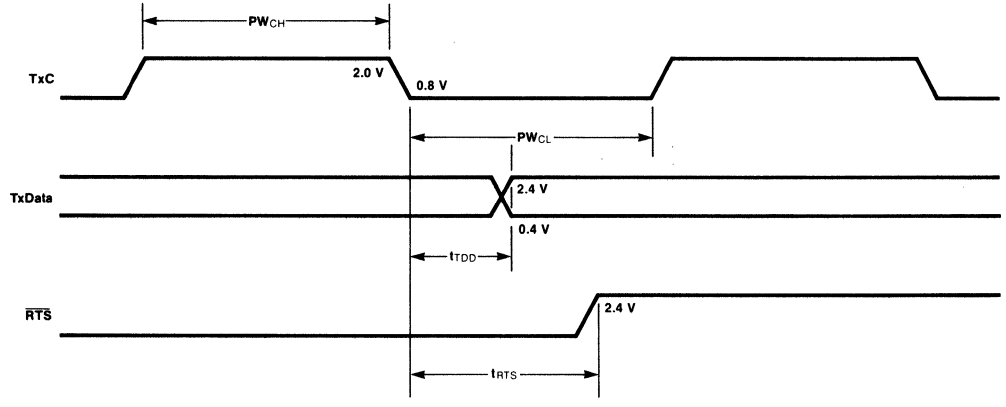


Fig. 7 TDSR/RDSR Delays, IRQ Release Delay, $\overline{RTS}$ and $\overline{DTR}$ Delay Timing

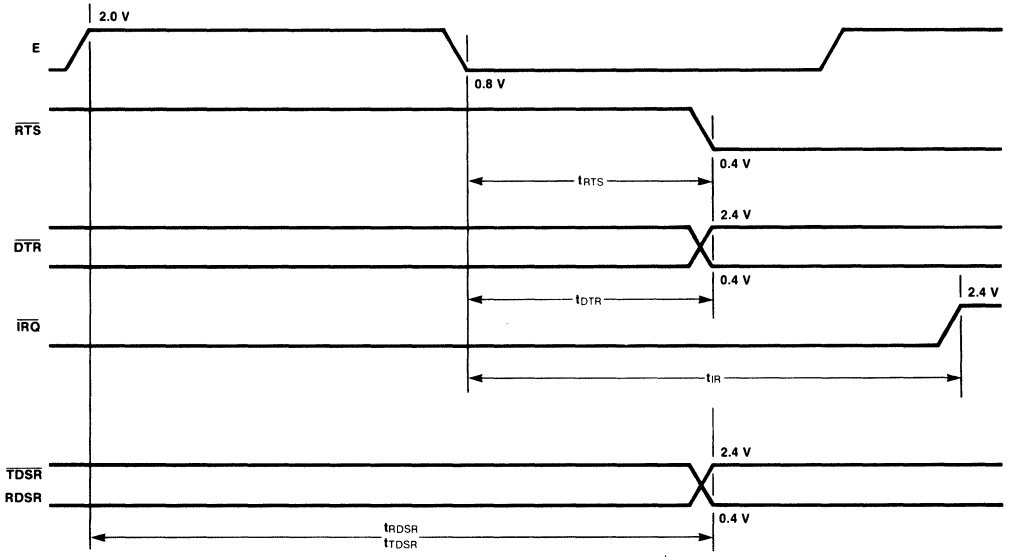
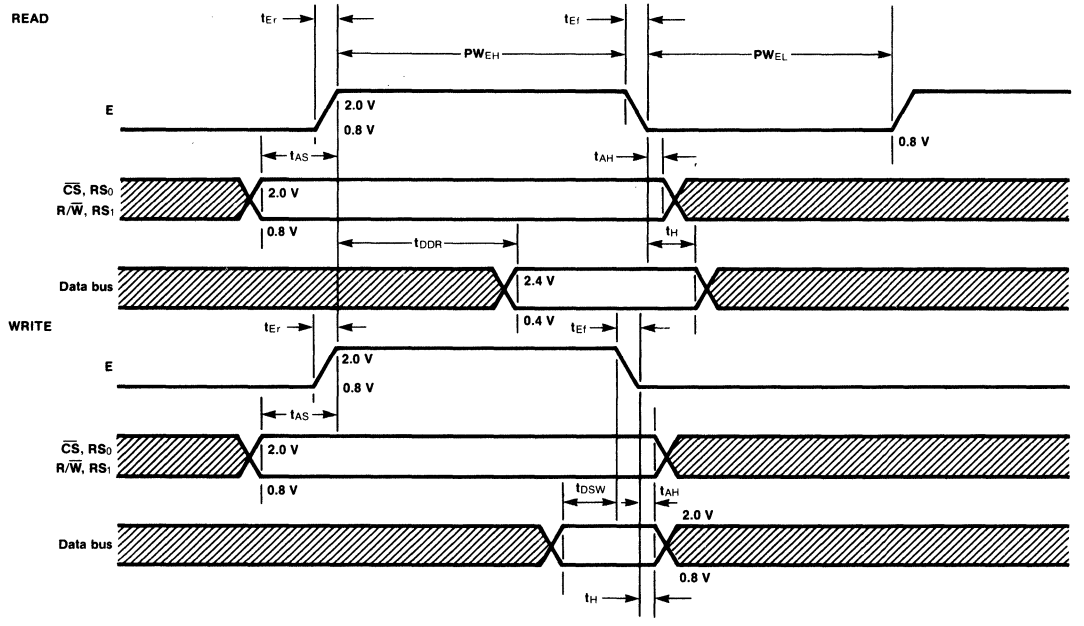


Fig. 8 Bus Read/Write Timing Characteristics



Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F6854P,S	0 to +70°C
	F6854CP,CS	-40 to +80°C
	F6854DL	-55 to +80°C
	F6854DM	-55 to +80°C
1.5 MHz	F68A54P,S	0 to +70°C
	F68A54CP,CS	-40 to +80°C
2.0 MHz	F68B54P,S	0 to +70°C

P= Plastic package. S = Ceramic package