FAIRCHILD
A Schlumberger Company

F3872/F38L72
Single-Chip Microcomputer

Microprocessor Product

Description

The Fairchild F3872 is a complete 8-bit microcomputer on a single MOS integrated circuit. It can execute the F8 instruction set of more than 70 commands, allowing expansion into multi-chip configurations with software compatibility. The device features 64 bytes of scratchpad RAM, 64 bytes of power-down executable RAM, a programmable binary timer, 32 bits of I/O, a single +5 V power supply requirement, and a choice of 1K, 2K, 3K, or 4K bytes of ROM. A low-power standby option for the executable RAM is available on the F38L72.

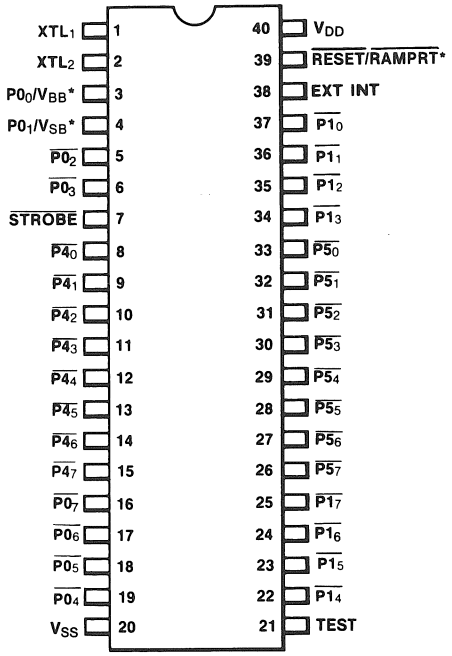
Utilizing Fairchild's double-ion-implanted, N-channel silicon-gate technology and advanced circuit design techniques, the single-chip F3870 offers maximum cost effectiveness in a wide range of control and logic replacement applications.

The F3872 is an expanded memory version of the F3870 single-chip microcomputer. It is identical to the F3870 in the following areas: instruction set, architecture, ac and dc characteristics, and pinout. The only difference between the F3872 and the F3870 lies in the memory expansion and the appropriate memory address registers.

- **Single-chip Microcomputer**
- **Same Pinout as F3870**
- **Software-Compatible with F8 Family**
- **1024-, 2048-, 3072-, or 4032-Byte Mask-Programmable ROM**
- **64-Byte Scratchpad RAM**
- **32-Bit (4-Port) TTL-Compatible I/O**
- **Programmable Binary Timer:**
  - **Interval Timer Mode**
  - **Pulse Width Measurement Mode**
  - **Event Counter Mode**
- **External Interrupt**
- **Crystal, LC, RC, or External Time Base**
- **Low Power (285 mW, Typical)**
- **Single +5 V ± 10% Power Supply**
- **64 Additional Bytes of Executable RAM Addressable by Program or Data Counter**
- **Standby Option for Executable RAM**
  - **Low Standby Power (8.2 mW)**
  - **3.2 V Minimum Standby Supply Voltage**
  - **No External Components Required to Trickle Charge Battery**

Connection Diagram

40-Pin DIP



(Top View)

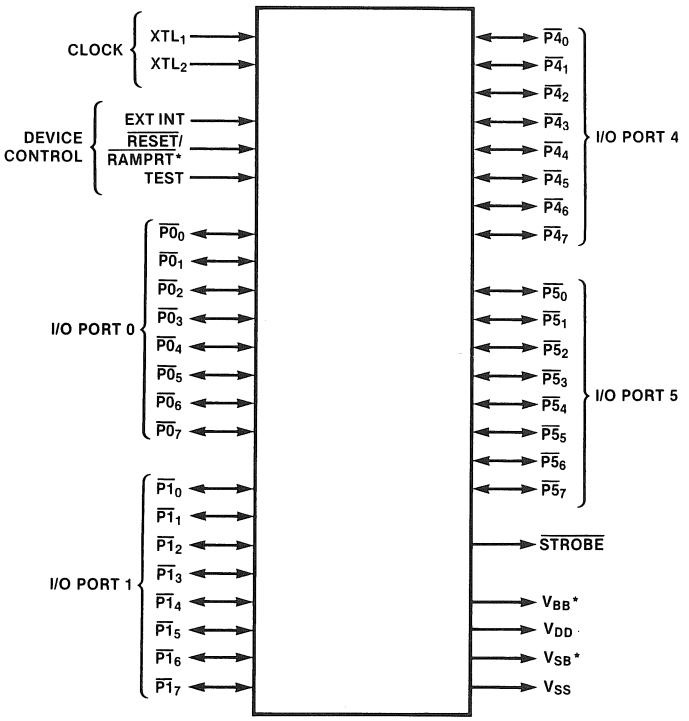
*Programmable pin; function determined by device option (standard or standby mode).

Signal Functions

The functions of the F3872 inputs and outputs are described in *Table 1.*

Fairchild Camera and Instrument, Microprocessor Division
3420 Central Expressway, Santa Clara, CA 95051
(408) 773-1000 TWX MICPSNTA

Signal Functions



Device Organization

This section describes the basic functional elements of the F3872 shown in *Figures 1* and *2.*

Main Control Logic

The instruction register (IR) receives the operation code (op code) of the instruction to be executed from the program ROM via the data bus. During all op code fetches, eight bits are latched into the IR. Some instructions are completely specified by the upper four bits of the op code; in such instructions, the lower four bits are an immediate register address or an immediate 4-bit operand. Once latched into the IR, the main control logic decodes the instruction and provides the necessary control gating signals to all circuit elements.

ROM Address Registers

There are four 12-bit registers associated with the program ROM of the F3872. *(In the F3872-1, -2, and -3, the 12-bit registers can address more memory space than is physically available on the chip; user caution is advised.)* These are the program counter (P0), the stack register (P), the data counter (DC), and the auxiliary data counter (DC1). The program counter is used to address instructions or immediate operands. The stack register is used to save the contents of P0 during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The data counter is used to address data tables. This register is autoincrementing. Of the two data counters, only DC can access the ROM. However, the XDC instruction allows DC and DC1 to be exchanged.

Associated with the F3872 address registers is a 12-bit adder/incrementer. This logic element is used to increment P0 or DC when required and is also used to add displacements to P0 on relative branches or to add the data bus contents to DC in the add data counter (ADC) instruction.

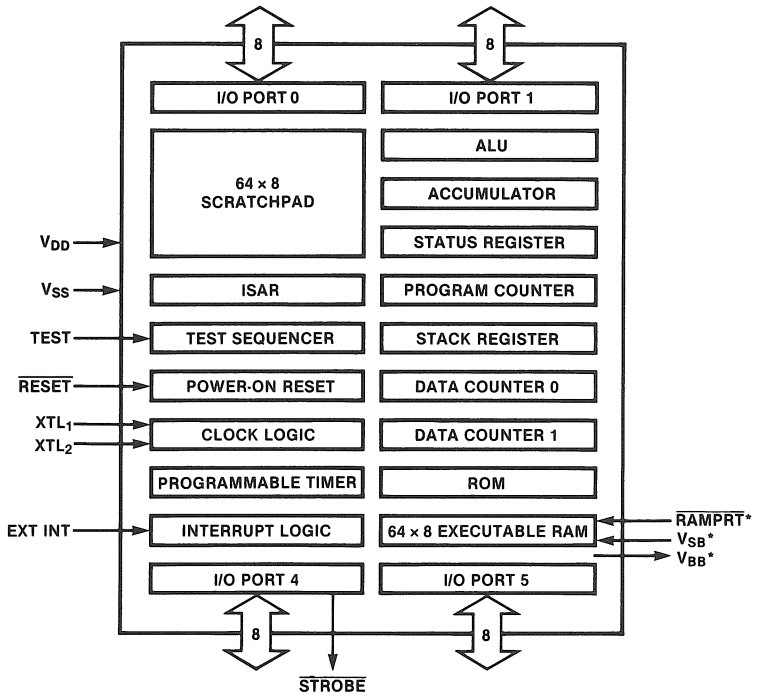
Program ROM

The microcomputer program and data constants are stored in the program ROM, which may be 1024 × 8 (F3872-1), 2048 × 8 (F3872-2), 3072 × 8 (F3872-3), or 4032 × 8 (F3872-4) bytes. When a ROM access is required, the appropriate address register (P0 or DC) is gated onto the ROM address bus and the ROM output is gated onto the main data bus. The first byte in the ROM is location zero.

Table 1 Signal Functions

Mnemonic	Pin No.	Name	Description
Device Control			
EXT INT	38	External Interrupt	Software-programmable input that is also used in conjunction with the timer for pulse width measurement and event counting.
$\overline{\text{RESET}}$/ $\overline{\text{RAMPRT}}$	39	External Reset/RAM Protect	Input that, in standard operating mode, may be used to externally reset the F3872. When pulled low, the F3872 resets; when then allowed to go high, the F3872 begins program execution at program location H'0000'. When RAM standby mode is selected, may be used as RAM protect control. When pulled low, the RAM is disabled and, therefore, protected from any alterations during loss of V_{DD}.
TEST	21	Test Line	An input used only in testing the F3872. For normal circuit operation, TEST is left unconnected or grounded.
Clock			
$\overline{\text{STROBE}}$	7	Ready Strobe	Normally high output that provides a single low pulse after valid data is present on the $\overline{P4_0}$-$\overline{P4_7}$ pins during an output instruction.
XTL_1, XTL_2	1, 2	Time Base	Inputs to which a crystal (1 MHz to 4 MHz), LC network, RC network, or external single-phase clock may be connected.
$\overline{P0_0}$-$\overline{P0_7}$ $\overline{P1_0}$-$\overline{P1_7}$ $\overline{P4_0}$-$\overline{P4_7}$ $\overline{P5_5}$-$\overline{P5_7}$	3-6, 8-19, 22-37	I/O Ports	Thirty-two bidirectional lines that can be individually used as either TTL-compatible inputs or latched outputs; $P0_0$ and $P0_1$ may also serve power outputs in standby mode.
Power			
V_{BB}	3	Substrate Decoupling	Substrate decoupling power pin that is used only when the standby option is selected; a 0.01 μF capacitor is required to provide substrate decoupling; alternative function of $P0_0$, which is the standard function.
V_{DD}	40	Power Input	+5 V ± 10% power supply
V_{SB}	4	Standby Power	The RAM standby power supply if the standby option (+5.5 V to +3.2 V) is selected; alternative function of $P0_1$, which is the standard function.
V_{SS}	20	Ground	Signal and power ground

Fig. 1 F3872 Architecture



*Standby Mode Only.

64 x 8 Executable RAM
The upper 64 bytes of the total memory of the F3872 is RAM. The first byte is at address 4032 decimal ('FC0' hexadecimal). As with the ROM, the RAM may be accessed by the P0 and DC address registers. It may be written to via the store (ST) instruction, and it may be read from via the load (LM) instruction. Additionally, instructions may be executed from the RAM. A mask-programmable standby power option is available in which the 64 x 8 RAM remains powered and protected so that its contents are saved during a loss of the normal circuit power supply.

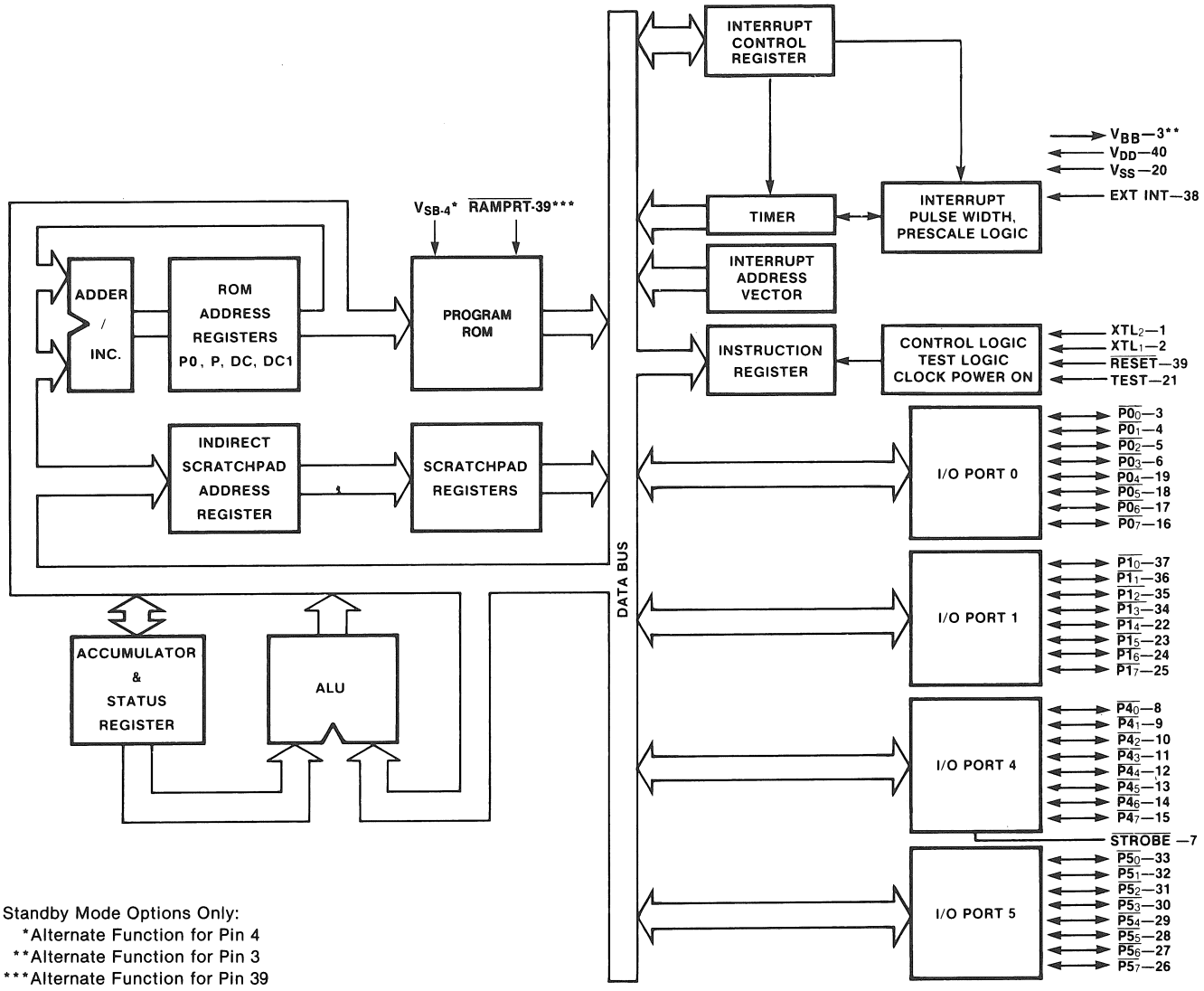
Scratchpad and ISAR
The scratchpad provides 64 8-bit registers that may be used as general-purpose RAM. The indirect scratchpad address register (ISAR) is a 6-bit register used to address the 64 registers. All 64 registers may be accessed using the ISAR. In addition, the lower order 12 registers may also be directly addressed.

The ISAR can be visualized as holding two octal digits. This division of the ISAR is important, since a number of instructions increment or decrement only the least significant three bits of the ISAR when referencing scratchpad bytes via the ISAR. This makes it easy to reference a buffer consisting of contiguous scratchpad bytes. For example, when the low-order octal digit is incremented or decremented, the ISAR is incremented from octal 27 to 20 or is decremented from octal 20 to 27. This feature of the ISAR is very useful in many program sequences. All six bits of the ISAR may be loaded at one time, or either half may be loaded independently.

Scratchpad registers 9 through 15 (decimal) are given mnemonic names (J, H, K, and Q) because of special linkages between these registers and other registers, such as the stack register. These special linkages facilitate the implementation of multi-level interrupts and subroutine nesting. For example, the instruction LR K, P stores the lower eight bits of the stack register in register 13 (K lower, or KL) and stores the upper four bits of P in register 12 (K upper, or KU). The scratchpad is not protected by the standby power option.

Arithmetic and Logic Unit (ALU)
After receiving commands from the main control logic, the ALU performs the required arithmetic or logic operations (using the data presented on the two input

Fig. 2 F3872 Block Diagram



Standby Mode Options Only:
*Alternate Function for Pin 4
**Alternate Function for Pin 3
***Alternate Function for Pin 39

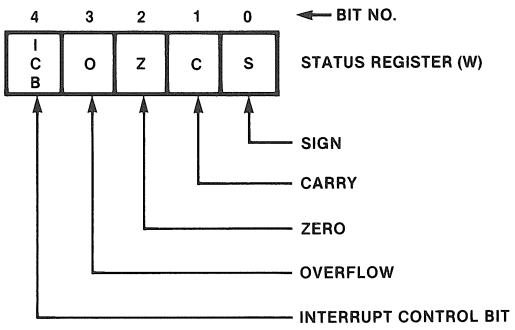
buses) and provides the result on the result bus. The arithmetic operations that can be performed in the ALU are binary add, decimal adjust, add with carry, decrement, and increment. The logic operations that can be performed are AND, OR, exclusive-OR, ones complement, shift right, and shift left. Besides providing the result on the result bus, the ALU also provides four signals presenting the status of the result. These signals, stored in the status register (W), represent the CARRY, OVERFLOW, SIGN, and ZERO conditions of the result of the operation.

Accumulator

The accumulator (ACC) is the principal register for data manipulation within the F3872. The ACC serves as one input to the ALU for arithmetic or logical operation. The results of ALU operations are stored in the ACC.

Status Register

The status register (also referred to as the W register) holds five status flags, as follows:



Summary of Status Bit

$$\text{OVERFLOW} = \text{CARRY}_7 \oplus \text{CARRY}_6$$

$$\text{ZERO} = \overline{ALU_7} \wedge \overline{ALU_6} \wedge \overline{ALU_5} \wedge \overline{ALU_4} \wedge \overline{ALU_3} \wedge \overline{ALU_2} \wedge \overline{ALU_1} \wedge \overline{ALU_0}$$

$$\text{CARRY} = \text{CARRY}_7$$

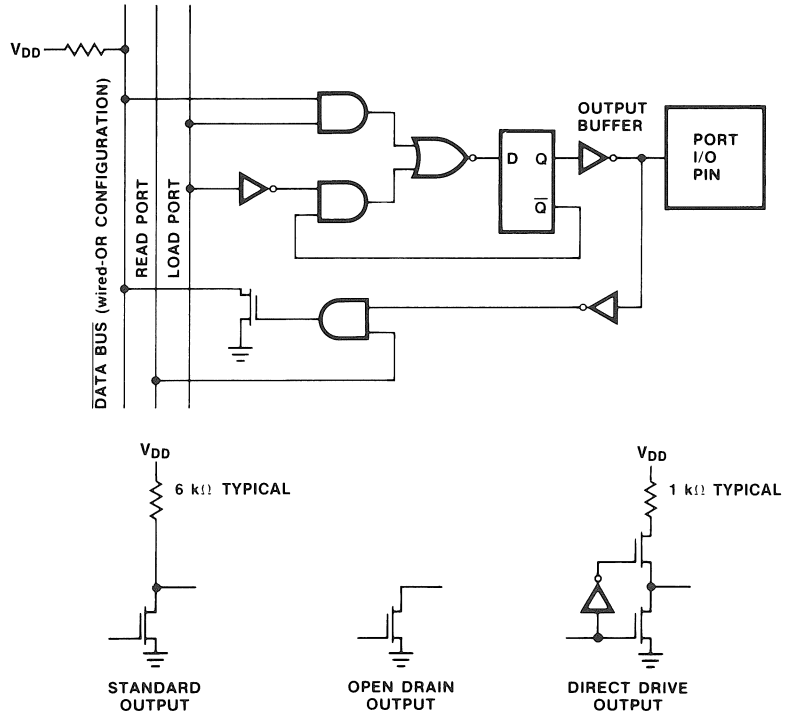
$$\text{SIGN} = \overline{ALU_7}$$

The interrupt control bit (ICB) of the status register may be used to allow or disallow interrupts in the F3872. This bit is not the same as the two interrupt enable bits in the interrupt control port (ICP). If the ICB is set and the F3872 interrupt logic communicates an interrupt request to the CPU section, the interrupt is acknowledged and processed upon completion of the first non-privileged instruction. If the ICB is cleared, an interrupt request is not acknowledged or processed until the ICB is set.

I/O Ports

The F3872 provides four complete bidirectional I/O ports; these are ports 0, 1, 4, and 5. In addition, the interrupt control register is addressed as port 6 and the binary timer is addressed as port 7. An output instruction (OUT or OUTS) causes the contents of the ACC to be latched into the addressed port. An input instruction (IN or INS) transfers the contents of the port to the ACC (port 6 is an exception that is described later). The I/O pins on the F3872 are logically inverted. The schematic of an I/O pin and conceptual illustrations of available output drive options are shown in *Figure 3.*

Fig. 3 I/O Port Diagram



Ports 0 and 1 are standard output type only.
Ports 4 and 5 may be any of the three output options, each pin individually assignable to any port.
The $\overline{\text{STROBE}}$ output is always configured similar to a standard output, except that it is capable of driving three TTL loads.
The $\overline{\text{RESET}}$ and EXT INT pins may have standard 6 kΩ (typical) pull-up or may have no pull-up.

An output ready strobe is associated with port 4. This flag may be used to signal a peripheral device that the F3872 has just completed a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. This $\overline{\text{STROBE}}$ signal may also be used to request new input information from a peripheral simply by doing a dummy output of H'00' to port 4 after completing the input operation.

Timer and Interrupt Control Port

The timer is an 8-bit binary down counter that is software-programmable to operate in one of three modes: the interval timer mode, the pulse width measurement mode, or the event counter mode; the timer characteristics are described in *Table 2.* As shown in *Figure 4,* associated with the timer is an 8-bit register called the interrupt control port, a programmable prescaler, and an 8-bit modulo-N register; a functional logic diagram is shown in *Figure 5.*

The desired timer mode, prescale value, starting and stopping the timer, active level of the EXT INT pin, and local enabling or disabling of interrupts are selected by outputting the proper bit configuration from the accumulator to the ICP (port 6) with an OUT or OUTS instruction. Bits within the ICP are defined as follows:

Interrupt Control Port (Port 6)

Bit 0—External Interrupt Enable
Bit 1—Timer Interrupt Enable
Bit 2—EXT INT Active Level
Bit 3—Start/Stop Timer
Bit 4—Pulse Width/Interval Timer
Bit 5— ÷ 2 Timer Prescale Values
Bit 6— ÷ 5 Timer Prescale Values
Bit 7— ÷ 20 Timer Prescale Values

A special situation exists when reading the ICP with an IN or INS instruction. The accumulator is not loaded with

Table 2 Timer Characteristics

Characteristic	Value
Interval Timer Mode	
Single Interval Error, Free-Running (Note 3)	$\pm 6t\phi$
Cumulative Interval Error, Free-Running (Note 3)	0
Error Between Two Timer Reads (Note 2)	$\pm (tpsc + t\phi)$
Start Timer to Stop Timer Error (Notes 1, 4)	$+ t\phi$ to $- (tpsc + t\phi)$
Start Timer to Read Timer Error (Notes 1, 2)	$- 5t\phi$ to $- (tpsc + 7t\phi)$
Start Timer to Interrupt Request Error (Notes 1, 3)	$- 2t\phi$ to $- 8t\phi$
Load Timer to Stop Timer Error (Note 1)	$+ t\phi$ to $- (tpsc + 2t\phi)$
Load Timer to Read Timer Error (Notes 1, 2)	$- 5t\phi$ to $- (tpsc + 8t\phi)$
Load Timer to Interrupt Request Error (Notes 1, 3)	$- 2t\phi$ to $- 9t\phi$
Pulse Width Measurement Mode	
Measurement Accuracy (Note 4)	$+ t\phi$ to $- (tpsc + 2t\phi)$
Minimum Pulse Width of EXT INT Pin	$2t\phi$
Event Counter Mode	
Minimum Active Time of EXT INT Pin	$2t\phi$
Minimum Inactive Time of EXT INT Pin	$2t\phi$

Definitions

Error = indicated time value – actual time value
tpsc = $t\phi$ × prescale value

Notes

1. All times that entail loading, starting, or stopping the timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times that entail reading the timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times that entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multi-cycle instruction.
4. Error may be cumulative if operation is repetitively performed.

the contents of the ICP; instead, accumulator bits 0 through 6 are loaded with zeros, while bit 7 is loaded with the logic level being applied to the EXT INT pin, thus allowing the status of the EXT INT pin to be determined without the necessity of servicing an external interrupt request. This capability is useful in establishing a high-speed, polled handshake procedure or for using EXT INT as an extra input pin if external interrupts are not required and the timer is used only in the interval timer mode.

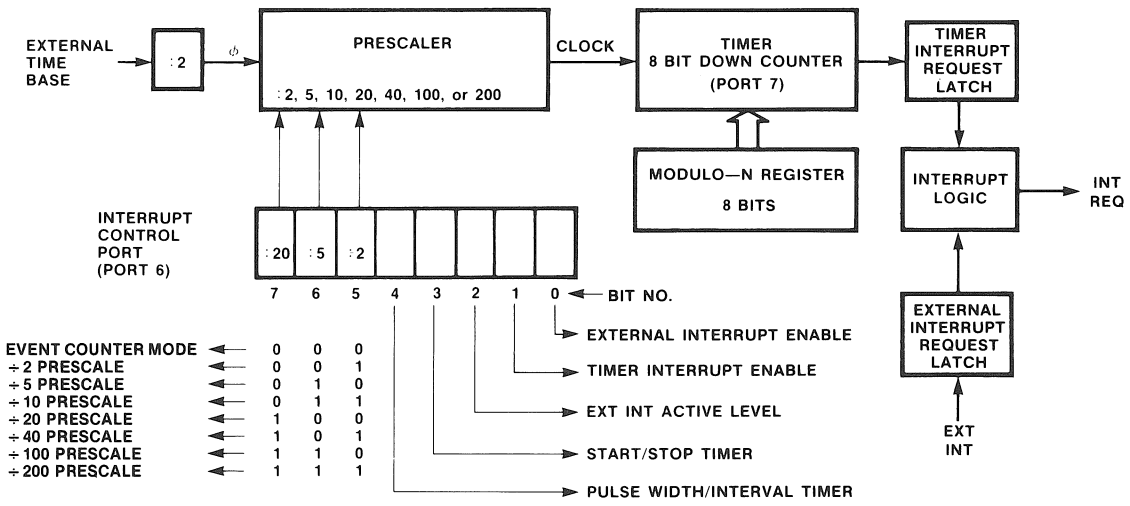
The rate at which the timer is clocked in the interval timer mode is determined by the frequency of an internal ϕ clock and by the division value selected for the prescaler. (The internal clock operates at one-half the external time base frequency.) If ICP bit 5 is set and bits 6 and 7 are cleared, the prescaler divides ϕ by 2. Likewise, if bit 6 or 7 is individually set, the prescaler divides ϕ by 5 or 20, respectively. Combinations of bits 5, 6, and 7 may also be selected. For example, if bits 5 and 7 are set while bit 6 is cleared, the prescaler divides by 40. Thus, possible prescaler values are: $\div 2$, $\div 5$, $\div 10$, $\div 20$, $\div 40$, $\div 100$, and $\div 200$.

Any of three conditions cause the prescaler to be reset: whenever the timer is stopped by clearing ICP bit 3, on execution of an output instruction to port 7 (the timer is assigned port address 7), or on the trailing edge transition of the EXT INT pin when in the pulse width measurement mode. These last two conditions are explained in the following paragraphs.

An OUT or OUTS instruction to port 7 loads the contents of the accumulator into both the timer and the 8-bit modulo-N register, resets the prescaler, and clears any previously stored timer interrupt request. As previously noted, the timer is an 8-bit down counter that is clocked by the prescaler in the interval timer mode and in the pulse width measurement mode. The prescaler is not used in the event counter mode. The modulo-N register is a buffer whose function is to save the value that was most recently output to port 7. The modulo-N register is used in all three timer modes.

Interval Timer Mode — When ICP bit 4 is cleared (logic 0) and at least one prescale bit is set, the timer operates in the interval timer mode. When bit 3 of the ICP is set, the timer starts counting down from the modulo-N value. After counting down to H'01', the timer returns to the modulo-N value at the next count. On the transition from H'01' to H'N', the timer sets a timer interrupt request latch. Note that the interrupt request latch is set by the transition of H'N' in the timer, thus allowing a full 256 counts if the modulo-N register is preset to H'00'. If bit 1 of the ICP is set, the interrupt request is passed to the CPU section of the F3872. However, if bit 1 of the ICP is a logic 0, the interrupt request is not passed, but the interrupt request latch remains set. If ICP bit 1 is subsequently set, the interrupt request is then passed to the CPU. Only two events can reset the timer interrupt request latch: when the timer interrupt request is acknowledged by the CPU, or when a new load of the modulo-N register is performed.

Fig. 4 Timer and Interrupt Control Port Block Diagram



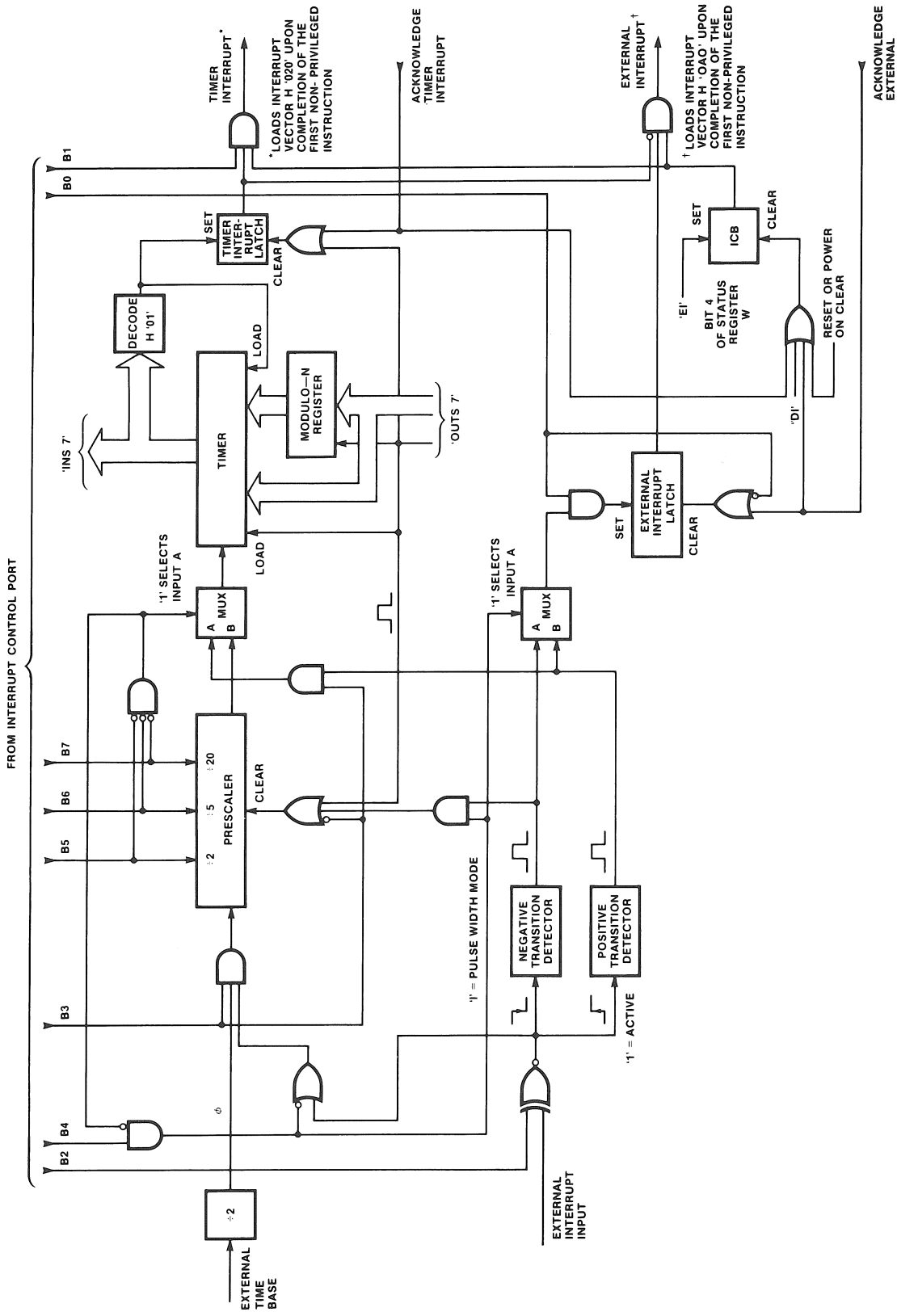


Fig. 5 Timer/Interrupt Functional Diagram

Consider an example in which the modulo-N register is loaded with H'64' (decimal 100). The timer interrupt request latch is set at the 100th count following the timer start, and the timer interrupt request latch is repeatedly set on precise 100-count intervals. If the prescaler is set at ÷ 40, the timer interrupt request latch is set every 4000 ϕ clock periods. For a 2 MHz ϕ clock (4 MHz time base frequency), this produces 2 ms intervals.

The range of possible intervals is from 2 to 51,200 ϕ clock periods (1 μs to 25.6 ms for a 2 MHz clock). However, approximately 50 ϕ periods is a practical minimum because the time between setting the interrupt request latch and the execution of the first instruction of the interrupt service routine is at least 29 ϕ periods (the response time is dependent upon how many privileged instructions are encountered when the request occurs). To establish time intervals greater than 51,200 clock periods is simply a matter of using the timer interrupt service routine to count the number of interrupts, saving the result in one or more of the scratchpad registers until the desired interval is achieved. With this technique, virtually any time interval, or several time intervals, may be generated.

The timer may be read at any time and in any mode using an input instruction (IN 7 or INS 7); this may take place on-the-fly without interfering with normal timer operation. The timer may also be stopped at any time by clearing bit 3 of the ICP. The timer holds its current contents indefinitely and resumes counting when bit 3 is again set. The prescaler, however, is reset whenever the timer is stopped; thus, a series of starts and stops results in a cumulative truncation error.

For a free-running timer in the interval timer mode, the time interval between any two interrupt requests may be in error by ± 6 ϕ clock periods, although the cumulative error over many intervals is zero. The prescaler and timer generate precise intervals for setting the timer interrupt request latch, but the time-out may occur at any time within a machine cycle. (There are two types of machine cycles: short cycles that consist of four ϕ clock periods, and long cycles that consist of 6 ϕ clock periods.) In the multi-chip F8 family, there is a signal referred to as the write clock, which corresponds to a machine cycle. Interrupt requests are synchronized with the internal write clock, thus giving rise to the possible ± 6 ϕ error. Additional errors may arise due to the interrupt request occurring while a privileged instruction or multi-cycle instruction is being executed. Nevertheless, for most applications, all of the above errors are negligible, especially if the desired time interval is greater than 1 ms.

Pulse Width Measurement Mode — When ICP bit 4 is set (logic 1) and at least one prescale bit is set, the timer operates in the pulse width measurement mode. This mode is used for accurately measuring the duration of a pulse applied to the EXT INT pin. The timer is stopped and the prescaler is reset when the EXT INT pin is at its inactive level. The active level of EXT INT is defined by ICP bit 2: if cleared, EXT INT is active-low; if set, EXT INT is active-high. If ICP bit 3 is set, the prescaler and timer start counting when EXT INT transfers to the active level. When EXT INT returns to the inactive level, the timer stops, the prescaler resets, and, if ICP bit 0 is set, an external interrupt request latch is set. (Unlike timer interrupts, external interrupts are not latched if the ICP interrupt enable bit is not set.)

As in the interval timer mode, the timer may be read at any time, or may be stopped at any time by clearing ICP bit 3, the prescaler and the ICP bit 1 function as previously described; the timer still functions as an 8-bit binary down counter with the timer interrupt request latch being set on the timer's transition from H'01' to H'N' (modulo-N value). Note that the EXT INT pin has nothing to do with loading the timer; its action is that of automatically starting and stopping the timer and of generating external interrupts. Pulse widths longer than the prescaler value times the modulo-N value are easily measured by using the timer interrupt service routine to store the number of timer interrupts in one or more scratchpad registers.

As for accuracy, the actual pulse duration is typically slightly longer than the measured value because the status of the prescaler is not readable and is reset when the timer is stopped. Thus, for maximum accuracy, it is advisable to use a small-division setting for the prescaler.

Event Counter Mode — When ICP bit 4 is cleared and all prescale bits (ICP bits 5, 6, and 7) are cleared, the timer operates in the event counter mode. This mode is used for counting pulses applied to the EXT INT pin. If ICP bit 3 is set, the timer decrements on each transition from the inactive level to the active level of the EXT INT pin. The prescaler is not used in this mode but, as in the other two timer modes, the timer may be read at any time, or may be stopped at any time by clearing ICP bit 3; ICP bit 1 functions are previously described, and the timer interrupt request latch is set on the timer's transition from H'01' to H'N' (modulo-N value).

Normally, ICP bit 0 should be kept cleared in the event counter mode; otherwise, external interrupts are generated on the transition from the inactive level to the active level of the EXT INT pin.

For the event counter mode, the minimum pulse width required on the EXT INT pin is 2 ϕ clock periods, and the minimum inactive time is 2 ϕ clock periods; therefore, the maximum repetition rate is 500 Hz.

External Interrupts
When the timer is in the interval timer mode, the EXT INT pin is available for non-timer-related interrupts. If ICP bit 0 is set, an external interrupt request latch is set when there is a transition from the inactive level to the active level of the EXT INT pin (EXT INT is an edge-triggered input). The interrupt request is latched until either acknowledged by the CPU or ICP bit 0 is cleared (unlike timer interrupt requests, which remain latched even when ICP bit 1 is cleared). External interrupts are handled in the same fashion when the timer is in the pulse width measurement mode or in the event counter mode, except that in the pulse width measurement mode the external interrupt request latch is set on the trailing edge of the EXT INT input; that is, on the transition from the active level to the inactive level.

Interrupt Handling
When either a timer or an external interrupt request is communicated to the CPU section of the F3872, it is acknowledged and processed at the completion of the first non-privileged instruction if the interrupt control bit of the status register is set. If the interrupt control bit is not set, the interrupt request continues either until the interrupt control bit is set and the CPU acknowledges the interrupt or until the interrupt request is cleared as previously described.

If there are a timer interrupt request and an external interrupt request when the CPU starts to process the requests, the timer interrupt is handled first.

When an interrupt is allowed, the CPU requests that the interrupting element pass its interrupt vector address to the program counter via the data bus. The vector address for a timer interrupt is H'20'; the vector address for an external interrupt is H'0A0'. After the vector address is passed to the program counter, the CPU sends an acknowledge signal to the appropriate interrupt request latch, which clears that latch. The execution of the interrupt service routine then commences. The return address of the original program is automatically saved in the stack register, P.

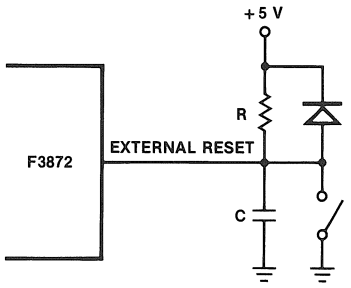
Power-On Clear
The F3872 contains power-on clear circuitry to automatically reset the internal logic following the application of external power. Since many variations of power supply circuitry exist, Fairchild cannot guarantee that the power-on clear will operate under every power-up condition.

The power-on clear circuitry contains on-chip sensors to monitor various conditions. The following conditions must be satisfied before the power-reset sequence is allowed to start:

1. Supply voltage must be above a certain value, typically +3 V to +4 V.
2. The clocks of the device must be functioning.
3. The substrate bias must reach a certain level.

All three conditions must be met before the power-on clear circuitry initiates a reset cycle. However, these conditions can be satisfied even with a supply voltage of as low as 3 volts. The latest versions of the F3872 have a modified delay circuit that gives a typical delay of 500 μs (with a 4 MHz crystal) after the above conditions are met. This is an improvement over the earlier F3872 versions.

Since the F3872 is only guaranteed to operate at a supply voltage of 4.5 V or greater, the user must ensure that the supply voltage is at least 4.5 V when the F3872 initiates the reset cycle. For power supplies having a slow rise time, an external RC network can be converted to the external reset input of the F3872 to hold the device in a reset state long enough to allow the power supply to reach a voltage of 4.5 V.



External Reset
When the $\overline{\text{RESET}}$ input is low, the contents of the program counter are pushed to the stack register and the program counter and the ICB of the status register are cleared. The original stack register contents are lost. As with power-on clear, ports 4, 5, 6, and 7 are loaded with H'00'. The contents of all other registers and ports are unchanged. When $\overline{\text{RESET}}$ is high, the first program instruction is fetched from ROM location H'0000'.

Test Logic
Special test logic is implemented to allow access to the internal main data bus for test purposes.

In normal operation, the TEST pin is unconnected or is connected to ground. When TEST is placed at a level of from 2.8 V to 3.0 V, port 4 becomes an output of the internal data bus and port 5 becomes a wired-OR input to the internal data bus. The data appearing on the port 4 pins is logically true, whereas input data forced on port 5 must be logically false. When TEST is placed at a high level (8.8 V to 9.0 V), the ports act as described above and, additionally, the program ROM is prevented from driving the data bus. In this mode, operands and instructions may be forced externally through port 5 instead of being accessed from the program ROM. When TEST is in either the TTL state or the high state, $\overline{\text{STROBE}}$ ceases its normal function and becomes a cycle clock (identical to the F8 multi-chip system write clock, except inverted).

Timing complexities render the capabilities associated with the TEST pin impractical for use in a user application, but these capabilities are sufficient to enable Fairchild to implement a rapid method for thoroughly testing the F3872.

Standby Power Option

If the standby power option is not selected, bits 0 and 1 of port 0 can be read from and written to. If the standby power-down option is selected, port 0 bit 1 is readable only; bit 0 remains both readable and writeable via software, although it is not connected to a package lead. The standby power source (V_{SB}) is connected to pin 4. (A 0.01 μF capacitor must be connected to pin 3; the purpose of this capacitor is to decouple noise coupled to the substrate of the circuit when V_{DD} is switched off and on.) Nickel-cadmium batteries (typical voltage of three series cells is 3.6 V) are recommended for use as the standby power source, since the F3872 can automatically trickle charge three such cells. If more than three cells in series are used, a charging circuit must be provided outside the F3872. When the $\overline{\text{RESET}}/\overline{\text{RAMPRT}}$ pin is brought low, the standby RAM (64 8-bit words in P0/DC address spaces 4032 to 4096_{10}, or $FC0_{16}$ to FFF_{16}) is disabled from being read from or written to. The RAM itself is also switched from V_{DD} power to the V_{SB} power.

Two modes are recommended for powering down. In the first mode (see *Figure 6A*), the processor must be interrupted early enough to save all necessary data before the V_{CC} falls below the minimum level. After the save is done, the $\overline{\text{RESET}}/\overline{\text{RAMPRT}}$ pin can fall. This prevents any further RAM accesses; V_{DD} may then fall.

The second mode (see *Figure 6B*) may be used if a special save data routine is not needed. External interrupt need not be used, and the only requirement to save the RAM data is that $\overline{\text{RAMPRT}}$ be low for V_{DD} drops below 4.5 V. For example, if a few key variables are to be stored in power-down RAM and it is desired that these be saved during a loss of power, two copies of each variable are kept with an associated flag in the power-down RAM; thus, no interrupt and save routine is necessary. The method of updating a variable is as follows:

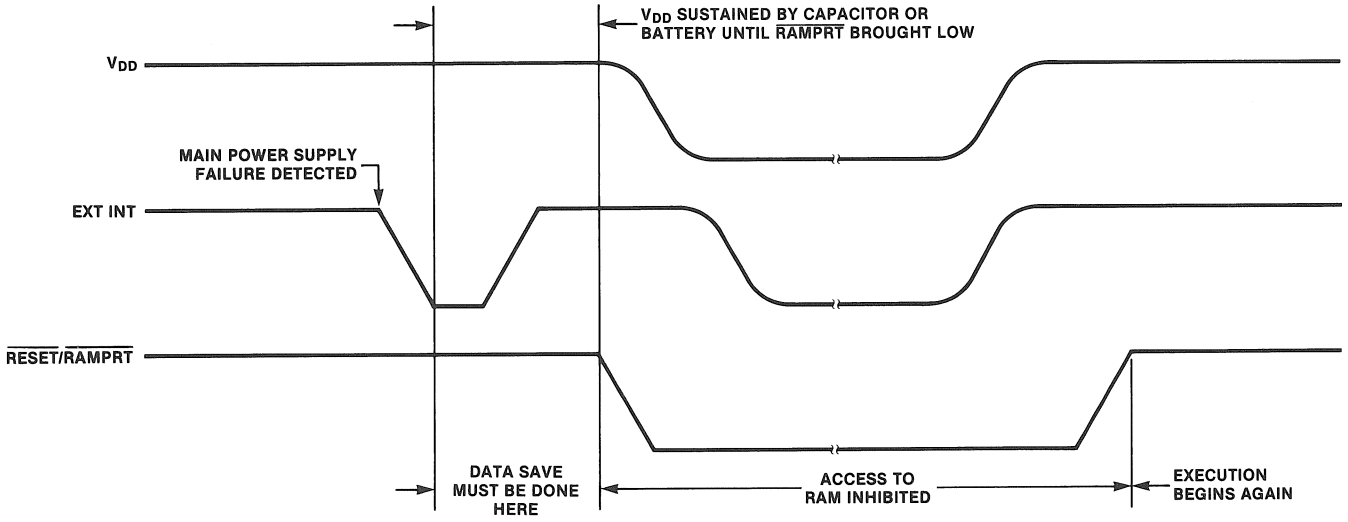
Clear Flag Word 1
Update Variable (Copy 1)
Set Flag Word 1
Clear Flag Word 2
Update Variable (Copy 2)
Set Flag Word 2

Execution may terminate at any time, even during the update of a variable of flag word, causing that byte in scratchpad to be "bad" data. There is always a "good" data byte that contains either the most recent or next-most recent value of the variable. Any copy of the variable in which the flag word is set is a good data byte. While this method significantly encumbers the data storage process, it eliminates the need for a power fail interrupt, which reduces external circuitry and leaves the external interrupt pin completely free for other uses.

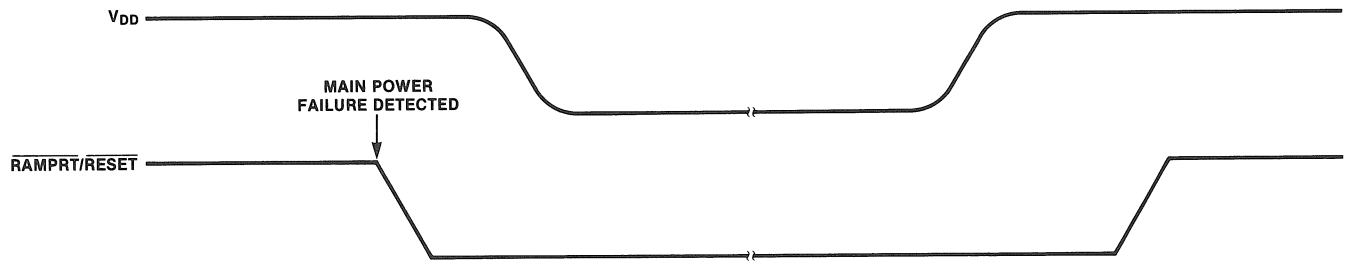
In either power-down mode, the $\overline{\text{RESET}}/\overline{\text{RAMPRT}}$ signal should be held low until V_{DD} is above the minimum level when power returns.

Fig. 6 Standby Power Option Modes

A. Data Save Routine, $V_{SB} \leq 3.2$ V



B. No Save Routine, $V_{SB} \leq 3.2$ V



F3872 Clocks

The time bases for the F3872 may originate from one of four external sources; the four external configurations are shown in *Figure 7.* There is an internal 26.5 pF capacitor between XTL_1 and GND, and also between XTL_2 and GND. Thus, external capacitors are not required. In all external clock modes, the external time base frequency is divided by 2 to form the internal ϕ clock.

Instruction Set

The F3872 executes the entire instruction set of the multi-chip F8 family (F3850 family), as shown in *Table 3.* Of course, the STORE instruction only accesses memory in locations FF0-FFF (the data counter, however, is incremented each time STORE is executed).

A summary of programmable registers and ports is given in *Figure 8.*

Also, for convenient reference, a programming model of the F3872 is given in *Figure 9.*

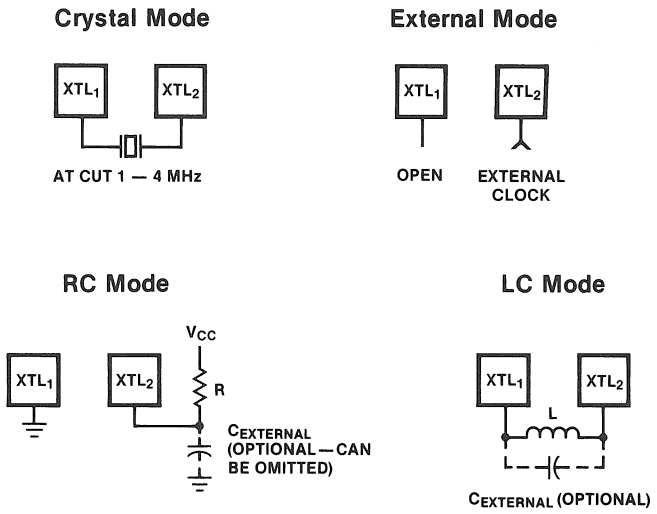
Mask Options

The ROM array may contain object program code and/or tables of nonvarying data. Every F3872 is implemented using a custom mask that specifies the state of every ROM bit, as well as certain address mask options that are external to the ROM array. The following mask options are specified:

1. The 1024, 2048, 3072, or 4096 bytes of ROM storage. This reflects programs and permanent data tables stored in the PSU memory.
2. Input/output ports can be any of the following three configurations:
   a. Standard pull-up
   b. Open drain
   c. Direct drive
3. Input/output ports 0 and 1 can be specified either cleared or unaltered following an external reset.
4. External interrupt and external reset can be specified to have or omit an internal pull-up resistor.
5. The I/O port output option choices are: the standard pull-up (option A), the open drain (option B), and the driver pull-up (option C).

The format for mask options must be submitted to Fairchild Microprocessor Division before device manufacture. The data to be stored in permanent memory may be submitted in the form of an EPROM or HP2644/HP2645 cartridge (Formulator format only). Other options must be specified on the Fairchild ROM Code Entry Form, available from a Fairchild representative.

Fig. 7 F3872 Clock Configurations



RC Mode	LC Mode
Minimum R = 4kΩ	Minimum L = 0.1 mH Minimum Q = 40
$C = 20.5\ pF \pm 2.5\ pF + C_{EXTERNAL}$	Maximum $C_{EXTERNAL} = 30\ pF$
$f_{MIN} \cong \frac{1}{1.1\ RC + 65\ ns}$	$C = 10\ pF \pm 1.3\ pF + C_{EXTERNAL}$
$f_{MAX} \cong \frac{1}{1.0\ RC + 15\ ns}$	$f \cong \frac{1}{2\pi\sqrt{LC}}$
Example with $C_{EXTERNAL} = 0$	Example with $C_{EXTERNAL} = 0$
R = 15 kΩ ± 5% f ≅ 2.9 MHz ± 26%	L = 0.3 mH ± 10% f ≅ 3.0 MHz ± 10%

Supplementary Notes

For total software compatibility when expanding into a multi-chip configuration, the F3871 Peripheral Input/Output circuit should be used. The F3871 has the same improved timer (binary count, readable, and three modes of operation) and ready strobe outputs as the F3872.

The interrupt control bit of the status register is automatically reset when an interrupt request is acknowledged. It is then the programmer's responsibility to determine when the ICB is again to be set (by executing the E1 instruction). This action prevents an interrupt service routine from being interrupted unless the programmer so desires.

Table 3 F3872 Instruction Set

Accumulator Group Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Add Carry	LNK		ACC←(ACC)+CRY	19	1	1	1/0	1/0	1/0	1/0
Add Immediate	AI	ii	ACC←(ACC)+H'ii'	24 ii	2	2.5	1/0	1/0	1/0	1/0
AND Immediate	NI	ii	ACC←(ACC) Λ H'ii'	21 ii	2	2.5	0	1/0	0	1/0
Clear	CLR		ACC←H'00'	70	1	1				
Compare Immediate	CI	ii	H'ii'+($\overline{ACC}$)+1	25 ii	2	2.5	1/0	1/0	1/0	1/0
Complement	COM		ACC←(ACC)⊕H'FF'	18	1	1	0	1/0	0	1/0
Exclusive OR Immediate	XI	ii	ACC←(ACC)⊕H'ii'	23 ii	2	2.5	0	1/0	0	1/0
Increment	INC		ACC←(ACC)+1	1F	1	1	1/0	1/0	1/0	1/0
Load Immediate	LI	ii	ACC←H'ii'	20 ii	2	2.5	—	—	—	—
Load Immediate Short	LIS	i	ACC←H'0i'	7 i	1	1	—	—	—	—
OR Immediate	OI	ii	ACC←(ACC) V H'ii'	22 ii	2	2.5	0	1/0	0	1/0
Shift Left One	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
Shift Left Four	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
Shift Right One	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
Shift Right Four	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

Branch Instructions

(In All Conditional Branches, P0 (P0)+2 if the Test Conditions Are Not Met. Execution Is Complete in 30 Cycles.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Branch on Carry	BC	aa	P0←[(P0)+1]+H'aa' if CRY=1	82 aa	2	3.5	—	—	—	—
Branch on Positive	BP	aa	P0←[(P0)+1]+H'aa' if SIGN=1	81 aa	2	3.5	—	—	—	—
Branch on Zero	BZ	aa	P0←[(P0)+1]+H'aa' if ZERO=1	84 aa	2	3.5	—	—	—	—
Branch on True	BT	t,aa	P0←[(P0)+1]+H'aa' if any test is true	8t aa	2	3.5	—	—	—	—
			t=TEST CONDITION							
			2^2 | 2^1 | 2^0							
			ZERO | CRY | SIGN							
Branch if Negative	BM	aa	P0←[(P0)+1]+H'aa' if SIGN=0	91 aa	2	3.5	—	—	—	—
Branch if No Carry	BNC	aa	P0←[(P0)+1]+H'aa' if CARRY≠0	92 aa	2	3.5	—	—	—	—
Branch if No Overflow	BNO	aa	P0←[(P0)+1]+H'aa' if OVF=0	98 aa	2	3.5	—	—	—	—
Branch if Not Zero	BNZ	aa	P0←[(P0)+1]+H'aa' if ZERO=0	94 aa	2	3.5	—	—	—	—
Branch if False Test	BF	t,aa	P0←[(P0)+1]+H'aa' if all false test bits	9t aa	2	3.5	—	—	—	—
			t=TEST CONDITION							
			2^3 | 2^2 | 2^1 | 2^0							
			OVF | ZERO | CRY | SIGN							
Branch if ISAR (Lower) 7	BR7	aa	P0←[(P0)+1]+H'aa' if ISARL≠7	8F aa	2	2.5	—	—	—	—
			P0←(P0)+2 if ISARL=7			2.0	—	—	—	—
Branch Relative	BR	aa	P0←[(P0)+1]+H'aa'	90 aa	2	3.5	—	—	—	—
Jump*	JMP	aaaa	P0←H'aaaa'	29 aaaa	3	5.5	—	—	—	—

Memory Reference Instructions (In All Memory Reference Instructions, the Data Counter Is Incremented DC←DC•1.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Add Binary	AM		ACC←(ACC)+[(DC)]	88	1	2.5	1/0	1/0	1/0	1/0
Add Decimal	AMD		ACC←(ACC)+[(DC)]	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC) Λ [(DC)]	8A	1	2.5	0	1/0	0	1/0
Compare	CM		[(DC)]+($\overline{ACC}$)+1	8D	1	2.5	1/0	1/0	1/0	1/0
Exclusive OR	XM		ACC←(ACC)⊕[(DC)]	8C	1	2.5	0	1/0	0	1/0
Load	LM		ACC←[(DC)]	16	1	2.5	—	—	—	—
Logical OR	OM		ACC←(ACC) V [(DC)]	8B	1	2.5	0	1/0	0	1/0
Store	ST		(DC)←(ACC)	17	1	2.5	—	—	—	—

*Privileged instruction

Note
JMP and PI change accumulator contents to the high byte address.

Table 3 F3872 Instruction Set (Cont.)

Address Register Group Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Add to Data Counter	ADC		DC←(DC)+(ACC)	8E	1	2.5	—	—	—	—
Call to Subroutine	PK*		P←(P0); P0U←(r12); PL←(r13)	0C	1	4	—	—	—	—
Call to Subroutine Immediate	PI*	aaaa	P←(P); P0←H'aaaa'‡	28 aaaa	3	6.5	—	—	—	—
Exchange DC	XDC		DC⟷DC1	2C	1	2	—	—	—	—
Load Data Counter	LR	DC,Q	DCU←(r14); DCL←(r15)	0F	1	4	—	—	—	—
Load Data Counter	LR	DC,H	DCU←(r10); DCL←(r11)	10	1	4	—	—	—	—
Load DC Immediate	DCI	aaaa	DC←H'aaaa'	2A aaaa	3	6	—	—	—	—
Load Program Counter	LR	P0,Q	P0U←(r14); P0L←(r15)	0D	1	4	—	—	—	—
Load Stack Register	LR	P,K	PU←(r12); PL←(r13)	09	1	4	—	—	—	—
Return From Subroutine	POP*		P0↔(P)	1C	1	2	—	—	—	—
Store Data Counter	LR	Q,DC	r14←(DCU); r15←(DCL)	0E	1	4	—	—	—	—
Store Data Counter	LR	H,DC	r10←(DCU); r11←(DCL)	11	1	4	—	—	—	—
Store Stack Register	LR	K,P	r12←(PU); r13←(P)	08	1	4	—	—	—	—

Scratchpad Register Instructions (Refer to Scratchpad Addressing Modes.)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Add Binary	AS	r	ACC←(ACC)+(r)	Cr	1	1	1/0	1/0	1/0	1/0
Add Decimal	ASD	r	ACC←(ACC)+(r)	Dr	1	2	1/0	1/0	1/0	1/0
Decrement	DS	r	r←(r)+H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
Load	LR	A,r	ACC←(r)	4r	1	1	—	—	—	—
Load	LR	A,KU	ACC←(r12)	00	1	1	—	—	—	—
Load	LR	A,KL	ACC←(r13)	01	1	1	—	—	—	—
Load	LR	A,QU	ACC←(r14)	02	1	1	—	—	—	—
Load	LR	A,QL	ACC←(r15)	03	1	1	—	—	—	—
Load	LR	r,A	r←(ACC)	5r	1	1	—	—	—	—
Load	LR	KU,A	r12←(ACC)	04	1	1	—	—	—	—
Load	LR	KL,A	r13←(ACC)	05	1	1	—	—	—	—
Load	LR	QU,A	r14←(ACC)	06	1	1	—	—	—	—
Load	LR	QL,A	r15←(ACC)	07	1	1	—	—	—	—
AND	NS	r	ACC←(ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
Exclusive OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

Miscellaneous Instructions

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
Disable Interrupt	DI		RESET ICB	1A	1	2	—	—	—	—
Enable Interrupt*	EI		SET ICB	1B	1	2	—	—	—	—
Input	IN	aa	ACC←(INPUT PORT aa)	26 aa	2	4	0	1/0	0	1/0
Input Short	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
Load ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1	—	—	—	—
Load ISAR Lower	LISL	a	ISARL←a	01101a**	1	1	—	—	—	—
Load ISAR Upper	LISU	a	ISARU←a	01100a**	1	1	—	—	—	—
Load Status Register*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
No-Operation	NOP		P0←(P0)+1	2B	1	1	—	—	—	—
Output	OUT	aa	OUTPUT PORT aa←(ACC)	27 aa	2	4	—	—	—	—
Output Short	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***	—	—	—	—
Store ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1	—	—	—	—
Store Status Register	LR	J,W	r9←(W)	1E	1	1	—	—	—	—

*Privileged instruction
**3-bit octal digit
***Two machine cycles for CPU ports
‡Contents of ACC destroyed

Table 3 F3872 Instruction Set (Cont.)

Notes
Each lower case character represents a hexadecimal digit.
Each cycle equals four machine clock periods.
Lower case denotes variables specified by the programmer.

Function Definitons

←	is replaced by
( )	the contents of
(—)	binary ones complement of
+	arithmetic add (binary or decimal)
⊕	logical OR exclusive
Λ	logical AND
V	logical OR inclusive
H'#'	hexadecimal digit

Register Names

a	address variable
A	accumulator
DC	data counter (indirect address register)
DC1	data counter #1 (auxiliary data counter)
DCL	least significant eight bits of data counter addressed
DCU	most significant eight bits of data counter addressed
H	scratchpad register #10 and #11
i and ii	immediate operand
ICB	interrupt control bit
IS	indirect scratchpad address register
ISAR	indirect scratchpad address register
ISARL	least significant three bits of ISAR
ISARU	most significant three bits of ISAR
J	scratchpad register #9
K	registers #12 and #13
KL	register #13
KU	register #12
P0	program counter
P0L	least significant eight bits of program counter
P0U	most significant eight bits of program counter
P	stack register
PL	least significant eight bits of program counter
PU	most significant eight bits of active stack register
Q	registers #14 and #15
QL	register #15
QU	register #14
r	scratchpad register (any address through 11)
W	status register

Scratchpad Addressing Modes (Machine Code Format)

r = C	(hexadecimal) register addressed by ISAR (unmodified)
r = D	(hexadecimal) register addressed by ISAR; ISARL incremented
r = E	(hexadecimal) register addressed by ISAR; ISARL decremented
r = F	(no operation performed)
r = 0-B	(hexadecimal) register 0 through 11 addressed directly from the instruction

Status Register

—	no change in condition
1/0	is set to 1 or 0, depending on conditions
CRY	carry flag

When reading the interrupt control port (port 6), bit 7 of the accumulator is loaded with the actual logic level being applied to the EXT INT pin, regardless of the status of ICP bit 2 (the EXT INT active level bit); that is, if the EXT INT pin is at +5 V, bit 7 of the accumulator is set to a logic 1, but if the EXT INT pin is at ground, accumulator bit 7 is reset to logic 0.

In *Table 3,* the number of cycles shown is "nominal machine cycles." A nominal machine cycle is defined as 4 ϕ clock periods, thus requiring 2 μs for a 2 MHz clock frequency (4 MHz external time base frequency).

Table 3 also uses the following nomenclature for register names:

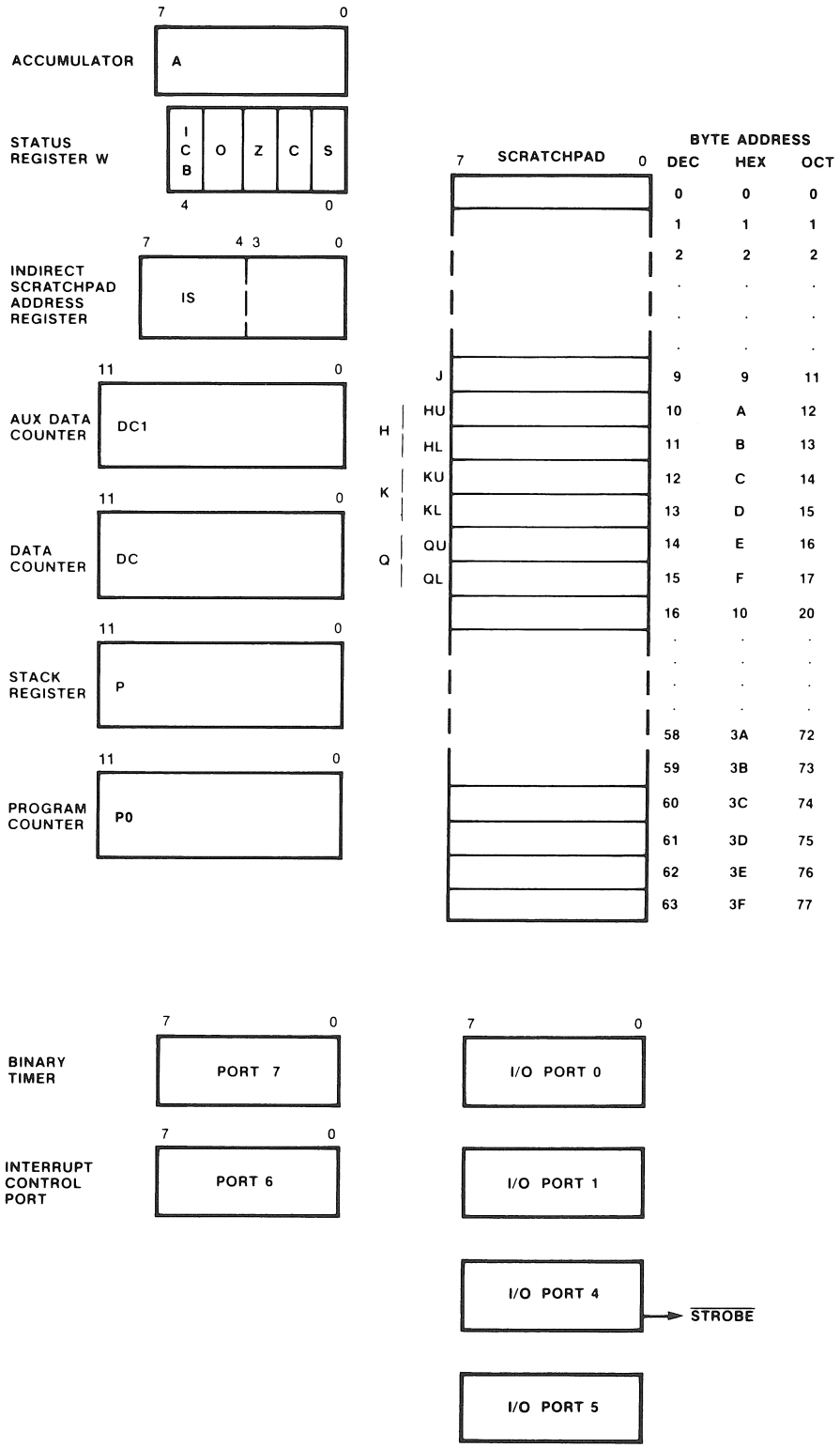
F8 ⟷ F3872
PC_0 = P0 Program Counter
PC_1 = P Stack Register
DC_0 = DC Data Counter
DC_1 = DC1 Auxiliary Data Counter

This nomenclature is used to be consistent with the assembly language mnemonics.

For the F3872, execution of an INS or OUTS instruction requires two machine cycles for ports 0 and 1, whereas ports 4 and 5 require four machine cycles.

When an external reset of the F3872 occurs, P0 pushes into P and the old contents of P are lost. It must be noted that an external reset is recognized at the start of the machine cycle and not necessarily at the end of an instruction. Thus, if the F3872 is executing a multi-cycle instruction, that instruction is not completed and the contents of P upon reset may not necessarily be the address of the instruction that would have been executed next. It may, for example, point to an immediate operand if the reset occurred during the second cycle of an L1 or C1 instruction. Additionally, several instructions (JMP, P1, PK, LR, P0 and Q) as well as the interrupt acknowledge sequence modify P0 in parts. That is, they alter P0 by loading first one part, then the other, and the entire operation takes more than one cycle. Should reset occur during this modification process, the value pushed into P is part of the old P0 (the as-yet unmodified part) and part of the new P0 (already-modified part). Thus, care should be taken (perhaps by external gating) to ensure that reset does not occur at an undesirable time if any significance is to be given to the contents of P after a reset occurs.

Fig. 8 Programmable Registers and Ports



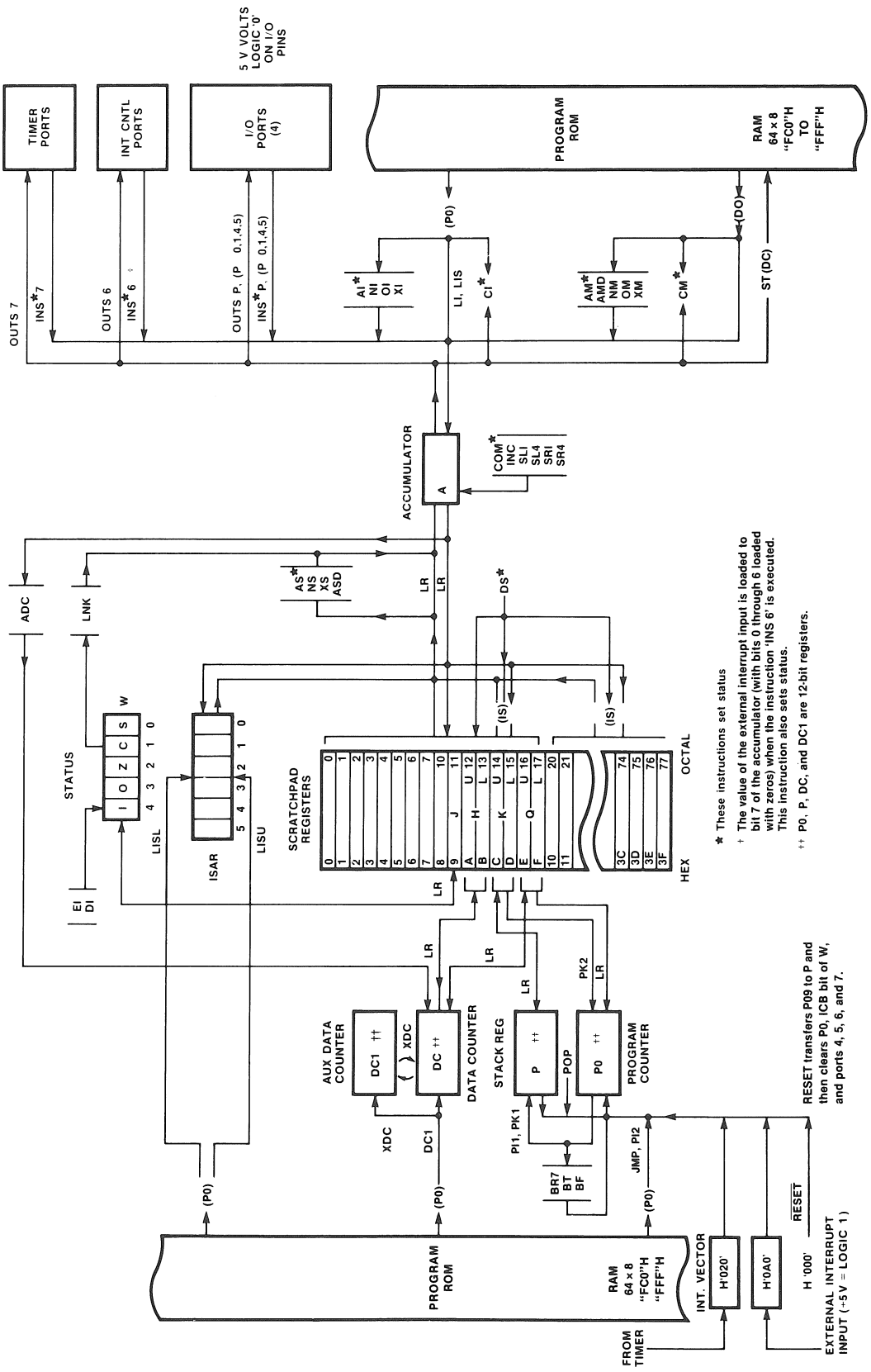


Fig. 9 Programming Model

Note:
The instructions PI and PK are shown in two sequential parts (PI1, PI2, and PK1, PK2).

Timing Characteristics

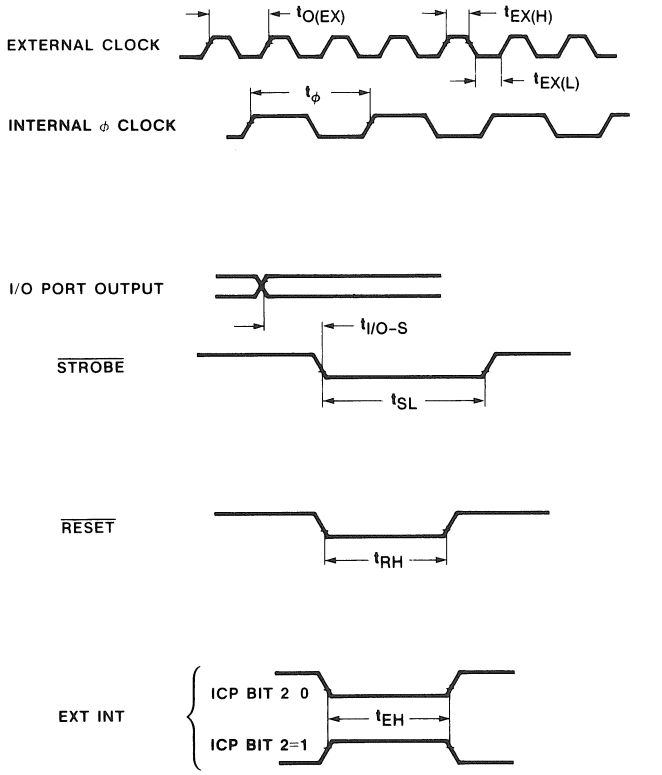
The F3872 timing characteristics are described in *Table 4* and illustrated in *Figures 10* and *11.*

Table 4 Timing Characteristics

Signal	Symbol	Characteristic	Min	Max	Unit	Notes
XTL_1 XTL_2	$t_o(EX)$	Time Base Period, All External Modes	250	1000	ns	4 MHz–1 MHz
	$t_{EX}(H)$	External Clock Pulse Width, High	90	700	ns	
	$t_{EX}(L)$	External Clock Pulse Width, Low	100	700	ns	
ϕ	t_ϕ	Internal ϕ Clock Period	$2t_\phi$			
WRITE	t_W	Internal WRITE Clock Period	$4t_\phi$ $6t_\phi$			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output Delay from Internal WRITE Clock	0	1000	ns	50 pF Plus One TTL Load
	$t_{sI/O}$	Input Setup Time to WRITE Clock	1000		ns	
$\overline{STROBE}$	$t_{I/OS}$	Output Valid to $\overline{STROBE}$ Delay	$3t_\phi$ -1000	$3t_\phi$ $+250$	ns	Note 1
	t_{SL}	$\overline{STROBE}$ Low Time	$8t_\phi$ -250	$12t_\phi$ $+250$	ns	
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ Hold Time, Low	$6t_\phi$ $+750$		ns	
EXT INT	t_{EH}	EXT INT Hold Time, Active State	$6t_\phi$ $+750$		ns	To Trigger Interrupt
		EXT INT Hold Time, Inactive State	$2t_\phi$		ns	To Trigger Timer; Note 2
	C_{IN}	Input Capacitance: I/O Ports, $\overline{RESET}$, EXT INT RAMPRT, TEST		7	pF	Unmeasured Pins Returned to V_{SS}; Note 3
	C_{XTL}	Input Capacitance: XTL_1, XTL_2	23.5	29.5	pF	Unmeasured Pins Returned to V_{SS}; Note 3

Notes
1. I/O load is 50 pF plus one standard TTL input; $\overline{STROBE}$ load is 50 pF plus three standard TTL inputs.
2. Specification is applicable when the timer is in the interval timer mode.
3. $T_A = 25°C$, f = 2 MHz.
4. $T_A = 0°C$ to $+70°C$, $V_{CC} = +5\ V \pm 10\%$, I/O power dissipation $\leq$ mW, unless otherwise noted.

Fig. 10 Timing Diagrams



Note
All measurements are referenced to V_{IL} max, V_{IH} min, V_{OL} max, or V_{OH} min

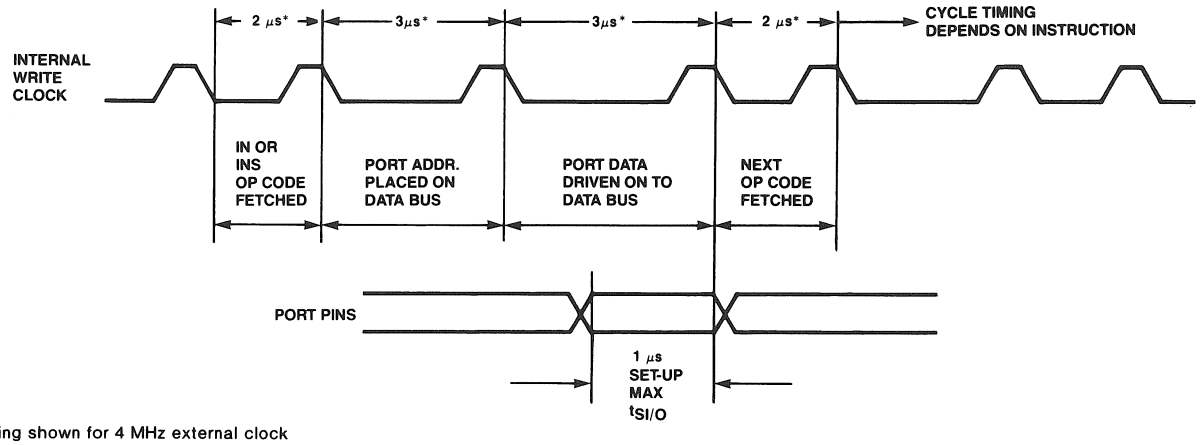
Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Voltage on any Pin with Respect to Ground (Except Open-Drain Pins)	− 1.0 V, + 7 V
Voltage on any Open-Drain Pin	− 1.0 V, + 13.2 V
Power Dissipation	1.5 W
Ambient Temperature Under Bias	0 °C, + 70 °C
Storage Temperature	− 55 °C, + 150 °C

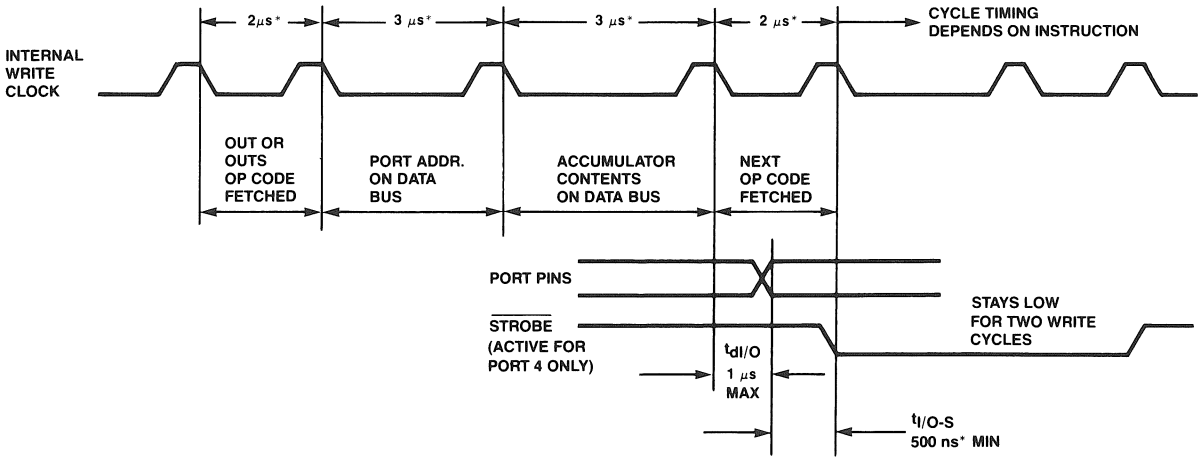
Fig. 11 Port Input/Output Timing Diagrams

A. Input on Port 4 or 5



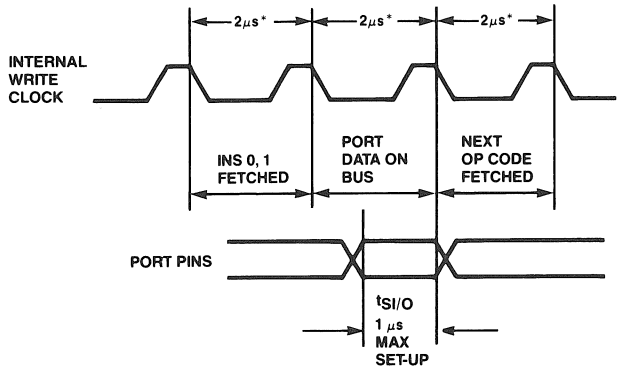
*Cycle timing shown for 4 MHz external clock

B. Output on Port 4 or 5



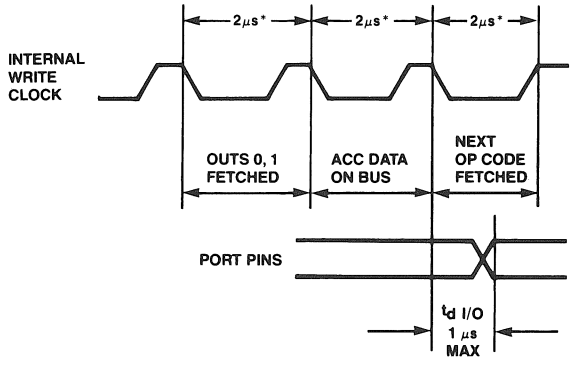
*Cycle timing shown for 4 MHz external clock

C. Input on Port 0 or 1



*Cycle timing shown for 4 MHz external clock

D. Output on Port 0 or 1



*Cycle timing shown for 4 MHz external clock

DC Characteristics

The dc characteristics of the F3872 are described in *Table 5.*

Table 5 DC Characteristics

Symbol	Characteristic	Min	Max	Unit	Conditions
I_{CC}	Power Supply Current		100	mA	Outputs Open
P_D	Power Dissipation		500	mW	Outputs Open
V_{IHEX}	External Clock Input High Voltage	2.4	5.8	V	
V_{ILHEX}	External Clock Input Low Voltage	−0.3	0.6	V	
I_{HEX}	External Clock Input High Current		100	μA	$V_{IHEX} = V_{DD}$
I_{ILEX}	External Clock Input Low Current		−100	μA	$V_{ILEX} = V_{SS}$
V_{IH}	Input High Voltage $\overline{\text{RESET}}$, EXT INT	2.0	5.8	V	$\overline{\text{RESET}}$ and EXT INT Have Internal Schmitt Triggers Giving Minimum 0.2 V Hysteresis
V_{IL}	Input Low Voltage $\overline{\text{RESET}}$, EXT INT	−0.3	0.8	V	
V_{IHOD}	Input High Voltage (Open-Drain Ports)	2.0	13.2	V	
I_{IL}	Input Low Current $\overline{\text{RESET}}$, EXT INT		−1.6	mA	$V_{IL} = 0.4V$ Note 1
I_{LOD}	Leakage Current (Open-Drain Ports)		10 −5.0	μA	$V_{IN} = 13.2$ V $V_{IN} = 0.0$ V Note 2
I_{OH}	Output High Current $\overline{\text{RESET}}$, EXT INT	−100 −30		μA	$V_{OH} = 2.4$ V $V_{OH} = 3.9$ V
I_{OHDD}	Output High Current (Direct-Drive Ports)	−0.1		mA	$V_{OH} = 2.4$ V
		−1.5		mA	$V_{OH} = 1.5$ V
			−8.5	mA	$V_{OH} = 0.7$ V
I_{OL}	Output Low Current	1.8		mA	$V_{OL} = 0.4$ V
I_{OHS}	Output High Current ($\overline{\text{STROBE}}$ Output)	−300		μA	$V_{OH} = 2.4$ V
I_{OLS}	Output Low Current ($\overline{\text{STROBE}}$ Output)	5.0		mA	$V_{OL} = 0.4$ V
V_{IHRPR}	$\overline{\text{RAMPRT}}$ Input High Level	1.9	5.8	V	Guaranteed 0.1 V less than V_{IH} for $\overline{\text{RESET}}$
V_{ILRPR}	$\overline{\text{RAMPRT}}$ Input Low Level	−0.3	0.4	V	Guaranteed 0.1 V less than V_{IL} for $\overline{\text{RESET}}$
V_{SB}	Standby V_{DD} for RAM	3.2	5.5	V	
I_{SB}	Standby Current		6.0 3.7	mA mA	$V_{SB} = 5.5$ V $V_{SB} = 3.2$ V
I_{CHG}	Trickle Charge Available on V_{SB} with $V_{DD} - 4.5$ to 5.5 V	−0.8	 −15	mA mA	$V_{SB} = 3.8$ V $V_{SB} = 3.2$ V
P_{DIO}	Power Dissipated by I/O Pins		600 60	mW mW	All Pins Any One Pin, Note 3

Notes
1. RESET or EXT INT programmed with standard pull-up.
2. RESET or EXT INT programmed without standard pull-up.
3. Power dissipation of I/O pins is calculated by $\Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
4. $T_A = 0°C$ to $+70°C$, $V_{DD} = +5$ V ± 10%, I/O power dissipation ≤ 100 mW.

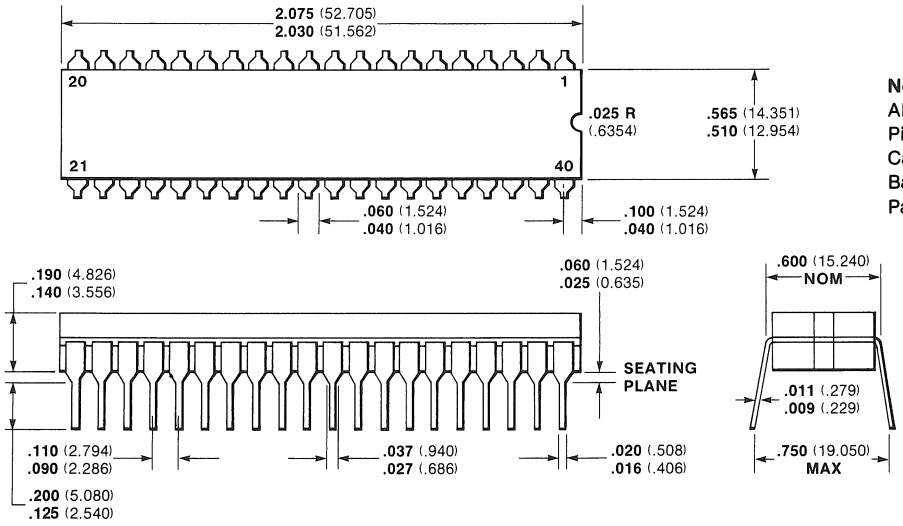
Ordering Information

Order Code	Package	Temperature Range*
F3872DC, F38L72DC	Ceramic	C
F3872DL, F38L72DL	Ceramic	L
F3872DM, F38L72DM	Ceramic	M
F3872PC, F38L72PC	Plastic	C
F3872PL, F38L72PL	Plastic	L
F3872PM, F38L72PM	Plastic	M

*C = Commercial Temperature Range 0°C to +70°C
L = Limited Temperature Range −40°C to +85°C
M = Military Temperature Range −55°C to +125°C

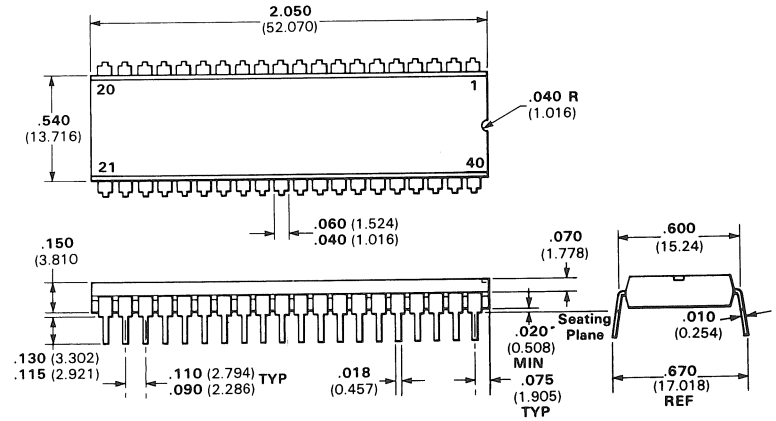
Package Outlines

40-Pin Ceramic Dual-In-Line



Notes
All dimensions are in inches **bold** and millimeters (parentheses).
Pin material is nickel gold-plated kovar.
Cap is kovar.
Base is ceramic.
Package weight is 6.5 grams.

40-Pin Plastic Dual In-Line Package



Notes
All dimensions are in inches **bold** and millimeters (parentheses).
Pins are tin-plated kovar.
Package material is plastic.
Packages are intended for insertion in hole rows on **0.600** (15.24) centers and are shipped with positive misalignment of pins to facilitate insertion.