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FUJITSU

PRODUCT PROFILE

MB86685
Integrated Terminal Controller (ITC_155)

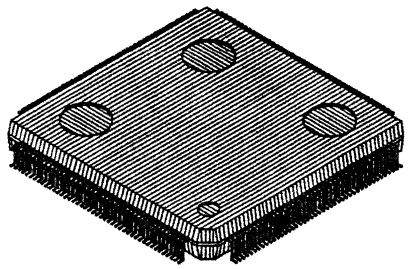
Integrated Terminal Controller

The FUJITSU MB86685, ITC155, is a single chip ATM controller for ATM terminal equipment. It integrates AAL5 Segmentation and Re-assembly processing with SONET framing at 155 Mbps and 51 Mbps.

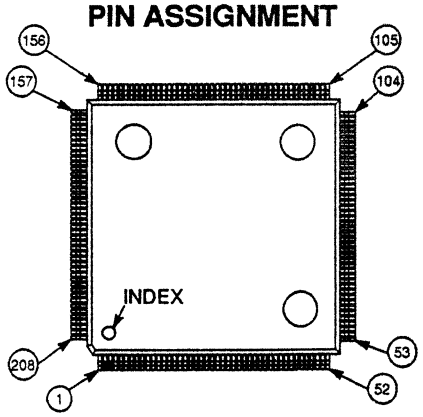
The ITC incorporates a PCI compliant 32-bit master / slave interface.

The ITC is targeted at low cost ATM Network Interface Cards for PCs and workstations. The device conforms to all relevant ATM Forum, CCITT, and ANSI standards.

PLASTIC PACKAGE
SQFP208



PIN ASSIGNMENT



FEATURES

- Combines a full-duplex segmentation and re-assembly controller with physical layer framing functions.
- Supports segmentation and reassembly on up to 4K simultaneous VCs, with 32 separate traffic profiles.
- Implements AAL5 adaptation layer protocols on each VC.
- Implements physical layer framing functions for SONET STS3c at 155.54 Mb/s, STS-1 at 51.84 Mb/s, and SDH STM-1 at 155.54 Mb/s.
- Supports local RAM interface for temporary storage of reordered receive cell data, allowing system bus decoupling from transceiver interface.
- Supports Linked Lists on System bus.
- Performs traffic shaping for each VC using peak and sustainable cell rate parameters, and also supports ABR traffic.
- Supports physical layer OAM functions for STS3c and STM-1 traffic flows.
- Includes a PCI compliant 32-bit master / slave interface in accordance with PCI Local Bus Specification Revision 2.0 (April 1993).
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1. OVERVIEW

The ITC is a bus master device. A system diagram is shown in Fig. 1.

It is a highly integrated ATM terminal controller, providing support for AAL5 adaptation layer and SONET STS-3c, STS-1 and SDH STM-1 physical layer functions. AAL5 frame processing, segmentation and re-assembly is supported on up to 4096 full duplex Virtual Channels (VC's) simultaneously. Four channels are reserved for use by the ITC.

Traffic shaping on each VC can be controlled by 32 separate traffic profiles, using Peak, Sustainable, CLP0 and CLP1 parameters, based on a 'Leaky Bucket' principle.

Each profile can be configured to support CBR, VBR or ABR traffic.

The ITC master supports Linked Lists on a channel basis, whereby data to be transferred across the system bus can be fragmented among multiple areas in main system memory.

In the receive direction, transceiver data can be temporarily buffered in Local Ram memory, on a channel basis, allowing data to be transferred across the system bus independently of the transceiver interface ordering.

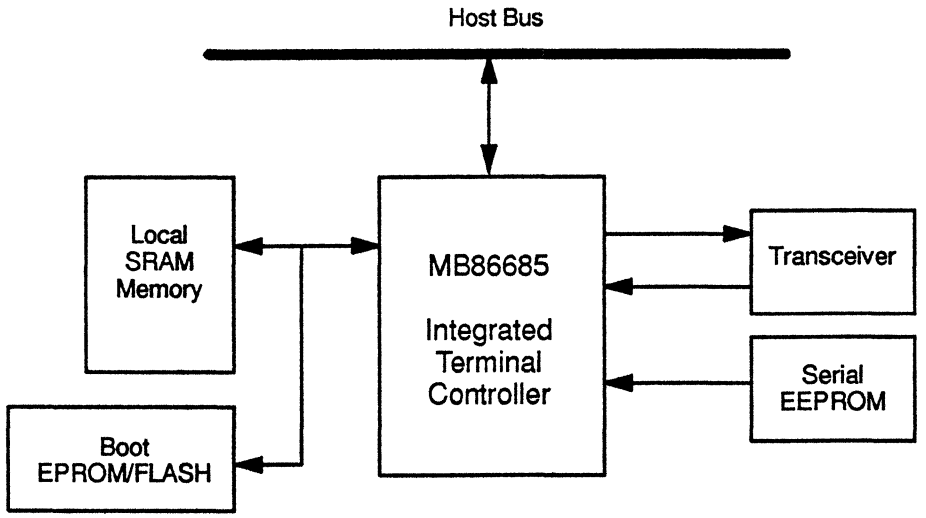


Fig. 1 – ITC system configuration

2. EXTERNAL INTERFACES

2.1 Logical Outline

A logical view of the ITC's external pins is as shown in Fig. 2, and the physical pin assignment lists (several pages) are as shown in Table 1.

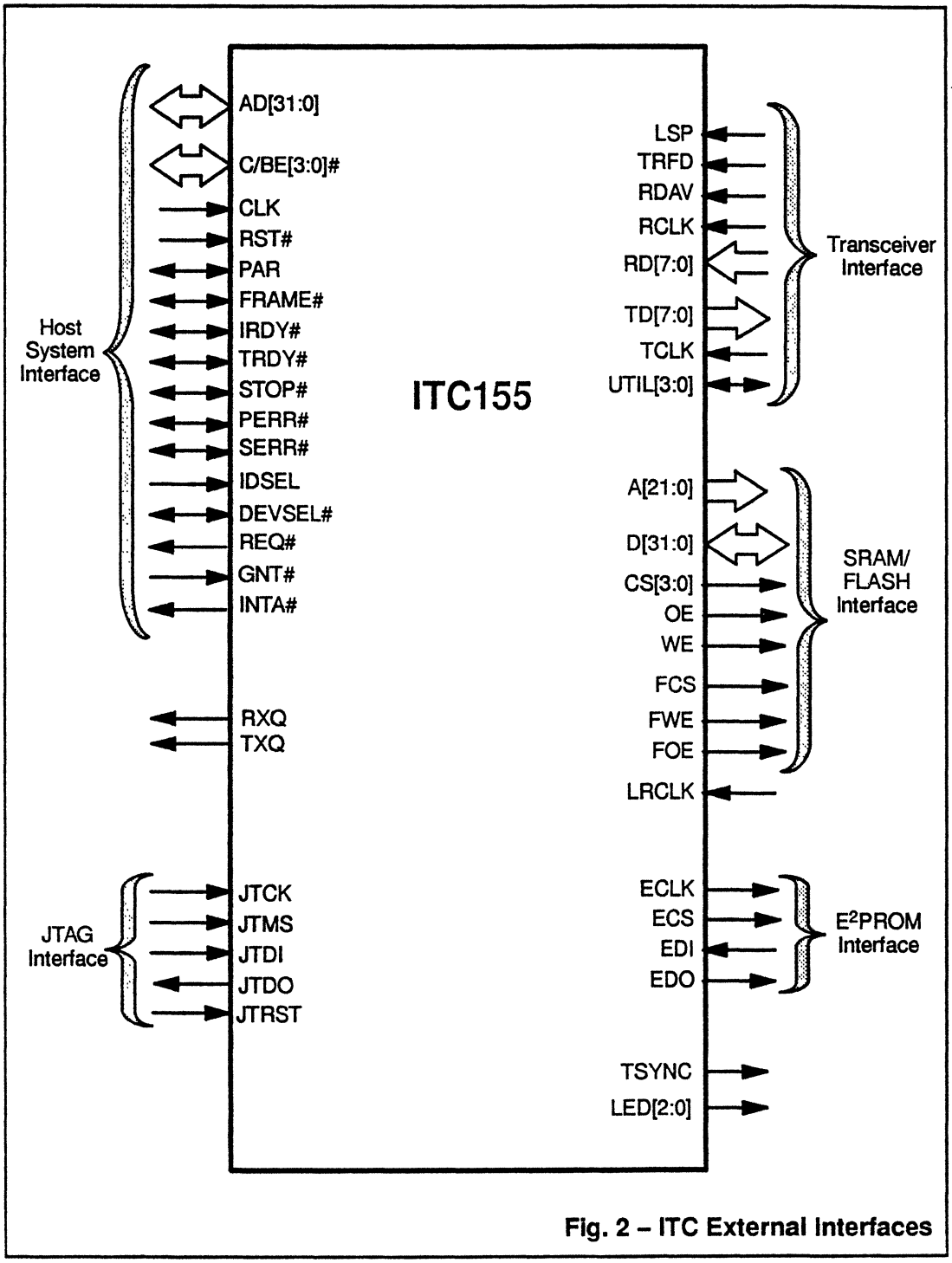


Fig. 2 – ITC External Interfaces

PIN	SIGNAL	POLARITY	TYPE
1	AD[30]	H	I/O
2	AD[29]		
3	VSS*		
4	AD[28]	H	I/O
5	AD[27]		
6	AD[26]		
7	AD[25]		
8	AD[24]		
9	VSS*		
10	VDD*		
11	C/BE[3]#	L	I/O
12	IDSEL	H	I
13	AD[23]	H	I/O
14	AD[22]		
15	VSS*		
16	VDD*		
17	AD[21]	H	I/O
18	AD[20]		
19	AD[19]		
20	AD[18]		
21	VSS*		
22	AD[17]	H	I/O
23	AD[16]		
24	C/BE[2]#	L	I/O
25	FRAME#	L	I/O
26	VSS*		
27	VDD*		
28	IRDY#	L	I/O
29	TRDY#	L	I/O
30	DEVSEL#	L	I/O
31	STOP#	L	I/O
32	VSS*		
33	PERR#	L	I/O
34	SERR#	L	W/O
35	PAR	H	I/O
36	C/BE[1]#	L	I/O
37	VDD*		

PIN	SIGNAL	POLARITY	TYPE
38	VSS*		
39	AD[15]	H	I/O
40	AD[14]		
41	AD[13]		
42	AD[12]		
43	VDD*		
44	VSS*		
45	AD[11]	H	I/O
46	AD[10]		
47	AD[9]		
48	AD[8]		
49	C/BE[0]#	L	I/O
50	VSS*		
51	AD[7]	H	I/O
52	AD[6]		
53	AD[5]		
54	AD[4]		
55	VSS*		
56	AD[3]	H	I/O
57	AD[2]		
58	AD[1]		
59	AD[0]		
60	VSS*		
61	VDD*		
62	VDD		
63	VSS		
64	LRCLK	PE	I
65	A[0]	H	O
66	A[1]		
67	VSS		
68	A[2]	H	O
69	A[3]		
70	A[4]		
71	A[5]		
72	VSS		
73	A[6]	H	O
74	A[7]		

PIN	SIGNAL	POLARITY	TYPE
75	A[8]	H	O
76	A[9]		
77	A[10]		
78	VSS		
79	VDD		
80	A[11]	H	O
81	A[12]		
82	A[13]		
83	A[14]		
84	A[15]		
85	VSS		
86	A[16]	H	O
87	A[17]		
88	A[18]		
89	A[19]		
90	VSS		
91	A[20]	H	O
92	A[21]		
93	CS[0]	L	O
94	CS[1]		
95	CS[2]		
96	VSS		
97	VDD		
98	CS[3]	L	O
99	OE	L	O
100	WE	L	O
101	D[31]	H	I/O
102	VSS		
103	D[30]	H	I/O
104	D[29]		
105	D[28]		
106	D[27]		
107	VSS		
108	D[26]	H	I/O
109	D[25]		
110	D[24]		
111	D[23]		

PIN	SIGNAL	POLARITY	TYPE
112	D[22]	H	I/O
113	VSS		
114	VDD		
115	D[21]	H	I/O
116	D[20]		
117	D[19]		
118	D[18]		
119	VSS		
120	D[17]	H	I/O
121	D[16]		
122	D[15]		
123	D[14]		
124	D[13]		
125	VSS		
126	D[12]	H	I/O
127	D[11]		
128	D[10]		
129	D[9]		
130	VSS		
131	VDD		
132	D[8]	H	I/O
133	D[7]		
134	D[6]		
135	D[5]		
136	D[4]		
137	VSS		
138	D[3]	H	I/O
139	D[2]		
140	D[1]		
141	D[0]		
142	VSS		
143	FOE	L	O
144	FWE	L	O
145	FCS	L	O
146	ECLK	PE	O
147	VDD		
148	ECS	H	O

PIN	SIGNAL	POLARITY	TYPE
149	EDI	H	I
150	EDO	H	O
151	LED[2]	L	O
152	LED[1]		
153	LED[0]		
154	VSS		
155	RXQ	H	O
156	TXQ	H	O
157	UTIL[3]	H	I/O
158	UTIL[2]		
159	VSS		
160	UTIL[1]	H	I/O
161	UTIL[0]		
162	LSP	H	I
163	RDAV	H	I
164	VSS		
165	VDD		
166	TRFD	H	I
167	VSS		
168	TD[0]	H	O
169	TD[1]		
170	VSS		
171	TD[2]	H	O
172	TD[3]		
173	VDD		
174	TD[4]	H	O
175	TD[5]		
176	VSS		
177	TD[6]	H	O
178	TD[7]		
179	TCLK	PE	I
180	RCLK	PE	I
181	VSS		
182	RD[0]	H	I
183	VDD		
184	RD[1]	H	I
185	RD[2]		

PIN	SIGNAL	POLARITY	TYPE
186	RD[3]	H	I
187	RD[4]		
188	RD[5]		
189	VSS		
190	RD[6]	H	I
191	RD[7]		
192	TSYNC	H	O
193	JTCK	PE	I
194	JTMS	H	I
195	JTDI	H	I
196	JTDO	H	O
197	JTRST	L	I
198	VSS		
199	VDD		
200	VSS*		
201	VDD*		
202	INTA#	L	W/O
203	RST#	L	I
204	CLK	PE	I
205	VSS*		
206	GNT#	L	I
207	REQ#	L	O
208	AD[31]	H	I/O

Polarity, H = High, L = Low, PE = Positive Edge, NE = Negative Edge
Type, I = Input, O = Output, I/O = Bi-directional, W/O = Wired-Or

VDD*, VSS* Supplies for PCI bus

Table 1 – Physical Pin Assignments

2.2 Detailed Description

2.2.1 Host Interface

The host interface to the ITC is a PCI bus interface, which can be driven directly by the ITC, at up to 33 MHz.

The ITC conforms to the Functional and Protocol details specified in revision 2.0 of the specification.

The following mandatory 49 signals provide full master / slave capability for a 32 bit address / data interface.

CLK
Master rising edge timing reference for all signals, except RST# and INTA#.

RST#
Asynchronous reset signal, used to bring PCI specific logic to a consistent state.

AD[31:0]
Multiplexed Address and Data bus.

C/BE[3:0]#
Bus command and Byte enables.

PAR
Even parity for AD and C/BE.

FRAME#
Start and duration of a bus access.

TRDY#
Target (Slave) Ready.

IRDY#
Initiator (Master) Ready.

STOP#
Target requests Master to stop current transaction.

DEVSEL#
Device Select.

IDSEL
Initialisation Device Select.

PERR#
Parity Error.

SERR#
System Error.

REQ#
Request to use the bus.

GNT#
Grant, ie permission to use the bus.

The following signal is optional for PCI bus compatibility, but is supported by the ITC :-

INTA#
Interrupt request.

Miscellaneous
The following two signals assist the host to determine the state of the ITC queues.

RXQ
The host memory receive queue contains entries.

TXQ
There is space for less than 16 more pairs of entries on the host memory transmit queue.

2.2.2 Local Ram Interface

The local ram interface is used to access the static ram, or an EPROM. The ram is used to store all descriptors and control information required by the ITC, and to store payload data.

A[21:0]
Ram or EPROM Address.

D[31:0]
Ram or EPROM Data.

CS[3:0]
Ram Chip Select signals.

OE
Ram Output Enable.

WE
Ram Write Enable.

LRCLK
Optional clock input, for local ram timing. The local ram bandwidth is determined by either the PCI clock (CLK) or the LRCLK input. If the PCI CLK frequency is not sufficient, a higher frequency LRCLK must be supplied, up to a maximum frequency of 40 MHz.

FCS
Chip Select for the Flash PROM.

FWE
Write enable for the Flash PROM.

FOE
Output enable for the Flash PROM.

2.2.3 Transceiver Interface

The receive and transmit interfaces connect directly to the Fujitsu transceiver chips MB582 and MB583.

RD[7:0]
Receive Data.

RDAV
Receive Data Available.

RCLK
Receive Clock (19.44 MHz).

LSP
Low received Signal Power from transceiver.

TD[7:0]
Transmit Data.

TCLK
Transmit Clock.

TRFD
Transmit Ready For Data.

UTIL[3:0]
Host programmable interface. These pins can be individually configured to be Inputs or Outputs.

2.2.4 E^2PROM Interface

The EEPROM is used for the storage of non-volatile information, eg chip ID.

ECLK
Clock.

ECS
Chip Select.

EDI
Data Input.

EDO
Data Output.

2.2.5 JTAG Interface

A 4-pin general purpose TAP (test access port) is provided for boundary scan access to the ITC. The port conforms to IEEE P1149.1-1990 and contains the following signals.

JTCK
Test Clock Input.

JTMS
Test Mode Select.

JTDI
Test Data Input. Serial input for test instructions and data.

JTDO
Test Data Output. Serial output for test instructions and data.

JTRST
Test Reset.

2.2.6 Miscellaneous

TSYNC
Start of SONET frame, or start of cell in unframed mode, for transmit data.

LED[2:0]
Host programmable LED indicators.

3. FUNCTIONAL DESCRIPTION

The ITC is divided into the following functional units, as shown in Fig. 3.

- Host Interface
- Local Ram Interface
- Address Map Module
- Traffic Management
- Transceiver Interface
- Miscellaneous
  - OAM
  - Transparent Modes
  - Initialisation
  - Statistics

3.1 Host Interface

The ITC is a bus master device, and supports a linked list mechanism, whereby data to be transferred across the system bus can be fragmented among multiple areas in main system memory.

Host access is via a memory mapped mechanism, as defined in the Functional Operations section.

Linked Lists
Data transfers across the system bus are controlled by descriptors. The descriptor format is shown in the Functional Operations section. A separate linked list is required for each channel.

The host must initialise two pools of descriptors in main memory, where each descriptor points to its own data area, and to the next descriptor in the chain.

The ITC will allocate descriptors from the receive pool to receive channels as required, and construct a linked list of data areas in host memory, on a per channel basis. The ITC will inform the host of the start address of each list.

Transmit linked lists must be constructed by the host, and the start address of each list sent to the ITC. The ITC will process the lists as required, and return used descriptors to the free transmit pool.

Various control options are available when each descriptor has been processed.

Data Transfers
Data is transferred across the PCI bus in bursts, where a burst consists of an address, followed by multiple data words. The maximum burst length of a data transfer is 12 transfers (48 bytes), which is sufficient to transfer one ATM cell payload. This avoids retaining ownership of the bus for long periods, while maintaining high throughput and low bus utilisation.

ITC Bus Utilisation
The ITC will support PCI bus operation up to 33 MHz, and must arbitrate for use of the bus. The arbitration can normally be carried out in parallel with an existing bus access, or may require up to two clock cycles for a high priority device. The (recommended) data burst transfer requires an address cycle, plus 12 data clock cycles, followed by an unused cycle at the end of the bus access.

This sequence requires on average 16 clock cycles for a 48 byte transfer. The control descriptors transferred at the start and finish of a frame require a total of about 24 clock cycles, which produces a total sequence of around 104 clock cycles, for a 5 cell frame.

The total ATM bi-directional traffic amounts to 35 MB/s. On a 33 MHz PCI bus, the ITC will therefore require about 45% bus utilisation.

3.2 Local Ram Interface

The local ram is used to store cell data, channel descriptors, and all other housekeeping information required by the ITC.

The organisation of the local ram is as shown in the Functional Operations section.

The interface is autonomously controlled by the ITC, using local ram descriptors, and once initialised does not require host attention.

Up to 16 M bytes of static ram can be supported, organised as N words by 4 bytes. To maintain ITC performance, the ram must have a maximum cycle time of about 25ns, but a separate ram clock allows faster or slower ram to be used in a cost/performance tradeoff.

3.3 Address Map Module

The ITC can support up to 4096 bi-directional channels. Virtual channels (VPI/VCI addresses) are mapped to physical channels (numbered from 0 upwards) using the following mechanism.

An ATM cell header contains an 8 bit VPI field, and a 16 bit VCI field. The ITC can only support a maximum of 13 address bits from the above two fields, as shown in Fig. 4.

The bit selections within each field must be contiguous, and start at bit 0.

The Concatenated VPI/VCI (CPC) Size parameter is used to select the total number of CPC bits used for address translations. The VPI Size parameter is used to select the number of VPI bits within the CPC address.

The address formed from the concatenated P and C bits is used to directly address a block of pointers in local ram. These pointers are then used to access the local ram descriptors.

A local ram descriptor pair (Rx and Tx) exists for each physical channel supported. The channels are numbered from 0 up to Maxch.

Reserved Channels
Three descriptors are reserved for OAM cells, RM cells and a Dump channel.

Maximum Channels
The ITC can be configured to support up to a maximum number of physical channels, using the Maxch parameter. The number of pointers initialised by the host must not exceed this value eg 3 in Fig. 4.

This strategy allows a large spread of VPI/VCI address bits to be used, while allowing only a small number of actual VCC channels to be supported.

Transmit channels can support a full width VPI / VCI address.

3.4 Traffic Management

The traffic management module is responsible for controlling all data transmitted by the ITC, and contains 32 traffic profiles. Each profile can be configured to control CBR, VBR or ABR traffic.

3.4.1 CBR Profile Parameters

Constant Bit Rate profiles operate on a leaky bucket principle, defined in terms of the following parameters.

Peak Transmission Rate
This parameter determines the rate at which cells can be transmitted. It consists of two 4-bit fields, a mantissa and an exponent. The method provides approximately a 6% resolution in cell transmission scheduling, and the time interval between transmitted cells can be varied between approximately 2 microseconds and 20 milliseconds.

Sustainable Cell Rate
This 5 bit counter determines the fractional tokens (N÷32) added to the leaky bucket, at peak rate intervals. Each time the counter overflows, a cell is added to the bucket, while the residue remains in the counter.

Leaky Bucket Capacity
This 8-bit register determines the size of the leaky bucket ie the maximum number of cells (represented by tokens) which can be sent at peak rate intervals. Each time a cell is transmitted the number of tokens in the bucket is decremented by one. A cell will only be transmitted if a token is available, and once empty, the bucket must be refilled before transmission can resume.

CLP0 Rate
This 7-bit counter determines the ratio of CLP0 to CLP1 cells. Normally, 1 in N cells will be scheduled to be sent as CLP1 ie the cell can be discarded in a congested network. Each time a cell is scheduled, the counter is decremented, and when it reaches zero, the cell is transmitted as CLP1.

The counter can be set to predefined values to enable cells to always be sent as either CLP0 (counter = 7E) or CLP1 (counter = 7F).

Profile Priority
This 2-bit field defines the profile priority. The lowest priority is 0, and the highest 3. Higher priority profile requests will pre-empt lower priority requests.

Pre-empted profile requests will be marked as pending, and serviced when no other higher priority profiles are scheduled.

Priority 0 profiles are of type ABR.

3.4.2 ABR Profile Parameters

Available Bit Rate profiles operate on an opportunistic, dynamically varying peak rate, and are defined in terms of the following parameters.

Allowed Cell Rate, ACR
A dynamically adjusted rate (controlled by MDF or AIR) at which cells are actually transmitted by the traffic manager, on a VC basis.

Peak Cell Rate, PCR
A per VC maximum cell rate, which must not be exceeded by the ACR.

Minimum Cell Rate, MCR
A per VC minimum value for the ACR.

Initial Cell Rate, ICR
A per VC initial value for ACR. The channel will drop to this rate, when idle.

Additive Decrease Rate, ADR
A per VC factor, which is used to decrease the ACR, at ACR intervals.

Multiplicative Decrease Factor, MDF
A per VC factor, used to calculate ADR.

Additive Increase Rate, AIR
A per VC factor used to increase the ACR, on reception of an RM cell.

Nrm
A per VC counter value, decremented at ACR intervals, which when zero gives the opportunity for the generation of an RM cell.

3.4.3 GFC Protocol

A per link ABR control mechanism is also available, defined in terms of the GFC field.

Four codes are specified in the Rx direction, as follows :-

0000 Null & No Halt
0100 Null & Halt
1000 Reset & No Halt
1100 Reset & Halt

Reset refers to a credit counter, which must contain tokens to allow ABR traffic to be scheduled. A reset command restores the initial value in the counter.

ABR cells sent in the Tx direction will have their GFC field set to 0001.

The GFC mechanism can be inhibited using a mode control bit.

3.4.4 Parameter Values

At call setup, the host must agree the quality of service required with the network. Traffic conformance is then maintained by setting the values of the parameters to meet the agreed profile.

3.4.5 Channel Assignments

Any VC can be assigned to any traffic profile. If multiple VC's are assigned to the same profile, the cells are transmitted contiguously, unless interrupted by a higher priority profile. All channels assigned to the higher priority profile will be serviced, before the lower priority profile queue is restarted. Diagrams are shown in Fig. 5 and Fig. 6.

CBR Traffic
CBR traffic can be handled by assigning the channels to the highest priority profile. This will ensure that the channel cells are always transmitted when the peak rate counter terminates, unless a clash occurs with another high priority profile. In these circumstances, the channels will be handled in the order in which the profiles are found, using the ITC search algorithm. This continuously checks all profiles, in a circular fashion, looking for terminated peak rate counters.

VBR Traffic
This is similar to CBR traffic, except that the data will occur in bursts, provided that the sustainable rate is less than the peak rate.

ABR Traffic
ABR traffic must be assigned to the lowest possible priority profile. This will ensure that the channel cells are only transmitted when other traffic is not scheduled.

ABR Channel Reassignment
If a channel assigned to a particular profile is required to alter its transmission rate, it is re-assigned to another profile automatically.

3.5 Transceiver Interface

Physical Interface
The transceiver interface consists of two sections, a receive and a transmit port. Each port contains an 8 bit parallel data bus, and associated control signals, and connects directly to the Fujitsu transceiver chips MB582 and MB853. A byte of data is transferred once every eight 155 MHz clock cycles, and converted to or from a serial bit stream in the transceiver chips.

The interface contains 4 signals for host use.

SONET & SAR
SONET and SAR functions are performed within the transceiver module. The internal interface to the local ram simply provides payload data for a given channel.

3.6 Miscellaneous

The following functions are also supported by the ITC.

OAM
All OAM cells are stored in a single area in local ram, for transfer to the host. All the ATM cell is stored, except for the HEC byte ie 52 bytes.

Transparent Modes
Two additional modes of operation are also possible, which are not covered by AAL5 framing, on a VC basis. These modes are Cell Transparent and Payload Transparent.

In Cell transparent, 52 bytes (all the ATM cell, except for the HEC byte) are stored in the local ram, for transfer to host memory,

In Payload transparent mode, only the payload is stored.

Initialisation
All descriptors, including the free lists, must be initialised by the host, before operations can begin. This is defined in the Functional Operations section.

Statistics
Various statistics are maintained by the ITC, to enable the host to monitor the system. These are detailed in the Functional Operations section.

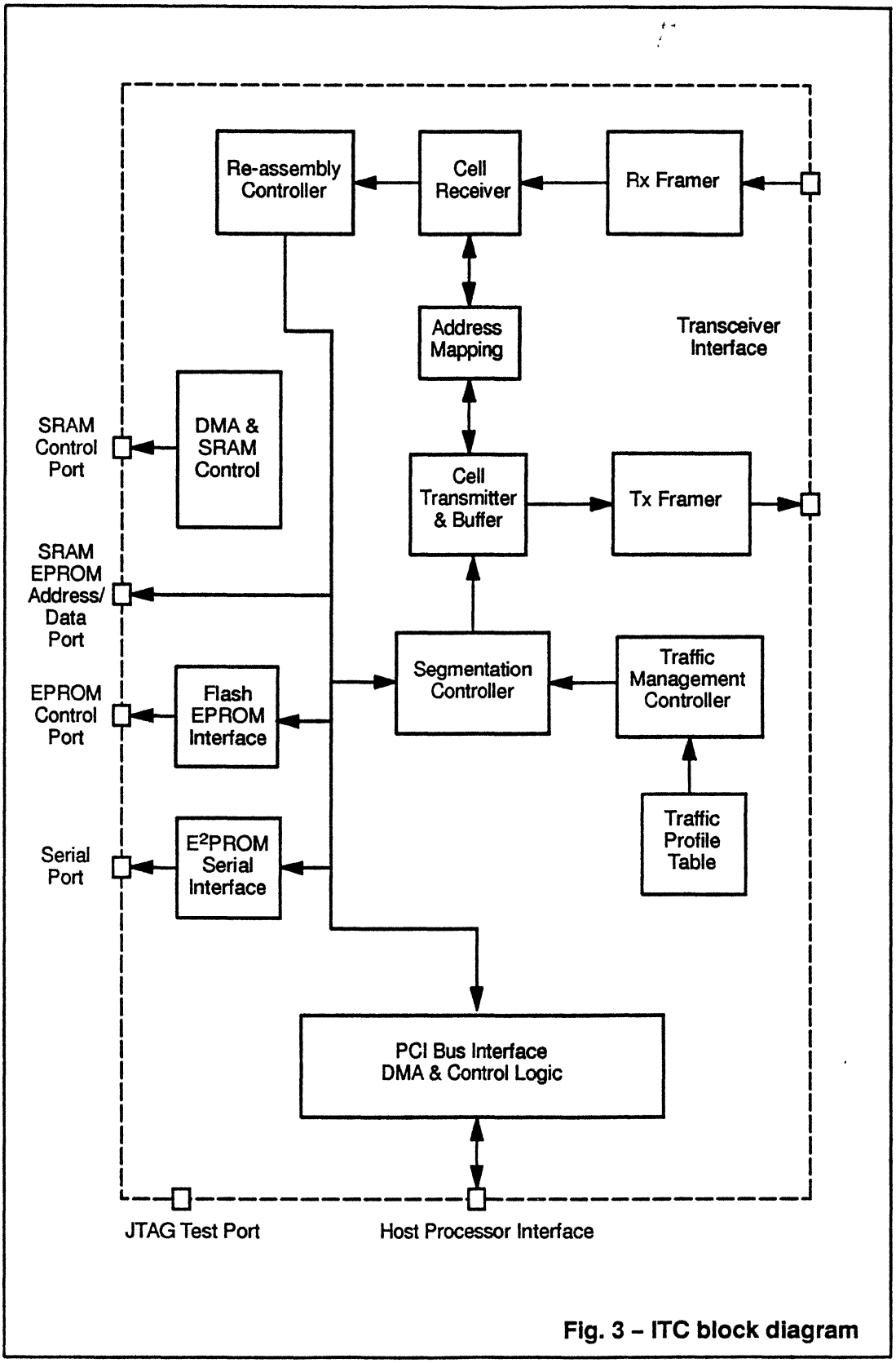
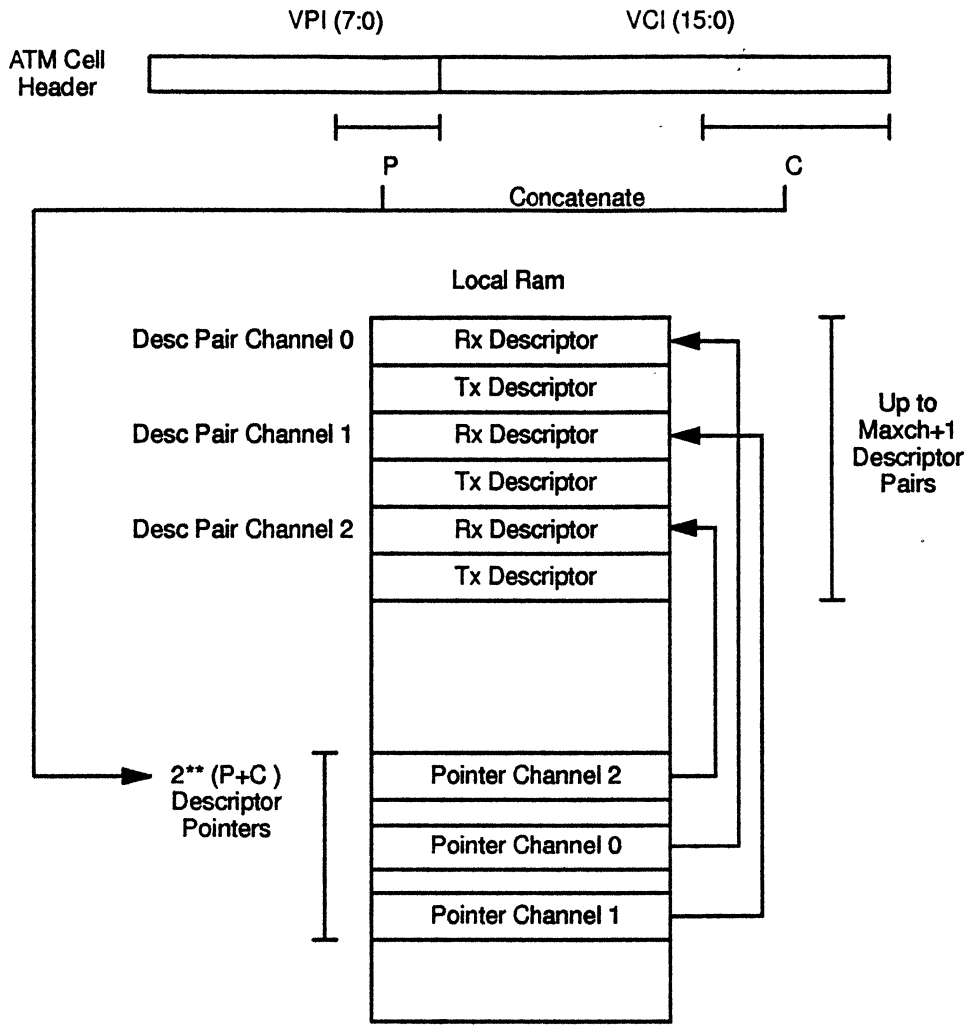


Fig. 3 – ITC block diagram

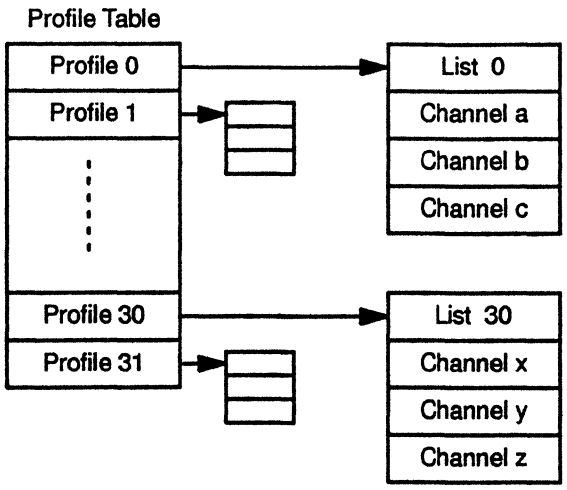


CPC Size	Total bits P + C	Pointers
0	7	128
1	8	256
2	9	512
3	10	1024
4	11	2048
5	12	4096
6	13	8192

VPI Size	P bits
0	1
1	2
2	3
3	4

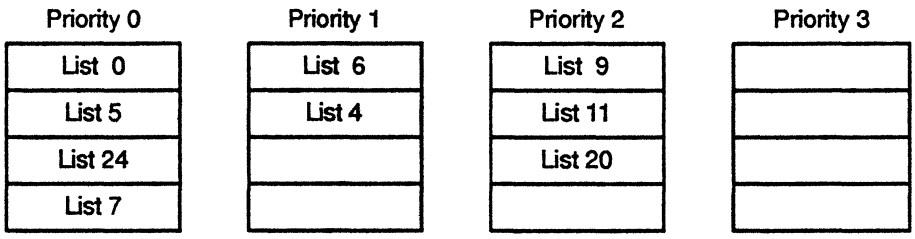
Address Translation field select codes

Fig. 4 – Address Map Channel Selection



Profile Channel Assignments

Fig. 5 – Profile Channel Assignments



Transmit Priority Queues

All channels in all lists in a high priority queue are serviced before lower priority queues. Processing of a low priority queue will be suspended (at the channel level, within a list) if a higher priority queue becomes valid.

Fig. 6 – Priority Queues

4. FUNCTIONAL OPERATIONS

4.1 Receive Operations

Receive operations are independent and asynchronous to transmit operations, and take priority over transmit operations.

The transceiver interface module decodes the physical layer framing functions, and the AAL5 adaption layer protocols. It supplies cell payload data in 48 byte blocks (in the order in which they were received on the transceiver interface) for storage in the local ram. The re-assembled data is stored on a logical channel basis, allowing it to be accessed independently of the transceiver interface reception ordering.

Two sets of descriptors are used to manipulate the storage and forwarding of the data to host memory, one set to control local ram accesses, and the second set to control system bus operations.

Local Ram Organisation
The local ram contains all descriptors necessary for data reception by the ITC, and space for the data payloads, as shown symbolically in Fig. 7.

Blocks of local ram are available for use by the ITC for payload data, organised as a linked list of 64 bytes each, called the receive free list, as shown in Fig. 8. These blocks can be allocated to any channel as required, on a dynamic basis, when receive data is stored in local ram. Individual channel data will then itself be stored as a linked list of blocks.

Each logical channel can store as many cells or frames of data as local ram capacity allows. Blocks are returned to the free list when data is transferred to host memory.

Local Ram Rx Descriptors
The descriptors used for linked list local ram operations are as shown in Fig. 9. The fields in the descriptor have the following functionality :-

- CRC
  This is the CRC for the AAL5 frame
- Write Frame Start
  This is the start of the frame currently being written into the local ram
- Write Last Cell
  This is the last cell in the frame currently being written into the local ram
- Read First Cell
  This is the first cell in the frame currently being read out of the local ram, for transfer to host memory
- Read Frame End
  This is the end of the frame currently being read out of the local ram, for transfer to host memory
- Write Cell Count
  A count of the number of blocks in the frame currently being written to local ram
- Write Byte Count
  A count of the number of bytes in the frame currently being written to local ram
- Read Cell Count
  A count of the number of blocks in the frame currently being read from local ram

- Read Byte Count
  A count of the number of bytes in the frame currently being read from local ram

- Status 1 (see Fig. 10).
  27 Threshold [0]
  28 Threshold [1]
  29 Rx priority [0]
  30 Rx priority [1]

- Status 2
  0 Same frame
  1 1st cell
  2 Frame complete
  3 CRC error
  4 Length formula error
  5 Abort, length zero
  6 Purge frame
  7 Purge channel
  8 Channel empty
  9 EFCI state
  10 On payload queue
  11 Cells lost, local ram full
  12 Payload Transparent
  13 Cell Transparent
  14 Length register error
  15 CLP1 cell received

Local Ram Receive Queues
A threshold level can be specified, on a channel basis, such that when the amount of data held in local ram exceeds the specified amount, it is scheduled for transfer to host memory. The ITC appends the channel number to one of four Receive Queues, specified by the priority bits. The receive queues exists in local ram, as shown in Fig. 11.

The queues are automatically serviced in priority order by the ITC, which accesses local ram and host bus descriptors as required.

Host Receive Descriptors Free Pool
The host must maintain a pool of linked descriptors in system memory, pointing to free host memory blocks, which the ITC can access as required. Fig. 12 illustrates the situation before and after data transfers to host memory, for two channels, requiring three memory areas.

When the ITC requires additional host memory in order to transfer data, it assigns the leading descriptor from the free area pool to the relevant channel. The ITC automatically updates the free pool control registers as required.

After the data has been transferred, the address of the first or only descriptor pointing to the frame data in system memory is written to the Host Memory Receive Queue, using pointers maintained by the ITC.

If a frame will fit in a single block of system memory, only a single descriptor is returned to the host.

If a frame will not fit in a single block of system memory, the ITC will generate the links between the fragmented block descriptors, to enable the host to find the data.

Host Memory Receive Queue
The host must maintain a Receive Queue list in system memory, to enable the ITC to inform the host that it has transferred receive data to main memory, as shown in Fig. 12.

The ITC places information in this list for the host to read, giving the address of the descriptor(s) pointing to the frame data in memory.

Information can be placed in this list when either an entire frame has been transferred to system memory, or when each fragmented block has been transferred, on an individual channel basis, using the block update bit in the channel host receive descriptor.

Host Receive Queue Control
The queue consists of a 4 kilobyte circular buffer, and is controlled by two ITC registers. The HMRQS register points to the start of the queue, and the HMRQC counter gives the number of entries in the queue.

The HMRQS register is under host control ie the host must write back the new address of the start of the queue, after items have been removed from the queue by the host.

The HMRQC counter is incremented by the ITC when entries are added to the queue, and adjusted by the ITC when the HMRQS register is altered by the host.

The queue must be located in host memory on a 4 KB boundary, using the HMRQB register.

Host Receive Queue Interrupt
When entries are first placed in the receive queue, a Status interrupt is generated for the host. The host must empty the queue before additional interrupts will be generated, which requires the host to check for additional entries (by reading the HMRQC), after reading the number of entries originally indicated by the HMRQC.

Host Receive Queue Signal
An ITC signal (RxQ) exists, which is activated when entries exist in the host memory receive queue. This signal can be monitored directly by the host, at the system level, as an alternative to the interrupt mechanism.

Host Memory Rx Descriptors
The descriptors used for linked list host bus operations are as shown in Fig. 13. The fields in a descriptor have the following functionality :-

- Channel Number
  This is the physical channel number to which a virtual channel is assigned
- Data Pointer
  A pointer to the data block controlled by this descriptor
- Next Descriptor Pointer
  A pointer to the next descriptor in the linked list
- Block Size
  The size of the data block in bytes

- Byte Count
  The number of data bytes in the data block
- AAL5 Length
  The length field contained in the AAL5 frame
- AAL5 Control
  The control field contained in the AAL5 frame
- Status
  0 Reserved (DNP)
  1 Host queue block update
  2 Block transferred correctly
  3 Reserved
  4 Reserved
  5 Reserved
  6 Reserved
  7 Reserved
  8 Reserved
  9 Frame end
  10 CRC error
  11 Abort, AAL5 length zero
  12 Length formula error
  13 Length register error
  14 Cells lost, local ram full
  15 CLP1 cells received

4.2 Transmit Operations

Host Transmit Descriptors Free Pool
The host must maintain a pool of linked descriptors in system memory, pointing to free host memory blocks, which can then be used by the host as required. Fig. 15 illustrates the situation before and after the ITC has transmitted data assembled by the host, for two channels, requiring three memory areas.

The ITC will return used descriptors to the end of the free pool, when data blocks have been transmitted, and update the free pool control registers as required.

Host Transmit Data Generation
The host must generate a list of linked descriptors in system memory, on a per channel basis, for all data to be transmitted to the ITC, as shown in Fig. 15.

Data can start on any byte boundary within a block. A data block can consist of partial or complete frames. Multiple blocks or frames can be linked, provided all data is for the same channel.

The host must also update the Host Memory Transmit Queue, to inform the ITC that transmit data is pending.

Host Memory Transmit Queue
The host must maintain a Transmit Queue list in system memory, to inform the ITC that transmit data is available. The host must write the start and finish addresses of the descriptor chain into the queue, as shown in Fig. 15, and increment an address register in the ITC, which points to the last entry in the queue. The ITC will automatically service the queue, when it contains entries.

Host Transmit Queue Control
The queue consists of a 4 kilobyte circular buffer, and is controlled by two ITC registers. The HMTQS register points to the start of the queue, and the HMTQF register points to the end of the queue.

The HMTQF register must be incremented by the host, when it writes items to the queue.

The HMTQS register is incremented by the ITC when entries are removed from the queue.

The queue must be located in host memory on a 4 KB boundary, using the HMTQB register.

Host Transmit Queue Signal
An ITC signal (TxQ) exists, which is activated if the host memory transmit queue starts to become full. This signal can be monitored directly by the host, at the system level, to check that space exists on the queue, rather than calculating the size of the queue from the values in the control registers.

Host Memory Tx Descriptors
The descriptors used for linked list host bus operations are as shown in Fig. 14. The fields in a descriptor have the following functionality :-

- Channel Number
  This is the physical channel number to which a Virtual Channel is assigned
- Data Pointer
  A pointer to the data block controlled by this descriptor
- Next Descriptor Pointer
  A pointer to the next descriptor in the linked list
- Byte Count
  The number of data bytes in the data block
- AAL5 Control
  The control field contained in an AAL5 frame
- Status
  0 Frame end
  1 More descriptors in chain
  2 Reserved (CE)
  3 Reserved
  4 Reserved
  5 Reserved
  6 Reserved
  7 Reserved
  8 Reserved (DNP)
  9 Reserved
  10 Reserved
  11 Reserved
  12 Reserved
  13 Reserved
  14 Payload Transparent
  15 Cell Transparent

Cell Buffers
Data transferred to the ITC using host descriptors is held in temporary cell buffers, until processed for transmission on the transceiver interface, using local ram transmit descriptors.

Local Ram Tx Descriptors
The descriptors used to format cells for transmission have the following fields, as shown in Fig. 17 :-

- CRC
  This is the CRC for the AAL5 frame

- ATM Cell Header
  Contains VPI, VCI addresses

- Status
  0 RM cell received
  1 EFCI = 0 sent
  2 Reserved (1st)
  3 Reserved (re-start)
  4 Channel empty
  5 Delete
  6 Off list
  7 Send RM
  8 Reserved
  9 Reserved
  10 Reserved
  11 Reserved
  12 Reserved
  13 Reserved
  14 Reserved
  15 Reserved

The remaining fields are relevant to traffic management functions, and will be described in that section.

4.3 Data Transfers

Data Alignment
The ITC utilises a Little Endian address mechanism. Receive data transferred to system memory from the ITC can initially be aligned on any byte boundary. Transmit data to be transferred from system memory to the ITC can also be initially aligned at any byte boundary in memory.

Data Deletion
The ITC can delete partially or wholly received frames stored in local ram, even if parts of the frame have already been sent to host memory. The ITC can also delete all receive data in a given channel. These operations are carried out by the ITC in response to specific host purge commands, on a channel basis.

4.4 Traffic Management

The ITC can only approximate the Forum requirements for ABR traffic, and does not implement precisely the currently proposed scheme (ATM Forum / 94-0438R2).

The ITC can autonomously process ABR related traffic management functions eg congestion and RM cell generation. Alternatively, the automatic ITC mechanism can be disabled, requiring these operations to be handled by the host.

Traffic Profiles
The traffic management module contains 32 profiles. A profile can be configured to control CBR, VBR or ABR traffic.

ABR profiles must form a contiguous block, within the profile tables, to enable the ABR traffic requirements to be met.

The organisation of the Profile Tables, Channel Lists, and list placements within the Local Ram are shown in Fig. 18.

Parameters for all types of profiles are as shown in Fig. 19, and have been defined in chapter 3.

Profile Channel Assignments
Each profile has a list of channels assigned to it by the host. A list can contain up to Maxch+1-4 entries.

Channels assigned by the host to CBR/VBR profiles will always remain attached to that profile.

Channels assigned by the host to ABR profiles can be moved by the ITC to different profiles. This allows the ITC to implement a strategy which is a close approximation of the ATM Forum requirements for ABR traffic.

Channel Movement
A channel is moved to a lower profile after a number of cells have been transmitted at ACR intervals. The number is specified by the ADR Count field in the channel traffic management descriptor.

A channel is moved to a higher profile when an RM cell is received.

RM Cell Generation
All ABR cells must normally be transmitted with the EFCI bit set to 1. One cell in every Nrm cells must be transmitted with the EFCI bit set to 0. The value of Nrm is specified by the Nrm Count field in the channel traffic management descriptor.

The EFCI = 0 cell is an opportunity for the destination end system to generate an RM cell, and hence increase the source ACR.

Profile Peak Rate Sequences
All ABR profiles must be arranged contiguously in the profile tables, as shown in Fig. 18. The peak values for the profiles should form an approximate linear sequence, between the highest and lowest ABR rates required. Profile 31 represents the lowest throughput channels, and must therefore contain the largest peak rate interval counter value.

ACR Decrease
A channel is always moved down by one profile (from profile N to profile N+1) when the ACR must be reduced.

ACR Increase
An RM cell must cause a nett increase in the channel ACR, to a profile with a higher peak rate than was in operation when the previous EFCI=0 cell was transmitted. This is achieved by copying the value of the RM AIR parameter from the profile at which the last EFCI=0 cell was transmitted, as shown in Fig. 16.

A subsequent ACR increase will cause the channel to be assigned to the profile specified by the copied RM AIR parameter.

Data Unavailability
If data is unavailable for transmission while a channel's ACR is above it's ICR, the channel will be moved down the profiles towards its ICR profile, using the normal rate reduction mechanism.

If data is unavailable for transmission while the channel's ACR is at or below its ICR profile, it will be deleted from the profile lists. The channel will then be assigned to it's ICR profile, if new data becomes available.

Traffic Management Descriptors
The descriptors used for traffic management control are shown in Fig. 17. The fields in the descriptor have the following meaning :-

- Initial Profile
  The profile to which a channel is initially assigned, and to which a channel will drop, when no data is available for transmission
- Minimum Profile
  The lowest profile to which a channel can drop, due to ACR decreases

- Maximum Profile
  The highest profile to which a channel can rise, due to ACR increases
- RM AIR Copy
  A copy of the RM AIR profile parameter
- ADR Count
  A count of the number of cells to be transmitted, before the ACR is decreased
- Nrm Count
  A count of the number of cells to be transmitted, before allowing an opportunity for an ACR increase.

CBR / VBR Profiles
These consist of the parameters shown in Fig. 19, and as described in chapter 3.

ABR Profiles
These consist of the parameters shown in Fig. 19, and as described in chapter 3.

There are also two counter decrement factors, held in the profile lists, associated with ABR profiles, as shown in Fig. 18. These values are used to decrement the ADR and Nrm counters specified in the traffic management descriptors.

Decrementing the ADR and Nrm counters by values other than one allows greater flexibility in traffic management strategies.

4.5 Reserved Channels

The reserved channel descriptors are used for OAM cells, RM cells and to control a dump channel.

4.5.1 OAM

OAM cells are processed in Cell Transparent mode. The ITC also optionally checks/generates the CRC10 field.

Receive
All OAM F5 cells are transferred to host memory using the Receive Descriptor for physical channel zero, which must be reserved for this purpose.

Transmit
F5 cells must be assembled by the host, and transmitted on descriptor channel 0.

F4 Cells
OAM F4 cells can be combined with the F5 cells on channel 0, or they can be transferred on separate F4 channels, using the normal pointer / descriptor mechanism. The initialisation of the pointers in the address translation module determines which mechanism is used.

4.5.2 RM Cells

RM cells can be processed automatically by the ITC, or else by the host. It is recommended that the ITC is allowed to process these cells, as the host mechanism cannot be tightly controlled.

ITC Processed
On receiving an RM cell, the ITC will set a status bit in the corresponding local ram transmit descriptor, to cause the channel to be moved to a new profile. The RM cell can also be scheduled for transmission to the host, for information purposes, if this mechanism is enabled, otherwise the cell is discarded.

Host Processed
Resource Management cells are processed in Cell Transparent mode. They are transferred to and from host memory on physical channel one, which must be reserved for this purpose.

To move a channel to a new profile, the host must write the number of the channel to the channel move register in the ITC.

Priority
When entries are first placed in the RM channel, the ITC will schedule the information for transmission to the host. When the channel has been emptied, the ITC will append the channel number to the host memory receive queue.

To transmit an RM cell, the host must attach it to the host memory transmit queue, as normal.

4.5.3 Dump Channel

All cells received by the ITC which cannot be correctly processed on other channels are sent to the dump channel. Dump channel cells are transferred to host memory using the Receive Descriptor for physical channel two, which must be reserved for this purpose.

Cells in this channel will include those for which bits outside the CPC range in the cell header are set, cells within the CPC range but for which descriptors do not exist, and cells containing PTI fields equal to 7.

Dump channel data can be transferred to host memory in one of two formats, under mode register control :-

a) In cell transparent format

b) In cell header format, which consists of the 4 byte cell header only, excluding the HEC byte

4.6 Congestion Queue

A receive congestion queue exists in the local ram, which operates similarly to the local ram receive queue for payload data.

Information in the queue can be read by the host, one entry at a time. The queue format is shown in Fig. 20.

Entries are placed in the queue under two conditions :-

a) The state of the congestion bit changes, on CBR/VBR channels (priority 0, 1 or 2)

b) The EFCI bit is zero, on an ABR channel (priority 3)

Congestion on ABR channels can be handled automatically by the ITC, or else by the host. The congested ABR channel numbers can also be scheduled for transmission to the host, for information purposes, if this mechanism is enabled.

ITC Processed
On detecting the EFCI bit set to zero on an ABR channel, the ITC will set a status bit in the corresponding local ram transmit descriptor. This will cause the ITC to automatically schedule an RM cell on the transmit channel.

Host Processed
The host must generate an RM cell in cell transparent format, and send it to the ITC on physical channel one. It will be scheduled for transmission by the traffic manager, at the ACR of the profile to which channel one is assigned.

Congestion Queue Control
The queue consists of a 4 kilobyte circular buffer, and is controlled by the ITC.

The queue must be located in local ram on a 4 KB boundary, using the LRCQB register.

Congestion Queue Processing
Entries in the congestion queue must be processed by the host. They must be read by the host one entry at a time.

4.7 Framer Operations

Alignment
Framer alignment is achieved by searching for the alignment bytes which signify the start of a frame. When these bytes have been detected at the start of two consecutive frames, alignment is assumed.

After frame alignment has been detected, the data is de-scrambled using the polynomial $1 + x^6 + x^7$.

An unframed mode of operation is also possible, whereby the framers are disabled, on a per link basis. The cells must be byte aligned in this mode.

Cell Receiver
The cell receiver provides an interface between the receive framer and the re-assembly controller. A list of the functions provided by the cell receiver is given below :-

1 Cell alignment based on HEC status.
2 Cell header error detection and correction, and cell discard.
3 Cell payload de-scrambling using polynomial $1 + x^{43}$
4 VC address translation
5 Discard of physical layer cells.

AAL5 Operations
These can be disabled for the Transparent modes of operation, on a per VC basis.

4.8 Statistics

Statistics for network management purposes are supported on 3 levels. These are the Physical layer, ATM layer and AAL5 layer, as follows :-

Physical Layer
This records information to support the MIB defined in Bellcore RFC 1595, which refers to both SONET (ANSI TI.105) and SDH (ITU-T G.783) standards.

ATM Layer
The following three counts (T, R, D) are required by the ATM Forum UNI 3.1 ILMI MIB :-

- The number of assigned ATM-layer cells transmitted (T)
- The number of assigned ATM-layer cells received and not dropped (R)
- The number of cells received and dropped (D), for any of the following reasons :-

a) Uncorrectable cell header errors

b) ATM-layer invalid cells ie physical layer cells

c) ATM-layer cells with headers which the ITC cannot support

The following information is also maintained :-

- An Out of Cell Delineation event (OCD) has occurred
- The number of cells received with header errors detected (HED)
- The number of cells received with header errors corrected (HEC)
- A count of the total number of cells lost, due to lack of local ram space, will also be maintained.
- A count of the total number of cells containing CRC10 errors.

AAL5 Layer
The following conditions are detected on a per PDU basis. They can be read by the host on a per PDU basis, to maintain statistics on a per VCC basis.

- CRC error
- Length error
  The byte count does not match the length field contained in the PDU trailer
- Maximum length error
  The number of cells exceeds a user programmable value
- Abort
  The length field in the PDU trailer was set to zero
- CLP1
  PDU contains cells which had the CLP bit set to 1
- Cells Lost
  PDU has lost at least one cell, due to lack of space in the local ram

4.8.1 Implementation

Statistics support is implemented by recording counts of events for the PHY and ATM levels, and setting status bits in PDU descriptors for the AAL5 level.

The counters are incremented when an event occurs, and reset to zero when read by the host. Each counter stops when it reaches a count of all ones.

A timer can be started when any counter is incremented from zero. All counters can be individually enabled to start the timer. When the timer interval expires, a maskable host interrupt can be generated.

The strategy is illustrated as shown in Fig. 21.

4.9 Loopback

Various loopback paths can be individually enabled within the ITC, as shown in Fig. 22.

LR1
This is a loopback path between the receive path data input pins from the transceiver, and the transmit path data output pins to the transceiver.

LR2
This is a loopback path between the point at which receive path frame processing has been completed, and transmit path frame processing is about to start.

The functions performed on the receive data up to this loopback point are to be defined. tbd

LT1
This is a loopback path between the transmit path data output pins to the transceiver, and the receive path data input pins from the transceiver.

LT2
This is a loopback path between the point at which transmit path frame processing is about to start, and receive path frame processing has been completed.

4.10 Transmit Test Patterns

The ITC can supply specific data sequences to the transceiver transmit interface, for line test purposes. These consist of a 16 bit data pattern, cyclically repeated.

4.11 Initialisation

All control registers, base registers, pointers, descriptors, traffic profiles and profile lists must be initialised by the host after reset, to configure the ITC for normal operation.

Pointers
Pointers used to access receive physical channel descriptors must be initialised to contain the physical channel number, as shown in Table 2. All unused pointers (ie accessed by unconfigured ATM VCC's) must be initialised to the dump channel.

Descriptor Tables
All descriptor initialisation values are as shown in Table 3 to Table 6.

Queues
Only the receive and congestion queue base registers need initialising by the host. The queue entries do not require initialisation.

Receive Free List
The Rx free list consists of byte aligned 64 byte blocks of local ram. The blocks must be initialised as shown in Table 7.

All unused 64 byte blocks of local ram, aligned on 64 byte boundaries, can be assigned to the free list by the host. This can include spare blocks within other base register buffer areas, or within individual traffic management profile list areas.

Profile Lists
Traffic profile lists must be initialised as shown in Table 8.

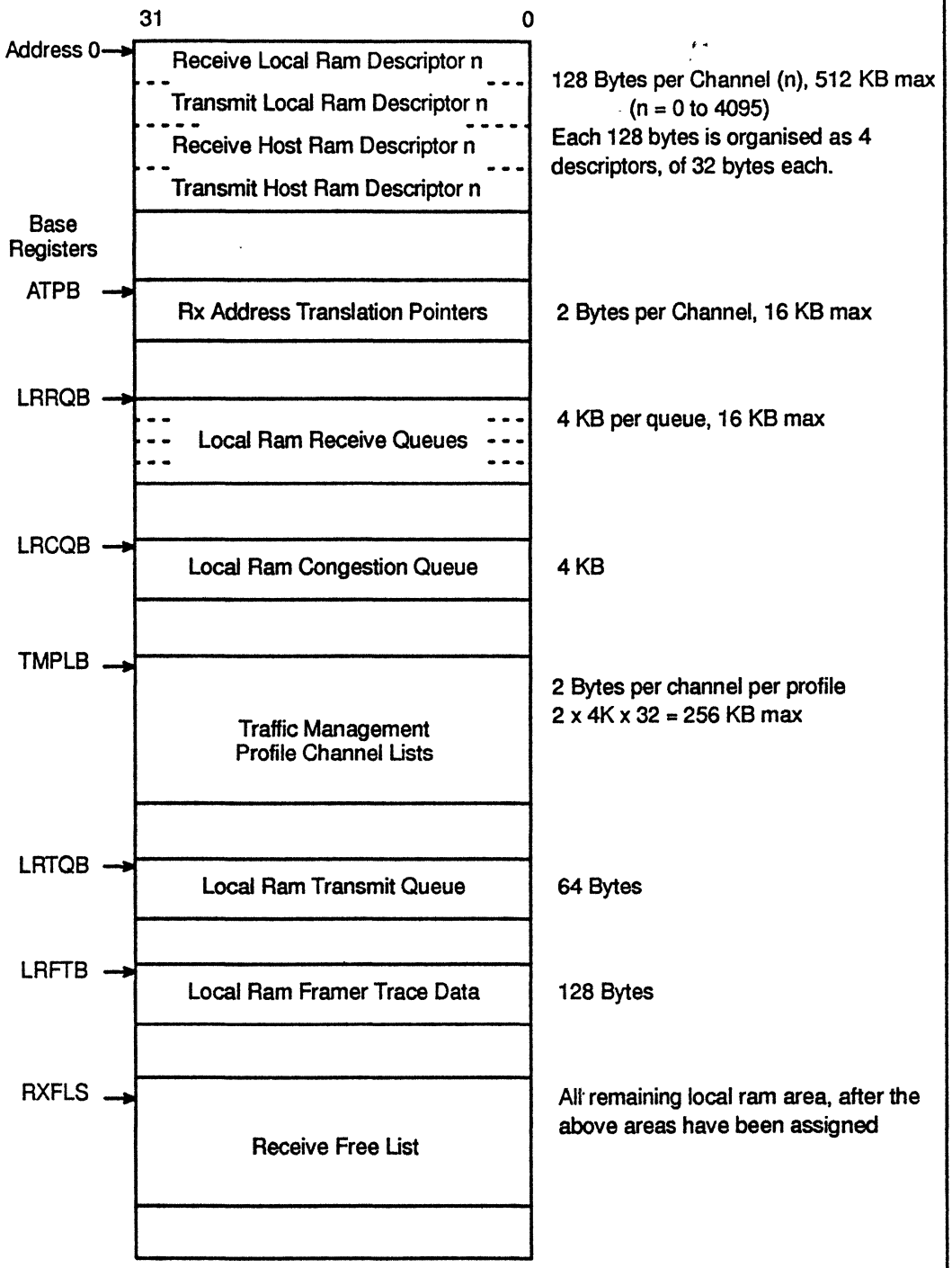


Fig. 7 – Local Ram Symbolic Organisation

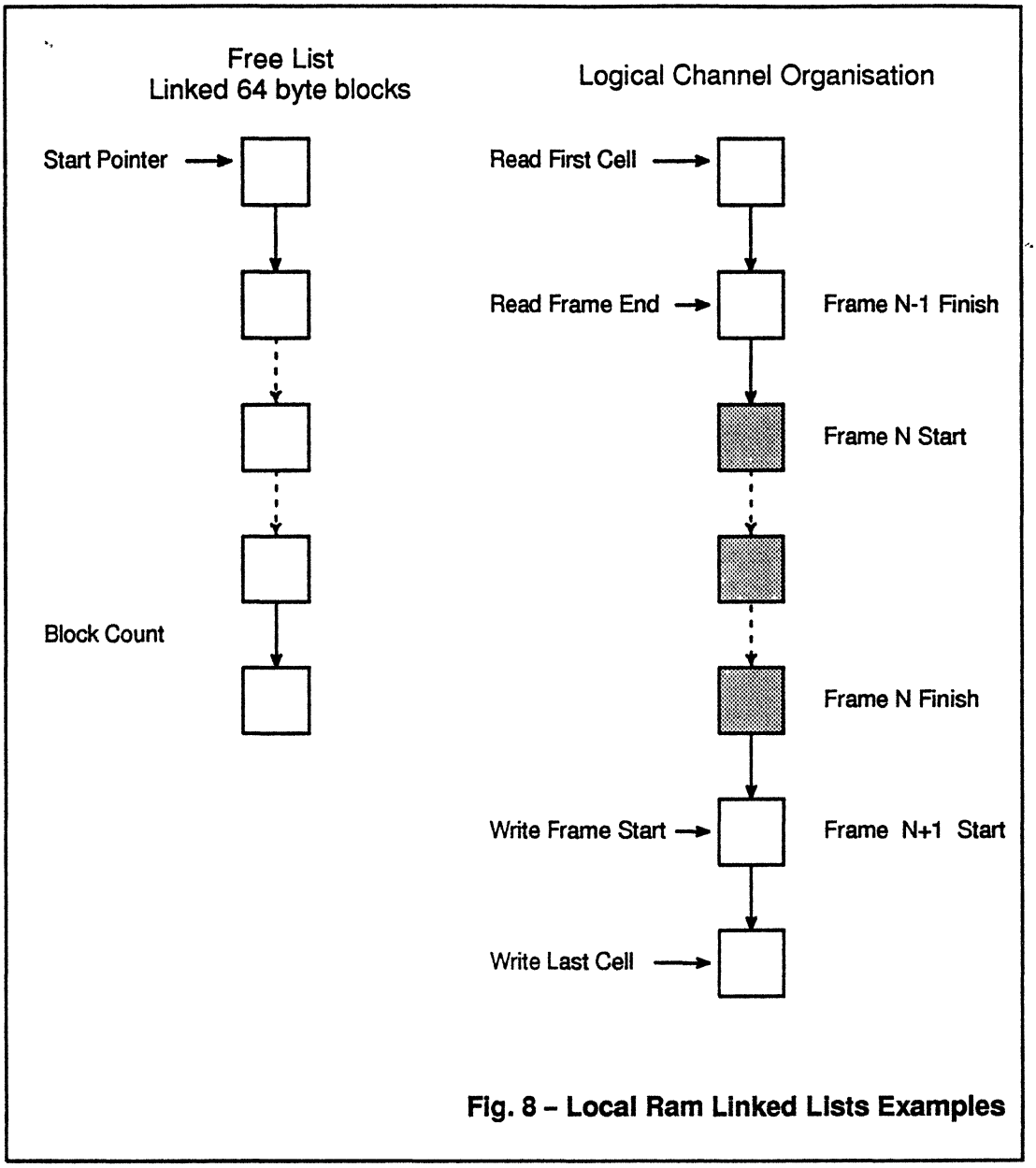


Fig. 8 - Local Ram Linked Lists Examples

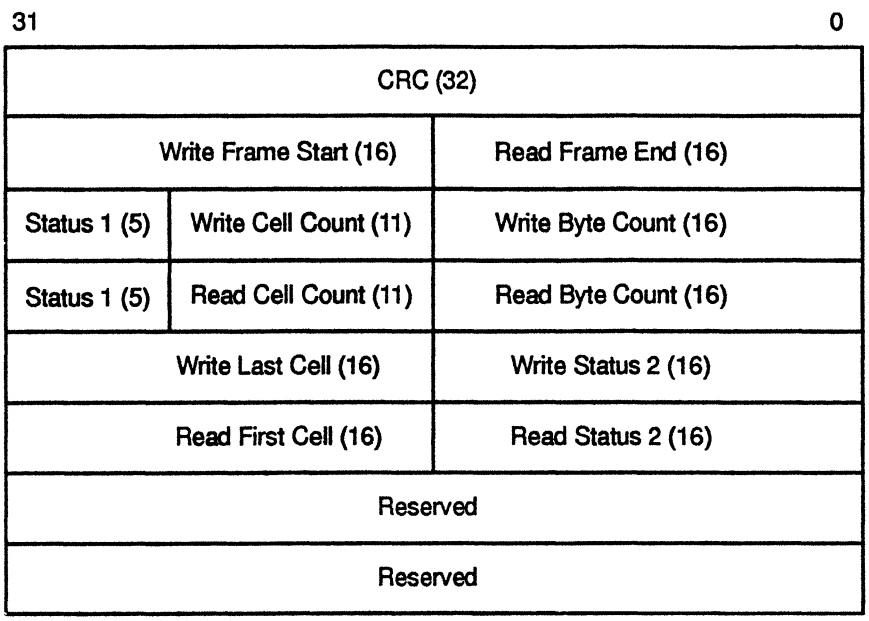


Fig. 9 – Receive Local Ram Descriptor Format

Threshold (1:0)	Number of Cells Stored
0, 0	1 cell
0, 1	1 frame
1, 0	Specified by threshold register 0
1, 1	Specified by threshold register 1

When Frame End is reached, the frame will be transferred to the host regardless of the values in the threshold registers.

Rx Priority (1:0)	Priority Levels
0, 0	High
1, 1	Low

Fig. 10 – Receive Local Ram Descriptor Status 1 Codes

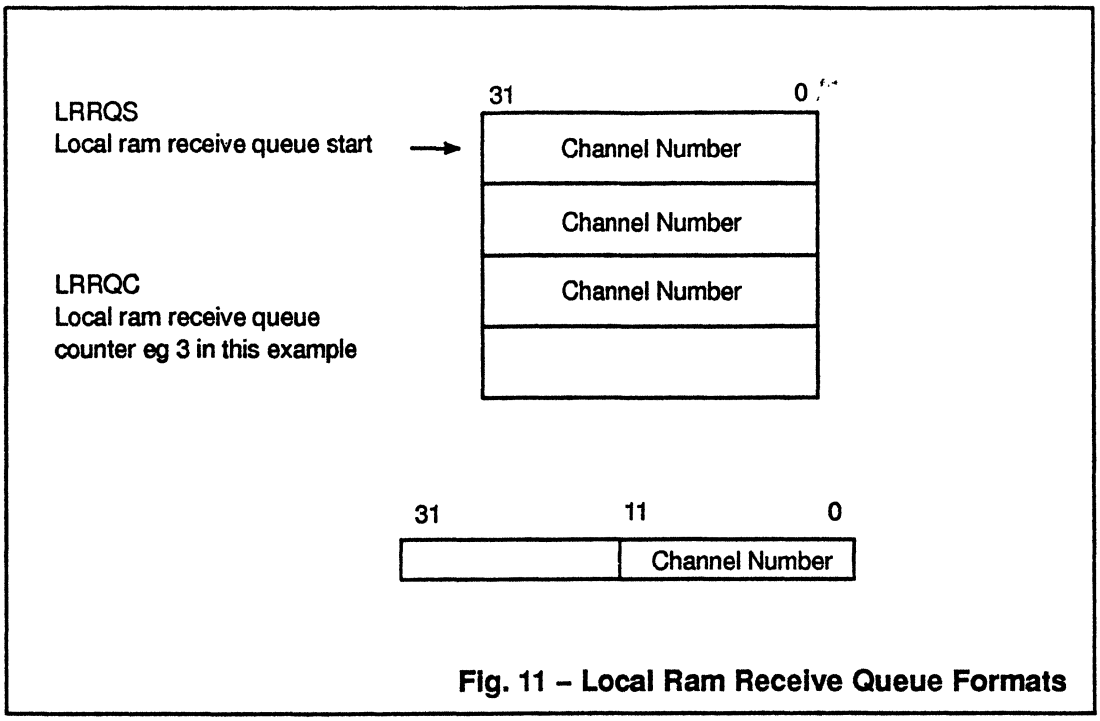


Fig. 11 – Local Ram Receive Queue Formats

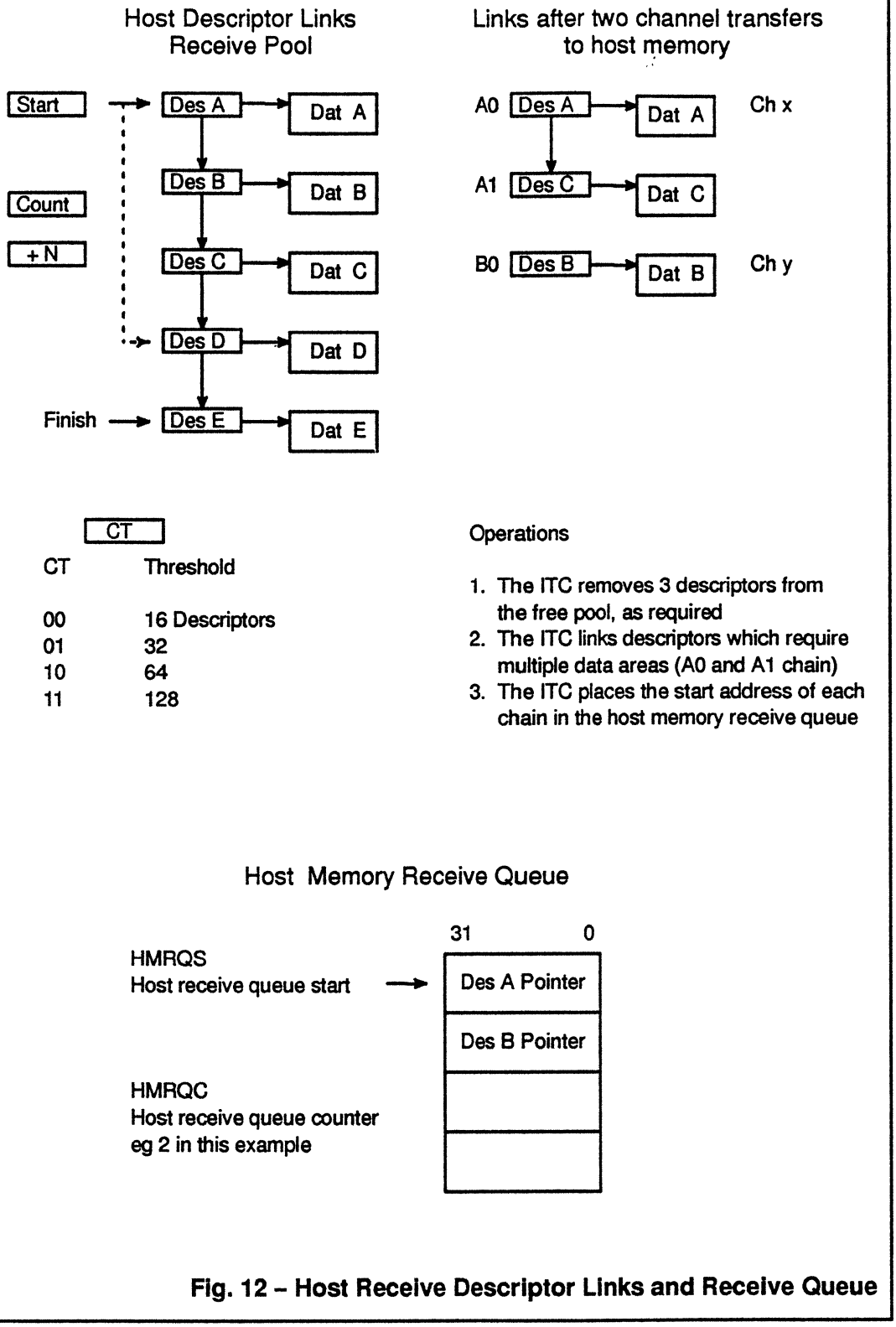


Fig. 12 – Host Receive Descriptor Links and Receive Queue

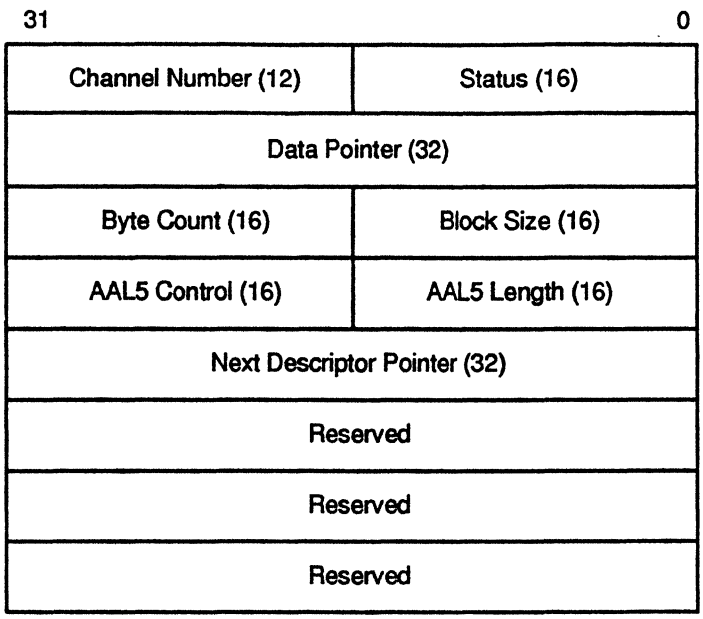


Fig. 13 – Receive Host Descriptor Format

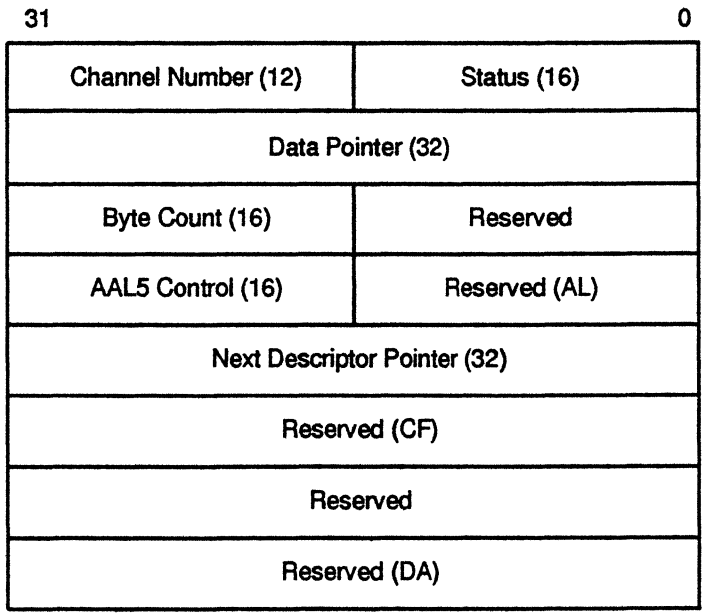
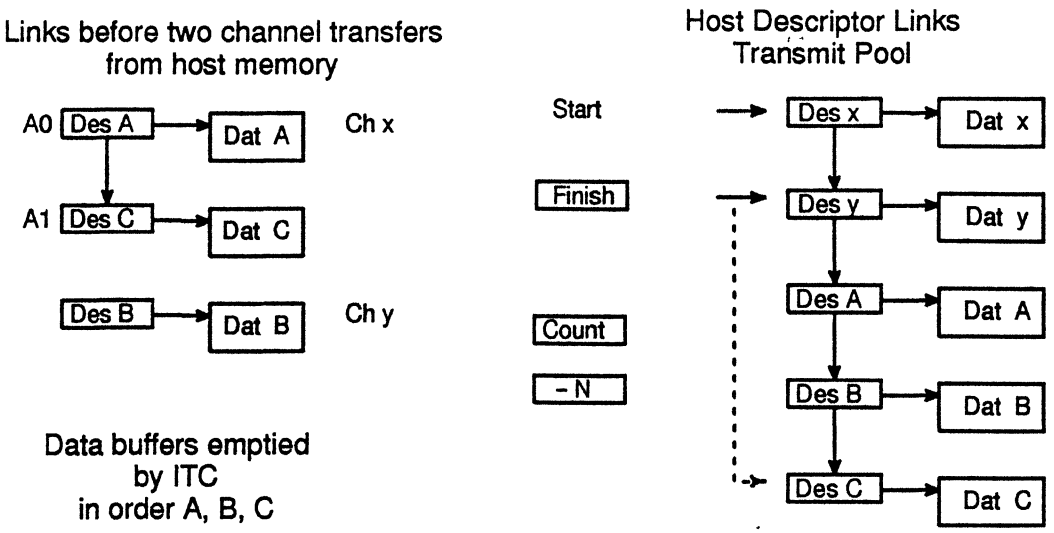


Fig. 14 – Transmit Host Descriptor Format



Operations

1. The host links descriptors which require multiple data areas (A0 and A1 chain)
3. The host places the start and finish address of each chain in the host memory transmit queue
4. The ITC will append used descriptors to the free list, as data blocks are transmitted

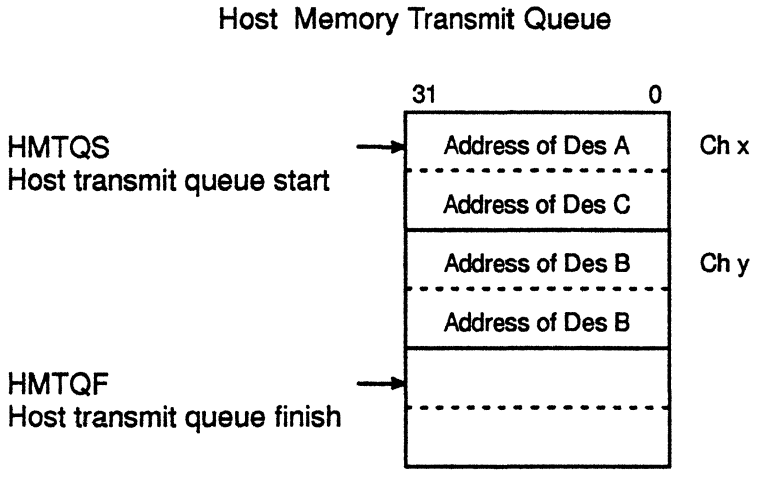


Fig. 15 – Host Transmit Descriptor Links and Transmit queue

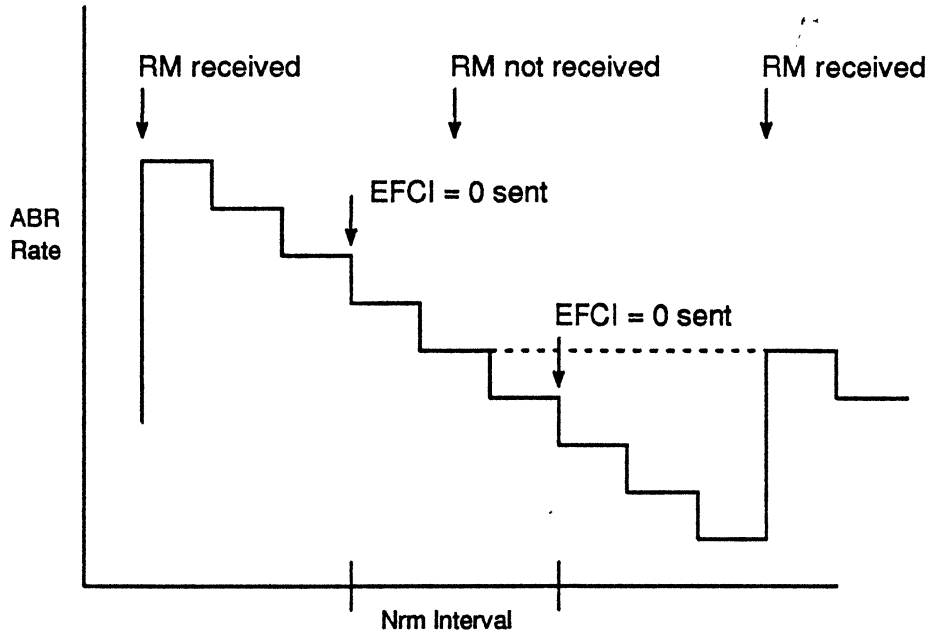
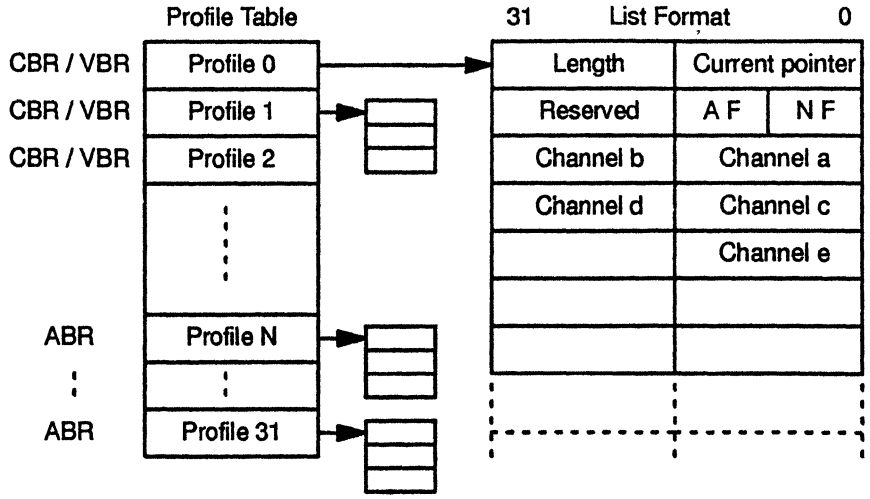


Fig. 16 – ABR RM Strategy

31 0

CRC (32)			
ATM Cell Header			
Maximum Profile	Reserved	Reserved	Nrm Count
Minimum Profile	Reserved	Reserved	ADR Count
		Reserved	Reserved
RM AIR Copy	Initial Profile	Status	
Reserved			
Reserved			

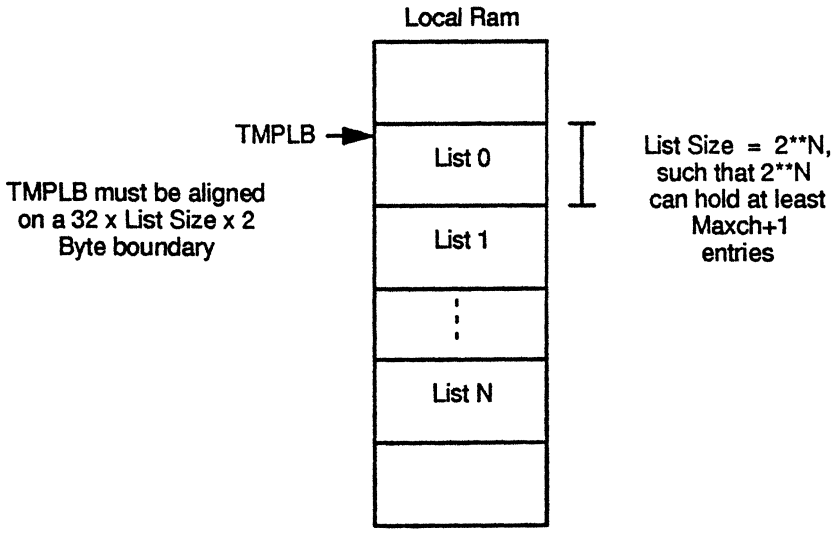
Fig. 17 – Transmit Local Ram Descriptor Format



Profile Table and List Organisation

A F, ADR Factor.
This is the amount by which the ADR Count is decremented

N F, Nrm Factor
This is the amount by which the Nrm Count is decremented

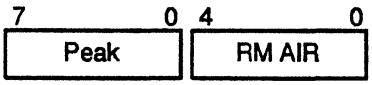


TM Local Ram Organisation

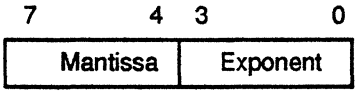
Fig. 18 – Profile Tables and Lists Organisation

CBR / VBR Profile Parameters

ABR Profile Parameters



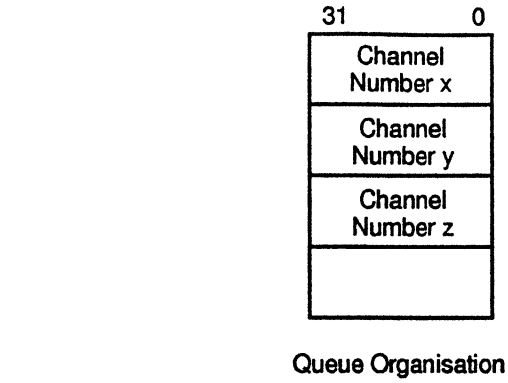
Peak Rate Counter



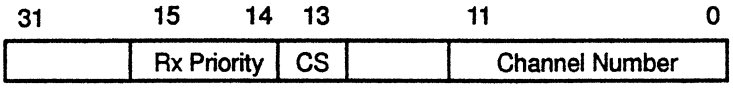
Exponent	Time Interval	Exponent	Time Interval
1	2 µs	A	1 ms
2	4	B	2
3	8	C	4
4	16	D	8
5	32	E	16
6	64	F	32
7	128		
8	256		
9	512		

Exponent = 0 is an inactive profile

Fig. 19 – Profile Parameters



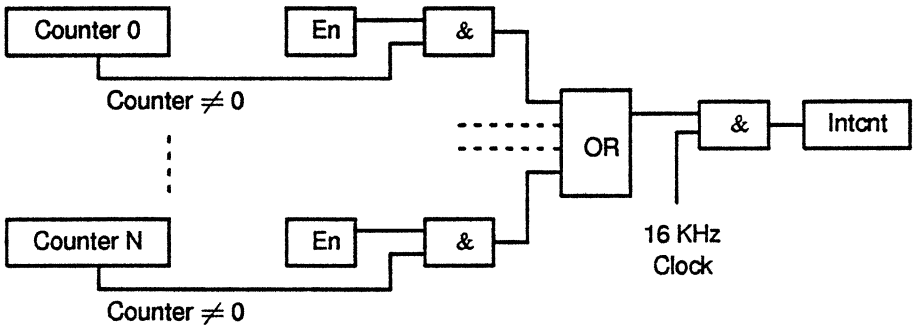
Queue Organisation



CS = Congestion state

Queue Data Format

Fig. 20 – Local Ram / Host Memory Congestion Queue Formats



When an individual counter is enabled, it will allow the interrupt counter to generate an interrupt, after the programmed interval.

Fig. 21 – Statistics

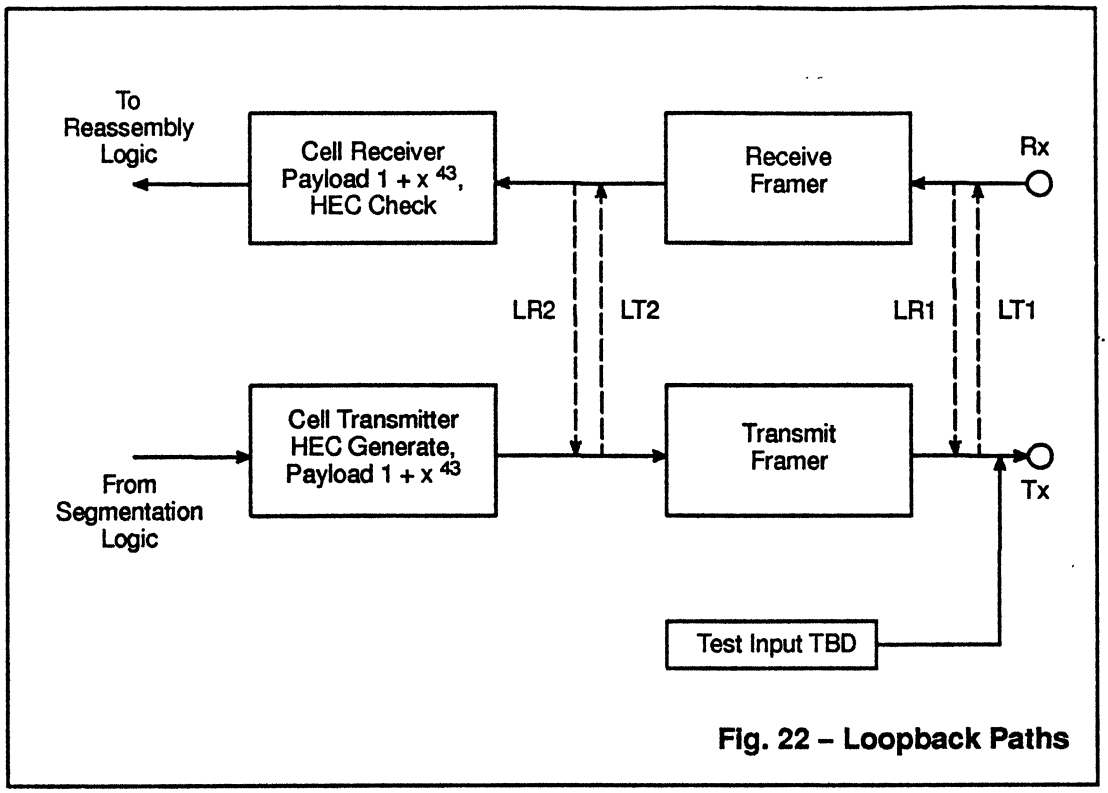


Fig. 22 – Loopback Paths

Pointers	Initialisation [31:0]	Pointer Function
Used	[31:30] = 0, [29] = PT, [28] = CT, [27:16] = Phy, [15:14] = 0, [13] = PT, [12] = CT, [11:0] = Phy	Phy = Physical channel number CT = Cell transparent channel PT = Payload transparent channel
Unused	[31:28] = 0001, [27:16] = Dump, [15:12] = 0001, [11:0] = Dump	Dump = Dump channel number

Table 2 – Address translation pointer initialisation

Bytes	Initialisation [31:0]	Descriptor Function
3:0	F F F F F F F F	CRC [31:0]
7:4	0	
11:8	0PPT T000 0 0 0 0 0 0	Status, Write counts PP = Priority [1:0] TT = Threshold [1:0]
15:12	0PPT T000 0 0 0 0 0 0	Status, Read counts PP = Priority [1:0] TT = Threshold [1:0]
19:16	0 0 0 0 00CP 1 0 2	Write status C = Cell transparent P = Payload transparent
23:20	0 0 0 0 00CP 1 0 2	Read status C = Cell transparent P = Payload transparent
27:24	0	Reserved
31:28	X	

Table 3 – Rx local ram descriptor initialisation

Bytes	Initialisation [31:0]	Descriptor Function
3:0	F F F F F F F F	CRC [31:0]
7:4	Host	ATM header
11:8	Host	Maximum profile, Nrm count
15:12	Host	Minimum profile, ADR count
19:16	X	
23:20	0 0 000I IIII 0 0 0 0	IIIII = Initial profile
27:24	X	
31:28	X	

Table 4 – Tx local ram descriptor initialisation

Bytes	Initialisation [31:0]	Descriptor Function
3:0	X X X X 0 0 0 00B1	Channel number, status B = 1, Inform host as buffers are filled
7:4	X	Data pointer
11:8	X	Byte count, block size
15:12	X	AAL5 count, length
19:16	X	Next descriptor pointer
23:20	X	Reserved
27:24	X	Reserved
31:28	X	Reserved

Table 5 – Rx host ram descriptor initialisation, local ram copy

Bytes	Initialisation [31:0]	Descriptor Function
3:0	H H H H CP00 1 0 00MF	H = Host, Channel number P = Payload transparent C = Cell transparent M = More data in linked list F = Frame end
7:4	X	Data pointer
11:8	X	Byte count, reserved
15:12	X	AAL5 count, reserved
19:16	X	Next descriptor pointer
23:20	X	Reserved
27:24	X	Reserved
31:28	X	Reserved

Table 6 – Tx host ram descriptor initialisation, local ram copy

Bytes	Initialisation [31:0]	Pointer Function
3:0	[31:16] = Next block pointer	Pointer x 2^6 gives local ram byte 0 address of next block in free list
7:4	0	Reserved

Table 7 – Rx free list blocks initialisation

Bytes	Initialisation [31:0]	Descriptor Function
3:0	0 0 0 2 0 0 0 2	Length of list, current pointer
7:4	0 0 0 0 A A N N	A = ADR count decrement amount N = Nrm count decrement amount
End:8	X	Channel numbers

Table 8 – Profile lists initialisation

5. MEMORY MAP OPERATIONS

The host can access the ITC internal registers through a 256 byte memory map. The block of 256 consecutive byte addresses must be aligned on any 256 byte boundary in the ITC memory map space.

Memory Register Maps

ITC registers will be accessible in different maps, each map referring to a different internal module. The first register in all maps is the global control register.

All registers are as shown in chapter 6.

5.1 PCI Access

Registers within the ITC exist in several independent clocking environments. If the ITC is unable to accept a host access, or is unable to assemble the data required by the host in time to conform to the PCI protocol recommendations, it will signal a retry.

When the host next attempts to obtain the required data, it should have been assembled by the ITC (as a result of the previous bus function), and will therefore be transferred normally across the PCI bus.

If the ITC is still unable to accept the host access, the retry mechanism will be repeated.

6. REGISTER MAPS

R 1 Global Control Register
Write / Read – Address 00 (hex)

D31

				C(3)	C(2)	C(1)	C(0)
			P(4)	P(3)	P(2)	P(1)	P(0)

D0

This register appears in all register maps, at address 0.

It is the register which dictates the meaning of the other locations in all register maps.

C[3:0]	Register Map Selected
0000	Reserved
0001	Local Ram
0010	Flash Prom
0011	Traffic Manager (Profile specified by **P[4:0]**)
0100	Transceiver
0101	Host Interface

R 2 Rx Free Pool Start Address (RFPSA)
Write / Read – Address 14 (hex)

D31

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Address of the first descriptor in the Rx free pool

NB D[1:0] must be set to 00

R 3 Rx Free Pool Count (RFPC)
Read Only – Address 18 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

The number of descriptors in the Rx free pool

R 4 Rx Free Pool Count Update (RFPCU)
Write Only – Address 1C (hex)

D15

D	D	D	D	D	D	D	D

D0

The number of descriptors to be added to the free pool count

R 5 Host Memory Receive Queue Base (HMRQB)
Write / Read – Address 0C (hex)

D31

				D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Defines the start (1k Dword boundary) of the host memory receive queue

R 6 Host Memory Receive Queue Start (HMRQS)
Write / Read – Address 04 (hex)

D15

						D	D
D	D	D	D	D	D	D	D

D0

Address of the first entry (in Dwords) in the host memory receive queue

R 7 Host Memory Receive Queue Finish (HMRQF)
Write / Read – Address 08 (hex)

D15

						D	D
D	D	D	D	D	D	D	D

D0

Address of the last entry (in Dwords) in the host memory receive queue

R 8 Host Memory Receive Queue Count (HMRQC)
Read Only – Address 10 (hex)

D15

						D	D
D	D	D	D	D	D	D	D

D0

Number of items in the host memory receive queue

R 9 Tx Free Pool Finish Address (TFPFA) Write / Read – Address 30 (hex)

D31

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Address of the last descriptor in the Tx free pool

NB D[1:0] must be set to 00

R 10 Tx Free Pool Count (TFPC) Write / Read – Address 34 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

The number of descriptors in the Tx free pool

R 11 Tx Free Pool Count Update (TFPCU) Write Only – Address 2C (hex)

D15

D	D	D	D	D	D	D	D

D0

The number of descriptors to be subtracted from the Tx free pool count

R 12 Host Memory Transmit Queue Base (HMTQB)
Write / Read – Address 28 (hex)

D31

				D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Defines the start (1k Dword boundary) of the host memory transmit queue

R 13 Host Memory Transmit Queue Start (HMTQS)
Write / Read – Address 20 (hex)

D15

						D	D
D	D	D	D	D	D	D	D

D0

Address of the first entry (in Dwords) in the host memory transmit queue

R 14 Host Memory Transmit Queue Finish (HMTQF)
Write / Read – Address 24 (hex)

D15

						D	D
D	D	D	D	D	D	D	D

D0

Address of the next free location (in Dwords) in the host memory transmit queue

R 15 E^2PROM Control Register
Write / Read – Address 38 (hex)

D15

			SIZE	ECS	ECLK	EDI	EDO

D0

EDO Serial data to be written to the E^2PROM

EDI Serial data read from the E^2PROM

ECLK Clock for E^2PROM (PCI Clock / 64)

ECS Chip Select for E^2PROM

SIZE 0 :- 1k
1 :- 4k

At reset the ITC will automatically generate the E^2PROM accesses necessary to initialise locations 0h & 8h in the PCI configuration space. The SIZE bit will be set to allow the host to determine the E^2PROM size.

The three control locations (ECS, ECLK and EDO) are under direct control of the host. EDI is a read only location and is a sampled copy of the EDO pin on the E^2PROM.

R 16 Enable Modules Register
Write / Read – Address 3C (hex)

D15

		TR-R	0	PCI	TM	TR-O	LR

D0

LR Enable the local ram module

TR-O Enable the transceiver interface control logic

TM Enable the traffic manager module

PCI Enable the PCI interface control logic

TR-R Enable the transceiver interface registers to be programmed

At reset, each bit is set to 0. To enable the bits, they must be set to 1 by the host.

R 17 ITC Status Register
Read Only – Address 40 (hex)

D31

				HCM	IBE	Reserved	LSP
UTIL	FM	PM	Timer	GHR	GC0	RxDT	RxFLZ
RxFLT	DUMP	OAM	RM	CQF	CQA	CQC/V	HMRQ
Rx3F	Rx3D	Rx2F	Rx2D	Rx1F	Rx1D	Rx0F	Rx0D

D0

0	**Rx0D**	Data exists in local ram receive queue 0
1	**Rx0F**	Local ram receive queue 0 is full
2	**Rx1D**	Data exists in local ram receive queue 1
3	**Rx1F**	Local ram receive queue 1 is full
4	**Rx2D**	Data exists in local ram receive queue 2
5	**Rx2F**	Local ram receive queue 2 is full
6	**Rx3D**	Data exists in local ram receive queue 3
7	**Rx3F**	Local ram receive queue 3 is full
8	**HMRQ**	Host memory receive queue contains entries
9	**CQC/V**	Congestion queue data exists, for CBR/VBR channels
10	**CQA**	Congestion queue data exists, for ABR channels
11	**CQF**	Congestion queue is full
12	**RM**	Data exists in RM channel, or RM cells have been received
13	**OAM**	Data exists in OAM channel
14	**DUMP**	Data exists in dump channel
15	**RxFLT**	Local ram receive free list is below threshold
16	**RxFLZ**	Local ram receive free list is zero
17	**RxDT**	Host receive descriptors are less than threshold
18	**GC0**	GFC credit count is zero
19	**GHR**	GFC halt command received
20	**Timer**	Timer interrupt
21	**PM**	Performance monitoring statistics table updated
22	**FM**	Fault management status update
23	**UTIL**	Change of state on UTIL pins
24	**LSP**	Change of state on LSP pin
25	**Reserved**	
26	**IBE**	Internal bus error (timeout) has occurred
27	**HCM**	Host initiated channel move completed

R 18 Interrupt Enable Register
Write / Read – Address 44 (hex)

D31

				HCM	IBE	Reserved	LSP
UTIL	FM	PM	Timer	GHR	GC0	RxDT	RxFLZ
RxFLT	DUMP	OAM	RM	CQF	CQA	CQC/V	HMRQ
Rx3F	Rx3D	Rx2F	Rx2D	Rx1F	Rx1D	Rx0F	Rx0D

D0

Bits in this register, when set, enable the corresponding bits in the status register, when set, to generate an interrupt.

R 19 Channel Move Register
Write / Read – Address 48 (hex)

D15

				D	D	D	D
D	D	D	D	D	D	D	D

D0

A channel number written to this register causes the channel to be moved from it's current profile to the profile specified by the RMAIR field in the current profile, provided that the Nrm counter has reached zero at least once.

R 20 Control Variables Register
Write / Read – Address 4C (hex)

D15

							LB
LB	LB	CT	CT	LRCKS	CS	CS	CS

D0

CS[2:0] Control Signals [M,L]

000	Logic 0, Logic 0
001	Logic 0, A[21]
010	A[21], A[20]
011	A[20], A[19]
100	A[19], A[18]
101	A[18], A[17]
110	A[17], A[16]
111	A[16], A[15]

The CS bits select pairs of local ram address signals, which are used to control the chip select lines.

[M,L]	CS0	CS1	CS2	CS3
0,0	0	1	1	1
0,1	1	0	1	1
1,0	1	1	0	1
1,1	1	1	1	0

LRCKS 1, use PCI CLK
0, use LRCLK

CT[5,4] Rx free pool descriptor threshold

0,0	16 descriptors
0,1	32
1,0	64
1,1	128

LB[8:6] Transceiver loopback controls

000	Normal operation
001	LR1 path
010	LT1
011	LR2
100	LT2

R 21 Local Ram Address
Write / Read – Address 04 (hex)

D31

		D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Address of local ram location to be accessed

R 22 Local Ram Data
Write / Read – Address 08 (hex)

D31

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Data for local ram access

R 23 Virtual to Physical Translation Table Base (ATPB)
Write / Read – Address 1C (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

D[11:0] Virtual channel to physical channel translation table base address pointer

This register is scaled by the ITC, depending on the size of the translation table, to form the local ram base address as shown :-

ATPB[11:0] x 2**(CPC+6)

D[15:12] Most significant 4 bits of the local ram free list start address (see R 28)

R 24 Local Ram Receive Queues Base (LRRQB) Write / Read – Address 20 (hex)

D15

		D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Base address for the 4 local ram receive queues. This register is scaled by a factor of 4, and the priority number of each queue is concatenated to form the individual queue base addresses :-

LRRQB[13:0] : PRI[1:0]

R 25 Local Ram Transmit Queue Base (LRTQB) Write / Read – Address 24 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Local ram transmit queue base address

R 26 Traffic Management Profile Lists Base (TMPLB) Write / Read – Address 28 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Base address of the traffic management profile lists. The base address of each list is found by concatenating the list number, and scaling by the size of each list :-

TMPLB[15:0] : List Number [4:0] : LS,

where 2**LS can hold at least MAXCH+1 entries

R 27 Framer Trace Base
Write / Read – Address 2C (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Local ram base address for the framer trace bytes area.

R 28 Receive Free List Start (RXFLS)
Write / Read – Address 30 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Local ram address of the start of the receive free list. The entire address is formed as follows :-

R 23 [15:12] : RXFLS [15:0], all shifted left by 4 places ie multiplied by 16

R 29 Receive Free List Count
Write / Read – Address 34 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Count of the number of 64 byte blocks in the receive free list

R 30 Rx Thresholds
Write / Read – Address 3C (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

These registers specify the number of cells which must accumulate in local ram (per channel) before they are scheduled for transmission to host memory

D[15:8] Register 1
D[7:0] Register 0

R 31 Tx Control
Write / Read – Address 38 (hex)

D15

		D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

D[11:0] Maxch, the maximum number of channels supported by the ITC

D[12] Auto purge, ie allow the ITC to purge unwanted AAL5 frames from the local ram, without informing the host

D[13] EFCI polarity :- 0, Search for EFCI = 0
1, Search for EFCI = 1

R 32 RM Channel / Auto Increment
Write / Read – Address 40 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	0	D	D	D

D0

D[15:4] RM Channel Number

D[2:0] Add 2**D[2:0] to the previous local ram address, after the address operation

R 33 Congestion Queue Base
Write / Read – Address 44 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

D[13:0] Local ram congestion queue base address

D[14] 1, Inhibit seting the RM cell received bit in the local ram transmit descriptor, on receipt of an RM cell

D[15] 1, Inhibit local ram storage of RM cells

R 34 Maximum Rx Frame Length
Write / Read – Address 48 (hex)

D15

				D	D	D	D
D	D	D	D	D	D	D	D

D0

D[10:0] The maximum length of a receive frame, before a length error is generated

D[11] Inhibit storage of ABR channels in congestion queue

R 35 Congestion Queue Data
Read Only – Address 4C (hex)

D15

D	D	D		D	D	D	D
D	D	D	D	D	D	D	D

D0

D[11:0] Channel number

D[13] Congestion state

D[15:14] Receive priority

R 36 Rx Free List Threshold
Write / Read – Address 50 (hex)

D15

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

The minimum number of 64 byte cell buffers which must exist in the free list, before the ITC informs the host that the free list is becoming empty.

R 37 PROM Address
Write / Read – Address 04 (hex)

D31

		D	D	D	D	D	D
D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D

D0

Prom Address

R 38 PROM Data
Write / Read – Address 08 (hex)

D15

D	D	D	D	D	D	D	D

D0

Prom Data

R 39 Profile Peak Register
Write / Read – Address 10 (hex)

D15

D	D	D	D	D	D	D	D

D0

D[7:4] Mantissa

D[3:0] Exponent

R 40 Profile Sustainable Register
Write / Read – Address 18 (hex)

D15

			D	D	D	D	D

D0

Sustainable Register

R 41 Profile Bucket Register
Write / Read – Address 20 (hex)

D15

D	D	D	D	D	D	D	D

D0

Bucket Register

R 42 Profile CLP0 Register
Write / Read – Address 28 (hex)

D15

	D	D	D	D	D	D	D

D0

CLP0 Register

R 43 Profile Priority Register
Write / Read – Address 30 (hex)

D15

						D	D

D0

Priority Register

R 44 Profile RM AIR Register
Write / Read – Address 38 (hex)

D15

			D	D	D	D	D

D0

RM AIR Register

R 45 16 KHz Reference Register
Write / Read – Address 04 (hex)

D15

				16KD11	16KD10	16KD9	16KD8
16KD7	16KD6	16KD5	16KD4	16KD3	16KD2	16KD1	16KD0

D0

16KD[11:0] : Programmed to divide the TCLK to give a 16 KHz reference.
[16KD = f_{TCLK} (in MHz) x 62.5]

e.g. for f_{TCLK} = 19.44 MHz, 16KD = $1215_{10} = 4BF_{16}$

This reference is used both for the integration of SONET fault management and for interrupt timing.

R 46 Interrupt Timer Control Register
Write / Read – Address 08 (hex)

D15

FR	RT	PM	FM	ITD11	ITD10	ITD9	ITD8
ITD7	ITD6	ITD5	ITD4	ITD3	ITD2	ITD1	ITD0

D0

ITD[11:0] : Interrupt Timer Divisor 0–4095
Divides the 16 KHz reference to give interrupts timed in ms.
[ITD = Interrupt Timeout in ms * 16]
e.g. for interrupt timeout = 100 ms, ITD = $1600_{10} = 640_{16}$

FM : Fault Management state change starts the timer, which runs until it expires and causes an interrupt
0 : Disabled
1 : Enabled

PM : Performance Monitoring event starts the timer, which runs until it expires and causes an interrupt
0 : Disabled
1 : Enabled

RT : Run the timer from the setting of this bit until it expires and causes an interrupt
0 : Disabled
1 : Enabled

FR : Free Run the timer from the setting of the RT bit and, when it expires and causes an interrupt, continue to run the timer so that another interrupt will be caused
0 : Disabled
1 : Enabled

(For a discussion of the interrupt timer, see XXXXXX.)

R 47 Cell Control Register #1
Write / Read – Address 0C (hex)

D15

				D_C10GEN	D_C10CHK	D_UD	D_IG
	CPC2	CPC1	CPC0			P1	P0

D0

P[1:0] : P, number of VPI bits supported
00 : P = 1
01 : P = 2
10 : P = 3
11 : P = 4

CPC[2:0] : C, number of VCI bits supported (derived from CPC – P)
[C must be ≥ 6]
000 : C = (7 – P)
001 : C = (8 – P)
010 : C = (9 – P)
011 : C = (10 – P)
100 : C = (11 – P)
101 : C = (12 – P)
110 : C = (13 – P)
111 : invalid

D_IG : Disable Idle cell Generation (unassigned cells are generated instead)
0 : Idle cells generated
1 : Unassigned cells generated

D_UD : Disable Unassigned cell Discard (unassigned cells are sent to the dump channel instead)
0 : Unassigned cells discarded
1 : Unassigned cells not discarded

D_C10CHK : Disable CRC10 checking & subsequent cell discarding due to error on receive
[N.B. CRC10 errors will still be counted in the statistics table.]
0 : CRC-10 checking enabled
1 : CRC-10 checking disabled

D_C10GEN : Disable CRC-10 generation & insertion on transmit
0 : CRC-10 generation enabled
1 : CRC-10 generation disabled

R 48 GFC Control Register
Write / Read – Address 10 (hex)

D15

		GHNH	GCRN	GCIV11	GCIV10	GCIV9	GCIV8
GCIV7	GCIV6	GCIV5	GCIV4	GCIV3	GCIV2	GCIV1	GCIV0

D0

GCIV[11:0] : GFC Counter Initial Value 0–4095

GCRN : GFC uses Counter + Reset / Null protocol
0 : Disabled
1 : Enabled

GHNH : GFC uses Halt / No Halt protocol
0 : Disabled
1 : Enabled

R 49 Cell Control Register #2
Write / Read – Address 14 (hex)

D15

						D_SHBEC	D_CPS
ALPHA3	ALPHA2	ALPHA1	ALPHA0	DELTA3	DELTA2	DELTA1	DELTA0

D0

DELTA[3:0] : Delta (+1 consecutive correct HECs to gain cell delineation) 0–15

Recommended value for framed modes : 6

ALPHA[3:0] : Alpha (consecutive incorrect HECs to lose cell delineation) 0–15

Recommended value for framed modes : 7

D_CPS : Disable Cell Payload Scrambling 0 : CPS enabled
1 : CPS disabled

D_SHBEC : Disable Single Header Bit Error Correction 0 : SHBEC enabled
1 : SHBEC disabled

R 50 Framer Control Register
Write / Read – Address 18 (hex)

D15

FTEST		D_RDI-P	D_RDI-L/MS	D_PT	D_FEBE	D_BIP	D_FS
						FORMAT1	FORMAT0

D0

FORMAT[1:0] : Format of framing
00 : unframed
01 : SONET STS-1
10 : SDH STM-1
11 : SONET STS-3c

D_FS : Disable Frame Scrambling
0 : FS enabled
1 : FS disabled

D_BIP : Disable BIP generation
0 : BIP generation enabled
1 : BIP generation disabled

D_FEBE : Disable FEBE insertion
0 : FEBE insertion enabled
1 : FEBE insertion disabled

D_PT : Disable Path Trace
0 : Path Trace handling enabled
1 : Path Trace handling disabled

D_RDI-L/MS : Disable RDI-L/MS insertion
0 : RDI-L/MS insertion enabled
1 : RDI-L/MS insertion disabled

D_RDI-P : Disable RDI-P insertion
0 : RDI-P insertion enabled
1 : RDI-P insertion disabled

FTEST : Framer test mode : user should set to 0
(shortens frame rows from 90 to 6 columns when set to 1)

R 51 Transmit Condition Forcing Control Register #1
Write / Read – Address 1C (hex)

D15

					RDI_X-P	RDI-P	RDI-L/MS
	OCD	SLM	AIS-P	LOP	AIS-L/MS	OOF	LOS

D0

The bits in this register cause various conditions to exist in the transmitted data, which will be detected by the receiving entity. The conditions must exist for certain periods of time to be recognised as alarm conditions. See XXXX for a discussion of the various conditions.

LOS :	Loss Of Signal (forces output data to all 0s)	0 : Disabled 1 : Enabled
OOF :	Out Of Frame (inverts A2 byte(s))	0 : Disabled 1 : Enabled
AIS-L/MS :	Alarm In Signal-L/MS (sets K2[6:8] = 111_2)	0 : Disabled 1 : Enabled
LOP :	Loss Of Pointer (sets {H1,H2} = $0F0F_{16}$)	0 : Disabled 1 : Enabled
AIS-P :	Alarm In Signal-P (sets {H1,H2} = $FFFF_{16}$)	0 : Disabled 1 : Enabled
SLM :	Signal Label Mismatch (sets C2 = EC_{16})	0 : Disabled 1 : Enabled
OCD :	Out of Cell Delineation (forces multiple cell header bit error pattern = 55_{16})	0 : Disabled 1 : Enabled
RDI-L/MS :	Remote Defect Indication-L/MS (sets K2[6:8] = 110_2)	0 : Disabled 1 : Enabled
RDI-P :	Remote Defect Indication-P (sets G1[5] = 1_2)	0 : Disabled 1 : Enabled
RDI_X-P :	Remote Defect Ind. (Extra)-P (sets G1[6] = 1_2)	0 : Disabled 1 : Enabled

R 52 Transmit Condition Forcing Control Register #2
Write / Read – Address 20 (hex)

D15

	CRC10E		SHBE		UE	FECV-P	CV-P
	NP3	NDF	ADV		FECV-L/MS	CV-L/MS	CV-S/RS

D0

The bits in this register cause various conditions to exist in the transmitted data, which will be detected by the receiving entity. The conditions will cause the recording of performance monitoring events at the receiving end. See XXXX for a discussion of the various conditions.

CV-S/RS :	Code Violation-S/RS	0 : Disabled
	(inverts B1)	1 : Enabled
CV-L/MS :	Code Violation-L/MS	0 : Disabled
	(inverts B2)	1 : Enabled
FECV-L/MS :	Far End Code Violation-L/MS	0 : Disabled
	(sets Z2 = X)	1 : Enabled
	[X = 8_{10} if format = STS-1 : X = 24_{10} otherwise]	
ADV :	Advance SPE/VC pointer	0 : Disabled
		1 : Enabled
	[See XXXXXX for a discussion of the use of this bit.]	
NDF :	New Data Flag	0 : Disabled
		1 : Enabled
NP3 :	New Pointer x 3	0 : Disabled
		1 : Enabled
CV-P :	Code Violation-P	0 : Disabled
	(inverts B3)	1 : Enabled
FECV-P :	Far End Code Violation-P	0 : Disabled
	(sets G1[1:4] = X :	1 : Enabled
	X = 8_{10} if format = STS-1	
	X = 24_{10} otherwise)	
UE :	UnEquipped	0 : Disabled
	(sets C2 = 00_{16})	1 : Enabled
SHBE :	Single Header Bit Error	0 : Disabled
		1 : Enabled
	[See XXXXXX for a discussion of the use of this bit.]	
CRC10E :	CRC-10 Error	0 : Disabled
		1 : Enabled

R 53 Transmit Test Pattern Control Register
Write / Read – Address 24 (hex)

D15

TTP15	TTP14	TTP13	TTP12	TTP11	TTP10	TTP9	TTP8
TTP7	TTP6	TTP5	TTP4	TTP3	TTP2	TTP1	TTP0

D0

TTP[15:0] : Transmit Test Pattern

0 : Disabled
Any other value is transmitted in bit order from TTP15 first to TTP0 last and repeats continuously.

R 54 UTIL Pin Register
Write / Read – Address 28 (hex)

D15

UP3IC1	UP3IC0	UP2IC1	UP2IC0	UP1IC1	UP1IC0	UP0IC1	UP0IC0
UP3D	UP2D	UP1D	UP0D	UP3O	UP2O	UP1O	UP0O

D0

UP[3:0]O : UTIL Pin 'x' Output 0–1

UP[3:0]D : UTIL Pin 'x' Drive control
0 : Pin is input
1 : Pin is output

UP[3:0]IC[1:0] : UTIL Pin 'x' Interrupt Control
00 : No interrupt
01 : Interrupt on falling edge
10 : Interrupt on rising edge
11 : Interrupt on both edges

N.B. An interrupt is only generated by a change of signal level on UTILx if the UPxD bit is cleared, i.e. the pin is defined as an input.

N.B. When this register is read, the value in the bottom four bits ([3:0]) will be **UP[3:0]I**, the signal levels sensed on the UTIL[3:0] pins. This will echo the UPxO bit values for those pins declared as outputs.

R 55 LSP Pin Register
Write / Read – Address 2C (hex)

D15

						LSPIC1	LSPIC0
							LSP

D0

LSP : LSP pin state 0–1
(read only : a write to this bit is ignored)

LSPIC[1:0] : LSP Interrupt Control
00 : No interrupt
01 : Interrupt on falling edge
10 : Interrupt on rising edge
11 : Interrupt on both edges

R 56 Fault Management Interrupt Control
Write / Read – Address 34 (hex)

D15

		OCD	OOF		RDI_X-P	RDI-P	RDI-L/MS
	LCD	SLM	AIS-P	LOP	AIS-L/MS	LOF	LOS

D0

The bits in this register, when set, enable a change of state in the corresponding bit in the Fault Management Status Register to generate a Fault Management interrupt. When a bit in this register is cleared, a change of state in the corresponding bit in the Fault Management Status Register will NOT cause an interrupt.

R 57 Performance Management Statistics Interrupt Control Write / Read – Address 38 (hex)

D15

E#15	E#14	E#13	E#12	E#11	E#10	E#09	E#08
E#07	E#06	E#05	E#04	E#03	E#02	E#01	E#00

D0

The bits in this register, when set, enable an update of an entry in the PM Statistics Table registers to generate a Performance Management interrupt. When a particular bit in this register is cleared, an update of the corresponding entry will NOT cause an interrupt.

R 58 Fault Management Status Register
Read – Address 3C (hex)

D15

		OCD	OOF		RDI_X-P	RDI-P	RDI-L/MS
	LCD	SLM	AIS-P	LOP	AIS-L/MS	LOF	LOS

D0

Local defects :

LOS : Loss Of Signal defect

LOF : Loss Of Frame defect [integrated from OOF]
- set when OOF persists for 3.03±0.03 ms
- cleared when OOF is cleared for 3.03±0.03 ms

AIS-L/MS : Alarm In Signal defect – Line / Multiplexer Section level

LOP : Loss Of (SPE/VC) Pointer defect

AIS-P : Alarm In Signal defect – Path level

SLM : Signal Label Mismatch defect

LCD : Loss of Cell Delineation defect [integrated from OCD]
- set when OCD persists for 4.03±0.03 ms
- cleared when OCD is cleared for 4.03±0.03 ms

Remote defects :

RDI-L/MS : Remote Defect Indication defect – Line / Multiplexer Section level

RDI-P : Remote Defect Indication defect – Path level

RDI_X-P : Remote Defect Indication (Extra) defect – Path level

Local status :

OOF : Out Of Frame
- set on detecting 5 consecutive frame alignment word mismatches
- cleared on detecting 2 consecutive frame alignment word matches

OCD : Out of Cell Delineation
- set on detecting α consecutive cell HEC mismatches
- cleared on detecting δ consecutive cell HEC matches

Performance Management Statistics Table
Read – Addresses 40 : 7C, In steps of 4 (hex)

D15

D0

These registers provide read access to the statistics in the table. The bit map of the counts is shown in the table below :

Reg Num	Address	Group	D15	D0
R 59	40	PHY-S/RS	SEF	CV-S
R 60	44	PHY-L/MS	CV-L/MS	
R 61	48	PHY-L/MS	FECV-L/MS	
R 62	4C	PHY-P	NDF	PJE
R 63	50	PHY-P	NP3	NJE
R 64	54	PHY-P	CV-P	
R 65	58	PHY-P	FECV-P	
R 66	5C	PHY-P	UE	
R 67	60	PHY-P	SLM	
R 68	64	ATM-M	T	
R 69	68	ATM-M	R	
R 70	6C	ATM-M	D	
R 71	70	ATM-I	HED	
R 72	74	ATM-I	OCD	HEC
R 73	78	AAL-I	CE	
R 74	7C	AAL-I	Lost	

N.B. When a register is read, the counts accessed through that register are reset to zero. If the count value read is all 1s, the counter has overflowed and the count value is not reliable.

Transceiver Registers