SA14-2054-00
(IBM Order Number)

MPC604E9VEC/D
(Motorola Order Number)

7/96

PowerPC™

Advance Information

PowerPC 604e™ RISC Microprocessor Family: PID9v-604e Hardware Specifications

The PowerPC 604e microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. In this document, the term “604” is used as an abbreviation for the phrase, “PowerPC 604™ microprocessor” and the term “604e” is used as an abbreviation for the phrase, “PowerPC 604e microprocessor.” The PowerPC 604e microprocessors are available from Motorola as MPC604e and from IBM as PPC604e. This document contains pertinent physical characteristics of the 604e.

This document contains the following topics:

Topic	Page
Section 1.1, “Overview”	2
Section 1.2, “Features”	2
Section 1.3, “General Parameters”	5
Section 1.4, “Electrical and Thermal Characteristics”	5
Section 1.5, “PowerPC 604e Microprocessor Pin Assignments”	17
Section 1.6, “PowerPC 604e Microprocessor Pinout Listings”	19
Section 1.7, “PowerPC 604e Microprocessor Package Description”	24
Section 1.8, “System Design Information”	31
Section 1.9, “Ordering Information	36

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1.1 Overview

The 604e is an implementation of the PowerPC family of reduced instruction set computing (RISC) microprocessors. The 604e implements the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision). For 64-bit PowerPC implementations, the PowerPC architecture provides additional 64-bit integer data types, 64-bit addressing, and related features.

The 604e is a superscalar processor capable of issuing four instructions simultaneously. As many as seven instructions can finish execution in parallel. The 604e has seven execution units that can operate in parallel—a floating-point unit (FPU), a branch processing unit (BPU), a condition register unit (CRU), a load/store unit (LSU), and three integer units (IUs)—two single-cycle integer units (SCIUs) and one multiple-cycle integer unit (MCIU).

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allows for rapid execution times, yields high efficiency and throughput. The 604e's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in-order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The 604e has separate memory management units (MMUs) and separate 32-Kbyte on-chip caches for instructions and data. The 604e implements two 128-entry, two-way set associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and the cache use least-recently used (LRU) replacement algorithms.

The 604e has a 64-bit external data bus and a 32-bit address bus. The 604e interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains data cache coherency for multiprocessor applications. The 604e supports single-beat and burst data transfers for memory accesses and memory-mapped I/O accesses.

The 604e uses an advanced, 2.5-V CMOS process technology and is fully compatible with TTL devices.

1.2 Features

This section summarizes features of the 604e's implementation of the PowerPC architecture. Major features of the 604e are as follows:

- High-performance, superscalar microprocessor
  - As many as four instructions can be issued per clock
  - As many as seven instructions can start executing per clock (including three integer instructions)
  - Single-clock-cycle execution for most instructions

- Seven independent execution units and two register files
  - BPU featuring dynamic branch prediction
    - Two-entry reservation station
    - Out-of-order execution through two branches
    - Shares dispatch bus with CRU
    - 64-entry fully-associative branch target address cache (BTAC). In the 604e, the BTAC can be disabled and invalidated.
    - 512-entry branch history table (BHT) with two bits per entry for four levels of prediction—not-taken, strongly not-taken, taken, strongly taken
  - Condition register logical unit
    - Two-entry reservation station
    - Shares dispatch bus with BPU
  - Two single-cycle IUs (SCIUs) and one multiple-cycle IU (MCIU)
    - Instructions that execute in the SCIU take one cycle to execute; most instructions that execute in the MCIU take multiple cycles to execute.
    - Each SCIU has a two-entry reservation station to minimize stalls
    - The MCIU has a single-entry reservation station and provides early exit (three cycles) for 16- x 32-bit and overflow operations.
    - Thirty-two GPRs for integer operands
  - Three-stage floating-point unit (FPU)
    - Fully IEEE 754-1985-compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Fully pipelined, single-pass double-precision design
    - Hardware support for denormalized numbers
    - Two-entry reservation station to minimize stalls
    - Thirty-two 64-bit FPRs for single- or double-precision operands
  - Load/store unit (LSU)
    - Two-entry reservation station to minimize stalls
    - Single-cycle, pipelined cache access
    - Dedicated adder performs effective address (EA) calculations
    - Performs alignment and precision conversion for floating-point data
    - Performs alignment and sign extension for integer data
    - Four-entry finish load queue (FLQ) provides load miss buffering
    - Six-entry store queue
    - Supports both big- and little-endian modes
- Rename buffers
  - Twelve GPR rename buffers
  - Eight FPR rename buffers
  - Eight condition register (CR) rename buffers

- Completion unit
  - The completion unit retires an instruction from the 16-entry reorder buffer when all instructions ahead of it have been completed and the instruction has finished execution.
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes executed, dispatched, and fetched instructions if branch is mispredicted
  - Retires as many as four instructions per clock
- Separate on-chip instruction and data caches (Harvard architecture)
  - 32-Kbyte, four-way set-associative instruction and data caches
  - LRU replacement algorithm
  - 32-byte (eight-word) cache block size
  - Physically indexed/physical tags. (Note that the PowerPC architecture refers to physical address space as real address space.)
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - Instruction cache can provide four instructions per clock; data cache can provide two words per clock
  - Caches can be disabled in software
  - Caches can be locked
  - Parity checking performed on both caches
  - Data cache coherency (MESI) maintained in hardware
  - Secondary data cache support provided
  - Instruction cache coherency maintained in hardware
  - Data cache line-fill buffer forwarding. In the 604 only the critical double word of the cache block was made available to the requesting unit at the time it was burst into the line-fill buffer. Subsequent data was unavailable until the cache block was filled. On the 604e, subsequent data is also made available as it arrives in the line-fill buffer.
- Separate memory management units (MMUs) for instructions and data
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - Both TLBs are 128-entry and two-way set associative
  - TLBs are hardware reloadable (that is, the page table search is performed in hardware)
  - Separate IBATs and DBATs (four each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
  - LRU replacement algorithm
  - 52-bit virtual address; 32-bit physical address
- Bus interface features include the following:
  - Selectable processor-to-bus clock frequency ratios (1:1, 3:2, 2:1, 5:2, 3:1, and 4:1)
  - A 64-bit split-transaction external data bus with burst transfers
  - Support for address pipelining and limited out-of-order bus transactions

  - — Four burst write queues—three for cache copyback operations and one for snoop push operations
  - — Two single-beat write queues
  - — Additional signals and signal redefinition for direct-store operations
  - — Provides a data streaming mode that allows consecutive burst read data transfers to occur without intervening dead cycles. This mode also disables data retry operations.
  - — No-$\overline{\text{DRTRY}}$ mode eliminates the $\overline{\text{DRTRY}}$ signal from the qualified bus grant and allows read operations. This improves performance on read operations for systems that do not use the $\overline{\text{DRTRY}}$ signal. No-$\overline{\text{DRTRY}}$ mode makes read data available to the processor one bus clock cycle sooner than if normal mode is used.
- Multiprocessing support features include the following:
  - — Hardware enforced, four-state cache coherency protocol (MESI) for data cache. Bits are provided in the instruction cache to indicate only whether a cache block is valid or invalid.
  - — Separate port into data cache tags for bus snooping
  - — Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power management
  - — NAP mode supports full shut down and snooping
  - — Operating voltage of 2.5 ± 0.3 V
- Performance monitor can be used to help in debugging system designs and improving software efficiency, especially in multiprocessor systems.
- In-system testability and debugging features through JTAG boundary-scan capability

1.3 General Parameters

The following list provides a summary of the general parameters of the 604e:

Technology	0.35 µm CMOS, five-layer metal
Die size	12.9 mm x 11.7 mm (148 mm^2)
Transistor count	5.1 million
Logic design	Fully-static
Packages	Surface mount 304-pin C4 ceramic quad flat pack (C4-CQFP) or 255-lead ceramic ball grid array (BGA)
Core power supply	2.5 V ± 5% V dc
I/O power supply	3.3 V ± 5% V dc

1.4 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 604e.

1.4.1 DC Electrical Characteristics

The tables in this section describe the 604e DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	–0.3 to 2.75	V
PLL supply voltage	AVdd	–0.3 to 2.75	V
I/O supply voltage	OVdd	–0.3 to 3.6	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OVdd by more than 2.5 V at all times including during power-on reset.
3. **Caution**: OVdd must not exceed Vdd/AVdd by more than 1.2 V at any time including during power-on reset.
4. **Caution**: Vdd/AVdd must not exceed OVdd by more than 0.4 V at any time including during power-on reset.

Table 2 provides the recommended operating conditions for the 604e.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	2.375 to 2.625	V
PLL supply voltage	AVdd	2.375 to 2.625	V
I/O supply voltage	OVdd	3.135 to 3.465	V
Input voltage	V_{in}	GND to 5.5	V
Junction temperature	T_j	0 to 105	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3 provides the thermal characteristics for the 604e.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Rating
C4-CQFP package thermal resistance, junction-to-top of die	θ_{JC}	0.03	°C/W
BGA package thermal resistance, junction-to-top of die	θ_{JC}	0.03	°C/W

Note: Refer to Section 1.8, “System Design Information,” for more details about thermal management.

Table 4 provides the DC electrical characteristics for the 604e.

Table 4. DC Electrical Specifications

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	0.0	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	0.0	0.4	V
Input leakage current, V_{in} = 3.465 V[1]	I_{in}	—	10	µA
V_{in} = 5.5 V[1]	I_{in}	—	245	µA
Hi-Z (off-state) leakage current, V_{in} = 3.465 V[1]	I_{TSI}	—	10	µA
V_{in} = 5.5 V[1]	I_{TSI}	—	245	µA
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 9 mA	V_{OL}	—	0.4	V
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10.0	pF
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15.0	pF

Notes:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

Table 5 provides the power dissipation for the 604e.

Table 5. Power Dissipation

CPU Clock: SYSCLK	Processor Core Frequency			Unit
	150 MHz	166 MHz	180 MHz	
Full-On Mode				
Typical	9.3	10.0	11.0	W
Maximum	12.5	15.0	17.0	W
Nap Mode				
Typical	TBD	TBD	TBD	W
Maximum	TBD	TBD	TBD	W

Notes:

1. These values apply for all valid PLL_CFG[0–3] settings and do not include output driver power (OVdd) or analog supply power (AVdd). OVdd power is system dependent but is typically ≤ 10% of Vdd. Worst-case AVdd = 15 mW.
2. Typical power is an average value measured at Vdd = AVdd = 2.5 V, OVdd = 3.3 V, T_j = 25 °C in a system executing typical applications and benchmark sequences. Typical power numbers should be used in planning for proper thermal management.
3. Maximum power is measured at Vdd = AVdd = 2.625 V, OVdd = 3.465 V, T_j = 0 °C using a worst-case instruction mix. These values should be used for power supply design.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 604e. These specifications are for 150, 166.67, and 180 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. All timings are specified respective to the rising edge of SYSCLK.

1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1. These specifications are for 150, 166.67, and 180 MHz processor core frequencies.

Table 6. Clock AC Timing Specifications

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_j ≤ 105 °C

Num	Characteristic	150 MHz		166.67 MHz		180 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Processor frequency	75	150	83.3	166.7	90	180	MHz	1
	VCO frequency	200	400	200	400	200	400	MHz	1
	SYSCLK frequency	25	66	25	66	25	66	MHz	1, 6
1	SYSCLK cycle time	15	40	15	40	15	40	ns	
2, 3	SYSCLK rise and fall time	1.0	2.0	1.0	2.0	1.0	2.0	ns	2

Table 6. Clock AC Timing Specifications (Continued)

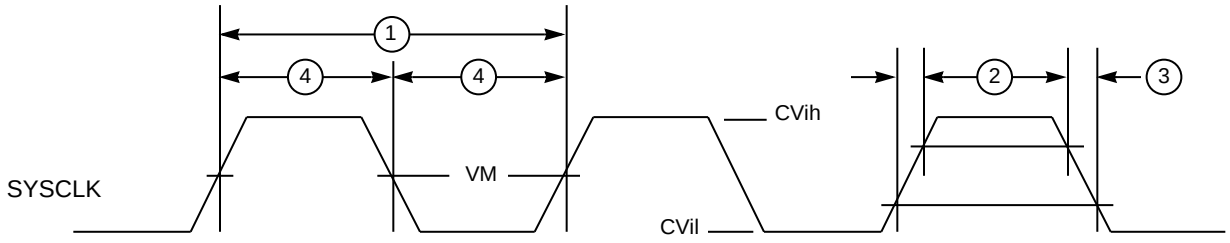
Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	150 MHz		166.67 MHz		180 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	40	60	%	3
	SYSCLK jitter	—	±150	—	±150	—	±150	ps	4
	604e internal PLL relock time	—	100	—	100	—	100	µs	3, 5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8, “System Design Information,” for valid PLL_CFG[0–3] settings, and to Section 1.9, “Ordering Information,” for available frequencies and part numbers.
2. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Cycle-to-cycle jitter, and is guaranteed by design.
5. PLL-relock time is the maximum time required for PLL lock after a stable Vdd, OVdd, AVdd, and SYSCLK are reached during the power-on reset sequence. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 µs) during the power-on reset sequence.
6. AC timing specifications are tested up to the maximum SYSCLK frequency shown here. However, it is theoretically possible to attain higher SYSCLK frequencies, if allowed for by system design or by using 604e Fast Out mode (see Table 13 for details).

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the 604e as defined in Figure 2. These specifications are for 150, 166.67 and 180 MHz processor core frequencies.

Table 7. Input AC Timing Specifications[1]

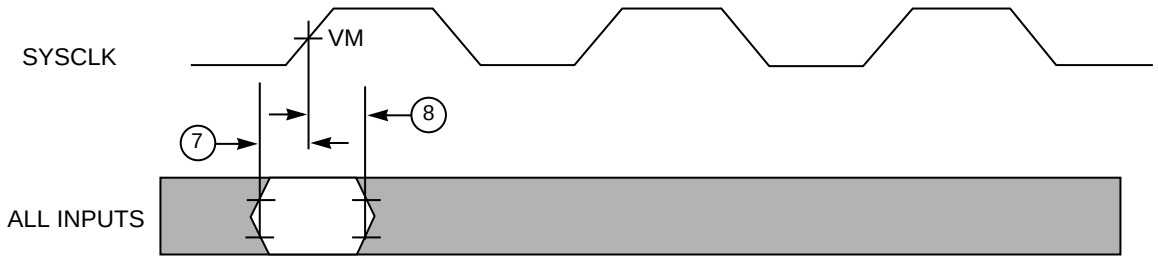
Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	150 MHz		166.67 MHz		180 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
7a	$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$,$\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, and $\overline{\text{DBWO}}$ valid to SYSCLK (input setup)	4.0	—	3.5	—	3.25	—	ns	
7b	All other inputs valid to SYSCLK (input setup)	2.5	—	2.25	—	2.0	—	ns	2
8	SYSCLK to all inputs invalid (input hold)	0	—	0	—	0	—	ns	2
9	Mode select input valid to $\overline{\text{HRESET}}$ (input setup for $\overline{\text{DRTRY}}$)	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	ns	3, 4, 5, 6
10	$\overline{\text{HRESET}}$ to mode select input invalid (input hold for $\overline{\text{DRTRY}}$)	0	—	0	—	0	—	ns	3, 4, 5, 6

Notes:

1. Input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 2).
2. All other input signals include the following signals—all inputs except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{DBWO}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TEA}}$, and JTAG inputs.
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
4. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
5. These values are guaranteed by design, and are not tested.
6. Note this is for configuration of the fast-L2 mode and the no-$\overline{\text{DRTRY}}$ mode.

Figure 2 provides the input timing diagram for the 604e.



VM = Midpoint Voltage (1.4 V)

Figure 2. Input Timing Diagram

Figure 3 provides the mode select input timing diagram for the 604e.

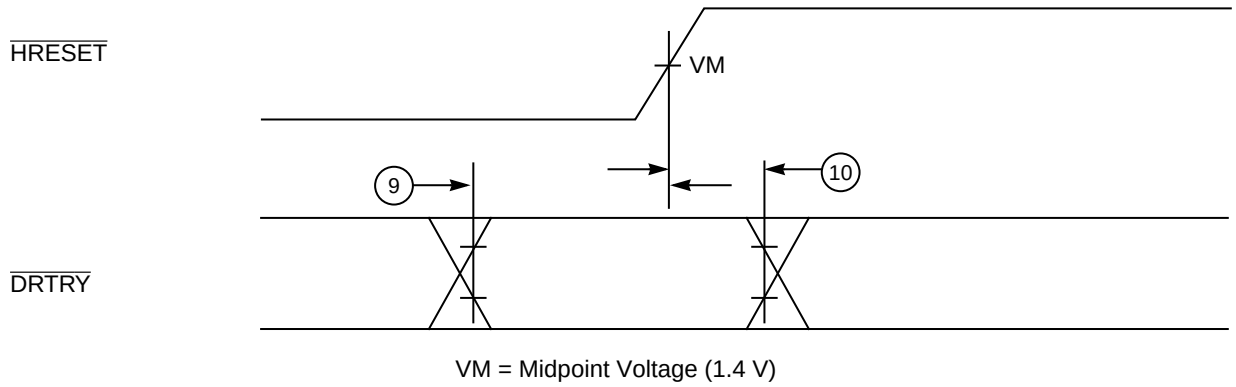


Figure 3. Mode Select Input Timing Diagram

1.4.2.3 Output AC Specifications

The output specifications of the 604e for both driving high and driving low depend on the capacitive loading on each output and the drive capability enabled for that output. Additionally, the timing specifications for outputs driving low also depend on the voltage swing required to drive to 0.8 V (either 5.5 V to 0.8 V or 3.6 V to 0.8 V). Table 8 provides the output AC timing specifications for a 50 pF load. In order to derive the actual timing specifications for a given set of conditions, it is recommended that IBIS simulation models be used. Contact the local Motorola or IBM sales office for information on the availability of these models.

The 604e adds a Fast Out output mode which will allow for increased system bus frequencies.Table 8 provides the output AC timing specifications for the 604e (shown in Figure 4) operating in 604 Compatibility mode and Fast Out mode. 604e Fast Out mode is selected by driving the L2_TSTCLK pin to GND. When Fast Out mode is enabled, the output valid and output hold times are reduced.

Table 8. Output AC Timing Specifications[1]

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C, Drive mode [01][7]

Num	Characteristic	150 MHz			166.67 MHz			180 MHz			Unit	Notes
		Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max		
11	SYSCLK to output driven (output enable time)	0.75	—	—	0.75	—	—	0.75	—	—	ns	2, 5
12a	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$ and $\overline{DBB}$ output valid (for 5.5 V to 0.8 V)	—	7.25	6.25	—	6.75	5.75	—	6.5	5.5	ns	3, 5
12b	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$ and $\overline{DBB}$ output valid (for 3.6 V to 0.8 V)	—	6.75	5.75	—	6.25	5.25	—	5.5	4.5	ns	5
13a	SYSCLK to all other signals output valid (for 5.5 V to 0.8 V)	—	8.25	7.25	—	7.75	6.75	—	7.5	6.5	ns	3, 5

Table 8. Output AC Timing Specifications[1] (Continued)

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_j ≤ 105 °C, Drive mode [01][7]

Num	Characteristic	150 MHz			166.67 MHz			180 MHz			Unit	Notes
		Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max		
13b	SYSCLK to all other signals output valid (for 3.6 V to 0.8 V)	—	7.75	6.75	—	7.25	6.25	—	6.5	5.5	ns	4
14	SYSCLK to output invalid (output hold)	0.5	—	0.0	0.5	—	0.0	0.5	—	0.0	ns	2, 5
15	SYSCLK to output high impedance (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	—	7.25	6.25	—	6.75	5.75	—	6.25	5.25	ns	
16	SYSCLK to output high impedance $\overline{\text{TS}}$, $\overline{\text{XATS}}$	—	7.25	6.25	—	6.75	5.75	—	6.25	5.25	ns	
17	SYSCLK to $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ high impedance after precharge	—	TBD	TBD	—	TBD	TBD	—	TBD	TBD	ns	4
18	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance before precharge	—	7.25	6.25	—	6.75	5.75	—	6.25	5.25	ns	
19	SYSCLK to $\overline{\text{ARTRY}}$, and $\overline{\text{SHD}}$ precharge enable	0.5* t_{sysclk} + 0.75	—	—	0.5* t_{sysclk} + 0.75	—	—	0.5* t_{sysclk} + 0.75	—	—	ns	4
20	Maximum delay to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ precharge	—	1.5* t_{sysclk}	1.5* t_{sysclk}	—	1.5* t_{sysclk}	1.5* t_{sysclk}	—	1.5* t_{sysclk}	1.5* t_{sysclk}	ns	
21	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge	—	2.0* t_{sysclk}	2.0* t_{sysclk}	—	2.0* t_{sysclk}	2.0* t_{sysclk}	—	2.0* t_{sysclk}	2.0* t_{sysclk}	ns	4
	Rise time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0	1.0		1.0	1.0		1.0	ns	6
	Rise time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0	1.0		1.0	1.0		1.0	ns	6
	Fall time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0	1.0		1.0	1.0		1.0	ns	6

Table 8. Output AC Timing Specifications[1] (Continued)

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_j ≤ 105 °C, Drive mode [01][7]

Num	Characteristic	150 MHz			166.67 MHz			180 MHz			Unit	Notes
		Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max	Min	Max	Fast Out Min/ Max		
	Fall time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0	1.0		1.0	1.0		1.0	ns	6

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 4).
2. This minimum parameter assumes C_L = 0 pF.
3. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from 3.6 V to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
5. Fast Out mode (L2_TSTCLK = GND) will improve output valid timing, Fast Out mode will reduce output hold times. The 604e powers up in Compatibility mode in a 604 system (L2_TSTCLK = OVdd)
6. These specifications are nominal values.
7. The drive mode signals must be DRVMODE0 = low, DRVMODE1 = high

Figure 4 provides the output timing diagram for the 604e.

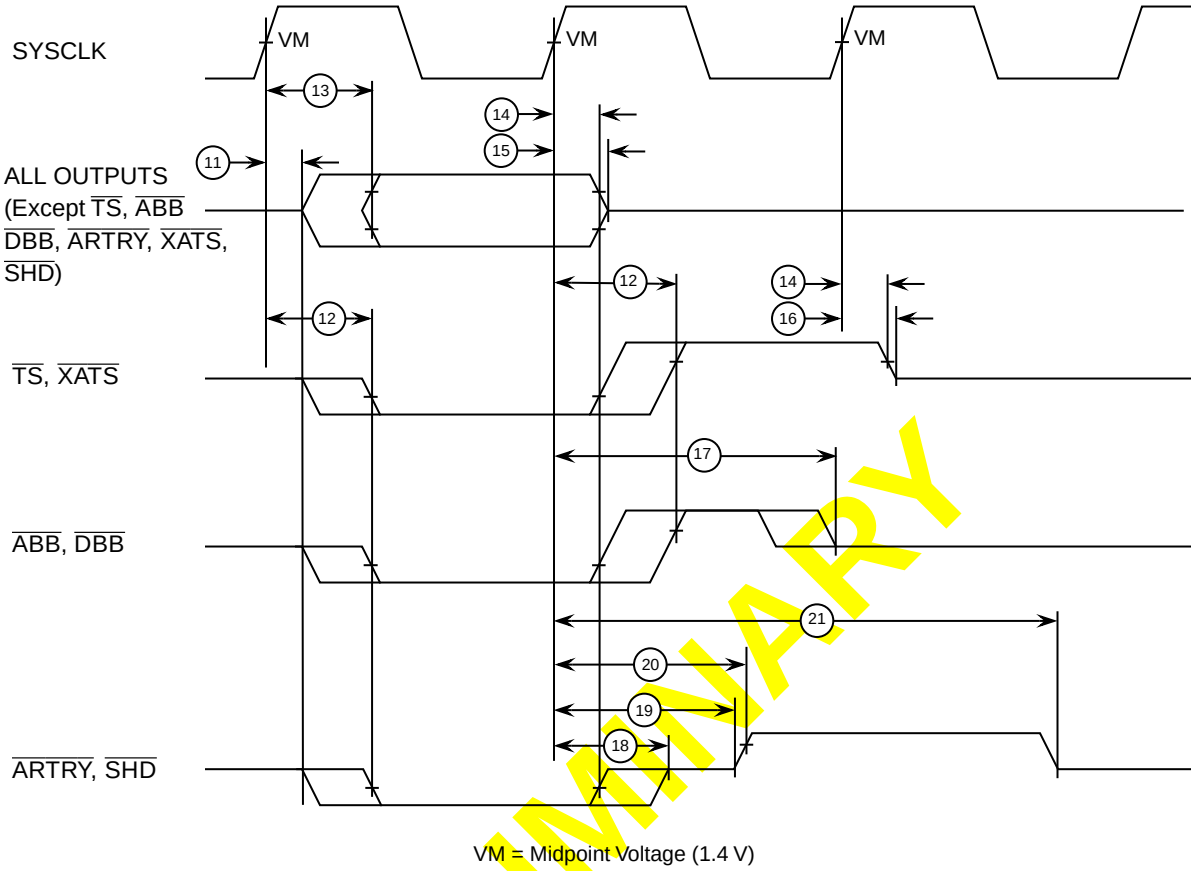


Figure 4. PowerPC 604e Microprocessor Output Timing Diagram

1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications.

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK)

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, C_L = 50 pF, $0 \le T_J \le 105$ °C

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.5 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	0	—	ns	2

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK) (Continued)

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	Min	Max	Unit	Notes
7	Boundary-scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.

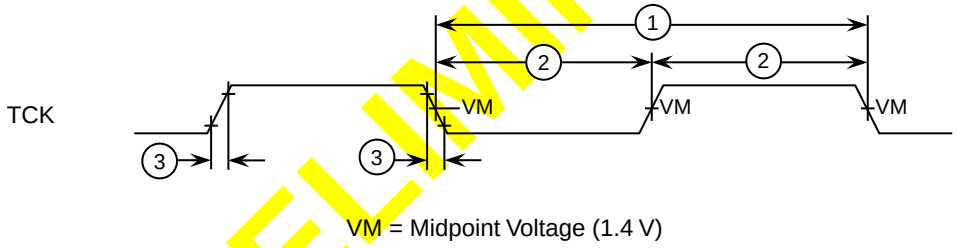


Figure 5. Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

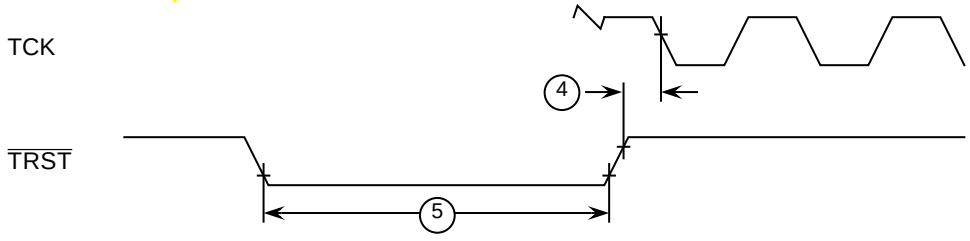


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

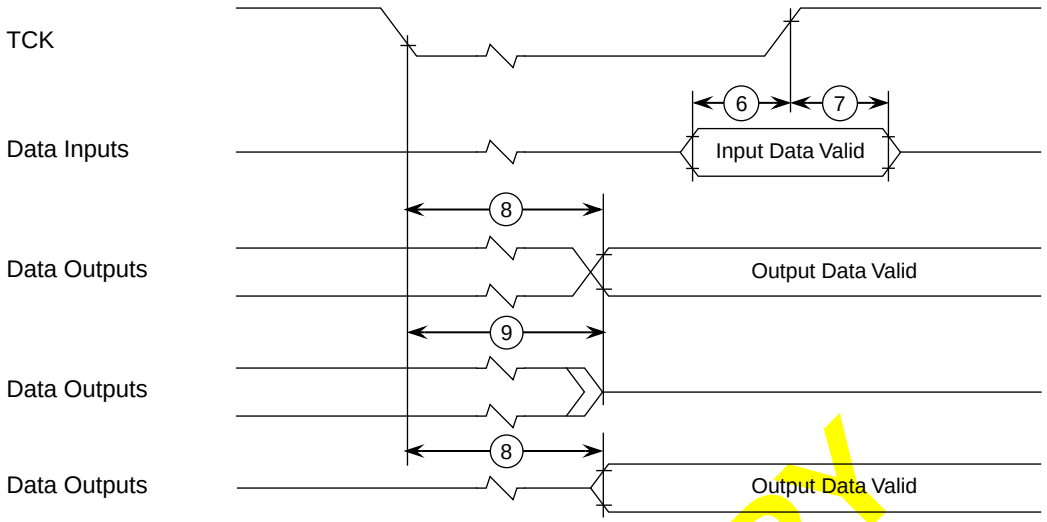


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

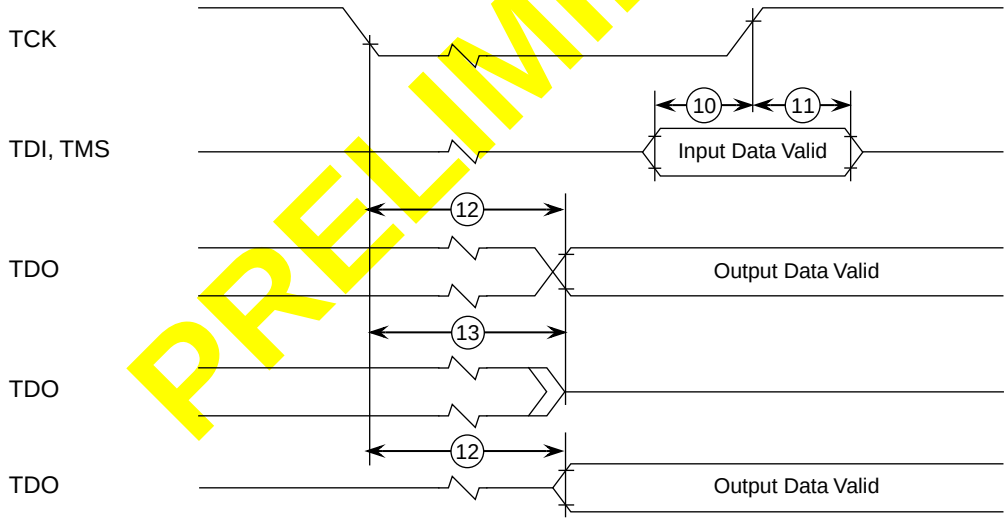


Figure 8. Test Access Port Timing Diagram

1.5 PowerPC 604e Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the 604e. Note that the 604e is currently offered in two packages. Motorola and IBM both offer a C4 ceramic quad flat pack (C4-CQFP), and a ball grid array (BGA) package. Both IBM and Motorola C4-CQFP and BGA packages have identical pinouts.

1.5.1 Pinout Diagram for the C4-CQFP Package

Figure 9 contains the pinout diagram of the C4-CQFP package for the 604e.

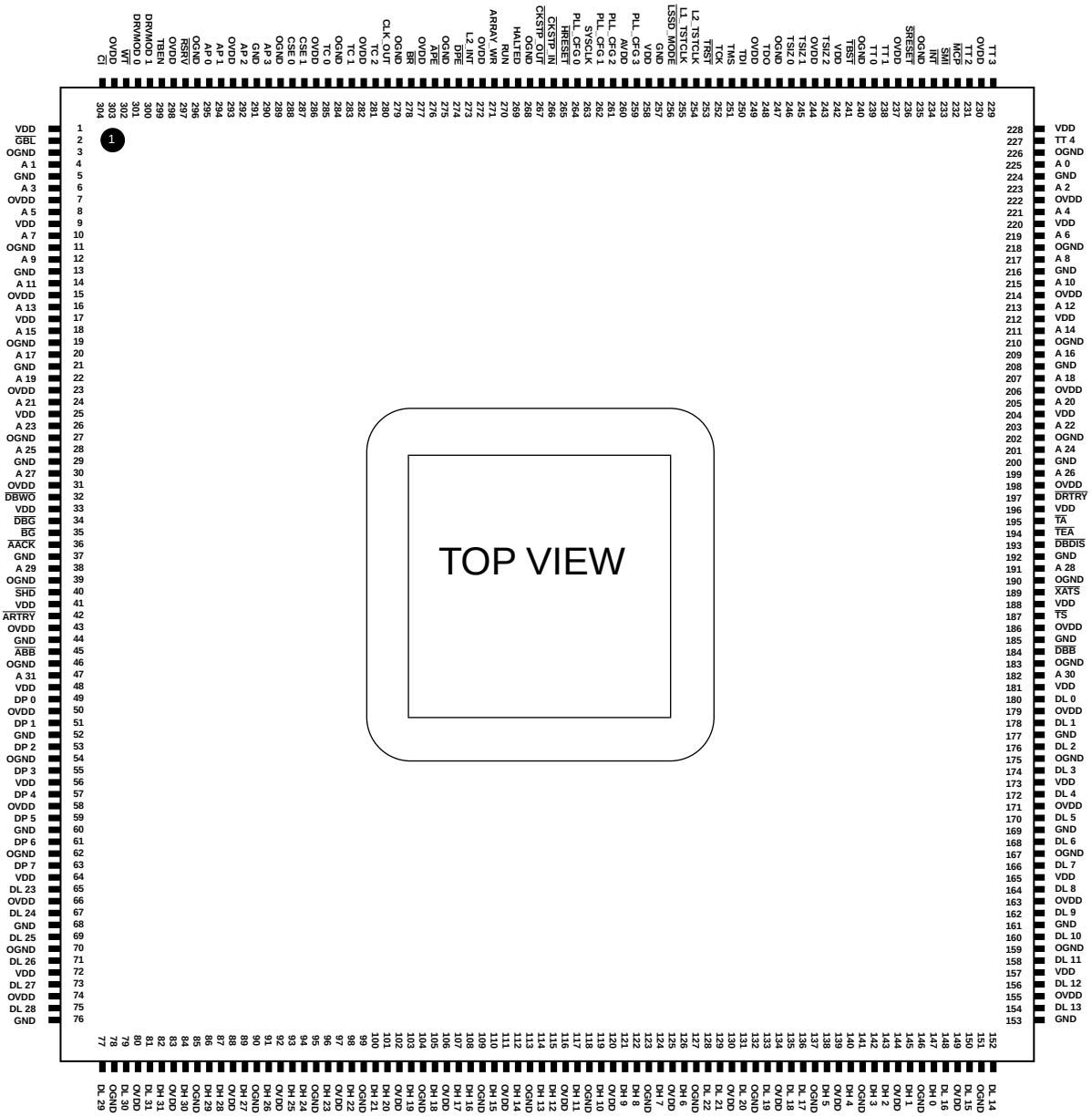
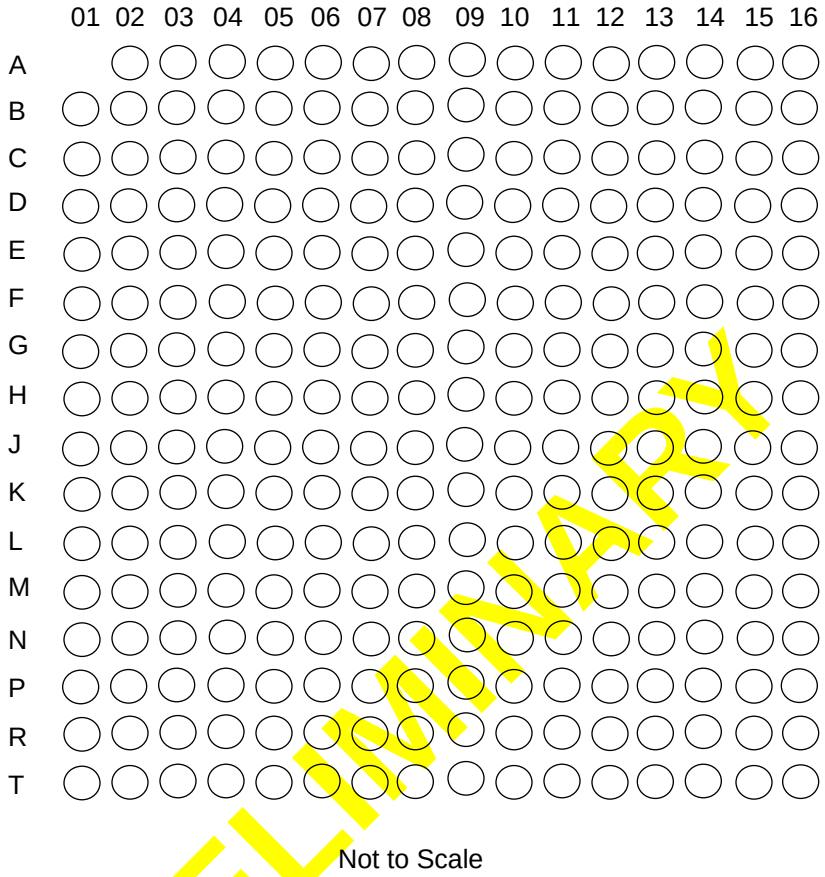


Figure 9. Pinout Diagram of the C4-CQFP Package

1.5.2 Pinout Diagram for the BGA Package

Figure 10 (in part A) shows the pinout of the BGA package as viewed from the top surface. Part B shows the side profile of the BGA package to indicate the direction of the top surface view.

Part A



Part B

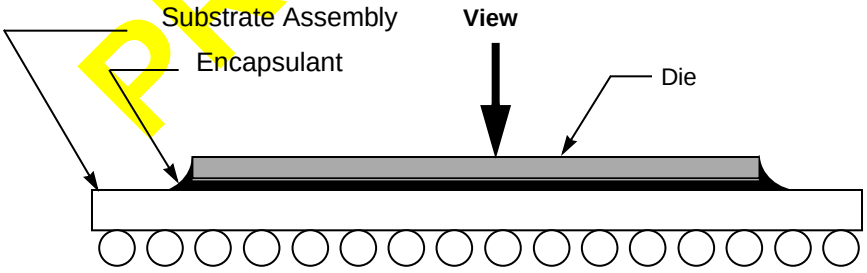


Figure 10. Pinout of the BGA Package as Viewed from the Top Surface

1.6 PowerPC 604e Microprocessor Pinout Listings

The following sections contain the pinout listings for the 604e C4-CQFP and BGA packages.

1.6.1 Pinout Listing for the C4-CQFP Package

Table 10 provides the pinout listing for the 604e C4-CQFP package.

Table 10. Pinout Listing for the C4-CQFP Package

Signal Name	Pin Number	Active	I/O
A[0–31]	225, 4, 223, 6, 221, 8, 219, 10, 217, 12, 215, 14, 213, 16, 211, 18, 209, 20, 207, 22, 205, 24, 203, 26, 201, 28, 199, 30, 191, 38, 182, 47	High	I/O
$\overline{\text{AACK}}$	36	Low	Input
$\overline{\text{ABB}}$	45	Low	I/O
AP[0–3]	295, 294, 292, 290	High	I/O
$\overline{\text{APE}}$	276	Low	Output
ARRAY_WR [1]	271	Low	Input
$\overline{\text{ARTRY}}$	42	Low	I/O
AVDD	260	—	—
$\overline{\text{BG}}$	35	Low	Input
$\overline{\text{BR}}$	278	Low	Output
$\overline{\text{CI}}$	304	Low	Output
$\overline{\text{CKSTP\_IN}}$	266	Low	Input
$\overline{\text{CKSTP\_OUT}}$	267	Low	Output
CLK_OUT	280	—	Output
CSE[0–1]	288, 287	High	Output
$\overline{\text{DBB}}$	184	Low	I/O
$\overline{\text{DBG}}$	34	Low	Input
$\overline{\text{DBDIS}}$	193	Low	Input
$\overline{\text{DBWO}}$	32	Low	Input
DH[0–31]	147, 145, 143, 142, 140, 138, 126, 124, 122, 121, 119, 117, 115, 114, 112, 110, 108, 107, 105, 103, 101, 100, 98, 96, 94, 93, 91, 89, 87, 86, 84, 82	High	I/O
DL[0–31]	180, 178, 176, 174, 172, 170, 168, 166, 164, 162, 160, 158, 156, 154, 152, 150, 148, 136, 135, 133, 131, 129, 128, 65, 67, 69, 71, 73, 75, 77, 79, 81	High	I/O
DP[0–7]	49, 51, 53, 55, 57, 59, 61, 63	High	I/O

Table 10. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	274	Low	Output
$\overline{\text{DRTRY}}$	197	Low	Input
DRVMOD0 [2]	301	Low	Input
DRVMOD1 [2]	300	High	Input
$\overline{\text{GBL}}$	2	Low	I/O
GND	5, 13, 21, 29, 37, 44, 52, 60, 68, 76, 153, 161, 169, 177, 185, 192, 200, 208, 216, 224, 257, 291	—	—
HALTED	269	High	Output
$\overline{\text{HRESET}}$	265	Low	Input
$\overline{\text{INT}}$	234	Low	Input
L1_TSTCLK [1]	255	Low	Input
L2_INT	273	High	Input
L2_TSTCLK [3]	254	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	256	Low	Input
$\overline{\text{MCP}}$	232	Low	Input
OGND	3, 11, 19, 27, 39, 46, 54, 62, 70, 78, 85, 90, 95, 99, 104, 109, 113, 118, 123, 127, 132, 137, 141, 146, 151, 159, 167, 175, 183, 190, 202, 210, 218, 226, 235, 240, 247, 268, 275, 279, 284, 289, 296	—	—
OVDD	7, 15, 23, 31, 43, 50, 58, 66, 74, 80, 83, 88, 92, 97, 102, 106, 111, 116, 120, 125, 130, 134, 139, 144, 149, 155, 163, 171, 179, 186, 198, 206, 214, 222, 230, 237, 244, 249, 272, 277, 282, 286, 293, 298, 303	—	—
PLL_CFG[0–3]	264, 262, 261, 259	High	Input
$\overline{\text{RSRV}}$	297	Low	Output
RUN	270	High	Input
$\overline{\text{SHD}}$	40	Low	I/O
$\overline{\text{SMI}}$	233	Low	Input
$\overline{\text{SRESET}}$	236	Low	Input
SYSCLK	263	—	Input
$\overline{\text{TA}}$	195	Low	Input
TBEN	299	High	Input
$\overline{\text{TBST}}$	241	Low	I/O

Table 10. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
TC0–TC2	285, 283, 281	High	Output
TCK	252	High	Input
TDI	250	High	Input
TDO	248	High	Output
$\overline{\text{TEA}}$	194	Low	Input
TMS	251	High	Input
$\overline{\text{TRST}}$	253	Low	Input
$\overline{\text{TS}}$	187	Low	I/O
TSIZ[0–2]	246, 245, 243	High	I/O
TT[0–4]	239, 238, 231, 229, 227	High	I/O
$\overline{\text{WT}}$	302	Low	Output
VDD	1, 9, 17, 25, 33, 41, 48, 56, 64, 72, 157, 165, 173, 181, 188, 196, 204, 212, 220, 228, 242, 258	—	—
$\overline{\text{XATS}}$	189	Low	I/O

Notes:
1. These are test signals for factory use only and must be pulled up to Vdd for normal machine operation.
2. To operate in accordance with these specifications, the drive mode signals must be DRVMODE0 = low, DRVMODE1 = high
3. This pin is connected to OVdd to select Compatibility mode output timing. Connecting it to GND will select Fast Out mode timing. See Section 1.4.2.3, “Output AC Specifications,” for more information.

1.6.2 Pinout Listing for the BGA Package

Table 11 provides the pinout listing for the 604e BGA package.

Table 11. Pinout Listing for the BGA Package

Signal Name	Pin Number	Active	I/O
A[0–31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0–3]	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
ARRAY_WR [1]	B07	Low	Input
$\overline{\text{ARTRY}}$	J04	Low	I/O

Table 11. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
AVDD	A10	—	—
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE[0–1]	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0–31]	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0–31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0–7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input
DRVMOD0 [2]	D05	Low	Input
DRVMOD1 [2]	C03	High	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
HALTED	B08	High	Output
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK [1]	D11	Low	Input
L2_INT	D06	High	Input
L2_TSTCLK [1]	D12	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	B10	Low	Input

Table 11. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{MCP}}$	C13	Low	Input
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0–3]	A08, B09, A09, D09	High	Input
$\overline{\text{RSRV}}$	D01	Low	Output
RUN	C08	High	Input
$\overline{\text{SHD}}$	H04	Low	I/O
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC[0–2]	A02, A03, C06	High	Output
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0–2]	A13, D10, B12	High	I/O
TT[0–4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
VOLTDETGND[3]	F03		
$\overline{\text{XATS}}$	J16	Low	I/O

Notes:

1. These are test signals for factory use only and must be pulled up to Vdd for normal machine operation.
2. To operate in accordance with these specifications, the drive mode signals must be DRVMODE0 = low, DRVMODE1 = high
3. NC (no-connect) in the 604; internally tied to GND in the 604e BGA package to indicate to the power supply that a low-voltage processor is present.

1.7 PowerPC 604e Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the 604e.

1.7.1 Motorola C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola C4-CQFP package.

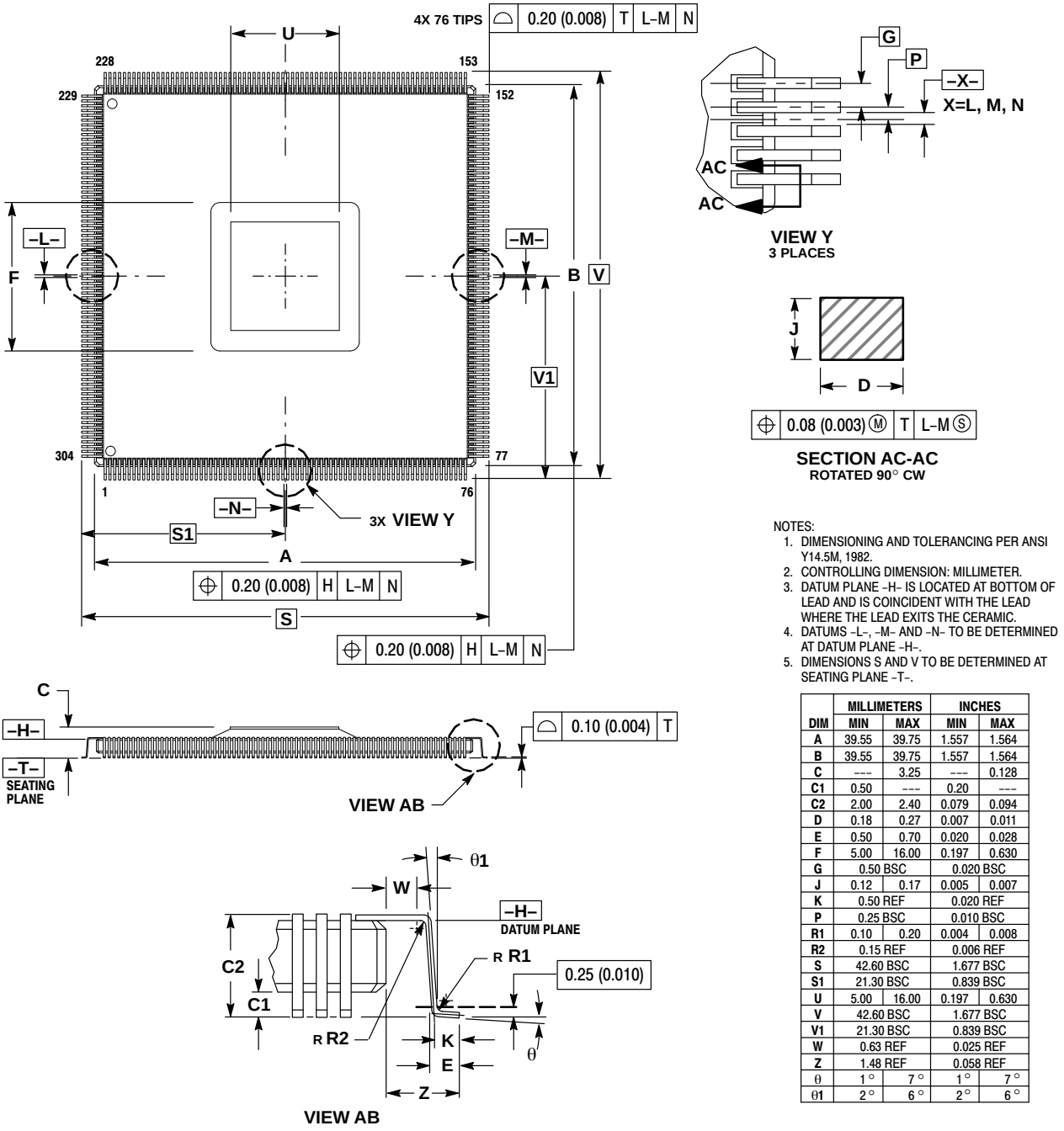
1.7.1.1 Package Parameters

The package parameters for the Motorola C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
C4 encapsulation	Glass-filled Epoxy
Maximum module height	3.25 mm
Co-planarity specification	0.10 mm

1.7.1.2 Mechanical Dimensions of the Motorola C4-CQFP Package

Figure 11 shows the mechanical dimensions of the Motorola C4-CQFP package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE CERAMIC.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	39.55	39.75	1.557	1.564
B	39.55	39.75	1.557	1.564
C	---	3.25	---	0.128
C1	0.50	---	0.20	---
C2	2.00	2.40	0.079	0.094
D	0.18	0.27	0.007	0.011
E	0.50	0.70	0.020	0.028
F	5.00	16.00	0.197	0.630
G	0.50 BSC		0.020 BSC	
J	0.12	0.17	0.005	0.007
K	0.50 REF		0.020 REF	
P	0.25 BSC		0.010 BSC	
R1	0.10	0.20	0.004	0.008
R2	0.15 REF		0.006 REF	
S	42.60 BSC		1.677 BSC	
S1	21.30 BSC		0.839 BSC	
U	5.00	16.00	0.197	0.630
V	42.60 BSC		1.677 BSC	
V1	21.30 BSC		0.839 BSC	
W	0.63 REF		0.025 REF	
Z	1.48 REF		0.058 REF	
θ	1°	7°	1°	7°
θ1	2°	6°	2°	6°

Figure 11. Mechanical Dimensions of the Motorola C4-CQFP Package

1.7.2 IBM C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM C4-CQFP package.

1.7.2.1 Package Parameters

The package parameters for the IBM C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
Lead encapsulation	Glass-filled Epoxy
C4 encapsulation	Glass-filled Epoxy
Maximum module height	3.1 mm
Co-planarity specification	0.08 mm

1.7.2.2 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 12 shows the mechanical dimensions for the IBM C4-CQFP.

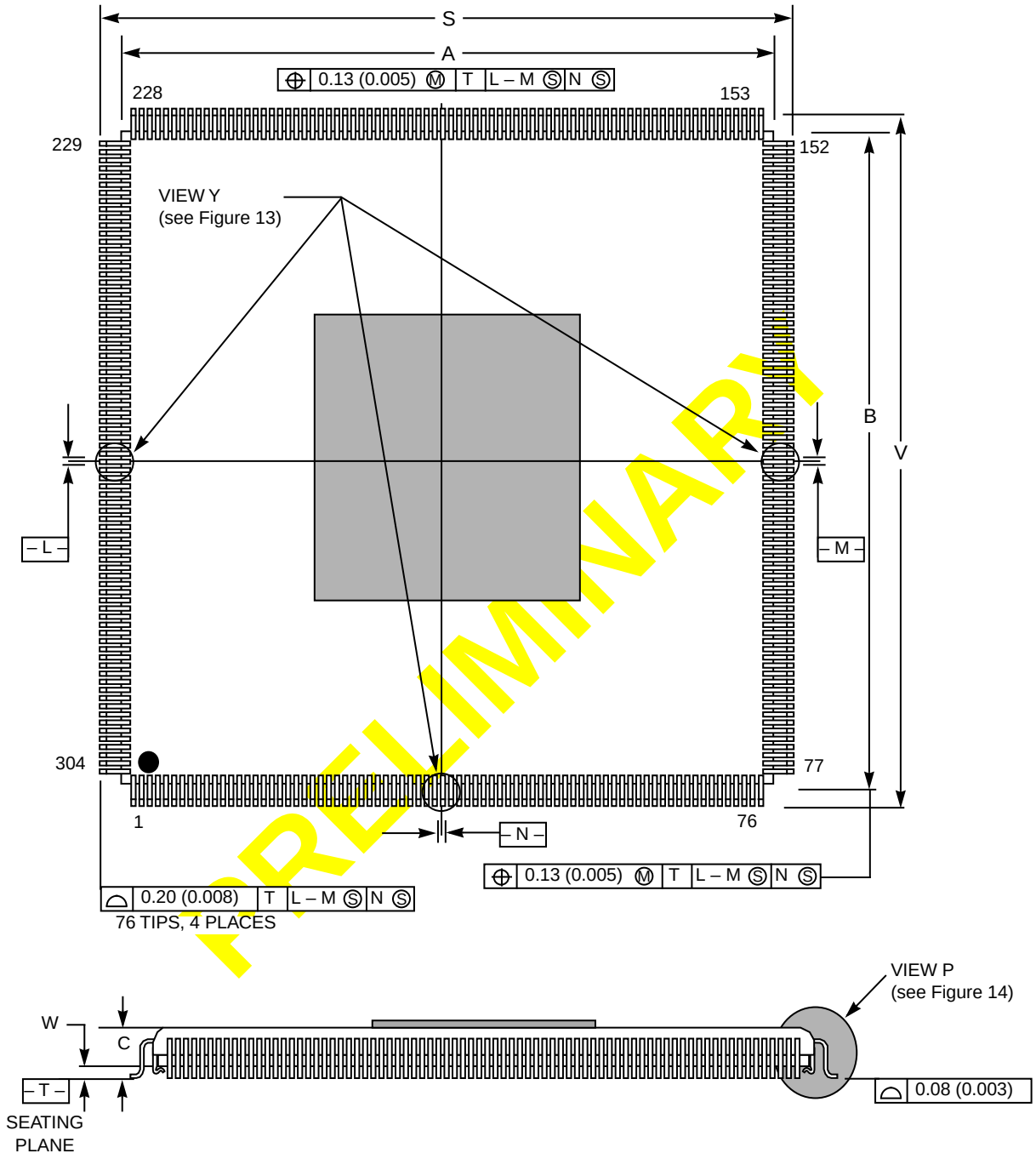


Figure 12. Mechanical Dimensions of the IBM C4-CQFP Package

Figure 13 and Figure 14 provide a more detailed representation of portions of IBM C4-CQFP package.

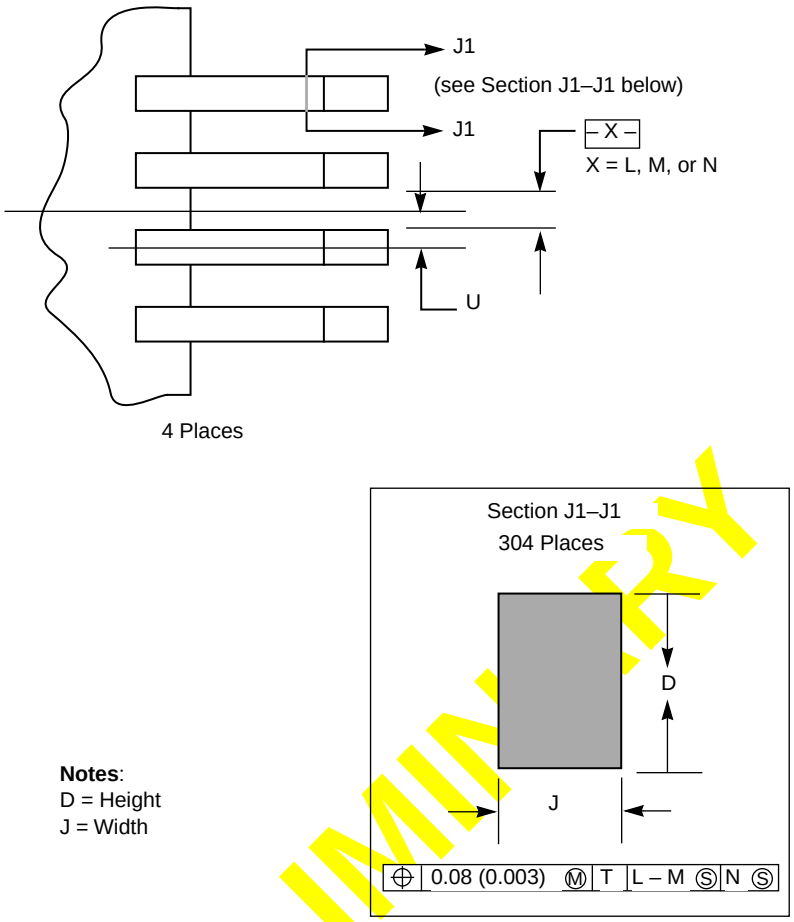


Figure 13. IBM C4-CQFP Mechanical Dimensions—View Y

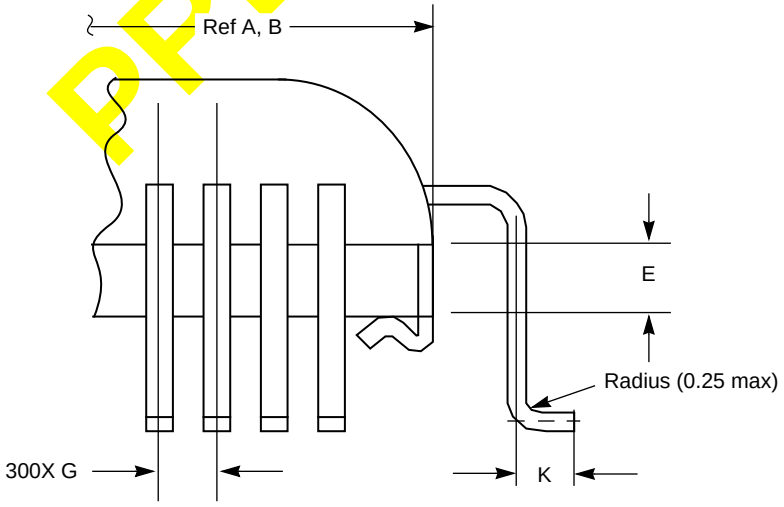


Figure 14. IBM C4-CQFP Mechanical Dimensions—View P

Table 12 lists the mechanical dimensions values for the IBM C4-CQFP package.

Table 12. Mechanical Dimensions Values

Dim	Millimeters	
	Min	Max
A	39.80	40.20
B	39.80	40.20
C	3.05	3.15
D	0.18	0.28
E	0.585	0.685
G	0.45	0.55
J	0.12	0.20
K	0.40	0.60
S	42.4	42.8
V	42.4	42.8
W	0.30	0.40

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimension—millimeter.
3. Datums – L –, –M –, and – N – to be determined at seating plane.
4. Dimensions S and V to be determined at seating plane – T–.
5. Dimensions A and B to outside of lead clip.

1.7.3 BGA Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM and Motorola BGA packages.

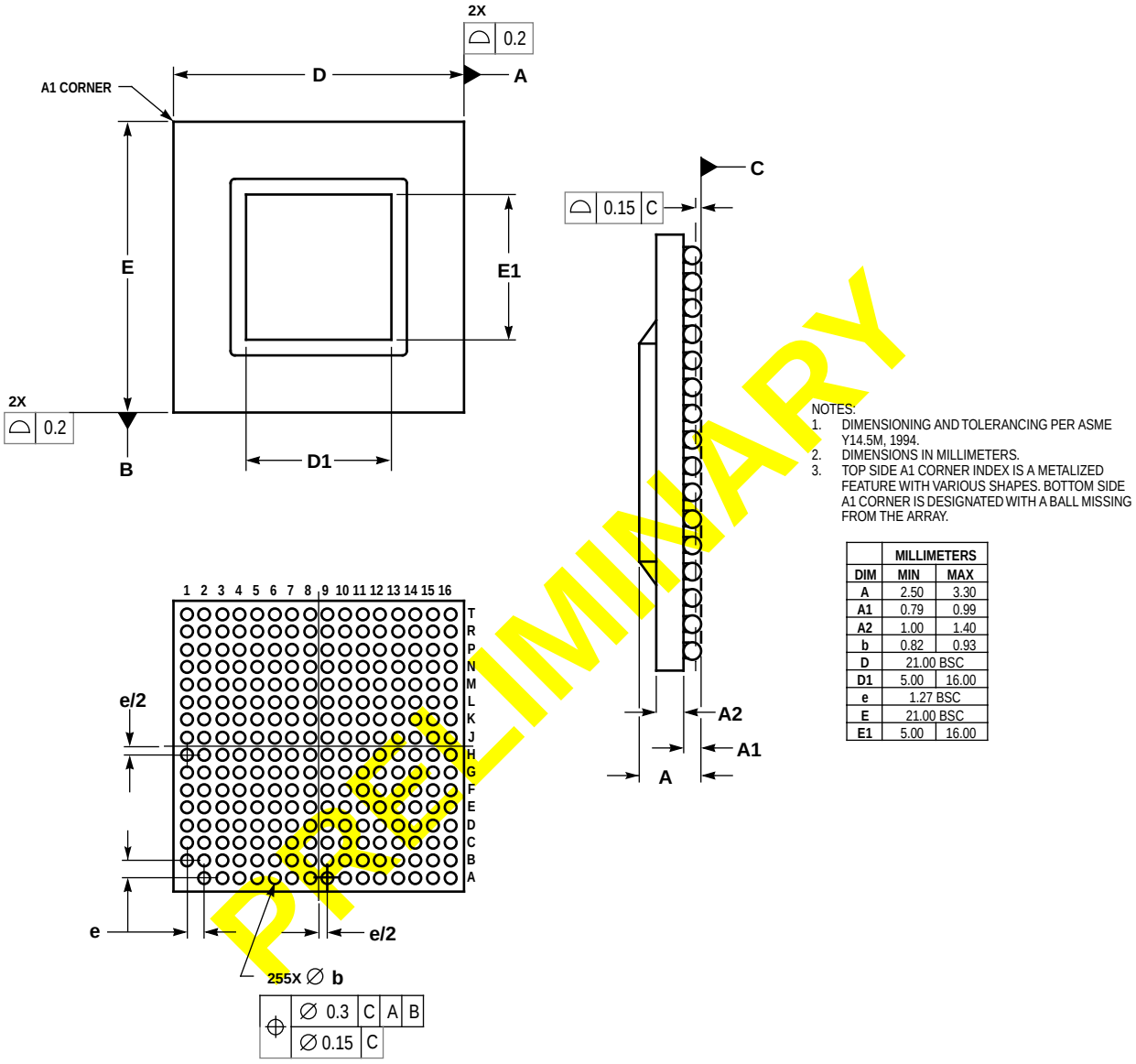
1.7.3.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 256-lead ceramic ball grid array (BGA).

Package outline	21 x 21 mm
Interconnects	255
Pitch	1.27 mm (50 mil)
Maximum module height	3.30 mm
Ball diameter	0.89 mm (35 mil)

1.7.3.2 Mechanical Dimensions of the BGA Package

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the IBM and Motorola BGA package.



	MILLIMETERS	
DIM	MIN	MAX
A	2.50	3.30
A1	0.79	0.99
A2	1.00	1.40
b	0.82	0.93
D	21.00 BSC	
D1	5.00	16.00
e	1.27 BSC	
E	21.00 BSC	
E1	5.00	16.00

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature of the BGA Package

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 604e.

1.8.1 PLL Configuration

The 604e PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the 603e is shown in Table 13 for nominal frequencies.

Table 13. PowerPC 604e Microprocessor PLL Configuration

PLL_CFG[0–3]	CPU Frequency in MHz (VCO Frequency in MHz)							
	CPU/ SYSCLK Ratio	VCO Multiplier	Bus 25 MHz	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.6 MHz
0100	2:1	x2	—	—	—	100 (200)	120 (240)	133 (267)
0101	2:1	x4	50 (200)	66.7 (267)	80 (320)	100 (400)	—	—
0110	2.5:1	x2	—	—	100 (200)	125 (250)	150 (300)	166 (333)
1000	3:1	x2	—	100 (200)	120 (240)	150 (300)	180 (360)	200 (400)
1010	4:1	x2	100 (200)	133 (267)	160 (320)	200 (400)	—	—
1100	1.5:1	x2	—	—	—	—	—	100 (200)
0011	PLL bypass							
1111	Clock off							

Notes:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not supported; see Section 1.4.2.2, “Input AC Specifications,” for valid SYSCLK and VCO frequencies.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.

1.8.2 PLL Power Supply Filtering

The AVdd power signal is provided on the 604e to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 16. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

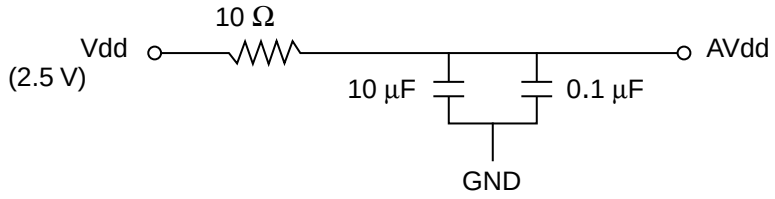


Figure 16. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the 604e's large address and data buses, and high operating frequencies, the 604e can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 604e system, and the 604e itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin of the 604e.

These capacitors should range in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantalum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance in the traces. Power and ground connections must be made to all external Vdd and GND pins of the 604e.

1.8.4 Connection Recommendations

To ensure reliable operation, it is recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND.

1.8.5 Thermal Management Information

This section provides thermal management information for the C4-CQFP and the BGA packages. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and the thermal interface material. Heat sinks are typically attached to a chip package by means of a spring clip to holes in the printed-circuit board; see Figure 17.

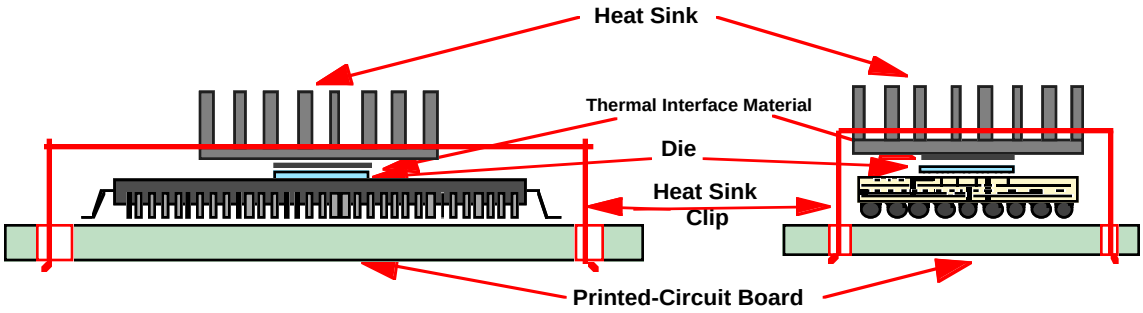


Figure 17. C4-CQFP and BGA Exploded Cross-Sectional View with Heat Sink

The board designer can choose between several types of heat sinks to place on the 604e. There are several commercially-available heat sinks for the 604e provided by the following vendors:

Thermalloy
2021 W. Valley View Lane 214-243-4321
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation (IERC)
135 W. Magnolia Blvd.
Burbank, CA 91502 818-842-7277

Aavid Engineering 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Ultimately, the final selection of an appropriate heat sink for the 604e depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.8.5.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 14, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

Table 14. Package Thermal Resistance

Thermal Metric	C4-CQFP	BGA
Junction-to-top of die thermal resistance	0.03 °C/W	0.03 °C/W
Junction-to-lead (ball) thermal resistance	18.0 °C/W	2.2 °C/W

Figure 18 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

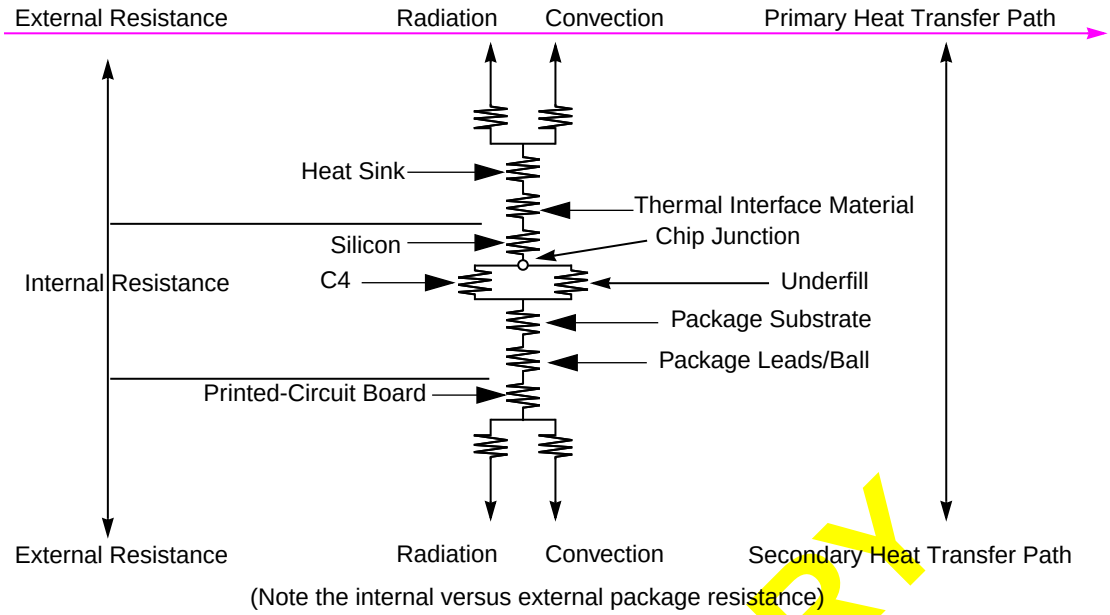


Figure 18. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms. The following section provides a thermal management example for the 604e using one of the commercially available heat sinks.

1.8.5.2 Thermal Management Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (R_{\theta jc} + R_a + R_{sa}) * Q$$

Where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the system cabinet
$R_{\theta jc}$ is the die-junction-to-top of die thermal resistance of the device
R_a is the thermal resistance of the thermal interface material (thermal grease or thermal compound)
R_{sa} is the heat sink-to-ambient thermal resistance
Q is the power dissipated by the device

Typical die-junction temperatures (T_j) should be maintained less than 105 °C. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. A computer cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The thermal resistance of the interface material (R_a) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, and a power dissipation (Q) of 18 watts, the following expression for T_j is obtained:

Junction temperature: $T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + R_{sa}) * 18\ W$

For a Thermalloy heat sink #2333B, the heat sink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 19.

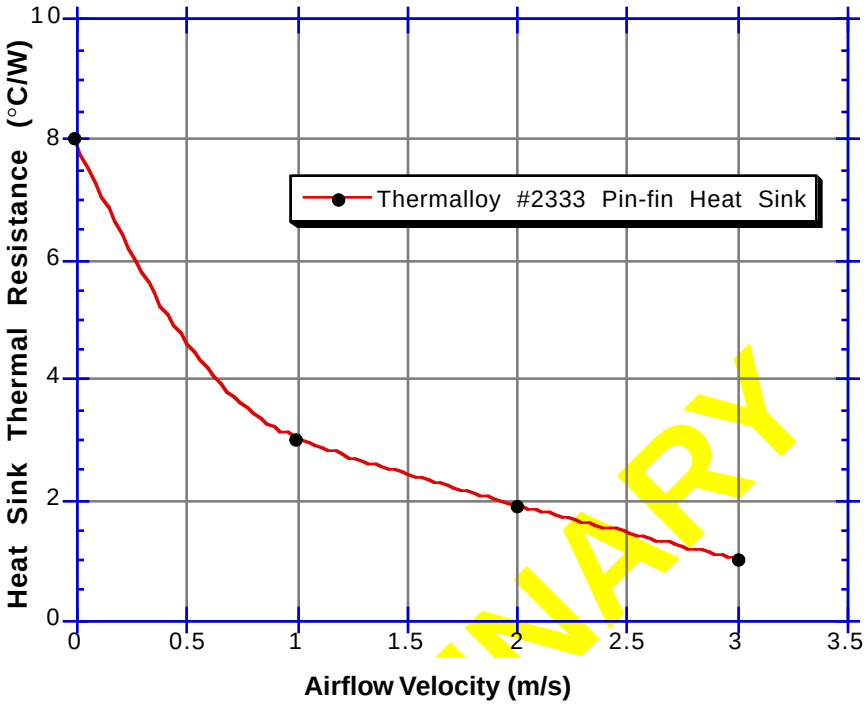


Figure 19. Thermalloy #2333B Pin-Fin Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Assuming an air velocity of 1 m/s, we have an effective R_{sa} of 3 °C/W, thus

$$T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + 3\ °C/W) * 17\ W,$$

resulting in a junction temperature of approximately 107 °C which is more than the maximum operating temperature of the part. To ensure maximum reliability, it is desirable to operate the 604e well within its operating temperature range. Thus, to keep a 17-Watt 604e within its proper operating range, an air velocity greater than 1 m/s should be used with the Thermalloy #2333B pin-fin heat sink.

Other heat sinks offered by Thermalloy, Aavid, Wakefield, and IERC offer different heat sink-to-ambient thermal resistances, and may or may not need air flow. It is necessary to perform an analysis as done above to select the desired heat sink.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are commonly used to compare the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's

microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs. To expedite system-level thermal analysis, several “compact” thermal-package models are available within FLOTHERM®. These are available upon request.

1.9 Ordering Information

This section provides the part numbering nomenclature for the 604e. Note that the individual part numbers correspond to a specific combination of 604e internal/bus frequencies, which must be observed to ensure proper operation of the device. For available frequency combinations, contact your local Motorola or IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier indicates the enhancement in the part from the original production design. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

1.9.1 Motorola Part Number Key

Figure 20 provides the Motorola part numbering nomenclature for the 604e.

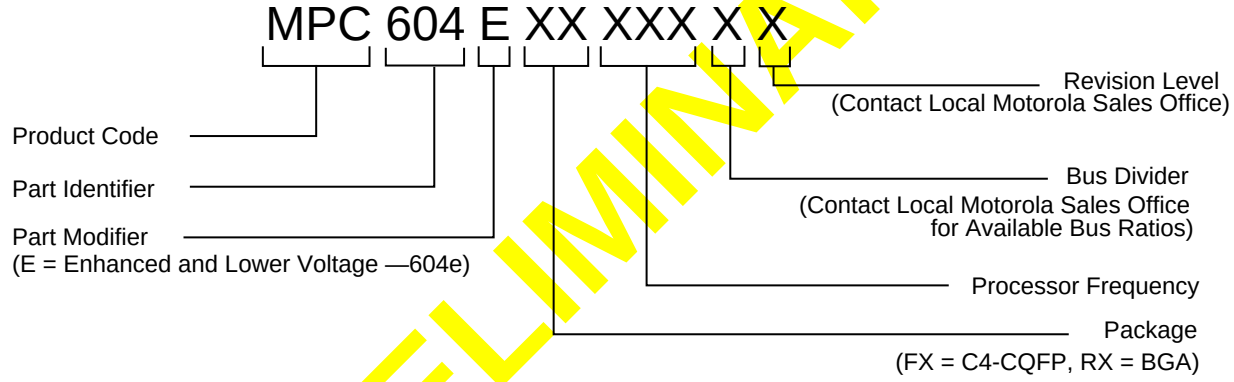


Figure 20. Motorola Part Number Key

1.9.2 IBM Part Number Key

Figure 21 provides the IBM part numbering nomenclature for the 604e.

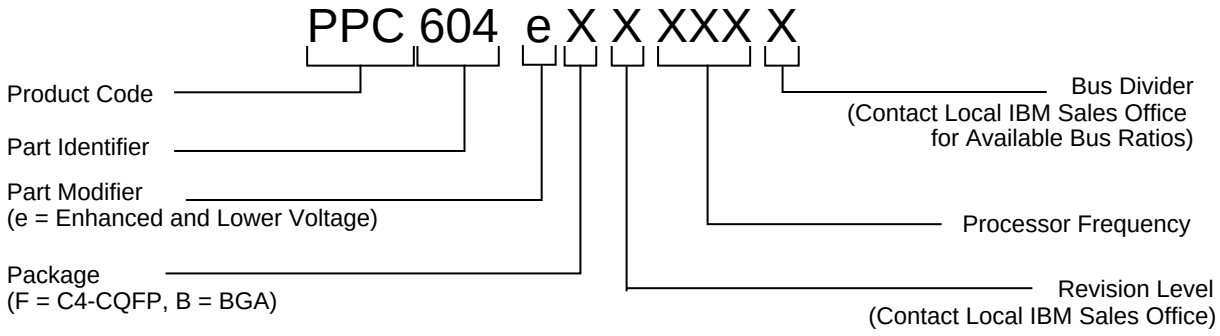


Figure 21. IBM Part Number Key

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