Intel® StrongARM* SA-1111 Microprocessor Companion Chip

Specification Update

March 2000

Notice: The SA-1111 may contain design defects or errors known as errata. Characterized errata that may cause the board's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278260-008

Contents

Revision History

Date	Version	Description
04/2/99	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
05/28/99	002	Modify the I/O type for the nOE pin. Modify the assignment for pin 131. Add a note to section 3.2.1. Convert TBDs to values for power and ground pins. Update the descriptions for nSDCS, nSDRAS, and SysClk. Change the normal frequency of UCLK48, UCLK12, and PCLK. Change the enabling condition for the Port Resume interrupt.
09/8/99	003	Add enabling DCLK errata, add pin multiplexing of MSCLK, MSDATA, and PWM1 pins in low-power state errata, add external Bitclk for Serial Audio errata, and add Bitclk, Sysclk, and PS/2 clock errata. All previous document changes (except for some of the TBD's) have been removed from the specification update and applied to the SA-1111 Developer's Manual. Change the description for the ID register.
09/22/99	004	Add 5 V I/O cell leakage errata, add 2 KV ESD test errata, and add cold-test USB errata.
10/5/99	005	Update SACR0 register definitions. Update nOE definitions. Remove cold-test USB errata. Change status for 5 V IO cell leakage errata to Fix. Change status for 2 KV ESD errata to Fix.
10/13/99	006	Update nOE_EN bit definitions in the SKCR register and classify the nOE update as a Specification Change.
10/21/99	007	Update Figure 7-4 MSB-Justified Data Formats (16 bits).
3/1/99	008	Remove errata for item 1 through 6 in the GDS1111BA version. Add note to SA-1111 DC Operating Conditions. Update SCLK definition in Section 2.4.2 and Section 8.1.1.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM® SA-1111 Microprocessor Companion Chip Developer's Manual	278242-002

Nomenclature

Errata are design defects or errors. These may cause the SA-1111's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® StrongARM* SA-1111 Microprocessor Companion Chip (SA-1111). Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A0	B0	#			
1	X			12	Fixed	Enabling DCLK hangs the system.
2	X			12	Fixed	Pin multiplexing of MSCLK, MSDATA, and PWM1 pins in low-power state is not correct.
3	X			12	Fixed	External Bitclk for Serial Audio (I2S) not implemented.
4	X			12	Fixed	The clock signals Bitclk, Sysclk, and the PS/2 clock hang the system.
5	X			13	Fixed	5 V I/O cell leakage.
6	X			13	Fixed	Fails testing for 2 KV human body model Electro-Static Discharge

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	A0	B0			
1		X	14	Fix	Add nOE Signal and Register Bit nOE_EN in the SKCR Register

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
1				15		None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278242-002	16	Doc	Functional Blocks: Section 2.1
2	278242-002	16	Doc	Intel® StrongARM® SA-1110 System Bus Interface - Signals: Section 3.1.1.
3	278242-002	17	Doc	DRAM Control Signal Generation: Section 3.2.3.5
4	278242-002	19	Doc	Control Register (SKCR): Section 3.3.1
5	278242-002	20	Doc	ID Register (SKID): Section 3.3.3
6	278242-002	20	Doc	RAB Central Address Decoder: Section 4.1.1.
7	278242-002	21	Doc	Serial Audio Common Control Register (SACR0): Section 7.4.1.1.
8	278242-002	22	Doc	AC and DC Signal Requirements: Section 13.1
9	278242-002	24	Doc	Absolute Maximum Ratings: Section 13.2.2

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
10	278242-002	24	Doc	DC Operating Conditions: Section 13.2.4
11	278242-002	24	Doc	I2S and MSB-Justified Serial Audio Formats: Section 7.3.2.2
12	278242-002	25	Doc	Doze Mode: Section 2.4.2
13.	278242-002	25	Doc	External Interface to SSP, SPI, or Microwire Peripherals: Section 8.1.1

Identification Information

Markings

GDS1111AA and GDS1111BA.

This document contains errata for the SA-1111. The revision that is affected by this errata can be identified as order number GDS1111AA and GDS1111BA. The GDS1111AA, which were engineering samples, can be identified by package marking GDS1111AA or by reading the value of 690CC200 in the SKID register. The GDS1111BA can be identified by package marking GDS1111BA or by reading the value of 690CC211 in the SKID register.

Errata

1. Enabling DCLK hangs the system.

Problem: The signal LatchedReq in the DmaArbiter does not reset on power-up. If LatchedReq comes up as a 1, it causes the signal anyreq to go active and the SMC requests the external system bus with the signal MBREQ. Because there is no real request from SAC or the USB, the internal handshake never completes and the system hangs.

Implication: The system hangs.

Workaround: A software fix does exist for this errata.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

2. Pin multiplexing of MSCLK, MSDATA, and PWM1 pins in low-power state is not correct.

Problem: Pins MSCLK, MSDATA, and PWM1 are multiplexed with L3 and the GPIO functions. If L3 is enabled, the pins are correctly switched to GPIO functions. If the PS/2 Mouse or the PWM1 is enabled, the pins are not switched over to GPIO functions.

Implication: Pins MSCLK, MSDATA, and PWM1 are not multiplexed with the GPIO functions if the PS/2 Mouse or the PWM1 is enabled.

Workaround: Disable the PS/2 Mouse or the PWM1 with software before going into a low-power state.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

3. External Bitclk for Serial Audio (I2S) not implemented.

Problem: The external Bitclk source for Serial Audio (I2S) does not function as described in the I*ntel*® *StrongARM*® *SA-1111 Microprocessor Companion Chip Developer's Manual*.

Implication: Using the external Bitclk with the Serial Audio function will not operate properly.

Workaround: Use the internal clock with the Serial Audio function.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

4. The clock signals Bitclk, Sysclk, and the PS/2 clock hang the system.

Problem: An improper waveform is present on the PLLClk, which affects clock signals Bitclk, Sysclk, and the PS/2 clock. This improper signal puts the clock state into an illegal state and the state machine does not recover.

Workaround: The system hangs.

Workaround: None.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

5. 5 V I/O cell leakage.

Problem: At very low test rates, currents can be detected coming out of the I/O cells during the input and tri-state leakage tests.

Implication: May affect long-term reliability.

Workaround: None.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

6. Fails testing for 2 KV human body model Electro-Static Discharge

Problem: SA-1111 devices that have undergone the 2 KV human body model Electro-Static Discharge (ESD) test, fail retesting for leakage currents, sleep currents, continuity, and functional failures.

Implication: The SA-1111 device may not function properly after receiving a 2 KV ESD test.

Workaround: None.

Status: Fixed in GDS1111BA and all subsequent steppings. This errata only existed with GDS1111AA, which were engineering samples (see Errata table on page 9).

Specification Changes

1. Add nOE Signal and Register Bit nOE_EN in the SKCR Register

Issue: The nOE signal was added to control transceiver direction. This signal is enabled by bit 13 in the SKCR register.

Affected Docs: *Intel® StrongARM® SA-1111 Microprocessor Companion Chip Developer's Manual.*

Status: Fix.

Specification Clarifications

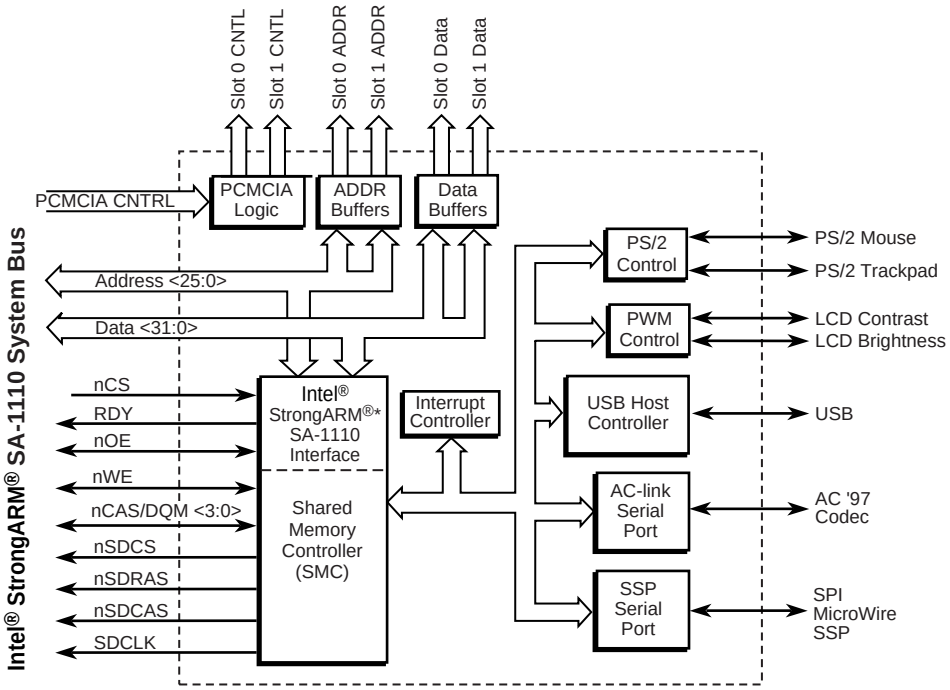
1. None for this revision of this specification update.

Documentation Changes

1. Functional Blocks: Section 2.1

Changed the signal nOE in Figure 2-1 from an input to a bi-directional arrow. Figure 2-1 now appears as follows:

Figure 2-1. SA-1111 Block Diagram



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2. Intel® StrongARM® SA-1110 System Bus Interface - Signals: Section 3.1.1.

Signal nOE changed from I to I and O/D. Table 3-1 now appears as follows:

Table 3-1. SA-1110 Memory Interface Signals - O(D) = Driven for DMA (Sheet 1 of 2)

Signal	Type	Description
A<25:0>	I and O(D)	26-bit address bus
D<31:0>	I/O	32-bit data bus
nCS	I	Chip select (dedicated to SA-1111 access), asserted low
nOE	I and O(D)	Output enable, asserted low for reads

Table 3-1. SA-1110 Memory Interface Signals - O(D) = Driven for DMA (Sheet 2 of 2)

Signal	Type	Description
nWE	I and O(D)	Write enable, asserted low for writes
RDY	O	Indicates SA-1111 has taken write data, or read data is available
DQM<3:0>	I and O(D)	SDRAM byte enable
MBREQ	O	Request to SA-1110 for bus ownership
MBGNT	I	Grant from SA-1110 - bus is available
nSDCS/nRAS	O(D)	SDRAM Chip Select, to any bank of SDRAM
nSDRAS	O(D)	RAS (Row Address Strobe), for SDRAM
nSDCAS	O(D)	CAS (Column Address Strobe) for SDRAM
SDCLK	O(D)	SDRAM Clock (48 MHz)

3. DRAM Control Signal Generation: Section 3.2.3.5

Signal nOE added to bulleted list, added text to this section, updated Figure 3-7 and Figure 3-8. This section now appears as follows:

On system initialization, the system must load the SMC register indicating what type of DRAM is being used. Bit 0 of the SMC Control Register (DTIM) must always be programmed with a one.

For SDRAM control, the SMC generates the following set of signals (see Figure 3-7 and Figure 3-8):

- SDCLK – 48 MHz clock
- nSDRAS – Row Address Strobe
- nSDCAS – Column Address Strobe
- nOE – Output enable
- nWE – Write enable
- nSDCS – chip select for SDRAMs
- DQM<3:0> byte enables

Signal SDCKE (Clock Enable) is always driven from the SA-1110. It is deasserted during the clock hand over period when bus ownership transfers between masters, then reasserted to enable the new owner's clock.

The SMC also drives signal nOE during DMA transfers. The behavior of nOE is programmable for use in systems with different bus architectures. The nOE behavior may be enabled or disabled. For example, a design may limit system bus loading by placing buffers and transceivers between the SA-1110 (with its system memory) and other peripherals, including the SA-1111. For DMA cycles, the SA-1111 must move data through the transceivers in either direction, depending on whether it is a read or write transfer. Signal nOE may be used to control transceiver direction if it is enabled. When enabled, it is asserted low on reads to SDRAM, and remains high for writes.

Other systems may not require nOE assertion for DMA transfers. If it is disabled, nOE is still driven by the SA-1111 but remains high (deasserted) for both reads and writes.

Figure 3-7. SDRAM Read Cycle, Burst of 2 - CAS Latency = 3

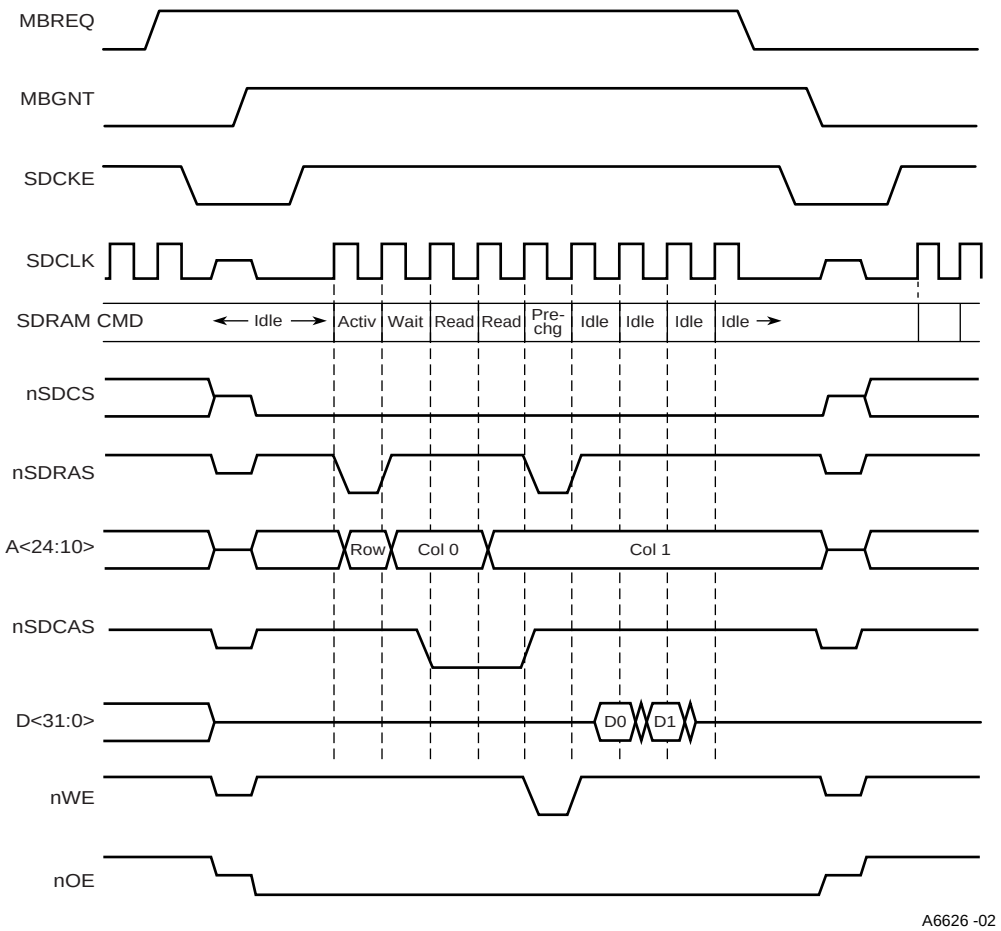
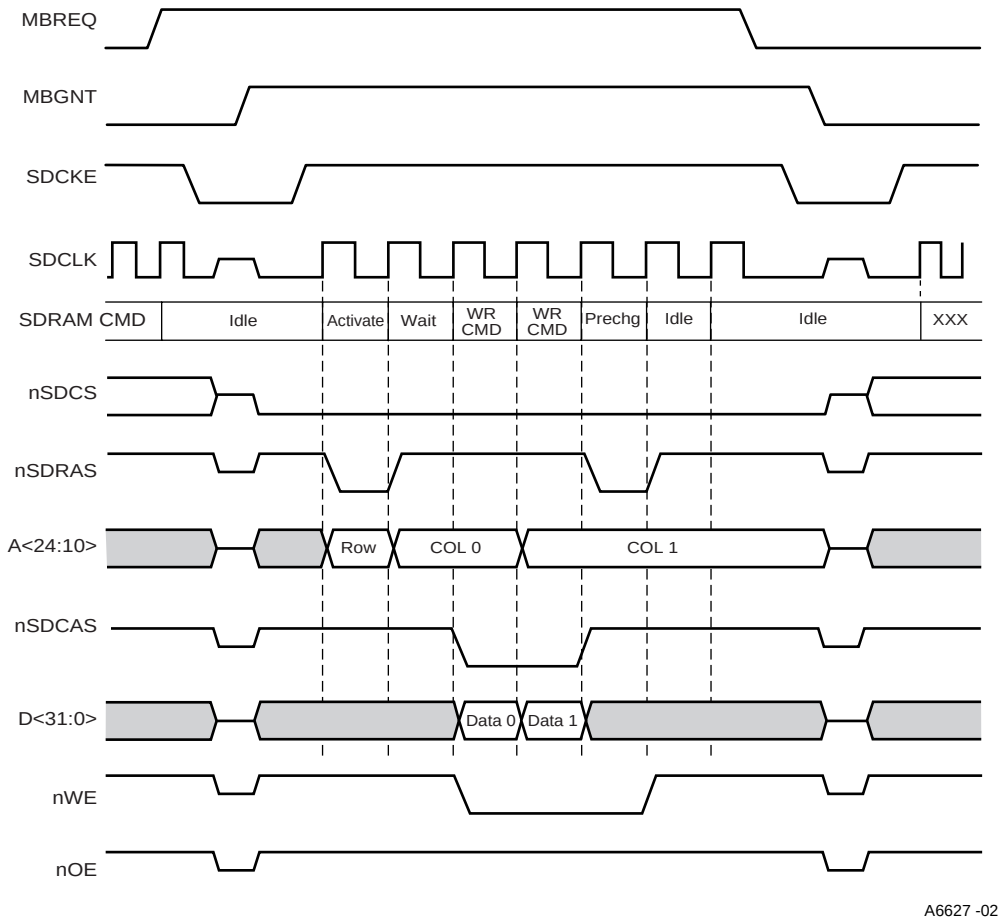


Figure 3-8. SDRAM Write Cycle, Burst of 2



4. Control Register (SKCR): Section 3.3.1

Added nOE to Table 3-9. Table 3-9 now appears as follows:

Table 3-9. SKCR Register Bit Descriptions

Bit	Name	Reset Value	Function
0	PLL_Bypass	0	Specifies on-chip PLL or external source for clocks 1 = Enable 0 = Bypass
1	RCLKEn	0	Enables Internal System Bus Clocks (RCLK and DCLK). 1 = Enable
2	Sleep	0	Force entry into Sleep mode 1 = Enter sleep mode
3	Doze	0	Force entry into Doze mode 1 = Enter doze mode

Bit	Name	Reset Value	Function
4	VCO_OFF	0	VCO on/off - enables or disables system PLL for clock generation 1= Off 0 = On
5	ScanTestEn	0	Enables scan test. Takes effect only in test mode. 1 = Enable
6	ClockTestEn	0	Enables clock test. Takes effect only in test mode. 1 = Enable
7	RdyEn	1	Enable RDY response (for SA-1110) vs. fixed-length register accesses 1 = Enable
8	SeLAC	0	Audio Feature Select 1 = AC Link 0 = 1^2S
9	OPPC	0	Out only pad control. Takes effect only in test mode. 1= Tri-states all the output pads.
10	PllTestEn	0	Enables Pll test. Takes effect only in test mode.
11	UsbIOTestEN	0	Enables USB IO cell test. Takes effect only in test mode.
12	—	0	Reserved.
13	nOE_EN	0	Enables nOE assertion on DMA read cycles from SDRAM: 0= Disable 1= Enable
15:14	—	0	Reserved.

5. ID Register (SKID): Section 3.3.3

Description changed in Table 3-11. The table now appears as follows:

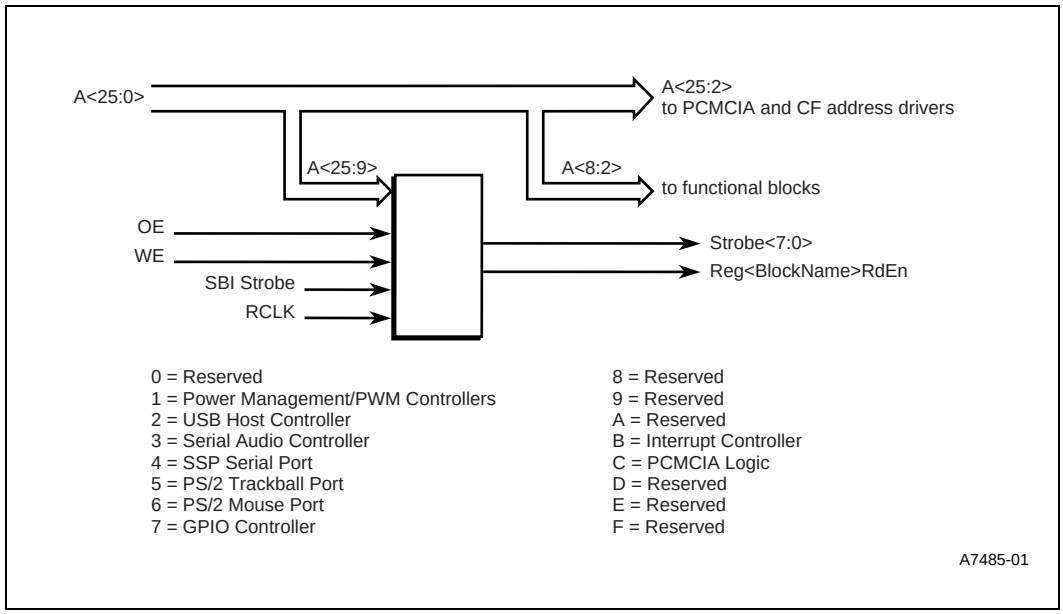
Table 3-11. SKID Register Bit Descriptions

Bit	Name	Function
7:0	Component Revision	Specifies the revision of the component in two hex value; bits 7:4 are the silicon revision level, bits 3:0 are the metal revision level.
31:8	Component Identifier	Specifies the identity of the SA-1111 as: 0x690CC2XX (where XX represents bits 7:0).

6. RAB Central Address Decoder: Section 4.1.1.

Updated address assignments in Figure 4-1. Figure 4-1 now appears as follows:

Figure 4-1. Decoder Block Diagram



7. Serial Audio Common Control Register (SACR0): Section 7.4.1.1.

Description changed for bit 2, BCKD, for the 0 and 1 states. The table now appears as follows:

Table 7-7. SACR0 Bit Descriptions

Bit	Name	FUNCTION
0	ENB	Enable SAC function: 0 = Pins function as GPIOs (SAC function is disabled) 1 = Pins function as Serial Audio Controller (SAC function is enabled)
1	—	Reserved
2	BCKD	Specify BIT_CLK pin direction: 0 = Output 1 = Input
3	RST	Reset the SAC Control and FIFOs except this register: 0 = Not reset 1 = Reset is Active to Other SAC Registers
7:4	—	Reserved
11:8	TFTH	Transmit FIFO interrupt or DMA threshold; set to value 0 – 15. This value should be set to the desired threshold value minus one. Larger values provide a longer latency than smaller values. Latency values of nine or greater have their bursts separated into two bursts. Using threshold values that are too large can result in an overflow condition. Using threshold values that are too small can result in an underflow condition. The optimum value, which is system dependent, results in the FIFO being half full.
15:12	RFTH	Receive FIFO interrupt or DMA threshold; set to value 0 – 15. This value should be set to the desired threshold value minus one. Larger values provide a longer latency than smaller values. Latency values of nine or greater have their bursts separated into two bursts. Using threshold values that are too large can result in an overflow condition. Using threshold values that are too small can result in an underflow condition. The optimum value, which is system dependent, results in the FIFO being half full.

8. AC and DC Signal Requirements: Section 13.1

Values need to be added for the following table.

Table 13-1. AC and DC Requirements

Name	Type	Description
SA-1110 Processor Interface - Register Access and SDRAM Interfacing		
A<25:0>	I/O	26-bit system address bus. Bits A<24:10> for SDRAM (output): setup 3ns, hold 1ns referenced to SDCLK. Bits A<25>, A<9:0> are functional test only.
D<31:0>	I/O	For SDRAM writes (output): setup 3ns, hold 1ns referenced to SDCLK
DQM<3:0>	I/O	For SDRAM writes (output Byte En): setup 3ns, hold 1ns referenced to SDCLK For register and PCMCIA and CF accesses (input): TBD
MBGNT	I	Input only; for DMA access
MBREQ	O	Output only; Rise and Fall times: min 1ns, max 5ns (30 pF load)
nSDCAS	O	For SDRAM (output): setup 3ns, hold 1ns referenced to SDCLK
nCS	I	Input only; for register access
nSDCS/nRAS	O	Chip Select output for SDRAM: setup 3ns, hold 1ns referenced to SDCLK
nSDRAS	O	For SDRAM (output): setup 3ns, hold 1ns referenced to SDCLK
nWE	I/O	For SDRAM (output): setup 3ns, hold 1ns referenced to SDCLK
RDY	O	Output only; Rise and Fall times: min 1ns, max 5ns (30 pF load)
SDCLK	O	Rising edge is timing reference point for all SDRAM signals Rise and Fall times: min 1ns, max 5ns (40 pF load)
USB Interface		
USB_MINUS	I/O	USB_PLUS and USB_MINUS pins, as outputs, must meet USB rev. 1.1 specification AC and DC requirements under specified load conditions
USB_PLUS	I/O	
AC-link Serial Port for Audio/GPIO_C Bits		
SYS_CLK	O	See I2S standard for rise/fall times and loading
Miscellaneous Signals		
INT	O	Standard CMOS output, point-to-point, max loading 30 pF

9. Absolute Maximum Ratings: Section 13.2.2

Values need to be added for the following table.

Table 13-4. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Note
V_{IP}	Voltage applied to any pin	TBD V	TBD V	1
T_S	Storage temperature	–20°C (–4°F)	+125°C (257°F)	1

NOTE: These are stress SA-1111 ratings only. Exceeding the absolute maximum ratings may permanently damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability.

10. DC Operating Conditions: Section 13.2.4

Values need to be added for the following table and a note was added to the first two rows. The table now appears as follows:

Table 13-6. SA-1111 DC Operating Conditions

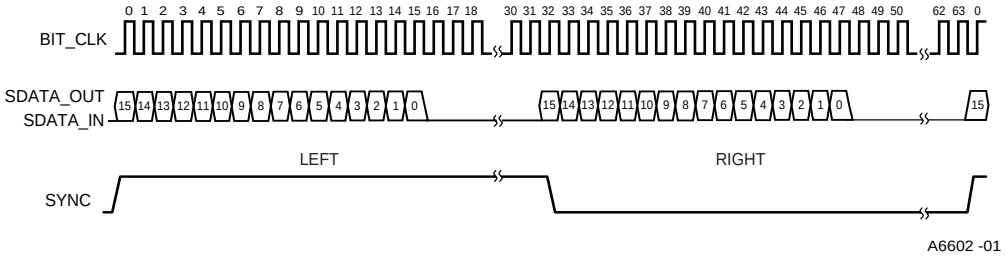
Symbol	Parameter	Minimum	Nominal	Maximum	Note
V_{OHC}	Output high 3.3V CMOS voltage	TBD V	—	TBD V	1
V_{OLC}	Output low 3.3V CMOS voltage	TBD V	—	TBD V	1
I_{OHC}	High level output current	—	—	TBD MA	—
T_A	Ambient operating temperature	0°C (32°F)	—	70°C (158°F)	—
I_{IN}	IC input leakage current	—	TBD µA	—	—
C_{IN}	Input capacitance	—	TBD pF	—	—
ESD	HBM model ESD	—	TBD KV	—	—

NOTES:
1. Drivers for address bits 25 and 9:0 are only driven to prevent bus float and will not meet these specifications at 4 ma.
2. Voltages measured with respect to VSS.
3. I – CMOS-level inputs (includes I and I/O pin types).
4. O – Output, CMOS levels, tristateable.

11. I²S and MSB-Justified Serial Audio Formats: Section 7.3.2.2

Update Figure 7-4 MSB-Justified Data Formats (16-bits). Figure 7-4 now appears as follows:

Figure 7-4. MSB-Justified Data Formats (16 bits):



12. Doze Mode: Section 2.4.2

Update 5th bullet for SCLK description. The bullet now appears as follows:

- SCLK
  The clock for the SSP Serial Controller, which typically ranges from 8KHz to 2 MHz. Selectively switching it on or off allows powering down of the Serial Controller.

13. External Interface to SSP, SPI, or Microwire Peripherals: Section 8.1.1

Modify the direction for SCLK in Table 8-1. The table now appears as follows:

Table 8-1. External Interface to Codec

Name	Direction	Description
SCLK	O (SSP mode)	Serial bit-rate clock
SFRM	O (SSP mode)	Frame indicator
TXD	O (SSP mode)	Transmit Data (serial data out)
RXD	I (SSP mode)	Receive Data (serial data in)