88SE9130 R3.0

One-Lane PCIe 2.0 to 3 or 6 Gbps SATA RAID I/O Controller

Datasheet

Doc No. MV-S107576-U0 Rev. C

August 3, 2018

Document Classification: Public

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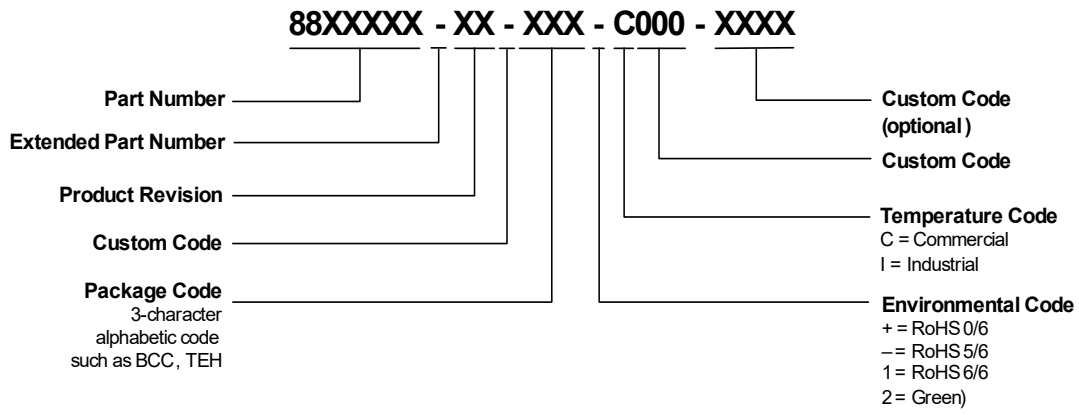
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE9130 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



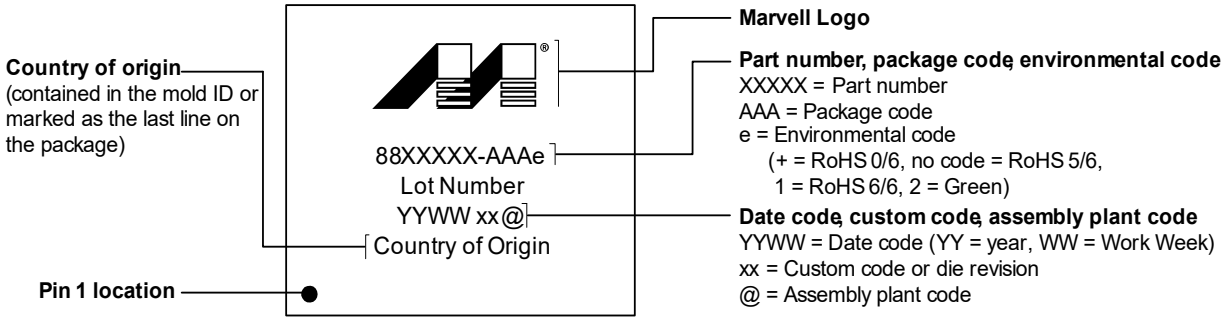
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SE9130C0-NAA2C000	76-pin QFN 9 mm × 9 mm, two 6 Gbps SATA ports.

The next figure shows a typical Marvell package marking.

88SE9130 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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88SE9130 Revision Notice

R3.0 (C0)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
1	General	ID	Updated the default values of REVID_F0 (R008h/R0008h [7:0]) from 12h (R2.2) to 20h (R3.0).	Updated the default values of REVID_F0 (R008h/R0008h [7:0]) from 12h (R2.2) to 20h (R3.0).	Yes	Page 11-38	N/A
2	PCIe	Design Change	Added Index Data Pair (IDP) access support for AHCI registers in BAR5 and its SATA Capability (SATACAP),	Added Index Data Pair (IDP) access support for AHCI registers in BAR5 and its SATA Capability (SATACAP), as described in the *Serial ATA AHCI 1.3 Specification* (www.intel.com).	No	N/A	N/A
3	PCIe	Design Change	Added capability to log the LCRC and Sequence Number error.	Added capability to log the LCRC and Sequence Number error. This data is logged in the PCIe Correctable Error Status (R110h/R0110h)	No	Page 10-63	N/A
4	PCIe	Design Change	Increased from 16 to 255 the default number of the Fast Training Sequence (N_FTS) to be transmitted. The increase is meant to recover more reliably from the L0s state with a Root Complex.	Increased from 16 to 255 the default number of the Fast Training Sequence (N_FTS) to be transmitted. The increase is meant to recover more reliably from the L0s state with a Root Complex.	No	N/A	N/A
5	Reset	Fixed Issue	Fixed the power-on sequence issue	Fixed the power-on sequence issue Removed the power ramp-up sequence limitation for the power-on reset.	No	N/A	N/A
6	SATA	Fixed Issue	Fixed the hanging issue when Register D2H FIS has a CRC error and FIS_RX_EN (R118h/R198h [4]) is enabled.	Fixed the hanging issue when Register Devices to Host (D2H) FIS has CRC error and FIS_RX_EN (R118h/R198h [4]) is enabled. This issue caused an error in FIS forwarding and as a result could not be completed. This fix qualifies the FIS to be valid and able to forward.	No	N/A	N/A

R3.0 (C0) (continued)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
7	SATA	Fixed Issue	Fixed the error-handling issue for the SYNC Escape by the H2D non-Data FIS when the FIS-based switching is disabled.	Fixed the error handling issue for the SYNC Escape by Host to Device (H2D) non-Data FIS when the FIS-based switching is disabled. The HBA must set PxIS.IFS to 1 to mark the condition as fatal whenever a SYNC Escape by the device occurs on an H2D non-Data FIS.	Yes	N/A	N/A
8	SATA	Fixed Issue	Fixed the error-handling issue for the R_ERR response to the H2D non-Data FIS.	Fixed the error-handling issue for the R_ERR response to the Host to Device (H2D) non-Data FIS. The HBA must set PxIS.INFS to 1 when an R_ERR is received on an H2D non-Data FIS.	Yes	N/A	N/A
9	SATA	Fixed Issue	Fixed the error-handling issue for SYNC Escape by the device on an D2H non-Data FIS.	Fixed the error-handling issue for SYNC Escape by the device on an D2H non-Data FIS. The HBA must set PxIS.IFS to 1 to mark the condition as fatal whenever a SYNC Escape by the device occurs on an D2H non-Data FIS.	Yes	N/A	N/A
10	SATA for Port Multiplier	Fixed Issue	Fixed the issue in Port Multiplier application in which PxFBS.DWE is not updated correctly, FIS Based Switching is enabled and SYNC Escape by device occurs on H2D non-Data FIS.	Fixed the issue in Port Multiplier application in which PxFBS.DWE is not updated correctly, FIS Based Switching is enabled and SYNC Escape by device occurs on H2D non-Data FIS. The HBA must update PxFBS. DWE that the error occurs when FIS Based Switching is enabled and SYNC Escape by device occurs on H2D non-Data FIS.	Yes	N/A	N/A
11	SATA for Port Multiplier	Fixed Issue	Fixed the issue in Port Multiplier application in which the FIS Based Switching is enabled and sends SRST to a device port.	Fixed the issue in Port Multiplier application in which the FIS Based Switching is enabled and sends SRST to a device port. The other device port sends D2H FIS. The command Issue (CI) register is not updated correctly.	Yes	N/A	N/A

R3.0 (C0) (continued)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
12	SATA	Fixed Issue	Fixed the issue of PxIS.PCSstatus handling.	Fixed the issue of PxIS.PCS status handling. In Power Saving mode, a COMINIT receipt must be handled as a fatal error. After the PCS status bit is set, the controller halts the execution until the PCS is cleared by the software.	Yes	N/A	N/A
13	PCIe	Fixed Issue	Fixed the issue when the PCIe Root Complex accesses an AHCI register with a length of two Dwords.	Fixed the issue when the PCIe Root Complex accesses an AHCI register with a length of two Dwords. Per the AHCI specification, the HBA controller must allow two Dwords access from the PCIe RC.	No	N/A	N/A
14	PCIe	Fixed Issue	Fixed the RequesterID field issue.	Fixed the RequesterID field issue. The RequesterID field in the controller Read Request and Write Request does not follow the PCIe Function Number. Some of the host drivers may check the consistency between the RequesterID and the Function Number of the controller. If they do not match, the host drivers eventually stop running.	No	N/A	N/A
15	PCIe MAC	Fixed Issue	Fixed the MAC compliance issue in which the when Root Complex and Endpoint are on Gen2 and the host initiates the Link Disable, the MAC was unable to recover.	Fixed the MAC compliance issue in which the when Root Complex and Endpoint are on Gen2 and the host initiates the Link Disable, the MAC was unable to recover.	No	N/A	
16	PCIe	Fixed Issue	Fixed the PCIe data-corruption issue in which the Rx lane noise caused write pointer misorder.	Fixed the PCIe data-corruption issue in which the Rx lane noise caused write pointer misorder.	No	N/A	N/A
17	SATA	Fixed Issue	Fixed the SATA IDE mode issue when using PIO mode READ in which the data transfer count is not 8-byte aligned.	Fixed the of SATA IDE mode issue when using PIO mode READ in which the data transfer count is not 8-byte aligned.	No	N/A	N/A

R3.0 (C0) (continued)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
18	Registers	Design Change	Updated the bit position of MAX_FUNC_NUM (R30718h [7:0]).	Updated the bit position of MAX_FUNC_NUM (R30718h [7:0]) from [31:29] to [7:0]. No firmware impact if using SPI Autoload patch.	See description	Page 11-66	N/A
19	Registers	Design Change	Added an interrupt handling scheme.	Added an interrupt handling scheme. The default operation mode of the interrupt handling has been changed, and relies on SPI Autoload or driver patch to change the operation mode in order to be compatible with the system drives. Added PCIe Interrupt Control Register (R32008h). No firmware impact if using SPI Autoload patch.	See description	Page 11-67	N/A

Known Issues Not Fixed in R3.0 (C0)

Item	Component	Type	Summary	Description	Register Location	Specs Location
1	AHCI	Known Issue	The 88SE9130 does not set PxIS.IPMS when a FIS is received with an invalid Port Multiplier port field.	The 88SE9130 does not set PxIS.IPMS when a FIS is received with an invalid Port Multiplier port field. When a Port Multiplier is connected, if a FIS is received from a device, the 88SE9130 does not set PxIS.IPMS when the PMP field does not match what is expected. **Workaround:** None	N/A	N/A
2	AHCI	Known Issue	The 88SE9130 does not set PxCMD.CR to 1 in P:Idle.	The 88SE9130 does not set PxCMD.CR to 1 in P:Idle. The 88SE9130 does not set PxCMD.CR when PxCMD.ST = 1, PxTFD,STS.BSY = 0, and PxTFD.STS.DRQ = 0. The 88SE9130 sets PxCMD.CR when the internal state machine is not at IDLE state. **Workaround:** None.	N/A	N/A
3	AHCI	Known Issue	The 88SE9130 does not set PxIS.OFScorrectly when padding zero for odd words transfer.	The 88SE9130 does not set PxIS.OFScorrectly when padding zero for odd words transfer. When receiving one more word than indicated in the PRD table due to the padding requirement, 88SE9130 falsely sets PxIS.OFS. According to AHCI spec, HBA must not signal this as an overflow condition. **Workaround:** None.	N/A	N/A

Known Issues Not Fixed in R3.0 (C0) (continued)

Item	Component	Type	Summary	Description	Register Location	Specs Location
4	AHCI	Known Issue	The 88SE9130 does not set IS.IPS[x] correctly when GHC.IE is 0.	The 88SE9130 does not set IS.IPS[x] correctly when GHC.IE is 0. When GHC.IE is cleared, the 88SE9130 does not set IS.IPS[x] when Port[x] has one or more interrupt status (PxIS) bit set while the corresponding interrupt enable (PxIE) bits are set. **Workaround:** None.	N/A	N/A
5	AHCI	Known Issue	The 88SE9130 issues PMREQ when PxCMD.ICC is written 2h or 6h in P:NotRunning state.	The 88SE9130 issues PMREQ when PxCMD.ICC is written 2h or 6h in P:NotRunning state. • When PxCMD.ST is 0 and PxCMD.ICC is set to 2h, 88SE9130 issues PMREQ_P to the device. • When PxCMD.ST is 0 and PxCMD.ICC is set to 6h, 88SE9130 issues PMREQ_S to the device. According to SATA AHCI Specification Rev 1.3, PxCMD.ICC only affects when in P:Idle state while PxCMD.ST is 1. **Workaround:** None.	N/A	N/A
6	AHCI	Known Issue	The CAP.SAM bit is set to 1 when GHC.AE is read/write.	The CAP.SAM bit is set to 1 when GHC.AE is read/write. The CAP.SAM is set in the 88SE9130 but GHC.AE is read/write. According to SATA AHCI Specification Rev 1.3, when CAP.SAM is 1, AE must be read only. **Workaround:** None.	N/A	N/A

Known Issues Not Fixed in R3.0 (C0) (continued)

Item	Component	Type	Summary	Description	Register Location	Specs Location
7	AHCI	Known Issue	The PxCMD.SUD bit is cleared and read/write when CAP.SSS is 0h.	The PxCMD.SUD bit is cleared and read/write when CAP.SSS is 0h. According to SATA AHCI Specification Rev 1.3, when CAP.SSS is 0h, PxCMD.SUD must be read-only and the default value must be set to 1h. **Workaround:** None.	N/A	N/A
8	PCIE	Known Issue	The 88SE9130 does not generate MSI or INTA_Assert messages correctly if a previous interrupt cannot be cleared quickly enough.	The 88SE9130 does not generate MSI or INTA_Assert messages correctly if a previous interrupt cannot be cleared quickly enough. For some timing relationships between the host driver clearing interrupt registers of the HBA, and the HBA setting interrupt registers across the PCIe interface, any subsequent interrupt may not be asserted to the PCIe Root Complex. **Workaround:** Program INTR_MODE (R32008h [22]) to 1h through SPI Autoload in order to eliminate this compatibility issue between the host drivers and devices.	Page 11-67	N/A

R2.2 (B2)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
1	General	ID	Changed the default values of REVID_F0 (R008h/R0008h [7:0]) and REVID_F1 (R008h/R1008h [7:0]) from 11h (R2.1) to 12h (R2.2).	Changed the default values of REVID_F0 (R008h/R0008h [7:0]) and REVID_F1 (R008h/R1008h [7:0]) from 11h (R2.1) to 12h (R2.2).	No	N/A	N/A
2	SATA IDE Controller	Fixed issue	Fixed the PRD address handling issue that caused the format problem in Windows XP.	Fixed the PRD address handling issue for the SATA IDE controller. This issue causes the Windows XP disk format and OS installation to fail when using the in-box PCI-IDE driver.	No	N/A	N/A
3	SATA IDE Controller	Fixed issue	Fixed the issue that caused the bus master interrupt INT_BM_1 (R02h [2]) to clear after reading the status register.	Fixed the issue that caused the bus master interrupt INT_BM_1 (R02h [2]) to clear after reading the status register. In the R2.2, the bus master interrupt is unchanged after reading the status register.	No	N/A	N/A

R2.1 (B1)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
1	General	ID	Changed the default values of REVID_F0 (R008h/R0008h [7:0]) and REVID_F1 (R008h/R1008h [7:0]) from 10h (R2.0) to 11h (R2.1).	Changed the default values of REVID_F0 (R008h/R0008h [7:0]) and REVID_F1 (R008h/R1008h [7:0]) from 10h (R2.0) to 11h (R2.1).	No	N/A	N/A
2	AHCI	Fixed issue	Fixed the interrupt generation that was incompliant with the AHCI standard and the Microsoft in-box AHCI driver.	Fixed the interrupt generation that was incompliant with the AHCI standard and the Microsoft in-box AHCI driver. Changed the interrupt generation from edge triggered to level triggered.	Yes	N/A	N/A

R2.1 (B1) (continued)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
3	GPIO	Design change	Changed the design to force GPIO High-Impedance mode.	Changed the design to force the GPIO pins to High-Impedance mode (Open-Drain type) when the chip drives active-low activity signals to logic high. This allows voltages up to 5.0V to be supplied to the external LEDs that connect to the GPIO pins.	No	N/A	N/A
4	GPIO	Design change	Changed the polarity of GPIO5 and GPIO2.	Changed the polarity of GPIO5 and GPIO2 for sample-at-reset. This design change eliminates the need for external pull-down resistors for some applications.	No	N/A	N/A
5	PATA Interface	Design change	Modified the PATA interface timing.	Modified the HSTROBE duty cycle in UDMA 6 mode to improve compatibility with some IDE drives.	No	N/A	N/A

R2.1 (B1) (continued)

<table>
<tr><th>Item</th><th>Component</th><th>Type</th><th>Summary</th><th>Description</th><th>Firmware Impact?</th><th>Register Location</th><th>Specs Location</th></tr>
<tr><td>6</td><td>PCI Express Controller</td><td>Design change</td><td>Changed the PCI configuration to modify the Device ID of function 0 and function 1 according to subclass code values.</td><td>Changed the PCI configuration to modify the Device ID of function 0 DEVID_F0 (R000h [31:16]), SSDEVID_F0 (R02Ch/R002Ch [31:16]), and function 1 DEVID_F1 (R000h/R1000h [31:16]), SSDEVID_F1 (R02Ch/R102Ch [31:16]), according to the following subclass code table:
<table>
<tr><th>Product Number</th><th>SATA 6 Gbps Capable?</th><th>SATA Ports</th><th>Function 1 Device ID (IDE)</th><th>Function 0 Device ID (Subclass Code = AHCI/IDE)</th></tr>
<tr><td>88SE9028</td><td>No</td><td>2</td><td>91A4h</td><td>9023h / 90A3h</td></tr>
<tr><td>88SE9128</td><td>Yes</td><td>2</td><td>91A4h</td><td>9123h / 91A3h</td></tr>
</table></td><td>Yes</td><td>N/A</td><td>N/A</td></tr>
<tr><td>7</td><td>PCI Express</td><td>Fixed issue</td><td>Fixed the directed speed change that caused some host chip sets to fail PCIe 5 Gbps negotiation.</td><td>Added a bootstrapping option on GPIO4 for selecting the PCIe 5 Gbps speed negotiation schemes. A value of 1h disables the directed speed change and 0h enables the directed speed change. This change makes GPIO4 an internal pull-up (PU).</td><td>No</td><td>N/A</td><td>N/A</td></tr>
<tr><td>8</td><td>PCI Express</td><td>Fixed issue</td><td>Fixed the ROM BAR enable bits ROMEN_F0 (R030h/R0030h [0]) and ROMEN_F1 (R030h/R1030h [0]) by changing the default value.</td><td>Changed the default value of ROMEN_F0 (R030h/R0030h [0]) and ROMEN_F1 (R030h/R1030h [0]) from 1h (enable) to 0h (disable).</td><td>No</td><td>N/A</td><td>N/A</td></tr>
</table>

R2.1 (B1) (continued)

Item	Component	Type	Summary	Description	Firmware Impact?	Register Location	Specs Location
9	SATA Controller	Fixed issue	Fixed the issue that occurs when using COMRESET for wake-up from Partial or Slumber modes.	Fixed the implementation of SATA Control (SControl/SCR2) (R12Ch/R1ACh) when the register is used to issue a COMRESET sequence but fails to trigger the SATA controller to wake-up from Partial or Slumber mode.	No	N/A	N/A
10	SATA Controller	Fixed issue	Fixed the implementation of SPD_SCR2 (R12Ch/R1ACh [7:4]).	Fixed the design to decode SPD_SCR2 (R12Ch/R1ACh [7:4]) as follows: **0h:** No speed negotiation restrictions. **1h:** Limit speed negotiation to a rate not greater than Generation 1 (SATA 1.5 Gbps) communication rate. **2h:** Limit speed negotiation to a rate not greater than Generation 2 (SATA 3.0 Gbps) communication rate. **3h:** Limit speed negotiation to a rate not greater than Generation 3 (SATA 6.0 Gbps) communication rate.	Yes	N/A	N/A
11	SATA Controller	Fixed issue	Fixed the issue that occurred when a new ATA command fails to trigger wake-up from Partial or Slumber mode.	Fixed the design issue that occurred when a new ATA command fails to trigger wake-up of the SATA Link Layer from Partial or Slumber mode into Active mode. This issue occurs only during Device Initiated Power Management (DIPM) mode.	No	N/A	N/A
12	SATA OOB	Design change	Changed the COMWAKE OOB qualification counter values.	Changed the default settings of the SATA OOB qualifier for received COMWAKE OOB and COMINIT OOB. This improves compatibility with some SATA drives.	No	N/A	N/A

CHANGE HISTORY

The following table identifies the document change history for Rev. C.

Document Changes *

Location	Type	Description	Date
Global	Update	Removed “preliminary” designation from titles and page headers.	April 4, 2018
Page 4-1	Update	Updated the following in Chapter 4, Layout Guidelines: The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design. to ***Note:*** *The information in this chapter is intended only to provide guidelines, and is not meant to restrict the customer from exercising discretion in implementing board designs. In cases where it is deemed necessary to deviate from the guidelines, Marvell recommends that customers consult with the Marvell FAEs to ensure that the performance of the Marvell product is not compromised.*	April 6, 2018

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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CONTENTS

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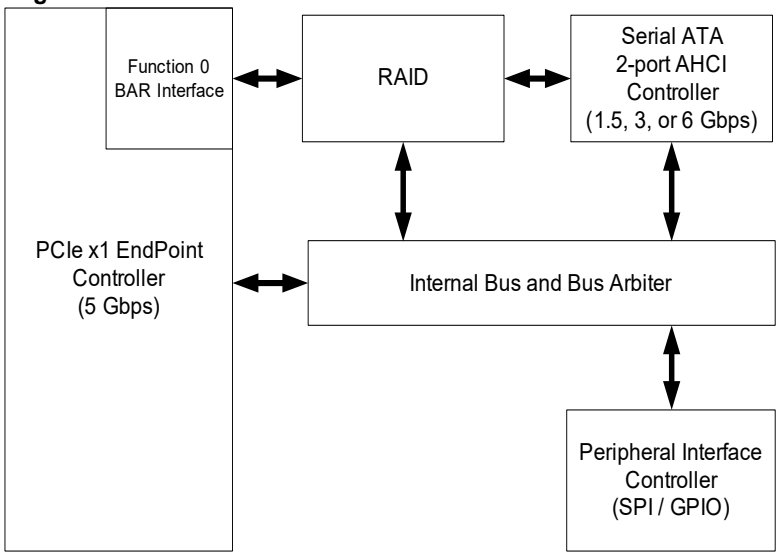
1 OVERVIEW

The 88SE9130 is a two-port, 3 Gbps or 6 Gbps SATA RAID I/O controller that provides a one-lane PCIe 2.0 interface. The 88SE9130 provides SATA controller functions. The 88SE9130 RAID I/O processor supplies two 6 Gbps SATA ports.

The 88SE9130 controller brings a high-performance 3 Gbps or 6 Gbps SATA RAID solution to desktop/consumer storage applications utilizing a one-lane PCIe 2.0 interface. The 88SE9130 supports devices compliant with the Serial ATA International Organization: Serial ATA Revision 3.0 specification. Figure 1-1 shows thesystem block diagram.

Figure 1-1 88SE9130 Block



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2 FEATURES

This chapter contains the following sections:

2.1 General

- 55 nm CMOS process, 1.0V digital core, 1.8V analog, and 3.3V I/O power supplies.
- An optional on-die regulator can be used with an external PNP bipolar device to generate a 1.0V supply to the chip from an 1.8V power source.
- Reference clock frequency of 25 MHz, provided by an external clock source or generated by an external crystal oscillator.

2.2 PCIe

- PCIe 2.0 endpoint device.
- Supports one lane.
- Compliant with PCIe 2.0 specifications.
- Supports communication speeds of 2.5 Gbps and 5.0 Gbps.
- Supports IDE programming interface registers for the SATA controller.
- Supports AHCI programming interface registers for the SATA controller.
- Supports aggressive power management.
- Supports error reporting, recovery, and correction.
- Supports Message Signaled Interrupt (MSI).

2.3 SATA Controller

- Compliant with Serial ATA Specification 3.0.
- Supports communication speeds of 6.0 Gbps, 3.0 Gbps, and 1.5 Gbps.
- Supports programmable transmitter signal levels.
- Supports Gen 1i, Gen 1x, Gen 2i, Gen 2m, Gen 2x, and Gen 3i.
- Supports two SATA ports.
- Supports AHCI 1.0 and IDE programming interface.
- Supports Native Command Queuing (NCQ).
- Supports Port Multiplier FIS-based switching or command-based switching.
- Supports Partial and Slumber Power Management states.
- Supports Staggered Spin-up.

2.4 SPI Interface Controller

- A four-pin interface provides read and write access to an external SPI flash or SPI ROM device.
- Vendor-specific information stored in the external device is read by the controller during the chip power-up.
- PCI BootROMs of PCIe function 0 can also be stored in the external SPI device and read through the Expansion ROM BAR and the SPI interface controller

2.5 Peripheral Interface Controller

- Six General Purpose I/O (GPIO) ports.
  - Each of the six GPIO pins can be assigned to act as a general input or output pin.
  - Each of the GPIO inputs can be programmed to generate an edge-sensitive or a level-sensitive maskable interrupt.
  - Each of the GPIO outputs can be programmed for a connected LED to blink at a user-defined fixed rate. The default rate is 100 ms.

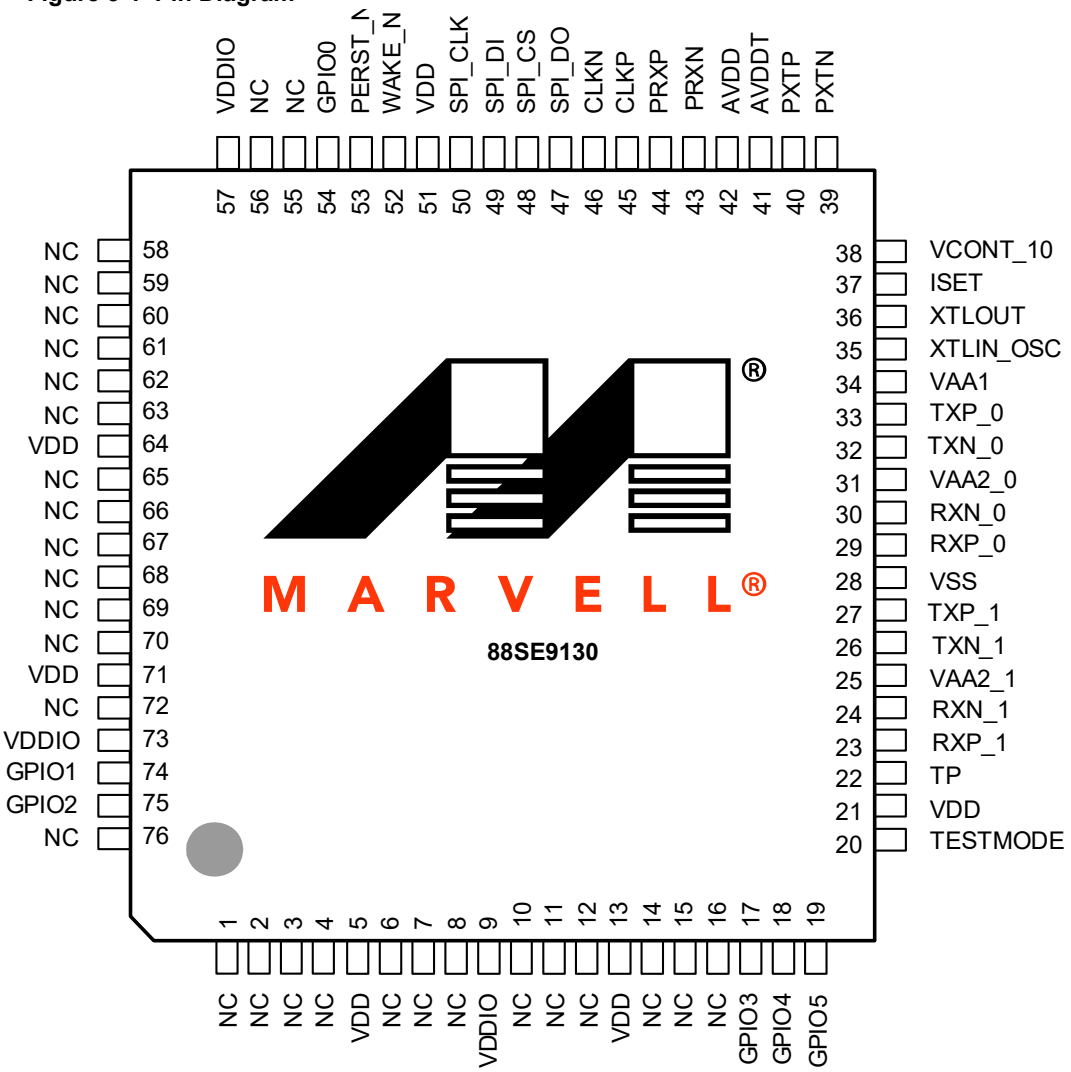
3 PACKAGE

This chapter contains the following sections:

3.1 Pin Diagram

The 76-pin QFN pin diagram is illustrated in Figure 3-1.

Figure 3-1 Pin Diagram

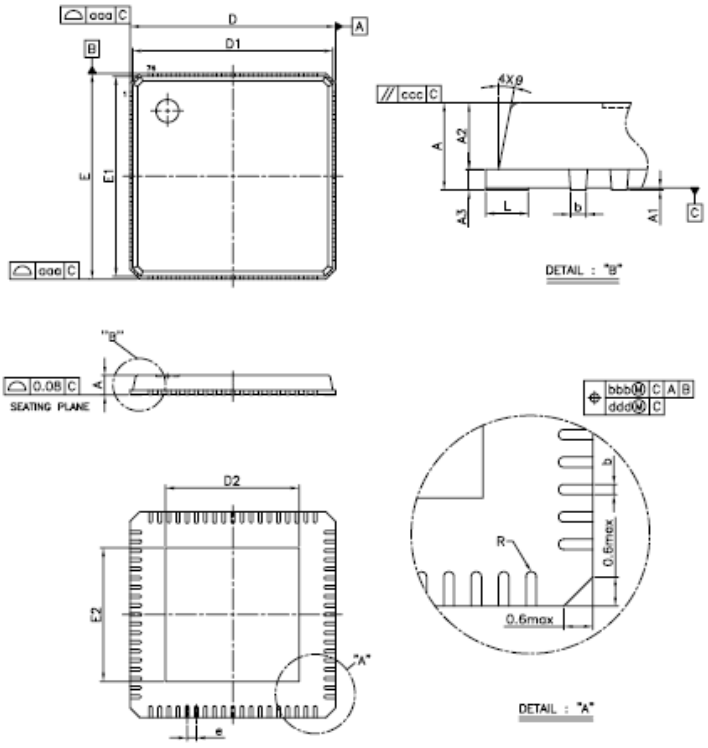


Note: The center area beneath the chip is the Exposed Die Pad (Epad). When designing the PCB, create a solder pad for the Epad and connect the Epad to ground.

3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2.

Figure 3-2 Package Mechanical Diagram



The package mechanical dimensions are shown in Figure 3-3.

Figure 3-3 Package Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
E	9.00 BSC			0.354 BSC		
E1	8.75 BSC			0.344 BSC		
e	0.40 BSC			0.016 BSC		
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
chamfer	---	---	0.60	---	---	0.024

Exposed Die Pad Size / Lead length Options			
Option	Symbol	Dimension in mm	Dimension in inch
Option #2	D2	3.80 ± 0.20	0.150 ± 0.008
	E2	3.80 ± 0.20	0.150 ± 0.008
	L	0.40 ± 0.10	0.016 ± 0.004

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

Note: 88SE9130 uses the exposed die pad (Epad) size option # 2.

3.3 Signal Descriptions

This section contains the pin types and signal descriptions for the 88SE9130 package.

3.3.1 Pin Type Definitions

Pin type definitions are shown in Table 3-1.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
mA	DC sink capability (All ATA I/Os are 12 mA)
5	5V tolerance (All ATA I/Os are 5V tolerance)
A	Analog
PU	Internal pull-up
PD	Internal pull-down
OD	Open-drain pad

3.3.2 Signal Descriptions

This section outlines the 88SE9130 pin descriptions. All signals ending with the letter N indicate an active-low signal.

Table 3-2 PCIe Express Interface Signals

Signal Name	Signal Number	Type	Description
PERST_N	53	5, I, PU	PCIe Platform Reset. Active low, indicates when the applied power is within the specified tolerance and stable.
WAKE_N	52	5, O, OD	PCIe Wake-up. An open-drain, active low signal that is driven low by a PCIe Express function to reactivate the PCIe Express Link hierarchy's main power rails and reference clocks.+ ***Note:*** *Do not connect to this pin. 88SE9130 does not support this function.* ***Note:*** *For applications that support a wake-up function, connect this pin to the WAKE# signal of a PCIe Express card slot or system board. Connect an external pull-up resistor from the PCIe Express card slot or system board to the 3.3V auxiliary supply. For applications that do not support a wake-up function, keep the WAKE_N pin on the 88SE9130 open.*

Table 3-2 PCIe Express Interface Signals (continued)

Signal Name	Signal Number	Type	Description
CLKP	45	I, A	PCIe Reference Clock of 100 MHz.
CLKN	46		
PRXP	44	I, A	PCIe Express differential signals to the controller's receiver.
PRXN	43		
PTXP	40	O, A	PCIe Express differential signals from the controller's transmitter.
PTXN	39		

Table 3-3 Serial ATA Interface Signals

Signal Name	Signal Number	Type	Description
TXN_0	32	O, A	Serial ATA Transmitter Differential Outputs.
TXP_0	33		
TXN_1	26		
TXP_1	27		
RXP_1	23	I, A	Serial ATA Receiver Differential Inputs.
RXN_1	24		
RXP_0	29		
RXN_0	30		

Table 3-4 Reference Signals

Signal Name	Signal Number	Type	Description
ISET	37	I/O, A	Reference Current for Crystal Oscillator and PLL. This pin has to be connected to an external 6.04 kΩ +/-1% resistor to Ground.
XTLOUT	36	O, A	Crystal Output.
XTLIN_OSC	35	I, A	Reference Clock Input. This signal can be from an oscillator, or connected to a crystal with the XTLOUT pin. The clock frequency must be 25 MHz ± 80 ppm.

Table 3-5 General Purpose I/O Signals

Signal Name	Signal Number	Type	Description
GPIO0	54	5, I/O, 12 mA, PU	General Purpose I/O.
GPIO1	74		
GPIO2	75		
GPIO3	17		
GPIO4	18		
GPIO5	19		

Table 3-6 SPI Flash Interface Signals

Signal Name	Signal Number	Type	Description
SPI_CLK	50	5, O, 12 mA	SPI Interface Clock.
SPI_DI	49	5, I, PU	Serial Data In. Connect to the serial flash device's serial data output (DO).
SPI_CS	48	5, O, 12 mA	SPI Interface Chip Select.
SPI_DO	47	5, O, 12 mA	Serial Data Out. Connect to the serial flash device's serial data input (DI).

Table 3-7 Test Mode Interface Signals

Signal Name	Signal Number	Type	Description
TP	22	I/O, A	Analog Test Point for PCIe Express PHY, SATA PHY, crystal oscillator, and PLL.
TESTMODE	20	5, I, PD	Test Mode. Enables chip test modes.

Table 3-8 Power and Ground Pins

Signal Name	Signal Number	Type	Description
VCONT_10	38	O, A	Voltage Control. Output signal which is connected to the base of an external BJT component to generate a 1.0V supply from 1.8V.
VAA2_0	31	Power	Analog power.
VAA2_1	25		1.8V analog power supply for SATA PHY.

Table 3-8 Power and Ground Pins (continued)

Signal Name	Signal Number	Type	Description
VAA1	34	Power	Analog power 1.8V analog power for crystal oscillator, reference current generator, PLL, and internal voltage regulator.
AVDD	42	Power	Analog power.
AVDDT	41		1.8V analog power supply for PCIe PHY.
VDDIO	9	Power	I/O Power.
	57		3.3V analog power supply for digital I/Os.
	73		
VDD	5	Power	1.0V Core Digital Power.
	13		
	21		
	51		
	64		
	71		
VSS	28	Power	Ground. The main ground is the exposed die-pad (ePad) on the bottom side of the package.

Table 3-9 No Connect Signals

Signal Name	Signal Number	Type	Description
NC	1, 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 55, 56, 58, 59, 60, 61, 62, 63, 65, 66, 67, 68, 69, 70, 72, 76		No Connect

4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE9130. It is written for those who are designing schematics and printed circuit boards for an 88SE9130-based system. Whenever possible, the PCB designer must try to follow the suggestions provided in this chapter.

Note: The information in this chapter is intended only to provide guidelines, and is not meant to restrict the customer from exercising discretion in implementing board designs. In cases where it is deemed necessary to deviate from the guidelines, Marvell recommends that customers consult with the Marvell FAEs to ensure that the performance of the Marvell product is not compromised.

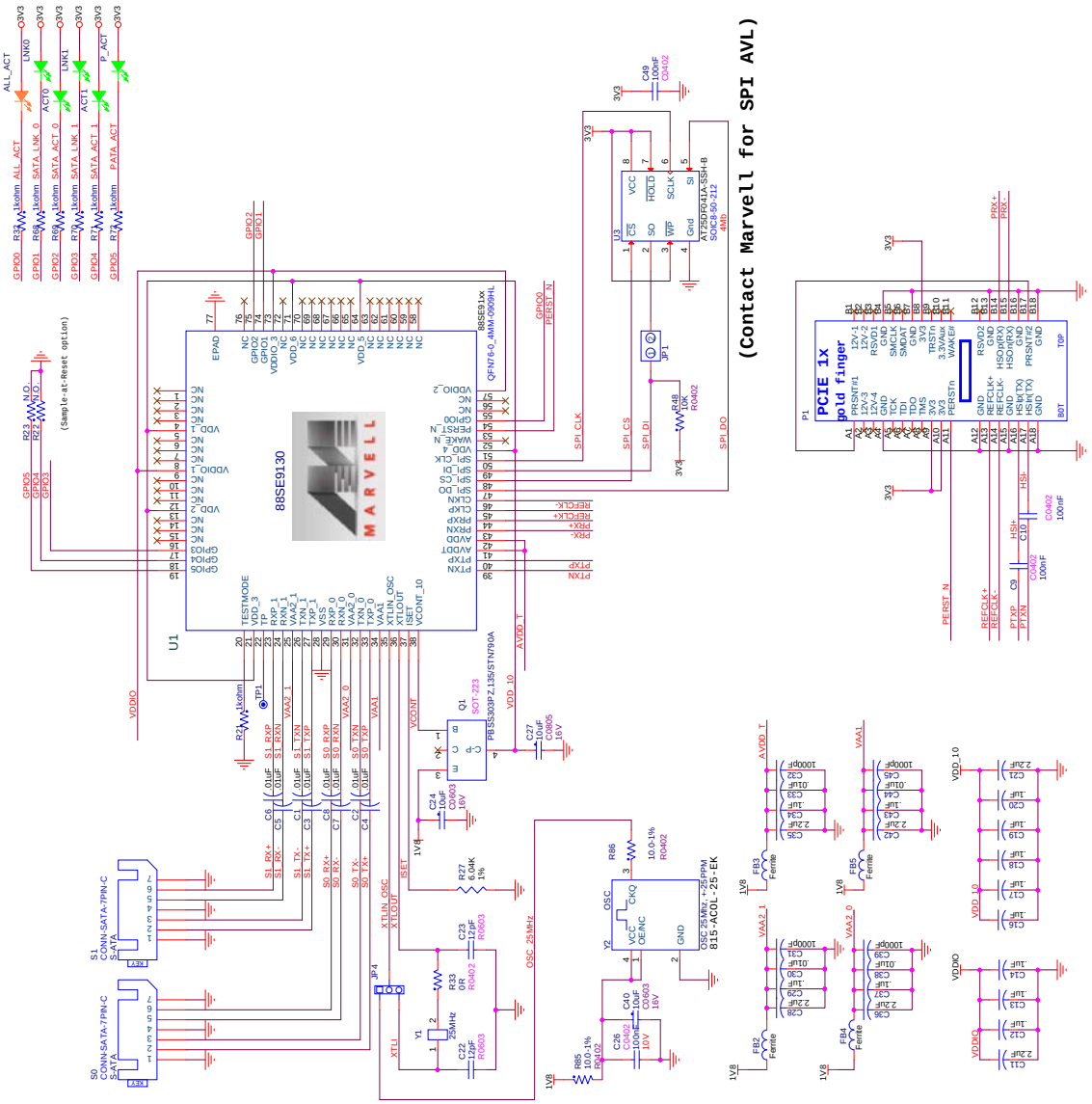
The chapter contains the following sections:

Refer to Chapter 3, Package, for package information.

4.1 Board Schematic Example

The board schematic consists of the major interfaces of the 88SE9130 including SATA and PCIe. Figure 4-1 shows an example board schematic.

Figure 4-1 88SE9130 Example Board Schematic



Note: Please contact your Marvell field applications engineer for the latest schematics.

4.2 External Voltage Regulator

The external voltage regulator consists of an external Bipolar Junction Transistor (BJT). The voltage level is on the VCONT_10 voltage control pin and it supplies VDD_10 to the core power. The collector of the BJT provides a stable voltage source and sufficient current to drive the 88SE9130.

The BJT's supply voltage, VAA, can use the same source as the 88SE9130's VAA1 or VAA2. The BJT and the internal regulator core forms a closed feedback loop to provide a stable voltage for VDD_10.

4.2.1 Recommended Components

For stability reasons, the loading capacitor on the collector output has a low Effective Series Resistance (ESR). The ESR is inversely proportional to the zero location. Table 4-1 describes the recommended components for the reference design.

Table 4-1 Component List

Symbol	Manufacturer	Part Number	Description
C1	Johansen Dialectrics	6R3R15X106KV4E	10 µF Tanceram Capacitor. • ESR of 20–50 mΩ at 1 MHz UGBW • High DC breakdown • Low DC leakage ***Note:*** *The second pole must be kept away from the UGBW because of parasitic RC inside the BJT.*
Q1	Phillips Semiconductor	PBSS5120T	Low V_{CESAT} PNP transistor.

4.2.2 External BJT Requirements

An h_{FE} of 200–400 is required when the BJT output current (IC) reaches its maximum, and low V_{CESAT} (about 200 mV at ICmax). The trace length between the BJT and the VCONT_10 pin of the 88SE9130must be less than 0.5 in. The control signal VCONT_10 connects to the base of the BJT. The PCB trace for the BJT and the load capacitor must be about 10 mils wide.

Regarding thermal characteristics, the mounting pad for the collector must be at least 1 cm^2 tin plated with single-sided copper. The typical power dissipation is approximately 0.5W for this BJT. Electrical requirements for the BJT are listed in Table 5-4, External BJT Requirements.

4.3 Layer Stack-up

The following layer stack up is recommended:

- Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane
- Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

5 mil traces and 5 mil spacing are the recommended minimum requirements.

4.3.1 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high speed signals.

4.3.2 Layer 2–Solid Ground Plane

A solid ground plane must be located directly below the top layer of the PCB. This layer must be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. No cutouts must exist in the ground plane. Use of 1 ounce copper is recommended.

4.3.3 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.3.4 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. Make sure there is no cut-out under the signal path.

4.4 Power Supply

The 88SE9130 operates using the following power supplies:

- VDD Power (1.0V) for the digital core
- Analog Power Supply (1.8V)

4.4.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 nF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The 2.2 µF ceramic decoupling capacitor is needed to filter the lower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors must be placed as close as possible to the channel VDD pins. At least one decoupling capacitor must be placed on each side of the IC package.

Short and wide copper traces must be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

4.4.2 Analog Power Supply (1.8V)

The PCIe analog supply provides power for the PCIe link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.4.3 Bias Current Resistor (RSET)

Connect a 6.04KΩ (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor must lie as close as possible to the ISET pin.

4.5 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-2.

Table 4-2 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power	1	N/A
4	Signal	0.5	50

4.6 Recommended Layout

Solid ground planes are recommended. However, special care must be taken when routing VAA and VSS pins.

The following general tips describe what must be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

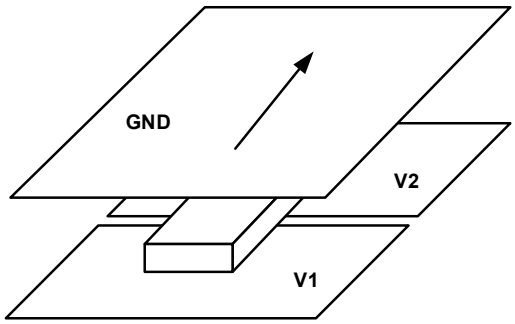
Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-2).
- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-2 Trace Has At Least One Solid Plane For Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals must avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.
- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.
- For dual strip-line routing, traces must only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes must be evenly distributed in order to minimize warping.
- Calculating or modeling impedance must be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.

- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.

- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces must not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-3). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.

  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-4).

  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-3 shows the ground layer close to the split power plane.

Figure 4-3 Close Power and Ground Planes Provide Coupling For Good Return Path

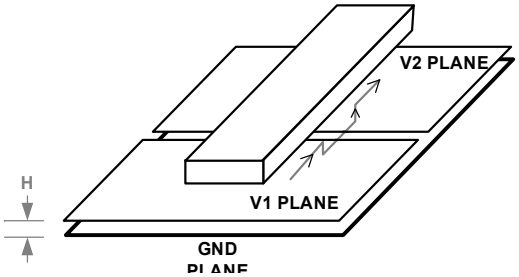
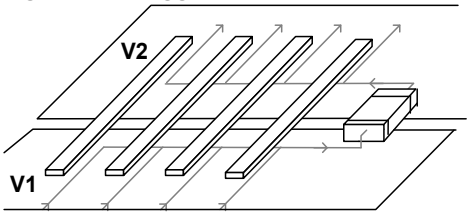


Figure 4-4 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-4 Suggested Thermal Ground Plane On Opposite Side of Chip



5 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

5.1 Absolute Maximum Ratings

Table 5-1 defines the absolute maximum ratings for the 88SE9130.

Table 5-1 Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Analog Power for PCIe PHY	$AVDD_{abs}$	-0.5	N/A	1.98	V
Absolute Analog Power for PCIe Tx	$AVDDT_{abs}$	-0.5	N/A	1.98	V
Absolute Analog Power for Crystal Oscillator and PLL	$VAA1_{abs}$	-0.5	N/A	1.98	V
Absolute Analog Power for SATA PHY	$VAA2\_0_{abs}$	-0.5	N/A	1.98	V
Absolute Analog Power for SATA PHY	$VAA2\_1_{abs}$	-0.5	N/A	1.98	V
Absolute Digital Core Power	VDD_{abs}	-0.5	N/A	1.21	V
Absolute Digital I/O Power	$VDDIO_{abs}$	-0.5	N/A	3.63	V

* Estimated values are provided until characterization is complete.

5.2 Recommended Operating Conditions

Table 5-2 defines the recommended operating conditions for the 88SE9130.

Table 5-2 Recommended Operating Conditions*

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY	$AVDD_{op}$	1.71	1.8	1.98	V
Analog Power for PCIe Tx	$AVDDT_{op}$	1.71	1.8	1.98	V
Analog Power for Crystal Oscillator and PLL	$VAA1_{op}$	1.71	1.8	1.98	V
Analog Power for SATA PHY	$VAA2\_0_{op}$	1.71	1.8	1.98	V
Analog Power for SATA PHY	$VAA2\_1_{op}$	1.71	1.8	1.98	V
Digital Core Power	VDD_{op}	0.95	1.0	1.21	V
Digital I/O Power	$VDDIO_{op}$	3.135	3.3	3.63	V
Internal Bias Reference	$ISET_{op}$	5.98	6.04	6.10	KΩ
Ambient Operating Temperature, Advanced Commercial	N/A	0	N/A	85	°C
Ambient Operating Temperature, Industrial†	N/A	-40	N/A	85	°C
Junction Operating Temperature, Advanced Commercial	N/A	0	N/A	125	°C
Junction Operating Temperature, Industrial†	N/A	-20	N/A	125	°C

* Estimated values are provided until characterization is complete.

† Engineering samples only. Estimated value provided until characterization is complete. Marvell does not have automotive or military qualification for industrial temperature versions of 88SE9130.

5.3 Power Requirements

Table 5-3 defines the power requirements for the 88SE9130.

Table 5-3 Power Requirements*

Parameter	Symbol	Maximum	Units
Analog Power for PCIe Transmitter	I_{AVDDT}	20	mA
Analog Power for PCIe PHY Transmitter	I_{AVDD}	70	mA
Analog Power for Crystal Oscillator and PLL	I_{VAA1}	10	mA
Analog Power for SATA PHY	I_{VAA2_0}	70	mA
Analog Power for SATA PHY	I_{VAA2_1}	70	mA
Digital Core Power	I_{VDD}	900	mA
Digital I/O Power	I_{VDDIO}	50	mA

* Estimated values are provided until characterization is complete.

5.4 Voltage Regulator Requirements

Table 5-4 defines the requirements for the external Bipolar Junction Transistor (BJT) used with the regulator core.

Table 5-4 External BJT Requirements*

Parameter	Symbol	Minimum	Typical	Maximum	Units
DC Current Gain of the BJT	h_{FE}	200	N/A	N/A	mA/mA
Collector-Emitter Saturation Voltage	V_{CEsat}	N/A	N/A	-200	mV
Power Dissipation of the BJT	P	N/A	N/A	500	mW
Equivalent series resistance of the capacitor	ESR	20	N/A	50	mΩ
Decoupling capacitor (ceramic)	C	10	N/A	N/A	µF

* Estimated values are provided until characterization is complete.

5.5 DC Electrical Characteristics

Table 5-5 defines the DC electrical characteristics for the 88SE9130.

Table 5-5 DC Electrical Characteristics*

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Input Low Level Voltage	V_{IL}	N/A	-0.4	N/A	0.25 × VDDIO	V
Input High Level Voltage	V_{IH}	N/A	0.8 × VDDIO	N/A	5.5	V
Output Low Level Current	I_{OL}	V_{PAD} = 0.4V	5	N/A	N/A	mA
Output High Level Current	I_{OH}	V_{PAD} = VDDIO – 0.4V	5	N/A	N/A	mA
Pull Up Strength	I_{PU}	V_{PAD} = 0.5 × VDDIO	10	N/A	N/A	µA
Pull Down Strength	I_{PD}	V_{PAD} = 0.5 × VDDIO	10	N/A	N/A	µA
Input Leakage Current	I_{LK}	0 < V_{PAD} < VDDIO	N/A	N/A	10	µA
Input Capacitance	C_{IN}	0 < V_{PAD} < 5.5V	N/A	N/A	5	pF

* Estimated values are provided until characterization is complete.

5.6 Thermal Data

It is recommended to read the application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 5-6 provides the thermal data for the 88SE9130. The simulation was performed according to JEDEC standards.

Table 5-6 shows the values for the package thermal parameters for the 76-lead Quad Flat Non-Lead package (QFN76) mounted on a four-layer PCB.

Table 5-6 Package Thermal Data

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient	29.9 C/W	26.6 C/W	25.5 C/W	24.8 C/W
Ψ_{JT}	Thermal characterization parameter: junction to top center	0.63 C/W	N/A	N/A	N/A

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