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TECHNICAL UPDATE
DEVELOPMENT TOOLS
MC68HC705JICS

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TECHNICAL UPDATE
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ICS05J1A

ICS05J1A Software

HC705JICS

Revision History

Date	Revision	Description
7/20/95	1.00	Includes tracker HC705JICS.001.

ICS05J1A Version 1.00 Bug List

Reference Document: Not applicable

Tracker Number: HC705JICS.001 Revision: 1.00

The bugs found in ICS05J1A version 1.00 have been corrected, and version 1.01 includes the changes. Version 1.01 can be found on the CSIC bbs through the following channels:

- WorldWideWeb: Set browser to URL:http:// freeware.aus.sps.mot.com/ and access the "68HC705J1A design contest" hotlink, then acces the "new release" hotlink.
- FTP: ftp to freeware.aus.sps.mot.com and get the file /pub/ 68hc05j/jics_101.zip.
- Dialup: Call (512)891-FREE, log onto CSIC bbs, go to 68hc05j directory of the files area and download the file jics_101.zip.

ICS05J1A version 1.00 bug list:

1. An asterisk (*) is not recognized as a parameter, but should be recognized as the address of the current opcode.
2. When LISTON and ZOOM commands are used together, the registers are displayed twice while stepping.

3. A command line parameter for COM port that is invalid locks the system.
4. Incorrect handling of PORTA interrupts. In this version, while interrupts are set to be positive-edge only and while one port A pin is held high, other port A pins transitioning to high can cause an interrupt. Normal operation is for one high PORTA interrupt pin to mask others because of the wired-OR architecture.
5. Clearing the IRQE bit in ISCR does not disable external interrupts.
6. If a parameter is used with the RESETGO command, the execution starts at that parameter. Execution should always start at the reset vector.
7. An external interrupt does not exit stop mode.
8. While executing code, a stop opcode exits to the debug window if ithe PC is hooked to the POD. The ICS05J1A should give a stop mode indicator and not return to the debug window prompt.
9. The verify command gives false positives.

CASM5J1A

CASM5J1A Software

HC705JICS

Revision History

Date	Revision	Description
7/20/95	1.00	Includes tracker HC705JICS.002.

CASM5J1A Version 1.00 Bug List

Reference Document: Not applicable

Tracker Number: HC705JICS.002 Revision: 1.00

The bugs found in CASM5J1A version 1.00 have been corrected, and version 1.01 includes the changes. Version 1.01 can be found on the CSIC bbs through the following channels:

- WorldWideWeb: Set browser to URL:http://freeware.aus.sps.mot.com/ and access the "68HC705J1A design contest" hotlink, then acces the "new release" hotlink.
- FTP: ftp to freeware.aus.sps.mot.com and get the file /pub/68hc05j/jics_101.zip.
- Dialup: call (512)891-FREE, log onto CSIC bbs, go to 68hc05j directory of the files area and download the file jics_101.zip.

CASM5J1A version 1.00 bug list:

1. The TIMER reserved label is not recognized by the assembler.

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Order this document by
MC68HC705J1AAD/D

SEMICONDUCTOR TECHNICAL DATA

Addendum to
MC68HC705J1A
HCMOS Microcontroller Unit
Technical Data

This addendum provides a correction and addition to the *MC68HC705J1A Technical Data* (Motorola document number MC68HC705J1A/D).

1. Page 4-5, **Figure 4-3. IRQ Status and Control Register** — Change as follows:

From:

		Bit 7	6	5	4	3	2	1	Bit 0
ISCR $000A	Read:	IRQE	0	0	IRQF	0	0	0	0
	Write:				R			IRQR	
	Reset:	1	0	0	0	0	0	0	0

= Unimplemented R = Reserved for factory test

Figure 4-3. IRQ Status and Control Register

To:

		Bit 7	6	5	4	3	2	1	Bit 0
ISCR $000A	Read:	IRQE	0	0	0	IRQF	0	0	0
	Write:				R			IRQR	
	Reset:	1	0	0	0	0	0	0	0

= Unimplemented R = Reserved for factory test

Figure 4-3. IRQ Status and Control Register

2. Page 4-6, section **4.6.2 Optional External Interrupts (PA0 through PA3)** — Add the following note:

NOTE: The $\overline{IRQ}$ pin has an internal Schmitt trigger. The optional external interrupts (PA0–PA3) do not have internal Schmitt triggers.

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