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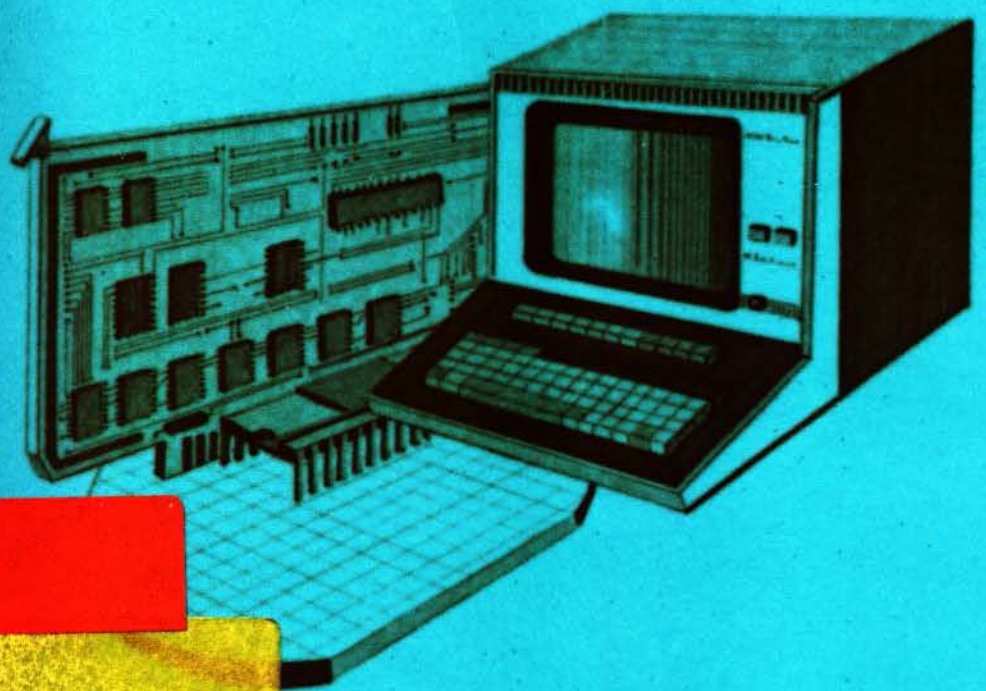

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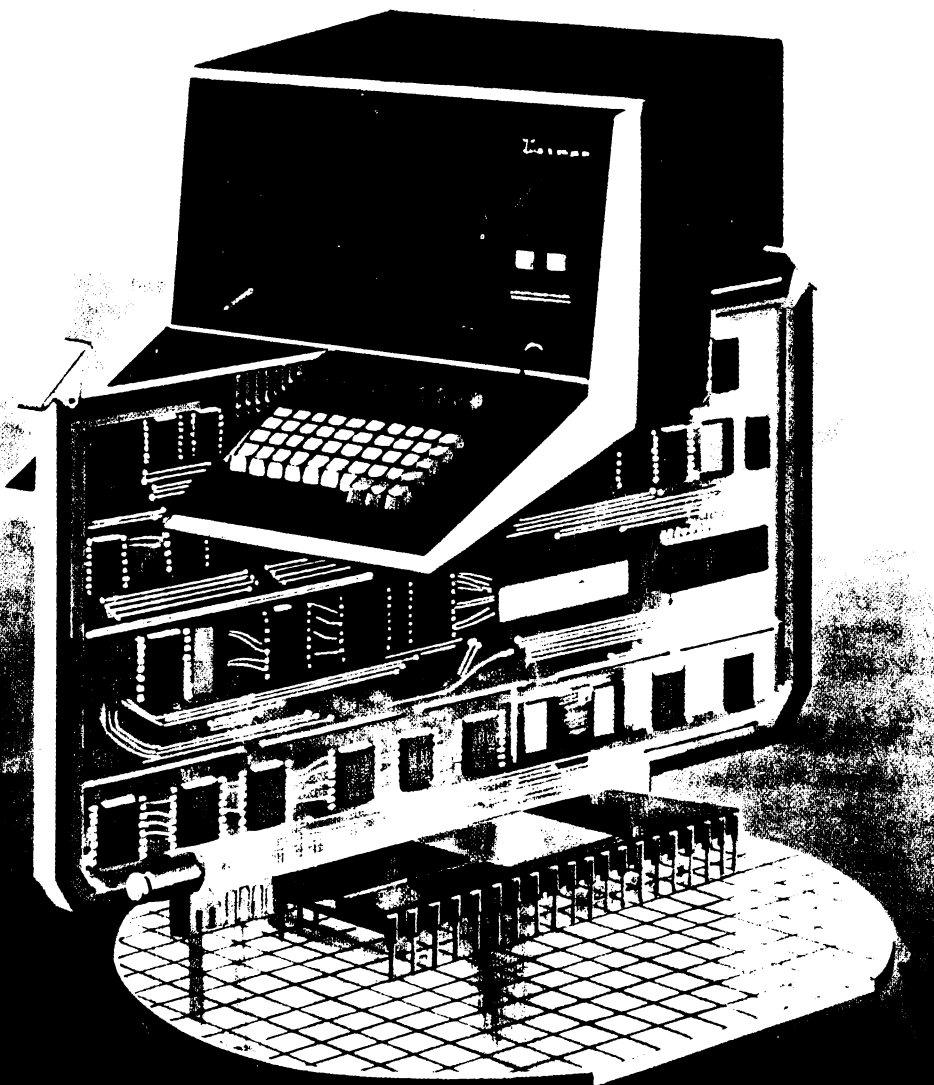

Instrumentation For System Design • Subsystems For System Implementation

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Here's what Motorola brings to your microcomputer

THE COMPONENTS

Starting your microcomputer system

Start with the chip set that precisely meets your design objective. Motorola manufactures the industry's most complete selection of solid-state microcomputer components to give you the performance you need and the design flexibility you want—

At A Glance...

Choice of . . .
Processing Capability
1-bit, 4-bit, 8-bit, 16-bit

Choice of . . .
Technology
NMOS, CMOS, TTL, ECL

Choice of . . .
Performance
Medium Speed, High Speed

Choice of . . .
Chip Complements
Multi-Chip applications versatility, Single-Chip applications simplicity

For Maximum Versatility . . .
The M6800 Microcomputer System — an NMOS system that is rapidly becoming an industry favorite. Start with the basic MC6800 8-bit Microprocessor and supplement it with just the right MSI/LSI support chips you need (I/O, memory, etc.) to optimize your final design . . .

Or — choose the MC6802/MC6846 combination that provides complete microcomputer performance with just two chips . . .

Or — go with the MC6801, a powerful microcomputer on a single chip that is, nevertheless, expandable with all M6800 support chips, should the need arise.
And, when even greater throughput is desired, choose the MC6809—an 8-bit processor with 16-bit internal processing capability.

For Dedicated Applications . . .
Two complete, single-chip microcomputers that could provide the simplest solutions to complex problems:

The MC3870 — an 8-bit NMOS system, that is ideal for low-cost, high-volume requirements;

The MC141000 Family — a 4-bit CMOS system for equipment demanding extremely low power requirements.

Where High Speed Counts . . .
Two bipolar 4-bit slice families composed of LSI components designed for microprogrammable computer implementation of any desired complexity.

The M2900 Family — a Schottky TTL system with a clock frequency range of 8.3 to 9.5 MHz.

The M10800 Family — a MECL system offering highest speed operation with a system clock frequency range of 10 to 15 MHz.

Special for Industrial Control Applications . . .
When the required answer from a computer is simply a yes-or-no, on-or-off, high-or-low indication, as in many industrial control systems, the 1-bit CMOS MC14500B Industrial Control Unit may provide the ideal solution. It offers simple design, simple programming and reliable performance.
Whatever your system needs, Motorola has the chip set that matches your design goals, conveniently and cost-effectively.
For more complete details, ask your Motorola representative.

design party...

MICROSYSTEMS

Instrumentation for System Development

There are important differences between system-design with hardwired circuitry and designing with microprocessors. With hardwired, dedicated circuitry, once the necessary components have been functionally interconnected, the job is done; with microprocessors, when the hardware of the system has been defined, that is when the real design starts—the job of designing the program that turns a basic uneducated computer into a functional system dedicated to a specific task.

The key to developing a dedicated microcomputer system and, ultimately, to manufacture and service the system, is an umbrella of support hardware and software ranging from evaluation and development aids to manufacturing and service instruments. The Motorola MPU/MCU Product Family is already complemented with an array of such user-oriented development products, and additional systems are being implemented as quickly as technological advances permit. It is part of a systematic plan to keep Motorola microcomputer elements foremost on the "preferred product" list of the system designer.

Subsystems for System Implementation

If you implement a large number of systems with the same design, designing a microcomputer system with individual components often becomes the most practical way to maximize profits. But if the number of systems you need is small, the design costs could be exorbitant. That is when it pays to consider the use of Motorola Micromodules.

Micromodules are a series of up-to-date microcomputer subsystem boards, prewired and tested to yield complete systems with minimum additional design demands. Since they are produced in volume design costs are amortized over a significant production run. And since they come with a range of functional capabilities, they can give your system the characteristics it needs at a very competitive overall price.

At A Glance...

Choice of . . .

System Development Tools

An umbrella of support products that can be tailored to your system design needs . . . and your budget. Page 4

Choice of . . .

Software Support

Assembly language or high-level language, Motorola software lets you design and debug your system with dedicated design systems. Page 12

Choice of . . .

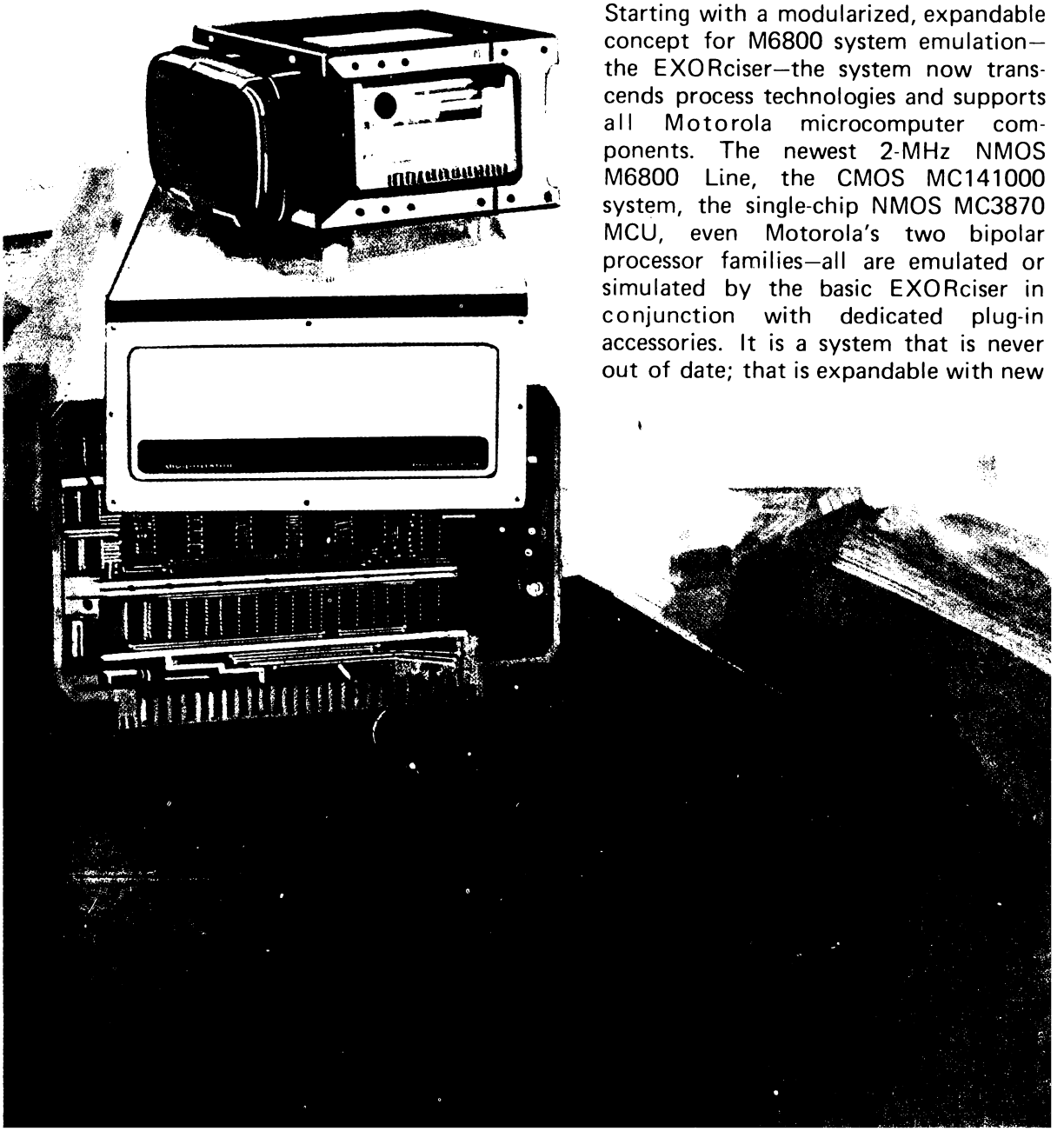
Modularized Microcomputer Subsystems

Multilevel subsystems, replete with peripherals, to let you start your hardware design at a higher level of componentry. Page 16

Choice of...

development systems

Motorola supports its various MPU/MCU lines with an array of hardware and software development systems that meets the wide range of customer needs. Starting with a modularized, expandable concept for M6800 system emulation—the EXORciser—the system now transcends process technologies and supports all Motorola microcomputer components. The newest 2-MHz NMOS M6800 Line, the CMOS MC141000 system, the single-chip NMOS MC3870 MCU, even Motorola's two bipolar processor families—all are emulated or simulated by the basic EXORciser in conjunction with dedicated plug-in accessories. It is a system that is never out of date; that is expandable with new



plug-in add-ons as quickly as new or improved component families are introduced; that offers unlimited flexibility at a modest cost.

Complementing the development systems is a selection of compatible peripherals—a series of dot-matrix printers, a keyboard entry/display terminal, a dual floppy disk storage system. Each is equipped with the appropriate interface circuitry that adapts it to the EXORciser and other Motorola development systems.

And Motorola facilitates the involved task of program development with a comprehensive software library of editors, assemblers, interpreters and compilers that provides the man/machine interface in a variety of languages. Assembly language—of course. But also available are "translators" that permit high-level language entry with MPL, FORTRAN, BASIC and COBOL.

At Motorola, product support development is a continuing large-scale effort that keeps pace with the development of the product itself.

At A Glance...

M6800 Development Systems:

EXORciser II, EXORciser I ..... for maximum versatility

EXORterm 220, EXORterm 200 ..... for program development

PDS family ..... for lowest cost

Add-On Accessories for Other MPU/MCU Lines:

EXOslice, MACE ..... for bipolar processors

MEX3870 ..... for NMOS 3870 Systems

MEX141000 ..... for CMOS 141000 Systems

Accessories for System Diagnosis and Manufacturing

Support Software:

Resident Software Options

System Peripherals:

EXORterm 150 ..... Display Terminal

EXORdisk II ..... Floppy Disk Storage System

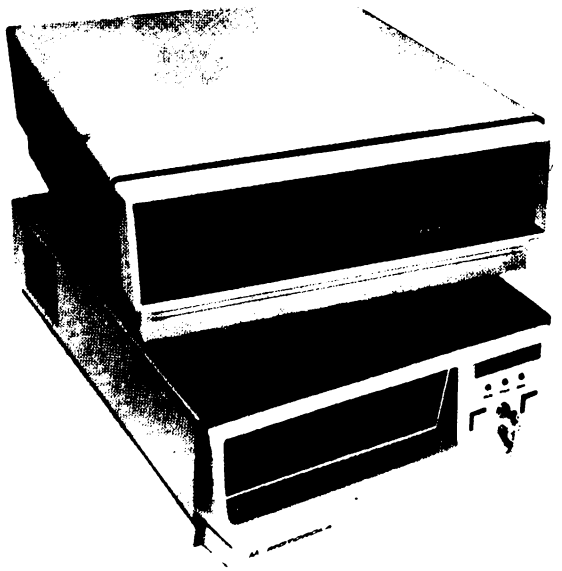
EXORprint ..... Dot-Matrix Printers

the EXORciser

To develop a computer, it takes a computer. One with even greater capacity than the system under development. The EXORciser is such a computer, developed expressly as a design, evaluation and diagnostic instrument for Motorola microcomputer systems.

Essentially, the EXORciser is an expandable "breadboarding" system that allows almost instantaneous emulation of any M6800-based microcomputer configuration, from the simplest to the most elaborate—and with optional accessories its powerful design and diagnostic functions can be extended to other Motorola microcomputer families as well . . . the popular NMOS MC3870 Microcomputer, the CMOS MC141000 Microcomputer and even the high-speed bipolar M2900 (TTL) and M10800 (MECL) systems. Built-in programming and diagnostic routines facilitate the development and debugging of dedicated programs for each.

Three versions of the EXORciser are currently available. Each consists of a cabinet with a built-in power supply, and a prewired bus-oriented motherboard with a basic complement of functional modules. Together, these form a complete development microcomputer, with the capability of adapting the unit to a specific design problem by adding optional interface circuitry or expanded memory capacity. The additional requirements are available as add-on modules, permitting the user to purchase as few, or as many, as needed for the anticipated end function(s) or the system(s) to be developed. Thus, the EXORciser is a system that is never out of date, being at all times upgradable as new and expanded microcomputer functions become available.

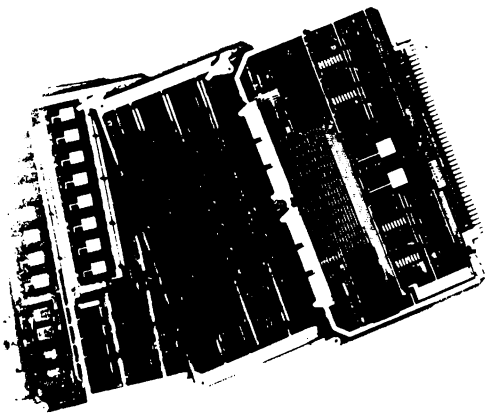


EXORciser II — Contains an MPU II module, and a Debug II module. The MPU module mounts the MC68B00 MPU, generating clock frequencies of 1.0, 1.5 and 2.0 MHz. This system, through its expanded Debug II capability, can operate in a "dual memory map" mode. This permits the debug programs to reside in an independent memory, leaving the full 64K memory capacity of the M6800 system available for the user's program. The motherboard has provisions for up to 12 add-on-plug-in assemblies so that a system of almost any complexity can be rapidly assembled.

EXORciser I — Earlier version of above, uses MPU I and Debug I modules. Useful for operating at frequencies up to 1 MHz, with only a single memory map. Provisions for up to 12 add-on modules.

...and its basic options

It might be convenient to own a single complete development system; on that would help design every microcomputer that might ever be required, from the smallest to the largest. But it would be expensive. That is why the EXORciser contains only the basic electronics that is required for all systems, regardless of size. The remaining circuitry—various interfaces, add-on memory, etc.—is offered as modular options, to be purchased when and if demanded by system design. This expandable feature assures maximum utility at low cost. It also guards against equipment obsolescence because new modules with greater capabilities are constantly being developed as the technology advances.
The Modules listed below expand the basic EXORciser capabilities for the development of microcomputer systems with M6800 type microprocessors. Add-ons for expansion of EXORciser capabilities to other MPUs and MCUs, and for even more sophisticated diagnostic functions, are described on subsequent pages.

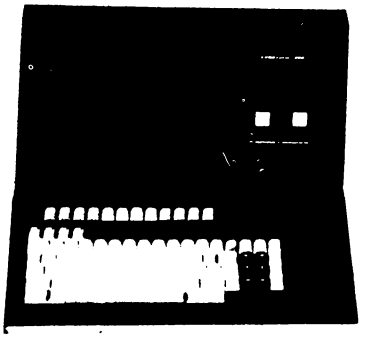


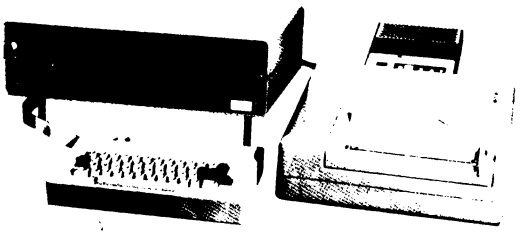
EXORciser Expansion Modules — All EXORciser II Modules will also operate with EXORciser I, but at a maximum frequency of 1 MHz.

For EXORciser 1 and EXORterm 200 (1 MHz frequency limit)	Function	For EXORciser II and EXORterm 220 (1, 1.5 and 2 MHz frequency)
	MEMORY ADD-ON	
M68MM06 MEX6812-1 M68MM09E2	2K Static RAM 2K Static RAM 2K CMOS RAM with battery	
M68MM09E4	4K CMOS RAM with battery	
MEX6815-3	8K Static RAM 8K Dynamic RAM	MEX6808-22
MEX6816-1HR MEX6816-1	16K Static RAM 16K Hidden Refresh RAM 16K Dynamic RAM	MEX6816-22S MEX6816-22D
MEX6832-1HR	32K Hidden Refresh RAM 32K Dynamic RAM	MEX6832-22
MEX6848-1HR	48K Hidden Refresh RAM 48K Dynamic RAM	MEX6848-22
MEX6864-1HR	64K Hidden Refresh RAM 64K Dynamic RAM	MEX6864-22
	I/O ADD-ON	
MEX6820	PIA Module with four 8-bit I/O ports for parallel-oriented peripherals	MEX6821-2
MEX6850	ACIA Module	MEX6850-2
	AUXILIARY MODULES	
MEX68PP3A/B/M	PROM Programmer	MEX68PP3A/B/M
MEX68USM	Universal Support Module to Support 6800 family of devices	MEX68USM
MEX68SA	Systems Analyser for Monitoring, Analyzing and trouble-shooting MC6800/MC6802 Microcomputer Systems	MEX68SA2
MEX68WW	Universal Wirewrap Module for prototype Development	MEX68WW
MEX68XT	Extender Module permits access to any development module from outside the EXORciser chassis	MEX68XT

development stations...

...and





The **EXORterm 200/220 Development Stations** add video display and keyboard entry facilities to the capabilities of the basic EXORciser/EXORciser II. They consist, fundamentally, of an integral card cage containing the EXORciser Debug Module and the MPU module. The cage has provisions for 6 more standard EXORciser modules, thereby providing considerable system design flexibility.

EXORterm 200/220 contains a high-quality CRT with a full 1920-character screen and easily readable 7 x 9 ASCII characters. A 59-key detachable keyboard incorporates 12 special keys encoded to invoke functions unique to a development system in each of its three command levels . . . DOS, EXbug and MAID. Its serial communications link uses speeds up to 9600 baud for information exchange.

The **Polyvalent Development System Family** provides an ideal first step into the world of microcomputer design. With its full ASCII keyboard, a 5" CRT Monitor displaying up to 16 lines of 64 characters, an audio-cassette interface for mass storage capability and a medium speed printer, it does not require any other terminal. A ROM resident Editor/Assembler and BASIC Interpreter is also available allowing sophisticated microcomputer applications development.

DEVELOPMENT SYSTEMS

Part Number	Name	Main Purpose	Firmware	MPU Module	Freq.	RAM	Included Options
M68TDS1	TDS1	Medium Size Software	Minibug 3E	SAC	921.6 kHz	8K	5" CRT, Keyboard, Kansas City Interface, Printer Interface, Editor/Assembler
M68TDS2	TDS2	Medium Size Software	Minibug 3E	SAC	921.6 kHz	8K	5" CRT, Keyboard, Kansas City Interface, Printer Interface, Editor/Assembler/Basic
M68TDS3	TDS3	Medium Size Software	Minibug 3E	SAC	921.6 kHz	16K	5" CRT, Keyboard, Kansas City Interface, Printer Interface, Editor/Assembler
M68TDS4	TDS4	Medium Size Software	Minibug 3E	SAC	921.6 kHz	16K	5" CRT, Keyboard, Kansas City Interface, Printer Interface, Editor/Assembler/Basic
M68SDTT2	EXORciser 1	Software/Hardware	EXbug 1.2	MPU	1 MHz	–	RS232/TTY Interface
M68SXS10200	EXORterm 200	Software	Exbug 1.2	MPU	1 MHz	-	12" CRT, Keyboard
M68SDTTU2B	Use EXORciser 1	Software/Hardware	EXbug 1.2	Use B	1 MHz	–	RS232/TTY Interface
M68SXS102B0	Use EXORterm 200	Software	EXbug 1.2	Use B	1 MHz	–	12" CRT, Keyboard
M68SDT2-2DM	EXORciser 2, Dynamic	Software/Hardware	EXbug 2	MPU2	2 MHz	32K Dyn	RS232 Interface
M68SDT2-2SM	EXORciser 2, Static	Software/Hardware	EXbug 2	MPU2	2 MHz	32K Stat	RS232 Interface
M68SDT2-2X	EXORciser 2	Software/Hardware	EXbug 2	MPU2	2 MHz	–	RS232 Interface
M68SXS2202	EXORterm 220	Software	EXbug 2	MPU2	2 MHz	–	12" CRT, Keyboard

non-6800 development systems

The modular concept of the EXORciser/EXORterm makes these ideal instruments for expansion as a development system for MPUs/MCUs other that the MC6800. For example:

The M6801 Support System

The problem—before you can get a simple-chip microcomputer from the factory, you must come up with the program that converts the chip into a functional microcomputer. The program is then built into the read-only memory portion of the components you receive.

The 6801 Support System is EXORciser/EXORterm compatible and is capable of operating with any of the existing M6800 modules, allowing the MC6801 software and hardware development in either the EXORciser I/II or EXORterm. The Support System consists of a control module, an extender cable terminated by a 40 pin male DIP plug and control software. This allows the user to evaluate and debug his own MC6801 system in either the single chip, expanded multiplexed or non-multiplexed mode, in real time (to be introduced).

The M6809 Support System

The same features are also available for the MC6809 microcomputer. The 6809 Support System is EXORciser/EXORterm compatible and also provides the user with USE (USER SYSTEM EVALUATOR) capability (to be introduced).

The M3870 Emulator

The MC3870 is a powerful, 8-bit, single chip Microcomputer (MCU) ideal for large-volume, dedicated applications.

The MEX3870M is a plug-in module that converts any one of the EXORcisers into a real-time MC3870 Emulator. That is, by means of equivalent hardware and associated software—an appropriate cross-assembler and an FBUG control and diagnostic program—it converts the EXORciser into a development system custom-tailored for the MC3870 microcomputer chip. The cross-assembler provides an object file (on disk) from the MC3870 source code which is loaded into the Emulator Module. Subsequently, the debug routine of FBUG permits examination and change in the instructions of the user's operating program. Then, when the program has been debugged, it can be loaded into ROM and plugged into an available socket on the Emulator, whereupon the board can be removed from the EXORciser and employed in the user's system to check out final system operation.

The MEX3870M includes the hardware module and the appropriate software and cross-assembler. Additional requirements for implementation include the MDOS, Editor and 24K bytes of memory.

The M141000 Simulator

What the MEX3870M does for the MC3870 NMOS MCU, the MEX141000M does for the MC141000/1200 CMOS MCU . . . it provides an EXORciser-based tool for debugging actual software configurations of the user's final system. The Simulator consists of a hardware module and an associated software package. Using the information generated by the Simulator, and the debug facilities provided by the Simulator, the user can find and correct problems in the source program. Thus, the Simulator offers an economical and expedient means for developing new applications prior to committing the programs to the final production masks.

The EXOslice Family

The EXOslice family, working with the EXORciser, provides the user with a mean of developping 2900 and 10800 4-bit slice Microcomputer systems.

The EXOslice family includes high speed expandable 1K x 32 bit MECL RAM modules for microcode storage, 16-input/32-output MECL modules and MECL-TTL adapter. A MECL PROM Programmer allows programming of MECL MCM10149 256 x 4 PROM devices. The FAST software provides a mean of dumping or loading user's files (configuration descriptions, microprogram) to and from several source or media (keyboard, papertape, cassette, diskette) and offers several debugging features for the user's microprogram.

MACE 29/800 – Microcode Analyzer and Control Storage Emulator

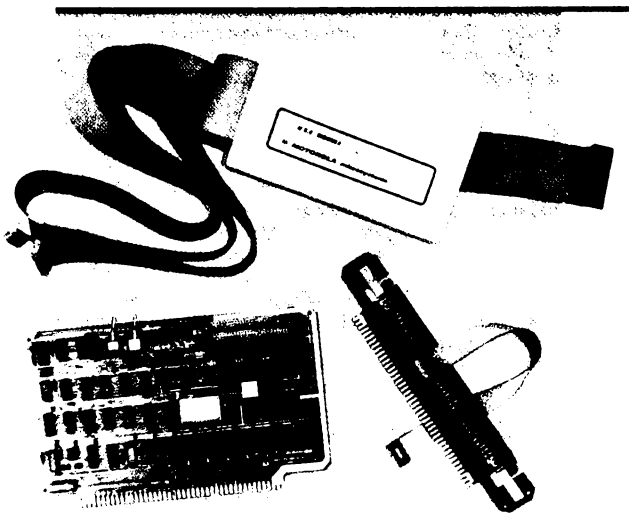
This development aid supports the bipolar M2900 TTL and M10800 MECL 4-bit slice systems. It is intended to minimize the time required to develop microcode for custom processors built with bit-slice components.

The MACE 29/800 provides Writable Control Storage (microprogram memory) and real-time microprogram diagnostic capabilities. Its chassis contains power supplies, a multilayer backplane, and a 10-slot card cage. PC modules containing the WCS, diagnostic, timing, control and interface hardware are mounted in the card cage, with adequate extra slots to house a user's prototype system. Alternatively the user's system may be developed externally, and interconnected with MACE via a cable interface system—or, the chassis may be used to house totally independent prototypes.

The MACE 29/800 is designed to work with the EXORciser which controls the system operation. All microprogramming tasks appear as M6800-oriented operations, with the necessary translation performed by a software package included with MACE. This takes advantage of the extensive hardware and software components that have been developed for the EXORciser, thereby reducing system cost.

accessories for system diagnosis... and

The EXORciser/EXORterms (and their basic options) are very versatile instruments for M6800 Microcomputer development. Through emulation of a user's system they take the guesswork out of hardware and software design. And with these additional modular options, they can be turned into complete, highly sophisticated post-design Centers.

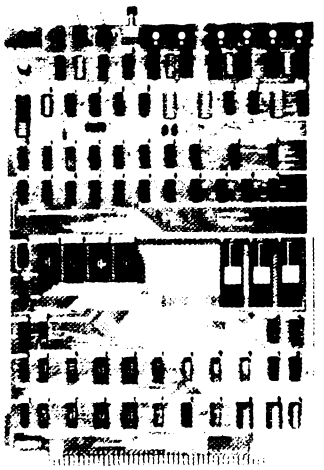


User System Evaluator (USEB) – MEX68USEB

The MEX68USEB module is a second-generation addition to the Options array. It not only permits complete emulation of an M6800 or M6802 Microcomputer system during design, it extends all the EXbug (diagnostic) functions into the user's prototype or final operating system.

USE consists of three assemblies—a Processor Module, an Intercept Module and a Cable and Buffer Assembly. The Processor Module is used in place of the MPU Module originally supplied with the EXORciser and permits the sharing of the EXORciser's inherent capabilities with the user's external system. The Cable and Buffer Assembly plugs into the MPU socket at the user's system and transfers control of the user's system operation to the EXORciser or EXORterm. The intercept Module adapts the system for mounting the optional Systems Analyzer for even greater diagnostic power.

The USE System may be pruchased to upgrade existing EXORcisers I and IA, or EXORterm 200, or these basic systems may be purchased with the USE System replacing the original MEX6800 MPU Module.



Systems Analyzer

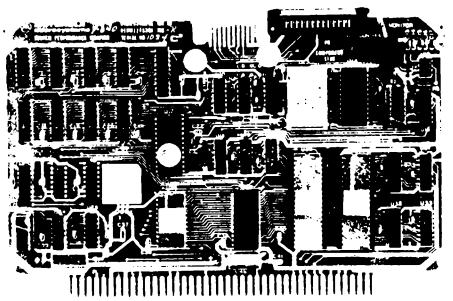
This unique instrument can be used to enhance the capabilities of the EXORciser or EXORterm as a design tool, or as an independent, portable troubleshooting unit for field service of bus-compatible equipment.

In field service applications, the Systems Analyzer derives operating power and I/O signals directly from the system under test. It can stop the system at any point in its program, step through the program, change the contents of the system memory, and monitor and record the MPU's operation during a selected portion of the program. It can even perform these functions without shutting down the operation of the system.

In EXORciser applications, it adds the same options to the system's inherent program development capabilities. In conjunction with the EXORciser and USE, it offers the most powerful combination of development and diagnostic tools available for microcomputer work.

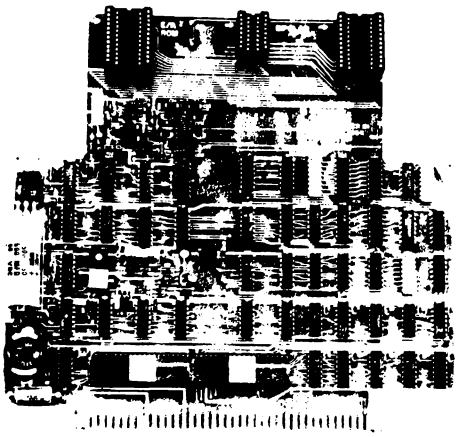
1 MHz Version, for EXORciser I and IA and EXORterm 200	MEX68SA
2 MHz Version, for EXORciser II and EXORterm 220	MEX68SA2

manufacturing



System Performance Monitor – MEX68SPM

The System Performance Monitor provides the means of monitoring an operational microcomputer system for the purpose of collecting data about processor utilization which is used to optimize the existing program. Monitoring consists of periodically sampling the address lines of the system under test. These samples are accumulated to produce a map of memory addresses and their corresponding frequency of reference. At the completion of an operation, the Monitor formats and prints a report on a control terminal. The system is particularly useful for the analysis of complex computer programs and can result in greatly improved software efficiency.

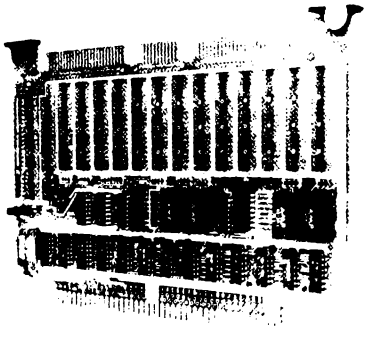


PROM Programmer – MEX68PP3

Once a program for the microprocessor system is designed and debugged, it is entered into a Read-Only Memory which becomes part of the dedicated MPU operated end system. When an end system is manufactured in large quantities, these programmed ROMs are often purchased in quantity from the component supplier. When only a few end systems are to be produced, the equipment manufacturer may elect to use a programmable ROM (PROM), or an Electrically Alterable PROM (EROM) and do the programming himself. The PROM Programmer will perform this function quickly, easily and inexpensively.

The PROM Programmer is designed to program a variety of MOS PROMs, EROMs and bipolar PROMs, including 30 device type numbers from 6 different manufacturers. It can verify the data in the PROM, transfer data from the PROM to the development system RAM memory, and transfer blocks of data from one memory location to another. Programming time varies depending on PROM used.

with Software on Cassette MEX68PP3A
with Software on Paper Tape MEX68PP3B
with Software on MDOS Diskette MEX68PP3M



Component Support Modules – MEX68USM

The universal Support Module is a printed circuit and wirewrap module used to support the 6800 family of devices. The lower portion of the board contains fully decoded EXORciser interface logic while the top portion is a wirewrap area. The module is also available with factory adaptation to support specifically the MC6845 CRT Controller device, the MC68488 GPIA device or the MC6854 ADLC device.

Choice of...

M6800 support software

Human programmers speak one set of languages; machines understand another. Hence, a number of computer routines have been developed to automatically convert the instructions associated with the various "programmer languages" into a sequence of instructions that can be followed by the computer. Such translation programs are called *assemblers, compilers or interpreters*.

Going hand-in-hand with the "translators" for programming purposes is the editor. This software routine permits the programmer to use a computer to make whatever changes may be required in creating, correcting or revising a program. The M6800 MPU Family is supported by a variety of such software programs in order to simplify the system designer's programming chores.

Motorola provides a compatible family of resident software that permits M6800 program development using Motorola Development and Evaluation Systems.

Resident Software Options

A resident development system provides the lowest program development cost where a number different M6800-based microcomputer systems are contemplated over a period of time. The software, designed for the EXORciser/EXORterm and PDS systems, includes an editor and an assembler/macroassembler. In addition, four high-level languages can now be used with the M6800 Microprocessor: FORTRAN, BASIC, MPL, and COBOL.

Firmware

Motorola provides a family of support firmware ROM's that permits M6800 program development using Motorola Development and Evaluation Systems.

User's Group Library

The User's Group Library provides a collection of general purpose programs and routines developped for the MC6800 MPU family. The library includes Test and Debug Programs, I/O Routines, Data manipulation and operating routines as well as Mathematics packages. The library is available either in binders form or on cassettes or diskettes media.

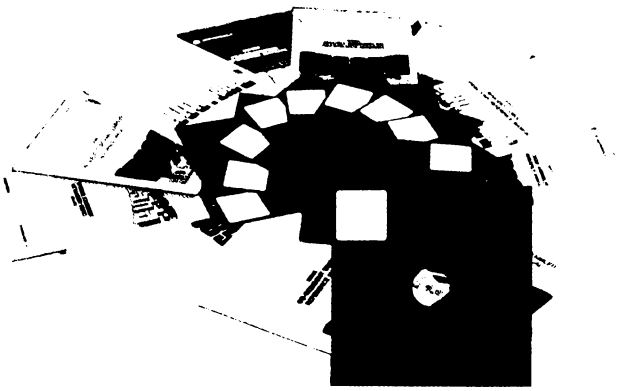
M6800 Resident Software Options
Ordering Information and Minimum RAM Requirements (Bytes)

Software	PDS	EXORciser/EXORterm	EXORciser/EXORterm + EXORdisk II
Co-resident Editor/Assembler	M68EAM1 (7K) (ROM Resident)	M68XAE6813 A/B (8K)	M68SMDOS100 (16K) (included in EXORDISK II)
Macroassembler/Linking Loader including 6801 instruction set	Not available	M68MASR010 A/B (16K)	M68SMDOS100 (24K) (included in EXORdisk II)
Resident BASIC Interpreter	M68EAB1 (14K) (ROM Resident, includes Editor/ Assembler)	M68BASR010 A/B (8K)	M68BASR010M (20K)
Resident COBOL Compiler	Not available	Not available	M68COBOL010M (32K)
Resident FORTRAN Compiler	Not available	Not available	M68FTNR012M (24K)
Resident MPL Compiler	Not available	Not available	M68MPLR010M (56K)

A suffix: Cassette B suffix: Papertape M suffix: MDOS Diskette

M6800 Firmware

Part Number	Description	System Family
MEC68MIN2	Minibug 2-executive program	PDS
MEC68MIN3E	Minibug 3E-executive and debugging program with 8 break-points capability	PDS
M68MM08A	Microbug-executive and debugging program with 8 break-points capability	Micromodule
MEX68EXB12	Exbug 1.2-executive and debugging program to be used with Debug module	EXORciser 1 EXORterm 200
M68IOS1	Input/Output Supervisor-CRT, Keyboard, Printer data handling program	PDS



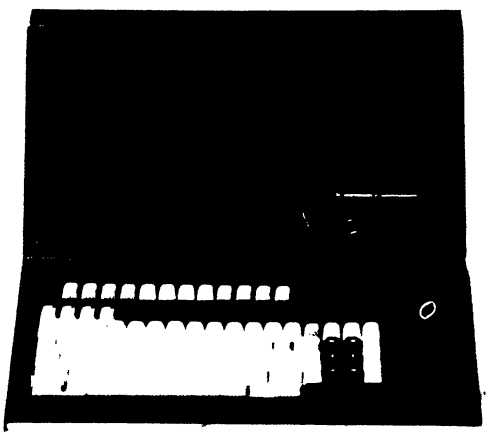
Choice of...

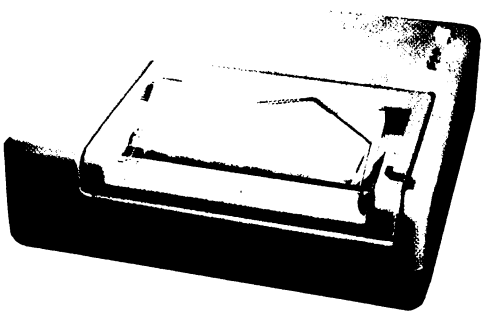
system peripherals

Peripherals are not necessarily an integral part of an MPU support line, but when designed for use in conjunction with a particular MPU development system they often precipitate savings by avoiding circuit redundancy. Motorola already supplies some dedicated peripherals for the EXORciser development system and has more under consideration. Each peripheral is supplied with the necessary circuitry to perform the EXORciser interface function.

EXORterm 150

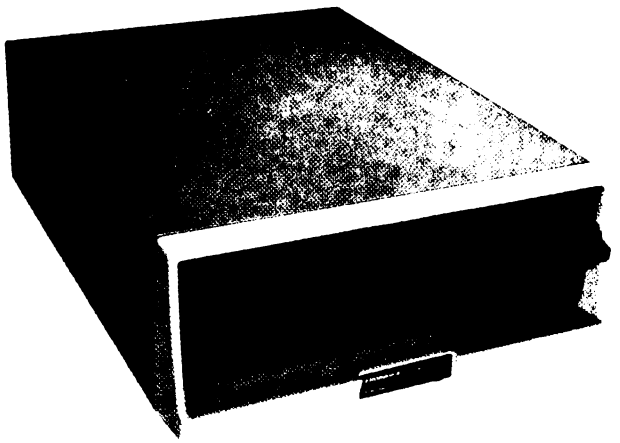
EXORterm 150 is a display terminal and console expressly personalized for use with the EXORciser. In this role, it facilitates the exchange of data between the user and the EXORciser via a high quality video interface in combination with keyboard entry and a serial communications link using speeds up to 9600 baud. To further enhance the efficiency of the User/EXORciser interface, special keys have been encoded to invoke functions unique to the EXORciser in each of its three command levels, EXbug, MAID, and DOS. For user convenience, the functions represented by each of these 12 special keys are displayed on the 23rd and 24th line of the screen. As the command level is changed, the function of the respective key changes and is displayed accordingly. EXORterm 150 includes Extended Display ROM and Editing/Cursor and Page Mode Control Keys.





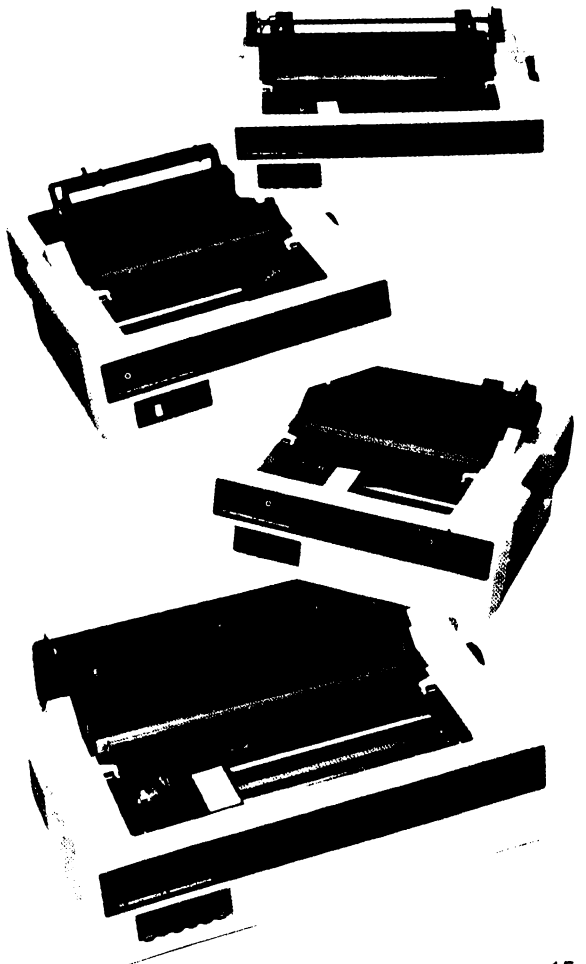
Medium Speed Printer

The MPR noiseless printer prints 80 characters per line at a speed of 30 characters per second on metallized paper (M68MPP1). It accepts 7-bit ASCII characters including Carriage Return and Line Feed codes and can be connected directly to the PDS products family (ADS, ADW, TDS).



EXORdisk II

EXORdisk II is a dual floppy disk storage system that extends the capacity of the EXORciser by up to 256,256 bytes of memory per diskette. It allows high-speed transfers because of fast headsettling time and logical sector arrangement. An interface card connects it to the EXORciser. The new software, MDOS, contained on a single diskette, permits random or sequential file organization and multiple I/O file activity. MDOS also features: job control files for batch-type use, file expansion with recopy, user-defined commands, user access to system routines, high-speed program loading, and binary memory image files to conserve disk space. Twenty MDOS commands provide the user with a comprehensive means to rapidly develop or modify software. The resident driver firmware is accessed by MDOS to control disk operations—various entry points are available to a user to perform certain operations. Specifically, a user has access to initialization and error checking, diskette operation, line printer drive and diskette mini-diagnostic routines. A minimum of 16K bytes of RAM, together with the EXORciser, and EXORdisk II provide a complete development system whose high-speed software capabilities can be matched only by much more expensive mini-computers.



Dot-Matrix Printers

Motorola offers a line of four dot-matrix printers to complement its microcomputer development systems. The line includes a full-range choice of features, such as:

80 and 132-column formats
60, 120 and 180 characters per second
Bidirectional and logic-seeking print heads.

All four printers are equipped with an Interface I/O Module and an Interconnection Cable Assembly that specifically adapt them to the EXORcisers and the EXORterm 200. In addition, these interface accessories permit the printers to be used with Motorola Micromodules to provide more complete single-source availability of microcomputer system components.

The four models in the line are:

Model 779 – a low-cost printer capable of printing from 80 to 132 columns of 5 x 7 dot-matrix at a rate from 21 to 90 lines per minute at 60 characters per second.

Model 781 – an 80-column character printer which features bidirectional, logic-seeking movement of the print head enabling throughput of up to 120 lines per minute.

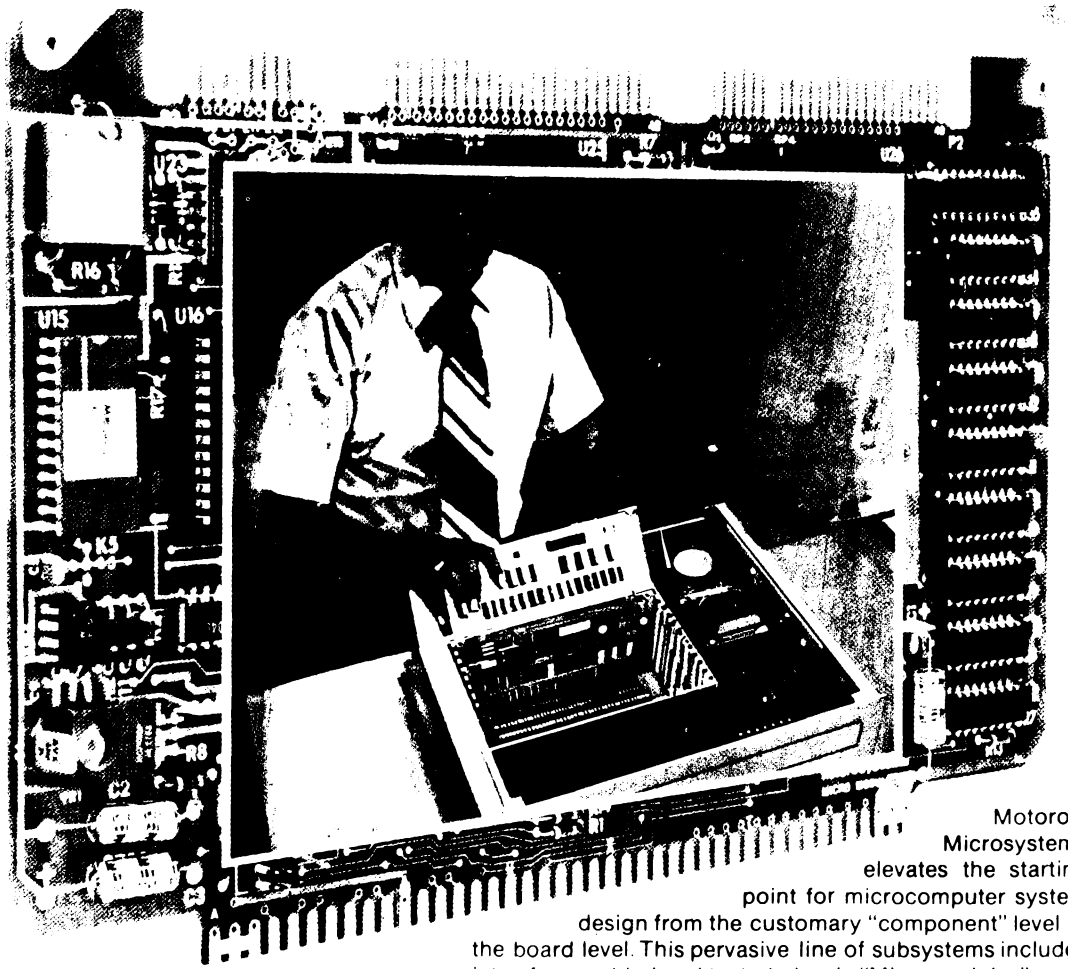
Model 702 – also equipped with bidirectional, logic-seeking print head, and with a head speed of 120 characters per second. This model has 132 character print columns and is capable of throughput from 45 to 185 lpm.

Model 703 – the top of the Motorola Microsystems printer line. This is an ideal printer for the business system. With a head speed of 180 characters per second, it provides high throughput rates from 70 to 280 lpm.

All models except 779 have tractor feed with a paper-out sensor. Each uses standard computer paper from one to six parts. Model 779 has pinch roll feed and uses standard teletype roll paper.

microcomputer subsystems

A high-level starting point for Microcomputer System Implementation



Motorola Microsystems elevates the starting point for microcomputer system design from the customary "component" level to the board level. This pervasive line of subsystems includes a variety of assembled and tested plug-in "Micromodules" ranging from monoboard microcomputers, ready for dedicated programming, to mix-and-match subassembly boards that give the designer a large number of system design and performance options. These subassemblies are supplemented by compatible support peripherals that reduce the hardware design and assembly phase of microcomputer system development to the simple interconnection of properly selected subsystems.

The Microsystem approach to microcomputer design is offered as an addition to, not necessarily a substitute for, fundamental designing with basic components. It is particularly suitable for equipment manufacturers with small-volume applications and limited development and manufacturing resources, or where design and development time-savings are of critical importance.

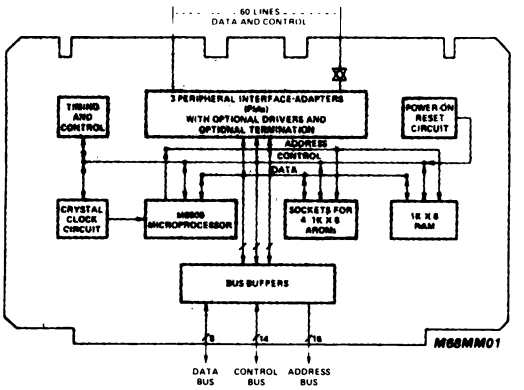
Choice of...

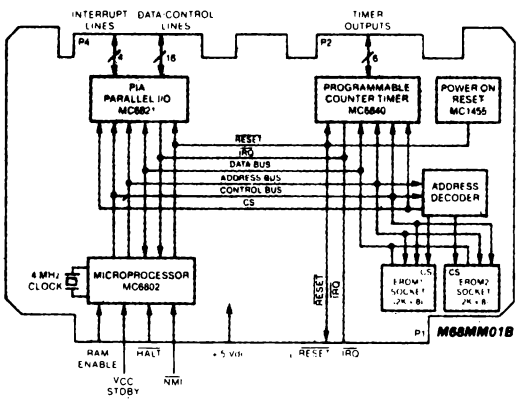
monoboard microcomputers

Choose from a selection of differently configured single-board microcomputers; add a suitable power supply and, perhaps, some additional external memory; put these into an appropriately available enclosure (or design your own); and you have a complete microcomputer—ready to receive your dedicated firmware (ROM, EROM or PROM) and go to work.

Motorola's Micromodule 1 series of monoboard microcomputers offers a choice of variations to best match a particular end-use requirement. All boards use the popular MC6800 or MC6802 microprocessor as the basic control unit. Variations consist principally of I/O selections and memory expansions.

FEATURES AND VARIATIONS





Micromodule 1—Part Number M68MM01

Basic MPU—MC6800

- 1 MHz Crystal-Controlled Clock
- 1K byte Static RAM
- Sockets for four 1K EROMs or ROMs
- Three MC6821 PIAs (60 peripheral I/O lines)
- 36K bytes available for external memory

Micromodule 1A—Part Number M68MM01A

Similar to above, but substitutes one MC6850 ACIA (with RS-232C interface) for one of the PIAs in the above unit. This adds communications (serial) interface capability and offers 40 lines of peripheral (parallel) I/O capacity. Permits up to 59K bytes of external memory addressing.

Micromodule 1A2—Part Number M68MM01A2

Same as Micromodule 1A but provides a convenient strap option that permits use of five different ROMs in the four on-board sockets—including:

- 1K EROM with multiple-voltage supply (MCM2708)
- 1K EROM with single (5 V) supply
- 2K EROM with single or multiple supply (MCM2716)
- 1K Mask-Programmable ROM (MCM68308)
- 2K Mask-Programmable ROM (MCM68317)

Micromodule 1B—Part Number M68MM01B

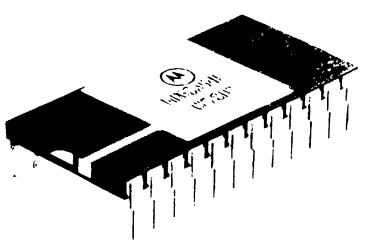
Basic MPU—MC6802

- 1 MHz Crystal-Controlled Clock
- 128 bytes of Static RAM
- Sockets for two 2K byte EROMs or ROMs
- One MC6821 PIA (20 peripheral lines)
- Three 16-Bit Programmable Timers (MC6840)

Micromodule 1B1—Part Number M68MM01B1

Similar to above, but adds the following capabilities:

- 256 (additional) bytes of Static RAM
- Serial I/O with RS-232C Interface



MICRObug MONITOR/DEBUG

MICRObug provides the user of Micromodules with a system development and debugging capability. It is intended for use with Monoboards, above, and with the CPU Module M68MM02 described on the following page.

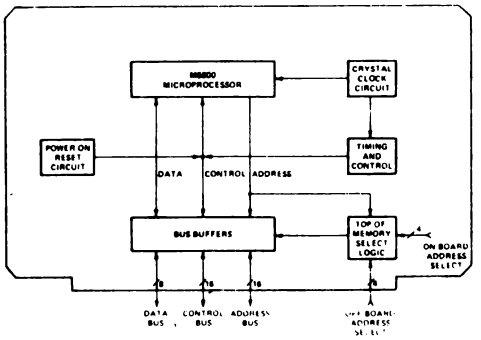
M68MM08A – MICRObug ROM only. Use with Monoboards M68MM01A/01A2/01B1.

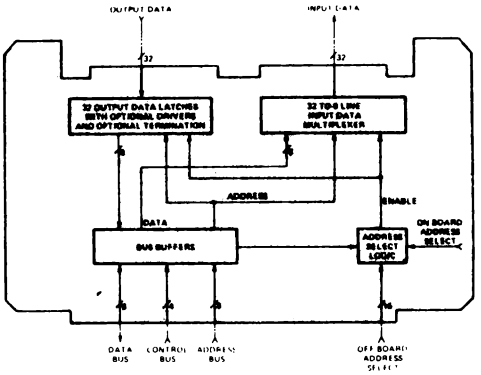
M68MM08 – MICRObug ROM with a MEX6850 Communications Interface Adapter Module. Use with Monoboards M68MM01/01B and CPU Module M68MM02.

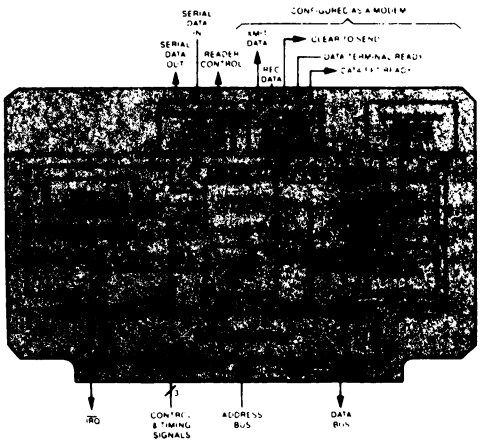
Choice of...

microcomputer subassemblies

When you need more design flexibility than a single monoboard computer can provide, choose from a wide selection of subassemblies to give your system the characteristics it needs, at an affordable cost. Motorola Micromodules allow almost limitless diversification or expansion of microcomputer functional capabilities.







All micromodules are electrically and mechanically compatible with each other, and with the EXORciser Development System (see Page 6). This means that they may be plugged into the EXORciser for hardware and software debugging, using the EXbug Firmware of the EXORciser Debug Module.

A CENTRAL PROCESSOR

CPU Module -- M68MM02

This is the cornerstone of a totally modular microcomputer system. It combines all of the processing and control power of the MC6800 Microprocessor with the necessary two-phase clock generator, the reset circuitry for power turn-on initialization, and the bus interface and control circuits. Moveover, it supplies the timing, priority, and refresh controls for 3-state and HALT operations and memory refresh.

INPUT/OUTPUT CAPABILITIES

Parallel I/O Modules

M68MM03 - Thirty-two TTL-compatible parallel inputs and 32 TTL-compatible latched and buffered parallel outputs are provided by this powerful I/O module. This permits interchange of four contiguous (8-bit) bytes of parallel data between the Central Processor and an external system. By using the Index Register of the MC6800 MPUs, all 32 input bits can be read and stored in 20 machine cycles, while only 18 cycles are required to load and latch the 32 output bits.
Up to 256 I/O modules may be used with a micromodule-based system, providing up to 8192 input and output bits.

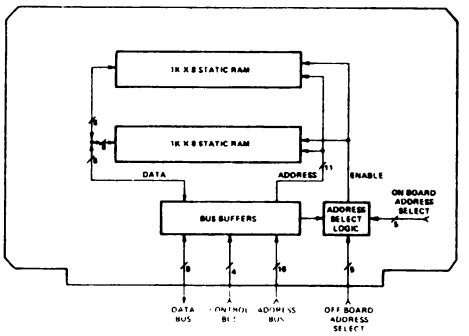
MEX6820 - Similar to above, but tailored as a development system with on-board address-select switches and provisions for installation of wire-wrap sockets for adding custom interface circuits.

MEX6821-2 2 MHz version of MEX6820

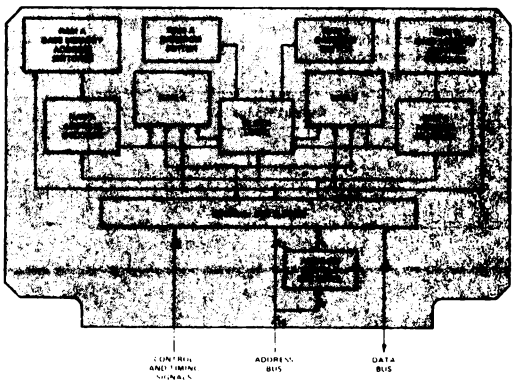
Serial I/O Module

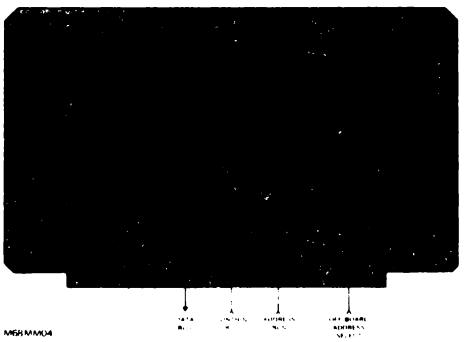
MEX6850 - This module interfaces the CPU module with an asynchronous data communications device. It permits 7 or 8-bit transmissions; TTY and RS-232C terminal interface; program selectable odd, even or no parity; eight switch-selectable baud rates from 110 to 9600 baud.

MEX6850-2 - 2 MHz version of MEX6850, but in addition, the module, with a minor jumper modification, will accomodate the SSDA device.



RAMs





MEMORY ADD-ONs

2K/4K Static RAMs

M68MM06 – This module provides 2K bytes of Static NMOS RAM, organized in two 1K x 8-bit groups which appear to the system bus as 2048 contiguous address locations. The base address can be assigned in 2K-byte increments throughout the range of 0000_{16} to $F000_{16}$. The address can be selected by means of on-board or off-board jumper connections that modify address-select bits A11 through A15.

MEX6812 – Similar to above, but tailored as a development system with on-board base address switches, and RAM/ROM switches that disable the write function, causing the RAMs to operate as ROMs.

M68MM09E2 – This module contains 2K-byte of static CMOS RAM with battery on the module, providing non volatile memory in Micromodules based systems. Data retention is as long as 30 days.

M68MM09E4 – This module is a 4K-byte version of the M68MM09E2.

8K to 48K RAM

The RAM modules described on page 7, with configurations of 8K, 16K, 32K and 48K-byte, static, pseudo-static (hidden refresh) or dynamic can be used in a Micromodule based system.

ROMs Prewired Boards

8K/16K EROM/ROM

M68MM04 (8K) – Permits installation of 8K bytes of either EROM or ROM for storing the required firmware programs. Simply plug the programmed memory devices (MCM68708 EROM or MCM68308 ROM) into the appropriate sockets and select the base memory address. Operates over address range of 0000_{16} to $E000_{16}$ in 8K-byte increments.

M68MM04-1 (16K) – Similar to above, but with 16 sockets, rather than 8, for 16K bytes of memory.

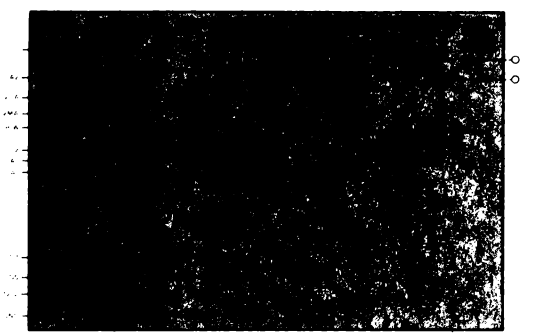
A-D/D-A CONVERSION MODULES

In many applications a digital computer is required to interface with analog signals. In such cases analog-to-digital and digital-to-analog conversion is required. As part of the Micromodule family, Motorola offers eight converters for this purpose. There are five input modules (A-to-D) and three output modules (D-to-A) as follows:

Type	No of Channels		Resolution	Input Voltage	Output
	Differential	Single-Ended			
A/D (Input)					
M68MM05A	8	–	12 bits	0 to 5/10 V, ±2.5/5/10 V	Binary
M68MM05B		16	12 bits	0 to 5/10 V, ±2.3/5/10 V	Binary
M68MM15A*	8	16	12 bits	0 to 5/10 V, ±5/10 V programmable gain	Binary or 2's complement
M68MM15A1*	16	32	12 bits	0 to 5/10 V, ±5/10 V programmable gain	Binary or 2's complement
M68MM15B	1 expandable to 4		16 bits	±25/55/80 mV for thermocouple or strain gage inputs	Binary
	No. of Output Channels			Output Range	
D/A (Output)					
M68MM05C	4		12 bits	0 to 5/10 V, ±2,5/5/10 V, @ 5 mA, 1Ω	
M68MM15CV*	1 to 4		12 bits	0 to 5/10 V, ±5/10 V, @ 5 mA, 0.2Ω	
M68MM15CI*	1 to 4		12 bits	4 to 20 mA current output, 9 V	

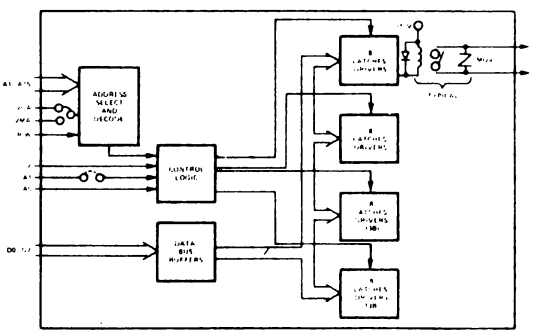
* Capable of working at 2 MHz.

HIGH ISOLATION I/O MODULES



Digital Input Modules

M68MM13C/D – These Micromodules provide 24 optically isolated input channels. The Modules sense the amplitude of the input voltages to determine if the input is read as a data "1" (greater than 17 V) or as a data "0" (less than 4 V). Data is outputted in banks of 8 bits. Address Lines A0 and A1 select the set of 8 inputs to be monitored. Module 13D incorporates a dc-to-dc converter which supplies the necessary wetting current to sense (user-supplied) contact closure currents as inputs.



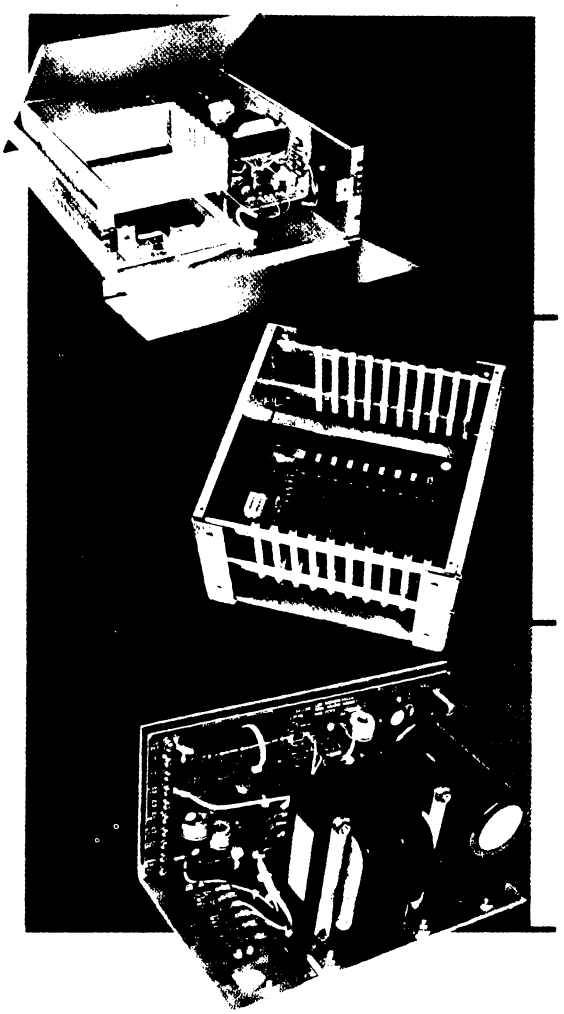
Relay Type Output Modules

M68MM13A/B – Some microcomputer applications require output circuits with low on-impedance, high output current and/or better isolation than provided by transistors. For such applications, the Motorola Micromodule Family includes output modules with reedrelay outputs. Module 13A has 16 digital output channels and Module 13B has 32 channels. Output relays are selected in banks of 8 by the Address Bus and the status (on/off) of each relay in the bank is controlled by the data on the Data Bus. Rated load is 10 watts (max.) per channel.

Choice of...

chassis, card cages and power supplies

Bringing your modularized microcomputer system on line is simple with these accessories designed to match the Micromodule architecture and your end use. Choose from a variety of chassis with power supply, and card cages with separate power supply to tailor the system to your requirements . . .



M68MMLC2 and M68MMSC2

Micromodule chassis with Power Supply for standard RETMA 19" rack mounting. Available in two pre-wired ready-to-use models: long 10-card chassis, M68MMLC2 and short 5-card model, M68MMSC2. Both versions use 15 A (@ 5 V) triple DC output power supply with specifications of M68MMPS1-2, below.

M68MMCC05 and M68MMCC10

Want to use a separate power supply? The two card cages with 10-card (M68MMCC10) or 5-card (M68MMCC05) capacity are sized to handle your Micromodule requirements effectively and efficiently. Cages may be mounted in five possible orientations and have accommodations for power connection.

M68MMPS1-2 (220 VAC)

Triple Output Power Supply designed to handle voltage and current requirements for up to 10 Micromodules. Offers 15 A output at 5 volts for five-volt MPU systems, plus separate +12 V and -12 V outputs (2.5 A and 1.5 A, respectively) for associated memory systems and other accessories. Dimensioned for mounting on either side of card cages described above.

Application Support

Design of MPU-based systems is not difficult. The nature of the required components reduces the hardware to a small number of easily compatible building block. However development of software to efficiently convert the computer into a dedicated machine is another matter. It demands a thorough knowledge of the interactive nature of the building block, as well as detailed knowledge of the processor's unique instruction set and its capabilities. Motorola's M6800 application support ranges from a literature library to personalized training and consultation.

Support Literature

Technical documentation
(Prices on application)

"M6800 Microprocessor Applications Manual"
A 700-page book discussing all aspects of the M6800 system from components to programming and applications.

"Motorola microcomputer components"
Technical description of all semiconductor components related to Motorola Microcomputers.

"M6800 Programming reference manual"
A book of 112 pages discussing all aspects of M6800 programming and including short description of firmware commands set.

"From the computer to the microprocessor"
An introductory book to computers and microprocessors available in English, French or German.

"Understanding microprocessors"
An introductory book to microprocessors covering aspects such as programming, system design and MPU market.

"Getting aboard the 488-1975 bus"
Implementation of the IEEE 488-1975 Instrumentation Bus will the MC68488 Interface Adapter.

Application notes

R-29-3-10	MC6870A, MC6871A, MC6871B microprocessor clock applications in M6800 microprocessor systems.
AI-75	An ICU Development Aid using an M6800 Family.
AN320	Interfacing MPU-MC6800 with CMOS systems.
AN322	Microprocessor control of industrial air conditioned plant.
AN731	Low-speed modem fundamentals (see also AN747 and EB-49).
AN747	Low-speed modem system design using MC6860 (see also AN731 & EB-49).
AN754	Device operation and system implementation of the Asynchronous Communications Interface Adapter (ACIA) MC6850.
AN757	Analogue-to-digital conversion techniques with the M6800 microprocessor system.
AN764	A floppy disk controller using the MC6852 SSDA and other M6800 microcomputer family parts.
AN770	Data acquisition networks with NMOS and CMOS.
AN771	MEK6800D2 microcomputer kit system expansion technique.
AN773	A CRT terminal using the M6800 clock generator/driver.
AN774	A simple high speed bipolar microprocessor illustrates system design and microprogram techniques.
AN775	M6800 systems utilizing the M6875 clock generator/driver.
AN777	A dual processor system for use in the EXORciser.
AN782	Interfacing and controlling digital temperature data using the MC6800.
AN783	Synchronizing two Motorola MC6802s on one bus.
EB-49	Application performance of the MC6860 modem (see also AN731 & AN747).

Specific detailed descriptions

More than 100 different booklets describe different products of hardware, software, firmware and allow Motorola to ship with each part a technical document covering all aspects of the equipment. (*Available with product*)

Data sheets

Each part is described in a separate data sheet available from your local Distributor or the Motorola Sales Office.

Microsystems Functional Guide

This booklet is a complete Microsystems functional guide, covering all products available with their respective part number and classified by major type of function.

System Design Courses and Seminars

After more than three years of training sessions held in major cities all over Europe, Motorola's 3-day, hands-on microprocessor course has emerged as one of the most popular ways for engineers to master the design of M6800 systems. The course is taught by experienced instructors, well qualified in microprocessor techniques. It is given according to a pre-published schedule in all countries, but can be presented at specific factory locations at a nominal cost.
For the latest schedule, and additional information, please contact your local Distributor or the Motorola Sales Office.

Engineering Assistance for Applications

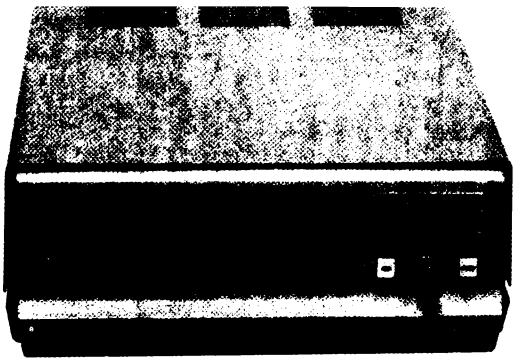
Assistance for MPU applications is available to the M6800 user. An international network of consultants has been set up all over Europe to provide you with the design support you may need. (*Please call your Motorola Sales Office or Distributor for names and addresses.*)

chapter 1

development hardware

M68SDT EXORciser 1

Emulator for M6800 Based Systems



The EXORciser is a modularized, expandable instrument that permits "instant breadboarding" and evaluation of any M6800-based microcomputer system. It consists of a prewired, bus-oriented chassis and power supply, together with three basic modules — an MPU Module, a Debug Module and a Baud Rate Module. These provide the basic control and interface functions of a microcomputer, and house the system development and diagnostic programs. A number of separately available, optional memory modules and additional interface modules (up to twelve) may be added, simply by plugging them into existing prewired sockets, to convert the basic system into an exact prototype of a desired end system. Thus, the EXORciser, with its built-in EXbug Firmware, enables the designer to configure, evaluate and debug his final system hardware and software using actual M6800 components.

Features

- Reduces system development time and cost
- Emulates final system architecture and performance through modular building block concept with standard M6800 components
- Permits debugging of final system design through built-in diagnostic firmware
- Facilitates program development using separately available Resident Software

EXORciser Options

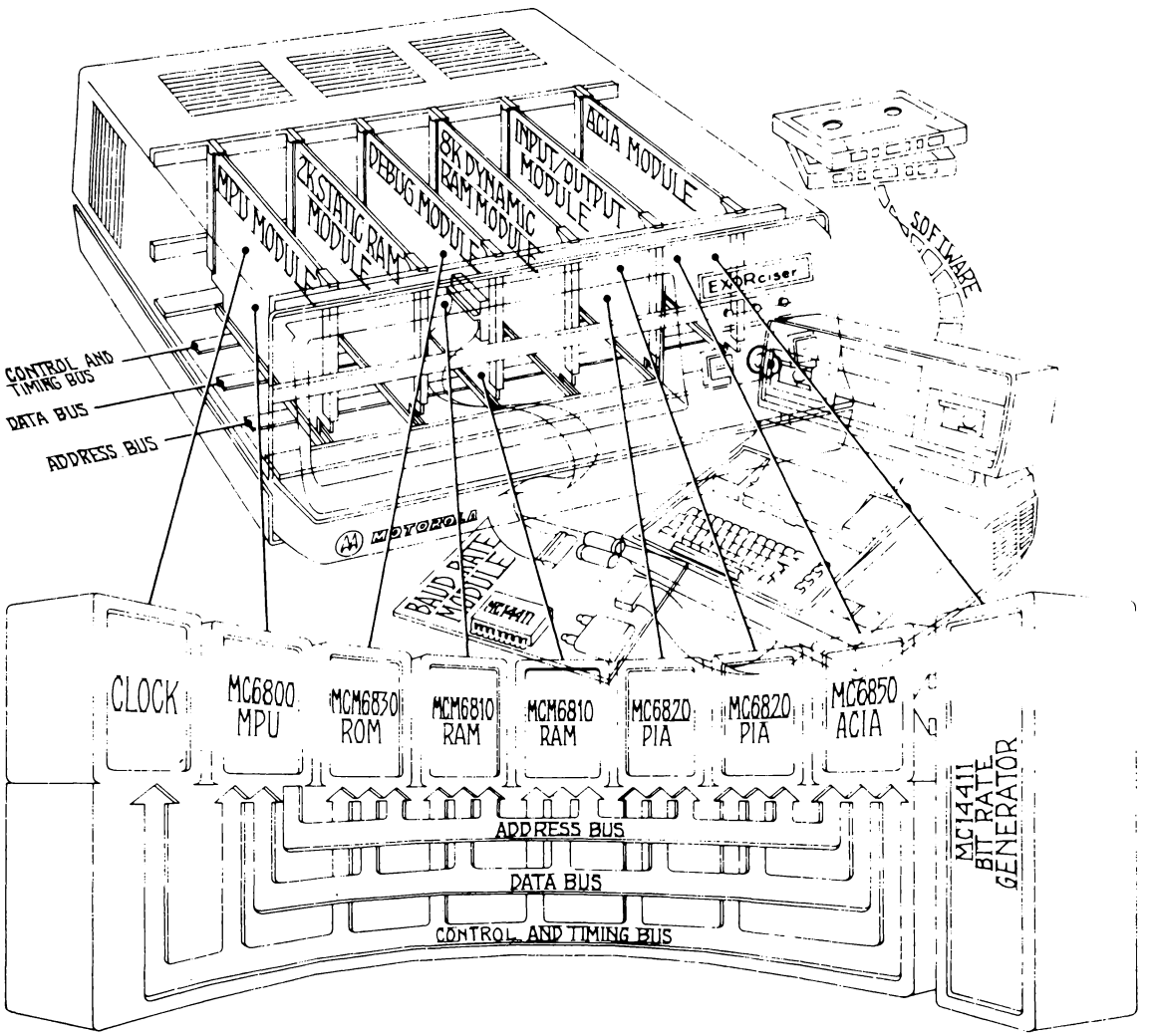
Basic Models:

M68DTT2	220 Volt Table Top EXORciser I
M68DTTU2B	220 Volt Table Top EXORciser I with USEB
(Dimensions:	19.25 x 17.5 x 7, W x D x H)
MEX68RK	Rack Mounted Conversion Kit

(Converts standard table-top model for rack mounting.)

EXORciser Specifications

Power Requirements	95-135/205-250 Vac 47-420 Hz 250 W
Word Size	
Data	8 Bits
Address	16 Bits
Instruction	8, 16, and 24 Bits
Memory Capability	65,536 bytes (maximum)
Instructions	72, variable length
Clock Cycle Time	Selectable: 1 μs crystal control clock or provisions for an external clock between 1 μs and 10 μs.
Interrupt	Maskable real-time
Data Terminal Interface Characteristics	
Baud Rates (Switch Selectable)	110, 150, 300, 600, 1200, 2400, 4800 and 9600
Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
Reader Control Signal	Control signal for TTY devices modified for external control
Operating Temperature	0-55°C


MPU MODULE
2K STATIC RAM MODULE
DEBUG MODULE
8K DYNAMIC RAM MODULE
INPUT/OUTPUT MODULE
ACIA MODULE
SOFTWARE
EXORciser
CONTROL AND TIMING BUS
DATA BUS
ADDRESS BUS
MOTOROLA
BAUD RATE MODULE
MC1411
CLOCK
MC6800 MPU
MCM6830 ROM
MCM6810 RAM
MCM6810 RAM
MC6820 PIA
MC6820 PIA
MC6850 ACIA
MC1411 BIT RATE GENERATOR
ADDRESS BUS
DATA BUS
CONTROL AND TIMING BUS

The M68SDT EXORciser

Description and Operation

The basic EXORciser contains the common ingredients of a microcomputer and offers the system designer a low-cost, versatile means of achieving unique final-system performance through the selective addition of separately available, optional modules. These separate assemblies plug directly into the EXORciser's bus so that system expansion becomes quick, easy, and essentially error-proof. With provisions for up to 12 add-on assemblies, a system of almost any complexity can rapidly be assembled.

The illustration on the preceding page shows the major components of the basic EXORciser as well as those of several optional EXORciser modules. Supplied with the basic EXORciser are the MPU Module, the Debug Module, and the Baud Rate Module. The Baud Rate Module contains, primarily, an MC14411 Bit Rate Generator that determines the data transfer rate between an external terminal and the EXORciser. The module supplies eight switch selectable baud rates. The Baud Rate Module, as shown, also provides the terminal connections, and serves as a feed-through between the terminal and the EXbug Firmware on the Debug Module.

The MPU Module includes a built-in, crystal-controlled 1 MHZ clock that provides the timing for the microprocessor system under development, as well as for the rest of the EXORciser. In addition, this module houses the MC6800 Microprocessing Unit which imparts to the EXORciser its computation and control capabilities.

The Debug Module, through its EXbug Firmware stored in the module's three MCM6830 ROMs, enables the user to evaluate and debug a system under development. The module's two MC6810 RAMs provide a 256 byte scratch-pad memory for the EXbug routines.

These functional subsystems of the basic EXORciser are supplemented by a power supply and a bus-oriented distribution system. This bus system transfers the power supply voltage as well as the data, address, and control signals to the optional modules.

Conspicuous by their absence from the basic EXORciser are the memory and input/output modules needed to turn this tool into a functional system. These memory and input/output modules are available as separate, optional modules and give the systems designer the flexibility to configure any desired system. Overall, the EXORciser can address up to 65K bytes of memory, and addresses the input/output modules (as well as the memory modules) as memory.

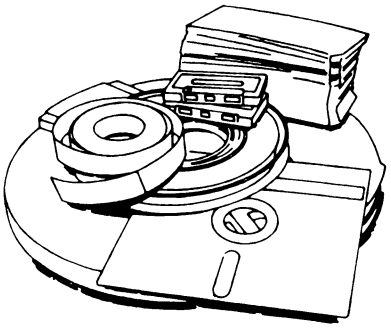
Typical Design Procedure

Microprocessor system designs can be implemented in many ways. Motorola provides a compatible family of host-computer and time-share programs upon which the user can develop his system software. However, where microprocessor systems are being developed for a variety of end uses and applications, the EXORciser with its resident software and hardware emulation capabilities may well prove to be the most efficient and least expensive system design and development tool.

Using the EXORciser in a typical design process normally begins by defining the functions to be performed by the proposed system. In this definition phase the designer makes the required trade-offs between the system hardware and software functions.

The designer now, using the appropriate memory and input/output modules, emulates his proposed system in the EXORciser. Recognizing that some systems may require special interface circuitry and customized circuitry, provisions have been made on the input/output modules for the designer to insert 14, 16 and 24 pin wirewrap sockets and construct the special interface circuitry. Also the designer can construct any customized circuitry on the Wirewrap Module.

The terminal, as illustrated, provides the means for communications between the designer and EXORciser. This can be done by means of the terminal keyboard, from paper tape, or from a cassette associated with the particular terminal in use.



The M6800 resident software, when loaded into the EXORciser, provides the designer with a powerful tool on which to develop his software. Using the capabilities of the M6800 Resident Editor, the designer enters a source program either via the terminal keyboard or from the selected medium. The user now can modify and change his source program as required to meet his proposed systems requirements. This includes:

Printing out all or any part of the program for detailed examination;
Changing any characters or string of characters in the source program;
Deleting or adding instruction lines or characters anywhere in the program.

At the end of the editing process, the Resident Editor will provide a source program that may be stored on paper tape, cassette, or diskette. This source program may be used in subsequent assembly operations on any of the compatible Motorola assemblers and cross assemblers.

The EXORciser's M6800 Co-Resident Assembler or the Resident Macro Assembler and Linking Loader can be used to automatically translate the source program into an object program. The Co-Resident Assembler requires a minimum of 8K bytes of memory while the Macro Assembler and Linking Loader requires a minimum of 14K bytes of memory.

The resultant Object Program is available from the EXORciser in three forms.

1. A printed assembly listing of the source program.
2. An Object Program on paper tape, cassette, or diskette.
3. A machine file, consisting of the machine-coded program stored directly into the EXORciser memory. This option permits the program to be executed immediately after assembly with no need for subsequent loading.

The Macro Assembler in its assembly process allows the assignment of the memory addresses of a program to be relocatable and assigned when loaded by the Linking Loader rather than fixed during the assembly operation. With the Co-Resident Assembler, the program address assignments are fixed and absolute in the assembly operation.

Once the designer has configured the EXORciser to emulate his hardware and has developed his programs, he is ready to debug his system. The EXORciser, with its EXbug system development Firmware, permits the user to debug both his system hardware and his system software as required until he has his system up and operating.

The EXORciser with its USE (User System Evaluator) option can be used to test and evaluate equipment external to its chassis. By removing the MC6800 Microprocessing Unit from the user's system and connecting the USE cable from the EXORciser into the MPU's socket, the EXORciser with its EXbug Firmware can be used to debug and troubleshoot microprocessor systems.

The EXORciser also can be used as a production tool. An EXORciser equipped with USE can be used in a final test area for testing the user's production system. With MOTEST, our component tester, the EXORciser also can be used to test the M6800 family of parts.

EXORciser Bus Signals

The EXORciser bus interfaces the MPU Module with other modules being used in the EXORciser. This bus permits the EXORciser to be configured to meet a user's specific application.

Data Bus (D0-D7) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers on the modules are three-state logic devices.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers.

Read/Write (R/W) – This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state.

Valid Memory Address (VMA) – This line, when high. indicates that the address on the bus is valid.

Valid User's Address (VUA) – This line, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi 1$ and $\phi 2$ non-overlapping clock signals.

Phase 1 ($\phi 1$) Clock – This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.

Phase 2 ($\phi 2$) Clock – This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bus Available (BA) – The Bus Available signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the Halt line is low or the MC6800 MPU is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU Module three-state output drivers will go to their off state and other outputs to their normally inactive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

Interrupt Request (IRQ) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

Reset – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser.

Three-State Control (TSC) – This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address and Valid User's Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is initially jumpered to ground on the MPU Module.

Refresh Request (REFREQ) – This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 1$ high and, through the Refresh Grant command, instructs the initiating memory module to refresh itself.

Refresh Grant (REFGRANT) – The MPU Module, on receiving a Refresh Request input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) – This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 2$ high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level.

Halt – When this input is low, all activity in the MC6800 MPU will be halted. This input is level sensitive. In the MC6800 MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the Halt line must not occur during the last 250 ns of $\phi 1$. To insure single instruction operation, the Halt line must go high for one $\phi 1$ clock pulse.

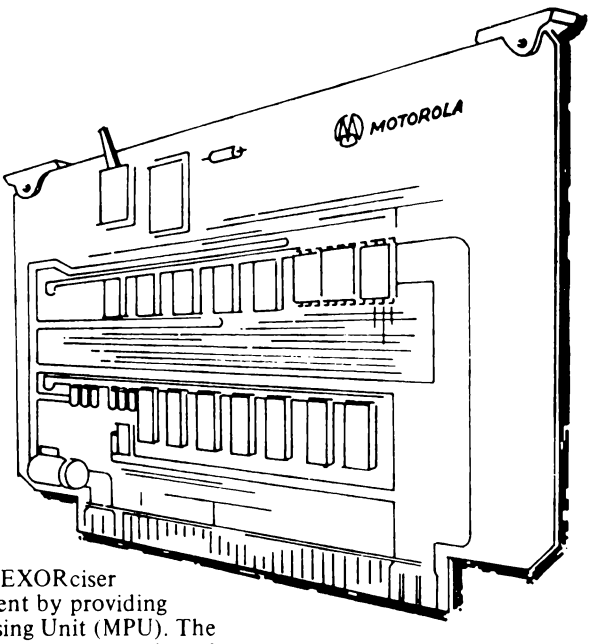
Refresh Clock (REFCLK) – This signal is generated by the dynamic memory module being used as the master refresh module. This signal is used to initiate a memory refresh operation on the dynamic modules functioning as slave refresh modules.

Stand By (STDBY) – This line is a low level during a power-fail condition and a high level during normal EXORciser operation.

Bus Control

It is possible for a module other than the MPU Module to gain control of the bus. This module would place a low level Halt on the bus and monitor the Bus Available signal. When the MPU Module completes the instruction it is performing, it generates a high level Bus Available signal. The module requesting control of the bus now must pull the Three-State Control line low, forcing the MPU Module address bus drivers to their high-impedance state. The requesting module now has control of the EXORciser bus until it elects to relinquish control.

MEX6800 MPU Module



- Provides the MPU and clock functions for both the EXORciser Debug system and the emulated user's system
- Crystal controlled 1 MHz clock
- Provisions for an external clock
- Automatic system initialization and restart capability
- Dynamic memory refresh capability on a cycle stealing basis
- Capable of working with slow external memories

The MEX6800 MPU Module is the heart of both the EXORciser Debug system and the user's system under development by providing both the system clock and the MC6800 Microprocessing Unit (MPU). The MPU Module also automatically initiates an EXORciser restart operation when power is first applied to the EXORciser.

The clock circuit generates a crystal-controlled 1 MHz signal, but the system may be operated with an external clock at frequencies between 100 kHz and 1 MHz by means of a switch mounted on the MPU Module.

In addition to generating the basic EXORciser timing signals, the clock circuit provides the EXORciser with the capability of refreshing dynamic memories and working with slow memories. The dynamic memories are refreshed on a cycle stealing basis. In working with slow memories, the MPU Module stretches the clock pulse to give the memory sufficient time to complete its assigned operation.

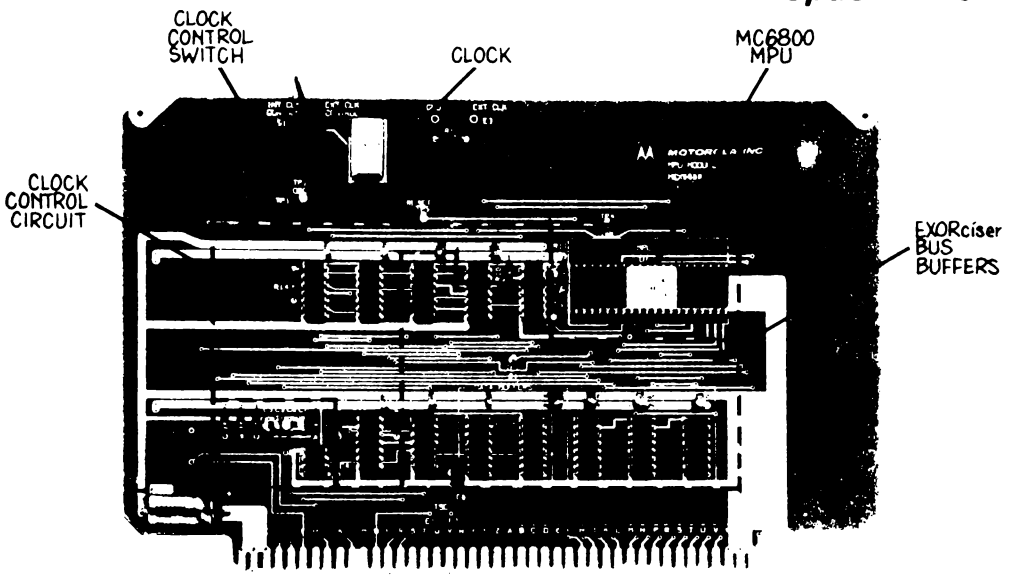
Specifications

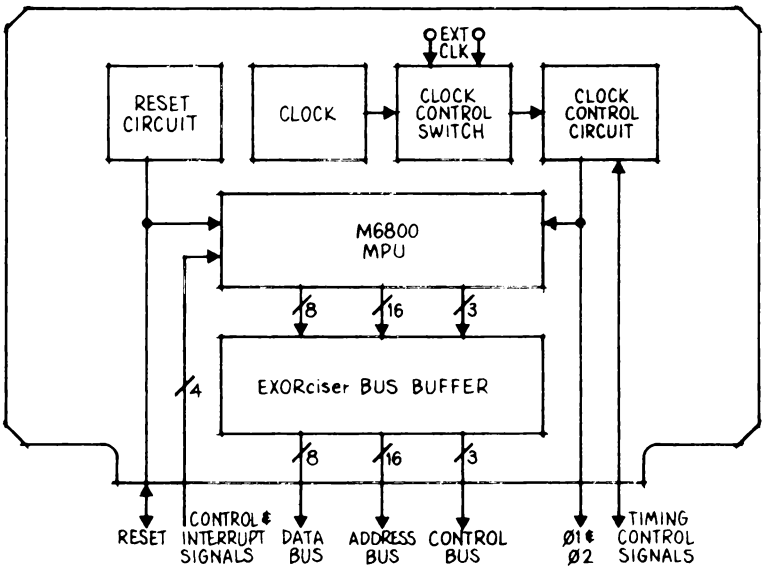
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Size Capability		65,536 bytes maximum
Word Size	Data	8-bits
	Address	16-bits
	Instruction	8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts Software interrupt
Clock Signal		1 MHz; provision for external clock between 100 kHz and 1 MHz
Input Control Signals		TTL Voltage Compatible
Logic "0"		0.0-0.8 V
Logic "1"		2.0-5.25 V
Address Bus and R/W		
Logic "0"		0.0-0.5 V
Logic "1"		2.4-5.25 V
Off-State Leakage Current		-40 μA
Data Bus		Three-state TTL voltage compatible
Input Logic "0"		0.0-0.8 V (-200 μA at 0.4 V)
Input Logic "1"		2.0-5.25 V (25 μA at 5.25 V)
Output Logic "0"		0.0-0.5 V (40 mA at 0.5 V through a resistor to V_{CC})
Output Logic "1"		2.6-5.25 V (-10 mA at 2.6 V through a resistor to ground)
Output Off-State Leakage Current		100 μA at 2.6 V
Output Control Signals		TTL voltage compatible
Logic "0"		0.0-0.4 V
Logic "1"		2.4-5.25 V
Operating Temperature		0 to 70°C
Power Requirements		5 Vdc at 700 mA
Physical Dimensions:		
W x H x T		9.75 x 5.75 x 0.062 in.

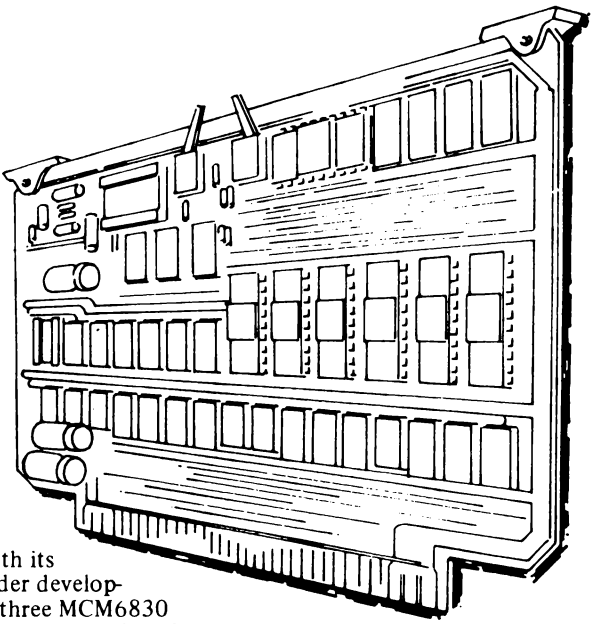
MEX6800
MPU Module

Resident
(also available as additional Optional Module)





Debug 1 Module



- Provides EXbug system development Firmware
- Contains the special hardware to implement the EXbug functions
- Enables the user to communicate with the EXbug Firmware via a data terminal
- Interfaces EXORciser front panel switches and controls with the MPU

The Debug Module, through its EXbug Firmware and implementation hardware, provides the EXORciser with its unique capabilities to evaluate and debug a system under development. The EXbug Firmware is stored in the module's three MCM6830 ROMs with the module's two MCM6810 RAMs serving as a scratch pad memory for the EXbug routines.

Using the EXbug routines provides the designer virtually unlimited freedom in examining and debugging his proposed system hardware and software. He can, for example, search the input medium for a file, load a file into EXORciser memory, verify the contents in the EXORciser memory, print out the contents of the EXORciser memory, and record the memory contents on the selected medium. In between these input/output functions, the user can examine and, if required, change the memory contents. He can insert and remove one hardware breakpoint and up to eight software breakpoints. He also can run in real time or trace through the user's program or a selected portion of the user's program. While using these routines, the user modifies his hardware and software as required until he has his system up and running. The DISABLE switch on the module may be used to disable the EXbug routines.

The user communicates with EXbug via an external terminal working in conjunction with the Baud Rate Module and the Debug Module. The STOP-ON-ADDRESS/SYNC ENABLE switch on the Debug Module is used to generate a sync pulse at a pre-selected address or to enable the hardware breakpoint function.

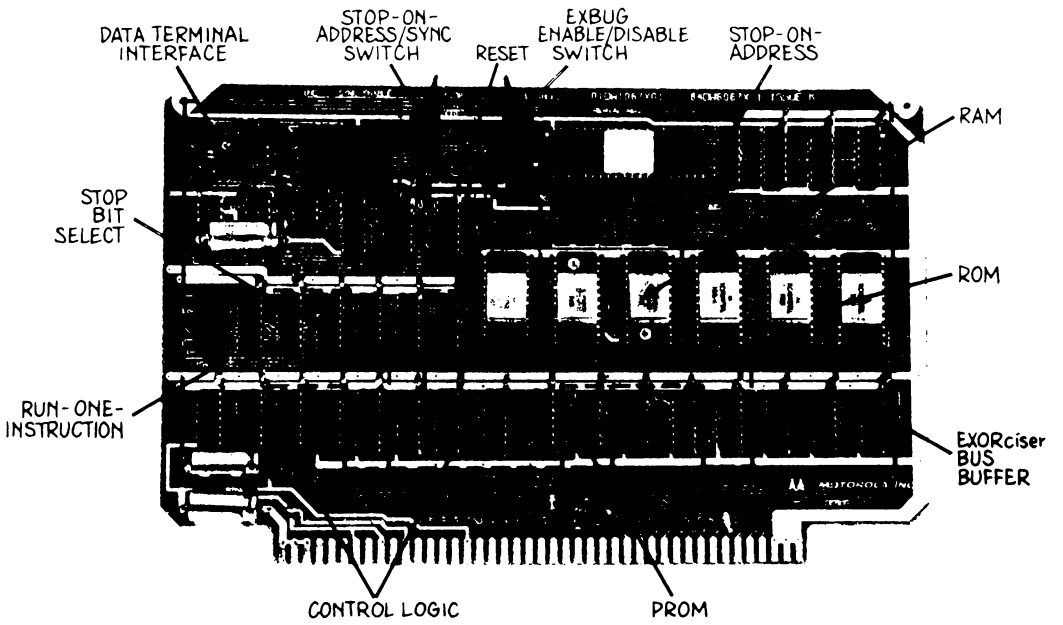
Specifications

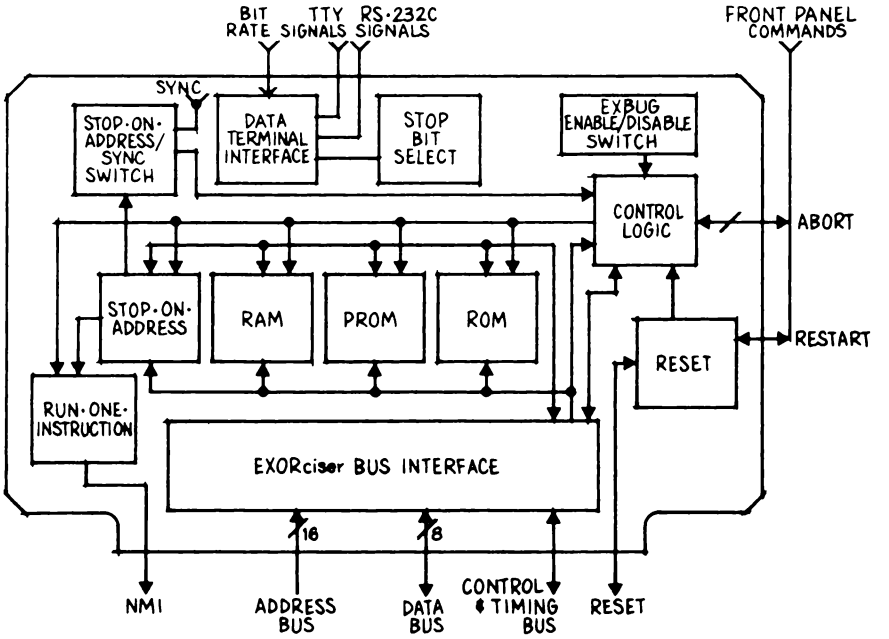
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Address and Control Bus	**TTL voltage compatible**
Logic "0"	**0.0-0.85 V (−200 μA max at 0.5 V)**
Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	**0.0-0.85 V (−200 μA max at 0.5 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at −10 mA through a resistor to ground**
Operating Temperature	**0 to 70°C**
Power Requirements	**+5 Vdc at 1.3 A** **+12 Vdc at 500 mA** **−12 Vdc at 500 mA**
Physical Dimensions	
W x H x T	**9.75 x 5.75 x 0.062 in.**

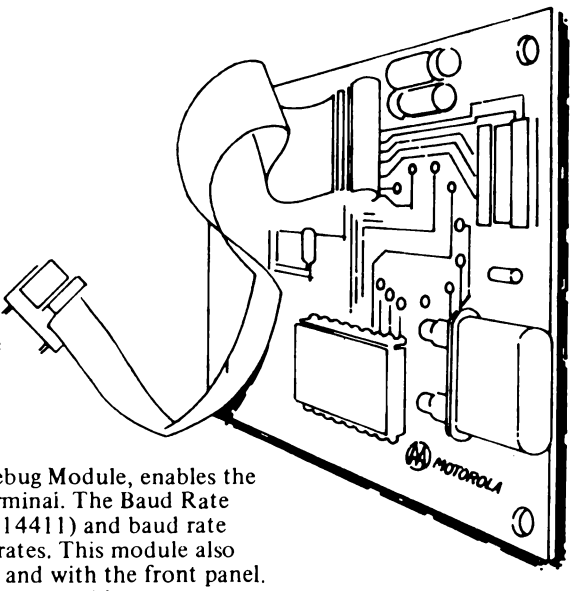
Debug Module

Resident





Baud Rate Module



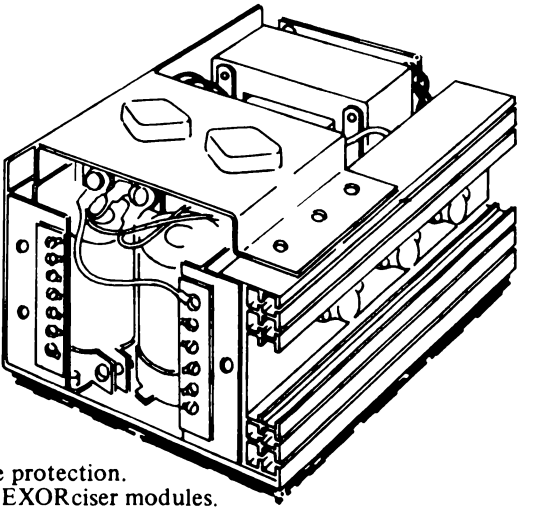
- Provides the EXORciser with eight switch-selectable baud rates between 110 and 9600.
- Provides an interface between the Debug Module and the selected data terminal
- Provides an interface between the front panel and the Debug Module

The Baud Rate Module, in conjunction with the Debug Module, enables the designer to communicate with EXbug via a data terminal. The Baud Rate Module's crystal oscillator baud rate generator (MC14411) and baud rate switch provide the EXORciser with eight standard rates. This module also interconnects the Debug Module to a data terminal and with the front panel. Included with the module is the front panel interconnect cable.

Specifications

Baud Rates: (Switch Selectable)	**110,150,300,600,1200, 2400,4800, and 9600**
Physical Dimensions: W x H x T	**3.688 x 5.25 x 0.062 in.**

Power Supply



- Provides all required EXORciser voltages
- Capable of supporting a full EXORciser rack of Modules

The power supply provides the EXORciser with +5 Vdc, +12 Vdc and -12 Vdc power sources. The +5 Vdc regulated source has both overload and overvoltage protection. This power source is capable of driving a complete rack of EXORciser modules.

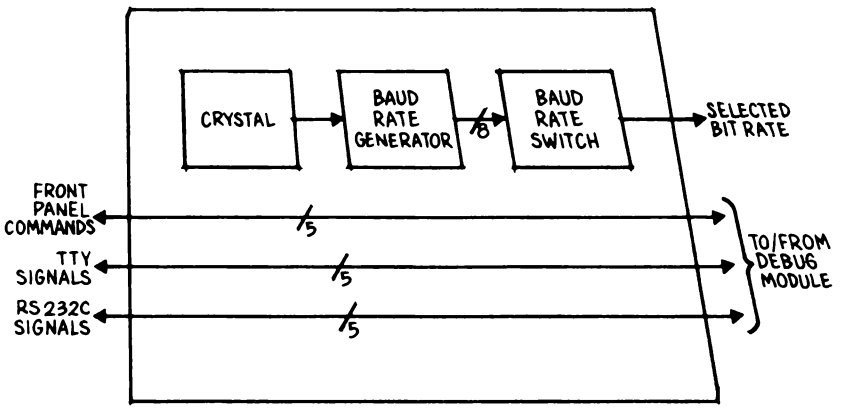
The +12 Vdc and -12 Vdc sources are used to power portions of the interface circuitry between the EXORciser and a data terminal. These sources have overload protection and may be used to power custom circuitry on other modules.

Specifications

Output Voltages:	**+5 Vdc @ 15 A**
	-12 Vdc @ 1.5 A
	+12 Vdc @ 2.5 A
Input Voltage:	**95-125/205-250 Vac**
Input Frequency:	**47 to 420 Hz, Single Phase**
Physical Dimensions: L x W x H	**9.50 x 6.25 x 5.00 in.**

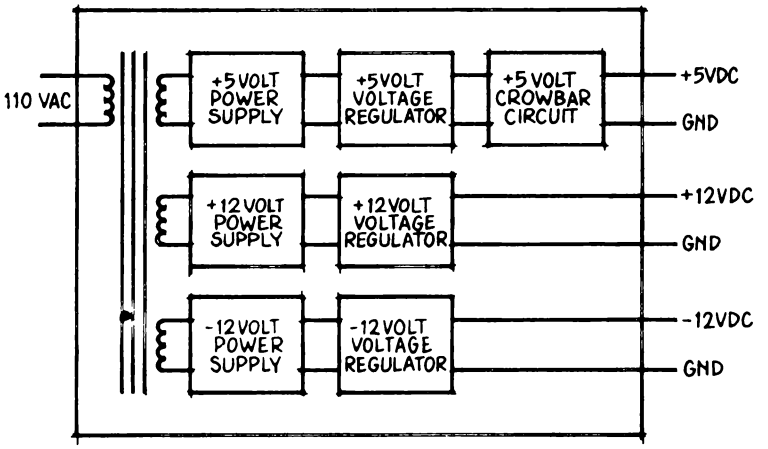
Baud Rate Module

Resident

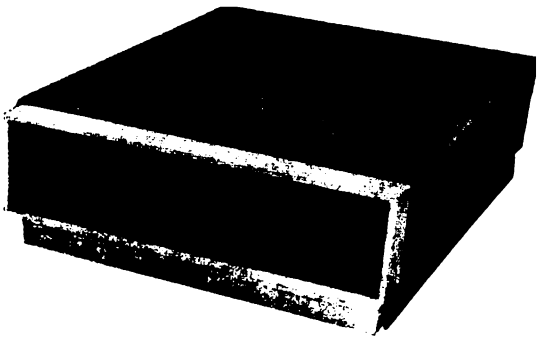


Power Supply

Resident



M68SDT II EXORciser II Development System



The EXORciser II Development System is the basic tool for designing and developing microprocessor-based systems using any of Motorola's families of microprocessor and microprogrammable parts. It is an extremely powerful and easy-to-use development system that has been designed to be highly user-oriented in order to reduce system development time and cost. The EXORciser II incorporates several advanced features, including Dual Memory Map mode of operation and the ability to develop higher performance systems using the MC68A and MC68B series parts (1.5 MHz and 2.0 MHz, respectively). In addition, a totally new set of optional support modules has been incorporated to meet the increased capabilities of EXORciser II.

Features

- Versatile and easily expandable design development tool used to evaluate and debug the user's system hardware and software
- Dual Memory Map mode of operation
- Selectable clock speeds of 1.0 MHz, 1.5 MHz, and 2.0 MHz
- 8 selectable baud rates from 110 to 9600 baud
- A single RS-232C compatible serial communications interface
- A chassis containing a 14-card motherboard and the necessary +5 Vdc and ±12 Vdc power supplies

Specifications

Power Requirements	95–135/205–250 Vac 47–420 Hz 250 W
Word Size	
Data	8 bits
Address	16 bits
Instruction	8, 16, and 24 bits
Memory Capability	65,536 bytes (maximum)
Instructions	72, variable length
Clock Signal	Crystal controlled 12 MHz with logic for generating 2-phase non-overlapping signal to MPU and system bus
Memory Speed	Jumper selectable 1.0, 1.5, or 2.0 MHz
Interrupt	Maskable and nonmaskable
Data Terminal Interface Characteristics	
Baud Rates (Jumper Selectable)	110, 150, 300, 600, 1200, 2400, 4800, and 9600
Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
Reader Control Signal	Control signal for TTY devices modified for external control
Operating Temperatures	0 to 55°C

Description and Operation

The basic EXORciser II contains the common ingredients of a microcomputer, and offers the system designer a low-cost, versatile means of achieving unique final-system performance through the selective addition of separately available, optional modules. These separate assemblies plug directly into the EXORciser's bus so that system expansion becomes quick, easy, and essentially error-proof. With provisions for up to 10 add-on assemblies, a system of almost any complexity can rapidly be assembled.

Supplied with the basic EXORciser II are the MPU II Module, the DEbug II Module. The DEbug II Module supplies eight selectable baud rates, and serves as a communication link between the terminal and the EXbug 2 Firmware on the DEbug Ii Module.

The MPU II Module provides the 1.0, 1.5, or 2.0 MHz clock timing for the microprocessor system under development, as well as for the rest of the EXORciser II. In addition, this module houses the MC68B00 Microprocessing Unit, which imparts to the EXORciser its computation and control capabilities. Also included are a Timer, MC6840, and Priority Interrupt Controller, MC6828.

The DEbug II module is a system development tool which provides the user with instant capability to communicate with his system, load programs, monitor the execution of his program in real time, and to isolate and analyze hardware and software problems. The DEbug II module places no restrictio.is upon the user's system design since all 64K bytes of memory space are available to the user.

These functional subsystems of the basic EXORciser are supplemented by a power supply and a bus-oriented distribution system. This bus system transfers the power supply voltage (as well as the data, address, and control signals) to the optional modules. Overall, the EXORciser can address up to 64K bytes of memory, and addresses the input/output modules (as well as the memory modules) as memory.

In order to provide the user additional flexibility, the appropriate EXORciser II modules have a 20-pin connector available for implementation of such system capabilities as priority interrupts, multi-paged memory and I/O systems, parity error detection, and power down/restart features.

Furthermore, the modules will have a standard jumpering arrangement for assigning memory and peripherals to either map in the dual map mode or to any page-extended memory systems.

Microcomputer Design With EXORciser II

A design normally begins by defining the functions to be performed by the proposed system. This is followed by design of both hardware and software and trade-off decisions between them.

Using the appropriate memory and input/output modules, the designer now emulates his proposed system in the EXORciser. Recognizing that some systems may require special interface circuitry and customized circuitry, provisions have been made on the input/output modules for the designer to insert wirewrap sockets and construct the special interface circuitry. Also, the designer can construct any customized circuitry on the Wirewrap Module.

The EXORciser II resident software provides the designer with a powerful software development tool. Using the Resident Editor, the designer enters a source program via the terminal keyboard. The user now can modify and change his source program as required to meet his proposed systems requirements. This includes:

- Printing out all or any part of the program for detailed examination
- Changing any characters or string of characters in the source program
- Deleting or adding instruction lines or characters anywhere in the program

At the end of the editing process, the Resident Editor will provide a source program that may be stored on paper tape, cassette, or diskette. This source program may be used in subsequent assembly operations on any of the compatible Motorola assemblers and cross assemblers. The EXORciser's Resident Macro Assembler can be used to translate the source program to produce:

- A printed assembly listing of the source program
- An object program on paper tape, cassette, or diskette
- A machine file, consisting of the machine-coded program stored directly into the EXORciser II memory. This option permits the program to be executed immediately after assembly with no need for subsequent loading

During the assembly process, the Macro Assembler allows the assignment of relocatable memory addresses which are assigned by the Linking Loader at load time, rather than fixed during the assembly operation.

Once the designer has configured the EXORciser II to emulate his hardware and has developed his software, he is ready to debug his system. The EXORciser II, with its EXbug 2 system development firmware, permits the user to debug both his system hardware and his system software, as required, until he has his system operating correctly.

Modules (Included With The EXORciser II)

MPU II Module

- 68B00-Based
- 1.0, 1.5, 2.0 MHz Clock Speeds
- Programmable Timer (MC6840)
- Priority Interrupt Controller (MC6828)
- Refresh Control
- Go/Halt Control
- User-Controlled Three-State Logic
- Internal or External Clock Option
- IRQ and 8-Level Interrupt Control
- Generation of $\phi 1$, $\phi 2$ and Memory Clock

The MEX6800-2 MPU Module includes both the system clock and the MC68B00 Microprocessing Unit (MPU). The MPU Module also automatically initiates an EXORciser RESTART when power is first applied to the EXORciser.

The clock circuit generates 1.0, 1.5, or 2.0 MHz clock signals. The system may be operated with an external clock over the range 800 kHz to 2.0 MHz.

In addition to generating the basic EXORciser II timing signals, the clock circuit provides the EXORciser with the capability of refreshing dynamic memories and working with slow memories. The dynamic memories are refreshed on a cycle-stealing basis. In working with slow memories, the MPU Module stretches the clock pulse to give the memory sufficient time to complete its assigned operation.

Debug Module

- EXbug 2 System Monitor Firmware (3K bytes)
- System Console Interface
- Dual Map Address Control
- STOP-ON-ADDRESS/SYNC ENABLE
- Power Up/Restart Control
- Load, Verify, Search Tape
- Display, Change Memory and MPU Registers
- Trace Instruction(s)
- Set Up to 8 Software Breakpoints
- Search Memory
- Line Printer Echo Option
- Parity Detect

The DEbug II Module, through its EXbug 2 firmware and associated hardware, provides the EXORciser II with its powerful hardware/software debug capability.

Using the EXbug routines provides the designer virtually unlimited freedom in examining and debugging his proposed system hardware and software. He can, for example, search the input medium for a file, load a file into EXORciser memory, verify the contents in the EXORciser memory, print out the contents of the EXORciser memory, and record the memory contents on the selected medium.

In between these input/output functions, the user can examine and, if required, change the memory contents. He can insert and remove one hardware breakpoint and up to eight software breakpoints. He also can run in real time or trace through the user's program or a selected portion of the user's program. While using these routines, the user modifies his hardware and software, as required, until he has his system operating to specifications.

The STOP-ON-ADDRESS/SYNC ENABLE switch on the DEbug Module is used to generate a sync pulse at a preselected address or to enable the hardware breakpoint function.

The DEbug II Module provides the EXORciser II with the ability to address two separate 64K memory maps (Dual Map mode). To accomplish this, the DEbug II Module takes the Valid Memory Address (VMA) signal from the MPU II Module and converts it to two other signals: Valid User Address (VUA) and Valid Executive Address (VXA). All EXORciser II hardware modules may be configured to respond to one of these enabling signals. As a result, two complete maps of 64K bytes are addressable for either random access data storate or for data I/O.

A serial I/O port allows interfacing with any RS-232C compatible terminal. Baud rates are selectable from 110 baud to 9600 baud. The module also interfaces to the EXORciser's front panel RESTART and ABORT switches.

The RESTART and ABORT push-button switches allow manual termination of program execution.

RESTART initializes the EXORciser II system and, depending upon the EXbug/USER toggle switch setting, forces program execution to start at either the EXbug 2 or the user's restart vector address.

ABORT generates a non-maskable interrupt and returns program control to the EXbug firmware.

Random Access Memory

Dynamic RAM

- 1.0, 1.5, 2.0 MHz Clock Speeds
- Individual Address and Enable for Each 16K Block
- System Cycle Stealing Refresh
- 16, 32, 48, 64K Single Board Versions
- Dual Map and Page Control
- Standard Parity

Static RAM

- Clock Speed Independent to 2.0 MHz
- RAM/ROM Mode Selection
- 8, 16K Single Board Versions
- Low Power
- Individual Address and Enable for Each 8K Block
- Standard Parity
- Dual Map and Page Control

Ordering Information

The following table lists information necessary for ordering the EXORciser II hardware and software options.

Type No.	Description
M68SDT2-2DM	EXORciser II Development System, 220 V with Dynamic Memory (32 K)
M68SDT2-2SM	EXORciser II Development System, 220 V with Static Memory (32 K)
M68SDT2-2X	EXORciser II Development System, 220 V without Memory

Optional Assemblies

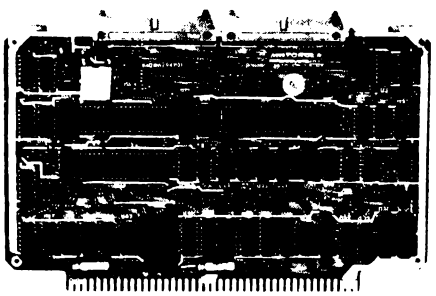
MEX6800-2	MPU II Module
MEX68DB2	DEbug Module
MEX6816-22D	16K Dynamic RAM Module with Parity
MEX6832-22	32K Dynamic RAM Module with Parity
MEX6848-22	48K Dynamic RAM Module with Parity
MEX6864-22	64K Dynamic RAM Module with Parity
MEX6808-22	8K Static RAM Module with Parity
MEX6816-22S	16K Static RAM Module with Parity
MEX6821-2	PIA Input Output Module 2
MEX6850-2	ACIA SSDA Module II
MEX68PI2	Printer Interface Module II
MEX68SA2	Systems Analyzer II
MEX68PP3A	PROM Programmer III with Software on Cassette
MEX68PP3B	PROM Programmer III with Software on Paper Tape
MEX68PP3M	PROM Programmer III with Software on MDOS Diskette

Type No.	Description
MEX68USM	Universal Support Module
MEX68488	GPIA Support Module
MEX6845	CRT Contoller Module
MEX6854	MC6854 ADLC Support Module
MEX68WW	Wirewrap Module
MEX68XT	Extender Module

Software Programs

M68XAE6813A	Resident Editor/Assembler on Cassette
M68XAE6813B	Resident Editor/Assembler on Paper Tape
M68MASR010A	Resident Relocatable Macro Assembler and Linking Loader on Cassette
M68MASR010B	Resident Relocatable Macro Assembler and Linking Loader on Paper Tape
M68SMDOS100	Resident Editor/Assembler/Relocatable Macro Assembler and Linking Loader with Disk Operating System on MDOS Diskette
M68BASR010A	Resident BASIC Interpreter on Cassette
M68BASR010B	Resident BASIC Interpreter on Paper Tape
M68BASR010M	Resident BASIC Interpreter on MDOS Diskette
M68MPLR010M	Resident MPL Compiler on MDOS Diskette
M68FTNR012M	Resident FORTRAN Compiler and Linking Loader on MDOS Diskette
M68COBOL010M	Resident ANS COBOL Compiler on MDOS Diskette

MEX3870M MC3870 Development System



- Emulator Module mounts directly into the EXORciser or EXORterm
- Real-Time Emulation of the 3870 single chip microprocessor
- Cable extension terminated by a 40-pin male connector inserts directly into the user's 3870 socket
- Dual memory map consisting of RAM and PROM
- RAM allows software development in the EXORciser or EXORterm environment
- PROM allows field verification of firmware prior to committing to mask programmed 3870s
- 3870 Cross Assembler on MDOS diskette
- Control software that allows evalution and debug of of programs under development

The 3870 plug-in module provides the EXORciser or EXORterm user with virtually all of the processing and control power of a 3870 single chip microcomputer. "TEST LOGIC" is the only function that is not provided by the emulator. The CPU functions, I/O ports 0 and 1, and the 64-byte scratchpad RAM are implemented using a 3850. The Data Counter and Program Counter functions are implemented with a 3853 STATIC MEMORY INTERFACE (SMI), while the 3870's ROM is emulated using RAM. The module contains 3K bytes of read/write memory, 2.5K of which is available to the user for program development. I/O ports 4 and 5, interrupt, and timer logic are provided by a 3871 PERIPHERAL INPUT OUTPUT (PIO) device.

In addition to the RAM, the module contains a socket for a 2K x 8 PROM (2716). This non-volatile storage affords verification of the user's firmware in an environment external to the EXORciser or EXORterm.

EM3870, the controlling software for the emulator module, permits the user to perform EXAMINE and CHANGE operations on the various programmable registers and memory, including the CPU scratchpad. The repertoire of functions also includes the ability to insert, display, and remove up to eight breakpoints in the user program. See Figure 1 for a description of the available USER commands.

The 3870 Cross Assembler requires approximately 24K of memory in conjunction with MDOS, and provides an object file on disk from the 3870 source code. Using the "LOAD" command in EM3870, this file may then be loaded into the Emulator Module for subsequent debug of the hardware and software.

The 3870 Module can operate independently of the EXORciser or EXORterm once the user has debugged his program by putting his program in a 2K EPROM in the socket provided for it on the module. See Figure 2 for an example of Stand Alone operation.

Minimum System Requirements

EXORciser or EXORterm
MDOS
Editor
24K Memory Total

EM3870 Command	Description
.A	Examine/change the user's Accumulator
.C	Continue execution at current program location counter
n.D	Examine/change user's Data Counter n (n = 0 or 1 only)
n.E	Execute the specified number of user instructions from the current program counter location with a register printout only after the last instruction
.G	Go to the program under test through its restart vector
.I	Examine/change the user's Indirect Scratchpad Address Register
n.L	Examine/change the user's location (Program) Counter n (n = 0 or 1 only)
.N	Trace the next instruction
n.O	Calculate the address offset (for branch instructions)
n.P	Examine/change the contents of Port n (n = 0,1,4,5, or 7 only)
.R	Examine the user's Registers
n.S	Examine/change scratchpad byte n (n = 0,1,2,...3F)
.T	Toggle the trace mode
.U	Remove breakpoints
.V	Display breakpoints
.W	Examine/change the user's Status Register
.X	Exit EM3870 and return to MAID
n/	Examine/change the contents of memory location n
(LF)	Display the contents of the next sequential memory location (LF – Line Feed character)
(space)	Display the contents of the next sequential memory location (SPACE – Space Bar character)
(CR)	Return the displayed contents to memory and accept the next command (CR – Carriage Return character)
LOAD	Load object file from DISC
SAVE	Write object file to DISC

Figure 1. User Commands

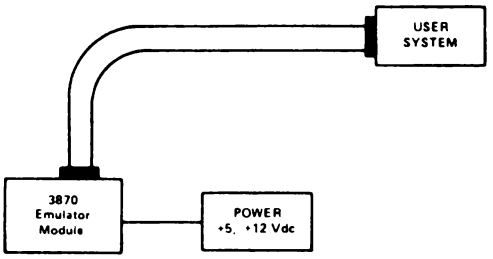


Figure 2. Stand Alone Operation

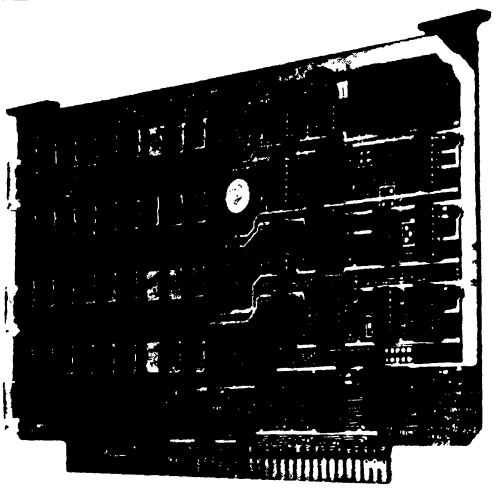
Ordering Information

Part Number	Description
MEX3870M	3870 Emulator, including Cross Assembler (EXORciser or EXORterm) and Emulator package (Module and Software)
MEX3870(D)	MC3870 Emulator User's Guide

MOTOROLA

MICROSYSTEMS

MEX6808-22
MEX6816-22
8K/16K Static RAM Modules



- 16,384 x 8 bits of static N-channel MOS memory in two arrays (16K module). 8192 x 8 bits of static N-channel MOS memory in single array (8K module).
- 1 MHz to 2 MHz memory speed
- Switch selectable base memory address for each memory array
- Switch selectable RAM/ROM for each memory array
- 4 pin header for implementation of multi-paged memory or parity error detection.
- Jumper selectable User Map or EXbug II Dual map
- Standby/power down options provided on module.
- TTL voltage compatible impedance inputs

The MEX6808-22S (8K, 2 MHz) Static RAM Modules consisting of eighteen 4096 x 1-bit static RAM devices provides the Development System with 8192 x 8 bit bytes of random access memory. The memory is organized in a single array. A base address switch permits the user to select base memory addresses in 8K increments.

The MEX6816-22S (16K, 2 MHz) Static RAM Modules consisting of thirty-six 4096 x 1-bit static RAM devices provides the Development System with 16,384 x 8 bit bytes of random access memory. The memory is organized into two 8192 x 8 bit byte arrays. Two base address switches permit the user to select base memory addresses for both arrays in 8K increments.

A RAM/ROM switch for each array permits the user to program the array to function as RAM or ROM. Address decoders on the module monitor the 16 address lines and determine when the system MPU is addressing their respective memory arrays. A logic circuit decodes inputs, reads the RAM/ROM switches, and determines the memory function to be performed – read data from memory, write data into memory, or inhibit the memory write function. The module circuitry generates and detects even parity. The module outputs a parity error signal to the system whenever a parity error is detected.

A Power Fail/Power Down option is provided on the module. In this mode, power is applied only to the memory arrays and power fail/power down circuitry. A control signal from the system bus is required to maintain this mode of operation.

Specifications

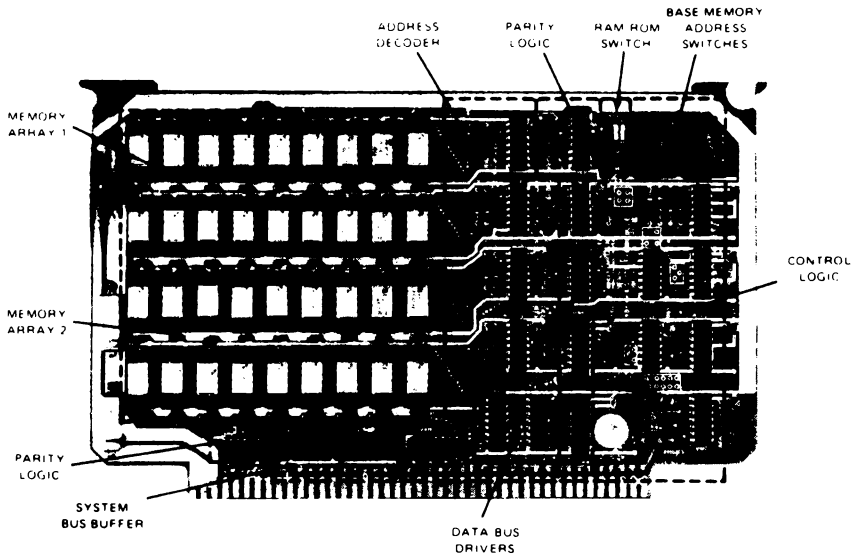
Type Memory	N-channel MOS Static RAM
Memory Speed	1.0 MHz to 2.0 MHz
Memory Organization	16,384 x 8 bits (two 8192 x 8 bit arrays) 16K, 8192 x 8 bits (single array) 8K.
Parity	Even
Read Access Time	230 ns from leading edge of memory clock
Input Signals	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	5 Vdc @ 2.6 A (max)
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in

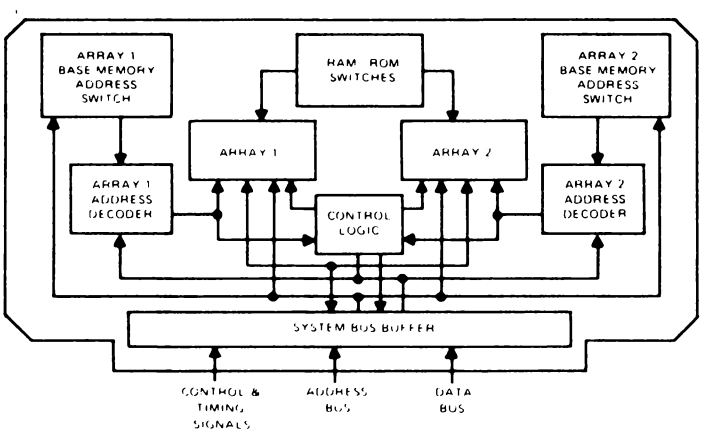
Ordering Information

The following table lists the information necessary for ordering modules or manuals.

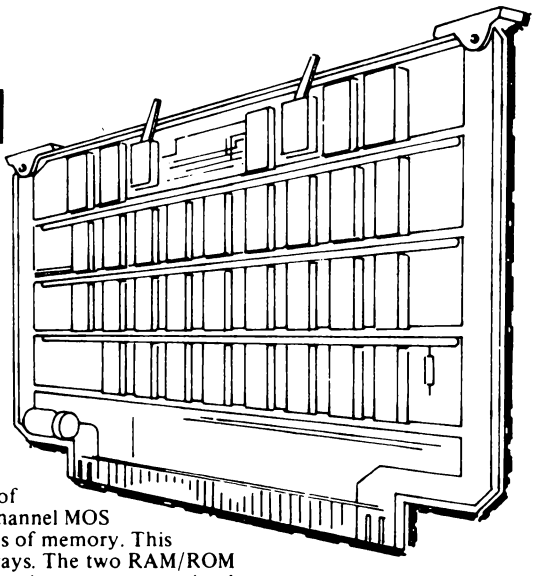
TYPE NUMBER	DESCRIPTION
MEX6808-22S	8K, 2.0 MHz Static RAM Module
MEX6816-22S	16K, 2.0 MHz Static RAM Module
MEX68162(D)	User's Guide (covers all versions)

MEX6808-22, MEX6816-22 8K/16K STATIC RAM MODULES





MEX6812-1 2K Static RAM Module



- 2048 x 8 bits of static N-channel MOS memory in 1K byte arrays
- Switch-selectable base memory address for each 1K RAM array
- Switch-selectable RAM/ROM (inhibited memory write function) capability for each array
- 500 nanosecond memory access time
- TTL voltage compatible
- Bus interface driver capability

The MEX6812-1 2K Static RAM Module, consisting of sixteen 2102-1 1024 x 1-bit RAMs or equivalent N-channel MOS memories, provides the EXORciser with 2048 x 8 bits of memory. This memory is organized into two separate 1024 byte arrays. The two RAM/ROM switches on the module determine whether their respective arrays are to simulate one (1024 x 8-bit) MCM6830 ROM or eight (128 x 8-bit) MCM6810 RAMs. Three-state bus buffers interface this module to the M6800 MPU over the EXORciser system bus.

The designer can select the base memory address, in 1024 bit increments, for each memory array by setting of the base memory address switches. Address decoders on this module monitor the 16 address lines and determine when the EXORciser's MPU is addressing their respective memory arrays. A logic circuit decodes three inputs, reads the RAM/ROM switches, and determines the memory function to be performed read data from the memory, write data into the memory, or inhibit the memory write function.

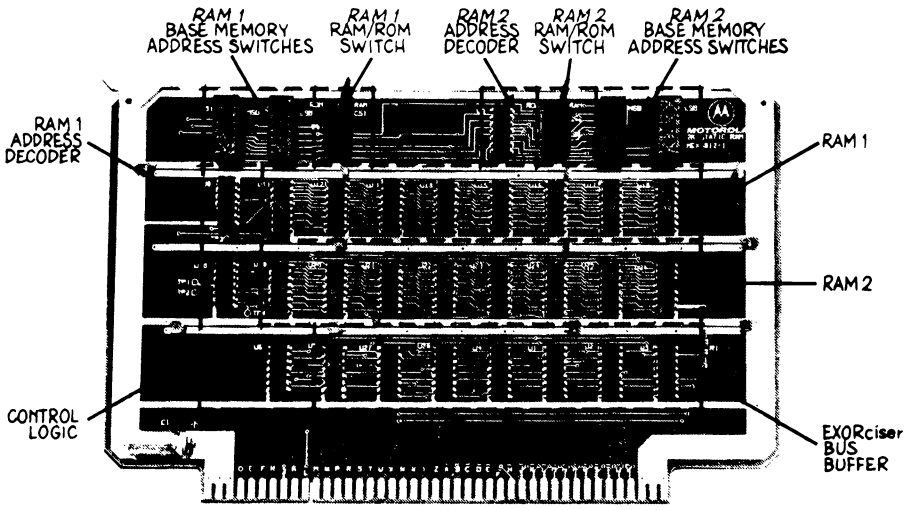
Specifications

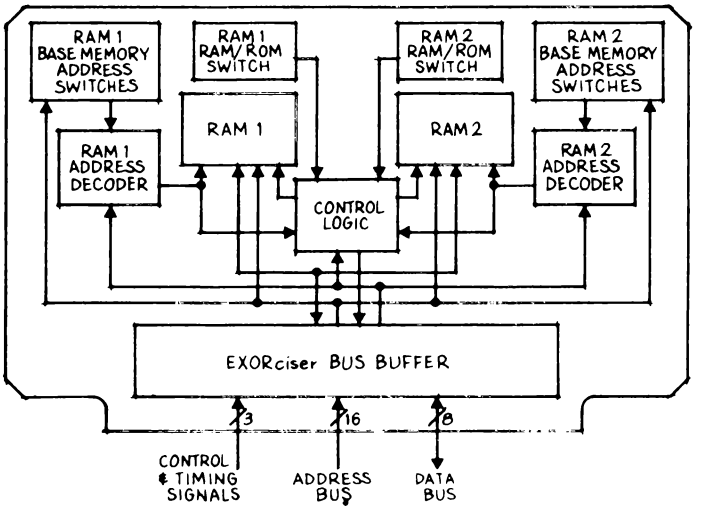
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Type Memory	MOS Static RAM
Memory Organization	2048 x 8 bits organized into two 1024 x 8 bit arrays
Memory Cycle Time	500 ns
Input Signals	TTL voltage compatible
Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	5 Vdc @ 1 A Max.
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

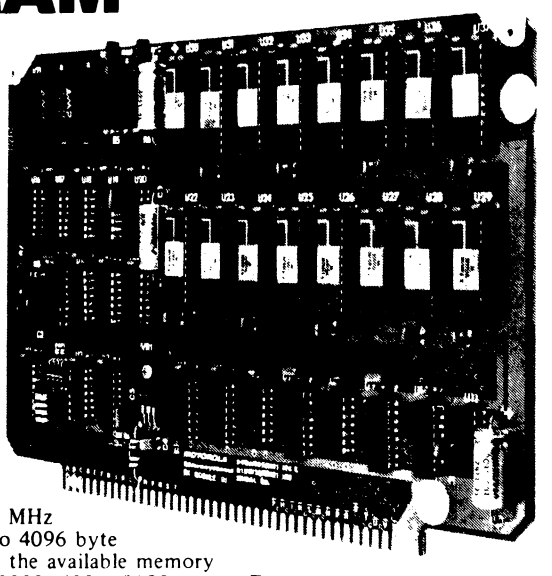
MEX6812-1
2K Static RAM Module

Option





MEX6815-3 8K Dynamic RAM Module



- 8192 x 8 bits of dynamic NMOS memory in two 4096 byte arrays
- Switch selectable base memory address for each memory array
- Each array switch selectable as RAM or ROM (RAM protected by inhibiting memory write function)
- Fully decoded or partial decoded module address selection
- Cycle stealing memory refresh operation
- TTL voltage compatible
- Bus driver capability
- Operates up to 1.5 MHz system clock

The MEX6815-3 8K Dynamic RAM Module consists of sixteen MCM6605, or equivalent, N-Channel MOS memory devices that provide the EXORciser with 8192 x 8 bits of memory which will operate up to 1.5 MHz system clock. This memory module is divided into two 4096 byte memory arrays which may be located anywhere within the available memory map by means of two base memory address switches (0000, 4096, 8192, etc.). For added flexibility, this module has an address line select switch for full or partial decoding of address lines and two ROM/RAM switches that inhibit the memory write capability thereby causing the RAM memory to look like ROM memory.

This module interfaces to the M6800 MPU over the EXORciser system bus via three-state bus buffers. Control logic initiates a memory refresh operation once every 32 μs; the module refreshes its memory on a cycle stealing basis.

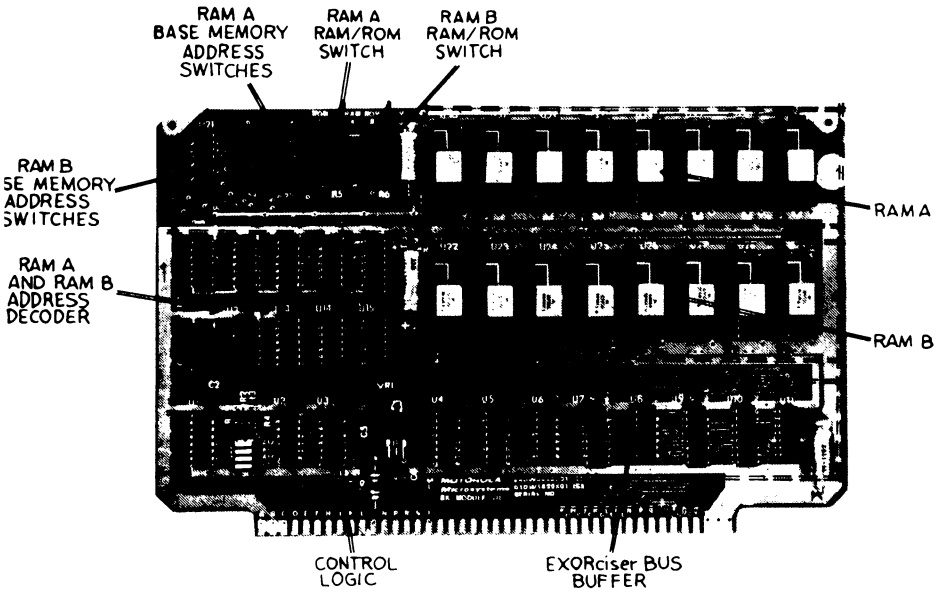
Specifications

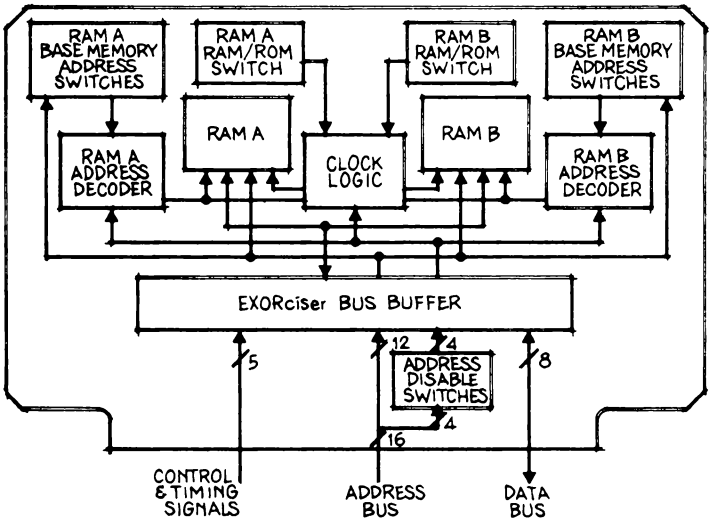
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Type	N-Channel MOS Dynamic RAM
Memory Organization	8192 x 8 bits organized into two 4096 x 8-bit arrays
Cycle Time	750 ns
Read Access Time	350 ns from memory clock
Input Signals	
Control Bus	
Logic "0"	0.0–0.8 V (–200 μA max at 0.5 V)
Logic "1"	2.0–5.25 V (25 μA max at 5.25 V)
Address Bus	
Logic "0"	0.0–0.8 V (–500 μA max at 0.5 V)
Logic "1"	2.0–5.5 V (80 μA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0–0.8 V (200 μA max at 0.5 V)
Input Logic "1"	2.0–5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at –10 mA through a resistor to ground
Operating Temperature	0° to 70°C
Power Requirements	+5 V at 600 mA +12 V at 250 mA –12 V at 50 mA
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

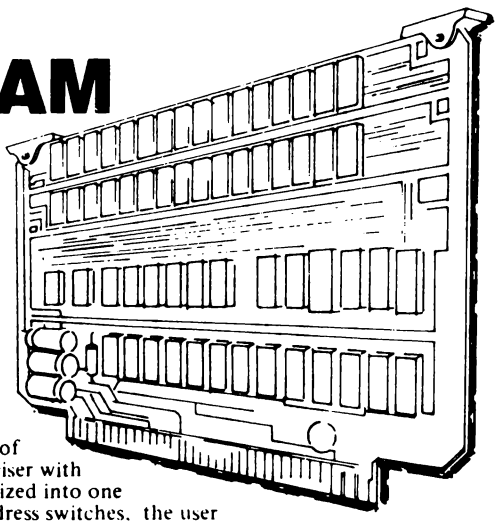
MEX6815-3
8K Dynamic RAM Module

Option





MEX6816-1 16K Dynamic RAM Module



- 16,384 x 8 bits of dynamic NMOS memory in one array
- Switch selectable base memory address for the memory array
- Cycle stealing memory refresh operation
- Optional even parity capability (consult factory)
- TTL voltage compatible
- Bus drive capability

The MEX6816-1 16K Dynamic RAM Module, consisting of 32 N-Channel MOS memory devices, provides the EXORciser with 16,384 bytes of dynamic memory. This memory is organized into one 16K memory array. Through use of the base memory address switches, the user can select one of four base memory addresses: 0, 4000_{16}, 8000_{16} or $A000_{16}$.

The address multiplexer in a refresh operation selects the memory location to be refreshed. The address decoder determines when the MPU is addressing its memory array and enables the control logic circuits. The control logic now decodes its control and timing inputs and determines the module's operation. Working with the EXORciser bus buffer, it controls the address multiplexing required by the memory devices. The control logic also decodes the Read/Write command and determines whether the module is to perform a memory read or memory write operation.

The control logic initiates a memory refresh operation once every 32 μs and the module refreshes its memory on a cycle stealing basis.

The optional parity circuit generates a parity bit during a memory write operation and checks that data during a memory read operation. On detecting a parity error, the circuit generates the PARITY ERROR and $\overline{\text{PARITY ERROR}}$ flag signals. Consult the factory for details on this option.

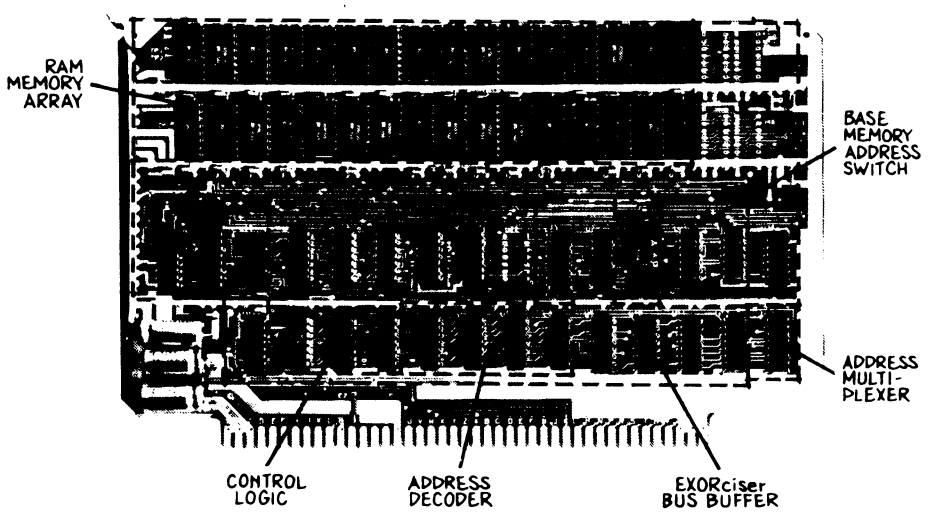
Specifications

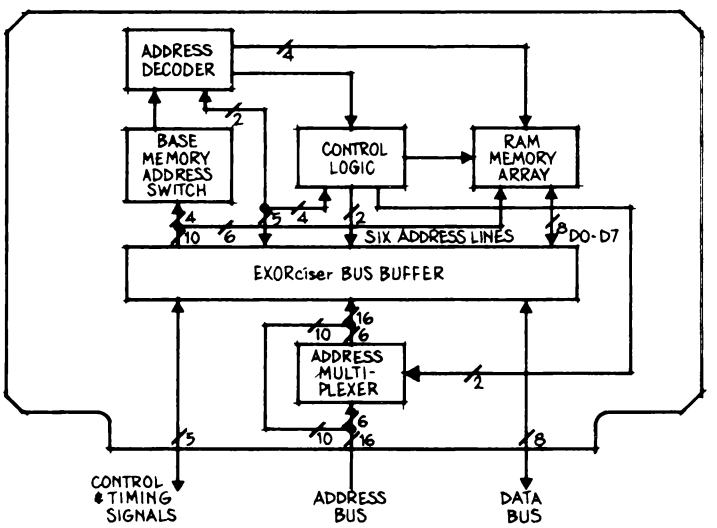
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Type	N-channel MOS dynamic RAM
Memory Organization	16,384 x 8 bits organized into one array
Parity	Optional even parity – consult factory
Read Access Time	350 ns from row address strobe (approximately 300 ns from memory clock)
Input Signals	TTL voltage compatible
Control Lines	
Logic "0"	0.0-0.85 V (-200 μA max at 0.4V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Address	
Logic "0"	0.0-0.8 V (-2.0 mA max at 0.5 V)
Logic "1"	2.0-5.25 V (1.0 mA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at -40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Operating Temperature	0 to 70° C
Power Requirements	+5 Vdc at 1.5 A max +12 Vdc at 1.6 A max -12 Vdc at 110 mA max
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

MEX6816-1
16K Dynamic RAM Module

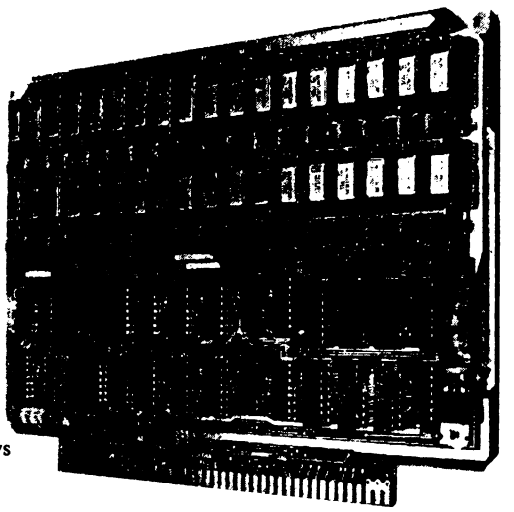
Option





MOTOROLA

MEX6816 — 1 HR
MEX6832 — 1 HR
MEX6848 — 1 HR
MEX6864 — 1 HR
16K / 64K Hidden Refresh RAM Module



- 16,384 x 8 bits of dynamic NMOS memory (16K), 32,768 x 8 bits (32K), 49,152 x 8 bits (48K), or 65,536 x 8 bits (64K) organized into one memory array of 4 rows
- Memory refresh without processor interruption
- Jumper selectable memory map assignment
- 20-pin header for implementation of priority interrupts, multi-paged memory, and I/O systems
- Even parity with jumper selectable outputs
- TTL voltage-compatible high-impedance inputs

The MEX6816-1HR Hidden Refresh RAM Module consisting of 9 N-Channel MOS memory devices provides the system with 16,384 bytes of memory. The MEX6832-1HR consists of 18 devices with 32,768 bytes, the MEX6848-1HR consists of 27 devices with 49,152 bytes, and the MEX6864-1HR consists of 36 devices with 65,536 bytes of memory. The memory is organized into independently addressable rows of 16K memory each.

The Development System is designed to operate on a two-phase clock. Phase 1 is dedicated to internal MC6800 MPU operations. Phase 2 is used to access external memory. During $\phi 1$ of the cycle, when memory is not being accessed, one row of memory is refreshed.

The module circuitry generates and detects even parity. A parity error signal is output to the system whenever a parity error is detected. The output is jumper selectable to the system bus as a parity error, or a non-maskable interrupt.

Specifications

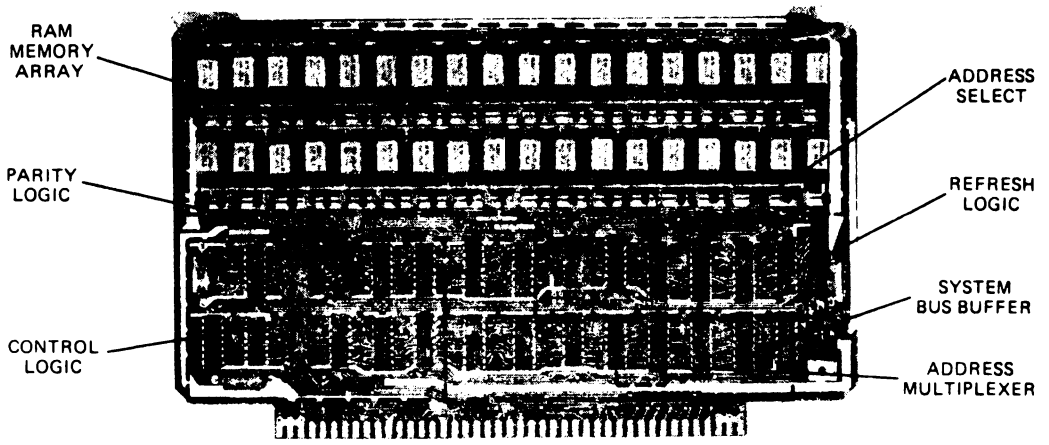
Memory Type	N-channel MOS dynamic RAM
Memory Organization	16,384 x 8 bits (16K), 32,768 x 8 bits (32K), 49,152 x 8 bits (48K), 65,536 x 8 bits (64K). 16K bits to a row
Parity	Even
Hidden Refresh	Row refresh during $\phi 1$ of each processor cycle
Input Signals	TTL voltage compatible
Control Lines	
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Address	
Logic "0"	0.0-0.8 V (2.0 mA max at 0.5 V)
Logic "1"	2.0-5.25 V (1.0 mA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Operating Temperature	0 to 70°C
Power Requirements	+5 Vdc at 1.0 A max +12 Vdc at 160 mA max -12 Vdc at 8 mA max
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

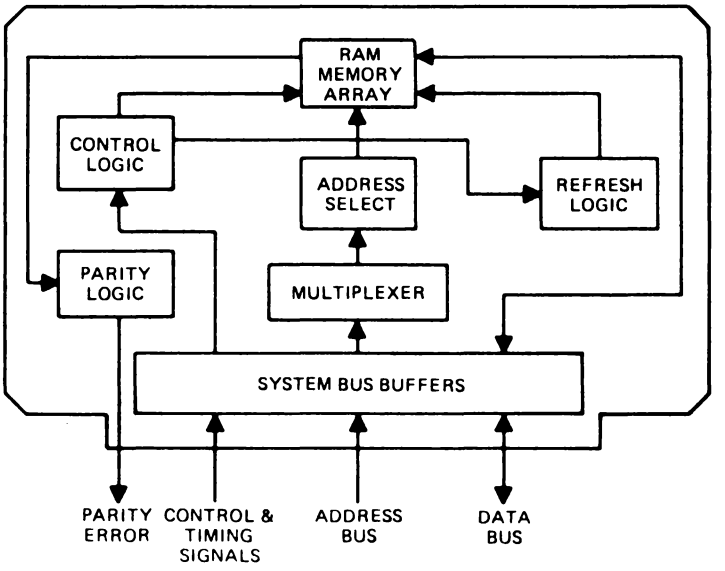
Ordering Information

The following table lists the information necessary for ordering modules, or manuals.

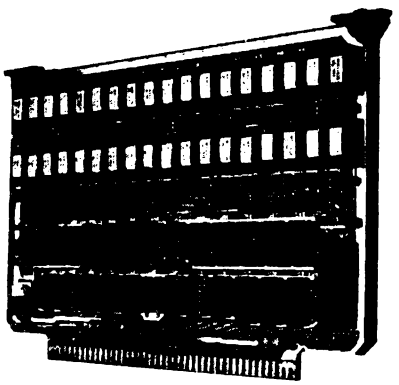
Type Number	Description
MEX6816-1HR	16K Hidden Refresh RAM Module
MEX6832-1HR	32K Hidden Refresh RAM Module
MEX6848-1HR	48K Hidden Refresh RAM Module
MEX6864-1HR	64K Hidden Refresh RAM Module
MEX6864HR(D)	User's Guide (covers all versions of module)

MEX6816 — 1 HR
MEX6832 — 1 HR
MEX6848 — 1 HR
MEX6864 — 1 HR
16K / 64K Hidden Refresh
RAM Module





MEX6816-22D
MEX6832-22
MEX6848-22
MEX6864-22
16K/64K Dynamic RAM Modules



- 16,384 x 8 bits (16K), 32,768 x 8 bits (32K), 49,152 x 8 bits (48K), or 65,536 x 8 bits (64K) of dynamic MOS memory organized in one memory array of four address rows.
- Switch selectable base memory address on 16K module.
- Jumper selectable 1 MHz, 1.5 MHz, or 2 MHz memory speed.
- Jumper selectable User Map or EXbug II Dual Map
- 20 pin header for implementation of multi-paged memory or parity error detection.
- Cycle stealing memory refresh operation.
- TTL voltage compatible high impedance inputs.
- Jumper selectable row address select disable/enable capability.

The MEX6816-22D (16K), MEX6832-22 (32K), MEX6848-22 (48K), and MEX 6864-22 (64K) Dynamic RAM Modules consisting of 36 RAM devices (16K and 64K), 18 RAM devices (32K), and 27 RAM devices (48K) provides the Development System with up to 65,536 x 8 bit bytes of memory. Multiple modules may be used to extend the memory capability. Memory is refreshed on a cycle stealing basis. When multiple modules are used, one module is the master refresh with the others as slave refresh modules.

A base address switch on the 16K module permits the user to select base memory addresses. The 32K, 48K, and 64K modules have a standard base of 0000. The module circuitry generates and detects even parity. The module outputs a parity error signal to the system whenever a parity error is detected. Memory speed is jumper selectable at 1.0 MHz, 1.5 MHz, or 2.0 MHz to allow the user to select the speed that comes closest to his system speed. A wire wrap header for row address select is factory wired. The user can disable specific rows of memory or rearrange the address order by removing and replacing jumpers.

MEX6816-22D
MEX6832-22
MEX6848-22
MEX6864-22
16K/64K Dynamic RAM Modules

Specifications

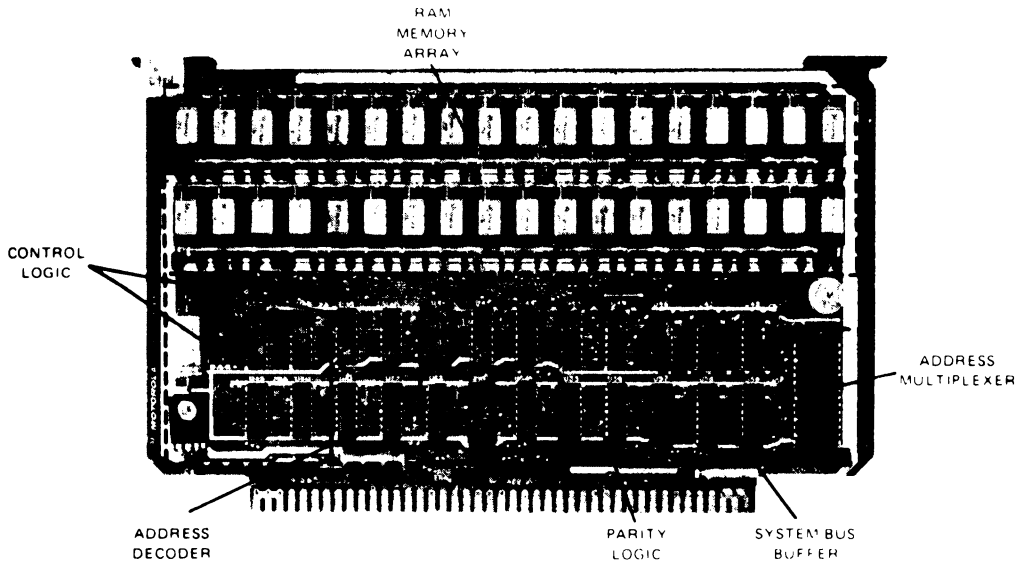
Type Memory	MOS Dynamic RAM
Memory Organization	16,384 x 8 bits (16K), 32,768 x 8 bits (32K), 49,152 x 8 bits (48K), 65, 536 x 8 bits (64) in a single array of 4 rows
Parity	Even
Read Access Time	230 ns from memory clock
Input Signals	
Control Bus	
Logic "0"	0.0 - 0.8 V (200 μA max at 0.5 V)
Logic "1"	2.0 - 5.25 V (25 μA max at 5.25 V)
Address Bus	
Logic "0"	0.0 - 0.8 V (500 μA max at 0.5 V)
Logic "1"	2.0 - 5.5 V (80 μA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0 - 0.8 V (200 μA max at 0.5 V)
Input Logic "1"	2.0 - 5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Operating Temperature	0° to 70°C
Power Requirements	+5 V at 1.5A max. +12 V at 1.6A max. -12 V at 110 mA max.
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

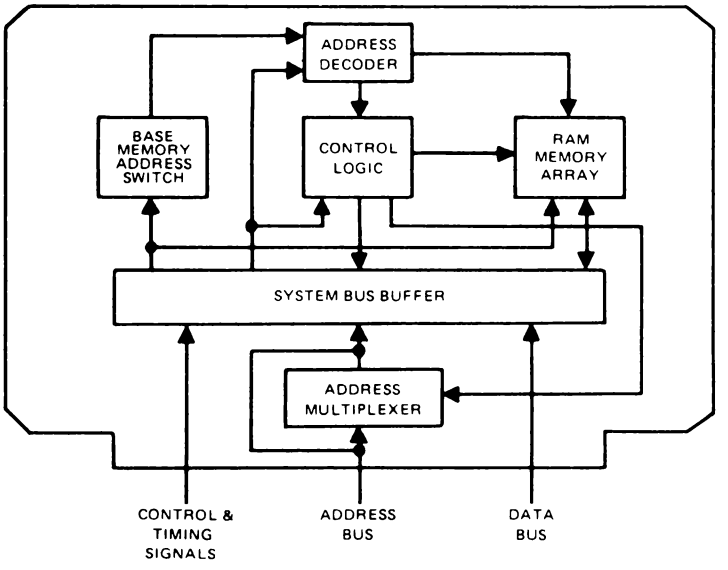
Ordering Information

The following table lists the information necessary for ordering modules or manuals.

TYPE NUMBER	DESCRIPTION
MEX6816-22D	16K Dynamic RAM Module
MEX6832-22	32K Dynamic RAM Module
MEX6848-22	48K Dynamic RAM Module
MEX6864-22	64K Dynamic RAM Module
MEX6864(D)	User's Guide (covers all versions)

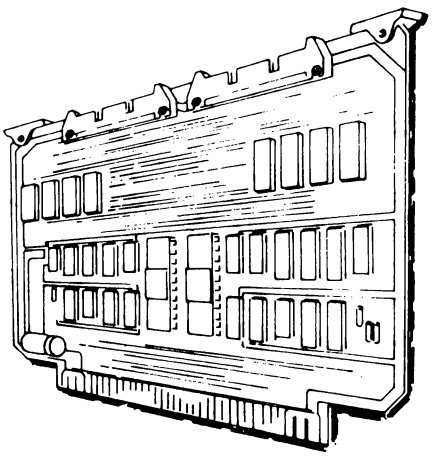
MEX6816-22D
MEX6832-22
MEX6848-22
MEX6864-22
16K/64K Dynamic RAM Modules





MOTOROLA MICROSYSTEMS

MEX6820 Input/Output Module



- Four 8-bit input/output ports for peripheral interfacing
- Eight individually controlled interrupt lines – four of which may be used as peripheral control lines
- Program controlled maskable interrupt capability
- Each MC6820 Peripheral Interface Adapter addressed as memory
- Switch selectable base memory address for each of the two MC6820 Peripheral Interface Adapter devices
- Provisions on the module for wirewrap sockets to be used in constructing custom interface circuitry

The MEX6820 Input/Output Module, containing two MC6820 Peripheral Interface Adapters (PIA's), provides a flexible means of interfacing the EXORciser with a user's defined process or peripheral device. This module, in effect, connects the two PIA's between the MPU and the peripheral device(s). The designer has the option of interfacing a peripheral directly to the PIA's TTL voltage compatible I/O ports and control lines, or through custom interface circuitry. (The peripheral interface lines of the PIA are PA0-PA7, PB0-PB7, CA1, CA2, CB1, and CB2.) The I/O Module has provisions for standard 14, 16, and 24 pin wirewrap sockets, thus permitting the construction of custom interfacing circuits on the module.

The EXORciser's MC6800 MPU addresses each of the PIA's as four locations in memory. Address switches allow the user to select base memory locations for each PIA. Altering the settings of the address enable/disable switches sets up the Input/Output Module to emulate a design that may or may not use all 16 address lines. Address decoders determine when the MPU is addressing a particular PIA's register and also signal the control logic to decode its inputs. The control logic, by decoding the MPU timing and control signals, manages the data flow through the I/O Module's buffers. These three-state buffers interface the I/O Module to the MC6800 MPU over the EXORciser bus.

MEX68IC I/O Interconnection Cables are used to connect an Input/Output Module to a peripheral. One end of this flatribbon cable is terminated with a 50-pin flatribbon connector; the other end is not terminated. Two MEX68IC cables should be ordered with each MEX6820 Input/Output Module.

Specifications

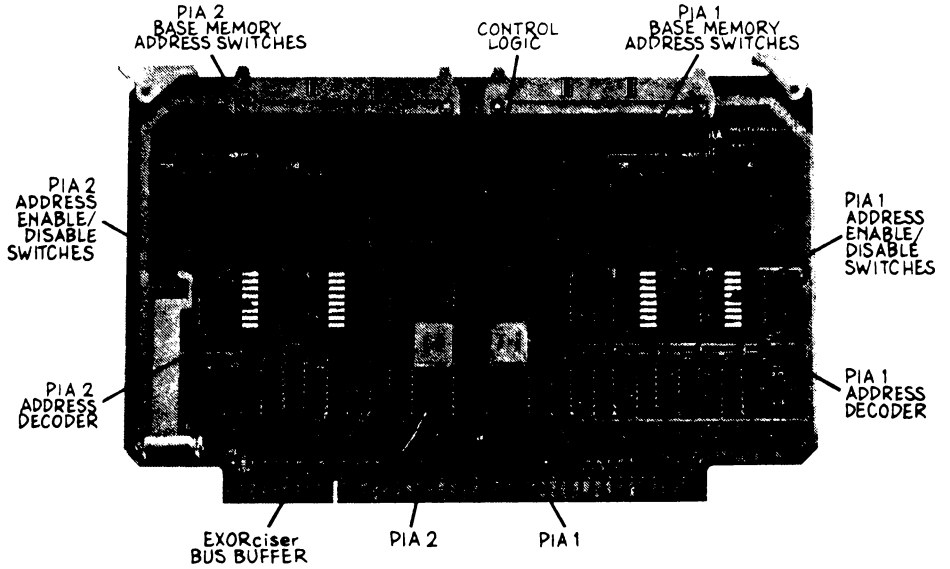
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

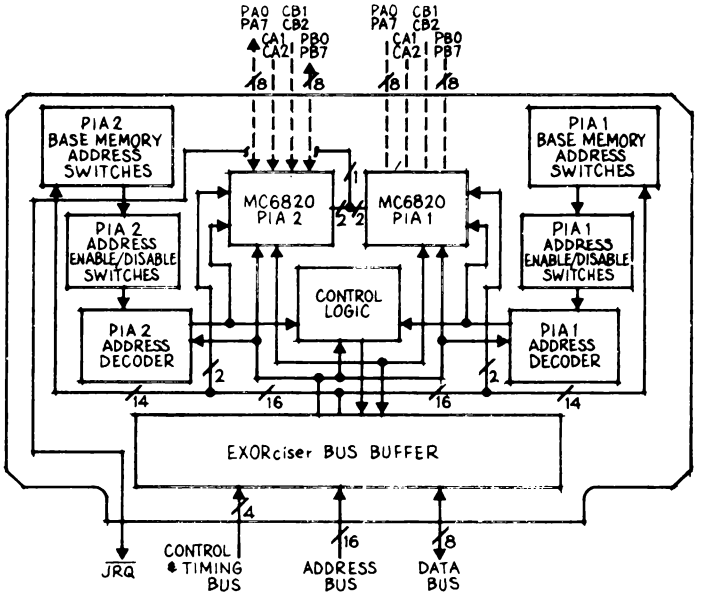
Input Signals	**TTL voltage compatible**
Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
MC6820 Peripheral Interface Adapter Signals*	
PA0-PA7 Input/Output Lines	TTL voltage compatible
PB0-PB7 Input/Output Lines	Three-state TTL voltage compatible
CA1, CA2, and CB1 Control Signals	TTL voltage compatible
CB2 Control Signal	Three-state TTL voltage compatible
IRQA and IRQB Signals	TTL voltage compatible
Operating Temperature	0 to 70°C
Power Requirements	5 Vdc at 2 A max
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

*See MC6820 data sheet for specifications on these signals.

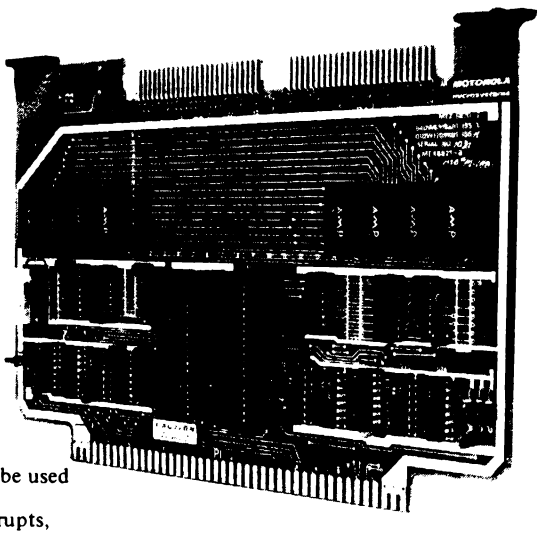
MEX6820 Input/Output Module

Option





MEX6821-2 Input / Output Module



- Four 8-bit input/output ports for peripheral interfacing
- Eight individually controlled interrupt lines – four of which may be used as peripheral control lines
- Program controlled maskable interrupt capability
- Each MC68B21 Peripheral Interface Adapter addressed as memory
- Switch selectable base memory address for each of the two MC68B21 Peripheral Interface Adapter devices
- Provisions on the module for wire-wrap sockets to be used in constructing custom interface circuitry
- 20-pin header for implementation of priority interrupts, multi-paged memory, and I/O systems
- Jumper selectable user address or EXbug 2 Dual map address
- Up to 2.0 MHz clock speed operation

The MEX6821-2 Input/Output Module, containing two M68B21 Peripheral Interface Adapters (PIA's), provides a flexible means of interfacing the Development System with a user's defined process or peripheral device. This module, in effect, connects the two PIA's between the MPU and the peripheral device(s). The designer has the option of interfacing a peripheral directly to the PIA's TTL voltage compatible I/O ports and control lines, or through custom interface circuitry. (The peripheral interface lines of the PIA are PA0-PA7, PB0-PB7, CA1, CA2, CB1, and CB2.) The I/O Module has provisions for standard 14-, 16-, and 24-pin wire-wrap sockets, thus permitting the construction of custom interfacing circuits on the module.

The M68B00 MPU addresses each of the PIA's as four locations in memory. Address switches allow the user to select base memory locations for each PIA. Altering the settings of the address enable/disable switches sets up the Input/Output Module to emulate a design that may or may not use all 16 address lines. Address decoders determine when the MPU is addressing a particular PIA's register and also signal the control logic to decode its inputs. The control logic, by decoding the MPU timing and control signals, manages the data flow through the I/O Module's buffers. These three-state buffers interface the I/O Module to the M68B00 MPU over the system bus.

MEX68IC2 I/O Interconnection Cables are used to connect an Input/Output Module to a peripheral. One end of this flatribbon cable is terminated with a 50-pin flatribbon connector; the other end is not terminated. Two MEX68IC2 cables should be ordered with each MEX6821-2 Input/Output Module.

Specifications

Input Signals	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
M68B21 Peripheral Interface Adapter Signals*	
PA0-PA7 Input/Output Lines	TTL voltage compatible
PB0-PB7 Input/Output Lines	Three-state TTL voltage compatible
CA1, CA2, and CB1 Control Signals	TTL voltage compatible
CB2 Control Signal	Three-state TTL voltage compatible
IRQA and IRQB Signals	TTL voltage compatible
Operating Temperature	0 to 70°C
Power Requirements	5 Vdc at 2 A max
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

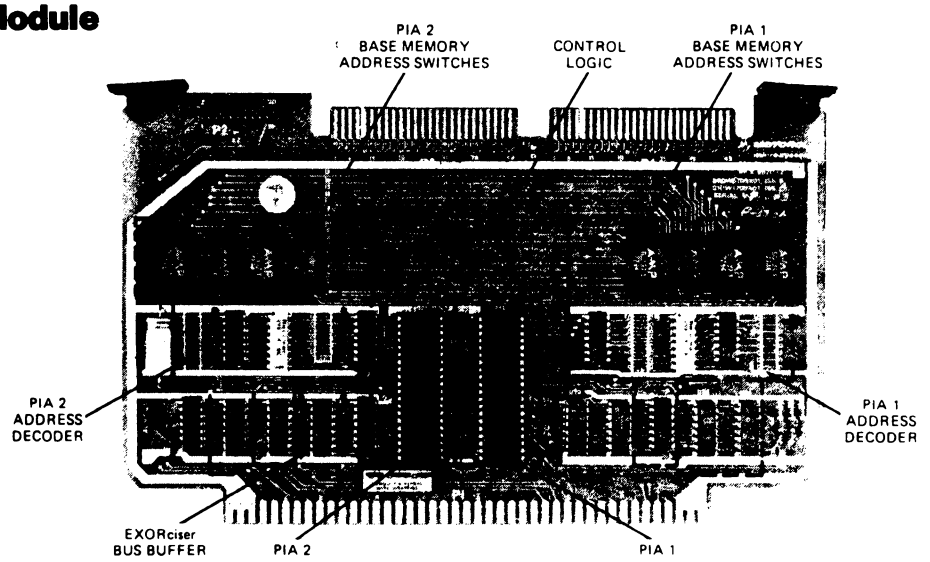
*See MC6821 data sheet for specifications on these signals.

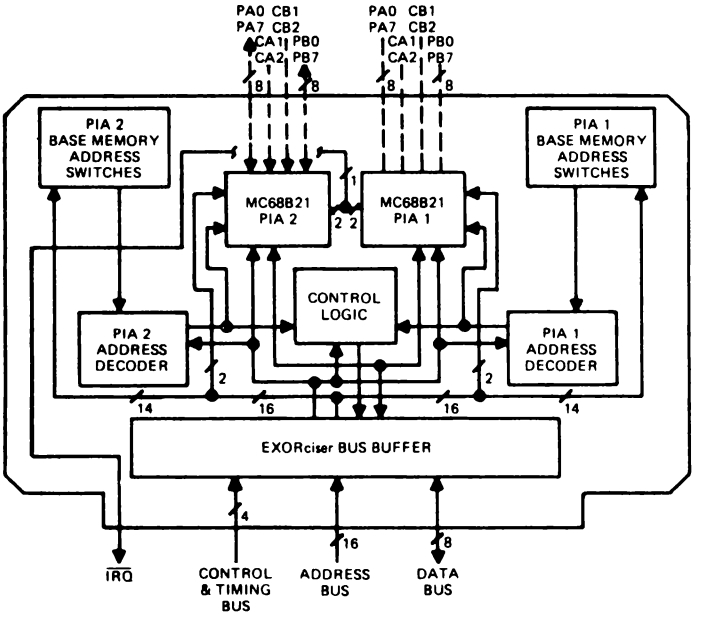
Ordering Information

The following table lists the information necessary for ordering modules, cables, or manuals.

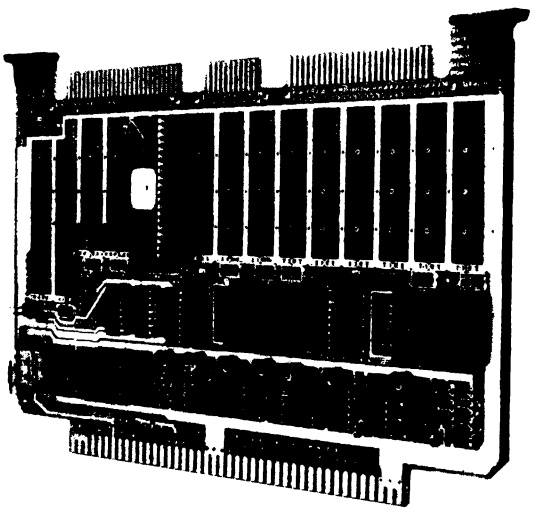
Type Number	Description
MEX6821-2	Input/Output Module
MEX68IC2	Interconnect Cable
MEX68212(D)	User's Guide

MEX6821-2
Input / Output Module





MEX6845 CRT Control Support Module



- Provides the interface to raster scan CRT displays for terminals in stand alone or cluster configuration.
- Fully decoded switch selectable address capability
- Fully buffered address bus and bidirectional data bus
- 20-pin header for implementation of priority interrupts, multi-paged memory, and I/O systems
- Two 50-pin edge connectors and one 20-pin edge connector provides interface for custom circuitry
- Large wire-wrap socket area for custom circuitry
- Jumper selectable memory map assignment

The MEX6845 CRT Controller Support Module provides the user with a minimal hardware design implementing the MC6845 CRTC device. The necessary data lines, and control signals are factory-wired to the device. The device is mounted in a wire-wrap socket which provides access to the MC6845 bus for connection of the user's custom circuitry. The three-edge connectors provide 120 lines for interface with the user's system.

Four hexidecimal address select switches allow the user to generate a fully decoded chip select function.

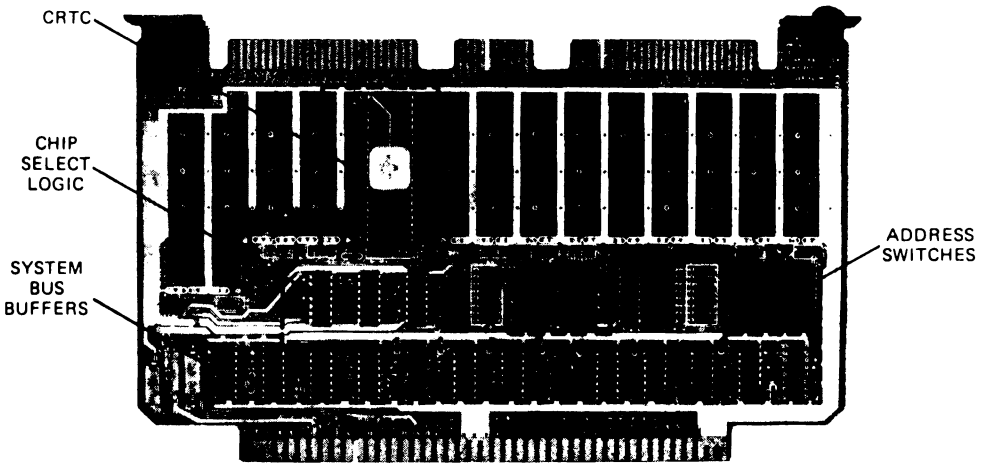
Specifications

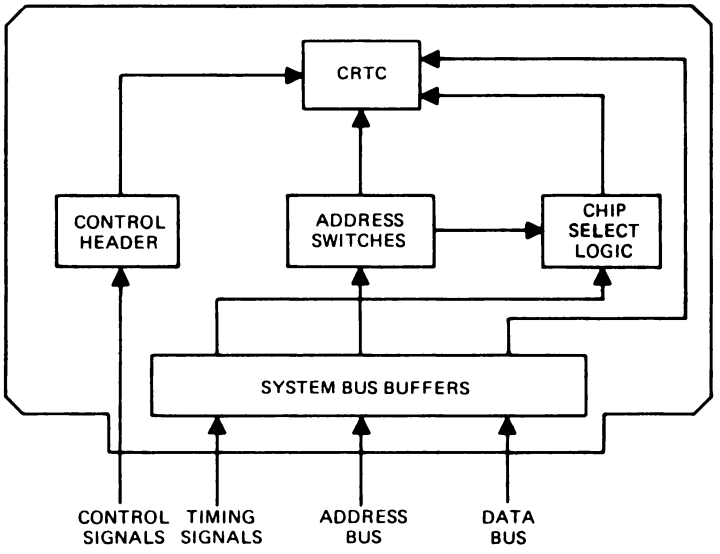
Address and Control Bus	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	+5 Vdc @ 2 A max
	+12 Vdc
	-12 Vdc
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

The following table lists the information necessary for ordering modules, manuals, or data sheets.

Type Number	Description
MEX6845	CRT Controller Support Module
MEX6845(D)	User's Guide
MC6845 Data Sheet	Data Sheet for MC6845 CRTC

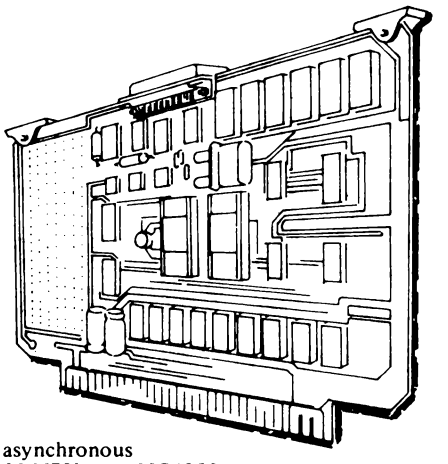
MEX6845
CRT Control Support Module





MOTOROLA MICROSYSTEMS

MEX6850 ACIA Module



- Eight or nine-bit transmission
- Program-selectable odd, even, or no parity
- TTY and RS-232C data terminal interface capability
- Program-selectable divide-by 16 and 64 clock modes
- Program-selectable one or two stop bits
- Eight switch-selectable baud rates between 110 and 9600 baud

The MEX6850 ACIA Module (Asynchronous Communications Interface Adapter) interfaces the EXORciser base system to an asynchronous data communications device. This module appears to the MC6800 MPU as an MC6850 ACIA. In preparing a program for this module, the designer determines parity, the number of stop bits and the ACIA's clock mode. The user can select one or two stop bits; odd, even, or no parity; the clock mode; and the number of data bits to be transferred.

The user, in setting up this module, selects one of the eight standard switch selectable baud rates between 110 and 9600. He has the option of interfacing directly with a TTY (20 mA neutral current loop), and an RS-232C compatible terminal, or of constructing a custom interface circuit for some other peripheral. The module can be configured to appear as a data terminal or modem to an external communications device. It has provisions for standard 14, 16, and 24 pin wirewrap sockets to allow for the construction of customized circuits.

The EXORciser's MPU addresses the ACIA as if it were two locations in memory. By proper setting of the base memory address switches, the user can select the base memory address for the ACIA. The address enable/disable switches activate or de-activate individual address lines. This allows the EXORciser to emulate systems not using all 16 address lines. The address decoder determines when the MPU is addressing its ACIA and enables the control logic to decode its inputs. The control logic, by decoding of the MPU timing and control signals, controls the flow of data through the EXORciser bus buffer. The EXORciser bus buffer interfaces the ACIA Module with the EXORciser bus.

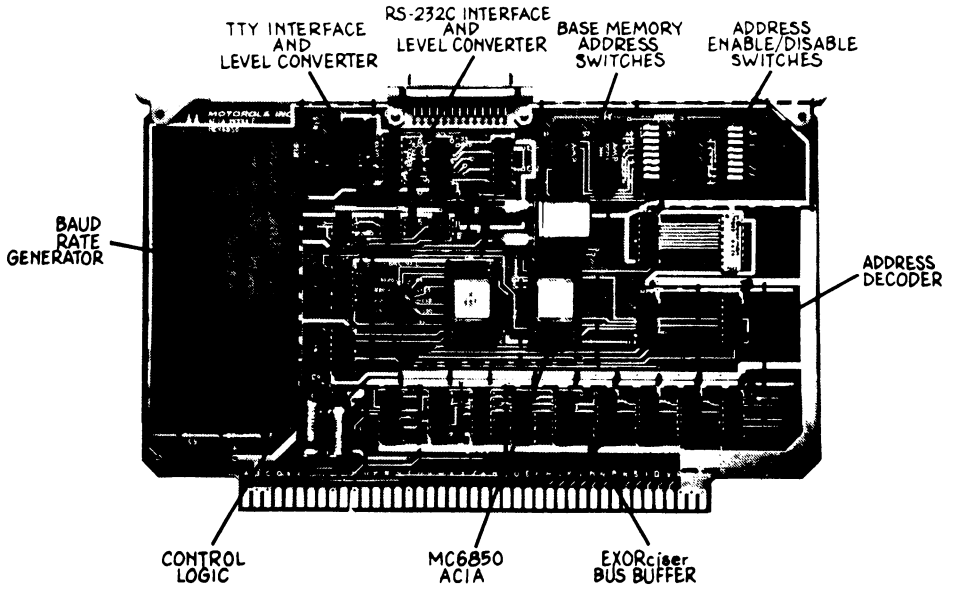
Specifications

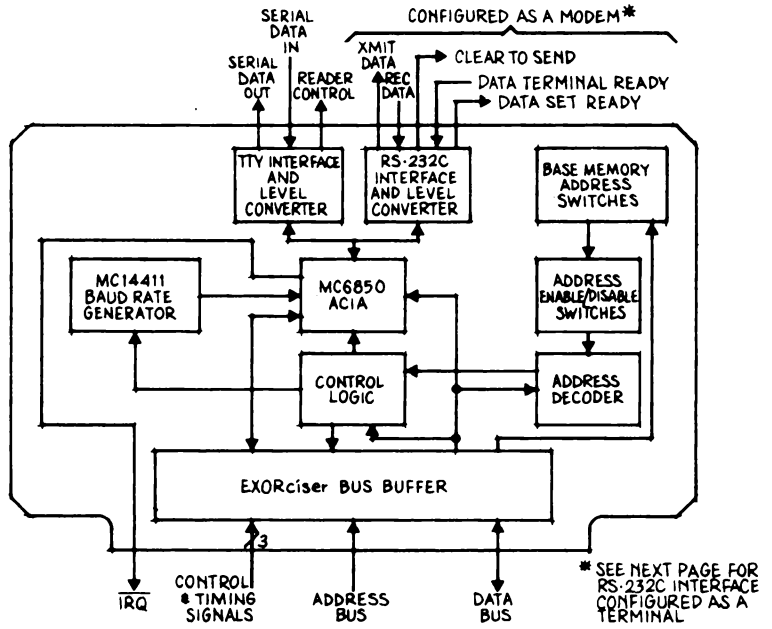
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Address and Control Bus	TTL voltage compatible
Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Switch selectable baud rates	110, 150, 300, 600, 1200, 2400, 4800, and 9600
Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
TTY Reader Control Signal	Control signal for TTY devices modified for external control
RS-232 Interface Signals	RS-232C signals to interface with an RS-232C data terminal. Can be modified to interface with any RS-232C modem.
Power Requirements	+5 Vdc @ 750 μA +12 Vdc @ 500 μA -12 Vdc @ 500 μA
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

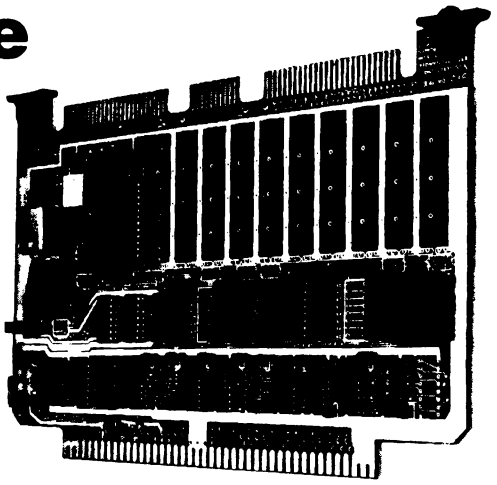
MEX6850
ACIA Module

Option





MEX6850-2 ACIA/SSDA Support Module



- Eight or nine bit transmission
- Program selectable odd, even, or no parity
- Program selectable divide by 16 and 64 clock modes
- Program selectable one or two stop bits
- Eight jumper selectable baud rates from 110 through 9600 baud
- Provisions on module to construct custom circuitry i.e. TTY and RS-232 Interfaces
- Easy conversion to MC68B52 Synchronous Serial Data Adapter (SSDA)

The MEX6850-2 ACIA/SSDA Support Module (Asynchronous Communications Interface Adapter/ Synchronous Serial Data Adapter) interfaces the Development System to a data communication device. The module is factory wired as an MC68B50 ACIA. The user has the option of interfacing this module with a TTY, cassette handlers, disk drives, external terminal, or an RS-232C compatible device. This module may be configured to appear as a data terminal or as a modem to the external communications device. The module may be converted to a Synchronous Serial Data Adapter by replacing the MC68B50 ACIA with an MC68B52 SSDA and making a few wiring changes.

In preparing a program for this module, the designer determines parity, the number of stop bits and the ACIA clock mode. The user can select one or two stop bits; odd, even, or no parity; the clock mode; and the number of data bits to be transferred.

The user, in setting up this module, selects one of eight standard jumper selectable baud rates from 110 through 9600. He has the option of interfacing, through custom circuitry, with a TTY (20 mA neutral current loop), and an RS-232C compatible terminal, or of constructing a custom interface circuit for some other peripheral. The module has provisions for standard 14, 16, and 24-pin wirewrap sockets to allow for the construction of customized circuits.

The system MPU addresses the ACIA or the SSDA as if it were two locations in memory. By proper setting of the base memory address switches, the user can select the base memory address for the ACIA or SSDA. The address decoder determines when the MPU is addressing its ACIA or SSDA and enables the control logic to decode its inputs. The control logic, by decoding of the MPU timing and control signals, controls the flow of data through the system bus buffers.

MEX6850-2
ACIA/SSDA
Support Module

Specifications

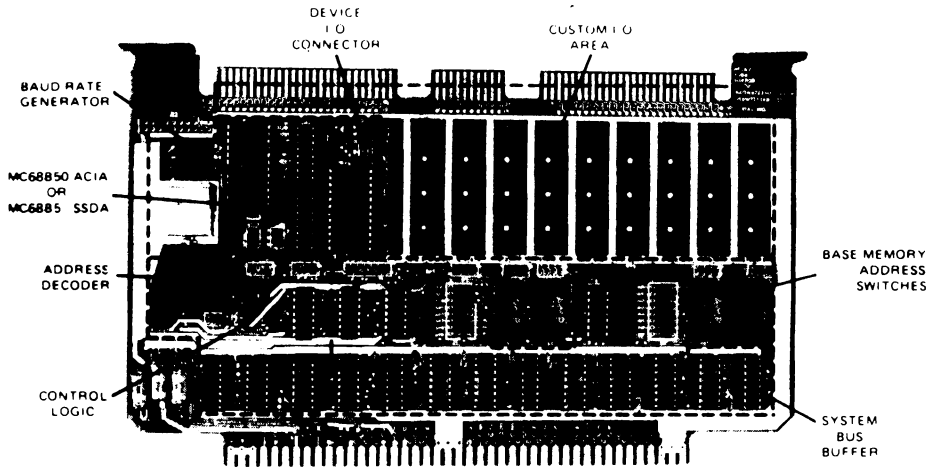
Address and Control Bus	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Swtich selectable baud rates	110, 150, 300, 600, 1200, 2400, 4800, and 9600
Power Requirements	+5 Vdc @ 750 μA +12 Vdc @ 500 μA -12 Vdc @ 500 μA
Physical Dimensions W x H x T	9.75 x 6.00 x 0.062 in.

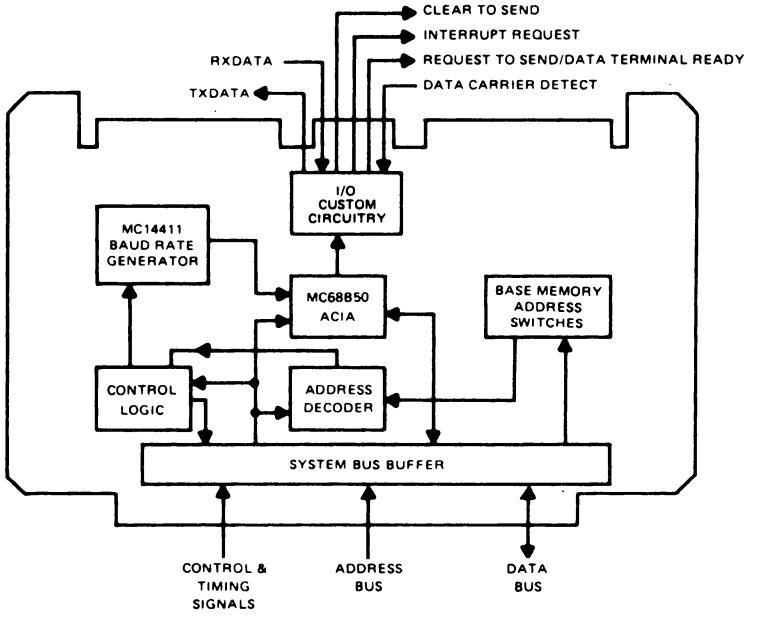
Ordering Information

The following table lists the information necessary for ordering modules, devices or manuals.

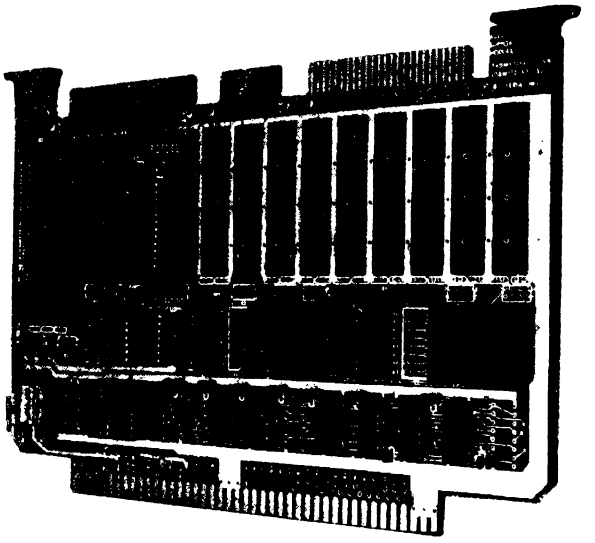
TYPE NUMBER	DESCRIPTION
MEX6850-2	ACIA/SSDA Module
MC68B52	SSDA Device
MEX68502 (D)	User's Guide

MEX6850-2
ACIA/SSDA
Support Module





MEX6854 ADLC Support Module



- Provides data communications interface for both primary and secondary stations in stand alone, polling, and loop configurations
- Fully decoded switch selectable address capability
- Fully buffered address bus and bidirectional data bus
- 20-pin header for implementation of priority interrupts, multi-paged memory, and I/O systems
- Two 50-pin edge connectors and one 20-pin edge connector provides interface for custom circuitry
- Large wire-wrap socket area for custom circuitry
- Jumper selectable memory map assignment

The MEX6854 ADLC (Advanced Data Link Controller) Support Module provides the user with a minimal hardware design implementing the MC6854 ADLC device. The necessary data lines and control signals are factory-wired to the device. The device is mounted in a wire-wrap socket which provides access to the MC6854 bus for connection of the user's custom circuitry. The three-edge connectors provide 120 lines for interface with the user's system.

Four hexidecimal address select switches allow the user to generate a fully decoded chip select function.

Specifications

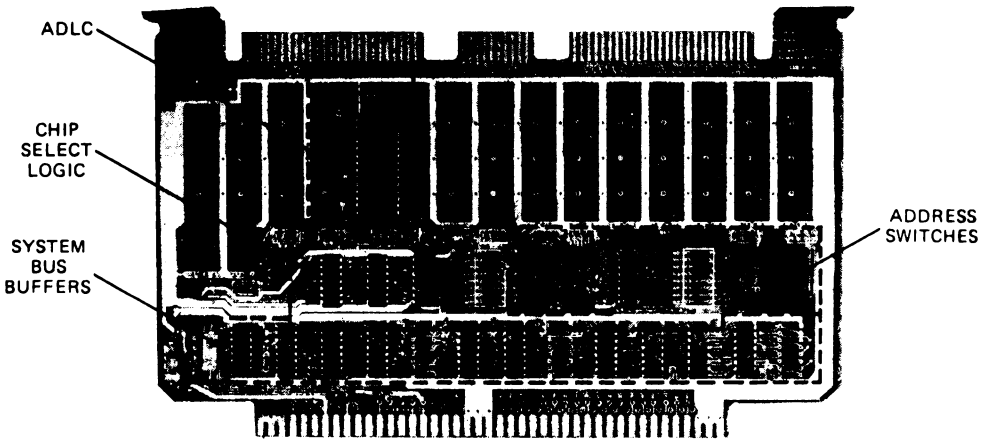
Address and Control Bus	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	+5 Vdc @ 2 A max
	+12 Vdc
	−12 Vdc
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

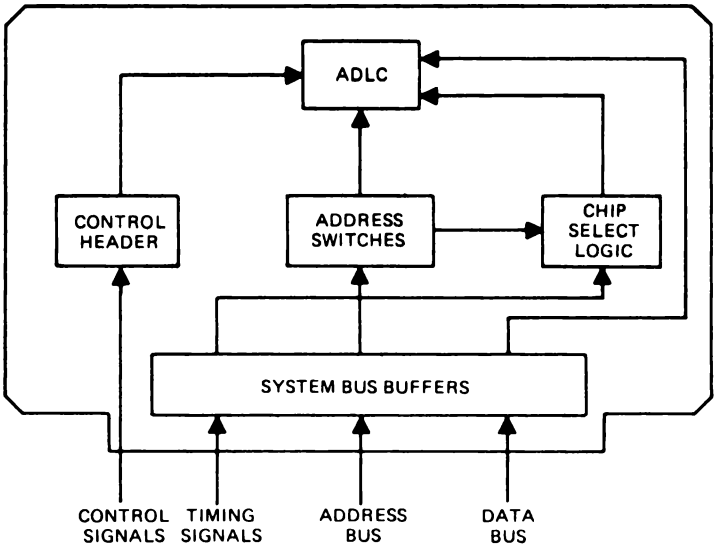
Ordering Information

The following table lists the information necessary for ordering modules, manuals, or data sheets.

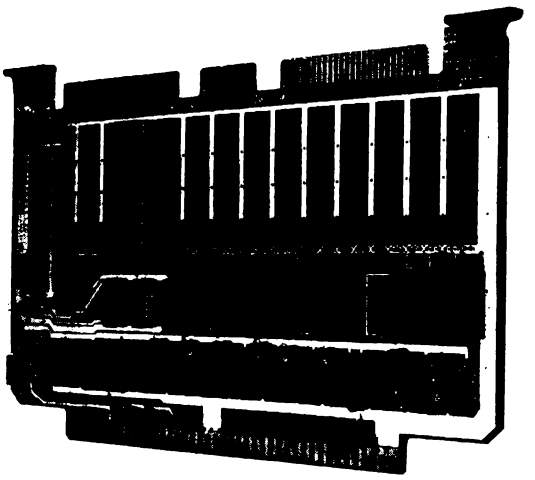
Type Number	Description
	ADLC Support Module
MEX6854 (D)	User's Guide
MC6854 Data Sheet	Data Sheet for MC6854 ADLC

MEX6854 ADLC Support Module





MEX68488 GPIA Support Module



- Provides a means for controlling and moving data from complex systems of multiple instruments
- Fully decoded switch selectable address capability
- Fully buffered address bus and bidirectional data bus
- 20-pin header for implementation of priority interrupts, multi-paged memory and I/O systems
- Two 50-pin edge connectors and one 20-pin edge connector provides interface for custom circuitry
- Large wire-wrap socket area for custom circuitry
- Jumper selectable memory map assignment

The MEX68488 GPIA (General Purpose Interface Adapter) Support Module provides the user with a minimal hardware design implementing the MC68488 GPIA device. The necessary data lines and control signals are factory-wired to the device. The device is mounted in a wire-wrap socket which provides access to the MC68488 bus for connection of the user's custom circuitry. The three edge connectors provide 120 lines for interface with the user's system.

Four hexidecimal address select switches allow the user to generate a fully decoded chip select function.

Specifications

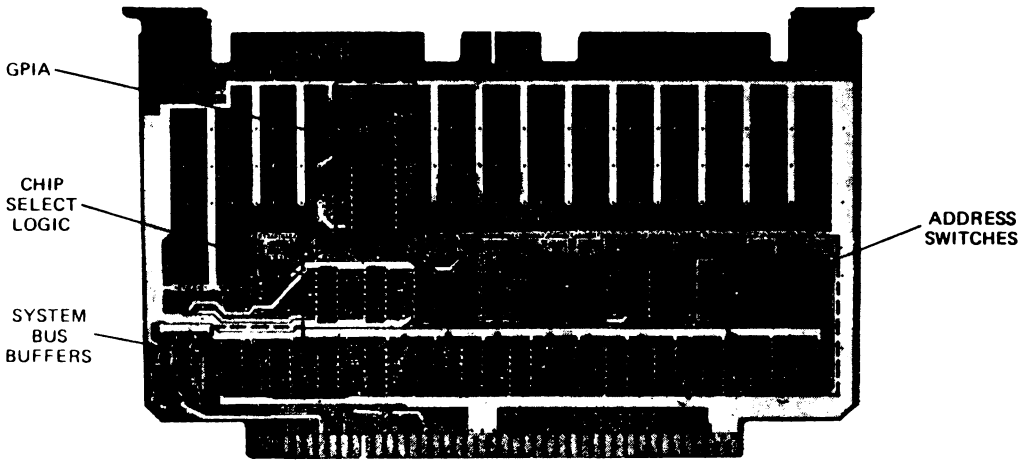
Address and Control Bus	TTL voltage compatible
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	+5 Vdc @ 2 A max
	+12 Vdc
	−12 Vdc
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

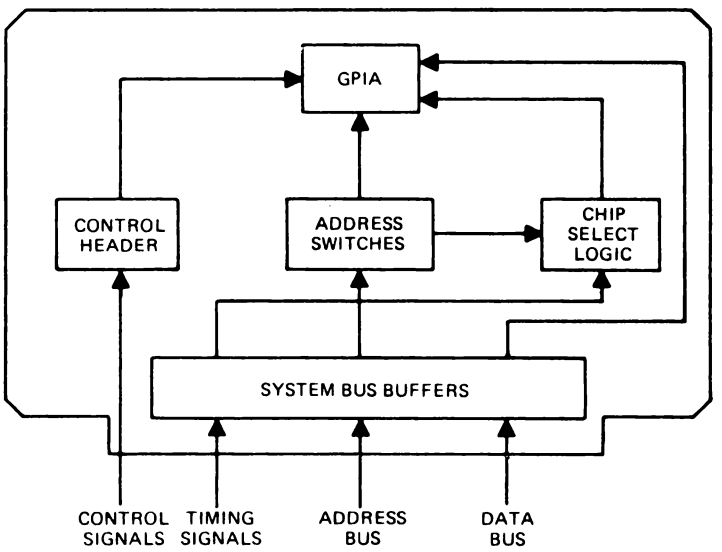
Ordering Information

The following table lists the information necessary for ordering modules, manuals, or data sheets.

Type Number	Description
MEX68488	GPIA Support Module
MEX68488(D)	User's Guide
MC68488 Data Sheet	Data Sheet for MC68488 GPIA

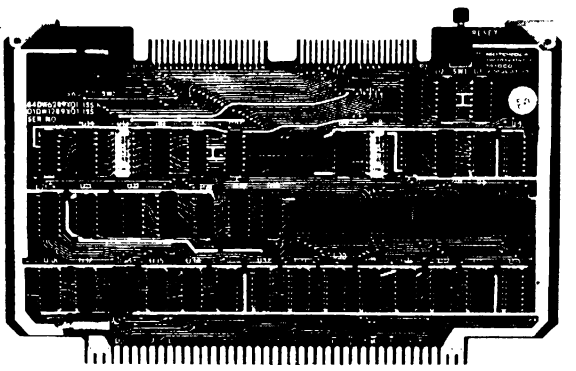
MEX68488 GPIA Support Module





MOTOROLA MICROSYSTEMS

MEX141000M MC141000/1200 Development System



- M6800 EXORciser or EXORterm based
- Complete software capabilities, including Cross Assembler, Loader, and Debug Package
- Provides an economical and expedient means for developing new applications prior to committing to final production masks
- Provides complete simulation of the 141000/1200 hardware characteristics
- MDOS based software

The purpose of the 141000/1200 simulator module is to provide an EXORciser or EXORterm based tool for debugging 141000/1200 applications in the actual hardware and software configuration of the user's final system. A ROM object program is generated by the EXORciser 141000/1200 Cross Assembler and is loaded and run by the simulator. Using the information generated by the simulator and the debug facilities provided by the simulator, the user can find and correct problems in the source program. It is possible for the user to simulate all of the 141000/1200 inputs and to examine all of the 141000/1200 outputs via software control, or control the inputs and outputs via external user hardware.

The 141000/1200 Simulator Package will consist of a hardware module and a software package. The module can be used in either an M6800 EXORciser or EXORterm. It will be possible to load and save the user's program and debug it with the software package. The module will provide such facilities as a power supply, clock, reset button, input and output connections with the necessary TTL/CMOS level conversions, and the hardware necessary to interface with the simulator software.

Figure 1 shows the data flow in the 141000/1200 Simulator System. The ROM object file resides on a disk file and can be accessed through the 141000/1200 simulator software. Inputs to the user program can come either from the terminal or the user's 141000/1200 system.

Figure 2 illustrates the hardware connections of the 141000/1200 Simulator System. The simulator board is inserted in the EXORciser or EXORterm. A cable with a DIL male connector will connect the simulator to the user's system.

Figure 3 shows the USER commands available with the simulator package.

Minimum System Requirements

EXORciser or EXORterm
MDOS
24K Memory
Editor

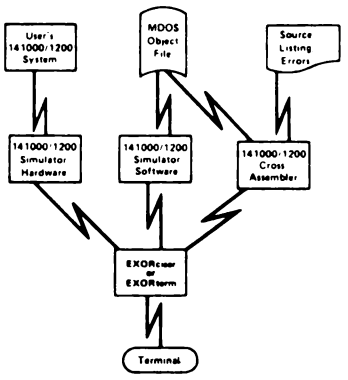


FIGURE 1. 141000/1200 Simulator System Data Flow

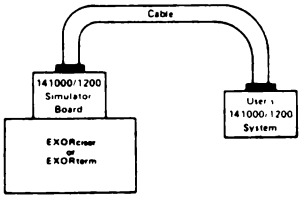


FIGURE 2. 141000/1200 Simulator Hardware Connections

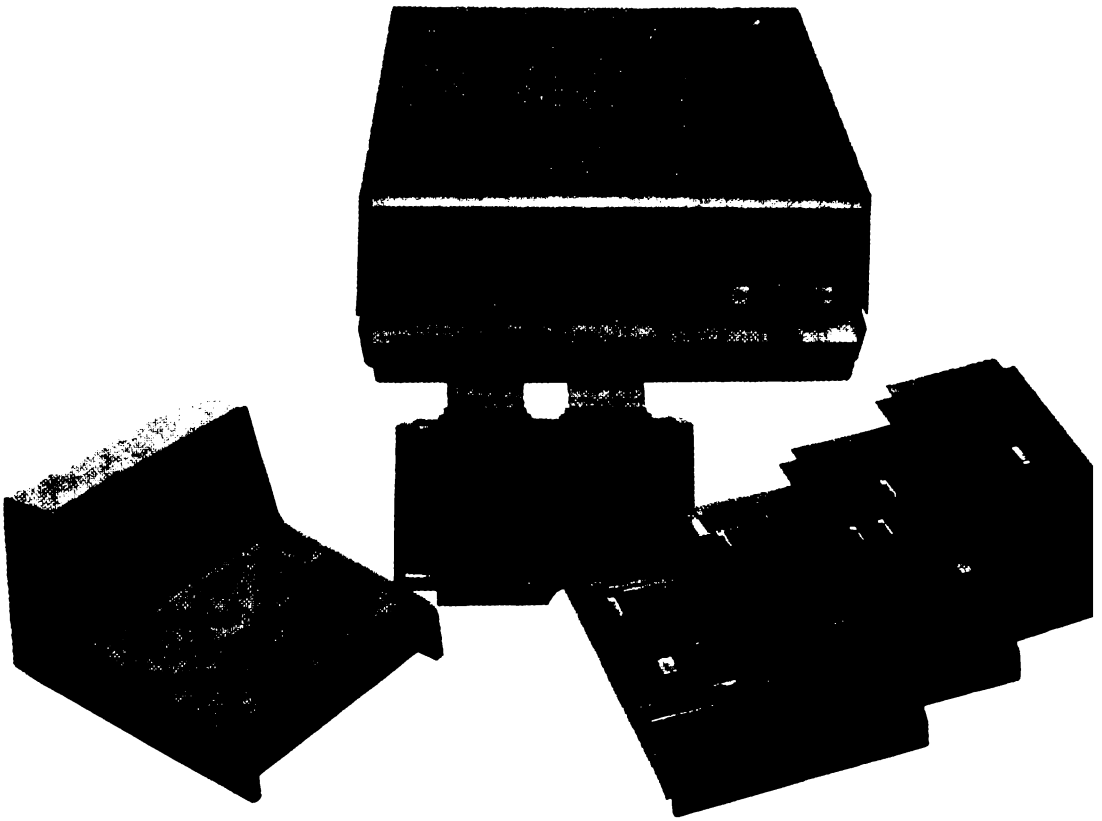
Command	Description
NNN/	Open simulated ROM byte addressed by N
NN.	Open simulated RAM byte addressed by N
NN-	Open simulated OPLA byte addressed by N
(LF)	Open next sequential location
(CR)	Close open location
(UA)	Open previous sequential location
X	Return to MAID (:P to continue)
S	Save a program on a new or existing disk file
L	Load a program from a disk file
M	Return to MDOS
N;V	Set breakpoint at location N
;U	Remove all breakpoints
N;U	Remove breakpoint at location N
;G	Execute user PGM from power up or intialize
N;G	Execute user PGM from location N
N;P	Execute until BKPT found N times
;P	Continue executing from encountered BKPT
;N	Trace one instruction
N	Trace one instruction
N;N	Trace N instructions
$V	Display breakpoints
$R	Display/change target program registers
$K	Print K and allow alteration
;K	Clear software K
$O	Print O-outputs

FIGURE 3. USER Commands

Ordering Information

Part Number	Description
MEX141000M	141000/1200 Simulator, including Cross Assembler (EXORciser or EXORterm) and Simulator Package (Module and Software)
MEX141000(D)	M141000/1200 Simulator User's Guide

MEX68CT MOTEST-I
Component Tester



MOTEST-I (MEX68CT) is a dynamic LSI tester that provides the EXORciser with the capability of testing the M6800 microcomputer family of parts in an environment that closely approximates the end use conditions. Presently, MOTEST-I has the capability of testing the MC6800 Microprocessor Unit (MPU), MC6820 Peripheral Interface Adapter (PIA), MC6850 Asynchronous Communications Interface Adapter (ACIA), MCM6810 128 x 8 Bit Static Random Access Memory (RAM), MCM6604 type Dynamic RAM, 4096K 1 Bit, and MCM6830 1024 x 8 Bit Read Only Memory (ROM). Using the Universal ROM card, additional TTL-compatible ROMs can also be accommodated.

- Functionally tests M6800 microcomputer family of parts in real time
- Can be adapted to test other devices: memories, TTL parts, CMOS parts, and other microprocessors
- One EXORciser will control up to eight test heads
- Uses internal EXORciser power (+5 Vdc) or external power (determined by user)
- Provides statistical log which indicates PART TYPE, TOTAL TESTED, TOTAL FAILED, and % GOOD for each test head
- Provides interlocking between test program and personality card in the test head
- Optional footswitch control
- Optional extender allows personality card to be located in environmental chamber for environmental testing
- PASS/FAIL indications

Ordering Information

When ordering MOTEST-I, the user selects the options he requires.

An appropriate suffix to each basic part number is required to define the medium on which the executive and test programs are to be supplied.

Part Number	Description
MEX68CT A,B,D,M	Component Tester Test Head (1) Control Card (1) Interface Cables (2) Executive Program (1)

Options

Part Number	Description
MEX68CT2, A,B,D,M	MPU (MC6800) Personality Card, Test Program
MEX68CT3 A,B,D,M	PIA (MC6820) Personality Card, Test Program
MEX68CT4 A,B,D,M	ACIA (MC6850) Personality Card, Test Program
MEX68CT5 A,B,D,M	ROM (MCM6830) Personality Card, Test Program
MEX68CT6-1 D,M (16-pin)	ROM Universal Personality Card, Test Program
MEX68CT6-2 A,B,D,M (24-pin)	Universal ROM Personality Card, Test Program
MEX68CT7 A,B,D,M	RAM (MCM6810) Personality Card, Test Program

A Suffix – Cassette, B – Paper Tape, D – EDOS Diskette, M – MDOS Diskette

MEX68CT MOTEST-I General Description

The MOTEST-I system requires an EXORciser containing an MPU Module, Debug Module, Baud Rate Module, and the required memory. The memory size is determined by the number of device types being tested. MOTEST-I, itself, consists of a control card which plugs into the EXORciser, interface cables, test head, Executive program, test programs and a personality card designed for each particular part. One EXORciser will control up to eight test heads without any restriction on the mix of parts being tested. When setting up your test system, it is important to remember that each test head requires a control card and a set of interface cables to connect the test head to the EXORciser. To set up the system, the interface cables are connected to the control card, and the control card is then inserted into the EXORciser. The other ends of the interface cables are connected to the test head. If external voltages are required, they can be connected to the external power jack located on the side of the test head. To test a part, the user simply selects and inserts the particular personality card into the test head, loads the Executive and appropriate test program (using the LOAD function of EXbug) into the EXORciser, and MOTEST-I is ready to evaluate the device. The user now installs the device to be evaluated into the test socket located on the personality card, presses the TEST switch and monitors the indicators to see if the part has passed or failed.

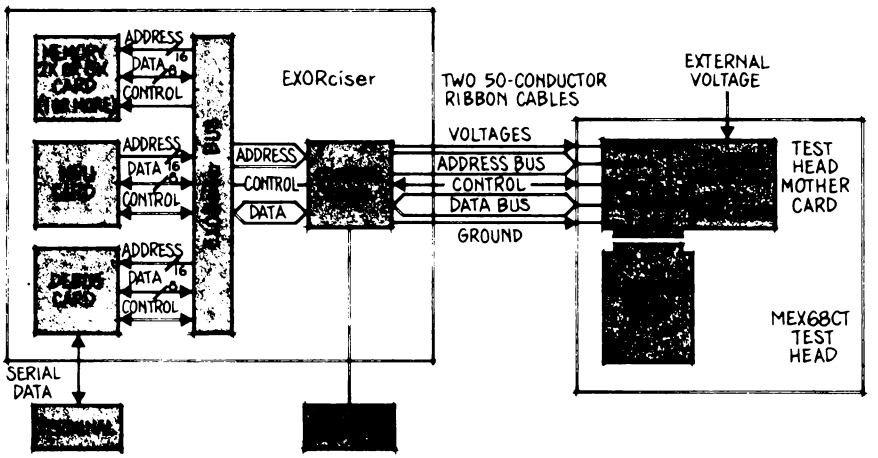
System Software

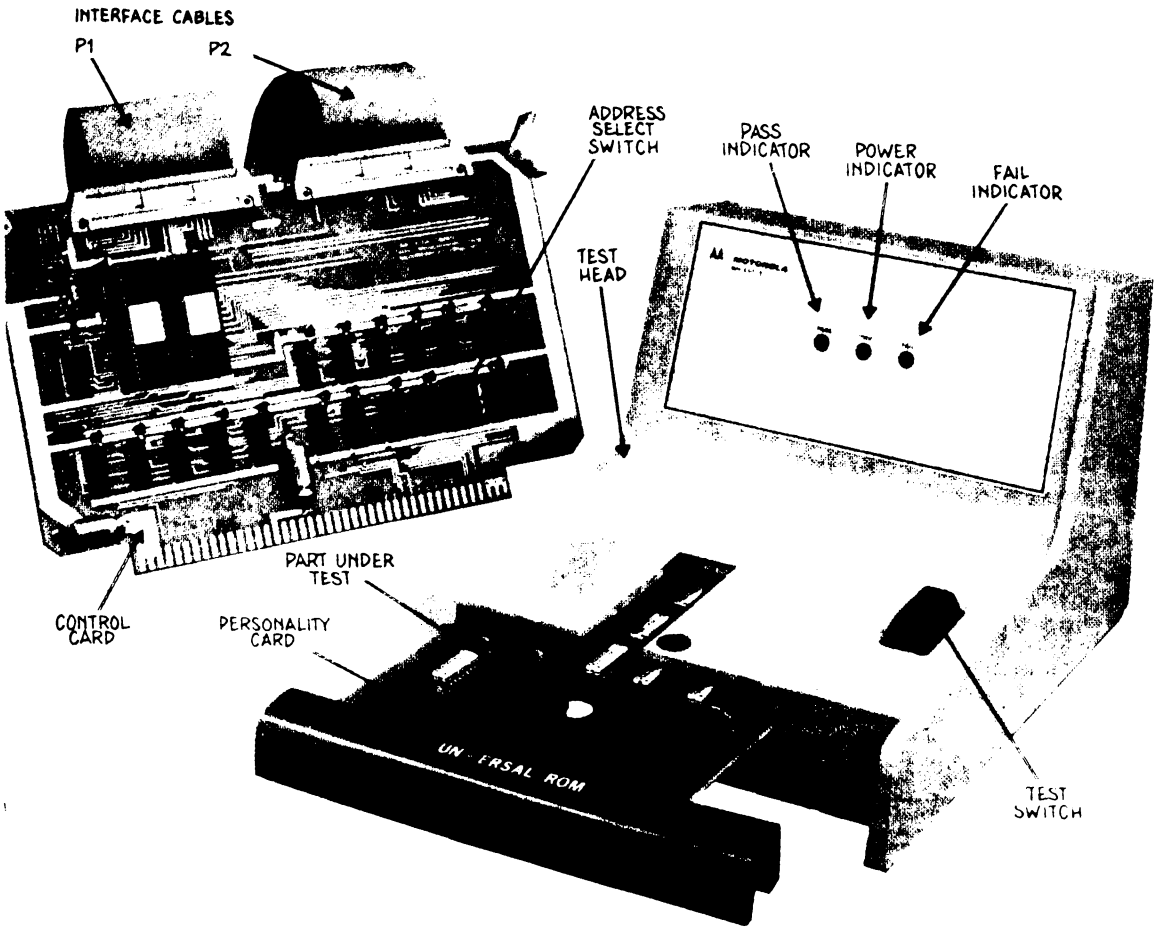
MOTEST-I system software consists of one Executive program and a test program for each personality card.

EXECUTIVE – The Executive performs the function of initializing and polling the control cards for a start test interrupt, verifying the device/test program interlock, controlling power to device under test so that it can be installed and removed with power off, providing a statistical log on request, and providing a command structure to aid setup.

TEST PROGRAM – The test program, upon receiving control from the Executive program, performs the following functions: calculates the test device address, sets up the control PIAs to perform the test, and sequentially tests each parameter of the test device. Control is returned to the Executive program as a result of a PASS or FAIL indication.

MEX68CT MOTEST-I
Component Tester





Component Testing *Control is returned to the Executive Program due to either PASS or FAIL.*

MPU Testing
The following tests are performed on the MPU:

- The test program is loaded into the two resident 128 byte RAMs.
- Control is transferred to the MPU under test, and the "instruction set" (1) is executed. Termination is a WAI causing BA to go true.
- The EXORciser looks for BA from the MPU under test or time out, whichever comes first.
- NMI and IRQ are independently pulled causing the MPU to go to another WAI in the program, depending upon the state of the interrupt mask described in the following step.
- Modification of the program changes the running address from $00XX_{16}$ to $55XX_{16}$. The instruction CLI is substituted for SEI on this pass.
- Assuming successful execution of the first pass, as evidenced by returning control to the EXORciser and reading the memory and comparing the results to known check sums, the program is modified.
- The program is now run again and the results checked.
- The program is again modifed to run at $2AXX_{16}$. The instruction SEI is exchanged for CLI on this pass.
- The program is now run again and the results checked.
- The instructions not previously executed, as described in footnote (1), are now run. These include stack and index register codes, subroutine jumps and returns flagged by the index register.
- Upon successful completion of the program that has just run, TSC is enabled by the EXORciser causing the MPU under test to execute the code in location $FFFF_{16}$.
- NMI is then enabled, vectoring the MPU to another WAI instruction.
- Memory is again checked for successful execution of the second program.

PIA Testing
The following tests are performed on the PIA:

- Test Reset Line clears all PIA registers.
- Test ability to read/write Data Direction Registers.
- Test A-Data Register as an output while driving B-Data Register as an input.
- Test A-side Chip Selects and B-side Write Enable.
- Test B-Data Register as an output while driving A-Data Register as an input.
- Test B-side Chip Selects and A-side Write Enable.
- Test three-state capability of CA2 and CB2.
- Test CA1 and CB1 as interrupt input lines.
- Test CA2 as an output line while CB2 is an input line.
- Test CB2 as an output line while CA2 is an input line.

ACIA Testing
The following tests are performed on the ACIA:

- Test Master Reset.
- Test ACIA for ability to transmit and receive data at 110 baud.
- Test ACIA for ability to transmit and receive data at 5200 baud.
- Test ACIA at different word lengths and parity selections using 500 kHz clock rate.
- Test for Transmit Interrupt and double buffering capability.
- Test Break.
- Test Ready to Send, RTS.
- Test Clear to Send, CTS.
- Test Data Carrier Detect, DCD.
- Test Receive Interrupt.
- Test Overrun Error.
- Test Framing Error.
- Test Chip Selects.
- Test False Start Bit Detection.
- Test Parity Error Detection.

Static RAM Testing
1028 x 8 Bits. The following tests are performed:

- Walking Address test.
- Bit pattern AA R/W test.
- Bit pattern 55 R/W test.
- Galloping Read test.
- Galloping Write test.
- Walking Bit Pattern tests.

10000000	00100000	00001000	00000010
01000000	00010000	00000100	00000001

- Test Chip Selects.

ROM Testing
The following tests are performed on the ROM:

- The message flag is tested. If the flag is a one, the ROM is read, and its contents are saved to be used as a reference pattern. The flag is then set to a zero. If the flag is a zero, the ROM is tested.

The following tests are then performed:

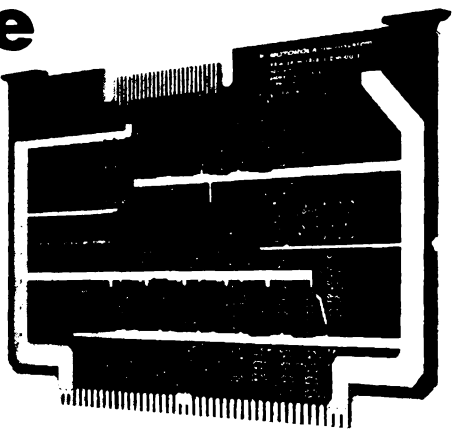
- The Chip Selects are enabled. The ROM is read, and its contents are compared to the reference pattern.
- One Chip Select at a time is disabled. The ROM is read to test the function of the respective Chip Select.

(1) The instruction set is incremented from 01 "NOP" to FF "STX". All undefined codes, index modification codes, JSR, RTI, stack or stack modification codes are omitted in the valid OP code file and tested separately.

MOTOROLA

MICROSYSTEMS

MEX68PI2 Printer Interface Module



- Provides interface between Development System and Centronics Printer
- Jumper selectable memory map assignment
- Provisions for customer supplied circuits are included
- A 20 pin header for implementation of priority interrupts, multi-paged memory, and special I/O system

The MEX68PI2 Printer Interface Module provides the interface required between the Development System and a printer. The configuration of the module, as wired at the factory, is for the standard Centronics interface. The address is preset to EC10 for use by the MDOS and EXbug software.

Provisions are included on the module for user supplied custom circuitry to facilitate interface with other printer specifications.

Specifications

Input Signals	**TTL voltage compatible**
Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
MC68B21 Peripheral Interface Adapter Signals*	
PA0-PA7 Input/Output Lines	TTL voltage compatible
PB0-PB7 Input/Output Lines	Three-state TTL voltage compatible
CA1, CA2, and CB1 Control Signals	TTL voltage compatible
CB2 Control Signal	Three-state TTL voltage compatible
IRQA and IRQB Signals	TTL voltage compatible
Operating Temperature	**0 to 70°C**
Power Requirements	**5 Vdc at 2 A max**
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

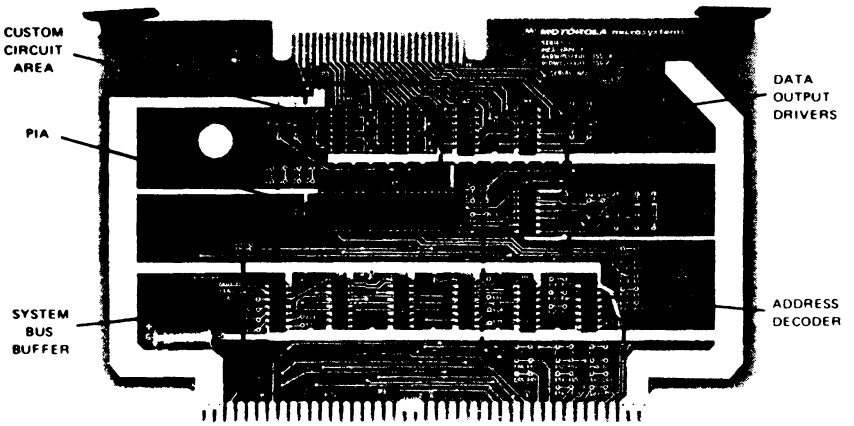
*See MC68B21 data sheet for specifications on these signals.

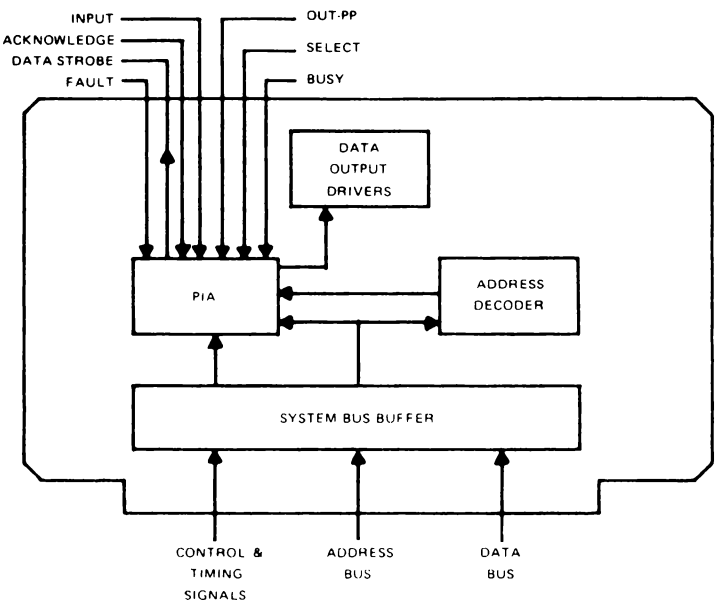
Ordering Information

The following table lists the information necessary for ordering modules, cables, or manuals.

TYPE NUMBER	DESCRIPTION
MEX68PI2	Printer Interface Module
MEX68PIC	Interconnect Cable
MEX68PI2(D)	User's Guide

MEX68PI2 PRINTER INTERFACE MODULE





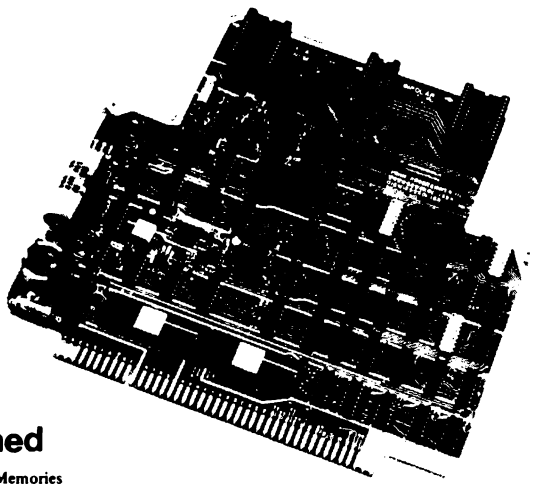
MOTOROLA

MICROSYSTEMS

MEX68PP3 EROM/PROM Programmer Module

The MEX68PP3 EROM/PROM Programmer Module provides the EXORciser or EXORterm with the capability of programming several types of EROM and PROM devices. This module plugs directly into the EXORciser or EXORterm and is compatible with the EXbug firmware and Disk Operating Systems, as well as MINIBUG II/III and Microbug.

The EROM/PROM Programmer Module, with its software, enables the user to program a device, verify the data in the device, and transfer data from the device to the EXORciser's or EXORterm's RAM memory. Software is available on cassette, paper tape, or diskette (EDOS and MDOS).



Devices that can be Programmed

Motorola

MCM68708	1K x 8 EROM
MCM2716	2K x 8 EROM
MCM7640/1	512 x 8 Bipolar
MCM2708	1K x 8 EROM
MCM7680/1	1K x 8 Bipolar

Intel

INT2708/58	1K x 8 EROM
INT2704	512 x 8 EROM
INT2716	2K x 8 EROM

Texas Instruments

TMS2708	1K x 8 EROM
TMS2716	2K x 8 EROM

Harris

HM-7601/1	256 x 4 Bipolar
HM-7620/1	512 x 4 Bipolar
HM-7640/1	512 x 8 Bipolar
HM-7644	1K x 4 Bipolar
HM-7680/1	1K x 8 Bipolar

Monolithic Memories

MMI5300/1	256 x 4 Bipolar
MMI5305/6	512 x 4 Bipolar
MMI5335/6	256 x 8 Bipolar
MMI5340/1	512 x 8 Bipolar
MMI5380/1	1K x 8 Bipolar
MMI5384/5	1K x 8 Bipolar
MMI6300/1	256 x 4 Bipolar
MMI6305/6	512 x 4 Bipolar
MMI6335/6	256 x 8 Bipolar
MMI6340/1	512 x 8 Bipolar
MMI6380/1	1K x 8 Bipolar
MMI6384/5	1K x 8 Bipolar

Signetics

82S126	256 x 4 Bipolar
82S129	256 x 4 Bipolar
82S130/1	512 x 4 Bipolar
82S140/1	512 x 8 Bipolar
82S180/1	1K x 8 Bipolar
82S2708	1K x 8 Bipolar
SIG2708	1K x 8 EROM
82S190/1	2K x 8 Bipolar

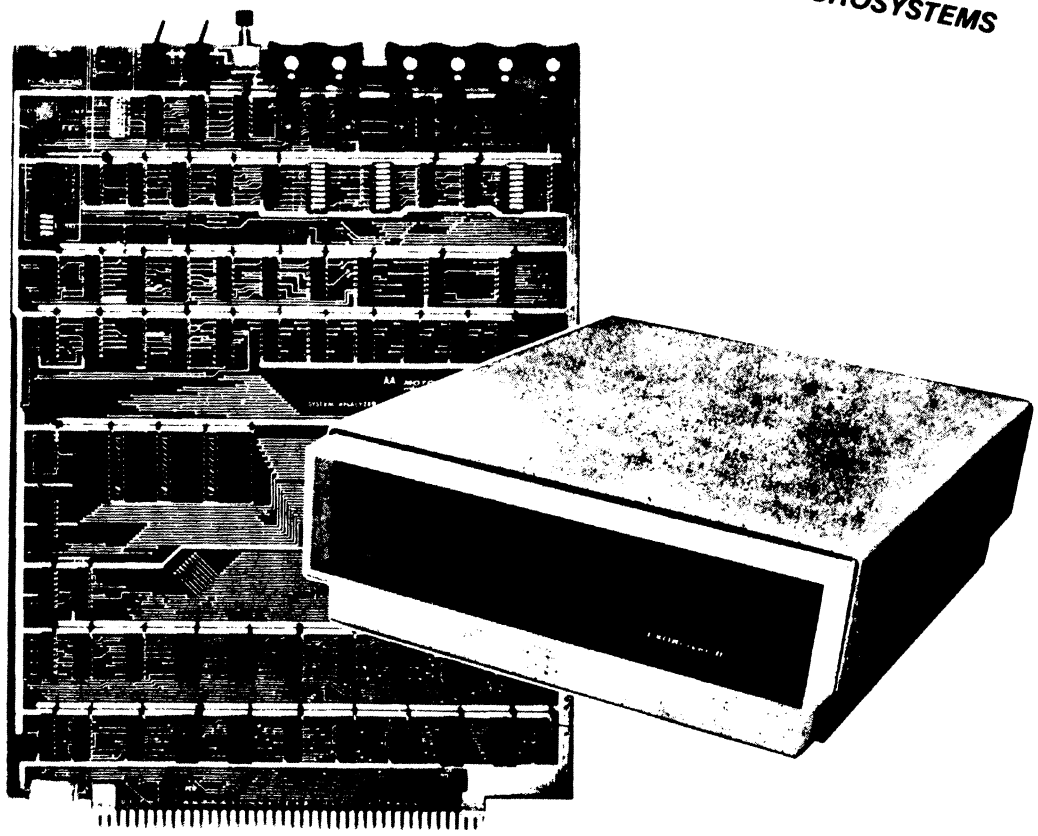
Ordering Information

The EROM/PROM Programmer Module is shipped with the resident software on the medium selected by the user. The following table lists the available options and the part number to be used when ordering.

Option	Part Number	Description
A	MEX68PP3A	Programmer Module with its software on cassette
B	MEX68PP3B	Programmer Module with its software on paper tape
D	MEX68PP3D	Programmer Module with its software on diskette (EDOS)
M	MEX68PP3M	Programmer Module with its software on diskette (MDOS)
	MEX68PP3(D)	PROM Programmer III User's Guide

MOTOROLA

MICROSYSTEMS



MEX68SA2 Systems Analyzer II For System Development and Troubleshooting

MEX68SA2
Systems Analyzer II

- Flexible means of analyzing and troubleshooting MPU systems
- May be used in the Development System or a stand alone troubleshooting tool
- Incorporates its own control switches and indicators
- Allows user to see what is going on inside his system
- Reduces troubleshooting time
- Allows user to analyze and troubleshoot his system in real time
- Monitors and records the MPU bus address, data, and control lines, during each MPU $\phi 2$ clock pulse
- Monitors up to four user selected optional inputs

The MEX68SA2 Systems Analyzer provides an efficient and economical means of monitoring, analyzing, and troubleshooting M6800 Microprocessor Systems. This module connects directly into the MPU's bus and permits the user access to the operations being performed inside of his MPU. The Systems Analyzer is capable of performing the following functions.

- Stop the MC6800, MC68A00, or MC68B00 MPU on detecting the selected compare conditions
- Step through the MPU's program
- Examine and, if required, change the contents in the MPU system's memory
- Trace through the MPU's program
- Monitor and record (takes a snapshot of) the MPU's operation during a selected portion of the MPU's program
- Print a hard copy of the data stored in the Systems Analyzer memory during the snapshot operation

The Systems Analyzer consists of six major blocks and has six modes of operation. The six major blocks are the Switch and Indicator Section, the Compare Section, the Memory Section, the Bus Buffer Section, the Hard Copy Interface Section, and the Control Section. The Control Section decodes the setting of the MODE SELECT switch and determines the module's mode of operation: MPU Run Mode, Step Mode, Standby Mode, Read Write Mode, Trace Mode, and Window Mode. The module performs its snapshot operation in the Trace and Window Modes.

Jumper selectable memory map assignment is provided to allow the user to select the address mode of the module. The jumper selections are: – Valid Memory Address (VMA), Valid User Address (VUA), Valid Executive Address (VXA) (Exbug), and Page Enable for multi-paged memory systems.

Specifications

Signal Characteristics	
Input Logic "0"	0.0-0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Memory Size	128 x 32 bits of random access memory consisting of four MCM68B10 RAM devices
Operating Temperature	0 to 70°C
Power Requirements	+5 Vdc @ 2.75 A
Physical Dimensions	
W x H x T	9.75 x 14.0 x 0.062 in.

Ordering Information

The following table lists the information necessary for ordering modules or manuals.

Type Number	Description
MEX68SA2	Systems Analyzer Module
MEX68SA2(D)	User's Guide

Systems Analyzer Circuitry

Switch and Indicator Section

This section provides the user with a means of entering the selected compare conditions and of monitoring the status of the MPU bus. The switch portion of this circuitry consists of four hexadecimal address switches, two hexadecimal data switches, and a connector to permit the user to insert up to four optional input signals that he wishes to monitor. The indicator portion of this circuit consists of four hexadecimal address displays, two hexadecimal data displays, and nine LED displays. The LEDs display the status of the MPU (running or halted), the status of the four MPU control signals (R/W, VMA, $\overline{IRQ}$, and $\overline{NMI}$), and the status of the four user-selected optional input signals to the module.

Compare Section

This section, when enabled, compares the MPU bus signals with the output of the hexadecimal switches in the switch and indicator section to detect the selected compare conditions. A switch in each of the compare lines can be enabled or disabled to meet the selected compare conditions. On detecting these conditions, this circuit applies a compare strobe to the other sections in the module.

Memory Section

This section consists of four MCM68B10 128 x 8-bit RAM memory devices arranged into a 128 x 32-bit memory array. This memory, when enabled stores the bus status – 16 address lines, 8 data lines, VMA, R/W, $\overline{IRQ}$, $\overline{NMI}$, and the four user selected optional inputs during each MPU $\phi 2$ clock pulse. The memory is enabled to record data during the snapshot operation in the Trace and Window Modes.

Bus Buffer Section

This section interfaces the Systems Analyzer Module into the Development System or the user's system. The data bus buffer devices may be changed to interface the module with a low-true or high-true system.

Display Interface Section

This section, working with the Development System's EXbug Firmware, permits the user to print a hard copy of the data stored in the module's memory. If the Systems Analyzer is not working with the Development System, and the user wishes to use the module's hard copy capability, he is required to develop the appropriate I/O routines in his system's program.

Control Section

This section decodes the setting of the MODE SELECT switch and determines which of the module's six modes of operation is to be used.

In the **MPU Run Mode** the Systems Analyzer is disabled and effectively removed from the user's system.

In the **Step Mode** the Systems Analyzer monitors the MPU bus and, on detecting the selected compare conditions, halts the MPU. The user now can step through the user's program.

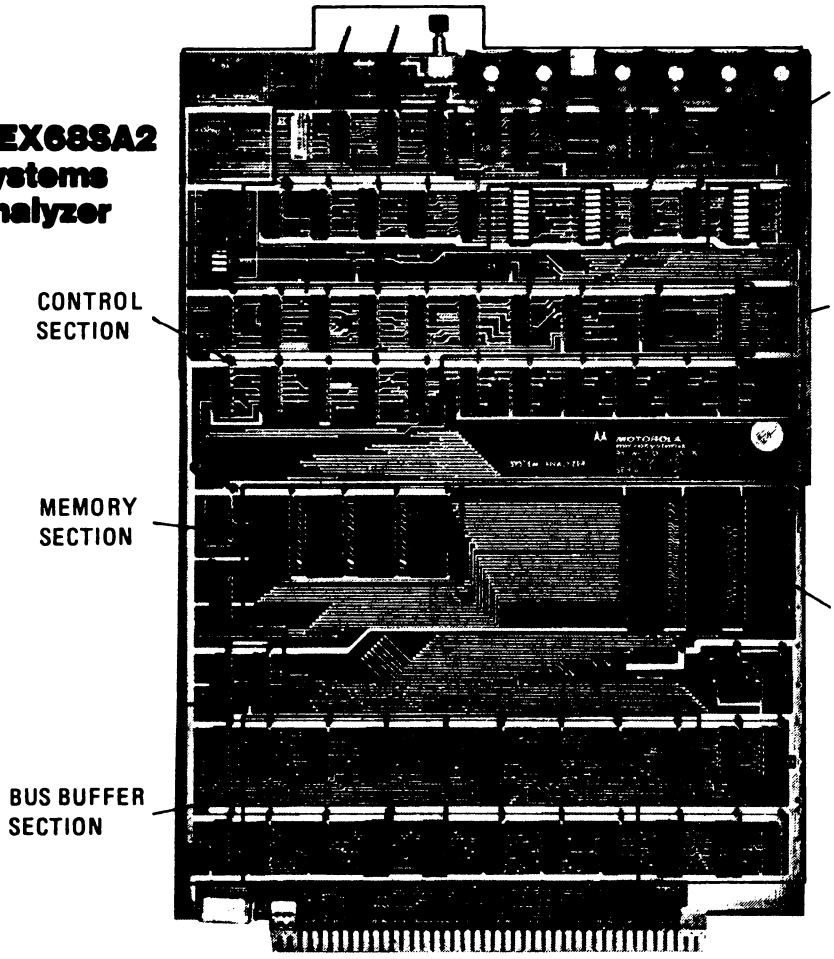
In the **Standby Mode** the Systems Analyzer holds the MPU in the state it was placed in while the module was in the Read/Write or Step Mode.

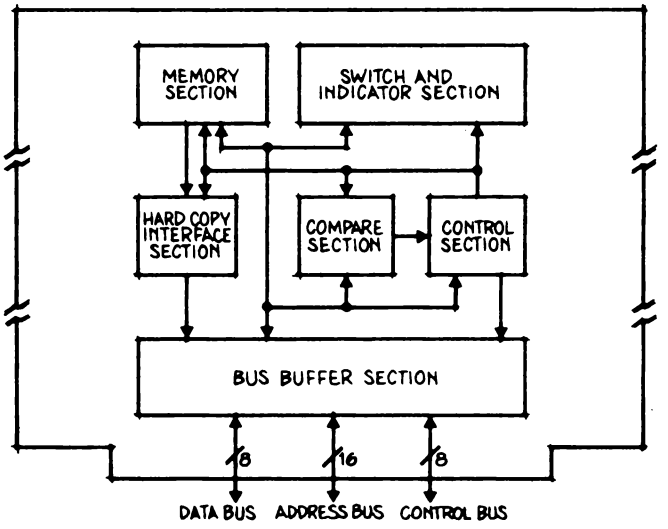
In the **Read/Write Mode** the Systems Analyzer halts the MPU on detecting the selected compare conditions. This now permits the user to examine and, if required, change the contents in the MPU's memory. The hexadecimal switches in the Switch and Indicator Section select the memory location to be examined and the hexadecimal data switches select the data to be written into memory.

In the **Trace Mode** the Systems Analyzer stores the MPU bus status in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions, the Systems Analyzer stores an additional 64 bus states and then halts the MPU. The user now can examine the 128 bus states – the 63 bus states before the selected compare conditions, the selected compare condition bus state, and 63 bus states after the selected compare conditions recorded in the module's memory.

In the **Window Mode**, as in the Trace Mode, the Systems Analyzer stores the MPU bus states in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions the module stores an additional 64 bus states and then stops storing data. In this mode, however, the MPU is not halted but continues running and the user has a snapshot or window view of the operations being performed in the selected portion of his program. The user can now examine the 128 bus states within the selected window area and, if desired, print a hard copy of these bus states.

MEX68SA2 Systems Analyzer





Systems Analyzer Interface Signals

The MEX68SA2 Systems Analyzer Module plugs directly into the Development System bus or may be connected to the MPU's bus in the user's system.

Data Bus ($\overline{D0}$-$\overline{D7}$) or Data Bus (D0-D7) – These eight bidirectional lines, when enabled, provide a two-way transfer of data between the MPU Module in the Development System or the MPU in the user's system and the selected memory location. When the MPU has been halted, the Systems Analyzer controls the flow of data on this bus. These bus signals in the Development System are low true. The user can, through installing the appropriate bus device, change these signals for high true operation.

Address Bus (A0-A15) These 16 lines, when enabled, transfer the selected address to the system's memory and input/output devices. When the Systems Analyzer is halted, it controls this line.

Read/Write (R/W) This MPU output signal indicates whether the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this line is read. Also, when the MPU is halted, this signal will be in the read state. The Systems Analyzer, in halting the MPU, gains control of this signal and can initiate a memory read or write operation.

Valid Memory Address (VMA) This line, when present, indicates to the memory and peripheral devices that the address on the bus is valid. The MPU's VMA output signal must be modified to allow the Systems Analyzer Module to pull this line high and address the memory and peripheral devices when the MPU is halted.

Valid User Address (VUA) – This signal is produced by the DEbug II Module. When high, this signal indicates that the address on the bus is valid, and the MPU is NOT addressing the EXbug program.

Valid Executive Address (VXA) – A high level signal generated by the DEbug II Module in place of the VUA signal when the Development System is operating in the Dual Map mode and the EXbug program is addressing the Executive portion of the memory map.

Page Enable (PEN) – This signal is generated by a user-built controller that converts the VMA signal from the MPU into one of several "pages" of 64 K bytes each. This addressing capability could be used in multiple terminal or disk, and extended memory systems.

Phase 2 ($\phi 2$) Clock Signal – This signal is between 100 kHz and 1 MHz, and is used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU clock.

Bus Available (BA) – This MPU output signal is normally in a low state. When activated, it will go high indicating that the MPU is available. This will occur if the $\overline{\text{Halt}}$ line is low or the MPU is in the WAIT state as the result of executing a WAIT instruction. At such time, all the MPU three-state output drivers will go to their off or high impedance state and all other outputs to their normally inactive state. An interrupt command removes the MPU from the WAIT state. The Systems Analyzer uses this signal to indicate the status of the MPU – halted or running.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the system. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the

Non-Maskable Interrupt ($\overline{\text{NMI}}$) This level sensitive input, on going low, requests that an interrupt sequence be generated within the system. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At this time, the MPU will begin its non-maskable interrupt routine. The Systems Analyzer also monitors this signal.

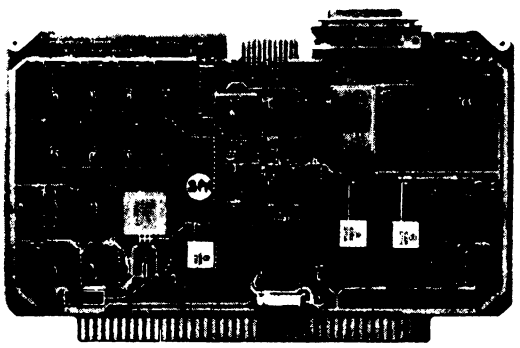
$\overline{\text{Reset}}$ This edge sensitive signal initiates an MPU power-on vectored interrupt initialize routine when the user resets his systems. This signal, in addition to resetting the system's MPU, is used to reset and initialize the Systems Analyzer's Peripheral Interface Adapter devices.

$\overline{\text{Halt}}$ When this level sensitive signal is low, all activity in the MPU will be halted. In the halt mode, the microprocessor will stop at the end of an instruction, the Bus Available signal will be at a high level, and all of the three-state lines will be in their high impedance state. The MPU's VMA signal must be modified to allow the Systems Analyzer Module access to the MPU system's memory and peripherals when it has halted the MPU.

MOTOROLA

MICROSYSTEMS

MEX68SPM System Performance Monitor



- Single board measurement tool - EXORciser/ EXORterm compatible
- No requirement for dedicated control terminal
- Simple operation
- Completely transparent to measured system
- Measurement data collected in real time
- Over 6000 samples per second
- Storage for experiments up to one week without loss of data
- SPM performs both data collection and data reduction

Serious efforts to improve computer programming, system throughput, and the quality of computer software must begin with software measurement. Motorola's System Performance Monitor (SPM) is a tool which measures the relative frequency of reference to memory locations in an M6800 microcomputer system. From the data, the user can determine processor utilization and identify program areas for reorganization or optimization. Data collected by the SPM also provides a quantitative basis for decisions regarding hardware/software tradeoffs and system capacity.

The SPM performs its function by periodically sampling the address lines of the measured system. This information is collected to produce a map of system address frequency characteristics. At the completion of an experiment, the SPM formats and prints a report on a control terminal. This terminal is also used to initialize system parameters.

Operating Modes

The SPM may be used to monitor any portion of the 64K M6800 address space, collecting data on RAM, ROM, or I/O utilization. Three monitoring modes are provided:

- **The entire 64K address space 256 byte resolution**
- **A 16K address block beginning at any mod 1000_{16} address 64 byte resolution**
- **A 4K address block beginning at any mod 1000_{16} address 16 byte resolution**

For 4K or 16K experiments, address references outside the specified region are accumulated and reported as a single statistic. Idle bus cycles are reported as an indication of processor utilization.

Control/Monitor Switch

A two-position switch on the top of the SPM board determines the two major operating modes. Whenever this switch is moved to the MONITOR position, the SPM prints an "M" on the control console and begins sampling the address bus and accumulating the address frequency data. When the switch is moved to the CONTROL position, the SPM suspends its monitoring operation. While in the CONTROL mode, the SPM will accept commands from the control console.

Command Summary

The following commands from the control console are recognized by the SPM:

I - Initialize all monitor parameters and clear all counters. The SPM responds to the I command with "A,S", which prompts the user to enter the beginning address and size of the memory area to be monitored.

H - Print results in histogram format, followed by a results summary.

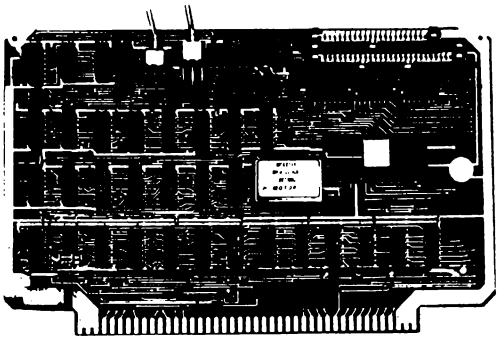
S - Print results summary only.

BREAK - Stop print operation and wait for next command.

Ordering Information

Part Number	Description
MEX68SPM	System Performance Module
MEX68SPM(D)	System Performance Module User's Guide

MEX68USEB User System Evaluator B



The MEX68USEB User System Evaluator (USE), working with the M6800 EXORciser/EXORterm and the optional MEX68SA Systems Analyzer Module, provides the user with the complete systems development tool. That is, USE extends all of the Development System EXbug functions and all of the optional Systems Analyzer functions into the user's system. The USE-equipped Development System provides the designer with the capability of configuring an emulation of his M6800 or M6802 microprocessor system in the EXORciser/EXORterm, external to the EXORciser/EXORterm, or a combination of EXORciser/EXORterm-mounted modules working with the user's external system. The designer also can develop his system software and firmware on the Development System and can use the USE-equipped Development System to debug his system hardware and software. In fact, a USE-equipped EXORciser/EXORterm can even be used to test and evaluate the user's production systems.

USE consists of three assemblies: the USE Processor Module, the USE Intercept Module, and the USE Cable and Buffer Assembly. The USE Processor Module is used in place of the MEX6800 MPU Module in the EXORciser/EXORterm and provides the following functions:

- Provides the EXORciser/EXORterm internal clock circuitry, when USE is not in use.
- Provides switch selectable option of using the EXORciser/EXORterm clock or USER's system clock for overall system (User's system and EXORciser/EXORterm).
- Provides switch selectable option of either User's system or EXORciser/EXORterm generation of $\overline{\text{NMI}}$ signal.
- Disable switches for RESET, NMI, IRQ, $\overline{\text{HALT}}$.
- Interfaces selected MC6800 MPU signals ($\overline{\text{IRQ}}$, $\overline{\text{NMI}}$, HALT, VMA, and BA) with the optional Systems Analyzer Module via the USE Intercept Module.

NOTE: If the Development System is using dynamic memory in an M6800 system and the user's system clock option is to be used, the user's system clock must have the capability to refresh dynamic memory in the EXORciser/EXORterm.

The USE Intercept Module plugs directly into the Development System bus and is used to mount the optional Systems Analyzer Module. A cable assembly couples the selected control signals between the Systems Analyzer and the USE Processor Module.

The USE Cable and Buffer Assembly connects the USE Processor Module into the user's system. A 40-pin connector on this assembly plugs into the MPU socket in the user's system permitting the USE Processor Module's MPU to control the operation of the user's system. In this application, everything within the EXORciser/EXORterm appears to be within the MPU in the user's system. Through special jumper connections, this assembly also can transfer the timing signals required by the dynamic memories in the Development System to operate with the user's system clock. In addition, the USE Cable and Buffer Assembly buffers the transferred signals.

MEX68USEB
User System
Evaluator B

Features

- Extends the EXbug functions into the user's M6800 or M6802 system.
- Operates from the user's system clock or from the EXORciser/EXORterm internal clock.
- Permits the user to share the EXORciser/EXORterm memory and input/output modules with the user's system.
- Extends the optional Systems Analyzer Module's functions into the user's system when the Systems Analyzer is used with the Development System.
- Provides convenient block/fault isolation.
- Uses present commands - no new protocol to be learned.
- Automatic system configuration - no need to enter memory locations; Development System modules are given priority over external memory at the same address.
- Jumper selectable for M6800 or M6802 USE (shipped as M6800 USE).

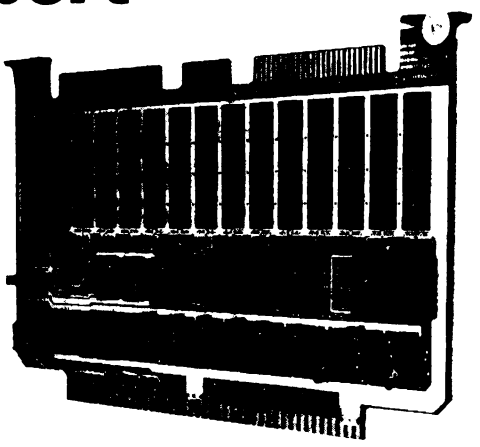
Ordering Information

The following table identifies the options of the MEX68USEB user System Evaluator B Module. For further information, contact your local sales office.

Part Number	Description
MEX68USEB	USEB, including Processor Module, Intercept Module, Cable and Buffer Assembly
MEX68USE2B	USEB Cable and Buffer Assembly (used to update previous MEX68USE to 6800/6802 capability)
M68DTTU2B	EXORciser with USEB, Table Top, 220 Vac
M68SXS102B0	EXORterm 200 with USEB, 220 Vac
MEX68USEB(D)	User System Evaluator User's Guide

MOTOROLA MICROSYSTEMS

MEX68USM Universal Support Module



- Fully decoded switch selectable address capability
- Large wire-wrap socket area for custom circuitry
- Fully buffered bi-directional address bus and data bus
- 20 pin header for implementation of priority interrupts, multi-paged memory, and special I/O systems
- Jumper selectable memory map assignment
- Two 50 pin edge connectors and one 20 pin edge provides custom circuitry interface.

The MEX68USM Universal Support Module provides the user with the capability to design a unique module to implement the M6800 family of parts. The complete development system bus is available for the user to implement by header, platforms, wire-wrap sockets, or switch selection. Three I/O edge connectors provide 120 lines accessible at plated-through holes.

Four hexadecimal address select switches allow the user to generate a fully decoded chip select. In addition, two header areas provide a "don't care" option on each address line.

Specifications

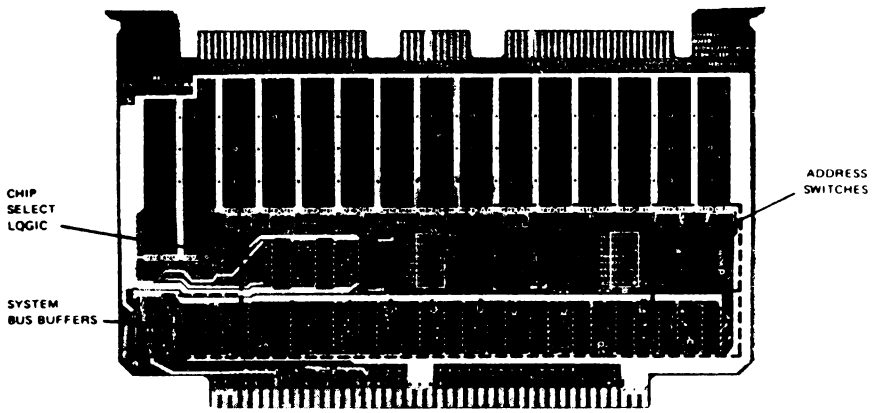
Address and Control Bus	TTL voltage compatible
Logic "0"	0.0–0.85 V (200 μA max at 0.4 V)
Logic "1"	2.0–5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0–0.85 V (200 μA max at 0.4 V)
Input Logic "1"	2.0–5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at 10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	+5 Vdc @ 2A max +12 Vdc -12 Vdc
Physical Dimensions	
W x H x T	9.75 x 6.00 x 0.062 in.

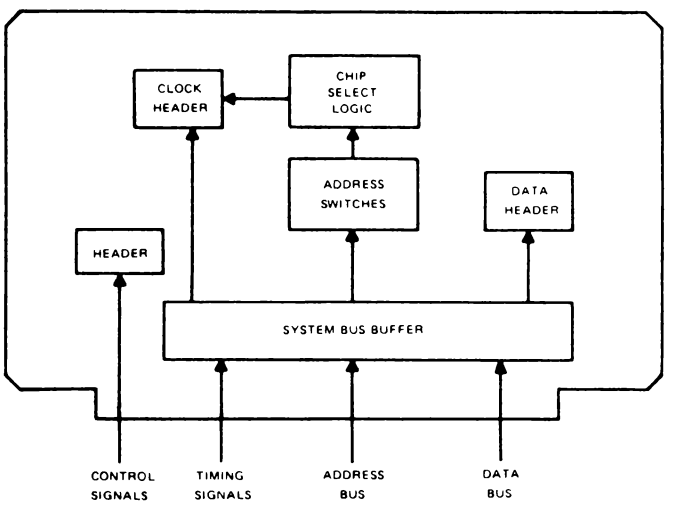
Ordering Information

The following table lists the information necessary for ordering modules, or manuals.

TYPE NUMBER	DESCRIPTION
MEX68USM	Universal Support Module
MEX68USM(D)	User's Guide

MEX68USM UNIVERSAL SUPPORT MODULE

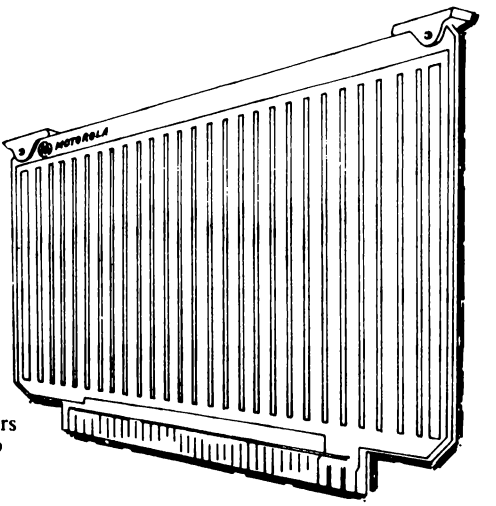




MOTOROLA

MEX68WW Wirewrap Module

Option



- Standard size EXORciser plug-in module
- Compatible with the EXORciser bus
- Standard pin spacing for 14, 16, and 24-pin wirewrap sockets
- Provisions for two 50-pin flatribbon cable connectors
- Permits user to incorporate his custom circuits into the EXORciser emulated system

The MEX68WW Universal Wirewrap Module permits the user to construct and incorporate his custom circuits into an EXORciser emulated system. Incorporated on the module are the power bus and the ground bus printed wiring runs. Also, the module has standard pin spacing and provisions for 14, 16, and 24-pin wirewrap sockets and for two 50-pin wirewrap flatribbon cable connectors.

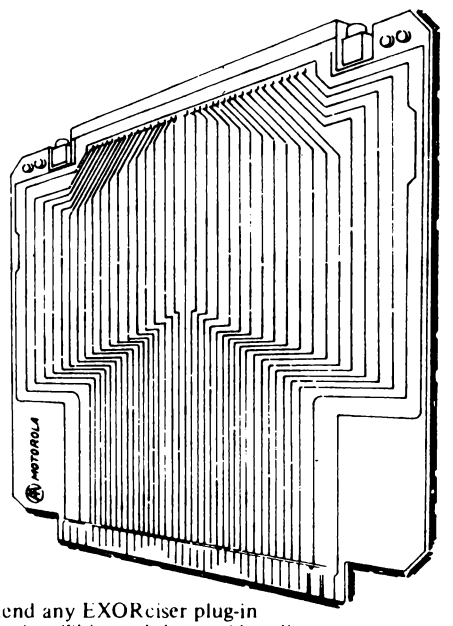
Specifications

Physical Dimensions:

W x H x T	9.75 x 5.75 x 0.062 in.

MEX68XT Extender Module

Option



- Extends any EXORciser plug-in module for testing, trouble-shooting, and debugging
- Interfaces with all EXORciser plug-in modules
- Compatible with the EXORciser bus
- Provides clip-on test points for all EXORciser bus signals

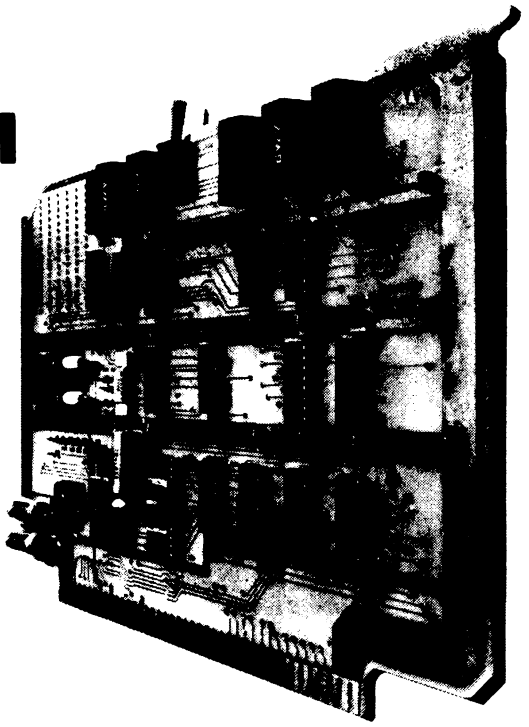
The MEX68XT Extender Module enables the user to extend any EXORciser plug-in module for servicing, testing, trouble-shooting, and debugging. This module provides clip-on test points, giving the user access to the EXORciser bus.

Specifications

Physical Dimensions:

W x H x T	9.75 x 9.00 x 0.062 in.

MGD6800DSM Data Security Module



- NMOS LSI implementation of DES
- 400Kbps operation (excluding software overhead)
- Block cipher or cipher feedback operating modes
- Switch selectable memory addresses
- Optional EROM capability
- EXORciser & Micromodule compatible
- TTL Voltage compatible

Description

The MGD6800DSM Data Security Module (DSM) provides encryption capability for the M6800 EXORciser and Micromodule systems. The algorithm employed in the DSM is the Data Encryption Standard (DES) as adopted by the U.S. Department of Commerce National Bureau of Standards (ref. FIPS PUB 46). The DES algorithm is implemented within a custom single chip NMOS LSI device. Provision is made on the DSM for inclusion of an optional MCM68708 or equivalent EROM for control program or encryption key storage. The DSM contains all circuitry required for total interface compatibility with any M6800 EXORciser or Micromodule system. Hexidecimally-coded switches are provided to allow the user to locate the base address of the DSM functions and the optional EROM anywhere within the allowable system memory field.

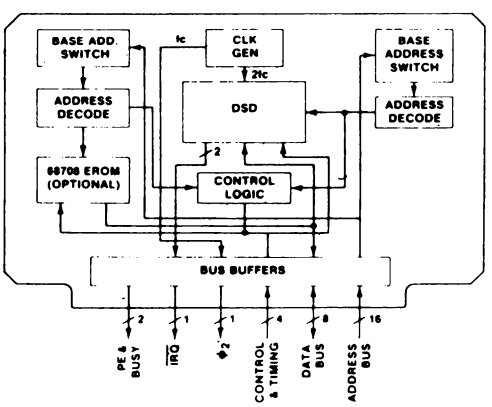
The DSM encryption functions include:

- enciphering data
- deciphering data
- loading of key (immediate active or major)
- loading and processing of previously ciphered key for immediate active utilization
- restoration of major key for immediate active utilization

The DSM provides active key parity status and algorithm processing status. These signals may be used to control data encryption for either polling or interrupt driven architectures.

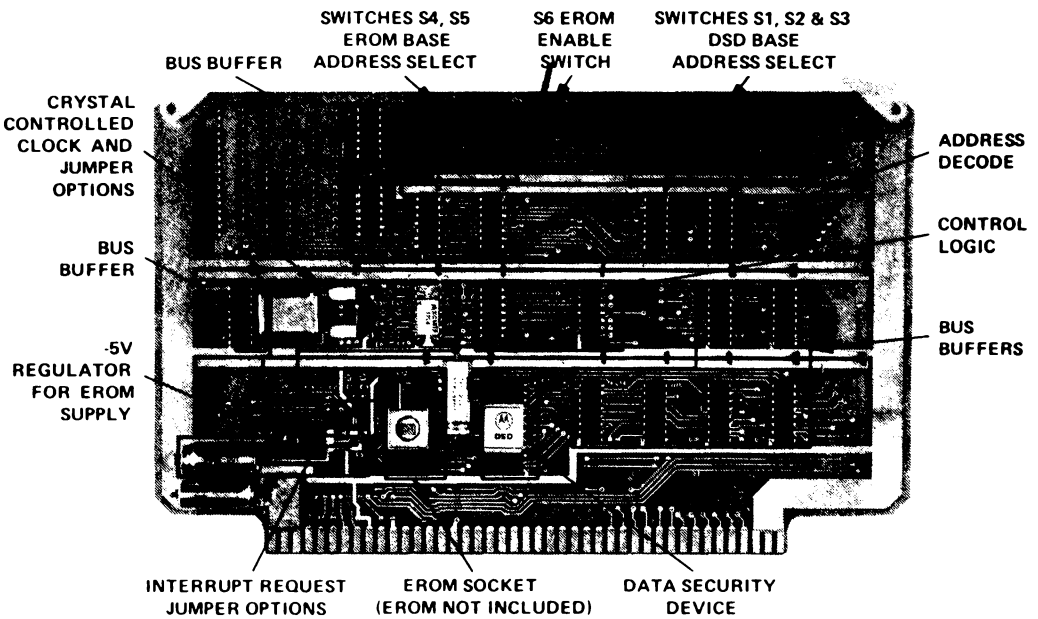
The DSM is designed to encipher or decipher 64 bit blocks of data under the control of a 56 bit key. Algorithm processing time is a direct function of clock rate with the minimum time being 160 μ seconds for a 64 bit block of data (DSM clock rate = 2.0 MHz and phase coherent MPU clock rate = 1.0 MHz). The total effective data encryption throughput rate in a specific system application is a function of the encryption mode utilized (e.g., block mode or cipher feedback mode) and the user-defined system control software/firmware.

A spare section of the DSM is configured as a 0.1" by 0.3" spaced matrix pattern for standard wire wrap sockets to accommodate special user defined circuitry.

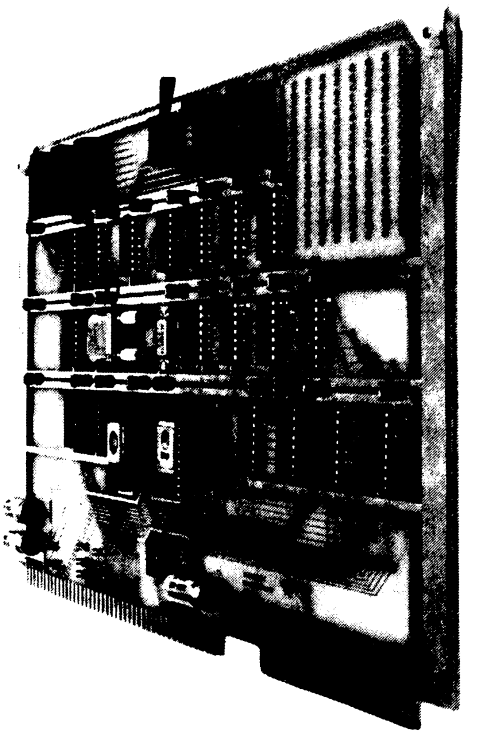


Specifications

Power Requirements		**+5 VDC at 900 mA max**
		+12 VDC at EROM spec
		-12 VDC at EROM spec plus 8 mA
Input Signals (address)	Logic '0'	**0.0-0.85V (-200 μA max at 0.4V)**
	Logic '1'	**2.0-5.25V (25 μA max at 5.25V)**
Input Signals (control)	Logic '0'	**0.0-0.8V (-400 μA max at 0.5V)**
	Logic '1'	**2.0-5.25V (40 μA max at 2.4V)**
Status Outputs (open collector)	Output Logic '0'	**0.5V max at 24 mA**
	Output Logic '1'	**250 μA through resistor to 5.25V with Vcc = 4.75V**
Data Bus	Input Logic '0'	**0.0-0.85V (-200 μA max at 0.4V)**
	Input Logic '1'	**2.0-5.25V (25 μA max at 5.25V)**
	Output Logic '0'	**0.5V max at 40 mA**
	Output Logic '1'	**2.6V min at -10 mA**
	Output OFF-STATE Leakage	**100 μA max at 2.6V**
Algorithm Process Time		**320 clock cycles, software overhead excluded**
Clock Frequency (2 x fc)		**100 kHz to 2.0 MHz**
Operating Temperature		**0 to 70° C**
Physical Dimensions W x H x T		**9.75 x 5.75 x 0.062 in.**



MGD8080DSM Data Security Module



- Data Encryption Standard (DES) algorithm
- NMOS LSI implementation of the DES
- 160 μ sec. algorithm process time (excluding software overhead)
- Block cypher or cypher feedback operation
- Switch selectable memory addresses
- Compatible with Intel® MDS and SBC Modules
- TTL voltage compatible

Description

The MGD8080DSM Data Security Module provides encryption capability for the Intel® MDS development system and SBC module family. The algorithm employed in the DSM is the Data Encryption Standard (DES) as adopted by the U. S. Dept. of Commerce National Bureau of Standards (ref. FIPS PUB 46). The DES algorithm is implemented within a custom, single chip, NMOS LSI device. Provision is made on the DSM for inclusion of an optional MCM68708 or equivalent EROM for control program or encryption key storage. The DSM contains all circuitry required for total interface compatibility with any MDS or SBC system. Hexidecimally-coded switches are provided to allow the user to locate the base address of the DSM and the optional EROM within the allowable system memory field.

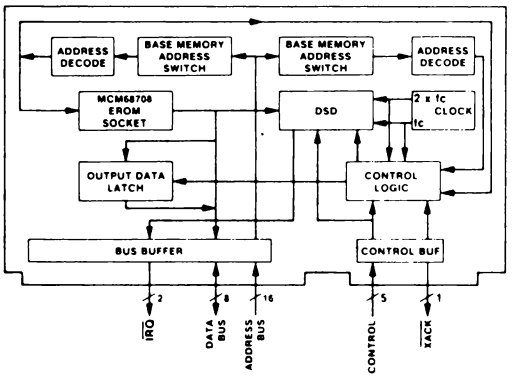
The DSM encryption functions include:

- enciphering data
- deciphering data
- loading of key (immediate active or major)
- loading and processing of previously ciphered key for immediate active utilization
- restoration of major key for immediate active utilization

The DSM provides active key parity status and algorithm processing status. These signals may be used to control data encryption for either polling or interrupt driven architectures.

The DSM is designed to encipher or decipher 64 bit blocks of data under the control of a 56 bit key. Algorithm processing time is a direct function of clock rate with the minimum time being 160 μ seconds for a 64 bit block of data, DSM clock rate = 2.0 MHz. The total effective data encryption throughput rate in a specific system application is a function of the encryption mode utilized (e.g., block mode or cipher feedback mode) and the user-defined system control software firmware.

A spare section of the DSM is configured as a 0.1" by 0.3" spaced matrix pattern for standard wire wrap sockets to accommodate special user defined circuitry.

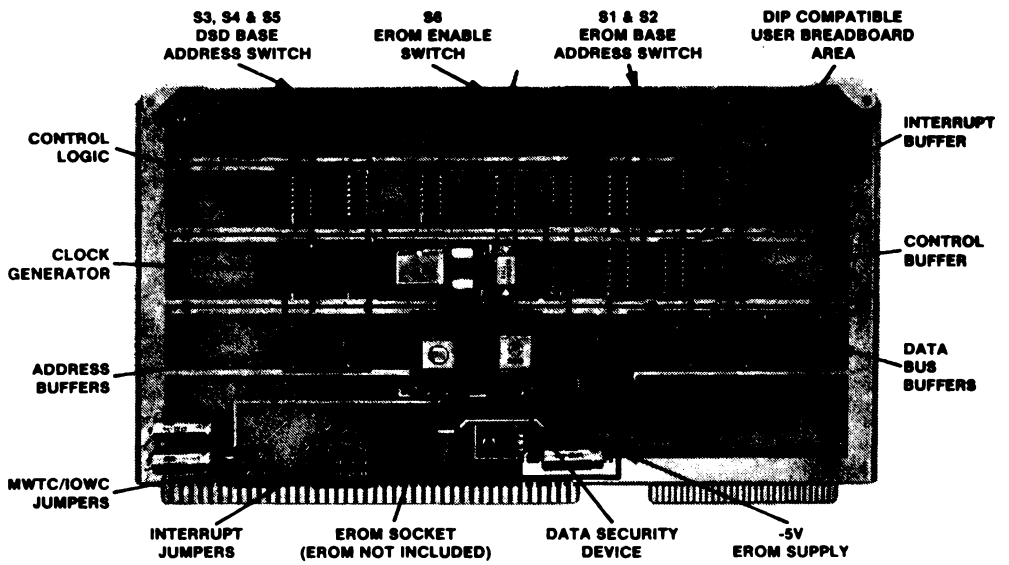


*Registered Trademark of INTEL Corporation

NOTICE: These products may not be exported without prior approval from the U.S. Dept. of State, Office of Munitions Control.

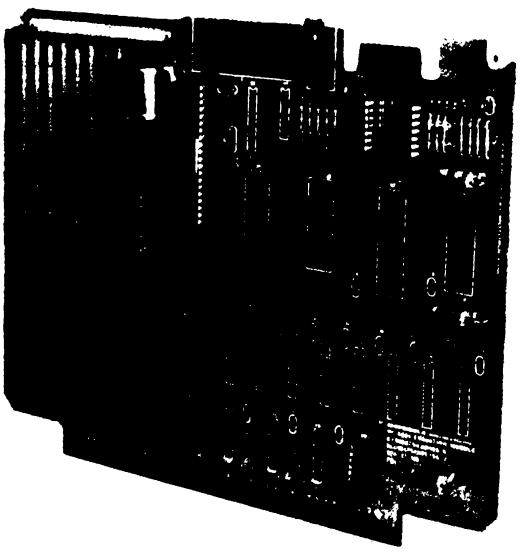
Specifications

Input Signals	Logic "0"	0.0-0.85V (-200 μA max. at 0.4V)
(control)	Logic "1"	2.0-5.25V (25 μA max. at 5.25V)
Input Signals	Logic "0"	0.0-0.8V (-2.0 mA max at 0.5V)
(address)	Logic "1"	2.0-5.25V (1.0 mA max at 5.5V)
Data Bus	Input Logic "0"	0.0-0.85V (-200 μA max at 0.4V)
	Input Logic "1"	2.0-5.25V (25 μA max at 5.25V)
	Output Logic "0"	0.5V max at -40mA thru resistor to Vcc
	Output Logic "1"	2.6V min at -10mA thru resistor to gnd.
	Output OFF State Leakage	100 μA max at 2.6V
Operating Temperature		0 to 70°C
Power Requirements		+5V at 1A max.
		+12V at EROM MFG's spec
		-12V at EROM MFG's spec plus 8 mA
Algorithm Operation		320 Cycles (software overhead excluded)
		160 μ sec at 2MHz DSD clock
Data Output		500 nsec per 8 bit byte
Physical Dimensions W x H x T		12.0 X 6.75 X 0.062 inch



MOTOROLA Microsystems

MEX6801EVM Evaluation module



Features

- Single Module – EXORciser-bus Compatible
- Incorporates an MC6801 Debug Monitor
- Provides RS-232C Interface
- Sockets can be added to incorporate Optional ACIA, PTM, 2K EPROM and 4K Bytes of Static RAM.
- Address Map Established by ROM to Permit Reconfiguration
- Additional Decoding Provided for 8K of Off-Board Memory
- Large Wire Wrap Area
- Two Modes of Operation: Single Chip or Expanded
- Low Cost

GENERAL DESCRIPTION

The MEX6801EVM Microcomputer Evaluation Module is a completely self-contained microcomputer on a single printed circuit card. The Microcomputer Evaluation Module provides the user with the means of evaluating the MC6801 microcomputer.

The system allows the user to easily evaluate the MC6801 microcomputer. As configured, the MC6801 may be evaluated in either the Single Chip or Expanded mode by attaching an RS-232C-compatible terminal to the serial port of the Module. Thus, the minimum functioning system consists of only the MC6801 and an MC1488 and MC1489.

The Evaluation Module provides the user with the ability to evaluate the MC6801 microcomputer in the Single Chip mode using the debug monitor via the serial I/O port and RS-232C interface. Refer to Table A for a description of the debug commands. A 2.4576 MHz crystal is used to generate the standard baud rates of 150, 600, and 4800 baud. Sufficient space remains within the on-chip RAM for the user to write a small I/O program to work in conjunction with the debug monitor. The debug monitor program (LILBUG) uses a patch table established within RAM for all I/O. Thus, the debug program's I/O routines can be readily modified by the user for the purpose of evaluation. Since the debug monitor uses the timer output and the serial I/O port, these resources are not available to the user in the Single Chip mode. However, by using the Expanded mode, the user has the choice of adding an ACIA or PTM, thereby freeing more of the on-chip resources. The Evaluation Module has provision for adding 4K bytes of static RAM and a 2K byte EPROM. This permits to develop his programs if desired. In addition, the Expanded mode allocates 8K bytes of off-board program space for further programming flexibility.

A wirewrap area is provided to permit the user to interface other peripheral devices or special interface circuits to the MC6801.

TABLE A. MEX6801EVM Debug Commands

COMMAND	EXPLANATION
L	Load a program from tape.
L <OFFSET>	Load a program from tape with an offset.
V	Verify that a program was properly loaded.
V <OFFSET>	Verify that a program was properly loaded with an offset.
D <ADDR1>,<ADDR2>	Display contents of memory from <ADDR1> to <ADDR2>.
P <ADDR1>,<ADDR2>	Punch/record on tape the contents of memory from <ADDR1> to <ADDR2>.
M <ADDR>	Examine/modify the contents of the specified address location.
<DATA>	Enter one byte of data to replace the value at the current address location.
LF	Display the contents of the next sequential memory location on the next line and enable the contents of this location to be changed (LF = Line Feed).
SP	Display the contents of the next sequential memory location on the same line and enable the contents of this location to be changed (SP = SPace).
,	Increment the memory location pointer, but do not display the address or data. The contents of this memory location may still be changed. This entry permits data to be entered at sequential memory locations without displaying the current address or data.
UA	Display the contents of the previous memory location on the next line and enable the contents of this location to be changed (UA = Up Arrow).
/	Display the current address of the memory location pointer and the contents of that location.
CR	Terminate the memory examine/modify command and accept next command (CR = Carriage Return).
<ADDR> /	Display the contents of the specified address location and enable the contents of this location to be changed.
/	Display the address and contents of the memory location last referenced by the memory examine/modify command.
O <ADDR1>,<ADDR2>	Calculate the relative offset of a branch instruction from ADDR1 to ADDR2.
B	Display all breakpoints.
B -	Delete all breakpoints.

COMMAND	EXPLANATION
B <ADDR>	Enter a breakpoint at the specified address.
B -<ADDR>	Remove a breakpoint at the specified address.
G <ADDR>	Start program execution at the specified address.
G	Start program execution at the current program counter setting.
R	Display/change the contents of the program registers and counter. Register contents are displayed using the following format: P-XXXX X-XXXX A-XX B-XX C-XX S-XX P- where: P = Program Counter X = Index Register A = Accumulator A B = Accumulator B C = Condition Code Register S = Stack Pointer XXXX = Current 16-bit value XX = Current 8-bit value
<DATA>	Replace current register value with new DATA.
SP	Display current register value (unless changed by the <DATA> command). Close the current register and display the next register mneumonic and dash. The R command terminates after examining/changing the stack pointer or whenever any character other than <DATA> or SP is entered (SP = SPace).
.	Trace one instruction.
T <HEX NUMBER>	Trace the number of instructions specified in hexadecimal.
C <ADDR>	Call and execute a user routine as a subroutine starting at the specified address. A return address to the debug program is stored in the user's stack. When the user's RTS instruction is executed (at the end of the user's routine), the debug program regains program control and the current contents of the registers are displayed.
C	Same as the C <ADDR> command except that the execution begins from the current address in the program counter.
LO	Set low speed–30/15 characters per second for on-chip clock.
HI	Set high speed–120/60 characters per second for on-chip clock.

MOTOROLA

M68ADS.
M68ADW.

POLYVALENT DEVELOPMENT SYSTEM

AUTONOMOUS DEVELOPMENT SYSTEMS

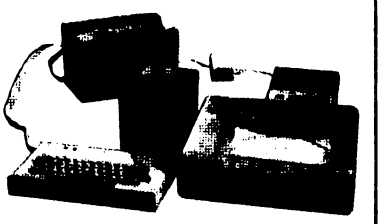
AUTONOMOUS DEVELOPMENT SYSTEM

The M68ADS. is a complete development system including facilities for developing a hardware/software design and provides a very cost effective CRT terminal capability that avoids the use of the noisy and slow teletypewriter. The Autonomous Development System consists of:

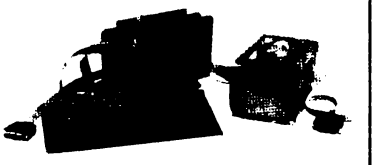
- 1 M68MEB1 Microprocessor Evaluation Board which includes:
  - 1 M68SAC1 Stand Alone Computer
  - 1 MEC68MIN2 MINIBUG II Firmware
- 1 M68DIM Display Interface Module
- 1 M68MDM1 5" Display Monitor
- 1 M68IOS1 Input/Output Supervisor Firmware
- 1 M68KBD1 Full ASCII Keyboard
- 1 M68ICC1 Interconnection Cables Set
- 1 M68BSC1 Bus System Card

The M68ADS. can be used as a complete development system with full MINIBUG II and IOS firmware capability or as a multi-terminal for the EXORciser. These configurations are switch selectable.

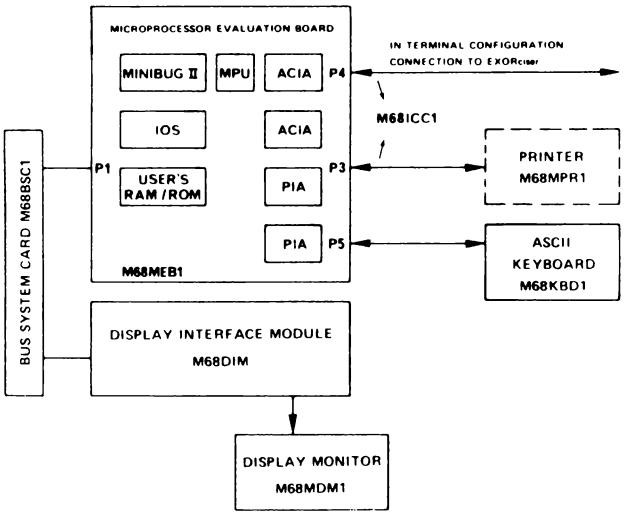
PDS



M68ADS.



BLOCK DIAGRAM



MINIBUG II FIRMWARE FEATURES

MEC68MIN2 ROM
MEC68MIN21 Listing

The Minibug II Firmware provides the user with an efficient means to debug his program. It communicates with a serial peripheral (which can be the IOS ACIA) through an ACIA located in 8008 and works with either 1 or 2 stop bits.

Memory Load	L
Load Binary object tape	Z
Print/Punch Dumps (from vect. A002/A003 to vect. A004/A005).	P
Punch Binary object tape (from vect. A002/A003 to vect. A004/A005)	Y
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC, B, A, X, PC, SP) (saved in stack vect. A008/A009)	R
Go to user's program	G nnnn
Memory test function (from vect. A002/A003 to vect. A004/A005)	W
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ⩾ 300 baud)
ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes
Restart Vector	ROM* (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A00A/A00B)
IRQ Apparent Vector	RAM* (A000/A001)

*1. If the MINIBUG II is used in conjunction with IOS Firmware, the actual vectors are fetched in IOS ROM, but after IOS service, control is given to MINIBUG II which fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the correcponding user's service routine.
The MINIBUG II ROM should be accessed with the following address pattern

1110 00XX XXXX XXXX

2. If the MINIBUG II ACIA (8008) is directly connected to a serial terminal and the IOS Firmware is not present, the actual vectors are fetched in MINIBUG ROM, but then, MINIBUG II fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine.
The MINIBUG II ROM should be accessed with the following address patterns

1110 00XX XXXX XXXX
or 1111 XX XXXX XXXX

Co-resident configuration

The co-resident software MINIBUG II and the user's program communicates with IOS Firmware through the IOS ACIA located at 8010.

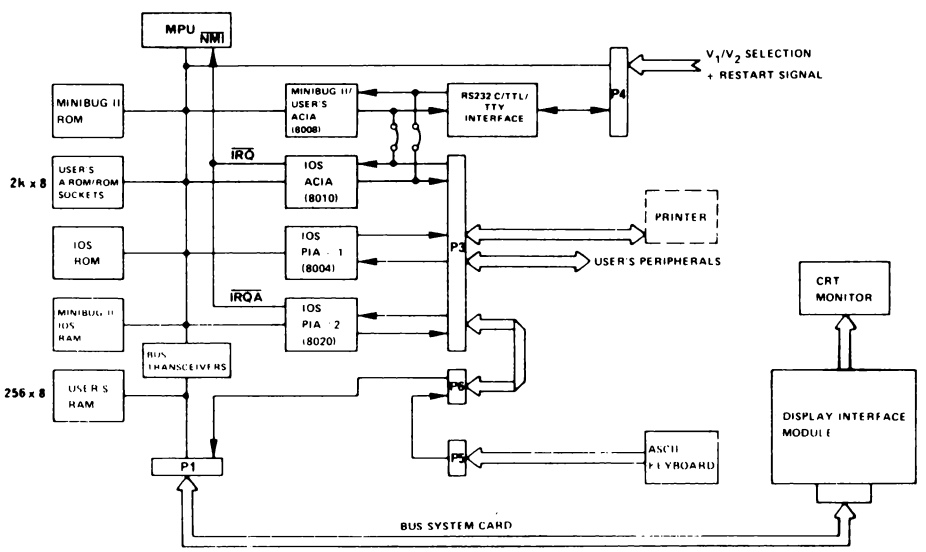
The IOS routines are accessed by NON MASKABLE INTERRUPTS generated by its interfaces. If another source generated the NMI, IOS gives control back to E005 location, which is the MINIBUG II NMI service routine.

– If a character was received in the IOS ACIA (8010) coming from the user's/MINIBUG II ACIA (8008) it is transmitted to the Printer PIA (8004) and to the Display Interface Module. The non-visuable characters are not transmitted.

– If a character was received in the Keyboard PIA (8020), it is transmitted to the IOS ACIA (8010), in order to be received later on in the user's/MINIBUG II ACIA (8008). If CtrlE (Erase screen) or CtrlB (Background Change for subsequent characters) were received from the Keyboard, they are not transmitted to the ACIA.

IOS ROM address	DC00 to DFFF*
IOS RAM address	A000 to A07F shared with MINIBUG II Firmware
IOS ACIA address	8010
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line pointer PIA address	8022
User's Stack Pointer	Saved
Space required in user's stack	28 bytes
Restart action	initializes IOS interfaces, jumps to MINIBUG Restart Routine
NMI action	IOS action and jumps to MINIBUG NMI Routine
SWI, IRQ action	jumps to MINIBUG SWI, IRQ Routine
Start up action	Erases screen, Restart

*The ROM should be wired with the following address patterns:
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX



Terminal Configuration

The external system, as the EXORciser, communicates with the IOS Firmware through ACIA located at 8008.
The characters to be printed are stored in a buffer of 123 characters, which is sent to the printer when full or at least each 300 ms without receiving a new character from the terminal ACIA. The PA7 line of the PIA (8020) is pulled high during Printer Operation. This line should be connected to the CTS line of the main system ACIA (i.e. DEBUG ACIA) in order to inhibit the transmission of new characters.
The Keyboard accesses to IOS routines by generating a NON MASKABLE INTERRUPT.
Two modes of operation are possible:

Local mode (Off-Line)

– The ACIA (8008) is not taken into account.
– The characters received from the Keyboard PIA (8020) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visuable characters are not transmitted.

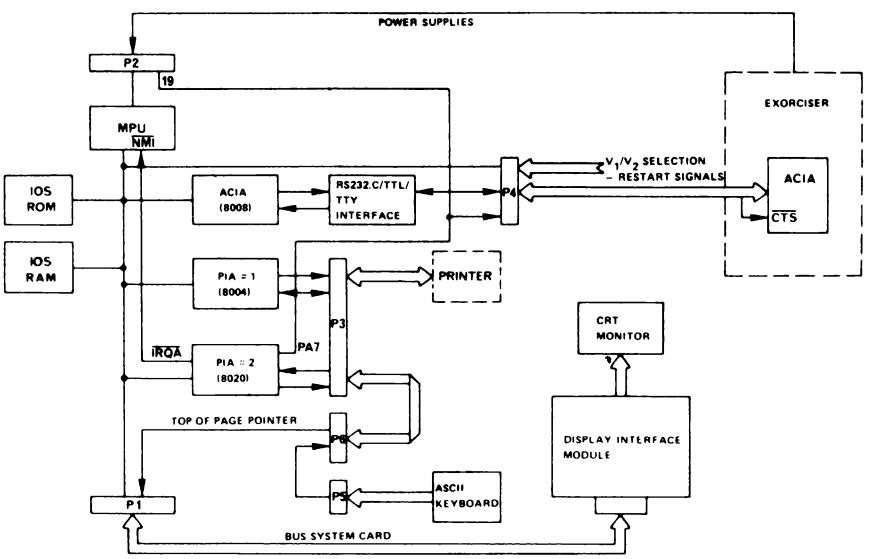
On-Line mode (full-duplex)

– The characters received from the ACIA (8008) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visuable characters are not transmitted.
– The characters received from the Keyboard PIA (8020) are transmitted to the ACIA (8008). All characters, except CtrlB, CtrlE and Ctrl0 are transmitted.

ROM address	DC00 to DFFF*
RAM address:	
scratch pad	A000 to A07F
Printer Buffer	0000 to 007F
ACIA address	8008
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line pointer PIA address	8022
CTS line	PA7 of PIA 8020

*The ROM should be wired with the following address pattern,
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX[1]

[1]Note: in this configuration, A9 is set to 0 by hardware when the MPU accesses to FFF8 to FFFF vectors.



INPUT/OUTPUT SUPERVISOR

The M68IOS1 Input/Output Supervisor Firmware provides the user with an efficient means to interface the Polyvalent Development System Peripherals (CRT, Keyboard, Printer) to either a co-resident MINIBUG Firmware and a user's software or to an external asynchronous line such as the TTY connection of the EXORciser.

- Compatible with M68DIM1 and M68DIM2 16-line x 32-character Display Interfaces
- Compatible with M68DIM6 16-line x 64-character Display Interface
- Can work with co-resident standard I/O routines
- Standard ACIA main system connection (8-bit word, 1 stop bit)
- Cursor control
- Background control (white-on-black or black-on-white display).

When the display page is full, the next line will be displayed at the bottom line, and the whole page is shifted one line up, loosing the top line (Scroll-up Display).

IOS CONTROL CHARACTERS

Code	Effect	Co-resident configuration received by		Terminal configuration		
				Off-line received by Keyboard	On-line received by	
		Keyboard	ACIA (8010)		Keyboard	ACIA (8008)
CtrlE	Erase screen	X	X	X	X	X
CtrlB	Background change for subsequent characters	X	X	X	X	X
CtrlO	Change mode of Operation (local/on-line)	–	–	X	X	X
CtrlG	Sound the bell (negative pulse on CA2 of PIA 8020)	–	X	X	–	X
CtrlU	Cursor Up one line	–	X	X	–	X
CtrlW	Cursor doWn one line	–	X	X	–	X
CtrlN	Cursor to Next character	–	X	X	–	X
CtrlH	Cursor to previous character (Back Space)	–	X	X	–	X
CtrlL	Cursor to home (Form-Feed)	–	X	X	–	X
CtrlC	Clear page from cursor	–	X	X	–	X
CtrlK	Kill line from cursor	–	X	X	–	X
Null	Not transmitted	–	X	X	–	X
Rubout	Not transmitted	–	X	X	–	X

ORDERING INFORMATION

OPTION	DESCRIPTION
M68ADS1	completely assembled and tested system, with a 5" CRT 16-line x 32-character Display
M68ADS6	completely assembled and tested system, with a 5" CRT 16-line x 64-character Display
M68ADW1	completely assembled and tested system, with 16-line x 32-character Interface, without CRT-monitor (for use with a standard TV-receiver, VHF, 55.25 MHz channel E3)
M68ADW2	completely assembled and tested system, with 16-line x 32-character Interface, without CRT-monitor (for use with a standard TV-receiver, UHF, 591.25 MHz, channel E36)
M68ADW6	completely assembled and tested system, with 16-line x 64-character Interface, without CRT-monitor (for use with a M68MDM9 9" CRT-monitor)

ACCESSORIES	DESCRIPTION
M68MDM9	9" CRT-monitor
M68MPR1	Motorola 30 chr/sec. Printer
M68MPP1	Electro-sensitive paper for MPR Printer
M68DMC1	Display Monitor Cabinet for 5" CRT Monitor
M68DMC9	Display Monitor Cabinet for 9" CRT Monitor
M68KBC1	Keyboard Cabinet for M68KBD1
M68EAM1	ROM resident Assembler/Editor Module
M68EAB1	ROM resident Assembler/Editor/BASIC Interpreter Module
MMS68103	16K-byte RAM module
MMS68103-1	8K-byte RAM module
M68CIM1	Audio Cassette Interface Module
M68PPR2	PDS PROM Programmer
M68MMLC2	Chassis with 10-slot card-cage and power-supply
M68MMSC2	Chassis with 5-slot card-cage and power-supply
M68MMCC05	5-slot card-cage
M68MMCC10	10-slot card-cage
MEC68MIN3E	MINIBUG 3E Firmware ROM, with Breakpoints capability.

MOTOROLA

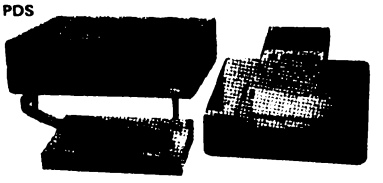
M68TDS.

TOTAL DEVELOPMENT SYSTEM

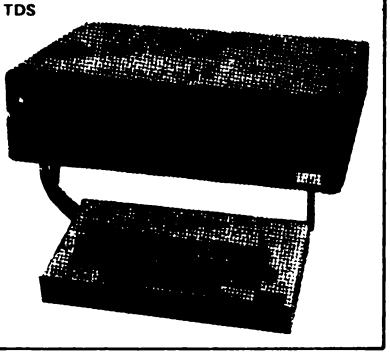
TOTAL DEVELOPMENT SYSTEM

The TDS is a complete development station including facilities for developing a hardware/software design. It consists of a M6800 based system with a full ASCII Keyboard, a 5" CRT Monitor displaying 16 lines of 64 characters, an audio-cassette interface for mass storage capability and a medium speed printer (MPR) interface, assembled in a finished table top cabinet with power supplies. It does not require any other terminal. The TDS also include 8K byte or 16K byte of RAM and a ROM resident Editor/Assembler allowing development of M6800 source code programs. As an option, a ROM resident BASIC interpreter is also available, allowing the TDS to be used with this very widly known high level language.
The resident debugging firmware, MINIBUG 3E, provides the TDS with the capability to insert up to eight software breakpoints and to perform the TRACE function, in addition to the standard LOAD, PUNCH, MEMORY CHANGE, GOTO and CONTINUE functions. The TDS has two spare slots, EXORciser/Micromodule compatible, allowing the user to add options like I/O interfaces, more memory and even a 2708 PROM Programmer (M68PPR1).

PDS



TDS



SPECIFICATIONS

CRT Monitor

Diagonal:	5" (127 mm)
Page format:	16-line x 25 to 64-character (magnifier)

Keyboard

Key layout:	Standard ASR-33 (53-Key)
Character code:	7-bit ASCII (71-character incl. BELL)
Functions keys:	Restart, 300/4800 bps

Printer interface — 7-bit parallel clocked data, TTL compatible

Audio-cassette interface (DIN Connector) — 300 bps, 1-stop bit, 50/500 mVpp, Kansas City Standard

Memory size

M68TDS1:	RAM	8K-byte
	ROM	9K-byte + 3 spare sockets
M68TDS2:	RAM	8K-byte
	ROM	16K-byte + 4 spare sockets
M68TDS3:	RAM	16K-byte
	ROM	9K-byte + 3 spare sockets
M68TDS4:	RAM	16K-byte
	ROM	16K-byte + 4 spare sockets

Power requirement — 220 V, 50 Hz, 0.7 A max.

Power supplies (output max.) 5 V @ 5 A, +12 V @ 1.5 A, 12 V @ 0.5 A

Physical dimensions

Total weight:	12.4 kg (net)
Chassis (W x D x H)	480 x 400 x 160 mm
Keyboard (W x D x H)	330 x 180 x 55 mm

Operating temperature — 0 to 50 °C

ORDERING INFORMATION

M68TDS1	TDS with Editor/Assembler and 8K RAM
M68TDS2	TDS with Editor/Assembler, BASIC Interpreter and 8K RAM
M68TDS3	TDS with Editor/Assembler and 16K RAM
M68TDS4	TDS with Editor/Assembler, BASIC Interpreter and 16K RAM

ACCESSORIES

M68MPR1	Medium speed printer
M68MPP1	Electrosensitive paper for MPR printer
M68PPR2	PDS PROM Programmer

MINIBUG 3E FIRMWARE FEATURES

The MINIBUG 3E Firmware provides the user with an efficient means to debug his program allowing to insert up to 8 breakpoints.

Memory load	L
Print/Punch Dump (from nnnn to mmmm)	P nnnn mmmm
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC, B, A, X, PC, SP) (saved in stack, vect. A032/A033)	R
Go to user's program	G nnnn
Continue execution from current location	C
Execute Next instruction	N
Trace nnnn instructions	T nnnn
Set a breakpoint at address nnnn	V nnnn
Reset the breakpoint at address nnnn	U nnnn
Delete all breakpoints	D
Print out all breakpoints	B
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ⩾ 300 baud)

ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes

Restart Vector	ROM (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A036/A037)
IRQ Apparent Vector	RAM* (A000/A001)

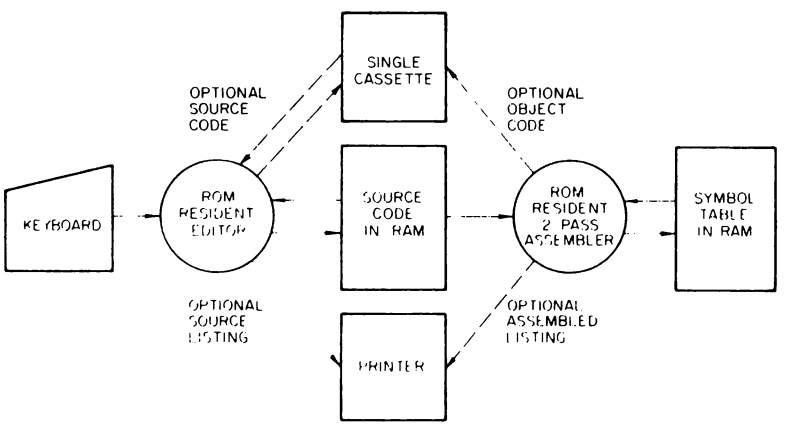
* As the MINIBUG 3E is used in conjunction with IOS Firmware, the actual vectors are fetched in IOS ROM; but after IOS service, control is given to MINIBUG 3E which fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine. The SWI apparent vector (RAM A036/A037) is initialized at E308 (MINIBUG 3E Breakpoint Routine) each time a reset is applied.

EDITOR/ASSEMBLER/BASIC MODULE

This 14K ROM module contains an adapted ROM co-resident Editor/Assembler and a ROM resident BASIC interpreter, to be used on the Total Development System equipped with a single audio-cassette set.
The source and/or the object code can be loaded from or dumped to the cassette. Both Editor/Assembler and Basic run from the ROM, leaving all RAM available as a buffer for source code and symbol table.
The Assembler requires that the source code has been loaded into the RAM by the Editor before performing automatically the two pass assembling. This feature allows to use a non-incremental single audio-cassette system.
The ROM resident BASIC interpreter provides a new tool for problem solving to the M6800 Microcomputer family of parts. BASIC is a high-level programming language widely used for general purpose and certain business-related applications.

- ROM Resident.
- Immediate access without software loading time.
- Uses only a low-cost non-incremental single audio-cassette.
- Software addresses: BASIC: from 4000 to 5BFF;
  Editor/Assembler: from 6400 to 7FFF.
- ACIA address: 8008 (alterable).
- High speed assembling directly from memory.
- Assembler RAM requirement: approx. 1.5K per 50 user's program statements.
- BASIC High Level Language features (TDS2 and TDS4 only):
  - decimal arithmetic;
  - string variable and array;
  - direct statement execution capability (calculator mode);
  - user programs may reside on audio-cassette;
  - optional LET statement;
  - string functions and concatenation.

EDITOR/ASSEMBLER BLOCK DIAGRAM



BASIC Commands

- LIST – display source
- RUN – execute program
- CONT – continue after stop or break
- NEW – define new program
- SAVE – save current program (tape)
- LOAD – load new program (tape)
- APPEND – add to program from tape
- PATCH – patch memory from MINIBUG
- TRACE ON – print line number as it is executed
- TRACE OFF – turn off trace
- LINE LENGTH – define maximum print line length
- DIGITS – establish the number of digits to right of decimal point
- POKE – sets absolute memory address

Subprograms

- DEF – define user function
- RETURN – return from subroutine
- GOSUB – go to subroutine

Intrinsic functions

- TAB – tab on print
- RND – random number
- INT – integer number
- ABS – absolute value
- SGN – sign of argument
- POS – Position of printhead
- LEN – Number of characters in string
- ASC – decimal value of any ASCII character
- CHR$ – string value of ASCII character
- STR$ – ASCII string value to numeric constant
- VAL – numeric constant equivalent to ASCII value
- LEFT$ – returns left-most string of characters
- RIGHT$ – returns right-most string of characters
- MID$ – returns middle string of characters
- PEEK – returns decimal memory value
- SIN – sine
- COS – cosine
- TAN – tangent
- ATAN – arc tangent
- LOG – natural logarithm
- EXP – inverse of LOG
- SQR – square root

BASIC Language Features

Data Types

- Range (1.0E – 99 to 9.99999999E + 99) may be represented as either integer, decimal, or exponential.

Variable Names

- Single alphabetic character or single alphabetic character followed by a digit (0 through 9).
- String variables, single alphabetic character followed by a $.

Arithmetic and Logical Operators

- Exponential
- Negate
- Multiplication
- Division
- Addition
- Subtraction
- Relational operators

Sequence Control Statements

- GOTO
- ON expression GOTO statement n, (m. . . .,1)
- ON expression GOSUB statement n, (m,. . .,1)
- IF relative
- FOR
- NEXT
- STOP
- END

I/O Statements

- INPUT
- READ
- DATA
- PRINT
- RESTORE

Specification Statements

- DIM – dimension variables and strings

Remark Statements

- REM

Optional Statements

- LET

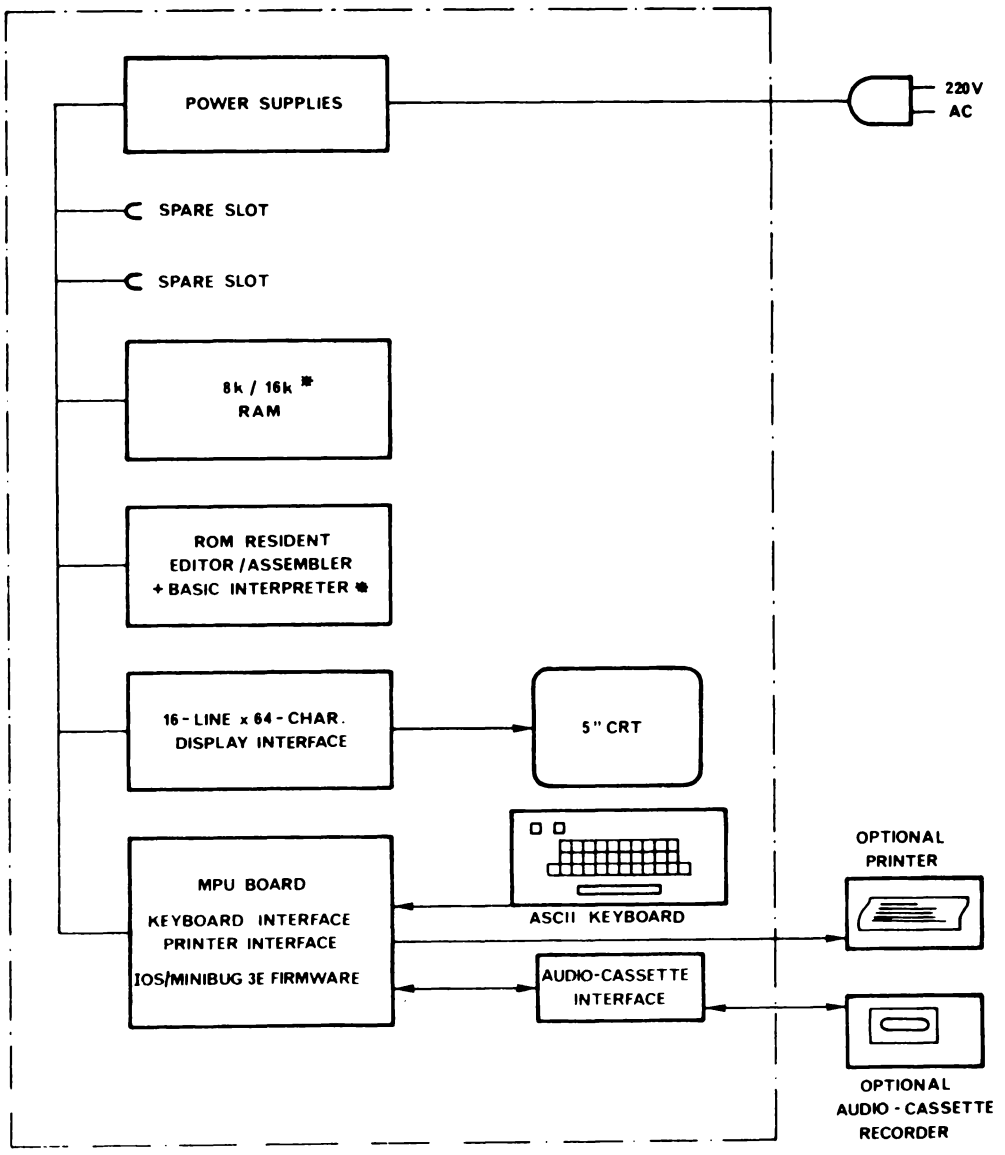
AUDIO-CASSETTE INTERFACE MODULE

The M68CIM1 is used to interface any ordinary audio-cassette recorder with the Total Development System (TDS). The audio-cassette is used as a storage media for object programs and data (dump and load) in general and for source programs when used with the Assembler/Editor or the BASIC interpreter.
The data is recorded on the cassette according the Kansas City standard. In the playback mode, the clock is recovered from the signal and is used to clock the receiving ACIA in the TDS system. This feature allows to cope with cassette speed variations of up to 30% without producing errors.

- Transmission rate : 300 bps
- Logical "1": 2400 Hz signal
- Logical "0": 1200 Hz signal
- Clock frequency: 4800 Hz
- Audio signal output (write): 50 mVpp or 500 mVpp (switchable)
- Audio signal input (read): 500 mVpp min.
- C-60 cassette capacity: approx. 100K-bytes

The module should be connected to an audio-cassette recorder having the following minimum requirements:
– normalized output signal (500 mVpp minimum) on normalized DIN connector;
– HF erasing and polarisation (avoid DC erasing);
– minimum bandwidth: 500 Hz to 6 KHz;
– good mechanical handling (C-90 and C-120 cassettes should be avoided).

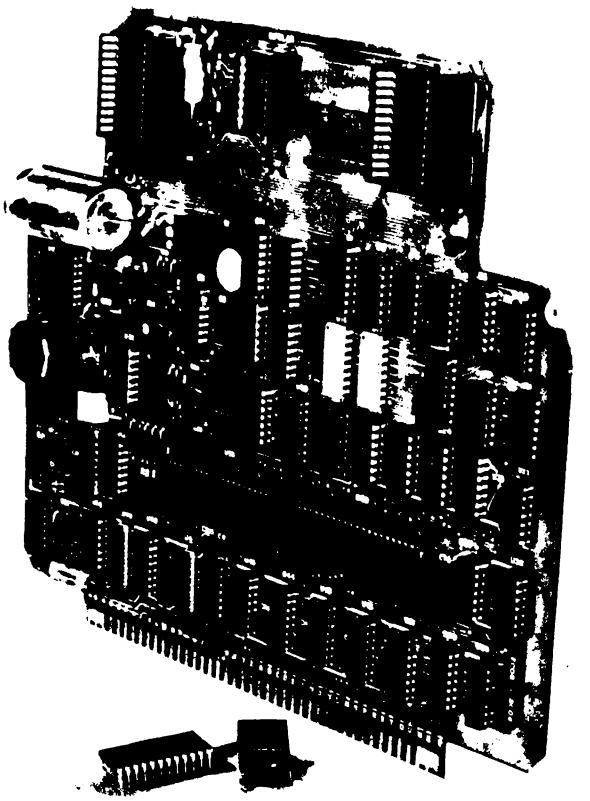
TDS BLOCK DIAGRAM



* OPTIONS

MOTOROLA MICROSYSTEMS

M68PPR2 PDS PROM Programmer



- PDS plug-in compatible.
- Programs following types of PROM/EPROM: MCM7640, MCM7680, MCM68708/2708, MCM7641, MCM7681, TMS2716, or equivalent.
- Allows direct programming from RAM content.
- Verify and back transfer function.
- Uses the +5 V ±12 V PDS bus power supply.
- Dimension (W x H x T): 248 x 192 x 1,6 mm (9.75"x7.50"x0.062").

The M68PPR2 PROM PROGRAMMER provides the PDS with the capability of programming 6 types of PROM/EPROM devices. The control firmware is contained in two ROM and is compatible with the MINIbug Firmware of the PDS. It allows to program (E)PROM devices, to verify the data in the (E)PROM and to transfer data from the (E)PROM to the PDS RAM memory.

Command	Description
CHCK aaa,zzz	Check aaa words of the EROM/PROM starting at EROM/PROM offset zzz for the unprogrammed state.
EXIT	Exit to the system monitor.
OFST nnnn	Set the memory offset parameter nnnn to the value entered.
PROG xxxx,yyyy,zzz	Program the EROM/PROM starting at EROM/PROM offset zzz from memory locations XXXX+nnnn through yyyy+nnnn.
READ xxxx,yyyy,zzz	Read the EROM/PROM to memory addresses xxxx+nnnn through yyyy+nnnn starting at EROM/PROM offset zzz.
SHWP aaa,zzz	Show the EROM/PROM contents in hex form. The ASCII form is also displayed.
STAT	Display the programmer's status.
VERF xxxx,yyyy,zzz	Verify the EROM/PROM starting at PROM offset zzz against memory locations xxxx+nnnn through yyyy+nnnn.
pppppppp	PROM type to be used: pppppppp is the part number. (Example: MCM68708)

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MOTOROLA

M68MEB1

MICROPROCESSOR EVALUATION BOARD

The M68MEB1 Evaluation Board provides the user with a quick and efficient means to evaluate the operating characteristics of the M6800 family of Parts.
The on-board crystal controlled clock circuit provides the module with the capability of working with dynamic memories and slow memories. The clock circuit also generates the basic timing signal used by the module's baud rate generator.
The Microprocessor Evaluation Board interfaces directly with either a TTY (20 mA current loop), a TTL or a RS232-C compatible terminal providing direct communication with the module's MINI-BUG II Firmware.

The MEB consists of:
1 M68SAC1 Stand-Alone Computer
1 MEC68MIN2 Minibug II Firmware ROM

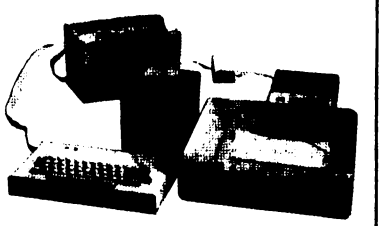
- Four 8-bit parallel Input/Output Ports and Control Lines for Peripheral Interfacing
- Two asynchronous Input/Output Ports with one RS232.C/TTL/TTY Current-Loop interface
- 384 bytes of RAM
- Three MCM68708 or equivalent AROM/ROM sockets
- One MCM6830 Minibug II Firmware ROM
- 921.6 KHz on-board crystal controlled clock generator
- Fully buffered Three-State Bus Connector
- Bus DMA Capability
- Fully compatible with all EXORciser modules

By adding options, the Microprocessor Evaluation Board can be upgraded to an Autonomous Development System.

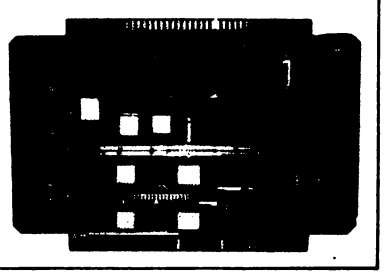
POLYVALENT DEVELOPMENT SYSTEM

MICROPROCESSOR EVALUATION BOARD

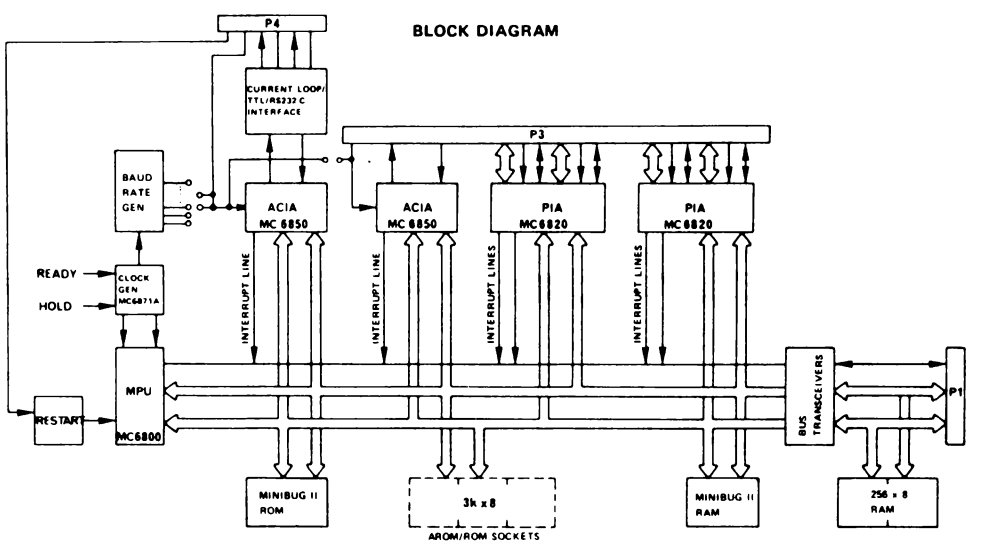
PDS



MEB



BLOCK DIAGRAM



MODULE SPECIFICATIONS

Specification		Value
Memory Size Capability		65, 536 bytes maximum.
On-Board Memory Size		384 bytes of RAM 3 x 1 K-byte MCM68708 compatible AROM/ROM Sockets 1 x 1 K-byte MCM6830 MINIBUG II ROM
Memory locations available for external expansion		44 K-byte: 0000 to 7FFF 9000 to 9FFF B000 to CFFF
Word Size	Data Address Instruction	8 bits 16 bits 8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts; Software interrupt
Clock Signal		921.6 KHz
Address Bus Data Bus Control Bus		Three-state TTL voltage compatible Three-state TTL voltage compatible TTL voltage compatible
MC6820 Peripheral Interface Adapter Lines MC6850 Asynchronous Communication Interface Adapter Serial Transfer Rate Terminal interface		TTL voltage compatible* TTL voltage compatible* 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600 baud RS232.C, TTL or 20 mA Current-Loop
Power requirements		+ 5 Vdc at 1,5 A + 12 Vdc at 200 mA − 12 Vdc at 200 mA − 5 Vdc on board converter
Operating temperature		0° to 70 °C
Dimensions Width Height Thickness PC Board Thickness		 248 mm 9.75 in. 165 mm 6.5 in. 13 mm 0.5 in. 1.6 mm 0.062 in.

*See MC6820 and MC6850 data sheets for specifications on these signals.

Minibug II Firmware Features

MEC68MIN2 ROM
MEC68MIN21 Listing

The Minibug II Firmware provides the user with an efficient means to debug his program. It communicates with a serial peripheral (which can be the IOS ACIA) through an ACIA located in 8008 and works with either 1 or 2 stop bits.

Memory Load	L
Load Binary object tape	Z
Print/Punch Dumps (from vect. A002/A003 to vect. A004/A005).	P
Punch Binary object tape (from vect. A002/A003 to vect. A004/A005)	Y
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC, B, A, X, PC, SP) (saved in stack vect. A008/A009)	R
Go to user's program	G nnnn
Memory test function (from vect. A002/A003 to vect. A004/A005)	W
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ⩾ 300 baud)
ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes
Restart Vector	ROM* (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A00A/A00B)
IRQ Apparent Vector	RAM* (A000/A001)

*The actual vectors are fetched in ROM, but then, MINIBUG II fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine.
To access its ROM vectors, the MINIBUG II ROM should be accessed with the following address patterns:

1110 00XX XXXX XXXX
or 1111 . XX XXXX XXXX

The SWI apparent vector (RAM A00A/A00B) is initialized at E227 (SWI Breakpoint MINIBUG II Routine) each time a Reset is applied.

MOTOROLA

M68CIM1

AUDIO CASSETTE INTERFACE MODULE

The M68CIM1 is used to interface any ordinary audio cassette recorder with any of the Polyvalent Development System configurations (SAC, MEB, ADS) except the terminal configuration.
The audio cassette is used as a storage media for object programs and data (dump and load) in general, and for source programs when used with the assembler/editor or the BASIC Interpreter in the ADS configuration.
The data is recorded on the cassette according the Kansas City standard. In the playback mode, the clock is recovered from the signal and is used to clock the receiving ACIA in the PDS system. This feature allow to cope with cassette speed variations of up to 30% without producing errors.

- Transmission rate: 300 bps.
- Logical "1": 2400 Hz signal.
- Logical "0": 1200 Hz signal.
- Clock frequency: 4800 Hz.
- Audio signal output (write): 50 mVpp or 500 mVpp (switchable)
- Audio signal input (read): 500 mVpp min.
- C-60 cassette capacity: approx. 100 k-bytes.
- Dimensions (HxLxD): 35 mm x 100 mm x 65 mm.

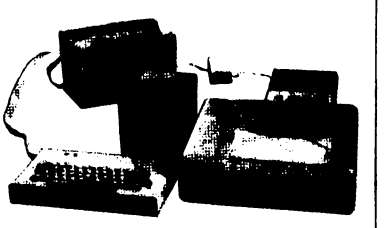
The module should be connected between the PDS ACIA and an audio cassette recorder having the following minimum requirements:

- normalized output signal (500 mVpp minimum) on normalized DIN connector;
- HF erasing and polarisation (avoid DC erasing);
- minimum bandwidth: 500 Hz to 6 kHz;
- good mechanical handling (C-90 and C-120 cassettes should be avoided).

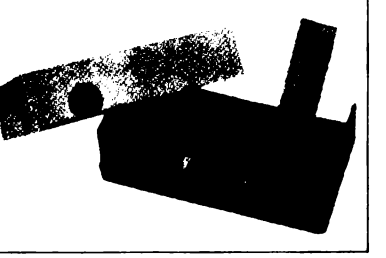
POLYVALENT DEVELOPMENT SYSTEM

CASSETTE INTERFACE MODULE

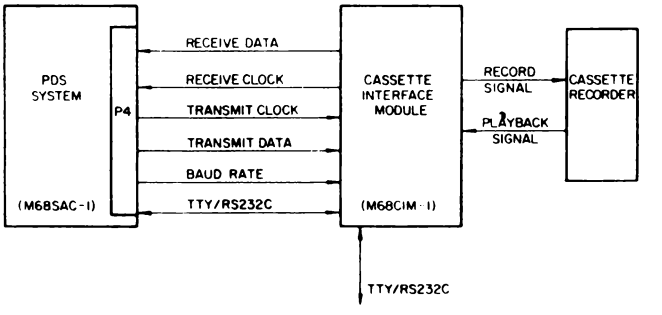
PDS



CIM



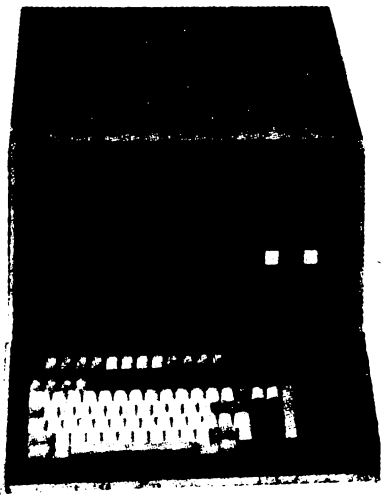
BLOCK DIAGRAM



Specifications subject to change without notice.

M68SXS
EXORterm 200/220

- M6800 Based CRT
- Standard EXORciser DEbug 1 or 2 with USE or MPU 1/2 modules
- Baud rate selectable to 9600 BPS
- Full 1920 character screen
- Easily read characters (7 x 9 dot matrix)
- A single keystroke for direct entry to EXbug, MAID, or DOS
- Isolated motherboard holds up to 8 EXORciser modules
- Dual Memory Map mode of operation (EXORterm 220)
- Selectable clock speeds of 1.0 MHz, 1.5 MHz and 2.0 MHz (EXORterm 220)



EXORterm 200/220, designed and manufactured by Motorola Microsystems, is a display terminal and console expressly personalized for use as a M6800 Development Support System. EXORterm 200/220 facilitates the exchange of data between the user and the system via a high-quality video interface in conjunction with a keyboard. To further enhance the efficiency of the interface, special keys have been encoded to invoke functions unique to the development system in each of its three command levels- EXbug, MAID, and DOS.

A basic EXORterm 200/220 incorporates a CRT chassis with a keyboard and isolated motherboard, MPU Module and DEbug Module. These items provide the basic control and interface functions of a microcomputer, and house the system's EXbug development and diagnostic programs, along with the capability of preparing M6800 Programs. With provisions for up to six more modules (EXORciser modules or Micromodules), a system of almost any complexity can be rapidly assembled.

EXORterm 200 is also offered with a MEX68USEB User System Evaluator (USE) installed in the isolated motherboard in place of the MPU Module. The User System Evaluator provides all the features of the MPU Module, plus it extends all EXbug functions and all of the optional Systems Analyzer functions into the user's system. The USE-equipped EXORterm provides the designer with the capability of configuring an emulation of his M6800 microprocessor system in the terminal, external to the terminal, or a combination of terminal-resident modules working with the user's external system. The designer also can develop his system software and firmware on the terminal, and can use the USE-equipped terminal to debug his system hardware and software. In fact, a USE-equipped EXORterm can even be used to test and evaluate the user's production systems.

In addition to using EXORterm 200/220 as a development system, the terminal may be used as an asynchronous editing terminal through connection to a host computer (or other external device) via the serial interface (RS-232C or current loop), essentially bypassing the isolated motherboard.

EXORterm 220 incorporates several advanced features, including Dual Memory Map mode of operation and the ability to develop higher performance systems, using the MC68A and MC68B series part (1.5 MHz and 2.0 MHz, respectively). The MPU II Module includes also a Timer, MC6840 and a Priority Interrupt Controller, MC6828.

EXORterm 220, through its DEbug II Module, places no restrictions upon the user's system design since all 64K bytes of memory space is available to the user. EXORterm 220 accepts all EXORciser II modules for implementation of such system capabilities as priority interrupts, multi-paged memory and I/O systems, parity error detection and power down/restart features.

Specifications

Display:
12" Diagonal, P4 Phosphor with anti-glare shield
24 lines, 80 characters per line
1920 character full display

Character Configuration:
7 x 9 dot character within a 9 x 12 dot matrix size field

Character Set:
ASCII 96 character subset with Greek alphabet and six special graphics

Cursor:
Blinking inverted video non-destructive 9 x 12 block
Incremental and absolute positioning (Addressable, Readable)

Keyboard:
Encoded, n-key rollover
12 function keys
62 alphanumeric and control keys
12 edit and cursor control keys
LED mode indicators
Full ASCII
Typewriter layout
Movable, detachable
Typamatic all keys

Interface:
Selectable baud rates - 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

Power Requirements:
230 volts ac, 50 Hz
less than 200 watts

Physical Dimensions:
Display - 12.5"H x 18.5"W x 29"D (including keyboard)
Keyboard - 2.7"H x 18.5"W x 9"D
Weight - less than 65 lbs.
Operating Temperature - +10° to + 40°C
Altitude - Not to exceed 10,000 ft.

Ordering Information

The following table identifies the options of the M6800 EXORterm 200 Development System. For further information, contact your local sales office.

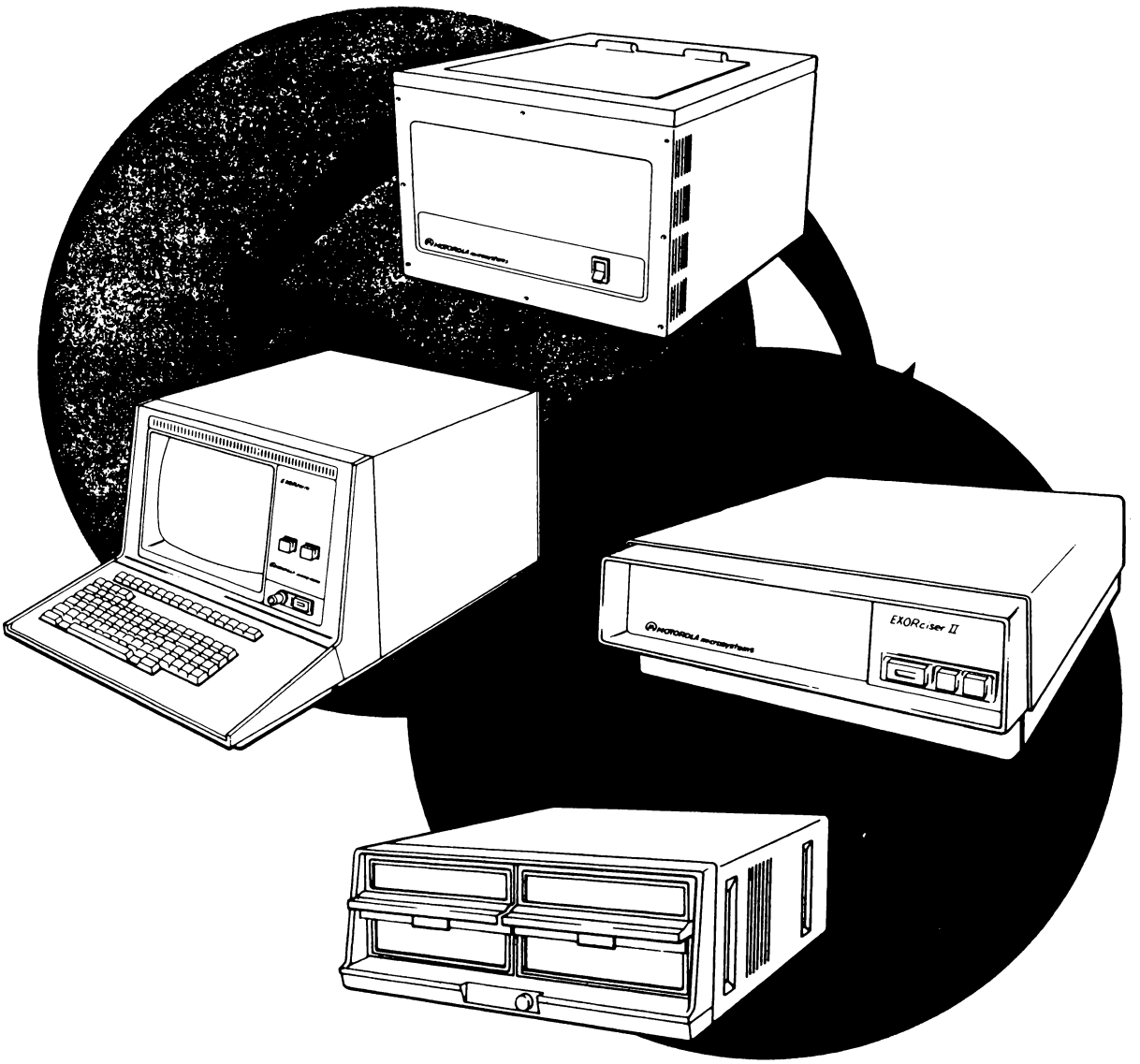
PART NO.	DESCRIPTION
M68SXS10200	EXORterm 200 Development System 220 V
M68SXS102B0	USE EXORterm 200 Development System 220 V
M68SXS2202	EXORterm 220 Development System 220 V

MOTOROLA MICROSYSTEMS

MACE 29/800

Microcode Analyzer and Control Storage Emulator

A Microprogrammable Processor Development System



MICROPROGRAMMED SYSTEMS

For some applications, LSI processors with fixed instruction sets and data widths are being used as replacements for random logic designs. Although these processors are very satisfactory for some new designs, their systems architectures are fixed. Consequently, they cannot be used optimally to emulate existing machine architectures and instruction sets.

On the other hand, bit-slice processors such as Motorola's M10800 ECL and M2900 LSTTL families permit alterable instruction sets and data widths. Both families are microprogrammable to emulate almost any instruction set and to optimize system instructions. The devices in both families perform special functions (i.e., ALU, microprogram control, memory I/O control, timing, etc.); this partitioning allows the devices to be connected, in varying configurations, to resemble many existing machine architectures. The M10800 family is compatible with Motorola's MECL 10,000 logic series, the M2900 is supported by a growing array of LSTTL devices.

Microprogramming and configurable multichip sets can be very practical tools to develop high throughput, cost-effective processor and controller systems. However, the combinations of hardware and software possibilities (the very advantages of microprogrammable devices) can lead to time-consuming design tradeoffs.

To minimize the time required to develop microcode for M2900/10800 processor/controller systems, as well as other MSI/LSI microprogrammed logic designs, Motorola now offers the Microcode Analyzer and Control Storage Emulator (MACE 29/800).

MOTOROLA MICROPROGRAMMING SYSTEM MACE 29/800

The MACE 29/800 is a development and diagnostic aid for microprogrammable processors and controllers. Its primary functions are.

- To provide Writable Control Storage (WCS) for microprograms
- To provide real-time microprogram diagnostic capabilities

The MACE 29/800 replaces the user's microprogram memory and interfaces with the user's system timing and data flow, as shown in Figure 1. In this configuration, the user can write or change microcode and/or run diagnostics on the system prototype.

The MACE 29/800 is housed in a 19" W X 19.5" D X 10.5" H chassis. The chassis contains power supplies, a multilayer backplane, and a 10-slot card cage. Printed-circuit modules containing WCS (microprogram memory), diagnostic, timing, control, and interface hardware are mounted in the card cage. The chassis can be used first as a "breadbox" to build user prototype systems in the remaining card slots. As a second use, cable interfaces that connect to the chassis hardware are available for external user-developed prototypes. Lastly, to take advantage of the high-speed backplane and available power supplies, the chassis can be used to house totally independent prototypes. The MACE 29/800 can power and support both TTL and ECL logic systems. In addition, interface address and data lines can be defined as active high or active low.

The WCS is expandable in both depth and width. Maximum ratios are 2K words X 112 bits, 4 K words X 48 bits, 6K words X 32 bits or 8K words X 16 bits. Intermediate configurations are also allowable. Depending on the configuration, memory-access times range from 50 ns to 80 ns. WCS is comprised of high-speed, bipolar RAMs; consequently, system prototypes can be operated at or near the maximum clock rate to minimize debug time and to detect ac glitches. Memory load, verify, modify, dump, and store are all under user control.

A programmable-frequency clock (20 MHz maximum frequency in 25 ns period increments) can operate in start, stop, single-step, and continue modes.

Optional real-time diagnostic capabilities include debug functions, memory- address sequence, 16 selectable inputs and clock control. A microprogram address and user data trace RAM, which can store 256 locations, provides a logic analyzer diagnostic function. Address sequencing, register contents, status bits, etc., can be traced and saved under various trigger modes. Typical diagnostic functions include: trace/save on a beginning, middle, or end reference address; stop on a reference address; jump on a reference address; and, clock-mode control.

COMPLETE MICROPROGRAMMING SYSTEM CONFIGURATION

The MACE 29/800 is controlled by the M6800 host computer of an EXORciser-bus compatible system. To a user, all microprogramming tasks appear as M6800-oriented operations. A software package, included with the MACE 29/800, performs the necessary translations. This configuration takes advantage of the extensive hardware and software components that have been developed for the EXORciser. Some inherent features of the host EXORciser are:

- Working storage (RAM and ROM) is available in the EXORciser
- EXbug monitor firmware available in the EXORciser
- EXORciser compatible with the EXORterm CRT terminals (for user interface)
- EXORciser compatible with the EXORprint printer (for hard-copy printout)
- EXORciser compatible with the EXORdisk II floppy-disk system (for bulk data storage)
- EXORciser resident software available (Assembler, Editor, Macroassembler, Linking Loader, Fortran Compiler, Basic Interpreter)
- MDOS (Motorola Disk Operating System for EXORdisk II)

Utilizing the MDOS, the MACE 29/800 utility and debug software tool, MBUG, is supplied resident on a floppy disk. MBUG's basic features include:

- A command package to load a disk into microprogrammed control storage, to change control storage, and write changes back to a disk file.
- Commands to enable user's address to memory.
- Commands to start or stop the clock, and to single cycle the clock.

The MACE Assembler, resident on a floppy disk and also utilizing the MDOS features, provides a general purpose assembler specifically designed to meet the needs of bit slice microprogrammed processor development. Flexible format statements permit microword size and format to be user-defined and thus applicable to any hardware configuration.

Optional features supplied with MACE 29/800 provide real-time diagnostic capabilities. These include:

- Microprogram address and user trace RAM.
- Trace/save on a beginning, middle or end reference address.
- Jump or stop on reference address.
- Multi-level breakpoints.

SUPPORT PRODUCTS FOR MICROPROGRAMMABLE PROCESSORS

M10800 PROCESSOR FAMILY (ECL)

MC10800L	4-Bit ALU Slice
MC10801L	Microprogram Control Function
MC10802L	* 4-Phase Timing Function
MC10803L	Memory Interface Function
MC10804L	4-Bit MECL-TTL Bidirectional Transistor
MC10805L	5-Bit MECL-TTL Bidirectional Transistor
MC10806L	32 X 9-Bit Dual Access Stack
MC10807L	* 5-Bit MECL-MECL Bidirectional Translator
MC10808L	16-Bit Programmable Shifter Function

* To be introduced.

MECL 10,000 MEMORIES

MCM10139L	32 x 8-Field PROM (15 ns)
MCM10143L	8 x 2 Multiport Register File (RAM) (10 ns)
MCM10144L	256 x 1-Bit RAM (26 ns) (10410)
MCM10145L	16 x 4-Bit RAM (15 ns)
MCM10146L	1024 x 1-Bit RAM (29 ns) (10415)
MCM10147L	128 x 1-Bit RAM (12 ns) (10405)
MCM10149L	256 x 4-Field PROM (25 ns)
MCM10152L	256 x 1 RAM (15 ns)

(MECL 10,000 Device Support: Over 75 Device Functions)

M2900 PROCESSOR FAMILY (LSTTL)

MC2901	4-Bit ALU
MC2901	4-Bit ALU (Redesign)
MC2901A	4-Bit ALU (Faster)
MC2902	Look-Ahead Carry
MC2905	Quad Bus Transceiver (OC)
MC2906	Quad Bus Transceiver Parity (OC)
MC2907	Quad Bus Transceiver Parity (OC)
MC2909	Microprogram Sequencer
MC2911	Microprogram Sequencer
MC2915A	Quad Bus Transceiver (TS)
MC2916A	Quad Bus Transceiver Parity
MC2917A	Quad Bus Transceiver Parity
MC2918	4-Bit Register

TTL MEMORIES

MCM93415/25	1024 X 1*	RAMS
MCM93L415	1024 X 1**	
MCM7620/21	512 X 4*	
MCM7640/41	512 X 8*	
MCM7642/43	1024 X 4*	PROMS
MCM7680/81	1024 X 8*	
MCM82707/08	1024 X 8*	

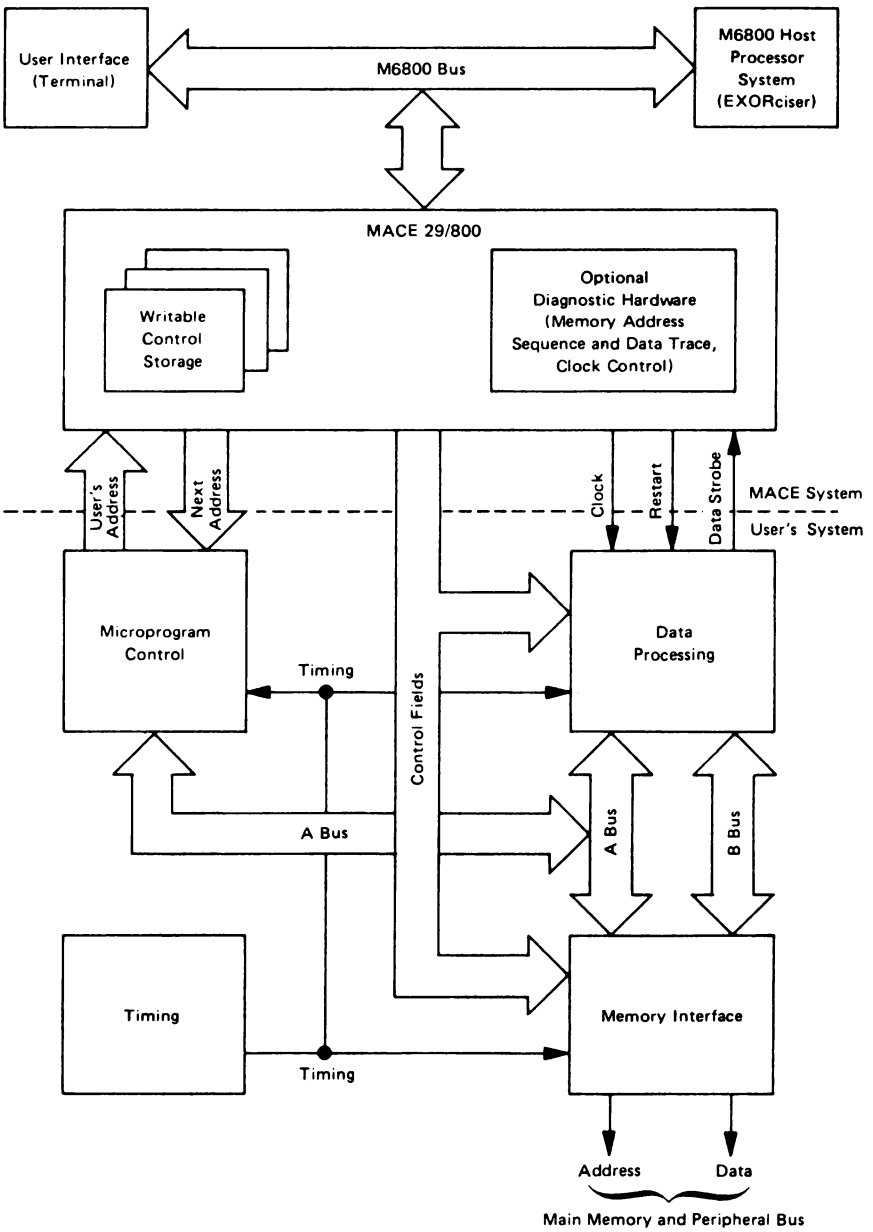
*Open Collector/Three-State Output
**Open Collector Output

(LSTTL Device Support: Over 150 Device Functions)

SYSTEMS SUPPORT PRODUCTS

Hardware	Software
EXORciser—System Development Tool	6800 Assembler, Editor
• I/O Modules	6800 Cross Assembler
• Memory Modules	6800 Simulator
User System Evaluator	6800 Macro Assembler
System Performance Monitor	6800 Linking Loader
Micromodules (OEM Hardware)	6800 BASIC Resident Interpreter
EXORdisk II Floppy Disk	6800 Fortran Compiler
EXORterm 100 CRT Terminal	6800 MPL Cross Compiler
EXORprint Printers	6800 MPL Resident Compiler
PROM Programmer	6800 COBOL Resident Interpreter
MACE 29/800	Disk Operating System
141000 CMOS Microprocessor Support Adapter	Micro Assembler
3870 Microprocessor Support Adapter	141000 Cross Assembler
	3870 Cross Assembler

FIGURE 1 – MICROPROGRAM DEVELOPMENT SYSTEM



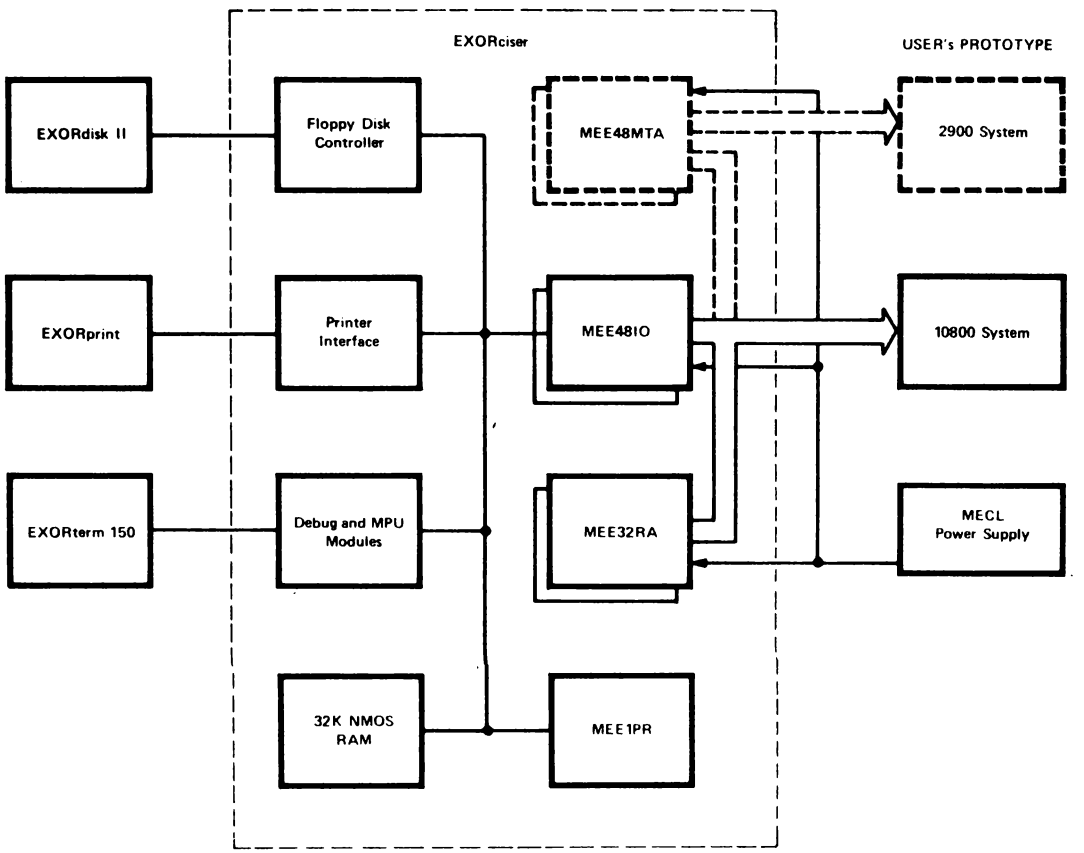
ORDERING INFORMATION

Part No.	Description
MEXMACE2	MACE 29/800 Development System, 220 V, 50 MHz, consisting of: • EXORciser Interface Module • Control Module • Writable Control Storage (WCS) RAM Modules (2K x 16,2 each) • Probe Buffer Module • Data Probe Modules (2 each) • Address Probe Module • 10-Card MACE Chassis With Power Supplz and Backplane • Microcode Assembler • System Executive
MEXMACEDP1	Data Probe Buffer
MEXMACERAM1	Writable Control Storage (WCS) RAM Module (2K x 16)

The EXOslice Family

The EXOslice family, working with the EXORciser, provides the user with a mean of developping 2900 and 10800 4-bit slice Microcomputer systems.

The EXOslice family includes high speed expandable 1K x 32 bit MECL RAM modules for microcode storage, 16-input/32-output MECL modules and MECL-TTL adapter. A MECL PROM Programmer allows programming of MECL MCM10149 256 x 4 PROM devices. The FAST software provides a mean of dumping or loading user's files (configuration descriptions, microprogram) to and from several source or media (keyboard, papertape, cassette, diskette) and offers several debugging features for the user's microprogram.



MOTOROLA

MEE4810

10800/2900 SUPPORT TOOLS

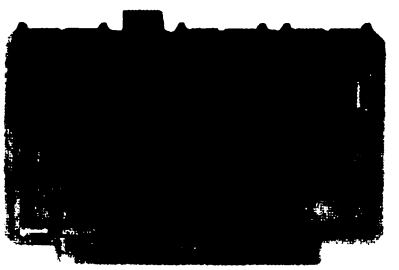
MECL I/O MODULE

16-INPUT/32-OUTPUT MECL MODULE

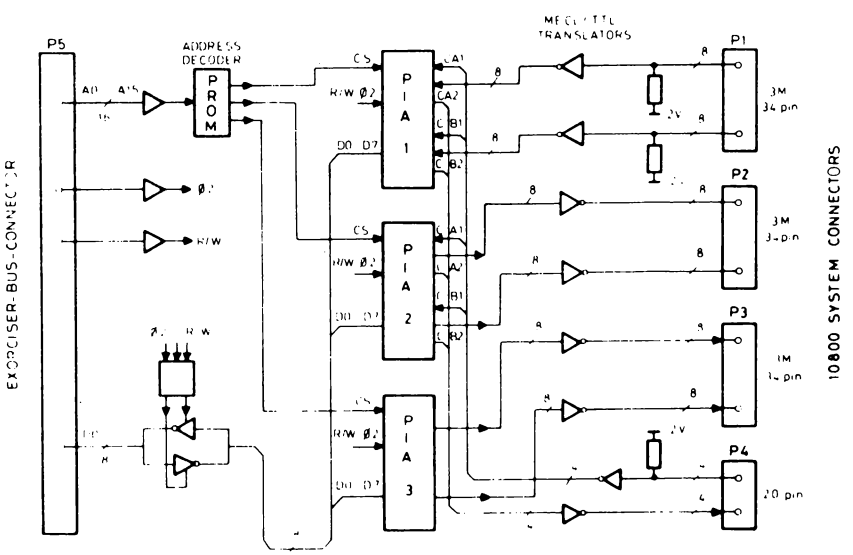
The MEE4810 input/output Module is specially designed to connect a MECL10800 system to a 10800/2900 Microprocessor Development system based on the EXORciser. In a typical configuration where the EXORciser simulates the microprogram PROM, the input-lines of the module receive the microprogram addresses and I-Bus informations, and the output-lines are used as micro-code output lines. This module plugs directly into the EXORciser and provides 16 input-lines and 32 output-lines with normalized MECL10K input/output features.

The input-lines have 110 Ω termination resistors. The output-lines can be OR-wired on a bus as they are open emitters. Termination resistors should be incorporated in the 10800 system.

- 16 MECL level input lines
- 32 MECL level output lines
- OR-wired capability for the output lines
- PROM address decoding
- Expandable up to 5 modules (80 input/160 output lines).
- Power requirements: + 5 Vdc 1 A
  − 5.2 Vdc 650 mA
  − 2 Vdc 50 mA
- Dimensions (WxHxT): 248 x 165 x 1 6 mm (9.75" x 6.5" x 0.062").



BLOCK DIAGRAM



MOTOROLA

MEE48MTA

10800/2900 SUPPORT TOOLS

MECL/TTL ADAPTER MODULE

MECL/TTL ADAPTER MODULE

The MEE48MTA MECL/TTL ADAPTER MODULE provides the user with the possibility to develop TTL 2900 bit slice system applications using the full power of the MECL support tools such as the 16 input/32 output modules, the 1K x 32 bit MECL RAM modules and the FAST software.

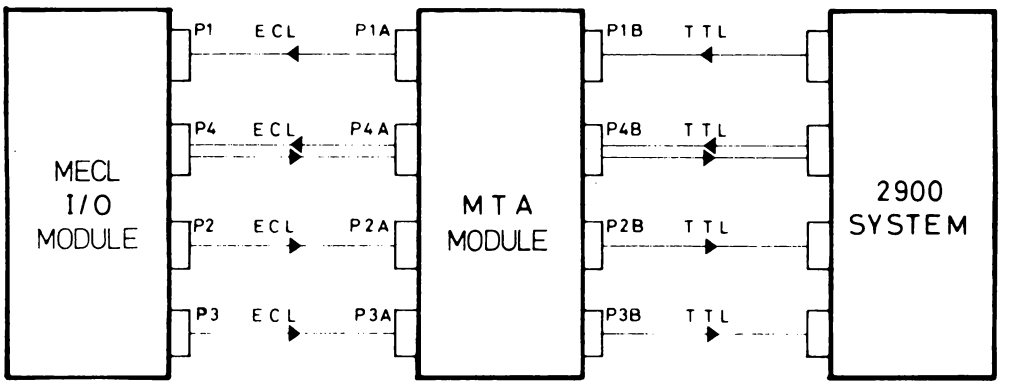
The MECL/TTL ADAPTER MODULE is a 20 lines TTL to MECL and 36 lines MECL to TTL translator specially designed for interfacing the MEE48IO MECL Input/Output Module to a TTL 2900 prototype system. The MECL lines DO 0 to DO 31 and the corresponding control lines are terminated by 100 ohm SIP resistors.

Specifications:

Connectors P1A to P4A signals		ECL voltage compatible
Connectors P1B to P4B signals		TTL voltage compatible
Power requirements		+5 Vdc, 370 mA
		- 5.2 Vdc, 570 mA
		- 2 Vdc, 120 mA
Dimensions	(W X H X T)	248 x 165 x 20 mm (9.75" x 6.5" x 0.79").

MTA

INTERCONNECTIONS



MOTOROLA

MEE32RA

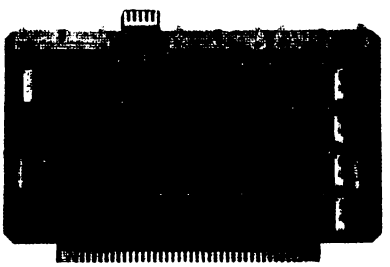
1K x 32-BIT MECL RAM MODULE

The MEE32RA high speed MECL RAM module is a 1K x 32-bits RAM board especially designed for microinstruction storage in a 10800/2900 Microprocessors Development System based on the EXORciser.
Once the microprogram has been partially debugged at reduced speed, it is transfered into the high speed MECL RAM module, allowing then real time execution and break points insertions under control of the EXORciser.
The module contains 32 MCM10146 MECL RAM devices, representing a total capacity of 1K word of 32 bits each. It is expendable to provide wider words (multiple of 32 bits) by using more modules sharing the same Address Bus. It is also expendable to provide larger capacity (multiple of 1024 words) by using more modules sharing the same Data Bus. An external address decoding circuit is then to be used to select the appropriate module through the CE line.

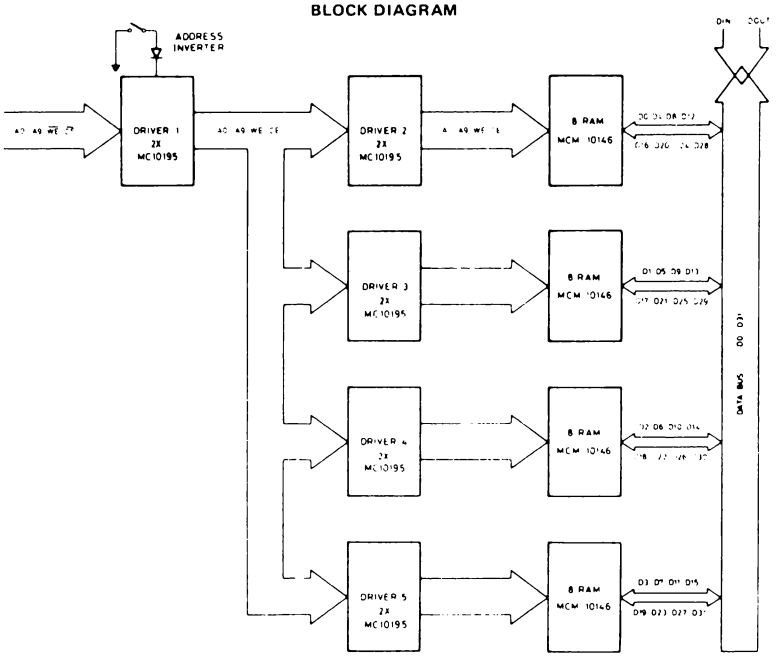
- 1024 words of 32 bits
- Fast access time: 28 ns (typical)
- All inputs/outputs MECL 10K compatible
- OR-wired capability on the Data Bus
- Switchable address lines complementing (positive or negative logic)
- Expandable memory capacity and word size
- Allows real time execution of microprogram
- Allows dynamic microprogramming
- Power supply requirement: −5.2 Vdc 3.5 A
  −2 Vdc 0.3 A
- Dimensions (WxHxT): 248 x 165 x 1.6 mm (9.75" x 6.5" x 0.062").

10800/2900 SUPPORT TOOLS

MECL
32K RAM MODULE



BLOCK DIAGRAM



MOTOROLA

MEE1PR

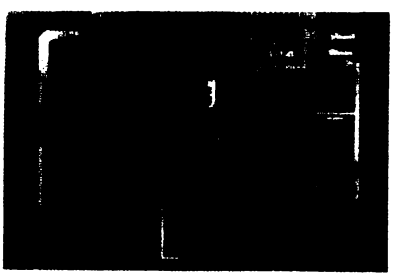
10800/2900 SUPPORT TOOLS

MECL
PROM PROGRAMMER

MECL PROM PROGRAMMER MODULE

The MEE1PR PROM Programmer Module provides the EXORciser with the capability of programming MECL MCM10149 256 x 4 PROM devices. This module plugs directly into the EXORciser.
The MECL PROM Programmer Module, with its software, enables the user to program a device, verify the data in the device and transfer data from the device to the EXORciser's RAM memory. The programming software is available on cassette, paper tape, or diskette (EDOS and MDOS).

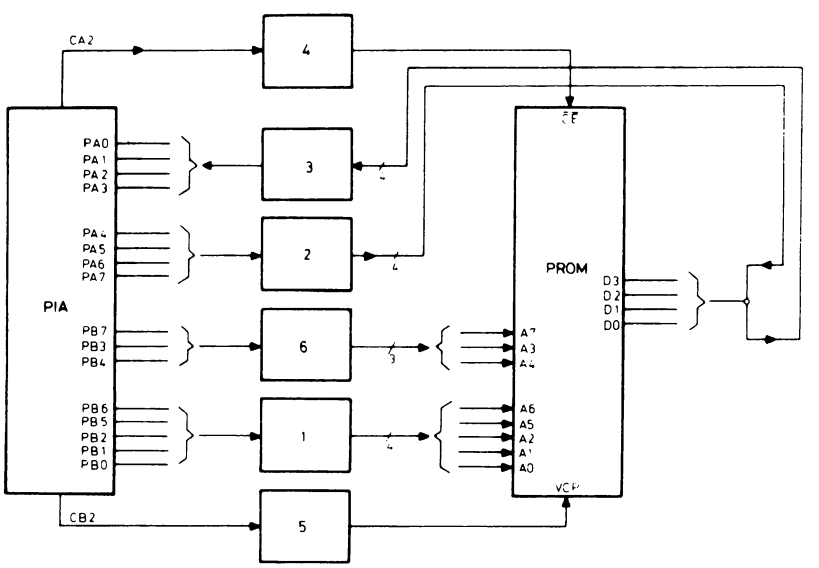
- Compatible with the MCM10149 256 x 4 MECL PROM
- PROM pattern loading: keyboard, paper-tape, diskette, master PROM
- Allows direct programming from microprogram format contained in RAM
- Positive and negative pattern capability
- Verify and dump function
- Uses the +5 V± 12 V EXORciser power supply
  + 5 Vdc 700 mA
  + 12 Vdc 525 mA (programming pulse)
  − 12 Vdc 350 mA
- Dimensions (WxHxT): 248 x 192 x 1.6mm (9.75" x 7.56" x 0.062").



ORDERING INFORMATION

Device Type	Description
MEE1PRA	MECL PROM Programmer with software on cassette
MEE1PRB	MECL PROM Programmer with software on paper-tape
MEE1PRD	MECL PROM Programmer with software on EDOS diskette
MEE1PRM	MECL PROM Programmer with software on MDOS diskette

BLOCK DIAGRAM



MOTOROLA

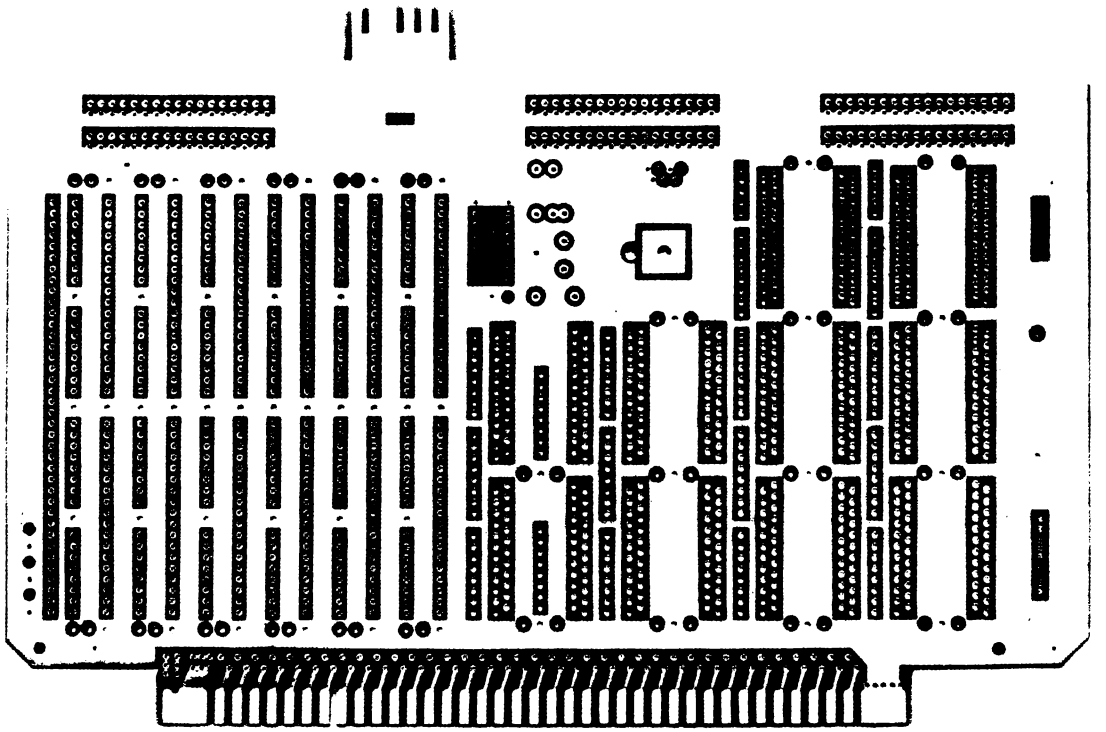
MEE1WW

UNIVERSAL MECL WIRE-WRAP BOARD

The MEE1WW Wire-Wrap Module provides the user with means to develop MECL slice system prototypes in wire-wrap technology. Provision is made on the card to implement 48-pin devices (up to 10), 24-pin and 16-pin devices, 6 x 34-pin flatt-ribbon connectors, 1 power regulator MC7902 or 1 clock generator based around an MC10116 or an MC10802.
A special connector is provided on the board for the MECL power supply (−5.2 Vdc and −2 Vdc).
Dimensions (WxHxT): 248 x 156 x 1.6 mm (9.75" x 6.5" x 0.062").

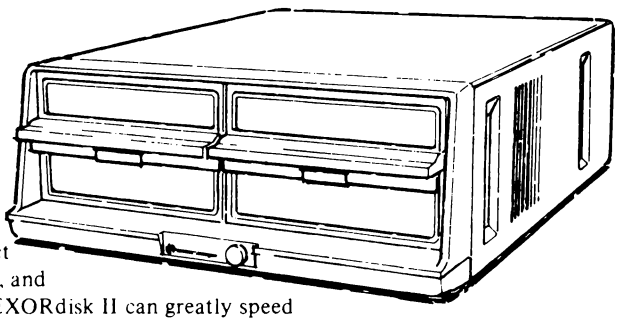
10800/2900 SUPPORT TOOLS

UNIVERSAL MECL WIRE-WRAP CARD



MOTOROLA MICROSYSTEMS

M68SFD
EXORdisk II



EXORdisk II is a dual drive floppy disk system which offers more than one half million bytes of on line storage and is designed for direct use with Motorola's EXORciser I, EXORciser II, and EXORterm 200 Development Systems. Use of EXORdisk II can greatly speed the task of developing software for microprocessor-based systems by reducing program load and peripheral access times.

The EXORdisk II hardware package consists of an EXORciser-resident controller module, an interconnecting cable assembly and the floppy disk drive unit which houses the dual side-by-side drives, power supply and associated electronics in an attractive tabletop cabinet.

The EXORdisk II disk operating system -- MDOS -- is a powerful program that offers an extensive selection of disk commands and utilities to the user. A simple set of disk primitives in firmware is also included in EXORdisk II.

Specifications

Diskette Format:

2,050,048	Bits/Diskette (soft sector)
256,256	Bytes/Diskette (soft sector)
77	Tracks/Diskette
26	Sectors/Track
128	Bytes/Sector

Performance:

Rotational Speed – 360 RPM
Track-to-Track Access Time – 10 ms (max)
Head Load – 40 ms (max)
Sector Read/Write Time – 2.4 ms (nom)
Average Latency Time -- 83.3 ms

Power Requirements:

230 Vac, 50 Hz, 350 Watts

Physical Characteristics (2-drive system):

L x H x D – 17.75 x 6.96 x 23.5 inches
Weight – 48 pounds

Electrical:

All signals are TTL, Low-True
16 Output Lines, 8 Input Lines

Options and Ordering Information

Part Number	Description
M68SFD2000	EXORdisk II Floppy Disk System, 220 V, 50 Hz –(Use with EXORciser I and EXORterm 200)– consists of the Floppy Disk Dual Drive Unit, the Controller Module and Cable Assembly, and a diskette containing the MDOS Operating System, the Co-Resident Editor/Assembler, the Relocatable Macro-Assembler and Linking Loader.
M68SFD2002	EXORdisk II Floppy Disk System, 220 V, 50 Hz as above but for use with EXORciser II and EXORterm 220.
M68SFDC	Floppy Disk Controller Module (1 MHz)
M68SFDC2	Floppy Disk Controller Module (2 MHz)
M68SFDRK2	EXORdisk II Rack Mounting Kit
M68SFDU2000	Floppy Disk Dual Drive Unit
M68SMDOS100	Diskette containing the MDOS Operating System, the Co-Resident Editor/Assembler, the MC6800/MC6801 Relocatable Macro-Assembler and Linking Loader.
M6833	Blank Diskette

Additional Support Products Available for Use with EXORdisk II

M6800EDITORM	Expanded Editor, operable in Scroll mode or CRT mode
M68FTNR012M	EXORciser/EXORterm Resident Relocatable FORTRAN Compiler and Linking Loader
M68BASR010M	EXORciser/EXORterm Resident BASIC Interpreter
M68MPLR010M	EXORciser/EXORterm Resident MPL Compiler
M68COBOL010M	EXORciser/EXORterm Resident ANS COBOL Compiler
M68MODOS010	MODOS Operating System
MEX68PP3M	PROM Programmer III (All EXORcisers)
MEX14100M	MC141000/1200 Development System
MEX3870M	MC3870 Development System
MEXMACE	2900/10800 Development System

EXORdisk II MDOS Commands

Name	Command
BACKUP	Duplicate disk or perform selected file reorganization
BINEX	Convert binary memory-image file to EXbug loadable file
BLOKEDIT	Copy selected lines from text files to a new file
CHAIN	Place console input under control of a file
COPY	Copy files from disk to device, device to disk, or disk to disk
DEL	Delete file name from directory and free corresponding disk space
DIR	Search directory for and display prescribed file names
DOSGEN	Write basis for support of MDOS file structure into any disk
DUMP	Display total content of any physical sector
ECHO	Duplicate console I/O on printer (EXORciser II only)
EMCOPY	Restructure EDOS 2.n file to MDOS basis
EXBIN	Convert EXbug-loadable file to binary memory-image file
FORMAT	Rewrite soft sector addressing information
FREE	Display number of available directory entries and number of available disk sectors
LIST	Print any MDOS file with an ASCII attribute
LOAD	Load any memory-image file into memory. Supports EXORciser II dual map
MERGE	Concatenate files
NAME	Change directory attributes of file (name, suffix, etc.)
PATCH	Modify memory-image file
REPAIR	Examine disk-resident system tables and allow correction
ROLLOUT	Copy memory to disk.

EXORdisk II Controller Firmware Functions

Disk Functions

- Load MDOS from disk
- Initialize disk, PIA, SSDA
- Check error status and printer error
- Display controller return status
- Read single/muliple sectors
- Read single/multiple sectors for CRC only
- Perform write/read test
- Position head to track zero
- Position head to track n
- Perform write test
- Write deleted data mark to single/multiple sectors
- Write single/multiple sectors; read back for CRC check
- Write single/multiple sectors

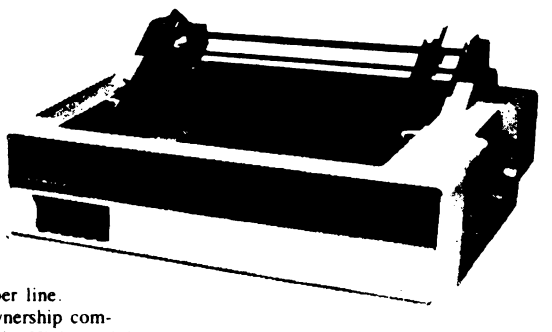
Printer Functions

- Initialize printer PIA
- Print character
- Print string, CR/LF
- Print string

MOTOROLA

MICROSYSTEMS

M68SP702
702 Printer



The Motorola Microsystems Model 702 Printer is a 132-column character impact serial printer with a bidirectional logic seeking print head which produces a 7 x 7 dot matrix pattern of crisp, clean print. The 64 ASCII character set is standard. A head speed of 120 characters per second, combined with the bidirectional logic seeking feature, gives a throughput of up to 65 lines per minute at 80 characters per line. Exceptional reliability, high throughput, and low cost of ownership combine to make the 702 one of the most versatile printers available. High reliability is achieved by few moving parts and an uncomplicated modular construction incorporating state-of-the-art microprocessor electronics for control. It comes equipped with a rear tractor feed capable of printing an original, plus five copies with excellent print quality, and also has a paper out sensor.

The complete printer package includes the Printer and the Printer Interface Cable Assembly, as well as the MEX68PI Printer Interface I/O Module, which normally is housed in a Development System chassis or other external system to interface with the printer.

- Prints original plus five copies
- 8 ips paper slew
- Stepper motor drive
- Table top
- Tractor feed
- Ballistic head
- Low cost of ownership
- Modular construction
- Bidirectional logic seeking printing
- Microprocessor electronics
- Ribbon cartridge
- Excellent print quality
- Character elongation

Specifications

Print Performance — Minimum Throughput:

Print Speed (cps)	Max. Print Width	10 Char Per Line (lpm)	80 Char Per Line (lpm)	132 Char Per Line (lpm)
120	13.2" (335 mm)	225	65	45

Characters:
7 x 7 dot matrix, 64 standard ASCII

Format:
10 characters per inch horizontal
6 lines per inch vertical
Elongated (double width) characters software selectable

Forms Handling:
Tractor feed, for rear feed forms
8 ips slew
Useable paper 4" (102 mm) to 17.3" (439 mm) width
Paper out sensor
Maximum width for L/R justification 15.75" (399 mm)
Paper tension adjustment

Ribbon System:
Ribbon cartridge
Continuous ribbon 9/16" (14 mm) wide, 10 yards (9.1 meters) long
Mobius loop allows printing on upper and lower portion on alternate passes

Panel Indicators:
Power ON — Indicates AC power is applied to printer
Select — Indicates printer can receive data
Alert — Indicates operator-correctable error condition

Operator Controls:

Select/deselect	Power ON/OFF
Forms thickness	Single line feed
Top of form	Paper empty override
Horizontal forms positioning	Self-test
Vertical forms positioning	

Internal Controls:
Electronic top of form — allows paper to space to top of form when command is received
Preset for 11" (279 mm) or 12" (305 mm) forms

Data Input:
7- or 8-bit ASCII parallel; microprocessor electronics; TTL levels with strobe
Acknowledge pulse indicates that data was received

Electrical Requirements:
50/60 Hz, 115/230 Vac

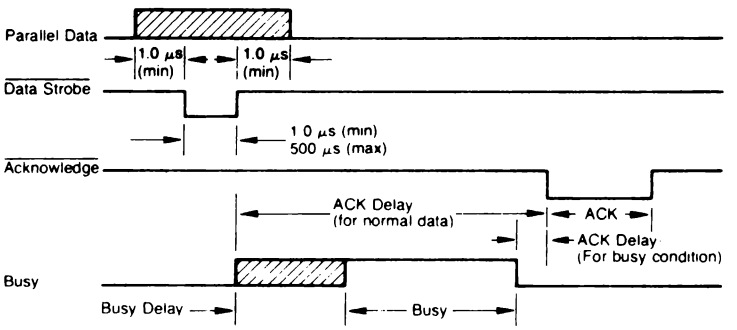
Physical Dimension:
Weight 60 lbs. (27 kg)
Width 24.5" (622 mm)
Height 8" (203 mm)
Depth 18" (457 mm)

Temperature:
Operating 40° to 100° F (4.4° to 37.7° C)
Storage -40° to 160° F (-40° to 71.1° C)

Humidity:
Operating 20% to 90% (No Condensation)
Storage: 5% to 95% (No Condensation)

Specifications (contd.)

INTERFACE TIMING



		702
Normal Data Input Timing	ACK Delay ACK	2.5-10 μs 3.5-4.5 μs
Busy Condition Timing	Busy Delay ACK Delay ACK Busy Duration Line Feed Vertical Tab (1-in.) Form Feed (11-in.) Delete Bell Select* Deselect Print Command Return Time (no busy)	0-1.5 μs 0-10 μs 3.5-4.5 μs 18-25 ms 70-80 ms 725-755 ms 50-300 μs 0 50-300 μs Until Printer is selected 5.6 ms/char N.A.

No busy if inhibit prime on select option is used

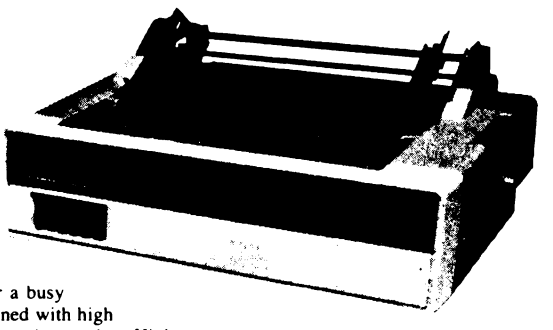
Options and Ordering Information

Part Number	Description
M68SP702A10	115V, 60 Hz option for 1 MHz Systems — consists of M68SP702B10 Printer MEX68P1 Printer Interface Module, and MEX68P1C Printer Interconnection Cable Assembly
M68SP702A20	230V, 50 Hz option for 1 MHz Systems Same as above except M68SP702B20 Printer
M68SP702C10	115V, 60 Hz option for 2 MHz Systems Same as M68SP702A10 except MEX68P12 Printer Interface Module
M68SP702C20	230V, 50Hz option for 2 MHz Systems Same as M68SP702A20 except MEX68P12 Printer Interface Module

MOTOROLA

MICROSYSTEMS

M68SP703
703 Printer



Motorola Microsystems Model 703 Printer represents the top of Microsystems' printer line. With 132 columns, 180 cps, bidirectional logic seeking, and dot matrix printing, the 703 is in a class approaching that of line printers. It provides high throughput rates from 70 to 280 lpm. The 703 is offered as a solution to business systems having high speed, high throughput requirements, as well as an ideal printer for a busy software development station. When this throughput is combined with high reliability and low cost of ownership, the 703 is an outstanding printer value. High reliability is achieved by few moving parts and an uncomplicated modular construction incorporating state-of-the-art microprocessor electronics for control. It comes equipped with a rear tractor feed capable of printing an original, plus five copies with excellent print quality, and also has a paper out sensor.

The complete printer package includes the Printer and the Printer Interface Cable Assembly, as well as the Printer Interface Module, which normally is housed in a Development System chassis or other external system to interface with the printer.

- Low cost of ownership
- Modular construction
- Bidirectional logic seeking printing
- Microprocessor electronics
- Ribbon cartridge
- Excellent print quality
- Character elongation
- Prints original plus five copies
- 15 ips paper slew
- Stepper motor drive
- Table top
- Tractor feed
- Ballistic head

Specifications

Print Performance — Minimum Throughput:

Print Speed (cps)	Max. Print Width	10 Char Per Line (lpm)	80 Char Per Line (lpm)	132 Char Per Line (lpm)
180	13.2" (335 mm)	280	90	70

Characters:
7 x 7 dot matrix, 64 standard ASCII

Format:
10 characters per inch horizontal
6 lines per inch vertical
Elongated (double width) characters software selectable

Forms Handling:
Tractor feed, for rear feed forms
15 ips slew
Useable paper 4" (102 mm) to 17.3" (439 mm) width
Paper out sensor
Maximum width for L/R justification 15.75" (399 mm)
Paper tension adjustment

Ribbon System:
Ribbon cartridge
Continuous ribbon 9/16" (14 mm) wide, 10 yards (9.1 meters) long
Mobius loop allows printing on upper and lower portion on alternate passes

Panel Indicators:
Power ON — Indicates AC power is applied to printer
Select — Indicates printer can receive data
Alert — Indicates operator-correctable error condition

Operator Controls:
Select/deselect
Forms thickness
Top of form
Horizontal forms positioning
Vertical forms positioning
Power ON/OFF
Single line feed
Paper empty override
Self-test

Internal Controls:
Electronic top of form allows paper to space to top of form when command is received
Preset for 11" (279 mm) or 11.7" (297 mm) forms

Data Input:
7- or 8-bit ASCII parallel; microprocessor electronics; TTL levels with strobe
Acknowledge pulse indicates that data was received

Electrical Requirements:
50/60 Hz, 115/230 Vac

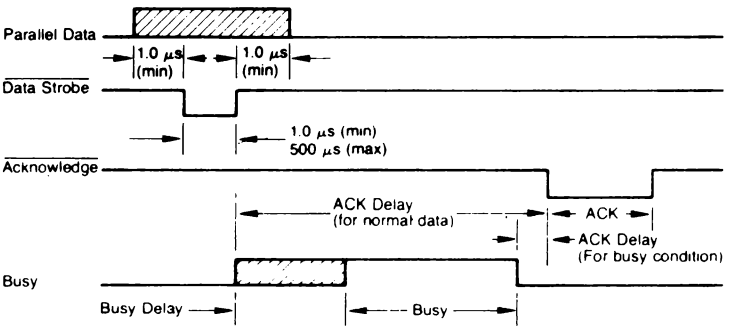
Physical Dimension:
Weight 60 lbs. (27 kg)
Width 24.5" (622 mm)
Height 8" (203 mm)
Depth 18" (457 mm)

Temperature:
Operating 40° to 100°F (4.4° to 37.7°C)
Storage -40° to 160°F (-40° to 71.1°C)

Humidity:
Operating 20% to 90% (No Condensation)
Storage: 5% to 95% (No Condensation)

Specifications (contd.)

INTERFACE TIMING



		703
Normal Data Input Timing	ACK Delay ACK	2.5-10 μs 3.5-4.5 μs
Busy Condition Timing	Busy Delay ACK Delay ACK Busy Duration Line Feed Vertical Tab (1-in.) Form Feed (11-in.) Delete Bell Select* Deselect Print Command Return Time (no busy)	0-1.5 μs 0-10 μs 3.5-4.5 μs 18-25 ms 70-80 ms 725-755 ms 50-300 μs 0 50-300 μs Until Printer is selected 5.6 ms/char N.A.

*No busy if inhibit prime on select option is used

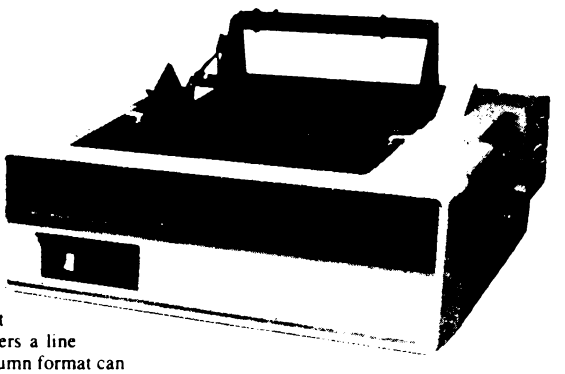
Options and Ordering Information

Part Number	Description
M68SP703A10	115V, 60 Hz option for 1 MHz Systems — consists of M68SP703B10 Printer MEX68PI Printer Interface Module, and MEX68PIC Printer Interconnection Cable Assembly
M68SP703A20	230V, 50 Hz option for 1 MHz Systems Same as above except M68SP703B20 Printer
M68SP703C10	115V, 60 Hz option for 2 MHz Systems Same as M68SP703A10 except MEX68PI2 Printer Interface Module
M68SP703C20	230V, 50 Hz option for 2 MHz Systems Same as M68SP703A20 except MEX68PI2 Printer Interface Module

MOTOROLA

MICROSYSTEMS

M68SP779
779 Printer



The Motorola Microsystems 779 Printer is a low-cost printer ideal for development systems where emphasis is on economy rather than speed. Low cost of ownership is accomplished by a low initial price and high reliability due to fewer moving parts and uncomplicated modular construction incorporating a single logic board with TTL logic. The 779 is a 5 x 7 serial dot matrix printer that prints 21 lines per minute at 80 characters a line (60 cps). Although it has an 80-column print image, 132-column format can be produced using the condensed printing feature. Condensed printing on eight-inch wide paper can result in substantial savings as does the use of standard TTY roll paper.

The complete printer package includes the Printer and the Printer Interface Cable Assembly, as well as the Printer Interface Module which normally is housed in a Development System chassis or other external system to interface with the printer.

- Low cost of ownership
- Modular construction
- Ribbon cartridge
- Excellent print quality
- Minimum of mechanical parts
- Pinch roll friction feed
- Ballistic print head
- Condensed print feature

Specifications

Print Performance:

Density (cpi)	Print Speed (cps)	Max. Print Width	10 Char Per Line (lpm)	80 Char Per Line (lpm)	132 Char Per Line (lpm)
10	60	8.0" (203 mm)	90	21	N/A
16.5	110	8.0" (203 mm)	130	36	21

Characters:
5 x 7 dot matrix
64 standard ASCII

Format:
10 to 16.5 characters per inch (operator adjustable)
6 lines per inch vertical

Forms Handling:
Pinch roll feed, 5.5 inches (140 mm) seconds slew rate
Roll paper to 9.8" (250 mm) core
Rear mounted roll paper holder
Column scale and tear bar

Ribbon System:
Ribbon cartridge
Continuous ribbon 9/16" (144 mm) wide, 10 yards (9.1 meters) long
Mobius loop allows printing on upper and lower portion on alternate passes

Panel Indicator:
Power ON — Indicates AC power is applied to printer

Operator Controls:
Print Switch
Forms Thickness
Horizontal forms positioning
Vertical forms positioning
Power ON/OFF
Print Density

Data Input:
7-bit ASCII parallel; TTL levels with strobe
Acknowledge pulse indicates that data was received

Electrical Requirements:
50/60 Hz, 115/230 Vac

Physical Dimensions:
Weight 45 lbs. (20 kg)
Width 19.5" (495 mm)
Height 8" (203 mm)
Depth 18" (457 mm)

Temperature:
Operating 40° to 100°F (4.4° to 37.7°C)
Storage -40° to 160°F (-40° to 71.1°C)

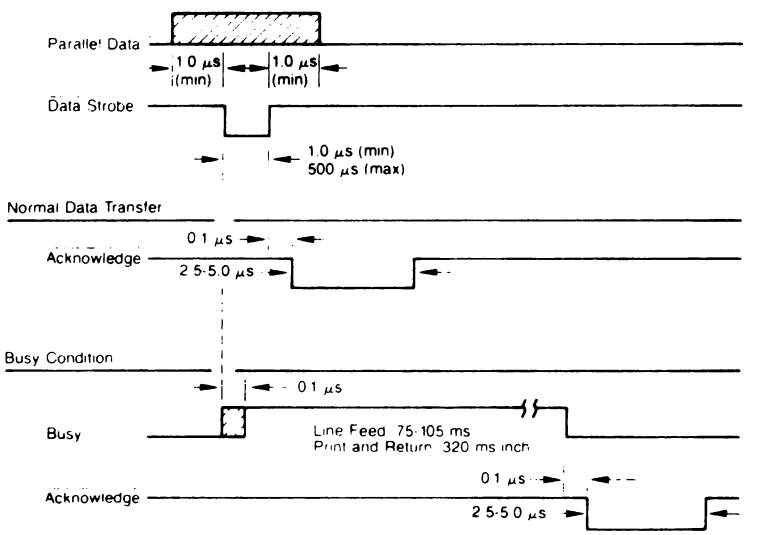
Humidity:
Operating 20% to 90% (No Condensation)
Storage: 5% to 95% (No Condensation)

Specifications (contd.)

INTERFACE PIN OUTS

Pin	Signal		
1	DATA STROBE	19	Twisted Pair Ground
2	DATA BIT 1	20	
3	DATA BIT 2	21	
4	DATA BIT 3	22	
5	DATA BIT 4	23	
6	DATA BIT 5	24	
7	DATA BIT 6	25	
8	DATA BIT 7	26	
9		27	
10	ACKNOWLEDGE	28	
11	BUSY	29	
12	PAPER OUT or PRINT OFF	30	
13	PRINTER SELECT	31	
14	GROUND	32	
15		33	GROUND
16	GROUND	34	
17	CHASSIS GROUND	35	
18	+5V	36	

INTERFACE TIMING



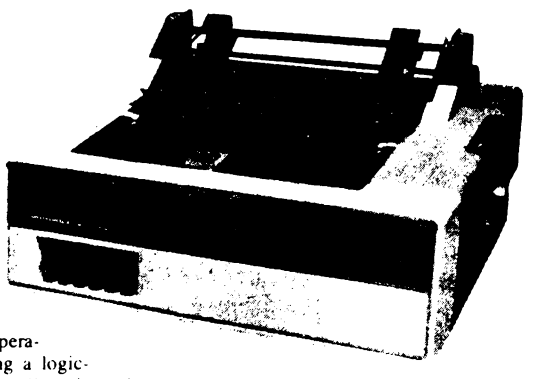
Options and Ordering Information

Part Number	Description
M68SP779A10	115V, 60 Hz option for 1 MHz Systems — consists of M68SP779B10 Printer MEX68PI Printer Interface Module, and MEX68PIC Printer Interconnection Cable Assembly
M68SP779A20	230V, 50 Hz option for 1 MHz Systems Same as above except M68SP779B20 Printer
M68SP779C10	115V, 60 Hz option for 2 MHz Systems Same as M68SP779A10 except MEX68PI2 Printer Interface Module
M68SP779C20	230V, 50 Hz option for 2 MHz Systems Same as M68SP779A20 except MEX68PI2 Printer Interface Module

MOTOROLA

MICROSYSTEMS

M68SP781
781 Printer



The Motorola Microsystems Model 781 Printer is an economic, 80-column character printer supplied in a stylish, low-profile cabinet. Its high throughput and low ownership cost make it ideal for software development and business applications. Cost of ownership is minimized by a low initial price and a design which combines an LSI-based modular concept with few-moving-parts construction to achieve near-maintenance-free operation. A maximum throughput of 120 lpm is achieved by using a logic-seeking, bidirectional print head that seeks the shortest path to the next line when printing successive lines of data. The Model 781 is a 5 x 7 serial dot matrix printer, and comes equipped with a rear tractor feed, capable of printing five-part paper, plus a paper out sensor.

The complete printer package includes the Printer and the Printer Interconnection Cable Assembly, as well as the Printer Interface Module, which is normally housed in a Development System chassis or other external system to interface that system with the printer.

- Minimum mechanical parts
- Table top
- Tractor feed
- Bidirectional logic seeking printing
- Ribbon cartridge
- Ballistic head
- Low cost of ownership
- Modular construction
- Custom LSI electronics
- Excellent print quality
- Character elongation
- Prints original, plus five copies

Specifications

Print Performance (Logic-Seeking and Bidirectional)

Print Speed (cps)	Max. Print Width	10 Char Per Line (lpm)	80 Char Per Line (lpm)
60	8.0 (203 mm)	120	43

Characters:
5 x 7 dot matrix, 64 standard ASCII

Format:
10 characters per inch horizontal
6 lines per inch vertical
Elongated (double width) characters software selectable

Forms Handling:
Tractor — For rear or bottom feed forms
Paper tension adjustment

Maximum Width	Maximum Width for L/R Justification
12.1" (307 mm)	10.2" (259 mm)

Ribbon System:
Ribbon cartridge
Continuous ribbon 9/16" (14 mm) wide, 10 yards (9.1 meters) long
Moblus loop allows printing on upper and lower portion on alternate passes

Panel Indicators:
Power ON — Indicates AC power is applied to printer
Select — Indicates printer can receive data
Alert — Indicates operator-correctable error condition

Operator Controls:
Select/deselect
Forms thickness
Horizontal forms positioning
Vertical forms positioning
Power ON/OFF

Data Input:
7- or 8-bit ASCII parallel; LSI electronics; TTL levels with strobe
Acknowledge pulse indicates that data was received

Electrical Requirements:
50/60 Hz; 115/230 Vac

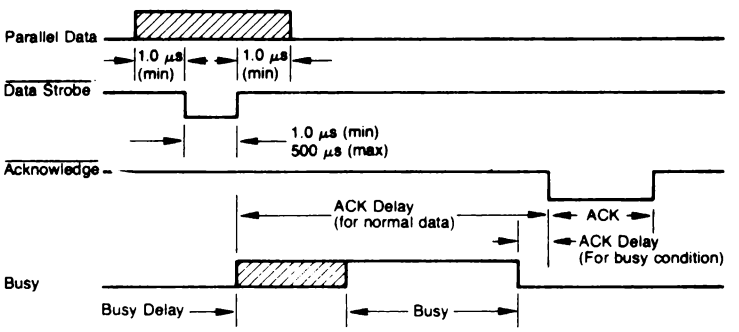
Physical Dimensions:
Weight 45 lbs. (20 kg)
Width 19.5" (495 mm)
Height 8" (203 mm)
Depth 18" (457 mm)

Temperature:
Operating 40° to 100°F (4.4° to 37.7°C)
Storage -40° to 160°F (-40° to 71.1°C)

Humidity:
Operating 20% to 90% (No Condensation)
Storage: 5% to 95% (No Condensation)

Specifications (contd.)

INTERFACE TIMING



		781
Normal Data Input Timing	ACK Delay ACK	2.5 -1.0μs 2.5-5.0 μs
Busy Condition Timing	Busy Delay ACK Delay ACK Busy Duration Line Feed Vertical Tab (1-in.) Form Feed (11-in.) Delete Bell Select* Deselect Print Command Return Time (no busy)	0-1.5 μs 0-10 μs 2.5-5.0 μs 75-105 ms 240-270 ms 2.07-2.11 sec. 100-400 μs 0 100-400 μs Until Printer is selected 16.7 ms/char N.A.

No busy if inhibit prime on select option is used

Options and Ordering Information

Part Number	Description
M68SP781A1A	115V, 60 Hz option for 1 MHz Systems — consists of M68SP781B10 Printer MEX68PI Printer Interface Module, and MEX68P1C Printer Interconnection Cable Assembly
M68SP781A2A	230V, 50 Hz option for 1 MHz Systems Same as above except M68SP781B20 Printer
M68SP781C1A	115V, 60 Hz option for 2 MHz Systems Same as M68SP781A1A except MEX68PI2 Printer Interface Module
M68SP781C2A	230V, 50 Hz option for 2 MHz Systems Same as M68SP781A2A except MEX68PI2 Printer Interface Module

MOTOROLA

M68MPR1

POLYVALENT DEVELOPMENT SYSTEM

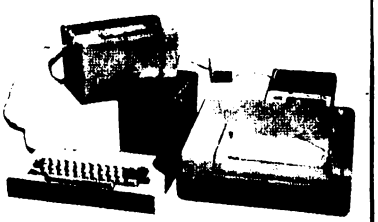
MEDIUM SPEED PRINTER

MEDIUM SPEED PRINTER

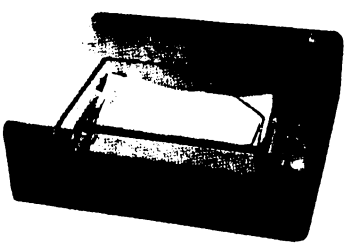
The M68MPR1 noiseless printer prints at 30 characters per second on metalized paper. It accepts 7 bit ASCII characters.

- 30 characters per second
- 80 characters per line
- noiseless (electro-sensitive paper)
- 64 ASCII characters
- 5 x 7 matrix
- Parallel interface
- Carriage Return and Line Feed ASCII codes

PDS



MPR



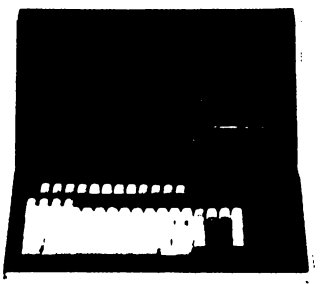
SPECIFICATIONS

Specification	Value
Line format	80 characters
Printing speed	30 characters per second
Character set	64 ASCII characters
Printing mechanism	5 x 7 matrix on electro sensitive paper
Carriage return	ASCII code
Line Feed	ASCII code
Interface	7-bit parallel clocked data, TTL compatible
Power Requirement	220 V 50 Hz, 50 VA
Operating temperature	5° to 45 °C
Dimensions	
Height	120 mm
Width	370 mm
Depth	330 mm
Weight	7 Kg

ACCESSORIES

M68MPP1	50 meter electro-sensitive Paper Roll
M68ICC1	Interconnection Cables Set

M68SXD
EXORterm 150



EXORterm 150 is a display terminal and console expressly personalized for use with the EXORciser, Motorola's M6800 Development Support System. EXORterm 150 uses the predominantly LSI components of the M6800 family to provide control of the display attributes, communications facility, terminal switch/indicator control, and keyboard inputs. Microexecutive firmware, in conjunction with control and application task firmware, coordinate the functions of EXORterm 150 in its EXORciser-oriented activity.

As an EXORciser display console, EXORterm 150 facilitates the exchange of data between the user and the system via a high quality video interface, keyboard entry, and a serial communications link using speeds up to 9600 bits per second. To further enhance the efficiency of the User/EXORciser interface, special keys have been encoded to invoke functions unique to the EXORciser in each of its three command levels: DOS, EXbug, and MAID. For user convenience, the functions presented by each of these 12 special keys and displays on the 23rd and 24th line of the screen. As the command level is changed, the function of the respective key changes and is displayed accordingly.

EXORterm 150 is housed in an attractive enclosure compatible in appearance with the full EXORciser line, providing a coordinated look suitable for office or laboratory.

Attention to the ergonomic considerations of glare reduction, keyboard "feel" and positioning, and control placement, make EXORterm 150 easy to use. Readily accessible controls include: power on/off, brightness, on/off line, upper case/lower case, Editing, Cursor and Page Mode Control Keys and automatic line feed/carriage return. Infrequently used switches and controls are located on the upper rear panel and include: baud rates selection, communications configuration switches, mode selection terminal reset, audible alarm adjustment, and RS-232/current loop connectors.

The basic EXORterm 150 may be connected for either RS-232 or 20/60 mA current loop operation. An extended communications option is available for use with 103- or 202-type modems. The cable supplied with this option permits supervisory channel operation with a 202-type modem.

Features

- **RS-232 and current loop interface**
- **Full 1920 character screen**
- **Easily readable 7 x 9 dot characters**
- **EXORciser integrated features**
- **Movable, detachable keyboard**
- **Editing Keys**
- **M6800-based**
- **Motorola design and manufacture**
- **LSI for maximum reliability**
- **Alternate glass TTY function**
- **Baud Rate selectable to 9600 BPS**

Specifications

Display:
- 12" diagonal, P4 phosphor with antiglare shield
- 24 lines, 80 characters per line
- 1920 character full display

Character Configuration:
- 9 x 12 dot matrix
- 7 x 9 character size

Character Set:
- ASCII-96 character subset with greek alphabet and six special graphics

Cursor:
- blinking inverted video, nondestructive, on 9 x 12 block
- Incremental and absolute positioning (addressable, readable)

Keyboard:
- Encoded, n-Key rollover
- 12 function keys
- LED mode indicators
- 62-key alphanumeric and control
- 12 edit and cursor control keys
- Full ASCII
- Typewriter layout
- Moveable and detachable
- All keys typamatic

Interface:
- Asynchronous
- RS-232 direct connect
- 20/60 mA current loop (source capable optional)
- HDX and FDX
- Selectable baud rates: 110, 150, 300, 600, 1200, 1800, 2400, 4800, or 9600
- Parity selection — odd, even, or none
- Word size — seven- or eight-bit
- Framing — one- or two-stop-bits
- 103/202 modem compatibility (optional)

Power Requirements:
- 95 to 230 Volts AC, 50/60 Hz
- Less than 200 watts

Physical Dimensions:
- Display — 12.5" H x 18.5" W x 20" D
- Keyboard — 2.7" H x 18.5" W x 8.4" D
- Overall — 12.5" H x 12.5" W x 29" D
- Weight — Less than 55 pounds

Environmental:
- Operating temperature — +10° to +40°C
- Nonoperating temperature — −20° to +75°C
- Altitude — Not to exceed 10,000 feet
- U.L. and C.S.A. approvable

Ordering Information

Part Number	Description
M68SXD10500	Basic EXORterm, EXORciser display console (220 V, 50 Hz option) – Consists of Video Display Enclosure, Keyboard and Connector Kit.
M68SXD(D)	EXORterm 100 User's Guide

chapter 2

software

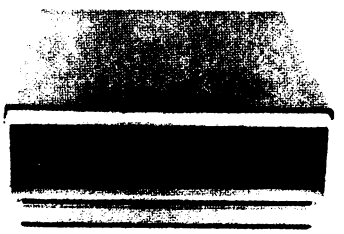
M6800 CO-RESIDENT SOFTWARE

M6800 CO-RESIDENT SOFTWARE

The optional M6800 Co-Resident Software, along with the M6800 EXORciser's EXbug Firmware, allows the EXORciser user to develope his system software in real-time with his peripheral devices incorporated into the system. This means that the user can prepare and assemble his software, and debug the software in its actual working environment. The M6800 Co-Resident Editor and Assembler are used to prepare and assemble the user's system software, while the EXORciser's EXbug Firmware is used to debug the system hardware as well as the software.

EXORciser CO-RESIDENT EDITOR and CO-RESIDENT ASSEMBLER

EXORciser



M6800 CO-RESIDENT EDITOR

The M6800 Co-Resident Editor may be used to create or modify alphanumeric text. In particular, the Editor gives the user an easy means to create and modify source programs for input into the M6800 Co-Resident Assembler. This interactive Editor offers character, line, and character string commands.

- Memory Sizing Capability
- Insert or Delete Lines
- Insert, Delete or Modify Character Strings
- Command Chaining
- Co-Resident with the M6800 Assembler or Stand Alone

M6800 CO-RESIDENT ASSEMBLER

The M6800 Co-Resident Assembler may be used with the M6800 EXORciser to translate M6800 Source Programs to machine language. This assembler is a two-pass assembler; that is, the Resident Assembler reads a user's program twice -- once to build a symbol table and a second time to produce the assembled output. Only pass two of the assembler is needed with programs having no forward references and with short programs. In the case of short programs, the forward references will be flagged with an error and the user is required to patch in the correct addresses after the symbol table is printed at the completion of the assembly. The Resident Assembler is compatible with the Cross Assemblers available from Motorola.

- Two Pass Assembler
- Limited One-Pass Capability
- Can Be Co-Resident with the M6800 Resident Editor or Stand Alone
- Compatible with Motorola's Cross Assemblers

EXbug FIRMWARE

The EXbug Firmware is an integral part of the M6800 EXORciser. This Firmware allows the user to load the M6800 Resident Assembler and Editor into the EXORciser and to verify that the Resident Software was correctly loaded, and to debug the user's system hardware and software. Also, this Firmware is used to print and/or punch the data stored in the EXORciser memory.

RESIDENT SOFTWARE REQUIREMENTS

- EXORciser
- 8K bytes of RAM minimum
- TTY (20 mA neutral loop current) or RS-232C data terminal with automatic reader/punch control

ORDERING INFORMATION

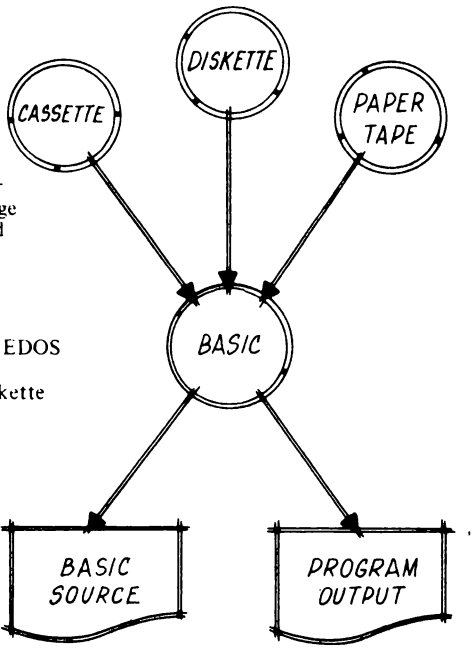
The user can select the media on which he wishes to receive his Resident Software. Table 1 shows the complete range of options, and the Part Number to be used when ordering. Contact your local Motorola Sales Office.

M6800 CO-RESIDENT SOFTWARE

TABLE 1 – M6800 CO-RESIDENT SOFTWARE OPTIONS

Part Number	Media	Description
M68XAE6813A	Cassette	
M68XAE6813B	Paper Tape	Co-Resident Editor/Assembler for EXORciser
M68XAE6813D	EDOS Diskette	
M6800EDITORM	*MDOS Diskette*	*Expanded Editor, operable in Scroll mode or CRT mode.*

M68BASR010 Resident BASIC Interpreter



The EXORciser-resident BASIC interpreter provides a new tool for problem solving to the M6800 Microcomputer family of parts. BASIC is a high-level programming language widely used for general purpose and certain business-related applications.

- Decimal arithmetic
- String variables and arrays
- Direct statement execution for Debug (calculator mode)
- Only 8K bytes of memory required for small programs on EDOS
- BASIC may reside on cassette, paper tape, or diskette
- User programs may reside on cassette, paper tape, or diskette
- Program output to printer or console
- Optional LET statement
- String functions and concatenation
- Dynamic file I/O on MDOS

System Configuration

The minimum system hardware configuration is:

- An EXORciser
- 8K bytes of memory on EDOS, 20 K bytes on MDOS
- An EXORciser compatible terminal

The minimum configuration may be expanded up to 65,536 bytes of memory and up to two disk drives providing over a half million bytes of disk storage. A disk is required for MDOS.

Language Features

Data Types
- Range (1.0E - 99 to 9.99999999E + 99) may be represented as either integer, decimal, or exponential.

Variable Names
- Single alphabetic character or single alphabetic character followed by a digit (0 through 9).
- String variables, single alphabetic character followed by a $.

Arithmetic and Logical Operators
- Exponential
- Negate
- Multiplication
- Division
- Addition
- Subtraction
- Relational operators

Sequence Control Statements
- GOTO
- ON expression GOTO statement n, (m, . . .,1)
- ON expression GOSUB statement n, (m, . . .,1)
- IF relative
- FOR
- NEXT
- STOP
- END

I/O Statements
- INPUT
- READ
- DATA
- PRINT
- RESTORE

Specification Statements
- DIM dimension variables and strings

Remark Statements
- REM

Optional Statements
- LET

MDOS Data File I/O
- OPEN
- CLOSE
- INPUT
- PRINT
- RESTORE

BASIC Commands

- LIST - display source
- RUN - execute program
- CONT - continue after stop or break
- NEW - define new program
- SAVE - save current program (tape or diskette only)
- LOAD - load new program (tape only)
- APPEND - add to program from tape (tape only)
- PATCH - patch memory from MAID
- TRACE ON - prints line number as it is executed
- TRACE OFF - turns off trace
- LINE LENGTH - define maximum print line length
- DIGITS - establishes the number of digits to right of decimal point
- POKE - sets absolute memory address

Subprograms

- DEF - define user function
- RETURN - return from subroutine
- GOSUB - go to subroutine

Intrinsic functions

- TAB - tab on print
- RND - random number
- INT - integer number
- ABS - absolute value
- SGN - sign of argument
- POS - position of printhead
- LEN - number of characters in string
- ASC - decimal value of any ASCII character
- CHR$ - string value of ASCII character
- STR$ - ASCII string value to numeric constant
- VAL - numeric constant equivalent to ASCII value
- LEFT$ - returns left-most string of characters
- RIGHT$ - returns right-most string of characters
- MID$ - returns middle string of characters
- PEEK - returns decimal memory value
- SIN - sine
- COS - cosine
- TAN - tangent
- ATAN - arc tangent
- LOG - natural logarithm
- EXP - inverse of LOG
- SQR - square root

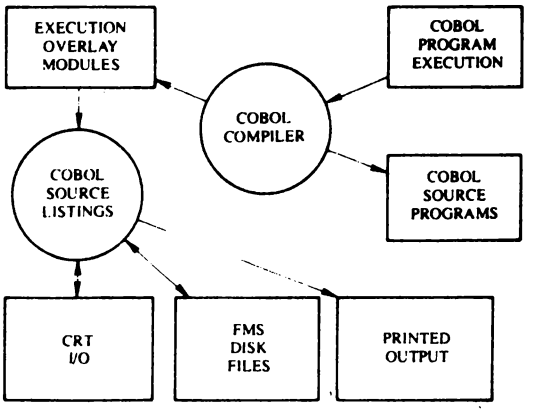
ORDERING INFORMATION

Option	Media	Part Number
1	Cassette	M68BASR010A
2	Paper Tape	M68BASR010B
3	Floppy Disk (EDOS)	M68BASR010D
4	Floppy Disk (MDOS)	M68BASR010M

M68COBOL010M Resident ANS COBOL Compiler

For sophisticated applications, Motorola's M6800 ANS COBOL Compiler adds a new dimension to Motorola's support for the M6800 family of products. COBOL is an industry-standard, high-level programming language, and is widely used for, but not limited to, business applications. COBOL is favored by many users because of ease of use, high degree of transferability, and self-documenting characteristics. M6800 ANS COBOL is a complete microcomputer implementation of COBOL, and includes many additional features beyond the level one ANS standard. In addition to the many higher level features, the following modules are supported.

- Nucleus
- Table handling
- Sequential access
- Random access
- Library



Performance Features

- Compile/execute on same system
- 500 lines per minute compile
- COPY statement included
- 30 character names
- Three-dimensional arrays
- CRT display/edit features:
  - Cursor control
  - Auto screen format
  - Input edit capability
  - Printer forms control
- On-line program editing
- Statement trace
- File management:
  - Sequential
  - Index sequential
  - Multiple files
  - Add, delete, update
  - Partial key retrieval
  - File restructure
  - File backup

System Configurations

The minimum system hardware configuration is:

- **An EXORterm 100 and EXORciser or an EXORterm 200**
- **An EXORdisk II**
- **32K bytes of memory**

Language Features

Data Types:
- Integer and fractional decimal
- Packed decimal
- Character strings to 4K bytes
- 18 edit specifications
- Hexadecimal constants
- Figurative constants
- ALL literal

Data Table Handling Statements:
- MOVE
- INSPECT
- SET
- SEARCH

Arithmetic Operators:
- Add
- Subtract
- Multiply
- Divide
- Compute verb
- ROUNDED option
- SIZE ERROR option
- Edited GIVING option

Input/Output Statements:
- START . . . KEY (=) . . .
- READ . . . INTO
- WRITE . . . FROM
- WRITE . . . BEFORE/AFTER LINE/PAGE
- DELETE
- REWRITE
- OPEN
- CLOSE
- ACCEPT
- DISPLAY
- INVALID KEY option
- AT END option

Sequence Control Statements:
- GO TO
- GO TO . . . DEPENDING ON
- Nested IF . . . ELSE . . .
- PERFORM . . . THRU . . .
- PERFORM . . . UNTIL . . . VARYING
- STOP
- EXIT

Conditional Operations:
- LESS, EQUAL, GREATER
- NOT, AND, OR
- POSITIVE, NEGATIVE, ZERO
- ALPHABETIC, NUMERIC

Ordering Information

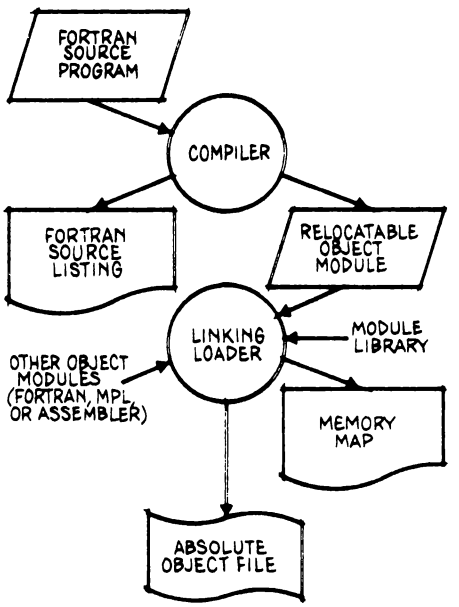
Part Number	Description
M68COBOL010M	Resident ANS COBOL Compiler on MDOS diskette.
M68COBO(D)	M6800 Resident COBOL Operations Reference Manual
M68COB(D)	M6800 Resident COBOL Language Reference Manual

MOTOROLA

M68FTNR012 Resident FORTRAN Compiler

The EXORciser-resident FORTRAN Compiler provides a new dimension to Motorola's support for the M6800 Microcomputer family of parts as a problem solving and development tool. FORTRAN is a high-level programming language widely used for scientific and engineering problem solving, with features also useful for certain business-related applications. The Resident FORTRAN is a subset of the ANSI standard for FORTRAN IV.

- Relocatable object output file compatible with the M6800 Linking Loader.
- Source and error message output to a printer or the terminal.
- FORTRAN library containing mathematical subroutines and run time I/O routines.
- Free field source input.
- Statement continuation.



System Configuration

The minimum system hardware configuration is:

- An EXORciser
- 24K bytes of memory (MDOS), 16K (EDOS)
- An EXORdisk (requires one floppy disk driver)
- An EXORciser-compatible terminal

The minimum configuration may be expanded up to 65,536 bytes of memory.

SOFTWARE OPTIONS

Option	Media	Part Number
D	Floppy Disk - EDOS	M68FTNR012D
M	Floppy Disk - MDOS	M68FTNR012M

Language Features

Data Types
- Two byte signed integer, maximum magnitude 32,767.
- Four byte real, magnitude 10^{-78} through 10^{75}.
- Literal, one byte character.

Variable Names
- One through six alphanumeric characters (first character must be A-Z).
- Implicit type declaration according to first character. I through N integer, A through H, O through Z real.

Arithmetic and Logical Operators
- Exponential
- Multiplication
- Division
- Addition
- Subtraction
- Relational operators
- IAND - logical AND
- IOR - logical OR
- IEOR - logical EOR
- ISHFT - 16-bit left/right shift

Sequence Control Statements
- Unconditional GOTO
- Computed GOTO
- Arithmetic IF
- Logical IF
- DO statement
- CONTINUE
- STOP
- END

I/O Statements
- Formatted READ from disk or terminal
- Formatted WRITE to disk or terminal
- Formatted PRINT to terminal
- Free format READ
- REWIND
- FORMAT conversions
  - I - conversions
  - E - conversions
  - F - conversions
  - A - conversions
  - Literal fields
  - Character positioning specifications
  - Group specifications

Specification Statements
- DATA initialization
- DIMENSION, three dimensions maximum
- Blank COMMON

Subprograms
- FUNCTION
- SUBROUTINE
- RETURN
- CALL

Intrinsic Functions/Subroutines
- SQRT - square root
- EXP - exponent base e
- SIN - sine
- COS - cosine
- ATAN - arctangent
- ALOG - natural logarithm
- ABS - absolute value
- POWER - computes a power
- OPENF - disk file open
- CLOSEF - disk file close

M68MASR010 Resident Macro Assembler and Linking Loader

The Resident Macro Assembler and Linking Loader extend the powerful software development capabilities of the EXORciser. The Macro Assembler supports Motorola's 6800, 6801 and 6802 microprocessors with a complete set of assembler features including macros, conditional assembly, relocation and linking. The Linking Loader combines relocatable object modules to produce an absolute object image. Operation of the Macro Assembler and Linking Loader are shown in the diagram.

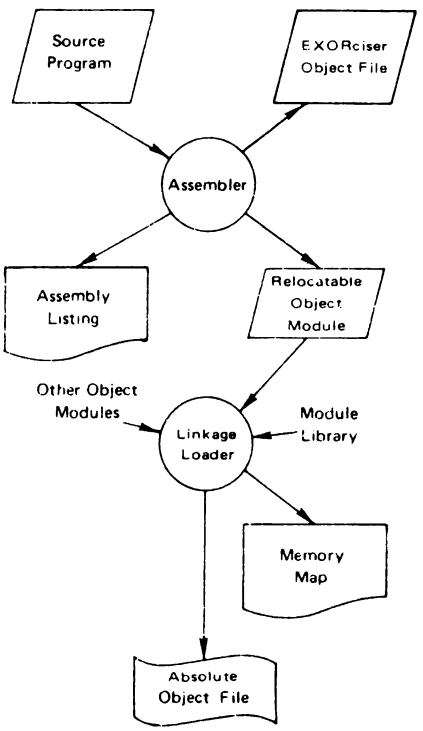
Macros
Macros are used to assign a name to a "template" sequence of assembly-language instructions. Subsequent use of the macro name causes that instruction sequence to be inserted into the assembler input stream. Arguments supplied with a macro call are inserted into specified locations in the template.

Conditional Assembly
Conditional assembly may be used to select or omit optional source statements for assembly.

Relocation
Relocation allows the assignment of absolute memory addresses to a program at linkage time rather than at assembly time. Programs assembled by the Macro Assembler can be loaded anywhere in memory by the Linking Loader.

Linking
Linking allows intermodule references to be resolved at linkage time rather than requiring absolute address assignment at assembly time. As relocatable programs are loaded by the Linking Loader, labels are assigned absolute addresses, and references to such labels in other program modules can be satisfied.

OPERATION OF MACRO ASSEMBLER/LINKING LOADER



Macro Assembler Features

Upward compatible with standard Resident Assembler with the following enhancement:

Microprocessor Supported
- 6800/6802
- 6801

Output
- Absolute object — EXORciser loadable format
- Relocatable object — Linking Loader (object module)

Program Sections
- Absolute — non-relocatable
- Base — directly addressable (0-255)
- Blank Common — uninitialized common
- Data — data section (external addressing)
- Program — instruction section
- Named Common — common sections included within one of the above

Linking
- External definitions
- External references

Macros
- Up to 36 arguments
- Strict character substitution for arguments
- Assembler generated symbols
- Up to 8 levels of nesting

Conditional Assembly
- String/expression tests
- Up to 8 levels of nesting

Other
- Symbol cross reference table
- Listing line width control
- Title on each page of listing
- SET — symbol redefintion
- BSZ — block storage — initially zero
- Expression evaluation — parenthesized expressions

EXORciser is a trademark of Motorola Inc.

Linking Loader Features

- Relocation of object modules
- Linking of object modules
- Two output modes
  - EXORciser Load Format
  - MDOS Load Format
- Memory load map
- Map of external symbols
- Undefined symbol list
- Flexible I/O device assignment
  - Disk
  - Console
  - Line printer

ORDERING INFORMATION

Option	Media	Part Number
A	Cassette	M68MASR010A
B	Paper Tape	M68MASR010B
D*	EDOS Diskette	M68MASR010D
M**	MDOS Diskette	M68SMDOS100

* 6801 Instruction Set not supported.

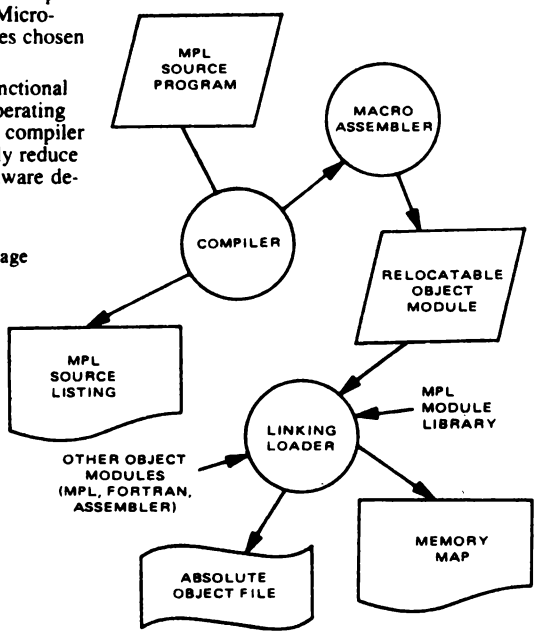
** Included in EXORdisk

M68MPLR010M Resident MPL Compiler

MPL is an EXORciser-compatible, high-level, user-oriented programming language for the Motorola MC6800 series Microprocessor. The language is a subset of PL/1 with features chosen for applicability to the Microprocessor environment.

MPL was designed to simplify the translation from functional requirements for a microprocessor application to an operating M6800 program. The MPL language and its associated compiler provide a powerful software tool which can significantly reduce the time and costs associated with microprocessor software development and maintenance.

- EXORciser and EXORterm Resident
- Based on PL/1, a Powerful High-Level Programming Language Widely Known and Used
- Supports Free Format, Block Structured Input
- Allows Embedded Assembly Language



System Configuration

The minimum system configuration is:

- An EXORciser or EXORterm 200
- An EXORdisk II Floppy Disk System
- 56K bytes of memory
- An EXORciser-compatible terminal
- Macro Assembler/Linking Loader Software
- Editor

MPL Advantages

- **Easy to Learn**
  The user orientation of MPL results in reduced training requirements and shorter project start-up times.
- **Easy to Read**
  The self-documenting nature of MPL simplifies software maintenance and product enhancement.
- **Easy to Write**
  User-oriented statement forms and free-format input simplify program writing. The MPL block structure encourages software modularity and structured programming.
- **Easy to Debug**
  A high-level language permits an emphasis on debugging algorithms and design flaws rather than on the details of an assembly language implementation.
- **Easy to Optimize**
  Assembly language output and the use of embedded assembly language allow the optimization of certain program segments for execution speed or memory space, without writing an entire program in assembly language. Calls to assembly language subroutines involve very little overhead.
- **Easy to Upgrade**
  Programs written in MPL for the M6800 will be translatable to future Motorola microprocessor products by recompiling, not rewriting.
- **Easy to use**
  - Higher productivity for software development
  - Lower software costs
  - Shorter design cycles
  - Easier product modification

Language Features

- **Stardard PL/I Statements**
  PROCEDURE
  DECLARE statement with INITIAL, DEFINED, BASED attributes
  IF, THEN, ELSE statement
  DO statement with TO, BY, WHILE clauses
  Assignment statement
  GOTO
  Subroutine CALL
  RETURN
  BEGIN
  END
- **Data Types**
  Bit
  Binary (1 or 2 bytes, signed or unsigned)
  Decimal (signed or unsigned)
  Character
  Label
- **Data Classes (Static or BASED)**
  Multidimensional arrays
  Structures
  Scalers
  Pointers
- **Arithmetic, Relational, and Logical Operations**
  Multiplication
  Division
  Subtraction
  Addition
  Shift
  Bitwise AND, OR, Exclusive OR
  EQ, NE, LT, GT, LE, GE
  AND, OR, NOT
- **Extensions**
  Address Constants
  Computed GOTO
  Embedded assembly language statements
  Optional subroutine CALL with register arguments
  Extensions for relocatability
  GLOBAL and EXTERNAL variables

Ordering Information

Part Number	Description
M68MPLR010M	Resident MPL Compiler on MDOS diskette

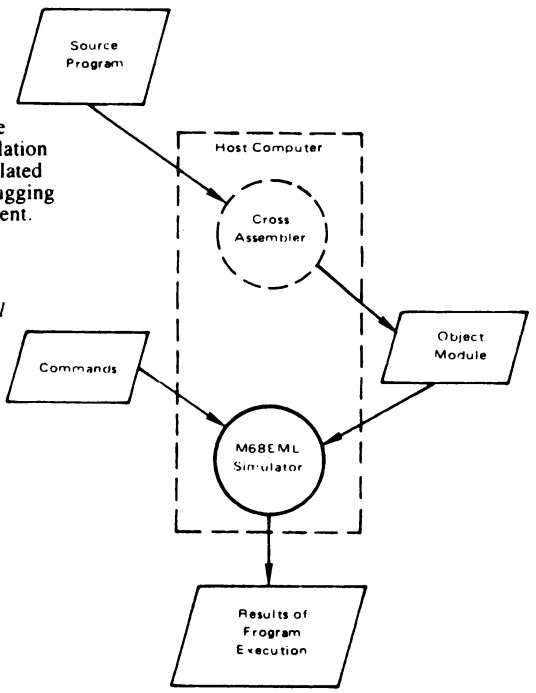
M68EML Simulator

The M68EML simulates the execution of M6800 machine language instructions in a host computer. Although the simulation is not performed in real time, it maintains a count of the simulated execution cycles. M68EML facilitates the testing and debugging of microprocessor programs in a host computer environment.

The M68EML Package includes:

- FORTRAN Source Program
- Formatted Source Listing and Installation Instructions
- A Copy of the *M6800 Programming Reference Manual*

OPERATION OF THE M6800 SIMULATOR



Inputs

- Object Module — EXORciser-compatible format (ASCII characters)
- Simulator Commands
  - D — Display Registers
  - DB — Set Display Base
  - DF — Set Display Flag
  - DL — Display Last Instruction
  - DM — Display Memory
  - EX — Exit
  - HR — Set Header Count
  - IB — Set Input Base
  - IM — Input Memory Tape
  - LW — Last Word Address
  - PF — Emulate Non-Maskable Interrupt
  - PO — Emulate Reset
  - R — Run
  - SD — Select Display Registers
  - SM — Set Memory
  - SR — Set Register
  - T — Trace Instruction Execution
  - TB — Trace Branches

A description of these commands is included in the *M6800 Programming Reference Manual*

Outputs

- Trace of Program Execution
  - Instruction Address
  - Operation Code Mnemonic
  - M6800 Registers
  - Effective Address
  - Timing
- Memory Dump
  - Print selected portions of simulated M6800 Memory

Host Computer Requirements

- Software
  - FORTRAN IV
  - Any operating system which will support FORTRAN programs
- Memory
  - 16 bit minimum word length (17 bits for 1's complement computers)
  - Memory size requirements vary due to computer and compiler differences. Estimates for common machines are included in Table 1
- Peripherals
  - M68EML uses three logical units
    - Command Input
    - Object Program Input (EXORciser-compatible ASCII format)
    - List output -- Simulation Results
  - In general the peripherals needed for FORTRAN are sufficient for M68EML

Source Media

M68EML consists of approximately 3000 source statements including comments. The source program is available in two forms:

- Cards — 80-Column Punched Cards in 029 Punch Code
- Magnetic Tape — Unlabeled 9-track 800 BPI, Odd Parity, ASCII Character Set, Card Image Records (80 characters/record)

Installation

Although M68EML was designed to be portable and machine independent, some program functions must be changed to adapt this simulator to the host computer. For computers listed in Table 1, machine dependent modifications already have been incorporated into the program. For these machines, installing M68EML consists of supplying the job control statements required to run a FORTRAN program.

Installation of M68EML on other machines is straightforward. Computer dependencies have been isolated and identified as separate program modules. Features which may require minor modification include:

- Input/Output including the assignment of logic devices
- Word-length Parameters
- Intrinsic Function (Logical AND, OR)
- Character Set Translation

The starting point for such an installation should be the Motorola-converted version of M68EML for the computer closest to the target system. Using the list in Table 1, match the computer characteristics first by the internal character set and then by word size.

TABLE 1 – ORDERING INFORMATION

Part Number	Media	Computer	HOST COMPUTER ATTRIBUTES			
			Character Set	Word Size	Negative Number	Memory Used[4]
M68EML0211E M68EML0211F	Cards Magnetic Tape	Sigma 9	8-Bit EBCDIC	32 Bits	2's Complement	17K Words
M68EML0411E M68EML0411F	Cards Magnetic Tape	HP2100[1]	8-Bit ASCII	16 Bits	2's Complement	16K Words
M68EML0711E M68EML0711F	Cards Magnetic Tape	IBM360/370	8-Bit EBCDIC	32 Bits	2's Complement	120K Bytes
M68EML0812E M68EML0812F	Cards Magnetic Tape	Nova[2]	8-Bit ASCII	16 Bits	2's Complement	18K Words
M68EML0911E M68EML0911F	Cards Magnetic Tape	Honeywell 6000	9-Bit ASCII	36 Bits	2's Complement	26K Words
M68EML1012E M68EML1012F	Cards Magnetic Tape	CDC6000	6/12-Bit Display Code	60 Bits	1's Complement	19K Words
M68EML1111E M68EML1111F	Cards Magnetic Tape	PDP-11[3]	8-Bit ASCII	16 Bits	2's Complement	18K Words

NOTES:
1. DOS III
2. RDOS
3. PDP11/05 DOS/BATCH
4. Although it may be possible to segment or overlay M68SAM, Motorola provides no information on how to do it. No attempt should be made to use less memory than that listed. Nor does Motorola guarantee this software to run on an operating system for 16-bit machines other than those listed.

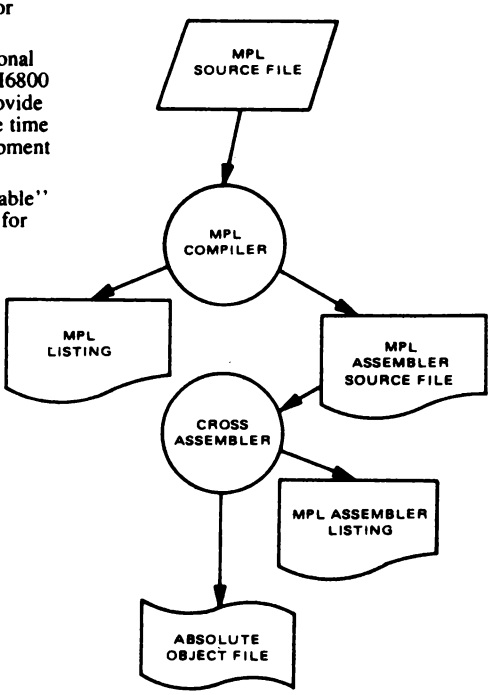
M68MPLC Cross Compiler

MPL is a high-level, user-oriented programming language for the Motorola M6800 Microprocessor. The language is a subset of PL/I with features chosen for applicability to the microprocessor environment.

MPL was designed to simplify the translation from functional requirements for a microprocessor application to operating M6800 programs. The MPL language and its associated compiler provide a powerful software tool which can significantly reduce the time and costs associated with microprocessor software development and maintenance.

MPL is available worldwide through timesharing. A "portable" version written in ANSI-standard FORTRAN is available for installation on in-house computer systems.

- Based on PL/I, a Powerful, High-Level Programming Language Which Is Widely Known and Used
- Supports Free Format, Block Structured Input
- Machine Independent
- Allows Embedded Assembly Language



Language Features

Standard PL/I Statements
- PROCEDURE
- DECLARE statement with INITIAL, DEFINED attributes
- IF, THEN, ELSE statement
- DO statement with TO, BY, WHILE clauses
- Assignment statement
- GOTO and GOTO with label arrays
- Subroutine CALL
- RETURN
- END

Data Types
- Bit
- Binary (1 or 2 bytes)
- Decimal (signed or unsigned)
- Character
- Labeled arrays

Data Classes (Static or BASED)
- Multidimensional arrays
- Structures
- Scalers
- Pointers

Arithmetic or Logical Operators
- Multiplication
- Division
- Subtraction
- *Addition*
- Shift
- Relational operators
- AND, OR, Exclusive OR

Extensions
- Address constants
- *Computed GOTO*
- Embedded assembly language statements
- ORIGIN
- Optional subroutine CALL with register arguments

MPL Advantages

- **Easy to Learn**
  The user-orientation of MPL results in reduced training requirements and shorter project start-up times.
- **Easy to Read**
  The self-documenting nature of MPL simplifies software maintenance and product enhancement.
- **Easy to Write**
  User-oriented statement forms and free-format input simplify program writing. The MPL block structure encourages software modularity and structured programming.
- **Easy to Debug**
  A high-level language permits an emphasis on debugging algorithms and design flaws rather than on the details of an assembly language implementation.
- **Easy to Optimize**
  Assembly language output and the use of embedded assembly language allow the optimization of certain program segments for execution speed or memory space, without writing an entire program in assembly language. Calls to assembly language subroutines involve very little overhead.
- **Easy to Upgrade**
  Programs written in MPL for the M6800 will be transferable to future Motorola microprocessor products by recompiling, not rewriting.
- **Easy to Use**
  - Higher productivity for software development
  - Lower software costs
  - Shorter design cycles
  - Easier product modification

Installation

The MPL Compiler has been designed to be as machine-independent as possible. However, some program functions must be changed to adapt it to a particular host computer. For computers listed in Table 1, machine dependent modifications already have been incorporated into the program. For these machines, installing MPL consists of supplying the job control statements required to run a FORTRAN program.

Installation of MPL on other machines is straightforward. Computer dependencies have been isolated and identified as separate program modules. Features which may require modification include:

- Input/Output including the assignment of logic devices
- Intrinsic Function (Logical AND, OR; Right and Left Shift)
- Character Set Translation

Host Computer Requirements

- Software
  - ANSI FORTRAN IV
  - Any operating system that supports ANSI FORTRAN IV
- Memory
  - 32-bit minimum word length
  - Memory size requirements vary due to computer and compiler differences. Estimates for machines for which the compiler is currently available are given in Table 1.
- Peripherals
  - MPL uses three or five logical units
    - Source Input
    - MPL Subroutine Library Input
    - Compiler Output
    - Terminal Input and Output on a Time-Sharing System
  - In general the peripherals needed for FORTRAN are sufficient for MPL.

Source Media

MPL consists of approximately 5500 source statements including comments. The source program is available in two forms:

- Cards — 80 Column Punched Cards in O29 Punch Code
- Magnetic Tape — Unlabeled 9-track 800 BPI, Odd Parity, ASCII Character Set, Card-Image Records (80 character/record).

The starting point for such an installation should be the Motorola-converted version of MPL for the computer closest to the target system. Using the list in Table 1, match the computer characteristics first by the internal character set and then by word size.

The output from MPL is assembly language, therefore an M6800 Assembler is required.

TABLE 1 – ORDERING INFORMATION

Part Number	Media	Computer	HOST COMPUTER ATTRIBUTES			
			Character Set	Word Size	Negative Number	Memory Used
M68MPL0212E M68MPL0212F	Cards Magnetic Tape	Xerox Sigma 9	8-Bit EBCDIC	32 Bits	2's Complement	25K Words
M68MPL0712E M68MPL0712F	Cards Magnetic Tape	IBM360/370	8 Bit EBCDIC	32 Bits	2's Complement	140K Bytes
M68MPL0912E M68MPL0912F	Cards Magnetic Tape	Honeywell 6000	9-Bit ASCII	36 Bits	2's Complement	26K Words
M68MPL1012E M68MPL1012F	Cards Magnetic Tape	CDC6000	6/12 Bit Display Code	60 Bits	1's Complement	30K Words

M68SAM Cross Assembler

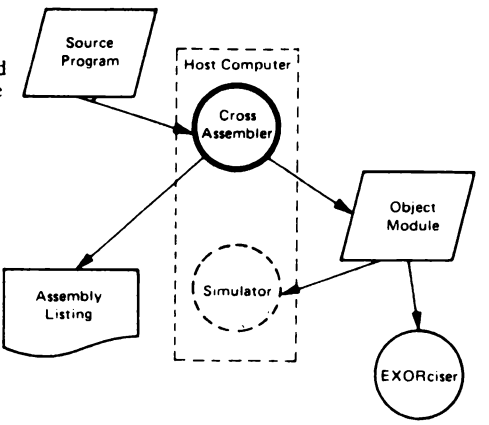
M68SAM is a Cross Assembler used to translate M6800 assembly language source programs into M6800 machine language. M68SAM is compatible with the time-sharing and resident assemblers for the M6800 MPU.

Using a host computer for software development reduces the load on the M6800 development systems and provides access to the host computer's other resources including text editors, file systems, and peripherals.

The M68SAM Package includes:

- FORTRAN Source Program
- Formatted Source Listings and Installation Instructions
- A Copy of the *M6800 Programming Reference Manual*

OPERATION OF THE M6800 CROSS ASSEMBLER



Assembly Language Input

- 72 Assembly Language Operation Codes
- 7 Address Modes
- 11 Assembler Directives (Pseudo-operations)

END	End of Program
EQU	Equate Symbol
FCB	Form Constant Byte
FCC	Form Constant Characters
FDB	Form Double Constant Byte
NAM	Name
ORG	Origin
PAGE	Top of Form
RMB	Reserve Memory Byte
SPC	Space Lines
OPT	Option
	DB8 Display Base Octal
	DB10 Display Base Decimal
	DB16 Display Base Hexadecimal (default)
	LIST (default)
	NOLIST

The M6800 Assembly Language is described in the *M6800 Programming Reference Manual*.

Assembler Output

- Object Module—EXORciser-compatible Format (ASCII Characters)
- Assembly Listing
  (Display Base Selectable: Octal, Decimal, Hexadecimal)
- Symbol Table

Host Computer Requirements

- Software
  - FORTRAN IV
  - Any operating system which will support FORTRAN programs
- Memory
  - 16 bit minimum word length
    (17 bits for 1's complement computers)
  - Memory size requirements vary due to computer and compiler differences. Estimates for common machines are included in Table 1.
- Peripherals
  - M68SAM uses three logical units
    - Source Input
    - Object Output (EXORciser-compatible ASCII format)
    - List Output
  - in general the peripherals needed for FORTRAN are sufficient for M68SAM.

Source Media

M68SAM consists of approximately 2500 source statements including comments. The source program is available in two forms:

- Cards — 80-Column Punched Cards in O29 Punch Code
- Magnetic Tape — Unlabeled 9-track 800 BPI, Odd Parity, ASCII Character Set, Card-Image Records (80 character/record).

Installation

Although M68SAM was designed to be portable and machine independent, some program functions must be changed to adapt this assembler to the host computer. For computers listed in Table 1, machine dependent modifications already have been incorporated into the program. For these machines, installing M68SAM consists of supplying the job control statements required to run a FORTRAN program.

Installation of M68SAM on other machines is straightforward. Computer dependencies have been isolated and identified as separated program modules. Features which may require minor modification include:

- Input/Output including the assignment of logic devices
- World-length Parameters
- Intrinsic Function (Logical AND, OR)
- Character Set Translation

The starting point for such an installation should be the Motorola-converted version of M68SAM for the computer closest to the target system. Using the list in Table 1, match the computer characteristics first by the internal character set and then by word size.

TABLE 1- ORDERING INFORMATION

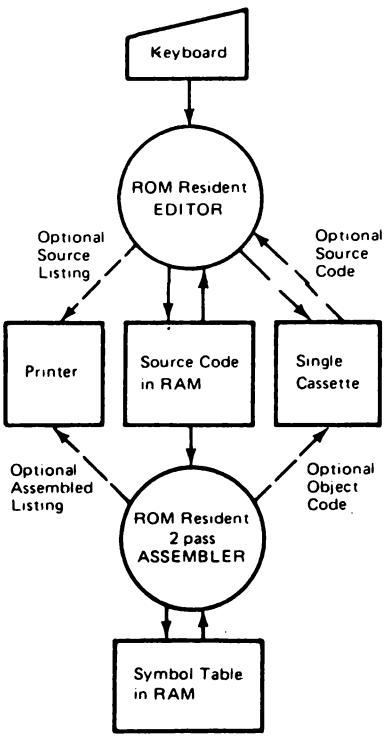
Part Number	Media	Computer	HOST COMPUTER ATTRIBUTES			
			Character Set	Word Size	Negative Number	Memory Used[4]
M68SAM0214E M68SAM0214F	Cards Magnetic Tape	Sigma 9	8 Bit EBCDIC	32 Bits	2's Complement	9K Words
M68SAM0413E M68SAM0413F	Cards Magnetic Tape	HP 2100[1]	8-Bit ASCII	16 Bits	2's Complement	15K Words
M68SAM0713E M68SAM0713F	Cards Magnetic Tape	IBM 360/370	8-Bit EBCDIC	32 Bits	2's Complement	64K Bytes
M68SAM0814E M68SAM0814F	Cards Magnetic Tape	Nova[2]	8-Bit ASCII	16 Bits	2's Complement	16K Words
M68SAM0912E M68SAM0912F	Cards Magnetic Tape	Honeywell 6000	9-Bit ASCII	36 Bits	2's Complement	17K Words
M68SAM1014E M68SAM1014F	Cards Magnetic Tape	CDC 6000	6/12-Bit Display Code	60 Bits	1's Complement	16K Words
M68SAM1112E M68SAM1112F	Cards Magnetic Tape	PDP-11[3]	8-Bit ASCII	16 Bits	2's Complement	16K Words

NOTES:
1. DOS III
2. RDOS
3. PDP11/05 DOS/BATCH
4. Although it may be possible to segment or overlay M68SAM, Motorola provides no information on how to do it. No attempt should be made to use less memory than that listed. Nor does Motorola guarantee this software to run on an operating system for 16-bit machines other than those listed.

M68EAB1 Editor/Assembler/ Basic Module

- M68ADS/ADW plug-in compatible
- ROM resident
- Immediate access without software loading time
- Uses only a low-cost non-incremental single audio-cassette
- Software addresses: BASIC – from 4000 to 5BFF
  Editor/Assembler – from 6400 to 7FFF
- ACIA address: 8008 (alterable)
- High speed assembly directly from memory
- Assembler RAM requirement: approx. 1.5K bytes per 50 user's program statements
- Basic high level language features:
  - decimal arithmetic
  - string variable and array
  - direct statement execution capability (calculator mode)
  - user programs may reside on audio-cassette
  - string functions and concatenation
- Dimensions (W X H X T): 9.8 X 6.5 X 0.5 inches

EDITOR / ASSEMBLER MODULE BLOCK DIAGRAM



The M68EAB1 is a 14K ROM module containing an adapted ROM co-resident Editor/Assembler and a ROM resident BASIC interpreter to be used on an autonomous Development System equipped with a single audio-cassette set. The source and/or the object code can be loaded from or dumped to the cassette. Both Editor/Assembler and Basic run from the ROM, leaving all RAM available as a buffer for source code and symbol table.

The Assembler requires that the source code has been loaded into the RAM by the Editor before automatically performing the two-pass assembly. This feature allows the use of a non-incremental single cassette system.

The ROM resident BASIC interpreter provides a new tool for problem-solving to the M6800 Microcomputer family of parts.

BASIC is a high-level programming language widely used for general-purpose and certain business-related applications.

EXORciser is a trademark of Motorola Inc.

BASIC Commands

- LIST display source
- RUN execute program
- CONT continue after stop or break
- NEW define new program
- SAVE save current program (tape)
- LOAD load new program (tape)
- APPEND add to program from tape
- PATCH patch memory from MINIbug
- TRACE ON print line number as it is executed
- TRACE OFF turn off trace
- LINE LENGTH - define maximum print line length
- DIGITS establish the number of digits to right of decimal point
- POKE sets absolute memory address

Subprograms

- DEF define user function
- RETURN - return from subroutine
- GOSUB - go to subroutine

Intrinsic functions

- TAB tab on print
- RND - random number
- INT - integer number
- ABS - absolute value
- SGN sign of argument
- POS - position of printhead
- LEN number of characters in string
- ASC decimal value of any ASCII character
- CHR$ - string value of ASCII character
- STR$ ASCII string value to numeric constant
- VAL numeric constant equivalent to ASCII value
- LEFT$ returns left-most string of characters
- RIGHT$ - returns right-most string of characters
- MID$ returns middle string of characters
- PEEK returns decimal memory value
- SIN sine
- COS cosine
- TAN tangent
- ATAN arc tangent
- LOG - natural logarithm
- EXP - inverse of LOG
- SQR - square root

BASIC Language Features

Data types

- Range (1.0E - 99 to 9.99999999E + 99) may be represented as either integer, decimal, or exponential

Variable names

- Single alphabetic character or single alphabetic character followed by a digit (0 through 9)
- String variables, single alphabetic character followed by a $

Arithmetic and logical operators

- Exponential
- Negate
- Multiplication
- Division
- Addition
- Subtraction
- Relational operators

Sequence control statements

- GOTO
- ON expression GOTO statement n, (m . . . , 1)
- ON expression GOSUB statement n, (m . . . , 1)
- IF relative
- FOR
- NEXT
- STOP
- END

I/O statements

- INPUT
- READ
- DATA
- PRINT
- RESTORE

Specification statement

- DIM dimension variables and strings

Remark statements

- REM

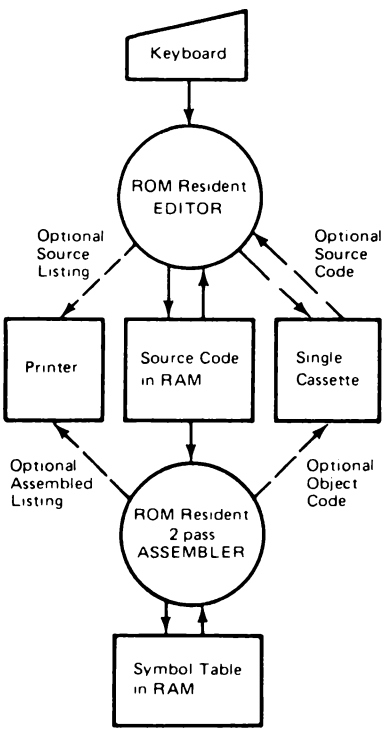
Optional statements

- LET

M68EAM1
Editor/Assembler Module

- M68ADS/ADW plug-in compatible
- EXORciser plug-in compatible
- ROM resident
- Immediate access without software loading time
- High speed assembly directly from memory
- Uses only a low-cost non-incremental single audio cassette
- ROM Monitor independent input/output routines
- Software addresses: from 6400 to 7FFF (hexadecimal)
- ACIA address: 8008 (alterable)
- RAM requirement: approximately 1.5K bytes per 50 user's program statements
- Dimensions (W X H X T): 9.8 X 6.5 X 0.5 inches

EDITOR / ASSEMBLER MODULE BLOCK DIAGRAM



The M68EAM1 is a 7K ROM module containing an adapted ROM co-resident Editor/Assembler for use on an autonomous development system equipped with a single audio-cassette set.

The source and/or the object code can be loaded from or dumped to the cassette. Both Editor and Assembler run from the ROM, leaving all RAM available as a buffer for source code and symbol table. The Assembler requires that the source code has been loaded into the RAM by the Editor before automatically performing the two-pass assembly. This feature allows the use of a non-incremental single cassette system.

The software is not dependent on any firmware monitor, although it uses the MINIbug II addressed ACIA as a communication device.

MOTOROLA

MEC68MIN3E

MINIBUG 3E FIRMWARE

The MINIBUG 3E Firmware provides the user with an efficient means to debug his program allowing to insert up to 8 breakpoints. It communicates with a serial peripheral (which can be the IOS ACIA) through an ACIA located in 8008 and works with either 1 or 2 stop bits.

MINIBUG 3E has the same Input/Output subroutines entry points as MINIBUG 2.

MINIBUG 3E FIRMWARE
(MCM6830 pin-out)

Memory load	L
Print/Punch Dump (from nnnn to mmmm)	P nnnn mmmm
Memory Examine/Change	M nnnn
– open next location	(LF)
– open previous location	↑
Print MPU Registers (CC,B,A,X,PC,SP) (saved in stack, vect. A032/A033)	R
Go to user's program	G nnnn
Continue execution from current location	C
Execute Next instruction	N
Trace nnnn instructions	T nnnn
Set a breakpoint at address nnnn	V nnnn
Reset the breakpoint at address nnnn	U nnnn
Delete all breakpoints	D
Print out all breakpoints	B
Select 2 stop bits (default value)	S1 (for Speed 110 baud)
Select 1 stop bit	S3 (for Speed ⩾ 300 baud)

ROM address	E000 to E3FF
RAM address	A000 to A07F
ACIA address	8008
User's stack pointer	saved
Space required in user's stack	14 bytes

Restart Vector	ROM (E3FE/E3FF)
NMI Apparent Vector	RAM* (A006/A007)
SWI Apparent Vector	RAM* (A036/A037)
IRQ Apparent Vector	RAM* (A000/A001)

*1. If the MINIBUG 3E is used in conjunction with IOS Firmware, the actual vectors are fetched in IOS ROM; but after IOS service, control is given to MINIBUG 3E which fetches the apparent NMI, SWI and IRQ vector in RAM and jumps to the corresponding user's service routine.
The MINIBUG 3E ROM should be accessed with the following address pattern:
1110 00 XX XXXX XXXX

2. If the MINIBUG 3E ACIA (8008) is directly connected to a serial terminal and the IOS Firmware is not present, the actual vectors are fetched in MINIBUG ROM; but then, MINIBUG 3E fetches the apparent NMI, SWI and IRQ vectors in RAM and jumps to the corresponding user's service routine.
The MINIBUG 3E ROM should be accessed with the following address patterns:
1110 00XX XXXX XXXX
or 1111 ..XX XXXX XXXX

3. The SWI apparent vector (RAM A036/A037) is initialized at E308 (MINIBUG 3E Breakpoint Routine) each time a reset is applied.

MOTOROLA

M68IOS1

INPUT/OUTPUT SUPERVISOR

POLYVALENT DEVELOPMENT SYSTEM

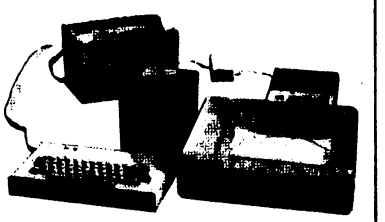
INPUT/OUTPUT SUPERVISOR

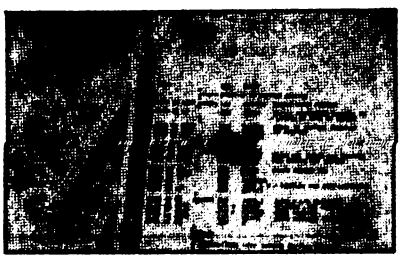
The M68IOS1 Input/Output Supervisor Firmware provides the user with an efficient means to interface the Polyvalent Development System Peripherals (CRT, Keyboard, Printer) to either a co-resident MINIBUG Firmware and a user's software or to an external asynchronous line such as the TTY connection of the EXORciser.

- Compatible with M68DIM1 and M68DIM2 16-line x 32-character Display Interfaces (PIA 8020, PB7 = 0)
- Compatible with M68DIM6 16-line x 64-character Display Interface (PIA 8020, PB7 = 1)
- Can work with co-resident standard I/O Routines
- Standard ACIA main system connection (8-bit word, 1 stop bit)
- Cursor control
- Background control (white-on-black or black-on-white display).

When the display page is full, the next line will be displayed at the bottom line, and the whole page is shifted one line up, loosing the top line (Scroll-up Display).

PDS





IOS CONTROL CHARACTERS

Code	Effect	Co-resident configuration received by		Terminal configuration		
				Off-line received by Keyboard	On-line received by	
		Keyboard	ACIA (8010)		Keyboard	ACIA (8008)
CtrlE	Erase screen	X	X	X	X	X
CtrlB	Background change for subsequent characters	X	X	X	X	X
CtrlO	Change mode of Operation (local/on-line)	–	–	X	X	X
CtrlG	Sound the bell (negative pulse on CA2 of PIA 8020)	–	X	X	–	X
CtrlU	Cursor Up one line		X	X		X
CtrlW	Cursor doWn one line		X	X		X
CtrlN	Cursor to Next character		X	X		X
CtrlH	Cursor to previous character (Back Space)		X	X		X
CtrlL	Cursor to home (Form Feed)		X	X		X
CtrlC	Clear page from cursor		X	X		X
CtrlK	Kill line from cursor		X	X		X
Null	Not transmitted		X	X		X
Rubout	Not transmitted		X	X		X

Co-resident configuration

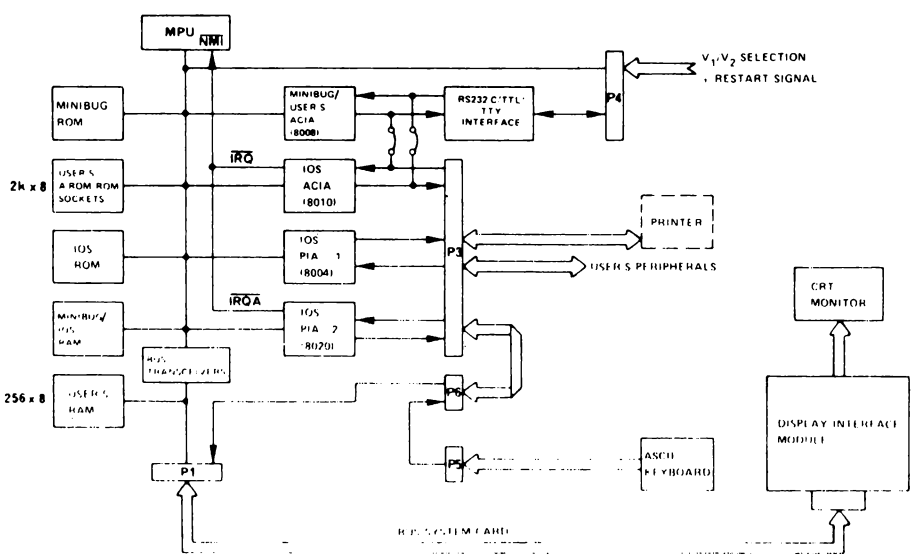
The co-resident software MINIBUG and the user's program communicates with IOS Firmware through the IOS ACIA located at 8010.

The IOS routines are accessed by NON MASKABLE INTERRUPTS generated by its interfaces. If another source generated the NMI, IOS gives control back to E005 location, which is the MINIBUG NMI service routine.

- If a character was received in the IOS ACIA (8010) coming from the user's MINIBUG ACIA (8008) it is transmitted to the Printer PIA (8004) and to the Display Interface Module. The non-visuable characters are not transmitted.
- If a character was received in the Keyboard PIA (8020), it is transmitted to the IOS ACIA (8010), in order to be received later on in the user's MINIBUG ACIA (8008). If CtrlE (Erase screen) or CtrlB (Background Change for subsequent characters) were received from the Keyboard, they are not transmitted to the ACIA.

ROM address	DC00 to DFFF*
RAM address	A000 to A07F shared with MINIBUG Firmware
IOS ACIA address	8010
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line pointer PIA address	8022
User's Stack Pointer	Saved
Space required in user's stack	28 bytes
Restart action	initializes IOS interfaces, jumps to MINIBUG Restart Routine
NMI action	IOS action and jumps to MINIBUG NMI Routine
SWI, IRQ action	jumps to MINIBUG SWI, IRQ Routine
Start up action	Erases screen, Restart

*The ROM should be wired with the following address patterns:
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX



Terminal Configuration

The external system, as the EXORciser, communicates with the IOS Firmware through ACIA located at 8008.
The characters to be printed are stored in a buffer of 123 characters, which is sent to the printer when full or at least each 300 ms without receiving a new character from the terminal ACIA. The PA7 line of the PIA (8020) is pulled high during Printer Operation. This line should be connected to the CTS line of the main system ACIA (i.e. DEBUG ACIA) in order to inhibit the transmission of new characters.
The Keyboard accesses to IOS routines by generating a NON MASKABLE INTERRUPT.
Two modes of operation are possible:

Local mode (Off-Line)

– The ACIA (8008) is not taken into account.
– The characters received from the Keyboard PIA (8020) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visuable characters are not transmitted.

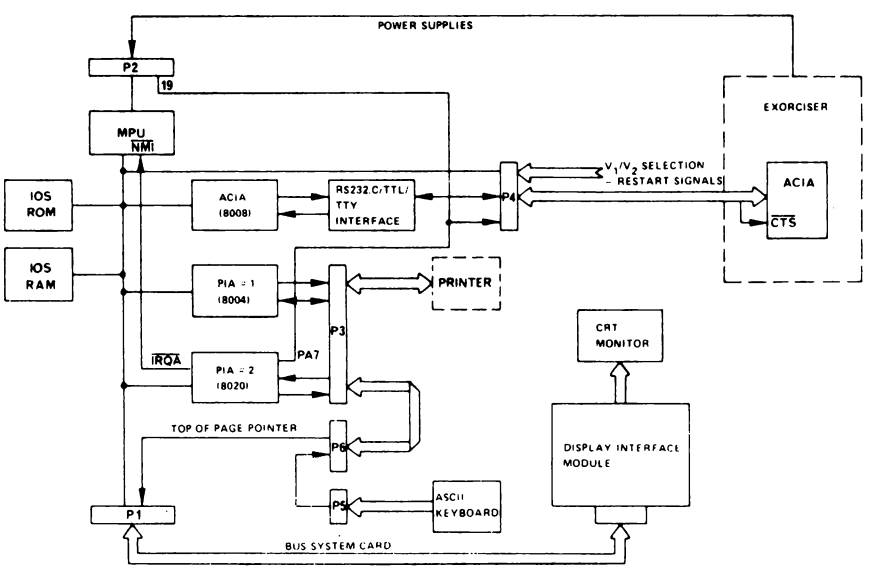
On-Line mode (full-duplex)

– The characters received from the ACIA (8008) are transmitted to the Display Interface Module and to the Printer Buffer. The non-visuable characters are not transmitted.
– The characters received from the Keyboard PIA (8020) are transmitted to the ACIA (8008). All characters, except CtrlB, CtrlE and Ctrl0 are transmitted.

ROM address	DC00 to DFFF*
RAM address:	
scratch pad	A000 to A07F
Printer Buffer	0000 to 007F
ACIA address	8008
Printer PIA address	8004
Keyboard PIA address	8020 (PA0 to PA6)
Bell line	CA2 of PIA (8020)
Hardware Top-of-Page line pointer PIA address	8022
CTS line	PA7 of PIA 8020

*The ROM should be wired with the following address pattern,
1101 11XX XXXX XXXX
or 1111 ..XX XXXX XXXX[1]

[1]Note: in this configuration, A9 is set to 0 by hardware when the MPU accesses to FFF8 to FFFF vectors.



chapter 3

microcomputer subsystems

MICROMODULE

CHASSIS/CARD CAGES/POWER SUPPLY

MICROMODULE CHASSIS

The M68MMLC Long Chassis and the M68MMSC Short Chassis offer two means of supporting the prototyping or production of M6800-based microcomputer systems. Each chassis comprises one M68MMPS1 Power Supply and a M68MMCC10 10-Card Cage or M68MM05 5-Card Cage in a long or short cabinet, respectively. The chassis motherboards are pin compatible with all M6800 EXORciser modules and micromodules.

An optional slide kit is available for mounting each chassis in a standard RETMA 19" rack. M68MMLC requires 19.5" and M68MMSC requires 12" of cabinet depth to provide adequate clearance for fan intake.

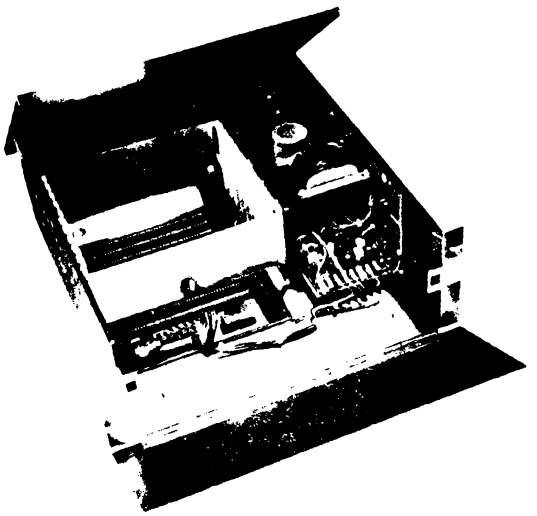
FEATURES

- Two pre-wired, ready-to-use models: long 10-card chassis, short 5-card chassis
- Standard RETMA 19" rack mounting using optional rack mounting kits
- Power Supply: 15 A at +5 V, 2.5 A at +12 V, 1.5 A at -12 V
- Motherboard pin compatible with all M6800 system modules — **Micromodules** and **EXORciser**
- Muffin fan cooling (accepts Howard 3-90-8099 filter)

PHYSICAL CHARACTERISTICS

Material — 0.060" cold rolled, low-carbon steel

Finish — Zinc plating, QQ-Z-326, Class 3, Type Z, yellow



MICROMODULE CARD CAGES

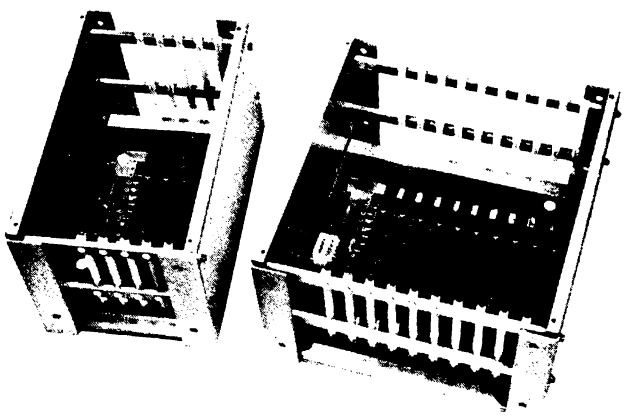
The M68MMCC10 and M68MMCC05 Card Cages offer additional support for the development or production of M6800-based microcomputer systems. Each cage of 10- and 5-card capacity, respectively, includes a motherboard with board connectors, card guides and accommodations for connecting power to the cage. Mounting holes are provided in all four sides and the bottom for mounting a cage in five of the six possible orientations. Provision is also made for mounting the M68MMPS1 Power Supply on either end of the cage.

FEATURES

- Two models: 5 and 10 card
- Five orientation mountings
- Provides micromodule bus interconnection

PHYSICAL CHARACTERISTICS

Material – 0.093" aluminum alloy
Finish – Class 1 double iridescent film, MIL-C-5541
Weight – 3.25 lbs (CC05)
5.5 lbs (CC10)



MICROMODULE POWER SUPPLY

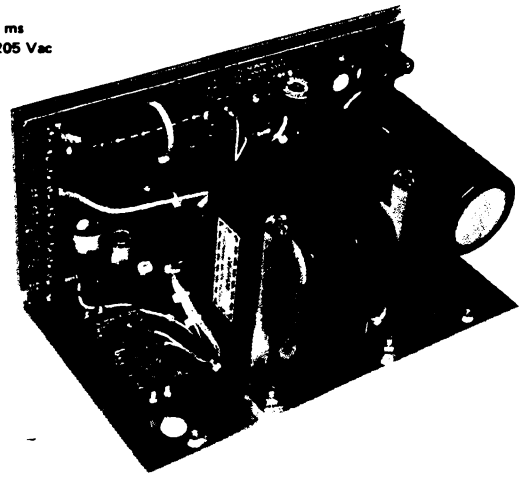
More than ample power at the voltages required by a microcomputer system built around the M6800 family modules: +5 Vdc, ±12 Vdc—is provided by the M68MMPS1 power supply. Its design provides internal protection against shorts and overload and its outputs recover automatically to normal voltage when an overload is removed. The +5 Vdc output is overvoltage protected dropping to 5 volts or less within 50 microseconds after rising to 7 volts. A remote sensing capability which can compensate for as much as 0.5 Vdc drop in connecting leads is also provided on the +5 Vdc output.

FEATURES

- +5 Vdc at 15 A, +12 Vdc at 2.5 A, −12 Vdc at 1.5 A
- +8 Vac at 0.1 A
- Short circuit protected
- Overload protected
- Overvoltage protection (5 Vdc output)
- Remote sensing (5 Vdc output)

PHYSICAL AND ELECTRICAL CHARACTERISTICS

Input Voltage	**95 to 125 Vac, 205 by 250 by jumper**
Input Frequency	**47 to 420 Hz, single phase**
Operating Temperature Range	**0°C to 50°C, derate current linearly to 70% of rated from 50°C to 70°C**
Voltage Isolation	**Input to case, 500 Vdc** **Output to case, 200 Vdc**
Power Fail Rating	**DC voltages maintained for 8 ms minimum at low line (95 or 205 Vac and rated load); all outputs**
Dimensions	**Length, 9.5"** **Width, 6.25"** **Height, 5.0"** **Weight, 11.25 lbs**



OUTPUTS

	+5 Vdc	+12 Vdc	−12 Vdc	8 Vac
Rated Current	15 A	2.5 A	1.5 A	0.1 A
Load Regulation	0.1%	0.1%	0.1%	
Line Regulation	0.1%	0.05%	0.05%	
RMS Ripple	2 mV	1 mV	1 mV	
P-to-P Ripple	10 mV	5 mV	5 mV	
Temperature Coefficient (%/°C)	0.05	0.05	0.05	

PRODUCT ORDERING INFORMATION

Part numbers of the chassis/card cage/power supply/mounting kit options are identified in the following table.

PART NO.	DESCRIPTION
M68MMLC1	Micromodule Chassis with 10-card cage, 115 Vac power supply
M68MMLC2	Micromodule Chassis with 10-card cage, 230 Vac power supply
M68MMSC1	Micromodule Chassis with 5-card cage, 115 Vac power supply
M68MMSC2	Micromodule Chassis with 5-card cage, 230 Vac power supply
M68MMPS1-1	Micromodule Power Supply, 95 to 125 Vac, 47 to 420 Hz, single phase
M68MMPS1-2	Micromodule Power Supply, 205 to 250 Vac, 47 to 420 Hz, single phase
M68MMCC05	Card Cage, 5 card
M68MMCC10	Card Cage, 10 card
M68MMLK	Rack Mounting Kit, Long Chassis
M68MMSK	Rack Mounting Kit, Short Chassis

M68MM01

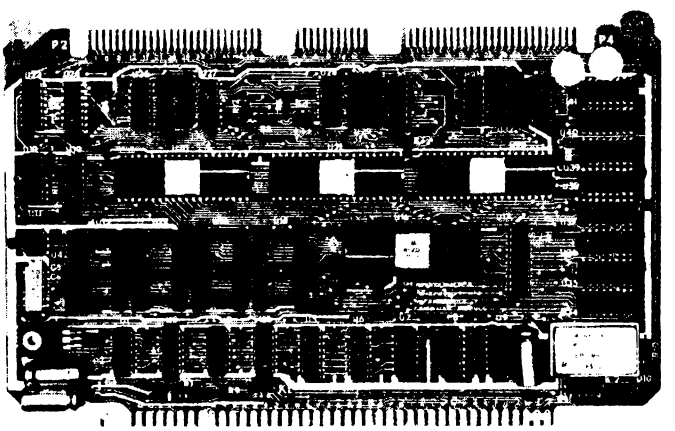
MONOBOARD MICROCOMPUTER 1

MICROMODULE 1

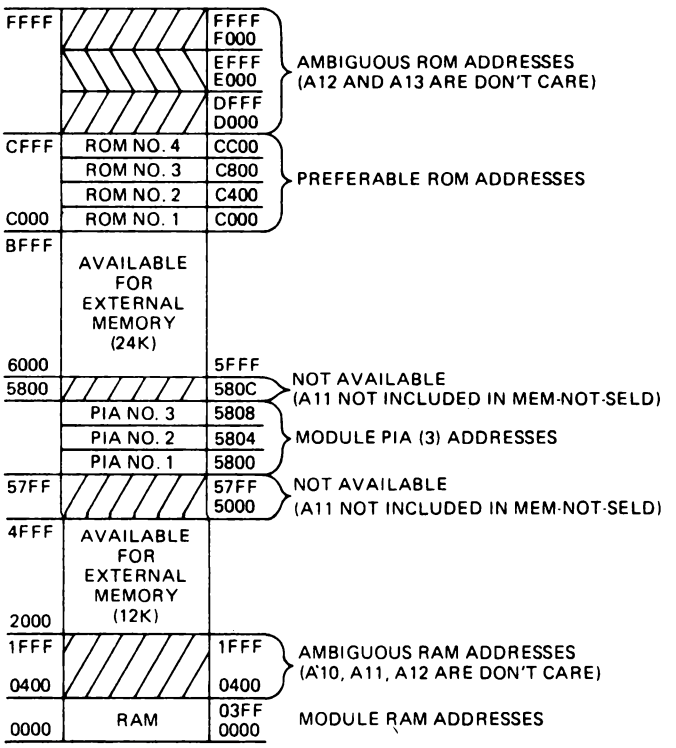
The M68MM01 Monoboard Microcomputer 1 – Micromodule 1 – is a complete computer-on-a-board that can provide the solution for most processing and control applications. Micromodule 1 contains all of the processing and control power of the M6800 Microprocessing Unit (MPU) plus: 1K of static RAM to provide temporary program (scratch) storage; three Peripheral Interface Adapters (PIAs) to provide programmable input/output parallel data lines for transferring data between Micromodule 1 and the external system; and four sockets for installing up to 4096 bytes of AROM or ROM memory used to store firmware programs. Micromodule 1 also incorporates the necessary two-phase clock generator, the power-on reset circuitry for initialization, address bus decoding for establishing the memory location for each addressable part, the refresh circuit required for use with optional external dynamic memories, and the bus interface and controls needed to satisfy the basic requirements of a microcomputer system.

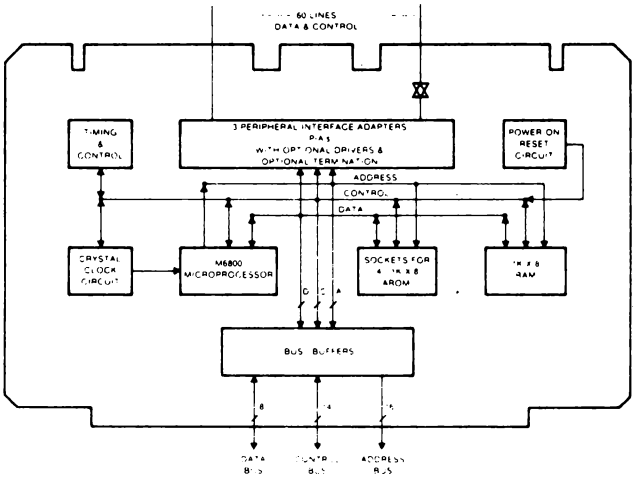
FEATURES

- Complete microcomputer on a board
- MC6800 Microprocessing Unit (MPU)
- 1 MHz crystal controlled clock
- On-board reset circuitry
- 1K static RAM
- Sockets for four 1K AROM or ROM firmware program memories
- Three MC6820 Peripheral Interface Adapters (PIAs)
- Dynamic memory refresh circuitry
- 36K bytes of unused memory addresses available
- EXORciser and Micromodule Family bus compatible



MEMORY MAP


FFFF
FFFF
F000
EFFF
E000
DFFF
D000
AMBIGUOUS ROM ADDRESSES
(A12 AND A13 ARE DON'T CARE)
CFFF
ROM NO. 4
CC00
ROM NO. 3
C800
ROM NO. 2
C400
C000
ROM NO. 1
C000
PREFERABLE ROM ADDRESSES
BFFF
AVAILABLE FOR EXTERNAL MEMORY (24K)
6000
5FFF
5800
580C
NOT AVAILABLE
(A11 NOT INCLUDED IN MEM-NOT-SELD)
PIA NO. 3
5808
PIA NO. 2
5804
PIA NO. 1
5800
MODULE PIA (3) ADDRESSES
57FF
57FF
5000
NOT AVAILABLE
(A11 NOT INCLUDED IN MEM-NOT-SELD)
4FFF
AVAILABLE FOR EXTERNAL MEMORY (12K)
2000
1FFF
1FFF
0400
0400
AMBIGUOUS RAM ADDRESSES
(A10, A11, A12 ARE DON'T CARE)
0000
RAM
03FF
0000
MODULE RAM ADDRESSES


60 LINES
DATA & CONTROL
TIMING & CONTROL
3 PERIPHERAL INTERFACE ADAPTERS
WITH OPTIONAL DRIVERS &
OPTIONAL TERMINATION
POWER ON RESET CIRCUIT
ADDRESS
CONTROL
DATA
CRYSTAL CLOCK CIRCUIT
M6800 MICROPROCESSOR
SOCKETS FOR
AROM
RAM
BUS BUFFERS
DATA BUS
CONTROL BUS
ADDRESS BUS

GENERAL DESCRIPTION

The two-phase clock generator consists of an MC6871 crystal controlled clock, operating at a frequency of 1 MHz, that provides a two-phase NMOS clock to the MPU, a single TTL-compatible $\phi 2$ clock used for synchronizing data transfers, and a single ungated memory clock and memory ready control for refreshing external dynamic memories. The $\phi 2$ TTL clock and the memory clock and memory ready control are available for external use via the control bus. The power-on reset circuitry provides reset control for the MPU and is also available for external use via the control bus.

The 16-bit MPU address bus is decoded on the board and provides addressable controls for RAM (0000_{16} to $03FF_{16}$), the three PIAs (5800_{16} to $580B_{16}$), and ROM ($C000_{16}$ to $CFFF_{16}$). Since the addresses are not fully decoded, certain addresses become ambiguous and, therefore, are not available. The address map clearly shows all of the addresses used by Micromodule 1 as well as those addresses that are or are not available due to this ambiguity. As indicated in the memory map, if additional Micromodules are to be used with Micromodule 1, the additional module addresses must be selected to reside within the available memory locations (2000_{16} to $4FFF_{16}$ and 6000_{16} to $BFFF_{16}$).

Sixty input/output lines are provided by the three PIAs: 24 programmable input/output parallel data lines, 12 buffered parallel data output lines with optional terminations (three 4.7 K ohm pull-up resistor networks or three 330/220 ohm pull-up/pull-down resistor networks), 12 buffered parallel data lines with optional TTL-compatible input or output configurations (also including the optional terminations), 6 programmable interrupt input control lines, 3 programmable peripheral control outputs, and 3 programmable interrupt inputs or control outputs. These input/output data and control lines permit data to be transferred in parallel between the microcomputer and the external system.

Micromodule 1 also incorporates features to permit easy modification of the module to operate with external memories in place of the on-board AROM or ROM devices or to change the B section peripheral data lines on the three PIAs from an output configuration to an input configuration.

Micromodule 1 is not only compatible with the Micromodule Family but also with the M6800 EXORciser, a versatile tool providing a system for developing and debugging hardware/software systems and troubleshooting production hardware. Advantage can also be taken of the EXORciser's AROM/ROM programming capability and optional memory and I/O modules.

It is not recommended that Micromodule 1 be used in the EXORciser in place of the CPU module to develop software and firmware programs, since the 1K of static RAM located on Micromodule 1 may be incompatible with the external RAM devices and therefore may cause malfunctions to occur due to the ambiguous operation of the RAM at address locations 0000_{16} to $03FF_{16}$. Micromodule 8, consisting of a monitor/debug ROM and an ACIA module, is available to aid in debugging hardware and software.

SPECIFICATIONS

Power Requirements	
Without AROMs/ROMs	+5 Vdc ± 5% @ 1.1 A (max)
or other optional	+12 Vdc ± 5% @ 0.0 mA
circuits installed	-12 Vdc ± 5% @ 0.5 mA (max)
With AROMs/ROMs and	+5 Vdc ± 5% @ 1.1 A (max)
other optional	+12 Vdc ± 5% @ 260 mA (max)
circuits installed	-12 Vdc ± 5% @ 180 mA (max)
Memory Size	
RAM	1024 8-bit bytes of Random Access Memory
AROM/ROM	Sockets for mounting up to four MCM68708 AROMs or MCM68308 ROMs
Interface Signals	
PA0 to PA7, CA1 and CA2	TTL-compatible
PB0 to PB7, CB1 and CB2	TTL-compatible with user selected interface terminations
Micromodule Bus Signals	
Address Bus	Three-state TTL-compatible buffered output
Data Bus	
Input	TTL-compatible buffered input
Output	Three-state TTL-compatible buffered output
Control Bus	
R/W, VMA (VUA)	Three-state TTL-compatible buffered output
Others	TTL-compatible
Operating Temperature	0° to 70° C
Physical Characteristics	
Width X Height	9.75 in. X 6.000 in.
Board Thickness	0.062 in.
Connectors (Optional)	
86-Pin Connector	Stanford Applied Engineering SAE-43D/1-2 or equivalent
50-Pin Connector (2)	3M Connector 3415-0001 or equivalent
20-Pin Connector	3M Connector 3461-0001 or equivalent

Specifications are subject to change without notice.

PRODUCT ORDERING INFORMATION

Use the part numbers listed below when ordering the Monoboard Microcomputer 1 Module or one of its optional configurations.

PART NO.	DESCRIPTION
M68MM01	Basic Monoboard Microcomputer 1 Module
M68MM01-1	Basic Monoboard Microcomputer 1 Module with 4 connectors and three 4.7 K ohm pull-up terminating resistor networks
M68MM01-2	Basic Monoboard Microcomputer 1 Module with 4 connectors and three 330/220 pull-up/ pull-down terminating resistor networks

M68MM01A

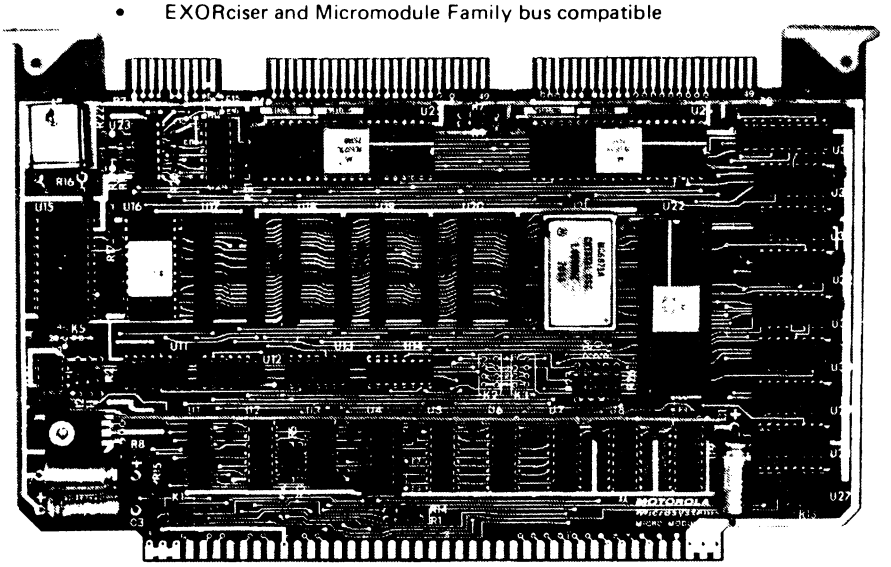
MONOBOARD MICROCOMPUTER 1A

MICROMODULE 1A

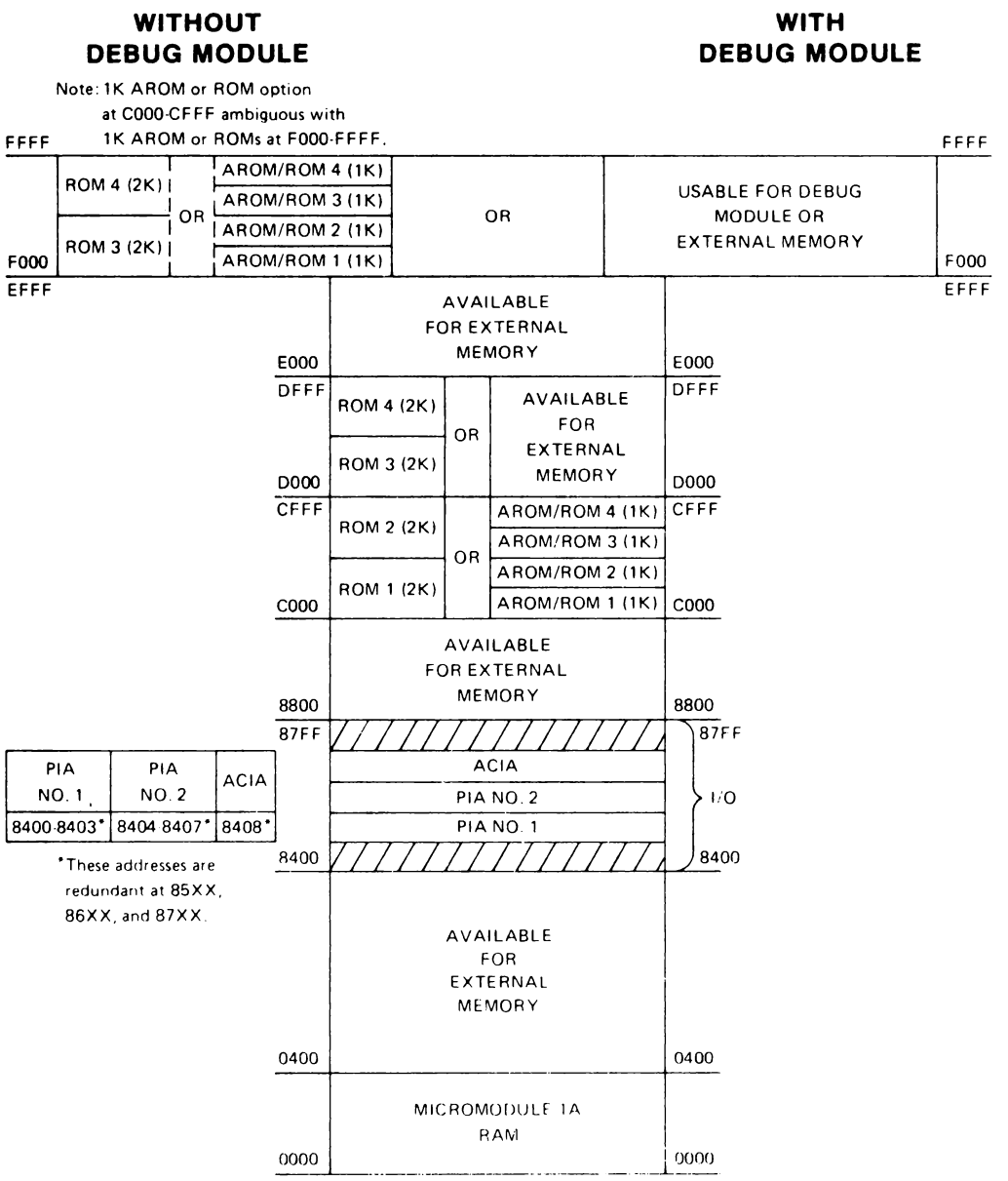
The M68MM01A Monoboard Microcomputer 1A — Micromodule 1A — is a complete computer-on-a-board that provides all of the processing and control power required for a microcomputer-based system, including one RS-232C serial input/output interface and two parallel input/output interfaces. Micromodule 1A incorporates an MC6800 MPU (Microprocessing Unit), 1K byte of static RAM for temporary program (scratch) storage, sockets for installing up to four 1K AROM or ROM (or 2K ROM) devices used to store firmware programs; one MC6850 ACIA with RS-232C interface for exchanging serial asynchronous data, and two MC6820 PIAs for exchanging parallel data.

FEATURES

- Complete microcomputer on a board
- MC6800 Microprocessing Unit (MPU)
- One MC6850 Asynchronous Communications Interface Adapter (ACIA) with RS-232C interface
- Two MC6820 Peripheral Interface Adapters (PIAs)
- 1 MHz crystal controlled clock
- 1K byte static Random Access Memory (RAM)
- Sockets for four 1K AROM or ROM (or 2K ROM) firmware program memories
- On-board reset circuitry
- Dynamic memory refresh circuitry
- 59K or 55K bytes of unused addresses available (depending on the type of ROM selected)
- EXORciser and Micromodule Family bus compatible



MEMORY MAP


WITHOUT DEBUG MODULE
WITH DEBUG MODULE
Note: 1K AROM or ROM option at C000-CFFF ambiguous with 1K AROM or ROMs at F000-FFFF.
FFFF
F000
EFFF
ROM 4 (2K)
ROM 3 (2K)
OR
AROM/ROM 4 (1K)
AROM/ROM 3 (1K)
AROM/ROM 2 (1K)
AROM/ROM 1 (1K)
OR
USABLE FOR DEBUG MODULE OR EXTERNAL MEMORY
AVAILABLE FOR EXTERNAL MEMORY
E000
DFFF
D000
ROM 4 (2K)
ROM 3 (2K)
OR
AVAILABLE FOR EXTERNAL MEMORY
CFFF
C000
ROM 2 (2K)
ROM 1 (2K)
OR
AROM/ROM 4 (1K)
AROM/ROM 3 (1K)
AROM/ROM 2 (1K)
AROM/ROM 1 (1K)
AVAILABLE FOR EXTERNAL MEMORY
8800
87FF
8400
ACIA
PIA NO. 2
PIA NO. 1
I/O
PIA NO. 1
PIA NO. 2
ACIA
8400-8403*
8404-8407*
8408*
*These addresses are redundant at 85XX, 86XX, and 87XX.
AVAILABLE FOR EXTERNAL MEMORY
0400
MICROMODULE 1A RAM
0000

GENERAL DESCRIPTION

Micromodule 1A incorporates a two-phase clock generator consisting of a single MC6871 crystal controlled clock, operating at a frequency of 1 MHz, that provides a two-phase NMOS clock to the MPU, a single TTL-compatible $\phi 2$ clock used for synchronizing data transfers, and a single ungated memory clock and memory ready control for refreshing external memories. The power-on reset circuitry provides reset control for the MPU and is also available for external use via the control bus.

On-board buffers and controls for address, data, and control bus signals allow Micromodule 1A to be interfaced with other members of the Micromodule Family or with the EXORciser. The 59K or 55K of addresses not allocated for on-board use (the allocation amount depends upon whether 1K AROM/ROM devices or 2K ROM devices are used for program storage) are available for system expansion. These addresses may be used for RAM and/or ROM, input/output expansion, or addressable peripherals.

Since Micromodule 1A only partially decodes the 16-bit MPU address bus to recognize on-board RAM, ROM, PIA, and ACIA addresses, certain blocks of addresses become ambiguous. Other address areas also become unavailable when Micromodule 1A is used in conjunction with the EXORciser's Debug Module. To illustrate the total addressability of Micromodule 1A, a memory map of this module has been included in this data sheet.

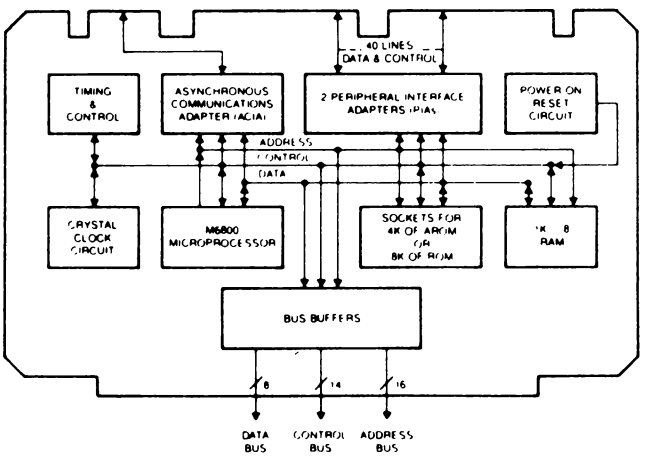
The ACIA and its associated RS-232C interface circuit provides an asynchronous serial data port for communicating with RS-232C compatible peripherals. Provision is made for on-board selection of one of four baud rates: 9600, 1200, 300, and 110. Micromodule 8A, a monitor/debug ROM, is available to aid the user in debugging his hardware and software.

The 40 input/output/control lines provided by the two PIAs for parallel interfacing are grouped by function as follows:

32 data lines that may be programmed for use as either inputs or outputs

4 interrupt inputs with programmable active transitions

4 lines selectable as either interrupt inputs or peripheral control outputs



SPECIFICATIONS

Power Requirements	+5 Vdc @ 1.1 A (max) +12 Vdc @ 20 mA (max) -12 Vdc @ 25 mA (max)
With four AROMs	+5 Vdc @ 1.3 A (max) +12 Vdc @ 260 mA (max) -12 Vdc @ 180 mA (max)
Micromodule Bus	
Address Bus	Three-state TTL-compatible buffered output
Control Bus	
R/W, VMA	Three-state TTL-compatible buffered output
Other Control Signals	TTL-compatible
Data Bus	
Input	TTL-compatible buffered input
Output	Three-state TTL-compatible buffered output
I/O (PIA signals)	
PA0-PA7, CA1 and CA2	TTL-compatible
PB0-PB7, CB1 and CB2	TTL-compatible with pull-up interface termination
I/O (ACIA signals)	RS-232C Compatible
Operating Temperature	0° to 70° C
Physical Characteristics	
Width	9.75 in.
Height	6.000 in.
Board Thickness	0.062 in.
Connectors	
86-Pin Connector	Stanford Applied Engineering SAC-43D/1-2 or equivalent
50-Pin Connector	3M type 3415-0001 or equivalent
20-Pin Connector	3M type 3461-0001 or equivalent

Specifications are subject to change without notice.

PRODUCT ORDERING INFORMATION

The following table identifies the options of the Monoboard Microcomputer 1A. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM01A	Basic Monoboard Microcomputer 1A
M68MM01A1	Basic Monoboard Microcomputer 1A with four connectors

M68MM01B MICROMODULE

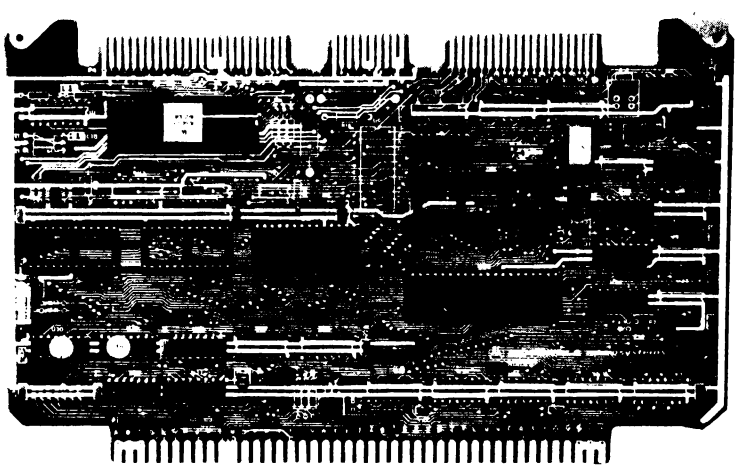
MONOBOARD MICROCOMPUTER

MICROMODULE 1B

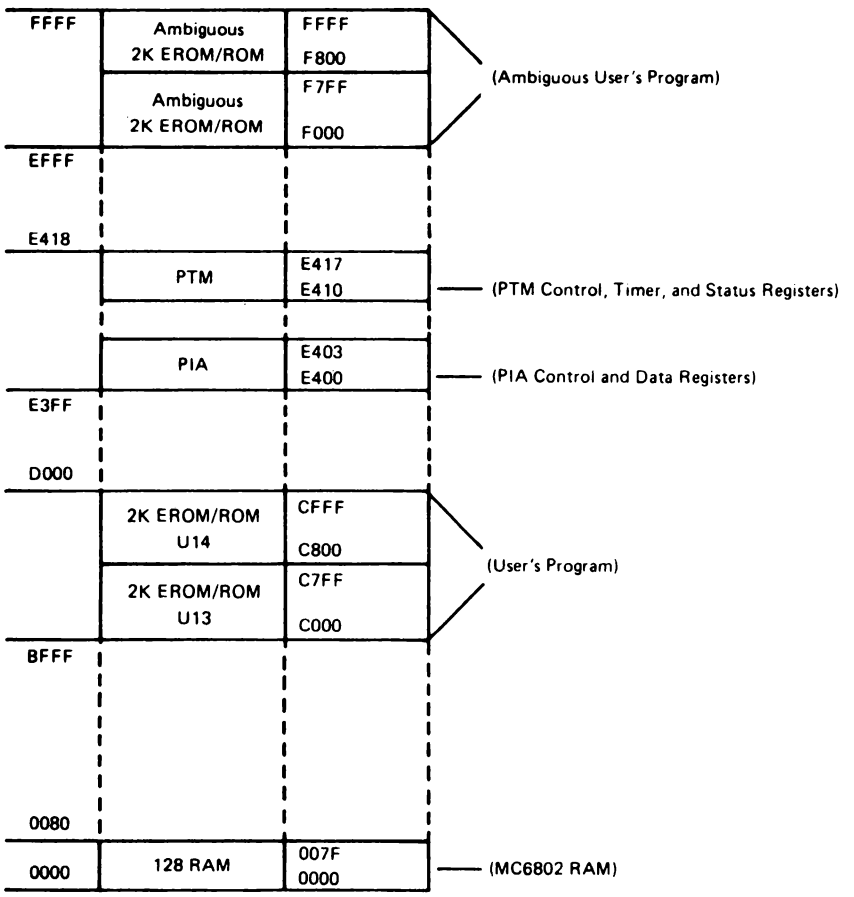
The M68MM01B Monoboard Microcomputer—Micromodule 1B – is a complete computer-on-a-board. The module incorporates the MC6802 MPU with a crystal clock, one MC6821 PIA providing two parallel I/O ports, one MC6840 triple 16-bit Programmable Timer/Clock, sockets for mounting two 2K EROM devices, and address decoding logic.

FEATURES

- Power-on restart
- Single +5V power supply
- 20 programmable I/O lines (MC6821 PIA)
- Three 16-bit programmable counter/timers (MC6840 PTM)
- Full compatibility with MC6800 software
- 128 bytes read/write static RAM
- Sockets for 4K bytes EROM/ROM program



MEMORY MAP


FFFF
Ambiguous 2K EROM/ROM
FFFF
F800
Ambiguous 2K EROM/ROM
F7FF
F000
(Ambiguous User's Program)
EFFF
E418
PTM
E417
E410
(PTM Control, Timer, and Status Registers)
PIA
E403
E400
(PIA Control and Data Registers)
E3FF
D000
2K EROM/ROM U14
CFFF
C800
2K EROM/ROM U13
C7FF
C000
(User's Program)
BFFF
0080
0000
128 RAM
007F
0000
(MC6802 RAM)

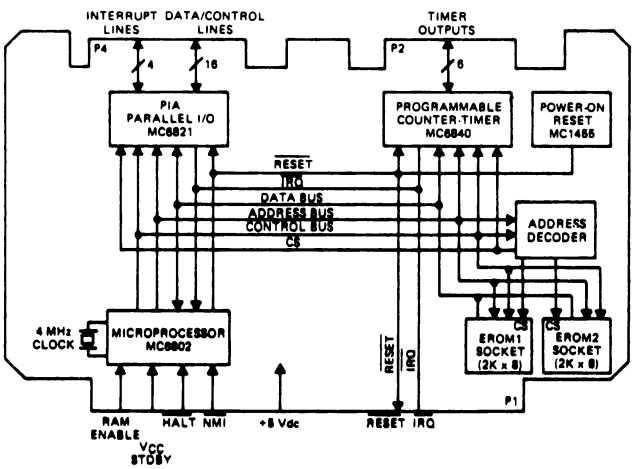
GENERAL DESCRIPTION

An MC1455 timing device, operated as a monostable multivibrator (one-shot) functions as a restart circuit that generates a low-level RESET signal after power is initially applied to Micromodule 1B. A valid RESET signal (one whose duration is > 8 MPU clock periods) causes the MPU to execute an initialization routine clearing all registers in the PIAs to logic zero (low) so that the PIAs may be configured. The RESET signal also presets the PTM latches and counters to their maximal count values, disables the counter clocks, clears the status register interrupt flags, and sets the control register internal reset bit which holds all timers in their preset state. Alternatively, an external RESET command may be applied to Micromodule 1B via connector P1.

A buffered 4 MHz crystal oscillator circuit provides the clock input to the MC6802 MPU. A divide-by-four circuit in the MPU generates the required two-phase MPU clock and the 1 MHz phase-two external clock for the rest of the system.

The Micromodule 1B data bus is used to transfer data between the MPU and various on-board devices (EROM/ROM, PIA, and PTM). Data transfers to the on-chip MPU RAM are handled within the chip.

The Micromodule 1B address bus is used to select the memory locations within the Micromodule board. A partially decoded addressing scheme is used to uniquely address each on-board EROM/ROM, PIA, and PTM. The addressing of the on-chip RAM is handled within the chip. The EROM/ROM, PIA, and PTM devices are selected by means of an address decoder circuit. The circuit consists of a pre-patterned PROM and PC board interconnections. The PROM decodes address bits A10 through A15 with one output used to select the PIA and PTM, one output to select EROM1, and one output to select EROM2.



SPECIFICATIONS

Power Requirements	+5 Vdc @ 350 mA
with EROMs	+5 Vdc @ 450 mA
System Clock	1 MHz ±0.1%
Word Size	
Instruction	8, 16, or 24 bits
Data	8 bits
Memory Addressing	
RAM	0000-007F
EROMs (sockets)	C000-CFFF or F000-FFFF
I/O-Timers	E400-E7FF
Parallel I/O	
16 Bidirectional programmable lines	
4 Bidirectional programmable lines or interrupts	
Interrupts	Vectored through software
Timers Input Frequency	1 MHz internal or asynchronous external gate/trigger inputs
Timers Operating Modes	Continuous (square wave) Single shot Frequency comparison Pulse/Width comparison
Physical Characteristics	
Width	9.75 in.
Height	6.00 in.
Board Thickness	0.062 in.
Connectors	
Microsystem Bus (P1)	
86-Pin	Stanford Applied Engineering SAC-43D/1-2 or equivalent
Parallel I/O Port (P4)	
50-Pin	3M type 3415-0001 or equivalent
Programmable Timers (P2)	
40-Pin	3M type 3464-0001 or equivalent

PRODUCT ORDERING INFORMATION

PART NO.	DESCRIPTION
M68MM01B	Basic Monoboard Microcomputer 1B
M68MM01B(D)	Monoboard Microcomputer 1B User's Guide

M68MM01B1 MICROMODULE

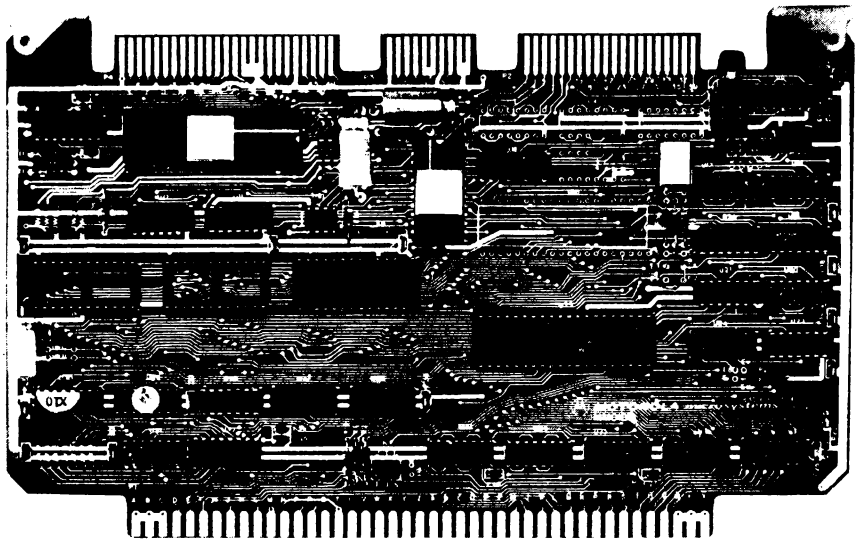
MONOBOARD MICROCOMPUTER 1B1

MICROMODULE 1B1

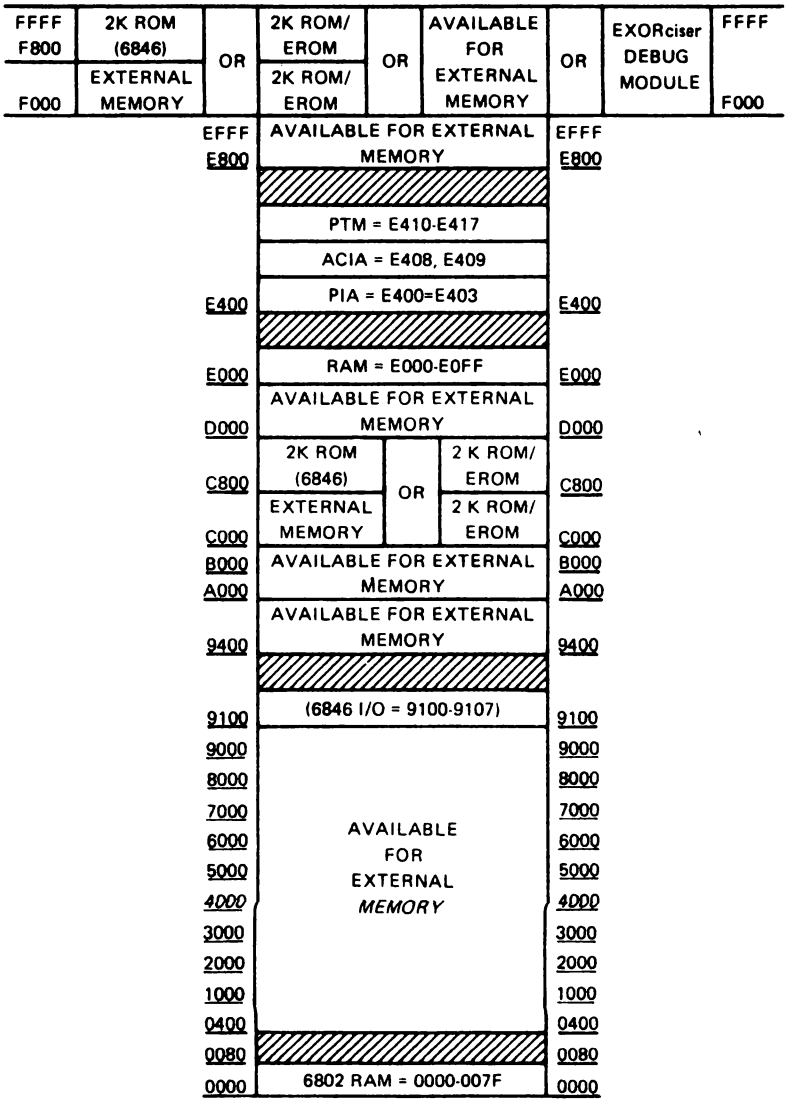
The M68MM01B1 Monoboard Microcomputer – Micromodule 1B1 – is a complete computer-on-a-board. The module incorporates the MC6802 with crystal clock, one MC6821 Peripheral Interface Adapter providing two parallel I/O ports, an MC6850 ACIA with RS-232C interface port, one MC6840 Triple 16-bit Programmable Timer Clock, sockets for mounting two 2K EROM devices, 384 bytes of RAM, and the bus buffers to interface with the Micromodule bus.

FEATURES

- Complete Microcomputer on a Single Board
- MC6802 Microprocessing Unit with 128 bytes on Chip Static RAM
- On Board Crystal Controlled Clock
- Sockets for up to 4K of Erasable/Programmable ROM
- 256 bytes of Read/Write Static RAM
- Power-on Reset
- 20 Programmable I/O Lines (MC6821 PIA)
- Three 16-bit Binary Programmable Timers (MC6840 PTM)
- Serial I/O Interface with RS-232C Drivers/Receivers and Software Programmable Baud Rate (110, 300, 1200, or 2400)
- Audio Tape Cassette Interface Circuitry
- Dynamic RAM Refresh Logic
- Buffered Address, Control, and Data Bus
- Full Compatibility with MC6800 Software, with Micromodule Family of Parts, and with Motorola EXORciser



MEMORY MAP


FFFF F800
2K ROM (6846)
OR
2K ROM/ EROM
OR
AVAILABLE FOR EXTERNAL MEMORY
OR
EXORciser DEBUG MODULE
FFFF F000
F000
EXTERNAL MEMORY
2K ROM/ EROM
EFFF
E800
AVAILABLE FOR EXTERNAL MEMORY
PTM = E410-E417
ACIA = E408, E409
E400
PIA = E400=E403
E000
RAM = E000-E0FF
AVAILABLE FOR EXTERNAL MEMORY
D000
2K ROM (6846)
EXTERNAL MEMORY
2 K ROM/ EROM
C800
C000
B000
AVAILABLE FOR EXTERNAL MEMORY
A000
9400
9100
(6846 I/O = 9100-9107)
9000
8000
7000
6000
5000
4000
3000
2000
1000
0400
AVAILABLE FOR EXTERNAL MEMORY
0080
0000
6802 RAM = 0000-007F

GENERAL DESCRIPTION

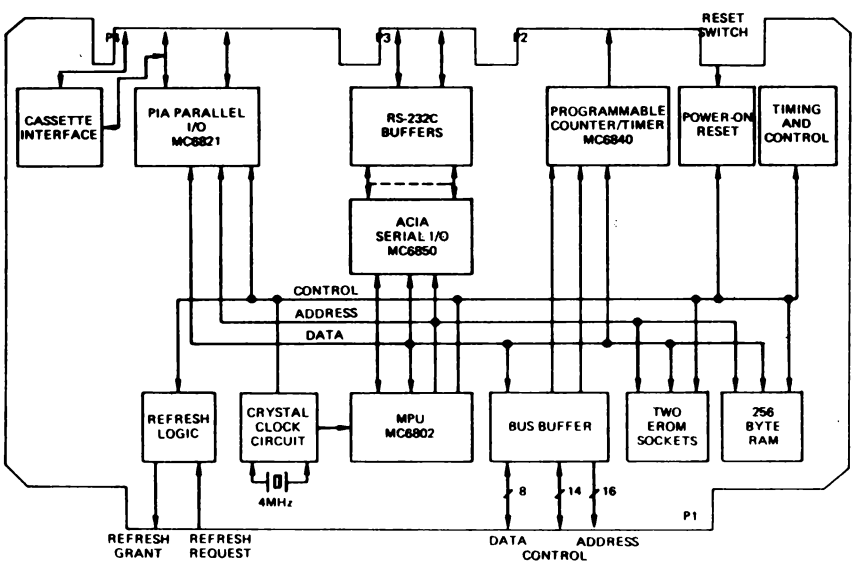
Monoboard Microcomputer 1B1 provides the user with a stand-alone microcomputer that has all the processing and control power of an MC6802 MPU with its self-contained clock circuit and 128 bytes of static RAM. The module contains sockets for up to 4K of EROM or ROM for programming, a Peripheral Interface Adapter (PIA) for parallel data transfers, and a Programmable Timer Module (PTM) which provides for such tasks as frequency measurements, event counting, interval measuring, square wave generation, gated delay signals, single pulses of controlled duration, pulse width modulation, and timed system interrupts. The module incorporates the necessary crystal clock circuits, the reset timer for power-on initialization, and address bus decoding for establishing the address of each part.

In addition to these features, the module has an additional 256 bytes of static RAM, provisions for off-board dynamic memory refresh, as Asynchronous Communications Interface Adapter (ACIA) with RS-232C interface circuits, and an Audio Tape Cassette interface circuit.

The Micromodule 1B1 address bus is used to select each of the memory locations within a Micromodule system. Micromodule 1B1 uses a partially decoded addressing scheme to uniquely address each on-board EROM/ROM, RAM, PIA, ACIA, and PTM. The address bus interface consists of three-state buffers.

The Micromodule 1B1 data bus is used to perform data transfers between the MPU and various devices (EROM, ROM, RAM, PIA, and ACIA). For greater memory and I/O capacity, additional devices can be added external to the Monoboard.

Monoboard Microcomputer 1B1 is also bus compatible with the M6800 EXORciser. This versatility provides the user with the means to develop and debug both his hardware and software, and to troubleshoot production hardware. Thus, the user can take advantage of the EXORciser's optional debug, memory, and I/O modules.



SPECIFICATIONS

Power Requirements	+5 Vdc @ 550 mA
	+12 Vdc @ 20 mA
	−12 Vdc @ 25 mA
with EROM's	+5 Vdc @ 650 mA
	+12 Vdc @ 260 mA
	−12 Vdc @ 180 mA
System Clock	1 MHz ± .1%
Word Size	
Instruction	8, 16, or 24 bits
Address	16 bits
Data	8 bits
Memory Addressing	
RAM (128 bytes)	0000-007F
RAM (256 bytes)	E000-E3FF
EROM's (sockets)	C000 to CFFF or F000 to FFFF or AMBIG C000/F000
PIA-ACIA-PTM	E400 to E7FF
Parallel I/O	
16 bidirectional programmable lines	
4 I/O control lines and/or interrupts	
Interrupts	Vectored through software
Timer Input Frequency	1 MHz, internal or asynchronous external gate/trigger inputs
Timer Operating Modes	Continuous (square wave)
	Single shot
	Frequency comparison
	Pulse/width comparison
Physical Characteristics	
Width	9.75 in.
Height	6.00 in.
Board Thickness	0.062 in.
Connectors	
Microsystem bus (P1)	
86 pin	Stanford Applied Engineering SAC-43D/1-2 or equivalent
Programmable Timers (P2)	
40 pin	3M Type 3464-0001 or equivalent
Serial I/O port (P3)	
20 pin	3M Type 3461-0001 or equivalent
Parallel I/O Port (P4)	
50 pin	3M Type 3415-0001 or equivalent

PRODUCT ORDERING INFORMATION

Use the following part numbers when ordering the Monoboard Microcomputer-Micromodule 1B1 and its associated technical manual. For further information, contact your local sales office.

Part No.	Description
M68MM01B1	Monoboard Microcomputer 1B1
M68MM01B(D)	Monoboard Microcomputer 1B Manual

MOTOROLA

M68MM02

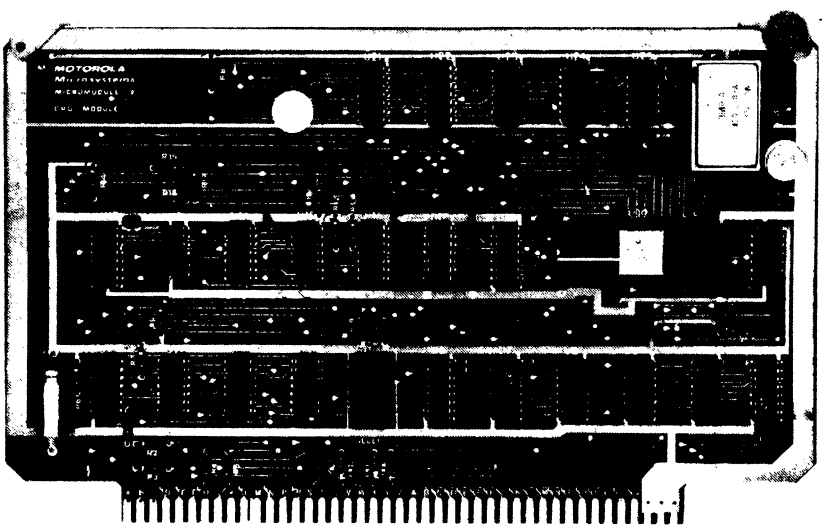
CENTRAL PROCESSING UNIT (CPU)

MICROMODULE 2

The M68MM02 CPU (Central Processing Unit) Module – Micromodule 2 – is the prime building block of a totally modular microcomputer system. Micromodule 2 combines all of the processing and control power of an MC6800 Microprocessor with the necessary two-phase clock generator, the reset circuitry for power turn-on initialization, and the bus interface and control circuitry needed to satisfy the basic requirements of a microcomputer system. In addition, Micromodule 2 contains the timing, priority, and refresh controls for three-state and halt (DMA) operations and memory refresh.

FEATURES

- MC6800 Microprocessing Unit (MPU)
- 1 MHz crystal controlled clock
- On-board reset circuitry
- Timing and control for three-state and halt (DMA) operations and memory refresh
- User selectable top of memory address
- EXORciser and Micromodule Family bus compatible



GENERAL DESCRIPTION

Micromodule 2 contains a two-phase clock generator consisting of an MC6871 crystal *controlled clock, operating at a frequency* of 1 MHz, that provides a two-phase NMOS clock to the MPU, a single TTL-compatible $\phi 2$ clock used for synchronizing data transfers, and a single ungated memory clock and memory ready control for use with low speed memories. The $\phi 1$ NMOS clock, $\phi 2$ TTL clock, and the memory clock and ready control are available for external use by the system via the control bus. The on-board reset circuitry provides power-on reset control for the MPU and is also available for external use. Timing and control circuitry synchronizes three-state control and halt with the $\phi 1$ clock and synchronizes refresh operations with the memory clock. The timing and control circuitry also provides three-state control for address, data, and control buses.

The CPU Module provides the capability of selecting the top of memory address location. This selection is accomplished in 4K-byte increments by installing on- or off-board jumpers that modify address select bits A12 through A15 (the bits used to address the top of memory locations). An address select socket with component platform provides an easy-to-use method of installing on-board jumper connections if desired. Otherwise, wirewrap pins located on the Micromodule motherboard may be used to install these connections off-board. As delivered, no jumper connections are installed; thus, the top of memory address is FFFF.

Regardless of whether or not the jumper connections have been installed to select the top of memory address location, the CPU Module and other modules within the microcomputer system may be installed in an EXORciser, permitting the system to be debugged using the EXbug Firmware on the EXORciser Debug Module. (The EXbug Firmware requires the use of memory locations F000 through FFFF.) When used in this manner, on-board decoding logic associated with the top of memory addressing circuitry automatically controls the top of memory address selection. When Micromodule 2 is not being used with the Debug Module, this same on-board decoding logic is used to modify the MC6800 MPU's vectoring addresses located at FFF8 through FFFF to the top of memory address location that has been selected (XFF8 through XFFF).

Micromodule 2 is not only compatible with the Micromodule Family, but also with the M6800 EXORciser. This versatile design tool provides a system to develop and debug the hardware/software system and to troubleshoot production hardware. Advantage can also be taken of the EXORciser's AROM/PROM programming capability and optional memory and I/O modules.

SPECIFICATIONS

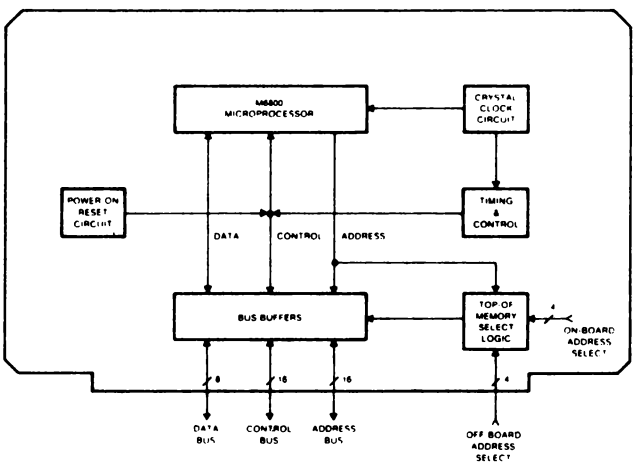
Power Requirements	+5 Vdc ± 5% @ 1A
Micromodule Bus Signals	
Address Bus	Three-state TTL-compatible buffered output
Data Bus	
Input	TTL-compatible buffered input
Output	Three-state TTL-compatible buffered output
Control Bus	
R/W, VMA, VUA	Three-state TTL-compatible buffered output
BA, REF GRANT, and TSC GRANT	TTL-compatible buffered output
IRQ, NMI, RESET, HALT	TTL-compatible buffered inputs with 4.7K
REF REQ, and TSC	ohm pull-up resistors
ϕ1 and ϕ2 Clocks	TTL-compatible buffered output with 10 ohms series impedance
Operating Temperature	0° to 70° C
Physical Characteristics	
Width X Height	9.75 in. X 6.000 in.
Board Thickness	0.062 in.
Connector	Stanford Applied Engineering SAE-43D/1-2

Specifications are subject to change without notice.

PRODUCT ORDERING INFORMATION

Use the following part number when ordering the CPU Module – Micromodule 2.

PART NO.	DESCRIPTION
M68MM02	CPU MODULE



MOTOROLA

M68MM03

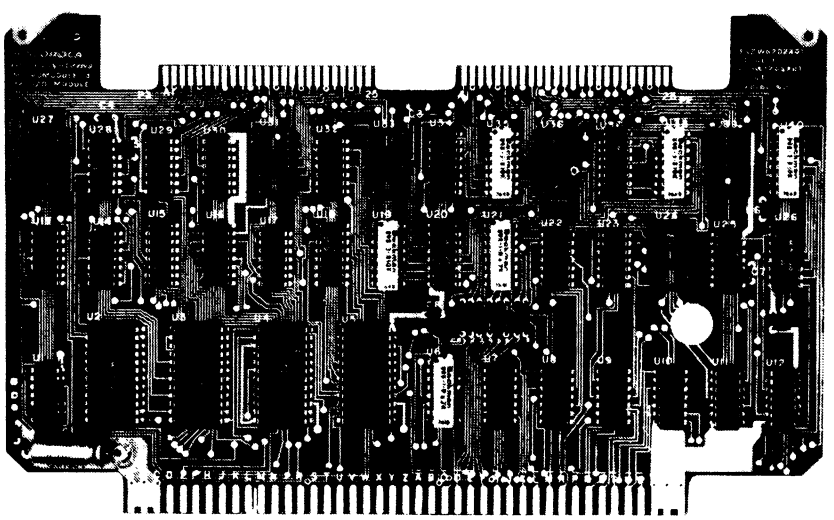
32/32 INPUT/OUTPUT MODULE

MICROMODULE 3

The M68MM03 32/32 Input/Output Module – Micromodule 3 – provides 32 TTL-compatible parallel inputs and 32 TTL-compatible latched and buffered parallel outputs. These 32 inputs and 32 outputs provide the means of transferring four contiguous 8-bit bytes of parallel data between the microcomputer and the external system. Thus, by using the M6800 MPU's (Microprocessing Unit's) index register, all 32 input bits can be read and stored in 20 machine cycles, while only 18 machine cycles are required to load and latch the 32 output bits. Micromodule 3 may be ordered with the TTL-compatible inputs and latched TTL-compatible buffered outputs having no terminating resistors, with 4.7 K ohm pull-up terminating resistors, or with 330/220 ohm pull-up/pull-down terminating resistors.

FEATURES

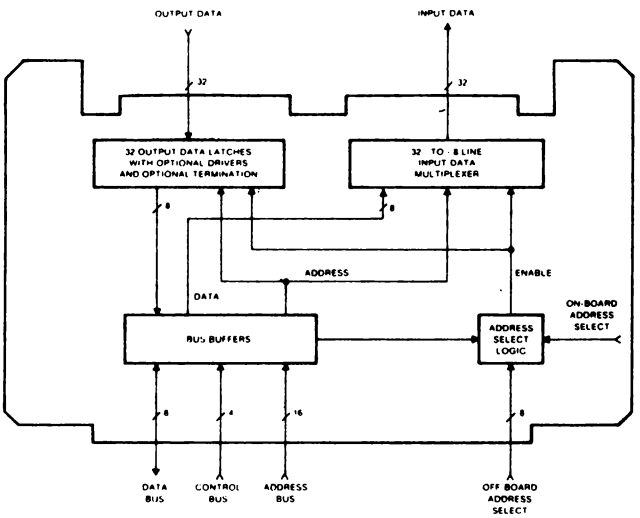
- 32 bits of parallel input in four contiguous 8-bit bytes
- 32 bits of latched and buffered parallel output in four contiguous 8-bit bytes
- User selectable input/output terminations
- User selectable base memory address
- EXORciser and Micromodule Family bus compatible



GENERAL DESCRIPTION

The base memory address can be selected in 4 byte increments from 8E00 to 8FFC and 9E00 to 9FFC by installing on- or off-board jumper connections that modify address select bits A2 through A8 and A12. This permits a maximum of 256 Micromodule 3's to be used in a Micromodule-based system (providing a maximum of 8192 input and 8192 output bits). An address select socket with component platform provides an easy-to-use method of installing the jumper connections on-board if desired. Otherwise, wirewrap pins located on the Micromodule motherboard may be used to install these connections off-board. As delivered, no jumpers are installed, automatically assigning the module address at 9FFC.

Micromodule 3 is not only bus compatible with the Micromodule Family, but also with the M6800 EXORciser. This versatile design tool provides a system to develop and debug hardware/software systems and to troubleshoot production hardware. Advantage can also be taken of the EXORciser's AROM/PROM programming capability and optional memory modules.



SPECIFICATIONS

Power Requirements	+5 Vdc ± 5% @ 800 mA (nominal)
Interface Signals	
Input Signals	TTL-compatible with optional terminations available (4.7 K ohm pull-up or 330/220 ohm pull-up/pull-down)
Output Signals	Latched TTL-compatible open collector with optional terminations available (4.7 K ohm pull-up or 330/220 ohm pull-up/pull-down)
Base Address Selection	Addressable in 4 byte increments from $8E00_{16}$ to $8FFC_{16}$ and $9E00_{16}$ to $9FFC_{16}$. Delivered modules are preaddressed to $9FFC_{16}$.
Micromodule Bus Signals	
Address Bus	TTL-compatible buffered input
Data Bus	
Input	TTL-compatible buffered input
Output	Three-state TTL-compatible buffered output
Control Bus	TTL-compatible buffered input
Operating Temperature	0° to 70° C
Physical Characteristics	
Width X Height	9.75 in. X 6.000 in.
Board Thickness	0.062 in.
Connector	
86-Pin Bus Connector	Stanford Applied Engineering SAE-43D/1-2 or equivalent
50-Pin Input/Output Connectors	Viking 3VH25/1JN5, 3M 3415-0001, or equivalent

Specifications are subject to change without notice.

PRODUCT ORDERING INFORMATION

Use the part number listed below when ordering the 32/32 I/O Module or one of its optional configurations.

PART NO.	DESCRIPTION
M68MM03	Basic 32/32 Input/Output Module with no terminations
M68MM03-1	Basic 32/32 Input/Output Module with 4.7 K ohm pull-up termination resistors
M68MM03-2	Basic 32/32 Input/Output Module with 330/220 ohm pull-up/pull-down termination resistors

MOTOROLA

M68MM04

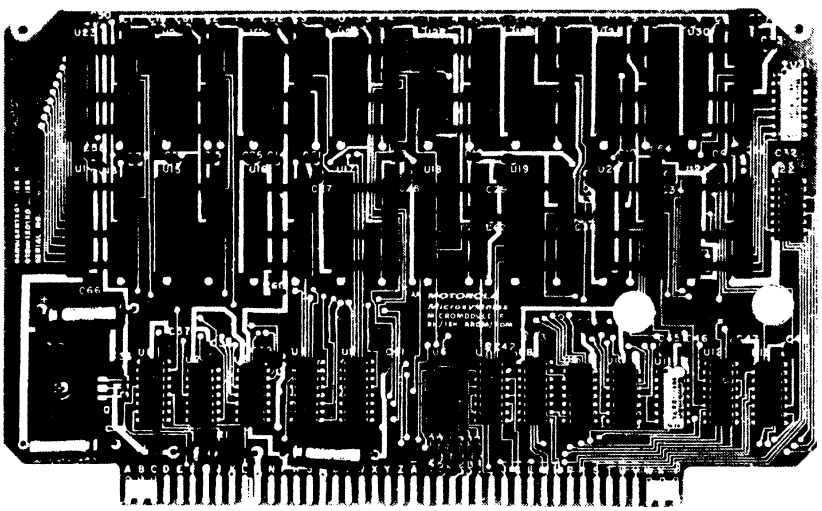
8K/16K AROM/ROM MODULE

MICROMODULE 4

The M68MM04 8K/16K AROM/ROM Module – Micromodule 4 – incorporates provisions for installing up to 8K or 16K bytes of AROM or ROM memory used to store firmware programs for a Micromodule-based system. Depending upon the option selected, Micromodule 4 provides either eight or sixteen sockets for mounting MCM68708 AROM devices or MCM68308 ROM devices.

FEATURES

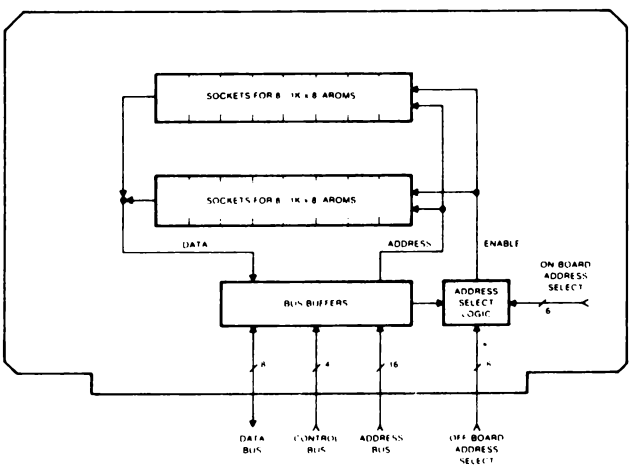
- Sockets for up to sixteen 1K X 8 bit AROM or ROM devices
- User selectable base memory address for each 8K memory block
- EXORciser and Micromodule Family bus compatible



GENERAL DESCRIPTION

The AROM/ROM memory section of this module is organized into two memory blocks, each containing eight sockets. (The 8K version of Micromodule 4 has only one memory block.) The only preparation required to use this module is to install your programmed AROM and/or ROM devices into the appropriate sockets and select the base memory address for each memory block. The base memory address for each memory block can be selected over the range of 0000_{16} to $E000_{16}$ in 8K byte increments by installing an on- or off-board jumper connection that modifies address select bits A13 through A15. An address select socket with component platform provides an easy-to-use method of installing on-board jumper connections if desired. Otherwise, wirewrap pins located on the Micromodule motherboard may be used to install these connections off-board. As delivered, the base memory addresses for the memory blocks are assigned $A000_{16}$ and $C000_{16}$ (only address $A000_{16}$ is assigned on the 8K version of this module). When reassigning the base memory address on the 16K version, avoid overlapping the addresses of each memory block.

Micromodule 4 is not only bus compatible with the Micromodule Family, but also with the M6800 EXORciser. This versatile design tool provides a system to develop and debug a hardware/software system and to troubleshoot production hardware. Advantage can also be taken of the EXORciser's AROM/PROM programming capability and optional memory and I/O modules.



SPECIFICATIONS

Power Requirements	
With 8 AROMs Installed	+5 Vdc ± 5% @ 430 mA +12 Vdc ± 5% @ 520 mA (max) -12 Vdc ± 5% @ 360 mA (max)
With 16 AROMs Installed	+5 Vdc ± 5% @ 520 mA +12 Vdc ± 5% @ 1040 mA (max) -12 Vdc ± 5% @ 720 mA (max)
Memory Size	
8K Option	Sockets for mounting up to eight MCM68708 AROMs or MCM68308 ROMs
16K Option	Sockets for mounting up to sixteen MCM68708 AROMs or MCM68308 ROMs
Memory Organization	16K bytes memory capability consisting of two 8K byte memory blocks. (The 8K option has only one memory block.)
Base Address Selection	Each memory block is jumper addressable in 8K byte increments from 0000_{16} to $E000_{16}$. Delivered modules are preaddressed to $A000_{16}$ (8K and 16K options) and $C000_{16}$ (16K option only).
Micromodule Bus	
Address Bus	TTL-compatible buffered input
Data Bus (Outputs Only)	Three-state TTL-compatible buffered output
Control Bus	TTL-compatible buffered input
Operating Temperature	0° to 70° C
Physical Characteristics	
Width X Height	9.75 in. X 6.000 in.
Board Thickness	0.062 in.
Connector	
86-Pin Bus Connector	Stanford Applied Engineering SAE-43D/1-2 or equivalent

Specifications are subject to change without notice.

PRODUCT ORDERING INFORMATION

Use the part numbers listed below when ordering either configuration of the 8K/16K AROM/ROM Module.

PART NO.	DESCRIPTION
M68MM04	8K/16K AROM/ROM Module with sockets for 8K bytes of memory
M68MM04 1	8K/16K AROM/ROM Module with sockets for 16K bytes of memory

M68MM05A, B, C MICROMODULE

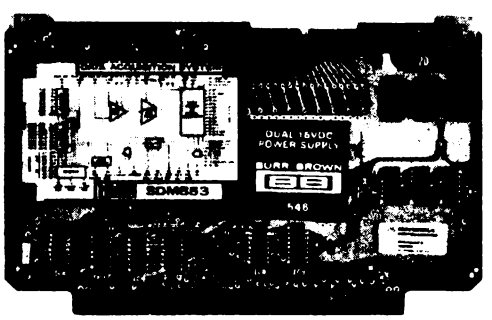
ANALOG I/O

MICROMODULE 5A, B, C

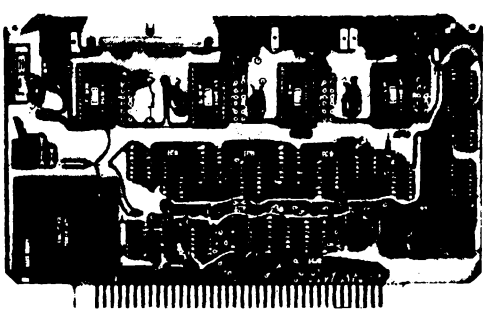
Micromodules M68MM05A, B, and C provide the user with the capability of Analog Data Acquisition (MM05A and B) and Analog Output (MM05C). The M68MM05A and M68MM05B provide 8 and 16 channels, respectively, of input analog-to-digital conversion while the M68MM05C provides 4 channels of output digital-to-analog conversions.

FEATURES

- Complete data acquisition system on a board (Micromodules 5A and 5B)
- Complete analog output system on a board (Micromodule 5C)
- 8 channel differential analog inputs (Micromodule 5A)
- 16 channel single-ended analog inputs (Micromodule 5B)
- 4 channel differential analog outputs (Micromodule 5C)
- High accuracy 12-bit resolution
- Full on-board address selection
- On-board dc/dc conversion (requires only +5 Vdc)
- Micromodule and EXORciser bus compatible



M68MM05B



M68MM05C

SPECIFICATIONS

	M68MM05A	M68MM05B
Analog Input		
Number Channels	8 differential	16 single-ended
Input range (strappable)	± 10 mV to ± 10 V	± 10 mV to ± 10 V
Gain range (resistor programmable)	1 to 1000 V/V	1 to 1000 V/V
Input Overvoltage	± 15 V	± 15 V
Input Impedance	100 Megohms	100 Megohms
Transfer Characteristics		
Resolution	12 bits binary	12 bits binary
Throughput Accuracy		
± 10 V Range	± 0.025% FSR	± 0.025% FSR
± 10 mV Range	± 0.01% FSR	± 0.1% FSR
Temperature Coefficient of Accuracy		
± 10 V Range	± 0.003% FSR/°C	± 0.003% FSR/°C
± 10 mV Range	± 0.01% FSR/°C	± 0.01% FSR/°C
CMRR (differential)	74 dB (dc to 2 kHz)	
Conversion Time (MPU is Halted)		
± 10 V Range	33 microseconds	33 microseconds
± 10 mV Range	100 microseconds	100 microseconds

	M68MM05C
Analog Outputs	4 Channels
Output Voltage Range (strappable)	± 10 V, ± 5V, ± 2.5 V, 0 to 10 V, 0 to 5 V
Output Impedance	1 ohm
Settling Time	Less than 10 microseconds
Transfer Characteristics	
Resolution	12 bits binary
Throughput Accuracy	± 0.0125% FSR
Temperature Coefficient of Accuracy	
Unipolar	± 0.003% FSR/°C
Bipolar	± 0.0045% FSR/°C

Physical Characteristics	
Height	9.75 in.
Width	6.00 in.
Board Thickness	0.062 in.
Connectors	
Microsystem bus	Stanford Applied Engineering SAC-43D/1-2 or equivalent
Input/Output ports	3M type 3417 or equivalent

PRODUCT ORDERING INFORMATION

The following table identifies the options of Micromodule 5. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM05A	Micromodule 5A – 8-channel, 12-bit differential input A/D converter module with interconnect cable assembly
M68MM05B	Micromodule 5B – 16-channel, 12-bit single-ended input A/D converter module with interconnect cable assembly
M68MM05C	Micromodule 5C – quad 12-bit D/A converter module with interconnect cable assembly

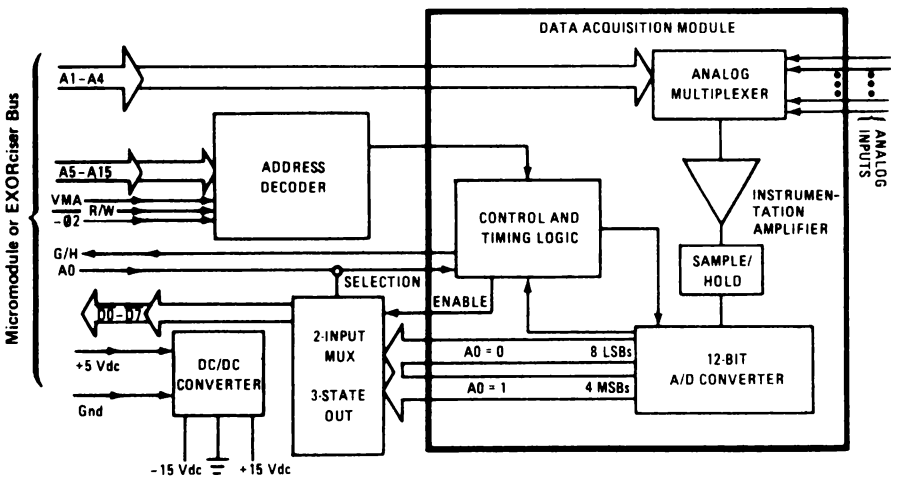
GENERAL DESCRIPTION

Micromodules 5A, B, and C microcomputer peripheral boards provide two necessary system interface functions: analog data acquisition (Micromodules 5A and 5B) and analog input (Micromodule 5C). Each analog system is completely contained on a single printed circuit board that is treated as a memory input and output. The analog input for each module is provided by a flat ribbon cable connector located at the opposite edge of the board from the system bus connector.

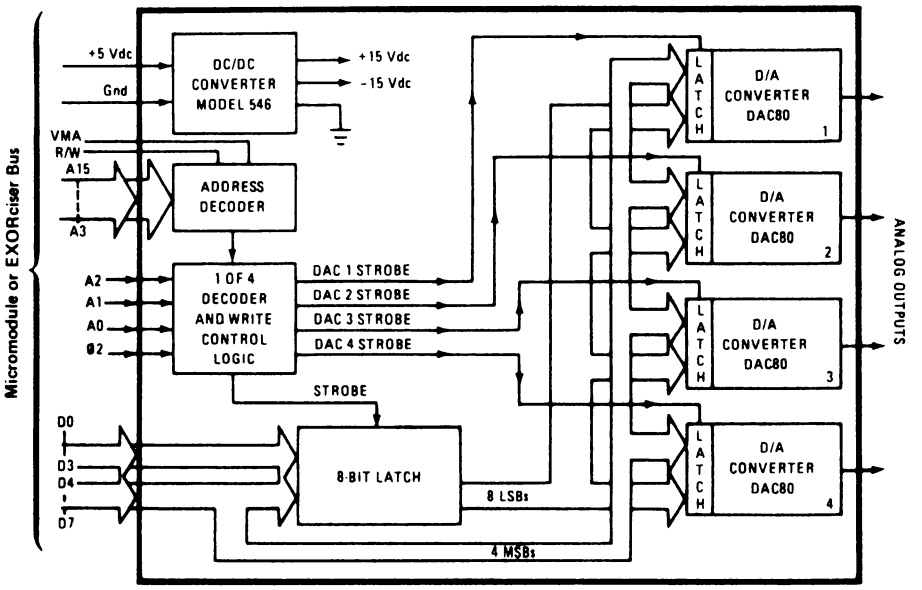
The analog data acquisition modules (Micromodules 5A and 5B) provide an 8-channel differential analog input or 16-channel single-ended analog input, respectively. A modular data acquisition system is used to implement both Micromodules. This modular data acquisition system includes an input multiplexer, a high gain instrumentation amplifier, a sample/hold circuit, and a 12-bit A/D converter. In addition, all of the necessary timing, decoding, and control logic is also included in each module. A dc/dc converter (+5 Vdc to ±15 Vdc) is also used to allow the use of the microcomputer's +5 Vdc power supply.

The analog output system (Micromodule 5C) provides four analog output channels. Each analog output is generated by separate on-board 12-bit D/A converters. The inputs to these D/A converters are double buffered so that a complete 12-bit word can be simultaneously loaded into the converter's input registers. A dc/dc converter (+5 Vdc to ±15 Vdc) is also used to allow the use of the microcomputer's +5 Vdc power supply.

MICROMODULE 5A, B - ANALOG INPUT



MICROMODULE 5C - ANALOG OUTPUT



MOTOROLA

M68MM06

2K STATIC RAM MODULE

MICROMODULE 6

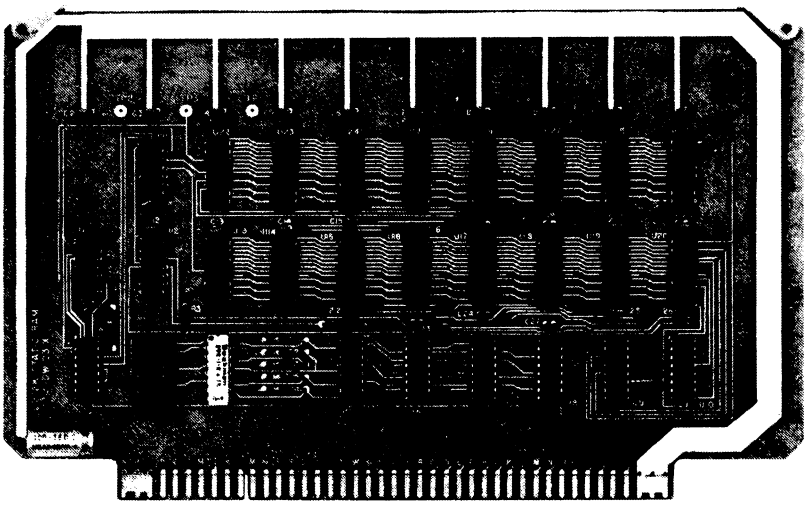
The M68MM06 2K Static RAM Module – Micromodule 6 – provides 2048 bytes of static random access memory for use in a Micromodule-based system.

The memory section of Micromodule 6 is organized into two 1K X 8-bit groups which appear to the system bus as 2048 contiguous address locations. The base address of Micromodule 6 can be assigned in 2K byte increments throughout the range of 0000_{16} to $F800_{16}$. *The base memory address can be selected by installing on- or off-board jumper* connections that modify address select bits A11 through A15. An address select socket with component platform provides an easy-to-use method of installing on-board jumper connections if desired. Otherwise, wirewrap pins located on the Micromodule motherboard may be used to install these connections off-board. As delivered, the base memory address is assigned 7800_{16}.

Micromodule 6 is not only bus compatible with the Micromodule Family, but also with the M6800 EXORciser. This versatile design tool provides a system to develop and debug the hardware/software system and to troubleshoot production hardware. Advantage can also be taken of the EXORciser's AROM/PROM programming capability and optional I/O modules.

FEATURES

- 2048 bytes of static random access memory
- User selectable base address
- EXORciser and Micromodule Family bus compatible



SPECIFICATIONS

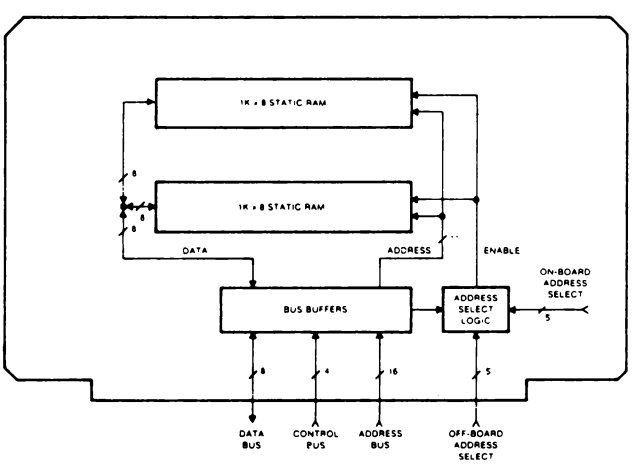
Power Requirements	+5 Vdc ± 5% @ 1.5 A (max)
Memory Size	2048 bytes of static random access memory
Memory Organization	Two 1K X 8-bit groups
Base Address Selection	Jumper selectable in 2K byte increments from 0000_{16} to $F800_{16}$. Delivered modules are preaddressed to 7800_{16}.
Micromodule Bus	
Address Bus	TTL-compatible buffered input
Data Bus	
Input	TTL-compatible buffered input
Output	Three-state TTL-compatible buffered output
Control Bus	TTL-compatible buffered input
Operating Temperature	0° to 70° C
Physical Characteristics	
Width X Height	9.75 in. X 6.000 in.
Board Thickness	0.062 in.
Connector	
86-Pin Bus Connector	Stanford Applied Engineering SAE-43D/1-2 or equivalent

Specifications subject to change without notice.

PRODUCT ORDERING INFORMATION

Use the part number listed below when ordering the 2K Static RAM Module.

PART NO.	DESCRIPTION
M68MM06	2K Static RAM Module



M68MM08, 8A
MICROMODULE
MICRObug MONITOR/DEBUG

MICROMODULE 8, 8A

Micromodule M68MM08/08A provides the users of Micromodules with a system software and hardware development and debugging capability. Micromodule MM08A is a firmware ROM containing the MICRObug monitor/debug functions, and is intended for use with Monoboard Microcomputer M68MM01A or M68MM01A2, which contains its own serial communications port. Micromodule MM08 consists of the MICRObug ROM and an MEX6850 Asynchronous Communications Interface Adapter (ACIA) module, and is intended for use with Micromodules MM01 or MM02.

FEATURES

- User-interactive program
- Provides 13 user commands as follows:
  - Load formatted tape
  - Open memory locations; display, change contents
  - Print/punch dump
  - Display MPU Register contents
  - Set communications speed
  - Set Breakpoints
  - Remove one Breakpoint
  - Remove all Breakpoints
  - Print all Breakpoints
  - Continue program from current location
  - Go to specified location and begin program execution
  - Execute next instruction only
  - Trace N instructions
- MICRObug source code listing provided
- Co-resident Assembler/Editor available (M68MAE6813)

ORDERING INFORMATION

The following table identifies the options of the MICRObug Monitor/Debug Micromodule. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM08	Consists of the MICRObug ROM and MEX6850 · · used with M68MM01 and M68MM02
M68MM08A	Consists of MICRObug ROM · · used with M68MM01A or M68MM01A2

MM08/8A DESIGN REFERENCE

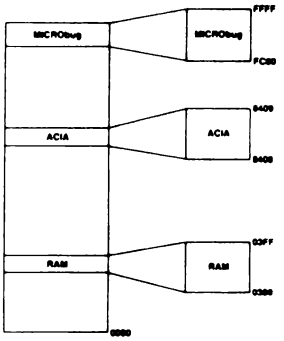
MICRObug COMMANDS

COMMAND		DESCRIPTION	COMMAND		DESCRIPTION
L		LOAD FORMATTED TAPE	T	XXXX	TRACE XXXX INSTRUCTIONS.
M	XXXX	OPEN MEMORY LOCATION XXXX	G	XXXX	GO TO LOCATION XXXX AND BEGIN EXECUTION.
P		PRINT/PUNCH DUMP.	D		DELETE ALL BREAKPOINTS
R		DISPLAY REGISTERS	U	XXXX	REMOVE BREAKPOINT AT XXXX.
SX		SET SPEED FOR FIRMWARE S1 = 10 CPS, S3 = 30 CPS	V	XXXX	SET A BREAKPOINT AT XXXX.
B		PRINT BREAKPOINTS	MICRObug PROMPT IS AN ASTERISK		
C		CONTINUE PROGRAM EXECUTION FROM CURRENT LOCATION.			
N		EXECUTE NEXT INSTRUCTION ONLY.			

USEFUL MICRObug ROUTINES

ADDRESS	DESCRIPTION
FC43	ENTER MICRObug SAME ENTRY AS RESET
FC66	ENTER MICRObug WITHOUT RESETTING ACIA AND TRACE CONSTANTS
FD26	OUTPUT ONE ASCII CHARACTER FROM 'A' REGISTER
FD33	INPUT ONE ASCII CHARACTER INTO 'A' REGISTER.
FD4B	OUTPUT DATA STRING POINTED TO BY THE INDEX REGISTER UNTIL TERMINATED BY '04' IN THE DATA STRING
FD96	OUTPUT FOUR HEX CHARACTERS POINTED TO BY THE INDEX REGISTER FOLLOWED BY A 'SPACE'
FD98	OUTPUT TWO HEX CHARACTERS POINTED TO BY THE INDEX REGISTER FOLLOWED BY A 'SPACE'
FE60	OUTPUT CR LF FOUR NULLS AND THE CONTENTS OF THE STACK
FE66	OUTPUT THE CONTENTS OF THE STACK

MICRObug MEMORY MAP



INTERRUPT VECTORS

THE USER CAN SET HIS OWN INTERRUPT VECTORS BY CHANGING THE CONTENTS OF THE FOLLOWING MEMORY LOCATIONS:

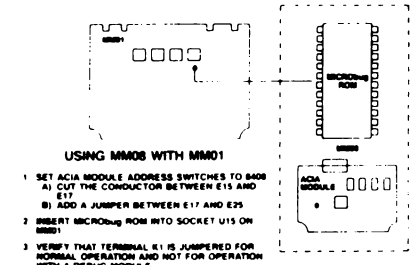
NMI	0386, 0387
IRQ	0380, 0381

PUNCH/PRINT ROUTINE

THE STARTING ADDRESS FOR THIS ROUTINE IS IN MEMORY LOCATIONS 0382, 0383; THE ENDING ADDRESS IS AT 0384,0385

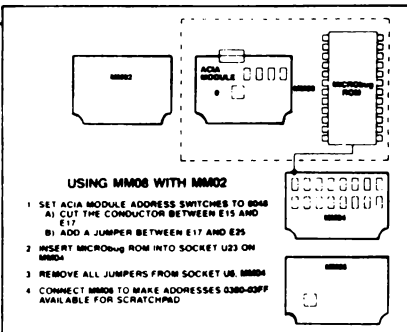
BE SURE THAT THE SELECTED BAUD RATE ON MM01A OR THE ACIA MODULE MATCHES THE BAUD RATE OF THE TERMINAL.

INSTALLING MICRObug



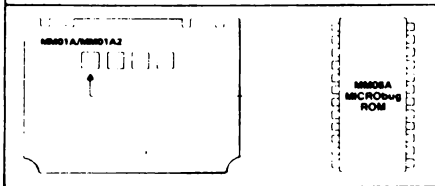
USING MM08 WITH MM01

1. SET ACIA MODULE ADDRESS SWITCHES TO 8408
   A) CUT THE CONDUCTOR BETWEEN E15 AND E17
   B) ADD A JUMPER BETWEEN E17 AND E25
2. INSERT MICROBug ROM INTO SOCKET U15 ON MM01
3. VERIFY THAT TERMINAL K1 IS JUMPERED FOR NORMAL OPERATION AND NOT FOR OPERATION WITH A DEBUG MODULE
4. MICROBug USES LOCATIONS 0380-03FF OF THE 1K RAM ON MM01 FOR SCRATCHPAD



USING MM08 WITH MM02

1. SET ACIA MODULE ADDRESS SWITCHES TO 8048
   A) CUT THE CONDUCTOR BETWEEN E15 AND E17
   B) ADD A JUMPER BETWEEN E17 AND E25
2. INSERT MICROBug ROM INTO SOCKET U23 ON MM04
3. REMOVE ALL JUMPERS FROM SOCKET U8, MM04
4. CONNECT MM08 TO MAKE ADDRESSES 0380-03FF AVAILABLE FOR SCRATCHPAD



USING MM08A WITH MM01A

1. INSERT MICROBug ROM INTO SOCKET U17
2. MICROBug USES LOCATIONS 0380-03FF OF THE 1K RAM ON MM01A FOR SCRATCHPAD

MOTOROLA

M68MM09E.

CMOS-RAM MODULE

The M68MM09E4 (M68MM09E2) are Micromodules/EXORciser bus compatible and provide 4096 x 8-bit (2048 x 8-bit) of non-volatile random access memory.

The Micromodule 9 includes:

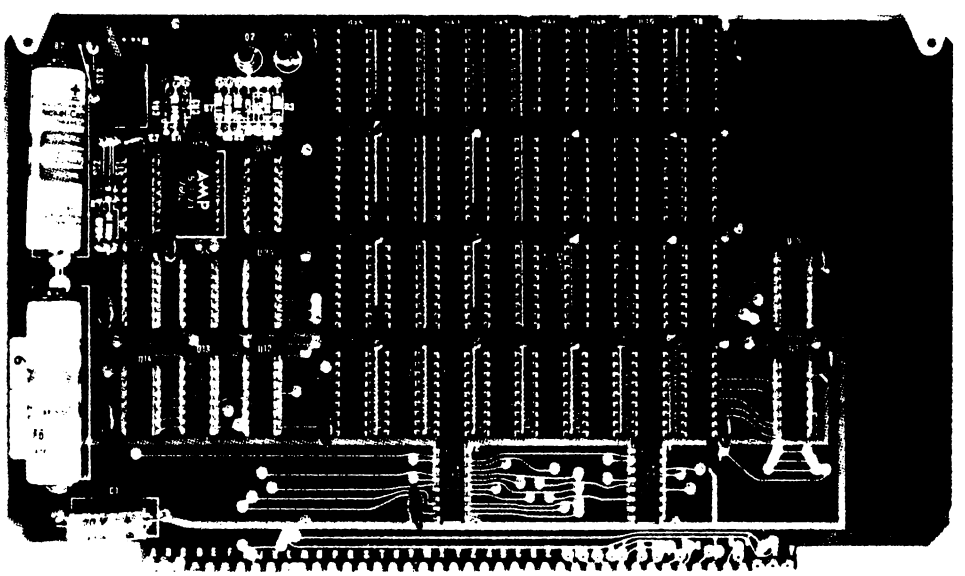
- TTL Voltage compatibility
- 4K x 8 (alt. 2K x 8)-bit of Static CMOS Memory
- On board rechargeable batteries with charging circuitry
- 30 days minimum data retention time
- Switch selectable base location address (4K increments)
- Switch selectable RAM/ROM capacity
- Bus interface drivers
- 32 (16) CMOS 1024 x 1 bit / 18 pin RAM Components

MICROMODULES

CMOS – RAM MODULES

ORDERING INFORMATION

M68MM09E2	2K x 8-bit CMOS-RAM Module
M68MM09E4	4K x 8-bit CMOS-RAM Module



Specification		Value
On board memory:	M68MM09E2	2048 Bytes
	M68MM09E4	4096 Bytes
Bus:	Address	TTL Voltage compatible
	Data	Three-state TTL voltage compatible
	Control	TTL Voltage compatible
Minimum data retention time (4K Bytes)		30 Days with fully bharged battery
Battery recharging time		24 hours for fully discharged battery
On board batteries		Two Cd-Ni 1.2 Volt/0,5 Ah.
MPU Cycle time		1 μs
Power requirement		+5 Vdc 350 mA
Operating temperature		0 °C to 50 °C
Dimensions (WxHxT)		9.75" x 5.75" x 0.71" (248 mm x 146 mm x 18 mm)
PC board thickness		0.06" (1.6 mm).

M68MM11 MICROMODULE

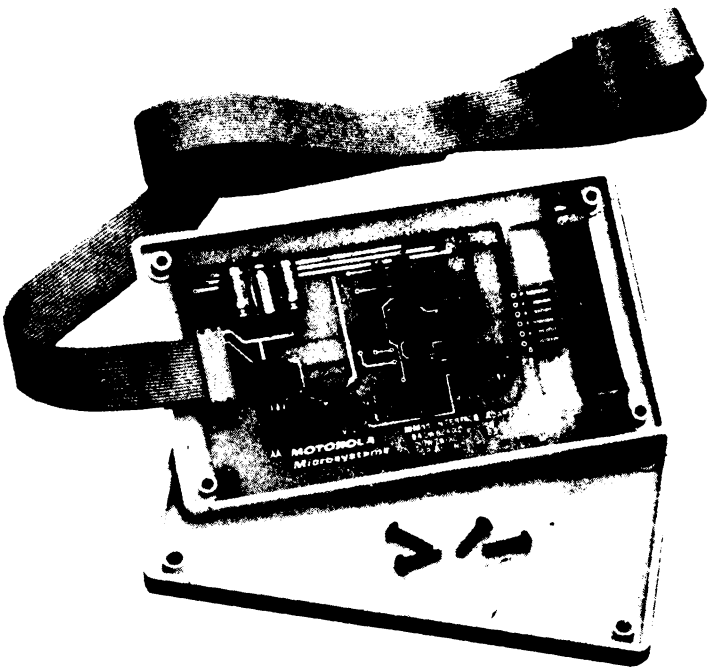
RS-232-TO-TTY ADAPTER

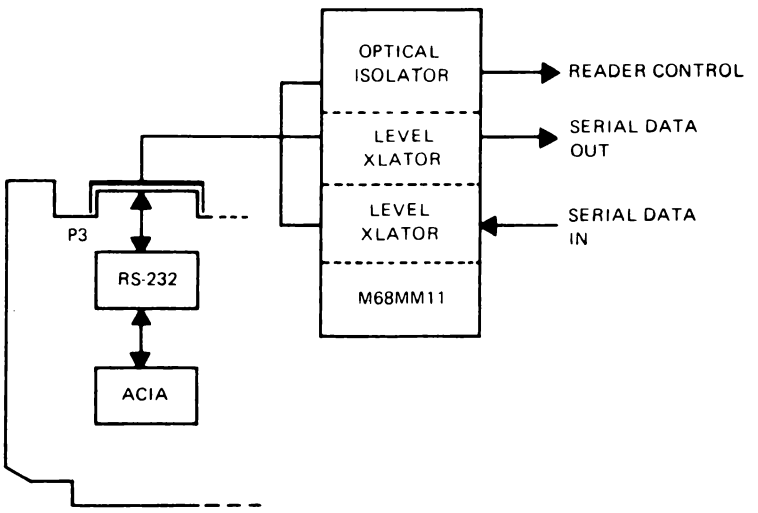
MICROMODULE 11

Micromodule M68MM11 provides a translation from the RS-232 serial data output port of Micromodule M68MM01, M68MM01A, or M68MM01B to the 20 mA neutral current loop signals required by an ASR33 Teletypewriter (TTY). The TTY data terminal shall be configured for automatic reader/punch control, full-duplex operation, and 20 mA neutral current loop operation. This Micromodule can also be used to provide these same functions for EXORciser II.

FEATURES

- Translates RS-232 serial data input/output to 20 mA neutral current loop data input/output
- Compatible with Micromodules 1A, 1A2, 1B1, and with EXORciser II
- 48" Micromodule interconnecting cable
- Housed in 7.5" x 4.5" x 1.0" high impact strength plastic case





PRODUCT ORDERING INFORMATION

The following table provides ordering information for Micromodule 11. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM11	Micromodule 11 — RS-232-to-TTY adapter module

M68MM13A, 13B MICROMODULE

DIGITAL OUTPUT (CONTACT CLOSURE)

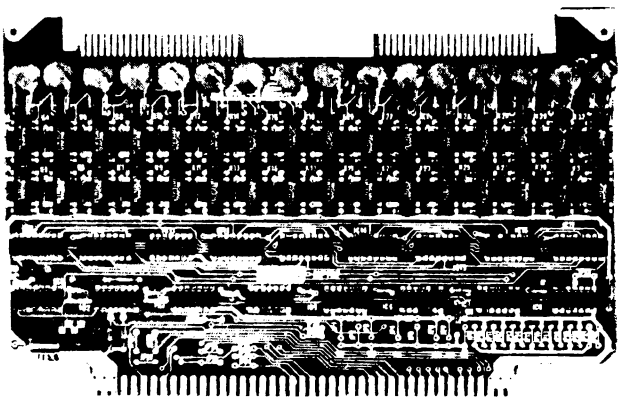
MICROMODULE 13A, 13B

Micromodule M68MM13A and M68MM13B are digital output (contact closure) microperipheral boards to be used with Motorola M6800 microcomputer systems. The M68MM13A has 16 digital output channels, while the M68MM13B has 32 digital output channels.

Relays are used in both the M68MM13A and 13B to provide high isolation for system-to-microcomputer and channel-to-channel transient protection. The relay contacts are protected from high voltage transients, that are encountered in industrial switching circuits, by the use of varistors across the contacts.

FEATURES

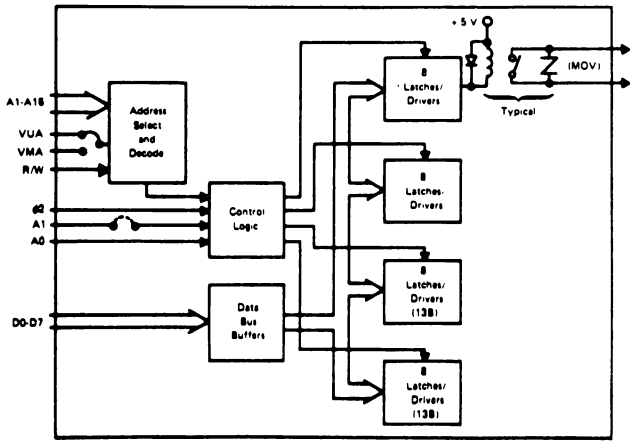
- Completely isolated digital output microperipheral (contact closure) on a board
- High isolation for system-to-microcomputer (600 Vdc) and channel-to-channel (300 Vdc)
- Low output impedance for high current drive
- 16 digital output channels (Micromodule 13A)
- 32 digital output channels (Micromodule 13B)
- On-board inductive load transient protection
- Full on-board address selection
- Micromodule and EXORciser bus compatible



GENERAL DESCRIPTION

Micromodules 13A and 13B microcomputer peripheral boards provide 16 or 32, respectively, digital output channels used to isolate the microcomputer from the system being controlled. Each output is isolated from the microcomputer bus up to 600 Vdc and from channel-to-channel up to 300 Vdc. In addition, since each channel is isolated, the voltage switched by each line is not critical and ground loops are avoided. Varistors are used to protect each reed relay contact by suppressing high voltage transients such as those encountered in inductive circuits.

These modules appear as memory locations to the user. Data written in the data bus controls the status of each output ("1" to close and "0" to open). Any memory write command may be used, with each command controlling the status of eight channels. Because the address block occupied by each module is user selectable, it can be placed anywhere in memory.



SPECIFICATIONS

Number of Channels	16 for M68MM13A 32 for M68MM13B
Relay Output Specifications:	
Rated Load	10 Watts (max), resistive 0.5 Amps (max), resistive 28 Vrms (max), resistive
Transient Protection (MOV)	250 mW continous 30 Watt-seconds discharge capacity
Operation	10^6 operations (min) 250 μs actuate time 250 μs de-actuate time 150 μs bounce time
Isolation	600 Vdc, output-to-microcomputer bus 300 Vdc, output-to-output
Physical Characteristics	
Width	9.75 in.
Height	6.00 in.
Board Thickness	0.062 in.
Connectors	
Microsystem bus	Stanford Applied Engineering SAE-43D/1-2 or equivalent
Output Ports	3M type 3415-0001 or equivalent

PRODUCT ORDERING INFORMATION

The following table provides the ordering information for Micromodules 13A and 13B. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM13A	Micromodule 13A – 16 digital outputs (contact closures) micromodule
M68MM13B	Micromodule 13B – 32 digital outputs (contact closures) micromodules

M68MM13C, 13D MICROMODULE

DIGITAL INPUT (OPTICALLY ISOLATED)

MICROMODULE 13C, 13D

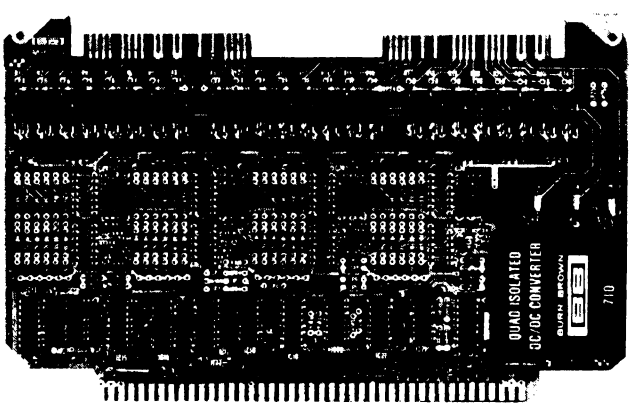
Micromodules M68MM13C and 13D are digital input microperipheral boards designed to be used with Motorola M6800 microcomputer systems. The microperipheral boards are electrically and mechanically compatible with Motorola's Micromodules and EXORciser development system. These micromodules have 24 channels of optically isolated digital input.

Module M68MM13C senses the user-supplied input voltage to determine if the input is read as a data one (greater than 17 V) or as a data zero (less than 4 V). Module M68MM13D provides an on-board isolated dc/dc converter to supply the necessary wetting current to sense user-supplied contact closures as inputs.

These boards appear as memory locations to the user. Data read on the data bus monitors the status of each input. Each Read command monitors the status of eight channels. Address bits A0 and A1 select which set of eight inputs is monitored. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory.

FEATURES

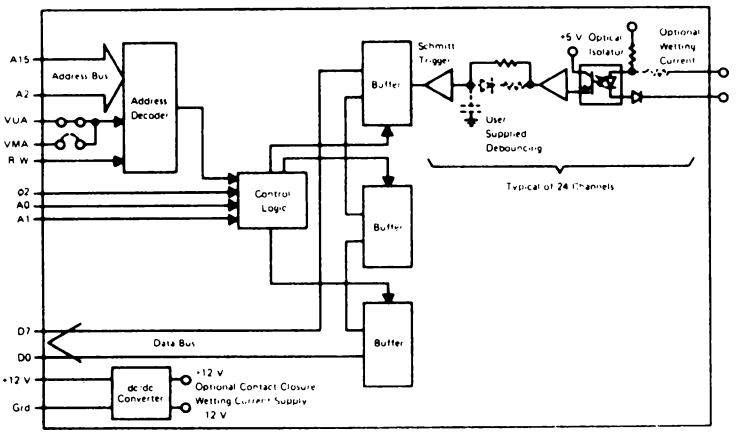
- Completely isolated digital input microperipheral on a board
- High isolation for system-to-microcomputer (600 Vdc) and channel-to-channel (300 Vdc)
- 24 channels of optically isolated voltage inputs (Micromodule 13C)
- 24 channels of optically isolated contact closure inputs (Micromodule 13D) — on-board isolated dc/dc converter provides wetting current
- Area provided for user-supplied debounce and ac sense circuitry
- Full on-board address selection
- Micromodule and EXORciser bus compatible



GENERAL DESCRIPTION

Micromodules 13C and 13D provide 24 optically isolated digital input channels for use with Micromodule-based systems or with the EXORciser. Micromodule 13C is designed for use with voltage inputs (wet relay contacts), while Micromodule 13D is designed for dry relay contacts. Micromodule 13D may also be modified by jumper selection to operate with voltage or contact closure inputs in any combination. Inputs to each module are arranged in groups of eight channels. Each input is isolated from the microcomputer bus up to 600 Vdc and from channel-to-channel up to 300 Vdc. In addition, since each channel is isolated, the voltage switched by each line is not critical and ground loops are avoided.

Both Micromodules are addressed like memory. Each input channel is one memory bit and any read command may be used ("0" is open and "1" is closed). Each read command inputs the status of eight channels. Because the address block occupied by each module is user selectable, it can be placed anywhere in memory.



SPECIFICATIONS

Number of Channels	24, Voltage Input for M68MM13C 24, Contact Closure for M68MM13D
Optically Isolated Input Specifications	
Voltage Input	
(Data = One)	Greater than 17 V
(Data = Zero)	Less than 4 V
Maximum Input	168 Vrms (max) 84 Vdc (max)
Contact Closure Input	On-board, isolated dc/dc Converter supplies wetting current supply (M68MM13D only)
Isolation	600 Vdc, input-to-microcomputer bus 300 Vdc, input-to-input
Physical Characteristics	
Width	9.75 in.
Height	6.00 in.
Board Thickness	0.062 in.
Connectors	
Microsystem bus	Stanford Applied Engineering SAC-43D/1-2 or equivalent
Input ports	3M type 3415-0001 or equivalent

PRODUCT ORDERING INFORMATION

The following table provides the ordering information for Micromodules 13C and 13D. For further information, contact your local sales office.

PART NO.	DESCRIPTION
M68MM13C	Micromodule 13C – optically isolated digital input module 24 voltage input channels
M68MM13D	Micromodule 13D – optically isolated digital input module 24 contact closure input channels

M68MM15A/15A1 MICROMODULE

HIGH-LEVEL A/D MODULE

MICROMODULE 15A,15A1

Micromodules 15A/15A1 are printed circuit board modules with which high-level analog data may be acquired and converted into a digital format for storage, transmission, or computation. This capability is commonly needed in data logging, industrial automatic test equipment, and a wide variety of industrial control applications.

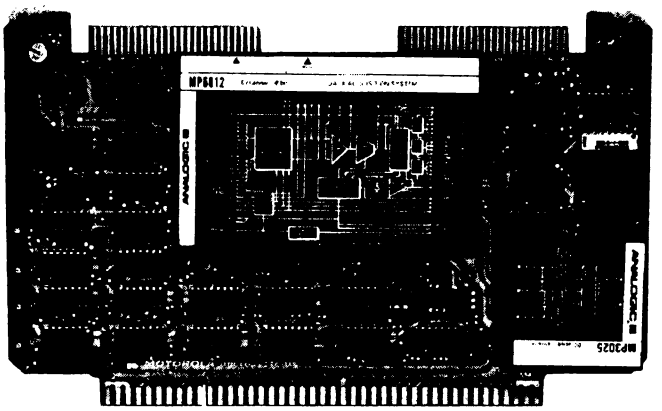
Micromodules 15A/15A1 accept analog input voltages ranging from 500 mV to 10 volts full scale, and converts them with nominal 12-bit resolution into a digital representation. Micromodule 15A provides 16 single-ended or 8 differential input channels while Micromodule 15A1 offers 32 single-ended or 16 differential input channels.

As with any M6800-based I/O devices, Micromodules 15A/15A1 and their registers are treated as memory by the system microprocessor since provision is made on board for decoding the 16 address bus signals. An address selection socket allows the required unique base address to be established for the modules through the use of appropriate jumpers.

Micromodules 15A/15A1 are bus compatible with the total Micromodule Family and all Motorola development systems, including the 2.0 MHz EXORciser II. This universality gives the user his choice of many tools with which to develop and debug his system software and hardware.

FEATURES

- 16 single-ended or pseudo-differential or 8 true-differential analog input channels (MM15A)
- 32 single-ended or pseudo-differential or 16 true-differential analog input channels (MM15A1)
- A/D converter of 12-bit nominal resolution
- Full scale inputs of 0 to +5 Vdc, 0 to +10 Vdc, ±5 Vdc, ±10 Vdc (strap options)
- Software programmable gain amplifier: factors of X1, X2, X4, or X8
- Software section of operating mode: Halt during conversion, Interrupt at end of conversion, software or external trigger start of conversion
- Single +5 Vdc operation, on-board dc-to-dc converter provides ±15 Vdc
- Address, data and control bus buffers for interface with EXORciser/Micromodules



GENERAL DESCRIPTION

Micromodule 15A/15A1 provides the capability for converting high-level analog signals into a 12-bit representation. The module comprises analog input multiplexers; means (strappable option) for operating with single-ended, pseudo-differential or true-differential inputs; means (strappable option) for choosing unipolar 5 or 10 volt full scale or choosing bipolar ±5 or ±10 volt full scale input levels. A software programmable gain amplifier offering gain factors of X1, X2, X4 or X8; and A/D converter of nominal 12-bit resolution; a 5-volt to ±15-volt-dc to dc converter; and TTL compatible buffers for the system address, control, and data busses are also provided.

Use of appropriate jumpers in address select socket U10 establishes address bits A2, A3, A4, A11, A12, A13, A14 and A15 as true or false enable signals in order to set the module's base address. This may be set anywhere in the range 0500 to FD1C, hexadecimal. Sequential memory locations for the module's four addressable registers are assigned automatically when the module's base address is established. The four registers accessible to the user are used for:

a. Gain/Mux address
b. Command/Status address
c. Output data, high byte
d. Output data, low byte

Wire wrap terminals allow selection of the module's input configuration and input voltage range options. Choice of output code, straight binary or two's complement, is also made using wire wrap terminals.

Once the base address, type of analog input and output code are set for the module, the user may program each register as desired. The GAIN/MUX register provides channel selection and gain. The COMMAND/STATUS register provides the programmer with control of the mode of operation and module status information. The OUTPUT DATA registers store the data from the last conversion of the A/D.

Means of calibrating the programmable gain amplifier, adjusting the A/D converter offset and adjusting the A/D converter gain as well as troubleshooting test points are also provided on Micromodule 15A/15A1.

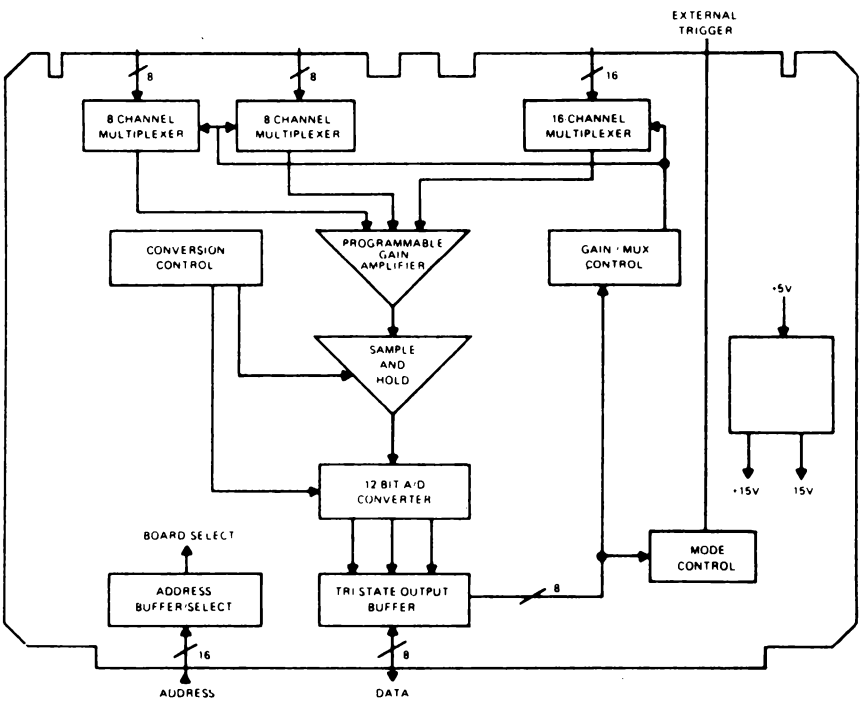
SPECIFICATIONS

Power Requirements	+5Vdc ±5% @ 1.2 A (max.)
Micromodule Bus Signals	
Address Bus	TTL compatible buffered input
Control Bus	TTL compatible buffered input
Data Bus	
Module Input	TTL compatible buffered input
Module Output	TTL compatible buffered output
Analog Input (P1 and P2)	
Operating (Signal plus common mode voltage)	−10.24 V to + 10.24 V
Maximum, continuous without damage	30 V
Impedance	>100 megohms
Current	1 nA (typical) at 25° C. 80 nA (max.) at 70° C.
Capacitance	10 pF (max.) off channel 600 pF (max.) differential 1200 pF (max.) single-ended
A/D Conversion	
Resolution	12 bits
Relative Accuracy (Linearity)	±0.03% FSR
Quantization Error	±1/2 LSB
3 Sigma Noise	0.01% FSR + 0.5 mV referred to input
Stability	
Tempco of Linearity	<6 PPM FSR/°C
Tempco of Gain	<13 PPM FSR/° C at Gain of 1 <30 PPM FSR/° C at Gains of 2, 4, or 8
Tempco of Offset	<25 PPM FSR/° C
Conversion Time	40 microseconds maximum
Operating Temperature	0° to 70° C
Physical Characteristics	
Width x Height	9.75 in. x 5.75 in.
Board Thickness	0.062 in.
Bus Mating Connector Types	
86-Pin Connector (1)	Stanford Applied Engineering SAC-43D/1-2 or equivalent
50-Pin Connector (2)	Viking 3VH25/1JN5 or equivalent

PRODUCT ORDERING INFORMATION

Use the part numbers below when ordering Micromodule 15A or Micromodule 15A1:

PART NO.	DESCRIPTION
M68MM15A	High-Level A/D Module 15A is a 16-channel single-ended input or strap selected 8-channel differential input 12-bit analog-to-digital converter.
M68MM15A1	High-Level A/D Module 15A1 is a 32-channel single-ended input or strap selected 16-channel differential input 12-bit analog-to-digital converter.



M68MM15CV/15CI MICROMODULE

ANALOG OUTPUT MODULE

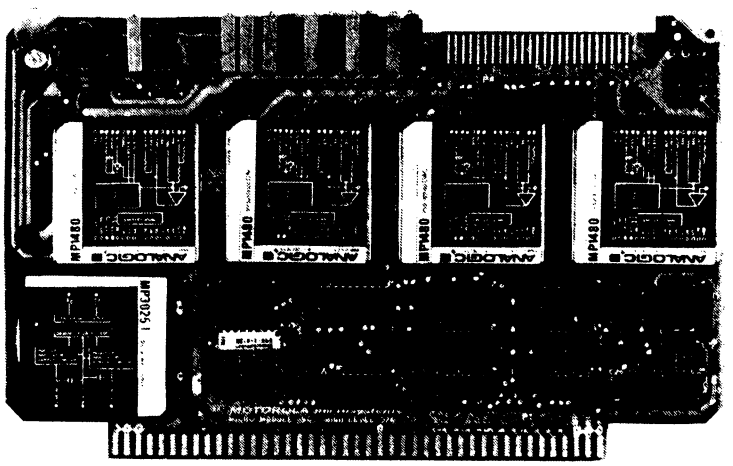
MICROMODULE 15CV/15CI

Micromodules 15CV/15CI are printed circuit board modules with which digital information may be converted into voltage or current for interfacing analog equipment. This function is needed to provide the display and control signals required for a wide variety of measurement and control application.

All the M68MM15CV voltage output and the M68MM15CI current output modules accept 12-bit TTL-compatible inputs for conversion and are available in versions offering from one to four channels. The output range—0 to +10 Vdc, ±10 Vdc, 0 to +5 Vdc or ±5 Vdc—of the voltage modules is selected by jumper. Output range of the current modules is 4 to 20 mAdc.

As with any M6800-based device, Micromodules 15CV/15CI and their registers are treated as memory by the system microprocessor, since provision is made on board for decoding the 16 address bus signals. An address selection socket allows the required unique base address to be established for the module through the use of appropriate jumpers.

Micromodules 15CV/15CI are bus compatible with the total Micromodule Family and all Motorola development systems, including the 2.0 MHz EXORciser II. This universality gives the user his choice of many tools with which to develop and debug his system software and hardware.



FEATURES

- One to four 12-bit Digital-to-Analog-Converter (DAC) channels per module
- Full-scale output voltages: 0 to +10 Vdc, ±10 Vdc, 0 to +5 Vdc and ±5 Vdc, each channel M68MM15CV series (strap option)
- Natural binary or two's complement input code (strap option)
- 4 to 20 mAdc output M68MM15CI series (strap option)
- Strap selectable module base memory address, 0500 to FD3F hexadecimal
- Single +5 Vdc operation, on board dc-to-dc converter provides ±15 Vdc
- Address, data, and control bus buffers for interface with EXORciser/Micromodules

GENERAL DESCRIPTION

The 15C series of Micromodules converts 12-bit digital input data into an equivalent voltage or current for output to analog equipment. Micromodules M68MM15CV1 through M68MM15CV4 provide one to four channels of analog output voltage, respectively. Micromodules M68MM15CI1 through M68MM15CI4, respectively, provide one to four channels of analog output current or analog output voltage.

Each module contains address bus buffers and address decoding logic for each on board DAC, data bus buffers and latches to hold a 12-bit input word, and the DAC or DACs for converting this information into an equivalent analog output.

The unique base address within the system memory map required for each on board DAC is established by the user through the installation of appropriate jumpers on an address socket on the module. The user's choice of either offset binary or two's complement as the module's input code and his choice of output polarity and range are set via wire-wrap connections between the appropriate pins on the module.

The Analog Output Modules contain provisions for calibrating reference and output voltages and output currents in order to obtain the highest accuracy for a specific application. Calibration is made using standard laboratory test equipment.

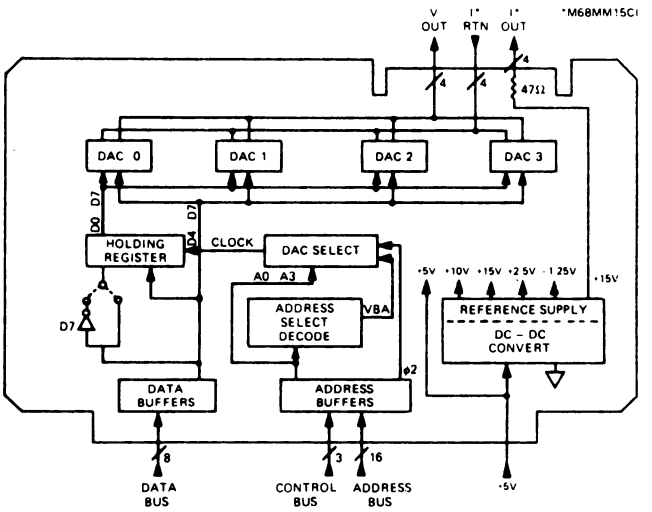
SPECIFICATIONS

Power Requirements	+5 Vdc ±5% @ 600 mA plus 220 mA/channel (max)
Micromodule Bus	
Address Bus	TTL compatible buffered input
Control Bus	TTL compatible buffered input
Data Bus	
Module Input	TTL compatible buffered input
Analog Output (voltage) Range	Strap selectable; 0 to +10 V, ±10 V, 0 to +5 V, ±5 V
Linearity	0.012%
Stability	
Drift @ 0 V	40 ppm FSR/°C (max)
Drift @ Full-Scale	50 ppm FSR/°C (max)
Noise (3 sigma with 100 kHz filter)	1 mV RMS
Output Impedance	0.2 Ω (max) at dc
Output Capacitance	750 pF (max)
Output Current	±5 mA (max)
Slew Rate (no external capacitance)	10 V/microsecond (max)
Analog Output (current, MM15CI)	
Range	4 to 20 mAdc
Compliance Voltage	9 V
ISA Standard	Type 4, non-isolated Class L with internal supply Class U with external supply
Linearity	0.01%
Stability	
Offset	40 ppm FSR/°C (max)
Full-Scale	55 ppm FSR/°C (max)
Noise	1 μA RMS
Slew Rate	2 mA/microsecond (min)
Fault Protection	
Open Circuit Voltage	Loop Supply Voltage
Reverse Polarity	No damage for less than -200 Vdc
Overvoltage Transient	No damage for less than +200 Vdc
110 Vac RMS	No damage for at least 5 minutes
Operating Temperature	0° to 70°C
Physical Characteristics	
Width X Height	9.75 inches X 5.75 inches
Board Thickness	0.062 inches
Bus Mating Connector Types	
86-Pin Connector (1)	Stanford Applied Engineering SAC-43D/1-2 or equivalent
50-Pin Connector (2)	Viking 3VH25/1JN5 or equivalent

PRODUCT ORDERING INFORMATION

Use the part numbers below when ordering Micromodule 15CV/15CI.

PART NO.	DESCRIPTION
M68MM15CV1	High-Level Voltage D/A Module 15CV1 is a single-channel, 12-bit digital-to-analog converter of strap selectable unipolar or bipolar, 5 or 10 Vdc output with zero adjust and full-scale adjust potentiometers.
M68MM15CV2	High-Level Voltage D/A Module 15CV2 is a dual-channel version of Micromodule 15CV1.
M68MM15CV3	High-Level Voltage D/A Module 15CV3 is a three-channel version of Micromodule 15CV1.
M68MM15CV4	High-Level Voltage D/A Module 15CV4 is a four-channel version of Micromodule 15CV1.
M68MM15CI1	Current D/A Module 15CI1 is a single-channel, 12-bit digital-to-analog converter of strap selectable 4 to 20 mAdc output or unipolar or bipolar 5 or 10 Vdc output with zero adjust and full-scale adjust potentiometers. The module has a 9-volt compliance voltage and the current output will meet ISA type 4 non-isolated current transmitter requirements.
M68MM15CI2	Current D/A Module 15CI2 is a dual-channel version of Micromodule 15CI1.
M68MM15CI3	Current D/A Module 15CI3 is a three-channel version of Micromodule 15CI1.
M68MM15CI4	Current D/A Module 15CI4 is a four-channel version of Micromodule 15CI1.



MOTOROLA

M68SAC1

STAND-ALONE COMPUTER

The M68SAC1 is a complete computer system that fits on a single printed circuit board, thus providing significant benefits in cost and size over multiboard systems.
The crystal controlled clock circuit provides the Stand-Alone Computer with the capability of working with dynamic memories and slow memories. The clock circuit also generates the basic timing signal used by the module's baud rate generator.
By setting jumpers, the user can tailor the module to work in different configurations to economically suit his needs.

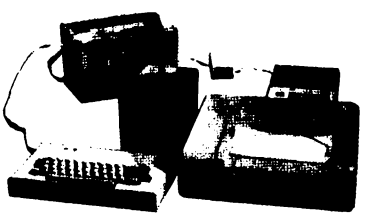
- Four 8-bit parallel Input/Output Ports and Control Lines for Peripheral Interfacing
- Two asynchronous Input/Output Ports with one RS232.C/TTL/-TTY Current Loop interface.
- 384 bytes of RAM
- Three MCM68708 or equivalent AROM/ROM Sockets:
- One MCM6830 ROM Socket
- 921.6 KHz on-board crystal controlled clock generator
- No restriction on Interrupt capability
- On board real-time clock capability
- Four jumper selectable vectors addresses.
- Fully buffered Three-State Bus Connector
- Fully compatible with all EXORciser modules

By adding options, the Stand-Alone Computer can be upgraded to an Autonomous Development System.

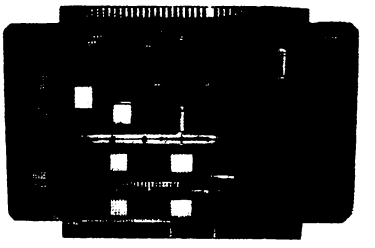
POLYVALENT DEVELOPMENT SYSTEM

STAND-ALONE COMPUTER

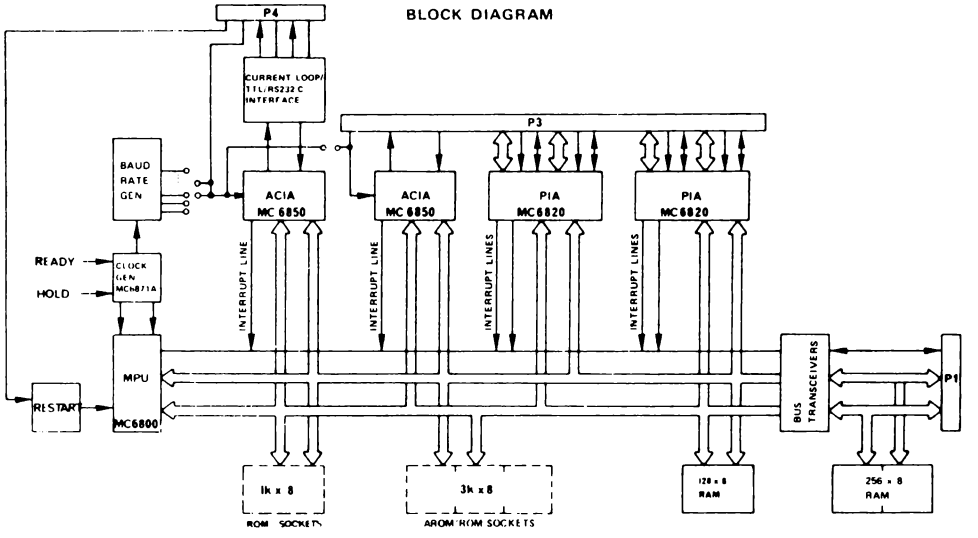
PDS



SAC



BLOCK DIAGRAM



MODULE SPECIFICATIONS

Specification		Value
Memory Size Capability		65, 536 bytes maximum.
On-Board Memory Size		384 bytes of RAM 3 x 1 K-byte MCM68708 compatible AROM/ROM Sockets 1 x 1 K-byte MCM6830 compatible ROM socket
Memory locations available for external expansion		44 K-byte: 0000 to 7FFF 9000 to 9FFF B000 to CFFF
Word Size	Data Address Instruction	8 bits 16 bits 8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts; Software interrupt
Clock Signal		921.6 KHz
Address Bus Data Bus Control Bus		Three-state TTL voltage compatible Three-state TTL voltage compatible TTL voltage compatible
MC6820 Peripheral Interface Adapter Lines MC6850 Asynchronous Communication Interface Adapter Serial Transfer Rate Terminal interface		TTL voltage compatible* TTL voltage compatible* 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600 baud RS232.C, TTL or 20 mA Current-Loop
Power requirements		+ 5 Vdc at 1,5 A + 12 Vdc at 200 mA – 12 Vdc at 200 mA – 5 Vdc on board converter
Operating temperature		0° to 70 °C
Dimensions Width Height Thickness PC Board Thickness		 248 mm 9.75 in. 165 mm 6.5 in. 13 mm 0.5 in. 1.6 mm 0.062 in.

*See MC6820 and MC6850 data sheets for specifications on these signals

MOTOROLA

M68DIM.

DISPLAY INTERFACE MODULE

The DIM is a complete alpha-numeric interface to a CRT monitor. M68DIM1-M68DIM2 are 16 lines of 32 characters interfaces and include HF modulator allowing to connect any ordinary TV display (European standards). The M68DIM6 is a 16 lines by 64 characters interface with an horizontal magnifier feature allowing to display 25 to 64 characters per line on the full width of the screen (controlled by an external 10K ohm linear potentiometer). The DIM includes a one page memory, an ASCII character generator and a video signal generator. While the one page memory is automatically accessed by the character generator, it can be normally accessed by a computer for reading and writing as the module emulates a standard 512/1024-byte RAM module beginning at address C000.

- Composite 625 lines positive or negative video signal generator
- One page memory
- Black-on-White or White-on-Black Display capability
- Fully buffered Three-State bus connector (EXORciser, PDS and Micro modules compatible)
- Hardware Top-of-Page pointer
- Jumper selectable base address
- Fully independant display refresh
- 128-character set

Options:

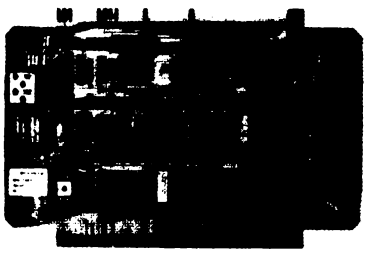
	M68DIM1	M68DIM2	M68DIM6
Page Format	16 lines of 32 characters	16 lines of 32 characters	16 lines of 25 to 64 characters (magnifier)
Memory capacity	512-byte	512-byte	1024-byte
HF modulator	55.25 MHz (channel E3, VHF)	591.25 MHz (channel E36, UHF)	N.A.

POLYVALENT DEVELOPMENT SYSTEM

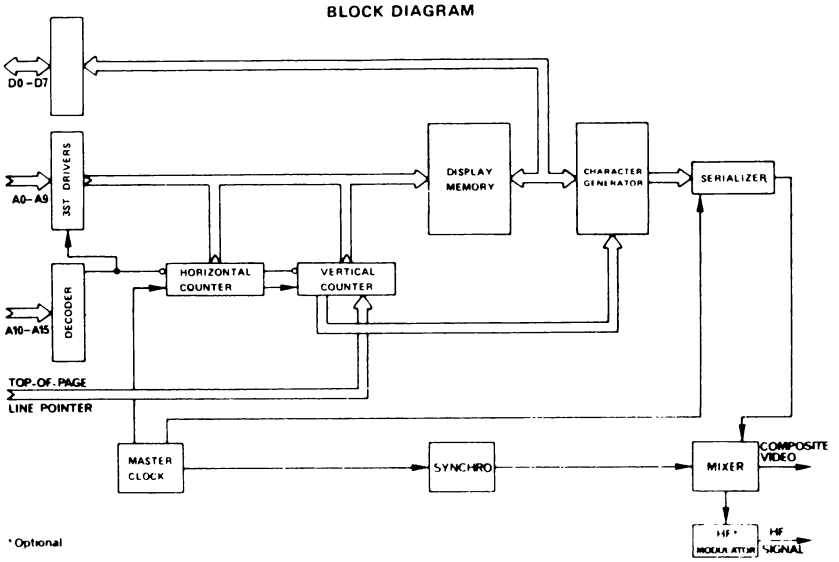
DISPLAY INTERFACE MODULES

DIM2

DIM6



BLOCK DIAGRAM



*Optional

MODULE SPECIFICATIONS

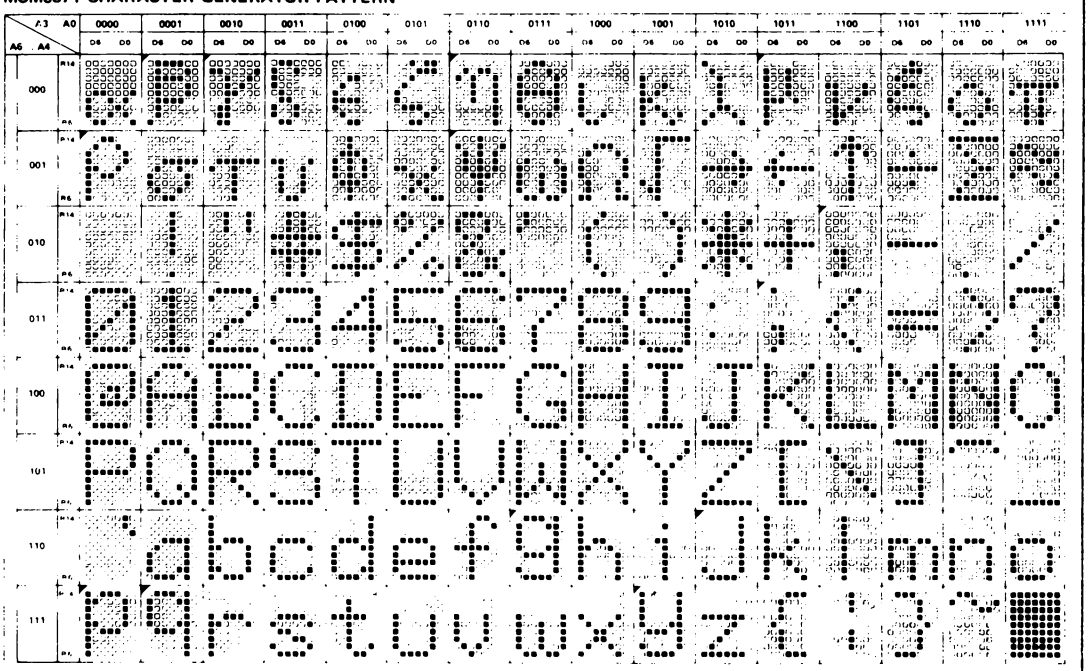
Specification	Value
On-board memory	512 bytes (X000* to X1FF)/1024 bytes (X000* to X3FF)
Address Bus	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Control Bus	TTL voltage compatible
Video signal	75Ω, 0.5V, composite, 625 lines positive or negative modulation
HF signal (M68DIM1 and M68DIM2)	60Ω, 5 mV, 55.25/591.25 MHz
Page size	16 lines of 32 characters
Character generator	96 ASCII characters, 32 Greek characters, 7 x 9 matrix Character-per-character Selectable (8th bit) white-on-black or black-on-white display.
Power Requirements	+5 Vdc at 1.5 A +12 Vdc at 70 mA
Operating temperature	0°C to 55°C
Dimensions	
Width	248 mm 9.75 in.
Height	165 mm 6.5 in.
Thickness	27 mm 1.1 in.
PC Thickness	1.6 mm 0.062 in.

*Jumper selectable.

Recommended Firmware

M68IOS1 The Input/Output Supervisor provides an efficient means of driving the Display Interface Module. See M68IOS1 Datasheet for detailed description.

MCM6571 CHARACTER GENERATOR PATTERN



MOTOROLA

M68MDM1

5" DISPLAY MONITOR

The M68MDM1 modular 5 inch display provides versatile performance features, contained on plug-in boards and modules, and placed in a compact chassis that fits right into terminals, which require a small, distinctly readable display.
Solid State: All components (except the picture tube) are completely transistorized.
Signal Inputs: Composite video.
DC Power: The M68MDM1 operates on 12V DC at less than one amp, making it independent of international power considerations.
Resolution: Video response to 12 MHz and the excellent geometry and small spot size of the picture tube combine to assure 650-line horizontal resolution for sharp picture detail.
Seviceability: 99% of the module circuitry is contained on two easily removable printed circuit boards for simple, expedient field maintenance.

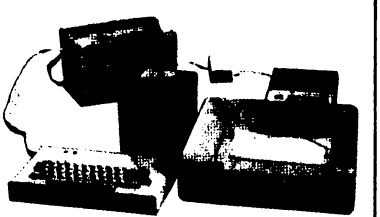
SPECIFICATIONS

Specification	Value
Picture tube	
diagonal	5" (127 mm)
viewing area	13 sq. in. (84 cm^2)
deflection angle	55°
phosphor	P4
Input signal	
composite video	0.5V to 2.5V, 75Ω, negative modulation
Video response	3dB, 10 Hz to 12 MHz
Resolution	
center	650 lines
corners	500 lines
Geometric distortion/linearity	less than 2%
High Voltage	9,5 KV at 50 μA beam current, nominal
Horizontal blanking interval	11 μs required
Scanning frequency	
horizontal	15 720 Hz ± 500 Hz
vertical	50 Hz
Power Requirement	12 Vdc at 900 mA
Operating temperature	0°C to 55°C
Dimensions	
height	117 mm
width	131 mm
depth	234 mm
Weight	1.6 Kg (Net)

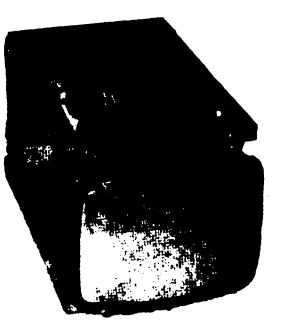
POLYVALENT DEVELOPMENT SYSTEM

5" DISPLAY MONITOR

PDS



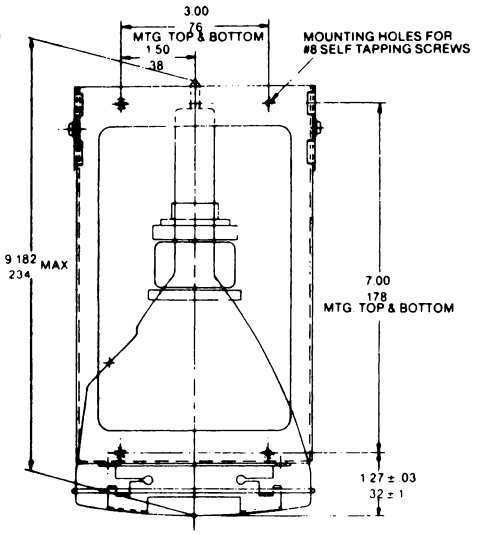
MDM1



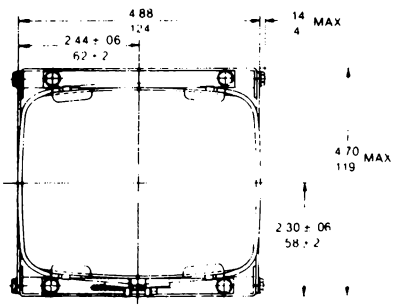
ACCESSORIES

M68DMC1	Display cabinet for 5" CRT

Top



Front



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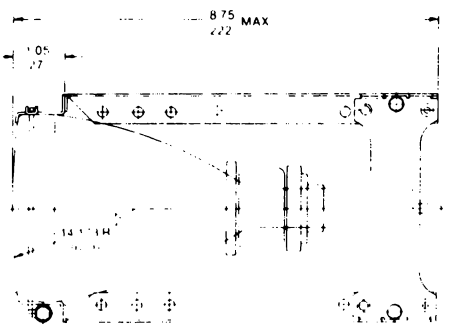


MOTOROLA

M68MDM9

9" DISPLAY MONITOR

The M68MDM9 modular 9 inch display provides versatile performance features, contained on plug-in boards and modules, and placed in a compact chassis that fits right into terminals, which require a distinctly readable display.
Solid State: All components (except the picture tube) are completely transistorized.
Signal Inputs: Composite video.
DC Power: The M68MDM9 operates on 12V DC at less than one amp, making it independent of international power considerations.
Resolution: Video response to 12 MHz and the excellent geometry and small spot size of the picture tube combine to assure 650-line horizontal resolution for sharp picture detail.
Seviceability: 99% of the module circuitry is contained on two easily removable printed circuit boards for simple, expedient field maintenance.

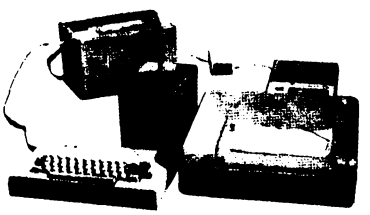
SPECIFICATIONS

Specification	Value
Picture tube	
diagonal	9" (228 mm)
viewing area	44 sq. in. (284 cm^2)
deflection angle	90
phosphor	P4
Input signal	
composite video	0.5V to 2.5V, 75Ω negative modulation
Video response	3dB, 30 Hz to 12 MHz
Resolution	
center	650 lines
corners	500 lines
Geometric distortion linearity	less than 2%
High Voltage	9.5 KV at 50 μA beam current, nominal
Horizontal blanking interval	11 μs required
Scanning frequency	
horizontal	15,720 Hz ± 500 Hz
vertical	50 Hz
Power Requirement	12 Vdc at 1000 mA
Operating temperature	0°C to 55°C
Dimensions	
height	184 mm
width	241 mm
depth	241 mm
Weight	3.6 Kg (Net)

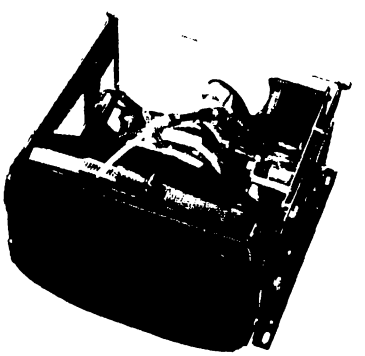
POLYVALENT DEVELOPMENT SYSTEM

9" DISPLAY MONITOR

PDS



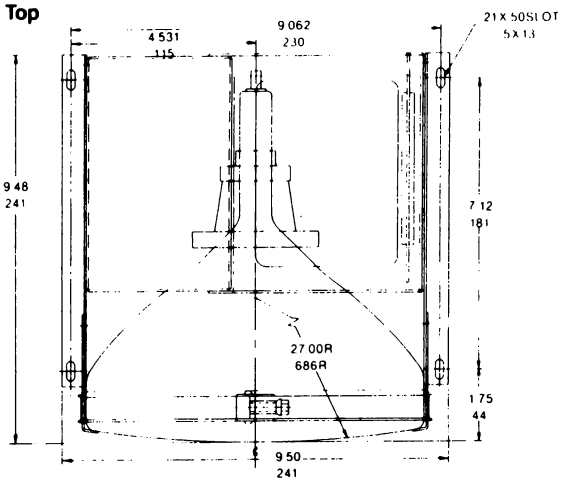
MDM9



ACCESSORIES

M68DMC9	Display cabinet for 9" CRT

Top



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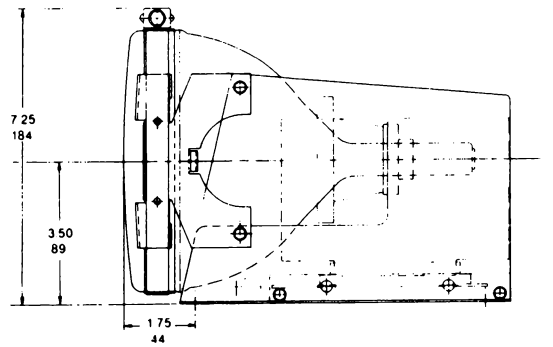
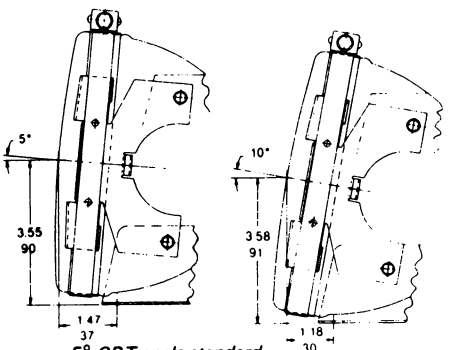




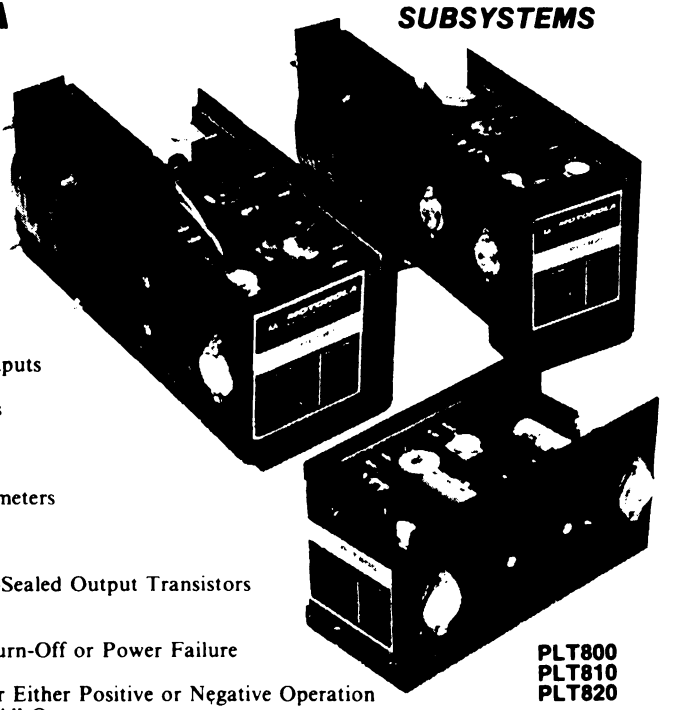
5° CRT angle standard
0° and 10° adaptable

MOTOROLA

SUBSYSTEMS

DC Power Supplies

Series Regulated Triple Output



PLT800
PLT810
PLT820

- Remote Sensing on +5 V
- Foldback Current Limiting on All Outputs with Automatic Recovery
- Overvoltage Protection on All Outputs
- 50°C Full Load Rating (70% of Rated Current at 70°C)
- Convection Cooled
- Excellent Ripple and Regulation Parameters
- One-Year Warranty
- 100% Burn-In
- Open Frame Construction
- Designed with All Metal Hermetically-Sealed Output Transistors
- Aluminum Heat Sink and Chassis
- 50 μ sec Transient Response
- No Voltage Overshoot on Turn-On, Turn-Off or Power Failure
- Integrated Circuit Regulation
- Fully Isolated Independent Outputs for Either Positive or Negative Operation
- Reverse Voltage Diode Protection on All Outputs

These triple output power supplies are designed to provide +5 volts dc at 2, 4, or 6 amps, respectively, for microprocessors and other IC logic, ±9 to ±12 volts dc at 0.3, 0.7, and 1.0 amps, respectively, for memory systems, operational amplifiers, A-to-D converters and other analog systems.

Throughout the design cycle particular attention was given to thermal layout, resulting in a unit featuring conservative ratings and inherent reliability. Each supply is capable of providing rated load current on all three outputs simultaneously at 50°C ambient.

Specifications

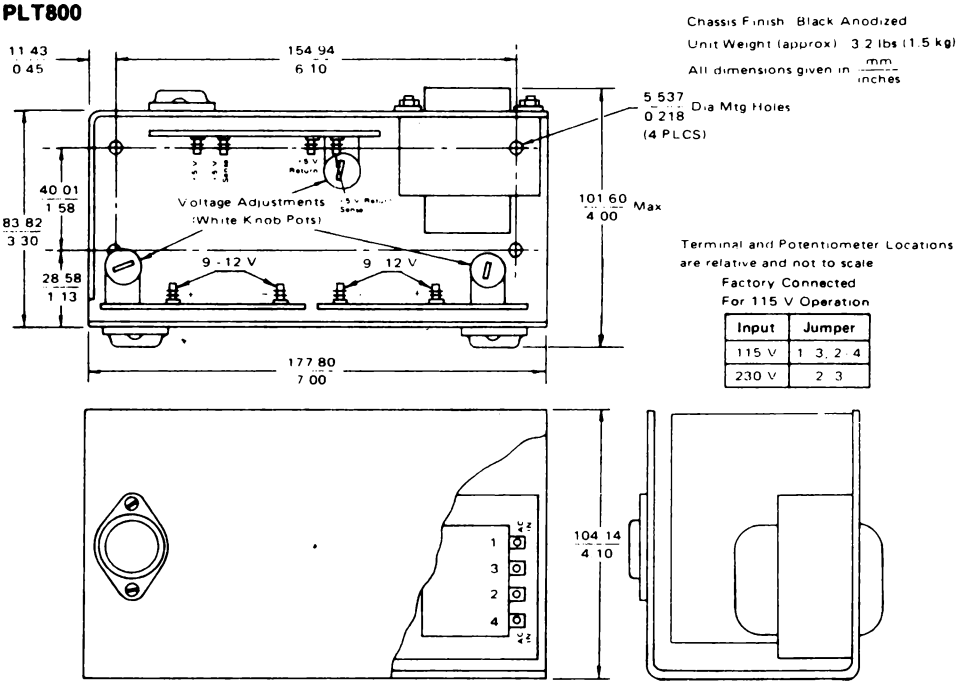
AC Input (Single Phase)	115 Vac ±10%, fully rated from 47 to 63 Hz, with jumper option for 230 Vac ±10% input.		
Device Number	**PLT800**	**PLT810**	**PLT820**
DC Output (Rated Load)	+5 Vdc ±0.5 Vdc @ 2 A	+5 Vdc ±0.5 Vdc @ 4 A	+5 Vdc ±0.5 Vdc @ 6 A
	±9 to ±12 Vdc @ 0.3 A	±9 to ±12 Vdc @ 0.7 A	±9 to ±12 Vdc @ 1.0 A
	±9 to ±12 Vdc @ 0.3 A	±9 to ±12 Vdc @ 0.7 A	±9 to ±12 Vdc @ 1.0 A
Short-Circuit Current	+5 Volt output — 0.6 A max	+5 Volt output — 1.25 A max	+5 Volt output — 1.8 A max
	±9 to ±12 Volt outputs — 0.15 A max	±9 to ±12 Volt outputs — 0.3 A max	±9 to ±12 Volt outputs — 0.4 A max
Load Regulation	0.1% max (no load to full load) — All outputs		
Line Regulation	±0.1% max (±10% Line Variation) — All outputs		
Output Ripple	1.5 mV RMS max, 5 mV P-P max		
Temperature Coefficient	0.025%/°C max		
Overvoltage Protection	Provided on all outputs. The +5 Volt output is set at 6.2 Vdc ±0.4 Vdc. The ±9 to ±12 Volt outputs are set at 13.7 Vdc ±1.1 Vdc.		
Isolation	1500 Vac applied input to output, input to chassis, output to chassis.		
Remote Sensing (+5 V output only)	Compensation for up to 0.5 Vdc drop in interconnecting leads.		
Transient Response	Output voltage will recover within regulation limits in 50 μ sec max in response to a 50% load step.		
Ambient Temperature	Operating: 0°C to +50°C at full rated load, derated linearly to 70% at +70°C. Storage: -40°C to +85°C.		

DC Power Supplies PLT800, PLT810, PLT820

Model Number	Output Voltage	Output Current (Amps)
PLT800	+5 ±9 to ±12 ±9 to ±12	2.0 0.3 0.3
PLT810	+5 ±9 to ±12 ±9 to ±12	4.0 0.7 0.7
PLT820	+5 ±9 to ±12 ±9 to ±12	6.0 1.0 1.0

Outline Drawings

PLT800



Chassis Finish: Black Anodized
Unit Weight (approx): 3.2 lbs (1.5 kg)
All dimensions given in mm / inches

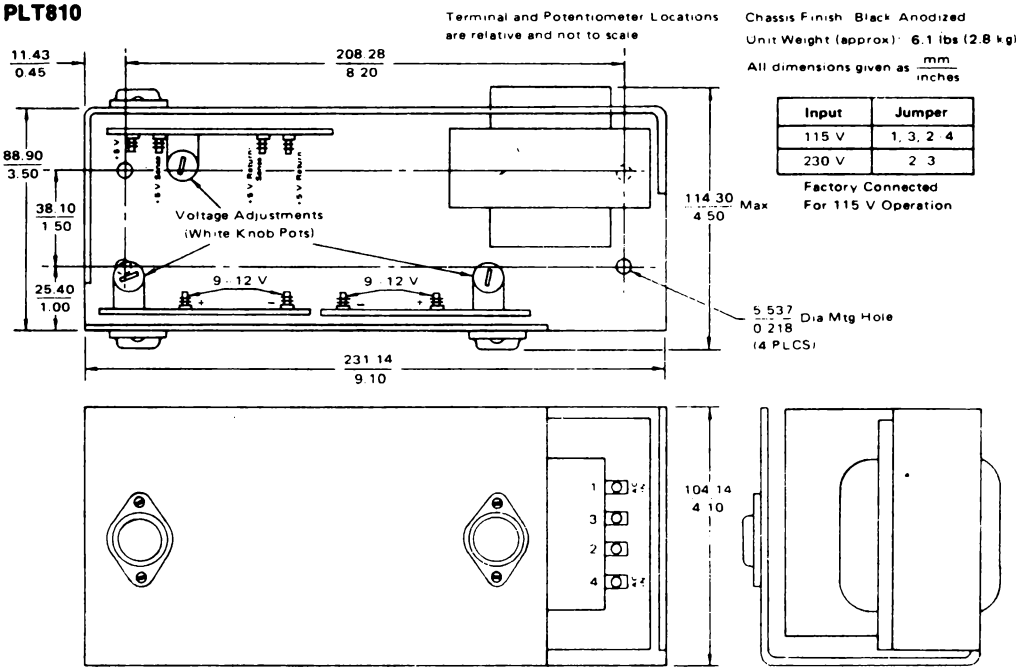
Terminal and Potentiometer Locations are relative and not to scale

Factory Connected
For 115 V Operation

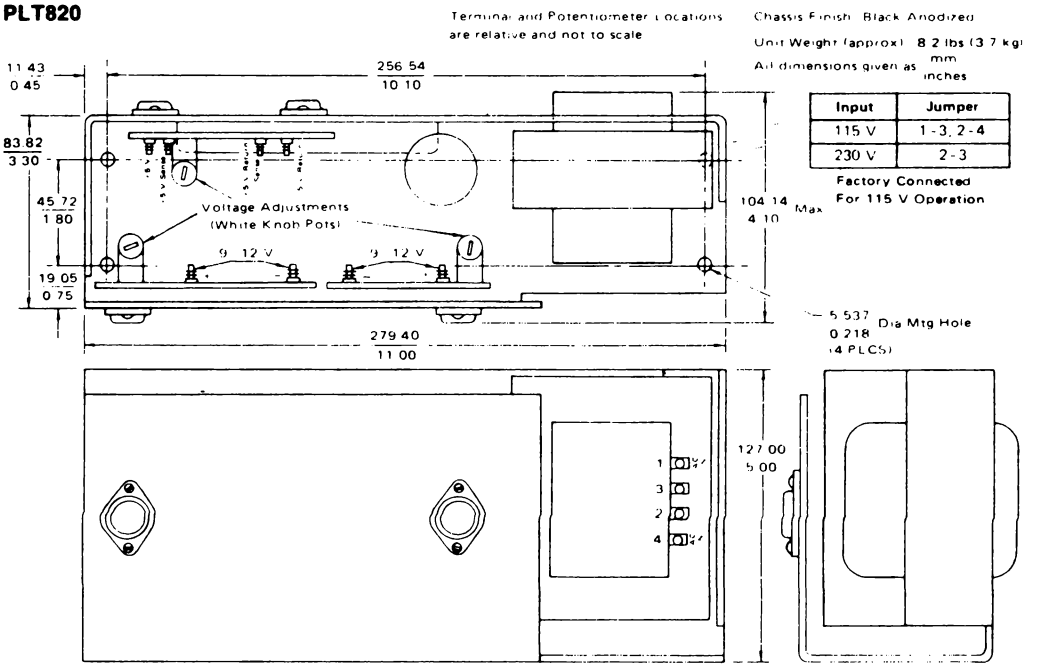
Input	Jumper
115 V	1-3, 2-4
230 V	2-3

DC Power Supplies PLT800, PLT810, PLT820

PLT810



PLT820

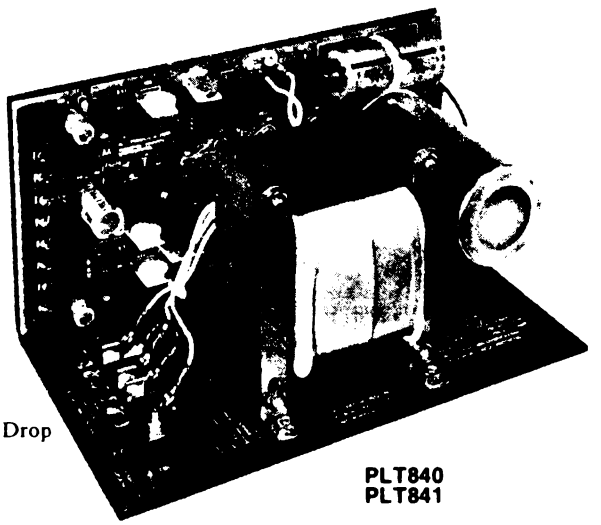


MOTOROLA

SUBSYSTEMS

DC Power Supplies

Series Regulated Triple Output



PLT840
PLT841

- Remote Sensing on +5 V
- Foldback Current Limiting on All Outputs with Automatic Recovery
- Overvoltage Protection on All Outputs
- 50°C Full Load Rating (with 50 CFM forced air cooling) (70% of Rated Current at 70°C)
- Eight Millisecond Hold Up Time After Line Drop Out (PLT841)
- Fully Isolated Outputs
- Excellent Ripple and Regulation Parameters
- One-Year Warranty
- 100% Burn-In
- Open Frame Construction
- All Metal Hermetically-Sealed Output Transistors
- Aluminum Heat Sink and Chassis
- 50 μ sec Transient Response
- No Voltage Overshoot or Undershoot on Turn-On, Turn-Off or Power Failure
- Integrated Circuit Regulation

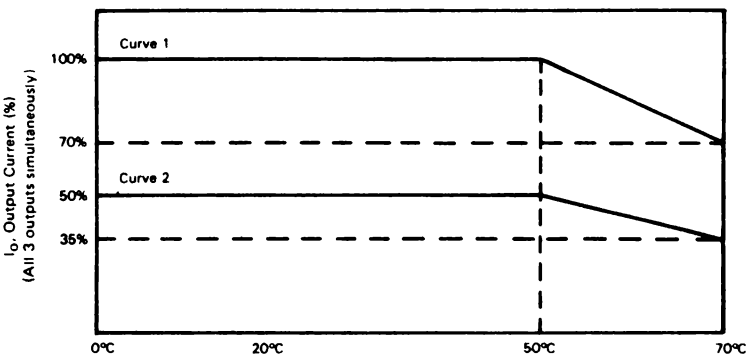
These triple output power supplies are designed to provide +5 volts dc at 15 amps for microprocessors and other IC logic, +12 volts and -12 volts at 2.5 amps and 1.5 amps, respectively, for memory systems, operational amplifiers, A-to-D converters and other analog systems.

Throughout the design cycle particular attention was given to thermal layout, resulting in a unit featuring conservative ratings and inherent reliability.

Specifications

AC Input (Single Phase)	95 to 125 Vac, fully rated from 47 to 420 Hz, with jumper option for 190 to 250 Vac input.		
DC Output (Rated Load)	Rated Load with 50 CFM forced air cooling:		
	+5 Vdc @ 15 Amps	+12 Vdc @ 2.5 Amps	-12 Vdc @ 1.5 Amps
Adjustment Range	+5 Volts ±0.5 Vdc	+12 Volts ±0.5 Vdc	-12 Volts ±0.5 Vdc
Load Regulation	0.1% max (no load to full load) — All outputs		
Line Regulation	For Full Input Voltage Variation:		
	+5 Vdc ±0.1% max	+12 Vdc ±0.05% max	-12 Vdc ±0.05% max
Output Ripple	2 mV RMS max, 10 mV P-P max (+5 Volt supply)		
	1 mV RMS max, 5 mV P-P max (±12 Volt supplies)		
Temperature Coefficient	0.05%/°C max		
Overvoltage Protection	Provided on all outputs. The +5 Volt output is set at 6.2 Vdc ±0.4 Vdc		
	The +12 Volt outputs are set at 13.7 Vdc ±1.1 Vdc.		
Short-Circuit Current	+5 Volt output — 5.0 Amps max		
	+12 Volt output — 0.8 Amps max		
	-12 Volt output — 0.5 Amps max		
Hold Up Time (PLT841 only)	8.0 ms @ 95 Vac input line and max rated load — All outputs loaded simultaneously		
Isolation	1500 Vac applied input to output, input to chassis, output to chassis		
Remote Sensing (+5 V output only)	Compensation for up to 0.5 Vdc drop in interconnecting leads.		
Transient Response	Output voltage will recover within regulation limits in 50 μ sec max in response to a 50% load step		
Ambient Temperature	Operating: 0°C to +50°C at full rated load, derated linearly to 70% at +70°C (See derating curve)		
	Storage: -40°C to +85°C		

DERATING CURVE

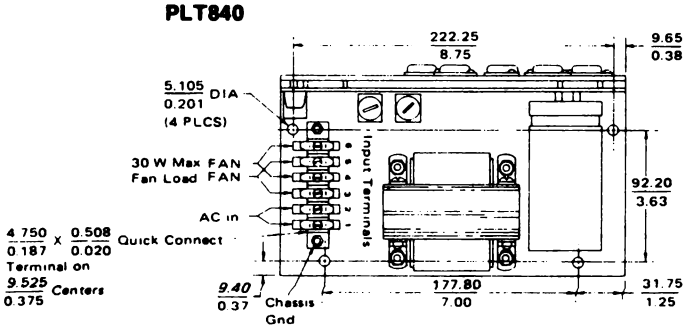


Curve 1 — with 50 CFM Forced Air Cooling
Curve 2 — Convection Cooling

Outline Drawings

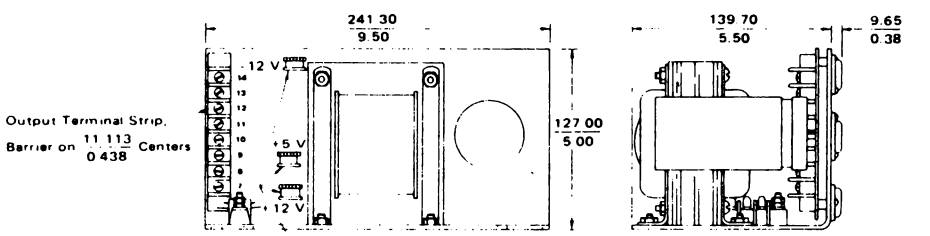
Unit Weight (approx): 11 lbs (5 Kg)
Chassis Finish: Black Anodized
All dimensions given as $\frac{\text{mm}}{\text{inches}}$

PLT840



Output Terminal	Function
14	-12 V Return
13	-12 V
12	+5 V
11	+5 V Sense
10	+5 V Return
9	+5 V Return Sense
8	+12 V
7	+12 V Return

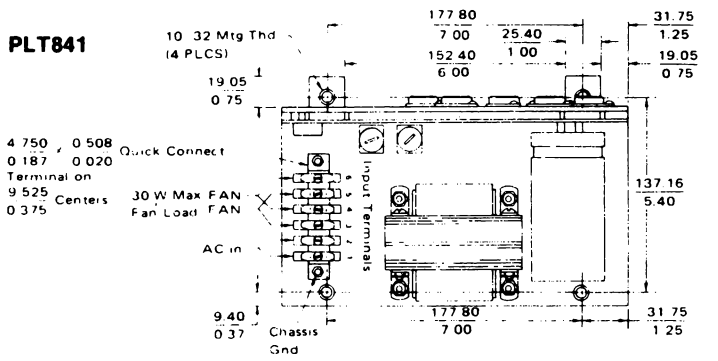
Input	Jumper
110 V	3-4, 5-6
230 V	4-5



DC Power Supplies PLT840, PLT841

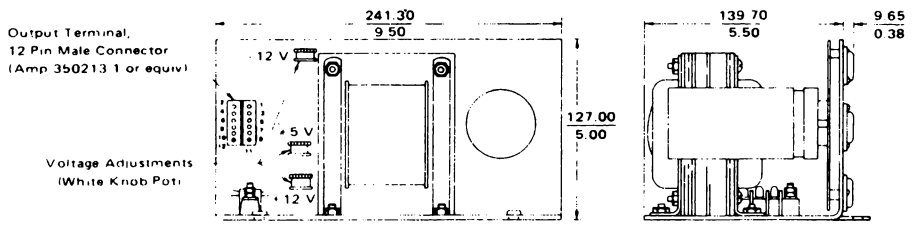
Unit Weight (approx): 11 lbs (5 Kg)
Chassis Finish: Black Anodized
All dimensions given as mm / inches

PLT841



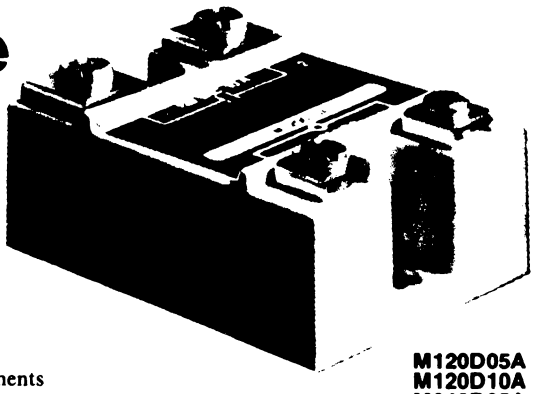
Output Terminal	Function
1 and 2	+5 V
3	+5 V Sense
4	+12 V Return
5	+5 V Return Sense
6	-12 V Return
7 and 9	+5 V Return
8	-12 V
10	+12 V
11 and 12	Not Used

Input	Jumper
110 V	3-4, 5-6
230 V	4-5



Solid-State Relays

Chassis Mount



M120D05A
M120D10A
M240D05A
M240D10A

- Zero Voltage Switching
- Photo Isolated
- Improved Input Characteristics
- Integrated Circuit Compatible
- High Output Transient Immunity
- Shock and Vibration Resistant
- High Surge Rating
- Designed to Meet UL and CSA Requirements
- All Solid-State
- Standard Package Dimensions.

This series of devices is specifically designed to provide reliable solid-state switching of high power ac loads. Units feature a choice of 120 or 240 Vac, 60 Hz line voltage ratings and output current ratings of either 5 or 10 amperes. All devices are optically isolated and utilize zero voltage turn-on and zero current turn-off to minimize line voltage transients. In addition, particular attention has been given to improving input characteristics.

These units are ideally suited for applications requiring interface from digital logic families to ac loads such as solenoids, motors, transformers, lamps, heaters, timers, etc. Typical applications include machine tool control, computer peripherals, process control, traffic control, business machines, heating controls, automatic test equipment and sequential power control circuits.

Electrical Specifications

Input Specifications (at -40°C to +80°C unless otherwise specified)

Parameter	Min	Max	Units
Control Voltage Range	3	32	Vdc
Input Current (at 5 V Control Voltage)	—	5.0	mA
Turn-On Voltage	—	3.0	Vdc
Turn-Off Voltage	1.0	—	Vdc
Isolation (Input to Output, Input to Case, Output to Case)	10^9	—	Ohms
Capacitance (Input to Output)	—	10	pF
Reverse Voltage Protection	50	—	Vdc
Dielectric Strength (Input to Output, Input to Case, Output to Case)	1500	—	Vac (RMS) 60 Hz

Output Specifications (at 25°C unless otherwise specified)

Output Current Rating (See Figure 3):			
M120D05A, M240D05A	—	5	Amps (RMS)
M120D10A, M240D10A	—	10	Amps (RMS)
Line Voltage Rating:			
M120D05A, M120D10A	—	140	Vac (RMS)
M240D05A, M240D10A	—	280	Vac (RMS)
Frequency Range	47	70	Hz
Peak Surge Current, Single-Cycle, 60 Hz (Mounting Base Temperature = +80°C; See Figure 4):			
M120D05A, M240D05A	—	5	Apeak
M120D10A, M240D10A	—	10	Apeak
Overvoltage Rating:			
M120D05A, M120D10A	300	—	Vpeak
M240D05A, M240D10A	600	—	Vpeak
Contact Voltage Drop (at Rated Current)	—	1.6	Vpeak
Off-State Leakage Current (TA = -40°C to +80°C):			
At 140 Vac (RMS): M120D05A, M120D10A	—	8	mA (RMS)
At 280 Vac (RMS): M240D05A, M240D10A	—	13	mA (RMS)
Off-State dv/dt	100	—	V/μs
Turn-On Time (60 Hz)	—	8.3	ms
Turn-Off Time (60 Hz)	—	16.6	ms
Thermal Resistance, Junction to Base (See Figure 3)	—	3.0	°C/Watt

Solid-State Relays
M120D05A, M120D10A, M240D05A, M240D10A

PART NUMBERING DEFINITIONS

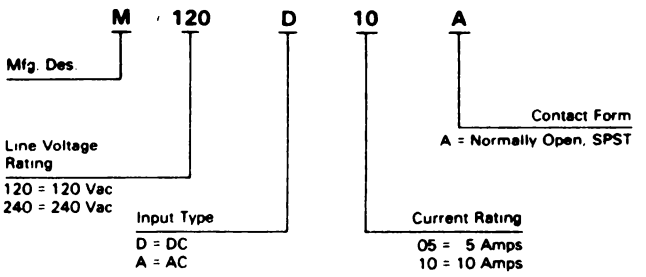


FIGURE 1 — CONTROL AND COUPLER CURRENT versus CONTROL VOLTAGE

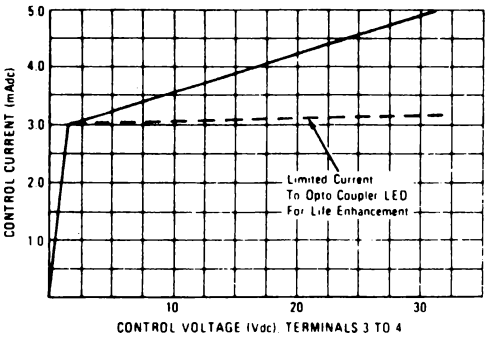


FIGURE 2 — CONTROL CHARACTERISTICS

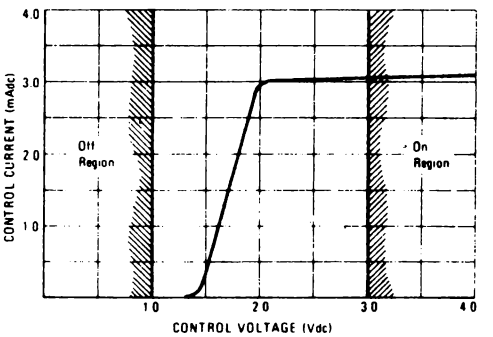


FIGURE 3 — MAXIMUM OUTPUT CURRENT versus AMBIENT TEMPERATURE

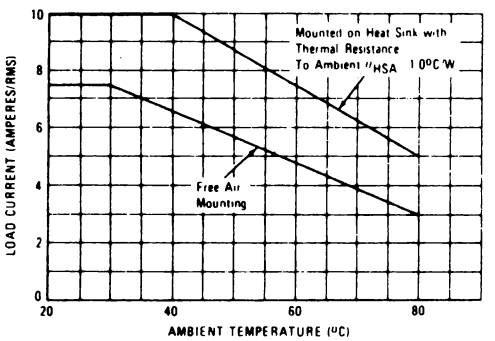
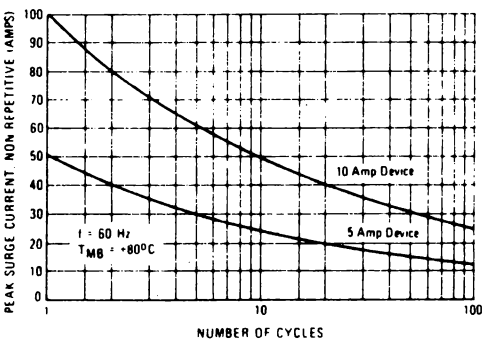
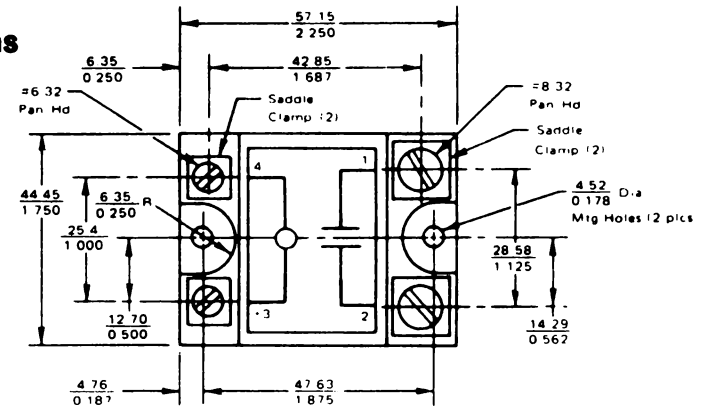


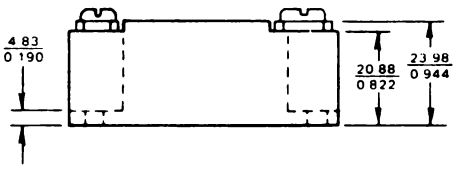
FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT



Solid-State Relays
M120D05A, M120D10A, M240D05A, M240D10A

Dimensions

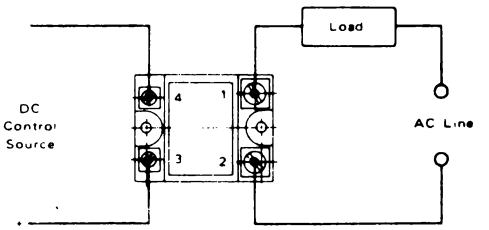




Ambient Temperature Range
Operating 40°C to +80°C
Storage 40°C to +100°C

Unit Weight (Approx) 110 grams
Standard Models are Furnished with Saddle Clamps 1/4"
Quick Connect Terminals May be Substituted on Request
All dimensions given as mm / inches

WIRING DIAGRAM

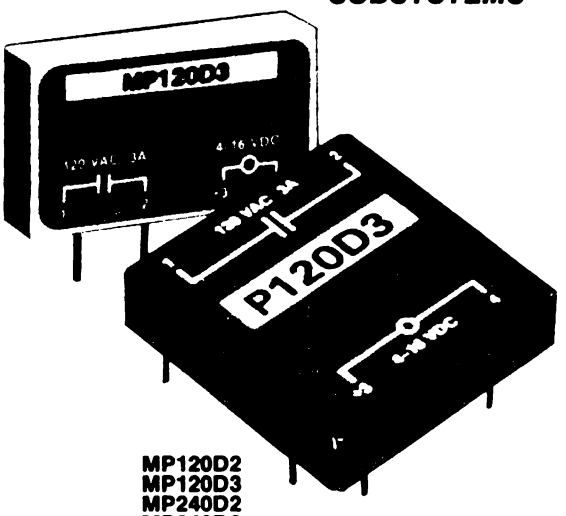


MOTOROLA

SUBSYSTEMS

Solid-State Relays

PC Mount



- Zero Voltage Switching
- Photo Isolated
- Integrated Circuit Compatible
- Shock and Vibration Resistant
- High Overvoltage Rating
- All Solid-State
- Built-In Snubber Network.

The P Series offers reliable solid-state switching featuring low profile construction for printed circuit board mounting with greater packaging density. The series consists of both 2- and 3-ampere versions and 120- and 240-volt units.

The MP Series offers the same electrical characteristics in a vertical mount package featuring only a 0.68 square inch footprint.

MP120D2
MP120D3
MP240D2
MP240D3

P120D2
P120D3
P240D2
P240D3

Electrical Specifications

Input Specifications

Parameter	Min	Max	Units
Turn-On Voltage	—	4	Vdc
Turn-Off Voltage	1	—	Vdc
Signal Input Impedance	500 Ohms Nominal*		
Dielectric Strength (Input to Output)	1500	—	Vac (RMS) 60 Hz

Output Specifications

Output Current Rating (See Figure 1):			
MP/P120D2, MP/P240D2	—	2	Amps (RMS)
MP/P120D3, MP/P240D3	—	3	Amps (RMS)
Load Voltage Rating:			
MP/P120D2, MP/P120D3	12	140	Vac (RMS)
MP/P240D2, MP/P240D3	24	280	Vac (RMS)
Frequency Range	25	65	Hz
Peak Surge Current (Single Cycle, 60 Hz):			
MP/P120D2, MP/P240D2	—	20	Amps (Peak)
MP/P120D3, MP/P240D3	—	55	Amps (Peak)
Overvoltage Rating:			
MP/P120D2, MP/P120D3	250	—	Vpeak
MP/P240D2, MP/P240D3	500	—	Vpeak
Contact Voltage Drop (at Rated Current)	—	1.6	Vpeak
Turn-On Time (60 Hz)	—	8.3	ms
Turn-Off Time (60 Hz)	—	8.3	ms
Off-State Leakage Current:			
At 140 Vac (RMS) MP/P120D2, MP/P120D3	—	5	mA (RMS)
At 280 Vac (RMS) MP/P240D2, MP/P240D3	—	5	mA (RMS)
Operating Temperature	-40	+100	°C

*220-Ohm Limiting Resistor in Series with Opto-Coupler Input

Solid-State Relays
P Series, MP Series

PART NUMBERING DEFINITIONS

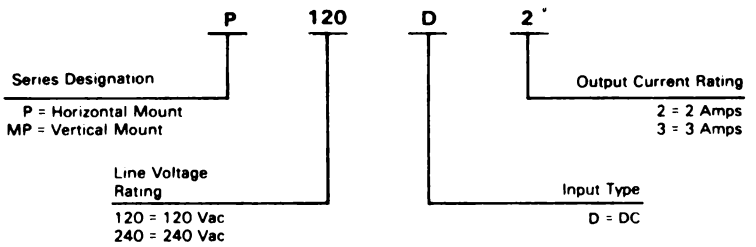
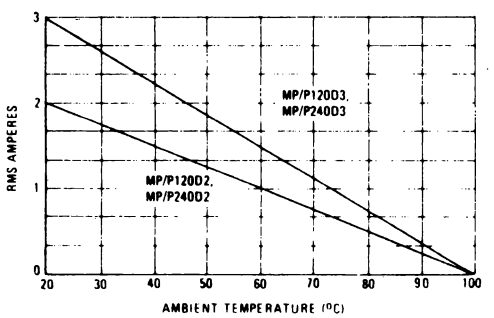


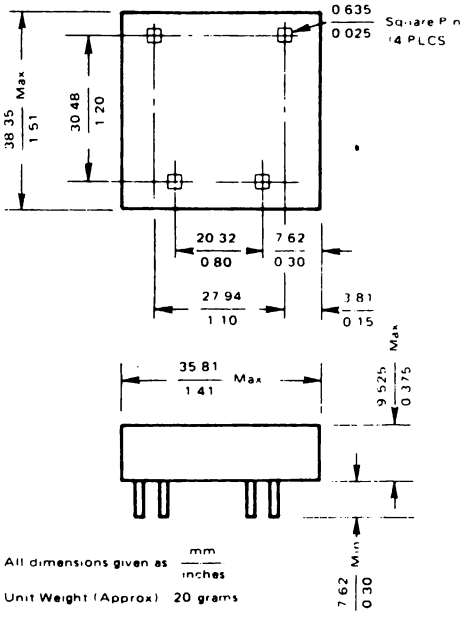
FIGURE 1 — MAXIMUM OUTPUT CURRENT versus AMBIENT TEMPERATURE



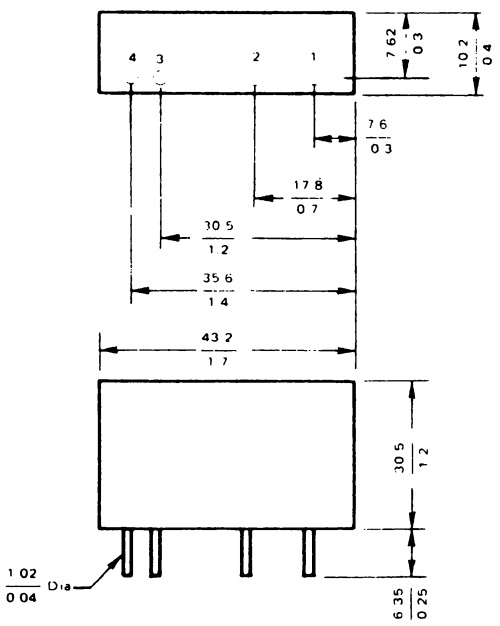
Solid-State
Relays
P Series, MP Series

Dimensions

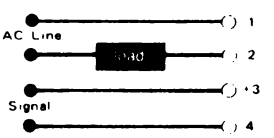
P Series



MP Series



WIRING DIAGRAM



MOTOROLA

IAC5

AC INPUT–LOGIC OUTPUT ISOLATION MODULE FOR MICROPROCESSOR INTERFACING

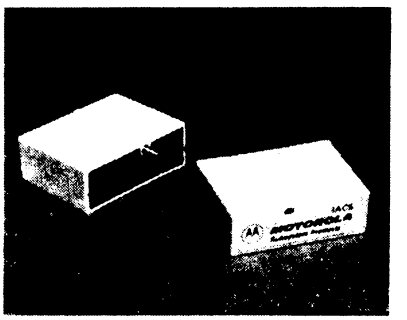
The IAC5 AC Input Module interfaces industrial AC signaling voltages with microprocessor input circuits, while providing high impedance isolation between the two systems. These modules, together with others from the IOM5 family, provide a means of serving all the input-output requirements of a microprocessor or computer-based control system. Card level systems using IOM5 modules will serve the Motorola EXORcisor system and micromodule product line.

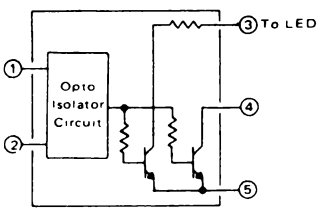
Features:

- Solid State Reliability
- Compatible with all 5-volt logic families: CMOS, TTL, LS, NMOS and PMOS
- Directly compatible with standard microprocessor input-output requirements
- Meets UL Isolation Requirements
- Compatible Second Source Available
- New Standard Package and Pin Outs

SUBSYSTEM PRODUCTS

INPUT-OUTPUT MODULE





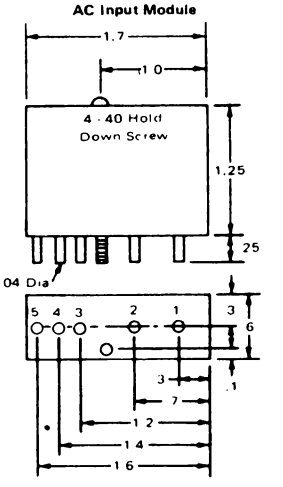
Simplified Circuit

SPECIFICATIONS

Rating	Value	Unit
Input Line Voltage	95–130	VAC
Input Current at 120 VAC Line Voltage	10	mA Maximum
Isolation Input to Output	1500	VAC (rms)
Allowable Input for No Output	1.5	mA*
Turn On Time Typical	10	ms
Maximum	20	ms
Turn-Off Time Typical	10	ms
Maximum	20	ms
Output Transistor Breakdown Voltage	30	Volts dc
Output Current	25	mA Maximum
Output Leakage at 30 Vdc, No Input	100	μA
LED Current	10	mA
Output Voltage Drop	0.4	Volt dc
Logic Supply Voltage	4.5–6.0	Volts dc
Operating Temperature Range	-40 to +80	°C

*Leakage Current of Limit Switches, Etc

AC Input Module



Dimensions in inches

MOTOROLA

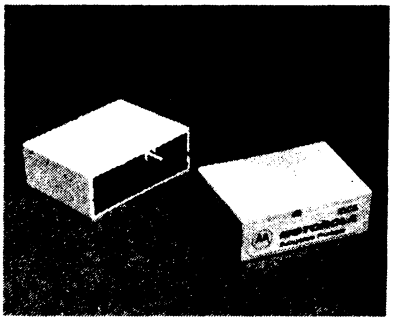
IDC5

DC INPUT–LOGIC OUTPUT ISOLATION MODULE FOR MICROPROCESSOR INTERFACING

SUBSYSTEM PRODUCTS

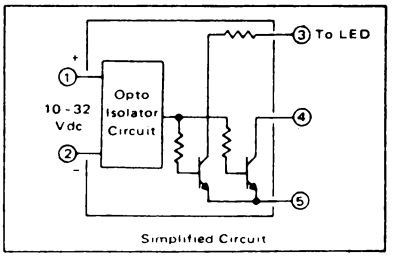
INPUT-OUTPUT MODULE

The IDC5 DC Input Module interfaces industrial DC signaling voltages with microprocessor input circuits, while providing high impedance isolation between the two systems. These modules, together with others from the IOM5 family, provide a means of serving all the input-output requirements of a microprocessor or computer-based control system. Card level systems using IOM5 modules will serve the Motorola EXORcisor system and micromodule product line.



Features:

- Solid State Reliability
- Compatible with all 5-volt logic families CMOS, TTL, LS, NMOS and PMOS
- Directly compatible with standard microprocessor input-output requirements
- Meets UL Isolation Requirements
- Compatible Second Source Available
- New Standard Package and Pin-Outs

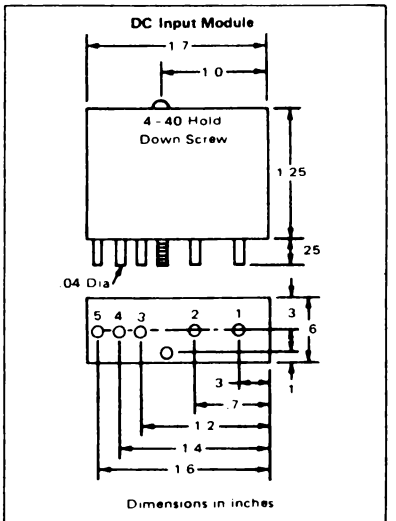


Simplified Circuit

SPECIFICATIONS

Rating	Value	Unit
Input Line Voltage	10 - 32	Volts dc
Input Current	34	mA Maximum
Isolation Input to Output	1500	Volts ac (rms)
Capacitance Input to Output	8	pF Maximum
Allowable Input for No Output	2	mA*
Turn-On Time Typical	2	ms
Maximum	5	ms
Turn-Off Time Typical	4	ms
Maximum	6	ms
Output Transistors Breakdown Voltage	30	Volts dc
Output Current	25	mA
Output Leakage at 30 Vdc, No Input	100	μA
Output Voltage Drop 25 mA Load	0 4	Vdc
Logic Supply Voltage	4 5 to 6	Vdc
Logic Supply Current	12	mA Maximum
LED Current	10	mA
Operating Temperature Range	-40 to +80	°C

*Leakage Current of Limit Switches, Etc



Dimensions in inches

MOTOROLA

OAC5

AC LOAD–LOGIC INPUT ISOLATION MODULE FOR MICROPROCESSOR INTERFACING

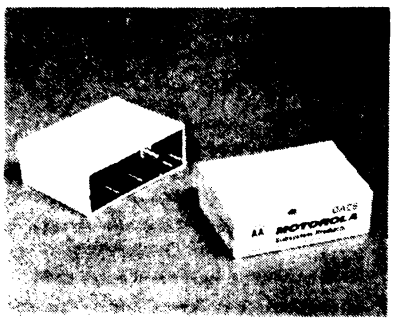
The OAC5 AC Output Module interfaces industrial 120 VAC loads with microprocessor output circuits, while providing high impedance isolation between the two systems. These modules, together with others from the IOM5 family, provide a means of serving all the input-output requirements of a microprocessor or computer-based control system. Card level systems using IOM5 modules will serve the Motorola EXORcisor system and micromodule product line.

Features:

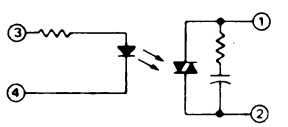
- Solid State Reliability
- Compatible with all 5-volt logic families: CMOS, TTL, LS, NMOS and PMOS
- Directly compatible with standard microprocessor input-output requirements
- Meets UL Isolation Requirements
- Compatible Second Source Available
- New Standard Package and Pin-Outs
- Zero Voltage Switching

SUBSYSTEM PRODUCTS

INPUT-OUTPUT MODULE



Zero voltage switching circuit not shown



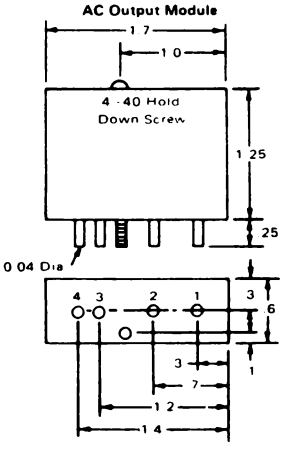
Simplified Circuit

SPECIFICATIONS

Rating	Value	Unit
Line Voltage	12 to 140	VAC
Current Rating	3	Amps*
1-Cycle Surge	55	Amps Peak
Signal Input Resistance	220	Ω
Signal Pick-Up Volts	3	Volts dc
Signal Drop-Out Volts	1	Volt
Peak Repetitive Voltage	400	Volts
Maximum Contact Drop	1.6	Volts
Off State Leakage	5	mA (rms)
Minimum Load Current	20	mA
Isolation Input to Output	1500	Volts (rms)
Capacitance Input to Output	8	pF Maximum
Operating Temperature Range	-40 to +80	°C

*Derate .033 Amp/°C from 20°C.

AC Output Module



Dimensions in inches

MOTOROLA

ODC5

DC LOAD–LOGIC INPUT ISOLATION MODULE FOR MICROPROCESSOR INTERFACING

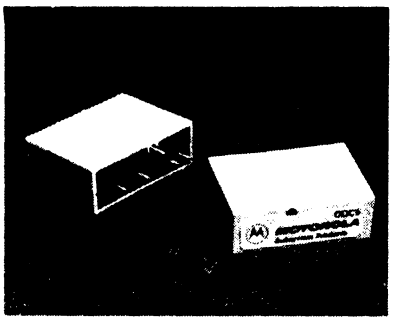
The ODC5 DC Output Module interfaces industrial DC load voltages with microprocessor input circuits, while providing high impedance isolation between the two systems. These modules, together with others from the IOM5 family, provide a means of serving all the input-output requirements of a microprocessor or computer-based control system. Card level systems using IOM5 modules will serve the Motorola EXORcisor system and micromodule product line.

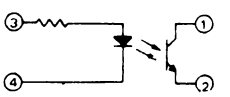
Features:

- Solid State Reliability
- Compatible with all 5-volt logic families: CMOS, TTL, LS, NMOS and PMOS
- Directly compatible with standard microprocessor input-output requirements
- Meets UL Isolation Requirements
- Compatible Second Source Available
- New Standard Package and Pin-Outs

SUBSYSTEM PRODUCTS

INPUT-OUTPUT MODULE





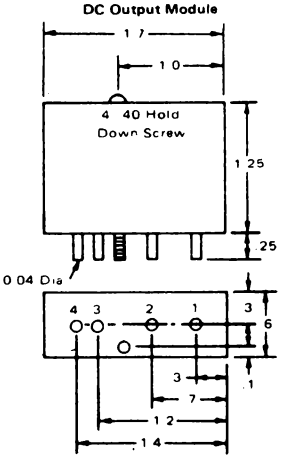
Simplified Circuit

SPECIFICATIONS

Rating	Value	Unit
Load Voltage Rating	60	Volts dc Maximum
Output Current Rating	3	Amps dc*
Off State Leakage	1	mA Maximum
Isolation Input to Output	1500	VAC (rms)
Signal Pick-Up Voltage	3	Volts
Signal Drop-Out Voltage	1	Volt dc
Signal Input Impedance	220	Ω
1 Second Surge	5	Amps Peak
Turn-On Time	500	μs
Turn-Off Time	2.5	ms
Operating Temperature Range	-40 to +80	°C

*Derate 0.033 Amp/°C from 20°C

DC Output Module



Dimensions in inches.

MOTOROLA

MS16

I/O MOUNTING SYSTEM

The MS16 is a socketed printed circuit board for mounting IAC5, OAC5, IDC5, and ODC5 Input/Output modules. The edge mounted barrier strip accommodates 3/16-inch quick connects or unterminated wires to 12 Ga. A five-ampere field replaceable fuse protects each module and a high brightness LED status indicator shows the state of each module. Supplied color coding markers indicate to field personnel the type of module used in each module location. The card edge connector pattern mates to a fifty-pin connector. This allows direct interfacing with flat cables to minicomputers and microprocessor systems. As any module type may be used in any module location, the system is unconstrained. Power may be supplied by the separate two-point barrier strip, or supplied through the edge connection by installation of jumpers.

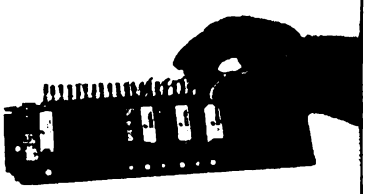
Standardization of mounting dimensions and connector give users multiple sourcing for this new standard I/O system.

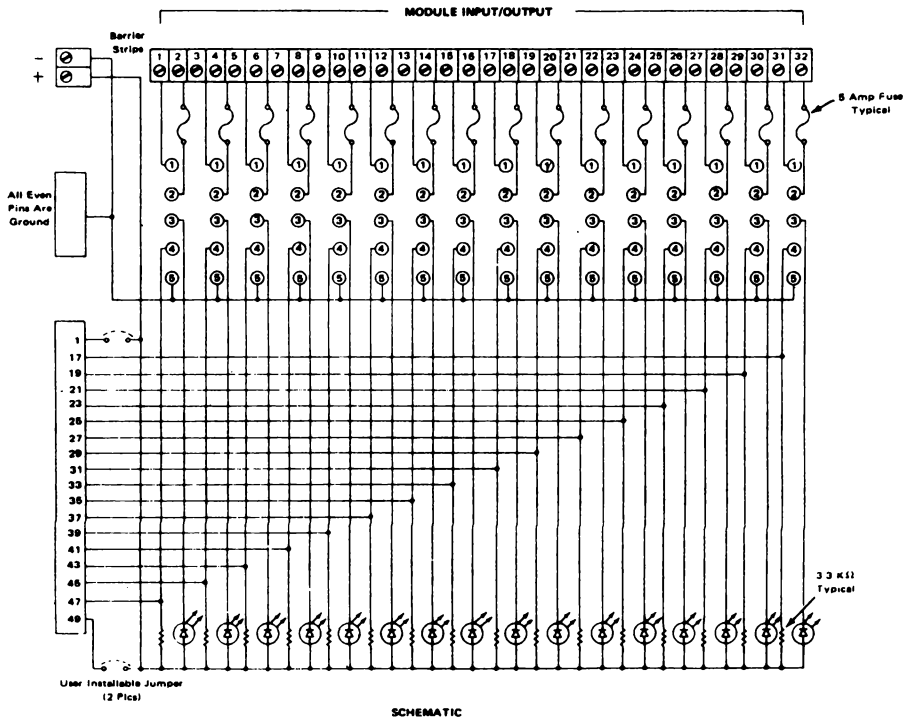
FEATURES

- Accommodates 16 Modules
- All Modules Protected by Fuses
- All Module Locations Color Codable
- Any Module Type Useable in Any Socket
- Quick Connects or Unterminated Field Wiring
- Standard Connectors
- Standard Mounting Dimensions

SUBSYSTEMS PRODUCTS

INPUT-OUTPUT MODULE MOUNTING SYSTEM





SCHEMATIC

DIMENSION DRAWING