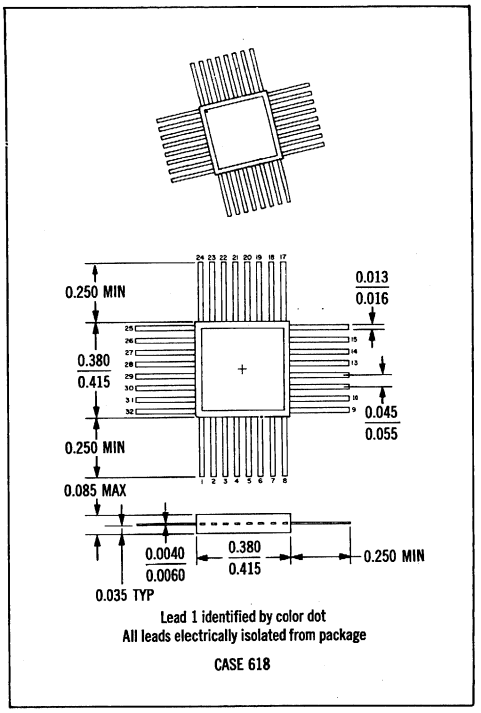
COMPLEX ARRAYS

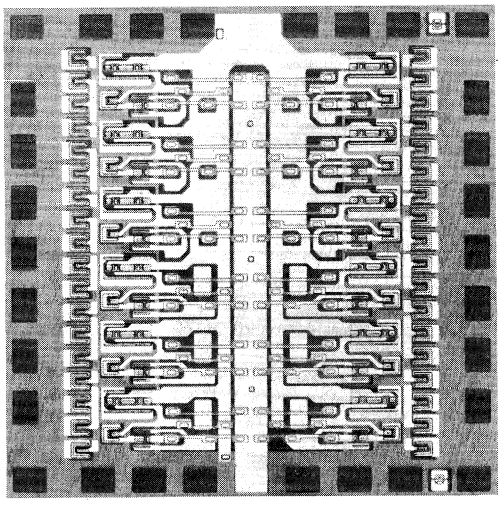
XC157

FOR COMPLEX FUNCTIONS USING CUSTOM 2nd LAYER METALIZATION

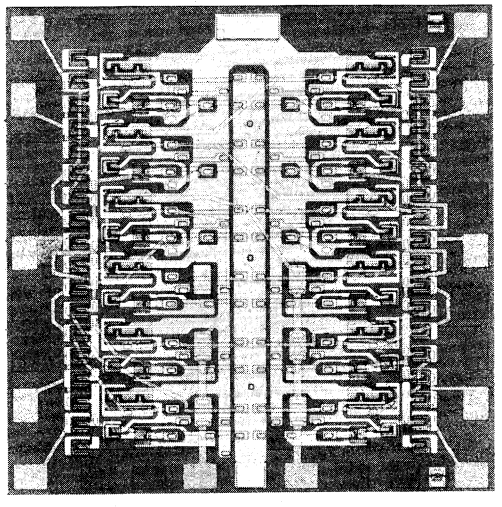
The XC157 is a monolithic 12-gate array developed to introduce a form of custom MSI. This array also serves as a vehicle for establishing customer-supplier interfaces which will ultimately lead toward more complex MSI and LSI systems. Each gate is intraconnected with a first layer of metalization but contains uncommited input logic diodes and output load resistors for increased design flexibility. The diode and load resistor intraconnections and the subsequent gate-to-gate interconnections are made with your custom-designed second layer of metalization.



From this silicon monolithic circuit array of 12 MDTL gates . . .
XC157



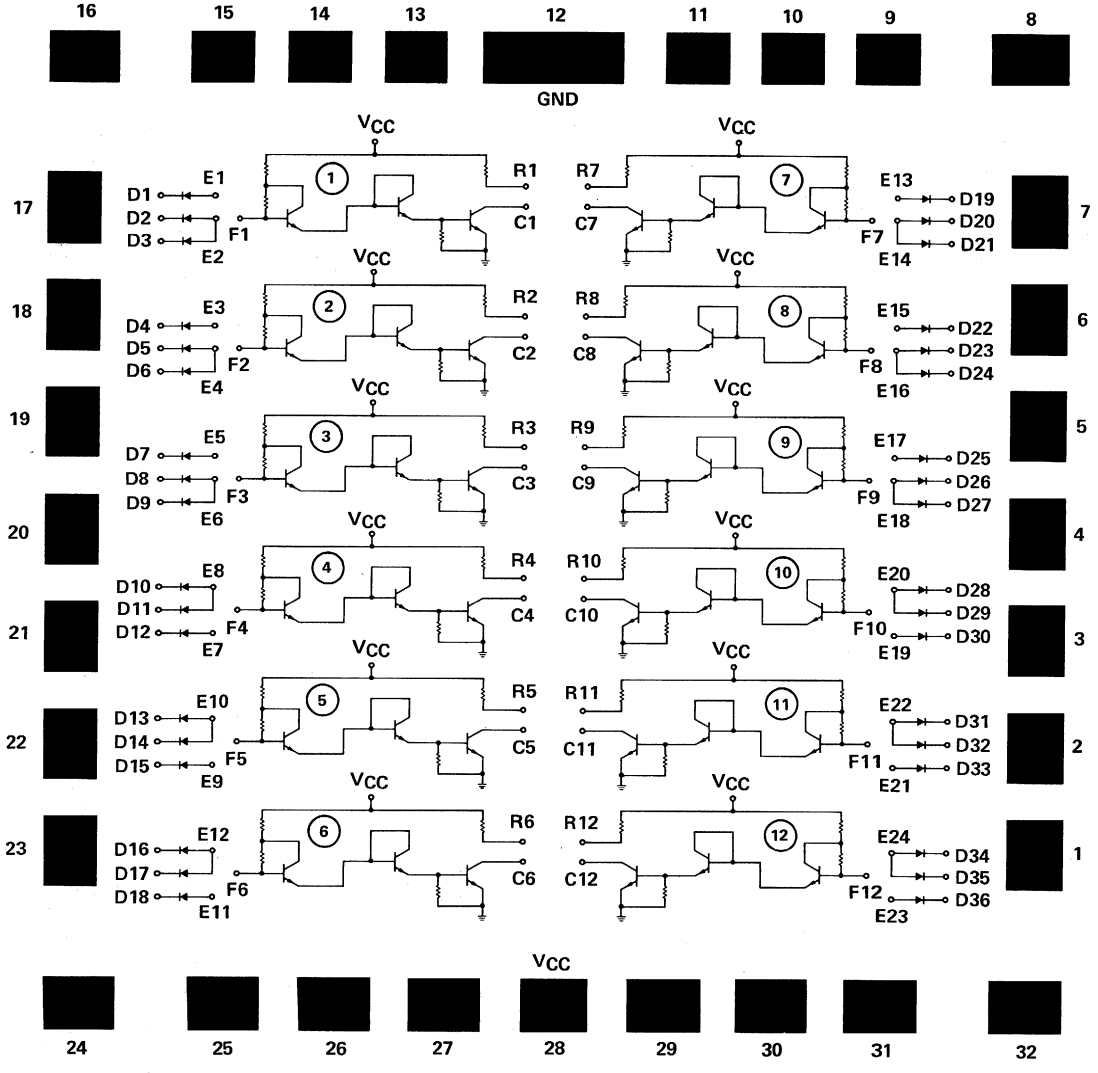
. . . you can design custom complex circuit functions such as . . .
4-CHANNEL CLOCKED LATCH WITH 2ND METALIZATION



SECOND METAL LAYER DESIGN PROCEDURE:

1. Sketch desired logic configuration, such as shown by Custom Design Examples. Consult CIRCUIT RULES and use the schematic diagram, Figure 1, as a reference.
2. Show desired interconnections on the circuit schematic (Figure 1). Prepare a preliminary layout, on Figure 2, of the required interconnections for a second layer metalization using the connection points designated on Figure 1.
3. Transfer resultant circuit connections to a node routing list (see example on page 8-8) for use as a guide, using the pad designations shown on Figure 2. On the same routing list indicate interconnection pads not used.
4. Prepare test specification, including test sequence, for acceptance testing of the final product in accordance with the electrical characteristics given for the individual gate. State logic equation to define required input-output relationships. When logic is sequential in nature, (i.e., flip-flops, counting elements, etc.) include timing diagram.
5. Forward items 1 thru 4 to your nearest Motorola Sales Office for product price and delivery quotation.

FIGURE 1 — CHIP SCHEMATIC



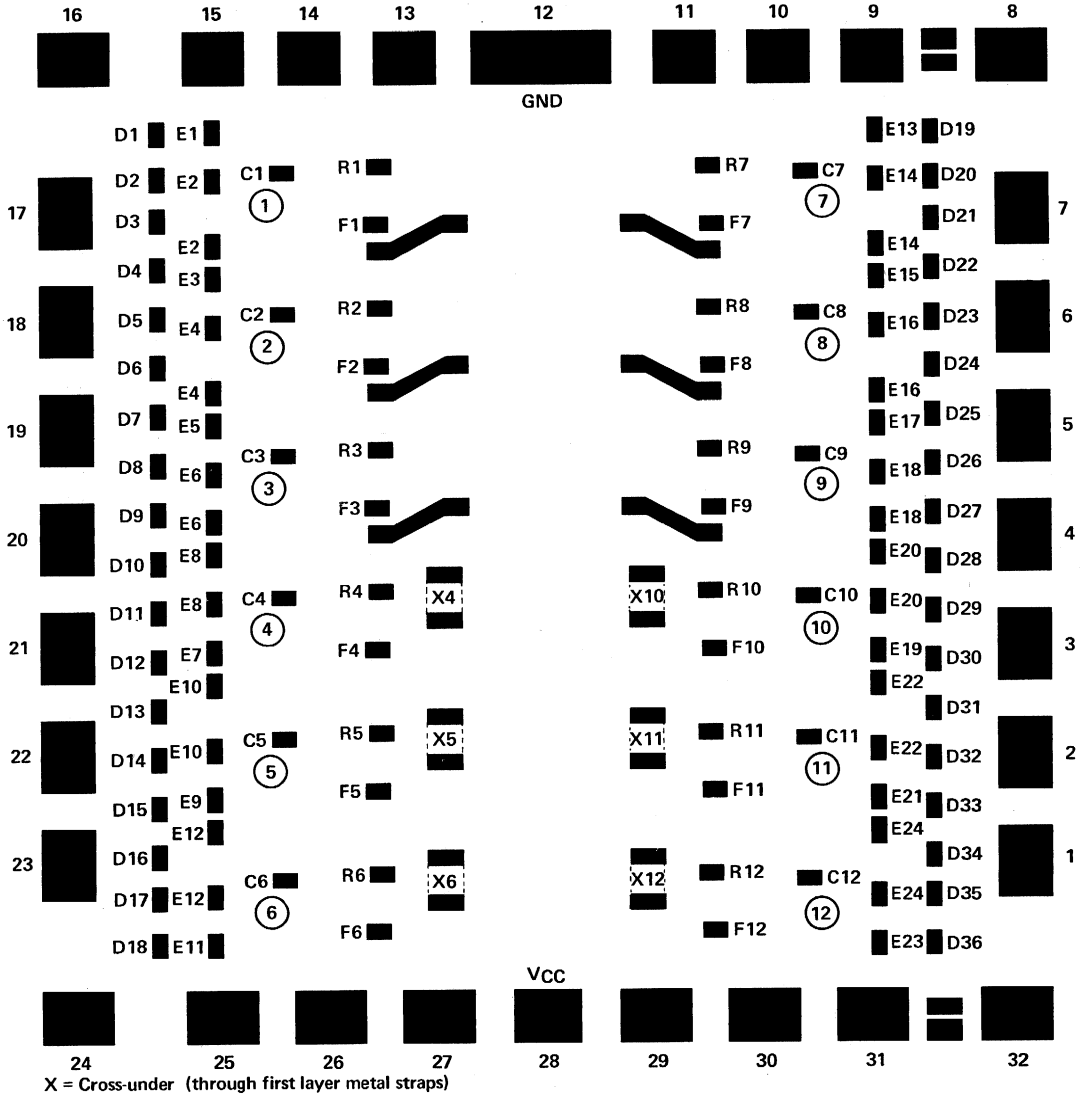
Cross-unders available as shown in Figure 2

CIRCUIT RULES:

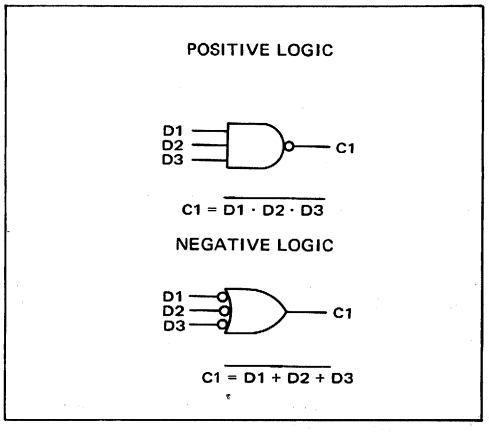
1. The number of inputs to any individual gate may be expanded to a maximum of 10 diodes.
2. For any individual gate the maximum allowable fan-out external to the package is limited to 5 loads. However, fan-out of any individual gate is allowable up to 10, if 5 of the fan-outs are internal and on the same side of the chip as the driver (e.g., Gate 1 must not drive Gates 7 thru 12); otherwise each internal fan-out must be subtracted from the allowable external fan-out of 5.
3. Each load resistor (R_L) used represents a fan-out load of one (1).
4. Collector ORing is allowable. Where one common load resistor is used, six gate outputs may be tied together.

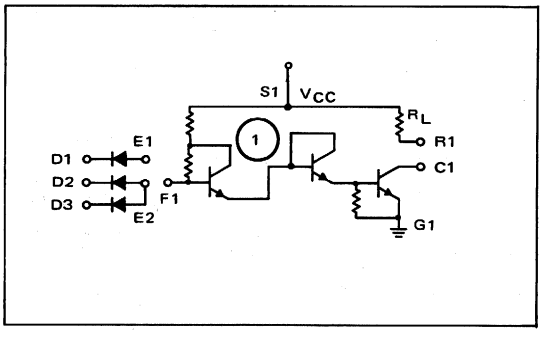
FIGURE 2 – INTERCONNECTION PAD LAYOUT

Points on the first metalization layer are made available through pads designated by letters with numbers on both Figures 1 and 2 (e.g., R1, D22, etc.). These pads are used to make the circuit interconnections discussed in the sections on design procedure and circuit rules, through use of a second layer of metalization. The bonding pads are designated by number only and correspond to the number system of the 32-pin flat package. Connection to these bonding pads must also be shown for the interconnecting metalization.



X = Cross-under (through first layer metal straps)





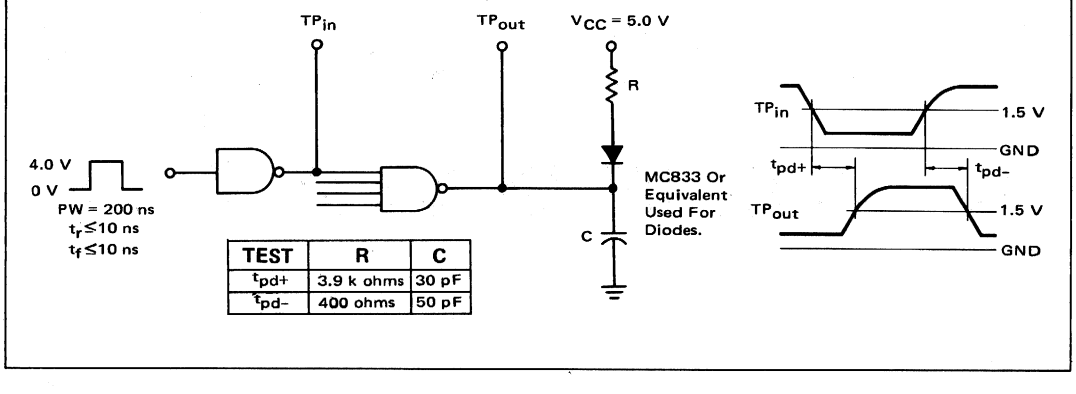
ELECTRICAL CHARACTERISTICS FOR INDIVIDUAL GATES

E1 and E2 are connected to F1; R1 is connected to C1; S1 and G1 are connected to pads 28 and 12 through the 1st layer of metalization.

NOTE: These characteristics are given to assist the user in specifying the input-output characteristics of the required complex function.

						TEST CURRENT / VOLTAGE VALUES @ T_A=25°C										
						mA		Volts								
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCH}	V_{max}	
						15.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	5.50	8.00	
		Pad Under Test	Test Limits +25°C			TEST CURRENT / VOLTAGE APPLIED TO PADS LISTED BELOW:										
Characteristic	Symbol		Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	C1	-	0.45	Vdc	C1	-	-	D1,D2,D3	-	-	-	S1	-	-	G1
	V_{OH}	C1	2.60	-	↓	-	C1	D1	-	-	-	-	↓	-	-	↓
				-		-	↓	D2	-	-	-	-		-	-	
				-		-		D3	-	-	-	-		-	-	
Short-Circuit Current	I_{SC}	C1	-	-1.63	mAdc	-	-	-	-	-	-	-	-	S1	-	D1,C1,G1
Reverse Current	I_R	D1	-	5.0	μAdc	-	-	-	-	-	D1	-	-	S1	-	D2,D3,G1
		D2	-	↓	↓	-	-	-	-	-	D2	-	-	↓	-	D1,D3,G1
		D3	-			-	-	-	-	-	D3	-	-		-	D1,D2,G1
Output Leakage Current	I_{CEX}	C1	-	50	μAdc	-	-	-	-	-	-	C1,S1	-	-	-	D1,G1
Forward Current	I_F	D1	-	-1.5	mAdc	-	-	-	-	D1	D2,D3	-	-	S1	-	G1
		D2	-	↓	↓	-	-	-	-	D2	D1,D3	-	-	↓	-	↓
		D3	-			-	-	-	-	D3	D1,D2	-	-		-	
Drain Current per Gate	I_{PDH}	S1	-	4.0	mAdc	-	-	-	-	-	-	-	S1	-	-	G1
	I_{max}	S1	-	6.8	mAdc	-	-	-	-	-	-	-	-	-	S1	D1,G1
Switching Times						Pulse In	Pulse Out									
	t_{pd+}	C1	25	80	ns	D1	C1	-	-	-	-	-	S1	-	-	G1
	t_{pd-}	C1	10	35	ns	D1	C1	-	-	-	-	-	S1	-	-	G1

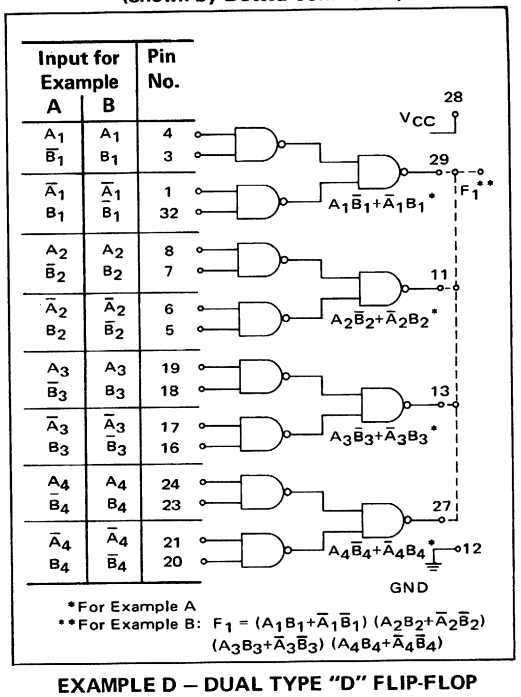
EQUIVALENT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

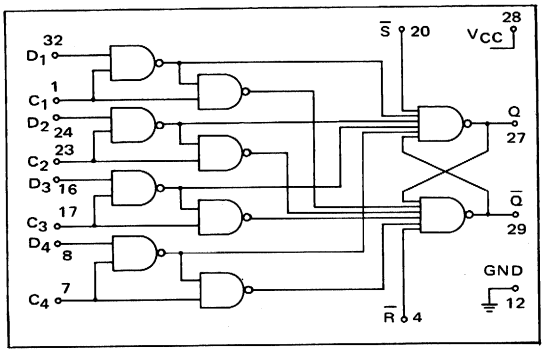
CUSTOM DESIGN EXAMPLES

EXAMPLE A – QUAD EXCLUSIVE "OR" GATE
or
EXAMPLE B – 4-BIT COMPARATOR
(Shown by Dotted Connection)

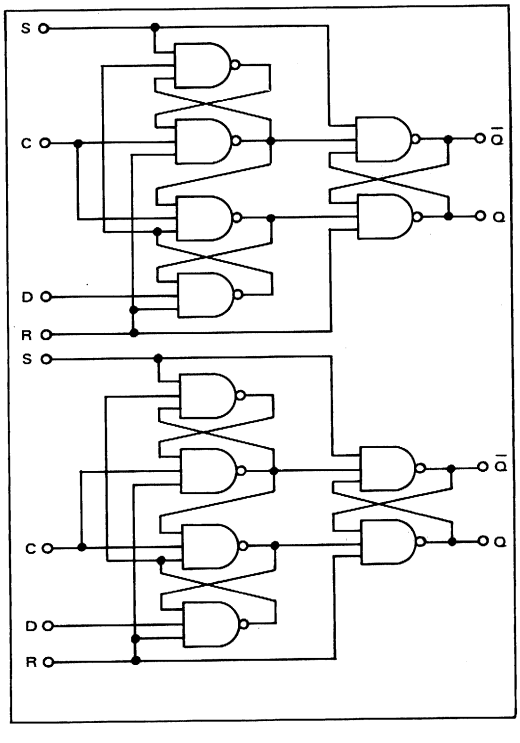


*For Example A
**For Example B: $F_1 = (A_1B_1+\bar{A}_1\bar{B}_1)(A_2B_2+\bar{A}_2\bar{B}_2)(A_3B_3+\bar{A}_3\bar{B}_3)(A_4B_4+\bar{A}_4\bar{B}_4)$

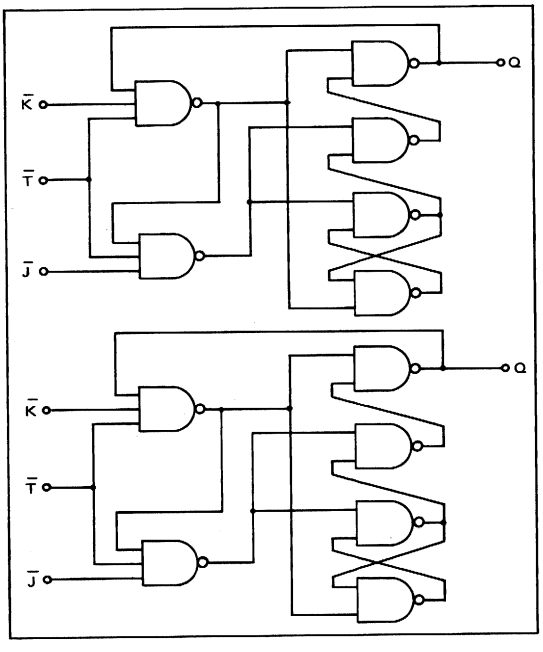
EXAMPLE C – 4-CHANNEL CLOCKED LATCH



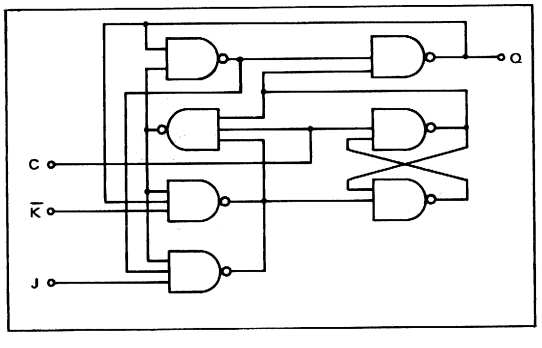
EXAMPLE D – DUAL TYPE "D" FLIP-FLOP



EXAMPLE E – DUAL TYPE "T" FLIP-FLOP



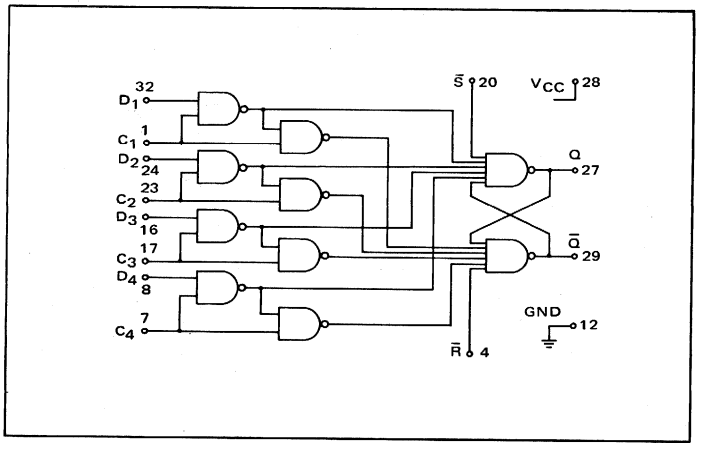
EXAMPLE F – J-$\bar{K}$ FLIP-FLOP



EXAMPLE OF PROCEDURE TO BE FOLLOWED

(USING CUSTOM DESIGN EXAMPLE C: 4-CHANNEL CLOCKED LATCH)

LOGIC DIAGRAM



NODE ROUTING LIST

D2-16	E12-F6
D3-D5-17	D12-R12-C12-D32
R1-C1-D6-D8	D35-32
D9-20	E24-F12
E5-E6-E7-E8-F3	D33-D34-1
D11-D13-C6-R6	F11-E21-E22
D14-D16-23	E17-E18-E19-E20-F9
D17-24	C11-R11-D29
E2-F1	D28-R3-C3-27 (thru X5, X6)
D7-R7-C7-D24	E16-F8
C2-R2-D26	D25-C8-R8
E4-F2	D21-D23-7
D10-R9-C9-29 (thru X10, X11, X12	D20-8
C5-R5-D30	E14-F7
E10-F5	D27-4

NODES NOT USED

D1	E11
D4	E13
D15	E15
D18	E23
D19	C4
D22	C10
D31	R4
D36	R10
E1	F4
E3	F10
E9	X4

ACCEPTANCE SPECIFICATION

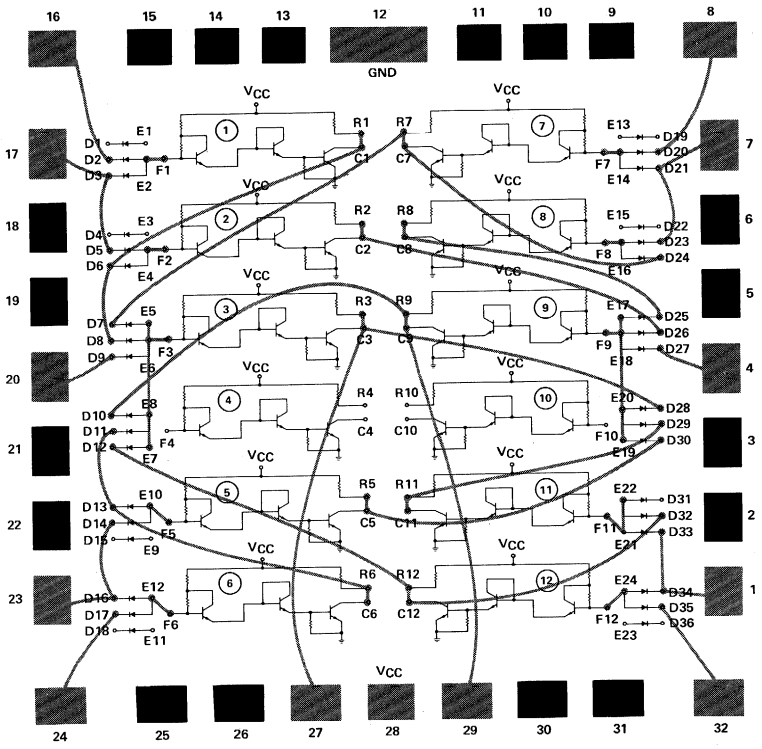
. . . to be prepared with format similar to that shown on page 8-6.

LOGIC EQUATION
and/or
TIMING DIAGRAM (when applicable)

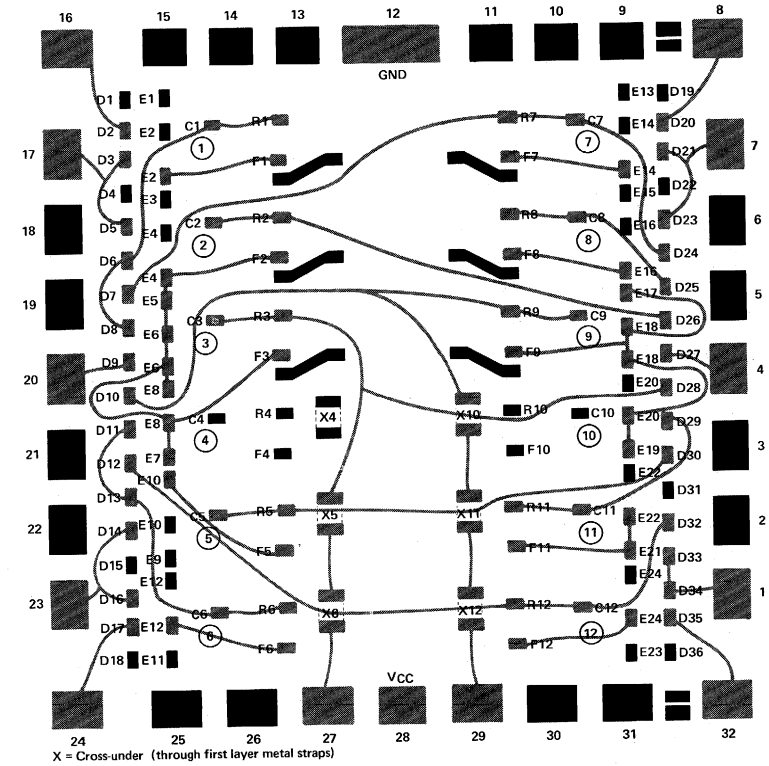
The process technology represented by the XC157 is a significant and necessary step for large-scale integration. It is, however, just a forerunner of the more complex arrays presently in development. Arrays with greater complexities and logic power utilizing other logic circuitry will soon become available. From these arrays circuits such as multiple independent Type D flip-flops, decade counters, shift registers, and complex ripple counters can be derived.

EXAMPLE OF PROCEDURE (continued)

CIRCUIT SCHEMATIC



INTERCONNECTION PAD LAYOUT



X = Cross-under (through first layer metal straps)