MOTOROLA

MC3470

Advance Specifications and Applications Information

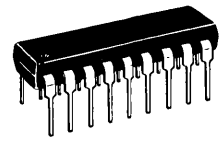
FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 5.0%

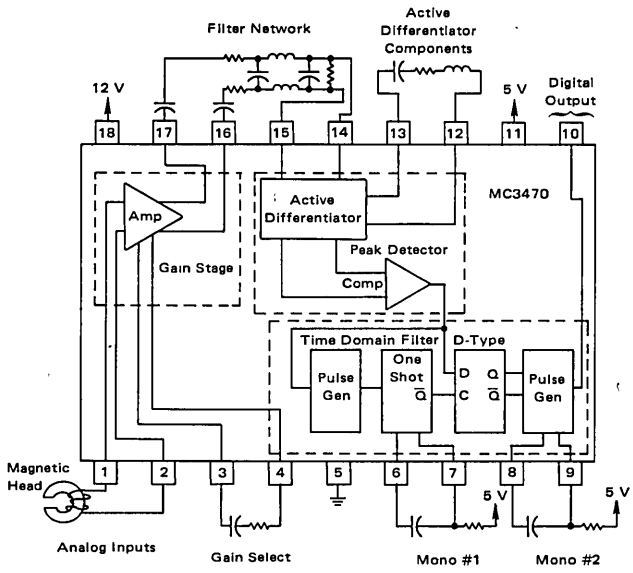
FLOPPY DISK READ AMPLIFIER SYSTEM

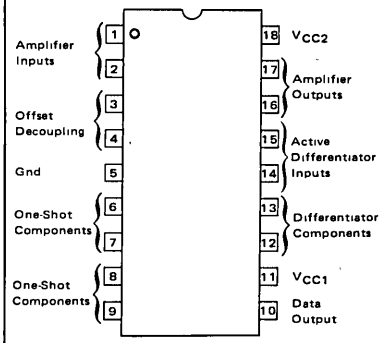
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701-01

TYPICAL APPLICATION





This is advance information and specifications are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS (Note 1)(T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V_{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V_I	−0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V_O	−0.2 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature Plastic Package	T_J	150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provices conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
GAIN AMPLIFIER SECTION						
Differential Voltage Gain (f = 200 kHz, V_{iD} = 5.0 mV(RMS))	2	A_{VD}	80	100	120	V/V
Input Bias Current	3	I_{IB}	–	−10	−25	μA
Input Common Mode Range Linear Operation (5% max THD)		v_{iCM}	−0.1	–	1.0	V
Differential Input Voltage Linear Operation (5% max THD)		v_{iD}	–	–	25	mVp-p
Output Voltage Swing Differential	2	v_{oD}	3.0	4.0	–	Vp-p
Output Source Current, Toggled		I_O	–	8.0	–	mA
Output Sink Current, Pins 16 and 17	4	I_{OS}	2.8	4.0	–	mA
Small Signal Input Resistance (T_A = 25°C)		r_i	100	250	–	kΩ
Small Signal Output Resistance, Single-Ended (T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V		r_o	–	15	–	Ω
Bandwidth, −3.0 dB (v_{iD} = 2.0 mV(RMS), T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	2	BW	5.0	–	–	MHz
Common Mode Rejection Ratio (T_A = 25°C, f = 100 kHz, A_{VD} = 40 dB, v_{in} = 200 mVp-p, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	5	CMRR	50	–	–	dB
V_{CC1} Supply Rejection Ratio (T_A = 25°C, V_{CC2} = 12 V, 4.75 ≤ V_{CC1} ≤ 5.25 V, A_{VD} = 40 dB)		–	50	–	–	dB
V_{CC2} Supply Rejection Ratio (T_A = 25°C, V_{CC1} = 5.0 V, 10 V ≤ V_{CC2} ≤ 14 V, A_{VD} = 40 dB)		–	60	–	–	dB
Differential Output Offset (T_A = 25°C, v_{iD} = v_{in} = 0 V)		V_{DO}	–	–	0.4	V
Common Mode Output Offset (v_{iD} = V_{in} = 0 V, Differential and Common Mode)		V_{CO}	–	3.0	–	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T_A = 25°C)	22	e_n	–	15	–	μV(RMS)

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 ($V_{OD} = V_{CC1}$)	6	I_{OD}	1.0	1.4	–	mA
Peak Shift (f = 250 kHz, v_{ID} = 1.0 Vp-p, i_{cap} = 500 μA, where $PS = 1/2 \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	7, 8	PS	–	–	5.0	%
Differentiator Input Resistance, Differential		r_{ID}	–	30	–	kΩ
Differentiator Output Resistance, Differential (T_A = 25°C)		r_{oD}	–	40	–	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = −0.4 mA)	9	V_{OH}	2.7	–	–	V
Output Voltage Low Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8.0 mA)	10	V_{OL}	–	–	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	–	–	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	–	–	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A,B}$	500	–	4000	ns
Timing Accuracy Mono #1 (t1 = 1.0 μs = 0.625 R1C1 + 200 ns) (R1 = 6.4 kΩ, C1 = 200 pF) Accurancy guaranteed for R1 in the range 1.5 kΩ ≤ R1 ≤ 10 kΩ and C1 in the range 150 pF ≤ C1 ≤ 680 pF. Note: To minimize current transients, C1 should be kept as small as is convenient.	12,13	E_{t1}	85	–	115	%
Timing Range Mono #2	11, 12	t2	150	–	1000	ns
Timing Accuracy Mono #2 (t2 = 200 ns = 0.625 R2C2) (R2 = 1 6 kΩ, C2 = 200 pF) Accuracy guaranteed for 1.5 kΩ ≤ R2 ≤ 10 kΩ, 100 pF ≤ C2 ≤ 800 pF	12, 13	E_{t2}	85	–	115	%

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MC3470 CIRCUIT SCHEMATIC

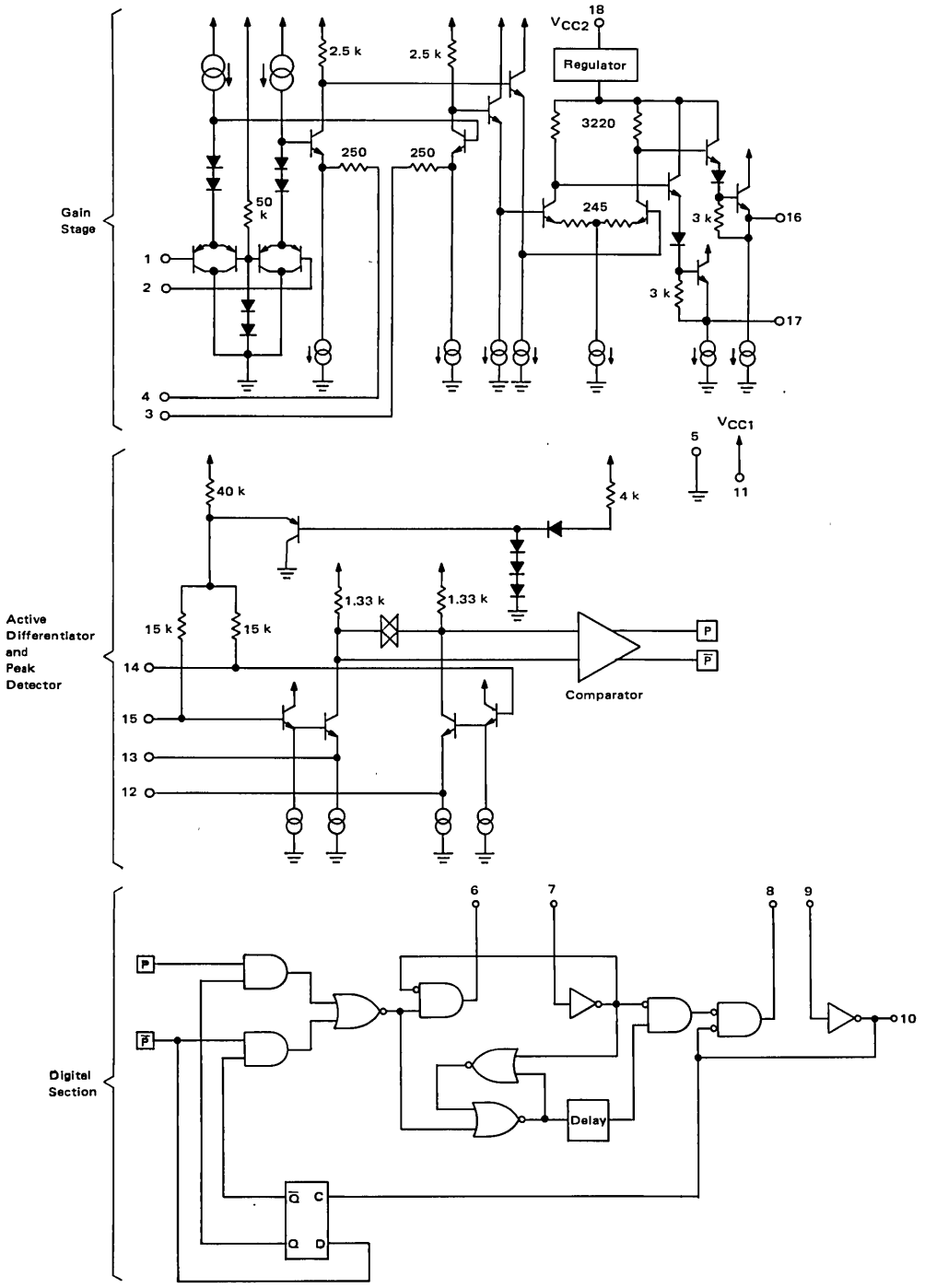

FIGURE 1 – POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

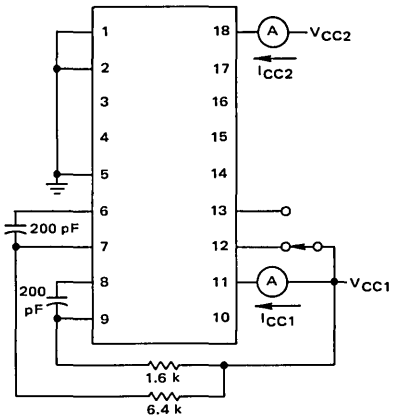

FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

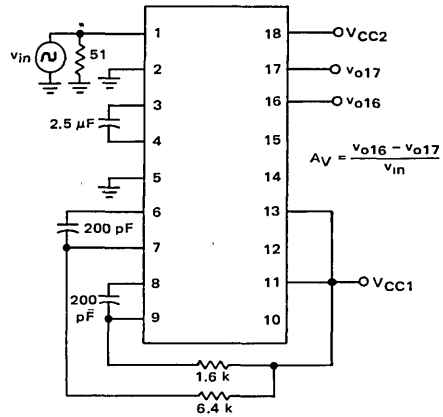

FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, I_{IB}

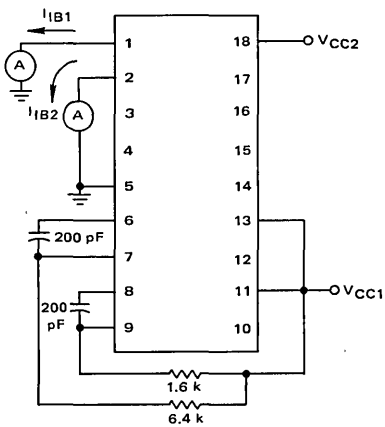

FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17

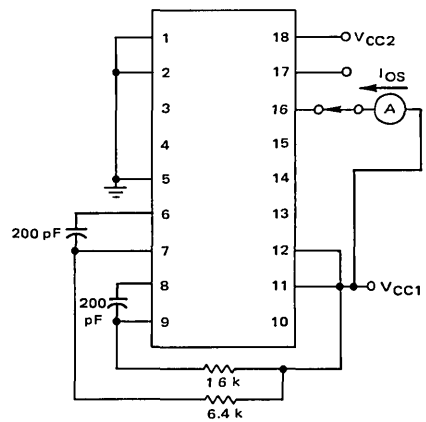

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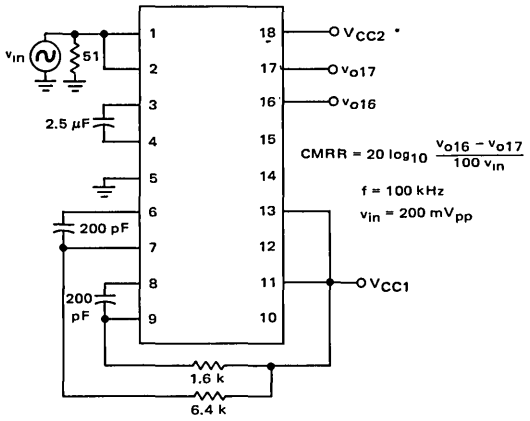
FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR



NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz *performance.*

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

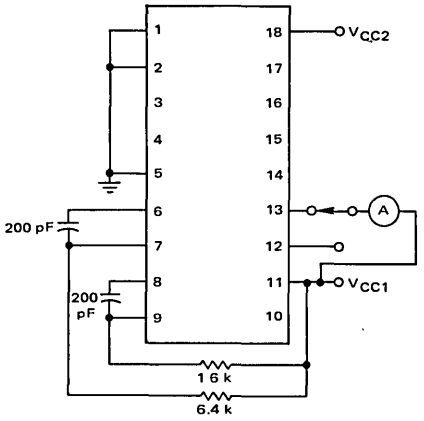


FIGURE 7 – PEAK SHIFT, PS

See Figure 8 for Output Waveform

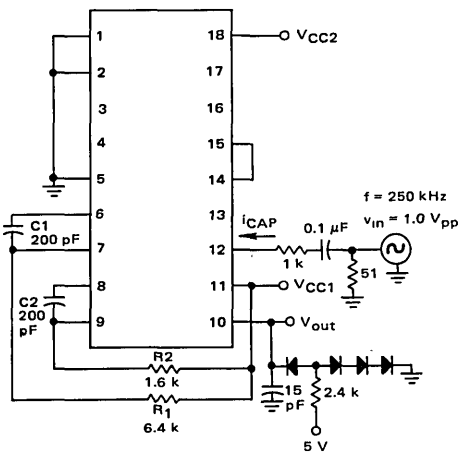


FIGURE 8 – PEAK SHIFT, PS

V_{in} = 1.0 V_{pp} f = 250 kHz

Test schematic on Figure 7

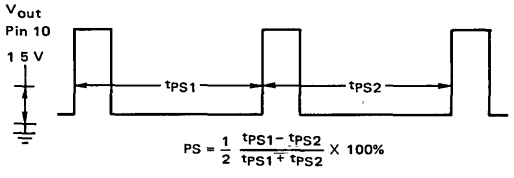


FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

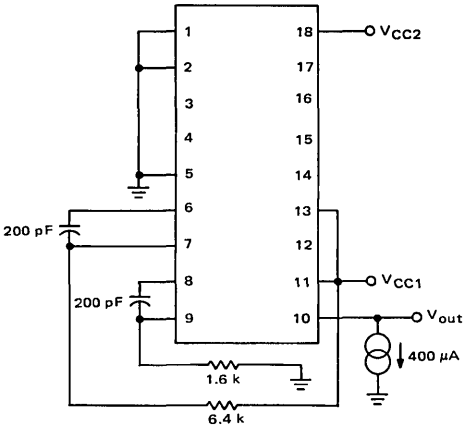


FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

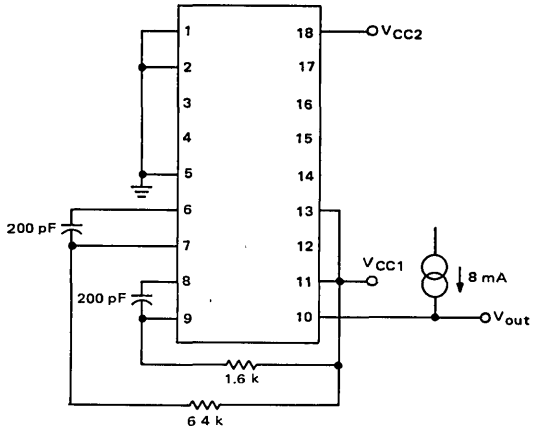
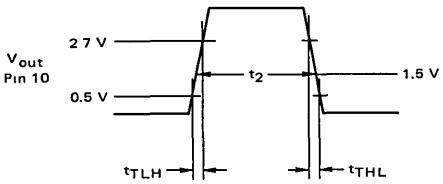


FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{T2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12



$$E_{T2} = \frac{t_2}{200\ ns} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

V_{in} shown on Figure 13

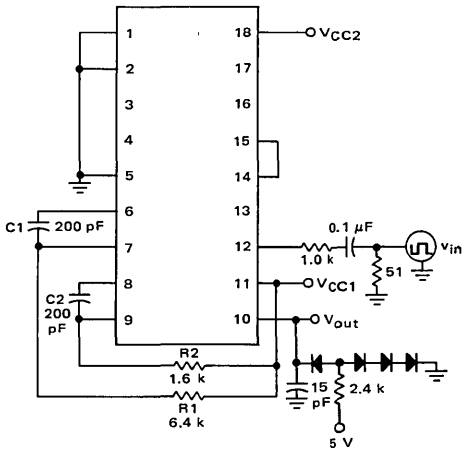


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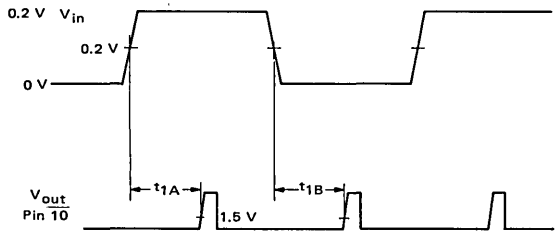
FIGURE 13 – TIMING ACCURACY MONO #1, E_{t1}

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

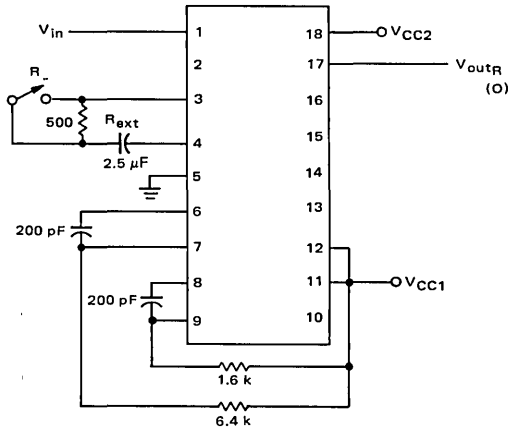


$$E_{t1A} = \frac{t_{1A}}{1000\ ns} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\ ns} \times 100\%$$

FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500\ \Omega$



f = 250 kHz

V_{in} = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{VO}}{A_{VR}} - 1\right)}$$

$$= \frac{500\ \Omega}{2\left(\frac{V_{outO}}{V_{outR}} - 1\right)}$$

FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT (I_{CC}/I_{CC} 25°C) versus TEMPERATURE

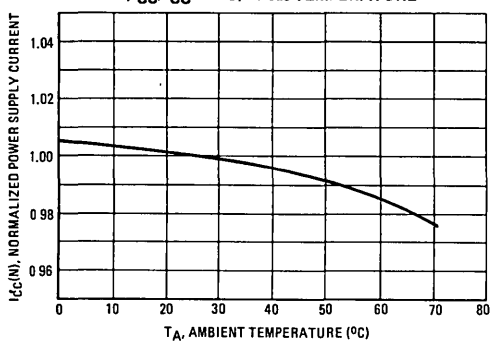


FIGURE 16 – NORMALIZED VOLTAGE GAIN (A_V/A_V 25°C) versus TEMPERATURE

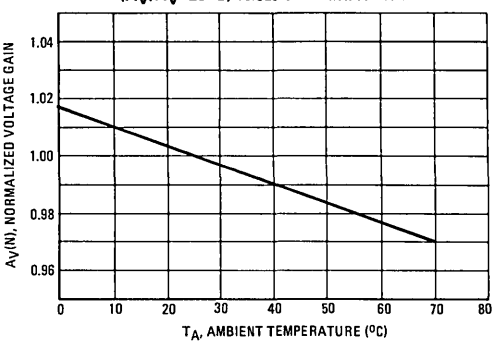


FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

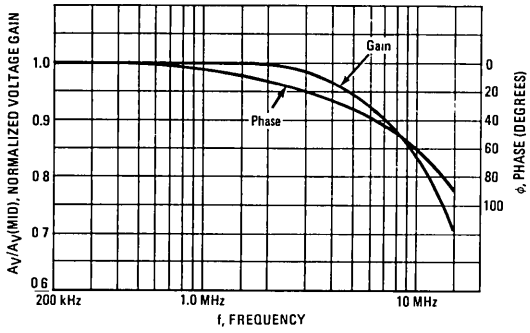


FIGURE 18 – NORMALIZED TIME DELAY t_1 versus TEMPERATURE

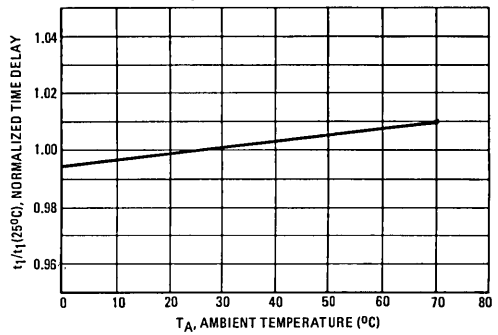


FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, t_2/t_2 25°C

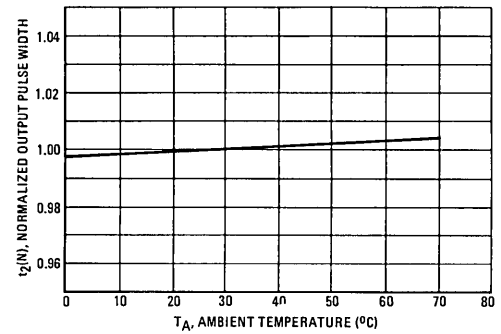


FIGURE 20 – NORMALIZED VOLTAGE GAIN, A_{VR}/A_{VR} 25°C

See Figure 14, Switch Position R

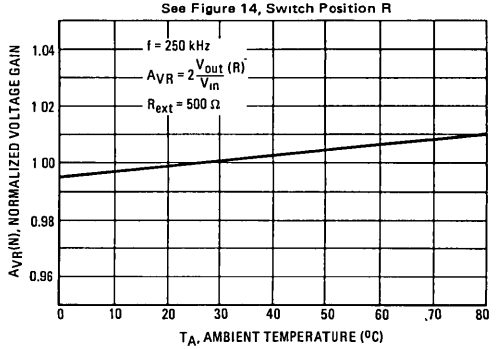


FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

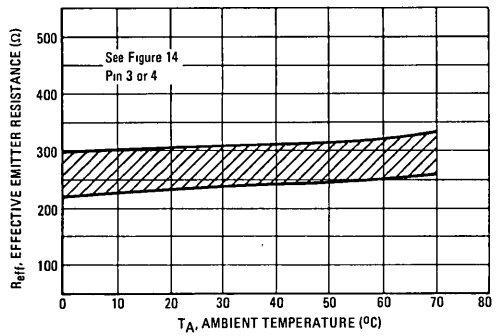
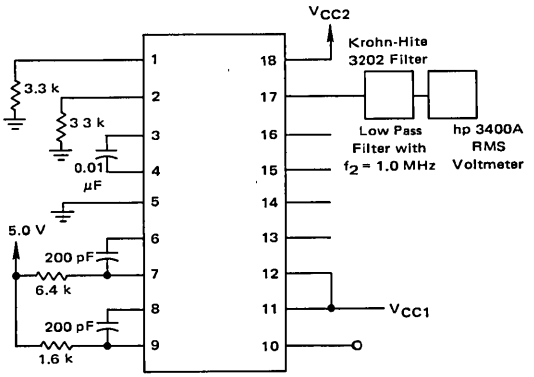


FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE



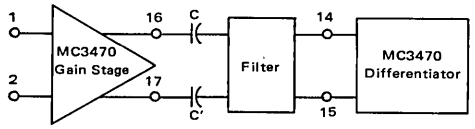
NOTE: Assume uncorrelated noise sources

e_n (differential noise at input) = $e_o\sqrt{2/100}$

APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a),

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



enabling the active differentiator and time domain filter to produce the desired output.

FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C' are placed before the filter as shown in Figure 23a. The charging and discharging of C and C' is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic – pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_P A_{VD})_{max}}{2.8\ mA}$$

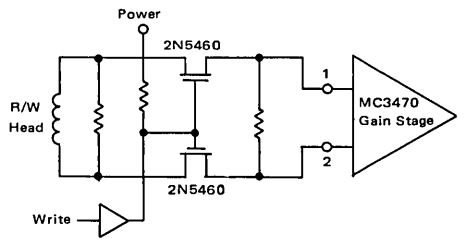
where E_p is the peak differential input voltage to the MC3470.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the

signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$\frac{A_{VO}}{A_{VR}} = \frac{R_{ext}}{2(r_e + R_e)} + 1$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,
$A_{VR} \triangleq$ voltage gain with the external resistor in,
$R_{ext} \triangleq$ the external resistor, and
$r_e + R_e \triangleq$ the resistance looking into pin 3 or pin 4.

Thus,

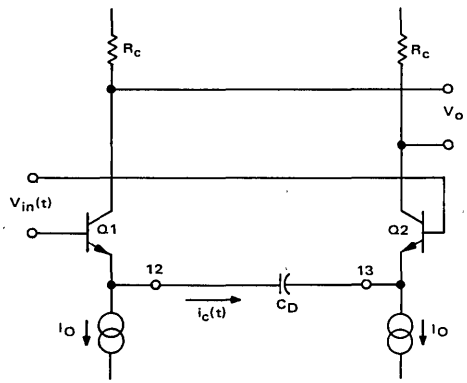
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling

FIGURE 24 — ACTIVE DIFFERENTIATOR NETWORK



the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

$$I = C dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

V_o is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_p \triangleq$ peak differential voltage applied to MC3470 amplifier input.

$E_p \sin \omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

$A_{VD} \triangleq$ differential voltage gain of input amplifier.

$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.

$= E_p A_{VD} \sin \omega t$ (Note: The filter is assumed to be lossless.)

$i_c(t) \triangleq$ current through capacitor C_D.

$R_O \triangleq$ output resistance of Q1 (Q2) at pin 12 (13).

If $v_{in}(t) = E_p A_{VD} \sin \omega t$, then the current through the capacitor C_D is given by

$$i_c(t) = C_D A_{VD} E_p \omega \cos \omega t$$

$$\text{and } V_O(t) = 2R_C C_D A_{VD} E_p \omega \cos \omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω, the maximum slew rate occurs for the maximum value of i_c or $\cos \omega t = 1$. Therefore,

$$i_c = C_D A_{VD} E_p \omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_c; therefore, C_D must be chosen such that the maximum i_c occurs at the maximum $A_{VD} E_p \omega$ product.

$$C_D = \frac{i_c max}{(A_{VD} E_p \omega)_{max}} = \frac{1\ mA}{(120)(E_p \omega)_{max}}.$$

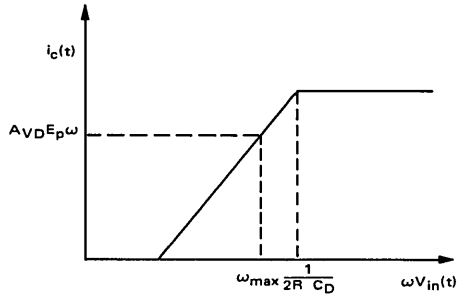
If the peak value specified for i_c is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2\,R_O C_D$. If this pole is ten times greater than the maximum operating frequency (ω_{max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 ω_{max} needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\, 10\, \omega_{max}}.$$

If R_O is not large enough to satisfy this condition, a series

FIGURE 25 – RESPONSE OF DIFFERENTIATOR USING ONLY C_D

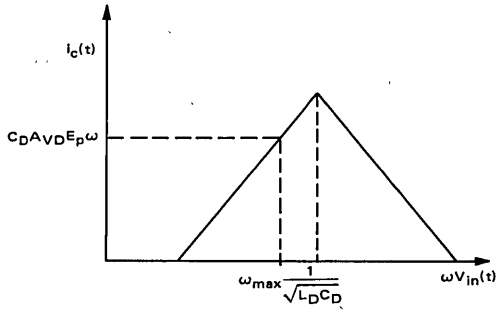


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\, 10\, \omega_{max}}.$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an

FIGURE 26 – COMPLETE RESPONSE OF DIFFERENTIATOR



inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_o) and the damping ratio (δ) to meet the systems requirements where

$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\ \omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100\ C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

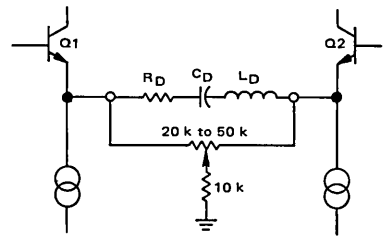
$$R = \frac{\delta}{5\ C_D\omega_{max}}$$

The total resistance (R) is the effective output resistance (R_O) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 – PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

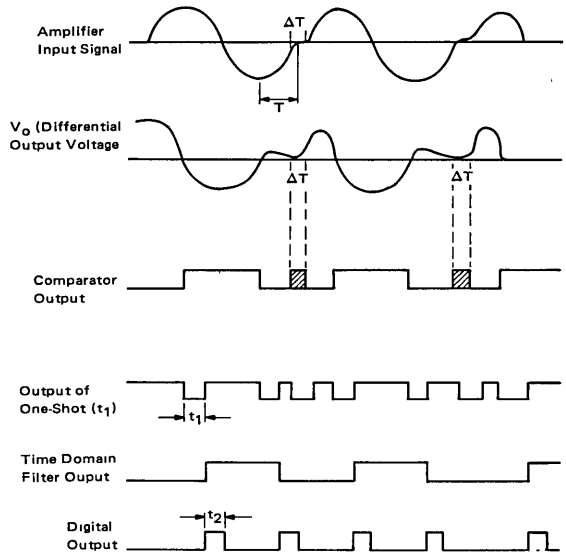
$$t_1 = R_1C_1K_1 + T_o$$

where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 > T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse t_2 (pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1, R_2, C_1, and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For t_1 = 1 μs and t_2 = 200 ns, suggested good values for the capacitors are

C_1 = 250 pF

C_2 = 160 pF

BOARD LAYOUT AND TESTING CONSIDERATIONS

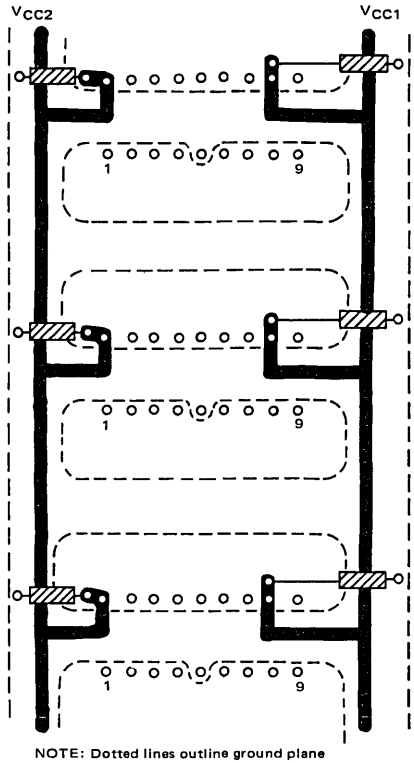
An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated

at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.