Calculating Power Dissipation for Differential Line Drivers

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Joe Vo
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INTRODUCTION

In many board and system level designs, it is often necessary to determine the total power dissipated by the individual components of that application. This determination of total device power dissipation is important for two reasons. First, it can be used to select the power supply best suited to satisfy the needs of the application. And second, a power dissipation calculation facilitates the analysis of how the board or system's operating conditions might adversely affect the reliability of, or otherwise damage, the on board components.

The purpose of this application note is to provide end users with a sample power dissipation calculation for typical TIA/EIA-422 and TIA/EIA-485 differential line drivers. Other topics which will be addressed by this application note include worst case power dissipation, and packaging/thermal considerations.

CONTRIBUTIONS TO TOTAL DEVICE POWER DISSIPATION

Under normal operating conditions, the total device power dissipation is determined primarily by output load current and quiescent current. These current terms are modified by external loading conditions, device switching frequency, power supply voltage and ambient operating temperature. The following discussion of device power dissipation will take all these factors into consideration.

The power dissipated by a device in its quiescent state and that dissipated by the outputs when the device is switching constitute the primary contributions to total device power dissipation. Quiescent power dissipation is defined as the product of power supply voltage (V_{CC}) and power supply current (I_{CC}).

$$PD_{QUIESCENT} = (V_{CC})\,(I_{CC}) \qquad (1)$$

The power dissipation by the outputs, takes into account the power dissipated by the output structures of the device when the outputs are driving a load. When the device output is in the LOW state, the output sinks a sufficient amount of load current to develop a V_{OL} with respect to ground. Conversely, when the device output is in the HIGH state, the output sources a load current sufficient to develop a V_{OH} with a respect to ground. The power dissipated, then, by a single channel is:

$$PD_{OUTPUT} = I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL}) \qquad (2)$$

where, I_{OH}= HIGH level output current
I_{OL} = LOW level output current

The general expression to describe the dissipated power for all outputs is:

$$PD_{OUTPUTS} = (\text{\# of channels})\,[I_{OH}(V_{CC} - V_{OH} + I_{OL}(V_{OL}))] \qquad (3)$$

Together, the sum of quiescent power dissipation and power dissipation at the device outputs approximates the total power dissipated by the device.

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} \qquad (4)$$

A more comprehensive total device power dissipation calculation, however, might also incorporate the contribution to device power dissipation from the device's switching frequency. Therefore, *Equation (4)* could be changed to look like the following.

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} + C_{OUT}(V_{CC})^2(f) \qquad (5)$$

where, C_{OUT} = device output capacitive load
f= device switching frequency

For this application note, the last term of *Equation (5)* was intentionally omitted. These are several reasons for this omission. First, switching frequency does not lend itself well to this general discussion of power dissipation since it varies from application to application. Second, in terms of the quiescent and output power dissipation components, the magnitude of the CV^2f term on total device power dissipation is negligibly small for most line drivers. And third, *Figure 1* demonstrates that switching frequency will not heavily impact quiescent device power dissipation (see *Equation (1)*) since the magnitude of the change in I_{CC} due to switching frequency is small.

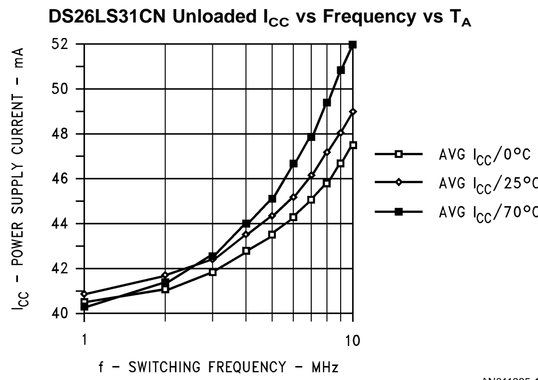

FIGURE 1. Supply Current vs Switching Frequency vs Temperature

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TYPICAL POWER DISSIPATION CALCULATIONS USING THE DS26LS31CN

To better illustrate a total power dissipation calculation in a typical TIA/EIA-422 application, consider the DS26LS31CN (molded DIP package) Quad Differential Line Driver operating under following conditions:

V_{CC} = 5.0V

Ambient Operating Temperature = 25˚C

Switching Frequency = 1 MHz

Duty Cycle = 50%

Measured V_{OH} = 3.2V

Measured V_{OL} = 0.3V

Termination Resistor = 100Ω

Figure 2 indicates that the I_{CC} typically associated with a V_{CC} of 5.0V, at room temperature, is approximately 39 mA. *Figure 1* indicated that a device, operating at room temperature, switching at 1 MHz will generate an I_{CC} of approximately 41 mA. Note in both *Figure 1* and *Figure 2* that the change in I_{CC} with respect to switching frequency and the change in I_{CC} with respect to V_{CC}, respectively, is rather small. Also note that in both figures there is little I_{CC} dependence on temperature.

For this typical calculation, 41 mA will be used for $I_{CCtypical}$ since it is a better representation of actual device operating conditions.

From (1), the static power dissipation is:

$$PD_{QUIESCENT} = (V_{CCtypical}\ (I_{CCtypical}) = (5.0V)\ (41.0\ mA) = 205.0\ mW$$

Given that the measured V_{OH} is 3.2V, one can extract the corresponding I_{OH} from *Figure 3*. The I_{OH} required to develop a V_{OH} of 3.2V is approximately 30 mA.

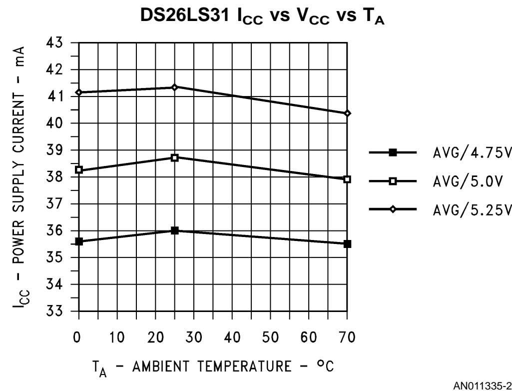

FIGURE 2. Supply Current vs Supply Voltage vs Temperature

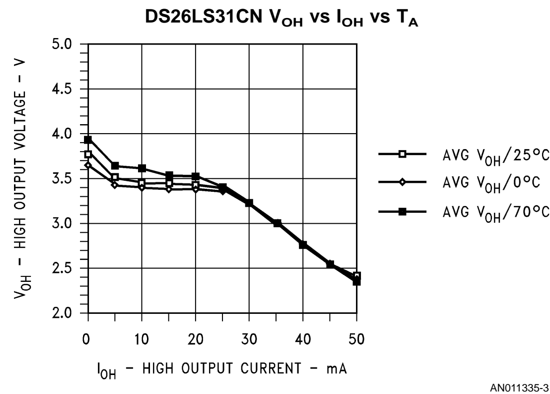

FIGURE 3. High Output Voltage vs High Output Current vs Temperature

From *Figure 4*, one can likewise obtain an I_{OL} of approximately 30 mA given a measured V_{OL} of 0.3V.

The outputs, then, of the DS26LS31CN dissipate power according to the following relationship:

$$PD_{OUTPUTS} = (\# \text{ of Channels}) [I_{OH} (V_{CC} - V_{OH}) + I_{OL} (V_{OL})]$$
$$= (4) [30 \text{ mA} (5.0V - 3.2V) + 30 \text{ mA} (0.3V)]$$
$$= (4) [54.0 \text{ mW} + 0.9 \text{ mW}]$$
$$= 252.0 \text{ mW}$$

From the given typical operating conditions, the total power dissipated by the DS26LS31CN is:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 205.0 \text{ mW} + 252.0 \text{ mW}$$
$$= 457.0 \text{ mW}$$

WORST CASE POWER DISSIPATION CALCULATIONS

While a typical power dissipation calculation is informative, a board or system level designer will invariably be forced to also perform a worst case calculation. With the exception of several minor changes, the same procedure is followed for both typical and worst case power dissipation calculations.

Starting with static power dissipation, this calculation must now use the maximum values for both power supply voltage (V_{CCmax}) and power supply current (I_{CCmax}). The I_{CCmax} used is normally that specified by the data sheet. However, if the application were to force the device beyond its 10 MHZ operating window, the I_{CCmax} could exceed the data sheet specifications of 60 mA (see *Figure 1*). In either case, the larger current value must be used for I_{CCmax} in the worst case quiescent power calculation.

The next step is to calculate the power dissipation from the device outputs. To do so, place the device under the worst case board or system conditions, and measure the resulting V_{OH} and V_{OL} levels. Given these worst case V_{OH} and V_{OL} values, one can extract the corresponding worst case I_{OH} and I_{OL} values with the help of *Figure 3* and *Figure 4*, respectively. A substitution of these values into *Equation (3)* will then yield the worst case power dissipation due to the device outputs.

An alternative method to calculate the power dissipated by the device outputs requires that a differential output voltage versus output current (V_{OD} vs I_O) curve be generated. Keeping in mind that $V_{OD} \equiv V_{OH} - V_{OL}$, a V_{OD} vs I_O curve can be developed by "subtracting" the V_{OL} vs I_{OL} curve from the V_{OH} vs I_{OH} curve. On the resulting V_{OD} vs I_O curve, draw a load line corresponding to the worst case loading conditions. This will then yield the output differential voltage and output currents being sourced and sunk by the device under a worst case loading condition. A substitution of these quantities into *Equation (6)* will yield the power being dissipated by the device outputs.

$$PD_{DIFFERENTIAL\ OUTPUTS} = (\# \text{ of channels}) [I_O(V_{CC} - V_{OD})] \quad (6)$$

As an example, consider the output voltage versus output current curves previously given for the DS26LS31CN (*Figure 3* and *Figure 4*). The V_{OD} vs I_O curve for the DS26LS31CN, as illustrated in *Figure 5*, can be drawn by "subtracting" *Figure 4* from *Figure 3*.

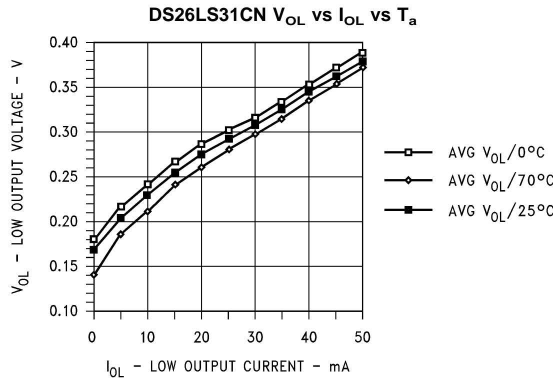

FIGURE 4. Low Output Voltage vs Low Output Current vs Temperature

DS26LS31CN V_{OD} vs I_O vs T_A

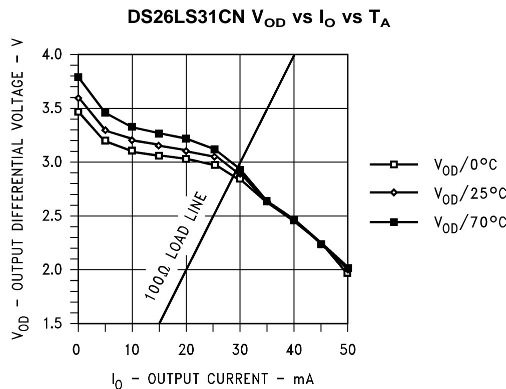

FIGURE 5. Output Differential Voltage vs Output Current vs Temperature

A sample worst case load line of 100Ω superimposed upon *Figure 5* reveals the corresponding worst case operating point for the DS26LS31CN; that is, it reveals the device's output differential voltage and output current given a sample worst case output load. When substituted into *Equation (6)*, these voltage and current quantities will yield the worst case power dissipation at the device outputs.

The sum of the worst case quiescent and output power dissipation components will approximate the total worst case device power dissipation.

POWER CALCULATION FOR TIA/EIA-485 DIFFERENTIAL LINE DRIVERS

Let's first compare a typical TIA/EIA-422 output structure to a typical TIA/EIA-485 output structure. As shown in *Figure 6*, the presence of Schottky diodes in the output stage of an TIA/EIA-485 device clearly differentiates it from a similar TIA/EIA-422 device. The addition of the Schottky diodes to the TIA/EIA-485 output stage enable it to safely operate in multipoint (multiple driver) applications over a −7V to +12V common mode range versus the −250 mV to +6V common mode range of TIA/EIA-422. However, the Schottky diodes in the TIA/EIA-485 outputs have the net effect of raising the value of V_{OL} by one diode drop and decreasing the value of V_{OH} by the same amount. This change in output voltage levels will, in turn, affect the amount of power being dissipated in the output stage.

Despite the fact that the output structure of an TIA/EIA-422 line driver differs from that of the TIA/EIA-485 line driver, the procedure outlined earlier to calculate power dissipation is applicable for both TIA/EIA-422 devices and TIA/EIA-485 devices. Quiescent and output power dissipation calculations for an TIA/EIA-485 line driver will again employ *Equations (1), (3)* respectively.

As with the sample power calculation for the TIA/EIA-422 device, the sum of the quiescent and output power components will yield the total approximated power dissipated by the TIA/EIA-485 device.

As an example, consider the worst case power dissipation of the DS96F172CJ (ceramic DIP package). Other than the fact that the DS96F172CJ is an TIA/EIA-485 device, it is pin for pin compatible with the DS26LS31CN. As outlined earlier, the first step is to calculate the quiescent power dissipation. From *Equation (1)*, the worst case quiescent power dissipation is:

$$PD_{QUIESCENTmax} = (V_{CCmax})\ (I_{CCmax})$$
$$= (5.25V)\ (50\ mA)$$
$$= 262.5\ mW$$

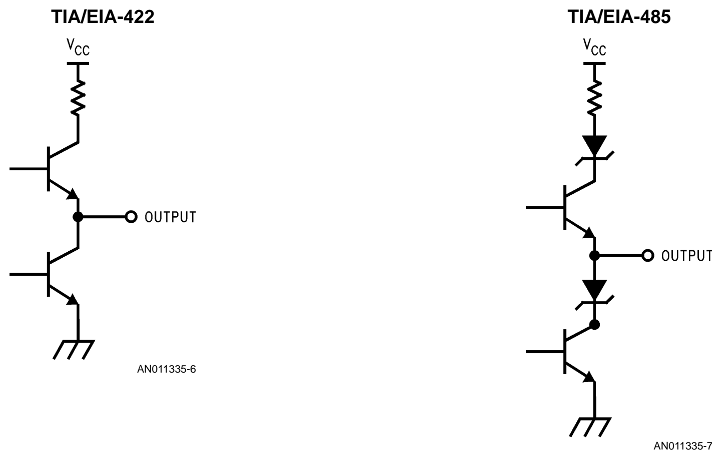

FIGURE 6. TIA/EIA-422 and TIA/EIA-485 Output Structures

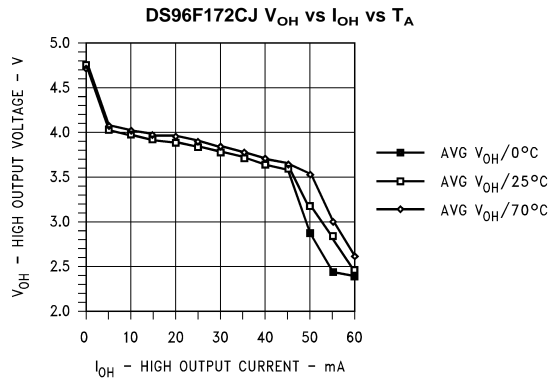

FIGURE 7. High Output Voltage vs High Output Current vs Temperature

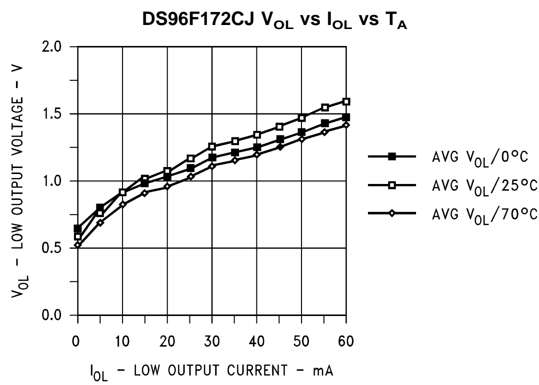

FIGURE 8. Low Output Voltage vs Low Output Current vs Temperature

The next step is to calculate the power dissipated at the device outputs under a worst case load condition. Again, there are two ways to do this. First, one can measure the worst case output voltage levels and reference them with *Figure 7* and *Figure 8* to extract the corresponding worst case output currents.

A substitution of these resulting quantities into *Equation (3)* will yield the power dissipated at the device outputs given a worst case load. The second method to calculate output power dissipation involves drawing a worst case load line on the differential output voltage versus output current curve. In the case of the DS96F172CJ, the worst case load line is assumed to be 60Ω. This assumption was made because in a typical TIA/EIA-485 application, both ends of the transmission line are terminated with 120Ω and so the TIA/EIA-485 driver is effectively loaded with 60Ω. In *Figure 9* a 60Ω load line has been superimposed upon the differential output versus output current curve and consequently, worst case values of output current and differential output voltage (under the given load) have been obtained.

DS96F172CJ V_{OD} vs I_O vs T_A

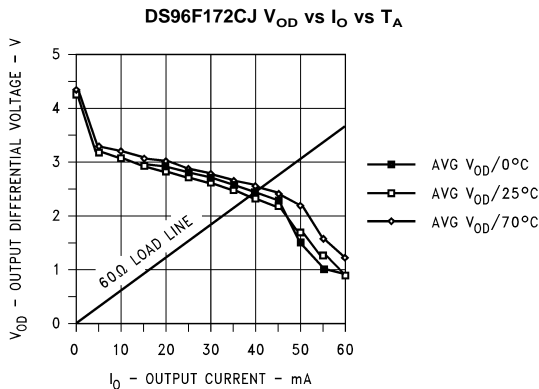

FIGURE 9. Output Differential Voltage vs Output Current vs Temperature

At room temperature, the worst case power dissipation at the device outputs is (from *Equation (6)*):

$$PD_{DIFFERENTIAL\ OUTPUTS}$$
$$= (\#\ of\ channels)\ [I_O\ (V_{CC} - V_{OD})]$$
$$= (4)\ [39\ mA\ (5.25V - 2.4V)]$$
$$= 444.6\ mW$$

The only remaining task is to sum together the quiescent and output power dissipation terms to obtain a total worst case power dissipation. From (4), the DS96F172CJ operating at room temperature, under a worst case load of 60Ω, will dissipate:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 262.5\ mW + 444.6\ mW$$
$$= 707.1\ mW$$

PACKAGING AND THERMAL CONSIDERATIONS

Having calculated the total power dissipated by the device, the next logical step is to ascertain that the power dissipated does not thermally damage the device. To do so, the following equation is used:

$$T_J = [PD_{TOTAL}(\theta_{JA})] + T_A \qquad (7)$$

where, θ_{JA} = Thermal Resistance from Junction to Ambient (˚C/W)

PD_{TOTAL}= Total Power Dissipated by Device (W)

T_J= Junction Temperature (˚C)

T_A= Ambient Temperature (˚C)

The only variable which remains unknown is θ_{JA}. θ_{JA} information for the available package types of most devices can be found in the respective device's data sheet. Keep in mind that the data sheet often refers to θ_{JA} in terms of derate factors. Determining θ_{JA} involves taking the inverse of the derate factor.

$$\theta_{JA} = 1/\text{Derate Factor} \qquad (8)$$

For example, all the information is now available for a sample calculation of the DS26LS31CN's junction temperature using the operating conditions specified earlier. The data sheet of the DS26LS31CN specifies a derate factor, for the plastic DIP package, of 11.9 mW/˚C. From (8), the θ_{JA} is:

$$\theta_{JA} = 1/\text{Derate Factor}$$
$$= 1/(0.0119\ W/˚C)$$
$$= 84.0\ ˚C/W$$

The thermal resistance from junction to ambient for the DS26LS31CN is now known. Also known are the ambient operating temperature and the total power dissipated (obtained earlier). From (7), the junction temperature is:

$$T_J = [(PD_{TOTAL})\ (\theta_{JA})] + T_A$$
$$= [(0.457W)\ (84.0˚C/W)] + 25˚C$$
$$= 63.4˚C$$

The maximum allowable junction temperature for plastic DIP packages is 150˚C. The junction temperature of the DS26LS31CN operating under the conditions specified earlier, by the typical power dissipation calculation, is well within the allowed maximum. Applications where the maximum allowable junction temperature is exceeded should be avoided since this condition may thermally damage the device and package.

Looking at this thermal analysis from a slightly different perspective, *Equation (7)* can be rewritten as:

$$PD_{PACKAGEmax} = (T_{Jmax} - T_A)/\theta_{JA} \qquad (9)$$

By substituting 150˚C for the maximum allowable junction temperature, the maximum allowable package power dissipation at 25˚C can be calculated using the θ_{JA} for the DS26LS31CN plastic DIP (N) package.

$$PD_{PACKAGEmax\ @\ 25^{\circ}C} = (T_{Jmax} - T_A)/\theta_{JA}$$
$$= (150^{\circ}C - 25^{\circ}C)/84.0^{\circ}C/W$$
$$= 1.48W$$

To calculate the maximum allowable package power dissipation at 70˚C, the 1.48W maximum at 25˚C must be derated using the following procedure:

$$PD_{PACKAGEmax\ @\ 70^{\circ}C} = PD_{PACKAGEmax\ @\ 25^{\circ}C} - (Derate)\ (\Delta T_A) = 1.48W - (0.0119W/^{\circ}C)(45^{\circ}C) = 0.94W \quad (10)$$

This sample calculation illustrates that as ambient temperature increases, the DS26LS31CN is able to dissipate less power before the maximum allowable junction temperature specification is violated. Keep in mind that this thermal analysis also applies to TIA/EIA-485 devices such as the DS96F172CJ.

It should be noted that this general thermal analysis is applicable to all other packages and device types assuming that the maximum power dissipation and θ_{JA} are known.

SUMMARY

A method for calculating the total power dissipated by an TIA/EIA-422 driver was presented. This method is also applicable to similar devices conforming to the TIA/EIA-485 standard. Samples calculations for the DS26LS31CN and the DS96F172CJ were presented. Worst case considerations were also discussed. And finally, the relationship between power dissipation and thermal/packaging limitations was introduced.

SPECIAL NOTES

Figure 1 :	Ten samples from three data codes.
Figure 2 :	Ten samples from three data codes. Outputs unloaded and V_{CC} = 5.0V.
Figure 3, *Figure 4*, *Figure 5* :	Ten samples from three date codes. V_{CC} = 5.0V
Figure 7, *Figure 8*, *Figure 9* :	Ten samples from two date codes. V_{CC} = 5.0V

The graphical data referenced in this application note are not intended to guarantee performance as they only represent typical values.

REFERENCES

HC-CMOS Power Dissipation, K. Karakotsios, National Semiconductor, 1988 CMOS Logic Data Book, Application Note AN-303.

Understanding Integrated Circuit Package Power Capabilities, C. Carinalli and J. Huljev, National Semiconductor, 1990 Interface Data Book, Application Note AN-336.

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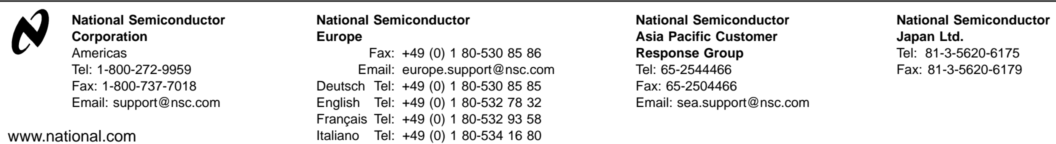

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