LVDS Display Interface (LDI) TFT Data Mapping for Interoperability with FPD-Link

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Michael Hinh
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INTRODUCTION

The purpose of this application note is to provide the data mapping to ensure interoperability between the LVDS display interface (DS90C387/DS90CF388 chipset) and 18-bit or 24-bit FPD-Link devices. This data mapping must be used, so that the most significant bits (MSB) for an 18-bit application are mapped exactly the same as the most significant bits in the 24-bit application from the VGA controllers. Only three LVDS serialized data lines are required for an 18-bit FPD-Link application while a 24-bit application uses 4 LVDS data lines. The additional least significant bits in the 24-bit application are mapped to the 4th LVDS data line.

The tables below show the connections needed when using LVDS chipsets (LDI or FPD-Link) for flat panel display applications. Starting from the left, the outputs of the VGA are noted from LSB (less significant bit) to MSB (most significant bit). VGA controllers typically name the LSB as R0, B0, and G0. The MSB remains the same from the VGA controller pin definition, but 24-bit and 18-bit color are named differently. This confuses the connections needed, so careful review of the following tables is recommended to ensure correct color bit mapping.

LVDS transmitters are available for 18-bit (i.e., DS90C365), 24-bit (i.e., DS90C385) and 24/48-bit (i.e., DS90C387) applications. The pin names for the devices are different, but the inputs to the transmitter will be serialized, so that the LVDS data signal positions are always the same. LVDS receivers are also available in 18-bit (i.e., DS90C364A), 24-bit (i.e., DS90CF384A) and 48-bit (i.e., DS90CF388). These receivers sample the serial LVDS data lines and output the parallel color bit information at the LVDS pixel clock rate.

Note, from an 18-bit to a 24-bit RGB mode, the VGA changes the name of color bits since two or more LSB bits are added. Adding R0 and R1 pushes the MSB bit from R5 to R7.

HOW TO READ THE TABLES

The tables are read from left to right. From the left, the R0, G0 and B0 are the least significant bit (LSB) as defined by the VGA controllers. These signals should be connected to the input data pins of the transmitters (i.e., color bit R0 in an 18-bit application must be connected to Txin0 or R10 depending on the transmitter being used). The output signals of the receiver are mirror images of the input signals to the transmitter. The DS90C387/DS90CF388 are capable of supporting single pixel, dual pixel, or single-in/dual-out pixel modes. Determine the mode to be used, and then review the corresponding table.

TABLE 1. Single Pixel per Clock Input Application

VGA — TFT Data Signal			Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
	24-bit	18-bit	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18-bit	24-bit
LSB	R0		Txin27		R16	Rxout27		R16		R0
	R1		Txin5		R17	Rxout5		R17		R1
	R2	R0	Txin0	Txin0	R10	Rxout0	Rxout0	R10	R0	R2
	R3	R1	Txin1	Txin1	R11	Rxout1	Rxout1	R11	R1	R3
	R4	R2	Txin2	Txin2	R12	Rxout2	Rxout2	R12	R2	R4
	R5	R3	Txin3	Txin3	R13	Rxout3	Rxout3	R13	R3	R5
	R6	R4	Txin4	Txin4	R14	Rxout4	Rxout4	R14	R4	R6
MSB	R7	R5	Txin6	Txin5	R15	Rxout6	Rxout5	R15	R5	R7
LSB	G0		Txin10		G16	Rxout10		G16		G0
	G1		Txin11		G17	Rxout11		G17		G1
	G2	G0	Txin7	Txin6	G10	Rxout7	Rxout6	G10	G0	G2
	G3	G1	Txin8	Txin7	G11	Rxout8	Rxout7	G11	G1	G3
	G4	G2	Txin9	Txin8	G12	Rxout9	Rxout8	G12	G2	G4
	G5	G3	Txin12	Txin9	G13	Rxout12	Rxout9	G13	G3	G5
	G6	G4	Txin13	Txin10	G14	Rxout13	Rxout10	G14	G4	G6
MSB	G7	G5	Txin14	Txin11	G15	Rxout14	Rxout11	G15	G5	G7

TABLE 1. Single Pixel per Clock Input Application (Continued)

VGA — TFT Data Signal			Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
	24-bit	18-bit	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18-bit	24-bit
LSB	B0		Txin16		B16	Rxout16		B16		B0
	B1		Txin17		B17	Rxout17		B17		B1
	B2	B0	Txin15	Txin12	B10	Rxout15	Rxout12	B10	B0	B2
	B3	B1	Txin18	Txin13	B11	Rxout18	Rxout13	B11	B1	B3
	B4	B2	Txin19	Txin14	B12	Rxout19	Rxout14	B12	B2	B4
	B5	B3	Txin20	Txin15	B13	Rxout20	Rxout15	B13	B3	B5
	B6	B4	Txin21	Txin16	B14	Rxout21	Rxout16	B14	B4	B6
MSB	B7	B5	Txin22	Txin17	B15	Rxout22	Rxout17	B15	B5	B7

In a single pixel application, the 48-bit Tx and Rx should be set for single pixel mode (DUAL=low). This disables half the inputs and outputs signals reducing the power dissipation of the chipset.

TABLE 2. Dual Pixel per Clock Input Application

VGA — TFT Data Signal			Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
	48-bit	36-bit	24-bit 2Tx (C385)	18-bit 2Tx (C365)	48-bit 1Tx (C387)	24-bit 2Rx (CF384A)	18-bit 2Rx (CF364A)	48-bit 1Rx (CF388)	36-bit	48-bit
LSB	RO0		Txin27		R16	Rxout27		R16		RO0
	RO1		Txin5		R17	Rxout5		R17		RO1
	RO2	RO0	Txin0	Txin0	R10	Rxout0	Rxout0	R10	RO0	RO2
	RO3	RO1	Txin1	Txin1	R11	Rxout1	Rxout1	R11	RO1	RO3
	RO4	RO2	Txin2	Txin2	R12	Rxout2	Rxout2	R12	RO2	RO4
	RO5	RO3	Txin3	Txin3	R13	Rxout3	Rxout3	R13	RO3	RO5
	RO6	RO4	Txin4	Txin4	R14	Rxout4	Rxout4	R14	RO4	RO6
MSB	RO7	RO5	Txin6	Txin5	R15	Rxout6	Rxout5	R15	RO5	RO7
LSB	GO0		Txin10		G16	Rxout10		G16		GO0
	GO1		Txin11		G17	Rxout11		G17		GO1
	GO2	GO0	Txin7	Txin6	G10	Rxout7	Rxout6	G10	GO0	GO2
	GO3	GO1	Txin8	Txin7	G11	Rxout8	Rxout7	G11	GO1	GO3
	GO4	GO2	Txin9	Txin8	G12	Rxout9	Rxout8	G12	GO2	GO4
	GO5	GO3	Txin12	Txin9	G13	Rxout12	Rxout9	G13	GO3	GO5
	GO6	GO4	Txin13	Txin10	G14	Rxout13	Rxout10	G14	GO4	GO6
MSB	GO7	GO5	Txin14	Txin11	G15	Rxout14	Rxout11	G15	GO5	GO7
LSB	BO0		Txin16		B16	Rxout16		B16		BO0
	BO1		Txin17		B17	Rxout17		B17		BO1
	BO2	BO0	Txin15	Txin12	B10	Rxout15	Rxout12	B10	BO0	BO2
	BO3	BO1	Txin18	Txin13	B11	Rxout18	Rxout13	B11	BO1	BO3
	BO4	BO2	Txin19	Txin14	B12	Rxout19	Rxout14	B12	BO2	BO4
	BO5	BO3	Txin20	Txin15	B13	Rxout20	Rxout15	B13	BO3	BO5
	BO6	BO4	Txin21	Txin16	B14	Rxout21	Rxout16	B14	BO4	BO6
MSB	BO7	BO5	Txin22	Txin17	B15	Rxout22	Rxout17	B15	BO5	BO7

TABLE 2. Dual Pixel per Clock Input Application (Continued)

VGA — TFT Data Signal			Transmitter Input Data Pin			Receiver Output Data Pin			TFT Panel Data Signal	
	48-bit	36-bit	24-bit 2Tx (C385)	18-bit 2Tx (C365)	48-bit 1Tx (C387)	24-bit 2Rx (CF384A)	18-bit 2Rx (CF364A)	48-bit 1Rx (CF388)	36-bit	48-bit
LSB	RE0		Txin27		R26	Rxout27		R26		RE0
	RE1		Txin5		R27	Rxout5		R27		RE1
	RE2	RE0	Txin0	Txin0	R20	Rxout0	Rxout0	R20	RE0	RE2
	RE3	RE1	Txin1	Txin1	R21	Rxout1	Rxout1	R21	RE1	RE3
	RE4	RE2	Txin2	Txin2	R22	Rxout2	Rxout2	R22	RE2	RE4
	RE5	RE3	Txin3	Txin3	R23	Rxout3	Rxout3	R23	RE3	RE5
	RE6	RE4	Txin4	Txin4	R24	Rxout4	Rxout4	R24	RE4	RE6
MSB	RE7	RE5	Txin6	Txin5	R25	Rxout6	Rxout5	R25	RE5	RE7
LSB	GE0		Txin10		G26	Rxout10		G26		GE0
	GE1		Txin11		G27	Rxout11		G27		GE1
	GE2	GE0	Txin7	Txin6	G20	Rxout7	Rxout6	G20	GE0	GE2
	GE3	GE1	Txin8	Txin7	G21	Rxout8	Rxout7	G21	GE1	GE3
	GE4	GE2	Txin9	Txin8	G22	Rxout9	Rxout8	G22	GE2	GE4
	GE5	GE3	Txin12	Txin9	G23	Rxout12	Rxout9	G23	GE3	GE5
	GE6	GE4	Txin13	Txin10	G24	Rxout13	Rxout10	G24	GE4	GE6
MSB	GE7	GE5	Txin14	Txin11	G25	Rxout14	Rxout11	G25	GE5	GE7
LSB	BE0		Txin16		B26	Rxout16		B26		BE0
	BE1		Txin17		B27	Rxout17		B27		BE1
	BE2	BE0	Txin15	Txin12	B20	Rxout15	Rxout12	B20	BE0	BE2
	BE3	BE1	Txin18	Txin13	B21	Rxout18	Rxout13	B21	BE1	BE3
	BE4	BE2	Txin19	Txin14	B22	Rxout19	Rxout14	B22	BE2	BE4
	BE5	BE3	Txin20	Txin15	B23	Rxout20	Rxout15	B23	BE3	BE5
	BE6	BE4	Txin21	Txin16	B24	Rxout21	Rxout16	B24	BE4	BE6
MSB	BE7	BE5	Txin22	Txin17	B25	Rxout22	Rxout17	B25	BE5	BE7

Note: O = Odd (First) Pixel, E = Even (Second) Pixel

The color mapping recommended for a dual pixel application requires 2 FPD-Link transmitters and/or receivers for 24-bit or 18-bit applications or 1 LDI chipset. The table does not show the DS90C387 (48-bit) transmitter's output. The DS90C387 provides 2 LVDS output clocks to support two 24-bit or two 18-bit FPD-Link receivers.

TABLE 3. Single Pixel per Clock Input to Dual Pixel per Clock Output Application (DS90C387/DS90CF388 only)

VGA — TFT Data Signal			Input Data Pin	Output Data Pin	TFT Panel Data Signal	
	24-bit	18-bit	48-bit 1Tx (C387)	48-bit 1Rx (CF388)	36-bit	48-bit
LSB	R0		R16	R16		RO0
	R1		R17	R17		RO1
	R2	R0	R10	R10	RO0	RO2
	R3	R1	R11	R11	RO1	RO3
	R4	R2	R12	R12	RO2	RO4
	R5	R3	R13	R13	RO3	RO5
	R6	R4	R14	R14	RO4	RO6
MSB	R7	R5	R15	R15	RO5	RO7
LSB	G0		G16	G16		GO0
	G1		G17	G17		GO1
	G2	G0	G10	G10	GO0	GO2
	G3	G1	G11	G11	GO1	GO3
	G4	G2	G12	G12	GO2	GO4
	G5	G3	G13	G13	GO3	GO5
	G6	G4	G14	G14	GO4	GO6
MSB	G7	G5	G15	G15	GO5	GO7
LSB	B0		B16	B16		BO0
	B1		B17	B17		BO1
	B2	B0	B10	B10	BO0	BO2
	B3	B1	B11	B11	BO1	BO3
	B4	B2	B12	B12	BO2	BO4
	B5	B3	B13	B13	BO3	BO5
	B6	B4	B14	B14	BO4	BO6
MSB	B7	B5	B15	B15	BO5	BO7
LSB			R16	R26		RE0
			R17	R27		RE1
			R10	R20	RE0	RE2
			R11	R21	RE1	RE3
			R12	R22	RE2	RE4
			R13	R23	RE3	RE5
			R14	R24	RE4	RE6
MSB			R15	R25	RE5	RE7
LSB			G16	G26		GE0
			G17	G27		GE1
			G10	G20	GE0	GE2
			G11	G21	GE1	GE3
			G12	G22	GE2	GE4
			G13	G23	GE3	GE5
			G14	G24	GE4	GE6
MSB			G15	G25	GE5	GE7

TABLE 3. Single Pixel per Clock Input to Dual Pixel per Clock Output Application (DS90C387/DS90CF388 only) (Continued)

VGA — TFT Data Signal			Input Data Pin	Output Data Pin	TFT Panel Data Signal	
	24-bit	18-bit	48-bit 1Tx (C387)	48-bit 1Rx (CF388)	36-bit	48-bit
LSB			B16	B26		BE0
			B17	B27		BE1
			B10	B20	BE0	BE2
			B11	B21	BE1	BE3
			B12	B22	BE2	BE4
			B13	B23	BE3	BE5
			B14	B24	BE4	BE6
MSB			B15	B25	BE5	BE7

Table 3 shows how the input signals (single pixel) are split into odd (first) and even (second) pixels (dual pixels). This is only supported with an even number of cycles during blanking (blanking occurs when DE = low). A single input is split into odd and even pixel data starting with the odd (first) pixel outputs (A0-A3). The next pixel goes to the even pixel outputs (A4-A7). The splitting of the data signal also starts with DE (data enable) transitioning from logic low to high indicating active data. Under this condition the 'R_FDE' pin must be set high.

TABLE 4. TFT Control Data Signal and CLK

VGA — TFT Data Signal	Input Data Pin			Output Data Pin			TFT Panel Data Signal	
	24-bit Tx (C385)	18-bit Tx (C365)	48-bit Tx (C387)	24-bit Rx (CF384A)	18-bit Rx (CF364A)	48-bit Rx (CF388)	18/36-bit	24/48-bit
HSYNC	Txin24	Txin18	HSYNC	Rxout24	Rxout18	HSYNC	HSYNC	
VSYNC	Txin25	Txin19	VSYNC	Rxout25	Rxout19	VSYNC	VSYNC	
DEN	Txin26	Txin20	DE	Rxout26	Rxout20	DE	DEN	
CLK	TxCLKin	TxCLKin	CLKIN	TxCLKout	TxCLKout	CLKOUT	CLK	

In the backward compatible (LDI) mode and for FPD-Link, control signals (DE, HYSNC, and VSYNC) are sent as regular data bits. *Table 4* above shows the mapping of the control signals for FPD-Link and LDI chipsets.

CONCLUSION

Using the recommended color mapping, interoperability is obtained between FPD-Link devices and the LDI chipset. It is also possible to directly interface a 24-bit VGA to an 18-bit panel as the additional LSB color bits are mapped to separate LVDS data lines. The LDI chipset supports two basic modes of operation. The first is a backward compatible mode, which supports the direct connection with FPD-Link devices as described above. The other mode, supports additional features that enhance cable drive capability of the transmitter by adding DC Balancing the data lines and also by providing, pre-emphasis and a cable de-skew operation. This new "LDI" mode is described in the DS90C387/DS90CF388 datasheet.

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

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Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

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