User's Manual

QUIKLOOK™

National Semiconductor

Advanced Information

User's Manual

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National Semiconductor

420306199-001

1 Introduction

The COP400-T01 QUIKLOOK™ tester provides GO/NO-GO functional tests for the COP400 family. At the customer's facility, QUIKLOOK performs a series of tests on the COPS™ chips similar to the tests performed at National Semiconductor prior to shipment.

All software necessary for the PDS/QUIKLOOK system operation is provided by National Semiconductor. To begin testing COPS, the user need only connect the cables and power, and verify the correct performance of the PDS/QUIKLOOK system using the supplied diagnostic software.

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2 System Description

This section illustrates and defines the PDS/QUIKLOOK hardware configuration, provides functional and hardware description of QUIKLOOK tester and its interfaces, identifies COPS functional tests performed by the system, and outlines the software supplied with the system.

2.1 System Requirements

National Semiconductor recommends the following system hardware configuration:

1. COP400-PDS Product Development System.
2. COP400-T01 QUIKLOOK Tester, chip interface and diagnostic cards.
3. CRT or TTY.
4. PDS Master Disk.
5. QUIKLOOK Master Disk.
6. Test TRANSMITTAL File.
7. Cables.

The system baseline configuration is illustrated in Figure 2.1. The minimum requirements are illustrated on white background, and options, which depend on customer application, are illustrated on gray background.

PDS serves as a test pattern generator for the QUIKLOOK tester and its diagnostic test.

The QUIKLOOK, with a corresponding chip interface card, provides COP400 functional chip tests at nominal 5V power.

CRT or TTY serve as system I/O consoles.

QUIKLOOK Master disk file contains the QUIKLOOK operating system and test application data files, described in the Software section.

PDS Master disk file contains PDS operating system, file manager and development application software.

TRANSMITTAL file contains chip options and ROM data for a specific COPS chip.

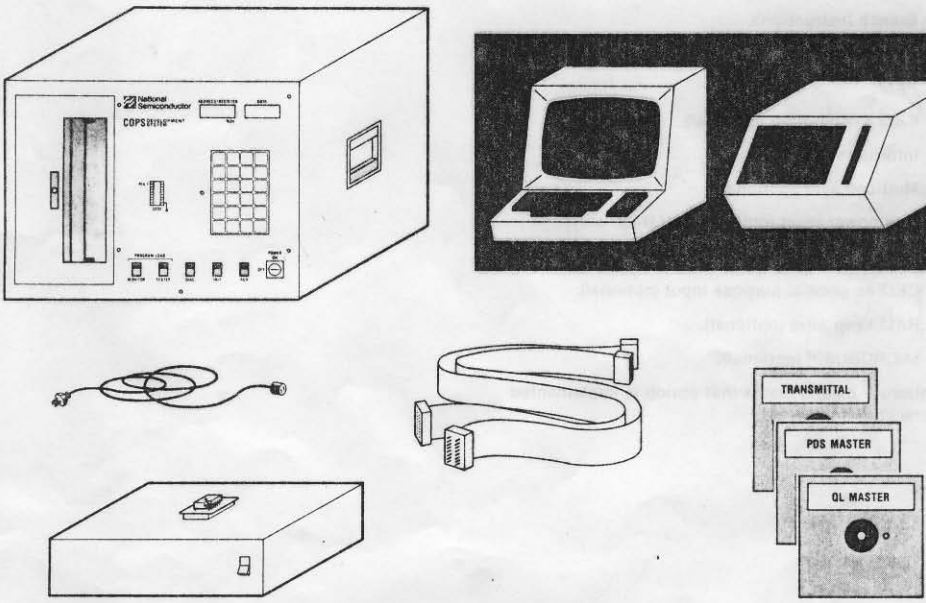

Figure 2-1. System Configuration

2.2 QUIKLOOK Tester Hardware

The tester is packaged into a 13.8 x 4.4 x 15-inch chassis containing printed circuit board, power supply, and a fan. (See Figure 2.1.)

The interface with the COPS chip and the operator is located on the top of the chassis and consists of one of the four 4 x 2.5-inch cards containing a zero insertion force DIP socket and two standard RS232 25-pin connectors on the reverse side. The diagnostic card contains two chips, two RS232 plugs, and direct pin-to-pin shorts.

The operator interface consists of three lights and START/STOP switch. The indicator lights are GREEN, RED, and YELLOW.

The PDS interface consists of two identical RS232 cables. One cable connects EMULATOR1 on PDS to EMULATOR1 on QUIKLOOK. The second cable connects EMULATOR2 on PDS to EMULATOR2 on QUIKLOOK.

2.3 COP Tests

The QUIKLOOK, under control of PDS, performs the following tests and marks the results via indicator lights: PASS = green, FAIL = red, and READY FOR TEST = yellow.

The following tests are performed on each chip at maximum frequency and 5V power supply:

1. Chip I/O.
2. Register/memory reference instructions.
3. Arithmetic.
4. Branch instructions.
5. ROM.
6. RAM.
7. CKO XTAL output (optional).
8. Interrupts (optional).
9. Multicop sync (optional).
10. Low power reset (optional 444L/445L only).
11. Dual clock (optional 420C/421C only).
12. CKO as general purpose input (optional).
13. RAM keep alive (optional).
14. MICROBUS™ (optional).

"Optional" means that if that option is implemented on the chip it is tested.

2.4 Software

The software and diagnostic programs are provided by National Semiconductor with the tester. The software, test data and diagnostic routines are resident on the COPTEST master disk.

The COPTEST MASTER disk contains QUIKLOOK system program COPTST.MP, a series of data files, used by COPTST to create the COPS chip test patterns, and the QUIKLOOK tester diagnostic program, QUIKDIAG. MP.

THE COPTEST MASTER disk file contains the following software and data:

COPTST	. MP	MAIN PROGRAM
TST410	. DAT	DATA
TST411	. DAT	DATA
TST420	. DAT	DATA
BAS420	. DAT	DATA
UCK420	. DAT	DATA
CKO420	. DAT	DATA
CKO421	. DAT	DATA
UBUS	. DAT	DATA
DUALCK	. DAT	DATA
TST444	. DAT	DATA
BAS444	. DAT	DATA
CKO444	. DAT	DATA
CKO445	. DAT	DATA
QUIKDIAG	. MP	MAIN PROGRAM

3 System Operation

This section describes the operation of the system. A list of commands is defined and an example is given to clarify the command. The creation of a TEST disk is then described, and an example test session is explained.

It is assumed that the PDS/QUIKLOOK system has been installed and the correct operation has been verified according to the procedures defined in Section 4, System Installation and Verification.

3.1 COPTST Commands

There are only seven commands that the operator needs to operate QUIKLOOK. They are:

Commands	Description
1. Build [<file name>][. TRN]]	Builds TEST file. NOTE 1
2. Directory	Displays or prints TEST file directory. NOTE 2
3. Help	Displays this list of commands available to the operator.
4. Load [<file name>]][. TRN]]	Loads TEST file into QUIKLOOK
5. New	Clears the accumulation of statistics report data.
6. Summary (*PR)	Prints the statistics of the test batch.
7. Test	Tests the chip in the QUIKLOOK socket.

Notes:

1. Only the first (underlined) character is required to execute the command.
2. Each command [<id>[. mod]] is terminated by carriage return CR, e.g., New (CR).

3.2 Operator Commands

This section describes the operator's commands issued from the system console or QUIKLOOK test button. The system requires only the first character of the command as indicated by the syntax. The remainder of the command word is optional.

INITIALIZATION

Syntax: COPTST [<FILE>[. TRN]] (CR)

Description: This is a PDS system command. It loads the COPTST program and jumps to the "Load" command. If a TEST TRANSMITTAL file is specified, it will be loaded from disk at program entry. The '.TRN' modifier is assumed if none is given. If no test file is given the disk directory is searched for a '.TRN' file and the last one found is loaded. Depressing the PDS's tester switch while in EXEC will effectively execute the 'COPTST' command with no filename.

Example:

```
EXEC, REV:A
X>@COPTST NZZ420C
COPTST,REV:X,        DATE
                COPTST COMMANDS
BUILD (B [<FILE>[. TRN]])
BUILD TRANSMITTAL FILE FOR COPTST
DIRECTORY (D)
DISPLAY DISK DIRECTORY
HELP (H)
DISPLAY THIS LIST
LOAD (L [<FILES>].) TRN]])
LOAD TESTER FOR TESTING COP CHIP
SPECIFIED BY TRANSMITTAL FILE
NEW (N)
CLEAR SUMMARY DATA
SUMMARY (S)
DISPLAY TEST SESSION SUMMARY
TEST (T)
EXECUTE TEST OF COP CHIP
LOADING FILE QUIKLOOK:NZZ420C.
TRN
TESTER READY
T>
```

GENERATION

Build Command

Syntax: B [<filename>[. TRN]](CR)

Description: The BUILD command creates a TEST TRANSMITTAL file used to test the chips. If the file name is omitted COPTST will prompt for the chip number and required option values, and read the ROM values from a chip which is known to be good. This method depends on confidence in the chips used in the ROM dump and verification. If a filename is included, the chip number, options, and ROM values will be read from the specified transmittal file. In both cases the option values are verified before the TEST TRANSMITTAL file is created. Building the test file from the input

transmittal file is the recommended method. A complete description and example of the "Build" command is included in Section 3.4.

Example:

```
T>BU CONTROL
OPTION 30:  COP BONDING
    00 = 28 PIN PACKAGE
    02-28 AND 24 PIN PACKAGES
OPTION 30:  COP BONDING 0
OPTION 30:  COP BONDING = 00
            (Y/N, CR-YES)? (CR)
ROM CODE? NZZ
COPTST DISK IN DRIVE (Y/N,CR-YES)? (CR)
CREATING FILE QUIKLOOK:NZZ420C. TRN
T>
```

LOADING

Load Command

Syntax: L [<FILES>[. TRN]](CR)

Description: The LOAD command will load QUIKLOOK with the test data to test COP chips. The test data is derived from the TEST TRANSMITTAL file given in the command. If no TRANSMITTAL file is given the disk directory is searched and the most recently created .TRN file is loaded. Upon completion of a successful load the following will occur.

a) A 'TESTER READY' message will be sent to the console.

b) The front panel display of the PDS system will read 'LOAD DONE'.

c) The lights on QUIKLOOK will cycle for light verification.

Example:

```
T>LO NGA420L
LOADING FILE QUIKLOOK: NGA420L. TRN
TESTER READY
```

TESTING

Test Command

Syntax: T (CR)

Description: The TEST command will test the COP chip if a test file has been loaded. Pushing the TEST button on the top of QUIKLOOK will also test the COP chip. The results of a test are sent to the console, PDS front panel and QUIKLOOK display lights.

Example:

```
T>T
PASS
```

New Session Command

Syntax: N (CR)

Description: This command allows the user to clear the summary data.

Example:

```
T>N
CLEAR SUMMARY DATA (Y/N,CR = YES)?
```

Help Command

Syntax: H (CR)

Description: This command displays all commands as follows:

Example:

```
H (CR)
BUILD (B [<FILE>[. TRN]])
BUILD TRANSMITTAL FILE FOR COPTST
DIRECTORY (D)
DISPLAY DISK DIRECTORY
HELP (H)
DISPLAY THIS LIST
LOAD (L [<FILE>[. TRN]])
LOAD TESTER FOR TESTING COP CHIP
SPECIFIED BY TRANSMITTAL FILE
NEW (N)
CLEAR SUMMARY DATA
SUMMARY (S)
DISPLAY TEST SESSION SUMMARY
TEST (T)
EXECUTE TEST OF COP CHIP
```

Directory Command

Syntax: D (CR)

Description: Directory command lists the contents of the disk file in the PDS and provides summary of sector usage.

Example: T>D

DIRECTORY FOR: QUIKLOOK "COMPLETED TEST DISK"

FN D	NAME		TYPE	SIZE	PL	VN
1	COPTST	.MP	MAIN PROGRAM	40	2	0
2	TST410	.DAT	DATA	8	2	0
3	TST411	.DAT	DATA	8	2	0
4	TST420	.DAT	DATA	8	2	0
5	BAS420	.DAT	DATA	4	2	0
6	UCK420	.DAT	DATA	4	2	0
7	CKO420	.DAT	DATA	4	2	0
8	CKO421	.DAT	DATA	4	2	0
9	UBUS	.DAT	DATA	4	2	0
10	DUALCK	.DAT	DATA	4	2	0
11	TST444	.DAT	DATA	8	2	0
12	BAS444	.DAT	DATA	4	2	0
13	CKO444	.DAT	DATA	4	2	0
14	CKO445	.DAT	DATA	4	2	0
15	QUIKDIAG.	.MP	MAIN PROGRAM	12	2	0
16	NZZ420C	.TRN	SYSTEM	12	2	0
17	NYY421C	.TRN	SYSTEM	12	2	0
18	NXX420L	.TRN	SYSTEM	12	2	0

SECTORS BAD: 0
SECTORS USED: 164
SECTORS FREE: 452

The last TEST TRANSMITTAL file built is also last on the disk directory. Unless a filename is specified, the TEST TRANSMITTAL file NXX4201 .TRN will be loaded if COPTST is loaded or the "Load" command is given.

Summary Command

Syntax: S[*PR](CR)

Description: Summary command displays the batch test report. This feature is particularly useful in incoming inspection and quality control. If the '*PR' option is used the summary will be sent to the printer.

a) BAD CLOCK refers to a failure in one of the following.
   1) XTAL output
   2) Low power reset
   3) SK output
   4) Multi cop sync

b) BAD LOGIC refers to a failure in one of the following.
   1) I/O port
   2) Instruction set
   3) RAM keep alive
   4) Dual clock

c) BAD ROM refers to a failure in the users ROM pattern.

Example:

```
T>S
PDS TEST SESSION SUMMARY
GOOD        4 80%   BAD CLOCK   1
BAD         1 20%       LOGIC   0
                        ROM     0
TOTAL       5
```

3.3 Creation Of Test Disk

When the PDS and QUIKLOOK operations have been verified a complete TEST disk should be constructed. A complete TEST disk consists of a duplicate of the MASTER TEST DISK received with the QUIKLOOK plus the TEST TRANSMITTAL file(s) created by the BUILD command. Figure 3.1 illustrates the generation process.

The TEST DISK file can be generated in one of two ways:

1. Using a TRANSMITTAL file as an input and QUIKLOOK MASTER as a program and data, or
2. Using a known good chip, QUIKLOOK tester and MASTER file.

The "Build" command provides an interactive method for putting a verified TRANSMITTAL file on the TEST disk. Either of the following two methods may be used to enter the required data.

1) The TRANSMITTAL file sent to NSC for the masking of the part is read to obtain chip number, option values, and ROM values. This is the preferred method.

***** SEE NOTE ON FOLLOWING PAGE *****

2) The chip number and option values are entered from the console. The ROM values are read from a chip that is known to be good, then verified with five other chips.

For both input methods the specified options will be checked for conflicts or obsolete values. Option values must be correct before the TEST TRANSMITTAL file is generated. The program will prompt for the new values of the required options. The TEST TRANSMITTAL file will be named ZZZXXX. TRN, where:

ZZZ = the three letter ROM CODE

XXXX = the chip number (and letter)

Both the ROM CODE and the chip number are stamped on the chip. For parts with a double bonding option, two output files will be generated, uniquely named by the ROM CODES and chip numbers. The files may be put on separate disks, a necessary procedure if the tester is to be used without a

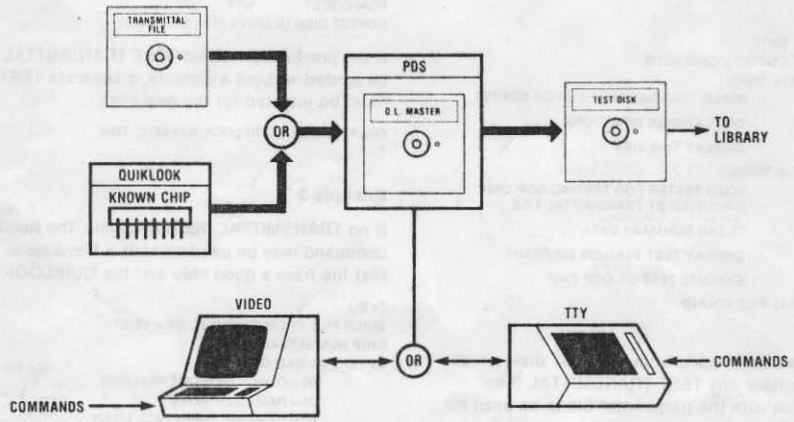

Fig. 3.1 Test Disk Generation

console. The "Build" command may be used without the tester if a TRANSMITTAL file is to be used as input. If a TRANSMITTAL file has valid option values, they are copied to the TEST TRANSMITTAL file.

NOTE

The TEST TRANSMITTAL file generated by COPTST will be a duplicate of the TRANSMITTAL file sent to NSC for the Cop chip's masking with two exceptions:

1) The user must use the same option values that are listed in the VERIFICATION FORM sent back from National Semiconductor. These are the same options received on the TRANSMITTAL file unless a conflicting option pair or obsolete option had been selected.

2) If the 'double bonding option' is requested a TEST TRANSMITTAL file is generated for both packages.

   Example: The User's chip die was placed in COP420 and COP421 packages. If this user wished to test a COP421 part it would be necessary to use the TEST TRANSMITTAL file generated by the "BUILD" command for the COP421 bonding.

3.3.1 Examples Of Build Sessions

This section provides two typical build sessions. The first example is based on command input from the system console and generating the TEST file. The second example illustrates a build procedure without a TRANSMITTAL file.

Example 1

Generate the TEST file:

```
X>@COPTST
COPTST,REV:X, DATE
            COPTST COMMANDS
BUILD (B [<FILE>[. TRN]])
                    BUILD TRANSMITTAL FILE FOR COPTST
DIRECTORY (D)       DISPLAY DISK DIRECTORY
HELP (H)            DISPLAY THIS LIST
LOAD (L [<FILE>[. TRN]])
                    LOAD TESTER FOR TESTING COP CHIP
                    SPECIFIED BY TRANSMITTAL FILE
NEW (N)             CLEAR SUMMARY DATA
SUMMARY (S)         DISPLAY TEST SESSION SUMMARY
TEST (T)            EXECUTE TEST OF COP CHIP
NO TRANSMITTAL FILE FOUND
T>
```

COPTST has been loaded from the TEST disk, which does not yet have any TEST TRANSMITTAL files. Insert the disk with the transmittal file to be used for input.

```
T>BU CONTROL
OPTION 30: COP BONDING
        00 = 28 PIN PACKAGE
        02 = 28 and 24 PIN PACKAGES
OPTION 30: COP BONDING 2
OPTION 30: COP BONDING = 02 (Y/N, CR = YES)?
INVALID CKO OPTION
CLOCK OPTION CONFLICT
```

The input TRANSMITTAL file contains obsolete CKO and Clock option values. The old values are ignored.

```
OPTION 02: CKO OUTPUT
        00 = CLOCK GEN OUT
        02 = GENERAL INPUT, VCC LOAD
        04 = GENERAL INPUT, HI-Z
OPTION 02: CKO OUPUT 2
OPTION 02: CKO OUTPUT = 02 (Y/N, CR = YES)
OPTION 03: CKI INPUT
        00 = OSC /16
        01 = OSC/8
        02 = OSC /32
OPTION 03: CKI INPUT 1
OPTION 03: CKI INPUT = 01 (Y/N, CR = YES)?
OPTION 28: DO OUTPUT
        00 = STANDARD OUTPUT
        01 = OPEN DRAIN
OPTION 28: DO OUTPUT 0
OPTION 28: DO OUTPUT = 00 (Y/N, CR = YES)?
OPTION 31: CLOCK MODE
        02 = NORMAL OSC IN, SKT INSTRUCTION
        03 = RC OSC/8, SKT INSTRUCTION
        04 = NORMAL OSC IN, IT INSTRUCTION
        05 = RC OSC/8 IT INSTRUCTION
        06 = NORMAL OSC, DUAL CLOCK(RC)
        07 = NORMAL OSC, DUAL CLOCK(EXT CLK)
OPTION 31: CLOCK MODE 3
OPTION 31: CLOCK MODE = 03 (Y/N, CR = YES)?
BONDING          420C
ROM CODE?        NZZ
```

The ROM CODE prompt indicates the above option values are valid. The option prompting continues until the values are valid.

```
COPTST DISK IN DRIVE (Y/N, CR = YES)?
```

A TEST disk should be inserted in the drive at this time.

```
CREATING FILE QUIKLOOK:NZZ420C. TRN
BONDING          421C
ROM CODE?        NYY
COPTST DISK IN DRIVE (Y/N, CR = YES)?
```

If the previously created TEST TRANSMITTAL file is to be loaded without a console, a separate TEST disk must be inserted for the new one.

```
CREATING FILE QUIKLOOK:NYY421C. TRN
T>
```

Example 2

If no TRANSMITTAL file is available, the Build command may be used without a filename to build a test file from a good chip and the QUIKLOOK™.

```
T<BU
BUILD FILE FROM CHIP (Y/N, CR = YES)?
CHIP NUMBER: 420L
OPTION 02: CKO OUTPUT
        00 = CLOCK GEN OUT XTAL/RES
        01 = RAM KEEP ALIVE
        02 = GENERAL INPUT, VCC LOAD
        03 = GENERAL INPUT, HI-Z
        04 = MULTICOP SYNC IN
        05 = MULTICOP SYNC ( /8 )
OPTION 02: CKO OUTPUT 2
OPTION 02: CKO OUTPUT = 02 (Y/N, CR = YES)?
```

```
OPTION 03: CKI INPUT
        00 = OSC /32
        01 = OSC /16
        02 = OCS/8
        03 = RC/4
        04 = OSC (SCHMITT IN)/4
OPTION 03: CKI INPUT 0
OPTION 03: CKI INPUT = 00 (Y/N, CR = YES)?
OPTION 35: COP BONDING
        00 = 28 PIN PACKAGE
        02 = 28 and 24 PIN PACKAGES
OPTION 35: COP BONDING 0
OPTION 35: COP BONDING = 00 (Y/N, CR = YES?
INSERT COP CHIP, CREATE TEST FILE (Y/N, CR = YES?
BAD COP CHIP
INSERT COP CHIP, CREATE TEST FILE (Y/N, CR = YES)?
```

This could result from improperly inserting the chip into the test socket. Verify proper insertion and try again.

```
CREATING TEST FILE, 3 MINS
MARK 5 COP CHIPS 1 THRU 5
INSERT COP CHIP #, COMPARE (Y/N, CR = YES)?
```

The following procedure allows a verification of the ROM data obtained from the first chip before creating the TEST TRANSMITTAL file. It compares ROM data with five other chips.

```
COMPARE DONE
INSERT COP CHIP #2, COMPARE (Y/N, CR = YES)?
COMPARE DONE
INSERT COP CHIP #3, COMPARE (Y/N, CR = YES)?
COMPARE DONE
INSERT COP CHIP #4, COMPARE (Y/N, CR = YES)?
COMPARE DONE
INSERT COP CHIP #5, COMPARE (Y/N, CR = YES)?
CHIP #1, PASS
CHIP #2, PASS
CHIP #3, PASS
CHIP #4, PASS
CHIP #5, PASS
ROM CODE? NXX
COPTST DISK IN DRIVE (Y/N, CR = YES)?
CREATING FILE QUIKLOOK:NXX420L. TRN
T>
T>D
```

DIRECTORY FOR: QUIKLOOK "COMPLETED TEST DISK"

FN	D	NAME		TYPE	SIZE	PL	VN
1		COPTST	.MP	MAIN PROGRAM	40	2	0
2		TST410	.DAT	DATA	8	2	0
3		TST411	.DAT	DATA	8	2	0
4		TST420	.DAT	DATA	8	2	0
5		BAS420	.DAT	DATA	4	2	0
6		UCK420	.DAT	DATA	4	2	0
7		CKO420	.DAT	DATA	4	2	0
8		CKO421	.DAT	DATA	4	2	0
9		UBUS	.DAT	DATA	4	2	0
10		DUALCK	.DAT	DATA	4	2	0
11		TST444	.DAT	DATA	8	2	0
12		BAS444	.DAT	DATA	4	2	0
13		CKO444	.DAT	DATA	4	2	0
14		CKO445	.DAT	DATA	4	2	0
15		QUIKDIAG	.MP	MAIN PROGRAM	12	2	0
16		NZZ420C	.TRN	SYSTEM	12	2	0
17		NYY421C	.TRN	SYSTEM	12	2	0
18		NXX420L	.TRN	SYSTEM	12	2	0

SECTORS BAD: 0
SECTORS USED: 164
SECTORS FREE: 452

The last TEST TRANSMITTAL file built is also last on the disk directory. Unless a filename is specified, the TEST TRANSMITTAL file NXX420L. TRN will be loaded if COPTST is loaded or the "Load" command is given.

3.4 Testing COP Chips

This section provides an overview of the hardware configuration in the test mode and provides two examples of a complete test session with and without system console as a command input and a report output device.

The hardware configuration in the test mode is illustrated in Figure 3.2. The system console is optional. If the TEST file is generated elsewhere, and a batch report is not required, the console is not necessary.

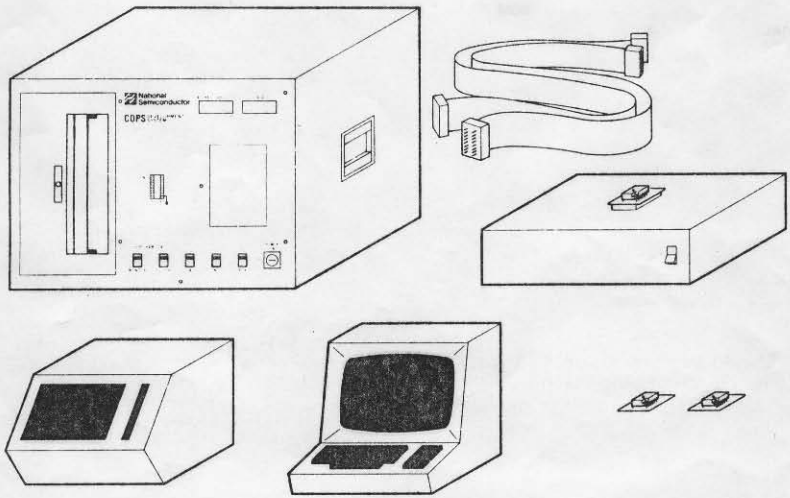

Fig. 3-2 Test Configuration

The loading of the TEST file into QUIKLOOK is executed via L[<filename>[, TRN]](CR) console command or by pressing the TESTER switch on the PDS.

T>

Example 1

LOAD TEST FILE INTO QUIKLOOK.

```
T>L NZZ420C
LOADING FILE QUIKLOOK: NZZ420C. TRN
TESTER READY
```

BEGIN TEST.

```
T>T
PASS
T>T
PASS
T>S
PDS TEST SESSION SUMMARY
GOOD        2   100%  BAD  CLOCK   0
BAD         0     0%       LOGIC   0
                           ROM     0
TOTAL       2
T>N
CLEAR SUMMARY DATA (Y/N, CR = YES)?

T>S
PDS TEST SESSION SUMMARY
GOOD        0   100%  BAD  CLOCK   0
BAD         0     0%       LOGIC   0
                           ROM     0
TOTAL       0
T>T
PASS
T>T
PASS
T>T
FAIL
```

GENERATE REPORT

```
T>S
PDS TEST SESSION SUMMARY
GOOD        2    67%  BAD  CLOCK   1
BAD         1    33%       LOGIC   0
                           ROM     0
TOTAL       3
```

LOAD ANOTHER FILE.

```
T>L NYY421C
LOADING FILE QUIKLOOK: NYY421C. TRN
TESTER READY
```

TEST CHIP NYY421C. TRN

```
:
:
```

GENERATE REPORT

```
T>S
PDS TEST SESSION SUMMARY
GOOD        0   100%  BAD  CLOCK   0
BAD         0     0%       LOGIC   0

TOTAL       0
T>T
PASS
```

Example 2

In this example the TEST file has been generated as in Example 1.

a. Turn on PDS.

b. Turn on QUIKLOOK.

c. Push PDS INIT switch.

d. Place TEST disk in disk drive.

e. Push PDS TESTER switch.

f. Wait for cycling lights on QUIKLOOK or PDS front panel message 'LOAD DONE'.

g. Place COP chip in test socket.

h. Push TEST button.

i. Read test results from display lights or PDS front panel display.

j. Remove and bin COP chip; get next chip and go to step 'g' if not done.

4 QUIKLOOK Installation and Verification

Once the PDS operation has been verified the verification of the tester can proceed using the following steps.

a. * * * * * * * * * * * * *
   * DO NOT insert Diagnostic Card until *
   * step m. Premature insertion may *
   * lead to damage of the QUIKLOOK. *
   * * * * * * * * * * * * *

b. Turn off the PDS.

c) Make sure the on/off switch on QUIKLOOK is off.

d) Plug in the two RS232 cables as described in the System Description.

e) Connect the system console.

f) Plug in the QUIKLOOK's power cord.

g) Turn on the PDS system.

h) Turn on QUIKLOOK.

i) If no 'CR' appears in the front panel of the PDS System depress the INIT switch.

j) Press the carriage return on the system console to log on the console.

k) Place the TEST disk in the disk drive.

l) Type @QUIKDIAG on the system console. The QUIKDIAG program will sign on with QUIKDIAG, REV A, date and a menue of commands. If this does not happen, go back to step a.

m) Insert the QUIKLOOK DIAGNOSTIC card on QUIKLOOK.

n) Type DI (CR) on the console. The PDS will now execute a complete Diagnostic on the QUIKLOOK. This should take about one minute. Upon successful completion of the test, a response of 'PASS DIAGNOSTIC' will be printed on the console. If this does not happen the user is referred to National Semiconductor's Microcomputer Technical Support Manager.

o. Remove the QUIKLOOK DIAGNOSTIC card from the QUIKLOOK.

The QUIKLOOK operation has now been verified, the QUIKLOOK is now ready for building test files and testing chips in the following steps.

a) Insert the correct Chip Interface Card on QUIKLOOK for the COP CHIP you will be testing.

b) Type @COPTST (CR) on the system console panel.

The PDS will respond by loading the COPTST system program. COPTST will load QUIKLOOK to test the COP chip specified by the last TEST TRANSMITTAL file that was found on the disk directory. If no TRANSMITTAL file is found, the program prompt is returned to the console.

Appendix A

This appendix describes the QUIKLOOK logic mechanization, control signals, timings and the interface between the tester and the chip test card interface.

A.1 Theory of Testing COP400 Microcontrollers

The following paragraphs provide some insight into the test mode and the mechanics of testing a COP400 Microcontroller. The basic test philosophy requires that four major functions be exercised. We need to:

1. Synchronize the device and QUIKLOOK TESTER.
2. Test the internal logic and I/O.
3. Test the RAM.
4. Verify the ROM program.

If the device performs all of these four steps properly, the device is good. This is a reasonable assumption with a standard device that has a debugged test routine and is ROM programmed. By attacking the problem on a "sum of the parts" approach there is no need to do an exhaustive functional test on routine production parts.

Built-In Test Features

The first step in testing the COP400 devices is to understand the built-in test control features. This involves the SI, SO and the L lines. The SO pin has been designed to be the control pin for testing. The pin will normally be in an active low state and, when forced high externally, place the chip in the test mode. It should be noted that this output can sink considerable current. By limiting the voltage to the 2.0-3.0V range one cannot damage the device, whereas the application of a higher voltage could. When forced into the test mode the SI pin controls the sub mode of the chip. With SI high the data placed on the L port is used as an instruction. When SI is low (and the L output is enabled) the contents of the ROM will be dumped out through the L port. Certain other internal functions have been implemented to allow these modes but these are not part of the basic operation.

Sync Between QUIKLOOK and DUT

In order to be able to test a COP chip, the tester is synchronized with the device under test (DUT). By using an external oscillator the two run at the same frequency. This is true regardless of the option or type of oscillator chosen for the chip. In addition to running at the same frequency, the chip and tester are in sync on a bit basis. The SK signal is used as a bit/instruction clock until stopped by software in the program. It should be noted that the oscillator frequency is programmed to a rate of 4, 8, 16, or 32 times higher than SK. The basic use of this "sync counter" is to derive the proper timing for loading data and instructions into the chip and to verify the outputs.

Internal Logic Test

With the device and the tester in sync, actual testing may begin. To place the chip into the logic test mode the SO output is pulled to a high level (between 2.0V and 3.0V) and SI is pulled to a high level. On power-up (or after reset) the SO line is set to a zero by the internal logic. An internal sense line will detect the forced condition and provide test control. The tester should at this point force instructions into the L port. These instructions will be executed as if they were from the ROM.

ROM Dump

Successful operation of the internal logic tests leads to the final test phase, ROM comparison. The ROM dump mode sequence begins by forcing a JMP to an address. After going to this address, execution of an "LEI 4" is done (L lines to the output port), external buffers are disabled, and the SI pin is taken low. This allows data out and removes potential level conflicts. The ROM dump test logic increments the PC for each SK cycle, allowing a byte-by-byte ROM comparison. In this mode the controller is not executing the code because the internal skip line is enabled throughout the sequence.

A.2 Theory of Operation

The chip test is organized in four major parts:

1. a. COP synchronization test
   b. Multicop sync test (optional)
   c. CKO XTAL output (optional)
   d. Low power reset (optional)

2. a. Logic test

   This test forces instructions (S1 = 1, SO = 1) and compares the G lines to the expected outputs. The forced instructions on the L lines come from shared memory. Tester memory 0-1k is used for the expected outputs and is 4 bits wide.

3. a. Chip I/O functions
   b. Interrupts
   c. Branch instructions
   d. RAM keep alive

   In this part, PDS shared memory contains alternating sections of forced instructions and partial ROM dumps. The sections of ROM tested in this part, combined with the ROM dump of part 4 test the entire ROM. Tester memory 1-2k contains expected outputs (4 bits), forced inputs (4 bits), and I/O select (4 bits).

4. a. ROM verification

   For this test PDS shared memory O/010 is filled with the required instructions to initialize the COP chip for a ROM dump. Locations 011 through the end are filled with the ROM pattern. Tester memory is unused and unaltered.

A.3 Description Of Implementation

In Figure A.1, lines D0-D7 are the data lines of shared memory. The address lines A0-A10 are the address lines of shared memory. EXT EVO-3 and the SKIP LINE are connected to the TRACE memory. RST*, PROMDIS*, and TRACEOUT are signals from the PDS TARGET card and CLK is a signal from the tester to the TARGET card.

There are three status latches (8334) to set up the operation of the tester. The latches, shown as part of the control logic in Figure A.1, are loaded only when the chip and the test board are reset. The test board is reset exactly as the Emulator cards are reset, i.e., via the target board RST* line. To load the latches the address lines are TRI-STATED and the pull-up resistors on these lines force an address of 07FF. The status word is placed at 07FF in PDS shared memory and the target board 'PROMDIS*' signal is brought from low to high to low to strobe the data into the latches.

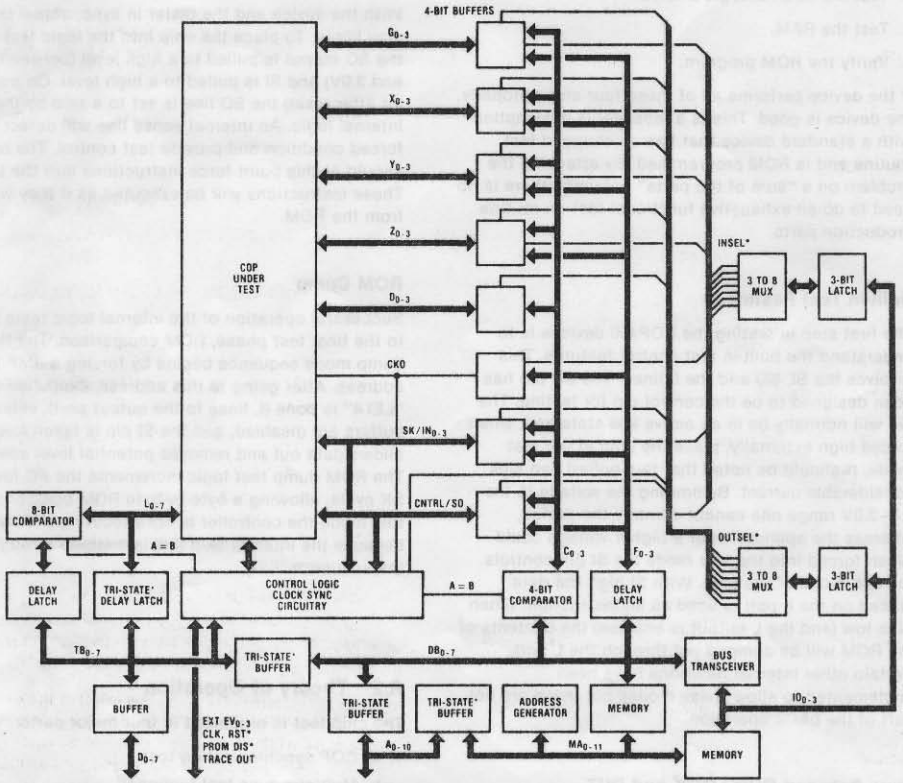

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Figure A-1. Tester Block Diagram

The data format for the latches is:

bit	7	6	5	4	3	2	1	0
data	x	x	A2	A1	A0	D2	D1	D0

WHERE:

A2	A1	A0	D2	D1	D0
0	0	0	FREQ2	FREQ1	FREQ0
0	0	1	TSTSIGEN*	XTAL*	EXTEVCTL
0	1	0	DUMP/TEST*	SYNCD	MULTI COP SYNC*
0	1	1	RESET CHP*	DIV1	DIV0
1	0	0	PC RESET*	LOAD*	RE/WR*
1	0	1	RAM KPALV	VCC/CK	DUAL CLK
1	1	0	PASS*	FAIL*	EOT*
1	1	1	LCPART	TRISTRST*	TST440

Description of Bits

FREQ 2/0 — These bits set the test board clock and the COP chip CKI according to the following table:

FREQ2	FREQ1	FREQ0	FREQUENCY	
0	0	0	0.250 MHz	
0	0	1	0.500 MHz	
0	1	0	1.000 MHz	
0	1	1	2.000 MHz	
1	0	0	4.000 MHz	
1	0	1	1.000 MHz-	L, CMOS PARTS
1	1	0	2.000 MHz-	L, CMOS PARTS

TSTSIGEN* — A low on this signal enables L line drivers, S1 driver and the IN line drivers on the the DUT, high they are TRI-STATED* .

XTAL — a high on this signal tristates all inputs to CKO.

EXTVCTL — This signal multiplexes signals out the external event lines and trace clock line according to the following table.

EXTEVCTL	EV11	EV10	EV01	EV00	TRACE CLOCK
0	CKO	CKI	SK*	SKD*	0.5 MHz
1	HALFSPD*	CKI	STARTSW	ERROR	SKD*

DUMP/TEST* — If high SHARED memory will be compared against the ROM of the COP chip. If low the board will be in the test mode.

SYNCD — When this signal is toggled low for n seconds the tester will sync with the COP chip.

WHERE: — n> = 1/SKD Hz *(CKI DIVIDER)

MULTI COP SYNC* — Will send the inverted sync to CKO.

RESET CHP* — This bit resets the COP chip. The PDS RST* also resets the COP chip.

DIV1/DIV0 — Will setup the divider of the developed SKD to that of the DUT according to the following table:

DIV1	DIV0	CKI DIVIDER
0	0	32
0	1	16
1	0	8
1	1	4

PC RESET* — Will rest the pseudo program counter to zero.

LOAD* — Reconfigures the test board to transfer SHARED memory to the test board's memory and verify it according to RE/WR*

RE/WR* — A high level configures the board to verify tester memory.

RAMKPALV — Puts +5v on CKO to power the ram on chips with that option.

V_{CC}/CK — A high level enables Vcc and clock to chip. A low level in combination with the TRISTRST* low applies low voltage to the chip to test power low reset.

DUAL CLK — A high level applies the board SKD to chip output DO to test the dual clock function.

PASS* — Signal to test box to signify a good device. Also goes to the handler thru opto isolators for proper binning of the parts.

FAIL* — Signal to the test box to signify a bad device. Also goes the handler for proper binning.

EOT* — Signal goes to the test box to signify that the tester is ready to test the next device. Also goes to the handler to signify that the tester has finished testing the previous part and valid PASS/FAIL data are present.

LCPART — A high level causes the SKD of the tester to be delayed by 1 microsecond, for correct signal strobing of low power and cmos parts. A low value causes SKD to be delayed by 200 nanoseconds needed for standard power parts.

TRISTRST* — If low the reset* line of the DUT is tristated from the tester and 4.2 volts is fed to V_{CC} of the DUT. The reset level may be read from the skip line to test low power reset. Hi the reset line is connected to the tester and V_{CC} is 5 V or 0 according to V_{CC}/CK.

TST440 — If this signal is high a double SKD is developed from a single SK for testing COP 440.

A.4 Loading of Tester Memory

Writing to memory is done by presetting the following latches.

a. set FREQ2-0 and DIV1-0 to low for slow data transfer.

b. set R/W* to low for writing data

c. set LOAD* low to put the test board in load and verify mode.

d. toggle PCRST* from hi to low back hi, to reset the address counters.

With all the latches set, load shared memory with data to be transferred to tester memory and perform a trace on address 07FE. When the trace is done the transfer is complete.

The address generator (pseudo PC) sends addresses to shared memory over lines A0-A10 and to tester memory. The test data is brought to the tester memory from shared memory on lines D0-D7.

To verify the tester memory, the latches are set as before except R/W* is set high. Memory data is transferred to the PDS trace memory by tracing on the beginning address of a block of 254 bytes of data to be verified. Before each verification trace, the PCRST* must be toggled as before. The data is brought to PDS via lines A0-A10.

To facilitate test organization, QUIKLOOK tester memory is configured differently for testing than for loading. During loading, tester memory is 2k x 8 bits, and is loaded directly from shared memory. The following is a map of tester memory during loading.

```
0     (C. 4 bits) (I. 4 bits)
        :           :
        :           :
1k    (C. 4 bits) F. 4 bits)
        :           :
        :           :
2k
```

During testing, tester memory 1k x 4 bits followed by 1k x 12 bits. The following is a map of tester memory during testing in parts two and three of the test.

```
0     (C. 4 bits)
        :
        :
1k    (C. 4 bits)(F. 4 bits)(I. 4 bits)
        :           :          :
        :           :          :
2k
```

The following is a complete map of memory used during testing in parts two and three of the test.

```
                SHARED MEMORY      TESTER MEMORY
0               (L. 8 bits)        (C. 4 bits)
                  :                  :
                  :                  :
1k              (L. 8 bits)        (C. 4 bits)(F. 4 bits)(I. 4 bits)
                  :                  :          :          :
                  :                  :          :          :
2k
```

where:

L. is defined as instructions forced on the L lines or ROM values dumped from the L lines.

C. is defined as data sent to a four bit comparator.

F. is defined as the data forced on selected input.

I. selects the output to be compared or the input to be forced according to the following table:

I. SELECT	C. DATA COMPARED TO:
0	Chip G outputs
2	R outputs bits 0-3 (COP440)
4	L lines compared to SHARED memory.
6	SO (bit 0)
8	Chip D outputs
A	R outputs bits 4-7 (COP440)
C	H outputs (COP440)
E	SK (bit 0)

I. SELECT	F. DATA FORCED TO:
1	Chip G inputs
3	R inputs bits 0-3 (COP440)
5	CKO (bit 0)
7	RST* PCS* SI SO (bits 3-0)
9	Not used
B	R inputs bits 4-7 (COP440)
D	H inputs (COP440)
F	IN inputs

PCS*	This signal will halt the test board at the corresponding address. The test board will resume testing at that address after toggling the LOAD* line.
IO	This signal determines if 13-1 are setting up an input or output latch. When an input or output latch is not selected they remain at the last value of 13-1 given.

During part one of the tests, the control latches are loaded to set up for multiCOP sync, clock, divide by, and tester sync. CKO, CKI, SK*, SKD*, are routed to the external event lines of TRACE memory and sampled with 0.5 MHz clock.

TRACE memory is then analyzed by PDS to determine that SK has the correct number of CKI pulses for the specified divide-by, and SKD* is in sync with SK*. If CKO is specified by the options to be part of the clock circuit, it is checked to be sure it is inverted CKI.

During part two of the test the control latches are loaded to set up for logic tests, and HALFSPD*, CKI, STARTSW, and ERROR are routed to the external event lines of TRACE memory and SKD* is used to clock TRACE memory. The chip logic is tested with the instructions coming from shared memory via the D0-D7 lines through a delay latch. The delay latch is used to offset any delay in the system memory. The instruction fetched from memory is offset one cycle such that the data is present in the latch at the time the data is required and the address is incremented during the time the chip is executing the previous instruction. The data to be compared to the G lines is routed to a four bit comparator and the result of the comparison is sampled on the rising edge of the tester generated SK in the control logic. If an error occurs the PDS is signalled via the external event lines.

During part three of the test the chip I/o functionality and transfer of control instructions are tested. Again, the D0-D7 lines force instructions and the input data is routed under control of the tester memory to the appropriate input. The appropriate output is compared to data supplied by the tester memory. The input and output ports are selected via the INSEL* and OUTSEL* multiplexers. During a portion of this test, the transfer of control instructions are tested by forcing instructions on D0-D7. When the chip's internal program counter has been set to the desired address, the SI/SO signals are set to output ROM data on the L lines. At that time the data on the L lines is compared to the data from shared memory via the 8 bit comparator. The data on D0-D7 at this time is ROM data in order to verify that the transfer of control instructions are functional.

For part four of the test, the data in shared memory is changed to contain some test instructions and the remainder of the user's ROM. The test instructions are forced on the L lines through D0-D7 top set the internal PC to a known location. At this time SI/SO are set to dump the ROM and the data on D0-D7 is then compared to shared memory to verify the ROM data for the chip under test.

A.5 Chip Handler Interface

QUIKLOOK provides optically buffered control signals for integrated circuit handlers. Before any attempt to connect a handler is made, QUIKLOOK should be verified as fully functional using the provided Chip Interface Card.

Chip handler control signals are available from the female RS232 socket labeled 'HANDLER' at the rear of QUIKLOOK. Table A.2 gives the signal pin description of the 'HANDLER' plug and Figure A.2 outlines the circuit diagram of the optical buffers.

A signal is required from the automatic handler to tell the tester to start a new test. The tester will delay start of new test 10 ms from the receipt of this signal or until this signal is removed in case the signal is from a switch that is being held down until the EOT signal is removed. The PASS and FAIL signals to control the binning precede the EOT signal by 700 microseconds. Table 7 outlines the logic conditions of the control signals with respect to the polarity strap.

If the HALFSPD* strap is in place the tester board will test the parts at a reduced speed. The frequency will be one half max frequency. The tester will furnish three signals for use with automatic handling equipment. The signals will be EOT, PASS, and FAIL. The tester will require one signal from the handler. That signal will be START TEST.

Table A.1 Optical Transistor State

			Polarity Strap		
Signal	**Light**		**In**		**Out**
PASS	On	!	Off	!	On
	Off	!	On	!	Off
FAIL	On	!	Off	!	On
	Off	!	On	!	Off
EOT	On	!	Off	!	On
	Off	!	On	!	Off
Signal	**Input**		**In**		**Out**
TEST	I = 12 ma	!	No Test	!	Test
	I = 0	!	Test	!	No Test

Table A.2 Handler Signal Pins

Pin No.	Signal name	Definition
10	PASS +	Bin signal for good chip, same operation as PASS lite
9	FAIL +	Bin signal for bad chip, same operation as FAIL lite.
8	EOT +	End-of-Test. Bin signals valid and ready to start another Test, same operation as EOT lite.
7	SIGCOM –	Signal Common return for PASS, FAIL and EOT.
6	POLARITY	A strap between POLARITY and POLSENCE will cause PASS, FAIL EOT and TEST Signals to be negative logic. (See Table 4)
5	POLSENCE	Part of POLARITY strap
4	TEST +	Input Signal to start a test, same operation as TEST Button.
3	TEST –	Return for TEST + signal.
2	HALFSPEED	A strap between HALFSPEED and HALFSENCE will cause the COP CHIP to be tested at Half its maximum clock speed.
1	HALFSENCE	Part of HALFSPEED strap

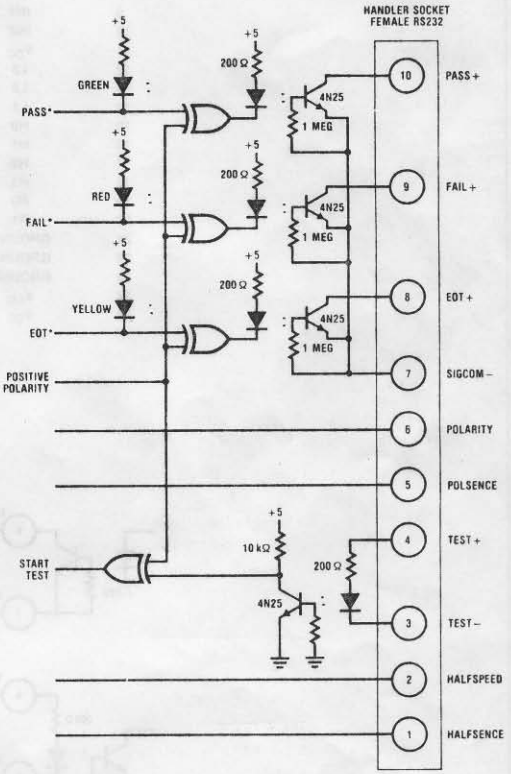

Figure A-2. Tester Handler Interface

The user's cable from the Tester's chip interface Card sockets to the handler should be kept under two feet. Table A.3 gives the pin outs of the Chip Interface Card RS232 connection sockets. The user must connect the signal pins in the same manner as the Chip Interface Card. In electrically noisy environments it may be necessary tc place a 680 pF capacitor from chip GND to V_{CC} at the handler test socket and test the chip at half speed using the HALF SPEED strap option. DO NOT attempt to connect chip ground to earth ground or any other equipment besides the chip test socket.

For the user's convenience Table A.4 gives the electrical characteristics of the 4N25 optical isolators used. A sample TTL interface circuit is given in Figure A.2. The handler interface has a POLARITY strap option that allows the user to invert the input and output control signals from positive to negative logic.

Table A.3 Pinouts For Chip Interface Card

Pin #	J6 Signal Name	J7 Signal Name
1	GROUND	R2
2	CKO	R3
3	CKI	R4
4	RESET*	R5
5	L7	R6
6	L6	R7
7	L5	L0
8	L4	S1
9	IN1	SO
10	IN2	SK
11	V_{CC}	IN0
12	L3	IN3
13	L2	G0
14	L1	G1
15	H0	G2
16	H1	G3
17	H2	D3
18	H3	D2
19	R0	D1
20	R1	D0
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	V_{CC}	V_{CC}
25	V_{CC}	V_{CC}

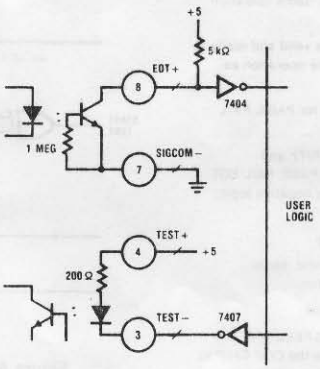

Figure A-3. Sample Interface

Table A.4 Electro-Optical Characteristics ($T_A = 25°C$, unless otherwise specified.)

	Parameter	Conditions	Min.	Typ	Max.	Units
LED Characteristics						
I_R	Reverse Leakage Current	$V_R = 3.0V$, (Note 4)			100	μA
V_F	Forward Voltage	$I_F = 50\,mA$, (Note 4)		1.2	1.5	V
C	Capacitance	$V_R = OV$, f = 1.0 MHz		150		pF
Phototransistors, $I_F = 0$						
H_{FE}	DC Current Gain	$V_{CE} = 5.0V$, $I_C = 500\,\mu A$		500		
I_{CBO}	Collector-Base Dark Current	$V_{CB} = 10V$ Emitter Open, (Note 4)			20	nA
BV_{CBO}	Collector-Base Breakdown Voltage	$I = 100\,\mu A$, $I_E = 0$, (Note 4)	70			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 1.0\,mA$, $I_B = 0$ (Note 4)	30			V
BV_{ECO}	Emitter-Collector Breakdown Voltage	$I_E = 100\,\mu A$, $I_B = 0$, (Note 4)	7.0			V
I_{CEO}	Collector-Emitter Dark Current	$V_{CE} = 10V$, Base Open			50	nA
Coupled Characteristics						
I_C	Collector Output Current	$V_{CE} = 10V$, $I_F = 10\,mA$, $I_B = 0$, (Note 4)	2.0	10		mA
V_{ISO}	Isolation Voltage		2500			V
$V_{CE(SAT)}$	Collector-Emitter Saturation	$I_C = 2.0\,mA$, $I_F = 50\,mA$, (Note 4)		0.2	0.5	V
C_{ISO}	Isolation Capacitance	V = 0, f = 1.0 MHz		0.5		pF
BW	Bandwidth	$I_F = 10\,mA$, $V_{CE} = 5.0V$, $R_L = 100\,\Omega$, (Note 3)		150		kHz
t_{ON}	Output "ON" Time	$I_F = 10\,mA$, pK = Fixed P.W. 8 μs Fixed ≈ 10% dc, $V_{CE} = 4V$ Fixed, $R_L = 22\,\Omega$, (Notes 1 and 2)		1		μs
R_{ISO}	Isolation Resistance	V = 500 V		10^{11}		Ω

Note 1: Test conditions: from t = 0 of I_F until I_C exceeds 1.0 mA

Note 2: Test conditions: from end of I_F until I_C decreases below 1.0 mA

Note 3: Specified as the point where the collector current transfer ratio is one-half that of the low frequency C.T.R. (100 Hz).

Note 4: JEDEC Registered Data.

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Dear Customer:

The QUIKLOOK™ COPS Chip Tester you have just received is the latest enhancement to the COPS Development System. This unit is designed with the customer in mind with regards to ease of use and reliability.

The users manual provided with this unit details complete set-up and checkout procedures as well as standard user information.

At the time of our first shipments, the Diagnostic module described in the manual is not available. It will be delivered to you in about three weeks. It is not required for normal operation of the QUIKLOOK tester. To ensure your receipt of this Diagnostic unit, fill out the attached form and return it to the Microcomputer Systems Service Center.

Before powering up the unit, install the switch key cap provided. Then please read the QUIKLOOK users manual for the necessary user directions.

NAME _____ DATE _____

COMPANY _____ ADDRESS _____

SERIAL NUMBER OF
QUIKLOOK TESTER _____ _____

Please send me one Diagnostic module once they become available.

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MANUAL CHANGE NOTICE #1

PUBLICATION NO. 420306199-001A

Chapter 4, Note 1 is incomplete in its coverage of modification to the COPS PDS Target Board (P/N 980305551-001). If the test conditions specified in the manual indicate that field modifications are required to the Target Board, the following changes are required:

1. Change resistor R2 to 1K ohm as specified in the manual.
2. ADD a new 10K ohm resistor to the Target. Connect this resistor between IC U19 pin 10 and +5VDC (at U19 pin 14).

All Target Boards shipped from the factory at Revision level F or above will have this correction completed. All earlier boards may require this change.

If additional assistance is required, please contact the Microcomputer Systems Service Center.