COMPUTE

the Club Of Microprocessor Programmers, Users, and Technical Experts

Georgia Marszalek, Editor • David Graves, Editor

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SC/MP KEYBOARD KIT!

National's new Keyboard Kit now gives SC/MP Kit users a low-cost input/output capability. This new kit replaces the Teletype* normally required by the SC/MP Kit and allows users to evaluate the SC/MP CPU and to develop a variety of application software.

The heart of SC/MP Keyboard Kit is a ROM firmware package (512 bytes) called SCMPKB. The SCMPKB ROM replaces the "Kit Bug" ROM originally supplied with the SC/MP Kit and allows the effective use of the hexadecimal keyboard, to execute programs, to examine or modify the contents of memory and the SC/MP registers, and to monitor program performance.

There is a hole pattern for additional integrated circuits on the SC/MP Kit PC card. By following the simple instructions in the SC/MP Keyboard Kit users manual, one can add buffers, decoders, drivers, multiplexers, etc. Simply replace the Kit Bug ROM (suppled in the SC/MP Kit) with the new SCMPKB ROM, connect the preassembled Keyboard cable connector to the kit card, and you are ready to go!

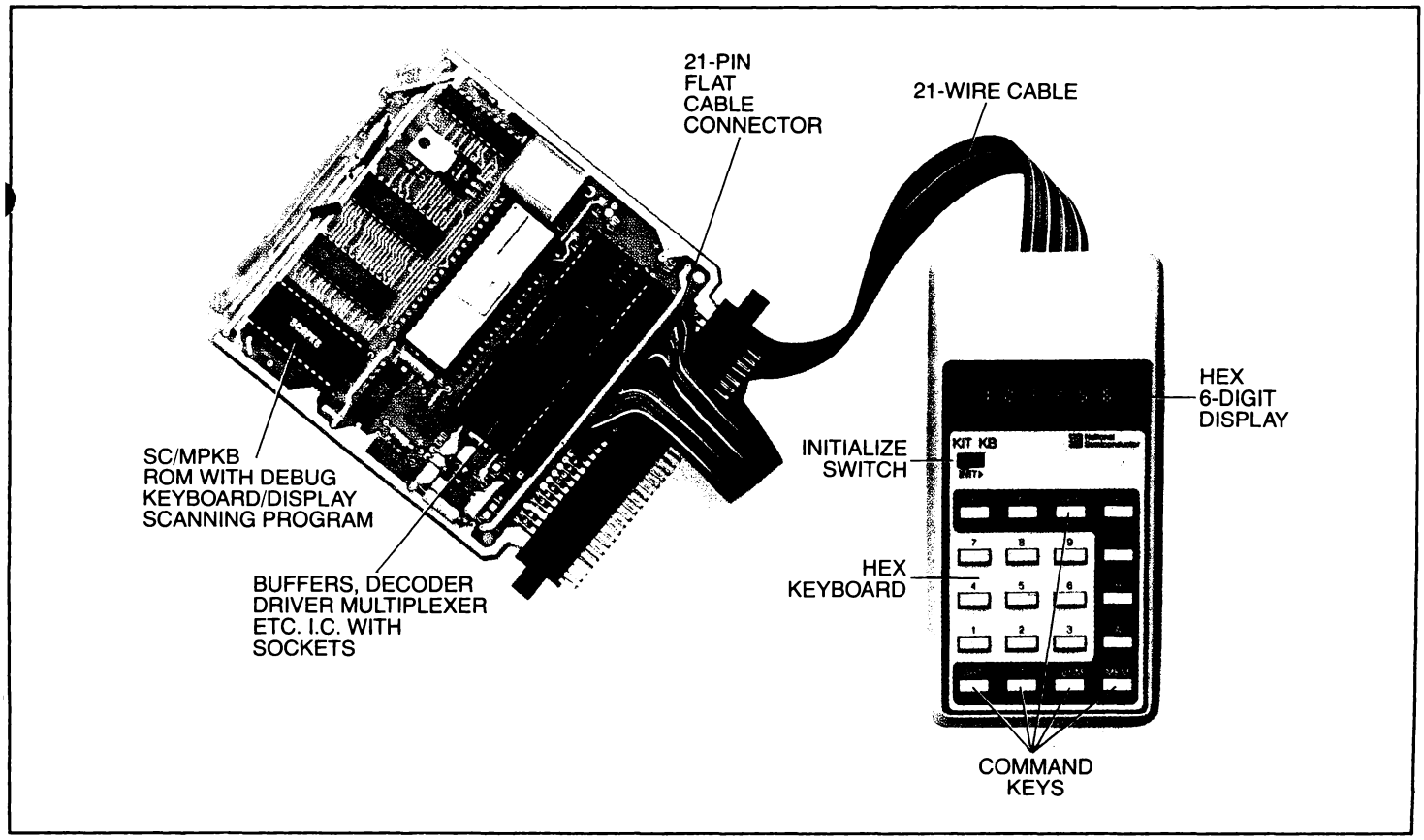
National's Keyboard Kit comes complete with manual, all required integrated circuits, resistors, keyboard display cable connector assembly, wire wrap connectors, precut wires—even a hand-held wire wrap tool.

This is a great kit for engineers and companies who don't have access to a Teletype. It is a low-cost teaching, learning, and developing tool for hobbyists, professors, students, and electronics entrepreneurs of all levels.

The Keyboard Kit is another step in the SC/MP tradition of simple, cost-effective solutions to your microprocessor needs.

To order your SC/MP Keyboard Kit: Call your local National Semiconductor distributor or sales representative. Ask for ISP-8K/400.

*A trademark of Teletype Corp.



MEMORIES . . . AT A GLANCE

The accompanying tables present a summary of National's wide range of semiconductor memory products. They show at a glance whether or not we supply a given memory type, its organization(s), and its production status.

The letters in the tables represent memory organizations, as shown in the legend below the tables. Letters without asterisks show memories that are in volume production. The asterisks indicate products yet to enter production, although some of these are already in the sampling phase.

A letter with an asterisk preceded by the same letter without an asterisk indicates that another version of the same device is to be put into production. The second version may differ from the first in speed, pin-out, number of leads, etc. Keep in mind, too, that a single letter entry in the tables may represent a number of product types differing, again, in speed, pin-out, number of leads, etc.

In addition to the memory products shown in the tables, National supplies shift registers, PLAS, character generators, code converters, etc. Full information and specifications for our complete line of memory products will be found in our *Memory Data Book* ($3.00); for information on asterisked products, contact your local National representative.

TOTAL BITS	RAMS			
	MOS (static)	MOS (dynamic)	CMOS	BIPOLAR
64			C	B,C
256	D		D,E	D
1024	G,I,I*		G,G*,I	G*
4096	P*,O*	O,O*		

TOTAL BITS	ROMS	
	MOS	BIPOLAR
256		F
1024	I,J	I
2048	M,N	M,N*
4096	P,P*,Q,Q*	Q
8192	R*,S	S
16,384	U*,V*	V,W

TOTAL BITS	PROMS/EPROMS	
	MOS	BIPOLAR
256		F
1024		I
2048	M,N	M,M*,N
4096	P,Q,Q*	P*,Q,Q*

Organization Codes

64 bits
A = 64 x 1
B = 32 x 2
C = 16 x 4

256 bits
D = 256 x 1
E = 64 x 4
F = 32 x 8

1024 bits
G = 1024 x 1
H = 512 x 2
I = 256 x 4
J = 128 x 8

2048 bits
K = 2048 x 1
L = 1024 x 2
M = 512 x 4
N = 256 x 8

4096 bits
O = 4096 x 1
P = 1024 x 4
Q = 512 x 8

8192 bits
R = 2048 x 4
S = 1024 x 8

16,384 bits
T = 16,384 x 1
U = 4096 x 4
V = 2048 x 8
W = 1024 x 16

TITLE-IMP-16 PAPER TAPE TITLING ROUTINE

TITLER converts as ASCII string of data to an eye readable paper tape format and outputs the result to the teletype. All printable ASCII characters except lower case alphabetic may be used. Illegal characters will be replaced by blanks on output. The string of ASCII characters may be packed either one or two characters per word, but must be terminated by a byte of zeroes in either case.

Memory Requirements:
Base sector—None
Top sector—X'F8 (248_{10}) words
Stack—4 + teletype output routine usage

Register and Flag Usage:
AC0, 1, 2, 3 and SEL Flag are used. Previous contents are destroyed.

Note: The program uses no scratch pad memory, so it may be used in either a RAM or ROM environment.

Contributed by Steve Shaiman,
Honeywell, Marine Systems Division,
Seattle, Washington.
Library program SL0030A
Listing—No Charge
Source Paper Tape $5.00

```
1 0000                  .TITLE IMP002, 'TITLER—PAPER TAPE
                        LABELING ROUTINE'
2 0000                  .ASECT
3 0000 0100 A           .=X'100
4 0100          ;
5 0100          ;
6 0100          ;       INPUTS: R2 = ADDRESS OF TITLE MESSAGE
7 0100          ;               R1 = 0 IF CHARACTERS ARE PACKED
                                     2/WORD
8 0100                               NON-ZERO IF CHARACTERS
                                     ARE PACKED 1/WORD
9 0100          ;
10 0100         ;
```

```
                ;       NOTES: TITLE MESSAGE MUST BE TERMINATED
                                BY A 0 BYTE ALL ILLEGAL CHARACTERS
                                WILL BE REPLACED BY BLANKS
                ;
                ;
4100 A TITLER:  PUSH  1         ;SAVE CHARACTER
                                 PACKING
4400 A NEXTWD:  PULL  0         ;R0 = CHARACTER
                                 PACKING
4000 A          PUSH  0         ;RETURN CHARACTER
                                 PACKING TO STACK
1504 A          BOC   5,ONLY1   ;BRANCH IF CHARACTERS
                                 1/WD
0A80 A          PFLG  2         ;CLEAR SEL FOR SHIFTING
8200 A          LD    0,(2)     ;R0 = CHARACTER WORD
5CF8 A          SHR   0,8       ;MOVE 1ST CHARACTER TO
                                 BITS 7-0
2906 A          JSR   CPUNCH    ;PUNCH CHARACTER ON
                                 TAPE
8200 A ONLY1:   LD    0,(2)     ;R0 = CHARACTER WORD
6126 A          AND   0,XFF     ;STRIP OFF BITS 15-8
2903 A          JSR   CPUNCH    ;OUTPUT CHARACTER IN
                                 BITS 7-0 TO TTY
4A01 A          AISZ  2,1       ;INCREMENT CHARACTER
                                 STRING POINTER
3081 A          NOP
21F3 A          JMP   NEXTWD
1116 A CPUNCH:  BOC   1,TITEND  ;BRANCH IF CHARACTER
                                 IS NULL (0)
E121 A          SKG   0,MINVAL  ;SKIP IF CHARACTER MAY
                                 BE VALID
2112 A          JMP   ILCHAR
E120 A          SKG   0,MAXVAL  ;DON'T SKIP IF CHARACTER
                                 IS VALID
2101 A          JMP   .+2
210F A          JMP   ILCHAR
8D1E A POINTC:  LD    3,PTABLE  ;R3 POINTS TO START OF
                                 CHAR GENERATOR
48E0 A          AISZ  0,-X'20   ;COMPUTE ADDRESS IN
                                 CHARACTER GENERATOR
3081 A          NOP             ;OF START OF CURRENT
                                 CHARACTER
3300 A          RADD  0,3       ;ADDRESS =
3000 A          RADD  0,0       ;PTABLE + (ASC11-X'20)*3)
3300 A          RADD  0,3
8300 A          LD    0,0(3)
290C A          JSF   PUT2C     ;OUTPUT 1ST 1/3 OF
                                 CHARACTER TO TTY
8301 A          LD    0,1(3)
290A A          JSR   PUT2C     ;OUTPUT 2ND 1/3 OF
                                 CHARACTER TO TTY
8302 A          LD    0,2(3)
2908 A          JSR   PUT2C     ;OUTPUT 3RD 1/3 OF
                                 CHARACTER TO TTY
4C00 A          LI    0,0
2906 A          JSR   PUT2C     ;OUTPUT NULL TO
                                 SEPERATE CHARACTERS
0200 A          RTS
4C20 A ILCHAR:  LI    0,X'20    ;REPLACE ILLEGAL
                                 CHARACTER WITH BLANK
21EF A          JMP   POINTC
4400 A TITEND:  PULL  0         ;PULL PARAMETER &
                                 INTERNAL RETURN OFF
4400 A          PULL  0         ;STACK
0200 A          RTS
3181 A PUT2C:   RCPY  0,1       ;R1 = 16 BITS FOR TTY
                                 OUTPUT
0A80 A          PFLG  2         ;CLEAR SEL FOR SHIFTING
5CF8 A          SHR   0,8       ;MOVE BITS 15-8 TO
                                 BITS 7-0
2D08 A          JSR   @PUTCP    ;OUTPUT BITS 15-8 TO TTY
3481 A          RCPY  1,0       ;R0 = 16 BITS FOR TTY
                                 OUTPUT
6102 A          AND   0,XFF     ;STRIP OFF BITS 15-8
2D05 A          JSR   @PUTCP    ;OUTPUT BITS 7-0 TO TTY
0200 A          RTS
                ;
00FF A XFF;     .WORD X'FF
001F A MINVAL:  .WORD X'1F      ;CHARACTER PRECEEDING
                                 1ST VALID ASCII
0060 A MAXVAL:  .WORD X'60      ;LAST VALID ASCII
                                 CHARACTER
0135 A PTABLE:  .WORD TABLE     ;ADDRESS OF START OF
                                 CHARACTER GENERATOR
7E59 A PUTCP:   .WORD X'7E59    ;ADDRESS OF PUTC
                .PAGE 'CHARACTER GENERATOR'
                ;
                ;
0000 A TABLE:   .WORD 00000,00000,00000 ;SPACE 20
0000 A
0000 A
0000 A          .WORD 00000,0DF00,00000 ;!          21
DF00 A
0000 A
0007 A          .WORD 00007,00000,00700 ;"          22
0000 A
0700 A
0014 A          .WORD 00014,03E14,03E14 ;#          23
3E14 A
3E14 A
444A A          .WORD 0444A,0FFFF,04A32 ;$          24
FFFF A
4A32 A
C323 A          .WORD 0C323,01008,06463 ;%          25
1008 A
6463 A
46A9 A          .WORD 046A9,091AA,044A0 ;&          26
91AA A
44A0 A
0004 A          .WORD 00004,00201,00000 ;'          27
0201 A
0000 A
0000 A          .WORD 00000,03C42,08100 ;(          28
3C42 A
8100 A
0081 A          .WORD 00081,0423C,00000 ;)          29
423C A
0000 A
002A A          .WORD 0002A,01C7F,01C2A ;*          2A
1C7F A
1C2A A
0808 A          .WORD 00808,03E08,00800 ;+          2B
3E08 A
0800 A
0080 A          .WORD 00080,04020,00000 ;,          2C
4020 A
0000 A
0808 A          .WORD 00808,00808,00800 ;-          2D
0808 A
0800 A
0000 A          .WORD 00000,0C0C0,00000 ;.          2E
C0C0 A
0000 A
8020 A          .WORD 08020,00804,00100 ;/          2F
0804 A
0100 A
7EA1 A          .WORD 07EA1,09189,0857E ;0          30
9189 A
857E A
8482 A          .WORD 08482,0FF80,08000 ;1          31
FF80 A
8000 A
C1A1 A          .WORD 0C1A1,09189,08186 ;2          32
9189 A
8186 A
8976 A
1814 A          .WORD 01814,012FF,01010 ;4          34
12FF A
1010 A
4F89 A          .WORD 04F89,08989,08971 ;5          35
8989 A
8971 A
7E91 A          .WORD 07E91,09191,09162 ;6          36
9191 A
9162 A
01C1 A          .WORD 001C1,02111,00907 ;7          37
2111 A
0907 A
7689 A          .WORD 07689,08989,08976 ;8          38
8989 A
8976 A
4689 A          .WORD 04689,08989,0897E ;9          39
8989 A
897E A
```

```
 98 0183 0000 A          .WORD 00000,06666,00000  ;:          3A
    0184 6666 A
    0185 0000 A
 99 0186 0040 A          .WORD 00040,06626,00000  ;;          3B
    0187 6626 A
    0188 0000 A
100 0189 0010 A          .WORD 00010,02844,08200  ;<          3C
    018A 2844 A
    018B 8200 A
101 018C 0028 A          .WORD 00028,02828,02800  ;=          3D
    018D 2828 A
    018E 2800 A
102 018F 0082 A          .WORD 00082,04428,01000  ;>          3E
    0190 4428 A
    0191 1000 A
103 0192 B109 A          .WORD 0B109,00909,00600  ;?          3F
    0193 0909 A
    0194 0600 A
104 0195 3C42 A          .WORD 03C42,05A5A,0520C  ;@          4D
    0196 5A5A A
    0197 520C A
105 0198 FC0A A          .WORD 0FC0A,00909,00AFC  ;A          41
    0199 0909 A
    019A 0AFC A
106 019B FF89 A          .WORD 0FF89,08989,08976  ;B          42
    019C 8989 A
    019D 8976 A
107 019E 7381 A          .WORD 07E81,08181,08142  ;C          43
    019F 8181 A
    01A0 8142 A
108 01A1 FF81 A          .WORD 0FF81,08181,0817E  ;D          44
    01A2 8181 A
    01A3 817E A
109 01A4 FF89 A          .WORD 0FF89,08989,08981  ;E          45
    01A5 8989 A
    01A6 8981 A
110 01A7 FF09 A          .WORD 0FF09,00909,00901  ;F          46
    01AB 0909 A
    01A9 0901 A
111 01AA 7E81 A          .WORD 07E81,081A1,0A162  ;G          47
    01AB 81A1 A
    01AC A162 A
112 01AD FF08 A          .WORD 0FF08,00808,008FF  ;H          48
    01AE 0808 A
    01AF 08FF A
113 01B0 0081 A          .WORD 00081,0FF81,0000   ;I          49
    01B1 FF81 A
    01B2 0000 A
114 01B3 4081 A          .WORD 04081,0817F,00101  ;J          4A
    01B4 817F A
    01B5 0101 A
115 01B6 FF08 A          .WORD 0FF08,01824,04281  ;K          4B
    01B7 1824 A
    01B8 4281 A
116 01B9 FF80 A          .WORD 0FF80,08080,08080  ;L          4C
    01BA 8080 A
    01BB 8080 A
117 01BC FF04 A          .WORD 0FF04,00808,004FF  ;M          4D
    01BD 0808 A
    01BE 04FF A
118 01BF FF06 A          .WORD 0FF06,00810,060FF  ;N          4E
    01C0 0810 A
    01C1 60FF A
119 01C2 7E81 A          .WORD 07E81,08181,0817E  ;O          4F
    01C3 8181 A
    01C4 817E A
120 01C5 FF09 A          .WORD 0FF09,00909,00906  ;P          50
    01C6 0909 A
    01C7 0906 A
121 01C8 7EB1 A          .WORD 07E81,081A1,0C1FE  ;Q          51
    01C9 81A1 A
    01CA C1FE A
122 01CB FF19 A          .WORD 0FF19,00929,04986  ;R          52
    01CC 0929 A
    01CD 4986 A
123 01CE 4689 A          .WORD 04689,08989,08972  ;S          53
    01CF 8989 A
    01D0 8972 A
124 01D1 0001 A          .WORD 00001,001FF,00101  ;T          54
    01D2 01FF A
    01D3 0101 A
125 01D4 7F80 A          .WORD 07F80,00080,0807F  ;U          55
    01D5 0080 A
    01D6 807F A
126 01D7 3F40 A          .WORD 03F40,08080,0403F  ;V          56
    01D8 8080 A
    01D9 403F A
127 01DA FF40 A          .WORD 0FF40,02020,040FF  ;W          57
    01DB 2020 A
    01DC 40FF A
128 01DD C324 A          .WORD 0C324,01818,024C3  ;X          58
    01DE 1818 A
    01DF 24C3 A
129 01E0 0001 A          .WORD 00001,002FC,00201  ;Y          59
    01E1 02FC A
    01E2 0201 A
130 01E3 C1A1 A          .WORD 0C1A1,09189,08583  ;Z          5A
    01E4 9189 A
    01E5 8583 A
131 01E6 0000 A          .WORD 00000,0FF81,08100  ;[          5B
    01E7 FF81 A
    01E8 8100 A
132 01E9 0104 A          .WORD 00104,00820,08000  ;\          5C
    01EA 0820 A
    01EB 8000 A
133 01EC 0081 A          .WORD 00081,081FF,00000  ;]          5D
    01ED 81FF A
    01EE 0000 A
134 01EF 0402 A          .WORD 00402,07F02,00400  ;↑          5E
    01F0 7F02 A
    01F1 0400 A
135 01F2 2070 A          .WORD 02070,0A820,02020  ;←          5F
    01F3 A820 A
    01F4 2020 A
136 01F5 0000 A          .WORD 00000,00102,00400  ;'          60
    01F6 0102 A
    01F7 0400 A
137 01F8                 .END
```

PROGRAMMING TIDBITS:

SOFTWARE STACK ROUTINE PACE MICROPROCESSOR

If the pace 10 word on-chip stack is not enough for your application, there is a software stack routine published in the PACE Users Manual (IPC-16P/968 pub. no. 4200068) Pages 3–35.

PROM SOCKETS

Need additional prom sockets for your programs (or RAMDUMP or DEBUGC)? If you don't have a card reader with your prototyping system, you can remove the ROMs at addresses and 7F00 through 7FFF and use these sockets for your own PROM'S or ROM's.

Microprocessor Service Center

Please use this address for return or repair of microprocessor hardware.

NATIONAL SEMICONDUCTOR
2921 COPPER ROAD
SANTA CLARA, CA. 95035
ATTN: MICROPROCESSOR SERVICE CENTER

the Bit·Bucket

Dear Georgia,

I just received the June, 1976, *COMPUTE*. The information on PACE interrupts was very interesting, as was the program NUMPRG on page 5. This program will not function properly if the CARRY flip flop happens to be set when the program is invoked. The problem, which results from the fact that "DECA" means Decimal Add with Carry, can be corrected by adding a "PFLG 7" instruction at the beginning of the program. Since the "PFLG 8" instruction at the end of the program isn't really necessary, the subroutine can still be made to fit in 48 words. It is very slow for numbers of large magnitude, though, taking 1.32 seconds to convert X'7FFF, whereas my version takes 2.25 milliseconds. NUMPRG is very clever, none the less.

Sincerely,
James Gaudreault
7909 14th Ave. 102
Hyattsville, Md. 20783

Attn: Georgia Marszalek,

I have had more than six months of concentrated IMP-16 programming experience with your IMP16P development system with floppy disc and high speed printer. Please include my name and company with your list of consultants as published in COMPUTE.

Keep up the good work and thanks.

Very truly yours,
Paul F. Fitts
Dir Sys Dev
Innovatek Microsystems Inc.
Smithfield Road
Mullerton, New York 12546

Dear Georgia:

I'm pleased to see that you're reprinting Hal Chamberlin's articles on his IMP-16 system. I've been following this series, as it has appeared in The Computer Hobbyist, with great interest, and am getting together the components to construct the system. I hope eventually to have a system somewhat comparable to the one outlined by Dean Lapham in Bit-Bucket, Vol. 1, No. 3, and Hal's system seems just about ideal for this.

I did note a few errors, though, in your reprinting of Part 2. They're fairly obvious, but I'll point them out anyway:

In Figure 3, the 8223 ROM "CPU-2" should be programmed 00101000 at Address 20.

In Figure 4, the programming of CPU-2 at time state 19 should be 00100010, and at time state 20 00101000. ROM address at time state 23 should be 2.

In Figure 5, the line labeled $\overline{\text{LOC RESET}}$ should be BUS CLOCK, and should connect to PUNIBUS line 27. The line you have labeled BUS CLOCK was $\overline{\text{LOC RESET}}$ in the original TCH version of Figure 5. However, I wonder if this was correct. If I understand the reset logic correctly, when you have power up, the $\overline{\text{PWR OK}}$ line goes low, this should put the output of the first 7413 high, and this, after delay in the RC network, outputs a logic zero from the second 7413. Inversion of this by a 7404 then should put the line in question high, i.e., LOC RESET. Likewise, it looks as though PUNIBUS line 33 comes out active high, or BUS RESET, while the line labelled LOC RESET is active low.

Figures 3 and 4 in the TCH version were relabelled 5 and 6 respectively in your reprinting, and vice versa. However, text references to these figures were not changed accordingly.

Very truly yours,
Norman F. Stanley
P.O. Box 723
Rockland, Maine 04841

LOW-COST DEVELOPMENT SYSTEM FOR SC/MP MICROPROCESSOR!

The SC/MP Low-Cost Development System (LCDS) is a simple-to-use controller that provides a maximum of flexibility at a minimum—and very affordable—cost. It has everything needed to develop and test SC/MP hardware and software designs for your applications.

LCDS features easy interfacing and expansion. Four prewired edge connectors, for example, provide a plug-in interface for SC/MP family cards, and also let you interconnect additional SC/MP applications hardware. (There's room for a fifth connector, too, if you wish to add it.) You can also add a flat cable connector for coupling the LCDS to an external card cage.

Built-in control and monitor functions permit transfer of control between the LCDS resident firmware—subroutines that let you enter software debug commands via the control and display panel, or an optional Teletype® —and your own application programs.

Expansion is easy, too, because of the cards offered for use with the LCDS. The 2K × 8 read/write memory and 4K × 8 ROM/PROM cards, for example, provide additional memory: just plug them into the card bus.

The minimum LCDS comprises a SC/MP CPU card, scratchpad memory, ROM-based firmware, and control logic. Also included are a 16-key dual-function hexidecimal keyboard, all necessary function keys and control switches, and a six-digit hexadecimal display.

With the basic LCDS configuration alone, you can examine and alter the SC/MP programs in continuous or single instruction mode, and even operate with an optional Teletype using SC/MP DEBUG.

LCDS Brochures are available from Marketing Services.

NATIONAL SEMICONDUCTOR
Attn: Marketing Services
2900 Semiconductor Drive
Santa Clara, CA 95051

The LCDS Part Number is ISP-8P/301
Price $499.00

Loading CASM on the Disc

CASM can be loaded on the IMP-16 disc by using the DISC LOADER with the following commands. When loading the tape the tape reader will stop with a Sequence error at the point where the first part of CASM stops and the second part begins, to continue loading push the RUN button on the control panel. One thing to remember is that CASM does not include any Disc I/O routines so that the source and object programs cannot be written to or read from the Disc with the DI and DO commands found in the Disc version of EDITING and IMPASM.

```
DISC LOADER (REV. E)
READY.←Load IMP-16 Disc Loader.
!LM(CR) ←Request Load Map.
!MP 0E7(CR)←Specify to which sector
            CASM is to be written.
!OTS0(CR)  }
           } Specify origin of Base
!OBS0(CR)  } and Top Sectors
!RLM(CR)←Load CASM PT from TTY
         or high-speed tape reader.
CEDT16  P00642A  2/21/75
SEQ     1AA6     78B5
BS = 0000:00FE   TS = 0000:0000
AS = 01EC:15C1   ENT = OFB0   Load map information.
!GO 0FB0(CR)←Write CASM to DISC with entry point 0FB0.
BS = 0000:00FE   TS = 0000:0000
AS = 01EC:15C1   PTR = 0100:0100
ENT = 0FB0
PGM WRITTEN TO SECTORS 00E7:00FB
!XEC 0E7(CR)←Execute CASM from DISC.
NSC CONVERSATIONAL ASSEMBLER 1/2/75
? KB(CR)
  •
  •
  •
```

Underlining indicates commands typed by user.
(CR) indicates carriage return.

SC/MP PRICES

SC/MP CHIP PARTS ID. NO.	DESCRIPTION	PRICE 1–24	PRICE 25 UP
ISP-8A/500D	SC/MP CPU Chip	$ 17.76	$ 16.50

SC/MP APPLICATION CARDS PARTS ID. NO.	DESCRIPTION	PRICE 1–9	PRICE 10 UP
ISP-8C/002	SC/MP Application RAM Card (2K x 8)	$160.00	$152.00
ISP-8C/004B	SC/MP Application ROM/PROM Card (4K x 9) (With sockets for eight MM5204/5214's)	125.00	119.00
ISP-8C/004P	SC/MP Application ROM/PROM Card (4K x 8) (With eight MM5204Q's supplied)	525.00	499.00
ISP-8C/100	SC/MP Application CPU Card (Includes 256 x 8 RAM & sockets for 512 x 8 of ROM/PROM)	250.00	238.00
ISP-8C/100R	SC/MP Application CPU Card (Includes 256 x 8 RAM & hole pattern for 1 or 2K by 8 of ROM/PROM	255.00	243.00

SC/MP KIT & DEVELOPMENT SYSTEM PARTS ID. NO.	DESCRIPTION	PRICE 1–24	PRICE 25 UP
ISP-8K/200	SC/MP Kit	$ 99.00	$ 95.00
ISP-8P/301	SC/MP LCDS (Low Cost Development System)	499.00	N/A

SC/MP CROSS ASSEMBLER SOFTWARE PACKAGES PARTS ID. NO.	DESCRIPTION	PRICE 1–24	PRICE 25 UP
ISP-8S/100C	SC/MP 4K (IMP-16 based) Package (object paper tapes and listings)	$150.00	N/A
ISP-8S/100Q	SC/MP 4K (IMP-16 based) Package (object punched cards and listings)	150.00	N/A
ISP-8S/101C	SC/MP 8K (IMP-16 based) Package (object paper tapes and listings)	150.00	N/A
ISP-8S/101Q	SC/MP 8K (IMP-16 based) Package (object punched cards and listings)	150.00	N/A
ISP-8S/102P	SC/MP (ANS FORTRAN) Package (Source punched cards and listings)	495.00	N/A

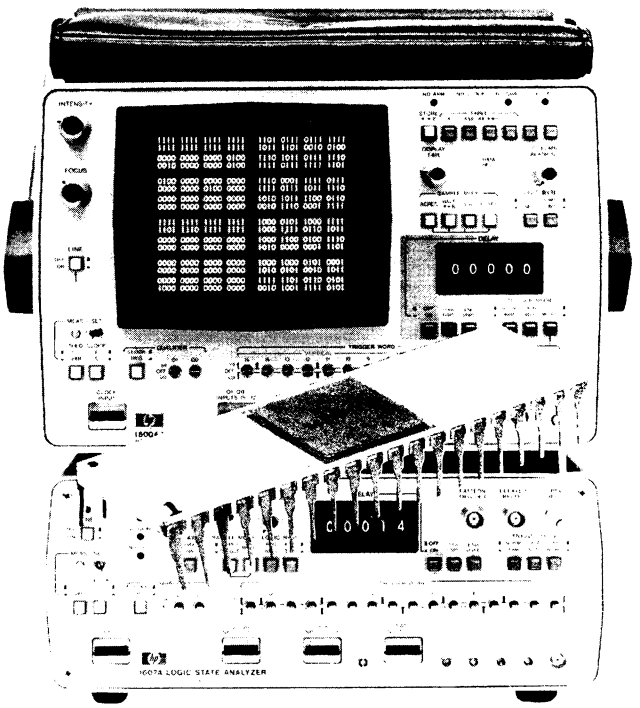
SC/MP MANUALS PARTS ID. NO.	DESCRIPTION	PRICE	PRICE
ISP-8S/994Y	SC/MP Assembly Language Programming Manual	$ 10.00	N/A

N8080 PRICES

PARTS ID NO.	DESCRIPTION	PRICE 1–9	PRICE 10–24	PRICE 25–99	PRICE 100 UP
INS8080AD	8-BIT CENTRAL PROCESSING UNIT (2 μs)	$35.00	$29.00	$24.50	$19.95

APPLICATION NOTE 167-18
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of National Semiconductor SC/MP microprocessor system.



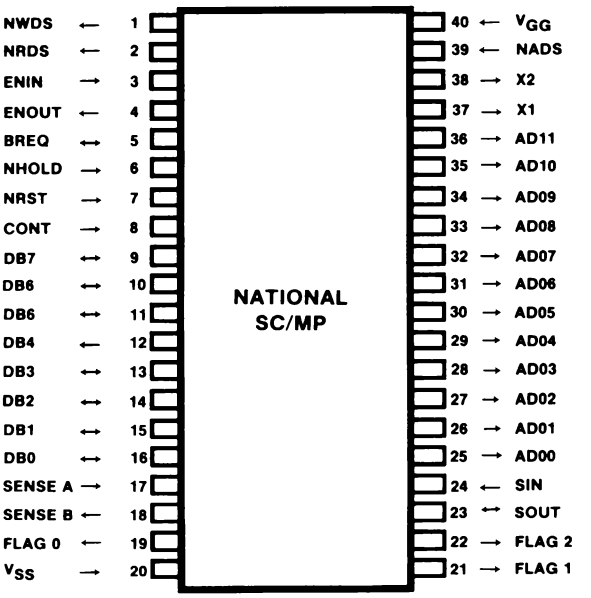
HEWLETT hp PACKARD

1. INTRODUCTION

This application note is designed to assist the user of the National Semiconductor SC/MP microprocessor in the real time analysis of his system in both design and troubleshooting environments. The note demonstrates real time analysis of actual program sequences, triggering on specific events, use of the map, paging technique, and observation of information flow on the data bus.

The SC/MP is a single-chip microprocessor packaged in a 40-pin DIP package and intended for use in general-purpose applications. The chip has self-contained timing circuits (frequency is set with an external crystal or capacitor), 16-bit addressing capability, and serial and parallel data transfer capability. The Central Processing Unit (CPU) contains an 8-bit data bus and a 12-bit address bus as well as three pointer registers capable of automatic incrementing or decrementing. The architecture makes possible a very low-cost system including internal I/O ports and compatability with most standard TTL/CMOS components.

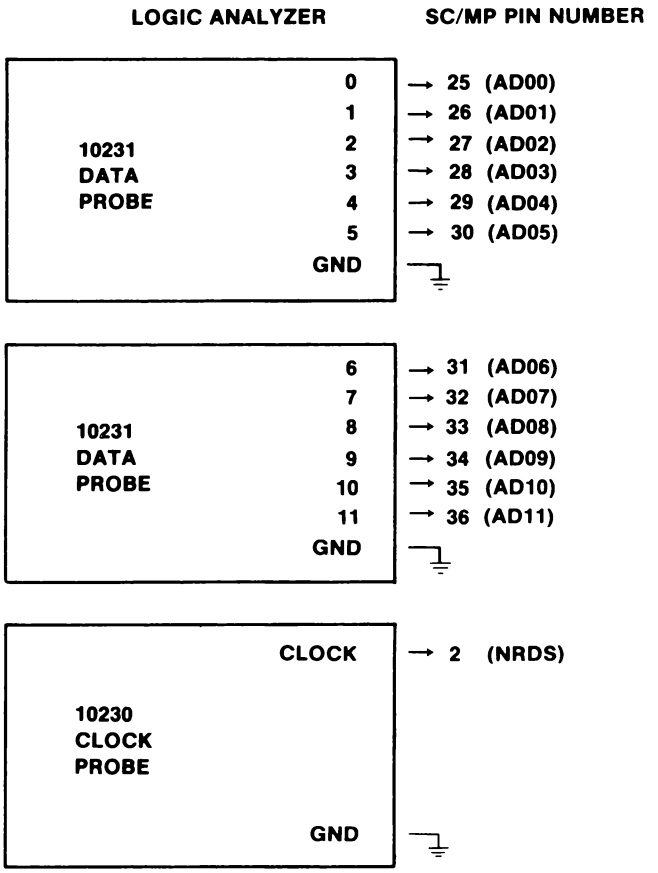
2. PIN ASSIGNMENTS



PIN NAME	FUNCTION
DB0-DB7	Data Bus
AD00-AD11	Address Bus
FLAG 0-FLAG 2	User Assigned, General-purpose Bit
X1, X2	To Ext Timing Xtal/Cap
NWDS	Write Strobe Output
NRDS	Read Strobe Output
ENIN	Enable Input
ENOUT	Enable Output
BREQ	Bus Request Input/Output
NHOLD	Hold Lengthens Input/Output Cycle
NRST	Reset Input
CONT	Continue Input
SENSE A-SENSE B	General Purpose Status Inputs
NADS	Address Strobe Output
SIN	Serial Input
SOUT	Serial Output
V_{SS}	Positive Supply Voltage
V_{GG}	Negative Supply Voltage

3. PROBE CONNECTIONS

A system that will not "come up" can frequently be debugged by monitoring address flow alone. With the SC/MP, the following Logic State Analyzer Probe connections will display activity on the SC/MP Address Bus.



4. SETTING THE CONTROLS

Turn power on to the Logic State Analyzer and set controls as follows:

Display Mode	Table A
Sample Mode	SGL
Start Display	ON
Trigger Mode	WORD
Threshold	TTL
Clock	⌐¯
All other pushbuttons	Out Position
Display Time	ccw
Column Blanking	Display 12 bits
Qualifiers	OFF
Trigger Word Switches	Set to Address at which you wish to trigger*

*If program is not looping or cycling through the selected address, press RESET and start your system. The first time the system passes through the selected trigger state, the display will be generated and stored.

5. DISPLAY INTERPRETATION

Figure 1 shows the display of information on the address bus (A) and the program from which it was derived (B). This figure will help you understand the Logic State Analyzer display. Your own program will do equally well. Proper system program operation is verified by a comparison of the table display with the program listing.

The entire program can be viewed in 16 word "Pages" by resetting the trigger word switches to correspond to the last (16th) word in each successive display. This paging technique can also be accomplished by using the Digital Delay thumbwheel switches advanced in increments of 16.

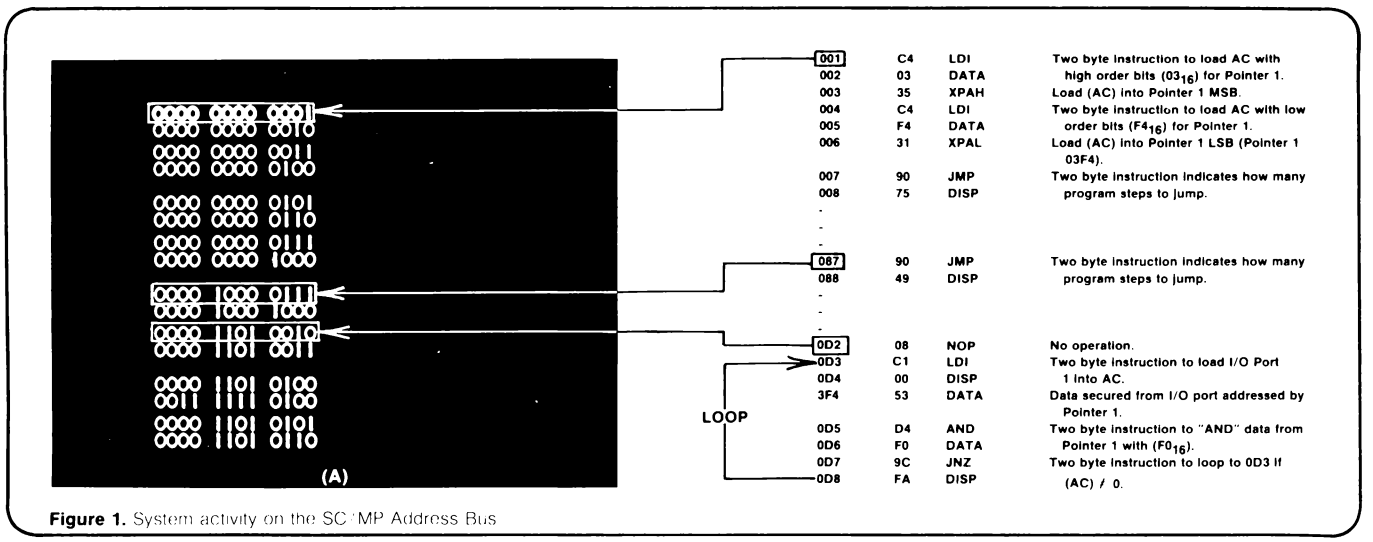


Figure 1. System activity on the SC/MP Address Bus

6. THE MAP

If a tabular display is not presented in the previous step, it means that the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program, switch to "map" (figure 2). The Logic State Analyzer trigger word switches are now operating in their cursor positioning mode. Use the trigger word switches to position the cursor (circle) over one of the dots on

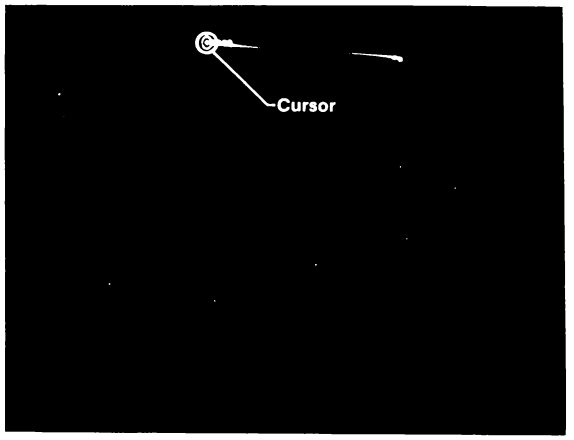


Figure 2. Map Display Shows Entire System Activity.

screen. Switch to MAP EXPAND and make the final positioning. The no trigger light will now go out and pressing Table A pushbutton will display the 16 address words beginning at the point located with the cursor.

7. VIEWING ADDRESS AND DATA LINES

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data Bus or in peripheral memory. Additional input channels now become very desirable. By combining the 1600A and the 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the full 16 bits of address, 8 bits of data, and eight other active lines to be viewed simultaneously. Connect the instrument as follows:

1. Connect the data cable between rear-panel connectors.
2. Connect trigger bus cable between instrument front panel bus connectors.
3. Select Trigger mode "WORD" on 1600A.
4. Select "BUS" and "OFF" on the 1607A.
5. Select "Start Display", SAMPLE MODE "Single" on both Analyzers, and TABLE "A&B" on the 1600A.
6. Set Threshold and Logic Polarity on 1607A to be the same as the 1600A.
7. Leave all other pushbuttons "out" on 1607A.
8. Leave the 1600A set up as in Section 3.
9. Connect data and clock inputs for 1607A to the SC/MP as follows:
   a. Data inputs on 1607A 0 through 7 to SC/MP DB0 through DB7 respectively.
   b. Clock input to SC/MP pin 2.
   c. Grounds to appropriate point(s).
10. Press "Reset" on both Logic State Analyzers and restart system.
11. Set Column Blanking on 1607A to display 8 columns.

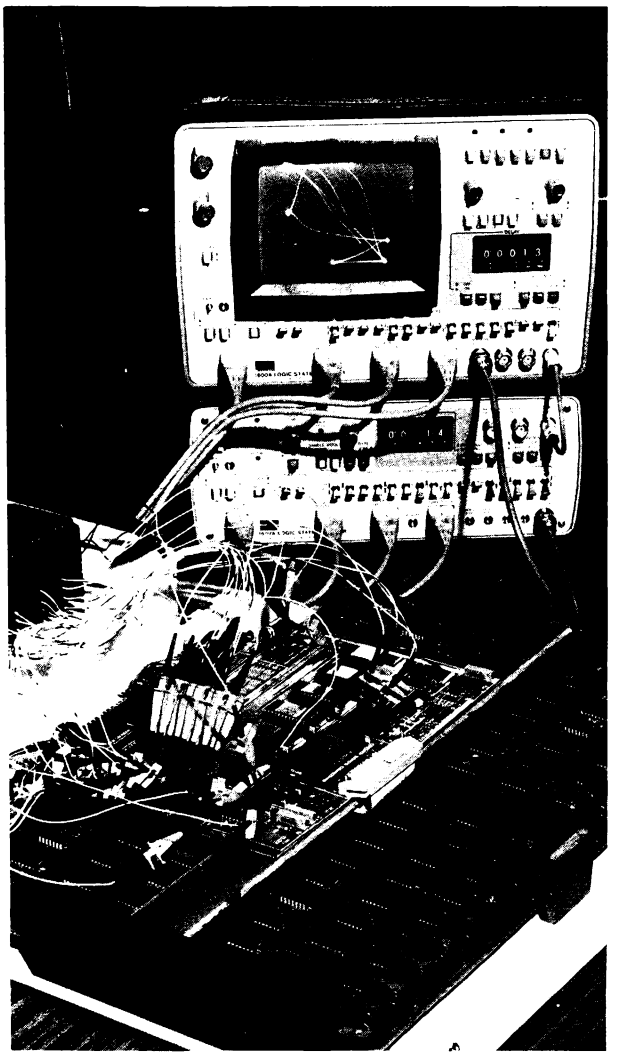


Figure 3. Typical Test Setup of 1600A and 1607A for Displaying up to 32 Bits of Information

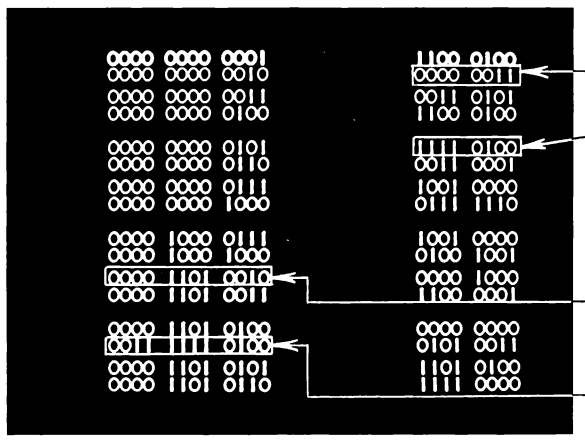
8. DISPLAY INTERPRETATION OF ADDRESS AND DATA BUSES

Operating the Logic State Analyzer system as set up in section seven, the display shows all the activity on the address and data buses during system operation. Even though there is a 16-bit address register in the SC/MP, the output is not latched in our test system and the display shows only what is on the 12-bit address bus.

Figure 4A is the Logic State Analyzer display of address and data activity in the SC/MP while operating from the program listed in figure 4B. The first six program steps load an 8-bit address into Pointer 1 for use later in the program. At program step 008 and 088, the program calls for a jump to address 0D2, and by examining the display you can see these jump instructions being executed. The next portion of the program loads data from I/O Port 1 into the accumulator. Pointer 1 addresses I/O Port 1 and it is here that the address 03F4 from earlier steps is used. The display shows that each of these program steps is completed accurately. Similiar analysis will show the implementation of each instruction in the program.

9. CONCLUSION

From the foregoing examples, it may be concluded that efficient troubleshooting of National Semiconductor SC/MP μP systems is expedited by two factors. First: availability of the program listing, the definitive document of program execution; and Second: the availability of real time Logic State Analysis to display system operation in terms of actual logic bits for rapid error detection and correction.



(A)

001	C4	LDI	Two byte instruction to load AC with high order bits (03_{16}) for Pointer 1.
002	03	DATA	
003	35	XPAH	Load (AC) into Pointer 1 MSB.
004	C4	LDI	Two byte instruction to load AC with low order bits ($F4_{16}$) for Pointer 1.
005	F4	DATA	
006	31	XPAL	Load (AC) into Pointer 1 LSB (Pointer 1 = 03F4).
007	90	JMP	Two byte instruction indicates how many program steps to jump.
008	7E	DISP	
087	90	JMP	Two byte instruction indicates how many program steps to jump.
088	49	DISP	
0D2	08	NOP	No operation.
0D3	C1	LD	Two byte instruction to load I/O Port 1 into AC.
0D4	00	DISP	
3F4	53	DATA	Data secured from I/O port addressed by Pointer 1.
0D5	D4	ANI	Two byte instruction to "AND" data from Pointer 1 with ($F0_{16}$).
0D6	F0	DATA	
0D7	9C	JNZ	Two byte instruction to loop to 0D3 if (AC) ≠ 0.
0D8	FA	DISP	

(B)

Figure 4. Display Showing Address and Data Bus Activity.

Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Calls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A)
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
167-8 Stable Displays of Disc System Waveforms Synchronized to Record Address (1620A)
167-9 Functional Analysis of Motorola M6800 Microprocessor Systems (1600A and 1607A).
167-10 Using the 1620A for Serial Pattern Recognition (1620A).
167-11 Functional Analysis of Intel 8008 Microprocessor Systems (1600A and 1607A).
167-12 Functional Analysis of Fairchild F8 Microprocessor Systems (1600A and 1607A).
167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A).
167-14 Functional Analysis of 8080 Microprocessor Systems (1600A and 1607A).
167-15 Functional Analysis of Intel 4004 Microprocessor Systems (1600A and 1607A).
167-16 Functional Analysis of Intel 4040 Microprocessor Systems (1600A and 1607A).
167-17 Functional Analysis of National IMP Microprocessor Systems (1600A and 1607A).

VIDEO TAPE SERIES: This four hour series titled "The Data Domain Its Analysis and Measurements" introduces logic state analysis and measurement techniques unique to the data domain. Contact your HP Field Engineer for price and availability of this color tape series.

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BINARY-TO-BCD CONVERSION PROGRAM

by Barry Cloud
Bower Industries
P.O. Box 1631
Orange, CA 92668

This program is designed to convert a binary number to a BCD format and output it on a teletype. The basis of the Program is a simple algorithm for binary to decimal conversion. The algorithm is as follows:

1. Find the highest order 'one' bit and set the 'accumulator' to one.
2. Shift to the next lowest order bit and double the accumulator.
3. If this bit is a 'zero' return to step 2. If it is a 'one' then add one to the accumulator and return to step 2.
4. Repeat steps 2 and 3 until each bit of the number has been processed. The 'accumulator' now contains the decimal representation of the binary number.

The program was tested on a PACE Development System and is written in two parts—conversion and TTY output. The output portion, which begins at lable TTY:, may be removed without impairing the execution of the conversion portion. In this case the BCD result would be found in AC0.

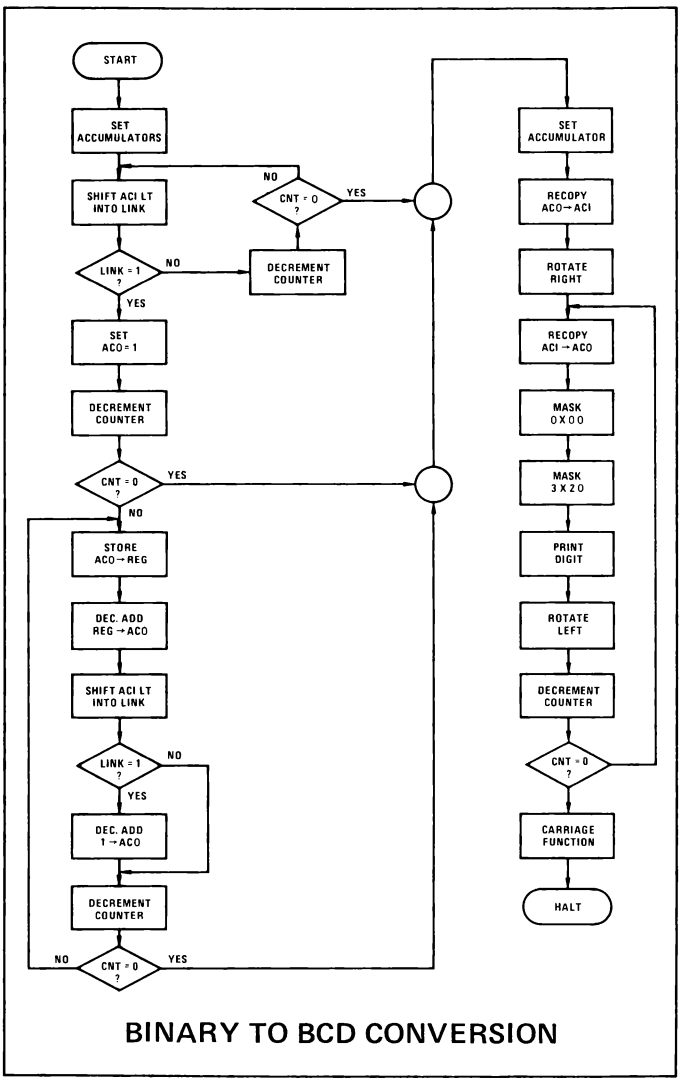
It is assumed that the main program has already loaded the number to be converted into AC1 and has cleared the remaining accumulators.

Even though the conversion algorithm is functional for any size binary number, this program restricts the magnitude to 9999 (decimal) due to accumulator overflow. Note that nowhere in the program is this limitation enforced.

The program listing and flowchart are shown below.

```
;MAX NUMBER IS 9999 DECIMAL
;AC0—ADDITION & OUTPUT REG
;AC1—NUM TO BE CONVERTED &
       OUTPUT SHIFTING
;AC2—DOWN COUNTERS

        .TITLE  BINBCD
CONV:   LI      0,0         ;LD AC0=0
        LI      2,16        ;LD AC2=16
SEEK:   SHL     1,1,1       ;SHIFT LEFT 1
        BOC     8,YES       ;TEST LINK=1
        AISZ    2,-1        ;DECR COUNTER
        JMP     SEEK        ;NOT ZERO
        JMP     TTY         ;ZERO
YES:    LI      0,1         ;LD AC0=1
        AISZ    2,-1        ;DECR COUNTER
        JMP     NEXT        ;NOT ZERO
        JMP     TTY         ;ZERO
NEXT:   ST      0,REG       ;SET REG=AC0
        SHL     1,1,1       ;SHIFT LEFT 1
        DECA    0,REG       ;DECIMAL ADD
        BOC     8,ADD       ;TEST LINK=1
DECR:   AISZ    2,-1        ;DECR COUNTER
        JMP     NEXT        ;NOT ZERO
        JMP     TTY         ;ZERO
ADD:    DECA    0,ONE       ;DECIMAL ADD 1
        JMP     DECR
TTY:    LI      2,4         ;SET AC2=4
        RCPY    0,1         ;COPY AC0 TO AC1
        ROR     1,4,0       ;ROTATE RT 4
ATTY:   RCPY    1,0         ;COPY AC1 TO AC0
        AND     0,MASK      AC0=0X00
        ADD     0,THIRTY    ;AC0=3X20
        JSR     @PUT2C      ;OUTPUT TO TTY
        ROL     1,4,0       ;ROTATE LT 4
        AISZ    2,-1        ;DECR COUNTER
        JMP     ATTY
        LD      0,FINISH    ;AC0=0D0A
        JSR     @PUT2C      ;OUTPUT TO TTY
        HALT
REG:    .WORD   0
ONE:    .WORD   X'0001
MASK:   .WORD   X'0F00
THIRTY: .WORD   X'3020
PUT2C:  .WORD   X'7EC1
FINISH: .WORD   X'0D0A
        .END    CONV
```



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☐ PACER ☐ SCAMPER

Program Title

Function

Required Hardware

Required Software

Input Parameters

Output Results

(use additional sheets if necessary)

Registers Modified: _____

Assembler/Compiler Used: _____

RAM Required: _____

Programmer: _____

ROM Required: _____

Company: _____

Date Submitted: _____

Address: _____

Maximum Subroutine Nesting Level: _____

Phone: _____

1. Complete Submittal Form as follows:

   a. Processor (check appropriate box)
   b. Program title: Name or brief description of program function
   c. Function: description of operations performed by the program
   d. Required hardware/firmware/software
      For example: TTY
      High Speed Printer
      Arithmetic CROM
      POWR I/O CROM
      EXTENDED CROM
      TTY routines
      Floating point package
      Support software required for cross products
   e. Input parameters: Description of register values, memory areas or values accepted from input ports
   f. Output results: Values to be expected in registers, memory areas or on output ports
   g. Program details
      1. Registers modified
      2. RAM required (bytes)
      3. ROM required (bytes)
      4. Maximum subroutine nexting level
   h. Assembler/Compiler used
      For example: SM/PL
      IMPASM, PASM
      PACE CROSS ASSEMBLER
      SC/MP CROSS ASSEMBLER
   i. Programmer and company

2. A source listing of the program and paper tape should be included

3. A test program which assures the validity of the contributed program is useful to include for user. This is for the user's verification:

   Each library program submitted entitles you or one of your colleagues to a free membership.

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