NEC Electronics Inc.

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ADVANCE PRODUCT INFORMATION

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μPD72120

Advanced Graphics Display Controller

User's Manual

Preliminary Product Information

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Section 1

Overview

The uPD72120 Advanced Graphic Display Controller (AGDC) displays characters and graphics on a raster scan CRT according to commands and parameters received from a host processor or CPU. It has high speed graphic drawing capabilities, video timing signal generation, large capacity display memory control (including Video RAMs) and a versatile CPU interface. These are some of the features that allow the AGDC to control graphics drawing and display of bit mapped systems.

Features

* High speed graphics drawing functions
  - ° Graphics drawing
    Dot, straight line, rectangle, circle, arc, sector, ellipse, ellipse arc and ellipse sector
    Maximum drawing speed: 500 ns/pixel (8 MHz, pixel mode)
    500 ns/dot (8 MHz, plane mode)
  - ° Painting (High speed processing in word units)
    Non-arbitrary enclosed area painting (Fill): triangle, trapezoid and circle.
    Arbitrary enclosed area painting (Paint): boundary dot retrieval
  - ° Data transfers in display memory
    Multiplane transfers
    Data transformation (90°/180°/270° rotation and reversal)
    Transfer speed: 500 ns/word max.
  - ° Image Processing
    Slant, arbitrary angle rotation, 16/N enlargement, N/16 shrinkage (N any integer from 1 to 16)
  - ° Position specification by X-Y coordinates
  - ° Logic operations between planes
* Video timing signal generation
  - ° High speed processing by two system clocks: display (for video sync signal generator) and graphics drawing clocks
  - ° External synchronization
* Large capacity display memory control
  - ° Display memory bus interface (24-bit address and 16-bit data bus for addressing up to 16 Mwords, 16 bits/word)
  - ° Video RAM (VRAM) control
  - ° Display memory bus arbitration

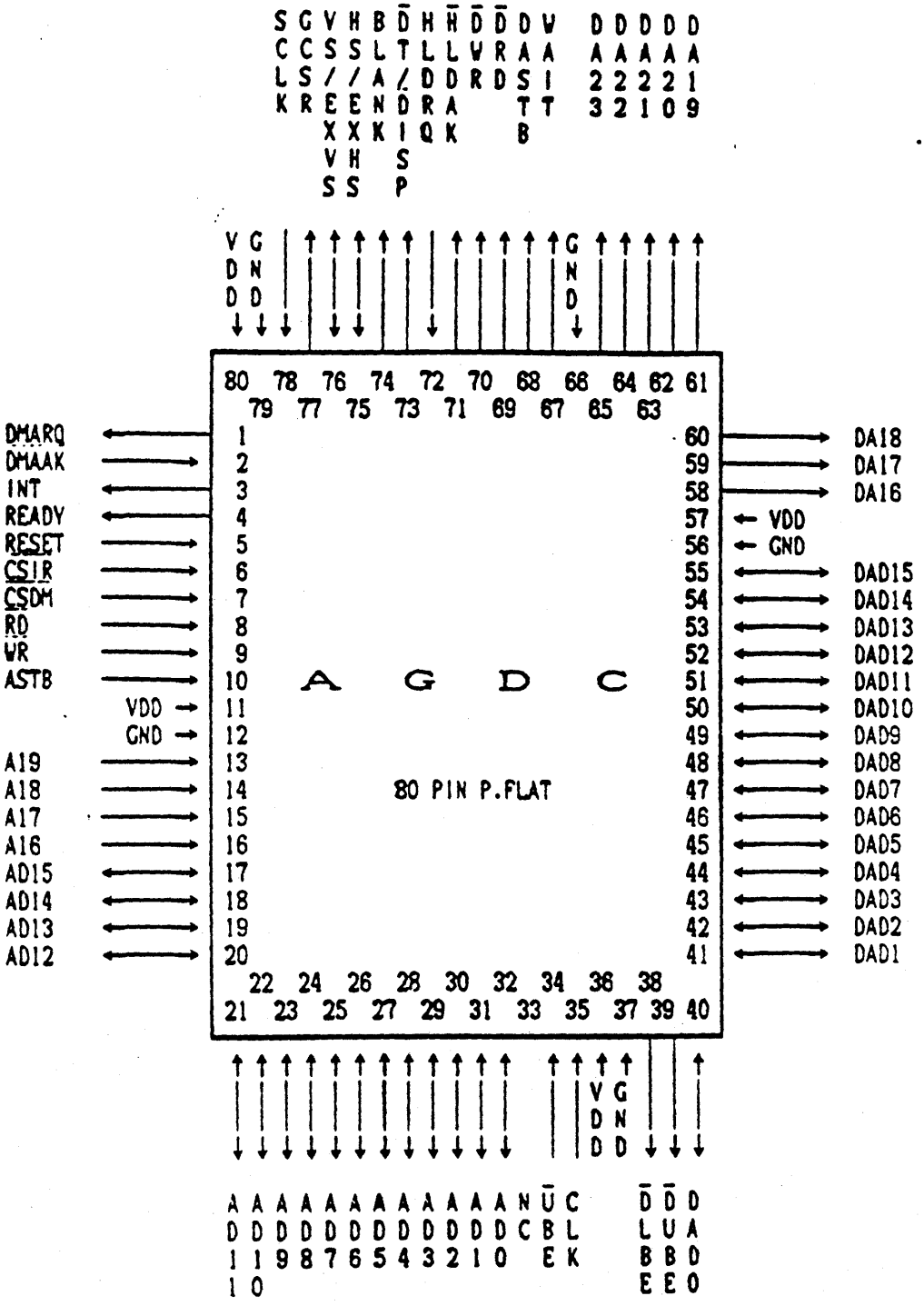
* Host Processor (CPU) Interface
  - System bus interface - 20-bit address bus, 8 or 16 bit data bus
  - System memory <—> display memory data transfer with external DMA Controller
    - From system memory to display memory (PUT)
    - From display memory to system memory (GET)
  - High speed pipeline processing with preprocessor before drawing processor
  - CPU memory or I/O mapping of internal registers and display memory - efficient system interface
* 8 MHz System Clock
* CMOS Technology
* Single +5 V Power Supply
* 80-pin flat package (uPD72120G) or 84-pin PLCC (uPD72120L)

Pin Configurations

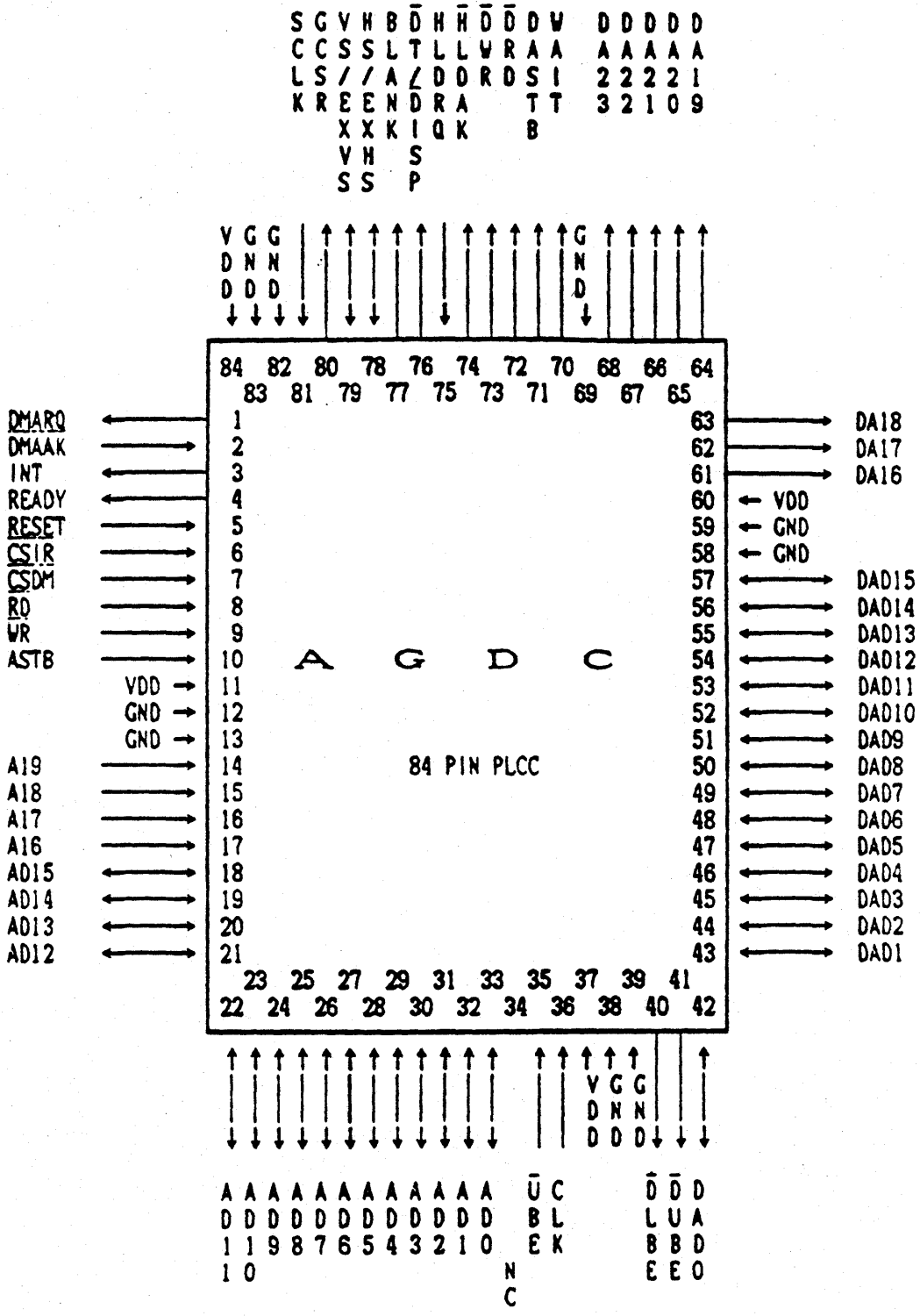
DMARQ: DMA Request
$\overline{\text{DMAAK}}$: DMA Acknowledge
INT: Interrupt Request
READY: Ready
RESET: Reset
$\overline{\text{CSIR}}$: Internal Register Chip Select
$\overline{\text{CSDM}}$: Display Memory Chip Select
$\overline{\text{RD}}$: Read
$\overline{\text{WR}}$: Write
ASTB: Address Strobe
MA19-16: Main Address Bus
MAD15-0: Main Data Bus
NC: No connection
$\overline{\text{UBE}}$: Upper Byte Enable
CLK: Clock
$\overline{\text{DLBE}}$: Display Memory Lower Byte Enable
$\overline{\text{DUBE}}$: Display Memory Upper Byte Enable

DA23-16: Display Memory Address Bus
DAD15-0: Display Memory Data Bus
DASTB: Display Memory Address Strobe
$\overline{\text{DRD}}$: Display Memory Read
$\overline{\text{DWD}}$: Display Memory Write
$\overline{\text{HLDAK}}$: Hold Acknowledge
HLDRQ: Hold Request
$\overline{\text{DT/DISP}}$: Data Transfer/Display Timing
BLANK: Blanking Signal
HS/EXHS: Horizontrol Sync/ External Horiz. Sync
VS/EXVS: Vertical Sync/External Vertic1 Sync
GCSR: Graphics Cursor
SCLK: Sync Generator Clock
GWAIT: Graphics Wait

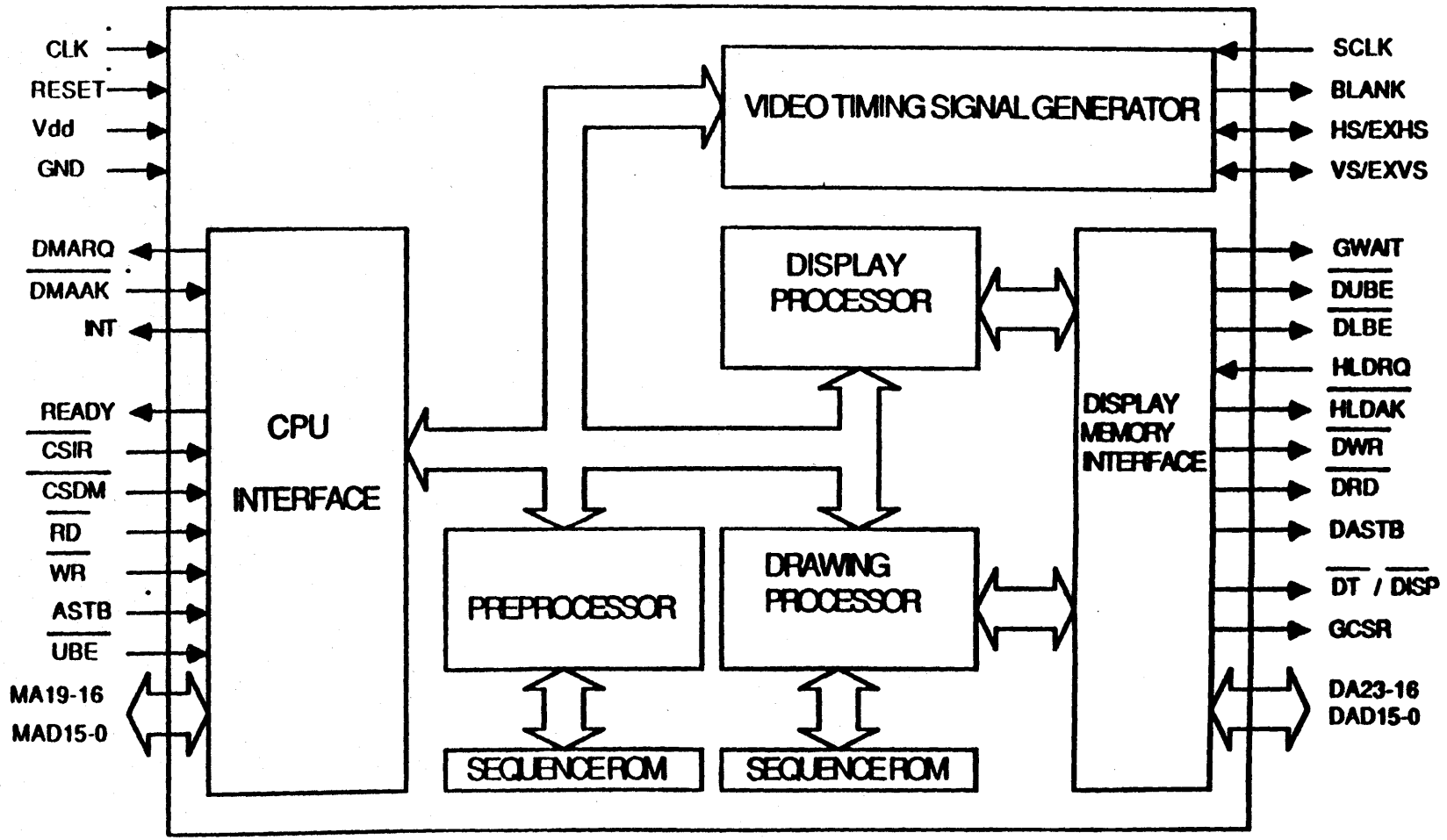
Pin Configuration (Flat)



Pin Configuration (PLCC)



AGDC BLOCK DIAGRAM



Block Diagram

Pin Functions

Clock Pins

Terminal Name	I/O	Active level	Function
CLK	I	-	Clock supplied to the circuits other than the the sync signal generator and display processor. The drawing processor and preprocessor speed depend on this clock frequency.
SCLK	I	-	Clock supplied to the sync signal generator and the display processor. This clock frequency is determined by the CRT timing requirements - i.e., horizontal sync frequency, the number of dots per line, etc.

System Bus Control Pins

Terminal Name	I/O	Active level	Function
MAD15-0	I/O	-	I/O bus to the CPU consisting of multiplexed 16-bit address and a bidirectional data bus.
MA19-16	I	-	Upper four address bits of the 20-bit address.
ASTB	I	H	Latches the address on MA19-16 and MAD15-0 on the falling edge.
UBE	I	L	Together with MAD0 defines the data access format as shown below. UBE should be tied high when connected to an 8-bit CPU. MAD0 $\overline{\text{UBE}}$ Data Access Format 0 0 Even address word 0 1 Even address byte 1 0 Odd address byte 1 1 Odd address byte

System Bus Control Pins (continued)

Terminal Name	I/O	Active level	Function
RD	I	L	Performs a read of data from the AGDC by the host CPU.
WR	I	L	Performs a write of data to the AGDC from the host CPU.
CSIR	I	L	Enables reading/writing of AGDC internal registers by the host CPU. The register is selected by the address input on MAD7-0.
CSDM	I	L	Enables reading/writing of display memory through the AGDC by the host CPU. The display memory address is generated by the address input on MA19-16 and MAD15-0 and by the bank register.
READY	O	H	Activated by the data access request (RD/WR) for the AGDC. During the access, the signal is low. RESET will set the READY line high.
INT	O	H	Signals an interrupt from the AGDC.
DMARQ	O	H	Indicates a request for data transfer (PUT/GET) to an external DMA controller. DMARQ will be low after RESET.
DMAAK	I	L	Acknowledgment of DMA request to the AGDC by the DMA controller.
RESET	I	H	Initializes operation of the AGDC. The internal parameter register is not cleared by RESET (it is initialized by setting data).

Display Memory Control Pins

Terminal Name	I/O	Active level	Function
DAD15-0	I/O	-	I/O pins for display memory - 16-bit address multiplexed with data.
DA23-16	O	-	Upper 8 bits of display memory address (the lower 16 bits of the 24-bit address are output on DAD15-0).
DASTB	O	H	Indicates that a display memory address is present on the falling edge.
DUBE DLBE	O	L	Defines the data format for accessing the display. RESET sets both pins low. AGDC — $\overline{DUBE}$ 0, $\overline{DLBE}$ 0 — Word 16-bit CPU — $\overline{DUBE}$ 0, $\overline{DLBE}$ 0 — Word 8/16-bit CPU — $\overline{DUBE}$ 0, $\overline{DLBE}$ 1 — High (odd) byte 16-bit CPU — $\overline{DUBE}$ 1, $\overline{DLBE}$ 0 — Low (even) byte 8-bit CPU — $\overline{DUBE}$ 1, $\overline{DLBE}$ 1 — High (odd) byte
DRD	O	L	Controls reading of the display memory by the AGDC. Set high by RESET.
DWR	O	L	Controls writing to the display memory by the AGDC. Set high by RESET.
HLDRQ	I	H	Requests control of the display memory bus by an external device to transfer display data
HLDAK	O	L	Indicates that the AGDC memory bus (DA23-16 and DAD15-0) is in the high impedance state so that an external device can have access to display memory bus. Set high by RESET.

Video Timing Signal Related Pins

Terminal Name	I/O	Active level	Function
VS/EXVS	I/O	H	When the AGDC operates as the master, VS is the vertical sync signal. When the AGDC operates as a slave, EXVS initializes the internal vertical sync signal on the rising edge.
HS/EXHS	I/O	H	When the AGDC operates as the master, HS is the horizontal sync signal output. When the AGDC operates as a slave, EXHS initializes the internal horizontal sync signal on the rising edge.

Display Signal Related Pins

Terminal Name	I/O	Active level	Function
BLANK	O	H	Used to blank the display.
DT/DISP	O	L	Set to DT in the DT mode (VRAMs used) and specifies the data transfer. In the cycle steal mode (VRAMs not used) indicates display cycle.
GCSR	O	H	Specifies the display of the graphics cursor
GWAIT	O	H	Graphics wait signal

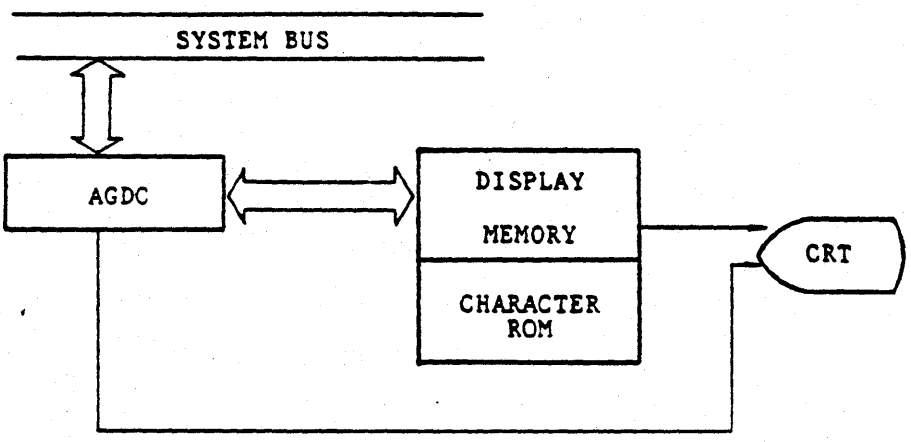
Power Supply and Ground Pins

Terminal Name	I/O	Active level	Function
V_{DD}	-	-	+5 V power supply
GND	-	-	Ground

Summary

The AGDC is an LSI device that can be used to control a raster scan CRT connected to a personal computer, word processor, or various kinds of work stations. The AGDC not only generates the video timing signals needed by the CRT, but can draw various kinds of characters and graphics at high speed. The AGDC also has abundant functions required by many advanced system.

The figure below shows the basic configuration of a system employing the AGDC.



Section 2

Functional Description

2.1 Features

High Speed Graphics Drawing

- Graphics Drawing

  The AGDC has graphic drawing commands to draw dots, straight lines, rectangles, circles and arcs, all of which are indispensable for CAD/CAM, office automation, document processing and printing. In addition, the AGDC supports the drawing of sectors, ellipses, ellipse arcs and ellipse sectors as advanced graphic primitives. These high speed graphics are drawn at maximum rate of 500 ns/pixel (8 MHz clock) for a straigh line, 1 us/pixel for a curved line (arc, etc.).

- Painting

  The AGDC can paint or fill in a triangle, rectangle, trapezoid or circle as well as any enclosed area. This powerful feature is useful not only for document processing but advanced three dimensional graphics as well. Since the tiling pattern for painting can be freely set in the display memory, the areas to be painted can be drawn with any of a wide assortment of colors.

  In the past, painting was performed by software on the host CPU which is time consuming. For this reason, painting was used in only limited applications. The AGDC can upgrade the performance for painting speed by as much as several hundred times compared to painting done by a host CPU. This enables painting to be applied more extensively through the use of the AGDC.

- Transfer of Data in Display Memory (COPY)

  The 'COPY' commands refers to bit-block transfers (also known as bilblt). This commands transfer a rectangular area of any size and bit position to another similarly sized rectangle. The 'COPY' command performs powerful character drawing and window control functions.

  In the past, a character could be displayed only with a fixed size and at a set position (word boundary) on the screen. The word processing applications of today require more flexibility in the display of characters. As a result, it is necessary to display characters of different fonts, styles and sizes and to proportionally space characters. The 'COPY' function of the AGDC can satisfy all of these demands and at high speed - 500 ns/16 bits.

  Personal computers are making use of multiple windows on display screens. The 'COPY' command allows the user to easily specify the

number, shape and size of multiple windows. Further, the 'COPY' command of the AGDC can perform various logical operations between source and destination planes.

- Image Processing

  The AGDC is able to do more than just copy data. It can slant copy, arbitrary angle rotation copy, 16/n enlargement copy or n/16 shrink copy (n any integer from 1 to 16). These copies transfer data from a rectangular source area to a non-rectangular destination.

  The slant copy can be used for drawing italic characters. The arbitrary angle rotation copy is useful for document preparation because it can rotate characters, graphics, images, etc. The enlarge and shrink copies are effective for editing and patching documents.

  These AGDC commands relieve the host CPU of what was a software intensive function. The AGDC can quickly accomplish these image processing tasks and for a lower cost.

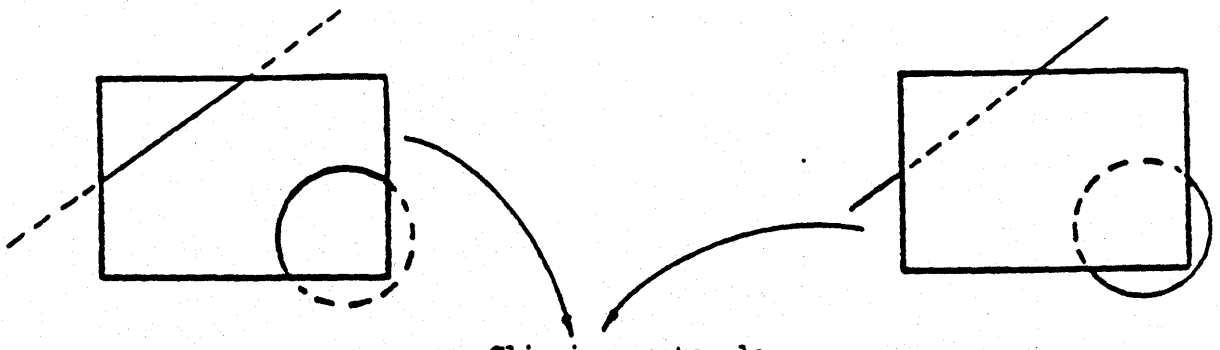
- Position Specification by X-Y Coordinates

  The graphics drawing and copy parameters can be given as X-Y coordinates thereby relieving the host CPU of the address calculation requirements.

- Hardware Clipping

  Clipping is used to draw either inside or outside a rectangular window defined by the user. For example, a command to draw a straight line from the outside to the inside of a window will only be seen inside (or outside) of the window when clipping is used.

  The AGDC implements clipping in hardware so that the user need only specify the coordinates of the rectangular window and the mode to indicate whether to clip inside or outside of the window.



Clipping rectangle

Inside drawing mode

Outside drawing mode

(- - - Invisible line)

Video Timing Signal Generation

- High Speed Processing by Dual System Clocks

  Dual system clocks can be input to the AGDC - the drawing clock and the display clock. In a graphics system, the display rate depends on the resolution of the CRT; the clock frequency of the display controller depends on the display rate. In the past, only a single clock was used for the display controller. It was often necessary to limit the clock to 5 MHz even though the capacity of the display controller was 8 MHz. Therefore, the AGDC was designed to have the display clock independent of the drawing clock so that drawing can be performed at the highest possible speed.

- External Sync Input

  In systems that incorporate a separate circuit to generate the video timing signals and use an AGDC only to draw graphics, or in systems that use multiple AGDCs to achieve higher performance, it is necessary to synchronize the AGDC with the external circuitry or the AGDC with other AGDCs. Therefore, the AGDC has external sync input capability to synchronize its operations with other AGDCs or with external circuitry.

Large Capacity Display Memory Control

- Display Memory Bus Interface

  With its 24-bit addressing and 16-bit data, 16 Mwords of 16 bits/word display memory can be configured with the AGDC. This means that up to 64 planes of 2048 x 2048 dots can be connected.

- Video RAM (VRAM) Control

  VRAMs are dual-ported DRAMs with internal line buffer shift registers (i.e., uPD41264). The VRAMs provide a separate port for display data so that when drawing, memory access time is greatly reduced. As a result, most of the entire memory cycle can be used as the drawing cycle to improve system throughput. The AGDC supplies the signals needed to control VRAMs.

- Display Memory Bus Arbitration

  In a basic system, the display memory is accessed by the AGDC only. However, in a more advanced system, the display memory may be accessed by other processors. In other words, a local bus is established between the display memory and the AGDC or other processors. In this case, it is necessary for the AGDC to periodically provide refresh and display control and thus act as the local bus master. Other processors on the display memory bus (i.e., an image processor) are slaves and must request use of the bus from the AGDC. The AGDC controls the display memory bus and can grant the use of the bus to other processors. The AGDC incorporates display memory bus arbitration logic enabling higher performance systems to be constructed for a lower cost.

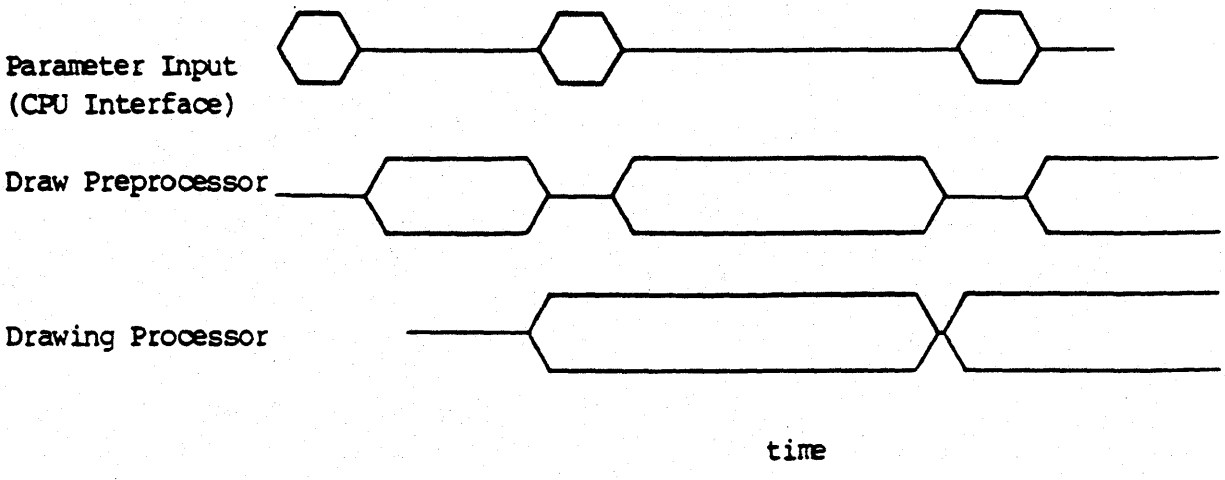
CPU Interface

- System Memory Bus Interface
- CPU Mapping of Internal Registers and Display Memory

  The AGDC system memory bus interface to the host CPU is independent of the display memory bus. The width of the address which the CPU can input to the AGDC is 20 bits and the data width is 8 or 16 bits. The 20-bit address is used when the display parameters, drawing parameters and commands are set and the CPU accesses the display memory directly. The internal AGDC registers and the display memory can be mapped in the CPU memory or I/O space. This allows the CPU to efficiently execute special drawing processing directly in the display memory. The mapping of AGDC registers in the CPU memory space provides for quick access of information to and from the AGDC.
- System Memory <—> Display Memory Data Transfer

  As described above, it is possible to map the display memory in the CPU memory space. It is also possible to execute PUT/GET commands - to transfer the data between the system memory and the display memory at high speed through the use of an external DMA controller. PUT is the command to transfer data from the system memory to the display memory. GET is the command to transfer data from the display memory to the system memory.
- High Speed Pipeline Drawing Processing

  The parameters given by the CPU to the AGDC are greatly reduced by using X-Y coordinates. However, it is necessary for the AGDC to calculate physical memory addresses for the drawing processor. The process to convert the X-Y coordinates from the CPU into physical addresses is done by the drawing preprocessor. The drawing processor executes the actual drawing commands independent of the preprocessor. Therefore the drawing processor and preprocessor can operate concurrently. As shown in the figure below, the throughput of the system is improved by the use of the drawing preprocessor and the drawing processor in a pipeline.



2.2 Command/Parameter Exchange Between the CPU and AGDC

It is necessary for the CPU to set various parameters and commands to operate the drawing and display control functions of the AGDC. To set these parameters and commands, the CPU writes them directly to the AGDC internal registers.

The internal registers of the AGDC can be classified into registers the CPU can read and write directly and registers in which reading or writing is prohibited. The registers which can be read and written are assigned unique addresses. They are mapped in the CPU memory or I/O space and referred to as the 'command/parameter table'. These registers are selected by the lower 8 bits (00H - FFH) of the address input on MAD0 - MAD7 to the AGDC when CSIR is low. The data to be read or written can be sent through the data bus in the same address cycle providing high speed command or parameter exchange.

The AGDC incorporates a preprocessor for drawing preprocessing and a drawing processor for the actual drawing. The drawing preprocessor calculates the effective (physical) address from X-Y coordinates (logical address) given by the CPU and generates the parameters of the micro-level codes interpreted by the drawing processor. The drawing preprocessor decodes commands and performs the drawing preprocessing necessary to execute commands in the command/parameter table. It is not necessary to write all the parameters in the command/parameter table. Only the required parameters for the particular command need be written.

Of the addresses 00H - FFH in the internal register space, 80H - FFH are not presently used. These are reserved for future use. The register addresses 00H-7FH can be grouped into four categories as shown in the following table.

Classification	Register Name	Address	CPU Access
(1) AGDC control	STATUS (Read)	3CH - 3DH	Read - at any time
	CTRL, BANK (Write)	3CH - 3DH	Write - at any time
(2) Display related registers	DISPLAY FLAGS	70H - 7FH	Read - inhibited
	DISPLAY PITCH		Write at any time
	DAD, WC, AC		
	GCSRX,GCSRYS,GCSRVE		
	CRS, CE		
	HS,HBP,HH,HD,HFP		
	VS,VBP,L/F,VFP		
(3) Drawing related registers	EADORG, dADORG	00H - 1FH	Read at any time
	EAD1, dAD1	40H - 6FH	Write - 3 types of
	EAD2, dAD2		handshaking selectable
	PDISPS, PDISPD		A. status flag
	PITCHS, PITCHD		B. ready signal
	PMAX,MOD1,MOD0		C. INT signal
	PLANES		
	PINP,PINCNT		
	STACK,SIMAX		
	CLIP		
	XCLMIN,XCLMAX		
	YCLMIN,YCLMAX		
	MACH,MAGV		
	X,DX,XS,XE,XC,DH		
	Y,DY,YS,YE,YC,DV		
	COMMAND		
(4) Data port	DMAPORT (during PUT/GET execution)	3EH - 3FH	
	DX (during READ DP/READ COL execution)	44H - 45H	

Note: The DX register is used as the logical address (coordinate) setting register and at the same time as the data port during execution of the READ DP/READ COL command.

The registers in the first classification - STATUS, CTRL and BANK - are assigned address 3CH - 3DH. The contents of the STATUS register can be read at any time. The CTRL and BANK registers can be written to by the CPU at any time.

The registers in the second group - display related registers - are assigned addresses in the range 70H - 7FH. The contents of these registers cannot be read. Data can be written to these registers at any time. However, writing to these registers can disturb the CRT display. To prevent this, the display can be blanked while writing to these registers. First set the SD bit in the DISPLAY FLAGS register (address 70H-71H) to '1'. Second, write the data into the display related register group. Third, set the SD bit from '1' back to '0'.

Follow these procedures to write data (SYNC parameters) such as HS, HBP, HH, HD, HFP, VS, VBP and L/F on the registers at address 7EH - 7FH:

1. Set the SYNC bit in the DISPLAY FLAGS register (70H - 71H) to '1'
2. Write, in the order listed, HS, HBP, HH, HD, HFP, VS, VBP, L/F AND VFP (address 7EH - 7FH).
3. Set the SYNC bit to '0'

The registers in the drawing related group are assigned addresses from 00H to 1FH and 40H to 6FH. The preprocessor resides in this register group. The read/write option of these registers are:

- Read

  The CPU can read the contents of these registers at any time. The preprocessor stops for one clock while the contents of a register are read.

- Write

  One of three writing procedures can be used:

  1. Check the STATUS register PPBSY flag (address 3CH)
  2. Use the READY signal
  3. Use the INT pin to signal an interrupt to the CPU

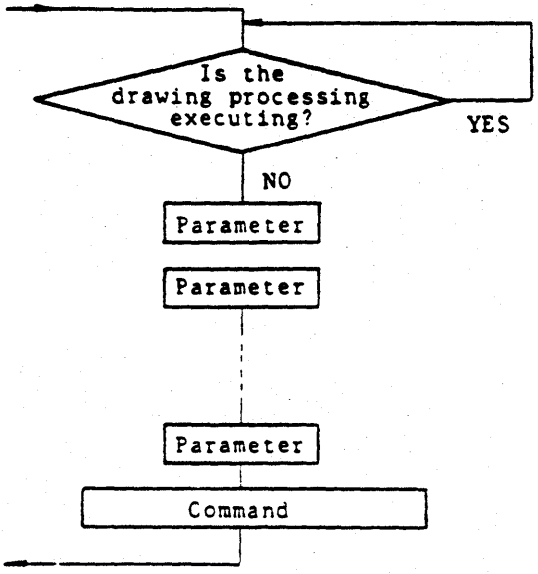
The method described by (1) is the general method. The contents of the status flag are read to check that the preprocessor is not in operation. If the preprocessor is not busy, then data can be written to the command/parameter table.

In the method described by (2), the CPU is tied to the AGDC's READY line. If the preprocessor is busy, the CPU cannot write the data until the preprocessor is finished and the READY line goes high. This procedure enables the command/parameter data to be sent at a higher speed.

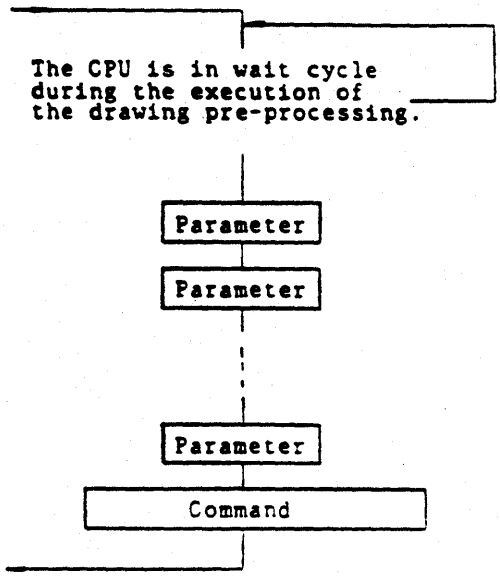
In the method described by (3), the CPU is interrupted by the AGDC when the preprocessor is available. The AGDC, through its INT line, informs the CPU to send command/parameter data. The CPU interrupt routine should send a command and parameters to the AGDC. The 'INT' line is enabled or disabled by a flag in the CTRL register (address 3DH).

The three write methods are illustrated below.

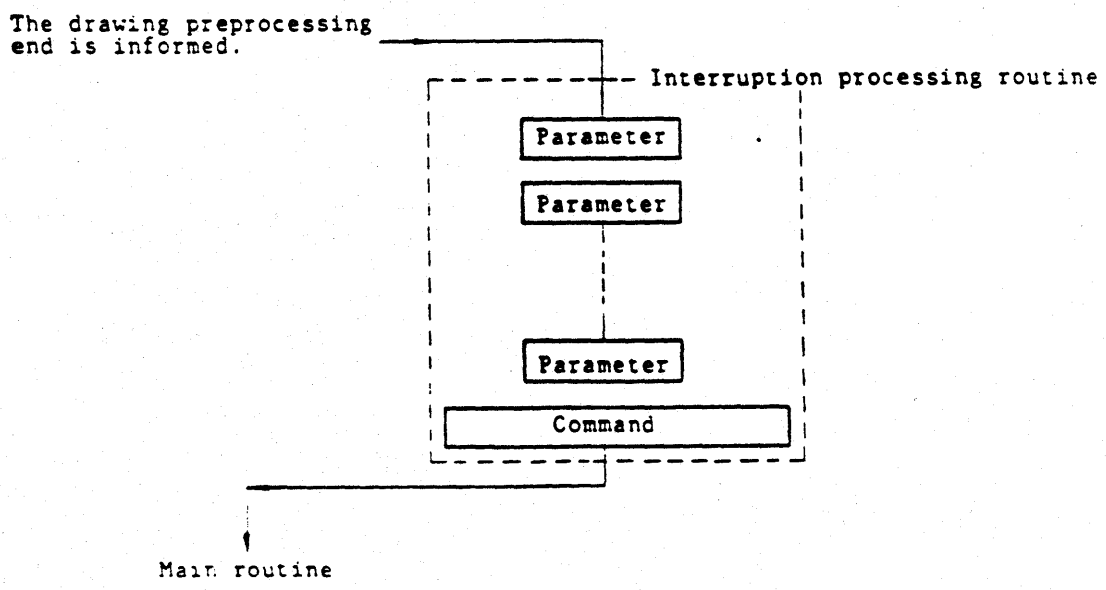
Procedure (A) ... Handshake by the busy flag



Procedure (B) ... Handshake by the READY signal



Procedure (C) .. Handshake by the INT signal



The data port register, DMAPORT, is at address 3EH - 3FH. The drawing processor uses this register during execution of the drawing preprocessing. Therefore, to read/write this register, follow the method for reading or writing the drawing preprocessor.

2.3 Reset and Abort Operation

The AGDC resets or aborts processing by any of the following procedures:

- Reset Operation
  1. Set the RESET input signal (pin 5) to a high level (hardware reset)
  2. Set the RESET flag in the CRTL register to '1' (software reset).
- Abort Operation
  3. Set the ABORT flag in the CTRL register to '1'.

Reset/Abort Operation	Operation
(1) Hardware Reset	- sets the display stop flag SD in the DISPLAY FLAGS register (70H - 71H) to '1' - sets all bits in the CTRL register (3DH) to '0' - all other registers maintain the same status - stops the preprocessor and the drawing processor - initializes the video timing signals - stops the image memory direct access
(2) Software Reset	- same as the hardware reset but does not set the display stop flag in the DISPLAY FLAGS register (70H - 71H) to '1' and does not initialize the video timing signals
(3) Abort	- all registers maintain their status - stops the preprocessor and drawing processor

Section 3

AGDC Operation

3.1 How to Use the Internal Registers

The internal registers of the AGDC are classified as shown in the table below:

Classification	Application	Register Name	Address (Hex)
AGDC control registers	Status	STATUS	3C
	Control	CTRL	3D
	Higher 8 bits of address in display memory direct access	BANK	3C
Display related registers	Display status setting	DISPLAY FLAGS	70 - 71
	Display area setting	DISPLAY PITCH, DAD, WC	72 - 77
	Cursor setting	CRS, CE, GCSRX, GCSRYS, GCSRVE	78 - 7D
	Horizontal sync signal setting	HS, HBP, HH, HD, HFP	7E - 7F
	Vertical sync signal setting	VS, VBP, L/F, VFP	7E - 7F
Drawing related registers	Logical address zero point setting	EADORG, dADORG	00 - 03
	Logical address setting	PITCHS, PITCHD	58 - 5B
	Plane setting	PMAX, PDISPS, PDISPD	0C - 15
	Inter-plane logical operation setting	MOD0, MOD1, PLANES	16, 5E - 5F
	Clipping setting	CLIP, XCLMIN, XCLMAX, YCLMIN, YCLMAX	6D, 62 - 69
	Enlarge/Shrink coefficient setting	MAGH, MAGV	6C

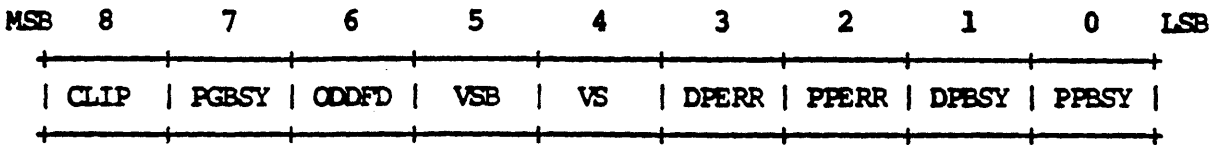
Classification	Application	Register Name	Address (Hex)
Drawing related registers (continued)	Painting pattern setting	PTNP, PTNCNT	18-1A,60-61
	AGDC work area set	STACK, STMAX	1C-1E,5C-5D
	Physical address (word addr) value setting	EAD1, EAD2	04-06,08-0A
	Physical address (dot addr.) value setting	dAD1, dAD2	07, 0B
	Logical address (X coord.) value set	X, DX*, XS, XE, XC, DH	40 - 55
	Logical address (Y coord.) value set	Y, DY, YS, YE, YC, DV	42 - 57
	Command	COMMAND	6E - 6F
Data port	Data port during execution of PUT/GET	DMAPORT	3E - 3F
	Data port during execution of READ DP/READ COL	DX*	44 - 45

*: The DX register is used as the logical address (X coordinate) value setting register and at the same time as the data port during the execution of a READ DP/READ COL command.

3.2 AGDC Control Registers

STATUS (Status)

No. of bits: 16
Address: 3CH - 3DH (Read)
Application: The status of the internal operation of the AGDC. The format is as follows:



Bit	Flag Name	Abbrev.	AGDC status when flag is '1'
0	PRE-PROCESSOR BUSY	PPBSY	The preprocessor is executing a command
1	DRAWING PROCESSOR BUSY	DPBSY	The drawing processor is executing a command
2	PRE-PROCESSOR ERROR	PPERR	An error was detected during the execution of the command by the preprocessor
3	DRAWING PROCESSOR ERROR	DPERR	An error was detected during the execution of a command by the drawing processor
4	VERTICAL SYNC PERIOD	VS	Indicates vertical sync period
5	VERTICAL BLANKING PERIOD	VSB	Indicates vertical blanking period
6	ODD FIELD	ODDFD	Indicates odd field during interlaced scanning

Status (continued)

Bit	Flag Name	Abbrev.	AGDC status when flag is '1'
7	PUT/GET BUSY	PGBSY	Indicates that data can be transferred during a PUT/GET command
8	CLIPPING	CLIP	Picking or object detected
9 - 15			Reserved for future use

BANK (Bank)

No. of bits: 8
Address: 3CH (Write)
Application: The CPU interface on the AGDC accomodates 20-bit addresses. The AGDC can address 32 Mbytes of display memory (24 bits). When the CPU addresses display memory directly, the lower 16 bits provided by the CPU (bits 0 - 15) is combined with the upper 8 bits (bits 16-23) of the BANK register to form the 24-bit display memory address.

CTRL (Control)

No. of bits: 8
Address: 3DH (Write)
Application:

MSB 7	6	5	4	3	2	1	0 LSB
DBIE	PBIE	CIE	0	0	0	ABORT	RESET

Bit	Flag Name	Abbrev.	AGDC status when flag is '1'
0	SOFTWARE RESET	RESET	Initializes AGDC*
1	PROCESSOR ABORT	ABORT	Stops any processing being performed and clears the processor busy status
2	NOT USED		
3	NOT USED		Must be set to '0'
4	NOT USED		
5	CLIPPING INTERRUPT ENABLE	CIE	Enables the INT signal when picking (drawing in the clipped region)
6	PRE-PROCESSOR BUSY INTERRUPT ENABLE	PBIE	Enables the INT signal on the INT pin. INT output when preprocesser status changes from BUSY to NOT BUSY
7	DRAWING PROCESSOR BUSY INTERRUPT ENABLE	DBIE	Enables the INT signal on the INT pin to be output when the drawing processor status changes from BUSY to NOT BUSY

*: Please refer to section 2.3, 'Reset and Abort Operation'

3.3 Display Related Register

DISPLAY FLAGS (Display Flags)

No. of bits: 16
Address: 70H - 71H (Write)
Application: To select the operation of the display processor and the video timing signal generator.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE/DT			DAD+		IN	RE	SC	FCCL	TCCL	MASK	M/S	SD	LEO	SYNC	VS

Bit 0: VS (Vertical Sync)

The AGDC incorporates a horizontal/vertical counter to keep track of the current position of the display by the scanning line number counted from the top of the screen or by the word number counted from the left side. When the AGDC is used in the slave mode, the VS defines the timing of the horizontal/vertical counter by the external sync signal, EXVS. When the AGDC is used in the master mode, the VS is ignored.

VS	Function
0	The total number of display lines in the 1st and 2nd fields is even
1	The total number of display lines in the 1st and 2nd fields is odd

DISPLAY FLAGS (continued)

Bit 1: SYNC (Sync Parameter Setting)

This bit permits the writing of data in the registers (HS, HBP, HH, HFP, VS, VBP, LF and VFP) assigned to the address 7EH - 7FH.

SYNC	Function
0	No writing is permitted
1	Writing is permitted

Bit 2: LEO (Display Lines per Frame in Interlace Mode)

This bit defines the total number of display lines per frame (the first and second fields) in the interlace mode (IN = 1 in DISPLAY FLAGS). For non-interlace mode (IN = 0), LEO is ignored.

LEO	Function
0	The total number of display lines in the 1st and 2nd fields is even
1	The total number of display lines in the 1st and 2nd fields is odd

Bit 3: SD (Stop Display)

This bit defines the output status of the BLANK pin. This bit is set to '1' when the RESET pin is high.

SD	Function
0	The BLANK pin is activated between the non-display period defined by the sync signal generator
1	The BLANK output pin is activated in all the period

DISPLAY FLAGS (continued)

Bit 4: M/S (Master/Slave)

This bit defines the master/slave mode of the AGDC

MS	Function
0	The AGDC is set to master mode (HSYNC, VSYNC)
1	The AGDC is set to slave mode (EXHS, EXVS)

Bit 5: MASK (Mask)

This bit defines the VSYNC output pin timing in the master mode (MS = 0 in DISPLAY FLAGS). It also defines the validity/invalidity of the EXHS and EXVS input pins in the slave mode (MS = 1 in DISPLAY FLAGS).

MS	MASK	FUNCTION
0	0	Only the VSYNC signal in the first field is output in the interlace display mode (IN = 1 in DISPLAY FLAGS)
	1	The usual VSYNC signal is output
1	0	The EXHS and EXVS external sync input signals are valid
	1	The EXHS and EXVS external sysnc input signals are invalid

DISPLAY FLAGS (continued)

Bit 6: TCCL (Timing Counter Clear)

The AGDC display the data by using two cycles of D1 and D2 as one unit. Therefore, the AGDC incorporates the display cycle counter to recognize the D1 cycle and the D2 cycle during display. This bit defines the initializing timing of the display cycle counter by the EXVS external sync input signal. In the master mode (MS = 0 in DISPLAY FLAGS), TCCL is ignored.

TCCL	Function
0	The display cycle counter is not initialized (to the D1 cycle) on the rising edge of EXVS
1	The display cycle counter is initialized (to the D1 cycle) on the rising edge of EXVS

Bit 7: FCCL (Field Counter Clear)

The AGDC incorporates the field counter to recognize the first field and the second field in the interlace display mode. This bit defines the initializing timing of this field counter by the EXVS external sync input signal. In the master mode (MS = 0 in DISPLAY FLAGS) or in the non-interlaced display mode (IN = 0 in DISPLAY FLAGS), FCCL is ignored.

FCCL	Function
0	The field counter is not initialized (to the first field) on the rising edge of EXVS
1	The field counter is initialized (to the first field) on the rising edge of EXVS

DISPLAY FLAGS (continued)

Bit 8: SC (Steal Count)

This bit defines the relationship between CLK and SCLK in the dual port DRAM (VRAM) drive mode (SE/DT = 1x in DISPLAY FLAGS). In the cycle steal mode (SE/DT = 0x in DISPLAY FLAGS), SC is ignored.

SC	Function
0	This bit is set to 0 when CLK ≠ SCLK
1	This bit is set to 1 when CLK = SCLK

Bit 9: RE (Refresh Enable)

This bit defines the DRAM refresh address output.

SC	Function
0	The DRAM refresh address is output when HSYNC is high
1	The DRAM refresh address is not output

Bit 10: IN (Interlace)

This bit sets the display screen mode.

IN	Function
0	The non-interlaced display mode is set
1	The interlaced display mode is set

DISPLAY FLAGS (continued)

Bits 11 - 13: DAD+ (Display Address Proceedings)

These bits define the progressive form of display addressing.

DAD+		Progressive form
000	DAD+1	DAD -> DAD+1 -> DAD+2 -> DAD+3 -> DAD+4 -> DAD+5 -> ...
001	DAD+2	DAD -> DAD+2 -> DAD+4 -> DAD+6 -> DAD+8 -> DAD+10 -> ...
010	DAD+4	DAD -> DAD+4 -> DAD+8 -> DAD+12 -> DAD+16 -> DAD+20 -> ...
011	DAD+8	DAD -> DAD+8 -> DAD+16 -> DAD+24 -> DAD+32 -> DAD+40 -> ...
100	DAD+16	DAD -> DAD+16 -> DAD+32 -> DAD+48 -> DAD+64 -> DAD+80 -> ..
101	DAD+32	DAD -> DAD+32 -> DAD+64 -> DAD+96 -> DAD+128 -> ...
110	DAD+1/4	DAD -> DAD -> DAD -> DAD -> DAD+1 -> ...
111	DAD+1/2	DAD -> DAD -> DAD+1 -> DAD+1 -> DAD+2 -> ...

DISPLAY FLAGS (continued)

Bits 14-15: SE/DT (Steal Enable/Data Transfer Mode)

These bits indicate whether VRAMs or DRAMs are used for the display memory. When DRAMs are used, drawing is accomplished by memory cycle stealing. When VRAMS are used, the timing mode of the data transfer signal DT is defined.

SE/DT	Function
0x	The cycle steal mode (the DISP signal indicating the display period output) is used
10	The DT signal is generated at the timing which satisfies at least one of the following three conditions: 1. At the start of the display on the screen 2. At the start of the display of each scan line on the screen 3. When all the lower 8 bits of the 24 bits of display address are 0
11	The DT signal is generated at the timing which satisfies at least one of the following two conditions: 1. At the start of the display on the screen 2. When all the lower 8 bits of the 24 bits of the display address are 0

DISPLAY PITCH (Display pitch)

No. of bits: 12
Address: 72H - 73H (Write)
Application: Sets the number of addresses in the horizontal direction of the image memory plane.

DISPLAY PITCH	No. of addresses
0000 0000 0000	0
0000 0000 0001	1
0000 0000 0010	2
.	.
.	.
.	.
1111 1111 1101	4093
1111 1111 1110	4094
1111 1111 1111	4095

AC (Address Control)

No. of bits: 3
Address: 73H (Write)
Application: These bits define the output of the 9 bit refresh address to the display address lines DA23 - DA16 and DAD15 - DAD0. The table below shows the change in the lower 8 bits of the display address which is used to set the output timing signal DT in the VRAM drive mode (SE/DT = 11 in DISPLAY FLAGS) according to the AC value.

AC	Refresh address output pins	The condition to activate the DT signal in the dual port DRAM drive mode
000	DAD8 - DAD0	When DAD7 - DAD0 are 0
001	-	prohibited
010	-	prohibited
011	-	prohibited
100	DAD9 - DAD1	When DAD8 - DAD1 are 0
101	DAD10 - DAD2	When DAD9 - DAD2 are 0
110	DAD11 - DAD3	When DAD10 - DAD3 are 0
111	DAD12 - DAD4	When DAD11 - DAD4 are 0

DAD (Display Address)

No. of bits: 24
Address: 74H - 76H (Write)
Application: These bits set the display starting physical address in the memory.

WC (Word Count)

No. of bits: 8
Address: 77H (Write)
Application: These bits set the number of address in the display period for one scanning period.

WC	No. of addresses
0000 0000	1
0000 0001	2
0000 0010	3
.	.
.	.
.	.
1111 1101	254
1111 1110	255
1111 1111	256

GCSRX (Graphics Cursor X Coordinate)

No. of bits: 12
Address: 78H - 79H (Write)
Application: These bits set the starting display address of the graphics cursor using the upper left corner of the screen as the origin. The graphics cursor display signal generation period in the horizontal direction is fixed to one display cycle period.

GCSRX	GCSR generation position/1 scan line
0000 0000 0000	Not defined
0000 0000 0001	1st display cycle
.	.
.	.
.	.
1111 1111 1110	4094th display cycle
1111 1111 1111	4095th display cycle

CRS (Cursor Out Select)

No. of bits: 1
Address: 79H (Write)
Application: This bit selects the logical OR or the logical AND of the horizontal coincidence signal with the vertical coincidence signal to be output at the GCSR pin.

CRS	Function
0	AND and output
1	OR and output

CE (Cursor Display Enable)

No. of bits: 1
Address: 79H (Write)
Application: Enables the graphics cursor output signal (GCSR)

CE	Function
0	Not enabled
1	enabled

GCSRYS (Graphics Cursor Y Coordinate Start)

No. of bits: 12
Address: 7AH - 7BH (Write)
Application: These bits set the Y coordinate of the graphics cursor display start on the screen using the upper left corner of the screen as the origin.

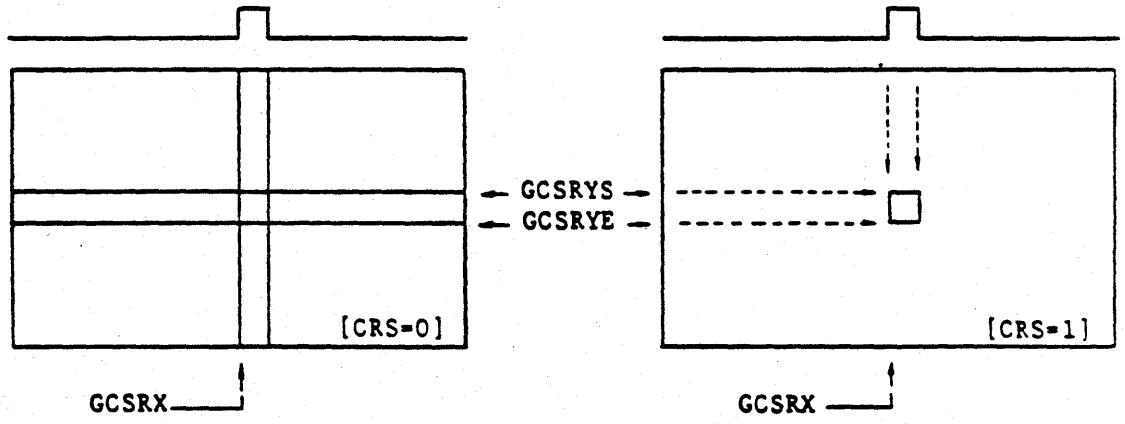
GCSRYS	GCSR generation position/1 scan line
0000 0000 0000	Not defined
0000 0000 0001	1st display cycle
.	.
.	.
.	.
1111 1111 1110	4094th display cycle
1111 1111 1111	4095th display cycle

GCRSYE (Graphics Cursor Y Coordinate End)

No. of bits: 12
Address: 7CH - 7DH (Write)
Application: These bits set the Y coordinate of the graphics cursor display end on the screen using the upper left corner as the origin.

GCSRYE	GCSR generation position/1 scan line
0000 0000 0000	Not defined
0000 0000 0001	1st display cycle
.	.
.	.
.	.
1111 1111 1110	4094th display cycle
1111 1111 1111	4095th display cycle

< Graphics Cursor Output Form >



When the value of GCSRYS < GCSRYE is not set, the graphics cursor output from the display line indicated by GCSRYS to the last display line is activated. When GCSRYS = GCSRYE, only one display line indicated by GCSRYS is displayed.

HS, HBP, HH, HD, HFP

HS (Horizontal Sync Signal)
HBP (Horizontal Back Porch; non-displayed period on the left of the CRT screen)
HH (Period from the HBP end to the center of one horizontal period)
HD (Horizontal display period)
HFP (Horizontal front porch; non-displayed period on the right of the CRT screen)

No. of bits: 12 each
Address: 7EH - 7FH (Write)
Application: These registers set the horizontal video timing parameters.

HS, HBP, HH, HD, HFP	No. of display cycles
0000 0000 0000	1
0000 0000 0001	2
0000 0000 0010	3
.	.
.	.
.	.
1111 1111 1101	4094
1111 1111 1110	4095
1111 1111 1111	4096

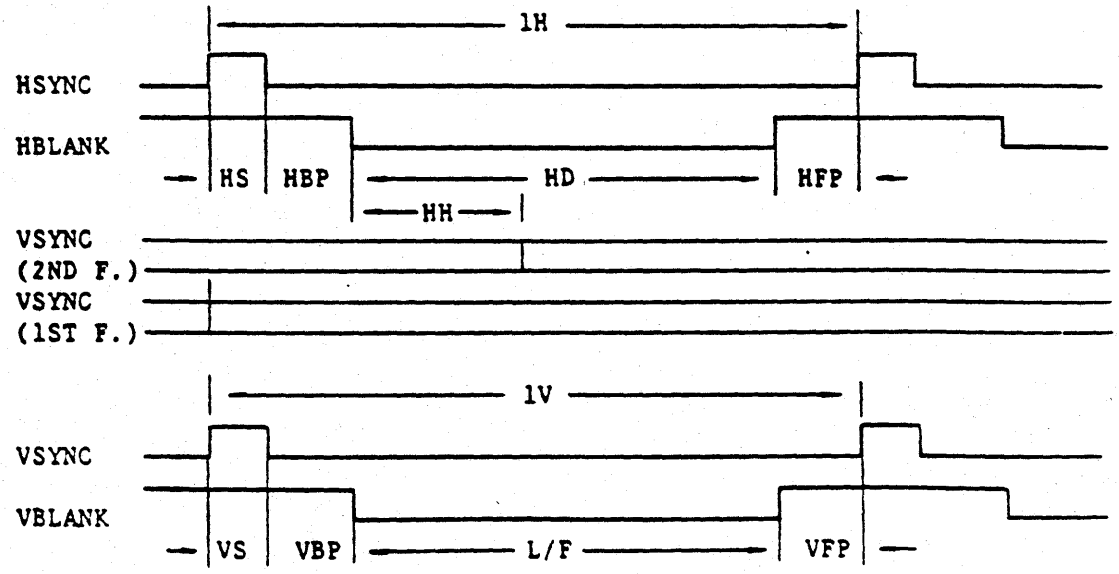
VS, VBP, L/F, VFP

VS (Vertical Sync signal)
VBP (Vertical Back Porch; non-displayed period on the upper part of the CRT screen)
L/F (Display period in the vertical direction)
VFP (Vertical Front Porch; non-displayed period on the lower part of the CRT screen)

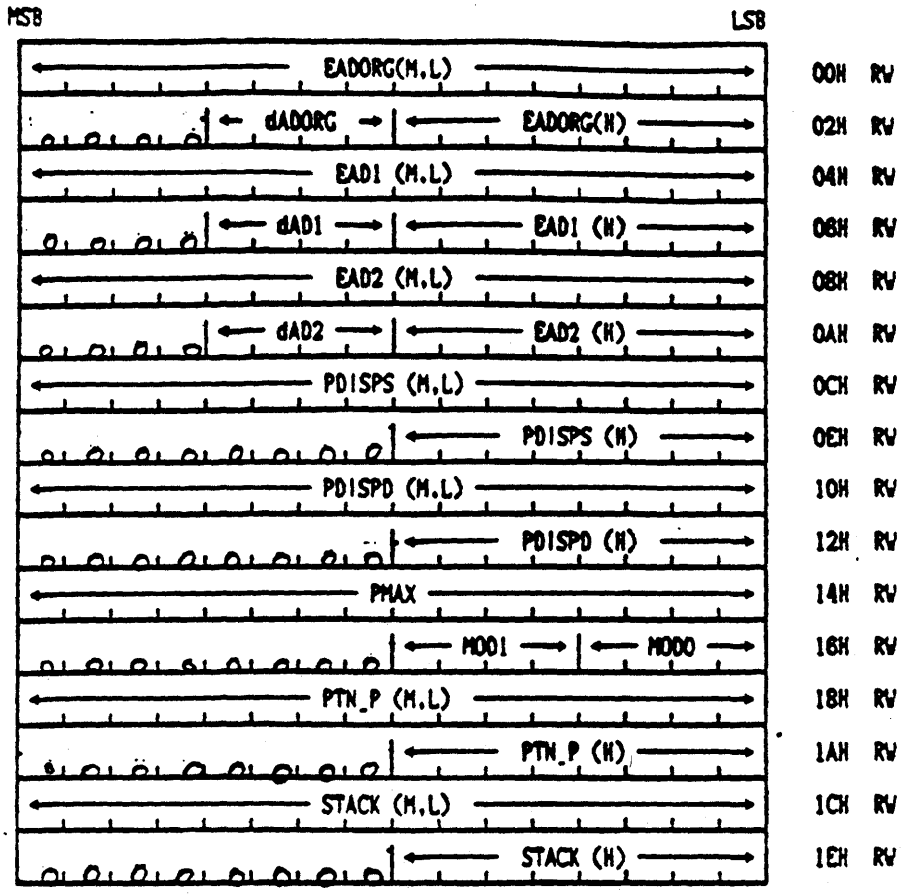
No. of bits: 12 each
Address: 7EH - 7FH
Application: These registers set the vertical video timing parameters.

VS, VBP, L/F, VFP	No. of display cycles
0000 0000 0000	1
0000 0000 0001	2
0000 0000 0010	3
.	.
.	.
.	.
1111 1111 1101	4094
1111 1111 1110	4095
1111 1111 1111	4096

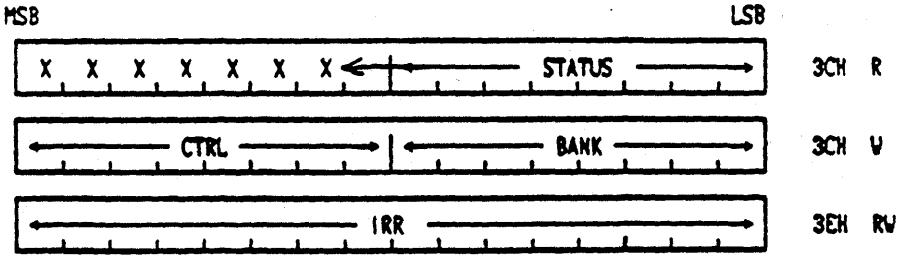
< Sync Signal Generation Diagram >



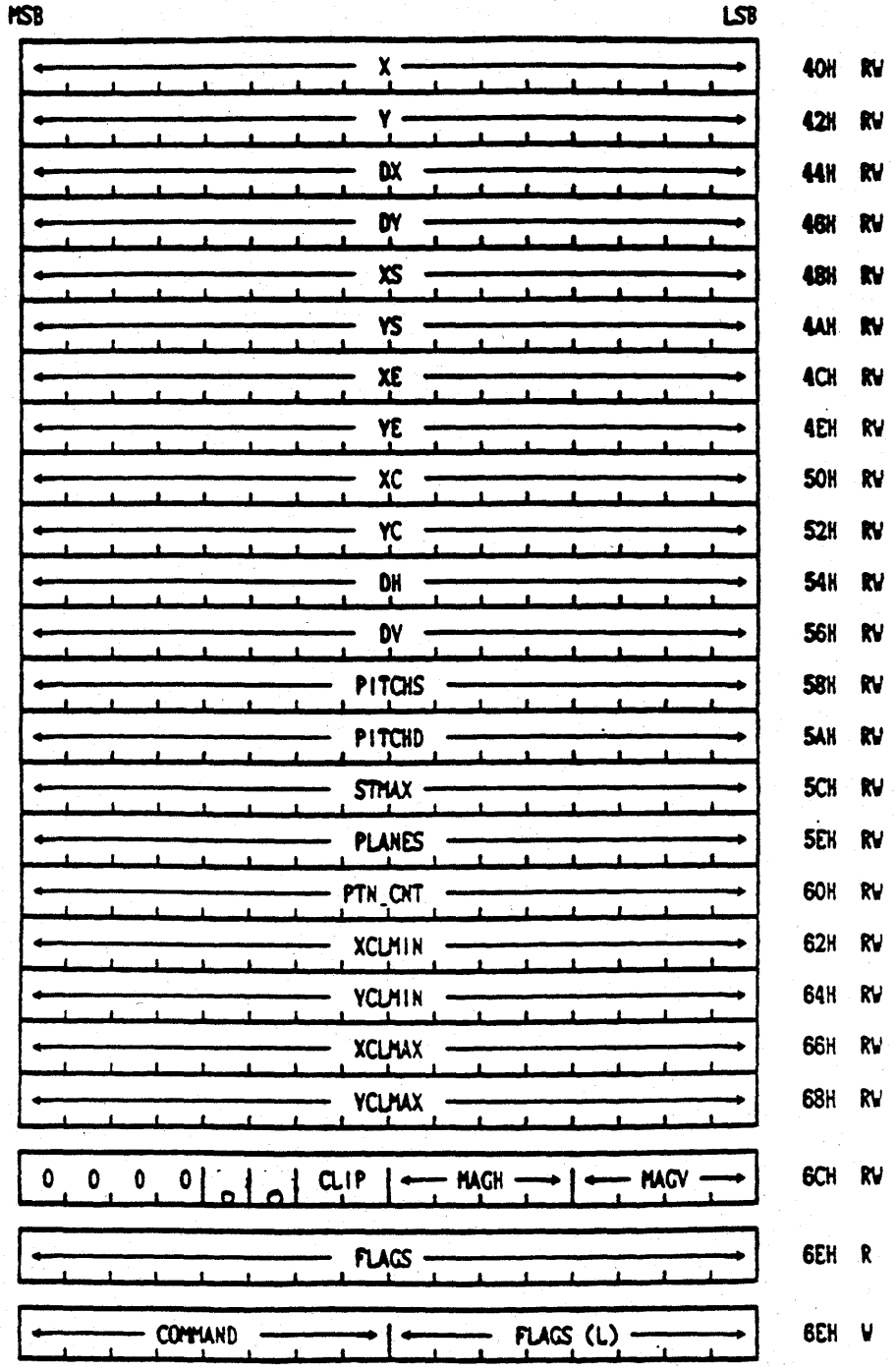
3.4 Internal Register Table



20H - 3BH : AGDC working registers

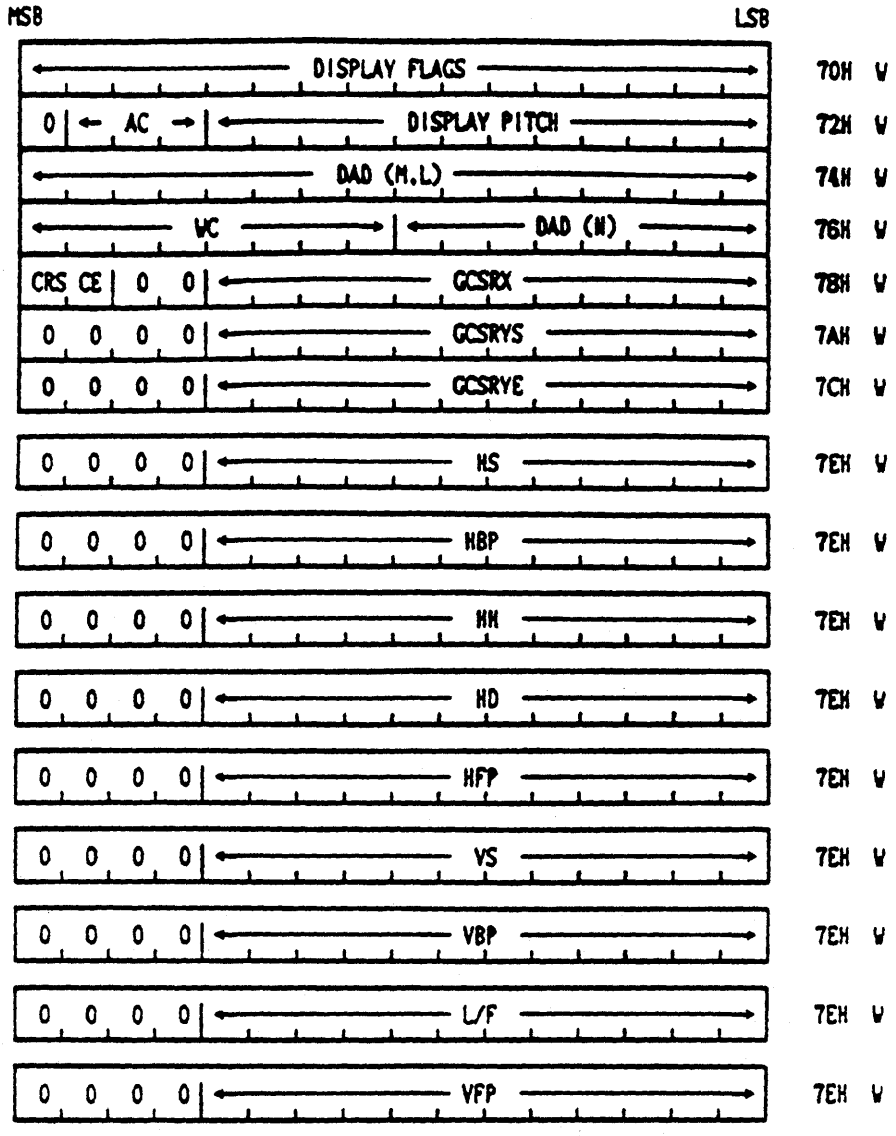


Internal Register Table (continued)



6AH - 6BH : AGDC working registers

Internal Register Table (continued)



RW : Read/Write
W : Write only
R : Read only

H: Higher 8 bits of 24-bit word
M: Middle 8 bits of 24-bit word
L: Lower 8 bits of 24-bit word

80H - FFH : Reserved

Section 4

Drawing Operations

4.1 Drawing Functions

The AGDC is an LSI device that can perform graphics drawing and copying at high speed. The host system specifies the drawing parameters and commands by writing to specific internal AGDC registers. Only the parameters that are needed to perform the drawing command are written. When the DRAW command is written, the AGDC starts the drawing process.

This section describes the variations of the DRAW command and the parameters required for each command.

4.2 Types of DRAW Commands

The DRAW command is set in the COMMAND register at address 6EH - 6FH. The type of drawing is selected according to the operation code written to 6FH. Various combinations are selected by the flags set in the register at 6EH.

The DRAW commands can roughly be classified as follows:

1. Data read command
2. Graphics drawing commands
   - Dot drawing
   - Straight line drawing
   - Curve drawing
3. Paint commands
   - Non-arbitrary area paint
   - Arbitrary area paint
4. Copy commands
   - Simple copy
   - 90° rotation copy
   - Arbitrary angle rotation copy
   - Enlarge/Shrink copy
5. PUT/GET commands
   - PUT
   - GET
   - 90° rotation GET

List of DRAW commands:

		Absolute Coordinate system	Relative Coordinate system
Data read commands	Coordinate value read	READ DP	
	Color information read	READ COL	
Graphics Drawing commands	Dot	DOT D A DOT M	R DOT M
	Straight Line	A LINE M0	R LINE M0
		A LINE M1	R LINE M1
		A LINE M2	R LINE M2
		A LINE D0	R LINE D0
		A LINE D1	R LINE D1
		A LINE D2	R LINE D2
		A LINE D3	
	Rectangle	A REC	R REC
	Circle	CRL	
	Arc	ARC	
	Sector	SEC	
	Circle Bow	CBOW	
	Ellipse	ELPS	
	Ellipse arc	EARC	
	Ellipse sector	ESEC	
	Ellipse bow	EBOW	
Paint Commands	Triangular area	A TRI FILL	
	Rectangular area	A REC FILL	R REC FILL
	Trapezoidal area	A TRA FILL	R TRA FILL
	Circular area	CRL FILL	
	Elliptic	ELPS FILL	
	Arbitrary enclosed area	PAINT	

List of DRAW commands (continued):

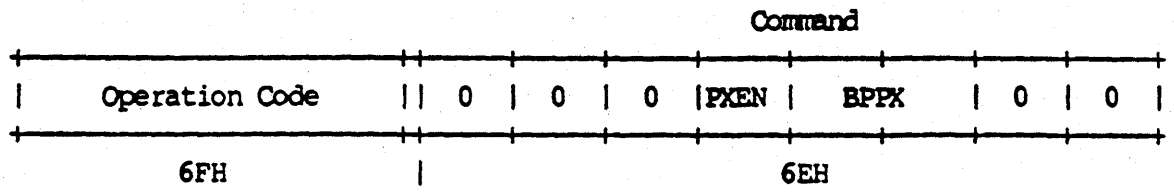
		Absolute Coordinate system	Relative Coordinate system
Copy Commands	Physical address-physical address	A COPY AA	
	Logical address-phsical address	A COPY CA	
	Physical address-logical address	A COPY AC	
	Logical address-logical address	A COPY CC	
PUT/GET Commands		PUT GET	

Summary of Operation Flags:

(1). Data read commands - there is no variation in these operation flags

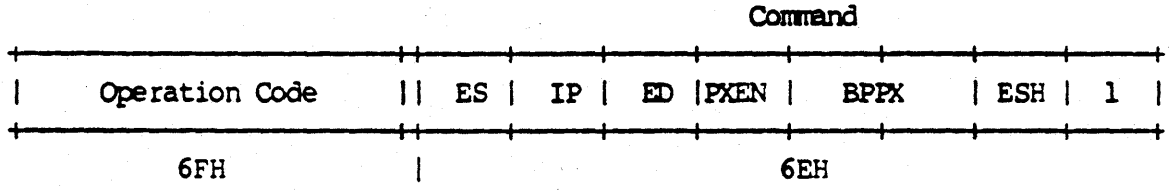
(2). Graphics drawing commands - the operation flags are shown in the figures below:

- Dot drawing commands



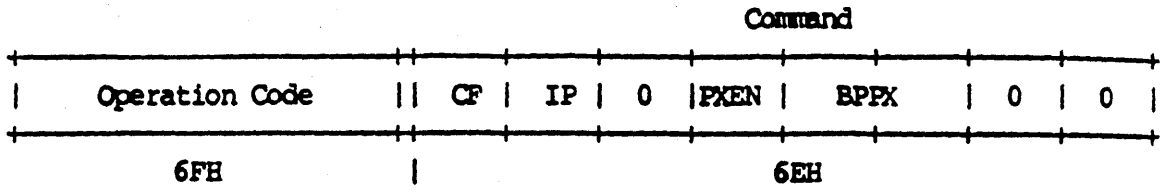
PXEN: Pixel mode specification
BPPX: No. of bits in one pixel

- Straight line drawing commands



ES: Enlarge/shrink or original size
IP: Specification of initialization of the type of line to be drawn
ED: Specification of thickening direction of line width in enlarge drawing
PXEN: Pixel mode specification
BPPX: Specification of the number of bits in one pixel
ESH: Enlarge or shrink specification (kind of line to be drawn)

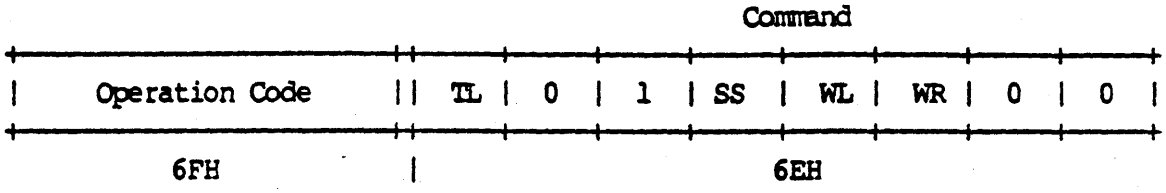
- Curve drawing commands



CF: Clockwise or counterclockwise drawing
IP: Specification of initialization of type of line to be drawn
PXEN: Pixel mode specification
BPPX: Specification of the number of bits in one pixel

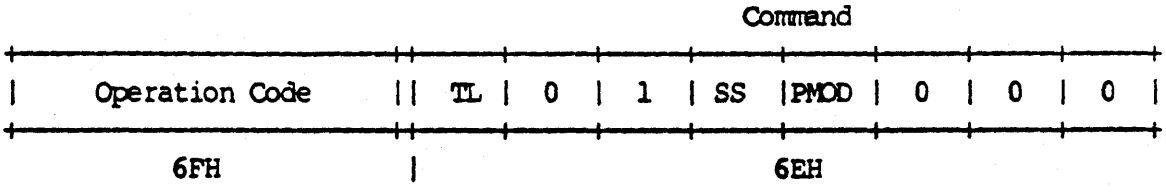
(3). Paint Commands - the operation flags are shown in the figures below:

- Non-arbitrary area paint commands



TL: Paint by tiling specification
SS: Color of monochromatic tiling specification
WL: Left boundary dot paint specification
WR: Right boundary dot paint specification

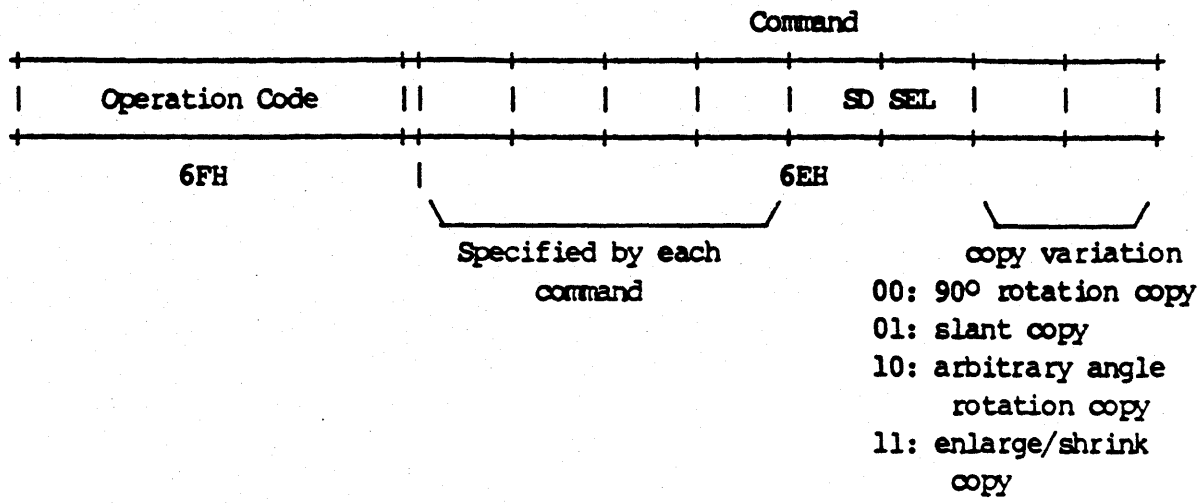
- Arbitrary area paint commands



TL: Paint by tiling specification
SS: Color or monochromatic specification
PMOD: Boundary color specification

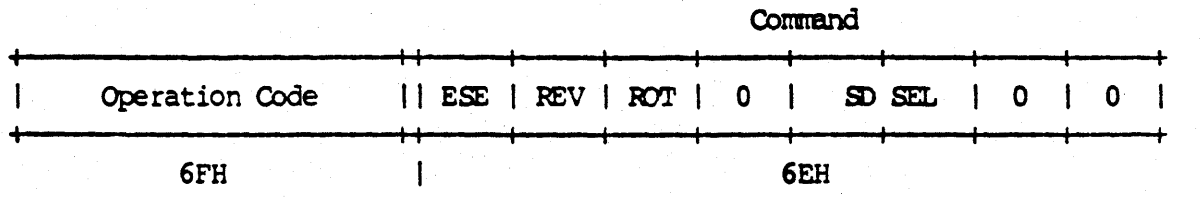
(4). Copy Commands - the operation flags are shown in following figures:

- General



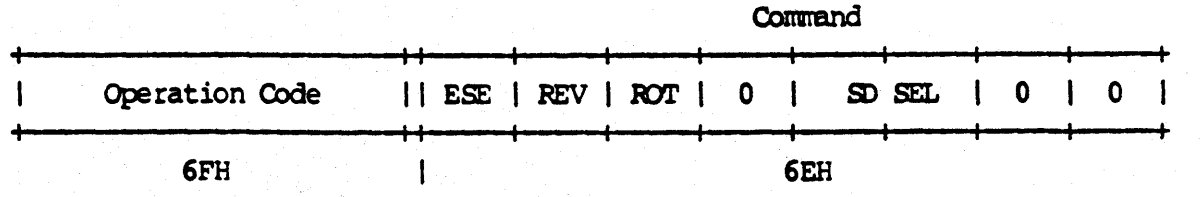
SD SEL: Copy plane specification

- Simple copy commands



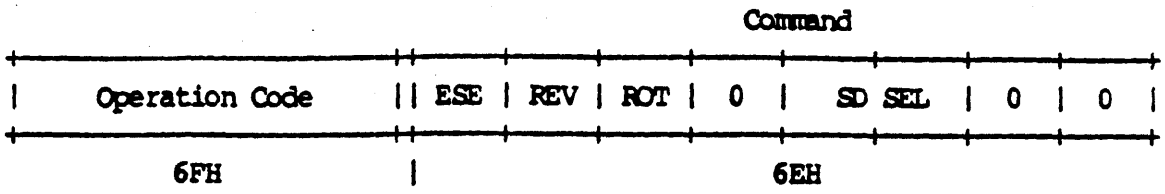
ESE: Source data reverse read specification
REV: Reverse specification
ROT: Rotation: 0 = no rotation; 1 = 180° rotation

- 90° Rotation Copy Commands



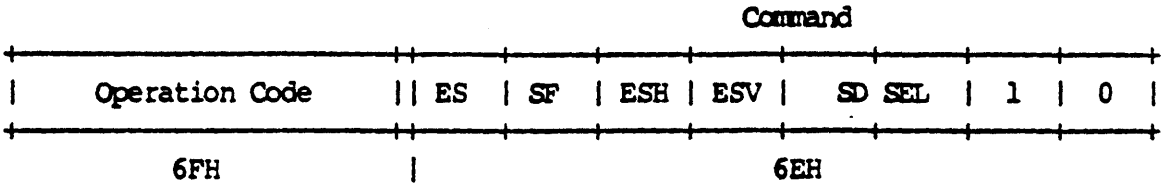
ESE: Source data reverse read specification
REV: Reverse specification
ROT: Rotation: 0 = 90° rotation; 1 = 270° rotation

- Slant Copy Commands



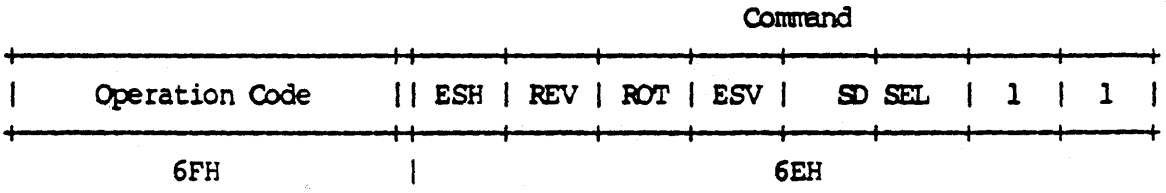
ESE: Source data reverse read specification
REV: Reverse specification
ROT: Rotation: 0 = no rotation; 1 = 180° rotation

- Arbitrary Angle Rotation Enlarge/Shrink Copy Commands



ES: Enlarge/shrink or original size specification
SF: Specification of a point not to be drawn
ESH: Enlarge/shrink specification in horizontal direction
ESV: Enlarge/shrink specification in vertical direction

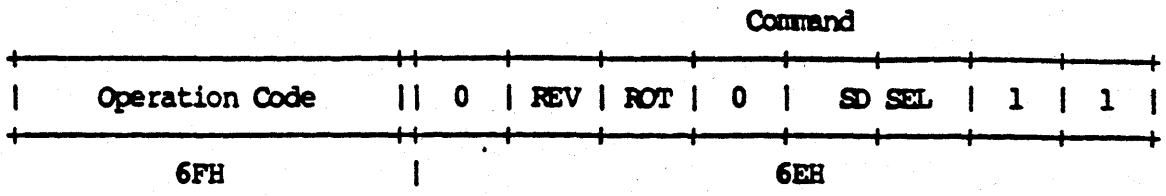
- Enlarge/Shrink Copy Commands



ESH: Enlarge/shrink specification in the horizontal direction
REV: Reversal specification
ROT: Rotation specificaton: 0 = no rotation; 1 = 180° rotation
ESV: Enlarge/shrink specification in the vertical direction

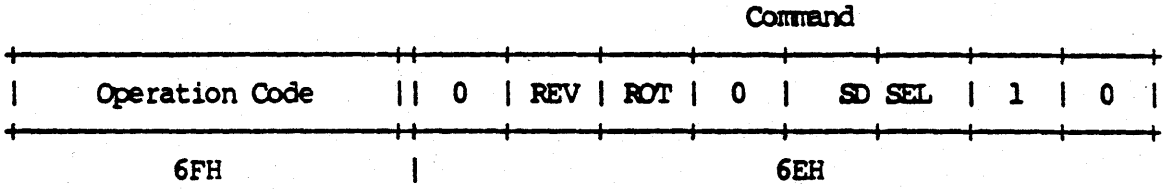
(5). PUT/GET Commands - the operation flags are shown in the following figures:

- PUT



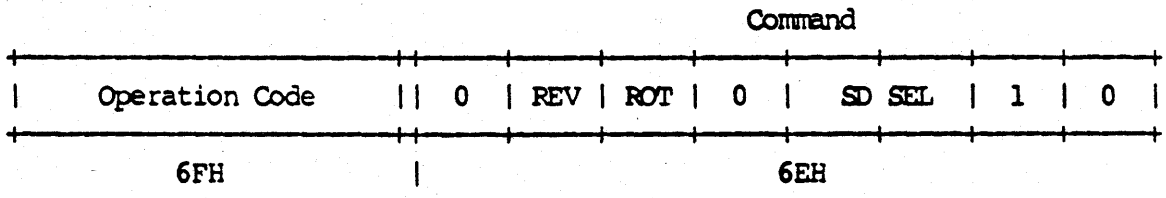
REV: Reversal specification
ROT: Rotation: 0 = no rotation; 1 = 180° rotation
SD SEL: Copy plane specification

- GET



REV: Reversal specification
ROT: Rotation: 0 = no rotation; 1 = 180° rotation
SD SEL: Copy plane specification

- 90° Rotation GET



REV: Reversal specification
ROT: Rotation: 0 = 90° rotation; 1 = 270° rotation
SD SEL: Copy plane specification

4.3 Detailed Description of DRAW Commands

4.3.1 Register Operation Commands

(1) READ DP (Read Drawing Pointer)

MSB								6FH								6EH								LSB
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0									

By this command, the drawing pointer (X#, Y#) held in the AGDC is read in the register (X, Y)

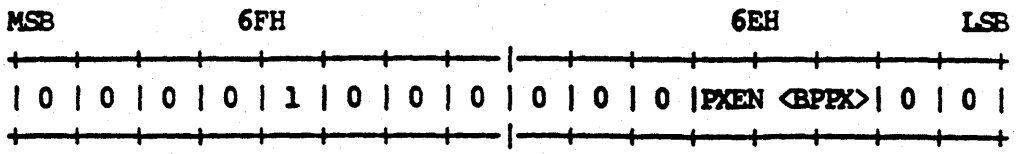
(2) READ COL (Read Color)

MSB								6FH								6EH								LSB
1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0									

By this command, the color information regarding the display memory location indicated by (X, Y) is read in the register

4.3.2 Graphics Drawing Commands

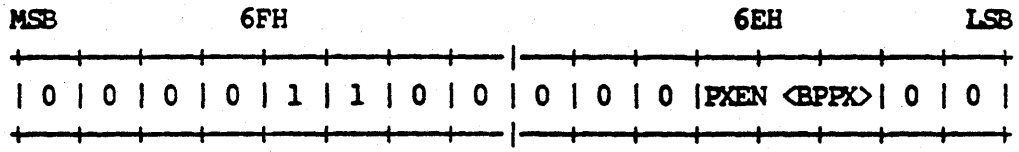
(1) DOT D (Dot Direct)



PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

One dot is drawn at the drawing pointer (X♯, Y♯) held in the AGDC. In this case, it is not necessary to set (X, Y) again.

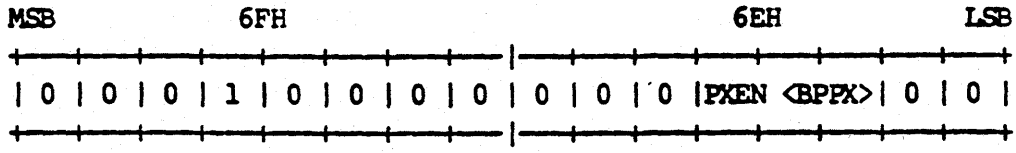
(2) A DOT M (Absolute Dot with Move)



PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

One dot is drawn at the coordinate indicated by (X, Y). The drawing pointer (X♯, Y♯) is converted into (X, Y). The dot which is enlarged by any magnification can be drawn by giving the horizontal magnification 'MAGH' and the vertical magnificaton 'MAGV'.

(3) R DOT M (Relative Dot with Move)



PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

One dot is drawn at the coordinate point (X+DX, Y+DY) generated by (X, Y) and (DX, DY). The drawing pointer (X♯, Y♯) changes to (X+DX, Y+DY).

(4) A LINE M0, A LINE M1, A LINE M2 (Absolute Line with Move 0, 1 or 2)

	MSB							6FH							6EH							LSB
A Line M0	0	0	0	1	0	1	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1
A Line M1	0	0	0	1	1	0	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1
A Line M2	0	0	0	1	1	1	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1

ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
ED: Specification of thickening direction of line width in enlarge drawing
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of a line to draw

A straight line is drawn from (X, Y) as the drawing start coordinates to the coordinates indicated by (XE, YE). However, the coordinates (XE, YE) are not drawn. The drawing pointer (X#, Y#) changes to (XE, YE).

A straight line can be enlarged/shrunk in the drawing direction and enlarged in thickness by giving the horizontal magnification 'MAGH', the vertical magnification 'MAGV' and the thickening parameters. The differences among these three commands are as follows:

A LINE M0: (X, Y) changes to (XE, YE)
A LINE M1: Both (X, Y) and (XS, YS) do not change
A LINE M2: (XS, YS) changes to (X, Y) and (X, Y) changes to (XE, YE)

(5) A LINE D0, A LINE D1, A LINE D2, A LINE D3 (Absolute Line Direct 0 - 3)

	MSB							6FH							6EH							LSB
A Line D0	0	0	1	0	0	0	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1					
A Line D1	0	0	1	0	0	1	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1					
A Line D2	0	0	1	0	1	0	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1					
A Line D3	0	0	1	0	1	1	0	0	ES	IP	ED	PXEN	<BPPX>			ESH	1					

ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
ED: Specification of thickening direction of line width in enlarge drawing
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of the line to draw

A straight line is drawn from (X, Y) as the drawing start coordinates to the coordinates indicated by (XE, YE). However, the coordinates (XE, YE) are not drawn. The drawing pointer (X*, Y*) changes to (XE, YE). It is not necessary to set (X, Y) again.

A straight line can be enlarged/shrunk in the drawing direction and enlarged in thickness by giving the horizontal magnification 'MAGH', the vertical magnification 'MAGV' and the thickening parameters. The differences among these four commands are as follows:

A LINE D0: (X, Y) changes to (XE, YE)
A LINE D1: Both (X, Y) and (XS, YS) do not change
A LINE D2: (XS, YS) changes to (X, Y) and (X, Y) changes to (XE, YE)
A LINE D3: The command is executed after changing (XE, YE) to (XS, YS). It is not necessary to set (XE, YE) again.

(6) R LINE M0, R LINE M1, R LINE M2 (Relative Line with Move 0 - 2)

	MSB							6FH							6EH	LSB
R Line M0	0	0	1	1	0	0	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	

	MSB							6FH							6EH	LSB
R Line M1	0	0	1	1	0	1	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	

	MSB							6FH							6EH	LSB
R Line M2	0	0	1	1	1	0	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	

ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
ED: Specification of thickening direction of line width in enlarge drawing
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of the line to draw

A straight line is drawn from (X, Y) as the drawing start point to the coordinates (X+DX, Y+DY) generated by (DX, DY). However, the coordinates (X+DX, Y+DY) are not drawn. The drawing pointer (X$, Y$) changes to (X+DX, Y+DY).

A straight line can be enlarged/shrunk in the drawing direction and enlarged in thickness by giving the horizontal magnification 'MAGH', the vertical magnification 'MAGV' and the thickening parameters.

The differences among these three commands are as follows:

R LINE M0: (X, Y) changes to (X+DX, Y+DY)
R LINE M1: Both (X, Y) and (XS, YS) do not change
R LINE M2: (XS, YS) changes to (X, Y) and (X, Y) changes to (X+DX, Y+DY)

(7) R LINE D0, R LINE D1, R LINE D2 (Relative Line Direct 0 - 2)

	MSB							6FH							6EH	LSB
R Line D0	0	0	1	1	1	1	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	
R Line D1	0	1	0	0	0	0	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	
R Line D2	0	1	0	0	0	1	0	0	ES	IP	ED	PXEN	<BPPX>	ESH	1	

ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
ED: Specification of thickening direction of line width in enlarge drawing
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of the line to draw

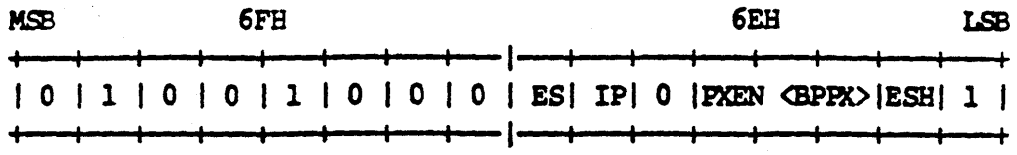
A straight line is drawn from (X, Y) as the drawing start point to the coordinate (X+DX, Y+DY). The point (X+DX, Y+DY) is not drawn. The drawing pointer (X#, Y#) changes to (X+DX, Y+DY). It is not necessary to set (X, Y) again.

A straight line can be enlarged/shrunk in the drawing direction and enlarged in thickness by giving the horizontal magnification 'MAGH', the vertical magnification 'MAGV' and the thickening parameters.

The differences among these three commands are as follows:

R LINE M0: (X, Y) changes to (X+DX, Y+DY)
R LINE M1: Both (X, Y) and (XS, YS) do not change
R LINE M2: (XS, YS) changes to (X, Y) and (X, Y) changes to (X+DX, Y+DY)

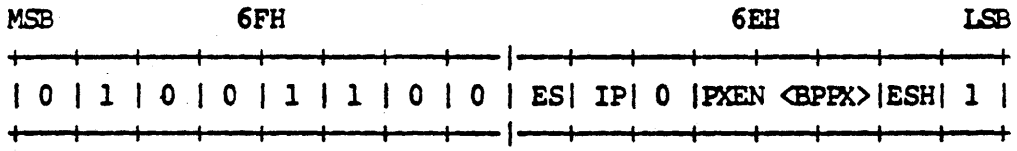
(8) A REC (Absolute Rectangle)



ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of the line to draw

A rectangle defined by (X, Y) as the drawing start coordinates and the diagonal coordinates (XS, YS) is drawn. A straight line enlarge/shrink in the drawing direction (by so doing, (XS, YS) does not change but the diagonal coordinates change) and enlarged in thickness can be drawn by giving the horizontal magnification 'MAGH' and the vertical magnification 'MAGV'.

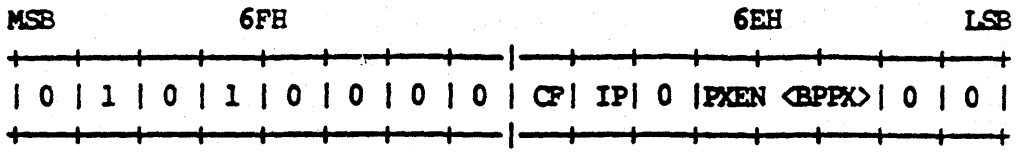
(9) R REC (Relative Rectangle)



ES: Original size or enlargement specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel
ESH: Specification of the thickness of the line to draw

A rectangle defined by (X, Y) as the drawing start coordinates and the diagonal coordinates (X+DX, Y+DY) generated by (DX, DY) is drawn. A rectangle enlarge/shrink in the drawing direction (by so doing, (X+DX, Y+DY) does not change, but the diagonal coordinates change) and enlarged in the thickness direction can be drawn by giving the horizontal magnification 'MAGH' and the vertical magnification 'MAGV'.

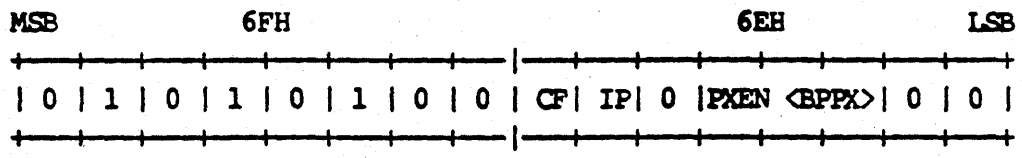
(10) CRL (Circle)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

A circle defined by the center coordinates (XC, YC) and the radius (DX) is drawn.

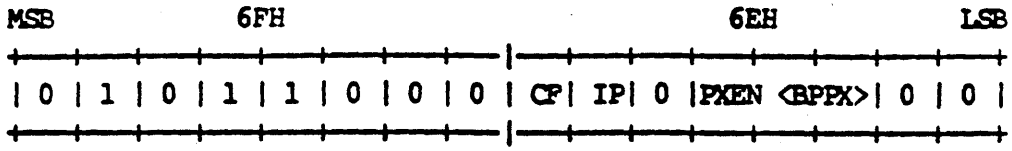
(11) ARC (Circle Arc)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

A circle arc defined by the center coordinates (XC, YC), the radius (DX), the drawing start coordinates (XS, YS) and the drawing end coordinates (XE, YE) is drawn.

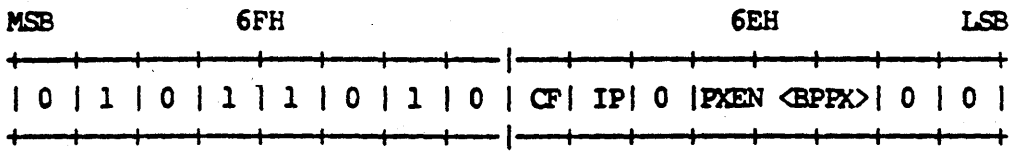
(12) CSEC (Circle Sector)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

A sector defined by the center coordinates (XC, YC), the radius (DX), the circle arc drawing start coordinates (XC, YC) and the circle arc drawing end coordinates (XE, YE) is drawn.

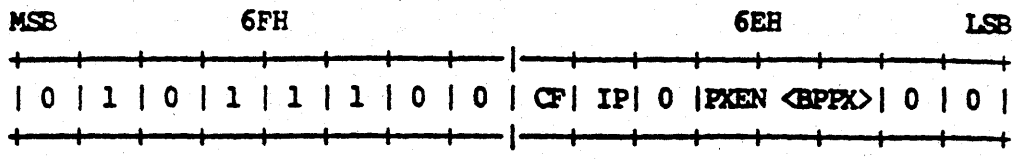
(13) CBOW (Circle Bow)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

A circle bow defined by the center coordinates (XC, YC), the radius (DX), the circle arc drawing start coordinates (XC, YC) and the circle arc drawing end coordinates (XE, YE) is drawn.

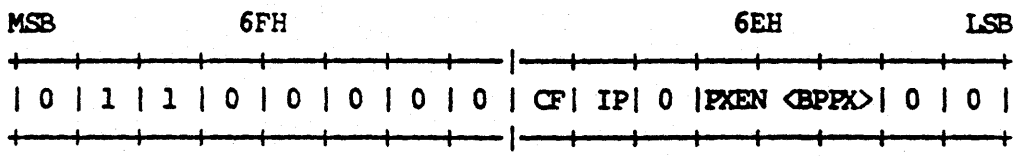
(14) ELPS (Ellipse)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the type of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

An ellipse defined by the center coordinates (XC, YC), the radius in the X axis direction (DX), the radius in the Y axis direction (DY), the square ration of the radius in the X axis and the square ratio of the radius in the Y axis direction is drawn (DH : DV = DX^2 : DY^2).

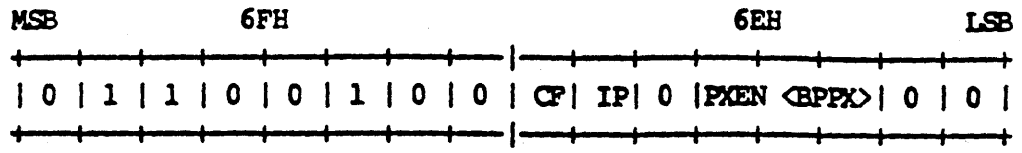
(15) EARC (Ellipse Arc)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the kind of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

An ellipse arc defined by the center coordinates (XC, YC), the radius in the X direction (DX), the radius in the Y direction (DY), the square ratio of the radius in the X axis (DH), the square ratio of the radius in the Y axis direction (DY), the drawing start coordinates (XS, YS) and the drawing end coordinates (XE, YE) is drawn (DH : DV = DX^2 : DY^2).

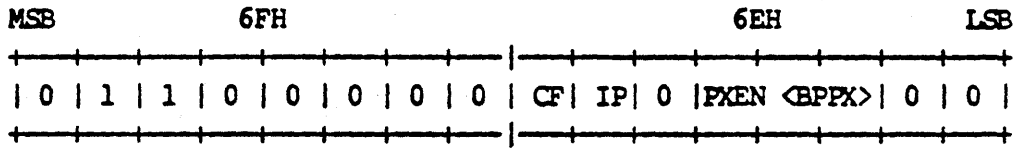
(16) ESEC (Ellipse Sector)



CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the kind of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

An ellipse sector defined by the center coordinates (XC, YC), the radius in the X axis direction (DX), the radius in the Y axis direction (DY), the square of the radius in the X axis direction (DH), the square of the radius in the Y axis direction (DV), the ellipse arc drawing start coordinates (XS, YS) and the ellipse arc drawing coordinates (XE, YE) is drawn ($DH : DV = DX^2 : DY^2$).

(17) EBOW (Ellipse Bow)

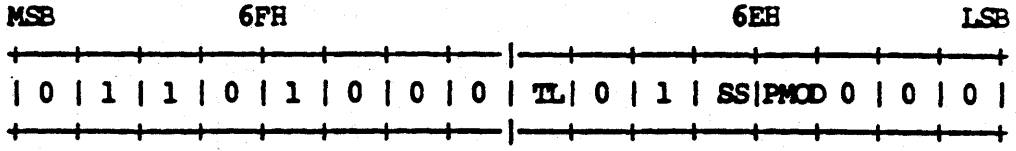


CF: Clockwise or counterclockwise drawing specification
IP: Initialization of the kind of line to draw
PXEN: Pixel mode specification
BPPX: Number of bits in one pixel

An ellipse bow defined by the center coordinates (XC, YC), the radius in the X direction (DX), the radius in the Y direction (DY), the square ratio of the radius in the X axis (DH), the square ratio of the radius in the Y axis direction (DY), the ellipse arc start coordinates (XS, YS) and the ellipse arc end coordinates (XE, YE) is drawn ($DH : DV = DX^2 : DY^2$).

4.3.3 Paint Commands

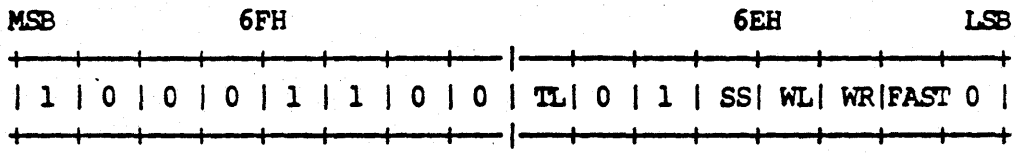
(1) PAINT (Arbitrary Paint within Enclosed Pattern)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
PMOD: Boundary color specification

An enclosed area between the boundary points is painted starting from the coordinates (X, Y). The boundary color is specified by DX (the DX specification is not required for painting with the color different from the boundary color).

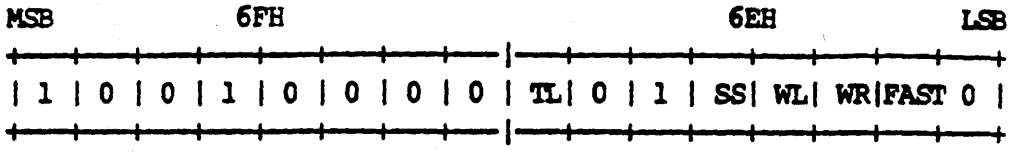
(2) A REC FILL (Absolute Rectangle Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge
FAST: Specification of normal or fast fill speed

A rectangle defined by the screen upper left coordinates (X, Y) as the drawing start coordinates and the screen lower right coordinates (XS, YS) as the diagonal coordinates is painted.

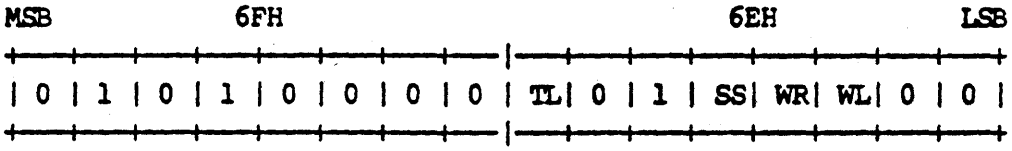
(3) R REC FILL (Relative Rectangle Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge
FAST: Specification of normal or fast fill speed

A rectangle defined by the screen upper left coordinates (X, Y) as the drawing start coordinates and the screen lower right coordinates generated by (DX, DY) as the diagonal coordinates (X+DX, Y+DY) is painted.

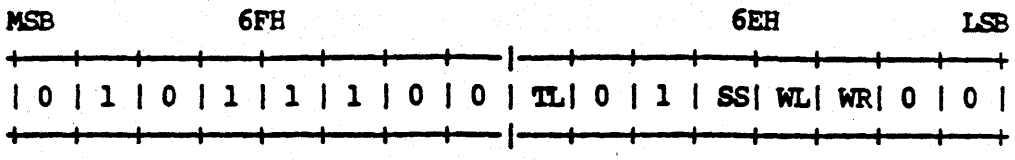
(4) CRL FILL (Circle Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge

A circle defined by the center coordinates (XC, YC) and the radius (DX) is painted.

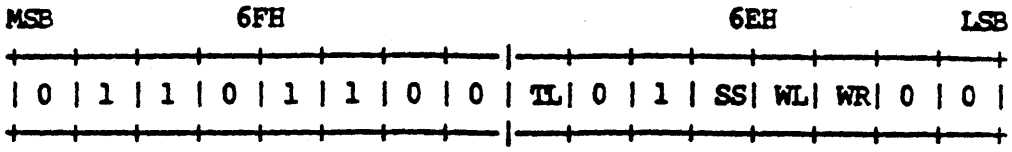
(5) ELPS FILL (Ellipse Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge

An ellipse defined by the center coordinates (XC, YC), the radius in the X axis direction (DX), the radius in the Y axis direction (DY), the square ratio of the radius in the X axis direction (DH) and the square ratio of the radius in the Y axis direction (DV) is painted ($DH : DV = DX^2 : DY^2$).

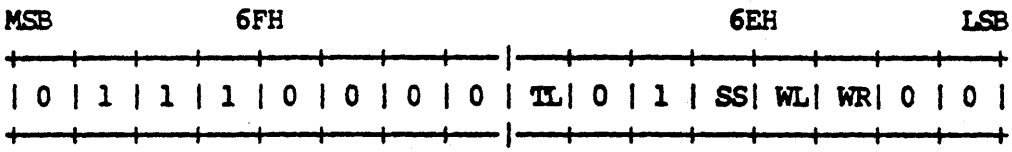
(6) A TRI FILL (Absolute Triangle Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge

A triangle defined by the three coordinates (X, Y), (XS, YS) and (XC, YC) is painted.

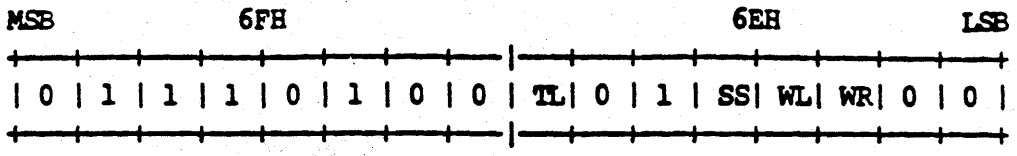
(7) A TRA FILL (Absolute Trapezoid Fill)



TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge

A trapezoid defined by 6 kinds of parameters showing four coordinates (X, Y), (XS, Y), (XC, YE) and (XE, YE) is painted.

(8) R TRA FILL (Relative Trapezoid Fill)

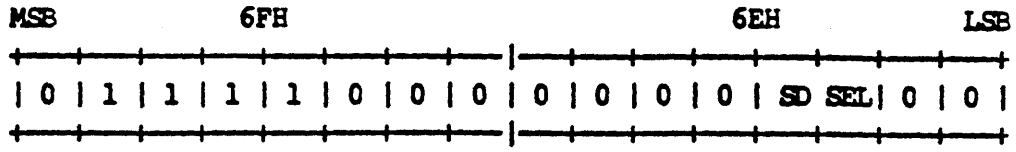


TL: Specification of painting by tiling
SS: Color or monochromatic tiling specification
WL: Specification of whether to paint on left edge
WR: Specification of whether to paint on right edge

A trapezoid defined by the screen upper left coordinates (X, Y), the screen upper right coordinates (XS, Y), the height (DY), the distance from the screen lower left point to the X axis (DX) and the distance from the screen lower right point to XS (XC) is painted.

4.3.4 COPY Commands

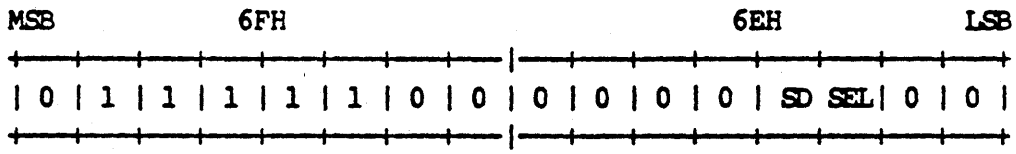
(1) A COPY AA (Absolute Copy Address to Address)



SD SEL: Transfer plane specfication

The data in a rectangular area defined by the address (EAD2) of the transfer start word of the display memory, the address (dAD2) of the transfer start dot in the word, the number of the dots in the horizontal direction 'DH' and the number of the dots in the vertical direction 'DV' is transferred to a rectangular area defined by the address (EAD1) of other transfer start word, the address 'dAD1' of the transfer start dot in the word, 'DH' and 'DV'.

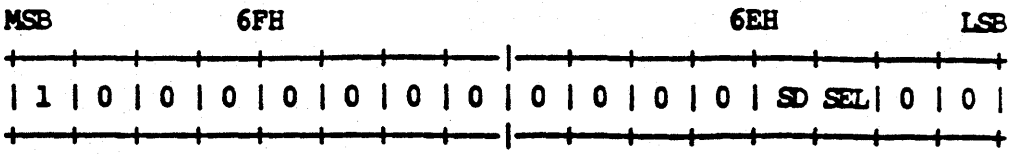
(2) A COPY CA (Absolute Copy Coordinate to Address)



SD SEL: Transfer plane specfication

The data in a rectangular area defined by the transfer start coordinates (XS, YS) on the display memory, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV' is transferred to another rectangular area defined by the address 'EAD1' of the transfer start word, the address 'dAD1' of the transfer start dot in the word, 'DH' and 'DV'.

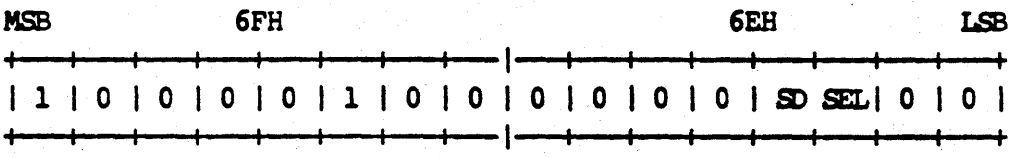
(3) A COPY AC (Absolute Copy Address to Coordinates)



SD SEL: Transfer plane specfication

The data in a rectangular area defined by the transfer start coordinates (XS, YS) in the display memory, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV' is transferred to a rectangular area defined by the other transfer start coordinates (X, Y), 'DH' and 'DV'.

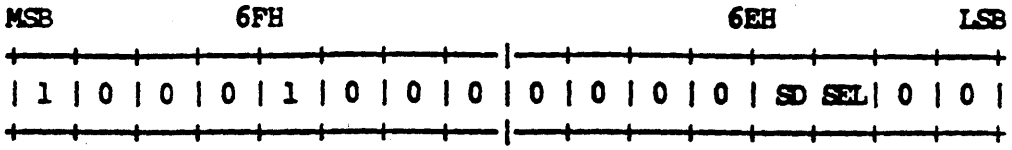
(4) A COPY CC (Absolute Copy Coordinate to Coordinate)



SD SEL: Transfer plane specfication

The data in a rectangular area defined by the transfer start coordinates (XS, YS) in the display memory, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV' is transferred to a rectangular area defined by the other transfer start coordinates (X, Y), 'DH' and 'DV'.

(5) R COPY CC (Relative Copy Coordinate to Coordinate)



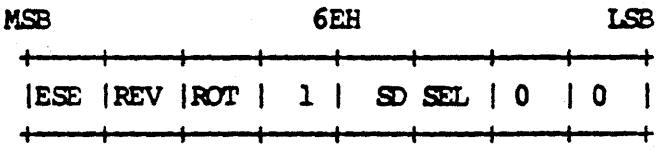
SD SEL: Transfer plane specfication

The data in a rectangular area defined by the transfer start coordinates (XS, YS) in the display memory, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV' is transferred to a rectangular area defined by the other start coordinates (XS+XC, YS+YC) generated by (XS, YS), (XC, YC), and 'DH' and 'DV'.

(6) Copy function extensions

The function of each COPY command can be extended by changing the lower 2 bits of the command code. This extension is defined in the lower byte (6EH) of the command register.

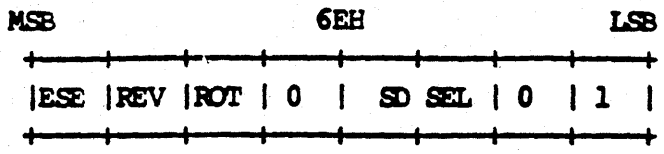
(a) 90° COPY (90° Rotation Copy)



ESE: Reverse data read specification
REV: Reversal specification
ROT: Rotation angle specification
SD SEL: Transfer plane specfication

The transfer area is rotated by 90°.

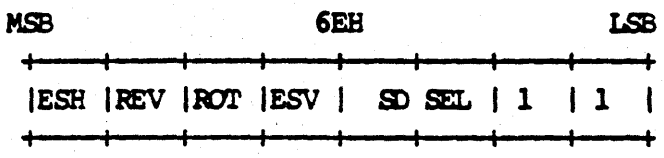
(b) SL COPY (Slant Copy)



ESE: Reverse data read specification
REV: Reversal specification
ROT: Rotation angle specification
SD SEL: Transfer plane specfication

The data in a rectangular area in the display memory is slanted by 'DX' in the X axis direction according to the change in the Y axis direction to transfer it into a parallogram area.

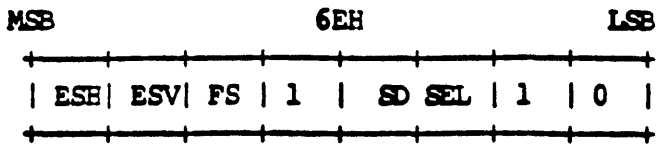
(c) ES COPY (Enlarge/Shrink Copy)



ESH: Enlarge/shrink specification (horizontal direction)
REV: Reversal specification
ROT: Rotation angle specification
ESV: Enlarge/shrink specification (vertical direction)
SD SEL: Transfer plane specfication

The transfer area is enlarged/shrunk by any magnification by giving the horizontal magnification 'MAGH' and the vertical magnification 'MAGV' factors.

(d) FR ES COPY (Free Angle Rotation Enlarge and Shrink Copy)

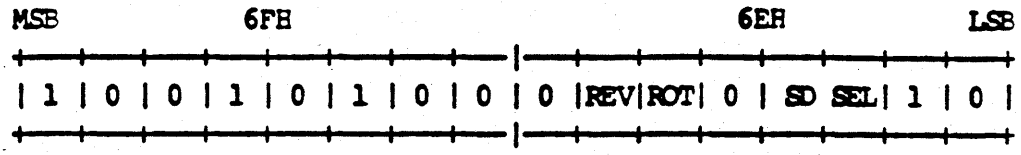


ESH: Enlarge/shrink specification in horizontal direction
ESV: Enlarge/shrink specification in vertical direction
SF: Specification of point not to be drawn
SD SEL: Transfer plane specfication

The transfer area is rotated by any angle are enlarged/shrunk by giving the horizontal magnification 'MAGH', the vertical magnification 'MAGV', and the angle defined by DX and DY.

4.3.5 PUT/GET Commands

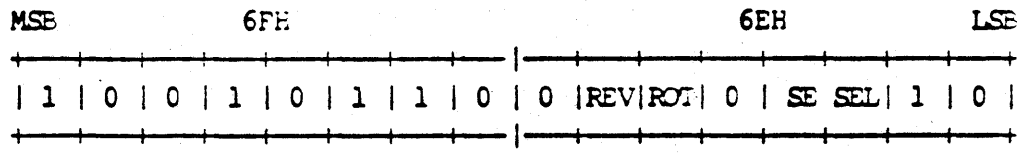
(1) PUT A (Put Data to Address Field)



REV: Reversal Specification
ROT: Rotation Specification
SD SEL: Transfer plane specfication

The data from the host system is transferred to a rectangular area defined by the address 'EAD1' of the transfer start word in the display memory, the address 'dAD1' of the transfer start dot in the word, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV'.

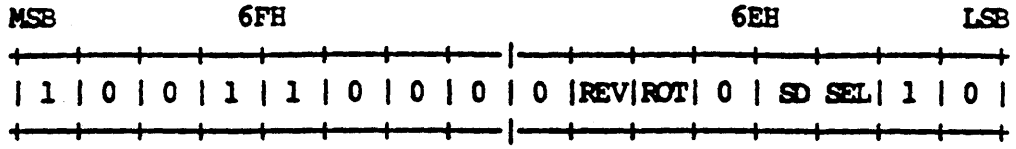
(2) PUT C (Put Data to Coordinate Field)



REV: Reversal Specification
ROT: Rotation Specification
SD SEL: Transfer plane specfication

The data from the host system is transferred to a rectangular area defined by the transfer start coordinates (X, Y) of the display memory, the number of dots in the horizontal directions 'DH' and the number of dots in the vertical direction 'DV'.

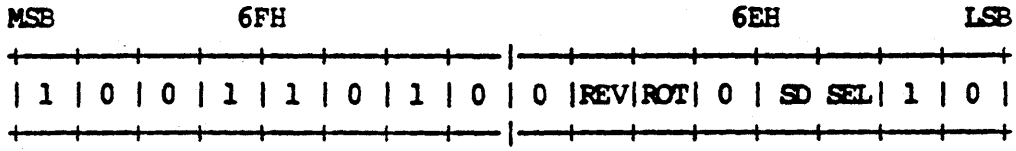
(3) GET A (Get Data from Address Field)



REV: Reversal Specification
ROT: Rotation Specification
SD SEL: Transfer plane specfication

The data from the host system is transferred to a rectangular area defined by the address 'EAD1' of the transfer start word in the display memory, the address 'dAD1' of the transfer start dot in the word, the number of dots in the horizontal direction 'DH' and the number of dots in the vertical direction 'DV'.

(4) GET C (Get Data from Coordinate Field)



REV: Reversal Specification
ROT: Rotation Specification
SD SEL: Transfer plane specfication

The data from the display memory is transferred to the host system from a rectangular area defined by the transfer start coordinates (X, Y) of the display memory, the number of dots in the horizontal directions 'DH' and the number of dots in the vertical direction 'DV'.

4.4 How to Use the Flag Bits

(1) PXEN: Pixel Drawing Enable
(2) BPPX: Bits per Pixel

Sixteen pixels are assigned to one 16-bit word in the display memory controlled by the AGDC principally to construct the plane configuration. The number of bits per pixel can easily be extended by increasing the number of planes in the display memory. In the packed configuration, in which each pixel is assigned to one word, straight lines, rectangles, circles, circle arcs, circle bows, arc sectors, ellipses, ellipse arcs, ellipse bows and ellipse arc sectors can still be drawn.

The plane or the pixel configuration is selected by PXEN and the number of bits in one pixel is defined by BPPX.

BPPX	PXEN	N bits/pixel
XX	0	1
00	1	2
01	1	4
10	1	8
11	1	16

(3) ES: Enlarge/Shrink
(4) ESH: Enlarge/Shrink Horizontal
(5) ESV: Enlarge/Shrink Vertical

Whether or not the enlarge/shrink function by any magnification (16/N or N/16, N an integer between 1 and 16) is enabled is determined by ES. The enlarge/shrink in the horizontal direction is selected by ESH. The enlarge/shrink in the vertical direction is selected by ESV. The horizontal magnification and the vertical magnification are set by the MAGH and MAGV registers, respectively.

ES	ESH	ESV	Function
0	X	X	No enlarge/shrink
1	0	X	Horizontal shrink
1	1	X	Horizontal enlarge
1	X	0	Vertical shrink
1	X	1	Vertical enlarge

ESH = 0

MAGH	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Magnification	1/16	2/16	3/16	4/16	5/16	6/16	7/16	8/16	9/16	10/16	11/16	12/16	13/16	14/16	15/16	16/16

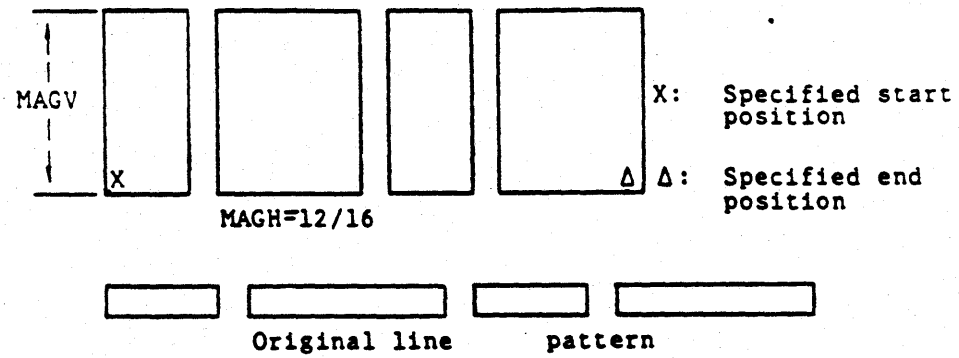
ESH = 1

MAGH	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Magnification	16/16	16/15	16/14	16/13	16/12	16/11	16/10	16/9	16/8	16/7	16/6	16/5	16/4	16/3	16/2	16/1

ESV = 0															
MAGV	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Magnification	1/16	2/16	3/16	4/16	5/16	6/16	7/16	8/16	9/16	10/16	11/16	12/16	13/16	14/16	15/16	16/16

ESV = 1																
MAGV	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Magnification	16/16	16/15	16/14	16/13	16/12	16/11	16/10	16/9	16/8	16/7	16/6	16/5	16/4	16/3	16/2	16/1

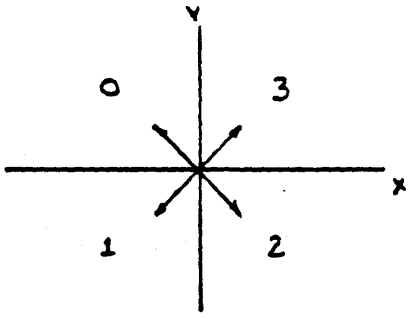
When enlarging straight lines or rectangles, the enlarge/shrink magnification of 16/N or N/16 of the line pattern is defined by MAGH. The integral magnification of the line width is defined by MAGV.



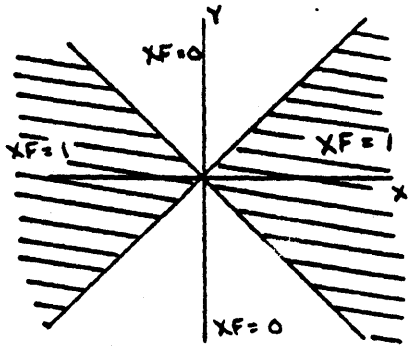
(6) ED: Enlargement Direction

ED selects the widening direction of a straight line drawing, as shown in the following table:

SP	0	1	2	3
XF	0	1	0	1	0	1	0	1
ED								
0	+X	+Y	-X	+Y	-X	-Y	+X	-Y
1	-X	-Y	+X	-Y	+X	+Y	-X	+Y



SP Quadrant Definition



XF Quadrant Definition

(7) IP: Initial Pattern Pointer

This bit selects the initialization/non-initialization of the pointer which specifies the drawing of a specific bit in the register storing the type of line (dotted, alternate long and short dashed, etc). In the case of drawing a folded line graph, etc., an alternate long and short dashed line is still drawn after passing the end point if this pointer is not initialized.

IP	Function
0	The pattern pointer is not initialized
1	The pattern pointer is initialized

(8) CF: Clockwise Flag

This bit selects the drawing direction of a circle, ellipse, etc.

CF	Drawing direction
0	Counterclockwise
1	Clockwise

(9) TL: Tiling Pattern
(10) SS: Single Source Pattern

This bit selects the pattern in painting. The following three selections are possible:

TL	SS	Selection
0	0	Not used
0	1	The same pattern set in the 'PTNCNT' register referred to for all the planes
1	0	The pattern stored in the display memory is read each time for each plane referred to it
1	1	The same pattern stored in the display memory is referred to for all the planes

To clear all the planes to '0', set TL = 0 and SS = 1, then it is not necessary to frequently read the pattern to be painted. This will allow the planes to be cleared quicker. When it is necessary to paint with a different color for each bit, set TL = 1 and SS = 0.

(11) **PMOD: Paint Mode**

This bit selects one of the two types of arbitrary enclosed areas shown in the following table:

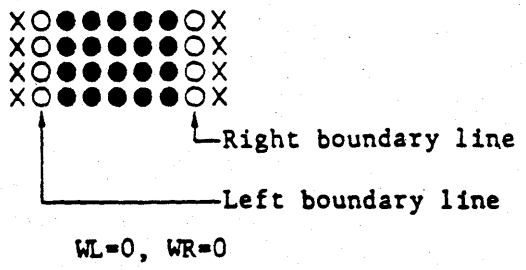
PMOD	Type of area
0	The boundary color is retrieved according to the type of boundary color preliminarily given and the space between the boundary points is painted
1	The color information at the start point of the boundary point retrieval. The boundary point is retrieved for all the colors other than the color of the boundary and the space between the boundary points is painted

(12) WL: Write Left
(13) WR: Write Right

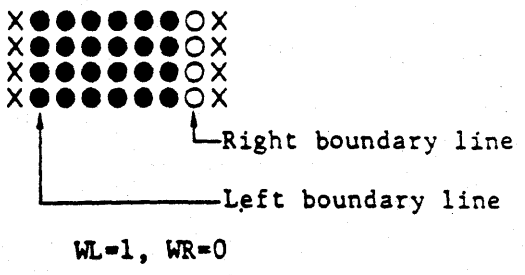
These bits specify the drawing of points on the boundary line in a quadrangle, circle, ellipse, triangle and trapezoid fill.

WL	Function
0	The points on the left boundary line are not painted
1	The points on the left boundary line are also painted

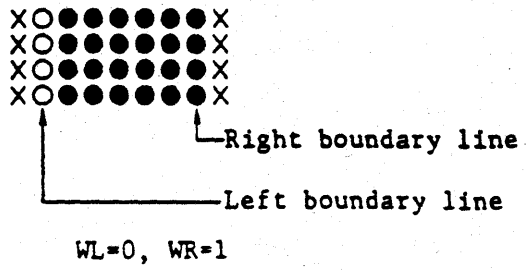
WR	Function
0	The points on the right boundary line are not painted
1	The points on the right boundary line are also painted



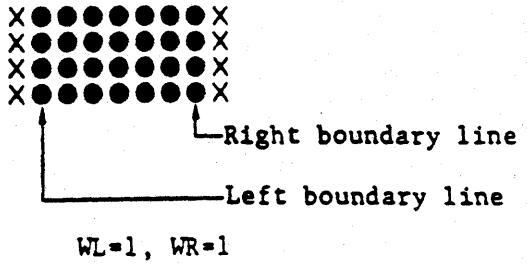
WL=0, WR=0



WL=1, WR=0



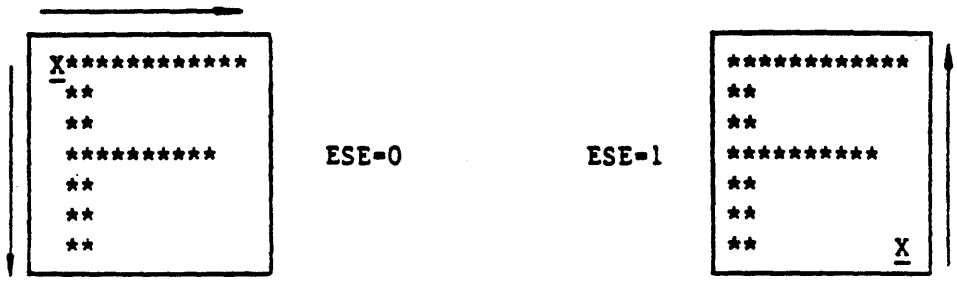
WL=0, WR=1



WL=1, WR=1

(14) ESE: Exchange Start with End

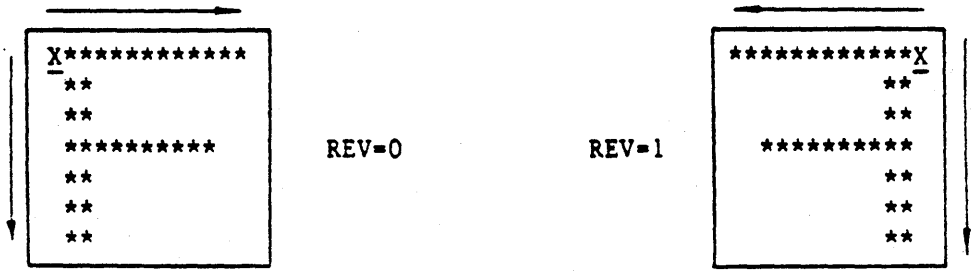
This bit defines the reading order of the source data in the copy operation.



X : Reading start point

(15) REV: Reverse

This bit defines the use of the reverse drawing in the copy operation.

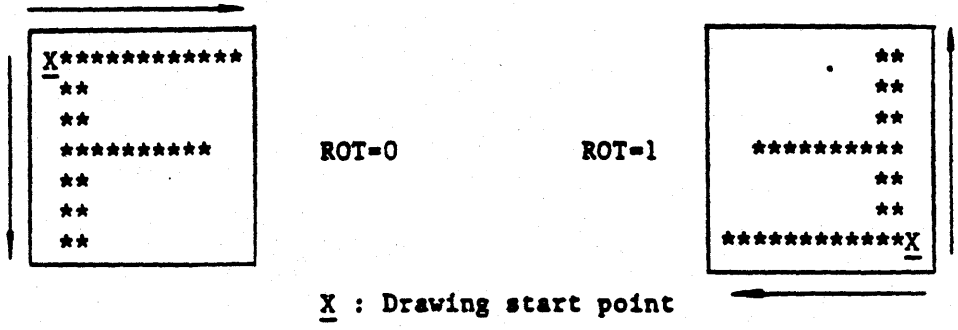


X : Drawing start point

--

(16) ROT: Rotation

This bit defines the use of the 180o rotation drawing in the copy operation.



X : Drawing start point

(17) SD SEL: Source Destination Mode Select

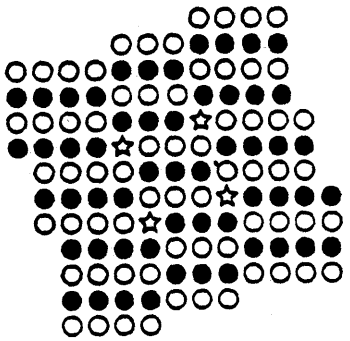
This bit selects the data transfer mode between the planes as shown in the table below (please refer to the section on inter-plane data transfer):

SD SEL	Function
00	Single source and destination
01	Multiple sources
10	Multiple destinations
11	Multiple sources and destinations

(18) FS: Fill Shortage

When the coordinate conversion is made during the arbitrary angle rotation copy, some points may not be drawn. This bit specifies whether to draw these points or not.

FS	Function
0	Points drawn
1	Points not drawn



☆ : The points

(19) PUT: Put

This bit specifies the transfer by the PUT command or transfer by the GET command.

PUT	Function
0	Transfer by GET
1	Transfer by PUT

(20) FAST: Fast

This bit specifies the normal or fast mode for drawing.

FAST	Function
0	Normal speed
1	Fast speed

However, the FAST mode cannot be used for all drawing operations:

REC FILL: The FAST mode cannot be used if clipping or painting with a tiling pattern. It can only be used for replacing data.

COPY: The FAST mode can be used only for ordinary COPY with replace. It cannot be used with other COPY operations or with multiple sources.

4.5 Painting Pattern Reference Examples

(1) TL = 0, SS = 1

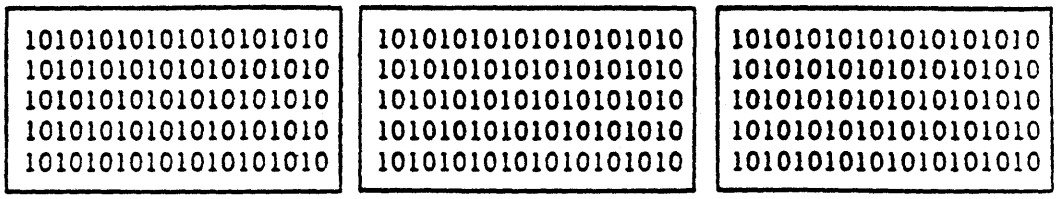
In this case, the contents of the 16-bit register, PTNCNT, in the AGDC is referred to as the painting pattern. When painting two or more planes is specified, painting is made in the same pattern.

Parameters to be set:

(A) Plane to be selected in drawing ...	PLANES
(B) Maximum number of planes to be selected in drawing ...	PMAX
(C) Painting pattern to be referred to ...	PTNCNT

Drawing Example:

PLANES = 7, PMAX = 4, PTNCNT = 5555H



(2) TL = 1, SS = 1

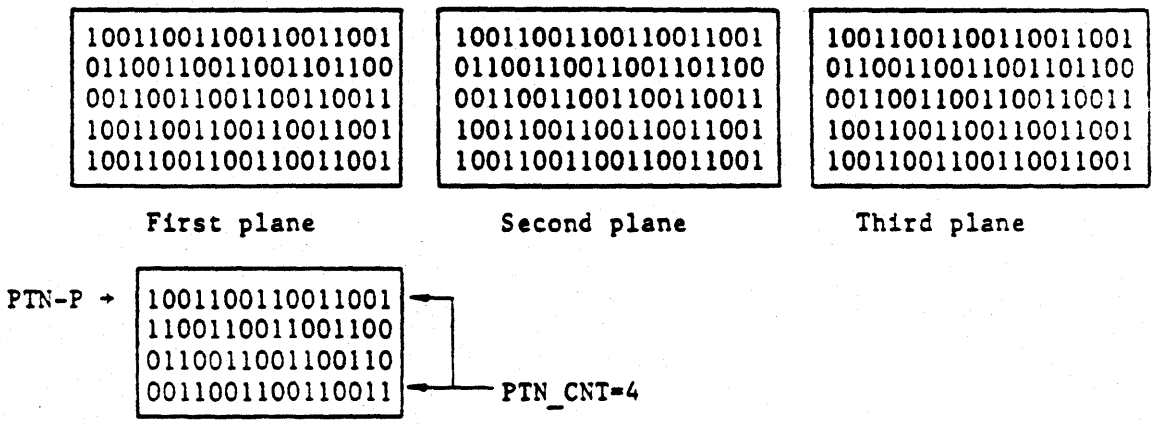
In this case, multiple painting patterns previously stored in the display memory are referred to. The painting pattern is automatically updated according to the move of the Y coordinate. When painting covering two or more planes is specified and when the Y coordinates are the same, the same pattern is referred to.

Parameters to be set:

(A) Plane to be selected in drawing ...	PLANES
(B) Maximum number of planes to be selected in drawing ...	PMAX
(C) The first address of the display memory containing the pattern ...	PTNP
(D) The number of words to be repeated for the painting pattern ...	PTNCNT

Drawing Example:

PLANES = 7, PMAX = 4, PTNCNT = 4



(3) TL = 1, SS = 0

The multiple painting patterns previously stored in the display memory are referred to. The painting pattern is automatically updated according to the move of the Y coordinate. When painting covering two or more planes is specified, the painting pattern corresponding to each plane is referred to.

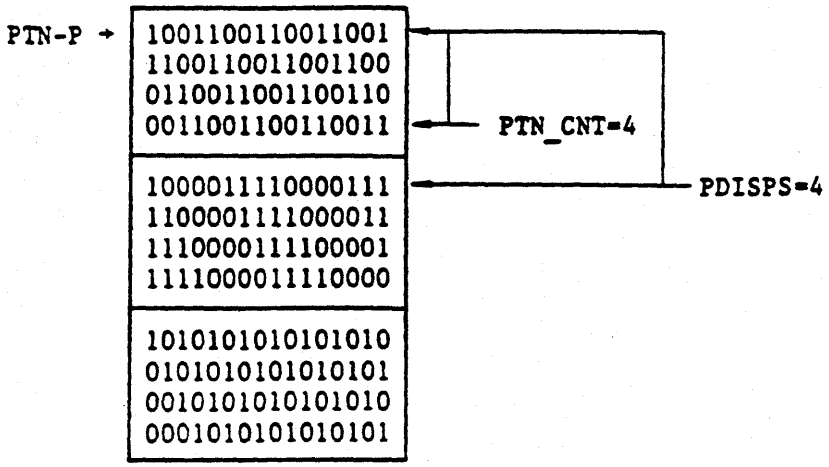
Parameters to be set:

(A) Plane to be selected in drawing ...	PLANES
(B) Maximum number of planes to be selected in drawing ...	PMAX
(C) The first address of the display memory containing the pattern ...	PTNP
(D) The number of words to be repeated for the painting pattern ...	PTNCNT
(E) The address displacement between the painting pattern prepared for each plane ...	PDISPS

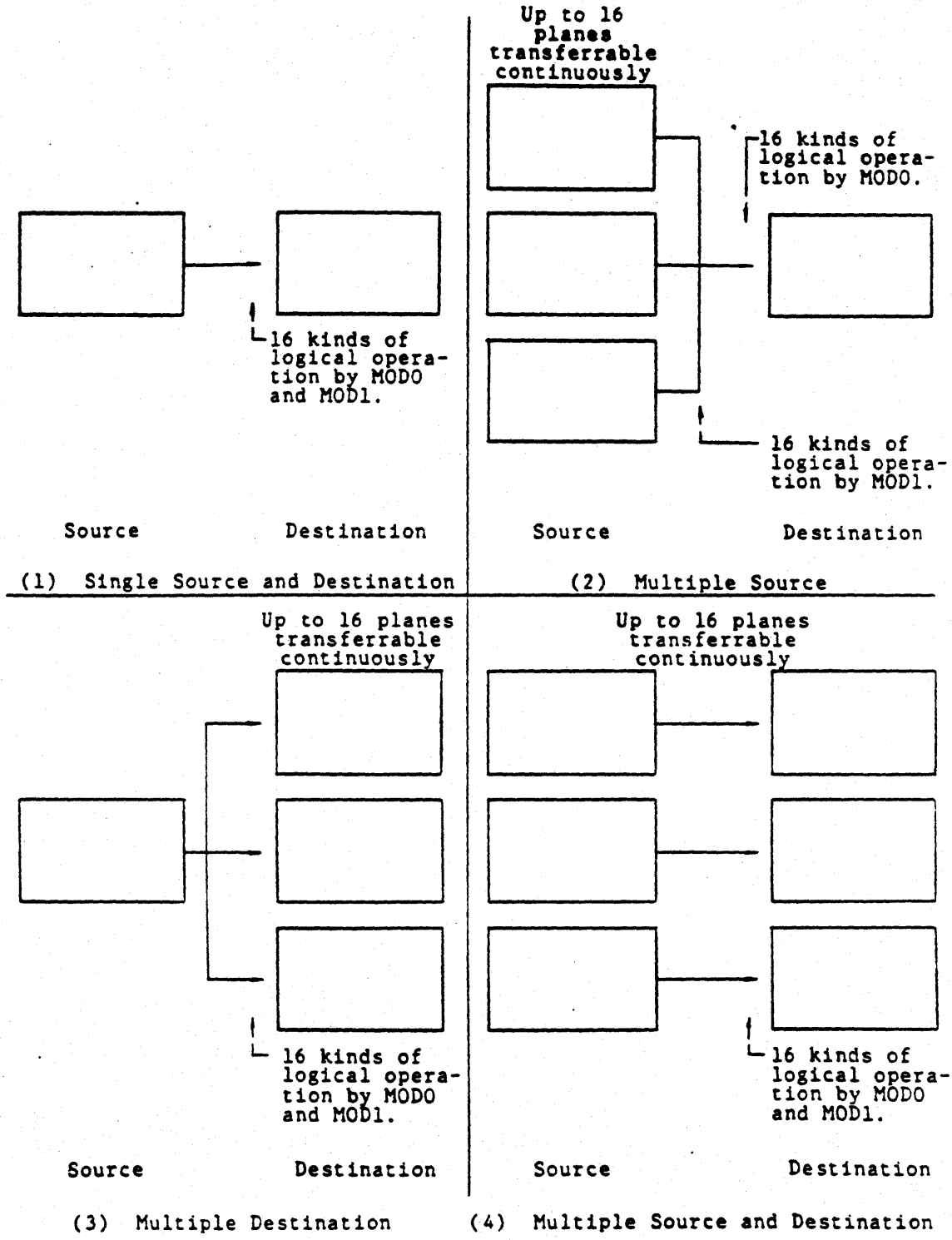
Drawing Examples:

PLANES = 7, PMAX = 4, PTNCNT = 4, PDISPS = 4

First plane	Second plane	Third plane
1001100110011001100 1100110011001100110 0110011001100110011 0011001100110011001 1001100110011001100	1000011110000111100 1100001111000011110 1110000111100001111 1111000011110000111 1000011110000111100	1010101010101010101 0101010101010101010 0010101010100010100 0001010101010001010 1010101010101010101



4.6 Inter-plane Data Transfers



4.7 Drawing Related Registers

The internal registers in which the parameters required for drawing are stored are described in this section.

(1) **EADORG** (Execution Address Origin)

No. of Bits: 24
Address: 00H - 02H
Application: This register sets the physical address (effective address) in the display memory corresponding to the origin (0,0) on the logical plane (the X-Y coordinate plane).

(2) **dADORG** (Dot Address Origin)

No. of Bits: 4
Address: 03H
Application: This register sets the dot position in the physical address (effective address) in the display memory corresponding to the origin (0,0) on the logical plane (the X-Y coordinate plane).

(3) **EAD1** (Execution Address 1)

No. of Bits: 24
Address: 04H - 06H
Application: This register sets the drawing start physical address value in the drawing processing when the drawing start position is given by the physical address (effective address).

(4) **dAD1** (Dot Address 1)

No. of Bits: 4
Address: 07H
Application: This register sets the dot position in the display memory when the drawing start position is given by the physical address (effective address).

(5) **EAD2** (Execution Address 2)

No. of Bits: 24
Address: 08H - 0AH
Application: This register sets the drawing start physical address in the drawing processor when the drawing start position is given by the physical address (effective address).

(6) **dAD2** (Dot Address 2)

No. of Bits: 4
Address: 0BH
Application: This register sets the dot position in the display memory when the drawing start position is given by the physical address (effective address).

(7) **PDISPS** (Plane Displacement Source)

No. of Bits: 24
Address: 0CH - 0EH
Application: This register sets the number of words which occupy one memory plane in the case of display memory configured with two or more planes. In the case of execution of the COPY command, the number of words per source plane is set. In the case of execution of the PAINT command, the number of words per plane containing the painting pattern (tiling pattern) is set.

(8) **PDISPD** (Plane Displacement Destination)

No. of Bits: 24
Address: 10H - 12H
Application: This register sets the number of words which occupy one memory plane in the case of display memory configured with two or more planes. In the case of execution of drawing commands, the number of words per plane for graphics drawing is set. In the case of execution of COPY commands, the number of words per destination plane is set. In the case of execution of painting commands, the number of words per painting plane is set.

(9) **PMAX** (Plane Maximum)

No. of Bits: 16
Address: 14H - 15H
Application: This register sets selects the number of planes (up to 16) in the display memory to be drawn, as shown in the following table:

PMAX	Plane to be drawn
0000 0000 0000 0001	Until 1st plane
0000 0000 0000 0010	Until 2nd plane
0000 0000 0000 0100	Until 3rd plane
.	.
.	.
.	.
0100 0000 0000 0000	Until 15th plane
1000 0000 0000 0000	Until 16th plane

(10) **MOD0** (Drawing Mode 0)

No. of Bits: 4
Address: 16H
Application: This registers defines the type of logical operation performed during drawing processing. When the bit in PLANES corresponding to the memory plane is 0 during drawing processing, the logical operation defined by MOD0 is executed.

(11) **MOD1** (Drawing Mode 1)

No. of Bits: 4
Address: 16H
Application: This registers defines the type of logical operation performed during drawing processing. When the bit in PLANES corresponding to the memory plane is 1 during drawing processing, the logical operation defined by MOD0 is executed.

(12) **PTNP** (Pattern Pointer)

No. of Bits: 24
Address: 18H - 1AH
Application: This registers sets the first physical address in the display memory area containing the painting (tiling) pattern.

(13) **STACK** (Stack Pointer)

No. of Bits: 24
Address: 1CH - 1EH
Application: This registers sets the first physical address in the display memory area to save data such as coordinates, etc., during the retrieval of the boundary point in the arbitrary enclosed area painting. It may be considered as the working area of the AGDC in the execution of the PAINT command.

(14) **X, Y, DX, DY, XS, YS, XE, YE, XC, YC, DH, DV**

No. of Bits: 16 each
Address: 40H - 57H, respectively
Application: This is the group of registers used to set the parameters required for the execution of various drawing commands. However, the DX registers is also used as the data port to output data read by the AGDC during execution of the READ COL command.

(15) **PITCHS** (Pitch Source)

No. of Bits: 16
Address: 58H - 59H
Application: This register sets the number of addresses in the horizontal direction of the source plane in the display memory during execution of the COPY command.

(16) **PITCHD** (Pitch Destination)

No. of Bits: 16
Address: 5AH - 5BH
Application: This registers set the number of addresses in the horizontal direction of the drawing plane in the display memory during execution of paint commands.

(17) **STMAX** (Store Maximum)

No. of Bits: 16
Address: 5CH - 5DH
Application: This register set the size of the display memory area used to save data such as coordinates, etc., during retrieval of the boundary point in the arbitrary enclosed area painting. It may be considered as the working area size of the AGDC during execution of the PAINT command.

(18) **PLANES** (Plane Select)

No. of Bits: 16
Address: 5EH - 5FH
Application: This register selects the type of logical operation in the drawing processing. Each bit in the PLANES registers directly corresponds to a plane. For the plane in which the logical operation defined by register MOD0 is to be executed, the corresponding bit in PLANES must be 0. For the plane in which the logical operation defined by register MOD1 is to be executed, the corresponding bit in PLANES must be 1.

(19) **PTNCNT** (Pattern Count)

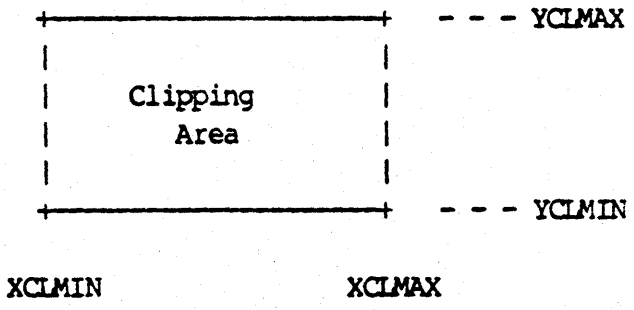
No. of Bits: 16
Address: 60H - 61H
Application: This register is set in the two ways listed below according to the painting pattern in the execution of the painting command:

1. In the case of painting by using the painting pattern previously generated in the display memory (TL = 1), the range of words from the address specified by the register PTNP to be referred to as the painting pattern is defined by the number of words.

2. When the 16-bit data in the register PTNCNT is used as the painting pattern (TL = 0), the actual painting pattern is defined.

(20) **XCLMIN, YCLMIN, XCLMAX, YCLMAX** (X/Y Clipping Minimum/Maximum)

No. of Bits: 16 each
Address: 62H - 69H, respectively
Application: These registers define the rectangular clipping area to be referred to during the drawing processing.



(21) **MAGH** (Horizontal Magnification)

No. of Bits: 4
Address: 6CH
Application: This register sets the enlargement/shrink magnification in the horizontal direction during execution of enlarge/shrink drawing. In the case of enlargement drawing, the magnifcation is 16/(MAGH+1). In the case of shrink drawing, the magnification if (MAGH+1)/16.

(22) **MAGV** (Vertical Magnification)

No. of Bits: 4
Address: 6CH
Application: This register sets the enlargement/shrink magnification in the vertical direction during execution of enlarge/shrink drawing. In the case of enlarge drawing, the magnification is 16/(MAGV+1). In the case of shrink drawing, the magnification is (MAGV+1)/16.

(23) **CLIP** (Clipping Mode)

No. of Bits: 2
Address: 6DH
Application: This register selects the clipping operation as shown in the following table:

CLIP	Function (Other than PAINT command)	Function (Paint command
00	Drawing only in the defined rectangular area	Boundary point retrieval and drawing only in defined rectangular area
01	No clipping operation	
10	Drawing only outside the defined rectangular area	Boundary point retrieval and drawing only outside the defined rectangular area
11	Not Used	

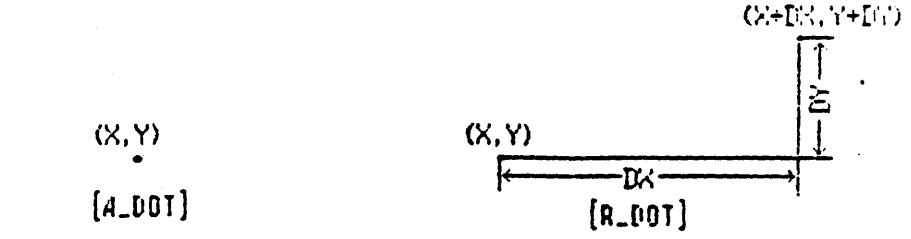
(24) **FLAGS, COMMAND** (Flags, Command)

No. of Bits: 16
Address: 6EH - 6FH
Application: This is the register used to write the command to be executed by the AGDC. It consists of the operation code (6FH) and the operation flags (6EH). When the operation code is written to the command register, AGDC begins processing.

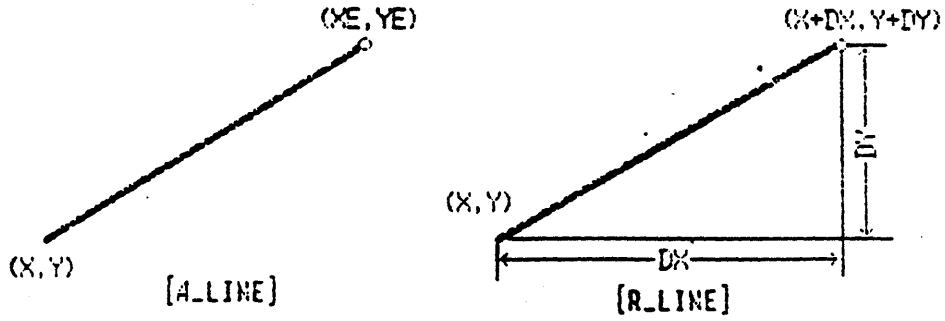
4.8 Parameters Corresponding to DRAW Commands

The parameters required for DRAW commands are illustrated in this section.

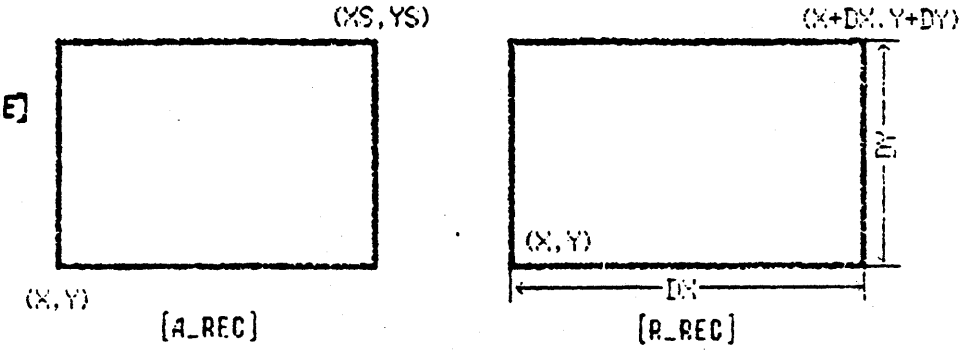
[DOT]



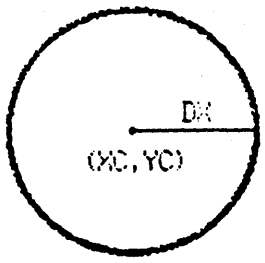
[LINE]



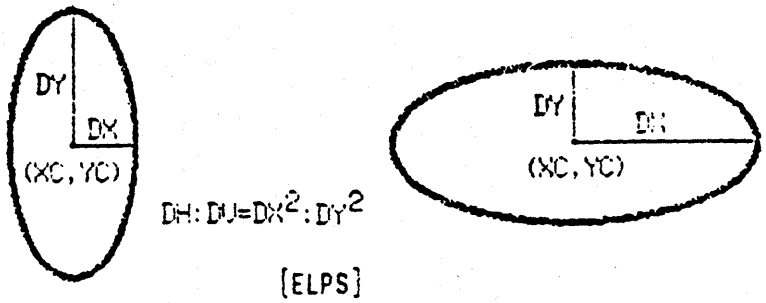
[RECTANGLE]



[CIRCLE]

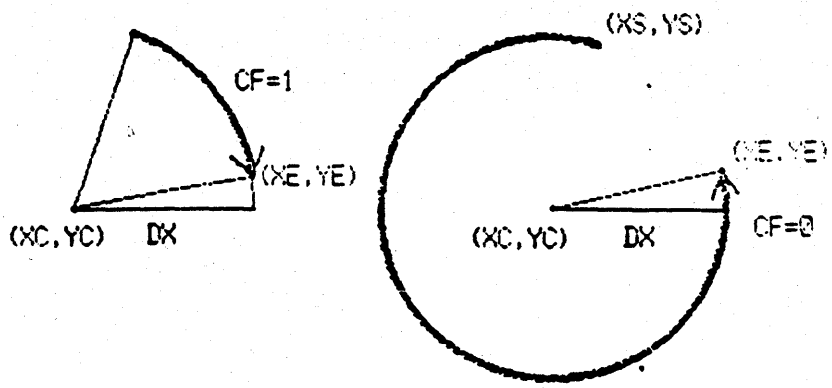


[ELLIPSE]



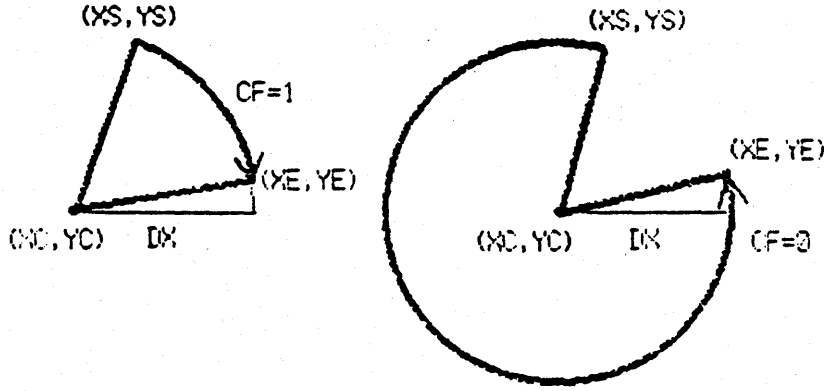
[ARC]

[CARC]



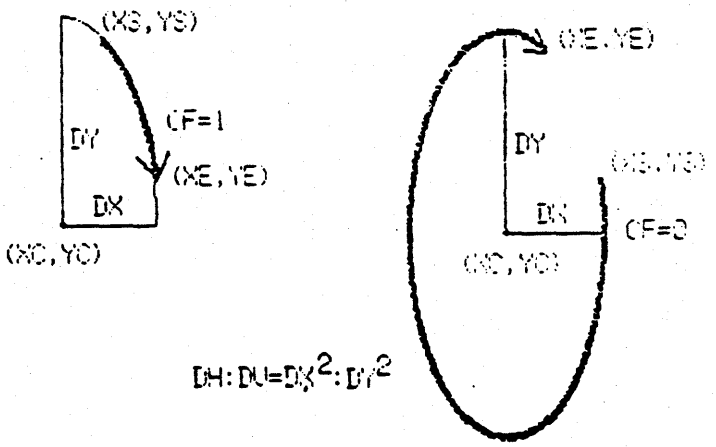
[SECTOR]

[CSEC]



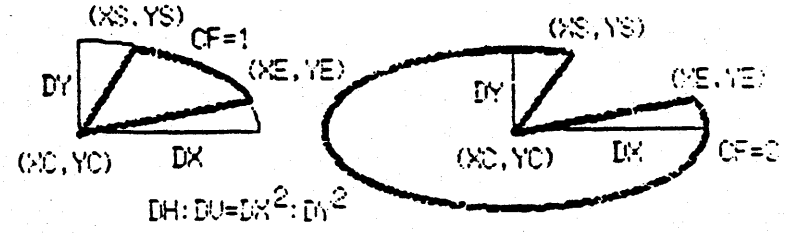
[ELLIPTICAL ARC]

[EARC]



[ELLIPTICAL SECTOR]

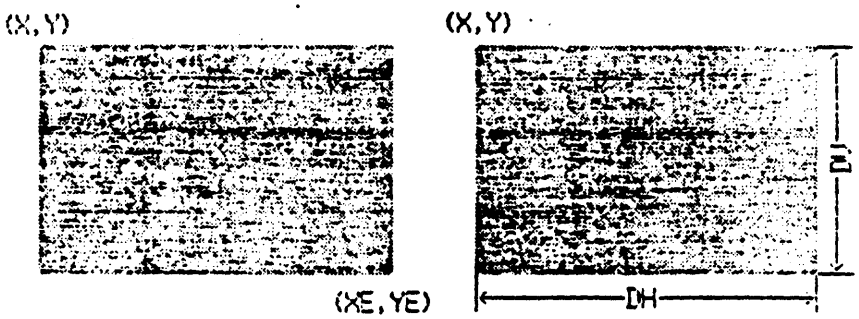
[ESEC]



[PAINT]

[PAINT]

[RECTANGLE FILL]

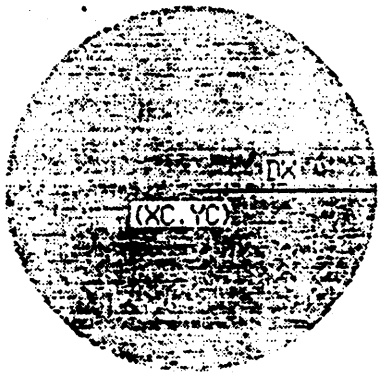


X≦XE Y≧YE
[A_REC_FILL]

DH≧0 DV≧0
[R_REC_FILL]

[CIRCLE FILL]

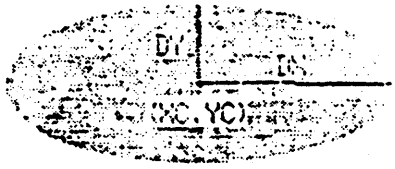
[CRL_FILL]



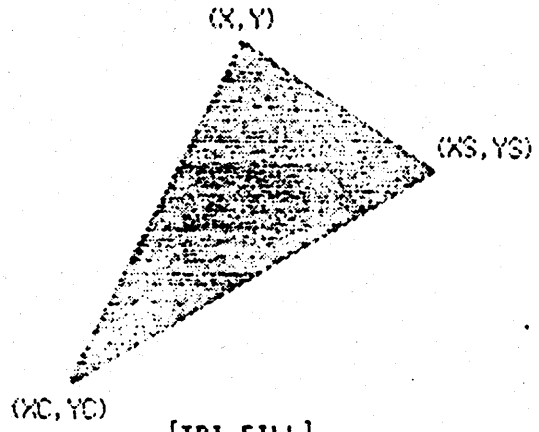
[ELLIPSE FILL]

[ELPS_FILL]

DH:DV=DX²:DY²

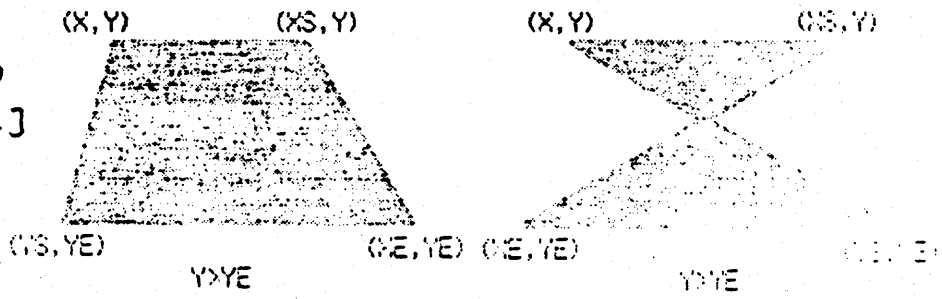


[TRIANGLE FILL]

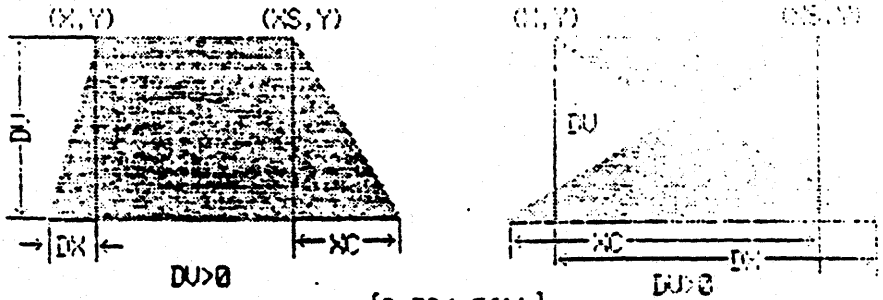


[TRI_FILL]

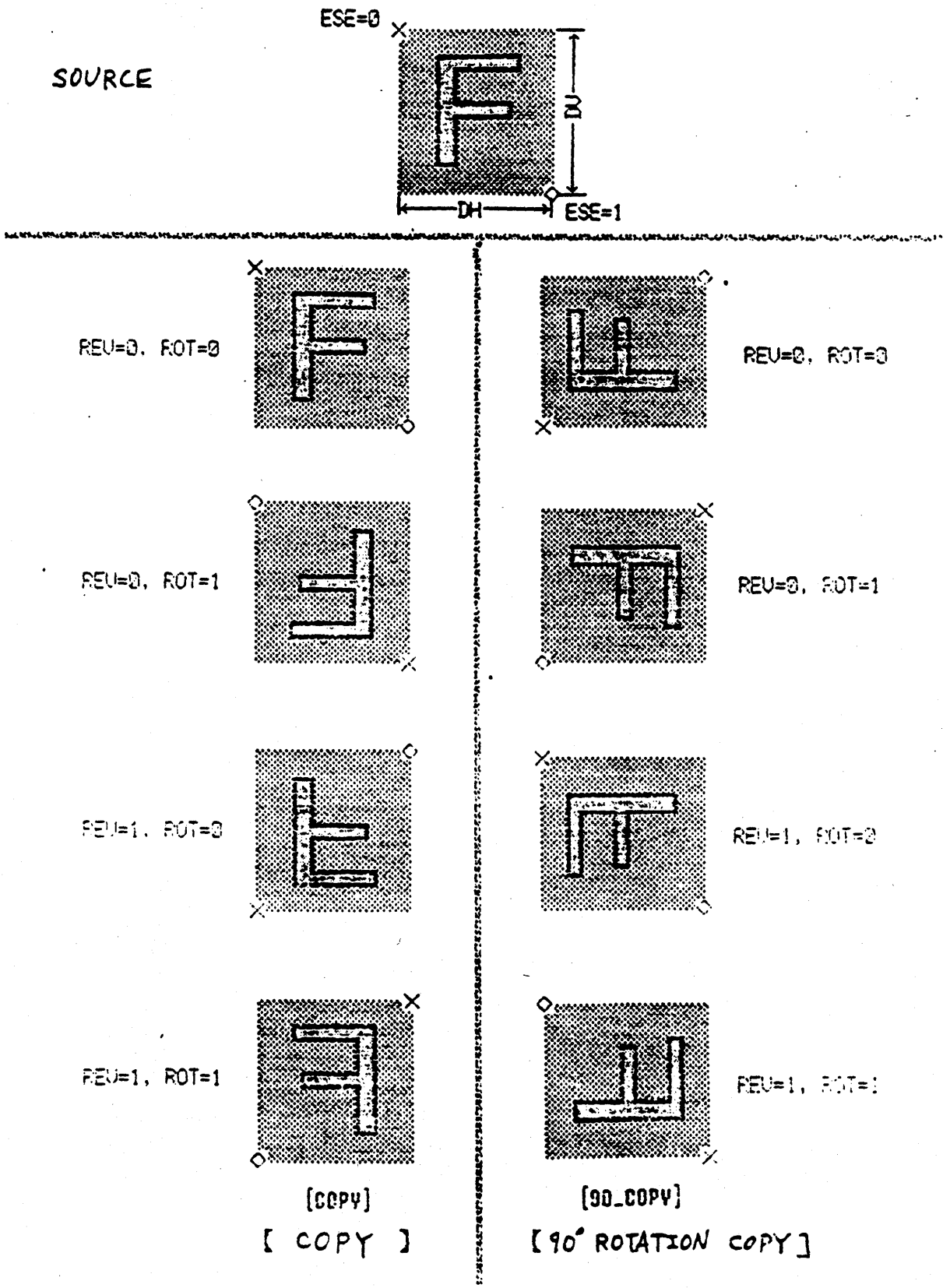
[TRAPEZOID FILL]



[A_TRA_FILL]



[R_TRA_FILL]


SOURCE
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DV
DH
ESE=1
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REV=0, ROT=1
REV=1, ROT=0
REV=1, ROT=1
REV=0, ROT=0
REV=0, ROT=1
REV=1, ROT=0
REV=1, ROT=1
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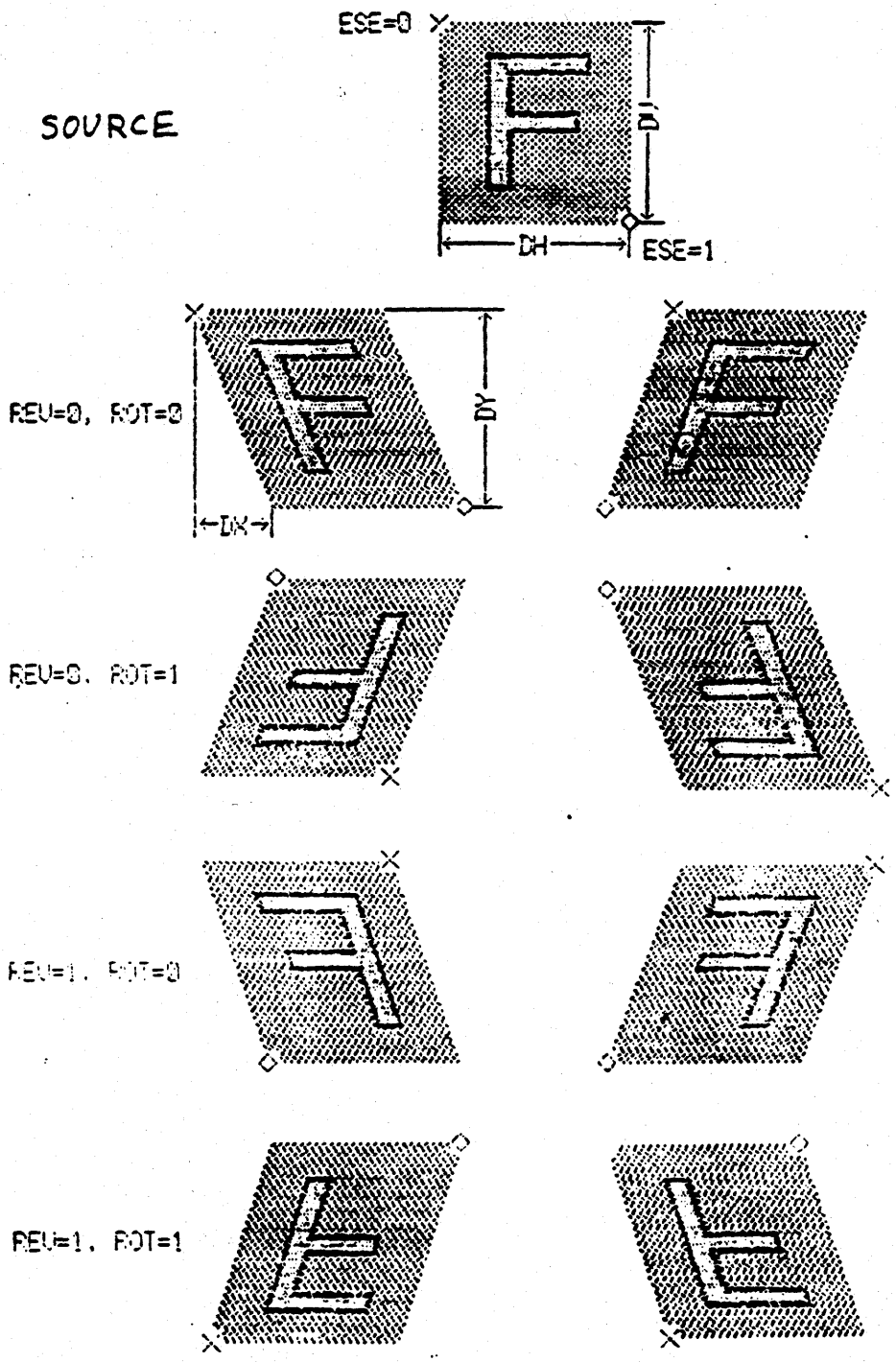
[COPY]
[90_COPY]
[90° ROTATION COPY]



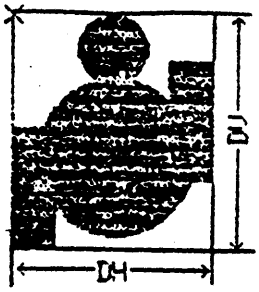
[SL_COPY]

[SLANT COPY]

[ENLARGE/SHRINK COPY]

[ES_COPY]

SOURCE



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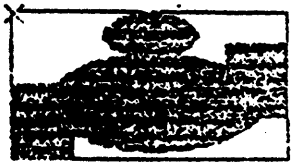

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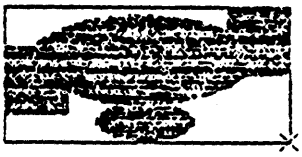
REV=0, ROT=1

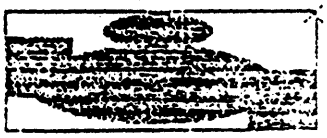


ESH=1, ESV=0

ESH=0, ESV=1

REV=1, ROT=0

ESH=0, ESV=0



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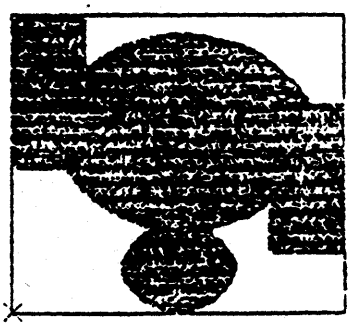
REV=1, ROT=1



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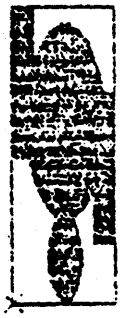

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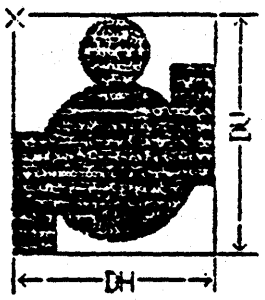
[ARBITRARY ANGLE ROTATION COPY]

[FR_ES_COPY]

SOURCE



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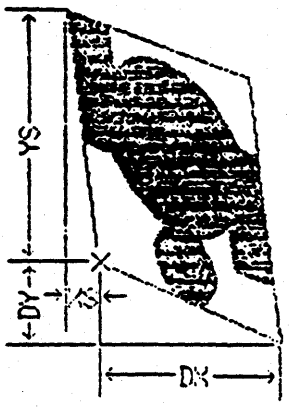
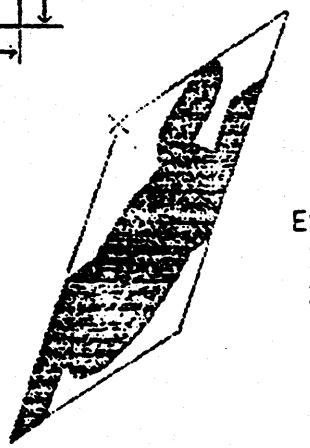
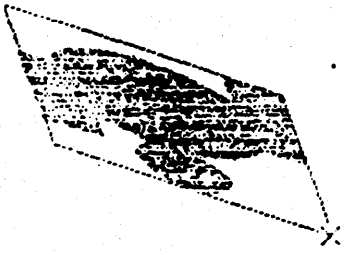
XS<0, YS>0

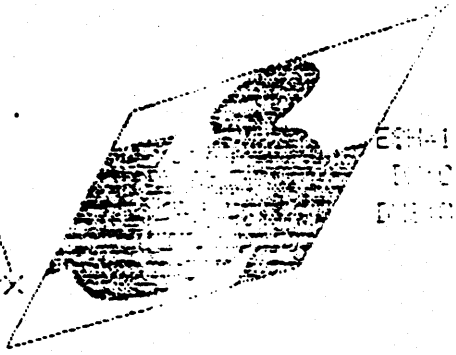




ESH=0, ESU=1
DX>0, DY>0
XS<0, YS<0

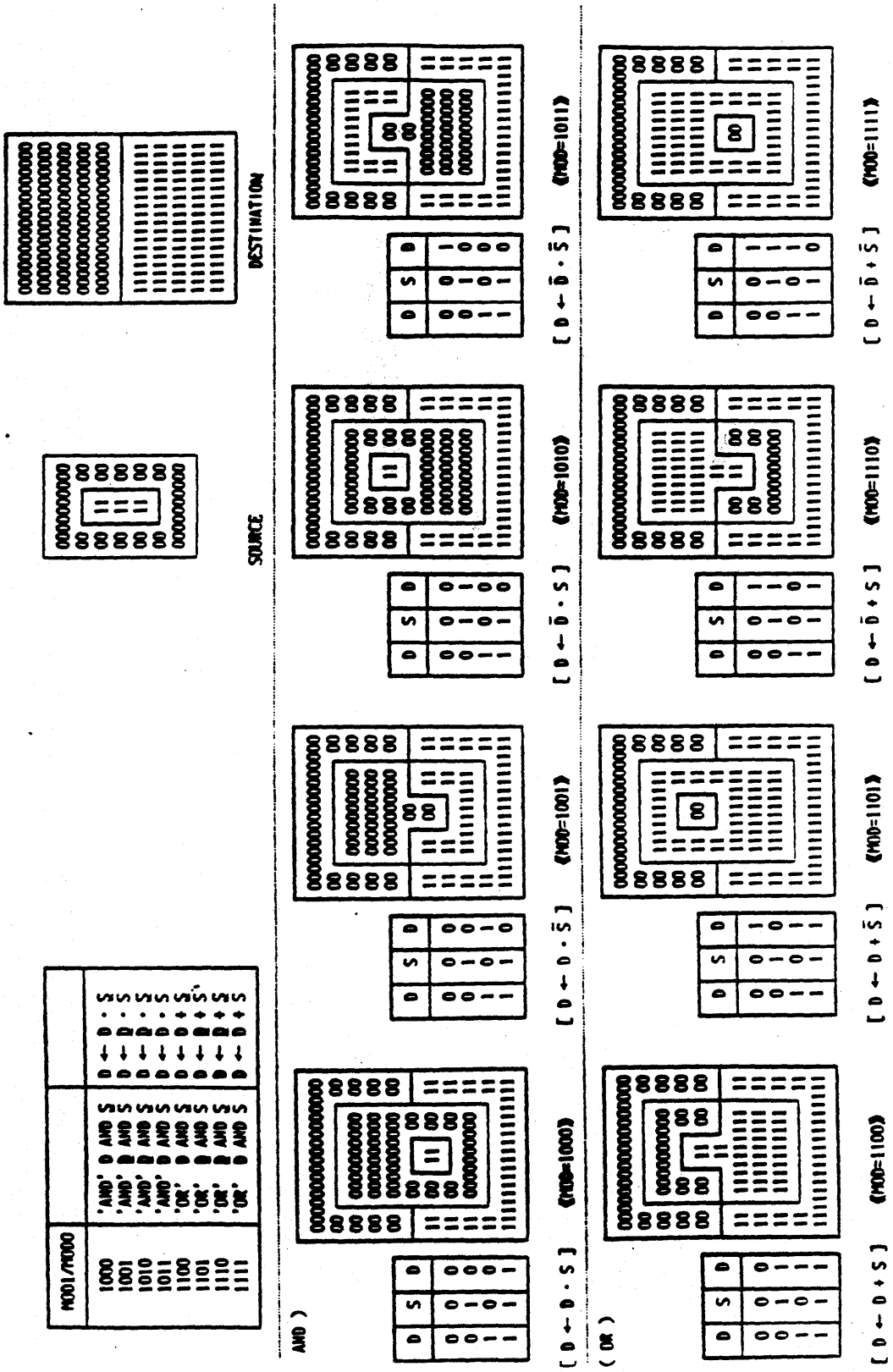
ESH=1, ESU=0
DX<0, DY>0
DXS<0, DYS>0



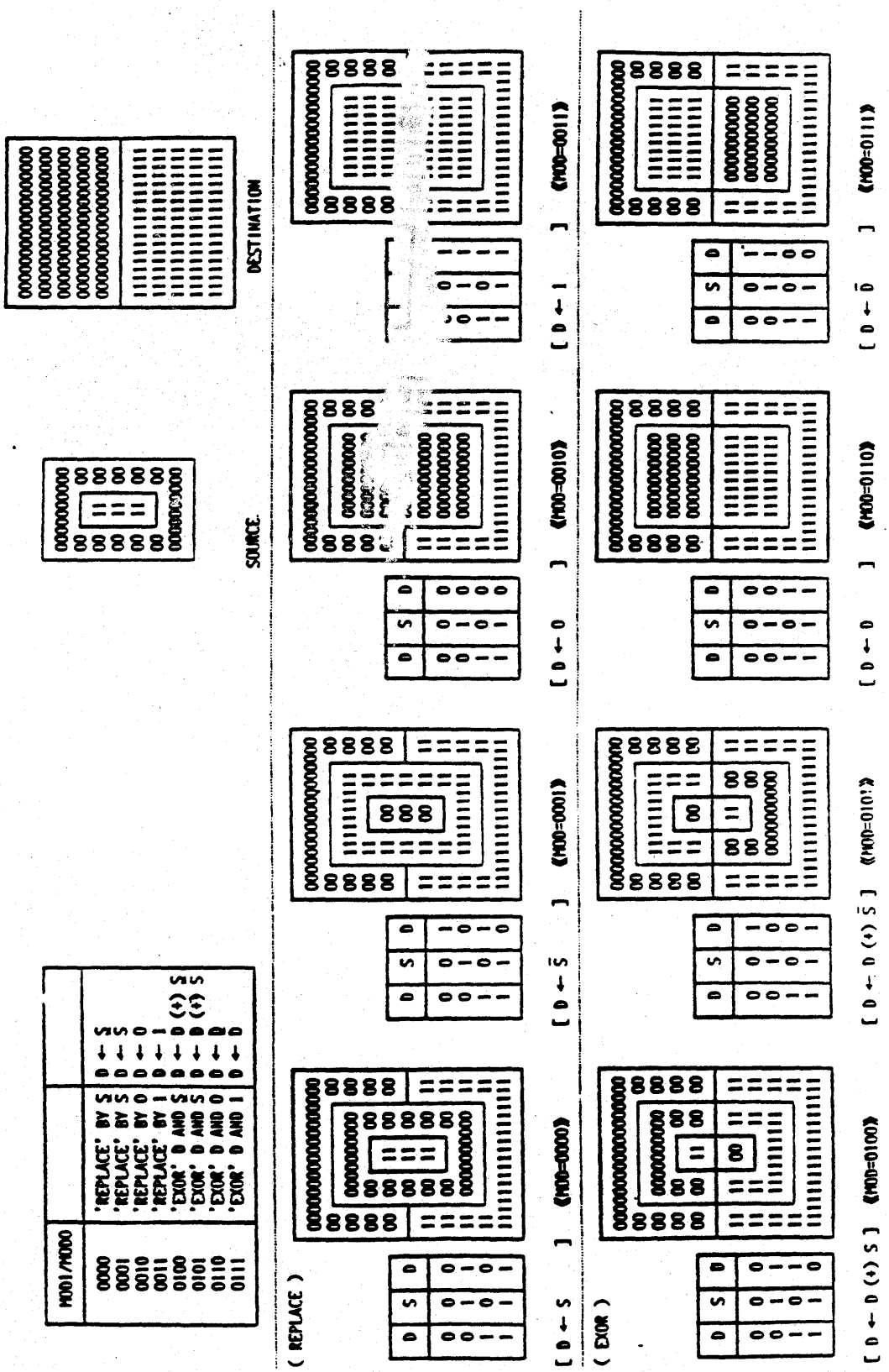


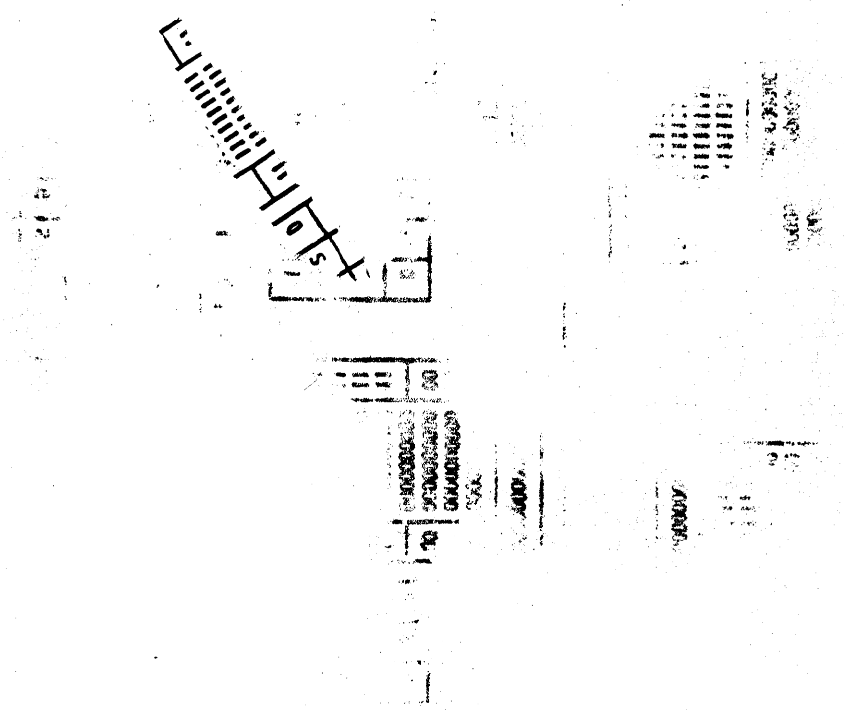
ESH=1, ESU=1
DX<0, DY<0
DXS<0, DYS<0

• RASTER OPERATION MODE (1)



• RASTER OPERATION MODE (2)





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