OTI-036

COLOR PALETTE WITH TRIPLE 6-BIT DAC

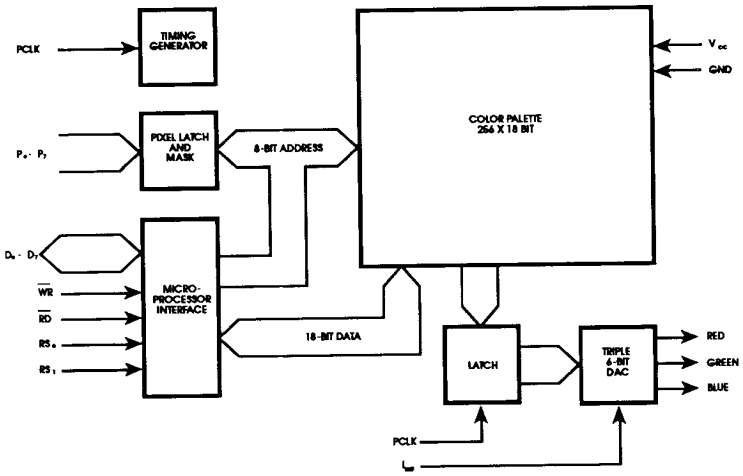
FEATURES

- Pixel Rates of 50 MHz (OTI-036-50) and 35 MHz (OTI-036-35)
- 256 x 18 Bit Color Palette
- 256K possible Colors
- Color Palette Read-back
- Three Internal 6-Bit DACs
- Direct Drive (75Ω) Video Cable
- RGB Analog Output
- Composite Blank
- Single +5V Power Supply
- Low Power, High Performance CMOS Processing
- TTL Compatible Inputs
- Full Asynchronous µP Interface
- Industry Standard 28-Pin DIL Plastic Package

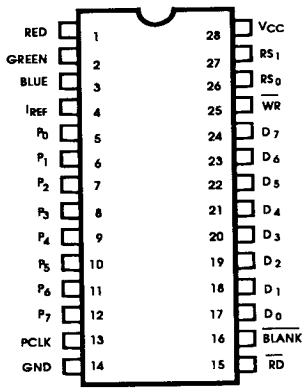
DESCRIPTION

The OTI-036, a monolithic triple 6-bit video digital-to-analog converters with on-chip 256 x 18 Bit color palettes is intended for graphics applications. The color palette makes possible the display of 256 colors selected from a total of 256K possible colors through the internal 6-bit RGB video DACs. The DACs are capable of driving single or double terminated 75Ω loads to normal video levels at pixel rates of 50 MHz (OTI-036-50) and 35 MHz (OTI-036-35). The OTI-036 provides a bidirectional microprocessor interface with TTL compatible inputs. The OTI-035-50 and OTI-036-35 are pin compatible with the Inmos IMS G171-35/G171-50.

BLOCK DIAGRAM



PIN CONFIGURATION



ORDER INFORMATION

Part Number	Package
OTI-036	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
RED GREEN BLUE	1 2 3	O O O	These signals are the analog outputs of the 6-bit DACs. These are the currents used for each of the guns in an RGB (Red, Green, Blue) video display. Each DAC is composed of 63 current sources. The output of each of these current sources is summed together according to the applied 6-bit binary value.
IREF	4	I	This is the Reference Current Input. The current forced out of this pin to ground determines the current sourced by each of the 63 current sources in each of the three 6-bit DACs. Each current source produces 1/30 of IREF when activated by the 6-bit digital input code.
P0 - P7	5-12	I	These are the Pixel Address lines. This byte-wide information is latched and masked by the Pixel Mask Register. The resulting value is used as an address of a location in the Color Palette RAM.
PCLK	13	I	The Pixel Clock signal is applied to this pin. The rising edge controls the latching of the Pixel Address and Blanking Inputs. It also controls the progress of these values through the three stage pipeline of the Color Palette and through the DACs to the outputs.
GND	14		This is the power supply connection, and is connected to ground.
$\overline{RD}$	15	I	This is the active Low READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines (D0-D7).
$\overline{BLANK}$	16	I	This is an active Low signal that forces the DAC's outputs to zero. When $\overline{BLANK}$ is asserted, a video monitor's screen becomes black and the DACs ignore any output values from the Color Palette. However, the Color Palette can still be updated through D0-D7.
D0-D7	17-24	I/O	These are the bidirectional Data I/O lines used by the host microprocessor to WRITE information (using the active Low $\overline{WR}$) into and READ information (using the active Low $\overline{RD}$) from the OTI-036-35/50 internal registers (Pixel Address register, Color Value register, and Pixel Mask register). During the WRITE cycle,the rising edge of $\overline{WR}$ latches the data into the selected register. The rising edge of $\overline{RD}$ determines the end of the READ cycle. With $\overline{RD}$ and $\overline{WR}$ equal to a logic HIGH, the Data I/O lines will no longer contain information from the selected register and will go into a tri-state mode.
$\overline{WR}$	25	I	This is the active Low WRITE signal, and controls the timing of the WRITE operations on the microprocessor interface inputs, D0-D7.
RS0,RS1	26, 27	I	These are the Register Select lines which control the selection of one of the three internal registers. These lines are sampled during the falling edges of the enable signals ($\overline{RD}$ or $\overline{WR}$). See Functional Description for more information regarding the internal registers.
VCC	28		This is the positive power supply pin. It is normally connected to +5V DC and bypassed with a 10µF tantalum capacitor.

FUNCTIONAL DESCRIPTION

The OTI-036-35/50 form the output stage for high resolution raster scan RGB video systems. It contains a Color Palette with 256 memory locations that are 18 bits wide. The color palette's output is connected to three high speed current output 6-bit video DACs. The devices use on-board registers to easily interface with microprocessors.

MICROPROCESSOR INTERFACE

The OTI-036-35/50 Microprocessor interface consists of three internal registers; Pixel Address Register, Color Value Register and Pixel Mask Register. These are individually accessed by register select signals, RS0 and RS1. The following table defines which register is selected by the logic states of RS0 and RS1 :

RS0	RS1	REGISTER
0	0	Pixel Address (Write Mode)
1	1	Pixel Address (Read Mode)
1	0	Color Value
0	1	Pixel Mask

The contents of the color palette can be accessed through the Color Value and Pixel Address registers.

All of the operations on tthe microprocessor interface can take place asynchronously to the pixel information currently being processed by the Color Palette.

The Pixel Address register is a byte-wide latch that receives and latches address information applied to pins P0-P7. It can be used in both Read and Write mode depending on the logic state of RS0 and RS1. With RS0 = RS1 = 0 (register select = 0,0), the Pixel Adress register is in the write mode. Two events normally precede WRITING one or more new color definitions to the color palette. The first is the specification of a color palette address. Second, the Color Value register must be loaded with a color definition. The sequence of data transfer is (1) the desired color palette address - this address is stored in the Pixel Address register and (2) the color definitions: RED, GREEN and lastly, BLUE. Refer to Figures 10 and 11.

When RS0 = RS1 = 1 (register select = 1,1), the Pixel Address register is in the Read mode. Once again, two events take place and normally precede **READING** one or more color definitions in the color palette. The first action is to specify an address within the color palette. The second is to load the Color Value register with the contents of the location addressed in the color palette. The color definition data transfer sequence is RED, GREEN and lastly, BLUE. Refer to Figures 9, 12, and 13.

The Color Value register is an internal 18-bit wide register used as a buffer between the microprocessor interface and the color palette. It is accessed by setting RS0 = 1 and RS1 = 0. A color definition can be read from or written to this register by a sequence of three byte-wide transfers to this register address. When a byte is written to this register, only the least significant six bits (D0 - D5) contain color information. When a byte is read from this register address, only the six least significant bits contain information - the most significant two bits are set to zero. Refer to Figures 9 - 13.

After the write sequence is completed, the Color Value register's contents are written to the specified color palette address stored in the Pixel Address register. Finally, the Pixel Address register is automatically incremented.

The color definitions can be read from the OTI-036-35/50 color palette. After setting RS0 and RS1 equal to 1, the desired color palette address is stored in the Pixel Address register. The color definition (18-bits) in the desired color palette location is then transferred to the Color Value register and the Pixel Address is auto-incremented. With successive read cycles, the color definitions pointed to by the incremented address is transferred to the Color Value register. Refer to Figure 12.

Attempting to update the color palette when $\overline{\text{BLANK}}$ is not asserted results in the data from the Color Value register taking precedence over the OTI-036-35/50 bit mapping operation. The output of the three 6-bit DACs will be based on the color definition from the memory location specified by the Pixel Address register and not the address found on P0 - P7. This conflict results in the DACs generating unexpected output levels. This can last as long as two PCLK periods.

The Pixel Mask register is a byte-wide latch. By setting RS0 = 0 and RS1 = 1, the Pixel Mask register can be accessed by the microprocessor interface, D0 - D7. This register is used to mask selected bits of the Pixel Address values applied to the Pixel Address inputs (P0 - P7). A "1" in any location in the Pixel Mask register leaves the corresponding bit to zero. The operation of the Pixel Mask register does not affect the address of the color definition when the microprocessor accesses the color palette. The masking operation makes it possible to alter the displayed colors without altering the contents of external video memory or the OTI-036-35/50 color palette.

WRITING TO THE COLOR PALETTE

A new color definition can be stored in the color palette by first specifying the initial address under write mode. this address is stored in the Pixel Address register (RS0 = RS1 = 0). The initial address is followed by RED, GREEN and BLUE color definition data (RS0 = 1, RS1 = 0). These six-bit inputs are collected together in the Color Value register for a total of 18 bits. This new color definition is then transferred to the location pointed to by the information stored in the Pixel Address register. As soon as this transfer is completed, the Pixel Address register is auto-incremented. This allows consec-

FUNCTIONAL DESCRIPTION (CONTINUED)

utive color palette locations to be updated without the microprocessor specifying each address. All that is necessary is to continue supplying the RED, GEEN and BLUE data for each consecutive address. Refer to Figures 10 and 11.

READING FROM THE COLOR PALETTE

To read a location in the color palette, an address is sent on the Data I/O lines (D0 - D7) under Read mode and stored in the Pixel Address register (RS0 = RS1 = 1). The color definition contained in the specified location is then transferred to the Color Value register. Once again, the Pixel Address register is auto-incremented. The color definition can now be retrieved with three sequential read operations (RS0 =1, RS1= 0). The first byte placed on the Data I/O lines contains the RED value. The next is GREEN and the final is BLUE. The two most significant bits are set to zero in each case. In a manner similar to the write mode, consecutive color palette locations can be read by simply specifiying the beginning address and reading color palette one or more times. Refer to Figures 9, 12 and 13.

If the Pixel address register is ever updated during a read or write operation, the current data sequence is terminated and a new read or write operation is initialized.

VIDEO PATH

The Video path consists of the Pixel Latch and Mask (inputs P0- P7), color palette (256 18-bit wide RAM), 18-bit wide bus, and an 18-bit wide latch on the inputs of the three 6-bit high-speed video DACs. The video path uses a three clock cycle (PCLK) pipeline for the Pixel Address and $\overline{\text{BLANK}}$ inputs. These signals are latched on the rising edge of PCLK.

ANALOG OUTPUTS

The analog outputs are designed to drive single-terminated 75Ω loads to a peak-white amplitude of 0.7V.

The reference current (IREF) for this output is set to 4.44 mA. The analog outputs can also drive double-terminated 75Ω loads with IREF set to 8.88 mA.

The analog outputs can be set to zero by using $\overline{\text{BLANK}}$ input. This is an active Low signal that forces the analog outputs to ground by placing all zeros on the DACs' inputs. The color definition selected by the Pixel Address is ignored. Each of the 63 current sources used in each of the 6-bit DACs produces 1/30 IREF. Therefore, the magnitude of peak white voltage is a function of the output loading and is determined by:

$$V_{PEAK\ WHITE} = 2.1\ (I_{REF})\ R_L$$

$$V_{BLACK\ LEVEL} = 0V.$$

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	OTI-036-35		OTI-036-50		Unit	Condition
		Min	Max	Min	Max		
tCHCH	PCLK Period	28		20		ns	
ΔtCHCH	PCLK Jitter		±2.5		±2.5	%	Note 1
tCLCH	PCLK Width Low	9		6		ns	
tCHCL	PCLK Width High	7		6		ns	
tPVCH	Pixel Word Setup Time	4		4		ns	Note 2
tCHPX	Pixel Word Hold Time	4		4		ns	Note 2
tBVCH	BLANK Setup Time	4		4		ns	Note 2
tCHBX	BLANK Hold Time	4		4		ns	Note 2
tCHAV	PCLK to valid DAC Output	5	30	5	30	ns	Note 3
ΔtCHAV	Differential Output Delay		1		1	ns	Note 4
tWLWH	WR Pulse Width Low	50		50		ns	
tRLRH	RD Pulse Width Low	50		50		ns	
tSVWL	Register Select Setup Time (Write Cysle)	15		10		ns	
tSVRL	Register Select Setup (Read Cycle)	15		10		ns	
tWLSX	Register Select Hold Time (Write Cycle)	15		10		ns	
tRLSX	Register Select Hold time (Read Cycle)	15		10		ns	
tDVWH	WR Data Setup Time	15		10		ns	
tWHDX	WR Data Hold Time	15		10		ns	
tRLQX	Output Turn-on Delay	5		5		ns	
tRLQV	RD Enable Access Time		40		40	ns	
tRHQX	Output Hold Time	5		5		ns	
tRHQZ	Output Turn-off Delay		20		20	ns	Note 5
tWHWL1	Successive Write Interval	3		3		tCHCH	
tWHRL1	WR followed by READ interval	3		3		tCHCH	
tRHRL1	Successive READ Interval	3		3		tCHCH	
tRHWLl1	RD followed by WRITE Interval	3		3		tCHCH	
tWHWL2	WR after Color Write	3		3		tCHCH	Note 6
tWHRL2	RD after Color Write	3		3		tCHCH	Note 6
tRHRL2	RD after Color Read	6		6		tCHCH	Note 6
tRHWL2	WR after Color Read	6		6		tCHCH	Note 6
tWHRL3	RD after Read Address Write	6		6		tCHCH	Note 6
	Read/Write Enable Transition Time		50		50	ns	

AC CHARACTERISTICS (CONTINUED)

Note 1: This parameter is the allowed variation in the pixel clock frequency. It does not permit the pixel clock period to vary below the minimum value for pixel clock (tCHCH) period specified.

Note 2: It is necessary that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of PCLK (this requirement includes blanking period).

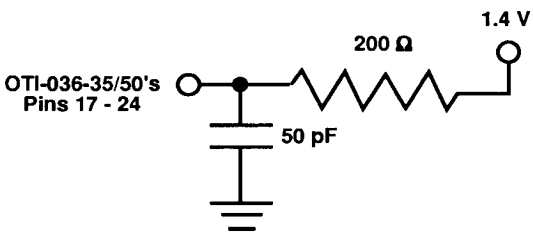
Note 3: A valid analog output is defined as the 50% point between successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

Note 4: This applies to different analog outputs on the same device. This is a design parameter, not 100% tested.

Note 5: Measured at ±200 mV from initial steady state output voltage.

Note 6: This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

AC TEST CONDITIONS



Input Pulse Levels	GND to 3V
Input Rise and Fall Times (10% to 90%)	2.5 ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

TIMING CHARACTERSITICS

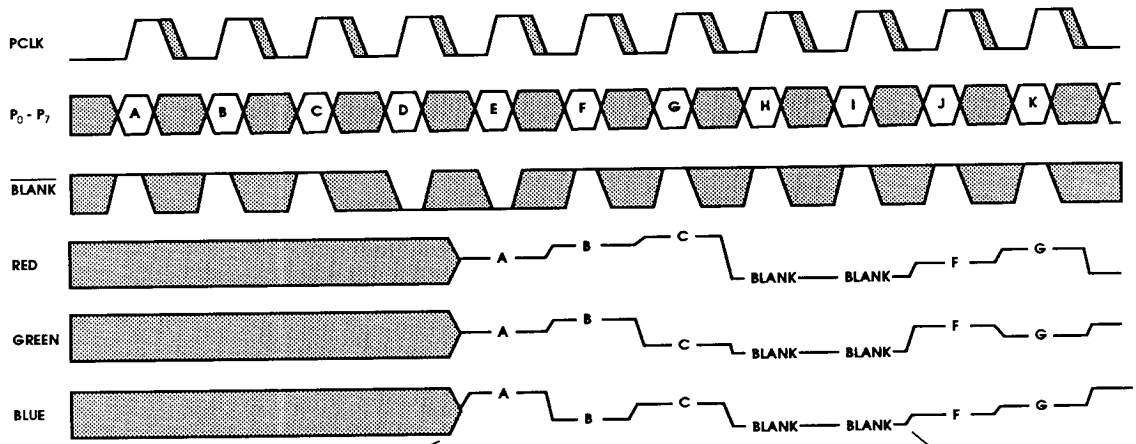


FIGURE 1. System Timing Diagram.

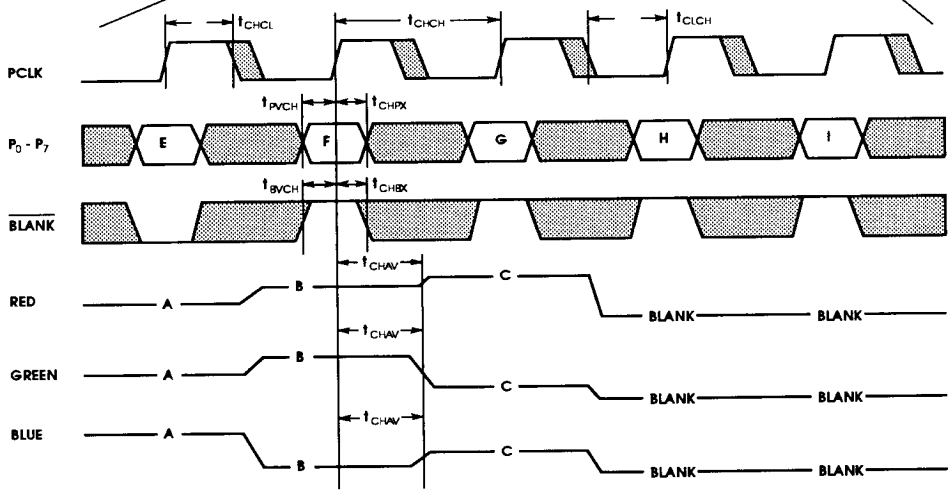


FIGURE 2. Timing Diagram Detailing Timing Specifications.

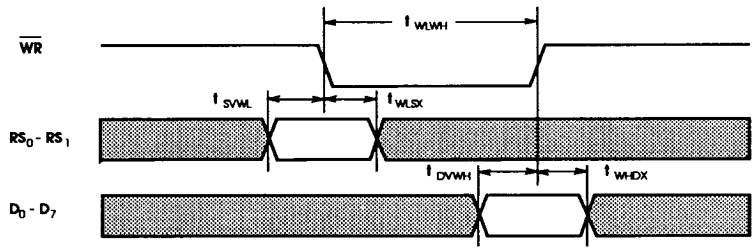


FIGURE 3. Basic Write Cycle Timing Diagram.

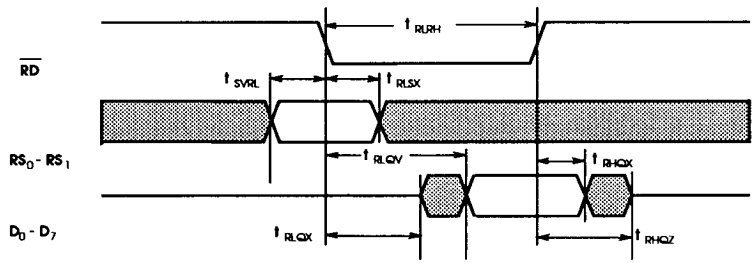


FIGURE 4. Basic Read Cycle Timing Diagram.

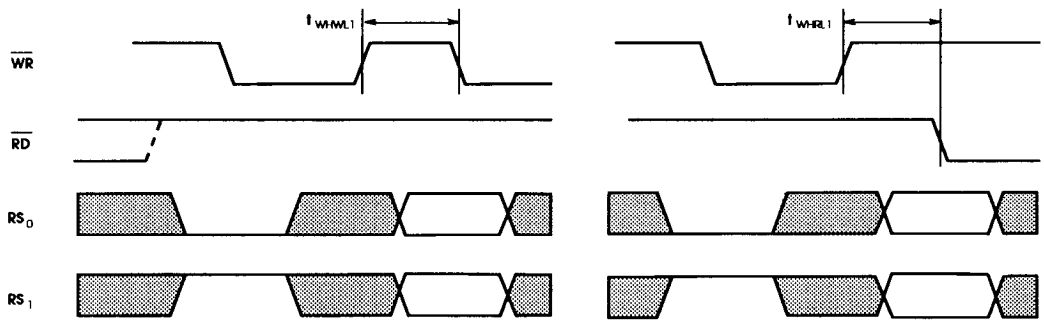


FIGURE 5. Write to Pixel Mask Register Followed by (a) Write and (b) Read.

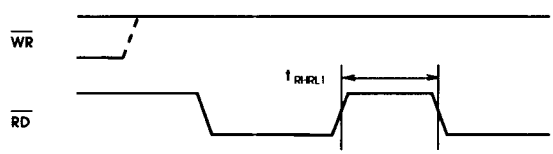


FIGURE 6a. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Read.

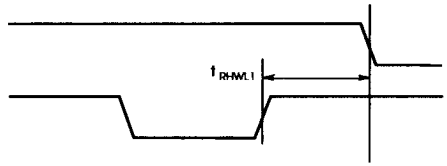


FIGURE 6b. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Write.

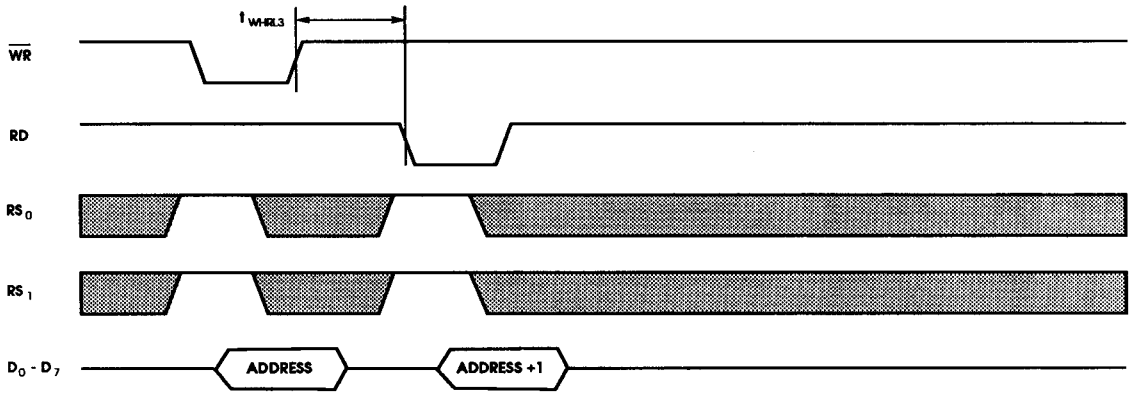


FIGURE 7. Write and Read Back Pixel Address Register (Read Mode).

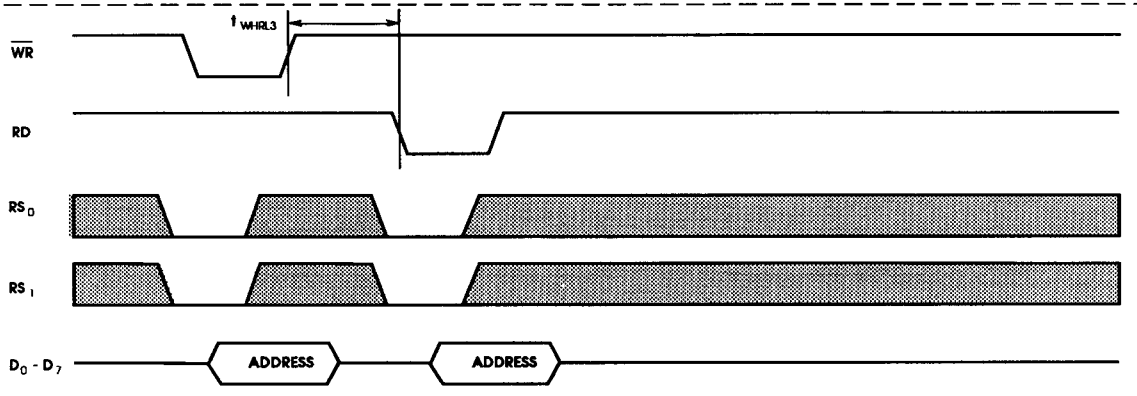


FIGURE 8. Write and Read Back Pixel Address Register (Write Mode).

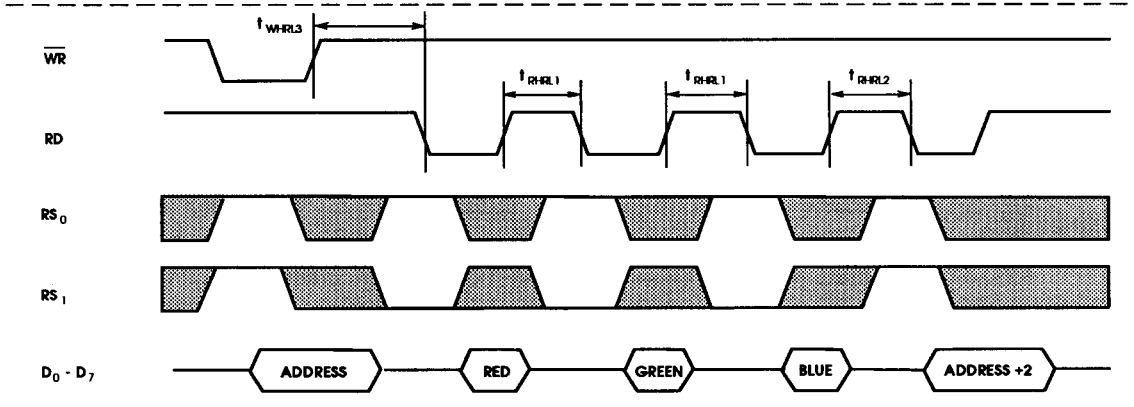


FIGURE 9. Read Color Value then Read Pixel Address Register (Read Mode).

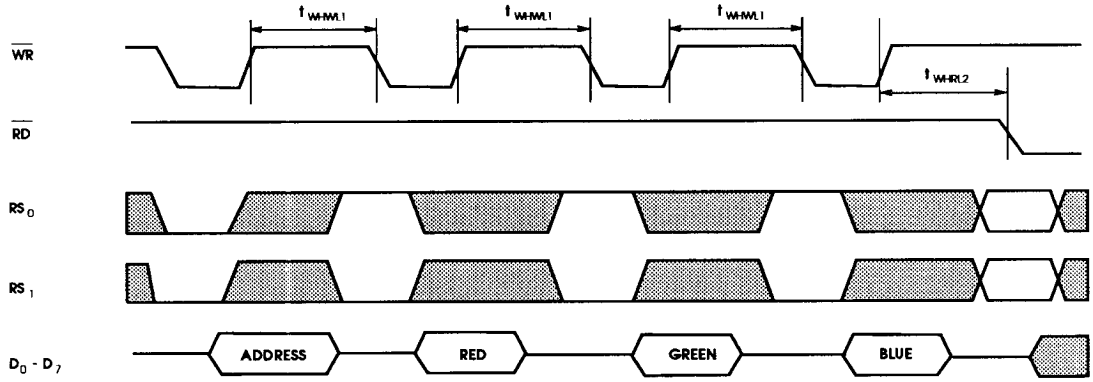


FIGURE 10. Color Value Write Followed by any Read.

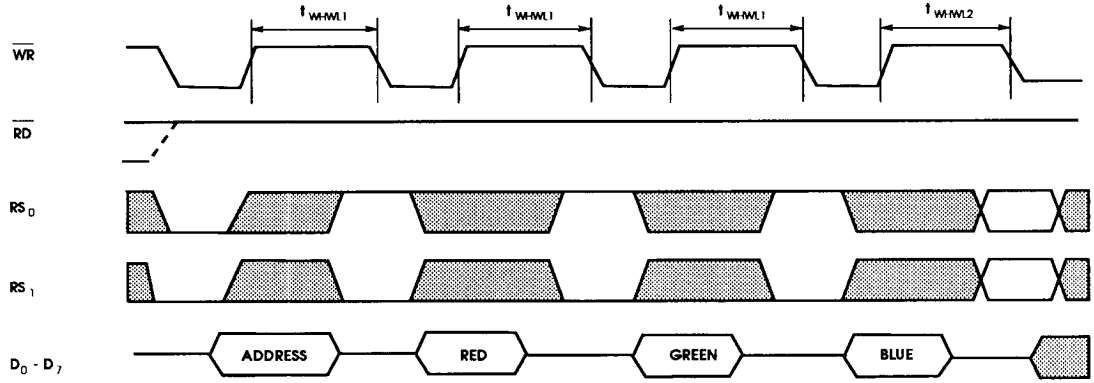


FIGURE 11. Color Value Write Followed by any Write.

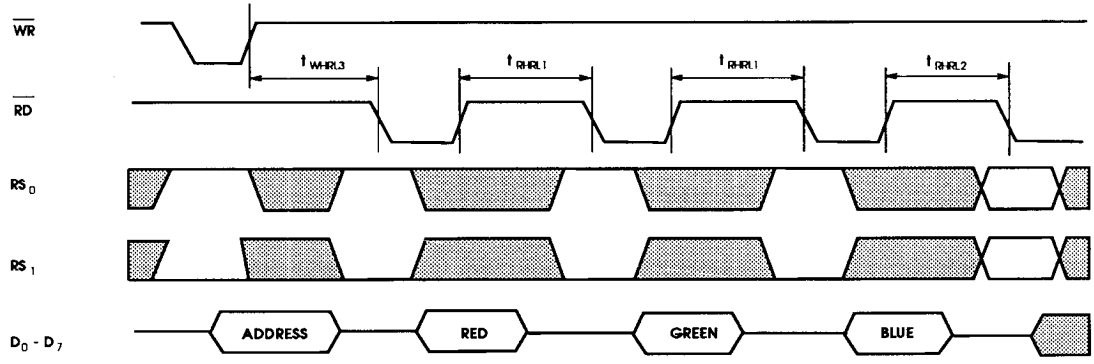


FIGURE 12. Color Value Read Followed by any Read.

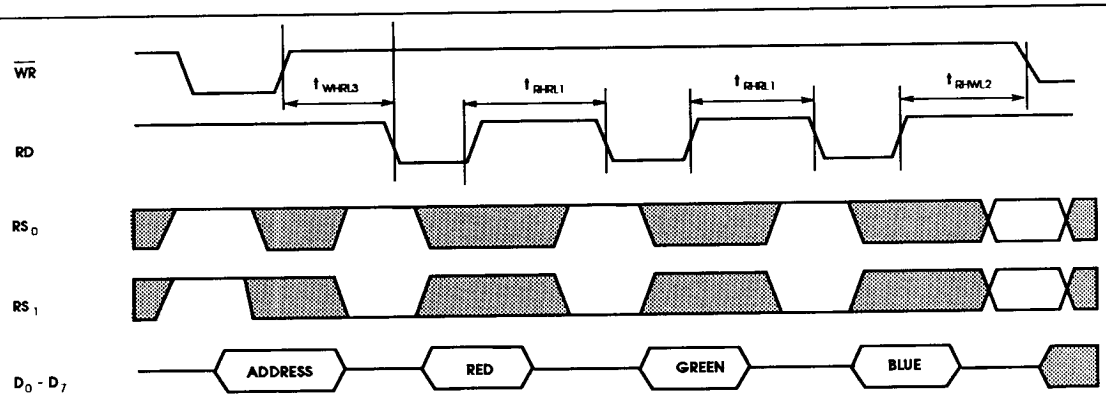


FIGURE 13. Color Value Read Followed by any Write.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0V
Applied Input Voltage	–0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = 400 µA
VOL	Output Low Voltage		0.45	V	
VIH	Input High Voltage	2.0	VCC + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	–10	10	µA	
OLI	Output Leakage Current	–10	10	µA	
IREF	Reference Curent	–3	–10	mA	
ICC	Operating Supply Current (OTI-036-35) Operating Supply Current (OTI-036-50)		150 160	mA mA	PCLK = 35 MHz PCLK = 50 MHz IOUT = Max. Digital Outputs Unloaded
VREF	Reference Voltage at IREF Pin	VCC-3		V	VCC = 4.5V, IREF = 10 mA
	DAC Resolution		6	BITS	

DC CHARACTERISTICS: (CONTINUED)

Symbol	Parameter	Min	Max	Unit	Condition
VOUT	Output Voltage Compliance (Pins 1-3)	1.5		V	IOUT ≤ 10 mA
IOUT	Output Current Compliance (Pins 1-3)		21	mA	VOUT ≤ 1V IREF ≤ 10 mA
	Full Scale Error Note 7		-7, +3	%	ZL = 75Ω +30 pF IREF = 4.44 mA ZL = 37.5Ω +30 pF IREF = 8.88 mA
	DAC-to DAC Mismatch Note 8		±1	%	ZL =75Ω +30 pF IREF = 4.44 mA
	Internal Linearity Note 9		±0.5	LSB	ZL =75Ω +30 pF IREF = 4.44 mA
tON	Rise Time Note 10		8	ns	ZL = 75Ω +30 pF IREF = 4.44 mA
	Full-Scale Setting Time (OTI-036-35) Full-Scale Setting Time (OTI-036-50) Note 11		28 20	ns	ZL = 75Ω +30 pF IREF = 4.44 mA
	Glitch Energy Note 12		±200	pV-sec	ZL = 75Ω +30 pF IREF = 4.44 mA
COUTA	Analog Capacitance (Pins 1-3)		10	pF	$\overline{\text{BLANK}}$ = Logic Low
VOUTBLANK	Blanking Output Voltage		±0.5	LSB	$\overline{\text{BLANK}}$ = Logic Low ZL = 75Ω +30 pF IREF = 4.44 mA
	Unadjusted Output Offset Error		±0.5	LSB	$\overline{\text{BLANK}}$ = Logic High ZL = 75Ω +30 pF IREF = 4.44 mA
	Clock Feedthrough (OTI-036-35) Clock Feedthrough (OTI-036-50) Note 13		-35 -30	dB dB	PCLK =35 MHz PCLK = 50 MHz ZL = 75Ω +30 pF IREF = 4.44 mA
PSS	Power Supply Sensitivity		5	%V	4.5V ≤ VCC ≤ 5.5V IOUT = Full-Scale ZL = 75Ω +30 pF IREF = 4.44 mA

Note 7: Full-scale error is defined as ([F.S. IOUT) RL - 2.1 (IREF) RL]/[2.1 (IREF) RL]) 100%. VBLACK LEVEL = 0V.
Note 8: The listed value is relative to the midpoint of the full-scale distribution of the internal three DACs.
Note 9: Zero and full-scale adjusted linearity error = [VOUT-VOFFSET- (D x VLSB))/VLSB, VLSB = (VFULLSCALE -VOFFSET)/63].
Note 10: The rise time is measured for 10% to 90% of the full scale transition.
Note 11: The output signal's setting time is measured from a 2% change at the transition's initial value until it has settled to within 2% of the final value.
Note 12: This value is determined using triangle approximation: glitch energy = (area of positive transient) - (area of negative transient).
Note 13: These values are referenced to full-scale output.

APPLICATION HINTS

POWER SUPPLY

The OTI-036-35/50 may draw large transient currents from the power supply. To ensure proper operation, it is necessary to utilize standard high frequency board layout techniques and power supply distrbution.

The transient currents required by the OTI-036-35/50 dictates that the AC impedance of the ground path must be kept to a minimum. This is accomplished by using the recommended decoupling capacitors, C1 and C2, as shown in Figure 14. These capacitors must have leads that are as short as possible. High frequency decoupling is accomplished with a 0.1µF chip capacitor, C1. A bead tantalum, between 10 µF to 47 µF, should be used for C2.

Differential ground noise can be created when voltage difference appears between pin 14 and the ground of the digital devices driving the OTI-036-35/50. This difference is caused by series impedance in the ground path and the current transients drawn by the OTI-036-35/50. The differential ground noise can be minimized by using large, low inductance ground paths between the digital devices that drive the OTI-036-35/50 and pin 14. Therefore, a ground plane layout is recommended.

ANALOG OUTPUT - LINE DRIVING

The connection between the OTI-036-35/50 outputs and the RGB inputs of the video monitor it is driving should be viewed as a transmission line. Impedance changes along this line will result inthe reflection of part of the video signal back to the DACs' outputs. These reflections may result in a degradation in the picture quality displayed on the monitor. To ensure good signal fidelity RF techniques shoud be observed. Any traces connecting the OTI-036-35/50 to an onboard connector should form a transmission line of 75Ω impedance. However, the need to ensure that the connecting traces form a transmission line can be eliminated by placing the DACs' output termination resistor at the output connector instead of the DACs' output pin. The coaxial cable that connects the OTI-036-35/50 outputs to a video monitor should have a characteristic impedance of 75Ω. Connectors on the coaxial line can cause impedance change. Any connectors used with the coaxial cable must match its characteristic impedance.

The OTI-036-35/50 DACs use switched current sources that are summed together, thus generating the output current. Each 6-bit DAC consists of 63 current sources, each of which has a magnitude of 1/30 (IREF). The digital input code determines the number of current sources that are active and contributing to the total output current. This output current, in conjunction with a termination resistance connected between each DAC output and ground, sets the full-scale magnitude of the output voltage. There are four different methods of terminating the OTI-036-35/50 DAC outputs:

(1) Single Termination at the DAC (75Ω)

(2) Single Termination at the Destination (75Ω)

(3) Double Termination (37.5Ω)

(4) Buffered Signal

(1) Single termination at the source involves placing a single termination resistor a each DAC output of the OTI-036-35/50. No other terminating load is present. Therefore, a high-nput impedance monitor should be used. The AC load driven by the DACs' outputs is the transmission line impedance in parallel with the load resistor. The transmission line's impedance should match the impedance f the load resistor. Thus, the DACs' output has an initial signal amplitude that is half the DC value expected. This half-amplitude signal is 100% reflected by the open cicuit presented by the monitor input. This restores the signal amplitude to the expected value. The reflections from the monitor propogate back towards the DAC outputs. The load resistor at each DAC output presents a correctly terminated transmission line so no further reflections occur. This arrangement is relatively tolerant to mismatches in the transmission line between the DAC and the monitor because no reflections occur at the DAC end of the transmission line. However, multiple monitors should not be connected in parallel despite each monitor's high input impedance.

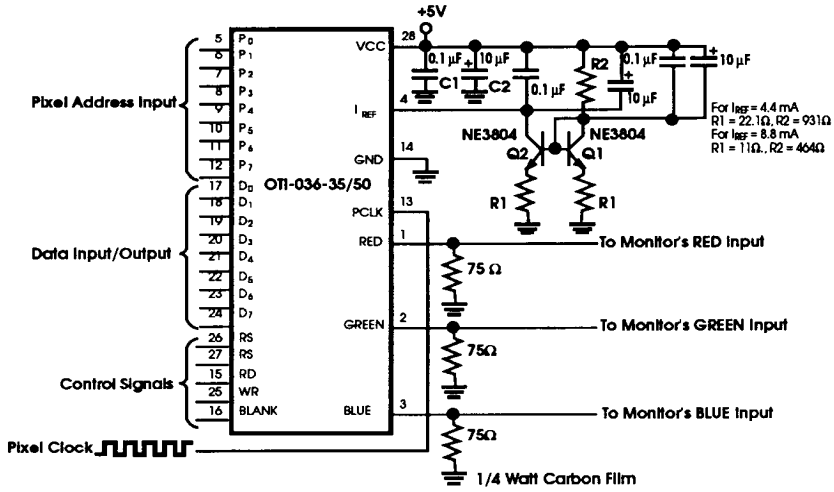
2) Single-termination at the destination has the termination impedance at the input of the monitor acting as both the load resistor for the DAC and the termination impedance of the cable (transmission line). If the connection between the OTI-036-35/50 correctly terminated there will be no reflections. However, if there are any line impedance variations along the cable, relflections will occur and create "ghost images" on the display. This occurs because there is a reflection from the point where the mismatch occurs back to the DACs' output. The signal then reflects off the DAC's output back toward the monitor. It arrives with a significant time delay following the original signal and "ghosting" results.

3) Double-termination of the DAC outputs allows each end of the transmission line to be correctly matched. This results in the least amount of reflection and the highest signal and display fidelity. This termination method also allows for the fastest rise time. The DAC termination's RC time constant sets the outputs' rise time. The greater the time constant, the slower the rise time. Therefore, the rise time will be minimized since the impedance using this termination technique is less than that achieved with single termination. With double-termination, it is necessary to increase IREF to 8.8 mA to ensure a full-scale output voltage of 700 mV.

4) By placing a buffer at the DAC's output the OTI-036-35/50 will be able to drive large capacitance loads such as long lossy cables. The buffer requires a high input impedance, a condition that is satisfied by the LM1201 and LM1203. A 75Ω load is placed at the buffer's input.

The buffer's low output impedance should be matched to the interconnecting cable with a series resistor. The cable should then be terminated with the same resistance at the monitor.

APPLICATION HINTS (CONTINUED)



NOTE: Bead-style tantalum capacitors should be used for the 10µF devices.
Thermally connect the NPN transistors together with a Wakefield 256 series Equalizing Link.

Figure 14. Typical Connection Showing IREF Generator.

ANALOG OUTPUT-PROTECTION

Each of the OTI-036-35/50 pins has on-chip electrostatic discharge damage (ESD) protection. However, proper precautions for handling these parts are recommended during manufacturing to reduce the possibility of ESD.

GENERATING IREF

An active current source for IREF is recommended to ensure that the OTI-036-35/50 has predictable and stable output currents. There are numerous methods available to generate the reference current. One of the simplest circuits is shown with the OTI-036 in Figure 14. As shown, this IREF generator will sink -4.44 mA (single termination) with R1 = 22.1Ω and R2 = 931Ω.

For applications that use double termination, R1 = 11Ω and R2 = 464Ω. The diode connected transistor, Q1, across Q2's base-emitter junction performs a first-order compensation for thermal variations.

Figure 15 shows an alternative method of generating IREF . The LM334 precision current source is used in a temperature compensated configuration. The reference current is set by a single resistor, R1, independent of VCC. The current's value is:

IREF = 33.85 mV/R1

Figure 16 shows an LM10 and a discrete transistor generating IREF. The LM's on-board 200 mV voltage reference is used along with the reference's amplifier to set the voltage on R1 to 200 mV. Ignoring the small amount of base current, the discrete transistor's collector current (and therefore, IREF) is found to be:

IREF = 200 mV/R1

For IREF = 4.44 mA, R1 is, to the nearest 1% value 44.2Ω; IREF = 8.88 mA gives an R1 of 22.1Ω. The circuit shown in Figure 17 operates in the same fashion as the LM10 circuit in Figure 16. The LM611's on-board reference produces a nominal 1.24V. The voltage divider connected to the reference's output, pin 3, creates 200 mV that is applied to R1. The current (IREF) through the discrete transistor's collector is:

IREF = 200 mV/R1

For IREF = 4.4 mA, R1 is, to the nearest 1% value 44.2Ω; IREF = 8.88 mA gives an R1 of 22.1Ω.

DECOUPLING IREF

The OTI-036-35/50 uses DACs composed of switched current sources. Each current source is based on a current mirror that produces (IREF)/30 when active. The total output current is determined by the number of active current sources switched to the output and the magnitude of IREF.

The magnitude of the current flowing through the internal current sources depends not only on IREF, but also on the voltage at pin 4 relative to VCC. Therefore, voltage variations between VCC and the IREF input can result in variations in the DAC's output current. These variations can be greatly attenuated by using a high frequency capacitor in parallel with a larger electrlytic capacitor to couple the IREF input to VCC. This allows the reference current input to track both high and low frequency variations in VCC.

APPLICATION HINTS (CONTINUED)

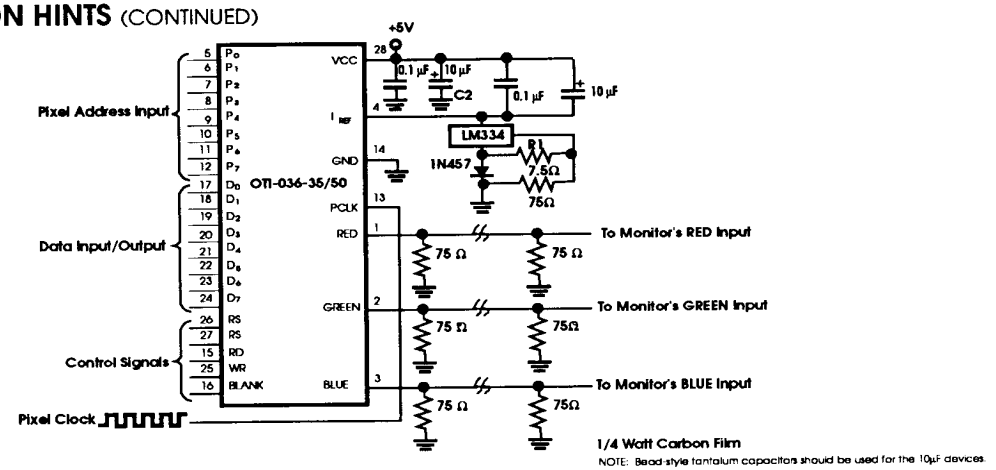


Figure 15. Double Termination with LM334 Current Source IREF Generator.

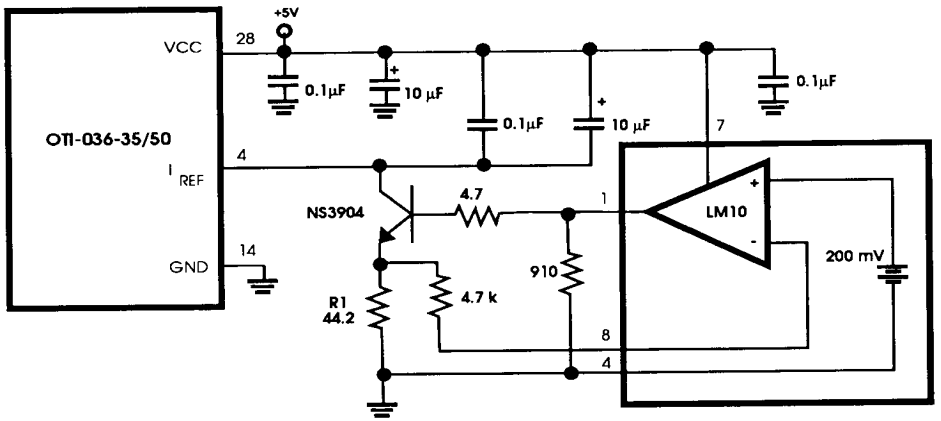


Figure 16. IREF Generator using LM10.

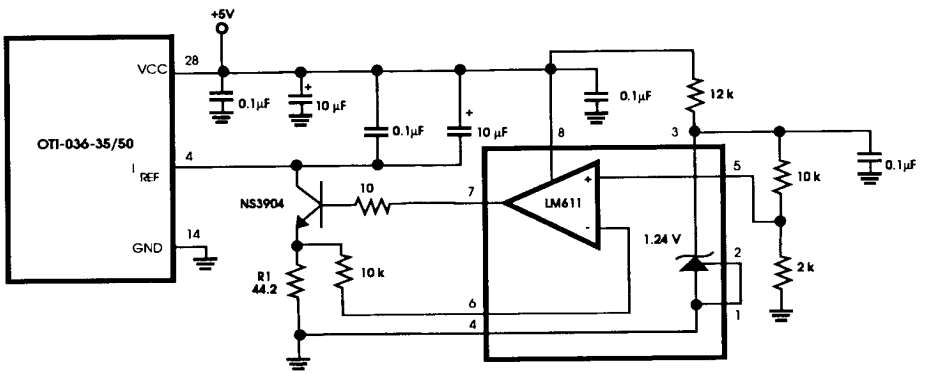


Figure 17. IREF Generator using LM611.