OPTi

OPTi-486SXWB PC/AT Chipset (82C493/82C392/82C206)

Preliminary

82C493/82C392 DATA BOOK

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OPTi, Inc., 2525 Walsh Avenue, Santa Clara, CA 95051 (408) 980-8178 FAX: 408-980-8860

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OPTi, Inc.

2525 Walsh Ave. Santa Clara, California 95051

Tel. (408) 980-8178
Fax (408) 980-8860

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OPTi, Inc., 2525 Walsh Avenue, Santa Clara, CA 95051 (408) 980-8178 FAX: 408-980-8860

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1 486SXWB OVERVIEW (82C493/82C392/82C206 CHIPSET)

1.1 Introduction

The OPTi 486SXWB is a three-chip solution offering optimal performance for high-end, 486DX and 486SX/487SX based AT systems. The OPTi 486SXWB chipset is designed for systems running from 20, 25 and up to 33 Mhz. It includes 82C493 System Controller (SYSC), the 82C392 Data Buffer Controller (DBC), and the 82C206 Integrated Peripheral Controller (IPC). Refer to the data book supplied by your third-party source for information on the 82C206.

1.2 Features

OPTi 486SXWB features include:

- o 1X and 2X clock source, supporting systems running up to 33 Mhz
- o two 160-pin CMOS Plastic Flat Package (PFP), and one 84-pin PLCC
- o Copy-Back Direct-Mapped Cache with size of 64 KB, 128 KB, 256 KB and 512 KB
- o up to 10% performance enhancement from write-through cache scheme
- o supports 2,1,1,1 or 3,2,2,2 cache and DRAM burst cycles respectively
- o on-chip comparator determines cache hit or miss
- o up to 64-MB of local high-speed, page-mode, DRAM memory space
- o burst-line-fill during Cache-Read-Miss
- o control of two non-cacheable regions
- o shadow RAM support
- o optional caching of shadowed Video BIOS
- o hidden refresh
- o slow refresh available for a laptop application.
- o 8042 emulation for fast CPU-reset and gateA20 generation
- o turbo/slow speed selection
- o AT bus clock selectable from CLK2IN/5, CLKIN/3, CLKIN/4 or CLKIN/6
- o 0 or 1 wait state selectable for 16-bit AT bus cycle
- o CAS# before RAS# refresh reduces power consumption
- o optional 0 or 1 wait state for Cache-Write-Hit
- o WEITEK 4167 coprocessor support

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1.3 SYSTEM BLOCK DIAGRAM

Figure 1 is a block diagram of a 486SXWB-based system

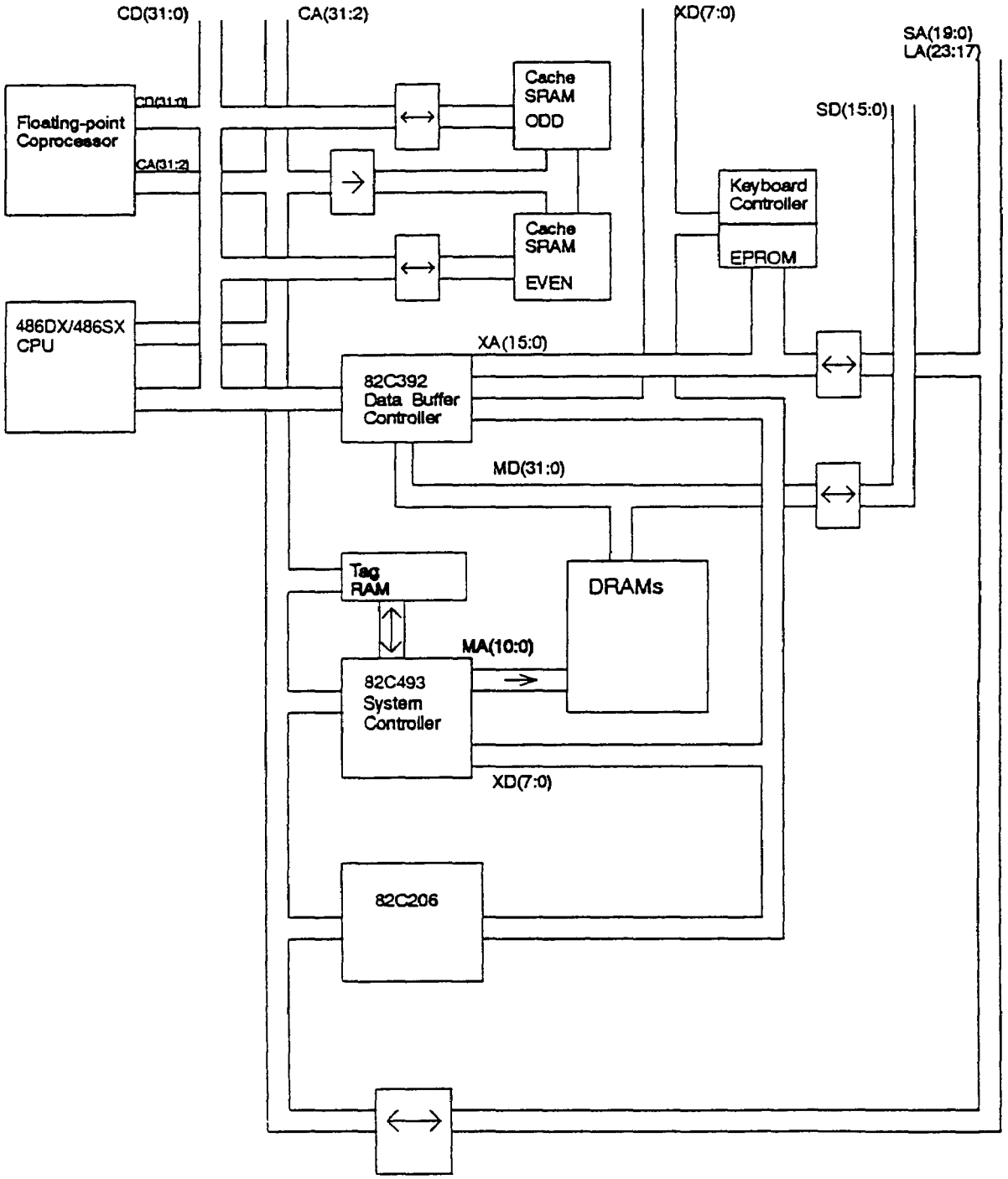

Figure 1. 486SXWB-Based System Block Diagram

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2 82C493 SYSTEM CONTROLLER (SYSC)

2.0 Features

The SYSC is a 160-pin PFP (Plastic Flat Package) device. The SYSC integrates a write-back-cache controller, local DRAM controller, AT bus state machine, and CPU state machine. 82C493 features include:

- o CPU reset control
- o CPU internal cache control
- o CPU burst mode control
- o CPU interface control.
- o integrated write-back cache controller with tag comparator.
- o page-mode DRAM controller
- o burst line fill control logic
- o two noncacheable address comparators
- o decoupling refresh for local DRAM and AT-bus memory
- o 2 DMA upper address latches

2.1 Reset Logic

The SYSC handles two reset inputs, RST1# and RST2#, to generate the CPU reset signal, CPURST. RST1# is a "cold reset" which is generated by the DBC when either PWRGD# (Powergood) goes low (from the power supply and indicating a low power condition) or the system reset button is pressed. RST2# is a "warm reset," asserted by a keyboard reset (CNTL + ALT + DEL simultaneously). Keyboard reset can be handled by either the keyboard controller (8042 or 8742) or the DBC. However, the reset from the DBC is recommended because it routes the reset faster to the SYSC. The reset from the DBC is used in the application system design to optimize the performance.

A software reset is also available by programming bit 0 (from 0b to 1b) of Index Register 20h, then executing a "HALT" instruction.

2.2 System Clock Generation

The SYSC has two high frequency clock inputs, CLKI and CLK2I. In single frequency operation, CLK2I and CLKI are connected to the same clock source. But in double frequency operation, CLK2I is fed by directly from the crystal oscillator and CLKI is derived from the output of divided by 2 flip-flop. So CLK2CLK2I frequency is twice of that of CLKI. CLK2I is used for the cache controller to generate the zero wait cache write cycle. Typically, double frequency is recommended for 20/25 Mhz operation, single or double frequency can be used 33 Mhz system. If single frequency clock is used, the cache write wait state must be set to "1". CLKI, which is driven by the output from a crystal oscillator or from the CLK2I through a divided by 2 circuitry, clocks the CPU as well as the SYSC's internal state machine.

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The SYSC generates the AT bus clock, ATCLK depending on the bit 1 and 0 of index 25h register. When the system is first powered on, bit 1 is cleared to "0" and bit 0 is reflects the pin status of BLCKS. ATCLK can be changed to any of four different speeds by programming the bit 1,0 of index register 25h. The speed can be one of the following; CLKI/4 (0, 1 for bit 1 and 0), CLKI/6 (0, 0 for bit 1 and 0), CLKI/3 (1, 0 for bit 1 and 0) and CLK2I/5(1, 1 for bit 1 and 0). An onboard, 2- position jumper establishes the initial level of BCLKS.

2.3 Cache Subsystem

The cache update scheme of SYSC is the copy-back(write-back) which is a superior scheme than traditional write-through scheme. There is no performance penalty in the cache write cycle, since the cache controller doesn't need to wait for the much slower DRAM controller to finish its cycle before proceeding to next cycle. So it dramatically improve the system performance.

The SYSC only support non-pipeline mode with a fixed 16-byte line size to simplify design without increasing cost or degrading system performance. A tag comparator is built inside the SYSC to improve system performance and reduce system board component count. and real-estate. The comparator asserts internal HIT# signal when the current address location matches the addresses stored inside the Tag RAM.. If HIT# is negated or NCA# (Non-Cacheable Address) is asserted, the current cycle is a cache-miss; otherwise the cycle is a cache-hit. Descriptions of possible cache cycles follow.

Cache-Read-Miss with the cache location's DIRTY bit negated. The cache controller does not need to update system memory with the cache's current data, because that data is unmodified. The cache controller asserts TAGWE#, causing the tag RAMs to update with the new address, and asserts CAWE(3:0)#, causing cache memory to update with data from DRAM.

Cache-Read-Miss with DIRTY bit asserted. The cache controller must update memory with data from the cache location that is going to be overwritten. The controller writes the 16-byte line from cache memory to the DRAM, then reads the new line from DRAM into cache memory. The controller asserts TAGWE# and CAWE(3:0).

Cache-Write-Hit. The cache controller does not need to update memory. The controller updates the tag RAMs and cache memory and sets the DIRTY bit. (DIRTY may already be set, but that does not affect this cycle.)

Cache-Write-Miss. The cache controller bypasses the cache entirely and writes the data directly into DRAM. DIRTY is unchanged.

The following table shows the cache sizes supported by the 82C493, with the corresponding tag RAM address bits, tag RAM size, cache RAM address bits, cache RAM size, and cacheable main memory size

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Cache Size (Kb)	Tag Field Address/ Tag RAM size	Cache RAM Address /Cache RAMs	Cachable Main Memory(Mb)
64	A23 - A16 4KX9	A15 - A4 8 8KX8	16
128	A24 -A17 8KX9	A16 - A4 16 8KX8	32
256	A25 - A18 16KX9	A17 - A4 8 32KX8	64
512	A25 - A19 32KX8	A18 - A4 16 32KX8	64

Speed(Oscillator)	Cache SRAM	Tag SRAM	DRAM*
20Mhz(40 Mhz)	25ns(note 1)	25ns	80ns(note 3)
25Mhz(50 Mhz)	25ns(note 1)	25ns	80ns(note 3)
33MHz(66 Mhz or 33 Mhz)	25ns(note 2)	15ns	80ns(note 3)
50 Mhz(50 Mhz)	20ns	12.5ns	80ns(note 3)

Note:
1: 20/25 Mhz system design can be implemented with or without data buffers for the cache memory. The design without data buffers requires faster output access time for cache SRAM. The SRAM speed listed above is based on the design without data buffers. In 25 Mhz based-system, 25 ns SRAMs with output access time smaller than 13 ns must be used.
2. The SRAM speed is for the design with data buffers and 8KX8 SRAMs are used. If 32KX8 SRAM is used, the .access time must be decreased to 20 ns.
3. DRAM and cache RAM are at their minimum wait states. Cache write at "0" wait state only when double frequency is used.

2.4 CPU Burst Mode Control

SYSC supports secondary cache size from 64KB up to 512 KB to compliment the internal 8KB cache of 486/487SX and 486DX. It greatly enhances the hit ratio of the cache system and dramatically improves the system performance. During the cache operation, that data is burst into the CPU when a cacheable location is read, whether it is a cache read-hit or read-miss. If read-miss occurs, the DRAM data is first burst into cache memory. In the cache read-hit cycle, BRDY# (Burst Ready) is asserted at the middle of the first T2 state when a 2-1-1-1 burst cycle is chosen, otherwise, it is asserted at the middle of the second T2 state.During the read-mis ; BRDY# is asserted after cache memory is updated. Once asserted, BRDY# stays low until BLST# (Burst Last) is detected. BRDY# is never active during DMA and MASTER cycles.

In order to support the cache burst cycle and still use the normal speed SRAM, a bank interleave cache access method is used. The addresses are applied to cache memory one clock cycle earlier, cache output enable signals then enable the cache RAMs to data bus. Since the output enable time is about half of the address access time, SYSC can achieve a cache burst mode and don't need to use more expensive and faster SRAMs in cache sub-system design. SYSC supports one or two pair of cache banks, each pair includes a even and odd bank. The even bank and odd bank share the same addresses lines. Signals

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pairs,BEA3 and BOA3, BEOE# and BOOE#, are used to distinguish the even and bank ccess respectively. If two pair banks are supported, CA16 and CA18 are used to select the corresponding bank.

2.5 Local DRAM Control Subsystem

The SYSC supports up to 4 banks of page-mode local memory. DRAM devices are either 256-Kb,1-Mb or 4-Mb large. Total memory is between 1 Mb and 64 Mb. The following table illustrates the configurations supported.

Bank 0	Bank 1	Bank 2	Bank 3	Total
256K	x	x	x	1M
256K	256K	x	x	2M
1M	x	x	x	4M
256K	1M	x	x	5M
256K	256K	1M	x	6M
1M	1M	x	x	8M
256K	1M	1M	x	9M
256K	256K	1M	1M	10M
1M	1M	1M	x	12M
256K	1M	1M	1M	13M
1M	1M	1M	1M	16M
4M	x	x	x	16M
1M	4M	x	x	20M
4M	1M	x	X	20M
1M	1M	4M	x	24M
1M	4M	1M	x	24M
4M	1M	1M	x	24M
1M	1M	1M	4M	28M
1M	4M	1M	1M	28M
4M	1M	1M	1M	28M
4M	4M	x	x	32M
1M	4M	4M	x	36M
4M	1M	4M	x	36M
4M	4M	1M	x	36M
4M	1M	4M	4M	40M
1M	4M	4M	1M	40M
4M	1M	4M	1M	40M
4M	4M	1M	1M	40M
4M	4M	4M	x	48M
1M	4M	4M	4M	52M
4M	1M	4M	4M	52M
4M	4M	4M	1M	52M
4M	4M	4M	4M	64M

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2.6 Shadow RAM

Because DRAM accesses are much faster than EPROM accesses, the SYSC provides shadow RAM capability to enhance system performance.. BIOS is copied, then write-protected, into a dedicated area in DRAM. Accesses to BIOS address space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h to FFFFFh. C0000h to EFFFFh are enabled in 16-Kb memory chucks. F0000h-FFFFFh, the location of system BIOS shadowing, are enabled in 64-Kb chucks. When shadowing is disabled (bit 7 of Index Register 22h is reset), BIOS is read from EPROM and (if applicable) written to DRAM. Normally, ROMs with address from E0000h - FFFFFh reside on XD bus and ROMCS# is generated. However, ROM with address range from C0000h to DFFFFh are directed to AT bus.

2.7 AT Bus State Machine

The AT state machine monitors status signals, M16#, IO16#, Chrdy and Nows# from the AT bus. The machine outputs AT bus signals, including command, bus conversion, and control. The AT bus state machine also routes data and address when an AT bus master or DMA controller accesses memory.

2.8 Bus Arbitration Logic

82C493 arbitration is based on first-come, first serve basis. The SYSC arbitrates between memory requests from the CPU, DMA controller, AT bus masters, and refresh logic. During DMA and AT bus master write cycles, the SYSC asserts HOLD to the CPU, then the CPU relinquishes bus control, returning HLDA. The SYSC asserts AHOLD and BOFF# during an AT memory code read cycle. During refresh (and when hidden refresh is enabled), HOLD remains negated, and the CPU continues its current program execution as long as it achieves cache hits.

2.9 Refresh Logic

The SYSC supports both normal refresh and hidden refresh. The average refresh period (time between refresh cycles) is either 16us or 64us, the latter when slow refresh is enabled. (Slow-refresh DRAMs must be used with slow refresh.) Hidden refresh separates refreshing of AT-bus memory and local DRAM; the AT-bus controller arbitrates between CPU accesses to the AT bus, DMA, and AT refresh, while the DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycles. Note that the DBC generates the refresh address during AT-bus refresh cycles.

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2.10 System BIOS ROM and I/O Ports

The SYSC supports both 8-bit and 16-bit EPROM cycles. If the system BIOS is eight bits wide, the system BIOS EPROM resides on the XD bus. If the system BIOS is 16 bits wide, the EPROM must reside on the MD bus, and ROMCS# is connected to M16# through a open collector; M16# informs the SYSC that the current system BIOS is 16 bits wide. The XD-bus data buffers always drive toward the XD bus, except during an I/O read cycle at an address smaller than 100h (byte-wide I/O), INTA cycle and an 8-bit BIOS ROM cycle.

2.11 Turbo and Non-Turbo Mode Operation

The system is operating at the full speed if the TURBO pin is asserted high. The non-turbo mode operation is implemented by applying a periodic clock to the FLUSH# pin of 486 processor. The cache flush causes continuous cache update and eventually slows down the whole system throughput. The clock source used is OSC (14.3818 Mhz) from 82C493. For the system design, the TURBO pin must always be pulled high through a 10K Ohm resistor.

2.12 Flexible Multiplexed DRAM Address

The following table describes how the DRAM address lines are multiplexed when different memory devices types are used.

Address to MA bus Mapping

Mem addr	256K		1M		4M	
	Col	Row	Col	Row	Col	Row
MA0	A2	A12	A2	A12	A2	A23
MA1	A3	A13	A3	A13	A3	A13
MA2	A4	A14	A4	A14	A4	A14
MA3	A5	A15	A5	A15	A5	A15
MA4	A6	A16	A6	A16	A6	A16
MA5	A7	A17	A7	A17	A7	A17
MA6	A8	A18	A8	A18	A8	A18
MA7	A9	A19	A9	A19	A9	A19
MA8	A10	A11	A10	A20	A10	A20
MA9	X	X	A11	A21	A11	A21
MA10	X	X	X	X	A12	A22

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3 SYSC SIGNALS DESCRIPTIONS

3.1 Clock and Reset

Name	Type	Pin No	Description
CLK2I	I	82	Crystal oscillator Input which has a frequency equal to twice the rated CPU clock if double clock scheme is chosen. This signal is used for secondary cache early write option only.
CLKI	I	79	Single clock input for SYSC internal state machine.
BCLKS	I	142	ATCLK Selection. Low ATCLK = CLKI/6. High ATCLK = CLKI/4.
ATCLK	O	159	ATCLK to AT bus; it is a free running clock. It could be one of following clock:CLKI/4, CLKI/6, CLKI/3 and CLK2I/5.
RST1#	I	134	Cold reset input either from Powergood signal of power supply or from Reset Switch
RST2#	I	135	CPU Reset input from Keyboard Controller or from DBC's ERST2# pin.
CPURST	O	25	Reset for 486 processor.

3.2 CPU Interface

Name	Type	Pin No	Description
CA(31:24)	B	88-83,68-67	CPU Address Lines 31-24. They are input pins during CPU cycle, and forced to be low for DMA and MASTER cycles which allow 486 invalidating the internal TAGs. Note that the CPU isn't on HOLD when AT refresh cycle undergoing.
CA(23:21)	I	66-64	CPU Address Lines 23-21; Input only.
CA20	B	63	CPU Address Lines 20; it's an input pin during CPU and DMA cycles, and becomes an output pin during MASTER cycle.
CA(19:17)	I	62-60	CPU Address Lines 19-17; Input only.
CA(16:8)	B	59-51	CPU Address Lines 16-8. These are input pins during CPU and MASTER cycles. CA(16:9) are output pins for DMA address A16-A9 by latching XD(7:0) during 16-bit DMA cycle and CA(15:8) are DMA address A15-A8 for 8-bit DMA cycle.

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Name	Type	Pin No	Description
CA(7:2)	I	49-44	CPU Address Lines 7-2; Input only.
BE(3:0)	B	31-34	Byte Enable 3-0. These are inputs during CPU cycle and are outputs during DMA and MASTER cycle, derived from SA0, SA1 and SBHE# from AT bus.
ADS#	I	43	Status input from CPU. This active low signal indicates that CPU is starting a new cycle.
WR#	I	36	CPU Write or Read Cycle Status. It indicates a write cycle if high and read cycle if low.
DC#	I	35	CPU Data or Code Cycle Status. It indicates data transfer operations when high, or control operations(code fetch, halt, etc.) when low.
MIO#	I	37	CPU Memory or I/O Cycle Status. It indicates a memory cycle if high, and I/O cycle if low.
LDEV#	I	18	Indication of CPU local Bus device Cycle, i.e. WEITEK 4167 coprocessor. This signal is sampled at the end of 1st T2.
BLST#	I	42	486 burst last cycle indication, SYSC terminates the burst cycle as long as the BLST# sampled low at the end of each T2 when BRDY# is active.
RDY#	O	38	Ready output for CPU to terminate the current cycle.This pin is not a tri-state output.
RDYI#	I	19	Local Device Ready Input, It will be synchronized by SYSC before sending to CPU.
BRDY#	O	39	Burst ready output for CPU to sample the read data during burst cycles. This pin is a tri-state output.
KEN#	O	29	Cachable or non-cachable status for the internal cache of CPU. This signal is low normally, and is brought high at the end of T1. SYSC will assert KEN# again if it is a cachable cycle.
BOFF#	O	27	Backoff output for CPU. This output forces the 80486 microprocessor to float its bus in the next clock and restart the cycle later.
TURBO	I	140	Turbo Mode Selection. I f Turbo pin is tied to high; the system runs at full speed. This pin is recommended to be always tied to high.
TLB#	O	110	i486 B stepping TLB corruption Problem Fix. This pin is not needed if C or later stepping of processor is used.

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3.3 Numeric Processor Interface

Name	Type	Pin No	Description
NPERR#	I	24	Numeric Processor Error Indication. Used to generate IGERR# for CPU.
IGERR#	O	21	This is a normally high signal and will become low as soon as the NPERR# is asserted. An IO write to either port F0h or F1h, or CPU reset will force this signal back to high.

3.4 External Cache Control

Name	Type	Pin No	Descriptions
TAG(7:0)	B	77-71,69	TAG RAM input/output Lines 7-0.
DRTY	B	78	Dirty Bit of Tag RAM to indicate its corresponding line has been written into.
TAGWE#	O	93	TAG RAM Write Enable. It is used to update the TAG RAM.
DTYWE#	O	94	Write strobe to Dirty Bit of TAG RAM
CAOE#	O	89	External Cache Output Enable.
CAWE(3:0)#	O	105-102	External Cache Write Enable; each signal corresponds to one byte of data
BECS#	O	91	External Cache Even Bank Chip Select; it is normally active and becomes high if CA2 is high during cache write hit cycle. Also it will toggle during cache line fill cycle.
BOCS#	O	92	External Cache Odd Bank Chip Select; it is normally active and becomes high if CA2 is low during cache write hit cycle. It will be a complement of BECS# during cache line fills.
BEOE#	O	98	External Cache Even Bank Data Buffers Enable; Activated for cache write cycle and, if CA2 is low, cache read cycle. Also, toggles during dirty write backs and CPU burst reads.
BOOE#	O	97	External Cache Odd Bank Data Buffers Enable. It is activated for cache write cycle and, if CA2 is high, cache read cycle. It will become a complement of BEOE# during dirty write back and CPU burst read cycle.

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Name	Type	Pin No	Description
BDIR#	O	96	External Cache Data Buffers Direction Control. It is normally high and forced to be low when writing data into cache.
BEA3	O	101	External Cache Even Bank Address Bit 3.It is tri-stated during T1 and first half T2 cycle. Then it simply reflects the status of CA3 and will toggle during dirty write back, cache line fill, and CPU burst read cycles.
BOA3	O	99	External cache oven bank address bit 3.It is tri-stated during T1 and first half T2 cycle. Then it reflects the status of CA3 and will toggle during dirty write back, cache line fill, and CPU burst read cycles.
CA3S#	O	95	External cache address bit 3 select; use this signal to choose between CA3 and BEA3 for even bank cache address bit 3, or BOA3 for odd bank cache address bit 3 respectively. becomes active for T1 and first T2 cycles.

3.5 Local DRAM Interface

Name	Type	Pin No	Description
DWE#	O	133	DRAM Write Enable signal.
RAS(3:0)#	O	132,131,129, 128	DRAM Row Address Strobe.
CAS(3:0)#	O	127-124	DRAM Column Address Strobe.
MA(10:0)	O	123,122, 119-111	DRAM Row/Column Address Line 10-0.

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3.6 DBC Interface

Name	Type	Pin No	Description
LMEN#	O	109	Local Memory Access Indication. Used by DBC to control the data bus flow.
DLE	O	107	DRAM Read Data Latch Enable; used for parity checking.
MIO16#	O	143	Latched AT-bus 16-bit Slave Status; used for bus conversion.
PCKEN#	O	106	Parity Checking Enable; used by DBC to perform parity checking.
ATCYC#	O	154	AT bus Cycle Indication.

3.7 Bus Arbitration

Name	Type	Pin NO	Description
HRQ	I	145	DMA or Master Cycle Request from 82C206
OUT1	I	146	Refresh Request from Timer1 Output.
HLDA	I	41	CPU Hold Acknowledge.
ADS8	I	152	8-bit DMA Transfer Address Strobe. The SYSC has to latch XD(7:0) by using ADS8 and translate to CA(15:8) outputs.
AEN8#	I	147	8-bit DMA Cycle Indication.
ADS16	I	153	16-bit DMA Transfer Address Strobe. The SYSC has to latch XD(7:0) by using ADS16 and translate to CA(16:9) outputs.
AEN16#	I	148	16-bit DMA Transfer Indication.
HOLD	O	28	HOLD Request to CPU. Hidden refresh will not hold the CPU.
HLDA1	O	7	DMA or Master Cycle Granted Notice.
RFSH#	B	158	AT Refresh Cycle Indication. It is an input pin during master or DMA cycle.
AHOLD	O	22	Address hold request to CPU; It will be activated when HLDA is active and CPURST isn't active, or right after AT memory code read cycle if HOLD is pending. AHOLD will last until HOLD ends.
EADS#	O	23	486 address snooping strobe; it's asserted for two T states during DMA or MASTER cycles.

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3.8 AT-BUS Interface

Name	Type	Pin No	Description
XA0	B	156	System Address Line 0. Input during master or 8-bit DMA cycles; output pin during CPU, 16-bit DMA, or refresh cycle.
XA1	B	157	System Address Line 1, it is an input pin during master or DMA cycle; becomes output pin during CPU or refresh cycle.
CHRDY	I	139	Channel Ready Input from AT-BUS. Schmitt trigger input pin.
NOWS#	I	138	Zero Wait State Input from AT-BUS. It is a Schmitt trigger input pin. The system BIOS ROM is treated as AT one wait state cycle.
IO16#	I	137	16-bit IO Slave Cycle Status. It is a Schmitt trigger input pin.
M16#	I	136	16-bit Memory Slave Cycle Status; Schmitt trigger input pin.
GATEA20	I	141	Gate A20 Input from 8042 or DBC emulated gateA20 pin. By default, SYSC uses this signal to qualify CA20 during CPU cycle.
A20M#	O	26	GateA20 ANDed with fast GATEA20 output to CPU; it will remain high during power up CPU reset period.
XD(7:0)	B	9-11,13-17	Peripheral Data Bus Line 7-0.Two purposes for these pins: program the internal index register.* latch the DMA high order address.
IORD#	B	4	AT IO Read Command. It is an input pin during DMA or master cycle.
IOWR#	B	5	AT IO Write Command. It is an input pin during DMA or master cycle.
MRD#	B	2	AT Memory Read Command. It is an input pin during DMA or master cycle.
MWR#	B	3	AT Memory Write Command. It is an input pin during DMA or master cycle.
SMRD#	O	149	AT Memory Read Command, for address below 1 Meg. It has to be activated during refresh cycle.
SBHE#	B	155	AT Bus High Enable. It is an input pin during master cycle.
SMWR#	O	151	AT Memory Write Command, for address below 1 MB memory space.
ALE	O	6	AT Bus Address Latch Enable to represent that the AT cycle has started. It is brought to high during non-CPU cycle.
INTA	O	144	Interrupt Acknowledge Cycle Indication. Hold will not send to CPU between the INTA* cycles.
ROMCS#	O	8	System BIOS ROM Output Enable. System BIOS ROM accessing could be either 8-bit or 16-bit. This signal will be asserted from the end of the first T2 to the end of the last T2.

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3.9 Ground and VCC

Name	Type	Pin No	Description
VCC	I	1,20,40,81,100,120	+5V
GND	I	12,30,50,70,80,90,108,121,130,150,160	VSS or Ground

4 SYSC REGISTERS DESCRIPTIONS

There are twelve configuration registers inside the 82C493. An indexing scheme is used to access all the registers of OPTi-486SXWB chipset. Port 22h contains the index register and port 24h is the data register. The index resets after every access; thus, every data access (via port 24h) must be preceded by a write to port 22h, even if the same register is being accessed. Unless mentioned otherwise, all reserved bits are set to zero by default and must be set to zero for future compatibility purpose.

Control Register 1
Index: 20h

BIT	FUNCTION	DEFAULT
7-6	Revision of 82C493 and is read-only.	01
5	Burst wait state control 1 = Secondary cache read hit cycle is 3-2-2-2 or 2-2-2-2. 0 = Secondary cache read hit cycle is 3-1-1-1 or 2-1-1-1. **If bit 5 is set to "1", bit 4 of index 20h must be set to "0".**	0
4	Cache memory data buffer output enable control 0 = disable 1 = enable When enabled, it will be activated half T state earlier during read hit cycle. **Bit 4 must be set "0" for frequency smaller than or equal to 33 Mhz. Otherwise, it must be set to "1".**	0
3	Single ALE Enable- SYSC will activate single ALE instead of multiple ALEs during bus conversion cycle if this bit is enabled. 0 =disable 1 =enable	0
2	Extra AT Cycle Wait State Enable. Insert one extra wait state in standard AT bus cycle. 0 = disable 1 =enable	0
*1	Emulation keyboard Reset Control - turn on this bit requires "Halt" instruction to be executed before SYSC generates CPURST. 0 =disable 1= enable **Note: This bit must be set to "1" in BIOS default value.**	0
0	Fast Reset Enable- alternative fast CPU reset. 0 = disable 1 =enable	0

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Control Register 2
Index: 21h

BIT	FUNCTION	DEFAULT
7	Master Mode Byte Swap Enable 0 = disable 1 = enable	0
6	Emulation Keyboard Reset Delay Control 0 = Generate reset pulse 2 us later 1 = Generate reset pulse immediately	0
5	Parity Check 0 = enable 1 =disable	0
4	Cache Enable 0 = Cache is disabled and DRAM burst mode is enabled 1 = Cache enable and DRAM burst mode is disabled	0.
3-2	Cache Size 3 2 Cache Size 0 0 64KB 0 1 128KB 1 0 256KB 1 1 512KB	00
1	Secondary Cache Read Burst Cycles Control 0 = 3 - 1 - 1 - 1 Cycle 1 = 2 - 1 - 1 - 1 Cycle	0
0	Cache Write Wait State Control 0 = 1 Wait state 1 = 0 Wait state	0

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Shadow RAM Control Register I
Index: 22h

BIT	FUNCTION	DEFAULT
7	ROM(F0000-FFFFFh) Enable 1 = read from ROM, write to DRAM. ROMCS# is generated during read access only. 0 = read/write on DRAM and DRAM is write-protected	1
6	Shadow RAM at D0000h - DFFFFh Area 0 = Disable 1 = Enable	0
5	Shadow RAM at E0000h - EFFFFh Area 0 = Disable shadow RAM, enable ROMCS# . The E0000-EFFFFh ROM is defaulted to reside on XD bus. 1 = Enable shadow RAM and disable ROMCS# generation	0
4	Shadow RAM at D0000h - DFFFFh Area Write Protect Enable 0 = Disable 1 = Enable	0
3	Shadow RAM at E0000h - EFFFFh Area Write Protect Enable 0 = Disable 1 = Enable	0
2	Hidden refresh enable (without holding CPU) 1 = Disable 0 = Enable. * **Please see the following note**.	1
1	Unused Bit	0
0	Slow Refresh Enable (4 times slower than the normal refresh) 0 = Disable 1 = Enable	0

Note: Hidden refresh must be disabled if 4MX1 or 1 MX4 bit DRAM are used.

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Shadow RAM Control Register II
Index: 23h

BIT	FUNCTION	DEFAULT
7	Shadow RAM at EC000h-EFFFFh area 0 = Disable 1 = Enable	0
6	Shadow RAM at E8000h-EBFFFh area 0 = Disable 1 = Enable	0
5	Shadow RAM at E4000h-E7FFFh area 0 = Disable 1 = Enable	0
4	Shadow RAM at E0000h-E3FFFh area 0 = Disable 1 = Enable	0
3	Shadow RAM at DC000h-DFFFFh area 0 = Disable 1 = Enable	0
2	Shadow RAM at D8000h-DBFFFh area 0 = Disable 1 = Enable	0
1	Shadow RAM at D4000h-D7FFFh area 0 = Disable 1 = Enable	0
0	Shadow RAM at D0000h-D3FFFh area 0 = Disable 1 = Enable	0

DRAM Control Register I
Index: 24h

BIT	FUNCTION	DEFAULT
7	0 = 256 K DRAM mode 1 = 1M and 4 M DRAM mode. See the following table	1
6-4	DRAM types used for bank0 and bank1. See the following table	000
3	Unused	0
2-0	DRAM types used for bank 2 and bank 3. See the following table.	111

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Bits 7 6 5 4	Bank 0	Bank 1
0 0 0 0	256K	X
0 0 0 1	256K	256K
0 0 1 0	256K	1M
0 0 1 1	X	X
0 1 X X	X	X
1 0 0 0	1M	X
1 0 0 1	1M	1M
1 0 1 0	1M	4M
1 0 1 1	4M	1M
1 1 0 0	4M	X
1 1 0 1	4M	4M
1 1 1 X	X	X

Bits 7 2 1 0	Bank 2	Bank 3
X 0 0 0	1M	X
X 0 0 1	1M	1M
X 0 1 0	X	X
X 0 1 1	4M	1M
X 1 0 0	4M	X
X 1 0 1	4M	4M
X 1 1 X	X	X

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DRAM Control Register II
Index: 25h

BIT	FUNCTION	DEFAULT
7-6	Read cycle wait state 7 6 Additional wait States 0 0 Not used 0 1 0 1 0 1 1 1 2 Note: Base wait states is "3".	11
5-4	Write cycle wait state 5 4 Additional wait states 0 0 0 0 1 1 1 0 2 1 1 3 Note: Base wait states is "2".	11
3	Fast decode enable. This function may be enabled in 20/25 Mhz operation to speed up the DRAM access. 0 = Disable fast decode, DRAM base wait states is not changed 1 = Enable fast decode, DRAM base wait states is decreased by 1 This bit is automatically disabled even when it is set to 1 when bit 4 of Index register 21h(cache enable bit) is enabled.	0
2	unused	0
1-0	ATCLK selection, bit 0 will reflect the BCLKS pin status and bit 1 will be set to 0 when 82C493 is reset. Bit 0 is 0 if BCLKS is tied to low and 1 if BCLKS is high. 1 0 ATCLK selection 0 0 ATCLK = CLKI/6(Default) 0 1 ATCLK = CLKI/4(Default) 1 0 ATCLK = CLKI/3 1 1 ATCLK = CLK2I/5	00 or 01 depending on the low or high state of BCLKS respectively during power on reset

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Shadow RAM Control Register III
Index: 26h

BIT	FUNCTION	DEFAULT
7	Not used	0
6	Shadow RAM copy enable for address area C0000h-CFFFFh 0 = Read/write at AT bus 1 = Read from AT bus and write into shadow RAM	0
5	Shadow write protect at address area C0000h-CFFFFh 0 = Write protect disable . 1 = Write protect enable	0
4	Shadow RAM enable at C0000h- CFFFFh area 0 = Disable 1 = Enable	0
3	Enable shadow RAM at CC000h-CFFFF area 0 = Disable 1 = Enable	0
2	Enable shadow RAM at C8000h-CBFFF area 0 = Disable 1 = Enable	0
1	Enable shadow RAM at C4000h-C7FFFh area 0 = Disable 1 = Enable	0
0	Enable shadow RAM at C0000h-C3FFFh area 0 = Disable 1 = Enable	0

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Control Register 3
Index: 27h

BIT	FUNCTION	DEFAULT
7	Enable NCA# pin to low state, 0=Disable 1 =Enable	1
6-5	Unused	00
4	Video BIOS at C0000h-C8000h area non-cacheable 0 = Cacheable 1 = Non-cacheable	1
3-0	Cacheable address range for local memory, see following table	0001

Note. Memory area at 640K-1M is defaulted to be non-cacheable.

Bits 3 2 1 0	Cachable Address range
0 0 0 0	0 - 64 Mb
0 0 0 1	0 - 4 Mb
0 0 1 0	0 - 8 Mb
0 0 1 1	0 - 12 Mb
0 1 0 0	0 - 16 Mb
0 1 0 1	0 - 20 Mb
0 1 1 0	0 - 24 Mb
0 1 1 1	0 - 28 Mb
1 0 0 0	0 - 32 Mb
1 0 0 1	0 - 36 Mb
1 0 1 0	0 - 40 Mb
1 0 1 1	0 - 44 Mb
1 1 0 0	0 - 48 Mb
1 1 0 1	0 - 52 Mb
1 1 1 0	0 - 56 Mb
1 1 1 1	0 - 60 Mb

Note: If total memory is 1 Mb or 2Mb, the cacheable range is 0 - 1 or 0 - 2Mb respectively and independent of the value of bit 0-3 of index register 27h. .

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Non-cachable Block 1 Register
Index: 28h

This register is used in conjunction with Index 29h register to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512 KB non-cacheable block is selected, its starting address is a multiple of 512 KB; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

BIT	FUNCTION	DEFAULT
7-5	Size of non-cachable memory block 1, See following table	100
4-2	Unused	000
1-0	Address bits of A25 and A24 of non-cachable memory block 1	00

7 6 5	Block Size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 x x	Disabled

Non-cachable Block 1 Register II
Index: 29h

BIT	FUNCTION	Default
7-0	Address bits A23-A16 of non-cachable memory block 1	0001xxxx

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

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Non-cachable Block 2 Register I
Index: 2Ah

This register is used in conjunction with Index 2Bh register to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512 Kb non-cacheable block is selected, its starting address is a multiple of 512 Kb; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

BIT	FUNCTION	DEFAULT
7-5	Size of non-cacheable memory block 1, See following table	100
4-2	Unused	000
1-0	Address bits of A25 and A24 of non-cachable memory block 1	00

7 6 5	Block Size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 x x	Disabled

Non-cachable Block 1 Register II
Index: 2Bh

BIT	FUNCTION	Default
7-0	Address bit A23-A16 of non-cachable memory block 1	0001xxxx

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

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5 82C392 DATA BUFFER CONTROLLER(DBC)

The DBC is a 160-pin PFP (Plastic Flat Package) device. The DBC integrates data buffers, AT bus control, decode logic for an external keyboard controller, reset logic, and clock generation logic.. It performs the following functions:

- o data bus conversion
- o parity generation/detection
- o AT-BUS direction control
- o reset logic
- o clock source for 206 and 8042
- o chip select for keyboard controller and RTC
- o speaker control
- o port B, 70H and NMI Logic
- o floating-point coprocessor interface
- o keyboard reset and gate A20 emulation logic

5.1 Data Bus Conversion

The DBC performs data bus conversion when the CPU accesses 16- or 8-bit devices through 32- and 16-bit instructions. The DBC also handles DMA and AT bus master cycles that transfer data between local DRAM or cache memory and locations on the AT bus. The DBC provides all of the signals necessary to control external bidirectional data buffers.

5.2 Parity Generation/Detection Logic

During local DRAM write cycles, the DBC generates a parity bit for each byte of write data from the processor. Parity bits are stored into dedicated local DRAM. Within the timing window of "PCKEN" during a DRAM read, the DBC checks if each parity bit is correct for its corresponding data byte. If it detects incorrect parity, the DBC generates a parity error. The parity error will cause the NMI interupt if parity check bit(bit 5 of index 21h) is set to 1.

5.3 Clock Generation and Reset Control

The DBC provides the clock sources for timer 1 of the 80C206 and for the 8042 keyboard controller to reduce the components count. The clocks are derived from 14.3 Mhz. The 00C206 clock is 1.19 Mhz. (14.3Mhz divided by 12). The 8042 clock is 7.15 Mhz. (14.3Mhz divided by 2.) The DBC also monitors both the PWGD# (Powergood) signal from power supply and the reset signal, RST1. from the reset switch. The DBC routes RST1 to the SYSC to generate the "cold reset". The DBC can also supply the RST2 keyboard controller "warm reset" sequence, or RST2 can come from the keyboard controller. The reset sequence is much faster when the DBC supplies RST2.

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5.4 Floating-Point Coprocessor Interface

The DBC monitors NPERR# and NPBUSY# to provide support for 387 and 3167 floating-point coprocessors. (The 486 has an internal coprocessor and does not need this support.) A coprocessor asserts NPERR# during a power on reset. to indicate it is there.. The coprocessor asserts NPBUSY# while executing a floating-point calculation, and asserts READY# when it is finished. If NPBUSY# is active and a coprocessor error occurs (the coprocessor asserts NPERR#), the DBC latches NPBUSY# and generates INT13. INT13 also come from WINT# from the Weitek 3167 coprocessor. Latched BUSY# and INT13 can be cleared by a I/O port F0H write command.

6 82C392 (DBC) PIN DESCRIPTIONS

6.1 Clock and Reset

Name	Type	Pin No	Description
OSCX1	I	43	14.3 Mhz osc. input.
OSCX2	O	42	14.3 Mhz osc. output.
OSC	O	82	14.3 Mhz osc. Output to AT bus.
OSC12	O	83	1.19 Mhz output to 206
OSC2	O	85	14.3 Mhz/2 output for 8042 clock.
OSC2#	O	84	14.3 Mhz/2 inverted output for 8042 clock.
PWGD#	I	16	Power Good Status from power supply. It is buffered through a Schmitt-trigger gate.
RSTSW	I	4	Reset Switch Input. It is buffered through a Schmitt-trigger gate.
RST1#	O	10	Power-up or cold Reset signal derived from PWGD# or RSTSW.

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6.2 Address and Data Buses

Name	Type	Pin No	Description
D(31:23)	B	79-71	CPU Data Bus
D(22:14)	B	69-61	CPU Data Bus
D(13:5)	B	59-51	CPU Data Bus
D(4:0)	B	49-45	CPU Data Bus
A(9:0)	I	119-110	Buffered AT SA (9:0) address lines.
SBHE#	I	25	Byte High Enable from AT bus and SYSC.
BE(3:0)#	I	39-36	CPU Byte Enables; used for data bus parity checking of valid byte.
MD(31:26)	B	156-151	Local DRAM Data Bus.
MD(25:17)	B	149-141	Local DRAM Data Bus
MD(16:8)	B	139-131	Local DRAM Data Bus
MD(7:0)	B	129-122	Local DRAM Data Bus
MP(3:0)	B	2,159-157	Local DRAM data bus Parity Bits.
XD(7:4)	B	104-101	XD Data Lines 7-4.
XD(3:0)	B	99-96	XD Data Lines 3-0.

6.3 Bus Arbitration

Name	Type	Pin No	Description
HLDA	I	32	Hold Acknowledge from CPU in response to hold request.
AEN8#	I	28	8-bit DMA Cycle Indication.
AEN16#	I	27	16-bit DMA Cycle Indication.
AEN#	O	106	DMA Cycle Indication.
MASTER#	I	26	Master Cycle Indication.
RFSH#	I	24	Refresh Cycle Indication.

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6.4 SYSC Interface

Name	Type	Pin No	Description
INTA#	I	23	Interrupt Acknowledge; for data flow direction.
ROMCS#	I	22	System BIOS ROM Chip Select,, used to direct the data bus flow.
LMEN#	I	21	Local Memory Enable. Indicate the current cycle is local DRAM Access. It is used to control the bus direction.
WR#	I	31	CPU Write or Read Cycle Indication.
DLE	I	17	DRAM Read Data Latch, used to latch the data for parity checking.
DWE#	I	3	DRAM Write Enable, to enable DRAM write.
ATCYC#	I	15	AT Cycle Indication. If asserted, the current access is AT bus cycle.
PCKEN#	I	18	Parity Checking Enable, to enable the Parity error signal if any.
MIO16	I	30	16-bit slave devices access indication. It is used to control the data flow path.
IOWR#	I	11	AT bus I/O Write Command.
IORD#	I	12	AT bus I/O Read Command.
MEMRD#	I	14	AT bus Memory Read Command.
MEMWR#	I	13	AT bus Memory Write Command.

6.5 Floating-Point Coprocessor Interfaces

* Note these signals won't be necessary if 486 processor is used.

Name	Type	Pin No	Description
NPERR#	I	87	Error from the coprocessor. It is an active low input indicating that an unmasked error happens.
NPBUSY#	I	88	Busy from the coprocessor to indicate a coprocessor instruction is under execution.
NPRST	O	89	Reset Numeric Processor
BUSY#	O	34	Latched Coprocessor Busy Output to 80386 to indicate a NPBUSY# or NPERR# signals has occurred.
BSYTOG#	I	9	Busy Toggled Control; used to toggle the BUSY# signal when the coprocessor is not installed.

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Name	Type	Pin No	Description
INT13	O	91	Coprocessor Interrupt; is an active high output. It is an interrupt request from numeric coprocessor and connected to IRQ13 of interrupt controller.
ERR#	O	33	Error signal to 80386. It reflect the NPERR# signal during the period from RST4# active to first ROMCS#.
WINT	I	92	Weitek 3167 Co-processor Interrupt Request.
PREQI	I	90	80387 coprocessor Request Input.
PREQO	O	35	Numeric Processor Request to 80386.

6.6 Miscellaneous Signals

Name	Type	Pin No	Description
KBDCS#	O	105	Keyboard Controller Chip Select.
NMI	O	95	Non-maskable Interrupt; due to parity error from local memory or AT bus channel check.
SPKD	O	8	Speaker Data Output, derived from the function of OUT2 and port 61H bit1.
GATE2	O	93	Timer 2 Gate Control.
ASRTC	O	94	Real Time Clock Address Strobe.
CHCK#	I	29	AT-BUS Channel Check.
OUT2	O	44	Timer 2 output.
FAST	I	5	FAST is an active high input which will enable the emulation of Fast GATEA20 and Reset Control Enable.
EGTA20	O	7	GateA20 output. It is generated by emulating Keyboard GATEA20.
ERST2#	O	6	RST2# output. It is generated by emulating keyboard RST2#.
M16#	O	19	Master Access Local DRAM invalidation.
SDEN#	O	107	MD-bus to SD-bus Buffer Enable Signal.
SDIR1#	O	109	MD(7:0) to SD(7:0) Buffer Direction Control.
SDIR2#	O	108	MD(15:8) to SD(15:8) Buffer Direction Control.

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6.7 Ground and VCC

Name	Type	Pin No	Description
VCC	I	20,60,86,100,140	+5V
GND	I	1,40,41,50,70,80,81,120,121,130,150,160	VSS or Ground

7 82C392(DBC) REGISTERS DESCRIPTIONS

Control Register Index 21h(write only)

Bit 7-4 is a duplication of control register index 21h of 82C491.
Bit 3-0 are not used.

I/O Port 60h

Port 60h and 64h emulate the registers of a keyboard controller, allowing the generation of a fast gate A20 signal. The sequence here is BIOS transparent, and there is no need for the modification of the current BIOS. The fast gate A20 generation is enabled when the "Fast" pin is wired high. The sequence involves writing data D1h to port 64h, then writing data 02h to port 60h.When "Fast" is asserted, I/O port 60h indicates the status of a system reset (bit 0) and gate A20 (bit 1).

I/O Port 61h(Port B)

Bit	Read/Write	Function
0	R/W	Timer 2 Gate.
1	R/W	Speaker Output Enable.
2	R/W	Parity Check Enable.
3	R/W	I/O Channel Check Enable.
4	R	Refresh Detect.
5	R	Timer OUT2 Detect.
6	R	I/O Channel Check.
7	R	System Parity Check.

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I/O Port 64h

I/O port 64h emulate the register inside a keyboard controller by generating a fast reset pulse. Writing data FEh to port 64h asserts the reset pulse. The pulse is generated immediately after the I/O write if bit 6 of Index 21h is set, otherwise the pulse is asserted 2us after the write.

Port 70h

Bit	Read/write	Function	Polarity
7	R/W	NMI Enable	0

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82C493/82C392 Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	70	C
Tstg	Storage Temperature	-40	125	C

Note : Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

82C493/82C392 DC Characteristics

Temperature: 0c to 70c, Vcc: 5V +/- 5%

Sym	Description	Min	Max	Units
Vil	Input Low Voltage	-0.5	0.8	V
Vih	Input High Voltage	2.0	5.5	V
Vol	Output Low Voltage (Iol = 4.0 mA)		0.4	V
Voh	Output High Voltage (Ioh = -1.6 mA)	2.4		V
Iil	Input Leakage Current (Vin = Vcc)		10	uA
Ioz	Tristate Leakage Current		10	uA
Cin	Input Capacitance		20	pF
Cout	Output Capacitance		20	pF
Icc	Power Supply Current		80	mA

Temperature : 0C to 70C, Vcc : 5V +/- 5%

Sym	Description	Min	Typ	Max	Units
t101	NPRST active delay from CLKI^		10		ns
t102	NPRST inactive delay from CLKI^		10		ns
t103	CPURST active delay from CLKI^		10		ns
t104	CPURST inactive delay from CLKI^		10		ns
t201	CAS* active to RAS* 0,3 active delay	10		20	ns
t202	CAS* inactive to RAS*0,3 inactive delay	10		20	ns
t203	RAS*0,3 active to RAS*1,2 active delay		15		ns
t204	RAS*0,3 inactive to RAS*1,2 inactive delay		15		ns
t301	D(31:0) valid to XD(7:0) valid delay	8		20	ns
t302	D(31:0) valid to MP(3:0) valid delay	8		18	ns
t303	D(31:0) invalid to XD(7:0) invalid delay	8		18	ns
t304	D(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t305	D(31:0) valid to MD(31:0) valid delay	8		18	ns
t306	D(31:0) invalid to MD(31:0) invalid delay	8		18	ns
t307	MD(31:0) valid to D(31:0) valid delay	8		18	ns
t308	MD(31:0) invalid to D(31:0) invalid delay	8		18	ns
t309	MD(31:0) valid to MP(3:0) valid delay	8		18	ns
t310	MD(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t311	MD(31:0) and MP(3:0) setup time to DLE inactive	6			ns
t312	MD(31:0) and MP(3:0) hold time to DLE inactive	6			ns
t313	A(9:0) to KBDCS* active delay	5		30	ns
t314	A(9:0) to KBDCS* inactive delay	5		30	ns
t315	DRD* active to MD(31:0) valid delay	6		20	ns
t316	DRD* inactive to MD(31:0) invalid delay	6		20	ns
t317	DRD* active to D(31:0) valid delay	6		20	ns
t318	DRD* inactive to D(31:0) invalid delay	6		20	ns
t319	MD(15:0) setup time to IORD*/MEMRD*^	6			ns
t320	MD(15:0) hold time to IORD*/MEMRD*^	6			ns
t321	MD(15:8) valid to MD(7:0) valid delay	8		18	ns
t322	MD(15:8) invalid to MD(7:0) invalid delay	8		18	ns
t401	CPU address and status valid to CAOE* active delay		18	23	ns
t402	CPU address and status valid to BEOE* acitve delay		18	23	ns
t403	CLKI^ to BEOE* /BOOE* inactive delay		12	18	ns
t404	CLKI^ to BOOE* active delay		12	18	ns
t405	CLKI^ to BDIR* inactive delay		15	22	ns
t406	CPU address and status valid to BDIR* active delay		16	23	ns
t407	CLKI^ to BRDY* active delay		18	25	ns
t408	CLKI^ to BRDY* inactive delay		18	25	ns
t409	CPU address and status valid to BECS*/BOCS* inactive delay		15	20	ns
t410	CPU address and status valid to BECS*/BOCS* active delay		15	20	ns
t411	CLK2Iv to CAWE* active delay		14	18	ns
t412	CLK2Iv to CAWE* inactive delay		12	17	ns

Sym	Description	Min	Typ	Max	Units
t413	CLKIv to CAWE* active delay		12	18	ns
t414	CLKIv to CAWE* inactive delay		12	18	ns
t415	CLK2Iv to DTYWE* active delay		14	18	ns
t416	CLK2Iv to DTYWE* inactive delay		12	17	ns
t417	CLKIv to DTYWE* active delay		12	17	ns
t418	CLKIv to DTYWE* inactive delay		12	17	ns
t419/ t421	CLKI^ to RDY* active delay		18	25	ns
t420/ t422	CLKI^ to RDY* inactive delay		18	25	ns
t423	CLKIv to TAGWE* active delay		12	18	ns
t424	CLKIv to TAGWE* inactive delay		12	18	ns
t425	CPU address and status valid to BEA3/BOA3 active delay		13	19	ns
t426	CLKI^ to BEA3/BOA3 inactive delay		13	19	ns
t427	CLKI^ to BDIR* active delay		16	22	ns
t428	CLKI^ to BDIR* inactive delay		16	22	ns
t429	CLKI^ to CAS* active delay	10		16	ns
t430/ t439/ t442	CLKI^ to CAS* inactive delay	11		18	ns
t431	CLKI^ to DLE active delay	10		16	ns
t432	CLKI^ to DLE inactive delay	11		18	ns
t433	CLKI^ to RAS* inactive delay	8		16	ns
t434	CLKI^ to RAS* active delay	12		20	ns
t435	CLKI^ to column address valid delay	8		16	ns
t436	CLKI^ to row address hold time	8		16	ns
t437	CLKI^ to DWE* active delay	11		18	ns
t438	CLKI^ to DWE* inactive delay	8		16	ns
t440	RAS* precharge time		4 CLKI		
t441	CAS* precharge time		1 CLKI		
t443	CLKI^ to row address valid time				
t444	CAS* active to DLE active delay	6		18	ns
t445	CAS* inactive to DLE inactive delay	6		18	ns
t446	CLKI^ to LMEN* active delay	5		22	ns
t447	CLKI^ to LMEN* inactive delay	5		22	ns
t448	MRD* active to BECS* active delay	8	15	20	ns
t449	MRD* inactive to BECS* inactive delay	7	15	21	ns
t450	MRD* active to BOCS* active delay	8	15	20	ns
t451	MRD* inactive to BOCS* inactive delay	8	14	20	ns
t452	MRD* active to CAOE* active delay	7	15	20	ns
t453	MRD* inactive to CAOE* inactive delay	7	15	21	ns
t454	MRD* active to BEOE*/BOOE* active delay	8	14	19	ns
t455	MRD* inactive to BEOE*/BOOE* inactive delay	8	14	19	ns
t456	MRD* active to BDIR* active delay	7	14	20	ns
t457	MRD* inactive to BDIR* inactive delay	8	15	21	ns
t458	MRD* active to RAS* active delay	8		16	ns
t459	MRD* inactive to RAS* inactive delay	8		16	ns
t460	MRD* active to CAS* active delay	10		20	ns
t461	MRD* inactive to CAS* inactive delay	8		18	ns
t462	MRD* active to column address valid delay	10		20	ns
t463	MRD* active to row address hold time	10		20	ns

Sym	Description	Min	Typ	Max	Units
t464	MWE* active to CAWE* active delay	7	15	20	ns
t465	MWE* active to DWE* active delay	8		18	ns
t466	MWE* inactive to DWE* inactive delay	8		18	ns
t501	BCLKv to ALE active delay	5		30	ns
t502	BCLK^ to ALE inactive delay	5		30	ns
t503	BCLKv to CMD active delay	5		30	ns
t504	BCLK^ to CMD inactive delay	5		30	ns
t505	BCLK^ to CMD active delay	5		30	ns
t506	M16* to BCLK^ setup time	8			ns
t507	M16* to BCLK^ hold time	8			ns
t508	IO16* to BCLK^ setup time	10			ns
t509	IO16* to BCLK^ hold time	10			ns
t510	NOWS* to BCLK^ setup time	10			ns
t511	NOWS* to BCLK^ hold time	10			ns
t512	CHRDY to BCLK^ setup time	12			ns
t513	CHRDY to BCLK^ hold time	12			ns
t515	ATCLKv to HOLD active delay	5		16	ns
t516	ATCLK^ to HOLD inactive delay	5		16	ns
t517	ATCLK^ to REF* active delay	8		30	ns
t518	ATCLK^ to REF* inactive delay	8		30	ns
t519	ATCLK^ to MEMRD* active delay	5		25	ns
t520	ATCLK^ to MEMRD* inactive delay	5		25	ns
t521	HRQ1 setup time to ATCLK^	10			ns
t522	HRQ1 hold time to ATCLK^	10			ns
t523	HLDA active to HLDA1 active delay	8		18	ns
t524	HLDA inactive to HLDA1 inactive delay	8		18	ns
t525	ATCYC* active to SDIR1*,SDIR2* active delay	5		25	ns
t526	ATCYC* inactive to SDIR1*,SDIR2* inactive delay	5		25	ns
t527	ATCYC* active to SDEN* active delay	5		25	ns
t528	ATCYC* inactive to SDEN* inactive delay	5		25	ns

Notes :

1. ^ means rising edge.
2. v means falling edge.

82C493/82C392 AC Characteristics (33MHz)

Preliminary

Temperature : 0C to 70C, Vcc : 5V +/- 5%

Sym	Description	Min	Typ	Max	Units
t101	NPRST active delay from CLKI^		10		ns
t102	NPRST inactive delay from CLKI^		10		ns
t103	CPURST active delay from CLKI^		10		ns
t104	CPURST inactive delay from CLKI^		10		ns
t201	CAS* active to RAS* 0,3 active delay	10		20	ns
t202	CAS* inactive to RAS*0,3 inactive delay	10		20	ns
t203	RAS*0,3 active to RAS*1,2 active delay		15		ns
t204	RAS*0,3 inactive to RAS*1,2 inactive delay		15		ns
t301	D(31:0) valid to XD(7:0) valid delay	8		20	ns
t302	D(31:0) valid to MP(3:0) valid delay	8		18	ns
t303	D(31:0) invalid to XD(7:0) invalid delay	8		18	ns
t304	D(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t305	D(31:0) valid to MD(31:0) valid delay	8		18	ns
t306	D(31:0) invalid to MD(31:0) invalid delay	8		18	ns
t307	MD(31:0) valid to D(31:0) valid delay	8		18	ns
t308	MD(31:0) invalid to D(31:0) invalid delay	8		18	ns
t309	MD(31:0) valid to MP(3:0) valid delay	8		18	ns
t310	MD(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t311	MD(31:0) and MP(3:0) setup time to DLE inactive	6			ns
t312	MD(31:0) and MP(3:0) hold time to DLE inactive	6			ns
t313	A(9:0) to KBDCS* active delay	5		30	ns
t314	A(9:0) to KBDCS* inactive delay	5		30	ns
t315	DRD* active to MD(31:0) valid delay	6		20	ns
t316	DRD* inactive to MD(31:0) invalid delay	6		20	ns
t317	DRD* active to D(31:0) valid delay	6		20	ns
t318	DRD* inactive to D(31:0) invalid delay	6		20	ns
t319	MD(15:0) setup time to IORD*/MEMRD*^	6			ns
t320	MD(15:0) hold time to IORD*/MEMRD*^	6			ns
t321	MD(15:8) valid to MD(7:0) valid delay	8		18	ns
t322	MD(15:8) invalid to MD(7:0) invalid delay	8		18	ns
t401	CPU address and status valid to CAOE* active delay		13	18	ns
t402	CPU address and status valid to BEOE* acitve delay		14	19	ns
t403	CLKI^ to BEOE* /BOOE* inactive delay		12	18	ns
t404	CLKI^ to BOOE* active delay		12	18	ns
t405	CLKI^ to BDIR* inactive delay		12	18	ns
t406	CPU address and status valid to BDIR* active delay		13	19	ns
t407	CLKI^ to BRDY* active delay		12	17	ns
t408	CLKI^ to BRDY* inactive delay		12	17	ns
t409	CPU address and status valid to BECS*/BOCS* inactive delay		13	18	ns
t410	CPU address and status valid to BECS*/BOCS* active delay		13	18	ns
t411	CLK2Iv to CAWE* active delay		14	18	ns
t412	CLK2Iv to CAWE* inactive delay		12	17	ns

Sym	Description	Min	Typ	Max	Units
t413	CLKIv to CAWE* active delay		12	18	ns
t414	CLKIv to CAWE* inactive delay		12	18	ns
t415	CLK2Iv to DTYWE* active delay		14	18	ns
t416	CLK2Iv to DTYWE* inactive delay		12	17	ns
t417	CLKIv to DTYWE* active delay		12	17	ns
t418	CLKIv to DTYWE* inactive delay		12	17	ns
t419/ t421	CLKI^ to RDY* active delay		12	17	ns
t420/ t422	CLKI^ to RDY* inactive delay		12	18	ns
t423	CLKIv to TAGWE* active delay		12	18	ns
t424	CLKIv to TAGWE* inactive delay		12	18	ns
t425	CPU address and status valid to BEA3/BOA3 active delay		13	19	ns
t426	CLKI^ to BEA3/BOA3 inactive delay		13	19	ns
t427	CLKI^ to BDIR* active delay		12	17	ns
t428	CLKI^ to BDIR* inactive delay		12	17	ns
t429	CLKI^ to CAS* active delay	10		16	ns
t430/ t439/ t442	CLKI^ to CAS* inactive delay	11		18	ns
t431	CLKI^ to DLE active delay	10		16	ns
t432	CLKI^ to DLE inactive delay	11		18	ns
t433	CLKI^ to RAS* inactive delay	8		16	ns
t434	CLKI^ to RAS* active delay	12		20	ns
t435	CLKI^ to column address valid delay	8		16	ns
t436	CLKI^ to row address hold time	8		16	ns
t437	CLKI^ to DWE* active delay	11		18	ns
t438	CLKI^ to DWE* inactive delay	8		16	ns
t440	RAS* precharge time		4 CLKI		
t441	CAS* precharge time		1 CLKI		
t443	CLKI^ to row address valid time				
t444	CAS* active to DLE active delay	6		18	ns
t445	CAS* inactive to DLE inactive delay	6		18	ns
t446	CLKI^ to LMEN* active delay	5		22	ns
t447	CLKI^ to LMEN* inactive delay	5		22	ns
t448	MRD* active to BECS* active delay	8	15	20	ns
t449	MRD* inactive to BECS* inactive delay	7	15	21	ns
t450	MRD* active to BOCS* active delay	8	15	20	ns
t451	MRD* inactive to BOCS* inactive delay	8	14	20	ns
t452	MRD* active to CAOE* active delay	7	15	20	ns
t453	MRD* inactive to CAOE* inactive delay	7	15	21	ns
t454	MRD* active to BEOE*/BOOE* active delay	8	14	19	ns
t455	MRD* inactive to BEOE*/BOOE* inactive delay	8	14	19	ns
t456	MRD* active to BDIR* active delay	7	14	20	ns
t457	MRD* inactive to BDIR* inactive delay	8	15	21	ns
t458	MRD* active to RAS* active delay	8		16	ns
t459	MRD* inactive to RAS* inactive delay	8		16	ns
t460	MRD* active to CAS* active delay	10		20	ns
t461	MRD* inactive to CAS* inactive delay	8		18	ns
t462	MRD* active to column address valid delay	10		20	ns
t463	MRD* active to row address hold time	10		20	ns

Sym	Description	Min	Typ	Max	Units
t464	MWE* active to CAWE* active delay	7	15	20	ns
t465	MWE* active to DWE* active delay	8		18	ns
t466	MWE* inactive to DWE* inactive delay	8		18	ns
t501	BCLKv to ALE active delay	5		30	ns
t502	BCLK^ to ALE inactive delay	5		30	ns
t503	BCLKv to CMD active delay	5		30	ns
t504	BCLK^ to CMD inactive delay	5		30	ns
t505	BCLK^ to CMD active delay	5		30	ns
t506	M16* to BCLK^ setup time	8			ns
t507	M16* to BCLK^ hold time	8			ns
t508	IO16* to BCLK^ setup time	10			ns
t509	IO16* to BCLK^ hold time	10			ns
t510	NOWS* to BCLK^ setup time	10			ns
t511	NOWS* to BCLK^ hold time	10			ns
t512	CHRDY to BCLK^ setup time	12			ns
t513	CHRDY to BCLK^ hold time	12			ns
t515	ATCLKv to HOLD active delay	5		16	ns
t516	ATCLK^ to HOLD inactive delay	5		16	ns
t517	ATCLK^ to REF* active delay	8		30	ns
t518	ATCLK^ to REF* inactive delay	8		30	ns
t519	ATCLK^ to MEMRD* active delay	5		25	ns
t520	ATCLK^ to MEMRD* inactive delay	5		25	ns
t521	HRQ1 setup time to ATCLK^	10			ns
t522	HRQ1 hold time to ATCLK^	10			ns
t523	HLDA active to HLDA1 active delay	8		18	ns
t524	HLDA inactive to HLDA1 inactive delay	8		18	ns
t525	ATCYC* active to SDIR1*,SDIR2* active delay	5		25	ns
t526	ATCYC* inactive to SDIR1*,SDIR2* inactive delay	5		25	ns
t527	ATCYC* active to SDEN* active delay	5		25	ns
t528	ATCYC* inactive to SDEN* inactive delay	5		25	ns

Notes :

1. ^ means rising edge.
2. v means falling edge.

Temperature : 0C to 70C, Vcc : 5V +/- 5%

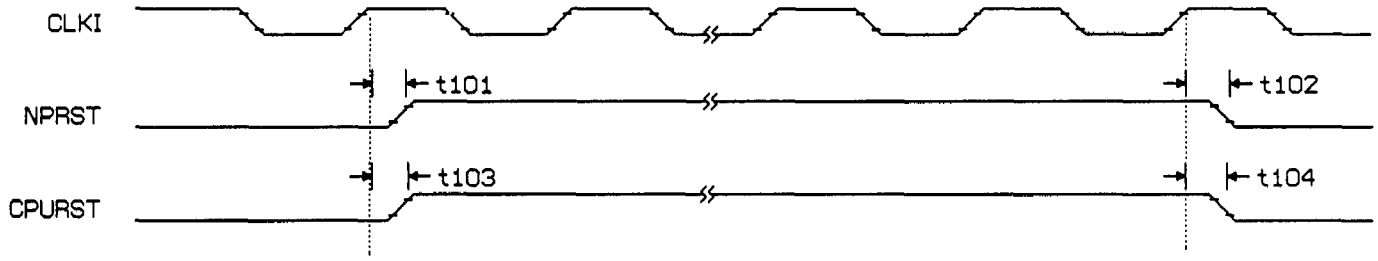
Sym	Description	Min	Typ	Max	Units
t101	NPRST active delay from CLKI^		10		ns
t102	NPRST inactive delay from CLKI^		10		ns
t103	CPURST active delay from CLKI^		10		ns
t104	CPURST inactive delay from CLKI^		10		ns
t201	CAS* active to RAS* 0,3 active delay	10		20	ns
t202	CAS* inactive to RAS*0,3 inactive delay	10		20	ns
t203	RAS*0,3 active to RAS*1,2 active delay		15		ns
t204	RAS*0,3 inactive to RAS*1,2 inactive delay		15		ns
t301	D(31:0) valid to XD(7:0) valid delay	8		20	ns
t302	D(31:0) valid to MP(3:0) valid delay	8		18	ns
t303	D(31:0) invalid to XD(7:0) invalid delay	8		18	ns
t304	D(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t305	D(31:0) valid to MD(31:0) valid delay	8		18	ns
t306	D(31:0) invalid to MD(31:0) invalid delay	8		18	ns
t307	MD(31:0) valid to D(31:0) valid delay	8		18	ns
t308	MD(31:0) invalid to D(31:0) invalid delay	8		18	ns
t309	MD(31:0) valid to MP(3:0) valid delay	8		18	ns
t310	MD(31:0) invalid to MP(3:0) invalid delay	8		18	ns
t311	MD(31:0) and MP(3:0) setup time to DLE inactive	6			ns
t312	MD(31:0) and MP(3:0) hold time to DLE inactive	6			ns
t313	A(9:0) to KBDCS* active delay	5		30	ns
t314	A(9:0) to KBDCS* inactive delay	5		30	ns
t315	DRD* active to MD(31:0) valid delay	6		20	ns
t316	DRD* inactive to MD(31:0) invalid delay	6		20	ns
t317	DRD* active to D(31:0) valid delay	6		20	ns
t318	DRD* inactive to D(31:0) invalid delay	6		20	ns
t319	MD(15:0) setup time to IORD*/MEMRD*^	6			ns
t320	MD(15:0) hold time to IORD*/MEMRD*^	6			ns
t321	MD(15:8) valid to MD(7:0) valid delay	8		18	ns
t322	MD(15:8) invalid to MD(7:0) invalid delay	8		18	ns
t401	CPU address and status valid to CAOE* active delay		10	13	ns
t402	CPU address and status valid to BEOE* acitve delay		11	13	ns
t403	CLKI^ to BEOE* /BOOE* inactive delay		10	12	ns
t404	CLKI^ to BOOE* active delay		11	13	ns
t405	CLKI^ to BDIR* inactive delay		11	13	ns
t406	CPU address and status valid to BDIR* active delay		11	13	ns
t407	CLKI^ to BRDY* active delay		10	13	ns
t408	CLKI^ to BRDY* inactive delay		10	13	ns
t409	CPU address and status valid to BECS*/BOCS* inactive delay		11	14	ns
t410	CPU address and status valid to BECS*/BOCS* active delay		11	14	ns
t411	CLK2Iv to CAWE* active delay		14	18	ns
t412	CLK2Iv to CAWE* inactive delay		12	17	ns

Sym	Description	Min	Typ	Max	Units
t413	CLKIv to CAWE* active delay		10	12	ns
t414	CLKIv to CAWE* inactive delay		10	12	ns
t415	CLK2Iv to DTYWE* active delay		14	18	ns
t416	CLK2Iv to DTYWE* inactive delay		12	17	ns
t417	CLKIv to DTYWE* active delay		10	12	ns
t418	CLKIv to DTYWE* inactive delay		10	12	ns
t419/ t421	CLKI^ to RDY* active delay		10	13	ns
t420/ t422	CLKI^ to RDY* inactive delay		10	13	ns
t423	CLKIv to TAGWE* active delay		11	14	ns
t424	CLKIv to TAGWE* inactive delay		11	14	ns
t425	CPU address and status valid to BEA3/BOA3 active delay		11	14	ns
t426	CLKI^ to BEA3/BOA3 inactive delay		12	14	ns
t427	CLKI^ to BDIR* active delay		11	13	ns
t428	CLKI^ to BDIR* inactive delay		11	13	ns
t429	CLKI^ to CAS* active delay	10		16	ns
t430/ t439/ t442	CLKI^ to CAS* inactive delay	11		18	ns
t431	CLKI^ to DLE active delay	10		16	ns
t432	CLKI^ to DLE inactive delay	11		18	ns
t433	CLKI^ to RAS* inactive delay	8		16	ns
t434	CLKI^ to RAS* active delay	12		20	ns
t435	CLKI^ to column address valid delay	8		16	ns
t436	CLKI^ to row address hold time	8		16	ns
t437	CLKI^ to DWE* active delay	11		18	ns
t438	CLKI^ to DWE* inactive delay	8		16	ns
t440	RAS* precharge time		4 CLKI		
t441	CAS* precharge time		1 CLKI		
t443	CLKI^ to row address valid time				
t444	CAS* active to DLE active delay	6		18	ns
t445	CAS* inactive to DLE inactive delay	6		18	ns
t446	CLKI^ to LMEN* active delay	5		22	ns
t447	CLKI^ to LMEN* inactive delay	5		22	ns
t448	MRD* active to BECS* active delay	8	15	20	ns
t449	MRD* inactive to BECS* inactive delay	7	15	21	ns
t450	MRD* active to BOCS* active delay	8	15	20	ns
t451	MRD* inactive to BOCS* inactive delay	8	14	20	ns
t452	MRD* active to CAOE* active delay	7	15	20	ns
t453	MRD* inactive to CAOE* inactive delay	7	15	21	ns
t454	MRD* active to BEOE*/BOOE* active delay	8	14	19	ns
t455	MRD* inactive to BEOE*/BOOE* inactive delay	8	14	19	ns
t456	MRD* active to BDIR* active delay	7	14	20	ns
t457	MRD* inactive to BDIR* inactive delay	8	15	21	ns
t458	MRD* active to RAS* active delay	8		16	ns
t459	MRD* inactive to RAS* inactive delay	8		16	ns
t460	MRD* active to CAS* active delay	10		20	ns
t461	MRD* inactive to CAS* inactive delay	8		18	ns
t462	MRD* active to column address valid delay	10		20	ns
t463	MRD* active to row address hold time	10		20	ns

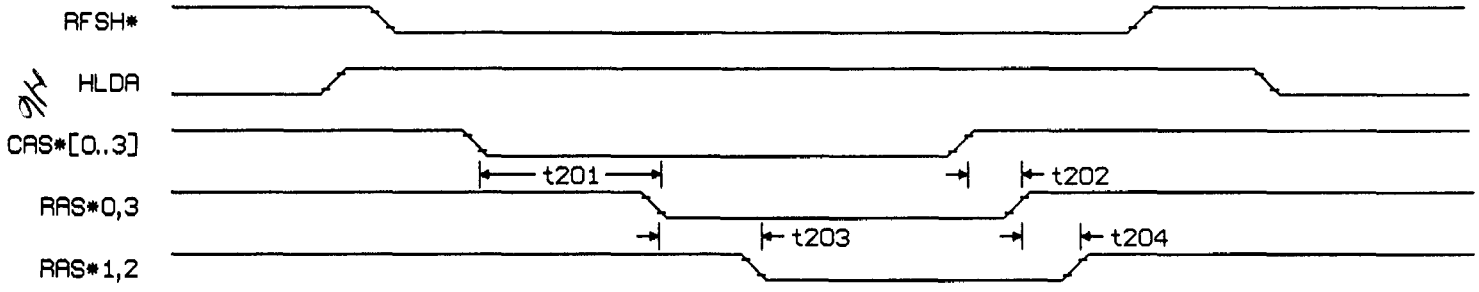
Sym	Description	Min	Typ	Max	Units
t464	MWE* active to CAWE* active delay	7	15	20	ns
t465	MWE* active to DWE* active delay	8		18	ns
t466	MWE* inactive to DWE* inactive delay	8		18	ns
t501	BCLKv to ALE active delay	5		30	ns
t502	BCLK^ to ALE inactive delay	5		30	ns
t503	BCLKv to CMD active delay	5		30	ns
t504	BCLK^ to CMD inactive delay	5		30	ns
t505	BCLK^ to CMD active delay	5		30	ns
t506	M16* to BCLK^ setup time	8			ns
t507	M16* to BCLK^ hold time	8			ns
t508	IO16* to BCLK^ setup time	10			ns
t509	IO16* to BCLK^ hold time	10			ns
t510	NOWS* to BCLK^ setup time	10			ns
t511	NOWS* to BCLK^ hold time	10			ns
t512	CHRDY to BCLK^ setup time	12			ns
t513	CHRDY to BCLK^ hold time	12			ns
t515	ATCLKv to HOLD active delay	5		16	ns
t516	ATCLK^ to HOLD inactive delay	5		16	ns
t517	ATCLK^ to REF* active delay	8		30	ns
t518	ATCLK^ to REF* inactive delay	8		30	ns
t519	ATCLK^ to MEMRD* active delay	5		25	ns
t520	ATCLK^ to MEMRD* inactive delay	5		25	ns
t521	HRQ1 setup time to ATCLK^	10			ns
t522	HRQ1 hold time to ATCLK^	10			ns
t523	HLDA active to HLDA1 active delay	8		18	ns
t524	HLDA inactive to HLDA1 inactive delay	8		18	ns
t525	ATCYC* active to SDIR1*,SDIR2* active delay	5		25	ns
t526	ATCYC* inactive to SDIR1*,SDIR2* inactive delay	5		25	ns
t527	ATCYC* active to SDEN* active delay	5		25	ns
t528	ATCYC* inactive to SDEN* inactive delay	5		25	ns

Notes :

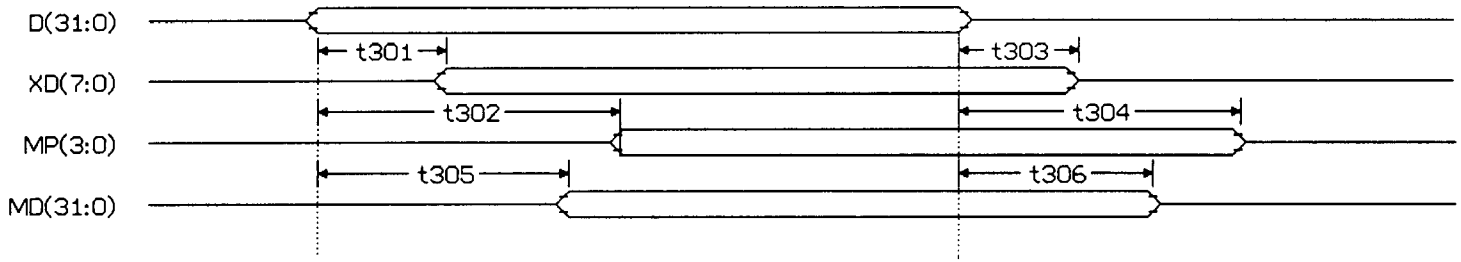
1. ^ means rising edge.
2. v means falling edge.



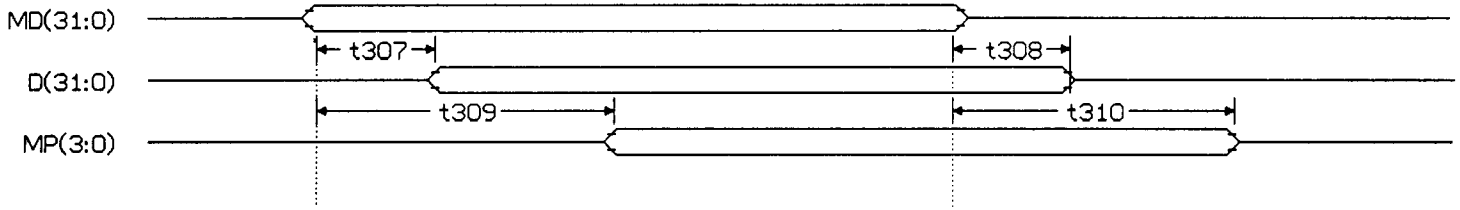
RESET TIMING



REFRESH CYCLE

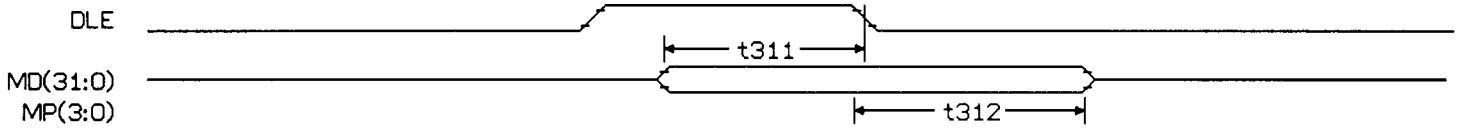


D TO XD, MP AND MD DELAY

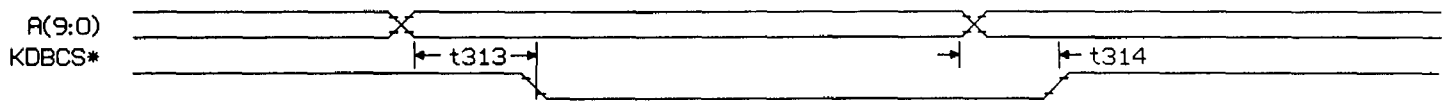


MD TO D AND MP DELAY

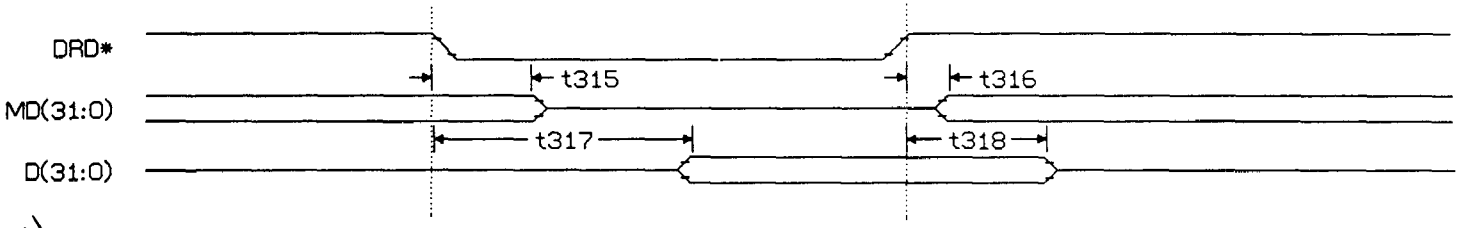
CH



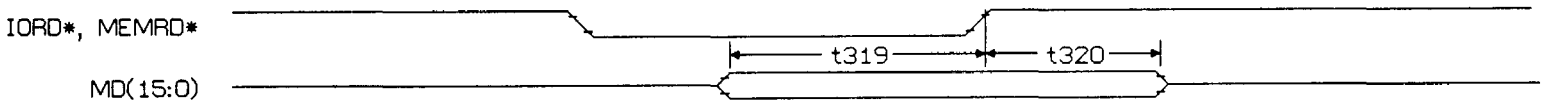
DATA SETUP AND HOLD TIME FOR DLE



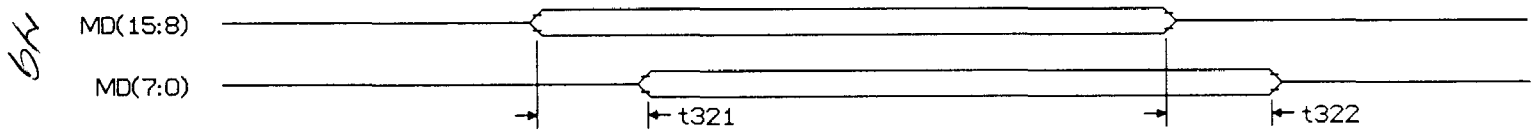
KDBCS* VALID AND INVALID DELAY



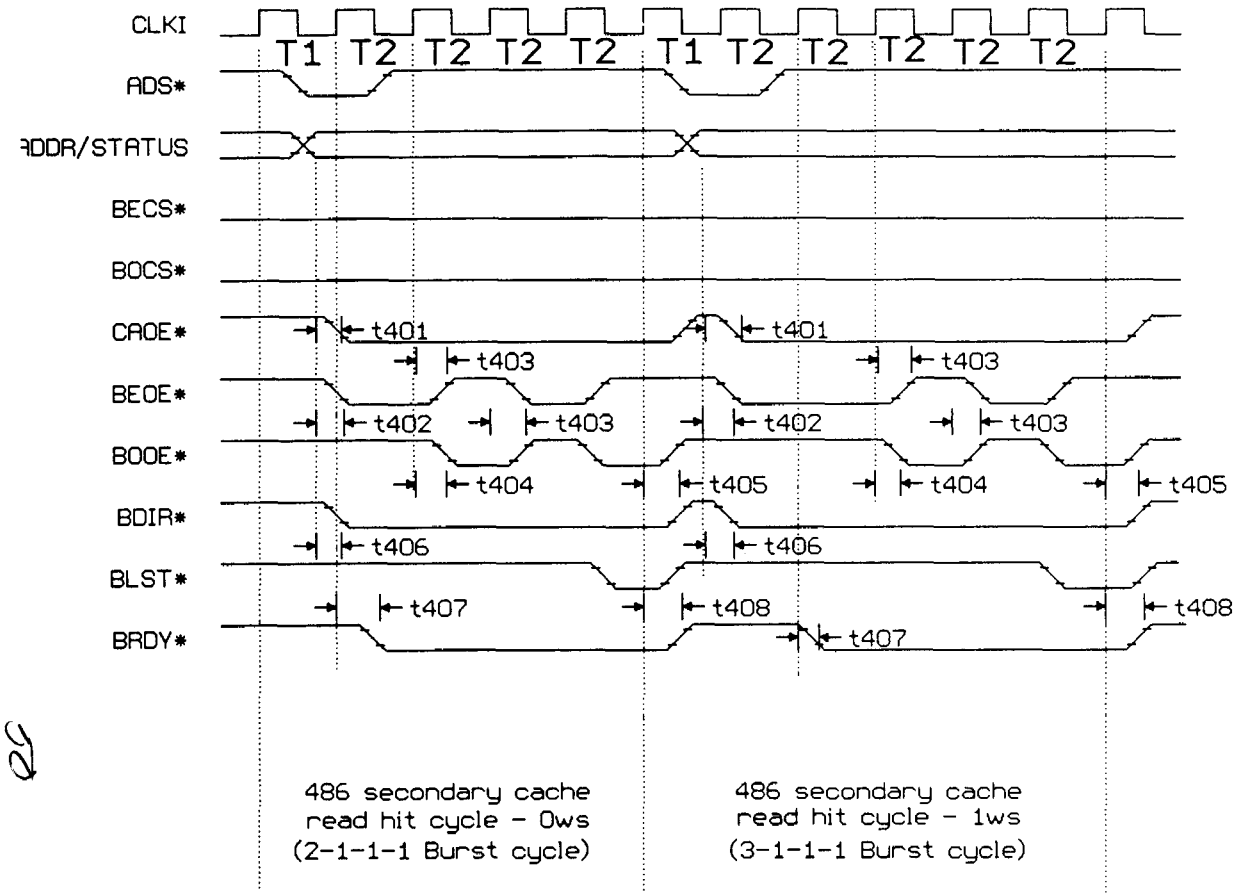
D(31:0) AND MD(31:0) TRISTATED
AND DRIVEN DELAY



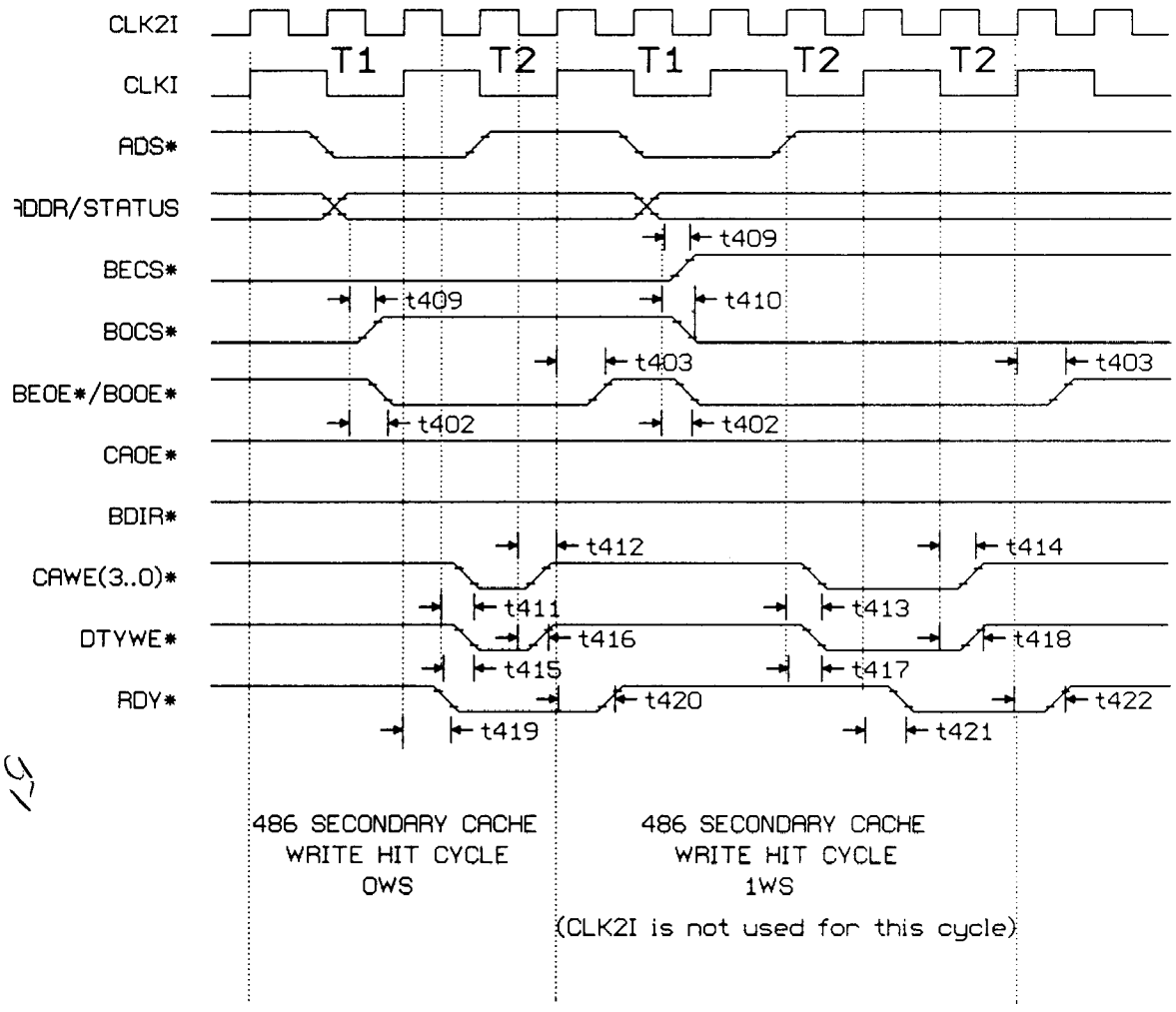
DATA SETUP AND HOLD TIME
(IORD* AND MEMRD*)



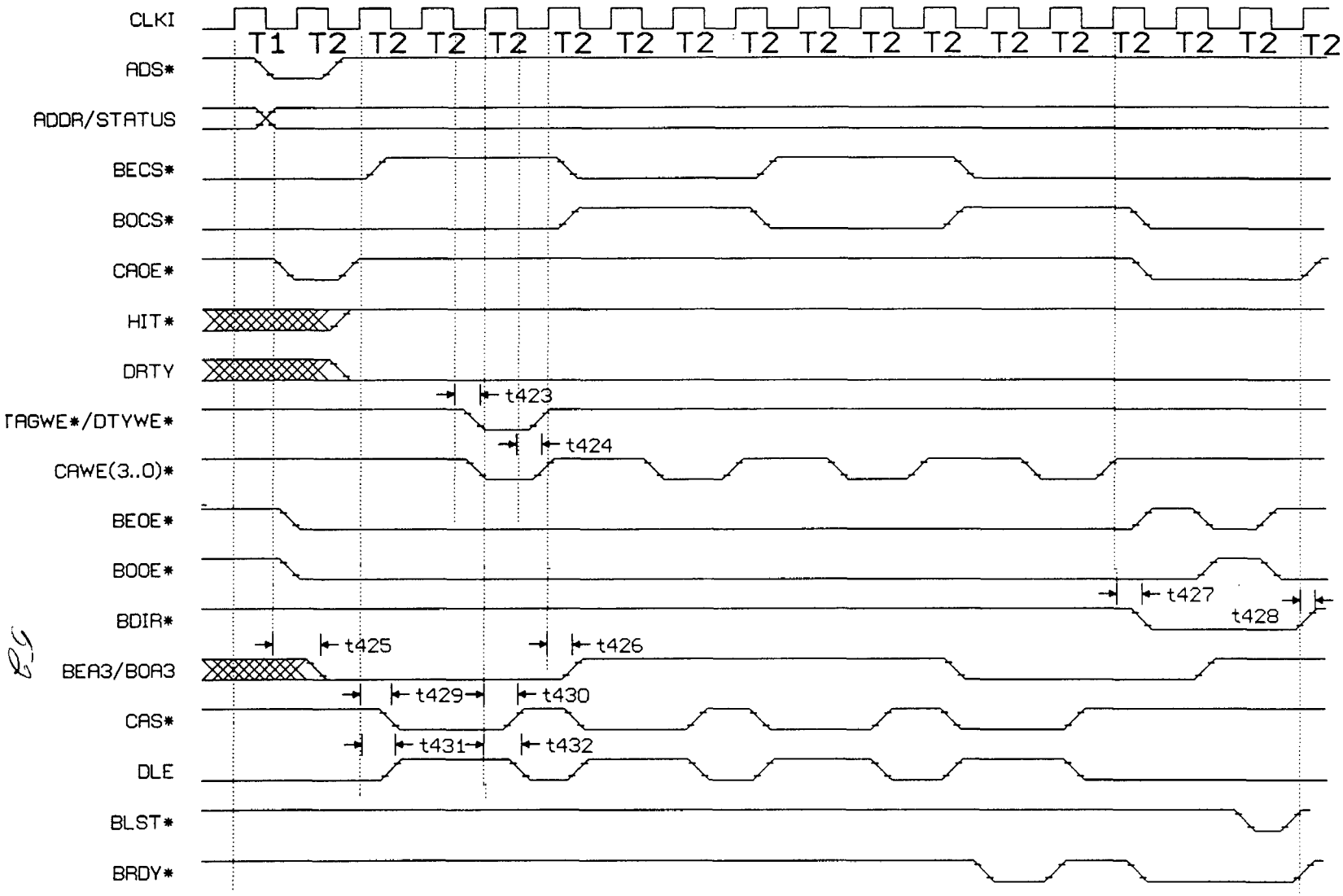
DATA VALID AND INVALID DELAY BETWEEN
MD(15:8) AND MD(7:0) SWAPPING



486 SECONDARY CACHE READ HIT CYCLE

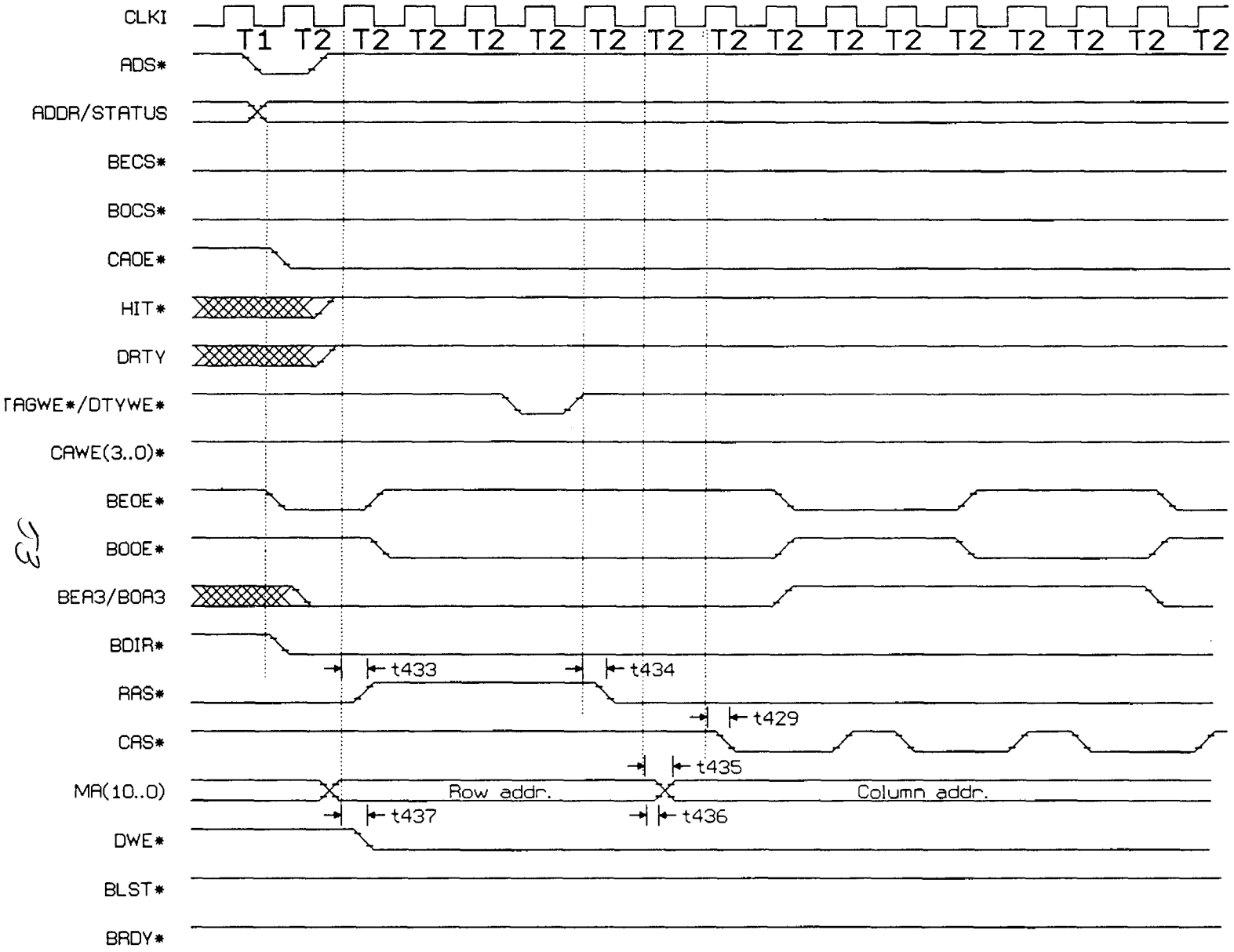


486 SECONDARY CACHE WRITE HIT CYCLE



486 SECONDARY CACHE READ MISS CYCLE (NOT DIRTY)

NOTE :
1. The diagram considers page hit on DRAM.
   In case of page miss only the first cycle will get affected as per DRAM page miss timing diagram.
2. This diagram considers the first address generated by 486 to be 0.



READ MISS DIRTY CYCLE

NOTE : This diagram considers the first address generated by 486 to be 0.

continued to next page

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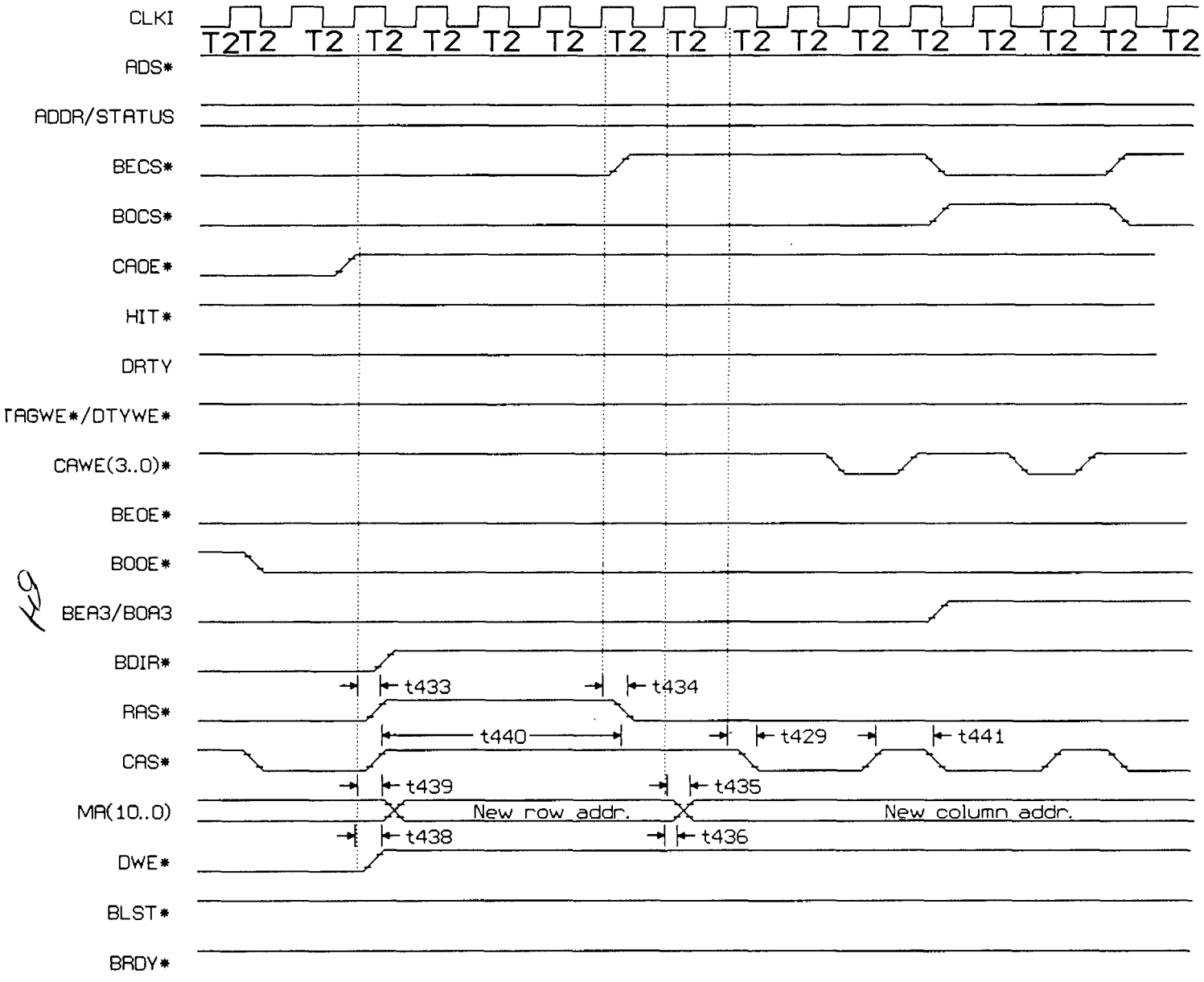

READ MISS DIRTY CYCLE

NOTE : This diagram considers the first address generated by 486 to be 0.

continued to next page

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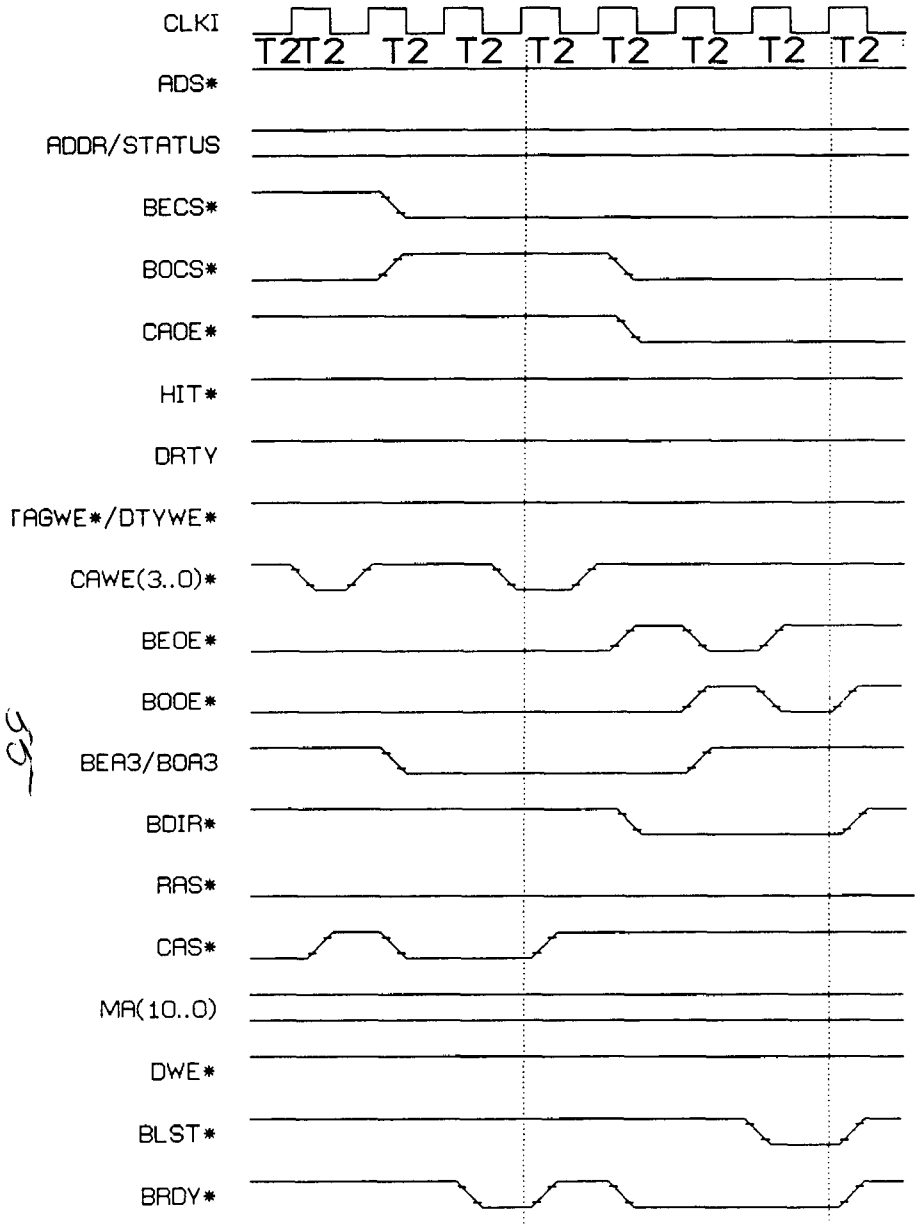

READ MISS DIRTY CYCLE

NOTE : This diagram considers the first address generated by 486 to be 0.

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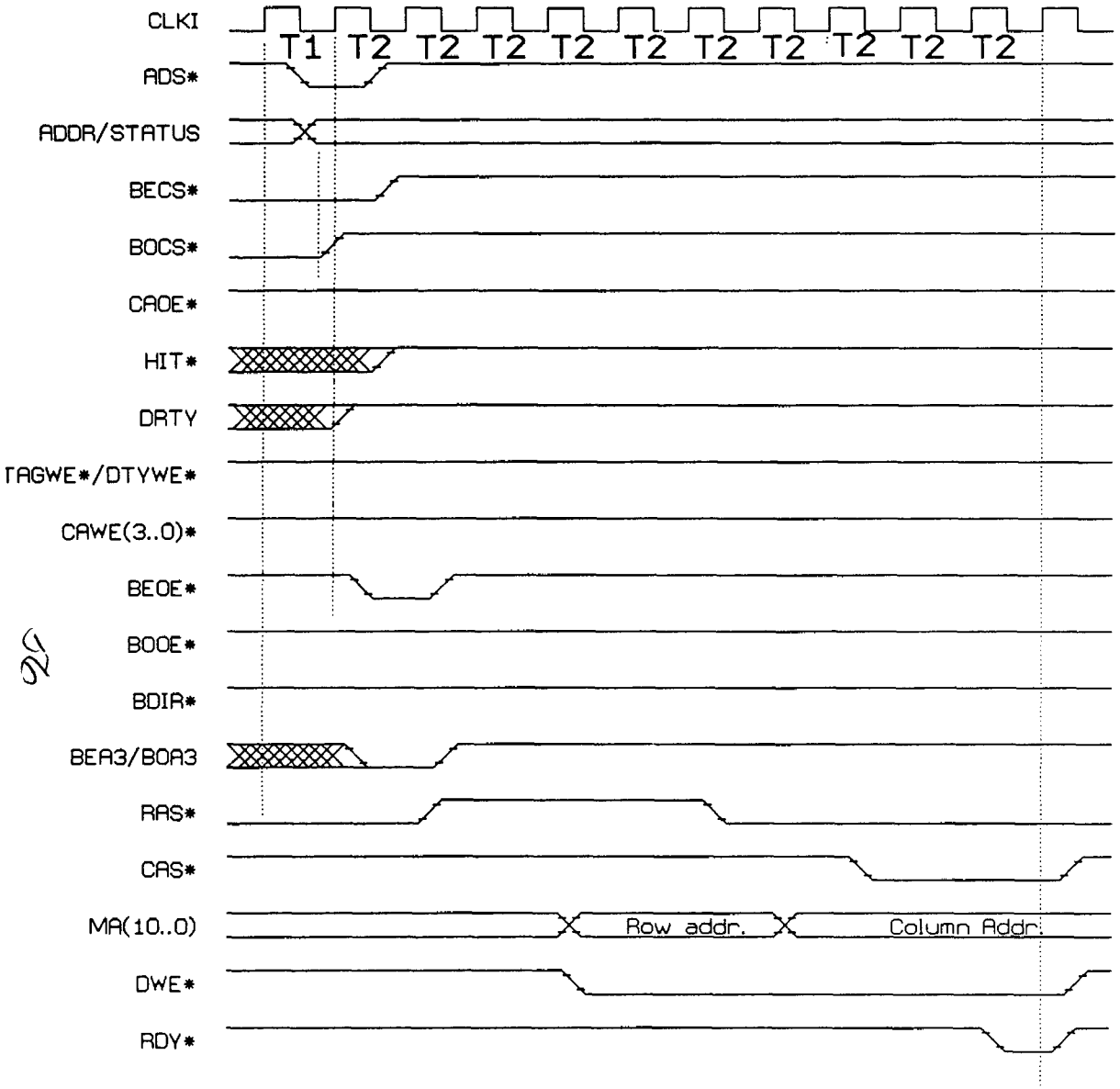
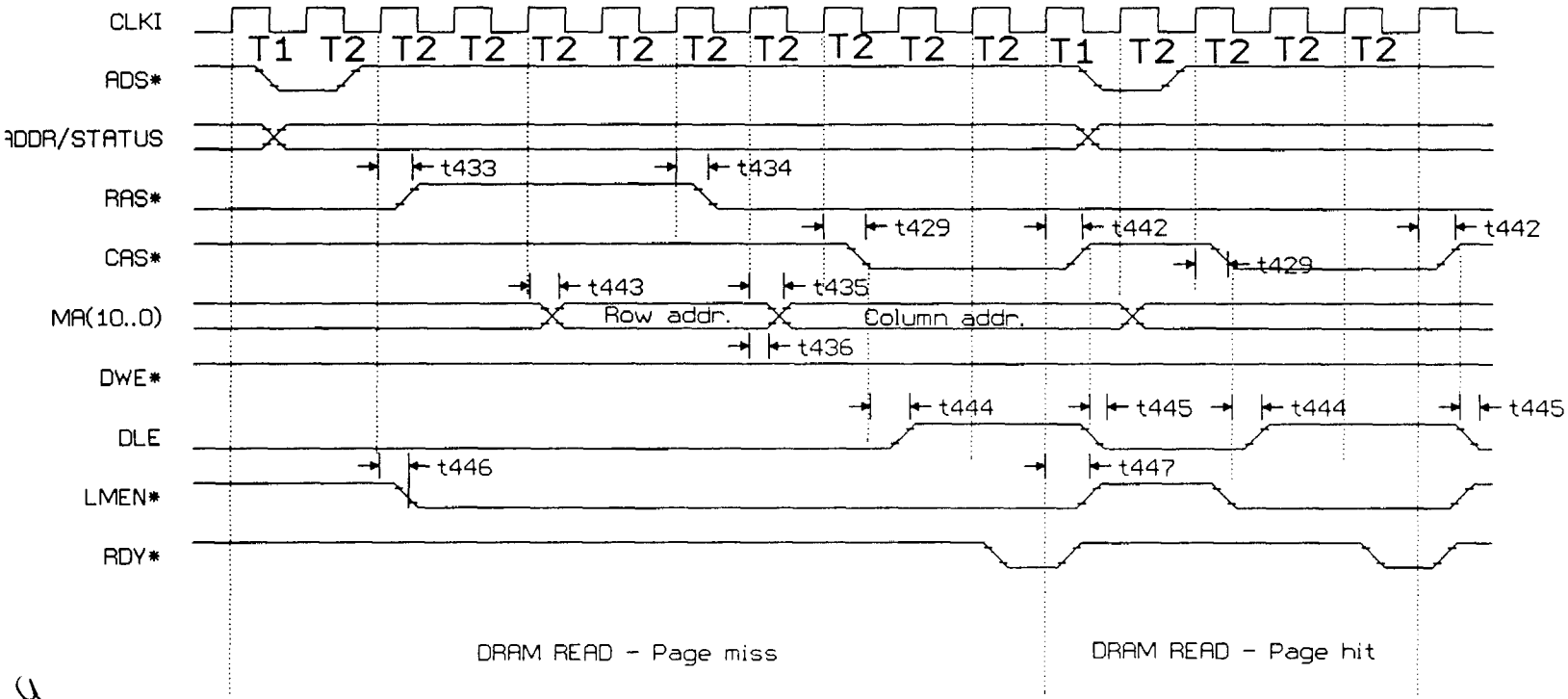
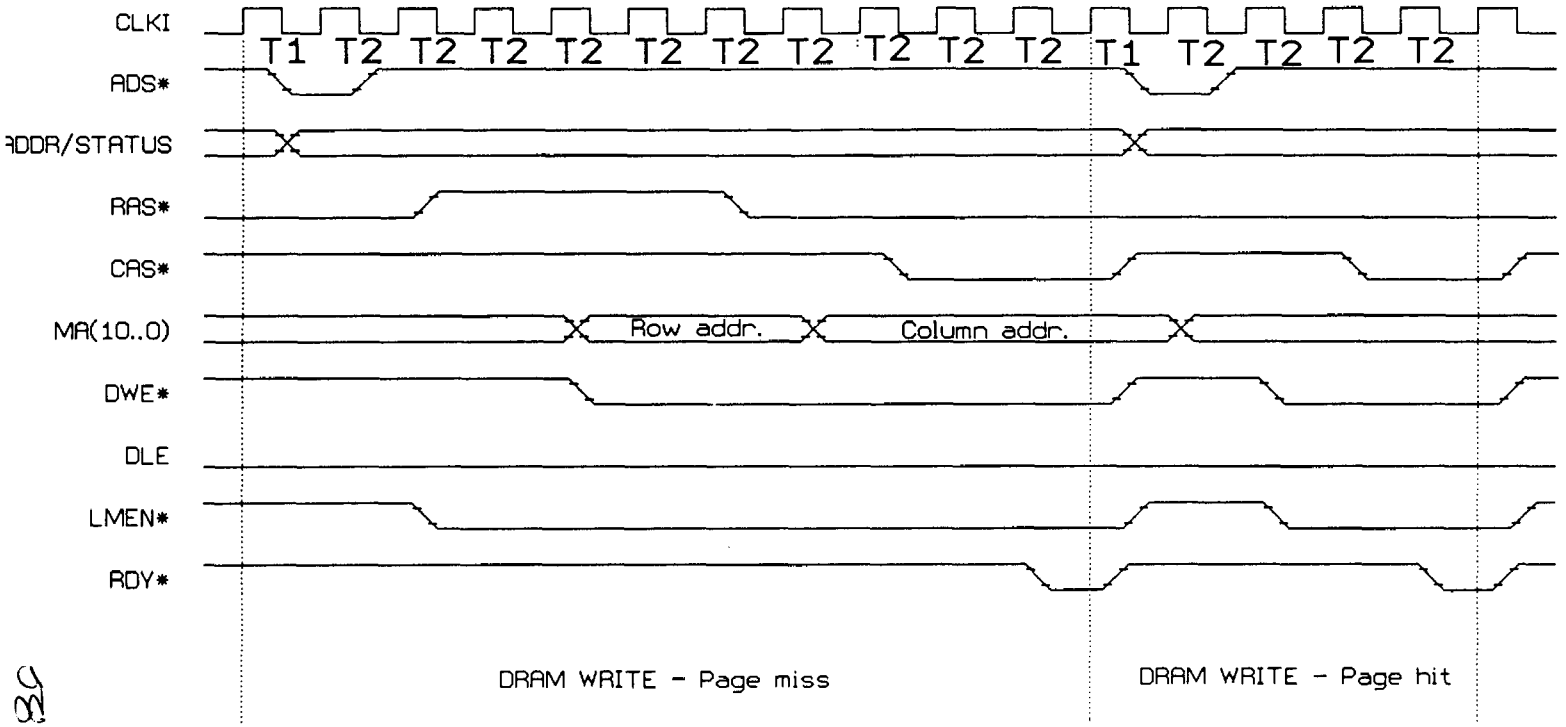


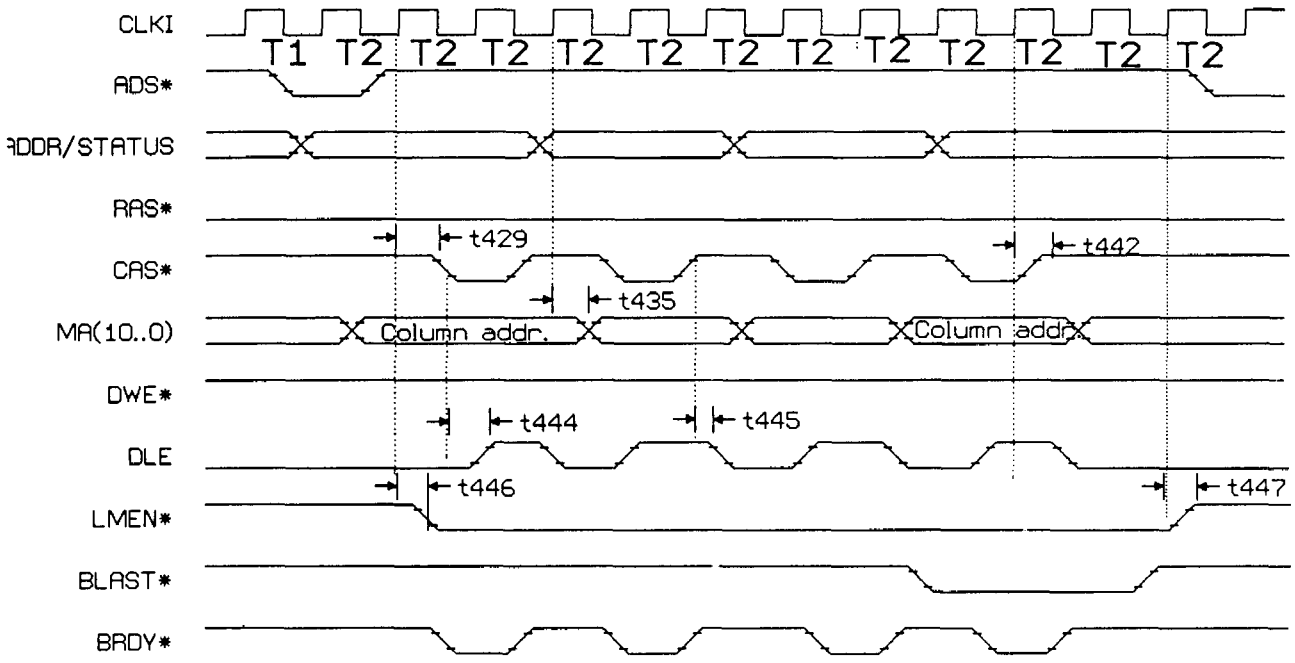
486 SECONDARY CACHE WRITE MISS CYCLE
(DRAM Write Cycle - Page miss)



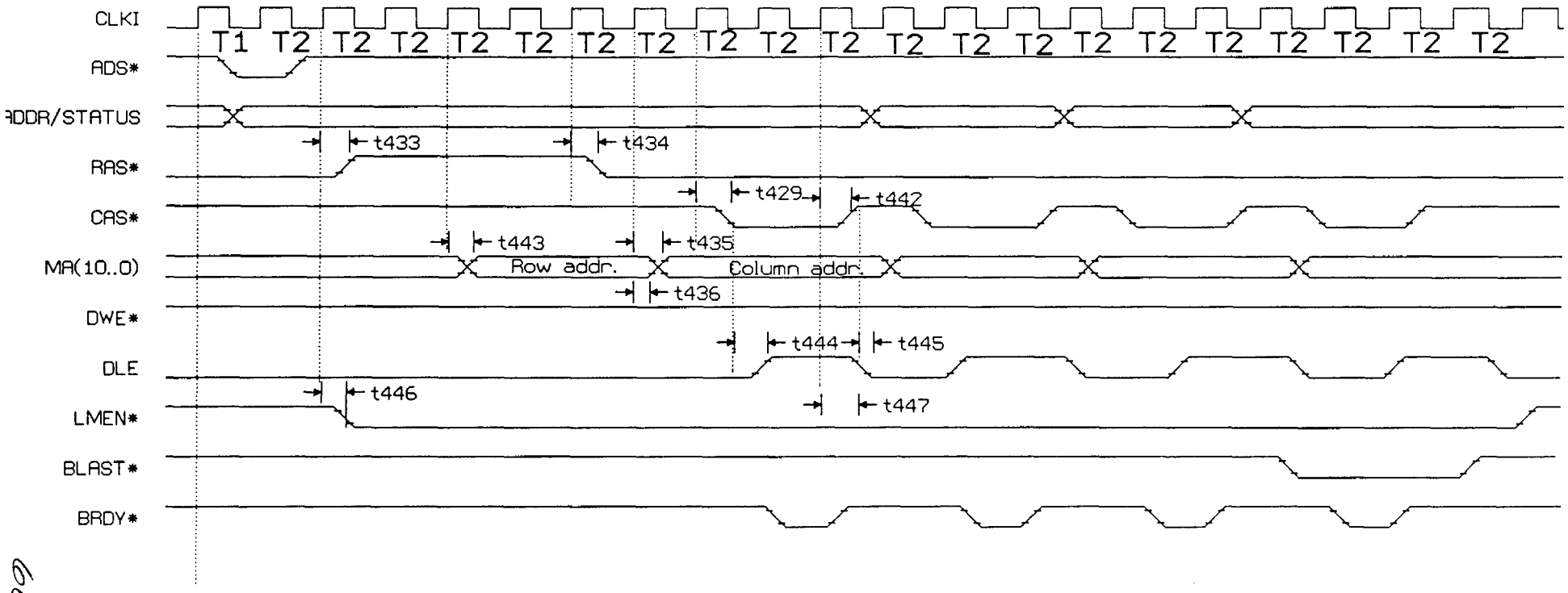
DRAM READ CYCLE



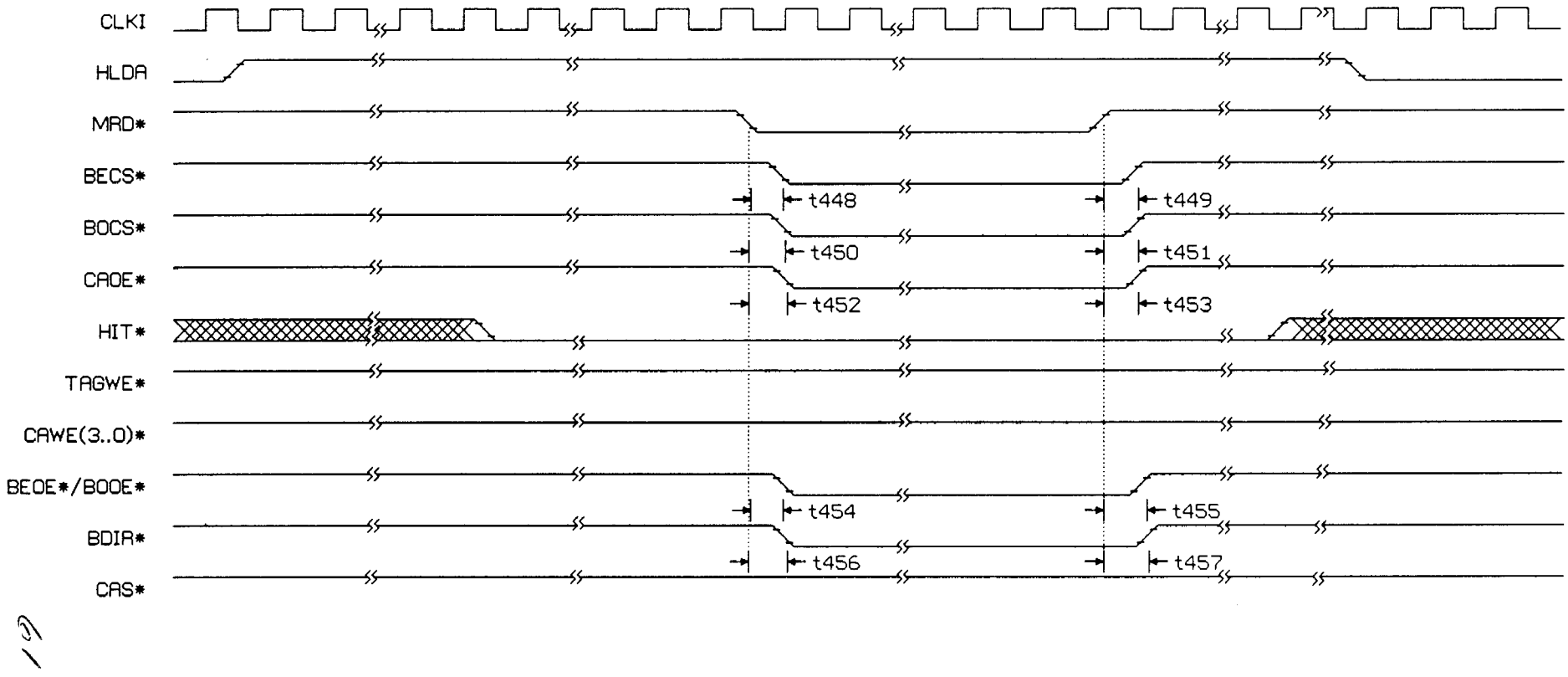
DRAM WRITE CYCLE



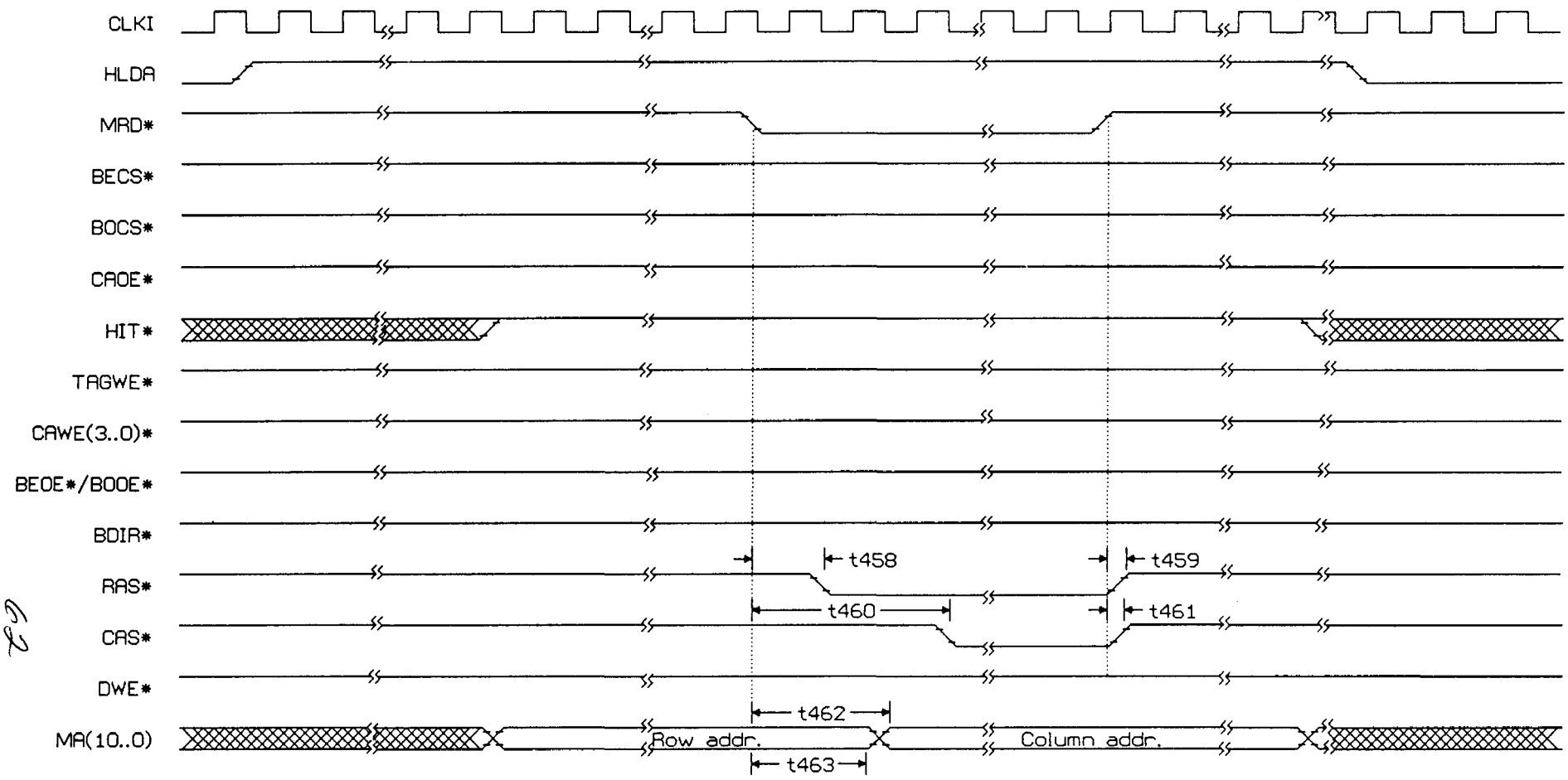
DRAM READ CYCLE - Page Hit



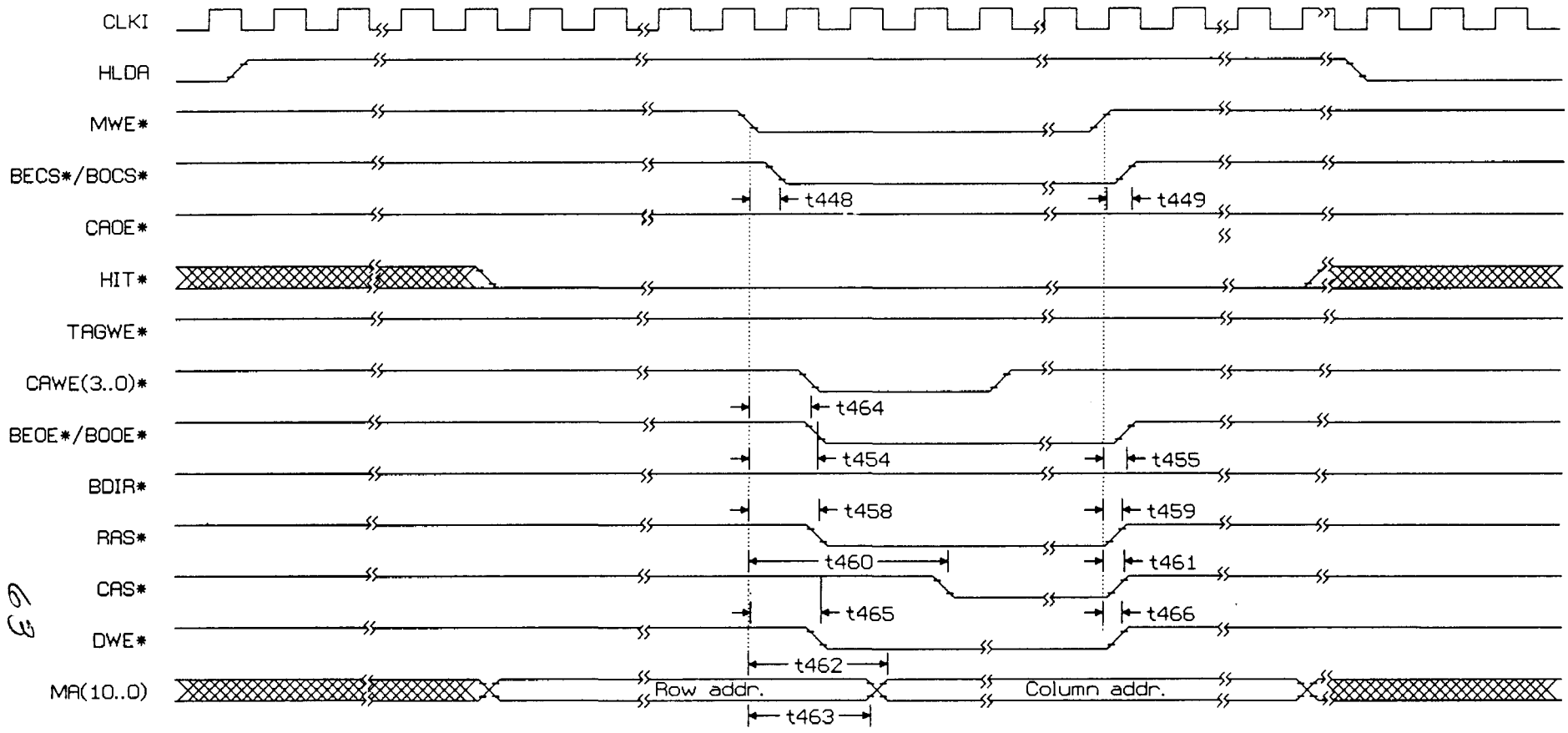
DRAM READ CYCLE - Page Miss



DMA READ CYCLE - SECONDARY CACHE HIT



DMA READ CYCLE - SECONDARY CACHE MISS



DMA WRITE CYCLE - SECONDARY CACHE HIT

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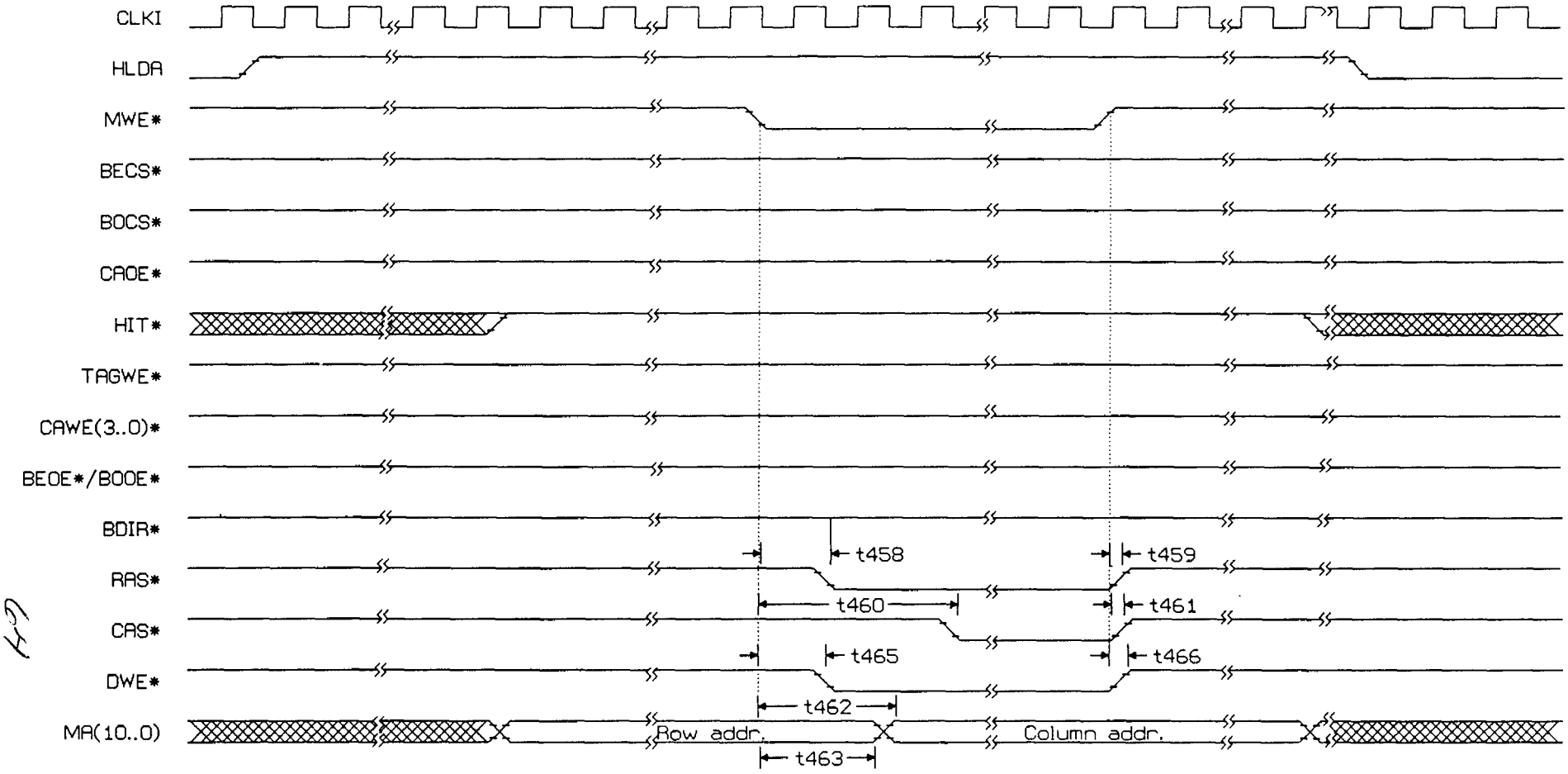
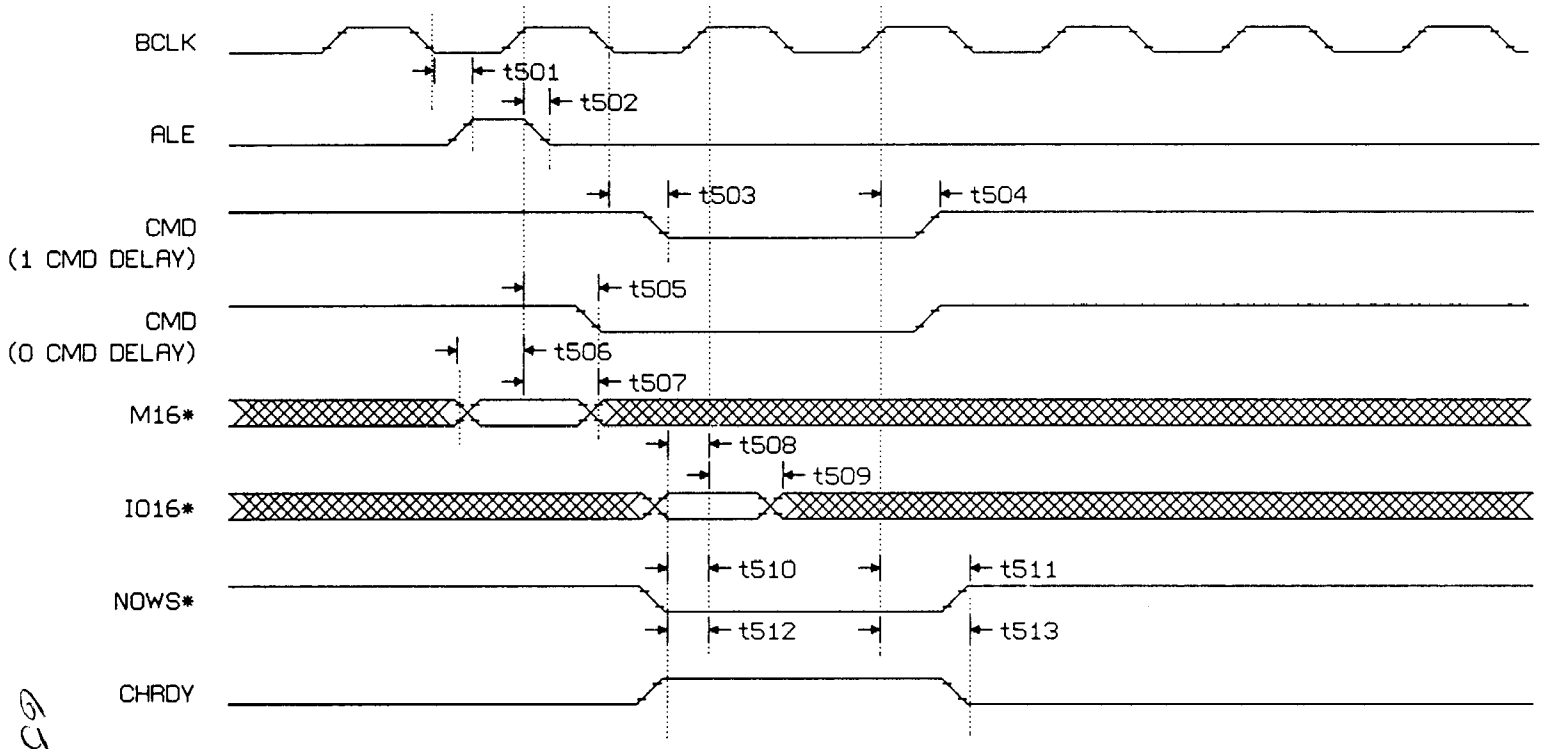


DMA WRITE CYCLE - SECONDARY CACHE MISS



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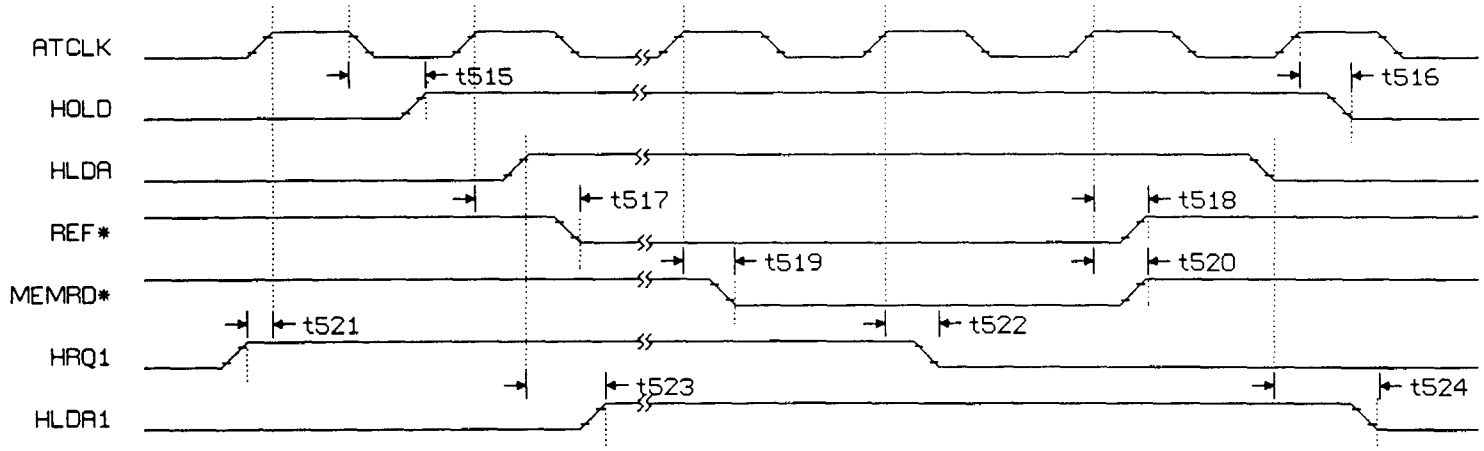
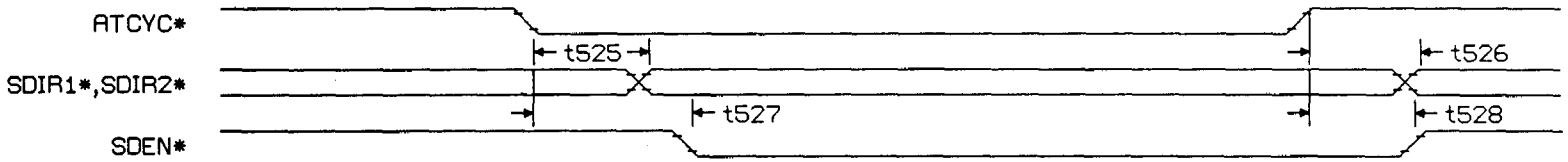
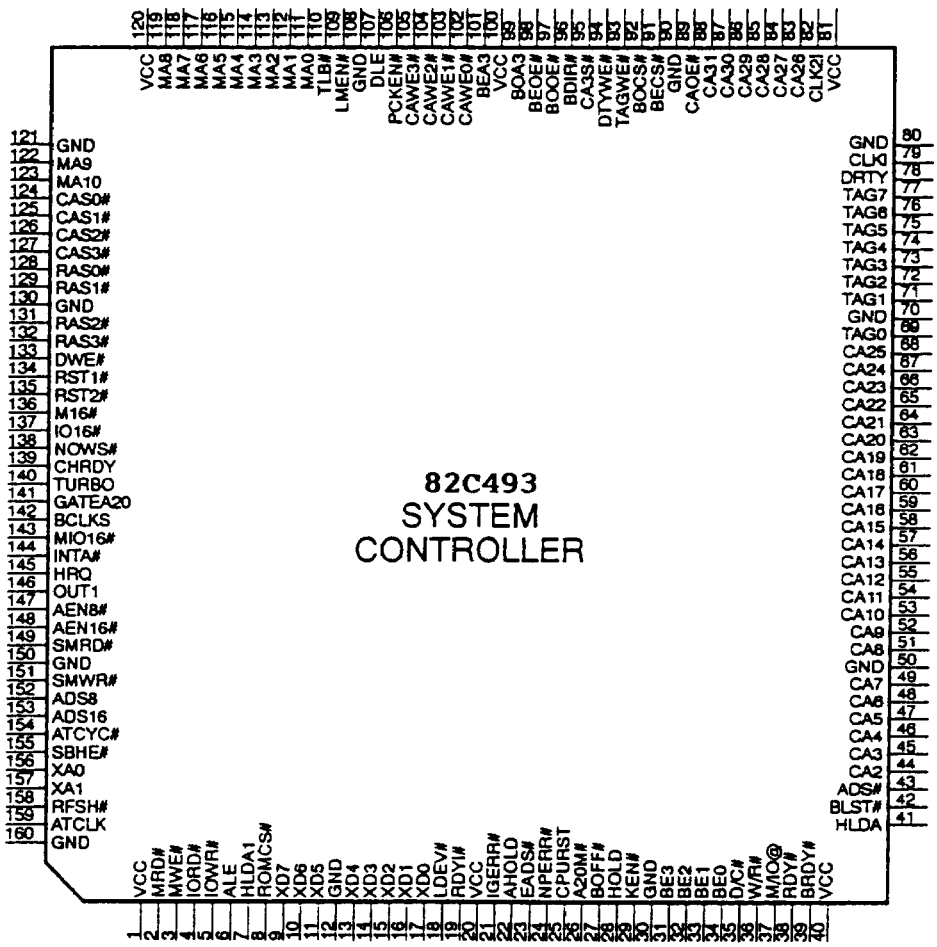
ATBUS TIMING



ATBUS HOLD TIMING



DIRECTION CONTROL



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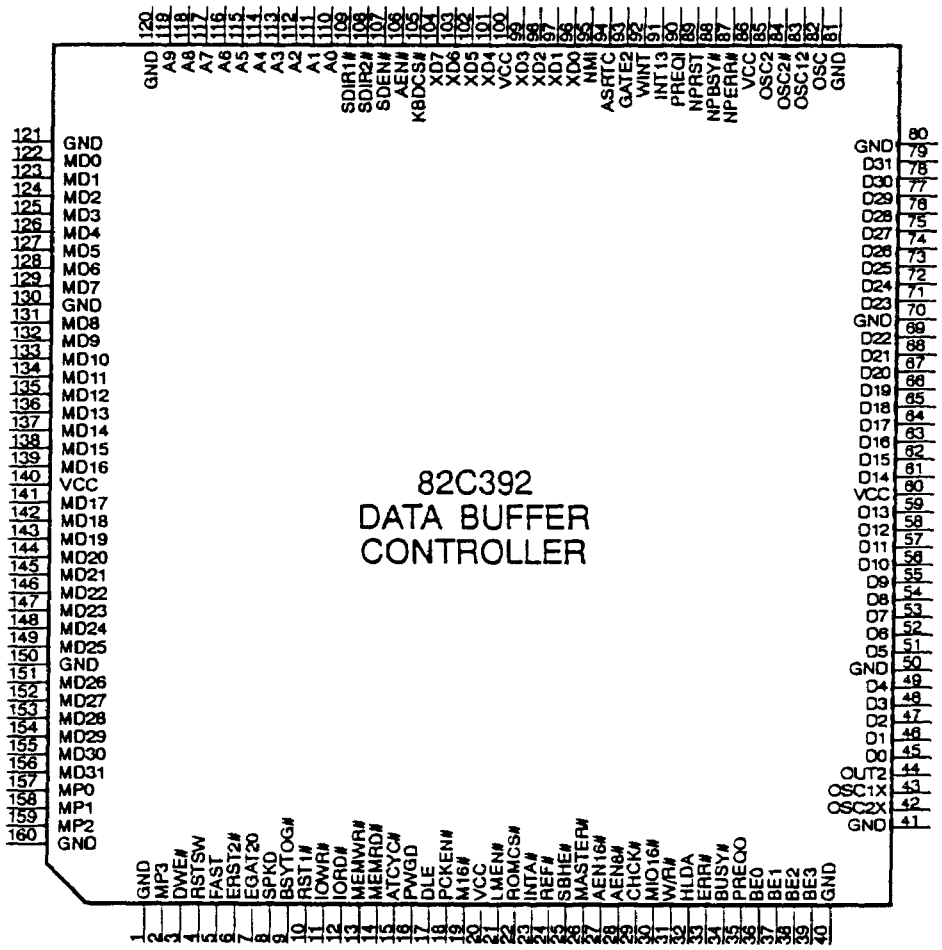

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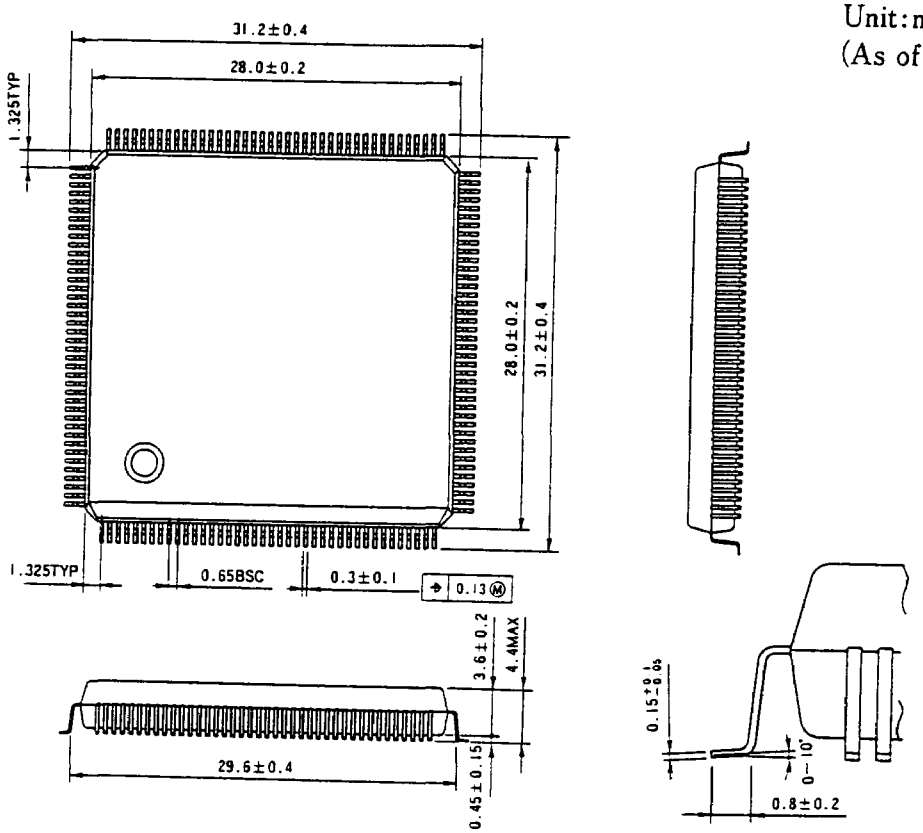
QFP160-P-2828(160-Pin Plastic Flat Package)

TENTATIVE

Unit: mm

(As of Jul. '89)



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OPTi Compatibility test Report
Hardware

Product: 486SXWB(82C493/82C392/82C206)
Date: 6/25/1991
Configuration: 20/25/33 MHz
8 / 64 Mb DRAM (80ns)
64K Cache memory

VENDOR	*PRODUCT*	*NOTE*
[CPU]		
INTEL	80486SX/80487SX	
[COPROCESSOR]		
WEITEK	4167	
[DISK CONTROLLER]		
ADAPTEC	SCSI AHA-1540/42B	
NCL	SCSI NCL500	
FUTURE DOMAIN	SCSI TMC-950	
ADAPTEC	SDI ACB-2322D	
DATA TECHNOLOGY	ESDI DTC-6280	
NCL	ESDI NDC535	
WESTERN DIGITAL	ESDI WD1007A-WA2	
WESTERN DIGITAL	ESDI WD1007V-SE2	
ULTRASTOR	ESDI ULTRA 12(F)	
ADAPTEC	RLL ACB-2370/72C	
SEAGATE	RLL ST-11	8 BIT CARD
DATA TECHNOLOGY	MFM DTC-5280	
DATA TECHNOLOGY	MFM DTC-7280	
WESTERN DIGITAL	MFM WD1003-WA2	
WESTERN DIGITAL	MFM WD1006V-MM2	
TMC	IDE IFSP-1.0	
TMC	DE CCAT-200/400	

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[DISK DRIVE]

FUJITSU	SCSI M2611SA	
MAXTOR	SCSI XT-4170S	
SEAGATE	SCSI ST-125N	
MAXTOR	ESDI XT-4380E	
MAXTOR	ESDI XT-8380E	
MICROPOLIS	ESDI 1355	
NEC	ESDI D5655	
SEAGATE	RLL ST-250R	
TOSHIBA	RLL MK134FA	
IMPRIMIS	MFM 94355-100	
MICROPOLICS	MFM 1335	
SEAGATE	MFM ST-SERIES	

[REMOVEABLE DISK]

PLUS	PASSPORT SYSTEM	

[FLOPPY DRIVE]

TEAC	FD-235HF	
TEAC	FD-55GFR	

[TAPE BACKUP]

MOUNTAIN	FILESAFE	INTERNAL TAPE BACKUP

[VIDEO CARD]

ATI	WONDER-16	
INFINITI	INVGA-16	
LCS	LCS-8856	8 BIT VGA
ORCHID	PRO-DESIGNER 800	8 BIT VEGA
ORCHID	PRO-DESIGNER-16	
ORCHID	PRO-DESIGNER II	
PARADISE	VGA PLUS-16	
TRIDENT	TVGA 8800CS-16	
VIDEO 7	VGA 1024i-16	
VIDEO 7	VGA VRAM VGA	

[EXPANDED MEMORY BOARD]

EVEREX	RAM-10000
INTEL	ABOVE BOARD

[INPUT DEVICE]

LOGITECH	BUS MOUSE
LOGITECH	SERIAL MOUSE
MICROSOFT	SERIAL MOUSE
PC MOUSE	SERIAL MOUSE

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OPTi Compatibility test Report
Software

Product: 486SXWB(82C493/82C392/82C206)
Date: 6/25/1991
Configuration: 20 /25/33 MHz
8/ 64 Mb DRAM (80ns)
64k Cache memory

VENDOR	*PRODUCT*	*NOTE*
[OPERATING SYSTEM /APPLICATION]		
SCO	UNIX/V	R3.2.0
SCO	XSIGHT(XWINDOWS)	R2.2.0
C/O WATERSIDE ASSOC.	SPEC BENCHMARK	R1.2
IBM	OPERATING SYSTEM /2	V1.1
IBM	OPERATING SYSTEM /2	V1.2
MICROSOFT	OPERATING SYSTEM /2	V1.1
MICROSOFT	DISK OPERATING SYSTEM	V3.3
[LAN] - SERVER/STATION/BRIDGE/INTERFACE		
NOVELL	NETWARE 286	V2.15
NOVELL	NETWARE SFT	V2.15
MICROSOFT	WINDOWS(NETWORKING)	V3.0
BORLAND	PARADOX386(LAN PACK)	R3.0
DATAPOINT	ARCNET	8 BIT
DATAPOINT	ARCNET	16 BIT
D-LINK	ETHERNET DE-100	8 BIT
D-LINK	ETHERNET DE-150	8 BIT
D-LINK	ETHERNET DE-200	16 BIT
EVEREX	ETHERNET SPEEDLINK/PC16	16 BIT
3COM	ETHERLINK II 3C503	8 BIT
3COM	ETHERLINK PLUS 3C505	16 BIT
[APPLICATION]		
WINDOWS/SHELL		
MICROSOFT	WINDOWS	V3.0
QUARTERDECK	DESQVIEW386	V2.3

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CAD/GRAPHICS/PAINT		
AUTODESK	AUTOCAD	V2.62
AUTODESK	AUTOCAD	V10
MICROSOFT	PAGEMAKER	V3.0
MICROSOFT	PAINTPRUSH	
ORCAD	ORCAD	V3.22
SOFTWARE PUBLISHING	HARDVARD GRAPHICS	V3.2
VIEW LOGIC	WORKVIEW	V4.0
DATA BASE/SPREAD SHEET		
BORLAND	PARADOX 386	V3.0
LOTUS	LOTUS 123	V2.2/V3.1
MICROSOFT	EXCEL	V2.1P
WORD PROCESSING		
MICROSOFT	WORD	V5.0
UTILITIES		
CENTRAL POINT	PCTOOLS	V5.5
EXECUTIVE SYSTEM	XTREE-PRO	V1.0
FIFTH GENERATION	FASTBACK	V2.10
SOFTLOGIC SOLUTION	DISK OPTIMIZER	V4.05
DIAGNOSTICS		
BYTE	BYTE BENCHMARK	V1.3
DIAGSOFT	QAPLUS	V4.52
DATA BASE	POWER METER	V1.5
LANDMARK	SPEED	V1.14
PC LAB	BENCH	V5.5
TOUCHSTONE	CHECKIT	V2.01
GAME		
MICROSOFT	FLIGHT SIMULATOR	V3.0

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OPTi-486SXWB Benchmark Test Report
(82C493 & 82C392)

Configuration :

486WB TMP Board, 64K cache, 8MB DRAM on board

Power Meter 1.5 :

20MHz - 8.838 mips
25MHz - 11.072 mips
33MHz - 14.707 mips
50MHz - 22.145 mips

Landmark Speed 1.14 :

20MHz - 90.8MHz
25MHz - 113.6MHz
33MHz - 151.3MHz
50MHz - 200+ MHz

PC Magazine 5.5 :

20MHz -

CPU instruction mix	1.84 secs
CPU 128 NOP loop	0.95 secs
CPU do nothing loop	0.70 secs
CPU integar addition	0.27 secs
CPU interger multiplication	0.30 secs
CPU string sort & move	0.57 secs
CPU prime number sieve	0.18 secs
CPU floating point mix	2.96 secs
Conventional memory read	0.33 secs
Conventional memory write	0.27 secs
Extended memory read	1.59 secs
Extended memory write	1.42 secs

25MHz -

CPU instruction mix	1.47 secs
CPU 128 NOP loop	0.75 secs
CPU do nothing loop	0.63 secs
CPU integar addition	0.22 secs
CPU interger multiplication	0.24 secs
CPU string sort & move	0.44 secs
CPU prime number sieve	0.14 secs
CPU floating point mix	2.36 secs

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Conventional memory read	0.28 secs
Conventional memory write	0.28 secs
Extended memory read	1.26 secs
Extended memory write	1.15 secs

33MHz -

CPU instruction mix	1.11 secs
CPU 128 NOP loop	0.57 secs
CPU do nothing loop	0.47 secs
CPU integar addition	0.15 secs
CPU interger multiplication	0.18 secs
CPU string sort & move	0.34 secs
CPU prime number sieve	0.10 secs
CPU floating point mix	1.81 secs
Conventional memory read	0.22 secs
Conventional memory write	0.16 secs
Extended memory read	1.20 secs
Extended memory write	1.10 secs

50MHz -

CPU instruction mix	0.71 secs
CPU 128 NOP loop	0.39 secs
CPU do nothing loop	0.32 secs
CPU integar addition	0.11 secs
CPU interger multiplication	0.12 secs
CPU string sort & move	0.24 secs
CPU prime number sieve	0.08 secs
CPU floating point mix	1.15 secs
Conventional memory read	0.16 secs
Conventional memory write	0.11 secs
Extended memory read	0.72 secs
Extended memory write	0.66 secs

Norton SI 4.5, Computing Index :

20MHz - 31.3
25MHz - 39.0
33MHz - 51.6
50MHz - 65.5

Byte Magazine 1.3 CPU Index :

20MHz - 2.87
25MHz - 3.60
33MHz - 9.60
50MHz - 14.4

OPTi-486SXWB Benchmark Test Report
(82C493 & 82C392)

Configuration :

486WB TMP Board, no secondary cache, 8MB DRAM on board

Power Meter 1.5 :

20MHz - 8.566 mips
25MHz - 10.707 mips

Landmark Speed 1.14 :

20MHz - 87.5MHz
25MHz - 110.3MHz

PC Magazine 5.5 :

20MHz -

CPU instruction mix	1.92 secs
CPU 128 NOP loop	0.83 secs
CPU do nothing loop	0.79 secs
CPU integar addition	0.28 secs
CPU interger multiplication	0.31 secs
CPU string sort & move	0.56 secs
CPU prime number sieve	0.17 secs
CPU floating point mix	3.25 secs
Conventional memory read	0.44 secs
Conventional memory write	0.33 secs
Extended memory read	2.47 secs
Extended memory write	2.30 secs

25MHz -

CPU instruction mix	1.53 secs
CPU 128 NOP loop	0.66 secs
CPU do nothing loop	0.63 secs
CPU integar addition	0.22 secs
CPU interger multiplication	0.24 secs
CPU string sort & move	0.46 secs
CPU prime number sieve	0.14 secs
CPU floating point mix	2.50 secs
Conventional memory read	0.33 secs
Conventional memory write	0.27 secs
Extended memory read	1.92 secs
Extended memory write	1.81 secs

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Norton SI 4.5, Computing Index :

20MHz - 31.1
25MHz - 41.0

Byte Magazine 1.3 CPU Index :

20MHz - 4.31
25MHz - 5.43

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486 WB TMP Board Jumper Information

(6 layers BABY AT Form Factor,Board # 486WB6A3.B1)

JP1 : OPEN - Color Monitor
CLOSE - Mono

JP2 : 1 - 2 Discharge 82C206
2 - 3 Battery Connection (normal operation)

JP3 : OPEN - ATCLK = CLK1/4
CLOSE - ATCLK = CLK1/6

JP4 : 1 - 2 Single phase clock
2 - 3 Double frequency clock

JP5 : 1 - 2 P23N Processor
2 - 3 80486 Processor
OPEN - P23 Processor

JP6 : 1 - 2 80486/P23N Processor
2 - 3 P23 Processor

JP7 : CLOSE - 80486/P23N Processor
OPEN - P23 Processor

JP8	OPEN	CLOSE
JP9	OPEN	CLOSE
JP10	OPEN	OPEN
CACHE	64K	256K

JP11 : OPEN - 64K CACHE
CLOSE - 256K CACHE

Other jumper and switch information can be read from the system board.

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486 WB TMP Board Jumper Information

(4 layer BABY AT Form Factor)

JP1 : 1 - 2 Discharge 82C206
2 - 3 Battery Connection (normal operation)

JP2 : OPEN - Color Monitor
CLOSE - Mono

JP3 : 1 - 2 P23N Processor
2 - 3 80486 Processor
OPEN - P23 Processor

JP4 : CLOSE - 80486/P23N Processor
OPEN - P23 Processor

JP5 : 1 - 2 80486/P23N Processor
2 - 3 P23 Processor

JP6 : OPEN - ATCLK = CLK1/4
CLOSE - ATCLK = CLK1/6

JP7 : 1 - 2 Single phase clock
2 - 3 Double frequency clock

JP8	OPEN	OPEN
JP9	OPEN	CLOSE
JP10	OPEN	CLOSE
CACHE	64K	256K

JP11 : TURBO LED

JP12 : OPEN - 64K CACHE
CLOSE - 256K CACHE

Other jumper and switch information can be read from the system board.

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