1.0 Overview

The OPTi Bus Master PCI IDE Module (MIDE) is designed for a fast and flexible interface between the PCI bus and two channels of IDE devices (Up to 4 devices). An integrated 8-level (32-byte) read-prefetch FIFO and a 8-level (32-byte) posted write FIFO supports zero wait-state bus mastering burst read and write operations on the PCI bus, substantially improving the performance over the typical slave IDE implementations. The enhanced ATA Specification can be supported either by setting Strap Options or by programming the internal registers up to mode 5 IDE timing.

2.0 MIDE Module Pin Descriptions

Pins of the MIDE Module may be multiplexed with other functional pins in the core logic chipsets and need external TTLs to de-multiplex them to go to the IDE connectors.

Name	Type	Description
IDEEN#	O	***IDE Enable.*** This pin is used to indicate that an IDE cycle is in progress. It should be connected to the chip enable of the external TTLs/De-multiplexers to select IDE control signals and data to go to the IDE connectors.
DINT0	I	***Primary Disk Interrupt.*** This signal is used to interrupt the host system for the primary IDE.
DINT1	I	***Secondary Disk Interrupt.*** This signal is used to interrupt the host system for the secondary IDE.
DA[2:0]	I/O	***Drive Address Line [2:0].*** These are the 3-bit binary coded address asserted by the host to access a register or data port in the drive.
DCHRDY	I	***I/O Channel Ready.*** This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the drive is not ready to respond to a data transfer request. When DCHRDY is not negated, DCHRDY is in a high impedance state.
DCS01#	I/O	***Primary Drive Chip Select 1.*** This is the chip select signal decoded from the host address bus used to select the Command Block Registers for the primary IDE.
DCS03#	I/O	***Primary Drive Chip Select 3.*** This is the chip select signal decoded from the host address bus used to select the Control Block Registers for the primary IDE.
DCS11#	I/O	***Secondary Drive Chip Select 1.*** This is the chip select signal decoded from the host address bus used to select the Command Block Registers for the secondary IDE.
DCS13#	O	***Secondary Drive Chip Select 3.*** This chip select signal is decoded from the host address bus used to select the Control Block Registers for the secondary IDE.
DD[15:0]	I/O	***Disk Data Bus Lines 0 to 15.*** These sixteen data bus lines require an external pull-up.
DIOR#	O	***Drive I/O read.*** This is the Read strobe signal. The low level of DRD# enables data from a register or the data port of the drive onto the data bus DD[7:0] or DD[15:0].
DIOW#	O	***Drive I/O write.*** This is the Write strobe signal. The rising edge of DWR# samples data from the data bus DD[7:0] or DD[15:0] into a register or the data port of the drive.
DDREQ0#	O	***Primary DMA Request.*** This is the DMA request of the Primary Bus-Mastering IDE.
DDACK0#	I	***Primary DMA Acknowledge.*** This is the DMA acknowledge of the Primary Bus-Mastering IDE.
DDREQ1#	O	***Secondary DMA Request.*** This is the DMA request of the Primary Bus-Mastering IDE.
DDACK1#	I	***Secondary DMA Acknowledge.*** This is the DMA acknowledge of the Primary Bus-Mastering IDE.

3.0 Configuration Register Descriptions

The configuration space for the Integrated Bus-Master IDE can be mapped in different locations in different OPTi chipsets. In the case of the 82C558M (Viper-M chipset) it can be mapped into two locations. It is controlled by Index FFh bit 4. If this bit is set to 0, the configuration space is mapped as Device 15h (AD31 = 1) function 0. If this bit is 1, it is mapped as Device 1h (AD 12 = 1) function 1. This section describes the registers implemented in the 256 byte configuration space. All registers not implemented always return zero during read cycles.

3.1 Vendor ID Register (00h, Read Only)

Bits	Mnemonic	Description	Default
15:0	VID	***Vendor ID:*** This register identifies the OPTi ID.	1045h

3.2 Device ID Register (02h, Read Only)

Bits	Mnemonic	Description	Default
15:0	DID	***Device ID:*** This register identifies the ID of the bus master IDE controller.	C621h

3.3 Command Register (04h, R/W)

Bits	Mnemonic	Description	Default
[15:7]	----	Reserved - Read only.	0
6	PEN	***Parity Checking Enable:*** When this bit is set, MIDE Module generates PERR# if a parity error occurs during I/O write cycles. If the bit is reset, parity checking is ignored. For I/O read cycles, MIDE Module always generates the parity bit.	0
5	----	Reserved - Read only.	0
4	MWI	***Memory Write and Invalid:*** When this bit is 1, MIDE Module may generate the command. When it is 0, Memory Write will be used instead.	0
3	----	Reserved - Read only.	0
2	MSTR	***Master Enable:*** When this bit is 1. The MIDE module is a PCI master to generate PCI accesses.	0
1	----	Reserved - Read only.	0
0	IOEN	***Input/Output Enable:*** When this bit is set, MIDE Module enables the I/O accesses. If reset, all I/O accesses are disabled.	1

3.4 Status Register (06h, R/W)

Bits	Mnemonic	Description	Default
15	PER	***Parity Error:*** This bit is set whenever the MIDE Module detects a parity error. This bit is cleared by writing 8000h to this register.	0
14	----	Reserved - Read Only.	0
13	MABORT	***Master Abort:*** As a PCI master, the MIDE Module sets this bit to 1 when its transaction is terminated with a master abort.	0
12	TABORT	***Target Abort:*** As a PCI master, the MIDE Module sets this bit to 1 when its transaction is terminated with a target abort.	0

Bits	Mnemonic	Description	Default
11	----	Reserved - Read Only.	0
[10:9]	SELTIM	***Select Timing:*** These are read only bits indicating allowable timing assertion for DEVSEL#.	01
8	DPER	***Data Parity:*** As a PCI master, the MIDE Module sets this bit to 1 when it detected a data parity error. 0 = No data parity detected 1 = Data parity detected.	0
7	BTB	***Back-To-Back Transactions.*** This is a read only bit, set to 1 to allow fast back-to-back transactions.	1
[6:0]	-----	Reserved - Read only.	0

3.5 Revision ID Register (08h, Read Only)

Bits	Mnemonic	Description	Default
7:0	REVID	***Revision ID:*** This register identifies the revision number of the bus master IDE controller.	0

3.6 Class Code Register (09h, R/W)

Bits	Mnemonic	Description	Default
23:8	CCODE (read only)	***Class Code:*** The MSB indicates the base class code for the mass storage controller. The middle byte indicates the sub class code (IDE controller).	0101h
7	PI7	***Bus-Mastering IDE Signature.*** This bit is read-only and is set to 1 to indicate Master Mode support.	1
6:4	----	Reserved - Read only	000
3	PI3	***Writability of the Native/Legacy Bit for Secondary IDE.*** This bit controls whether bit-2 of this register is read only or read/write. 0 = bit-0 read only 1 = bit-0 read/write This bit is set only when both the FNC0 and the RELOC bit (Configuration Offset 40h bits[3:2]) are set.	0
2	PI2	***Native/Legacy for Secondary IDE.*** This bit controls whether the secondary IDE is in Native or Legacy Mode. 0 = Legacy Mode 1 = Native Mode	0
1	PI1	***Writability of the Native/Legacy Bit for Primary IDE.*** This bit controls whether bit-0 of this register is read only or read/write. 0 = bit-0 read only 1 = bit-0 read/write If the RELOC bit (Configuration offset 40h bit 2) is reset, this bit is 0. When the RELOC bit is set, this bit is 1.	0
0	PI0	***Native/Legacy for Primary IDE.*** This bit controls whether the primary IDE is in Native or Legacy Mode. 0 = Legacy Mode 1 = Native Mode	0

3.7 Header Type Register (0Eh, Read Only)

Bits	Mnemonic	Description	Default
7:0	HDR	***Header Type:*** Single function device.	00h

3.8 Command Block Base Address Register (10h, R/W) (Primary IDE)

Bits	Mnemonic	Description	Default
31:0	IO1	***Command Block Base Address:*** This register is the I/O space indicator for the Drive Command Block. The address block has a size of 8 bytes. Bit [2:0] of this register are read only and default to 001. Bits [31:3] are writable if RELOC bit is set to 1. If the RELOC bit is set to 0, bits [31:0] are read only and return 0.	1F1h w/ RELOC=1

3.9 Control Block Base Address Register (14h, R/W) (Primary IDE)

Bits	Mnemonic	Description	Default
31:0	IO2	***Control Block Base Address:*** This register is the I/O space indicator for the Drive Control Block. The address block has a size of 4 bytes. Bit [1:0] of this register are read only and default to 01. Bits [31:2] are writable if RELOC bit is set to 1. If the RELOC bit is set to 0, bits [31:0] are read only and return 0.	3F5h w/ RELOC=1

3.10 Command Block Base Address Register (18h, R/W) (Secondary IDE)

Bits	Mnemonic	Description	Default
31:0	IO3	***Command Block Base Address:*** This register is the I/O space indicator for the Drive Command Block. The address block has a size of 8 bytes. Bit [2:0] of this register are read only and default to 001. Bits [31:3] are writable if RELOC bit is set to 1. If the RELOC bit is set to 0, bits [31:0] are read only and return 0.	171h w/ RELOC=1 FNC0=0

3.11 Control Block Base Address Register (1Ch, R/W) (Secondary IDE)

Bits	Mnemonic	Description	Default
31:0	IO4	***Control Block Base Address:*** This register is the I/O space indicator for the Drive Control Block. The address block has a size of 4 bytes. Bit [1:0] of this register are read only and default to 01. Bits [31:2] are writable if RELOC bit is set to 1. If the RELOC bit is set to 0, bits [31:0] are read only and return 0.	375h w/ RELOC=1 FNC0=0

3.12 Bus-Master IDE Base Address Register (20h, R/W)

Bits	Mnemonic	Description	Default
31:0	IO5	***Bus-Master IDE Base Address.*** This register is the I/O base address indicator for the Bus Master IDE registers. The address block has a size of 16 bytes. Bit [3:0] of this register is read-only and default to 0001. Bit [31:4] is writable.	8000 0001h

3.13 Interrupt Line Register (3Ch, R/W)

Bits	Mnemonic	Description	Default
7:0	INTL	***Interrupt Line.*** This register indicates which input of the system interrupt controller the INTA# interrupt pin is routed to.	Eh

3.14 Interrupt Pin Register (3Dh, Read Only)

Bits	Mnemonic	Description	Default
7:0	INTP	***Interrupt Pin.*** The content of this register is 1 (i.e., INTA# will be used).	1

3.15 IDE Initialization Control Register (40h, R/W)

Bits	Mnemonic	Description	Default
31:8	----	Reserved - Must be written 0.	
7:6	EMODE[1:0]	***Enhanced Mode[1:0].*** These two bit are for IDE Device Mode 4 and 5 for 16-bit Cycle Times. If EMODE[1:0] are set to 00, bit [1:0] of this register will be used to control the Cycle Time. 00: Mode 0, 1, 2 or 3] 01: Mode 4 10: Mode 5 11: Reserved	00
5	ESLAVE	***Enhanced Slave.*** 0: 82C621A compatible slave mode, uses 16-byte FIFO 1: Enhanced slave mode, uses 32-byte FIFO.	0
4	IDEP	***Default ISA ownership.*** 0: MIDE Module request ISA bus only when MIDE Module needs to access IDE cable. 1: MIDE Module request ISA bus always.	0
3	FNC0	***Function 0.*** Function 0 enables or disables the secondary IDE as follows: 0: Secondary IDE enabled. 1: Secondary IDE disabled.	0
2	RELOC	***Address Relocation.*** RELOC decides whether the I/O space addresses are relocatable through programming configuration space registers. 0: Fixed I/O addresses (1F0h-1F7h, 3F6h for primary; 170h-177h, 376h for secondary) 1: Relocatable I/O addresses.	0

Bits	Mnemonic	Description	Default
[1:0]	MODE[1:0]	***Mode [1:0].*** MODE[1:0] sets the IDE Device Mode for 16-bit cycle times: Mode 1 Mode 0 Cycle time 0 0 ≥ 600ns 0 1 ≥ 383ns 1 0 ≥ 240ns 1 1 ≥ 180ns	00

4.0 I/O Register Descriptions

4.1 I/O Registers for Primary IDE

The register addresses are referred to in this section by their power-up default addresses. If the power-up default is modified by writing to configuration register IO1, then these registers will be relocated accordingly.

The MIDE Module contains registers at seven I/O ports accessible after two consecutive 16-bit I/O reads from address 1F1h. Any other I/O cycle between these two reads will disable access to the MIDE Module registers.

4.1.1 Internal ID Register (1F2h, Write Only)

Bits	Mnemonic	Description	Default
7	CNFDIS	***Configuration Disable:*** This bit must be set to '0' in order to access MIDE Module A Internal Registers. Any write to this register with CNFDIS = 1 will disable all accesses to the MIDE Module registers until another two consecutive I/O reads from 1F1h.	1
6	CNFOFF	***Configuration Off.*** This bit must be set to '0' in order to access MIDE Module Internal Registers. Any write to this register with CNFOFF = 1 will disable all accesses to the MIDE Module registers until power down or reset.	0
[5:2]	----	Reserved - Must be written 0.	
[1:0]	----	Reserved - Must be written 11.	

4.1.2 Read Cycle Timing Register-A (1F0h, Index-0, R/W)

This register shares the I/O address with the Read Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.1.3 Read Cycle Timing Register-B (1F0h, Index-1, R/W)

This register shares the I/O address with the Read Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.1.4 Write Cycle Timing Register-A (1F1h, Index-0, R/W)

This register shares the I/O address with the Write Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.1.5 Write Cycle Timing Register-B (1F1h, Index-1, R/W)

This register shares the I/O address with the Write Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). SeeTable 2-7.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.1.6 Control Register (1F3h, R/W)

Bits	Mnemonic	Description	Default
7	REGTIM2	***Enable Timing Registers-B.*** When set, this bit enables cycle-timing registers-B (1F0h & 1F1h of the Index-1) to override the IDE timing set by the PCI configuration offset 40h bit [1:0] for any drive not selected by 1F3h bit [3:2]. It also enables the miscellaneous timing register 1F6h bits [5:1] to override the timing set by the PCI configuration offset 40h bit [1:0].	0
[6:5]	----	Reserved: Must be written with 0.	0
4	EN1WSRD	***Enable 1-Wait State Read.*** 1 = 1WS minimum for data reads, 0 = 2 WS minimum.	0
3	REGTIM1	***Enable Timing Register-A, Drive 1:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the PCI configuration offset 40h bit [1:0] for Drive-1.	0
2	REGTIM0	***Enable Timing Register-A, Drive 0:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the PCI configuration offset 40h bit [1:0] for Drive-0.	0
1	----	Reserved - Must be written 0.	0
0	----	Reserved - Must be written 1.	1

Note For all new software controls the IDE timing through registers programming, bits 2, 3 and 7 of the Control register should be enabled after the Cycle Timing Registers and Miscellaneous Register are programmed. See Table 2-2 for programming options.

4.1.7 Strap Register (1F5h)

Bits	Mnemonic	Description	Default
7	----	Reserved - Must be written 1.	0
[6:5]	REV[1:0]	***Revision Number Register (Read Only).*** When the value of this register is set to 11, the content of REVID register should be used to find the revision level of the chip.	11
4	DINTR	***DINTR Status (Read Only).*** Returns the state of DINTR input.	
[3:2]	MODE[1:0]	***Mode (Read Only).*** Returns information about drive speed as determined by MODE[1:0] bits. Please refer to the Mode Bit description for specific information.	00
1	----	Reserved - Must be written 1.	
0	SPD0	***CLK Speed (Read/Write).*** PCI-Bus CLK frequency select. SPD0 CLK 0 33 MHz 1 25 MHz	0

4.1.8 Miscellaneous Register (1F6h, R/W)

Bits	Mnemonic	Description	Default
7	----	Reserved - Must be written 0.	0
6	ENPREF	***Enable Read Prefetch:*** Enables/Disables Read Prefetch. At reset time, the value of this register is set by ENPREF strap option. 1 = Enable, 0 = Disable.	0
[5:4]	ASU[1:0]	***Address Setup Time:*** The value programmed in this register determines the address setup time between the DRD# or DWR# going active and the DA[2:0], DCS3#, DCS1# being presented, measured in CLKs. See Table 2-5.	x
[3:1]	DRDY[2:0]	***DRDY Delay:*** The value programmed in this register determines the minimum number of CLKs between DRDY# going high and DRD# or DWR# going inactive. See Table 2-6.	xx
0	INDEX-0	***Index-0:*** This bits is used to select between Cycle Timing Registers-A and -B located at 1F0h and 1F1h.	0

4.2 I/O Registers for Secondary IDE

The register addresses are referred to in this section by their power-up default addresses. If the power-up default is modified by writing to configuration register IO3, then these registers will be relocated accordingly.

The MIDE Module contains registers at seven I/O ports accessible after two consecutive 16-bit I/O reads from address 171h. Any other I/O cycle between these two reads will disable access to the MIDE Module registers.

4.2.1 Internal ID Register (172h, Write Only)

Bits	Mnemonic	Description	Default
7	CNFDIS	***Configuration Disable:*** This bit must be set to '0' in order to access MIDE Module Internal Registers. Any write to this register with CNFDIS = 1 will disable all accesses to the MIDE Module registers until another two consecutive I/O reads from 171h.	1

Bits	Mnemonic	Description	Default
6	CNFOFF	***Configuration Off.*** This bit must be set to '0' in order to access MIDE Module Internal Registers. Any write to this register with CNFOFF = 1 will disable all accesses to the MIDE Module registers until power down or reset.	0
[5:2]	----	Reserved - Must be written 0.	
[1:0]	----	Reserved - Must be written 11.	

4.2.2 Read Cycle Timing Register-A (170h, Index-0, R/W)

This register shares the I/O address with the Read Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.2.3 Read Cycle Timing Register-B (170h, Index-1, R/W)

This register shares the I/O address with the Read Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in CLKs (for a 16-bit read from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSSx# being presented (after a 16-bit read from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.2.4 Write Cycle Timing Register-A (171h, Index-0, R/W)

This register shares the I/O address with the Write Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.2.5 Write Cycle Timing Register-B (171h, Index-1, R/W)

This register shares the I/O address with the Write Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in CLKs (for a 16-bit write from the IDE Data Register). See Table 2-7.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSSx# being presented (after a 16-bit write from the IDE Data Register), measured in CLKs. See Table 2-8.	xxxx

4.2.6 Control Register (173h, R/W)

Bits	Mnemonic	Description	Default
7	REGTIM2	***Enable Timing Registers-B.*** When set, this bit enables cycle-timing registers-B (170h & 171h of the Index-1) to override the IDE timing set by the PCI Configuration offset 40h bit [1:0] for any drive not selected by 173h bit [3:2]. It also enables the miscellaneous timing register 176h bits [5:1] to override the timing set by the PCI Configuration offset 40h bit [1:0].	0
[6:4]	----	Reserved: Must be written with 0.	0
3	REGTIM1	***Enable Timing Register-A, Drive 1:*** When set, this bit enables cycle-timing registers-A (170h & 171h of the Index-0) to override the IDE timing set by the PCI Configuration offset 40h bit [1:0] for Drive-1.	0
2	REGTIM0	***Enable Timing Register-A, Drive 0:*** When set, this bit enables cycle-timing registers-A (170h & 171h of the Index-0) to override the IDE timing set by the PCI Configuration offset 40h bit [1:0] for Drive-0.	0
1	----	Reserved - Must be written 0.	0
0	----	Reserved - Must be written 1.	1

Note For all new software controls the IDE timing through registers programming, bits 2, 3 and 7 of the Control register should be enabled after the Cycle Timing Registers and Miscellaneous Register are programmed. See Table 2-2 for programming options.

4.2.7 Strap Register (175h)

Bits	Mnemonic	Description	Default
7	----	Reserved - Must be written 1.	1
[6:5]	REV[1:0]	***Revision Number Register (Read Only).*** When the value of this register is set to 11, the content of REVID register should be used to find the revision level of the chip.	11
4	SDINTR	***SDINTR Status (Read Only).*** Returns the state of SDINTR input.	
[3:2]	----	Reserved - Must be written 0.	
1	----	Reserved - Must be written 1.	
0	----	Reserved - Must be written 0.	

4.2.8 Miscellaneous Register (176h, R/W)

Bits	Mnemonic	Description	Default
7	----	Reserved - Must be written 0.	0
6	ENPREF	***Enable Read Prefetch:*** Enables/Disables Read Prefetch. At reset time, the value of this register is set by ENPREF strap option. 1 = Enable, 0 = Disable.	0
[5:4]	ASU[1:0]	***Address Setup Time:*** The value programmed in this register determines the address setup time between the DRD# or DWR# going active and the DA[2:0], DCSS3#, DCSS1# being presented, measured in CLKs. See Table 2-5.	x
[3:1]	DRDY[2:0]	***DRDY Delay:*** The value programmed in this register determines the minimum number of CLKs between DRDY# going high and DRD# or DWR# going inactive. See Table 2-6.	xx
0	INDEX-0	***Index-0:*** This bits is used to select between Cycle Timing Registers-A and -B located at 170h and 171h.	0

5.0 Physical Region Descriptor Table

Before the MIDE Controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This table contains some number of Physical Region Descriptors (PRD) which describe areas of memory that are involved in the data transfer. The descriptor table must be aligned on a 4 byte boundary and the table cannot cross a 64K boundary in memory.

5.1 Physical Region Descriptor

The physical memory region to be transferred is described by a Physical Region Descriptor (PRD). The data transfer will proceed until all the regions described by the PRDs in the table have been transferred.

Each Physical Region Descriptor entry is 8 bytes in length. The first 4 bytes specify the start address of a physical memory region. The next bytes specify the size of the region in bytes (64K byte limit per region). A value of zero in these 2 bytes indicates 64K. Bit 7 of the last byte indicates the end of the table; bus master operation terminates when the last descriptor has been retired.

5.2 Physical Region Descriptor Table Entry

Bits	Mnemonic	Description	Default
Byte-0 bit[0]	------	0: Read-only	0
Byte-[3:1], Byte-0 bit[7:1]	BASE	Memory Region Physical Base Address [31:1]	xxxxxxxx
Byte-4 bit[0]	------	0: Read-only	0
Byte-5, Byte-4 bit[7:1]	COUNT	Byte Count[15:1]	xxxx
Byte-6	-------	Reserved	xx
Byte-7 bit[6:0]	-------	Reserved	xx
Byte-7 bit[7]	EOT	End of Table	x

Note The memory region specified by the descriptor is further restricted such that the region cannot straddle a 64K boundary. This means the byte count is limited to 64K, and the incrementer for the current address register only extends from bit[1] to bit[15].

6.0 Bus Master IDE Registers

The bus master IDE function uses 16 bytes of I/O space. The base address of this block of I/O space is pointed to by Bus-Master IDE Base Address Register (IO5) in the PCI Configuration space. All bus master IDE I/O space registers can be accessed as byte, word, or dword quantities. The description of the 16 bytes of I/O registers is shown in Table 2-1.

Table 2-1 Bus Master IDE Registers

Offset	Register	Register Access
00h	Bus Master IDE Command Register for Primary IDE	R/W
01h	Device Specific	
02h	Bus Master IDE Status Register for Primary IDE	RWC
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address for Primary IDE	R/W
08h	Bus Master IDE Command Register for Secondary IDE	R/W
09h	Device Specific	
0Ah	Bus Master IDE status Register for Secondary IDE	RWC
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address for Secondary IDE	R/W

6.1 Bus Master IDE Command Register for Primary IDE (00h, R/W)

Bits	Description	Default
7:4	Reserved - Must be written 0.	0000
3	Read or Write Control: This bit sets the direction of the bus master transfer. When set to 0, PCI bus master reads are performed. When set to 1, PCI bus master writes are performed. This bit must NOT be changed when the bus master function is active.	0
2:1	Reserved: Must be written 0.	00
0	Start/Stop Bus Master: Writing a 1 to this bit enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing 0 to this bit. All state information is lost when a 0 is written; master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit of the Bus Master IDE Status Register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status Register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded before being written to memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE Active bit or the Interrupt bit of the Bus Master IDE Status Register for that IDE channel.	0

6.2 Bus Master IDE Status Register for Primary IDE (02h, R/W Clear)

Bits	Description	Default
7	Simplex only: This read-only bit indicates that both bus master channels (primary and secondary) can be operated at the same time.	0
6	Drive 1 DMA Capable: This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.	0
5	Drive 0 DMA Capable: This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.	0
4:3	Reserved Must be written 0.	00
2	Interrupt: This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a 1 is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is read as a 1 all data transferred from the drive is visible in system memory.	0
1	Error: This bit is set when the controller encounters an error transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a 1 is written to it by software.	0
0	Bus Master IDE Active: This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command Register. When this bit is read as 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.	0

6.3 Descriptor Table Pointer Register for Primary IDE (04h, R/W)

Bits	Description	Default
31:2	Base address of Descriptor table. Corresponds to A[31:2]	0000h
1:0	Reserved.	00

Note The Descriptor Table must be dword aligned and must not cross a 64K boundary in memory.

6.4 Bus Master IDE Command Register for Secondary IDE (08h, R/W)

Bits	Description	Default
7:4	Reserved - Must be written 0.	0000
3	Read or Write Control: This bit sets the direction of the bus master transfer. When set to 0, PCI bus master reads are performed. When set to 1, PCI bus master writes are performed. This bit must NOT be changed when the bus master function is active.	0
2:1	Reserved: Must be written 0.	00

Bits	Description	Default
0	Start/Stop Bus Master: Writing a 1 to this bit enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing 0 to this bit. All state information is lost when a 0 is written; master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit of the Bus Master IDE Status Register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status Register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded before being written to memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE Active bit or the Interrupt bit of the Bus Master IDE Status Register for that IDE channel.	0

6.5 Bus Master IDE Status Register for Secondary IDE (0Ah, R/W Clear)

Bits	Description	Default
7	Simplex only: This read-only bit indicates that both bus master channels (primary and secondary) can be operated at the same time.	0
6	Drive 1 DMA Capable: This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.	0
5	Drive 0 DMA Capable: This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.	0
4:3	Reserved Must be written 0.	00
2	Interrupt: This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a 1 is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is read as a 1 all data transferred from the drive is visible in system memory.	0
1	Error: This bit is set when the controller encounters an error transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a 1 is written to it by software.	0
0	Bus Master IDE Active: This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command Register. When this bit is read as 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.	0

6.6 Descriptor Table Pointer Register for Secondary IDE (0Ch, R/W)

Bits	Description	Default
31:2	Base address of Descriptor table. Corresponds to A[31:2]	0000h
1:0	Reserved.	00

Note The Descriptor Table must be dword aligned and must not cross a 64K boundary in memory.

7.0 Programming the MIDE Module Registers

7.1 Standard Programming Sequence for the Bus-Mastering Operations:

To initiate a bus master transfer between memory and an IDE DMA slave device, the following steps are required:

1. Software prepares a PRD Table in system memory. Each PRD is 8 bytes long and consists of an address pointer to the starting address and the transfer count of the memory buffer to be transferred. In any given PRD Table, two consecutive PRDs are offset by 8-bytes and are aligned on a 4-byte boundary.
2. Software provides the starting address of the PRD Table by loading the PRD Table Pointer Register. The direction of the data transfer is specified by setting the Read/Write Control bit. Clear the Interrupt bit and Error bit in the Status register.
3. Software issues the appropriate DMA transfer command to the disk device.
4. Engage the bus master function by writing '1' to the Start bit in the Bus Master IDE Command Register for the appropriate channel.
5. The controller transfers data to/from memory responding to DMA requests from the IDE device.
6. At the end of the transfer, the IDE device signals an interrupt.
7. In respond to the interrupt, software resets the Start/Stop bit in the command register. It then reads the controller status and then the drive status to determine if the transfer completed successfully.

7.2 Programming the IDE Mode Timing:

The following steps describe how to program the MIDE Module index registers to support IDE mode[3:0]. For IDE mode 4 and 5, data transfer timing can be programmed by PCI configuration offset 40h bit [7:6].

1. Program proper values into 1F0h and 1F1h, they are the default for Timing Register-A.
2. Set bit 0 of 1F6h to 1 to switch to Timing Register-B.
3. Program proper values into 1F0h and 1F1h, they reflect Timing Register-B.
4. Program proper values into bits [5:1] of 1F6h. It affects both Timing Register-A and Timing Register-B.
5. Enable bits 2, 3 and 7 in 1F3h. The following table describes the options for programming these three bits:

Table 2-2 REGTIMx Programming Options

REGTIM0	REGTIM1	REGTIM2	Drive 0 Control	Drive 1 Control
1*	0	1	Index-0	Index-1
0	1	1	Index-1	Index-0
0	0	1	Index-1	Index-1
1	0	0	Index-0	Straps
0	1	0	Straps	Index-0
0	0	0	Straps	Straps
1	1	x	Index-0	Index-0

*: Recommended Configuration

The following tables show the recommended index register clock settings to interface to different modes of the IDE drives.

Table 2-3 16-Bit Timing (LCLKs)

	PCI Bus Frequency							
	25MHz, 40ns				33MHz, 30ns			
Mode	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1
Command Pulse	5	4	3	2	6	5	4	3
Recovery Time	8	4	2	2	11	6	2	2
DRDY	2	2	2	2	2	2	2	2

Table 2-4 8-Bit Timing (LCLKs)

	PCI Bus Frequency							
	25MHz, 40ns				33MHz, 30ns			
Mode	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1
Command Pulse	9	9	9	9	11	11	11	11
Recovery Time	8	8	8	8	11	11	11	11
DRDY	5	5	5	5	6	6	6	6

Note The 8-bit settings are fixed and cannot be programmed.

Table 2-5 Address Setup

Bit 5	Bit 4	Timing, in LCLKs
0	0	1
0	1	2
1	0	3
1	1	4

Note Index Registers 1F6h/176h bits [5:4]

Table 2-6 DRDY Delay

Bit 3	Bit 2	Bit 1	Timing, in LCLKs
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7
1	1	0	8
1	1	1	9

Note Index Registers 1F6h/176h bits [3:1]

Table 2-7 Read/Write Command Pulse

Bit 7	Bit 6	Bit 5	Bit 4	Timing, in LCLKs	
				Read Command 1F0h/ 170h	Write Command 1F1h/ 171h
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	3	3
0	0	1	1	4	4
0	1	0	0	5	5
0	1	0	1	6	6
0	1	1	0	7	7
0	1	1	1	8	8
1	0	0	0	9	9
1	0	0	1	10	10
1	0	1	0	11	11
1	0	1	1	12	12
1	1	0	0	13	13
1	1	0	1	14	14
1	1	1	0	15	15
1	1	1	1	16	16

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write), Index 0/1, bits [7:4]

Table 2-8 Read/Write Recovery Time

Bit 3	Bit 2	Bit 1	Bit 0	Timing, in LCLKs	
				Read Recovery 1F0h/ 170h	Write Recovery 1F1h/ 171h
0	0	0	0	2	2
0	0	0	1	3	3
0	0	1	0	4	4
0	0	1	1	5	5
0	1	0	0	6	6
0	1	0	1	7	7
0	1	1	0	8	8
0	1	1	1	9	9
1	0	0	0	10	10
1	0	0	1	11	11

Bit 3	Bit 2	Bit 1	Bit 0	Timing, in LCLKs	
				Read Recovery 1F0h/ 170h	Write Recovery 1F1h/ 171h
1	0	1	0	12	12
1	0	1	1	13	13
1	1	0	0	14	14
1	1	0	1	15	15
1	1	1	0	16	16
1	1	1	1	17	17

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write) Index 0/1, bits [3:0]