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ENGINEERING FILE

EQUATIONS SPEED COMMON EMITTER BIAS DESIGN

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When designing transistor bias circuits for temperature stability an often used parameter is the incremental dc current gain or stability factor. This is defined as:

$$S = \frac{dI_c}{dI_{co}} \qquad (1)^*$$

where dI_c is the change in collector current associated with a change in collector to base leakage current dI_{co}. In circuit design, dI_{co} can be found from the manufacturers' literature and the permissible dI_c can be determined by consideration of the load line on the collector characteristics. Thus S can be calculated to give the maximum permissible stability factor.

Derivation of the stability factor equations for a number of common emitter circuits has shown that the relation:

$$S = \frac{k}{k-\alpha} \qquad (2)$$

is generally true with the equation for k depending on the particular circuit. Accordingly, only the k-factors are shown with the circuits given in the figures. For design purposes it is often more useful to re-arrange equation 2 to the form:

$$k = \frac{S\alpha}{S-1} \qquad (3)$$

In some cases k can be simplified to the form:

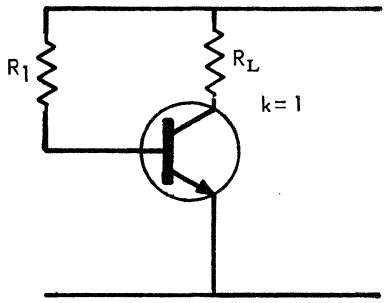
$$k = 1 + \frac{R_e}{R_2} \qquad (4)$$

to serve as a first approximation and, since R_e is usually chosen or known, R_2 can be found from:

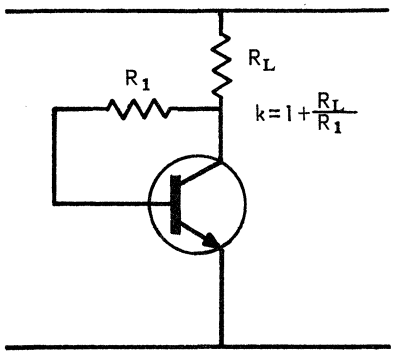
$$R_2 = \frac{R_e}{k-1} \qquad (5)$$

* R. F. Shea, Principles of Transistor Circuits, John Wiley and Sons, Inc., New York.

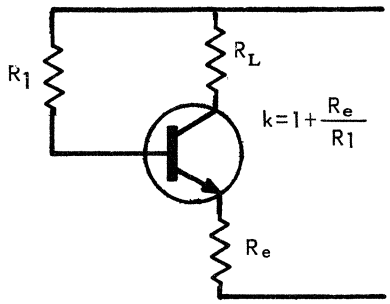
(1) SIMPLE BIAS



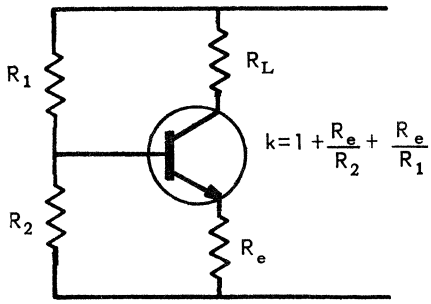
(2) SHUNT STABILIZATION



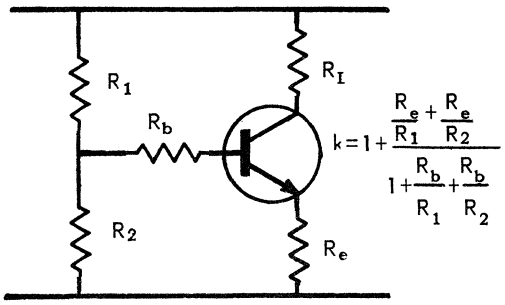
(3) SERIES STABILIZATION



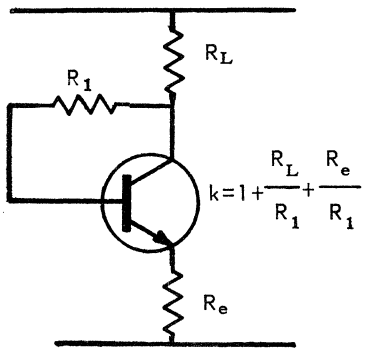
(4) SERIES STABILIZATION



(5) DEGRADED SERIES STABILIZATION



(6) COMPOUND STABILIZATION



(7) COMPOUND STABILIZATION