BA6589K

Read/write amplifier

The BA6589K IC incorporates read, write, and erase circuits for use with 3 in., 3.5 in., and 5 in. floppy disk drives.

It can be operated at either 5 V or 12 V. It has a power save mode which ensures the IC has a very low average current draw.

Features

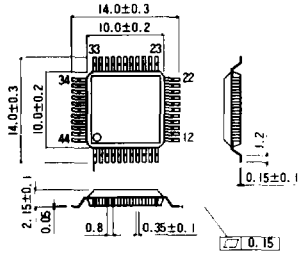
- available in a QFP44 package
- low power consumption, typically
  - — read mode is 250 mW
  - — write mode is 90 mW
  - — standby (power save) mode is 12 mW
- preamplifier differential voltage gain is 47.5 dB (5 V operation)
- includes a capacitor to set up the read data time constant and the pulse width
- includes a switching differential constant circuit
- write current is selectable as follows:
  - — double density inner track
  - — double density outer track
  - — high density inner track
  - — high density outer track
- selectable two-stage time domain filter
- includes a low voltage sensing circuit to avoid miswrites due to voltage fluctuations

Applications

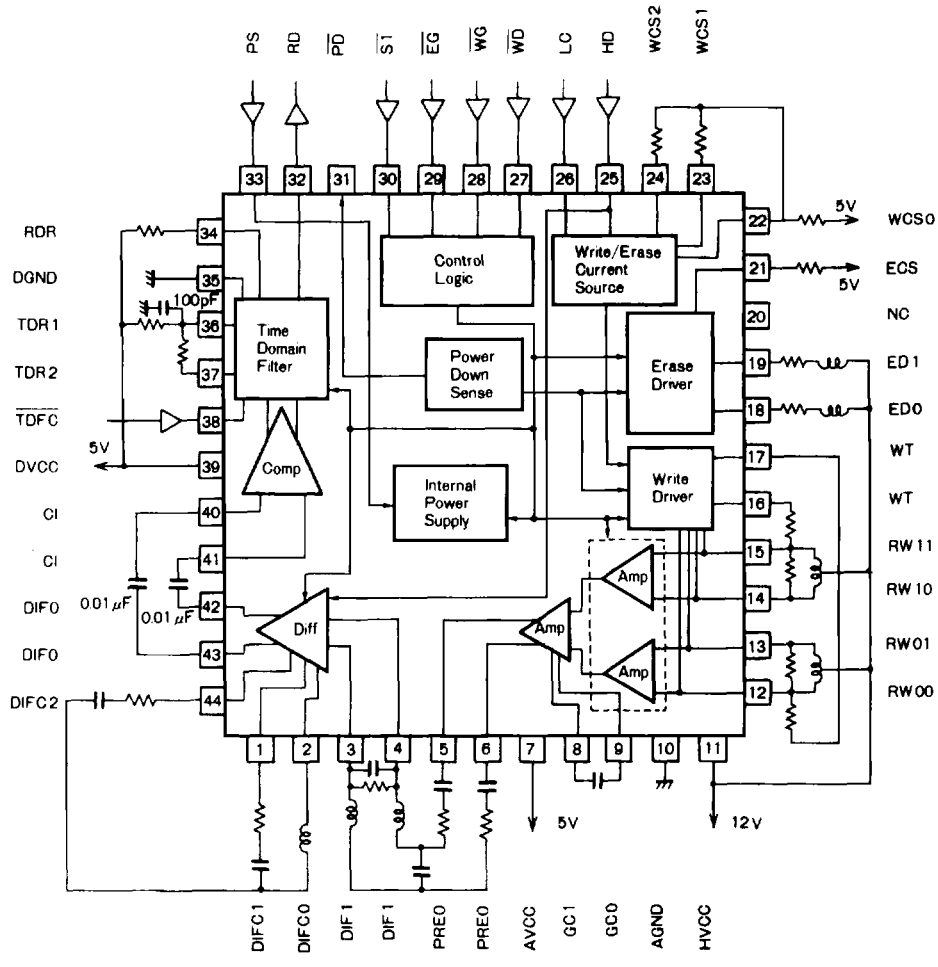
- 3 in., 3.5 in., and 5 in. high- or double density floppy disk drives

Dimensions (Units : mm)

BA6589K (QFP44)



Block diagram and external circuit



Note: Depending on the read/write head characteristics, when the write current switches, the current waveform may tend to cause oscillation (especially if the phase inverts at a frequency approaching 2 MHz). In this situation, use a circuit such as the one shown to the right, and check for oscillations.

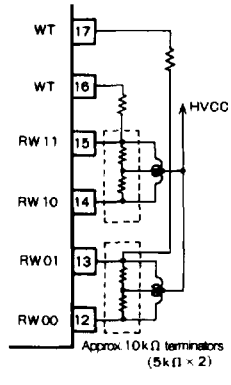


Table 1 Pin functions

Function	Pin no.	Symbol	Description
Head switching count	12, 13	RW00, RW01	Connections for side 0 read/write head
	14, 15	RW10, RW11	Connections for side 1 read/write head
Read preamp	9, 8	GC0, GC1	Gain adjust pins
	6, 5	PREO	Preamplifier differential outputs
Different-iator	4, 3	DIF1	Differentiator differential inputs
	2 1 44	DIFCO DIFC1 DIFC2	Connections for external differentiator circuit constant components
	43, 42	DIF0	Differentiator differential outputs
Comparator	41, 40	C1	Comparator differential inputs
Time domain filter	37	TDR2	Connection point for time domain filter time constant
	36	TDR1	Pin to set time domain filter
	34	RDR	Pin to set read data output pulse width
	32	RD	Read data output
Write circuit	22 23 24	WCS0 WCS1 WCS2	Pin to set write current Write current correction pin 1 (Valid when LC pin is HIGH) Write current correction pin 2 (Valid when HD pin is HIGH)
	16, 17	WT	Connection point for write damping resistor
Erase circuit	18	ED0	Side 0 erase output
	19	ED1	Side 1 erase output
	21	ECS	Pin to set erase current
Control logic input	25	HD	Standard density- to-high density switching pin (see note 1 on page 250).
	26	LC	Track inner/outer switching pin (see note 1 on page 250).
	27	$\overline{WD}$	Write data input
	8	$\overline{WG}$	Write enable input
	29	$\overline{EG}$	Erase enable input
	30	$\overline{S1}$	Input to switch head side
	33	PS	Power save mode input
	38	TDFC *3	Input to switch time domain filter constants (see note 2 on page 250).
Power-down sense	31	$\overline{PD}$	Power down sense output
Power supply	11	HVCC	Preamplifier supply voltage
	7 39	AVCC DVCC	Analog circuit supply voltage Digital circuit supply voltage
	10 35	AGND DGND	Analog circuit ground Digital circuit ground
	20	NC	Not used

Note 1:

HD	LC	Write current	Differentiator constants
HIGH	HIGH	Current set by pins 22, 23, and 24	Circuit constants between pins 44 and 2 are in effect.
	LOW	Current set by pins 22 and 24	
LOW	HIGH	Current set by pins 22 and 23	Circuit constants between pins 1 and 2 are in effect.
	LOW	Current set by pin 22	

Note 2: Correction applied when pin is HIGH. External correction resistors are placed in parallel with the primary resistances to set the values.

Absolute maximum ratings (T_a = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	AV_{CC}	+7	V
	DV_{CC}	+7	V
	HV_{CC}	+16	V
Digital circuit input voltage	V_I	−0.3 ~ DV_{CC} +0.3	V
RW pin voltage	V_{RW}	+25	V
PD pin output voltage	V_{PD}	+16	V
Erase drive current	I_{ER}	100	mA
EO pin voltage	V_{ER}	+25	V
Operating temperature	T_{opr}	0 ~ +70	°C
Storage temperature	T_{stg}	−55 ~ +125	°C

Recommended operating conditions (T_a = 0°C ~ 70°C)

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	AV_{CC}	4.4	5.0	6.0	V
	DV_{CC}	4.4	5.0	6.0	V
	HV_{CC}	10.8	12.0	13.2	V

Electrical characteristics (unless otherwise noted, T_a = 25°C, AV_{CC} = DV_{CC} = 5 V, HV_{CC} = 12 V) (Sheet 1 of 5)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test circuit
Supply current							
Supply current, standby	I_{CCHS}		0.33	0.80	mA	@ HV_{CC}	Fig. 3
	I_{CCDS}		0.82	1.3	mA	@ DV_{CC}	
	I_{CCAS}		0.8	1.3	mA	@ AV_{CC}	
Supply current, read	I_{CCHR}		5.80	8.10	mA	@ HV_{CC}	
	I_{CCDR}		20.0	28.0	mA	@ DV_{CC}	
	I_{CCAR}		17	23.5	mA	@ AV_{CC}	
Supply current, write	I_{CCHW}		0.60	1.20	mA	@ HV_{CC}, I_{WR} = I_{ER} = 0 mA	
	I_{CCDW}		10	18	mA	@ DV_{CC}, I_{WR} = I_{ER} = 0 mA	
	I_{CCAW}		7.0	10	mA	@ AV_{CC}, I_{WR} = I_{ER} = 0 mA	
Low voltage sensing circuit							
Threshold voltage	V_{TH}	3.5	3.9	4.2	V	LVS @ AV_{CC}	Fig. 4
Hysteresis voltage	V_H	50			mV		
Output low level voltage	V_{OL}			0.4	V	V_{CC} = 2 V, I_{OL} = 0.5 mA	
Output leakage current	I_{OH}			1	µA		
Recovery time							
Power save → read	$t_{\gamma 1}$			1	ms	Invoked by PS: With 0.01 µF coupling capacitors between differentiator and comparator, and <1 µF capacitors from differentiator input to GND	Fig. 5
Read → write	$t_{\gamma 2}$			4	µs	Invoked by $\overline{WG}$: Circuit constant capacitors (pin 44↔2 & pin 1↔2) are <0.01 µF	
Write → read	$t_{\gamma 3W}$			300	µs	Invoked by $\overline{WG}$	
	$t_{\gamma 3E}$			20	µs	Invoked by $\overline{EG}$	
Side0 ↔Side1	$t_{\gamma 4}$			40	µs	Invoked by $\overline{S1}$	
Preamplifier							
Diff. output voltage gain	G_{VD}	46	49	52	dB	f = 250 kHz, V_{IN} = 2.5 mV_{pk-pk}	Fig. 6
Frequency characteristic	BW	3			mHz	250 kHz = 0 dB, –3 dB	
Crosstalk side0 ↔ side1	G_{CTLK}	50			dB	f = 250 kHz	
Diff. input resistance	R_{ID}	20			kΩ		Fig. 7

Electrical characteristics (unless otherwise noted, T_a = 25°C, AV_{CC} = DV_{CC} = 5 V, HV_{CC} = 12 V) (Sheet 2 of 5)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test circuit
Input conversion noise voltage (1)	V_{N1}		4.5	8	μV_{rms}	f = 400 ~ 1 MHz	Fig. 8
Input conversion noise voltage (2)	V_{N2}		5	10	μV_{rms}	f = 400 ~ 1 MHz. Measured with 1 V_{pk-pk}, 250 kHz signal applied to differentiator input. TDF pulse width = 1.2 µs; RD pulse width = 0.5 µs	
Input sink current	I_{SINK}		100	200	µA		Fig. 9
Diff. input voltage max amplitude	V_{INmax}			15	mV_{pk-pk}	Includes measurements made with correction resistor between pins 8 & 9	Fig. 6
Diff. output voltage amplitude	V_{OD}	2			V_{pk-pk}	Distortion rate = 5%	
Diff. output resistance	R_{OD}		120		Ω		
Diff. output current amplitude	I_{OD}	5.8	7.4		mA_{pk-pk}		
Common mode rejection ratio	CMRR	50			dB	L = 330 µH, f = 250 kHz, V_{IN} = 100 mV_{pk-pk},	Fig. 10
Power supply rejection ratio	PSRR	60			dB	L = 330 µH, f = 125 kHz	Fig. 11
		40			dB	V_{IN} = 100 mV_{pk-pk} f = 400 kHz	
Differentiator							
Voltage gain	G_{VD}	14	16	18	dB	f = 250 kHz, R_E = 510 Ω	Fig. 12
Frequency characteristic	BW	3			MHz	250 kHz = 0 dB, −3 dB	
Crosstalk DIFC1 ↔ DIFC2	G_{CTLK}	45			dB	f = 250 kHz	
Differentiator input resistance	R_{ID}	30			kΩ		Fig. 13
Differentiator constants setting pin output resistance	R_{CD}		100		Ω		Fig. 12
Differentiator constants setting pin current	I_{SINK}	0.5	0.75		mA		Fig. 14
Diff. output resistance	R_{OD}		50		Ω		Fig. 12
Diff. output voltage amplitude	V_{OD}	2			V_{pk-pk}	Distortion rate = 5%	
Output sink current	I_{OSINK}	1.8	2.8		mA		Fig. 14

Electrical characteristics (unless otherwise noted, T_a = 25°C, AV_{CC} = DV_{CC} = 5 V, HV_{CC} = 12 V) (Sheet 3 of 5)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test circuit
Comparator and pulse shaper							
Differential input resistance	R_{ID}	10			kΩ		Fig. 15
Max differential input voltage	$V_{IN\ max}$	4			V_{pk-pk}		Fig. 17
TD monostable multivibrator pulse width adjustment range	t_{rD}	500		3000	ns		
TD monostable multivibrator pulse width accuracy (With Pin 37 (TDR2) open)	E_{TD1}	−20		+20	%	R_{TD} = 200 kΩ, *(t_{TD} ≈ 2.35 µs)	
	E_{TD2}	−12		+12	%	R_{TD} = 40 kΩ, C_{TD} = 100 pF, (t_{TD} ≈ 2.35 µs)	
TD monostable multivibrator pulse width voltage dependency With Pin 37 (TDR2) open	PSt_{rD1}	−12	−5	+4	%/V	R_{TD} = 200 kΩ, (t_{TD} ≈ 2.35 µs)	
	PSt_{rD2}	−6	−1	+4	%/V	R_{TD} = 40 kΩ, C_{TD} = 100 pF	
RD monostable multivibrator pulse width adjustment range	t_{RD}	125		1500	ns		
RD monostable multivibrator pulse width accuracy	E_{RD}	−20		+20	%	R_{RD} = 36 kΩ, t_{RD} ≈ 0.5 µs	
RD monostable multivibrator pulse width voltage dependency	PS_{tRD}	−12	−2	+12	%/V	R_{RD} = 36 kΩ, t_{RD} ≈ 0.5 µs	
Rise time	t_{TLH}			70	ns		
Fall time	t_{THL}			25	ns		
Peak shift	PS			1	%	V_{IN} = 0.15 ~ 2 V_{pk-pk}	
Low level output voltage	V_{OL}			0.5	V	I_{OL} = 2 mA	Fig. 16
High level output voltage	V_{OH}	2.7			V	I_{OH} = −0.4 mA	

Electrical characteristics (unless otherwise noted, T_a = 25°C, AV_{CC} = DV_{CC} = 5 V, HV_{CC} = 12 V) (Sheet 4 of 5)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test circuit
Write circuit							
Write current adjustment range	IWR	2		20	mA	Includes LC and HD pin correction currents. See note 1 on page 250	Fig. 18
Corrected write current adjustment range	IWC			5	mA	At LC and HD pin	
Write current accuracy	ACI_W	−7		+7	%	I_{WR} = 6 mA, R_{WCSO} = 1.9 kΩ	
Write current mismatch	ΔI_{WR}	−2		+2	%	R_{WCSO} = 1.9 kΩ	
Write current supply voltage dependency	PSI_W	−4	−2	+1	%/V	R_{WCSO} = 1.9 kΩ	
Output saturation voltage	V_{SATRW}		1.3	1.8	V	With Pin 37 (TDR2) open	
Off state leakage current	I_{LKRW1}			20	µA	Deselected side, V_{RW} = 14 V. With Pin 37 (TDR2) open	Fig. 18
	I_{LKRW2}			50	µA	Selected side, V_{RW} = 14 V $V_{RW\ pin}$ when output voltage set for I_W of 12 mA and decreased slowly to 10.8 mA	
Write data min pulse width	t_{WD}	70			ns		Fig. 19
Timing balance	ΔI_W			0.5	%	f = 500 kHz	Fig. 18
Erase output							
Erase current adjustment range	I_{ER}	5		100	mA		Fig. 20
Output saturation voltage	V_{SATER}		0.8	1.4	V	I_{ER} = 100 mA, R_{ECSO} = 1.8 kΩ	
Output leakage current	I_{OH}			100	µA	V_{OH} = 20 V	

Electrical characteristics (unless otherwise noted, T_a = 25°C, AV_{CC} = DV_{CC} = 5 V, HV_{CC} = 12 V) (Sheet 5 of 5)

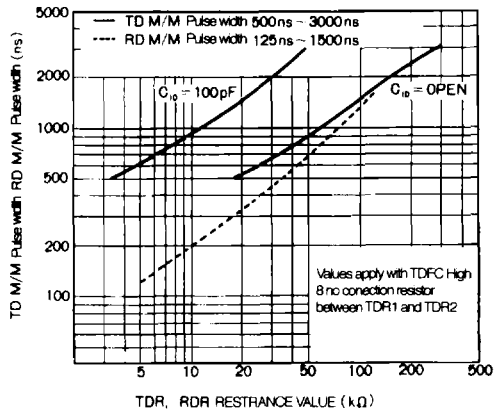
Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test circuit
Logic inputs							
High level input voltage 1	V_{IH1}	2			V	LC, HD, TDFC, PS	Fig. 21
Low level input voltage 2	V_{IL1}			0.8	V	LC, HD, TDFC, PS	
High level input voltage 1	V_{IH2}	2			V	$\overline{WG}$, $\overline{EG}$, $\overline{S1}$	
Low level input voltage 2	V_{IL2}			0.8	V	$\overline{WG}$, $\overline{EG}$, $\overline{S1}$	
Input volt hysteresis 2	V_{H2}	0.2			V	$\overline{WG}$, $\overline{EG}$, $\overline{S1}$	
High level input voltage 3	V_{IH3}	2			V	$\overline{WD}$	
Low level input voltage 3	V_{IL3}			0.7	V	$\overline{WD}$	
Input volt hysteresis 3	V_{H3}	0.2			V	$\overline{WD}$	
High level input current 1	I_{IH1}			10	µA	LC, HD, TDFC, PS V_{OH} = 2.8 V	
Low level input current 1	I_{IL1}			40	µA	LC, HD, TDFC, PS V_{OL} = 0.4 V	
High level input current 2	I_{IH2}			10	µA	$\overline{WG}$, $\overline{EG}$, $\overline{S1}$, V_{OH} = 2.8 V	
Low level input current 2	I_{IL2}			40	µA	$\overline{WG}$, $\overline{EG}$, $\overline{S1}$, V_{OL} = 0.4 V	
High level input current 3	I_{IH3}			10	µA	$\overline{WD}$, V_{OH} = 2.8 V	
Low level input current 3	I_{IL3}			400	µA	$\overline{WD}$, V_{OL} = 0.4 V	

The pin used to set the time domain filter TD monostable multivibrator pulse width (TDR1) has an internal capacitance of 15 pF. Therefore, the TD monostable multivibrator pulse width can be set using R_{TD} only. (R_{TD} is the external resistor used to pull-up the TDR1 pin to AVCC).

If this method is used, when TDFC is HIGH (no correction), the TD monostable multivibrator pulse width will have frequency characteristics due to the internal capacitance of the TDR2 pin.

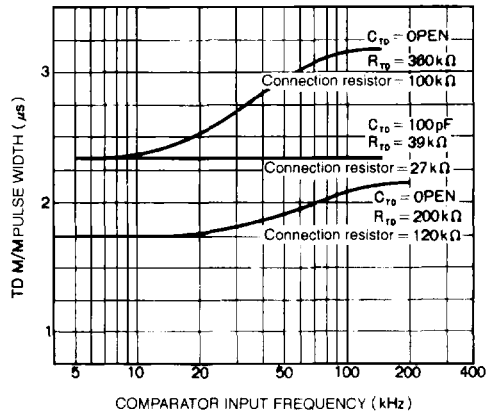
The effect of the internal capacitance of pin TDR2 can be reduced by inserting a 100 pF capacitor, C_{TD}, between the TDR1 pin and GND, to adjust the time constant. This will ensure that the TD monostable multivibrator pulse width does not vary with frequency. It will also reduce the influence of the 15 pF internal capacitance at TDR1, thus improving the accuracy of the TD monostable multivibrator pulse width timing.

Figure 2 shows the TD min/max pulse width against comparator input frequency when the value of C_{TD} is 100 pF, and when it is not in the circuit.



Values are for TDFC = HIGH and no resistor between TDR1 and TDR2

Figure 1 Time domain filter



Values are for TDFC = HIGH

Figure 2

Test circuits

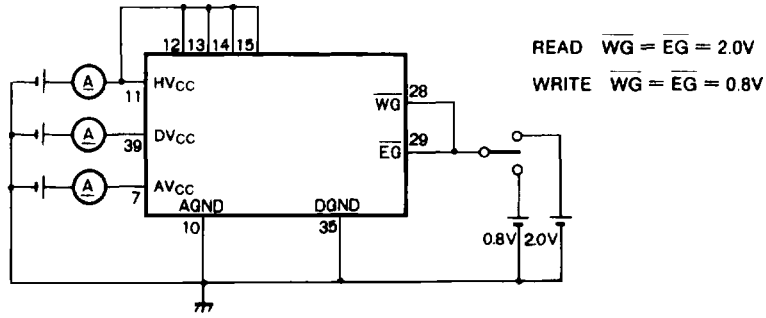
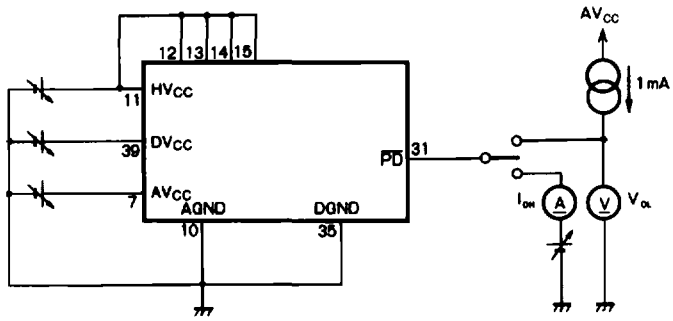


Figure 3 Supply current: I_{CCHS}, I_{CCHR}, I_{CCHW}, I_{CCDS}, I_{CCDR}, I_{CCDW}, I_{CCAS}, I_{CCAR}, I_{CCAW} test circuit



MONITOR I_{WR} (RW 00, RW 01, RW 10, RW 11)

I_{ER} ($E_0$0, $E_0$1)

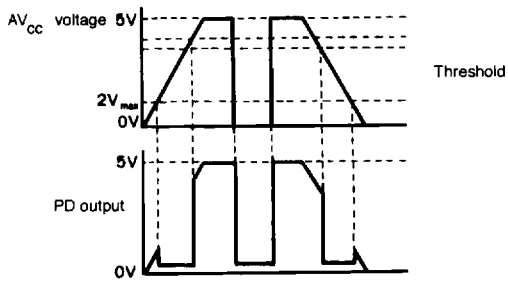


Figure 4 Power down (LVS at AV_{CC}): V_{TH}, V_H, V_{OL}, I_{OH} test circuit

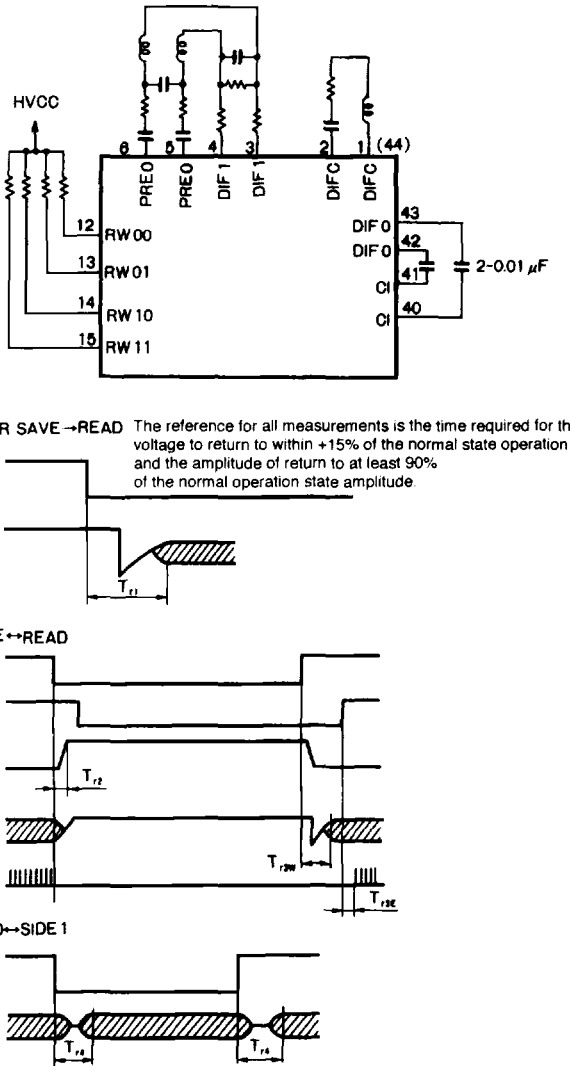


Figure 5 Recovery time: T_{r1}, T_{r2}, T_{r3W},T_{r3E}, T_{r4} test circuit

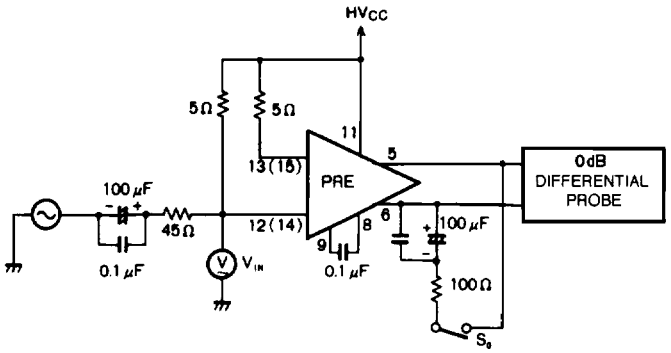
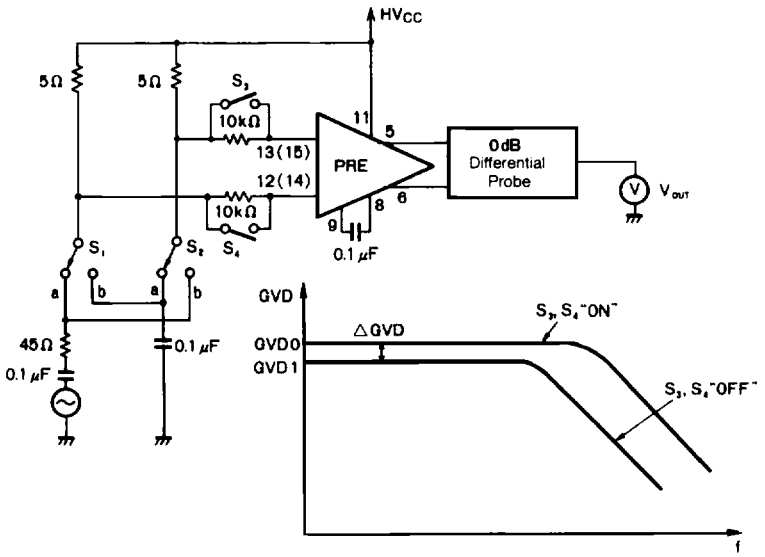


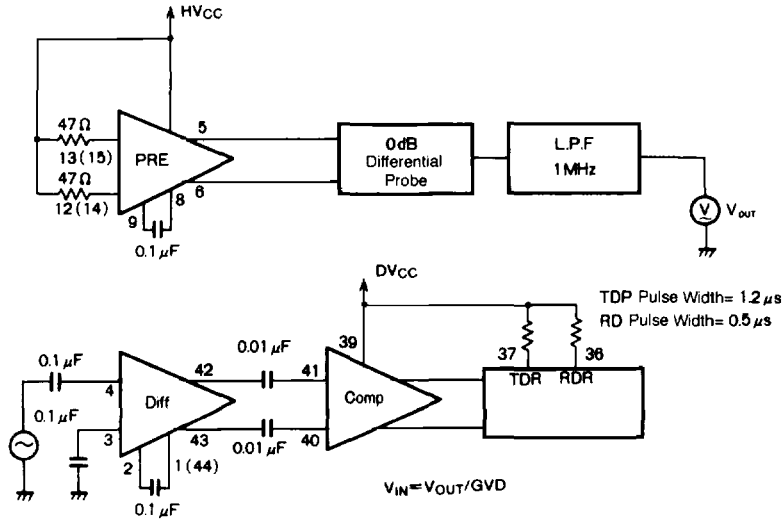
Figure 6 Preamplifier: G_{VD}, BW, G_{CTLK}, V_{INmax}, V_{OD}, R_{OD} test circuit



$$R_{ID}=\left(\frac{10^{-\Delta GVDa/20}}{1-10^{-\Delta GVDa/20}}+\frac{10^{-\Delta GVDb/20}}{1-10^{-\Delta GVDb/20}}\right)\times 1\Omega\ [k\Omega]$$

$\Delta GVDa$ = GVD (indB) when S_1 and S_2 are in the "a" position
$\Delta GVDb$ = GVD (indB) when S_1 and S_2 are in the "b" position

Figure 7 Differential input resistance test circuit



Note: Measure V_{N1} with no input signal to comparator
Measure V_{N2} with input signal to comparator and circuit outputting read data.

Figure 8 Input conversion noise voltage: V_{N1}, V_{N2} test circuit

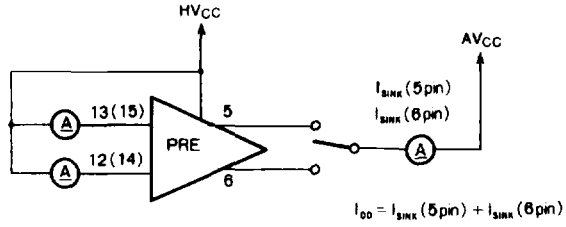


Figure 9 Input sink current I_{SINK} and diff output current amplitude I_{OD} test circuit

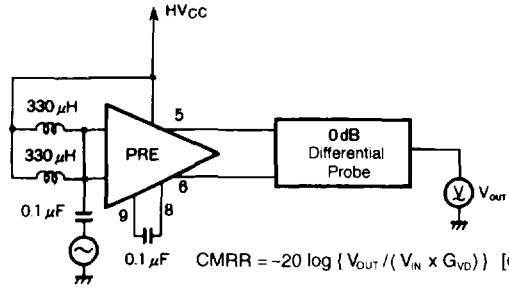


Figure 10 Common mode rejection ratio (CMRR) test circuit

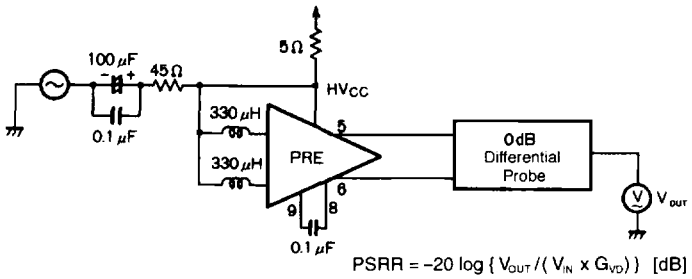


Figure 11 Power supply rejection ratio (PSRR) test circuit

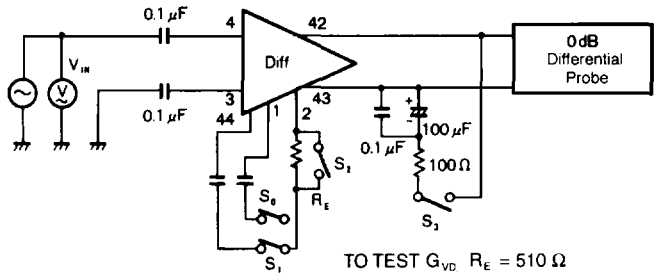


Figure 12 Differentiator: GVD, BW, G_{CTLK}, R_{CD}, V_{OD}, R_{OD} test circuit

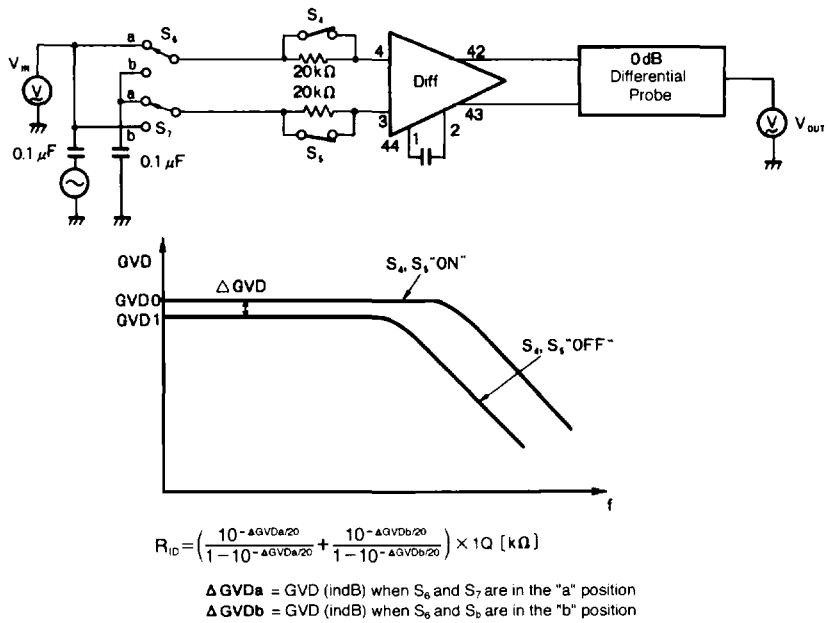


Figure 13 Differential input resistance R_{ID} test circuit

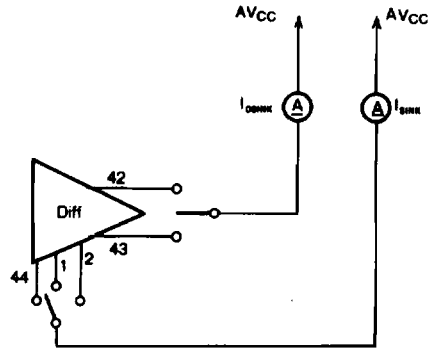


Figure 14 Differentiator constant, pin current & output sink current test circuit

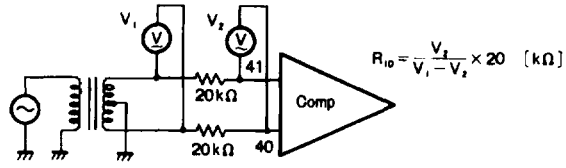


Figure 15 Comparator: Diff input resistance (R_{ID}) test circuit

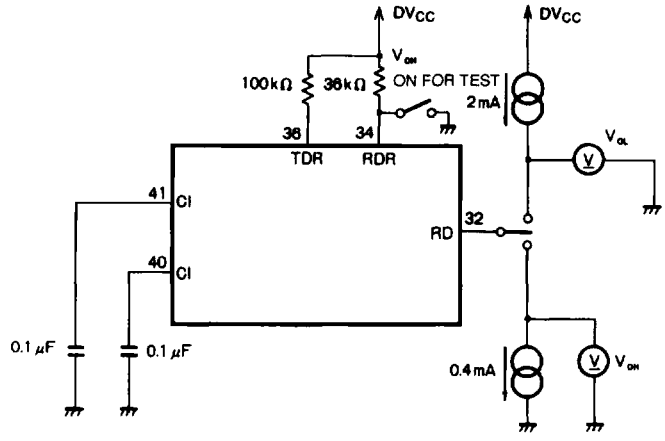


Figure 16 Comparator time domain filter: V_{OH}, V_{OL} test circuit

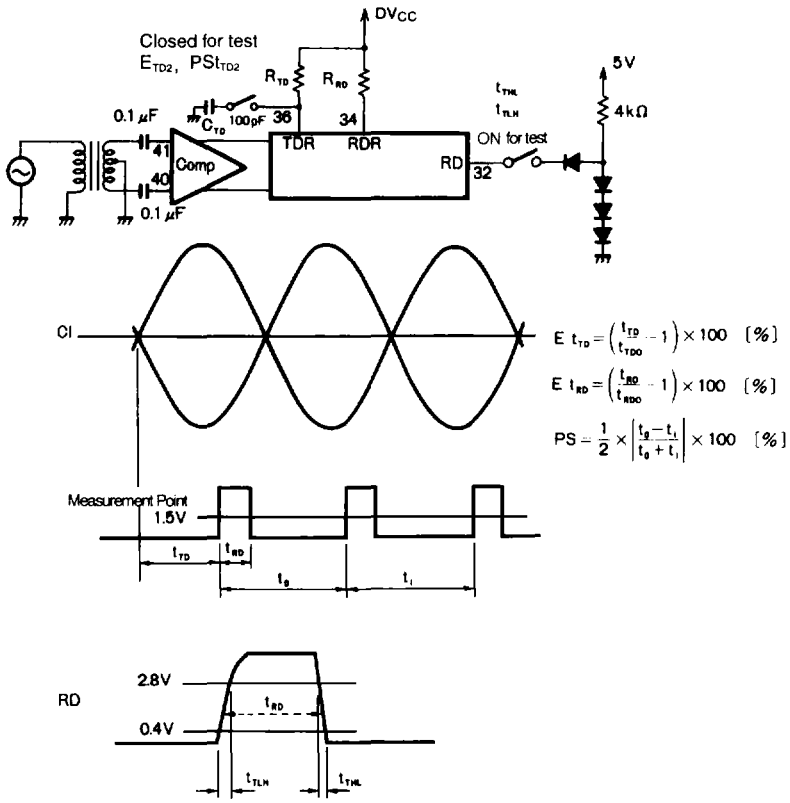
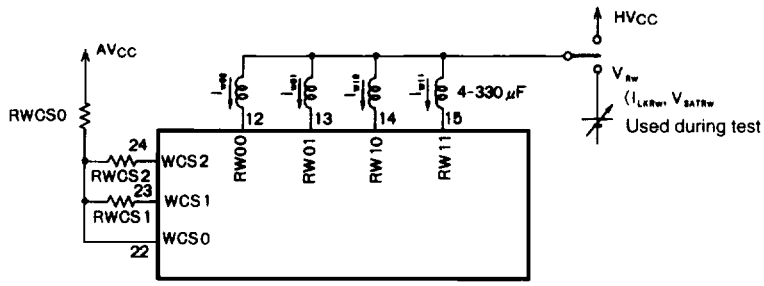


Figure 17 Comparator time domain filter: V_{INmax}, t_{TD}, E_{TD}, t_{RD}, E_{RD}, and PS test circuit



Write current equation

$$I_{WR} = \begin{vmatrix} I_{W00} - I_{W01} \end{vmatrix} \quad (SI = H)$$
$$\begin{vmatrix} I_{W10} - I_{W11} \end{vmatrix} \quad (SI = L)$$

Equation for setting write current

$$I_{WRO} = \frac{1.22\,V}{RWCSO} \times 9.6$$

Equations for setting write correction current

$$I_{WC1O} = \frac{1.22V - V_{WCS}}{RWCS_1} \times 9.6$$

$$I_{WC2O} = \frac{1.22V - V_{WCS_2}}{RWCS2} \times 9.6$$

$$ACI_W = \frac{I_{WR} - 6(mA)}{6(mA)} \times 100 \qquad R_{WCS0} = 1.91k\Omega$$

$$\Delta I_{WR} = \frac{2 \begin{vmatrix} I_{W_{00}} - I_{W_{01}} \end{vmatrix}}{\begin{vmatrix} I_{W_{00}} + I_{W_{01}} \end{vmatrix}} \times 100$$

$$= \frac{2 \begin{vmatrix} I_{W_{10}} - I_{W_{11}} \end{vmatrix}}{\begin{vmatrix} I_{W_{10}} + I_{W_{11}} \end{vmatrix}} \times 100$$

$$PSIW = \frac{2 \begin{vmatrix} I_{WH} - I_{WL} \end{vmatrix}}{\begin{vmatrix} I_{WH} + I_{WL} \end{vmatrix}} \times \frac{1}{1.6}$$

V_{WCS1} : Voltage between AV_{CC} – WCS1 controlled by (LC)

V_{WCS2} : Voltage between AV_{CC} – WCS2 controlled by (HD)

I_{WH} : Write current at AV_{CC}=6.0V

I_{WL} : Write current at AV_{CC}=4.4V

Definition of selected side offset current:
Currents other than the write current flowing equally in the RW pins of the selected side (for activating write-terminate circuits.)

Figure 18 Write circuit: I_{WR}, ACI_W, ΔI_{WR}, V_{SATRW}, I_{LKRW}, I_{WC}, L_{RWOFF} test circuit

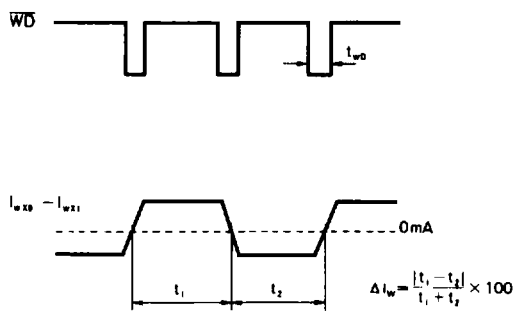
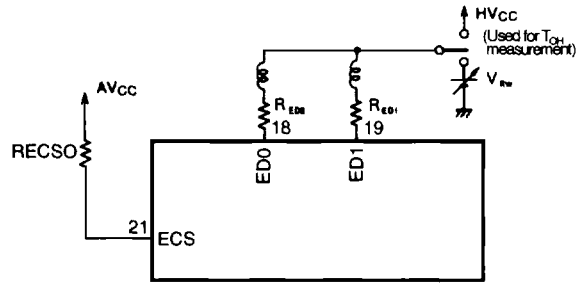
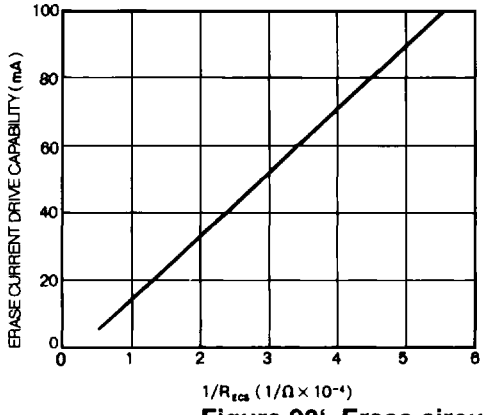


Figure 19 Write circuit: ΔI_W, t_{WD} waveforms





Erase current I_{ER}: 5 ~ 100 mA
To provide drive capability in excess of the set erase current, use graph to determine value of R_{ECS}
The erase current is determined as follows:

$$I_{ER} \approx \frac{V_{CC} - (V_{SATER} + V_{EHEAD})}{R_{ED}}$$

where:
V_{EHEAD} = voltage drop across erase head

$R_{ED} = R_{ED0}$ (when E_{O0} is selected)

$R_{ED} = R_{ED1}$ (when E_{O1} is selected)

Figure 20' Erase circuit: I_{ER}, I_{OH}, V_{SATER} test circuit

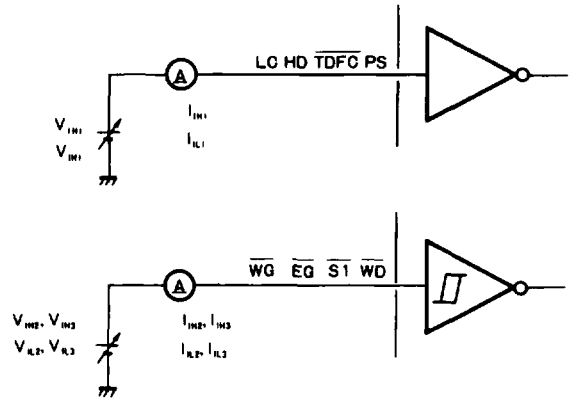


Figure 21 Control logic: V_{IH}, V_{IL}, V_H, I_{IH}, & I_{IL} test circuit