Scenic/MX2

MPEG-1 Audio/Video Decoder

Preliminary

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S3 Incorporated
2770 San Tomas Expressway
Santa Clara, CA 95051-0968

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

When k is used, it refers to the decimal form. For example, 1 kbit means 1000 bits.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department, 2770 San Tomas Expressway, Santa Clara, CA 95051-0968.

Telephone: 408-980-5400, Fax: 408-980-5444

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Section 1: Introduction

The Scenic/MX2™ MPEG-1 audio/video decoder (hereinafter referred to as the Scenic/MX2) is optimized for the PC platform. It can be used in conjunction with any S3® graphics accelerator that provides color space conversion and the S3 Scenic Highway™ interface (such as the Trio64V+™). The other video features supported by these graphics accelerators, including video scaling, can be used to enhance the display of the MPEG-1 video decompressed by the Scenic/MX2.

1.1 GENERAL CAPABILITIES

Scenic/MX2 integrates into a single device the following functions:

- MPEG-1 30 frames/second video decoding
- MPEG-1 CD-quality audio decoding
- A timer to facilitate synchronization of decoded audio and video
- A serial output port for direct connection of a low cost stereo audio D/A converter
- A Scenic Highway interface to enable the host (via the S3 graphics/video accelerator) to access Scenic/MX2 registers and private memory and to burst write compressed audio and video data to the Scenic/MX2. The Scenic/MX2 uses the Scenic Highway to transmit decompressed video to the S3 graphics/video accelerator's frame buffer for display in synchronization with the decompressed audio

Scenic/MX2 works in tandem with the host CPU and graphics accelerator to decode and display MPEG-1 video and audio:

- The host CPU is responsible for demultiplexing the MPEG-1 system stream into separate compressed video and audio data streams and for preprocessing the compressed audio data.
- The Scenic/MX2 is responsible for decompressing the MPEG-1 video stream into a sequence of YUV video images and for decompressing the preprocessed audio stream into 16-bit stereo audio samples for playback. Scenic/MX2's on-chip timer enables the software driver to control the synchronization of audio and video during playback.
- The graphics accelerator is responsible for receiving the sequence of decompressed video images over the Scenic Highway, converting the YUV images into RGB format for display on a computer monitor, and for any additional video processing (video scaling and overlay, video effects, etc.).

1.2 PRODUCT FEATURES

Scenic/MX2's main features are listed below by functional area:

1.2.1 General Features

- MPEG-1 video and audio decompression (30 frames per second)
- Simultaneous video decompression and audio decompression
- Complete audio and video synchronization support

1.2.2 Video Features

- Decompression of "Constrained Parameter" MPEG-1 bit streams
- MPEG-1 video slow playback, fast search, fast forward, freeze frame, audio mute, single step, and random access
- MPEG-1 video error detection and resynchronization
- 4:2:2 video data format output

1.2.3 Audio Features

- Decompression of any MPEG-1 level 1 or 2 compressed audio bit stream
  - 32, 44.1 and 48 KHz sampling rates
  - 32 to 448 kbit/sec compressed bit rates
  - Single-channel, dual-channel, stereo, and joint-stereo stream decompression
- Decompressed audio is transmitted to an external stereo audio D/A converter through a serial audio port
- Audio mute and de-emphasis supported

1.2.4 System Interface

Scenic/MX2 has four main functional interfaces:

- 8-bit Scenic Highway interface to an S3 graphics/video accelerator
- 16-bit page mode DRAM interface
- Serial audio interface to an audio DAC
- Digitized Video Port (DVP) Interface for NTSC/PAL input

1.2.5 Packaging

Scenic/MX2 is available in a 128-pin plastic quad flat pack (PQFP) package.

1.3 SOFTWARE SUPPORT

S3 will provide software drivers which allow Scenic/MX2, in conjunction with the appropriate graphics accelerator, to decode MPEG-1 compressed video and/or games conforming to the following standards and APIs:

- CD- I movies ("Green Book")
- Video CD movies ("White Book")
- Microsoft Windows® 3.1 and Windows® 95 MCI MPEG API
- Open MPEG (OM/1) DOS API

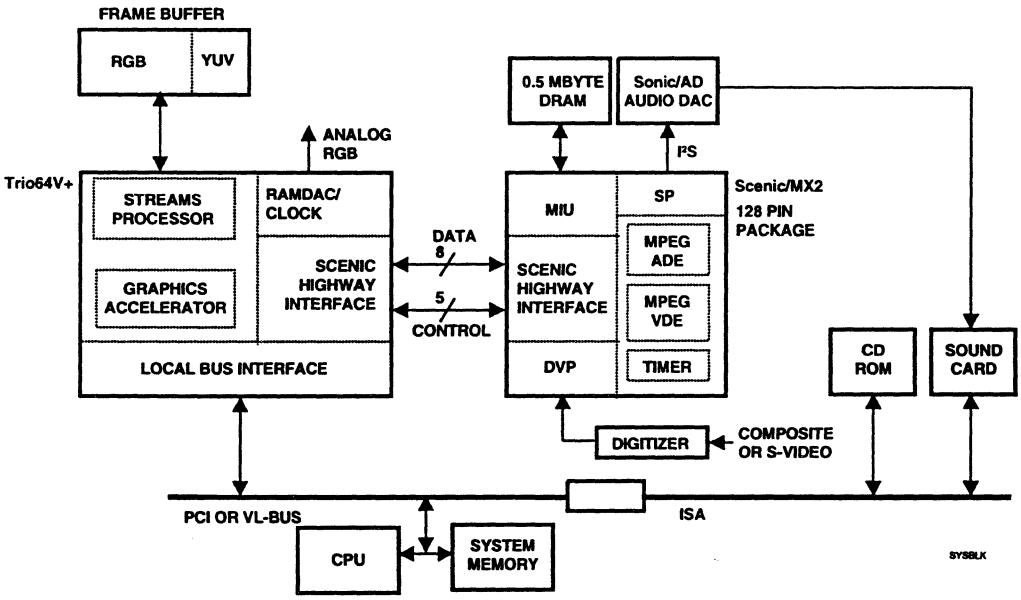

Figure 1-1. System Architecture

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Typ	Unit
Thermal Resistance Θ_{JC}	TBD	°C/W
Thermal Resistance Θ_{JA} (Still Air)	24.0	°C/W
Power Dissipation	2.25	W

2.2 MECHANICAL DIMENSIONS

The Scenic/MX2 comes in a 128-pin PQFP package. The mechanical dimensions are given in Figure 2-1.

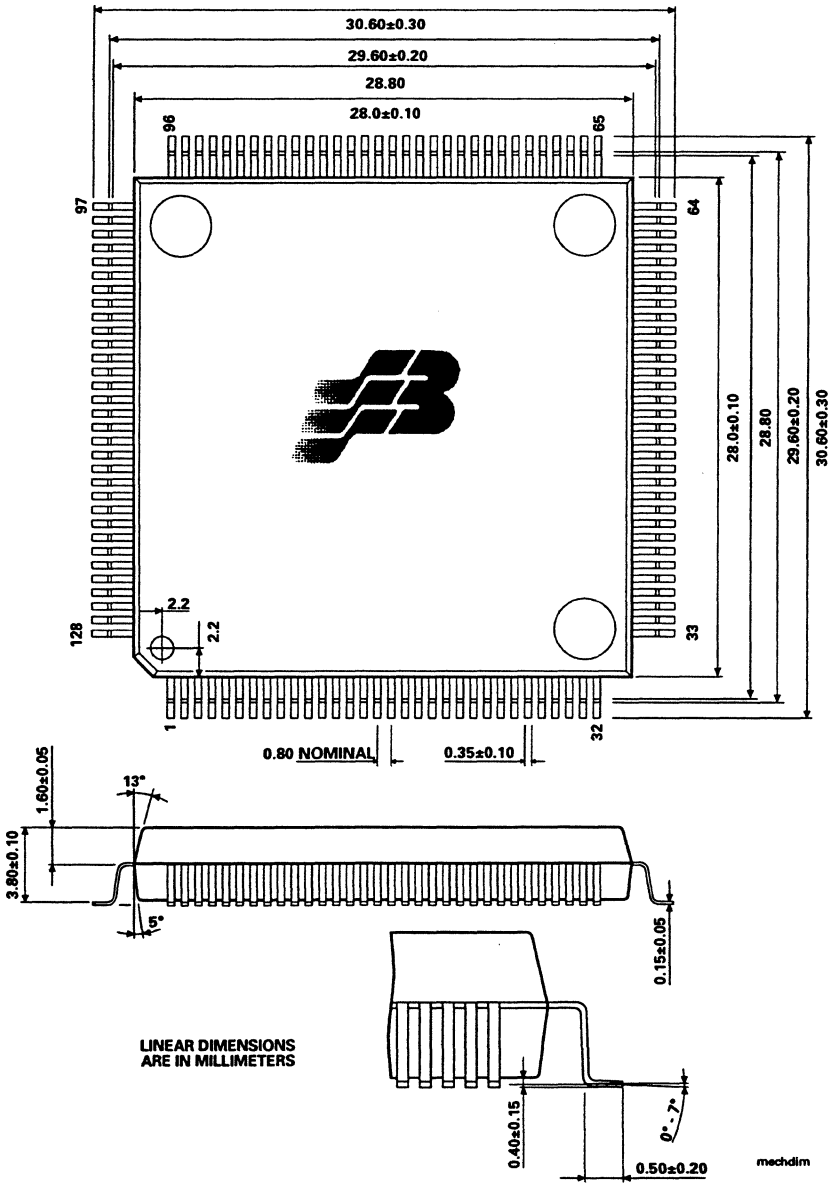

Figure 2-1. 128-pin PQFP Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

The Scenic/MX2 comes in a 128-pin PQFP package. The pinout is shown in Figure 3-1. An active low pin is indicated by an overbar.

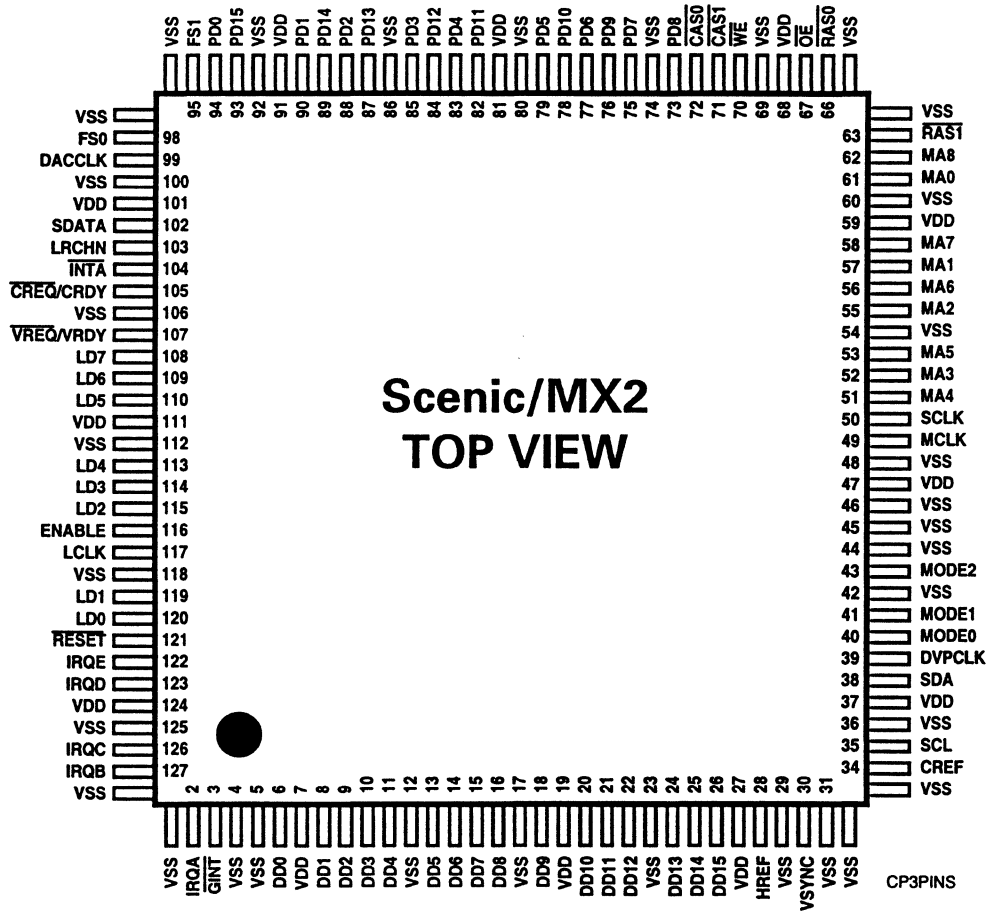

Figure 3-1. Pinout

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each Scenic/MX2 pin. The following definitions are used in these descriptions:

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Scenic/MX2 Pin Descriptions

Symbol	Type	Pin Number(s)	Description
PCI BUS INTERFACE			
$\overline{\text{INTA}}$	O	104	PCI Interrupt Output. This signal is asserted whenever an internal interrupt is generated and bit 11 of R0000 is set to 1 or when the $\overline{\text{GINT}}$ input is asserted and bit 12 of R0000 is set to 1.
$\overline{\text{GINT}}$	I	3	PCI Interrupt Input. When this signal is asserted, INTA is asserted if bit 12 of R0000 is set to 1. This allows Scenic/MX2 to source one PCI interrupt output for a board with two chips.
ISA BUS INTERFACE			
$\overline{\text{RESET}}$	I	121	System Reset. Asserting this signal forces the Scenic/MX2 registers and state machines to a known state.
IRQ[E:A]	O	122, 123, 126, 127, 2	ISA Interrupts. Bits 15-13 of R0000 determine which of these signals is asserted upon generation of an internal interrupt.
Scenic Highway INTERFACE			
LD[7:0]	B	108-110, 113-115, 119, 120	Scenic Highway Bus Data. These signals also carry address data for single register/memory reads and writes.
LCLK	O	117	LPB Clock. LCLK controls transactions on the LPB.
$\overline{\text{CREQ}}$/CRDY	O	105	Scenic/MX2 Request/Ready. When sending data: low = requesting to send high = not requesting to send When receiving data: low = not ready to receive high = ready to receive
$\overline{\text{VREQ}}$/VRDY	I	107	S3 Video Processor Request/Ready. When sending data: low = requesting to send high = not requesting to send When receiving data: low = not ready to receive high = ready to receive
ENABLE	I	116	Scenic/MX2 Enable. Asserting this input enables Scenic/MX2 operation on the Scenic Highway. When this signal is low, Scenic/MX2 tri-states its LD[7:0] pins.

Table 3-1. Scenic/MX2 Pin Descriptions (Continued)

DIGITIZED VIDEO PORT (DVP) INTERFACE			
DD[15:8]	I	26-24, 22-20, 18, 16	Digitized Video Data [15:8]. In 16-bit data mode (R0500_17 = 0), these are Cb[7:0] and Cr[7:0], with the data expected in that order. These pins are not used in 8-bit data mode.
DD[7:0]	I	15-13, 11-8, 6	Digitized Video Data [7:0]. In 16-bit data mode (R0500_17 = 0), these are the luminance inputs Y[7:0]. In 8-bit data mode, these are multiplexed luminance and difference inputs. If R0500_18 is 0, the input sequence is Cb-Y0-Cr-Y1. If R0500_18 is 1, the input sequence is Y0-Cb-Y1-Cr.
HREF	I	28	Horizontal Reference. HSYNC input from the digitizer.
VSYNC	I	30	VSYNC. Vertical sync input from the digitizer.
CREF	I	34	Clock Reference. In 16-bit data mode (R0500_17 = 0), this input can be used to qualify the clock. See the definition for bit 1 of R0500. This pin is pulled up internally.
DVPCLK	I	39	DVP Clock. 27 MHz input.
PRIVATE MEMORY INTERFACE			
Address and Data			
PD[15:0]	B	93, 89, 87, 84, 82, 78, 76, 73, 75, 77, 79, 83, 85, 88, 90, 94	Private Memory Data Bus.
MA[8:0]	O	62, 58, 56, 53, 51, 52, 55, 57, 61	Private Memory Address Bus.
Memory Control			
MCLK	I	49	Memory Clock. External clock source input; controls data transfer rate between Scenic/MX2 and private memory.
$\overline{\text{RAS[1:0]}}$	O	63, 66	Row Address Strobe.
$\overline{\text{CAS[1:0]}}$	O	71-72	Column Address Strobes.
$\overline{\text{WE}}$	O	70	Write Enable.
$\overline{\text{OE}}$	O	67	Output Enable.
I^2C INTERFACE			
SCL	B	35	I^2C clock.
SDA	B	38	I^2C data.
SERIAL INTERFACE			
SCLK	O	50	Serial Data Clock. Clock input to the audio DAC. Its relationship with LRCHN and DACCLK is specified in R0300_11-9.
SDATA	O	102	Serial Data. Data input to the audio DAC.

Table 3-1. Scenic/MX2 Pin Descriptions (Continued)

LRCHN	O	103	Left/Right Channel Select. Channel indicator for the audio DAC. This is the same as the sampling frequency.
FS[1:0]	O	95, 98	Frequency Select. These outputs are reflections of the values programmed in R0300_3-2. They specify a sampling frequency of 32, 44.1 or 48 KHz. These outputs are decoded externally to allow correct programming of the desired DACCLK frequency.
DACCLK	I	99	DAC Clock. This input is generated by an external clock source and is used by Scenic/MX2 to generate the audio DAC control signals. Its relationship with LRCHN and SCLK is specified in R0300_11-9.
MODE SELECT			
MODE0	I	40	The strapping state of this pin on reset is latched in R0500_16. A value of 0 indicates the DVP is active. A value of 1 indicates the DVP is inactive (no digitizer).
MODE1	I	41	The strapping state of this pin on reset is latched in R0500_17. See Table 5-4 for a description of the options.
MODE2	I	43	The strapping state of this pin on reset is latched in R0500_18. See Table 5-4 for a description of the options.
POWER AND GROUND			
VDD	I	7, 19, 27, 37, 47, 59, 68, 81, 91, 101, 111, 124	Power supply
VSS	I	1, 4, 5, 12, 17, 23, 29, 31, 32, 33, 36, 42, 44-46, 48, 54, 60, 64, 65, 69, 74, 80, 86, 92, 96, 97, 100, 106, 112, 118, 125, 128	Ground

3.3 PIN LISTS

Table 3-2 lists all Scenic/MX2 pins alphabetically. Table 3-3 lists all Scenic/MX2 pins in numerical order.

Table 3-2. Alphabetical Pin Listing

Name	Pins
CAS[1:0]	71-72
CREF	34
CREQ/CRDY	105
DACCLK	99
DD[15:0]	26-24, 22-20, 18, 16, 15-13, 11-8, 6
DVPCLK	39
ENABLE	116
FS[1:0]	95, 98
GINT	3
HREF	28
INTA	104
IRQ[E:A]	122, 123, 126, 127, 2
LCLK	117
LD[7:0]	108-110, 113-115, 119, 120
LRCHN	103
MA[8:0]	62, 58, 56, 53, 51, 52, 55, 57, 61
MCLK	49
MODE[2:0]	43, 41, 40
OE	67
PD[15:0]	93, 89, 87, 84, 82, 78, 76, 73, 75, 77, 79, 83, 85, 88, 90, 94
RAS[1:0]	63, 66
RESET	121
SCL	35
SCLK	50
SDA	38
SDATA	102
VDD	7, 19, 27, 37, 47, 59, 68, 81, 91, 101, 111, 124
VREQ/VRDY	107
VSS	1, 4, 5, 12, 17, 23, 29, 31, 32, 33, 36, 42, 44-46, 48, 54, 60, 64, 65, 69, 74, 80, 86, 92, 96, 97, 100, 106, 112, 118, 125, 128
VSYNC	30
WE	70

Table 3-3. Numerical Pin Listing

Pin #	Name
1	**VSS**
2	IRQA
3	$\overline{\text{GINT}}$
4	**VSS**
5	**VSS**
6	DD0
7	**VDD**
8	DD1
9	DD2
10	DD3
11	DD4
12	**VSS**
13	DD5
14	DD6
15	DD7
16	DD8
17	**VSS**
18	DD9
19	**VDD**
20	DD10
21	DD11
22	DD12
23	**VSS**
24	DD13
25	DD14
26	DD15
27	**VDD**
28	HREF
29	**VSS**
30	VSYNC
31	**VSS**
32	**VSS**
33	**VSS**
34	CREF
35	SCL
36	**VSS**
37	**VDD**
38	SDA
39	DVPCLK
40	MODE0

Pin #	Name
41	MODE1
42	**VSS**
43	MODE2
44	**VSS**
45	**VSS**
46	**VSS**
47	**VDD**
48	**VSS**
49	MCLK
50	SCLK
51	MA4
52	MA3
53	MA5
54	**VSS**
55	MA2
56	MA6
57	MA1
58	MA7
59	**VDD**
60	**VSS**
61	MA0
62	MA8
63	$\overline{\text{RAS1}}$
64	**VSS**
65	**VSS**
66	$\overline{\text{RAS0}}$
67	$\overline{\text{OE}}$
68	**VDD**
69	**VSS**
70	$\overline{\text{WE}}$
71	$\overline{\text{CAS1}}$
72	$\overline{\text{CAS0}}$
73	PD8
74	**VSS**
75	PD7
76	PD9
77	PD6
78	PD10
79	PD5
80	**VSS**

Table 3-3. Numerical Pin Listing (Continued)

Pin #	Name
81	**VDD**
82	PD11
83	PD4
84	PD12
85	PD3
86	**VSS**
87	PD13
88	PD2
89	PD14
90	PD1
91	**VDD**
92	**VSS**
93	PD15
94	PD0
95	FS1
96	**VSS**
97	**VSS**
98	FS0
99	DACCLK
100	**VSS**
101	**VDD**
102	SDATA
103	LRCHN
104	$\overline{\text{INTA}}$
105	$\overline{\text{CREQ}}$/CRDY
106	**VSS**
107	$\overline{\text{VREQ}}$/VRDY
108	LD7
109	LD6
110	LD5
111	**VDD**
112	**VSS**
113	LD4
114	LD3
115	LD2
116	ENABLE
117	LCLK
118	**VSS**
119	LD1

Pin #	Name
120	LD0
121	$\overline{\text{RESET}}$
122	IRQE
123	IRQD
124	**VDD**
125	**VSS**
126	IRQC
127	IRQB
128	**VSS**

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Table 4-2. DC Specifications (VDD = 5V ± 5%, operating temperature 0° C to 70° C)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	2.4		V
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		TBD	pF
C_{OUT}	Output Capacitance		TBD	pF
I_{CC}	Power Supply Current		TBD	mA

4.3 AC SPECIFICATIONS

TBD

Section 5: Reset and Initialization

The $\overline{\text{RESET}}$ signal resets Scenic/MX2's internal state machines and places all registers in their power-on default states. It also initiates several configuration actions, as described in this section.

5.1 CONFIGURATION STRAPPING

Certain Scenic/MX2 configuration information, as detailed in this section, is set by hardware strapping. The PD[15:0] pins can be individually pulled high or low through a 47 KΩ resistor. These pull-ups and pull-downs do not affect normal operation of the pins as part of the private memory data bus, but force the pins to a defined state during reset. The Scenic/MX2 samples this state at the rising edge of the reset signal and loads the data into register bits as noted in Table 5-1 and Section 10.

Table 5-1. Definition of PD[15:0] at the Rising Edge of the Reset Signal

Register Number	Bit(s)	PD Pins	Value	Function
		15		Reserved for future use
	SCLK Inverted			
R0300	22	14	0	Data latched on rising edge of SCLK
			1	Data latched on falling edge of SCLK
	Audio DAC Absent			
R0300	21	13	0	Audio DAC present
			1	Audio DAC absent
	Audio Data Bit Order			
R0300	20	12	0	Audio data bit 0 first
			1	Audio data bit 15 first
	Lag Time			
R0300	19	11	0	First 16 bits latched on an LRCHN phase
			1	Last 16 bits latched on an LRCHN phase

Table 5-1. Definition of PD[15:0] at the Rising Edge of the Reset Signal (Continued)

Register Number	Bit(s)	PD Pins	Value	Function
	SCLK and LRCHN Definition			
R0300	14 - 12	[10:8]	000	256 DAC clocks per LRCHN, 2 DAC clocks per SCLK
			001	256 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			010	384 DAC clocks per LRCHN, 2 DAC clocks per SCLK
			011	384 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			100	384DAC clocks per LRCHN, 6 DAC clocks per SCLK
			101	384 DAC clocks per LRCHN, 8 DAC clocks per SCLK
			110	512 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			111	512 DAC clocks per LRCHN, 8 DAC clocks per SCLK
	LRCHN Channel Interpretation			
R0300	11	7	0	LRCHN active high left channel
			1	LRCHN active high right channel
	$\overline{\text{RAS}}$ Length Select			
R0230	6	6	See Tables 5-2 and 5-3	This bit together with bits 5-4 sets $\overline{\text{RAS}}$ Precharge value - see Table 5-2 for details. Also, this bit together with bits 3-2 set $\overline{\text{RAS}}$ Pulse width - see Table 5-3.
	$\overline{\text{RAS}}$ Precharge			
R0230	5 - 4	[5:4]	See Table 5-2	These bits together with bit 6 set the $\overline{\text{RAS}}$ Precharge Length
	$\overline{\text{RAS}}$ Pulse Width			
R0230	3 - 2	[3:2]	See Table 5-3	These bits together with bit 6 set the $\overline{\text{RAS}}$ Pulse Width
	$\overline{\text{CAS}}$/$\overline{\text{OE}}$/$\overline{\text{WE}}$ Stretch			
R0230	1 - 0	[1:0]	00	6.5 ns (nominal)
			01	5.0 ns (nominal)
			10	3.5 ns (nominal)
			11	0 ns - no stretch

Table 5-2. Setting $\overline{RAS}$ Precharge Length

R0230 bits 5-4 (default is the value strapped on PD[5:4])	R0230 bit 6 value: $\overline{RAS}$ Length Select	Resulting $\overline{RAS}$ Precharge length used
00	0	4 MCLKs
00	1	4.5 MCLKs
01	0	3 MCLKs
01	1	3.5 MCLKs
10	0	2 MCLKs
10	1	2.5 MCLKs
11	0	reserved
11	1	reserved

Table 5-3. Setting $\overline{RAS}$ Pulse Width

R0230 bits 3-2 value (default is the value strapped on PD[3:2])	R0230 bit 6 value: $\overline{RAS}$ Length Select	Resulting $\overline{RAS}$ Pulse Width used
00	0	7 MCLKs
00	1	6.5 MCLKs
01	0	6 MCLKs
01	1	5.5 MCLKs
10	0	5 MCLKs
10	1	4.5 MCLKs
11	0	4 MCLKs
11	1	3.5 MCLKs

The MODE[2:0] strapping is shown in Table 5-4.

Table 5-4. Definition of MODE[2:0] at the Rising Edge of the Reset Signal

Register Number	Bit(s)	MODE Pin	Value	Function
	DVP Mode Definition			
R0500	16	0	0	DVP active (LCLK = DVPCLK)
			1	DVP inactive (no digitizer)
	17	1	0	If bit 16 = 0, 16-bit data mode If bit 16 = 1 and bit 18 = 1, LCLK = 1/2 MCLK
			1	If bit 16 = 0, 8-bit data mode If bit 16 = 1 and bit 18 = 1, LCLK = 2/3 MCLK
	18	2	0	If bit 16 = 0 and bit 17 = 1, data input sequence is Cb-Y0-Cr-Y1 If bit 16 = 1, LCLK = DVPCLK
			1	If bit 16 = 0 and bit 17 = 1, data input sequence is Y0-Cb-Y1-Cr If bit 16 = 1, LCLK determined by MODE1 (bit 17) setting

5.2 RESET BEHAVIOR

5.2.1 Hardware Reset

Hardware reset occurs when the $\overline{\text{RESET}}$ signal is asserted. Upon a hardware reset, these actions occur:

- All Scenic/MX2 internal operations are halted and the chip modules having powerdown or idle states enter those states
- All internal control and configuration registers assume their default values as specified in Section 9
- The memory control pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$ go high and the strappings on the PD and MODE pins are read
- The SP module stops driving the audio DAC

5.2.2 Soft Reset

Soft reset occurs when software sets bit 16 of the R0034 register to 1. A soft reset has the same consequences as a hard reset.

Section 6: Hardware Interfaces

Scenic/MX2 has four main interfaces:

- S3 Scenic Highway
- Local memory
- Audio DAC
- Video digitizer

This section describes the interfaces, their functional characteristics, and related information.

6.1 Scenic Highway INTERFACE

The hardware interface for the Scenic Highway is shown in Figure 6-1 for the S3 Trio64V+integrated graphics/video accelerator. The following protocols and functional timings will also reference this chip. The interface, protocols and timings will be the same for any S3 chip containing the Scenic Highway function as part of its Local Peripheral Bus (LPB) capability. This interface is fully bi-directional. Scenic/MX2 registers and private memory can be accessed, compressed audio and video data received and decompressed video data sent to the S3 graphics/video accelerator.

If a digitizer is present, the 27 MHz clock from that device (DVPCLK) will be used to clock the LPB. If no digitizer is present, the MODE2 pin can be strapped high. On reset, this value is latched in R0500_18 and causes the Scenic Highway to be clocked at 1/2 or 2/3 the MCLK rate, depending on the strapping of the MODE1 pin. If the MODE2 pin is strapped low, Scenic/MX2 expects an external LCLK source attached to the DVPCLK pin.

6.1.1 Scenic/MX2 Register/Memory Access

To read/write a Scenic/MX2 register or private memory location (other than to transfer com-

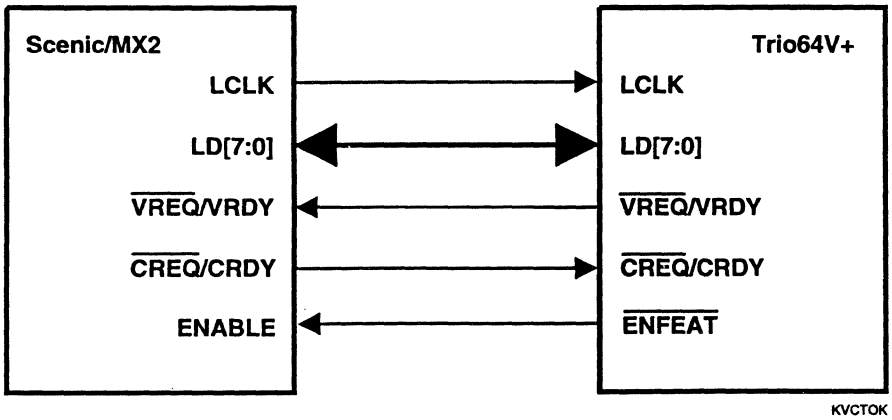

Figure 6-1. Scenic Highway Interface

pressed data), the LPB Direct Read/Write Address register in the Trio64V+ (offset FF14) is written. The new register/memory data is then read from or written to the LPB Direct Read/Write Data register (offset FF18).

For a write access, the data register write triggers the sequence shown in Figure 6-2 if the Scenic/MX2 is ready to receive the data ($\overline{\text{CREQ}}$/CRDY remains high). One cycle after the Trio64V+ asserts its $\overline{\text{VREQ}}$/VRDY signal, it sends the address in three byte writes. The first byte is composed of bits 23-16 of the address register. The three upper bits are 000b to define this as a write. Bit 4 is 1 for a register access and 0 for a memory access. Bits 3-0 are bits 19-16 of the address. The second byte is bits 15-8 of the address register and the third byte is bits 7-0. The different interpretations of bits 19-0 for memory and register accesses are explained in Section 9-1. The data immediately follows the address information in four byte writes. Data is written in the opposite byte order to that for the address, i.e., least significant byte (bits 7-0) first and most significant byte (bits 31-24) last. The Trio64V+ then deasserts $\overline{\text{VREQ}}$/VRDY. The Host repeats the above sequence for another write if required.

If the Scenic/MX2 is not ready to receive data, it drives its $\overline{\text{CREQ}}$/CRDY signal low during the A0-0 byte (LSB) of the address phase. The Trio64V+ then delays sending the data until the Scenic/MX2 raises $\overline{\text{CREQ}}$/CRDY. This is depicted in Figure 6-3.

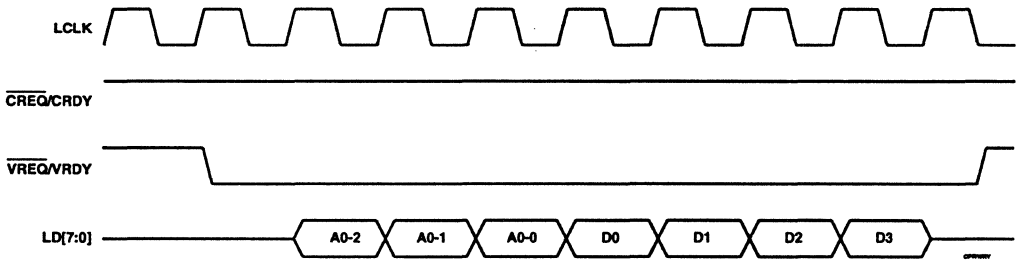

Figure 6-2. Register/Memory Write (Scenic/MX2 Ready)

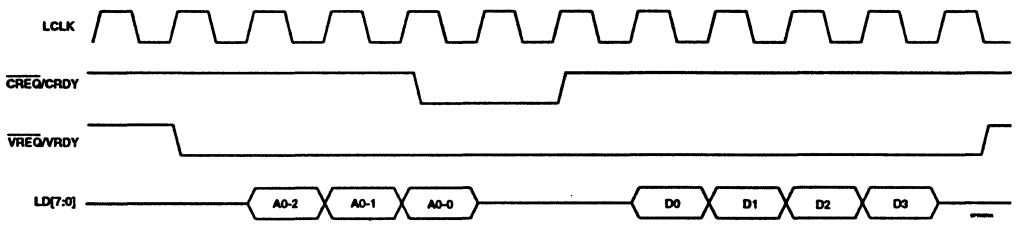

Figure 6-3. Register/Memory Write (Not Ready)

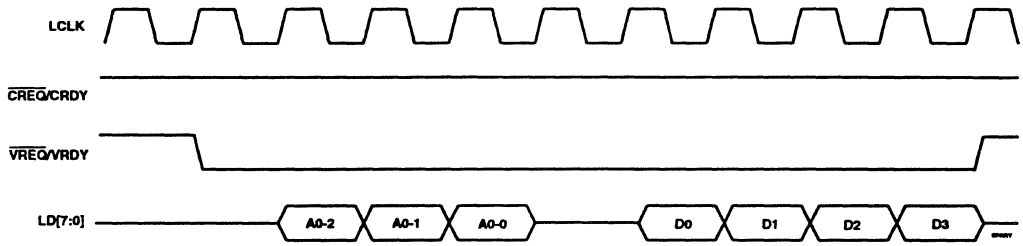

Figure 6-4. Register/Memory Read (Scenic/MX2 Ready)

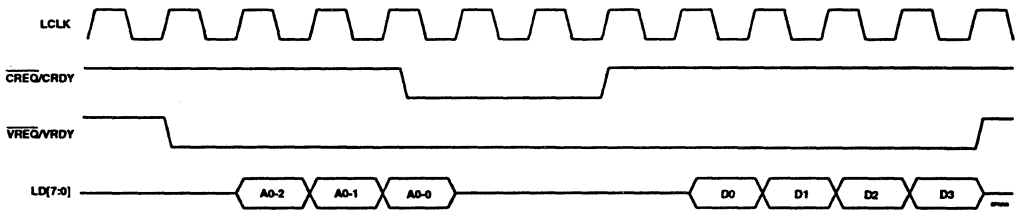

Figure 6-5. Register/Memory Read (Not Ready)

Figure 6-4 shows a Scenic/MX2 register/memory read when the Scenic/MX2 is ready to provide data. This is indicated by the Scenic/MX2 holding the CREQ/CRDY high throughout the cycle. The three upper bits of the first address byte are 001 to define a read.

If the Scenic/MX2 is not ready to provide data, it drives its CREQ/CRDY signal low during the address phase. The Trio64V+ then waits until the Scenic/MX2 raises CREQ/CRDY and provides register data. This is depicted in Figure 6-5.

If CREQ/CRDY and VREQ/VRDY are both driven low on the same cycle (request contention), CREQ/CRDY (the Scenic/MX2) wins.

6.1.2 Scenic/MX2 Burst Writes

The Trio64V+ has an output FIFO for handling the transfer of compressed video data from the Host to the Scenic/MX2. The Host must first check the number of empty slots (FF04_3-0), then send no more than this many doublewords (32 bits) of compressed data to the FIFO. A sixteen doubleword address range (FF40H - FF5CH) is provided for this FIFO. Writes to any of these addresses are directed to the FIFO.

FF00_17-16 are programmed to specify the number of doublewords of data to burst to the Scenic/MX2. R0020_7-6 in the Scenic/MX2 must also be programmed with a value equal to or larger than the value programmed in the Trio64V+. If

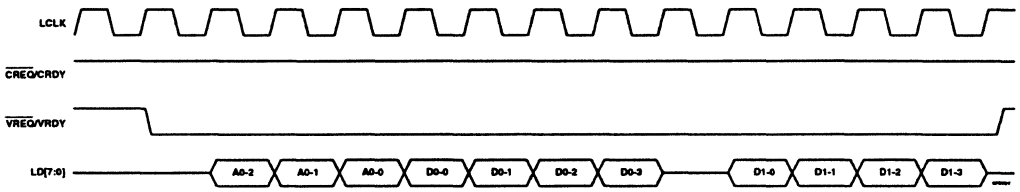

Figure 6-6. Burst Write (Scenic/MX2 Ready)

FF00_17-16 are programmed to 11b (8 doublewords), then R0020_0 should be programmed to 0 to override R0020_7-6 and allow the 8 doubleword burst.

A write to the output FIFO then initiates a compressed data burst write to the Scenic/MX2. This is depicted in Figure 6-6 for a burst count of 2 (FF00_17-16 = 01b) for the case where the Scenic/MX2 is ready to receive the data. The address and first doubleword are transferred exactly as for a register write. Following doublewords in the burst are each separated by one dead cycle. The address has no meaning except for the upper three bits, which are forced to 110b by hardware to specify a compressed data transfer.

A compressed data transfer when the Scenic/MX2 is not ready to receive data is almost the same as a register write for the same circumstances (see Figure 6-3). The only difference is that after the Scenic/MX2 returns its CRDY signal, additional doubleword packets may be burst to the Scenic/MX2 as shown in Figure 6-6.

6.1.3 Scenic/MX2 Video Output

The Trio64V+ signals its readiness to accept data by driving $\overline{\text{VREQ}}$/VRDY high. This is done automatically when the Trio64V+ does not need to drive this signal low such as to initiate a register access or to indicate an LPB video FIFO full state. The Scenic/MX2 responds by sending a VSYNC ($\overline{\text{CREQ}}$/CRDY low for one cycle) possibly followed by an HSYNC ($\overline{\text{CREQ}}$/CRDY low for two cycles). This is shown in Figure 6-7. As indicated in the figure, the time between VSYNC and HSYNC is variable. HSYNC can occur before or after a line, as selected by R0020_10.

After the VSYNC/HSYNC sequence, the Scenic/MX2 can pull $\overline{\text{CREQ}}$/CRDY low at any time and begin sending data three clocks later. This is

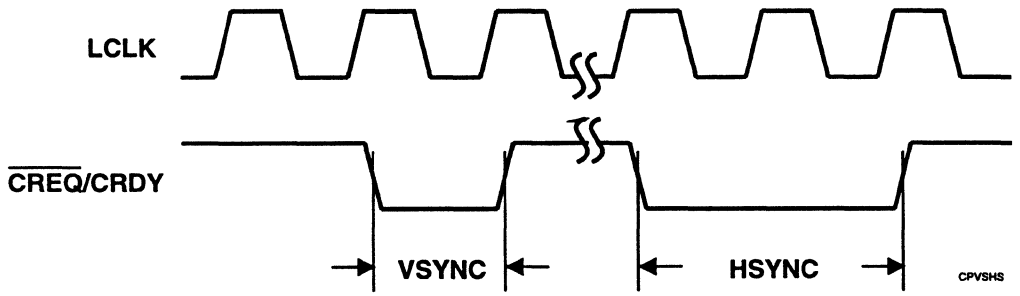

Figure 6-7. VSYNC and HSYNC Protocols

shown in Figure 6-8. The Trio64V+ assumes data has begun any time CREQ/CRDY is held low for more than two cycles. When the Scenic/MX2 is sending the last byte, it drives CREQ/CRDY high. The Scenic/MX2 always sends data in 4-byte packets.

Figure 6-8 shows what happens when the Trio64V+ is ready to receive all the data. If the Trio64V+ cannot accept more data, such as when its LPB video FIFO is full, it drives its VREQ/VRDY signal low during the first byte phase of a 4-byte packet. All bytes starting with this one are rejected by the Trio64V+ and must be resent by the Scenic/MX2 after the Trio64V drives its VREQ/VRDY signal high again. This is depicted in Figure 6-9, where the Dn0 byte, which is the first byte of the nth 4-byte packet, is rejected. When the Trio64V+ can accept more data, it drives VREQ/VRDY high. The Scenic/MX2 drives CREQ/CRDY high (two cycles later) and then drives it low when it is ready to resend the data. The resend of Dn0 and subsequent bytes starts two cycles later.

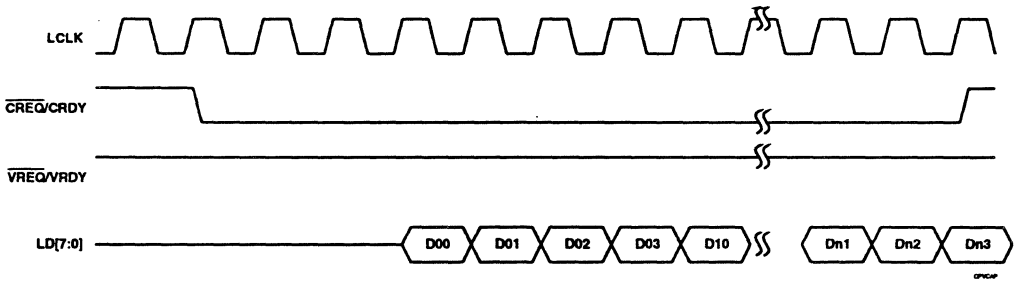

Figure 6-8. Video Output (Trio64V+ Ready)

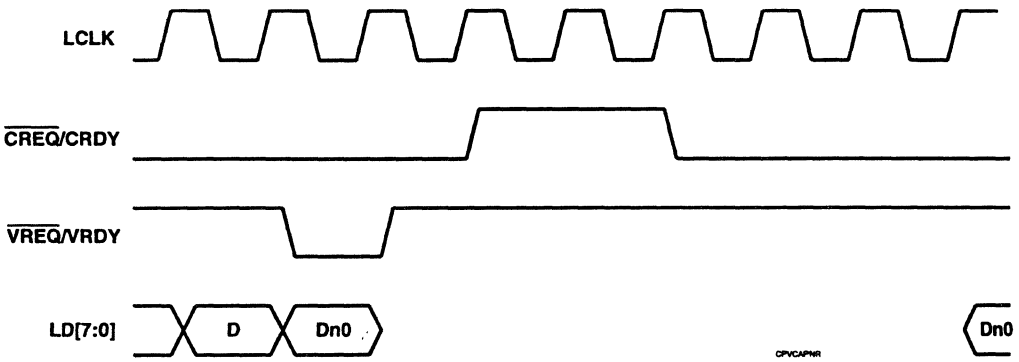

Figure 6-9. Video Output (Trio64V+ Not Ready)

6.2 LOCAL MEMORY INTERFACE

Scenic/MX2 can use either 512 KBytes or 1 MByte of fast page mode 256Kx16 DRAMs. The memory interface operates at the system clock frequency of 40 MHz, allowing use of inexpensive DRAMs. Scenic/MX2 contains all necessary interface and refresh circuitry for these DRAMs.

6.2.1 Memory Configurations

Figure 6-10 shows a 0.5 MByte configuration using a 256Kx16 DRAM. $\overline{RAS0}$ selects the first 512K; when an additional 0.5 MByte is used, $\overline{RAS1}$ selects the second 512K.

In general, 512 KBytes is sufficient for decoding most MPEG-1 data streams. 1 MByte is required for decoding streams such as Green Book encoded PAL video.

6.2.2 Memory Functional Timing

Figure 6-11 shows the functional timing for a fast page mode read cycle, and Figure 6-12 shows fast page mode write cycle timing. These diagrams also show how certain parameters for various control signals can be adjusted to meet the access time requirements of a variety of DRAMs.

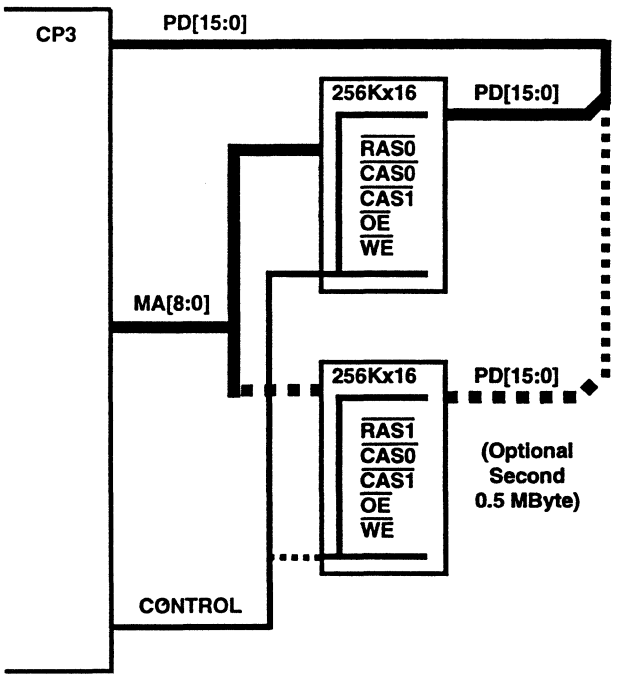

Figure 6-10. 256Kx16 DRAM Configuration

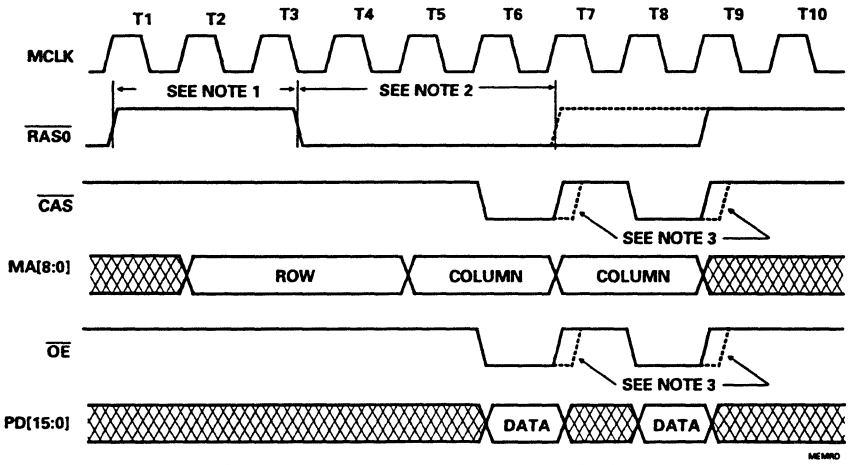

Figure 6-11. Fast Page Mode Read Cycle

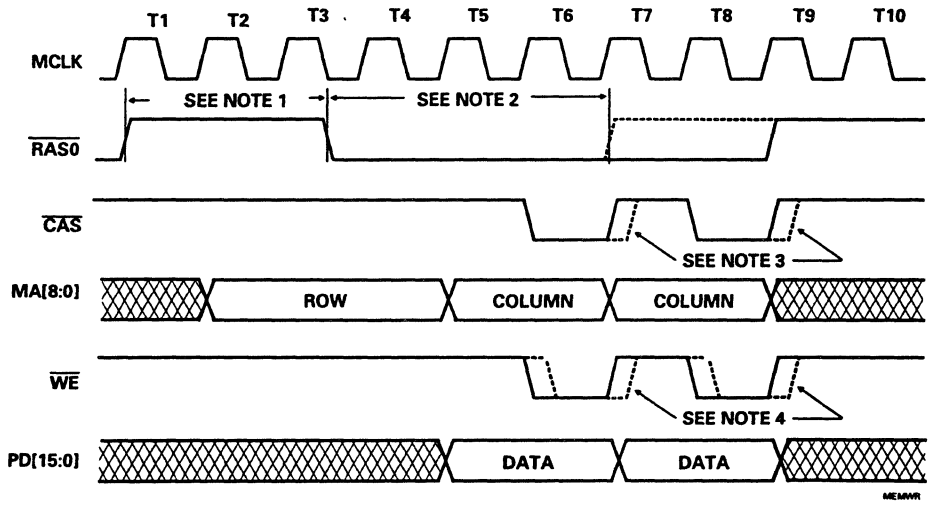

Figure 6-12. Fast Page Mode Write Cycle

Notes

1. The minimum $\overline{RAS}$ Precharge time can be adjusted using register R0230 bits 5-4.
2. The minimum $\overline{RAS}$ Pulse Width can be set using register R0230 bits 3-2.
3. The $\overline{CAS}$ and $\overline{OE}$ low times can be adjusted using register R0230 bits 1-0
4. The $\overline{WE}$ pulse can be delayed using R0230 bit 7.

6.3 SERIAL AUDIO INTERFACE

Scenic/MX2's programmable serial audio interface is designed to interface to a variety of audio DACs with few or no additional parts. When the S3 Sonic/AD™ audio DAC is used, as shown in Figure 6-13, no glue logic is required. A design using the Sonic/AD requires only a clock crystal plus a small number of analog discretes to implement the low-pass filters required on the analog outputs.

Functional timing for the audio DAC interface is shown in Figures 6-14 and 6-15.

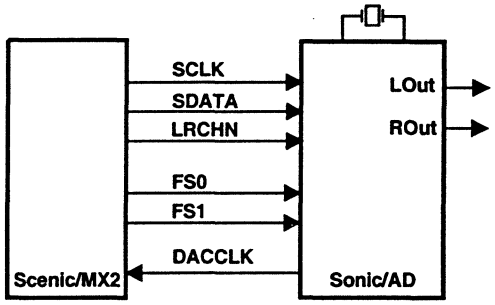

Figure 6-13. Audio DAC Interface

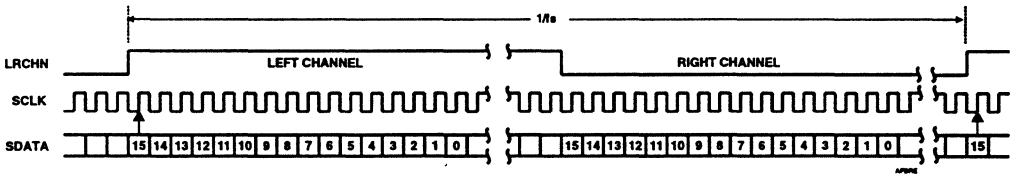

Figure 6-14. First Audio Bits Latched on Rising Edge

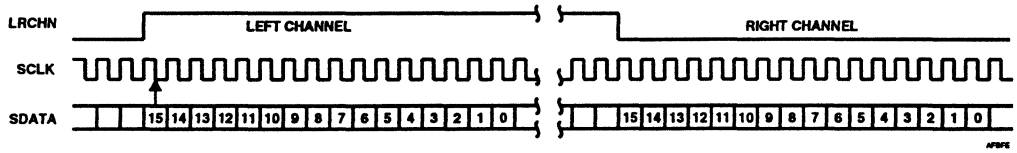

Figure 6-15. First Audio Bits Latched on Falling Edge

6.4 DIGITIZED VIDEO PORT (DVP) INTERFACE

The DVP allows direct, glueless connection of a number of 8- and 16-bit video digitizers. The video data is captured and transferred directly to the S3 graphics/video accelerator via the Scenic Highway. The Scenic/MX2 cannot decode audio or video data or drive its Serial Port while the DVP is in use.

6.4.1 Digitizers Supported

A glueless interface is provided for the ITT 3220 and Philips SAA7111 in both 8- and 16-bit modes. The Philips SAA7110 is also supported gluelessly in 16-bit mode. This interface is depicted in Figure 6-16. The interface is reasonably generic and should allow interfacing of other devices. For 8-bit mode, all data is transmitted on LD[7:0] and LD[15:8] are unused.

6.4.2 DVP Input

The basic DVP mode is set by power-on strapping of the MODE[2:0] pins at power-on reset. This information is latched in R0500_18-16. See Table 5-4 for a complete description of all the strapping options.

DVP operation is enabled by setting R0500_0 to 1. R0500_2-4 allow specification of the polarity of the CREF, HREF and VSYNC inputs respectively. R0500_1 allows use of an internal or external CREF for 16-bit modes.

The functional timing for the digitizer interface will vary according to the type of digitizer used. Scenic/MX2 conforms to the timing requirements of all of its supported digitizers and correct functional timing diagrams can be found in the appropriate digitizer data book.

6.4.3 DVP Output

R0050_5 is programmed to select the sequence for transmitting the video data over the Scenic Highway. R0050_6 defines the timing of generation of a New Frame (VSYNC) sequence on the Scenic Highway. HSYNC sequence generation timing is specified by R0500_7. (These sequences are described in Figure 6-7.)

The functional timing of the transfer of data from Scenic/MX2 to the S3 graphics/video accelerator over the Scenic Highway is the same as for the transfer of decoded MPEG data. This is described in Section 6.1.3. One difference is that if the S3 accelerator is not ready to receive DVP data, video data will be lost as the Scenic/MX2 does not store the digitized video input. This condition does not occur for supported video digitizers.

6.5 INTERRUPT GENERATION

The Scenic/MX2 has both PCI and ISA (VL-Bus systems) interrupt handling capabilities.

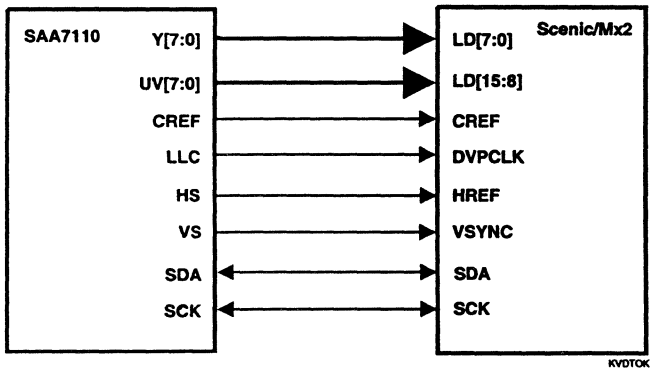

Figure 6-16. Philips SAA7110 Digitizer Interface

6.5.1 PCI Interrupts

The PCI specification requires that only one interrupt be sourced from a single card. Scenic/MX2 provides an interrupt input ($\overline{GINT}$) and output ($\overline{INTA}$) for PCI card designs. If R0000_11 is set to 1, generation of a Scenic/MX2 internal interrupt causes assertion of the $\overline{INTA}$ signal. If R0000_12 is set to 1, assertion by another device of the $\overline{GINT}$ input causes the Scenic/MX2 to assert $\overline{INTA}$. This allows the Scenic/MX2 to be the single interrupt source for two devices.

6.5.2 ISA Interrupts

Five ISA interrupt outputs (IRQ[A:E]) are provided for VL-Bus system designs. R0000_15-13 are programmed to select which of these interrupts (if any) is to be asserted upon generation of an internal Scenic/MX2 interrupt. Only one of the five can be asserted at a time.

Section 7: Functional Description

7.1 OVERVIEW

This section provides a high level description of Scenic/MX2 operation and system data flow.

MPEG is described by the ISO/IEC document IS11172. An MPEG-encoded system stream contains a video stream and one or more audio streams, and optionally may also have private data streams. In a Scenic/MX2 application, the Host acts as a front end preprocessor, separating the video and audio streams, which it then routes to Scenic/MX2. The Host processor provides high level data flow control and sets control parameters for Scenic/MX2.

The primary functions of the Scenic/MX2 are:

- Decoding MPEG1 video and audio streams sent to it via the S3 graphics/video accelerator and the Scenic Highway by a Host processor
- Returning a stream of decompressed video data via the Scenic Highway to the S3 graphics/video processor
- Providing decompressed audio data output to an audio DAC
- Capturing digitized video and transferring this via the Scenic Highway to the S3 graphics/video accelerator

These processes are shown in the context of system data flow in Figure 7-1.

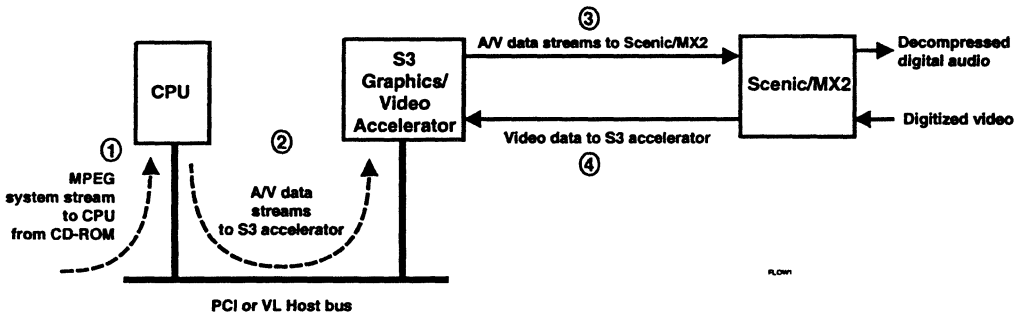

Figure 7-1. System Data Flow

The overall hierarchy of system-level control is shown in Figure 7-2. The application accesses Scenic/MX2 through the application interface level, using Windows- or DOS-compatible calls. These are interpreted by Scenic/MX2 driver software, which commands and controls Scenic/MX2.

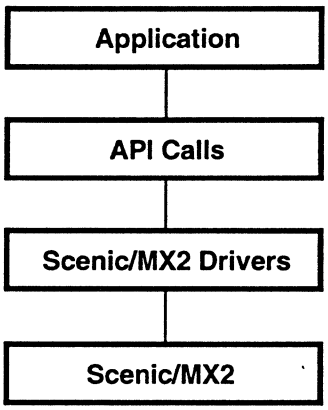

Figure 7-2. Control Hierarchy

7.2 Scenic/MX2 FUNCTIONAL PARTITIONING

Figure 7-3 shows the main functional modules within Scenic/MX2 together with the related external components. The functions of these modules are described in the following sections.

7.3 VIDEO DECOMPRESSION ENGINE (VDE)

The Video Decompression Engine:

- Accepts input streams of MPEG compressed video data
- Outputs decompressed video data

7.4 AUDIO DECOMPRESSION ENGINE (ADE)

The Audio Decoding Engine:

- Accepts input streams of MPEG compressed audio data
- Outputs decompressed audio data

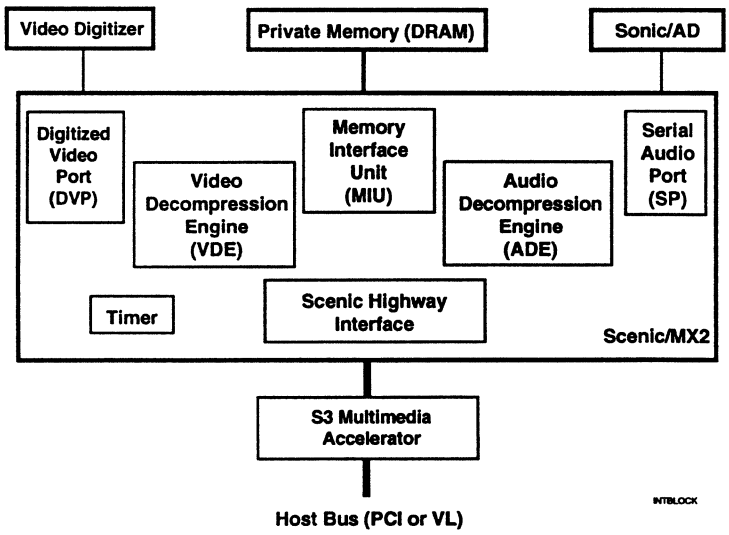

Figure 7-3. Internal Block Diagram

7.5 MEMORY INTERFACE UNIT (MIU)

The Memory Interface Unit:

- Controls buffers in private memory (local DRAM)
- Manages DMA access to/from private memory
- Provides DRAM refresh control
- Performs arbitration of memory access by all Scenic/MX2 functional modules

Scenic/MX2 uses external dedicated DRAM for data buffers. It needs only 0.5 MByte DRAM for data storage when decoding most MPEG-1 bit streams, but has provision for using 1 MByte (2 DRAMs). The memory size supported is 256Kx16.

7.6 Scenic Highway UNIT

- Handles all transactions with the S3 graphics/video accelerator across the Scenic Highway

For a complete description of Scenic Highway functions, see Section 6.1.

7.7 SERIAL AUDIO PORT (SP)

- Provides digital stereo audio interface to an external audio DAC
- Accepts DACCLK timing from the audio DAC
- Compatible with the I^2S standard.

7.8 DIGITIZED VIDEO PORT (DVP)

- Provides an 8- or 16-bit interface with a video digitizer

For a complete description of DVP functions, see Section 6.4.

7.9 TIMER

The on-chip timer enable the software driver to control the synchronization of audio and video during playback.

Section 8: Software Driver

This section provides a description of the functions supported by the driver software for the Scenic/MX2.

The Scenic/MX2 drivers will support two standard MPEG software interfaces: the Microsoft Windows 3.1 and Windows 95 MCI MPEG interface, and the Open MPEG (OM/1) DOS API.

8.1 FUNCTIONS SUPPORTED BY DRIVER SOFTWARE

Low-level Scenic/MX2 functions supported by Scenic/MX2 software driver is:

Close	Closes Scenic/MX2 as a device; mutes the audio output
Get	Returns driver settings
Open	Opens and initializes Scenic/MX2 as a device
Pause	Pauses playing, stops audio and resumes from the stopping point
Seek	Puts output in pause mode, seeks required place in data source
Set	Puts system information into system memory and sets Scenic/MX2 configuration
Step	Multiple types of stepping supported
Freeze	Freezes last displayed frame and continues outputting audio
Unfreeze	Resumes playing after a freeze. Restarts from video frame corresponding to the current audio state.
Play	Play MPEG video and audio

8.2 DRIVER MEMORY ACCESS

The Scenic/MX2 driver does not use the first 2 KBytes of private memory. This area is reserved and should not be accessed by other software.

Section 9: Control Register Descriptions

This section describes the Control Registers for the Scenic/MX2.

In all register bit descriptions, the letter "R" identifies reserved bits (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit). In Power-On Default values, "S" in a bit position means that upon a reset the bit assumes the value of the related strap.

9.1 REGISTER MAPPING AND ADDRESSING

The Scenic/MX2 interfaces to 0.5 or 1.0 MByte of private memory. This memory and 2 KBytes of internal control and status registers are accessed for a single read/write via the LPB Direct Read/Write Address (offset FF14H) and LPB Direct Read/Write Data (offset FF18H) registers in the S3 accelerator to which Scenic/MX2 is interfaced. First, the LPB Direct Read/Write Address register is read or written using the following format:

Bits 23-21 000 = Write
001 = Read

Bit 20 0 = Memory access
1 = Register Access

For memory accesses:

Bits 19-0 Value = Memory address

For Register accesses:

Bits 19-16 Byte Enables. A 1 in any of the bit positions 19-16 disables access to the corresponding byte 3-0 in the register.

Bits 15-11 Reserved

Bits 10-0 Register address

The data is then written to the LPB Direct Read/Write Data register. This write triggers output of the address information to Scenic/MX2 in three bytes, from high order (23-16) to low order (7-0). The data is then output in 4 bytes, from low byte to high byte.

The 2-KByte address space for Scenic/MX2 control registers is subdivided into 8 equally sized address blocks. Each address block is associated with the registers for a programmable/observable hardware module. Each address block contains 256 bytes of control/status information.

Table 9-1. Module Register Base Addresses

Module Name	Module Address (hex)
LPB	0
MIU	2
SP	3
DVP	5

In this section's register descriptions, register addresses are given as a three digit hexadecimal value labeled 'Offset'. The first hex digit of the offset is the base address of the module containing the register. The next two digits are the two-byte index position of the register within the module. For example, the MIU's DRAM Configuration register is in module 2 at index 30H and has an offset value of 230H.

9.2 Scenic Highway REGISTERS

Scenic Highway Module Address = 0H

Scenic Highway Configuration (R0000)

Read Only Offset: 0000H
Power-On Default: 0000 00C3H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Revision								Device ID							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 7-0 Device ID

This is hardwired to C3H.

Bits 15-8 Revision

This is hardwired to 00H for the first production revision.

Bits 31-16 Reserved

Note: Index positions 04H - 1CH are reserved per the Scenic Highway specification.

Scenic Highway Control/Status (R0020)

Read/Write Offset: 0020H
Power-On Default: 0001 07C8H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISA INT			PEIE	PIIE	HO	MBRL		MBWL		R	R	R	R	R	MB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 MB - 8 Doubleword Maximum Burst Size
0 = Maximum burst write length is 8 doublewords.
1 = Maximum burst write length defined by R0020_7-6.

Bits 2-1 Reserved

Bits 4-3 Reserved = 10b

Bit 5 Reserved

Bits 7-6 MBWL - Maximum Burst Write Length
00 = 1 32-bit DWORD
01 = 2 DWORDs
10 = 4 DWORDs
11 = 6 DWORDs (default)

The value programmed in this field must be equal to or greater than the value programmed in bits 17-16 of the LPB Mode (offset FF00) register of the S3 accelerator to which Scenic/MX2 is interfaced.

Bits 9-8 MBRL - Maximum Burst Read Length
00 = 2 32-bit DWORDs
01 = 4 DWORDs
10 = 8 DWORDs
11 = Unlimited DWORDs (default)

Bit 10 HO - HSYNC Orientation
0 = HSYNC sequence executed before each line
1 = HSYNC sequence executed after each line (default)

This applies to burst read data other than DVP data.

Bit 11 PIIE - PCI Internal Interrupt Enable
0 = When an internal interrupt occurs, no PCI interrupt ($\overline{\text{INTA}}$) is asserted
1 = When an internal interrupt occurs, a PCI interrupt ($\overline{\text{INTA}}$) is asserted

Bit 12 PEIE - PCI External Interrupt Enable
0 = When an external interrupt occurs (GINT asserted), a PCI interrupt (INTA) is not asserted
1 = When an external interrupt occurs (GINT asserted), a PCI interrupt (INTA) is asserted

Bits 15-13 ISA INT - ISA Interrupt Selection
000 = No ISA interrupt asserted
001 = IRQA asserted
010 = IRQB asserted
011 = IRQC asserted
10x = IRQD asserted
11x = IRQE asserted

Bit 16 Reserved = 1

Bits 31-17 Reserved

DMA Control/Status (R0034)

Read Only Offset: 0034H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	SR

Bits 15-0 Reserved

Bit 16 SR - Soft Reset

Setting this bit to 1 cause a soft reset of the Scenic/MX2. The consequences are explained in Section 5.

Bits 31-17 Reserved

I²C Port Control/Status (R0060)

See Bit Descriptions Offset: 0000H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											ENB	DR	CR	DW	CW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 CW - I²C Clock Write (Read/Write)
0 = I²C clock output (SCL) driven low by Scenic/MX2
1 = I²C clock output (SCL) tri-stated by Scenic/MX2

Bit 1 DW - I²C Data Write (Read/Write)
0 = I²C data output (SDA) driven low by Scenic/MX2
1 = I²C data output (SDA) tri-stated by Scenic/MX2

Bit 2 CR - I²C Clock Read (Read Only)
0 = I²C clock pin (SCL) is low
1 = I²C clock pin (SCL) tri-stated (no device driving this line)

Bit 3 DR - I²C Data Read (Read Only)
0 = I²C data pin (SDA) driven low by Scenic/MX2
1 = I²C data pin (SDA) tri-stated (no device driving this line)

Bit 4 ENB - Enable I²C Port (Read/Write)
0 = Use of bits 3-0 of this register disabled
1 = Use of bits 3-0 of this register enabled

Bits 33-5 Reserved

9.3 MEMORY INTERFACE UNIT (MIU) REGISTERS

MIU Module Address = 2H

DRAM Configuration (R0230)

Read/Write Offset: 0230H
Power-On Default: 0000 00SSH

DRAM configuration parameters listed here require hardware strapping. For details on hardware pin strapping, see Section 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	RAS LS	RAS PC		RAS PW		CAS/OE/ WE	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 1-0 CAS/OE/WE Stretch
00 = 6.5 ns (nominal)
01 = 5.0 ns (nominal)
10 = 3.5 ns (nominal)
11 = 0 ns (no stretch)

These bits set the additional duration by which $\overline{CAS}/\overline{OE}/\overline{WE}$ are extended.

Bits 3-2 RAS PW - $\overline{RAS}$ Pulse Width
00 = 7 or 6.5 MCLKs
01 = 6 or 5.5 MCLKs
10 = 5 or 4.5 MCLKs
11 = 4 or 3.5 MCLKs

These bits are used in combination with bit 6 to select a pulse width. For example, setting bits 3-2 to 01 and bit 6 to 1 will select 5.5 MCLKs as the $\overline{RAS}$ pulse width. See Tables 5-2 and 5-3.

Bits 5-4 RAS PC - $\overline{RAS}$ Precharge
00 = 4 or 4.5 MCLKs
01 = 3 or 3.5 MCLKs
10 = 2 or 2.5 MCLKs
11 = Reserved

These bits are used in combination with bit 6 to select a precharge duration.

Bit 6 RAS LS - $\overline{RAS}$ Length Select - Default: PD6 strap
0 = $\overline{RAS}$ Precharge = 2, 3, or 4 MCLKs;
$\overline{RAS}$ Pulse Width= 4, 5, 6, or 7 MCLKs
1 = $\overline{RAS}$ Precharge = 2.5, 3.5, or 4.5 MCLKs
$\overline{RAS}$ Pulse Width= 3.5, 4.5, 5.5, or 6.5 MCLKs

This bit is used together with bits 3-2 and bits 5-4 to select timing values. See details in Section 5.

Bits 31-7 Reserved. (Returns zero upon read)

Refresh Count (R0238)

Read/Write Offset: 0238H
Power-On Default: 0000 1200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	REF EN	RCT											

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 RCT - Refresh Count in MCLKs
The default value is 512.

Bit 12 REF EN - Refresh Enable
0 = Disable DRAM Refresh
1 = Enable DRAM Refresh (default)

Bits 31-13 Reserved. (Returns zero upon read)

9.4 SERIAL PORT (SP) REGISTERS

SP Module Address = 3H

Data Output (R0300)

See bit descriptions Offset: 0300H
Power-On Default: 0000 0000 0SSS S000 0SSS S001 0000 0101 b

Certain bits of this register require hardware strapping to set the values upon power up. These bits are identified in the accompanying text below and the corresponding signal line to strap is identified. For details of hardware pin strapping, see Section 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SLD			LRC	R	AM		AF	Reserved			SF		R	SA EN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	AFS	SCI	ADA	ABO	LT	R	R	R

Bit 0 SA EN - Software Audio Enable (read/write)
0 = Audio Enable
1 = Audio Disable (default)

Bit 1 Reserved

Bits 3-2 SF - Sampling Frequency (read/write)
00 = 32 KHz
01 = 44.1 KHz (default)
10 = 48 KHz
11 = PLL Select (S3 Sonic/AD)

Bits 6-4 Reserved

Bit 7 AF - Audio Freeze (read/write)
When this is asserted, the data in the output FIFO is untouched. Scenic/MX2 can resume without losing samples when this is deasserted.
0 = Audio Freeze off (default)
1 = Audio Freeze on

Bit 9-8 AM - Audio Mute (read/write)
Sets audio mask to zero and also sends mute control bit to audio DAC.
00 = No mute
01 = Hard mute (default)
10 = Soft mute (10 ms)
11 = Soft mute (20 ms)

Bit 10 Reserved (Returns zero upon read)

Bit 11 LRC - LRCHN Channel Interpretation (read)
0 = LRCHN active high left channel
1 = LRCHN active high right channel

Bits 14-12 SLD - SCLK and LRCHN Definition (read)
000 = 256 DAC clocks per LRCHN, 2 DAC clocks per SCLK
001 = 256 DAC clocks per LRCHN, 4 DAC clocks per SCLK
010 = 384 DAC clocks per LRCHN, 2 DAC clocks per SCLK
011 = 384 DAC clocks per LRCHN, 4 DAC clocks per SCLK
100 = 384 DAC clocks per LRCHN, 6 DAC clocks per SCLK
101 = 384 DAC clocks per LRCHN, 8 DAC clocks per SCLK
110 = 512 DAC clocks per LRCHN, 4 DAC clocks per SCLK
111 = 512 DAC clocks per LRCHN, 8 DAC clocks per SCLK

Bits 18-15 Reserved (Returns zero upon read)

Bit 19 LT - Lag Time (read)
0 = First 16 bits latched on an LRCHN phase
1 = Last 16 bits latched on an LRCHN phase

Bit 20 ABO - Audio Bit Order (read)
0 = Bit 0 first
1 = Bit 15 first

Bit 21 ADA - Audio DAC Absent (read)
0 = Audio DAC present
1 = Audio DAC absent

Bit 22 SCI - SCLK Inverted (read) - Default: PD14
0 = Data latched on rising edge of SCLK
1 = Data latched on falling edge of SCLK

Bit 23 AFS - Audio FIFO Starved (read)
0 = No starvation
1 = FIFO was starved

This bit clears on reset or audio disable.

Bits 31-24 Reserved (Returns zero upon read)

S3 DAC Control Data (R0308)

Read/Write Offset: 0308H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL RC								PLL LC							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	R	APR LC	ISF SEL

Bits 7-0 PLL LC - PLL Data on Left Channel
M[7:0] data for the S3 Sonic/AD

Bits 15-8 PLL RC - PLL Data on Right Channel
N[7:0] data for the S3 Sonic/AD

Bit 16 ISF SEL - ISF Select
0 = Choose the sampling frequency from external FS pins
1 = Choose the sampling frequency from the audio data

Bit 17 APR LC - S3 Sonic/AD PLL Registers Load Control
0 = Do not load PLL registers
1= Load S3 Sonic/AD PLL registers from SDATA

Bits 31-18 Reserved. (Returns zero upon read)

9.5 DIGITIZED VIDEO PORT (DVP) CONTROL REGISTERS

DVP Module Address = 5H

DVP Control Status (R0500)

See Bit Descriptions Offset: 0500H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	LC VAL	DHO	NF TIME	DVP OUT	VSY POL	HR POL	CR POL	EXT CR	DVP ENB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	M2	M1	M0

Bit 0 DVP ENB - DVP Enable (Read/Write)
0 = DVP function disabled
1 = DVP function enabled

Bit 1 EXT CR - External CREF (Read/Write)
0 = DVP creates its own CREF set by the rising edge of HREF to determine which inputs to examine each cycle in 16-bit data mode
1 = DVP uses the CREF input to determine which inputs to examine each cycle in 16-bit data mode

Bit 2 CR POL - CREF Polarity
0 = CREF input is active high
1 = CREF input is active low

Bit 3 HR POL - HREF Polarity
0 = HREF input is active high
1 = HREF input is active low

Bit 4 VSY POL - VSYNC Polarity
0 = VSYNC input is active high
1 = VSYNC input is active low

Bit 5 DVP OUT - DVP Output Sequence
0 = DVP output sequence to LPB is Cb-Y0-Cr-Y1
1 = DVP output sequence to LPB is Y0-Cb-Y1-Cr

Bit 6 Reserved

Bit 7 DHO - DVP Horizontal Orientation
0 = LPB HSYNC sequence executed before each line
1 = LPB HSYNC sequence executed after each line

This bit applies only to DVP data. Bit 10 of R0000 is used for other data.

Bit 8 LC VAL - Line Counter Valid
0 = Resync the line counter between the current frame and the next
1 = The line counter has been resynchronized

Software optionally clears this bit to 0 to resync the line counter. The hardware sets the bit to 1 when synchronization is complete.

Bits 15-9 Reserved

Bit 16 M0 - MODE0
0 = DVP active (LCLK is DVPCLK)
1 = DVP inactive (no digitizer)

The MODE0 pin is strapped to set the initial value of this bit.

Bit 17 M1 - MODE1
0 = If bit 16 of this register is 0, the DVP operates in 16-bit data mode
If bit 16 of this register is 1 and bit 18 of this register is 1, LCLK = 1/2 DVPCLK
1 = If bit 16 of this register is 0, the DVP operates in 8-bit data mode
If bit 16 of this register is 1 and bit 18 of this register is 1, LCLK = 2/3 DVPCLK

The MODE1 pin is strapped to set the initial value of this bit.

Bit 18 M2 - MODE2
If bit 16 of this register = 1 (no digitizer)
0 = LCLK is DVPCLK (external clock attached to DVPCLK pin)
1 = LCLK is 1/2 or 2/3 MCLK, depending on setting of bit 17 of this register

If bit 16 of this register = 0 (DVP active) and bit 17 of this register = 1 (8-bit data)
0 = Data input sequence is Cb-Y0-Cr-Y1
1 = Data input sequence is Y0-Cb-Y1-Cr

The MODE2 pin is strapped to set the initial value of this bit.

Bits 31-19 Reserved

S3 Incorporated, 2770 San Tomas Expressway, Santa Clara, CA 95051-0968 Tel: 408-980-5400, Fax: 408-980-5444

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