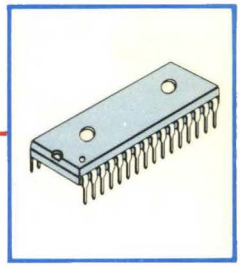
SAMSUNG

Data Book

MOS Memory

1993/94



- EEPROM
- MASK ROM

SAMSUNG

MOS Memory Data Book
(EEPROM/MASK ROM)

1993/94

TABLE OF CONTENTS

Ⅰ. FUNCTION GUIDE

Ⅱ. EEPROM DATA SHEETS

Ⅲ. MASKROM DATA SHEETS

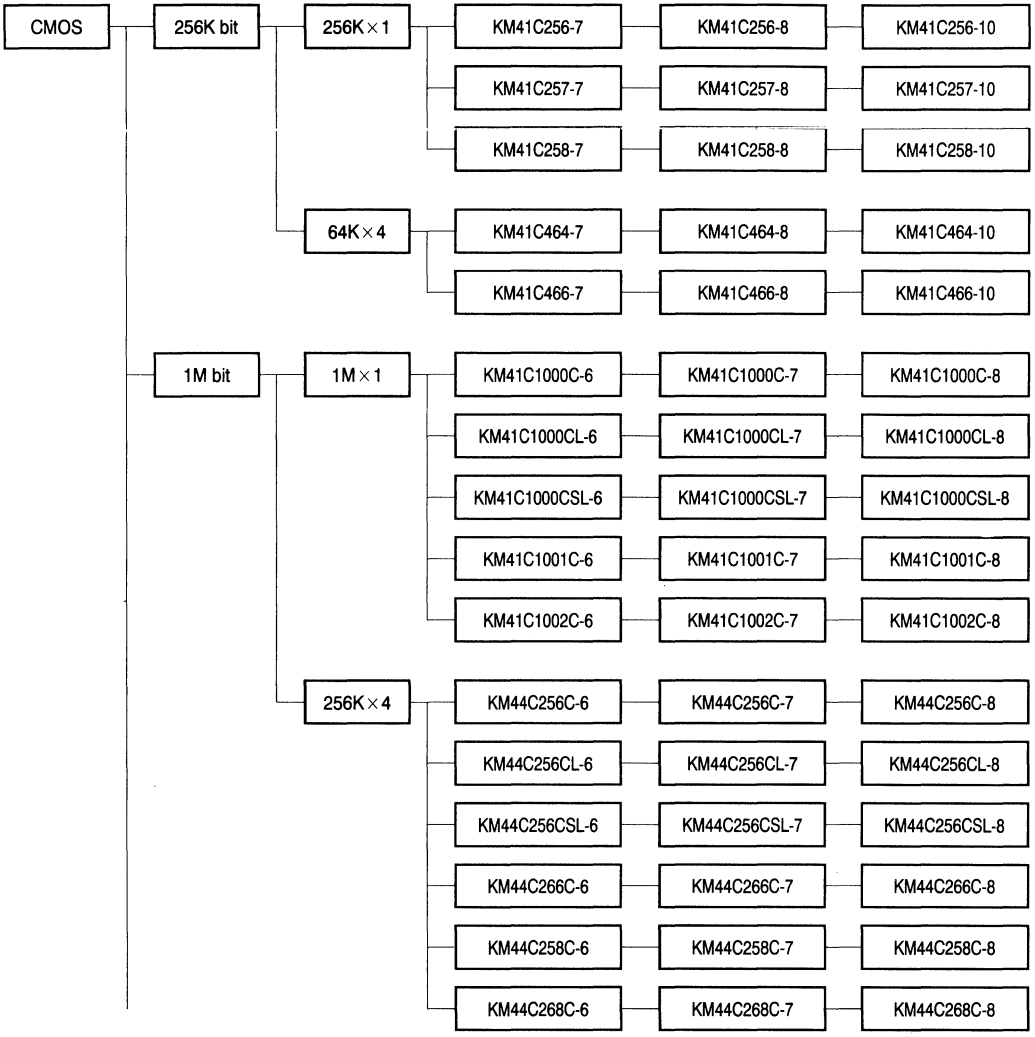
TABLE OF CONTENTS (Continued)

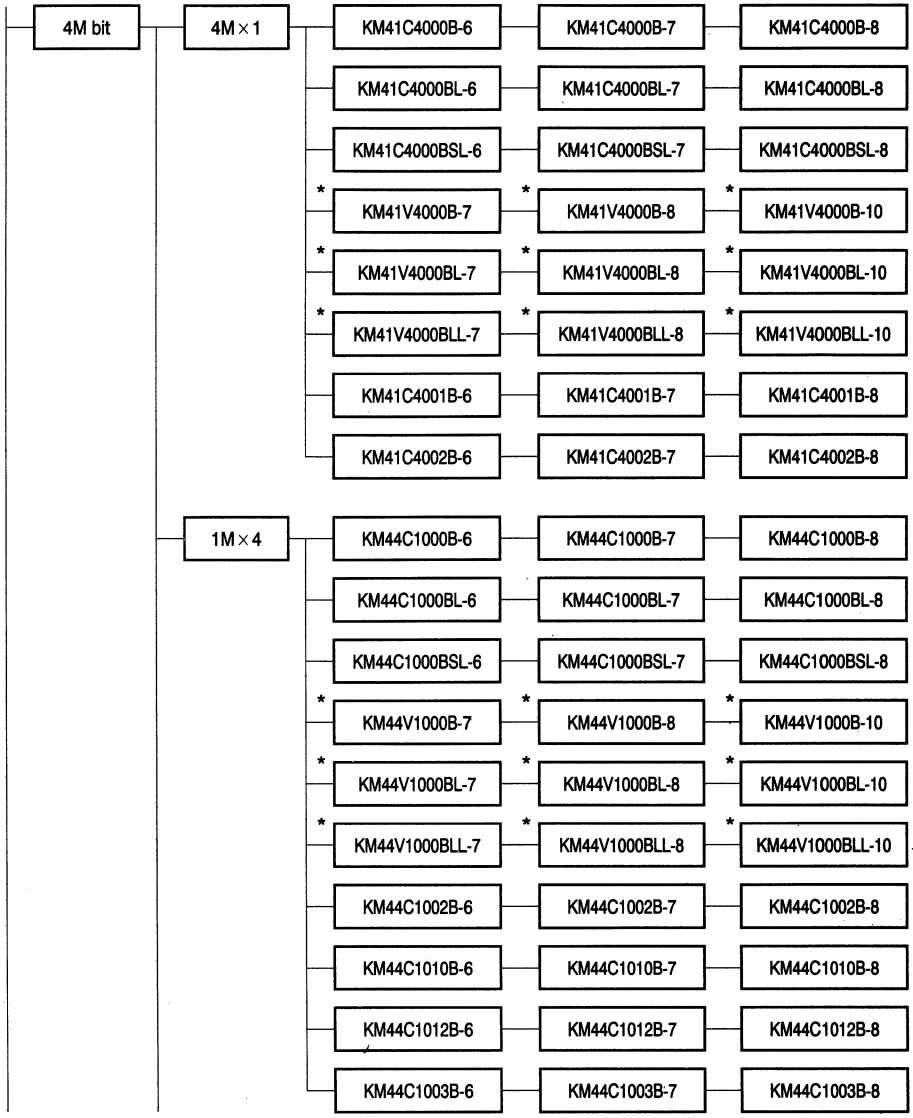
FUNCTION GUIDE 1

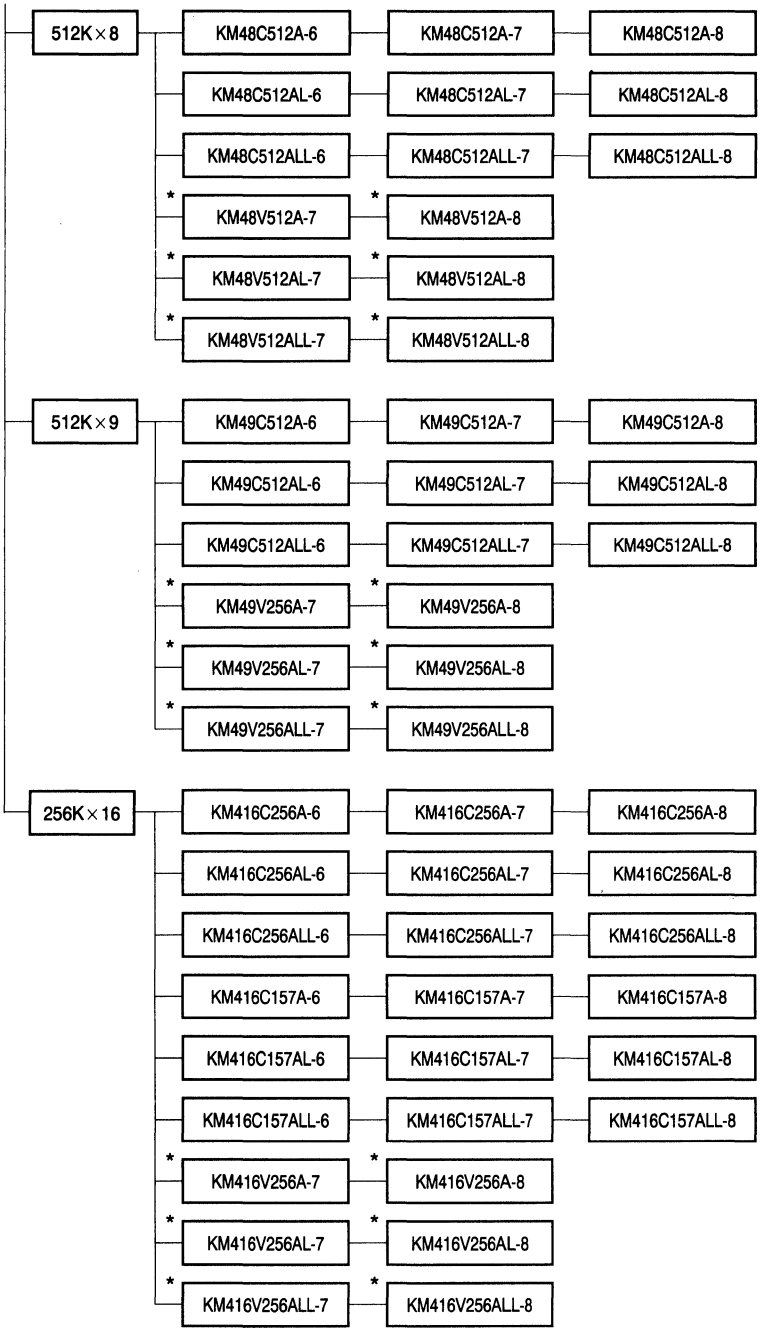
1. Introduction
2. Product Guide
3. Cross Re
4. Orderin

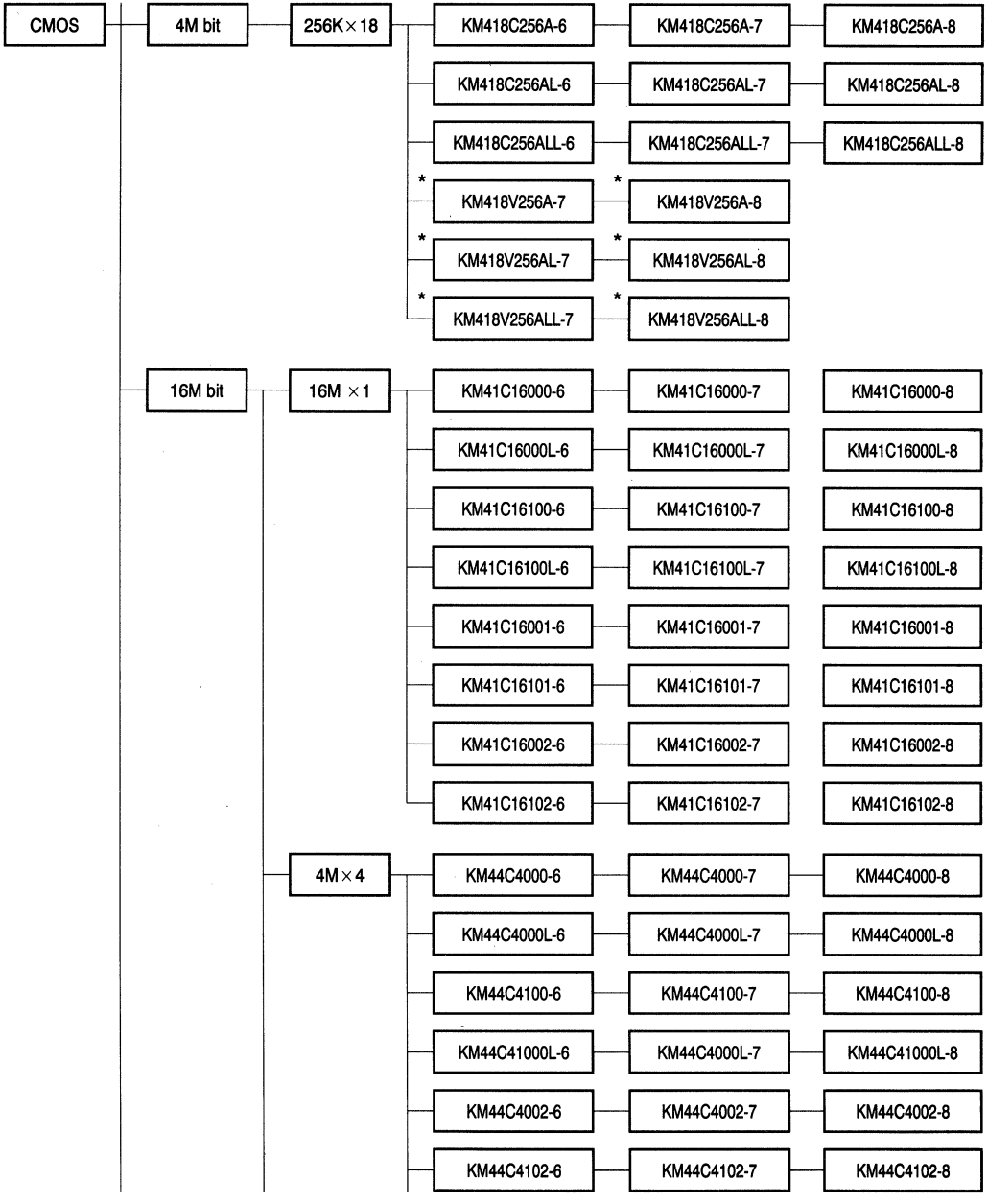
1. INTRODUCTION

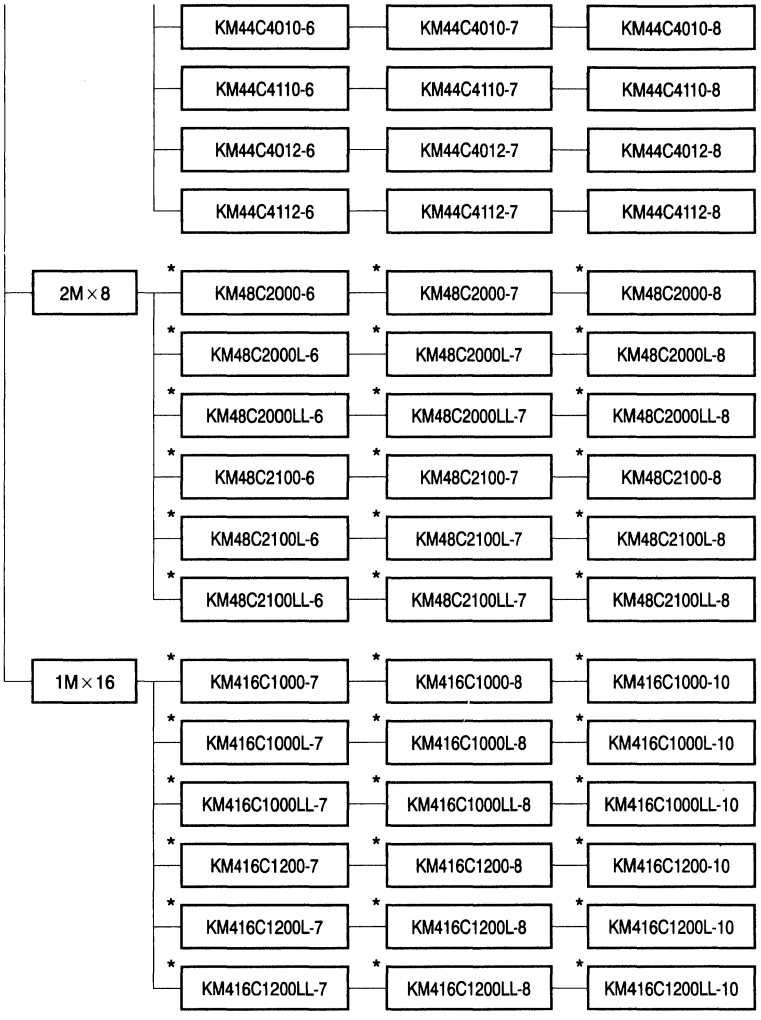
1.1 Dynamic RAM




4M bit
4M × 1
KM41C4000B-6
KM41C4000B-7
KM41C4000B-8
KM41C4000BL-6
KM41C4000BL-7
KM41C4000BL-8
KM41C4000BSL-6
KM41C4000BSL-7
KM41C4000BSL-8
* KM41V4000B-7
* KM41V4000B-8
* KM41V4000B-10
* KM41V4000BL-7
* KM41V4000BL-8
* KM41V4000BL-10
* KM41V4000BLL-7
* KM41V4000BLL-8
* KM41V4000BLL-10
KM41C4001B-6
KM41C4001B-7
KM41C4001B-8
KM41C4002B-6
KM41C4002B-7
KM41C4002B-8
1M × 4
KM44C1000B-6
KM44C1000B-7
KM44C1000B-8
KM44C1000BL-6
KM44C1000BL-7
KM44C1000BL-8
KM44C1000BSL-6
KM44C1000BSL-7
KM44C1000BSL-8
* KM44V1000B-7
* KM44V1000B-8
* KM44V1000B-10
* KM44V1000BL-7
* KM44V1000BL-8
* KM44V1000BL-10
* KM44V1000BLL-7
* KM44V1000BLL-8
* KM44V1000BLL-10
KM44C1002B-6
KM44C1002B-7
KM44C1002B-8
KM44C1010B-6
KM44C1010B-7
KM44C1010B-8
KM44C1012B-6
KM44C1012B-7
KM44C1012B-8
KM44C1003B-6
KM44C1003B-7
KM44C1003B-8

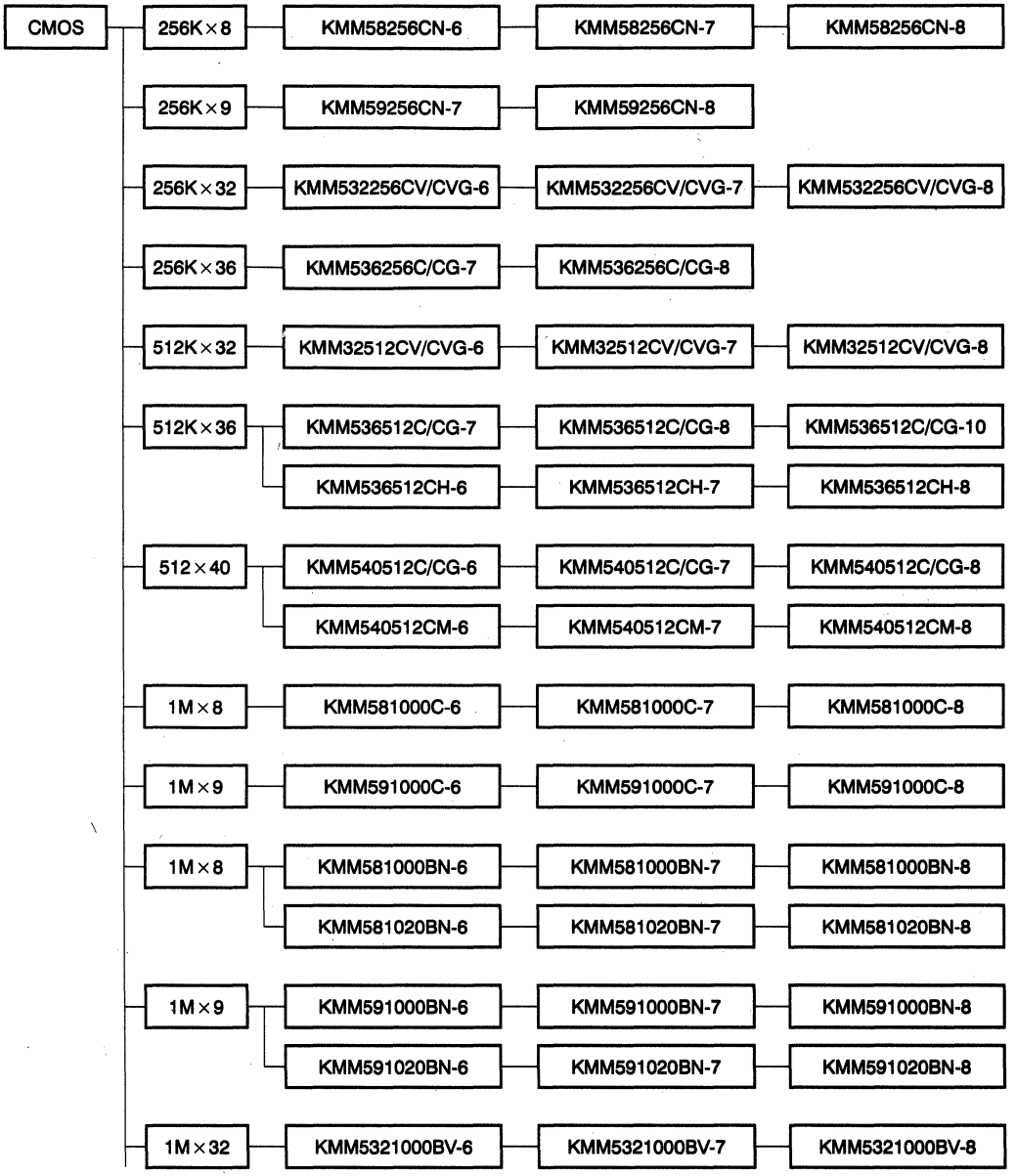

512K×8
KM48C512A-6
KM48C512A-7
KM48C512A-8
KM48C512AL-6
KM48C512AL-7
KM48C512AL-8
KM48C512ALL-6
KM48C512ALL-7
KM48C512ALL-8
* KM48V512A-7
* KM48V512A-8
* KM48V512AL-7
* KM48V512AL-8
* KM48V512ALL-7
* KM48V512ALL-8
512K×9
KM49C512A-6
KM49C512A-7
KM49C512A-8
KM49C512AL-6
KM49C512AL-7
KM49C512AL-8
KM49C512ALL-6
KM49C512ALL-7
KM49C512ALL-8
* KM49V256A-7
* KM49V256A-8
* KM49V256AL-7
* KM49V256AL-8
* KM49V256ALL-7
* KM49V256ALL-8
256K×16
KM416C256A-6
KM416C256A-7
KM416C256A-8
KM416C256AL-6
KM416C256AL-7
KM416C256AL-8
KM416C256ALL-6
KM416C256ALL-7
KM416C256ALL-8
KM416C157A-6
KM416C157A-7
KM416C157A-8
KM416C157AL-6
KM416C157AL-7
KM416C157AL-8
KM416C157ALL-6
KM416C157ALL-7
KM416C157ALL-8
* KM416V256A-7
* KM416V256A-8
* KM416V256AL-7
* KM416V256AL-8
* KM416V256ALL-7
* KM416V256ALL-8

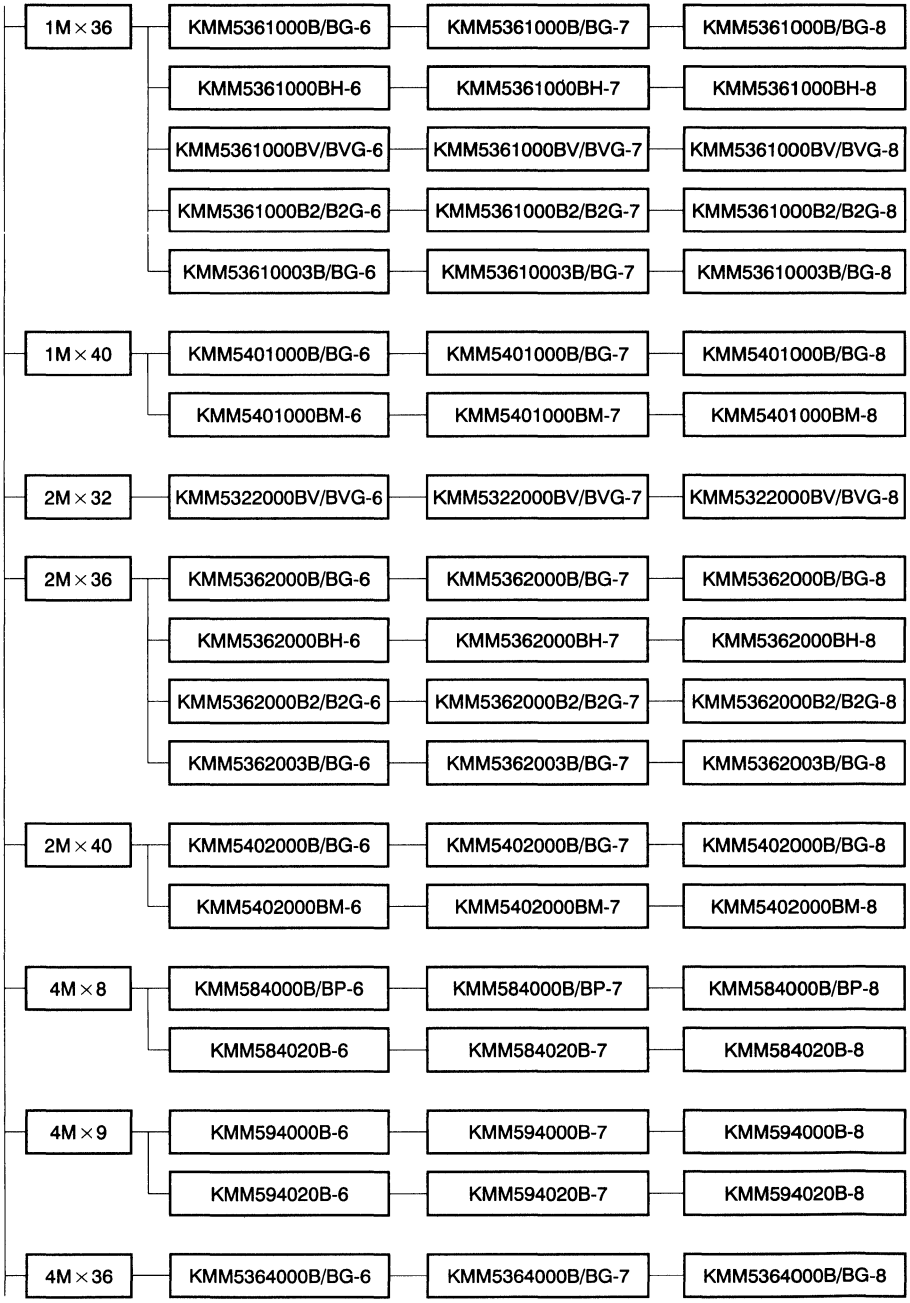

CMOS
4M bit
256K×18
KM418C256A-6
KM418C256A-7
KM418C256A-8
KM418C256AL-6
KM418C256AL-7
KM418C256AL-8
KM418C256ALL-6
KM418C256ALL-7
KM418C256ALL-8
* KM418V256A-7
* KM418V256A-8
* KM418V256AL-7
* KM418V256AL-8
* KM418V256ALL-7
* KM418V256ALL-8
16M bit
16M ×1
KM41C16000-6
KM41C16000-7
KM41C16000-8
KM41C16000L-6
KM41C16000L-7
KM41C16000L-8
KM41C16100-6
KM41C16100-7
KM41C16100-8
KM41C16100L-6
KM41C16100L-7
KM41C16100L-8
KM41C16001-6
KM41C16001-7
KM41C16001-8
KM41C16101-6
KM41C16101-7
KM41C16101-8
KM41C16002-6
KM41C16002-7
KM41C16002-8
KM41C16102-6
KM41C16102-7
KM41C16102-8
4M×4
KM44C4000-6
KM44C4000-7
KM44C4000-8
KM44C4000L-6
KM44C4000L-7
KM44C4000L-8
KM44C4100-6
KM44C4100-7
KM44C4100-8
KM44C41000L-6
KM44C4000L-7
KM44C41000L-8
KM44C4002-6
KM44C4002-7
KM44C4002-8
KM44C4102-6
KM44C4102-7
KM44C4102-8

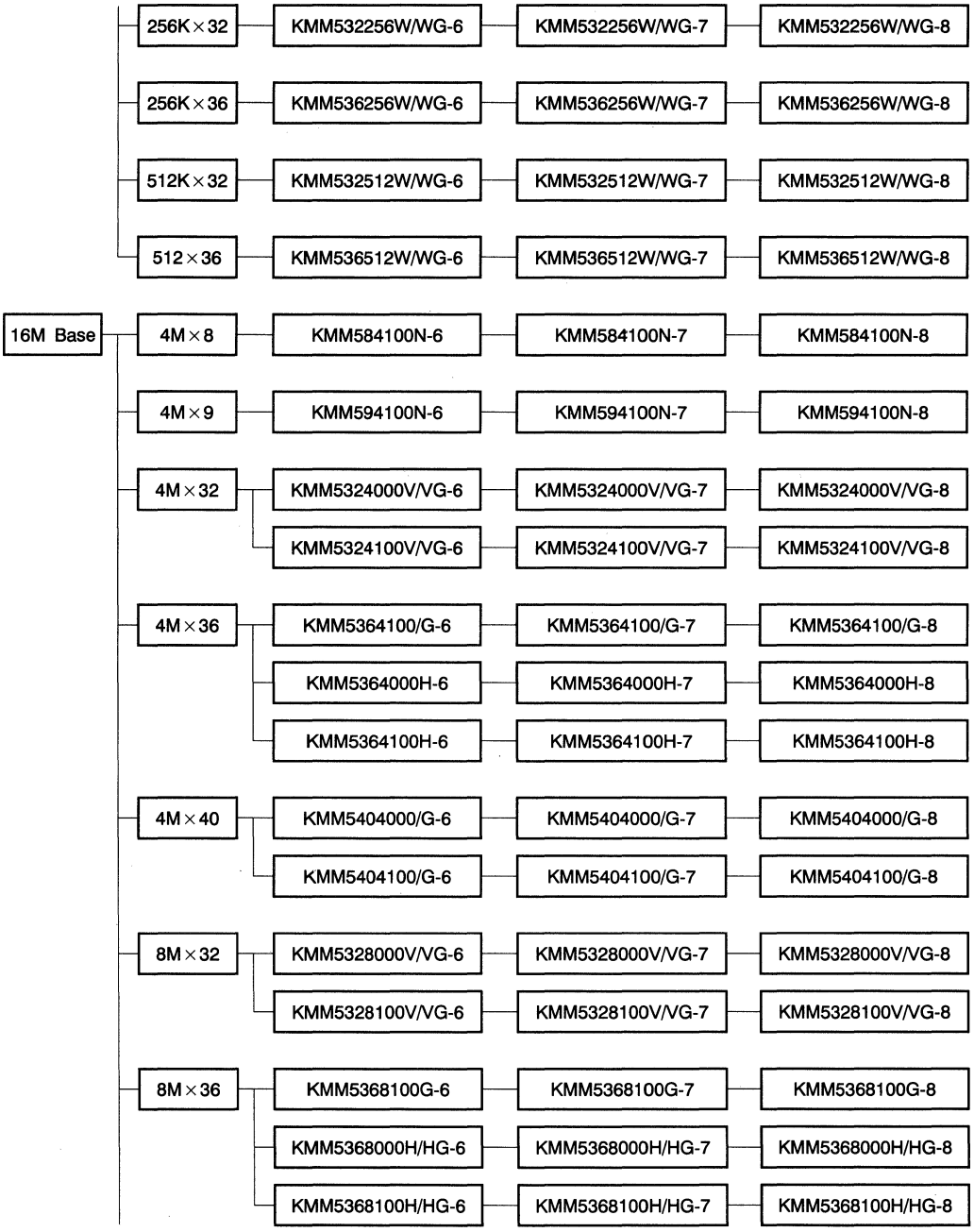


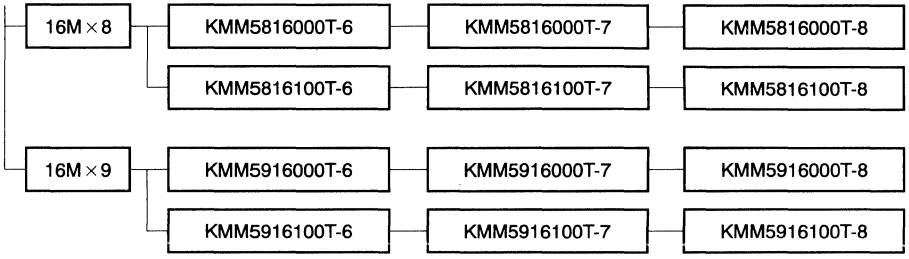
* : New Product
† : Preliminary Product
†† : Under Development

1.2 Dynamic RAM Module

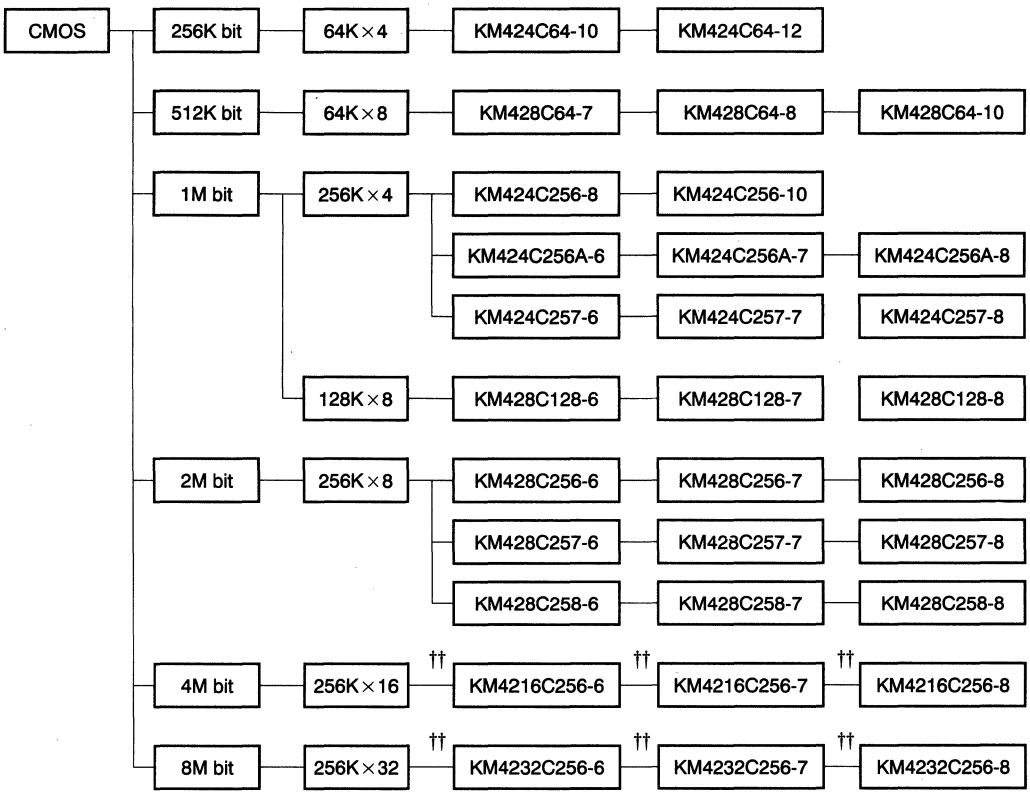



1M × 36
KMM5361000B/BG-6
KMM5361000B/BG-7
KMM5361000B/BG-8
KMM5361000BH-6
KMM5361000BH-7
KMM5361000BH-8
KMM5361000BV/BVG-6
KMM5361000BV/BVG-7
KMM5361000BV/BVG-8
KMM5361000B2/B2G-6
KMM5361000B2/B2G-7
KMM5361000B2/B2G-8
KMM53610003B/BG-6
KMM53610003B/BG-7
KMM53610003B/BG-8
1M × 40
KMM5401000B/BG-6
KMM5401000B/BG-7
KMM5401000B/BG-8
KMM5401000BM-6
KMM5401000BM-7
KMM5401000BM-8
2M × 32
KMM5322000BV/BVG-6
KMM5322000BV/BVG-7
KMM5322000BV/BVG-8
2M × 36
KMM5362000B/BG-6
KMM5362000B/BG-7
KMM5362000B/BG-8
KMM5362000BH-6
KMM5362000BH-7
KMM5362000BH-8
KMM5362000B2/B2G-6
KMM5362000B2/B2G-7
KMM5362000B2/B2G-8
KMM5362003B/BG-6
KMM5362003B/BG-7
KMM5362003B/BG-8
2M × 40
KMM5402000B/BG-6
KMM5402000B/BG-7
KMM5402000B/BG-8
KMM5402000BM-6
KMM5402000BM-7
KMM5402000BM-8
4M × 8
KMM584000B/BP-6
KMM584000B/BP-7
KMM584000B/BP-8
KMM584020B-6
KMM584020B-7
KMM584020B-8
4M × 9
KMM594000B-6
KMM594000B-7
KMM594000B-8
KMM594020B-6
KMM594020B-7
KMM594020B-8
4M × 36
KMM5364000B/BG-6
KMM5364000B/BG-7
KMM5364000B/BG-8


256K×32
KMM532256W/WG-6
KMM532256W/WG-7
KMM532256W/WG-8
256K×36
KMM536256W/WG-6
KMM536256W/WG-7
KMM536256W/WG-8
512K×32
KMM532512W/WG-6
KMM532512W/WG-7
KMM532512W/WG-8
512×36
KMM536512W/WG-6
KMM536512W/WG-7
KMM536512W/WG-8
16M Base
4M×8
KMM584100N-6
KMM584100N-7
KMM584100N-8
4M×9
KMM594100N-6
KMM594100N-7
KMM594100N-8
4M×32
KMM5324000V/VG-6
KMM5324000V/VG-7
KMM5324000V/VG-8
KMM5324100V/VG-6
KMM5324100V/VG-7
KMM5324100V/VG-8
4M×36
KMM5364100/G-6
KMM5364100/G-7
KMM5364100/G-8
KMM5364000H-6
KMM5364000H-7
KMM5364000H-8
KMM5364100H-6
KMM5364100H-7
KMM5364100H-8
4M×40
KMM5404000/G-6
KMM5404000/G-7
KMM5404000/G-8
KMM5404100/G-6
KMM5404100/G-7
KMM5404100/G-8
8M×32
KMM5328000V/VG-6
KMM5328000V/VG-7
KMM5328000V/VG-8
KMM5328100V/VG-6
KMM5328100V/VG-7
KMM5328100V/VG-8
8M×36
KMM5368100G-6
KMM5368100G-7
KMM5368100G-8
KMM5368000H/HG-6
KMM5368000H/HG-7
KMM5368000H/HG-8
KMM5368100H/HG-6
KMM5368100H/HG-7
KMM5368100H/HG-8


16M×8
KMM5816000T-6
KMM5816000T-7
KMM5816000T-8
KMM5816100T-6
KMM5816100T-7
KMM5816100T-8
16M×9
KMM5916000T-6
KMM5916000T-7
KMM5916000T-8
KMM5916100T-6
KMM5916100T-7
KMM5916100T-8

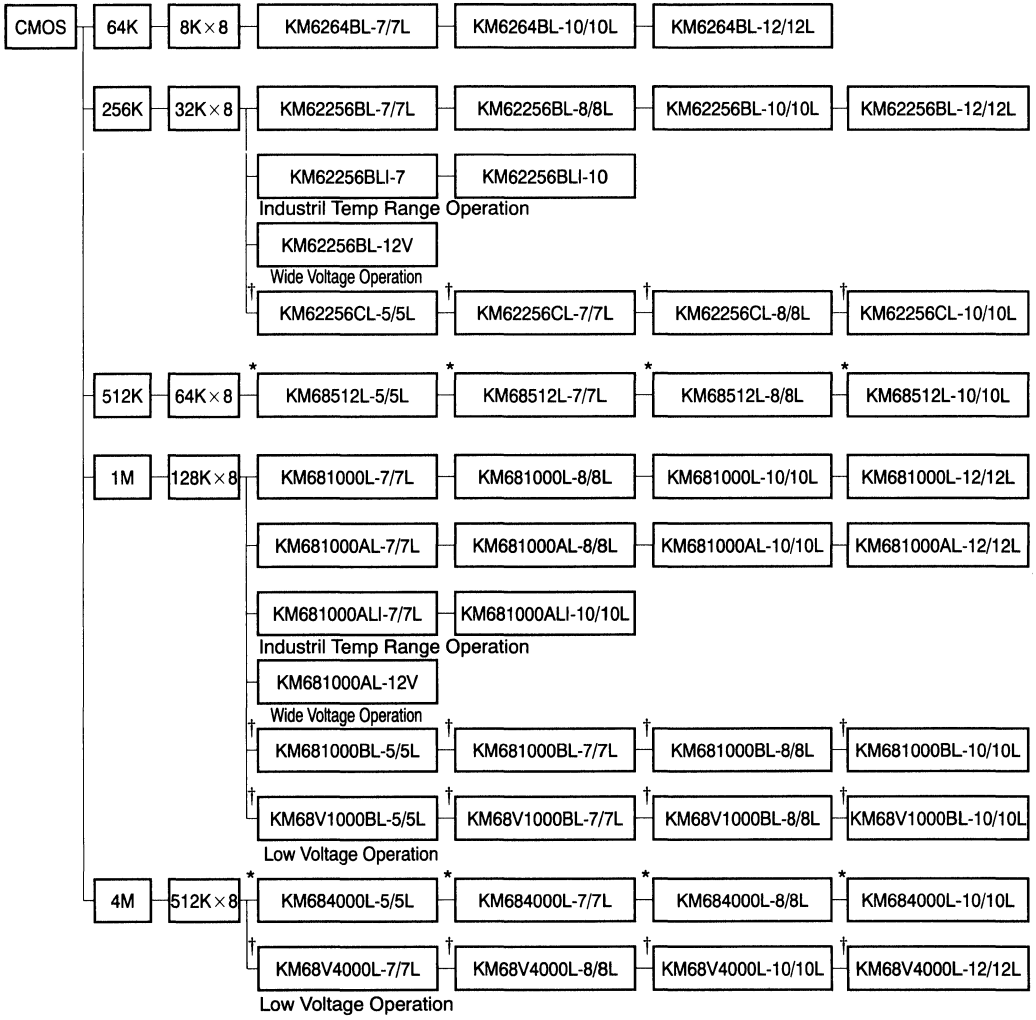
1.3 Video RAM



†† Under Development

1.4 Static RAM

Low Power SRAM



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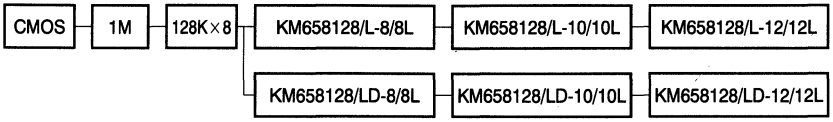
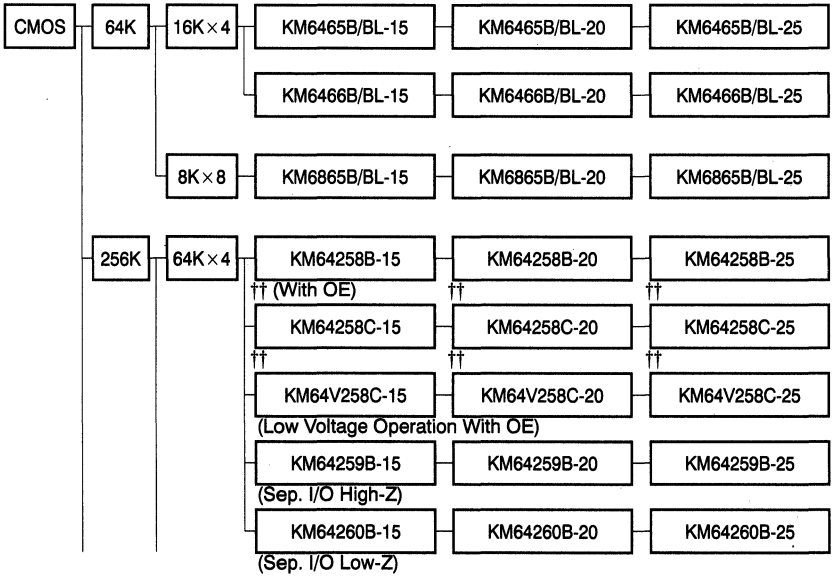
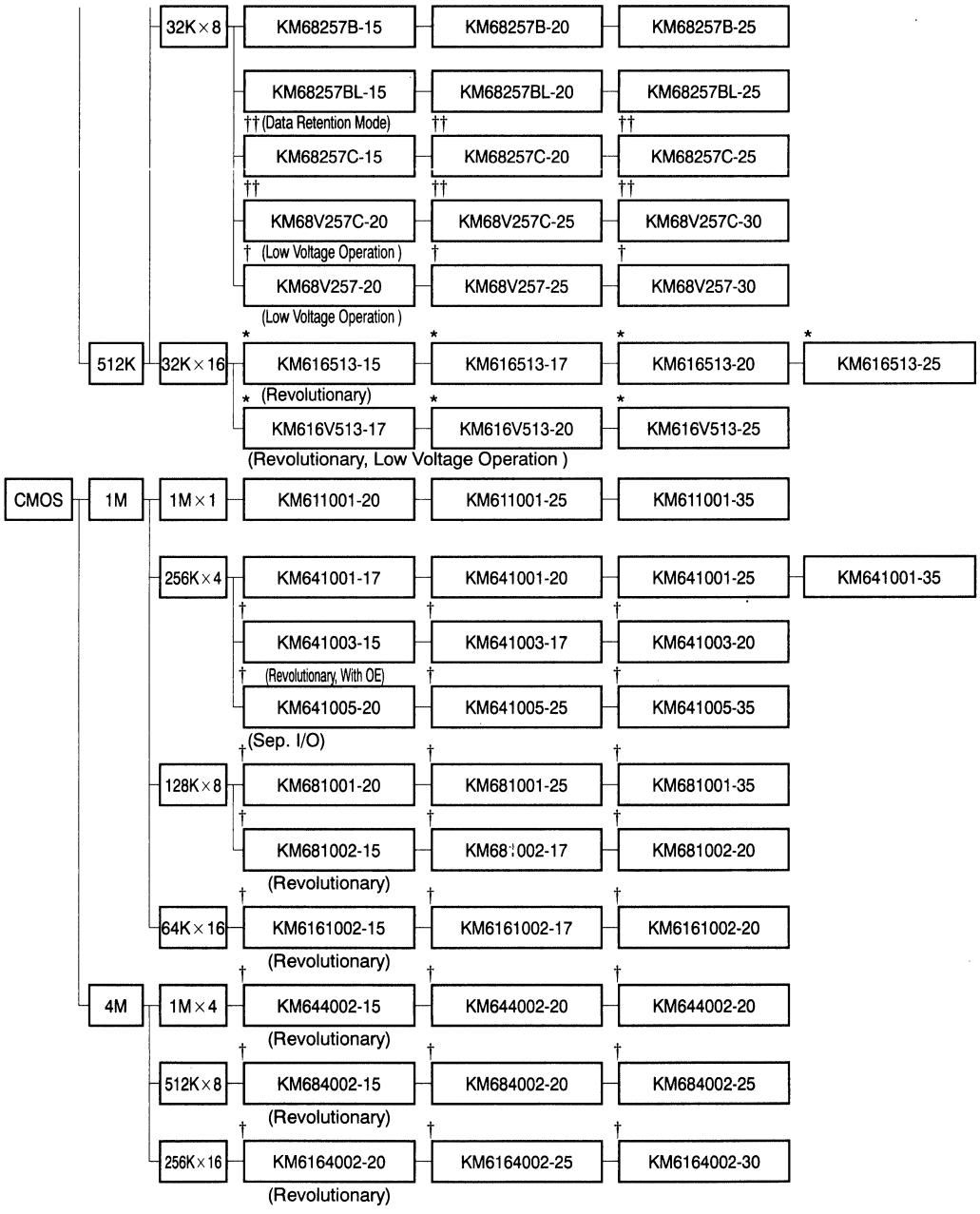
Pseudo SRAM



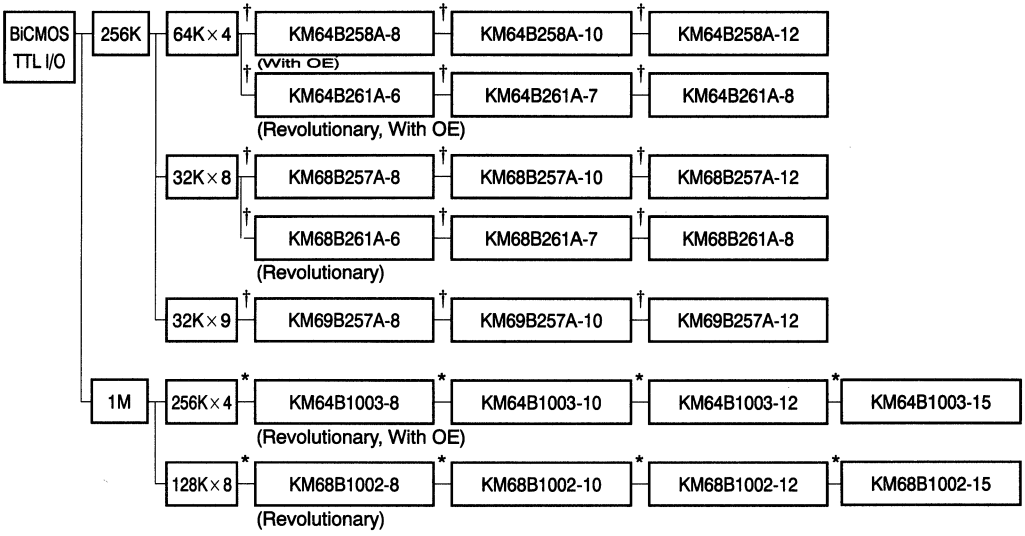
* New Product
† Preliminary
†† Under Development

High Speed SRAM

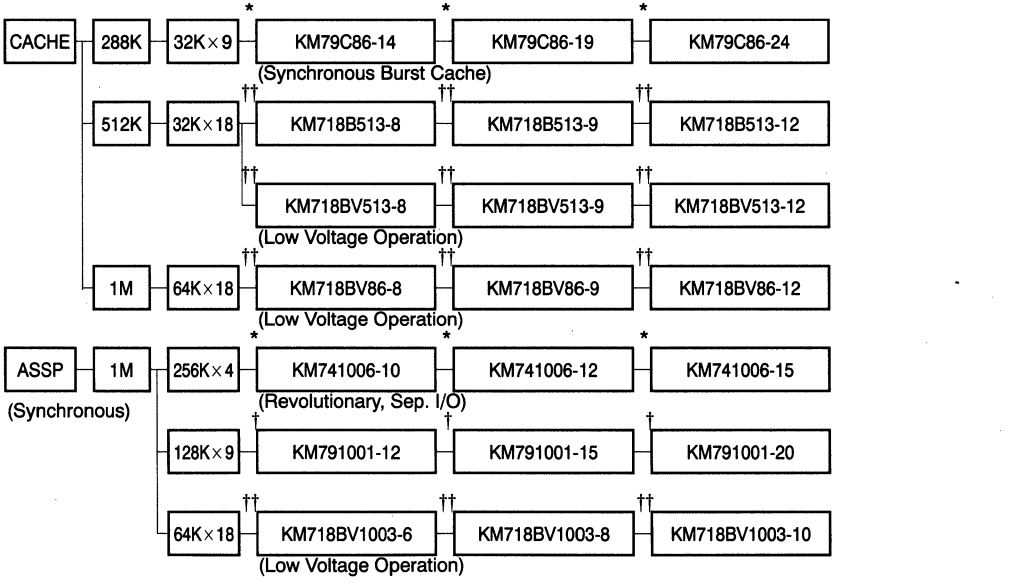



32K×8
KM68257B-15
KM68257B-20
KM68257B-25
KM68257BL-15
KM68257BL-20
KM68257BL-25
†† (Data Retention Mode)
KM68257C-15
KM68257C-20
KM68257C-25
KM68V257C-20
KM68V257C-25
KM68V257C-30
† (Low Voltage Operation)
KM68V257-20
KM68V257-25
KM68V257-30
(Low Voltage Operation)
512K
32K×16
KM616513-15
KM616513-17
KM616513-20
KM616513-25
* (Revolutionary)
KM616V513-17
KM616V513-20
KM616V513-25
(Revolutionary, Low Voltage Operation)
CMOS
1M
1M×1
KM611001-20
KM611001-25
KM611001-35
256K×4
KM641001-17
KM641001-20
KM641001-25
KM641001-35
KM641003-15
KM641003-17
KM641003-20
† (Revolutionary, With OE)
KM641005-20
KM641005-25
KM641005-35
† (Sep. I/O)
128K×8
KM681001-20
KM681001-25
KM681001-35
KM681002-15
KM681002-17
KM681002-20
(Revolutionary)
64K×16
KM6161002-15
KM6161002-17
KM6161002-20
(Revolutionary)
4M
1M×4
KM644002-15
KM644002-20
KM644002-20
(Revolutionary)
512K×8
KM684002-15
KM684002-20
KM684002-25
(Revolutionary)
256K×16
KM6164002-20
KM6164002-25
KM6164002-30
(Revolutionary)

BiCMOS SRAM



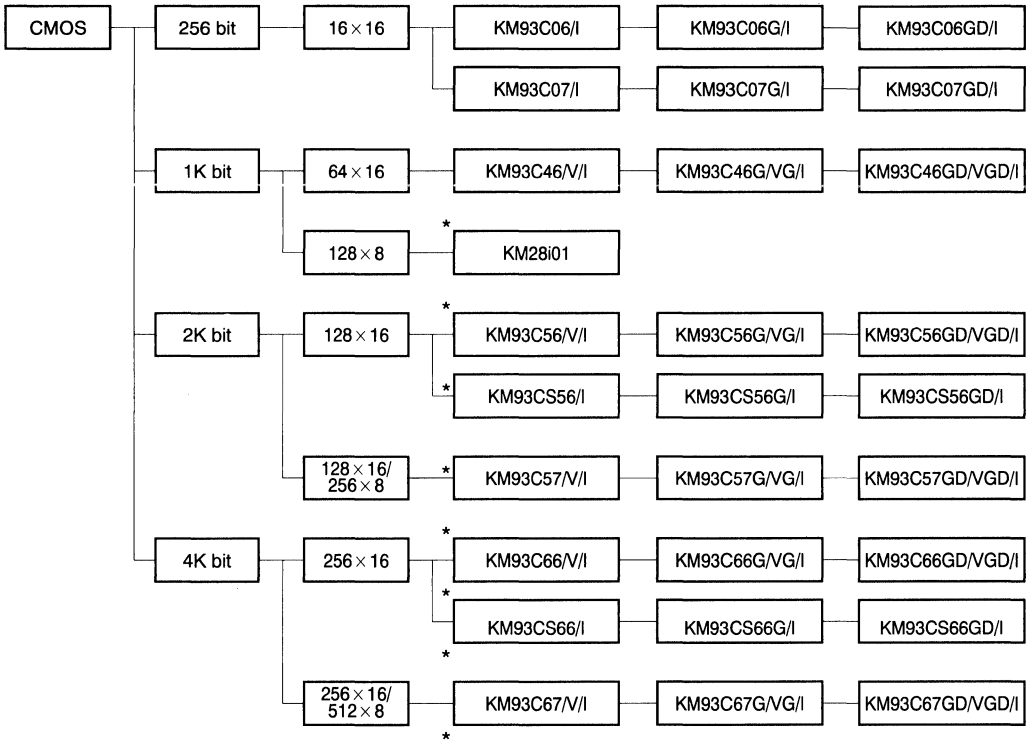
Specialty SRAM



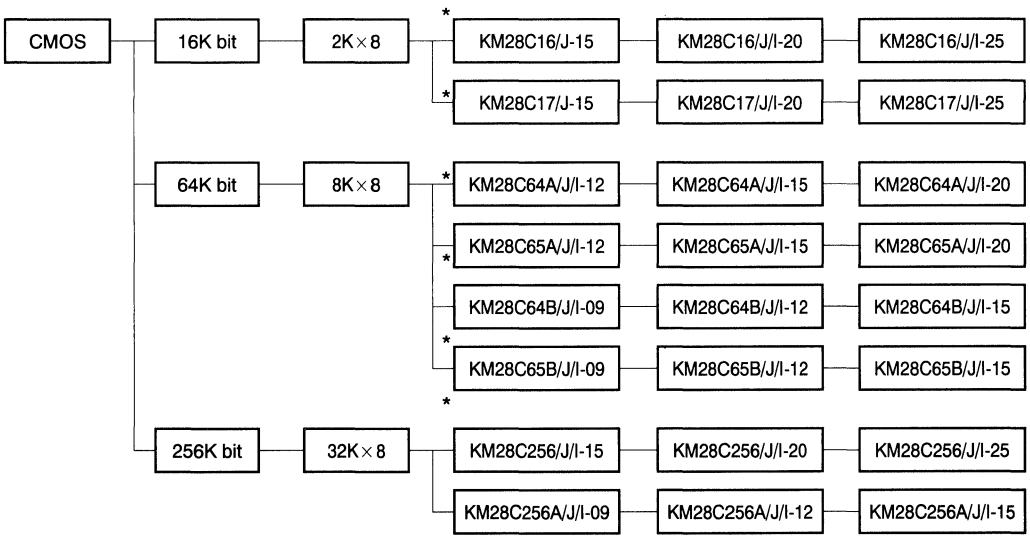
* : New Product
† : Preliminary Product
†† : Under Development

1.5 EEPROM

***Serial EEPROM**



***Parallel EEPROM**



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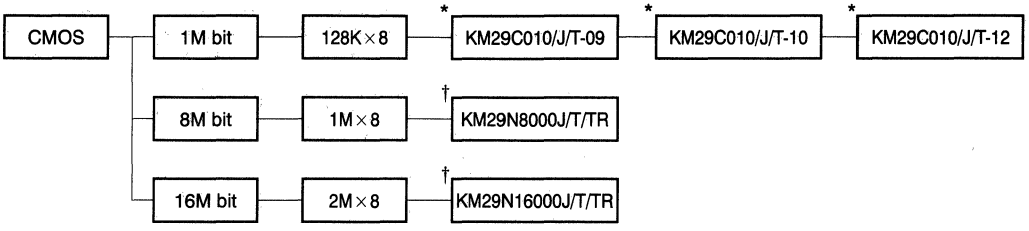
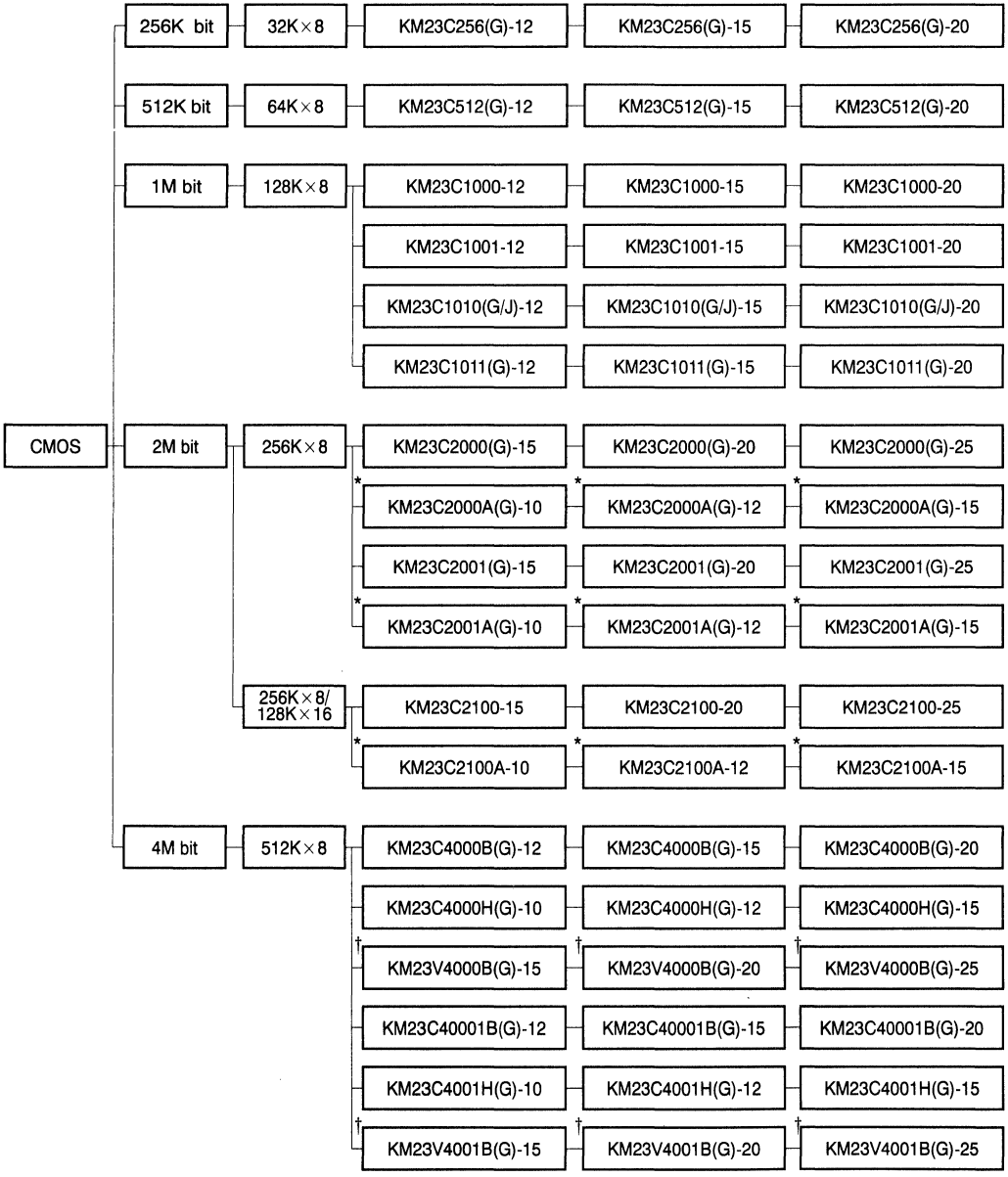
***Flash Memory**



* : New Product
† : Preliminary Product

1.6 Mask ROM

Low Density

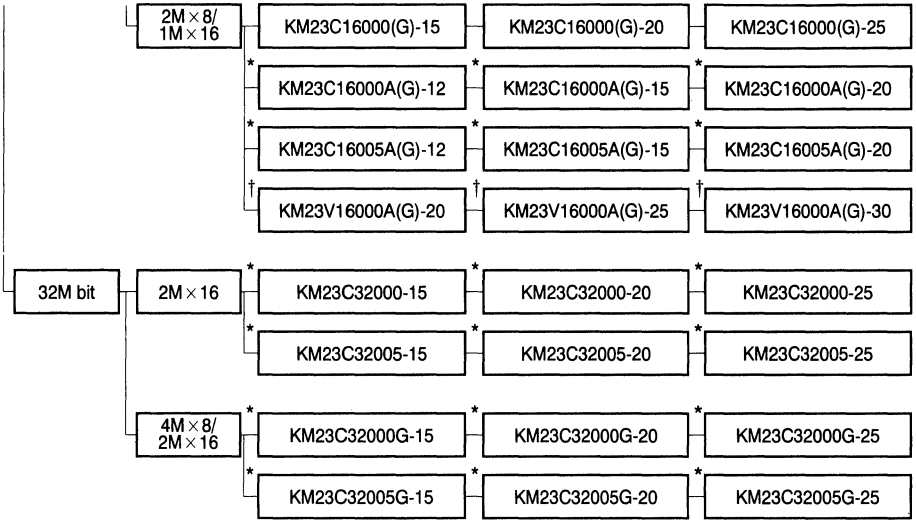


512K×8/ 256K×16	KM23C4100B(G/FP)-12	KM23C4100B(G/FP)-15	KM23C4100B(G/FP)-20
	KM23C4100H(FP)-10	KM23C4100H(FP)-12	KM23C4100H(FP)-15
	KM23C4200B(J)-12	KM23C4200B(J)-15	KM23C4200B(J)-20

* : New Product
† : Under Development

High Density

CMOS	8M bit	1M×8	KM23C8000A(G)-15	KM23C8000A(G)-20	KM23C8000A(G)-25
			†KM23C8000B(G)-10	*KM23C8000B(G)-12	*KM23C8000B(G)-15
			†KM23C8005B(G)-10	*KM23C8005B(G)-12	*KM23C8005B(G)-15
			†KM23V8000B(G)-15	†KM23V8000B(G)-20	†KM23V8000B(G)-25
			KM23C8001A(G)-12	KM23C8001A(G)-20	KM23C8001A(G)-20
			†KM23C8001B(G)-10	*KM23C8001B(G)-12	*KM23C8001B(G)-15
			†KM23V8001B(G)-15	†KM23V8001B(G)-20	†KM23V8001B(G)-25
		1M×8/ 512K×16	KM23C8100A(G)-15	KM23C8100A(G)-20	KM23C8100A(G)-25
			†KM23C8100B(G)-10	*KM23C8100B(G)-12	*KM23C8100B(G)-15
			†KM23C8105B(G)-10	*KM23C8105B(G)-12	*KM23C8105B(G)-15
			†KM23V8100B(G)-15	†KM23V8100B(G)-20	†KM23V8100B(G)-25
	16M bit	2M×8	*KM23C16100A-12	*KM23C16100A-15	*KM23C16100A-20
			†KM23V16100A-20	†KM23V16100A-25	†KM23V16100A-30
			*KM23C16101A-12	*KM23C16101A-15	*KM23C16101A-20
			†KM23V16101A-20	†KM23V16101A-25	†KM23V16101A-30



* : New Product
† : Under Development

SAMSUNG ELECTRONICS

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM41C256P	256K×1	70/80/100	CMOS	Fast Page	16 Pin DIP	Now
	KM41C256J	256K×1	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C256Z	256K×1	70/80/100	CMOS	Fast Page	16 Pin ZIP	Now
	KM41C257P	256K×1	70/80/100	CMOS	Nibble Mode	16 Pin DIP	Now
	KM41C257J	256K×1	70/80/100	CMOS	Nibble Mode	18 Pin PLCC	Now
	KM41C257Z	256K×1	70/80/100	CMOS	Nibble Mode	16 Pin ZIP	Now
	KM41C258P	256K×1	70/80/100	CMOS	Static Column	16 Pin DIP	Now
	KM41C258J	256K×1	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C258Z	256K×1	70/80/100	CMOS	Static Column	16 Pin ZIP	Now
	KM41C464P	64K×4	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C464J	64K×4	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C464Z	64K×4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C466P	64K×4	70/80/100	CMOS	Static Column	18 Pin DIP	Now
	KM41C466J	64K×4	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C466Z	64K×4	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
1M bit	KM41C1000CP	1M×1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CJ	1M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CZ	1M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CV	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CVR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CT	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CTR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CLP	1M×1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CLJ	1M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CLZ	1M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CLV	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CLVR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CLT	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CLTR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CSLP	1M×1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CSLJ	1M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CSLZ	1M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CSLV	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CSLVR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CSLT	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CSLTR	1M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	* KM41C1000CG	1M×1	60/70/80	CMOS	Fast Page	18 Pin PLCC	Now
	* KM41C1000CLG	1M×1	60/70/80	CMOS	Fast Page	18 Pin PLCC	Now
	* KM41C1000CSLG	1M×1	60/70/80	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C1001CP	1M×1	60/70/80	CMOS	Nibble Mode	18 Pin DIP	Now
	KM41C1001CJ	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin SOJ	Now
	KM41C1001CZ	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin ZIP	Now
	KM41C1001CV	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Forward)	Now
	KM41C1001CVR	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Reverse)	Now
	KM41C1001CT	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Forward)	Now
	KM41C1001CTR	1M×1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Reverse)	Now
	KM41C1002CP	1M×1	60/70/80	CMOS	Static Column	18 Pin DIP	Now
	KM41C1002CJ	1M×1	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM41C1002CZ	1M×1	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM41C1002CV	1M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
1M bit	KM41C1002CVR	1M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM41C1002CT	1M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM41C1002CTR	1M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C256CP	256K×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CJ	256K×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CZ	256K×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CV	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CVR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CT	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CTR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CLP	256K×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CLJ	256K×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CLZ	256K×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CLV	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CLVR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CLT	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CLTR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CSLP	256K×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CSLJ	256K×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CSLZ	256K×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CSLV	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CSLVR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CSLT	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CSLTR	256K×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C266CP	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C266CJ	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C266CZ	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C266CV	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C266CVR	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C266CT	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C266CTR	256K×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C258CP	256K×4	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM44C258CJ	256K×4	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM44C258CZ	256K×4	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM44C258CV	256K×4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM44C258CVR	256K×4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM44C258CT	256K×4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM44C258CTR	256K×4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C268CP	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C268CJ	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C268CZ	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin ZIP	Now
	KM44C268CV	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C268CVR	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C268CT	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C268CTR	256K×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Reverse)	Now
4M bit	KM41C4000BP	4M×1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM41C4000BJ	4M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000BZ	4M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000BV	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C4000BVR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C4000BT	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M bit	KM41C4000BTR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C4000BLP	4M×1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM41C4000BLJ	4M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000BLZ	4M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000BLV	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C4000BLVR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C4000BLT	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C4000BLTR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C4000BSLP	4M×1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM41C4000BSLJ	4M×1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000BSLZ	4M×1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000BSLV	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C4000BSLVR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C4000BSLT	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C4000BSLTR	4M×1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C4001BP	4M×1	60/70/80	CMOS	Nibble	20 Pin DIP	Now
	KM41C4001BJ	4M×1	60/70/80	CMOS	Nibble	20 Pin SOJ	Now
	KM41C4001BZ	4M×1	60/70/80	CMOS	Nibble	20 Pin ZIP	Now
	KM41C4001BT	4M×1	60/70/80	CMOS	Nibble	20 Pin TSOP-II(Forward)	Now
	KM41C4001BTR	4M×1	60/70/80	CMOS	Nibble	20 Pin TSOP-II(Reverse)	Now
	KM41C4001BV	4M×1	60/70/80	CMOS	Nibble	20 Pin TSOP-I(Forward)	Now
	KM41C4001BVR	4M×1	60/70/80	CMOS	Nibble	20 Pin TSOP-I(Reverse)	Now
	KM41C4002BP	4M×1	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM41C4002BJ	4M×1	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM41C4002BZ	4M×1	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM41C4002BT	4M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM41C4002BTR	4M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM41C4002BV	4M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM41C4002BVR	4M×1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	* KM41V4000BP	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM41V4000BJ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM41V4000BZ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM41V4000BT	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM41V4000BTR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now
	* KM41V4000BV	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM41V4000BVR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
	* KM41V4000BLP	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM41V4000BLJ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM41V4000BLZ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM41V4000BLT	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM41V4000BLTR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now
	* KM41V4000BLV	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM41V4000BLVR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
	* KM41V4000BLLP	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM41V4000BLLJ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM41V4000BLLZ	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM41V4000BLLT	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM41V4000BTLLR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now
	* KM41V4000BLLV	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM41V4000BVLLR	4M×1	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
	KM44C1000BP	1M×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C1000BJ	1M×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M bit	KM44C1000BZ	1M×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000BT	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C1000BTR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C1000BV	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C1000BVR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C1000BLP	1M×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C1000BLJ	1M×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C1000BLZ	1M×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000BLT	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C1000BLTR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C1000BLV	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C1000BLVR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C1000BSLP	1M×4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C1000BSLJ	1M×4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C1000BSLZ	1M×4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000BSLT	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C1000BSLTR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C1000BSLV	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C1000BSLVR	1M×4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C1002BP	1M×4	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM44C1002BJ	1M×4	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM44C1002BZ	1M×4	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM44C1002BT	1M×4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM44C1002BTR	1M×4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C1002BV	1M×4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM44C1002BVR	1M×4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM44C1010BP	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C1010BJ	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C1010BZ	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C1010BT	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C1010BTR	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C1010BV	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C1010BVR	1M×4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C1012BP	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C1012BJ	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C1012BZ	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin ZIP	Now
	KM44C1012BT	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C1012BTR	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C1012BV	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C1012BVR	1M×4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Reverse)	Now
	* KM44V1000BP	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM44V1000BJ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM44V1000BZ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM44V1000BT	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM44V1000BTR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now
	* KM44V1000BV	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM44V1000BVR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
	* KM44V1000BLP	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM44V1000BLJ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM44V1000BLZ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM44V1000BLT	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM44V1000BLTR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
	* KM44V1000BLV	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM44V1000BLVR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
	* KM44V1000BSLP	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin DIP	Now
	* KM44V1000BSLJ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin SOJ	Now
	* KM44V1000BSLZ	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin ZIP	Now
	* KM44V1000BSLT	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Forward)	Now
	* KM44V1000BSLTR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-II(Reverse)	Now
	* KM44V1000BSLV	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Forward)	Now
	* KM44V1000BSLVR	1M×4	70/80	CMOS	Fast Page(3.3V)	20 Pin TSOP-I(Reverse)	Now
4M B/W	KM48C512AJ	512K×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM48C512AZ	512K×8	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM48C512AT	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	KM48C512ATR	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	KM48C512ALJ	512K×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM48C512ALZ	512K×8	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM48C512ALT	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	
	KM48C512ALTR	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	KM48C512ALLJ	512K×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM48C512ALLZ	512K×8	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM48C512ALLT	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	KM48C512ALLTR	512K×8	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	* KM48V512AJ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM48V512AZ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now
	* KM48V512AT	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM48V512ATR	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	* KM48V512ALJ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM48V512ALZ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now
	* KM48V512ALT	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM48V512ALTR	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	* KM48V512ALLJ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM48V512ALLZ	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now
	* KM48V512ALLT	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM48V512ALLTR	512K×8	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	KM49C512AJ	512K×9	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM49C512AZ	512K×9	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM49C512AT	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	KM49C512ATR	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	KM49C512ALJ	512K×9	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM49C512ALZ	512K×9	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM49C512ALT	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	KM49C512ALTR	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	KM49C512ALLJ	512K×9	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	KM49C512ALLZ	512K×9	60/70/80	CMOS	Fast Page	28 Pin ZIP	Now
	KM49C512ALLT	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	KM49C512ALLTR	512K×9	60/70/80	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	* KM49V512AJ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM49V512AZ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now
	* KM49V512AT	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM49V512ATR	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	* KM49V512ALJ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM49V512ALZ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
	* KM49V512ALT	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM49V512ALTR	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	* KM49V512ALLJ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin SOJ	Now
	* KM49V512ALLZ	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin ZIP	Now
	* KM49V512ALLT	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Forward)	Now
	* KM49V512ALLTR	512K×9	70/80	CMOS	Fast Page(3.3V)	28 Pin TSOP-II(Reverse)	Now
	KM416C256AJ	256K×16	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM416C256AZ	256K×16	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM416C256AT	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM416C256ATR	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	KM416C256ALJ	256K×16	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM416C256ALZ	256K×16	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM416C256ALT	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM416C256ALTR	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	KM416C256ALLJ	256K×16	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM416C256ALLZ	256K×16	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM416C256ALLT	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM416C256ALLTR	256K×16	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	* KM416V256AJ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM416V256AZ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now
	* KM416V256AT	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM416V256ATR	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	* KM416V256ALJ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM416V256ALZ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now
	* KM416V256ALT	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM416V256ALTR	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	* KM416V256ALLJ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM416V256ALLZ	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now
	* KM416V256ALLT	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM416V256ALLTR	256K×16	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	KM418C256AJ	256K×18	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM418C256AZ	256K×18	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM418C256AT	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM418C256ATR	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	KM418C256ALJ	256K×18	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM418C256ALZ	256K×18	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM418C256ALT	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM418C256ALTR	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	KM418C256ALLJ	256K×18	60/70/80	CMOS	Fast Page	40 Pin SOJ	Now
	KM418C256ALLZ	256K×18	60/70/80	CMOS	Fast Page	40 Pin ZIP	Now
	KM418C256ALLT	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Forward)	Now
	KM418C256ALLTR	256K×18	60/70/80	CMOS	Fast Page	40 Pin TSOP-II(Reverse)	Now
	* KM418V256AJ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM418V256AZ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now
	* KM418V256AT	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM418V256ATR	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	* KM418V256ALJ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM418V256ALZ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now
	* KM418V256ALT	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM418V256ALTR	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	* KM418V256ALLJ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin SOJ	Now
	* KM418V256ALLZ	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin ZIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
	* KM418V256ALLT	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Forward)	Now
	* KM418V256ALLTR	256K×18	70/80	CMOS	Fast Page(3.3V)	40 Pin TSOP-II(Reverse)	Now
	* KM416C157AJ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin SOJ	Now
	* KM416C157AZ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin ZIP	Now
	* KM416C157AT	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Forward)	Now
	* KM416C157ATR	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Reverse)	Now
	* KM416C157ALJ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin SOJ	Now
	* KM416C157ALZ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin ZIP	Now
	* KM416C157ALT	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Forward)	Now
	* KM416C157ALTR	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Reverse)	Now
	* KM416C157ALLJ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin SOJ	Now
	* KM416C157ALLZ	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin ZIP	Now
	* KM416C157ALLT	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Forward)	Now
	* KM416C157ALLTR	256K×16	60/70/80	CMOS	Fast Page(2WE)	40 Pin TSOP-II(Reverse)	Now
16M	KM41C16000J	16M×1	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM41C16000T	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM41C16000TR	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM41C16000LJ	16M×1	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM41C16000LT	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM41C16000LTR	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM41C16100J	16M×1	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM41C16100T	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM41C16100TR	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM41C16100LJ	16M×1	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM41C16100LT	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM41C16100LTR	16M×1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM41C16001J	16M×1	60/70/80	CMOS	Nibble	24 Pin SOJ	Now
	KM41C16001T	16M×1	60/70/80	CMOS	Nibble	24 Pin TSOP-II(Forward)	Now
	KM41C16001TR	16M×1	60/70/80	CMOS	Nibble	24 Pin TSOP-II(Reverse)	Now
	KM41C16101J	16M×1	60/70/80	CMOS	Nibble	24 Pin SOJ	Now
	KM41C16101T	16M×1	60/70/80	CMOS	Nibble	24 Pin TSOP-II(Forward)	Now
	KM41C16101TR	16M×1	60/70/80	CMOS	Nibble	24 Pin TSOP-II(Reverse)	Now
	KM41C16002J	16M×1	60/70/80	CMOS	Static Column	24 Pin SOJ	Now
	KM41C16002T	16M×1	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Forward)	Now
	KM41C16002TR	16M×1	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Reverse)	Now
	KM41C16102J	16M×1	60/70/80	CMOS	Static Column	24 Pin SOJ	Now
	KM41C16102T	16M×1	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Forward)	Now
	KM41C16102TR	16M×1	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Reverse)	Now
	KM44C4000J	4M×4	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM44C4000T	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM44C4000TR	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM44C4000LJ	4M×4	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM44C4000LT	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM44C4000LTR	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM44C4100J	4M×4	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM44C4100T	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM44C4100TR	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM44C4100LJ	4M×4	60/70/80	CMOS	Fast Page	24 Pin SOJ	Now
	KM44C4100LT	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Forward)	Now
	KM44C4100LTR	4M×4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II(Reverse)	Now
	KM44C4002J	4M×4	60/70/80	CMOS	Static Column	24 Pin SOJ	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
	KM44C4002T	4M×4	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Forward)	Now
	KM44C4002TR	4M×4	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Reverse)	Now
	KM44C4102J	4M×4	60/70/80	CMOS	Static Column	24 Pin SOJ	Now
	KM44C4102T	4M×4	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Forward)	Now
	KM44C4102TR	4M×4	60/70/80	CMOS	Static Column	24 Pin TSOP-II(Reverse)	Now
	KM44C4010J	4M×4	60/70/80	CMOS	Static Column	24 Pin SOJ	Now
	KM44C4010T	4M×4	60/70/80	CMOS	Fast Page with WPB	24 Pin TSOP-II(Forward)	Now
	KM44C4010TR	4M×4	60/70/80	CMOS	Fast Page with WPB	24 Pin TSOP-II(Reverse)	Now
	KM44C4110J	4M×4	60/70/80	CMOS	Fast Page with WPB	24 Pin SOJ	Now
	KM44C4110T	4M×4	60/70/80	CMOS	Fast Page with WPB	24 Pin TSOP-II(Forward)	Now
	KM44C4110TR	4M×4	60/70/80	CMOS	Fast Page with WPB	24 Pin TSOP-II(Reverse)	Now
	KM44C4012J	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin SOJ	Now
	KM44C4012T	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin TSOP-II(Forward)	Now
	KM44C4012TR	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin TSOP-II(Reverse)	Now
	KM44C4112J	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin SOJ	Now
	KM44C4112T	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin TSOP-II(Forward)	Now
	KM44C4112TR	4M×4	60/70/80	CMOS	Static Column with WPB	24 Pin TSOP-II(Reverse)	Now
16M B/W	* KM48C2000J	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM48C2000LJ	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM48C2000LLJ	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM48C2100J	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM48C2100LJ	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM48C2100LLJ	2M×8	60/70/80	CMOS	Fast Page	28 Pin SOJ	Now
	* KM416C1000J	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now
	* KM416C1000LJ	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now
	* KM416C1000LLJ	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now
	* KM416C1200J	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now
	* KM416C1200LJ	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now
	* KM416C1200LLJ	1M×16	70/80	CMOS	Fast Page	42 Pin SOJ	Now

2.2 Dynamic RAM Module

Based Component	Part Number	Organization	Speed(ns)	Features	Packages	PCB height(In)	Remark
1M DRAM Base	KMM58256CN	256K×8	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM59256CN	256K×9	70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM532256CV/CVG	256K×32	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM536256C/CG	256K×36	70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM32512CV/CVG	512K×32	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM536512C/CG	512K×36	70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM536512CH	512K×36	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM540512C/CG'	512K×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM540512CM	512K×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM581000C	1M×8	60/70/80	Fast Page	S, 30 Pin SIMM	805	Now
	KMM591000C	1M×9	60/70/80	Fast Page	S, 30 Pin SIMM	805	Now
4M DRAM Base	KMM581000BN	1M×8	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM581020BN	1M×8	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM591000BN	1M×9	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM591020BN	1M×9	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM5321000BV/BVG	1M×32	60/70/80	Fast Page	S, 72 Pin SIMM	855	Now
	KMM5361000B/BG	1M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5361000BV/BVG	1M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1250	Now
	KMM5361000BH	1M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5361000B2/B2G	1M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM531003B/BG	1M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5401000B/BG	1M×40	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5401000BM	1M×40	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5322000BV/BVG	2M×32	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5362000B/BG	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1250	Now
	KMM5362000BH	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5362000B2/B2G	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5362003B/BG	2M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5402000B/BG	2M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5402000BM	2M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM584000B	4M×8	60/70/80	Fast Page	S, 72 Pin SIMM	805	Now
	KMM584020B	4M×8	60/70/80	Fast Page	S, 72 Pin SIMM	805	Now
	KMM594000B	4M×9	60/70/80	Fast Page	S, 72 Pin SIMM	805	Now
	KMM594020B	4M×9	60/70/80	Fast Page	S, 72 Pin SIMM	805	Now
	KMM5364000B/BG	4M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1290	Now
4M B/W Wide DRAM Base	KMM532256W/WG	256K×32	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM536256W/WG	256K×36	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM532512W/WG	512K×32	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM536512W/WG	512K×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
16M DRAM Base	KMM584100N	4M×8	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM594100N	4M×9	60/70/80	Fast Page	S, 30 Pin SIMM	650	Now
	KMM5324000V/VG/VP	4M×32	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5324100V/VG/VP	4M×32	60/70/80	Fast Page	S, 72 Pin SIMM	1000	Now
	KMM5364100/G	4M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5364000H	4M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1250	Now
	KMM5364100H	4M×36	60/70/80	Fast Page	S, 72 Pin SIMM	1250	Now
	KMM5404000/G	4M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5404100/G	4M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5328000V/VG/VP	8M×40	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now

2.2 Dynamic RAM Module (Continued)

Based Component	Part Number	Organization	Speed(ns)	Features	Packages	PCB height(In)	Remark
16M DRAM Base	KMM5328100V/VG/VP	8M×32	60/70/80	Fast Page	D, 72 Pin SIMM	1000	Now
	KMM5368100G	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1375	Now
	KMM5368000H/HG	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1250	Now
	KMM5368100H/HG	8M×36	60/70/80	Fast Page	D, 72 Pin SIMM	1250	Now
	KMM5816000T	16M×8	60/70/80	Fast Page	D, 30 Pin SIMM	900	Now
	KMM5816100T	16M×8	60/70/80	Fast Page	D. 30 Pin SIMM	900	Now
	KMM5916000T	16M×9	60/70/80	Fast Page	D, 30 Pin SIMM	900	Now
	KMM5916100T	16M×9	60/70/80	Fast Page	D, 30 Pin SIMM	900	Now

2.3 Static RAM

***Low Power SRAM**

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissition		Package	Remark
					Active Max(mA)	Standby Max(μA)		
64K	KM6264BL/BL-L	8K×8	70/100/120	CMOS	55	100/50	DIP/SDIP/SOP	Now
256K	KM62256BL/BL-L	32K×8	70/85/100/120	CMOS	70	100/20	DIP/SDIP/SOP/TSOP	Now
	KM62256BLI	32K×8	70/100	CMOS	70	50	DIP/SOP	Now
	KM62256BL-V	32K×8	120/240	CMOS	15	20	DIP/SDIP/SOP/TSOP	Now
	†† KM62256CL/CL-L	32K×8	55/70/80/100	CMOS	-	-	DIP/SDIP/SOP/TSOP	4Q, '93
512K	* KM68512L/L-L	64K×8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP	Now
1M	KM681000L/L-L	128K×8	70/85/100/120	CMOS	70	100/20	DIP/SOP/TSOP	Now
	KM681000AL/AL-L	128K×8	70/85/100/120	CMOS	70	100/20	DIP/SOP/TSOP	Now
	KM681000ALI/ALI-L	128K×8	70/100	CMOS	70	100/50	DIP/SOP	Now
	KM681000AL-V	128K×8	120/240	CMOS	15	20	DIP/SOP/TSOP	Now
	† KM681000BL/BL-L	128K×8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP	4Q,'93
	† KM68V1000BL/BL-L	128K×8	70/85/100/120	CMOS	40	50/10	DIP/SOP/TSOP	4Q,'93
4M	* KM684000L/L-L	512K×8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP	NOW
	† KM68V4000L/L-L	512K×8	70/85/100/120	CMOS	40	50/10	DIP/SOP/TSOP	4Q,'93

* : New Product † : Preliminary Product †† : Under Development

***Pseudo SRAM**

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissition		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	KM658128/L/L-L/LD/LD-L	128K×8	80/100/120	CMOS	70	1/0.2/0.1	DIP/SOP	Now

* : New Product † : Preliminary Product †† : Under Development

***High Speed & Ultra High Speed SRAM**

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissiption		Package	Remark
					Active Max(mA)	Standby Max(mA)		
64K	KM6465B/BL	16K×4	15/20/25	CMOS	140	1/0.1	22 SDIP	Now
	KM6466B/BL	16K×4	15/20/25	CMOS	140	1/0.1	24 SDIP/SOJ	Now
	KM6865B/BL	8K×8	15/20/25	CMOS	140	1/0.1	28 SDIP/SOJ	Now
256K	KM64258B	64K×4	15/20/25	CMOS	140	2	28 SDIP/SOJ	Now
	†† KM64258C	64K×4	15/20/25	CMOS	150	2	28 SOJ	4Q,'93
	†† KM64V258C	64K×4	15/20/25	CMOS	100	0.1	28 SOJ	1Q,'94
	† KM64B258A	64K×4	8/10/12	BiCMOS	185	20	28 SOJ	3Q,'93
	† KM64B261A	64K×4	6/7/8	BiCMOS	170	20	28 SOJ	4Q,'93
	KM64259B	64K×4	15/20/25	CMOS	140	2	28 SDIP/SOJ	Now
	KM68260B	64K×4	15/20/25	CMOS	140	2	28 SDIP/SOJ	Now
	KM68257B	32K×8	15/20/25	CMOS	150	2	28 SDIP/SOJ	Now
	KM68257BL	32K×8	15/20/25	CMOS	150	0.1	28 SDIP/SOJ	Now
	† KM68257C	32K×8	15/20/25	CMOS	165	2	28 SOJ	4Q,'93
	†† KM68V257C	32K×8	15/20/25	CMOS	100	0.1	28 SOJ	1Q,'94
	† KM68B257A	32K×8	8/10/12	BiCMOS	185	20	28 SOJ	3Q,'93
	† KM68B261A	32K×8	6/7/8	BiCMOS	170	20	32 SOJ	4Q,'93
	KM68V257	32K×8	20/25/30	CMOS	90	0.1	28 SDIP/SOJ	3Q,'93
	KM69B257A	32K×9	8/10/12	BiCMOS	185	20	32 SOJ	3Q,'93
512K	* KM616513	32K×16	15/17/20/25	CMOS	200	1	40 SOJ	NOW
	* KM616V513	32K×16	17/20/25	CMOS	120	0.1	40 SOJ	NOW
1M	KM611001	1M×1	20/25/35	CMOS	130	2	28 SDIP/SOJ	NOW
	KM641001	256K×4	17/20/25/35	CMOS	150	2	28 SDIP/SOJ	NOW
	† KM641003	256K×4	15/17/20	CMOS	170	2	32 SOJ	3Q,'93
	* KM64B1002	256K×4	8/10/12/15	BiCMOS	155	10	28 SOJ	NOW
	* KM64B1003	256K×4	8/10/12/15	BiCMOS	155	10	32 SOJ	NOW
	KM641005	256K×4	20/25/35	CMOS	150	2	32 SDIP/SOJ	NOW
	KM681001	128K×8	20/25/35	CMOS	170	2	32 SDIP/SOJ	NOW
	† KM681002	128K×8	15/17/20	CMOS	170	2	32 SOJ	3Q,'93
	* KM68B1002	128K×8	8/10/12/15	BiCMOS	165	10	32 SOJ	NOW
	† KM6161002	64K×16	15/17/20	CMOS	230	2	44 SOJ	3Q,'93
4M	† KM644002	1M×4	15/20/25	CMOS	170	3	32 SOJ	4Q,'93
	† KM684002	512K×8	15/20/25	CMOS	180	3	36 SOJ	1Q,'94
	† KM6164002	256K×16	20/25/35	CMOS	240	3	44 SOJ	1Q,'94

* : New Product † : Preliminary Product †† : Under Development

Specialty SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissition		Package	Remark
					Active Max(mA)	Standby Max(mA)		
288K	* KM79C86	32K×9	14/19/24	CMOS	190	50	44 PLCC	NOW

* : New Product † : Preliminary Product †† : Under Development

Synchronous SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissition		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	* KM741006	256K×4	10/12.5/15	CMOS	190	40	36 SOJ	NOW
	† KM791001	128K×9	12.5/15/20	CMOS	200	40	32 SOJ	4Q '93

* : New Product † : Preliminary Product †† : Under Development

2.4 Video RAM

Capacity	Part Number	Orgnization	Speed(ns)	Technology	Features	Package	Remark
256K	KM424C64	64K×4	100/120	CMOS	M/F	24Pin DIP/ZIP	NOW
512K	KM428C64	64K×8	70/80/100	CMOS	M/F	40PIN SOJ	NOW
1M	KM424C256A	256K×4	60/70/80	CMOS	M/F	28Pin ZIP/SOJ	NOW
	KM424C257	256K×4	60/70/80	CMOS	E/F	28Pin ZIP/SOJ	NOW
	KM428C128	128K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
2M	KM428C256	256K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428V256	256K×8	70/80	CMOS	E/F(3.3V)	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C257	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C258	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
4M	† KM4216C256	256K×16	60/70/80	CMOS	F/F	64Pin SSOP/TSOP-Ⅱ	2Q '94

* : New Product † : Under Development

2.5 EEPROM

Density	Part Number	Org.	Speed(ns)	Tech.	Features	Packages	Remark
256K bit	KM93C06/G/GD/I	16×16	1MHz	CMOS	Ext.-timed	8DIP/8SOP	Now
	KM93C07/G/GD/I	16×16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
1K bit	KM93C46/G/GD/I	64×16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64×16	250KHz	CMOS	3.0V-Operation	8DIP/8SOP	Now
	KM28i01	128×8	4.9145MHz	CMOS	Intelligent feature	8COP	4Q,93
2K bit	KM93C56/G/GD/I	128×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93CS56/G/GD/I	128×16	1MHz	CMOS	Data Protect	8DIP/8SOP	Now
	KM93C57/G/GD/I	128×16/256×8	1MHz	CMOS	Select Organization	8DIP/8SOP	Now
	KM93C56V/VG/VGD/I	128×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	4Q,93
	KM93C57V/VG/VGD/I	128×16/256×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	4Q,93
4K bit	KM93C66/G/GD/I	256×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93CS66/G/GD/I	256×16	1MHz	CMOS	Data Protect	8DIP/8SOP	Now
	KM93C67/G/GD/I	256×16/512×8	1MHz	CMOS	Select Organization	8DIP/8SOP	Now
	KM93C66V/VG/VGD/I	256×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	4Q,93
	KM93C67V/VG/VGD/I	256×16/512×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	4Q,93
16K bit	KM28C16/J	2K×8	150/200/250	CMOS	32B Page Mode, $\overline{D}$-P	24DIP/32PLCC	Now
	KM28C16I/JI	2K×8	150/200/250	CMOS	Industrial	24DIP/32PLCC	Now
	KM28C17/J	2K×8	150/200/250	CMOS	32B Page Mode, $\overline{D}$-P, R/$\overline{B}$	28DIP/32PLCC	Now
	KM28C17I/JI	2K×8	150/200/250	CMOS	Industrial	28DIP/32PLCC	Now
64K bit	KM28C64A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, $\overline{D}$-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, $\overline{D}$-P, T-B R-$\overline{B}$	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C64B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, $\overline{D}$-P, T-B	28DIP/32PLCC	3Q.93
	KM28C64BII/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q.93
	KM28C65B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, $\overline{D}$-P, T-B, R-$\overline{B}$	28DIP/32PLCC	3Q.93
	KM28C65BI/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q.93
256K bit	KM28C256/J	32K×8	150/200/250	CMOS	64B Page Mode, $\overline{D}$-P, T-B	28DIP/32PLCC	Now
	KM28C256I/JI	32K×8	150/200/250	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C256A/AJ	32K×8	90/120/150	CMOS	64B Page Mode, $\overline{D}$-P, T-B	28DIP/32PLCC	4Q,93
	KM28C256AI/AJI	32K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	4Q,93
1M bit	KM29C010/J/T	128K×8	100/120/150	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	Now
8M bit	KM29N8000J/T/TR	1M×8	t_R = 5 μs t_{RC} = 100ns	CMOS	256B Page Mode 4K Block Erase	28(24)SOJ 44(40)TSOP	2Q.93
16M bit	KM29N16000J/T/TR	2M×8	t_R = 5 μs t_{RC} = 80ns	CMOS	256B Page Mode Chip Erase	28(24)SOJ 44(40)TSOP	3Q.93

* $\overline{D}$-P : Data-Polling, R/$\overline{B}$: Ready/Busy, T-B : Toggle Bit

2.6 MASK ROM

Capacity	Part Number	Orgnization	Speed(ns)	Tech.	Features	Package	Remark
256K	KM23C256(G)	32K×8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
512K	KM23C512(G)	64K×8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
1M	KC23C1000	128K×8	120/150/200	CMOS	Programmable CE	28DIP	Now
	KM23C1001	128K×8	120/150/200	CMOS	Programmable OE	28DIP	Now
	KM23C1010(G)	128K×8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C1010J	128K×8	120/150/200	CMOS	Programmable CE & OE	32PLCC	Now
	KM23C1011(G)	128K×8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
2M	KM23C2000(G)	256K×8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	* KM23C2000A(G)	256K×8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C2001(G)	256K×8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	* KM23C2001A(G)	256K×8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C2100	256K×8 128K×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	Now
	* KM23C2100A	256K×8 128K×16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	Now
4M	KM23C4000B(G)	512K×8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4000H(G)	512K×8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	* KM23V4000B(G)	512K×8	150/200/250	CMOS	Programmable CE & OE,3.0V/3.3V	32DIP(32SOP)	'93.3Q
	KM23C4001B(G)	512K×8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C4001H(G)	512K×8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	* KM23V4001B(G)	512K×8	150/200/250	CMOS	Programmable OE,3.0V/3.3V	32DIP(32SOP)	'93.3Q
	KM23C4100B(G/FP)	512K×8/ 256K×16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP/ 44QFP)	Now
	KM23C4100H(FP)	512K×8/ 256K×16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	* KM23V4100B(FP)	512K×8/ 256K×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode,3.0V/3.3V	40DIP(44QFP)	'93.3Q
	KM23C4200B(J)	512K×8/ 256K×16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44PLCC)	Now
8M	KM23C8000A(G)	1K×8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	* KM23C8000B(G)	1K×8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	* KM23C8005B(G)	1K×8	100/120/150 (t_{PA}>50)	CMOS	Programmable CE & OE Page Mode	32DIP(32SOP)	Now
	† KM23V8000B(G)	1K×8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	'93.3Q
	KM23C8001A(G)	1K×8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C8001B(G)	1K×8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	† KM23V8001B(G)	1K×8	150/200/250	CMOS	Programmable OE, 3.0V/3.3V	32DIP(32SOP)	'93.3Q
	KM23C8100A(G)	1M×8/ 512K×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	Now
	* KM23C8100B(G)	1M×8/ 512K×16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode, Page Mode	42DIP(44SOP)	Now
	* KM23C8105B(G)	1M×8/ 512K×16	100/120/150 (t_{PA}>50)	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	Now
	† KM23V8100B(G)	1M×8/ 512K×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode, 3.0V/3.3V	42DIP(44SOP)	'93.3Q
16M	* KM23C16100A	2M×8	120/150/200	CMOS	Programmable CE & OE	36DIP	NOW

* : New Product † : Under Development

2.6 MASK ROM (Continued)

Capacity	Part Number	Orgnization	Speed(ns)	Tech.	Features	Package	Remark
	† KM23V16100A	2M×8	200/250/300	CMOS	Programmable CE & OE,3.0V/3.3V	36DIP	'93.4Q
	* KM23C16101A	2M×8	120/150/200	CMOS	Programmable OE	36DIP	NOW
	† KM23V16101A	2M×8	200/250/300	CMOS	Programmable OE, 3.0V/3.3V	36DIP	'93.4Q
	KM23C16000(G)	2M×8/ 1M×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	* KM23C16000A(G)	2M×8/ 1M×16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	* KM23C16005A(G)	2M×8/ 1M×16	120/150/200 (t_{PA}>50)	CMOS	Programmable CE & OE Word/Byte Mode, Page Mode	42DIP(44SOP)	NOW
	† KM23V16000A(G)	2M×8/ 1M×16	200/250/300	CMOS	Programmable CE & OE Word/Byte Mode, 3.0V/3.3V	42DIP(44SOP)	'93.4Q
32M	* KM23C32000	2M×16	150/200/250	CMOS	Programmable CE & OE	42DIP	NOW
	* KM23C32000G	4M×8/ 2M×16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	NOW
	* KM23C32005	2M×16	150/200/250 (t_{PA}>70)	CMOS	Programmable CE & OE Page Mode	42DIP	NOW
	* KM23C32005G	4M×8/ 2M×16	150/200/250 (t_{PA}>70)	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	NOW

* : New Product † : Under Development

3. CROSS REFERENCE GUIDE

3.1 DRAM

Density	Org.	Mode	Samsung	Toshiba	Hitachi	Fujitsu	NEC	Oki
256K	×1	F.Page	KM41C256	TC51256	HM51256	MB81256	μPD41256	MSM51C256
		Nibble	KM41C257	TC51257	—	MB81257	—	MSM41257
		S. Column	KM41C258	TC51258	HM51258	MB81258	—	—
	×4	F.Page	KM41C464	TC51464	HM50464	MB81464	μPD41464	MSM41464
		S. Column	KM41C466	TC51466	—	MB81466	—	—
1M	×1	F.Page	KM41C1000	TC511000	HM511000	MB81C1000	μP0421000	MSM511000
		Nibble	KM41C1001	TC511001	HM511001	MB81C1001	μP0421001	MSM511001
		S. Column	KM41C1002	TC511002	HM511002	MB81C1002	μP0421002	MSM511002
	×4	F.Page	KM44C256	TC514256	HM514256	MB81C4256	μP0424256	MSM514256
		S. Column	KM44C258	TC514258	HM514258	MB81C4258	μP0424258	MSM514258
4M	×1	F.Page	KM41C4000	TC514100	HM514100	MB814100	μPD424100	MSM514100
		Nibble	KM41C4001	TC514101	HM514101	MB814101	μPD424101	MSM514101
		S. Column	KM41C4002	TC514102	HM514102	MB814102	μPD424102	MSM514102
	×4	F.Page	KM44C1000	TC514400	HM514400	MB814400	μPD424400	MSM514400
		S. Column	KM44C1002	TC514402	HM514402	MB814402	μPD424402	MSM514402
	×8	F.Page	KM48C512	TC514800A	HM514800	MB814800A	μPD424800	—
	×9	F.Page	KM49C512	TC514900A	HM514900	—	μPD424900	—
	×16	F.Page	KM416C256	TC514170B	HM514170	MB814170A	μPD424170	—
	×18	F.Page	KM418C256	TC514280B	HM514280	—	μPD424280	—
16M	×1	F.Page	KM41C16000	TC5116100	HM5116100	MB8116100	μPD4216100	—
	×4	F.Page	KM44C4000	TC5116400	HM5116400	MB8116400	μPD4216400	—
	×8	F.Page	KM48C2000	TC5116800	HM5116800	MB8116800	μ PD4216800	—
	×16	F.Page	KM416C1000	TC5116160	HM6116160	MB8116160	μ PD4216160	—

3.2 DYNAMIC RAM MODULE

Density	Orgnization	Samsung	Toshiba	Hitachi	NEC
2M bit	256K×8(2C)	KMM58256CN	THM82500	HB56025608	—
2.3M bit	256K×9(2C)	KMM59256CN	THM92500	HB56025609	—
8M bit	1M×8	KMM581000	THM81000	HB56A18	MC-421000A8
9M bit	1M×9	KMM591000	THM91000	HB56A19	MC-421000A9
8M bit	256K×32	KMM532256	THM322500	HB56025632	—
9M bit	256K×36	KMM536256	—	—	—
16M bit	512K×32	KMM532512	THM325120	HB56051232	—
18M bit	512K×32	KMM536512	—	HB56051236	—
20M bit	512K×40	KMM540512	—	—	—
8M bit	1M×8(2C)	KMM581000AN	—	HB56G18	—
9M bit	1M×9(3C)	KMM591000AN	—	HB56G19	—
32M bit	4M×8	KMM584000	THM84000	HB56A48	MC-424100A8
36M bit	4M×9	KMM594000	THM94000	HB56A49	MC-424100A9
32M bit	1M×32	KMM5321000	THM321000	HB56D132	—
36M bit	1M×36	KMM5361000	THM5361020	HB56D236	MC-421000A36
64M bit	2M×32	KMM5322000	THM322020	HB56D232	—
72M bit	2M×36	KMM5362000	THM362020	HB56D236	MC-422000A36
40M bit	1M×40	KMM5401000	THM401020	HB56A140	—
80M bit	2M×40	KMM5402000	THM402020	—	—

3.3 Video RAM

Density	Feature	Organization	Samsung	Micron	Toshiba	NEC	Hitachi	Ti
256K	Minimum	64K×4	KM424C64	MT42C4064		μPD41264 μPD42264	HM53461(2)	TMS4461
512K	Minimum	64K×8	KM428C64					
1M	Minimum	256K×4	KM424C256 KM424C256A		TC524256 TC524256A TC524256B TC524257	μPD42273	HM534251 HM534251A	TMS44C250 SMJ44C250
		128K×8			TC528126A TC528126B		HM538121 HM538121A	
	Extended	256K×4	KM424C257		TC524258A TC524258B	μPD42274	HM534253A	
		128K×8	KM428C128		TC528128A TC528128B		HM538123A	
2M	Extended	256K×8	KM428C256	MT42C8255				
	Full	256K×8	KM428C257 KM428C258	MT42C8256 MT42C8254	TC528267	μPD482234 μPD482235	HM538253	
4M	Full	256K×32	KM4216C256	MT42C256K16A1				

3.4 EEPROM

*** Serial I/O EEPROM**

Density	Samsung	N.S	Exar	Micro Chip	SGSThomson	Catalyat	Rohm	AsahiKasai
256K	KM93C06	NM9306			ST93C06			AK93C06
	KM93C07	NM9307		ER59256				
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AK93C46
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56A	XRM93C56A				BR93C56A	AK93C57
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93CS56	NM93CS56			ST93CS56			
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AK93C67
	KM93C67			93C66		CAT35C104		
	KM93CS66	NM93CS66			ST93CS66			
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

*** Parallel EEPROM**

Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
16K	KM28C16	X2816B X2816C	DQ2816A DQ5516A	XL2816A	AT28C16		MSM28C16A	CAT28C16A
	KM28C17		DQ2817A DQ5517A	XL2817A	AT28C17			CAT28C17A
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
	KM28C64B	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65B		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
256K	KM28C256	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
	KM28C256A	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256

*** Flash Memory**

Density	Samsung	Toshiba	Seeq	Exel	Atmel	Hitachi	Oki	Catalyst
1M	KM29C010				AT29C010			
8M	KM29N8000							
16M	KM29N16000	TC5816F						

3.5 Static RAM

* Low Power SRAM

Density	Org.	Samsung	Hitachi	Sony	Toshiba	Mitsubishi	NEC
64K	8K×8	KM6264BL/BL-L	HM6264A/AL/AL-L	CXK5864B-L/B-LL	TC6565AL/AL-L	M5M5165/L	μPD4364L/L-L
256K	32K×8	KM62256BL/BL-L	HM62256A/AL/AL-L	CXK58257A/A-L/A-LL	TC55257BL/BL-L	M5M5255B/B-L/B-LL	μPD43256B/BL
512K	64K×8	KM68512L/L-L	–	–	–	–	–
1M	128K×8	KM681000L/L-L KM681000AL/AL-L	HM628128/L/L-L HM628128A/AL/AL-L	CXK581000/L CXK581001/L	TC551001L/L-L TC551001AL/AL-L	M5M51008/L –	– μPD431000A/A-L/A-LL
4M	512K×8	KM684000L/L-L	HM628512/L/L-L	CXK584000(1)-L	–	M5M5408L/LL	μPD434000/L/LL

* Pseudo SRAM

Density	Org.	Samsung	Hitachi	Toshiba	NEC	Oki	Motorola
1M	128KX8	KM658128/L/L-L/LD/LD-L	HM658128A/AL/AL-L	TC518128A/AL/AL-L	μPD428128A/AL/AL-L	MSM548128	MCM518128

* High Speed SRAM

Density	Org.	Samsung	Hitachi	Cypress	Fujitsu	Micron	Idt	Motorola	Toshiba	Sony
64K	16KX4	KM6465B	HM6288/L	CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288	TC55416	CXK5465
	16KX4 (With OE)	KM6466B	HM6289/L	CY7C166A	MB81C75	MT5C6405	IDT7189	MCM6290	TC55417	CXK5465
	8KX8	KM6865B	–	CY7C186A	MB81C78	MT5C6308	IDT7164	MCM6264	TC5588	CXK5863
256K	64KX4 (With OE)	KM64258B	–	CY7C196	–	MT5C2565	IDT61298	MCM6209	TC55465	–
	64KX4(Sep. I/O, H-Z)	KM64259B	–	CY7C191	MB81C86	–	IDT71282	–	–	–
	64KX4(Sep. I/O, L-Z)	KM64260B	–	CY7C192	–	–	IDT71282	–	–	–
	32KX8	KM68257B/L	HM63832UH/L	CY7C199	–	MT5C2568	IDT71256	MCM6206	TC55328	CXK58258B
1M	1MX1	KM611001	HM61100A/L	CY7C107	–	MT5C1001	–	–	–	–
	256KX4	KM641001	HM624256A/L	CY7C106	–	MT5C1005	IDT1028	MCM6229W	–	–
	256KX4(Sep. I/O)	KM641005	HM624257A/L	CY7C101	–	–	–	–	–	CXK541000
	128KX8	KM681001	–	CY7C108	–	MT5C1008	IDT71024	MCM6226W	–	CXK581020

*** BICMOS SRAM**

Density	Organization	Samsung	Hitachi	Cypress	Toshiba	Motorola	Idt
256K	64KX4(With OE)	KM64B258A	HM6709A	CY7B195	TC55B465	MCM6709A	IDT61B298
	32KX8	KM68B257A	HM628325H	CY7B199	TC55B328	MCM6706A	IDT71B256
	32KX9	KM69B257A	—	—	TC55B329	MCM6705A	—
1M	256KX4(With OE)	KM64B1003	—	—	—	MCM6728A	—
	128KX8	KM68B1002	HM678127UH	—	TC55B8128	MCM6726A	IDT71B024

3.6 MASK ROM

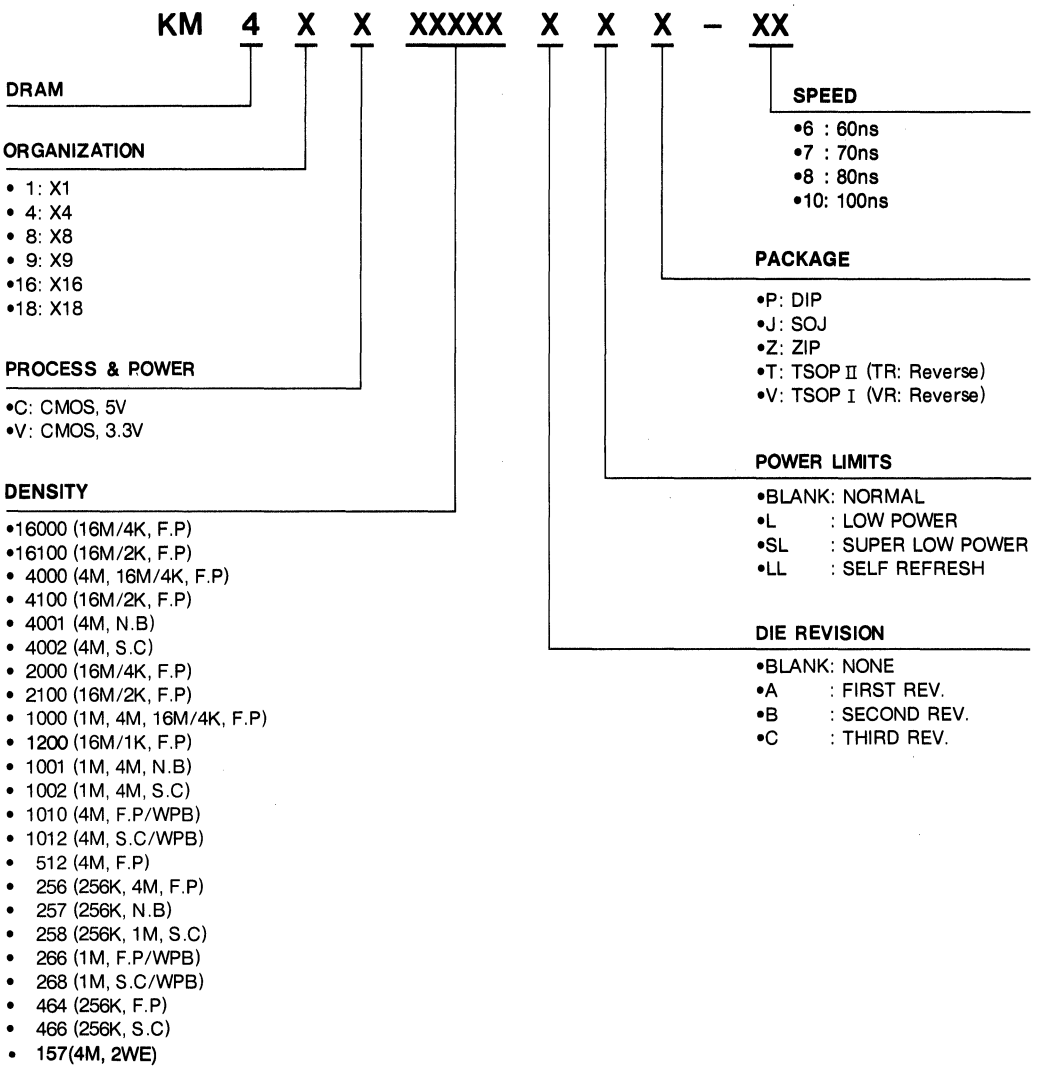
DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	KM23C256		HN623257P HN623258P		LH23255 LH53259	M5M23256P	MB83256	CXK38256
512K	KM23C512			TC53512C	LH53514 LH53515		MB83512	
1M	KM23C1000	μPD23C1000A	HN62321P HN62321BP HN62331P	TC531000C	LH231000B LH531000A	M5M23C100 M5M231000	MB831000 MB831124	CXK381000P
	KM23C1001	μPD23C1010A	HN62321EP HN62331EP	TC531001		M5M231001		
	KM23C1010	μPD23C1001E μPD23C1000E	HN62321A HN62331A		LH231100B LH530800			
	KM23C1010J KM23C1011	μPD23C1001 μPD23C100EA			LH530900			
2M	KM23C2000	μPD23C2001			LH532300 LH532100B		MB832000 MB832001	CXK382001
	KM23C2000A	μPD23C2001			LH532300 LH532100B		MB832000 MB832001	CXK382001
	KM23C2001				LH532200B LH532400			
	KM23C2001A				LH532200B LH532400			
	KM23C2100	μPD23C2000 μPD23C2000A	HN62412P HN62422P		LH532000B LH532500			
	KM23C2100A	μPD23C2000 μPD23C2000A	HN62412P HN62422P		LH532000B LH532500			
4M	KM23C4000B	μPD23C4001E	HN62304B HN62314B HN62324B HN62344B	TC534000	LH534100B	M5M23C401AP	MB834000A	CXK384001
	KM23C4000H	μPD23C4001E	HN62304B HN62314B HM62324B HN62344B	TC534000	LH534100B	M5M23C401AP	MB834000A	CXK384001
	KM23V4000B			TC534000A				
	KM23C4001B				LH534300 LH5344400		MB834000AL	
	KM23C4001H				LH534300 LH534400			
	KM23C4100B	μPD23C4000 μPD23C4000A	HN62404P HN62414P HN62424P HN62444P	TC534200	LH534000B LH534500	M5M23C400AP	MB834100A MB834200A	
	KM23C4100H	μPD23C4000 μPD23C4000A	HN62404P HN62414P HN62424P HN62444P		LH534000B LH534500		MB834100AL	
	KM23V4100B KM23C4200B							

3.6 MASK ROM (Continued)

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
8M	KM23C8000A	μPD23C8001E	HN62308B		LH538100 LH538200	M5M23801P	MB838000	CSK388000
	KM23C8000B	μPD23C8001E	HN62308B		LH538100 LH538200	M5M23801P	MB838000	
	KM23C8005B KM23V8000B KM23C8001A KM23C8001B KM23V8001B							
	KM23C8100A KM23C8100B KM23C8105B KM23V8100B	μPD23C8000 μPD23C8000	HN62408P HN62408P	TC538200 TC538200	LH538000 LH538000	M5M23800P M5M23800P	MB838200 MB838200L	
16M	KM23C16100A KM23V16100A KM23C16101A KM23V16101A							
	KM23C16000	μPD23C16000	HN624016P HN624017P	TC5316200	LH5316000	M5M23160P	MB831620P	
	KM23C16000A KM23C16005A KM23V16000A	μPD23C16000	HN624016P HN624017P	TC5316200	LH5316000	M5M23160P M5M23168P	MB831620P	
32M	KM23C32000 KM23C32005				LH5332000			

4. ORDERING INFORMATION

4.1 DRAM



4.2 DRAM MODULE

MODULE PART NUMBERING SYSTEM

KM M W WW XXXX Y Y Y Y Y Y —ZZ

MEMORY

MODULE

PIN/EDGE CONNECTOR

- •5: DRAM SIMM (EDGE CONNECTOR)
- •4: DRAM SIP (PINS)

ORGANIZATION

- •8 : X8 bits wide
- •9 : X9 bits wide
- •18 : X18 bits wide
- •32 : X32 bits wide
- •33 : X33 bits wide
- •36 : X36 bits wide
- •40 : X40 bits wide
- •144: X144 bits wide

DENSITY & MODE/FEATURE

- 16000: 16M F. Page, 4K refresh
- 16100: 16M F. Page, 2K refresh
- 8000: 8M F. Page, 4K refresh
- 8100: 8M F. Page, 2K refresh
- 4000: 4M F. Page, 1K/4K refresh
- 4001: 4M Nibble
- 4002: 4M S. Column
- 4020: 4M F. Page (Low Power)
- 4040: 4M F. Page (S. Low Power)
- 4100: 4M F. Page, 1K/2K refresh
- 1000: 1M F. Page
- 1001: 1M Nibble
- 1002: 1M S. Column
- 1020: 1M F. Page (Low Power)
- 1040: 1M F. Page (S. Low Power)
- 512: 512K Page
- 514: 512K S. Column
- 532: 512K Page (Low Power)
- 256: 256K Page
- 258: 256K S. Column
- 276: 256K Page (Low Power)

SPEED

- •5 : 50ns
- •6 : 60ns
- •7 : 70ns
- •8 : 80ns
- •10: 100ns

LEAD FINISH/SPEC CUSTOMER

—STD. MODULE
- •BLANK: SOLDER
- •G : GOLD

—CUSTOMER
- •D: DEC
- •P: APPLE
- •H: HP
- •Q: COMPAQ
- •M: IBM
- •X: CAMBEX

× 32 & × 33 ONLY PCB

- •V: ×32 & ×33 ONLY

NUMBER OF COMPONENTS

- •BLANK: MORE THAN 7 CHIPS
- •N : LESS THAN 8 CHIPS
- •W : BYTE-WORD WIDE BASE

PACKAGE (PCB) REVISION

- •BLANK: NONE
- •1 : FIRST REV.
- •2: SECOND REV.

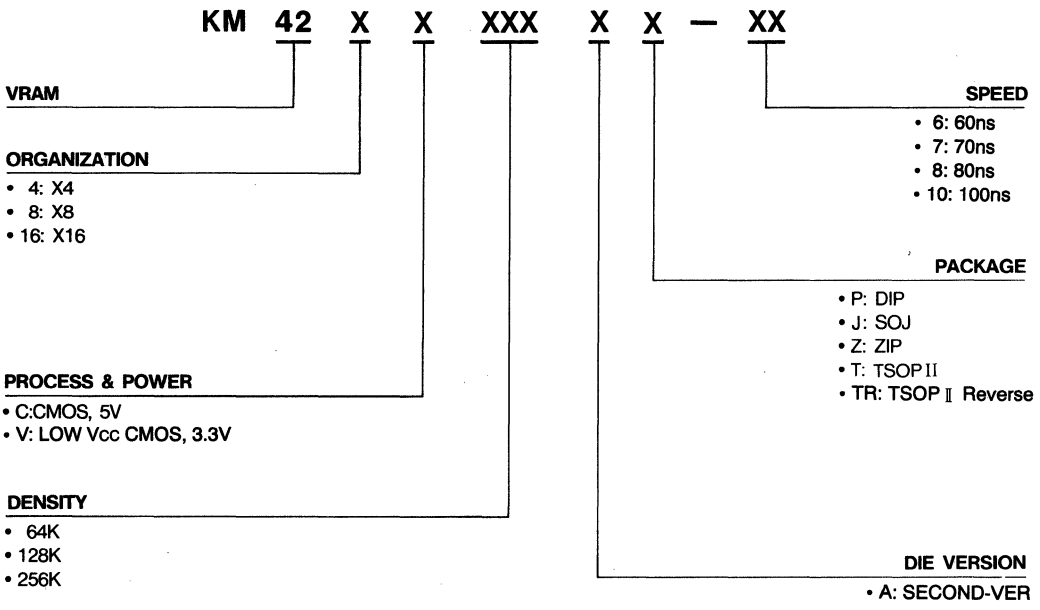
PACKAGE (COMPONENT) TYPE

- •BLANK: SOJ OR PLCC
- •*T : TSOP

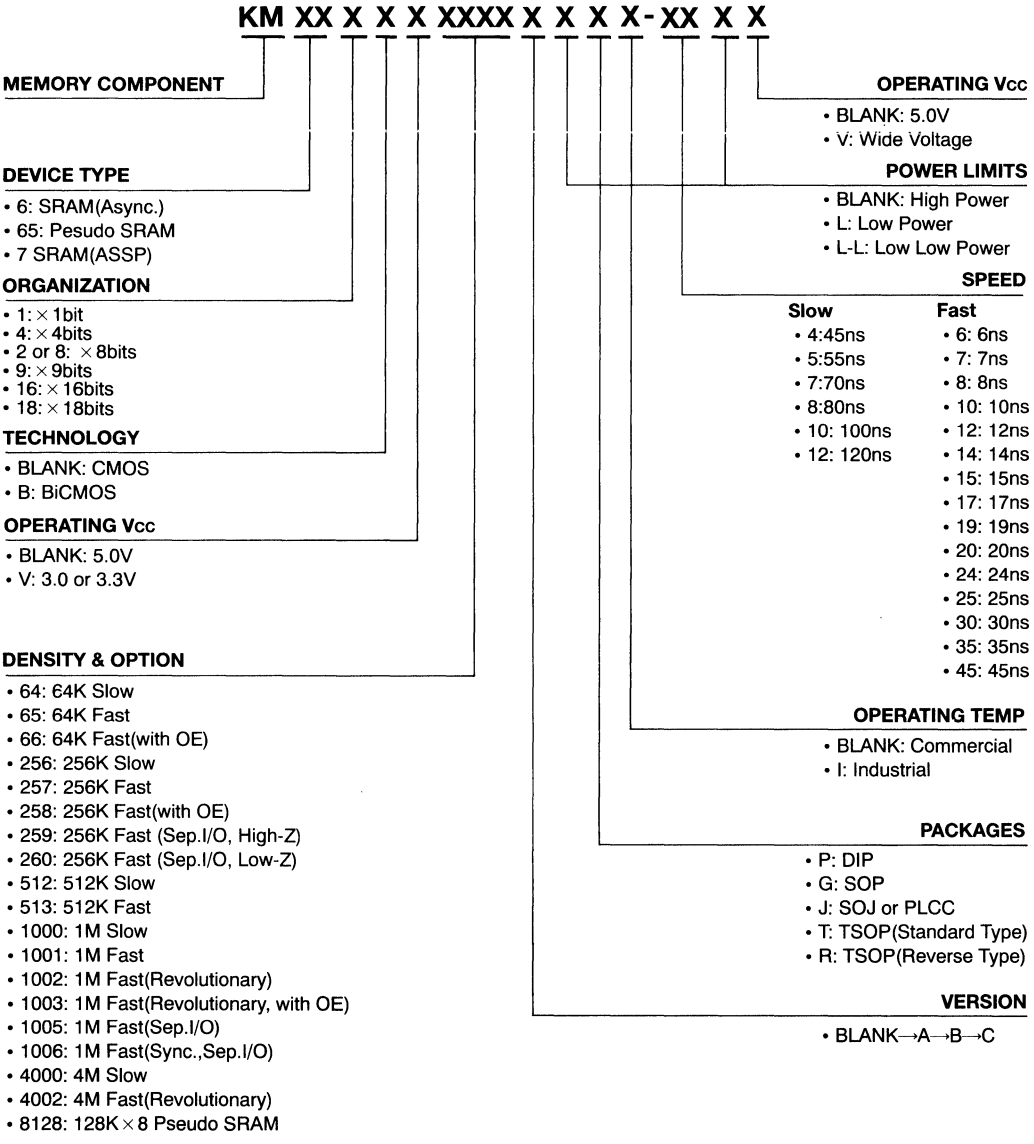
DIE (COMPONENT) REVISION

- •BLANK: NONE
- •A : FIRST REV.
- •B : SECOND REV.
- •C : THIRD REV.

4.3 VRAM

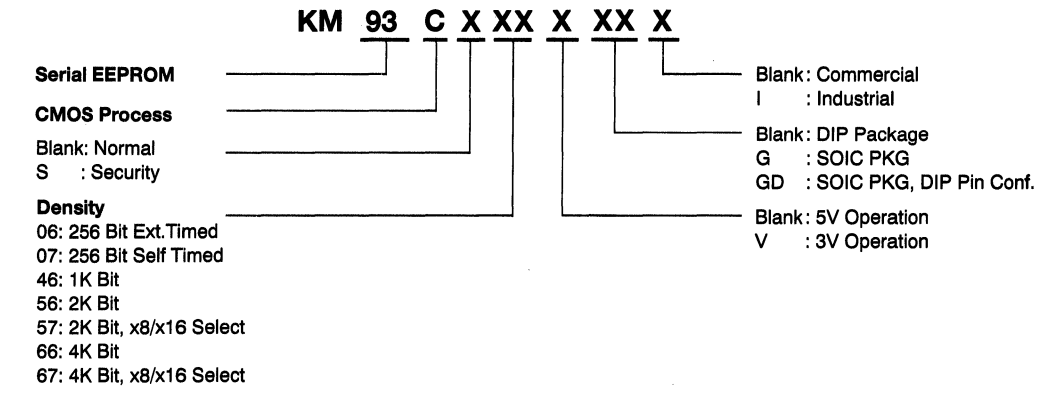

KM 42 X X XXX X X – XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
• V: LOW Vcc CMOS, 3.3V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 7: 70ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
• TR: TSOP II Reverse
DIE VERSION
• A: SECOND-VER

4.4 Static RAM

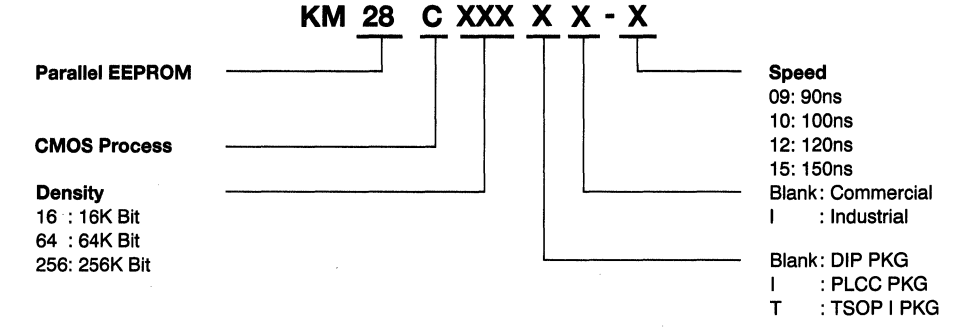


4.5 EEPROM

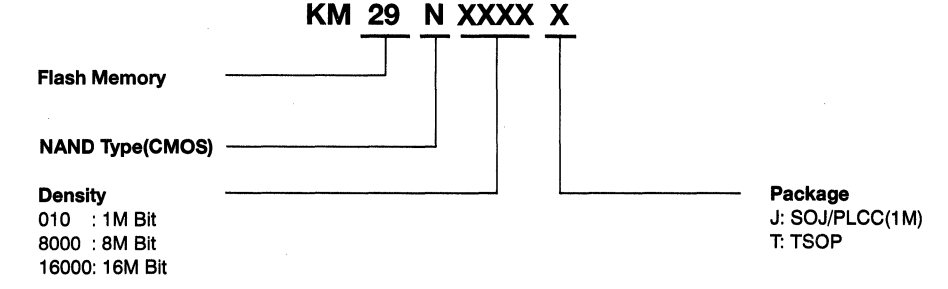
*** Serial EEPROM**



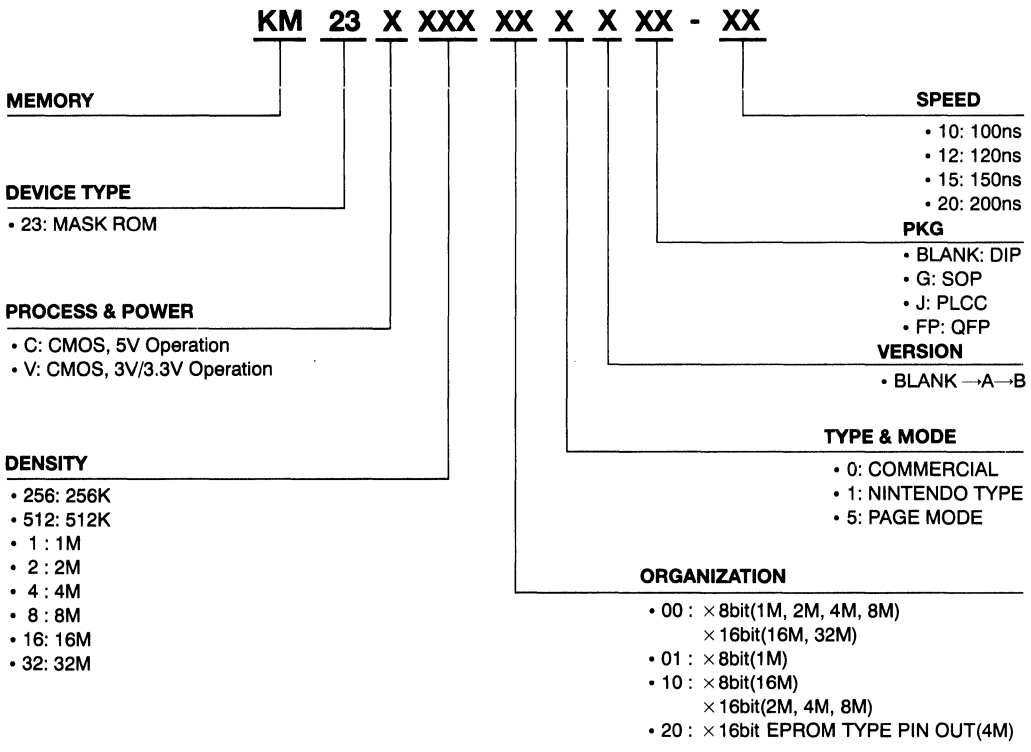
*** Parallel EEPROM**



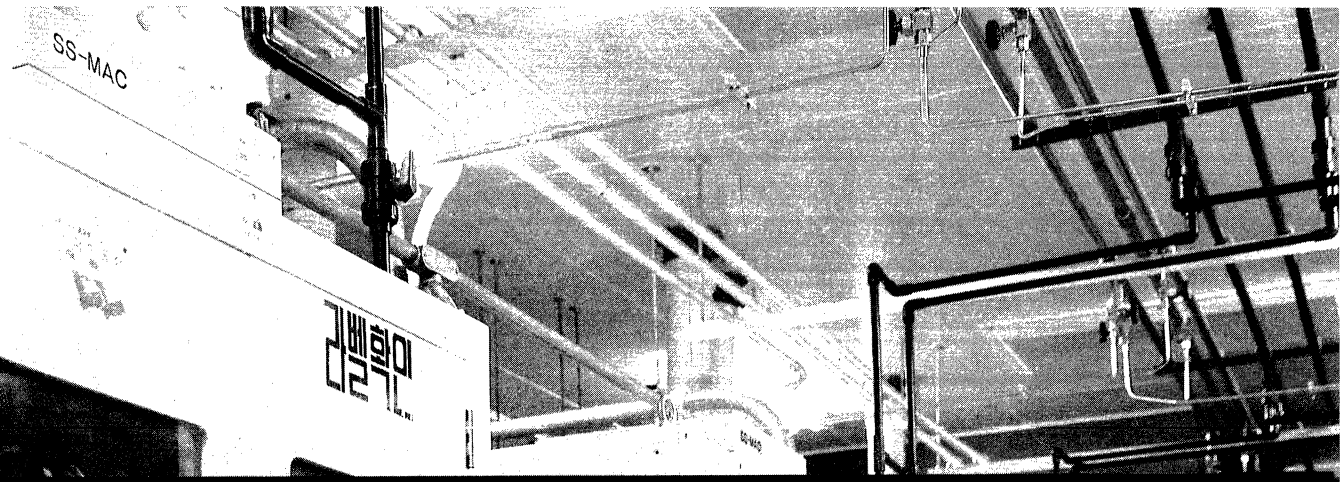
*** Flash Memory**



4.6 Mask ROM


KM 23 X XXX XX X X XX - XX
MEMORY
DEVICE TYPE
• 23: MASK ROM
PROCESS & POWER
• C: CMOS, 5V Operation
• V: CMOS, 3V/3.3V Operation
DENSITY
• 256: 256K
• 512: 512K
• 1 : 1M
• 2 : 2M
• 4 : 4M
• 8 : 8M
• 16: 16M
• 32: 32M
ORGANIZATION
• 00 : ×8bit(1M, 2M, 4M, 8M)
×16bit(16M, 32M)
• 01 : ×8bit(1M)
• 10 : ×8bit(16M)
×16bit(2M, 4M, 8M)
• 20 : ×16bit EPROM TYPE PIN OUT(4M)
TYPE & MODE
• 0: COMMERCIAL
• 1: NINTENDO TYPE
• 5: PAGE MODE
VERSION
• BLANK →A→B
PKG
• BLANK: DIP
• G: SOP
• J: PLCC
• FP: QFP
SPEED
• 10: 100ns
• 12: 120ns
• 15: 150ns
• 20: 200ns

NOTES



EEPROM DATA SHEETS 2

1. KM93C06
2. KM93C07
3. KM93C46
4. KM93C46V
5. KM93C56/KM93C66
6. KM93C56V/KM93C66V
7. KM93C57/KM93C67
8. KM93C57V/KM93C67V
9. KM93CS56/KM93CS66
10. KM28i01
11. KM28C16/KM28C17
12. KM28C64A/KM28C65A
13. KM28C64B/KM28C65B
14. KM28C256
15. KM28C256A
16. KM29C010

256-Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C06: Commercial**
  - **— KM93C06I: Industrial**
- **16 x 16 serial read/write memory**
- **High performance advanced CMOS technology**
- **Reliable floating gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3 mA (TTL)**
- **TTL compatible**
- **Available in plastic DIP and SOP**

GENERAL DESCRIPTION

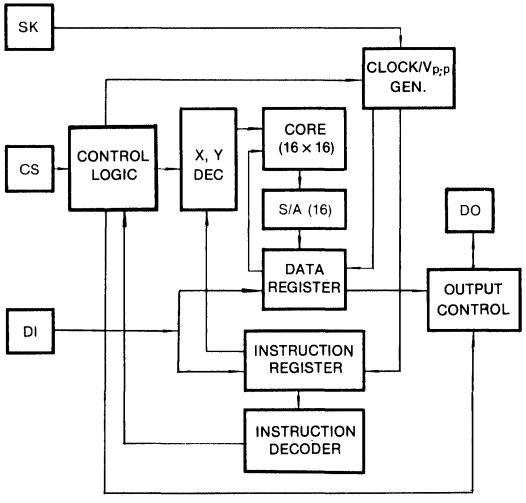
The KM93C06 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

The KM93C06 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor.

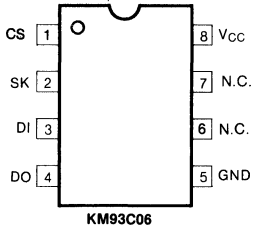
The KM93C06 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

2

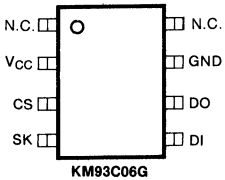
FUNCTIONAL BLOCK DIAGRAM



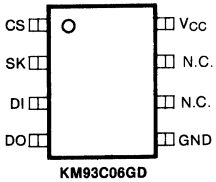
PIN CONFIGURATION



KM93C06



KM93C06G
(SC06)



KM93C06GD
(C06D)

PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C06: $T_A = 0°C$ to 70°C, Voltages referenced to V_{SS}
KM93C06I: $T_A = -40°C$ to 85°C, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C06 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

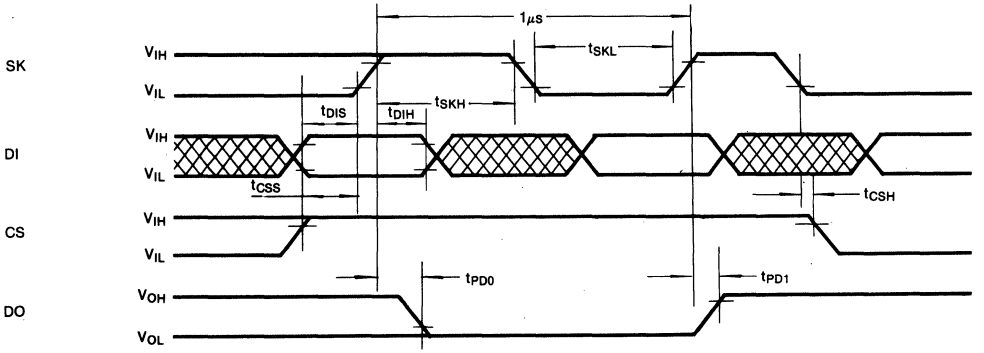
AC OPERATING CHARACTERISTICS

KM93C06: T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.
KM93C06I: T_A = −40°C to 85°C, V_{CC} = 5V ± 10%, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Program Cycle Time	$t_{E/W}$		10	30	ms
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1μs.
e.g., if t_{SKL} = 250ns then the minimum t_{SKH} = 750ns in order to meet the SK frequency specification.

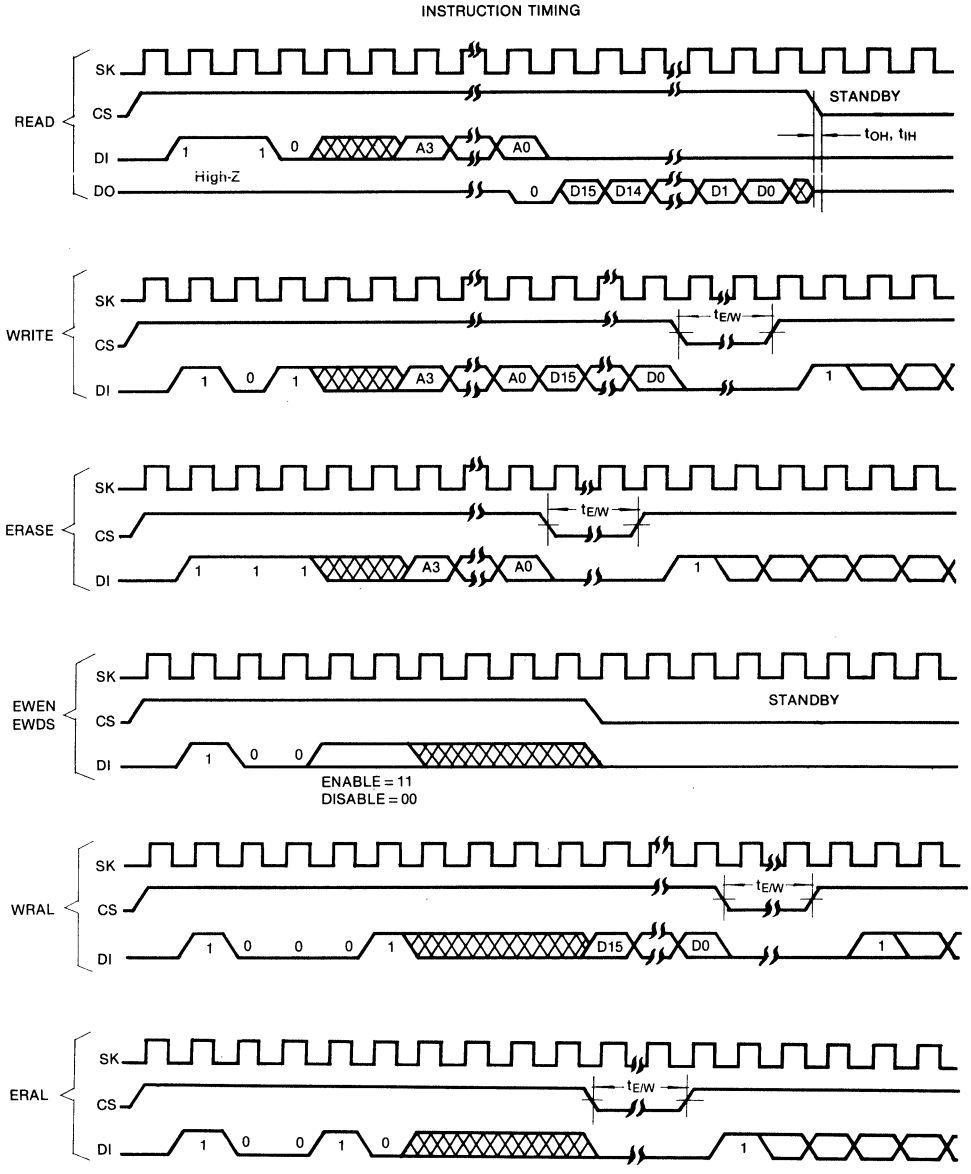
TIMING DIAGRAMS
SYNCHRONOUS DATA TIMING



DON'T CARE

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



SAMSUNG ELECTRONICS

DEVICE OPERATION

The KM93C06 is a 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. All the operations of the chip are preceded by an instruction set, consisting of a start bit and two OP code bits, facilitating inherent protection against false writes. The DO pin is in high-Z except for the read period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") preceds the 16 bit data output string.

EWEN / EWDS

The KM93C06 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. A chip starts an erase cycle by dropping CS low after an erase instruction and address set is input. The erase cycle is ended by raising CS input high after the program cycle time ($t_{E/W}$) is satisfied.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the write cycle. Like the erase operation, the write cycle is completed by the rising edge of the CS input.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

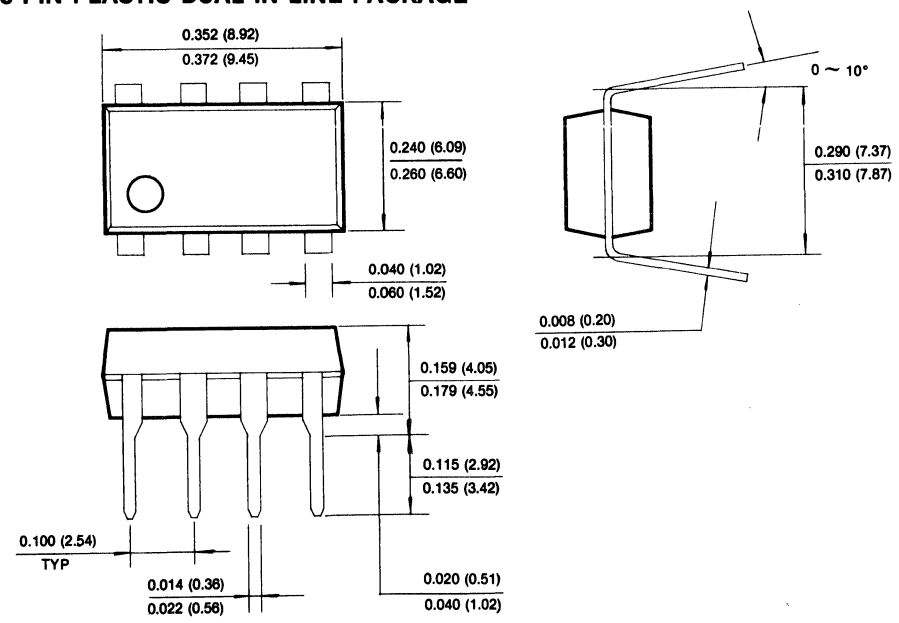
WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

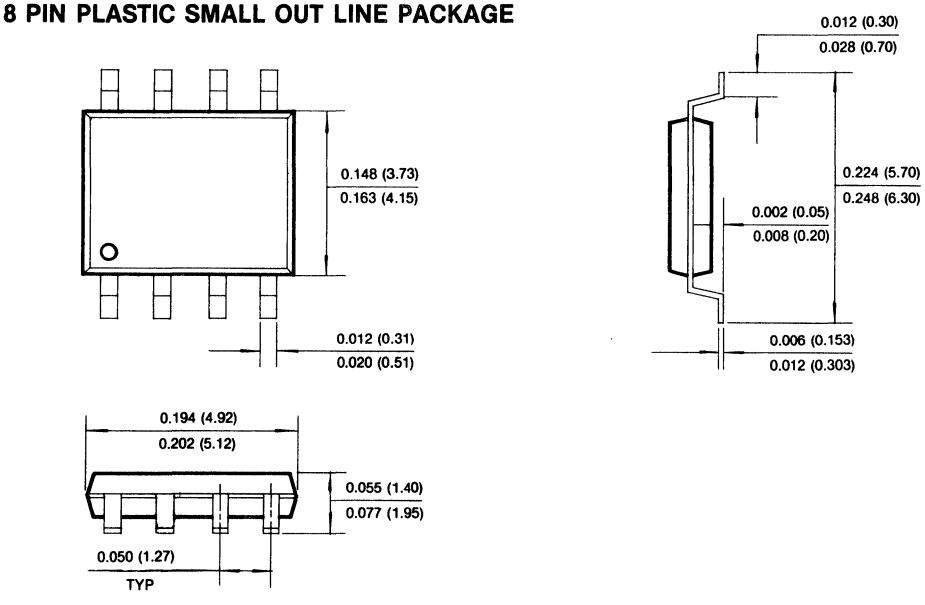
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



256-Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C07: Commercial**
  - **— KM93C07I: Industrial**
- **16 x 16 serial read/write memory**
- **High performance advanced CMOS technology**
- **Reliable floating gate technology**
  - **— Endurance : 100,000 cycle/byte**
  - **— Data retention: 10 years**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3 mA (TTL)**
- **TTL compatible**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **Available in plastic DIP and SOP**

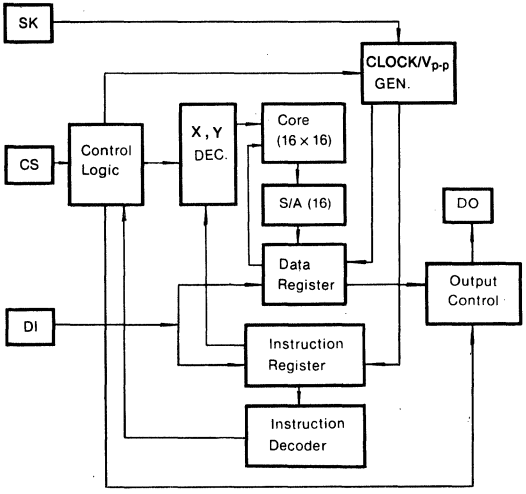
GENERAL DESCRIPTION

The KM93C07 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

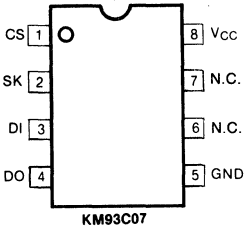
The KM93C07 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the Ready/$\overline{\text{Busy}}$ status of the device.

The KM93C07 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

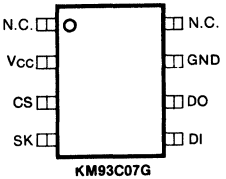
FUNCTIONAL BLOCK DIAGRAM



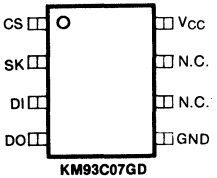
PIN CONFIGURATION



KM93C07



KM93C07G
(SC07)



KM93C07GD
(C07D)

PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

KM93C07: $T_A = 0°C$ to $70°C$, Voltages referenced to V_{SS}
KM93C07I: $T_A = -40°C$ to $85°C$, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C07 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

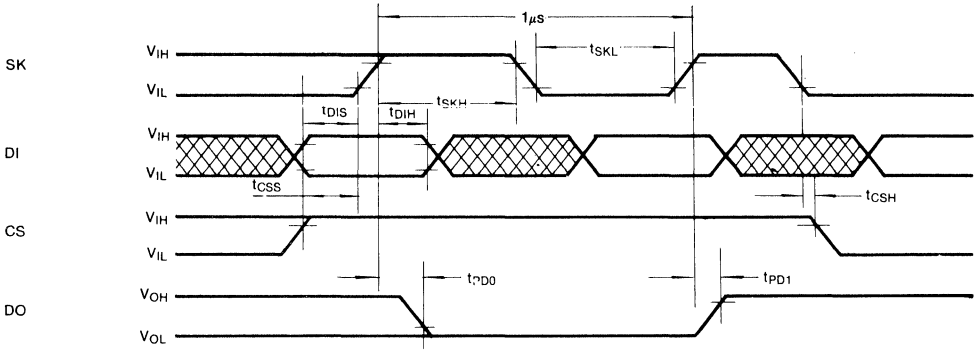
KM93C07: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM93C07I: $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		500	ns
Output Low Delay Time	t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.4V$		500	ns
Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}	(Note 2)	250		ns
Rising Edge of CS to Status Valid	t_{SV}			500	ns
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1μs.
e.q., if $t_{SKL} = 250$ns then the minimum $t_{SKH} = 750$ns in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum 250ns(t_{CS}) between consecutive instruction cycles.

TIMING DIAGRAMS

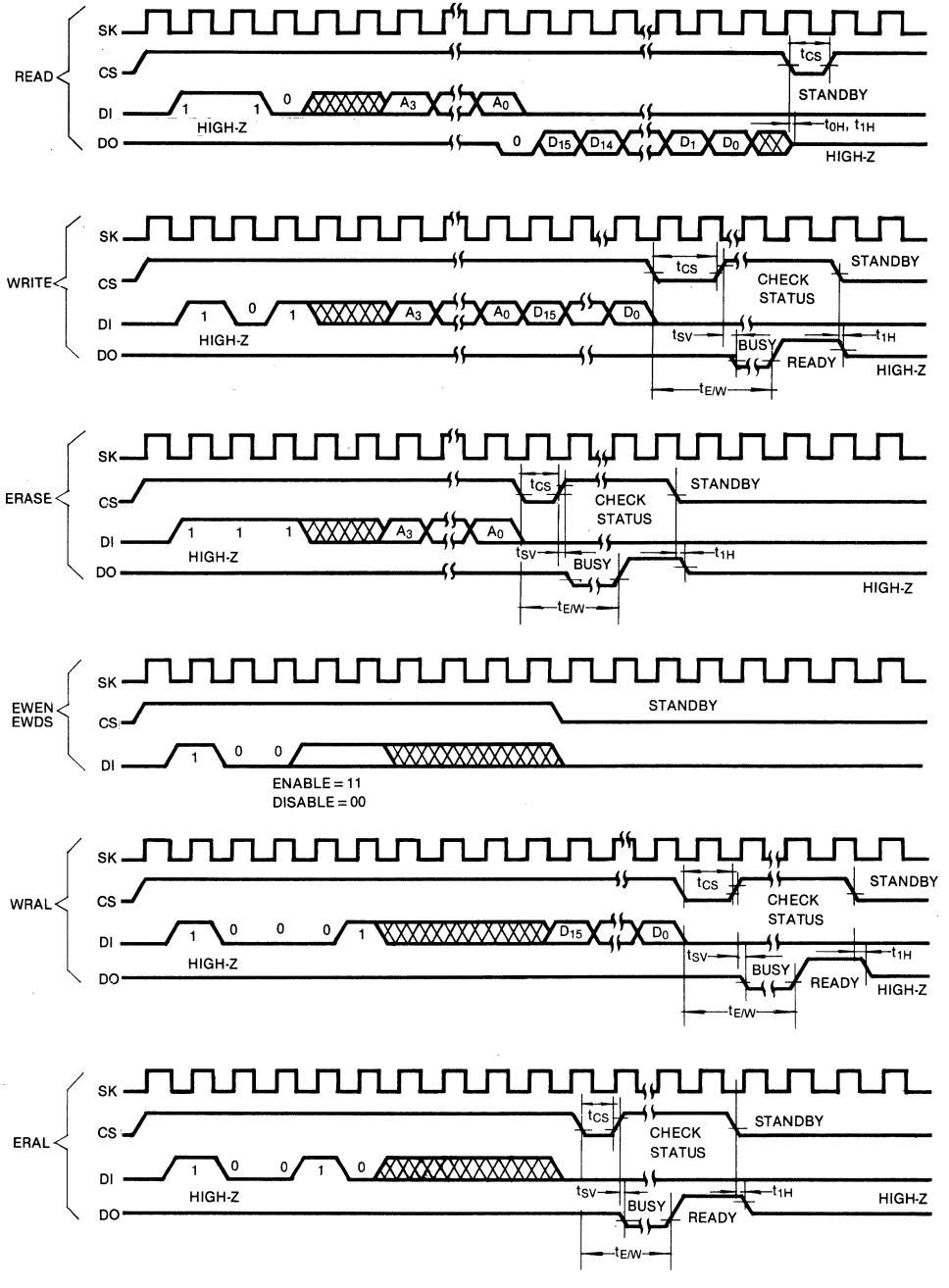
SYNCHRONOUS DATA TIMING



DON'T CARE

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



SAMSUNG ELECTRONICS

DEVICE OPERATION

The KM93C07 is a 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C07 is self-timed with the ready/busy status of the chip indicated at the DO pin. All the operations of the chip is preceded by a two OP code bits, facilitating inherent protection against false writes. The DO pin is high-Z except for the read period and the ready/busy indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C07 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts a self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/busy status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/busy function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

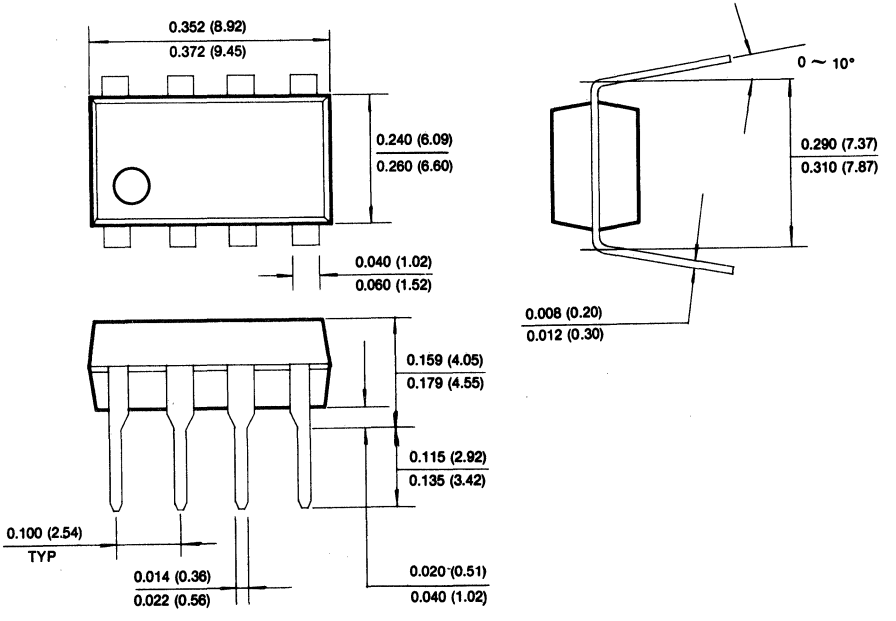
READY / BUSY

The ready/busy status of the KM93C07 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after th self-timed programming cycle has been initiated, will produces logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

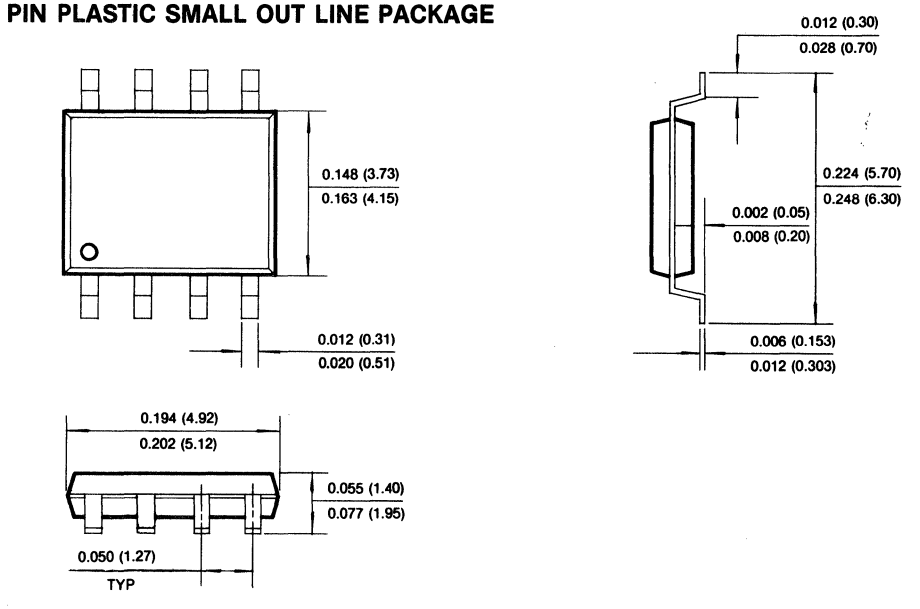
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



1K Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C46: Commercial**
  - **— KM93C46I: Industrial**
- **Single 5 Volt supply**
- **High performance advanced CMOS technology**
  - **— Reliable floating gate technology**
- **64 x 16 serial read/write memory**
- **TTL compatible**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 3 mA (TTL)**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **100,000 Cycle Endurance**
- **Available in plastic DIP and SOP**

GENERAL DESCRIPTION

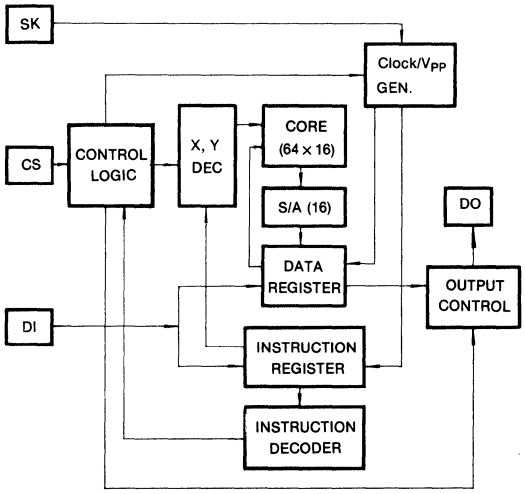
The KM93C46 is a CMOS 5V-Only 1,024 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

The KM93C46 is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

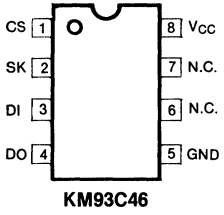
The KM93C46 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

2

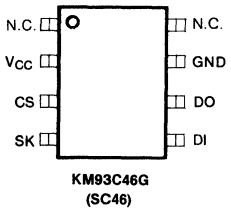
FUNCTIONAL BLOCK DIAGRAM



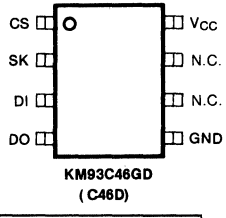
PIN CONFIGURATION



KM93C46



KM93C46G (SC46)



KM93C46GD (C46D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C46 $T_A = 0$ to 70°C, Voltages referenced to V_{SS}
KM93C46I $T_A = -40$ to 85°C, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D15-D0	Write all registers

The KM93C46 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and following 8 bits carry the OP code and the 6-bit address for 1 of 64, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

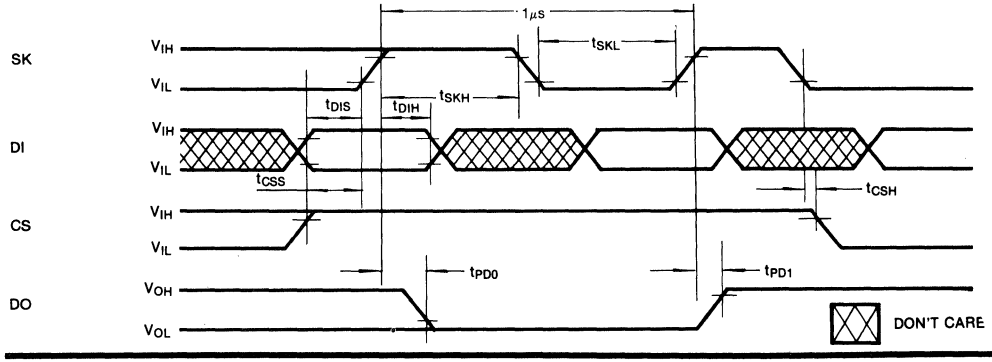
KM93C46 T_A=0°C to 70°C, V_{CC}=5V±10%, unless otherwise noted.
KM93C46I T_A=−40°C to 85°C, V_{CC}=5V±10%, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V V_{IL}=0.45V, V_{IH}=2.4V		500	ns
Output Low Delay Time	t_{PD0}			500	ns
Self-Timed Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}	(Note 2)	250		ns
Rising Edge of CS to Status Valid	t_{SV}			500	ns
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1μs.
e.q., if t_{SKL}=250ns then the minimum t_{SKH}=750ns in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum 250ns(t_{CS}) between consecutive instruction cycles.

TIMING DIAGRAMS

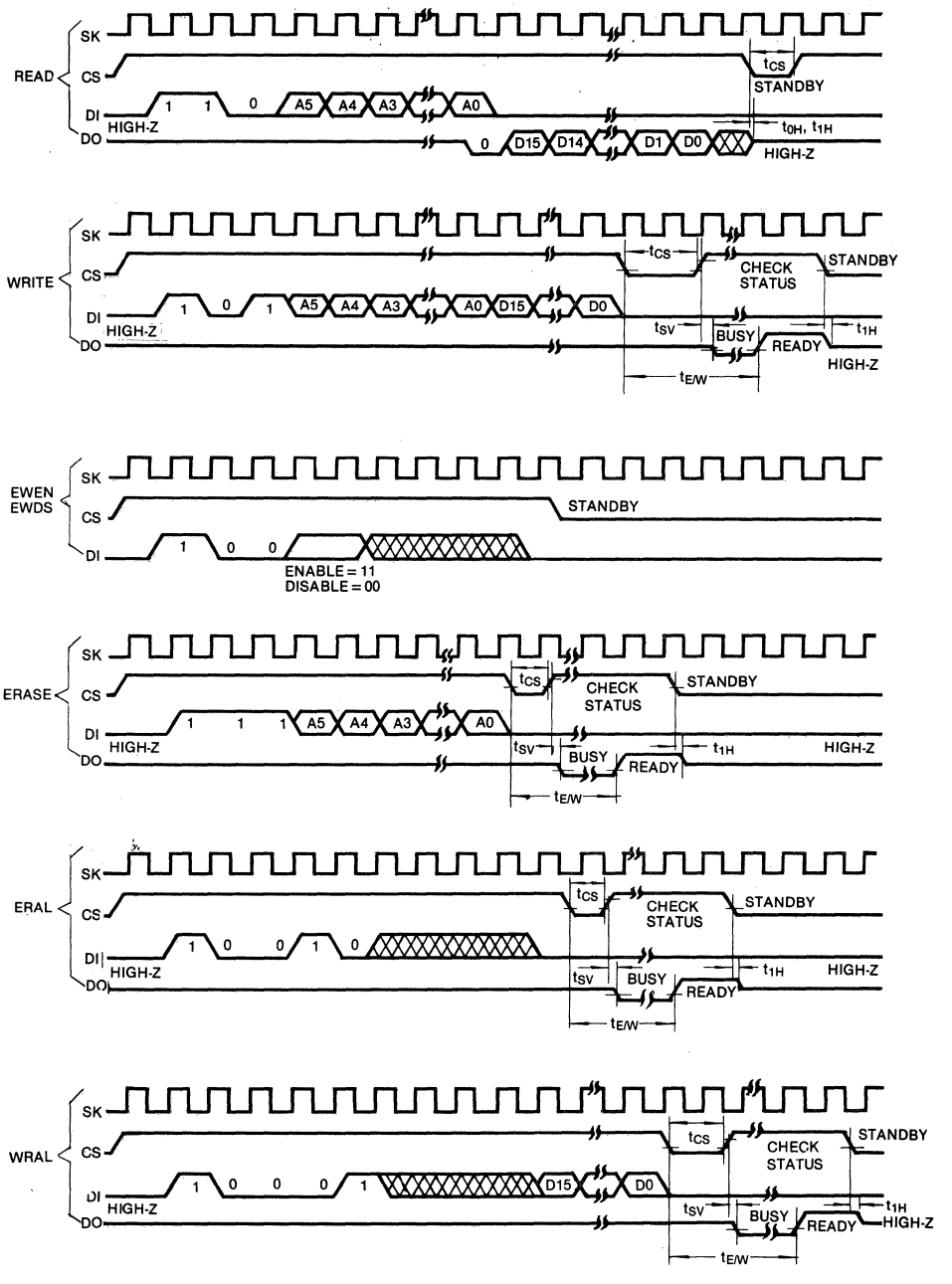
SYNCHRONOUS DATA TIMING



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



SAMSUNG ELECTRONICS

DEVICE OPERATION

The KM93C46 is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C46 is self-timed with the ready/$\overline{busy}$ status of the chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C46 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental distrubance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{busy}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array needs to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

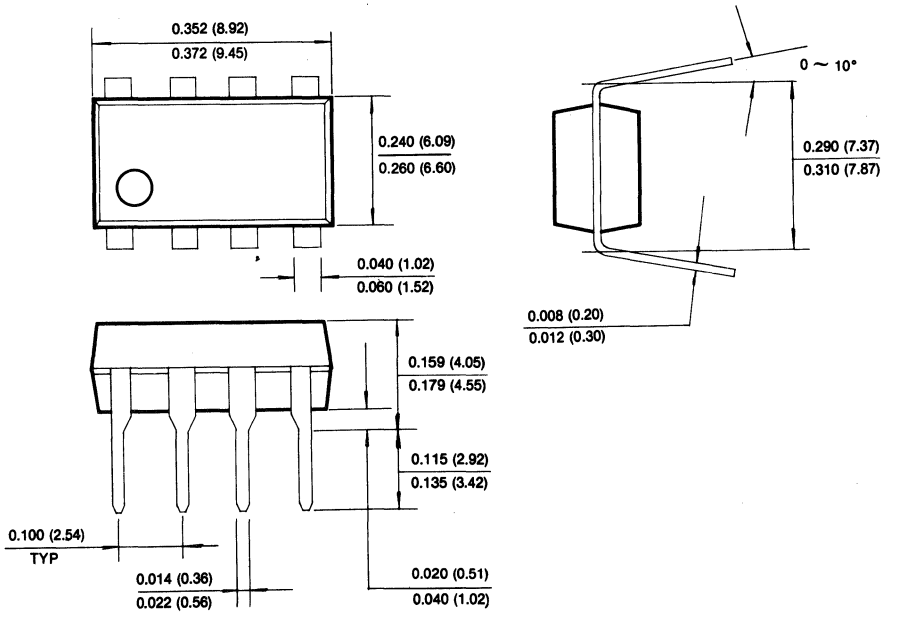
READY / $\overline{BUSY}$

The ready/$\overline{busy}$ status of the KM93C46 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after self-timed programming cycle has been initiated, will produce logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

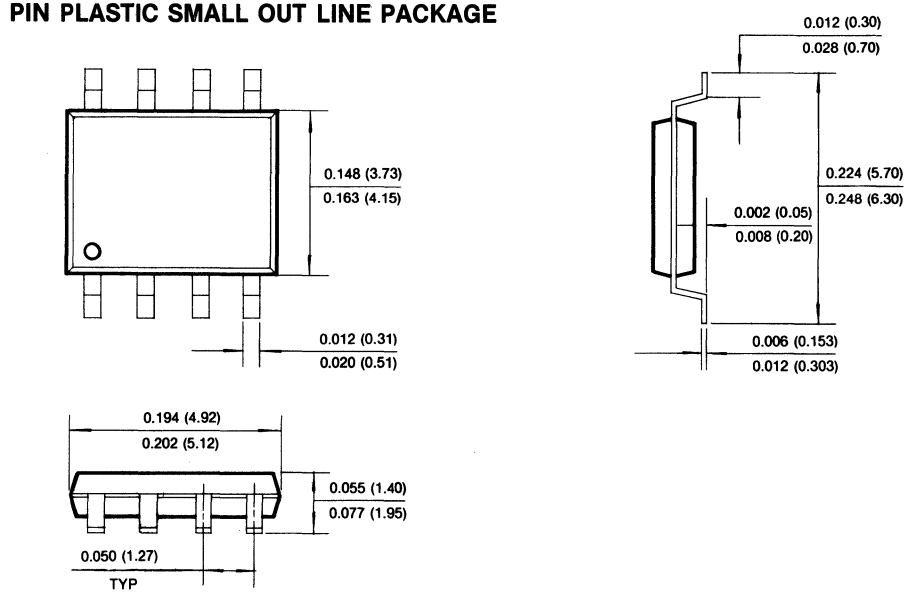
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



1K Bit Serial Electrically Erasable PROM

FEATURES

- Operating Temperature Range
  - KM93C46V : Commercial
  - KM93C46VI: Industrial
- **Enhanced extended operating voltage: 3.0V~5.5V**
- High performance Advanced CMOS Technology
  - Reliable floating gate technology
- 64 x 16 serial read/write memory
- TTL compatible
- Low power dissipation
  - **Standby current: 250μA (TTL)**
  - **Active current: 3mA (TTL)**
- Self-timed programming cycle
- Device status signal during programming
- 100,000 Cycle Endurance
- Available in plastic DIP and SOP

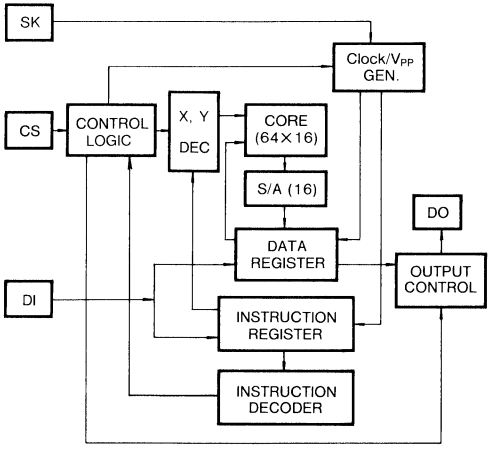
GENERAL DESCRIPTION

The KM93C46V is an extended voltage CMOS 1,024 bit nonvolatie, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

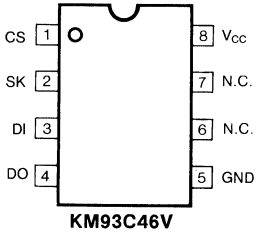
The KM93C46V is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operate in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

The KM93C46V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

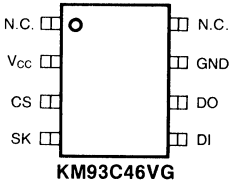
FUNCTIONAL BLOCK DIAGRAM



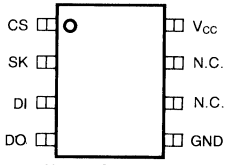
PIN CONFIGURATION



KM93C46V



KM93C46VG (C46V)



KM93C46VGD (46VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C46V: Voltage reference to V_{SS}, T_A=0°C to +70°C
KM93C46VI: Voltage reference to V_{SS}, T_A=−40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	—	5.5	V
Ground	V_{SS}	0	0	0	V

DC CHARACTERISTICS (Recommended operating conditions otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		3.0	5.5	V
Operating Current (DC)	I_{CC1}	V_{CC}=5.5V, CS=2.0V, SK=2.0V	—	1	mA
Operating Current (AC)	I_{CC2}	V_{CC}=5.5V, fsk=250KHz	—	3	mA
Standby Current (TTL)	I_{SB1}	4.5≤V_{CC}≤5.5, CS=0.8V	—	250	μA
Standby Current (CMOS)	I_{SB2}	V_{CC}=5.5V, CS=0V	—	100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 V_{CC}+0.3	V V
Output Voltage Levels (4.5≤V_{CC}≤5.5)	V_{OL1} V_{OH1}	I_{OL}=2.1mA I_{OH}=−400μA	— 2.4	0.4 —	V V
Output Voltage Levels (3.0V≤V_{CC}≤4.5)	V_{OL2} V_{OH2}	I_{OL}=10μA I_{OH}=−10μA	— 1.5	0.2 —	V V
Input Leakage Current	I_{LI}	V_{IN}=5.5V	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.5, CS=0V	—	10	μA

INDTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D_{15}-D_0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D_{15}-D_0	Write all registers

The KM93C46V provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and following 8 bits carry the OP code and the 6-bit address for 1 of 64, 16-bit registers.

AC TEST CONDITIONS

Parameter		Value
Input Pulse Levels		0.2V to 2.6V
Input Rise and Fall Times		20ns
Timing Measurement Reference Level	Input	0.8V and 2.0V
	Output	0.8V and 1.5V
Output Load		1 TTL GATE and CL=100 pF

AC OPERATING CHARACTERISTICS

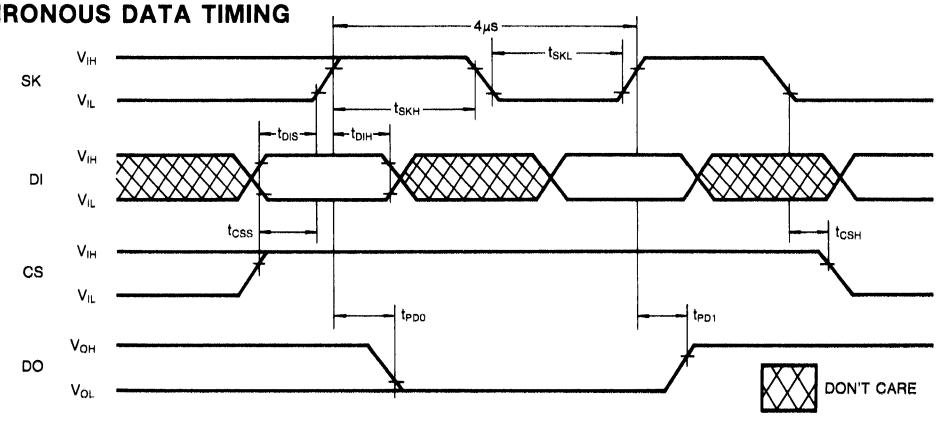
KM93C46V : T_A=0°C to +70°C
KM93C46VI: T_A=−40°C to +85°C

Parameter	Symbol	Conditions	Min	Max	Unit
SK Frequency		—	0	250	KHz
SK High Time	t_{SKH}	—	1	—	μs
SK Low Time	t_{SKL}	—	1	—	μs
Chip Select Setup Time	t_{CSS}	—	0.2	—	μs
Chip Select Hold Time	t_{CSH}	—	0	—	μs
Data Setup Time	t_{DIS}	—	0.4	—	μs
Data Hold Time	t_{DIH}	—	0.4	—	μs
Output High Delay Time	t_{PD1}	V_{OL}=0.8V, V_{OH}=1.5V	—	2	μs
Output Low Delay Time	t_{PD0}	V_{IL}=0.2V, V_{IH}=2.6V	—	2	μs
Self-Timed Program Cycle Time	$t_{E/W1}$	4.5≤V_{CC}≤5.5V	—	10	ms
	$t_{E/W2}$	3.0≤V_{CC}≤4.5	—	15	ms
Min CS Low Time	t_{CS}	—	1	—	μs
Rising Edge of CS to Status Valid	t_{SV}	—	—	1	μs
Falling Edge of CS to D_{OUT} High-Z	t_{0H}, t_{1H}	—	—	0.4	μs

Notes: 1. The SK frequency spec. specifies a minimum SK clock period of 4μs, therefore in a SK clock t_{SKH}+t_{SKL} must be greater than or equal to 4μs.
2. CS must be brought low for a minimum 1μs (t_{CS}) between consecutive instruction cycles.

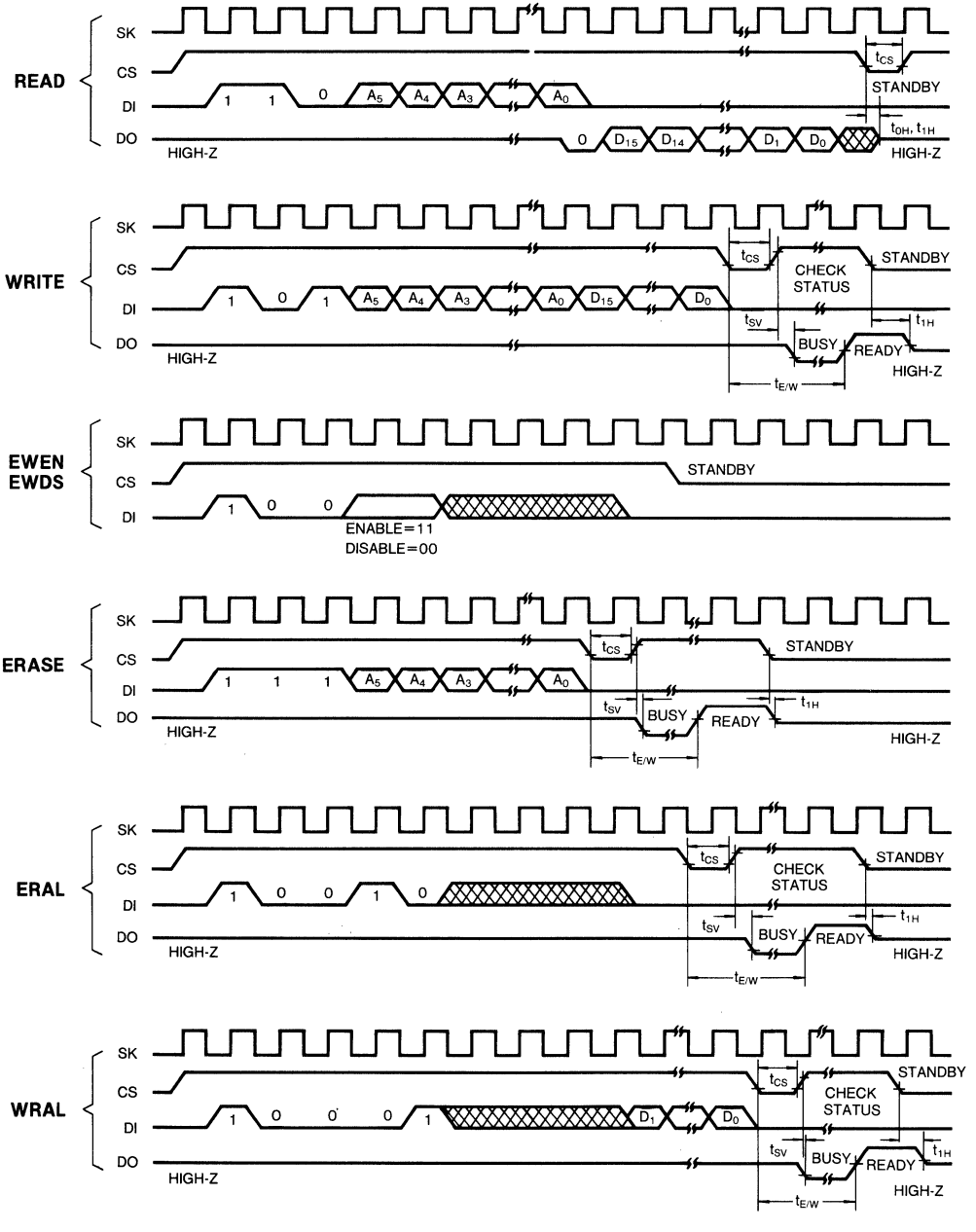
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C46V is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a 3.0V to 5.5V single power supply. The erase and write cycle of the KM93C46V is self-timed with the read/$\overline{busy}$ status of the chip indicated at the D0 pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The D0 pin is high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C46V is at the erase/write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until a erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low befor the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{busy}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e, logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is indentical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array needs to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

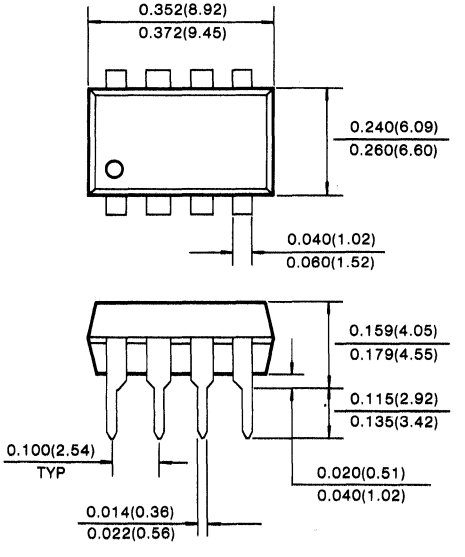
READY/$\overline{BUSY}$

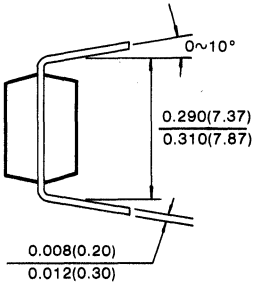
The ready/$\overline{busy}$ state of the KM93C46V during all the selftimed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after self-timed programming cycle has been initiated, will produce logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

PACKAGE DIMENSIONS

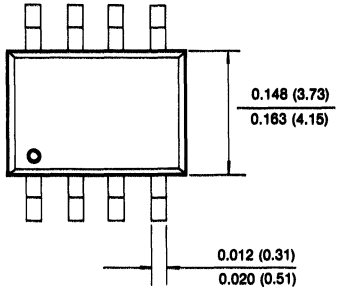
8 PIN PLASTIC DUAL IN LINE PACKAGE

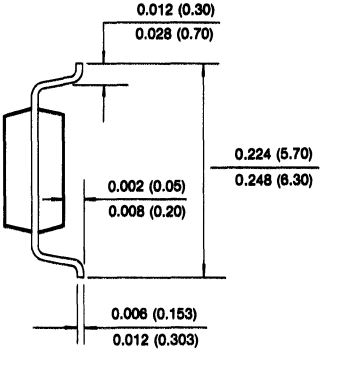
unit; inches (millimeters)

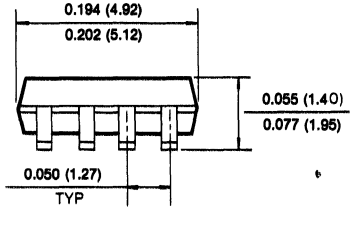




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Low power consumption**
  - **Active: 3 mA (TTL)**
  - **Standby: 250 μA (TTL)**
- **Memory organization:**
  - **128 x 16 bits for KM93C56**
  - **256 x 16 bits for KM93C66**
- **System Clock Frequency: 1 MHz (max.)**
- **Self timed write cycle**
  - **Automatic erase before write**
  - **R/B status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **Endurance : 100,000 cycle**
  - **Data retention: 10 years**

GENERAL DESCRIPTION

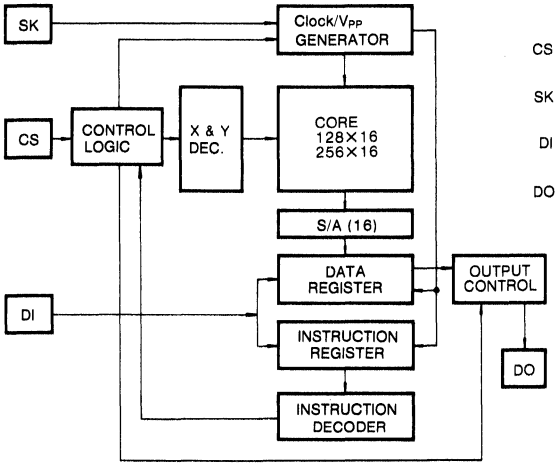
The KM93C56/66 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

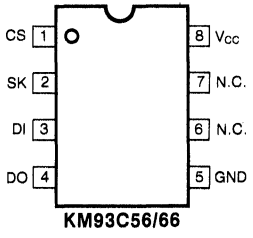
The KM93C56/66 can be organized as 128/256 registers of 16 bits each, which can be read/written serially by a microprocessor.

The KM93C56/66 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

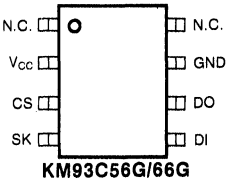
2

FUNCTIONAL BLOCK DIAGRAM

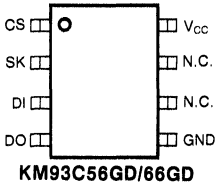




KM93C56/66



KM93C56G/66G (SC56/66)



KM93C56GD/66GD (C56D/66D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	250	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	100	μA
Input Low Voltage Levels		V_{IL}		-0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	Vcc+0.3	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A7A6A5A4A3A2A1A0	D_{OUT}	Read register at specified address
WRITE	1	01	A7A6A5A4A3A2A1A0	D_{15}-D_0	Write the data at specified address
ERASE	1	11	A7A6A5A4A3A2A1A0	—	Erase the data at specified address
EWEN	1	00	11XXXXXX	—	Erase/Write enable
EWDS	1	00	00XXXXXX	—	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	Write all registers
ERAL	1	00	10XXXXXX	—	Erase all registers

Note: 1. A7 is a "don't care" address for KM93C56.

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

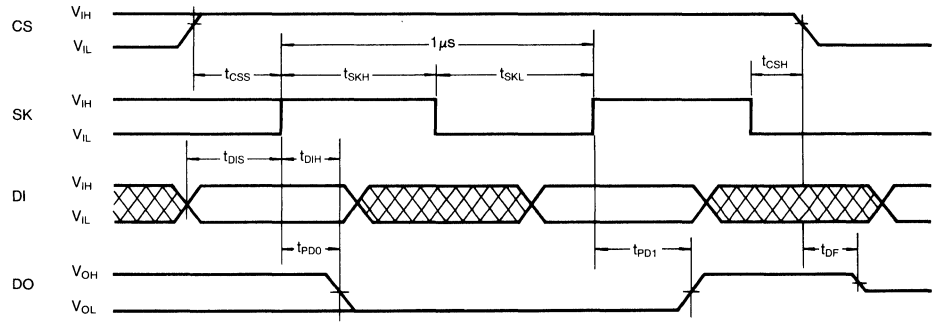
AC OPERATING CHARACTERISTICS (V_{CC}= 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output delay to data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

TIMING DIAGRAMS

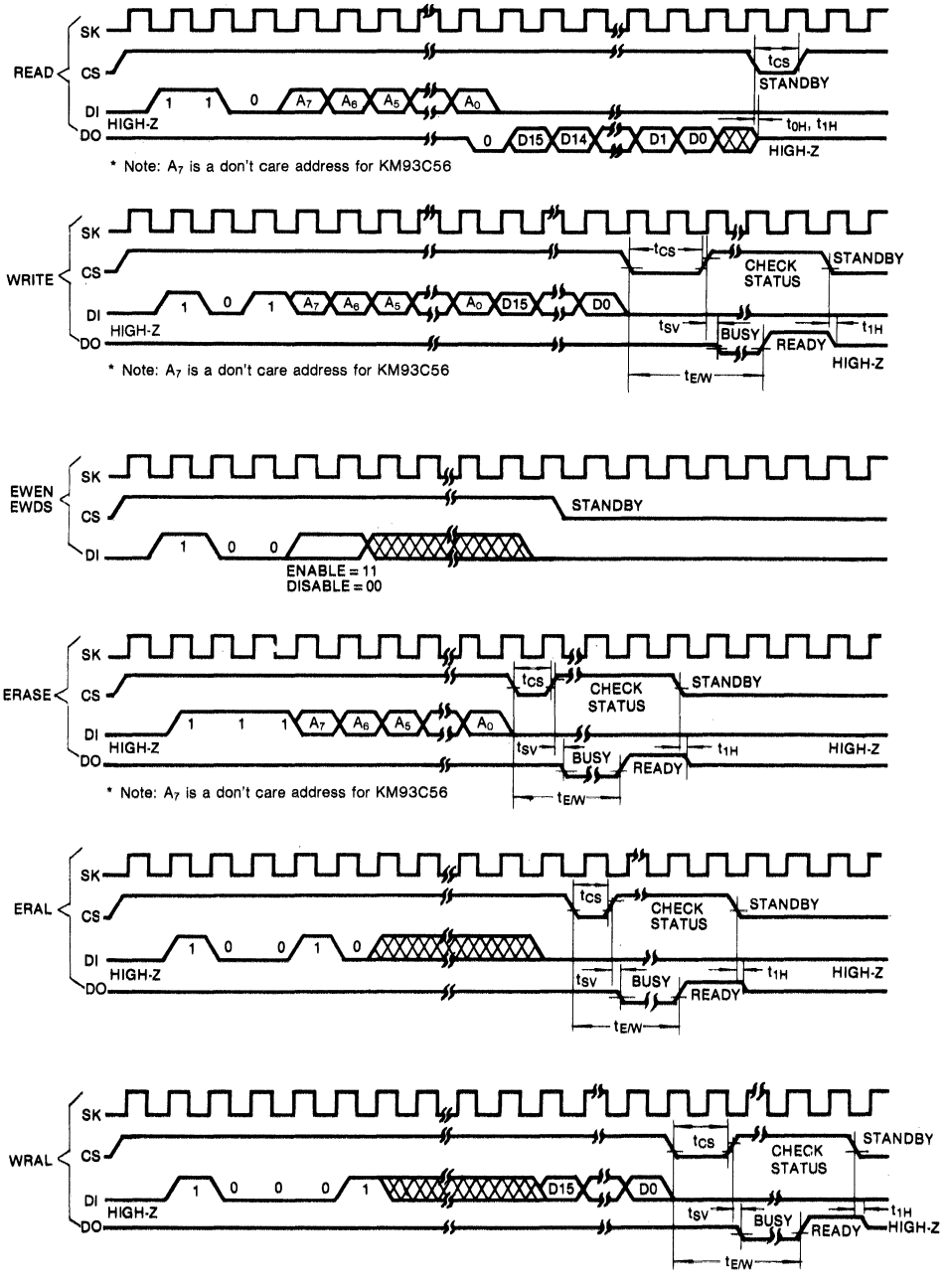
SYNCHRONOUS DATA TIMING



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



INTRODUCTION

The KM93C56/66 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93C56/66 is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C66/56 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are written simultaneously with given data.

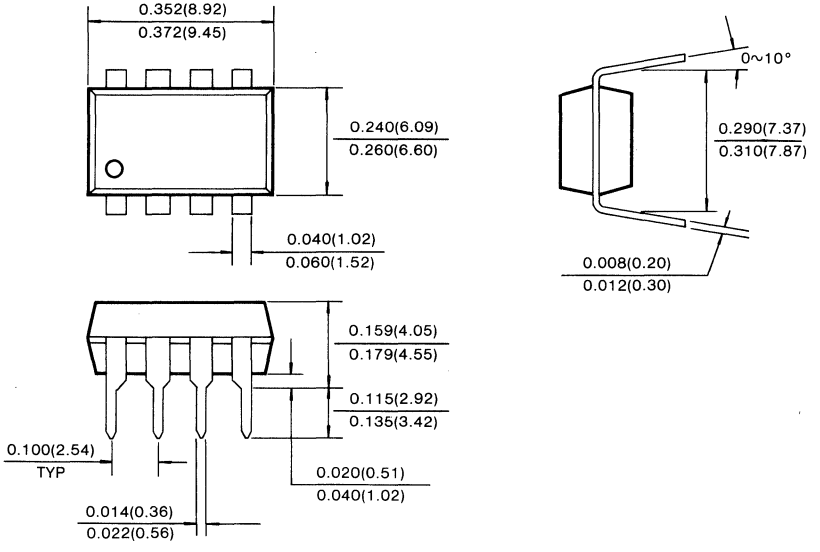
ERAL

The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

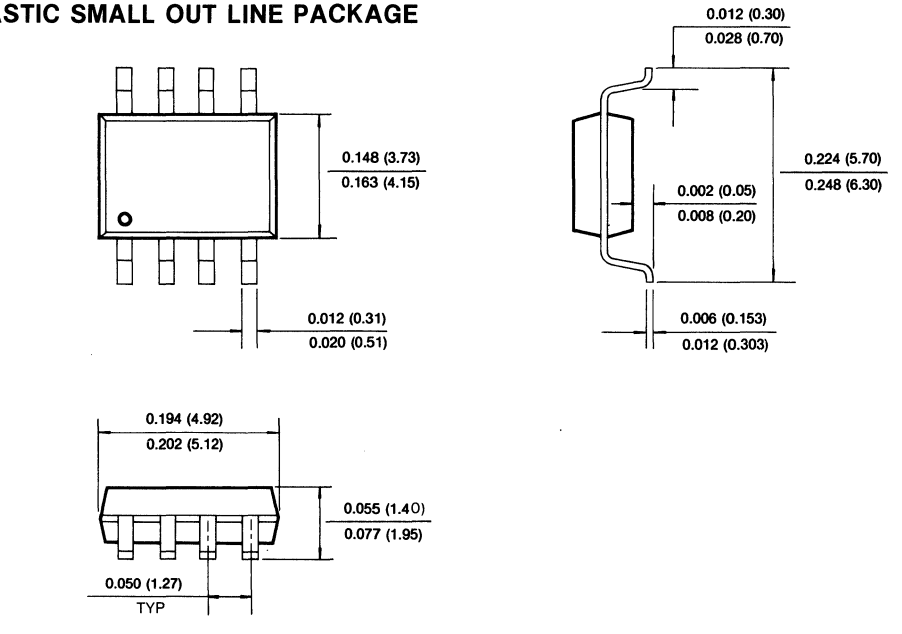
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Enhanced extended operating voltage: 3.0V~5.5V**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- Memory organization:
  - — 128 x 16 bits for KM93C56V
  - — 256 x 16 bits for KM93C66 V
- System Clock Frequency: 1 MHz (max.)
- Self timed write cycle
  - — Automatic erase before write
  - — R/B status signal during programming
- Reliable CMOS floating-gate technology
  - — Endurance : 100,000 cycle
  - — Data retention: 10 years

GENERAL DESCRIPTION

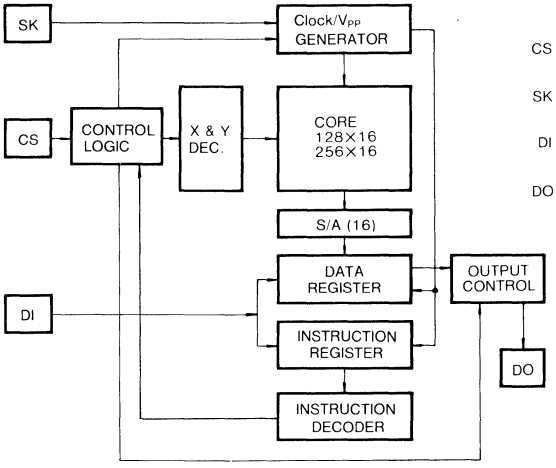
The KM93C56V/66V is a extended voltage 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

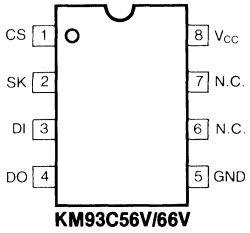
The KM93C56V/66V can be organized as 128/256 registers of 16 bits each, which can be read/written serially by a microprocessor.

The KM93C56V/66V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

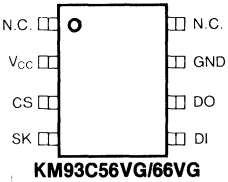
2

FUNCTIONAL BLOCK DIAGRAM

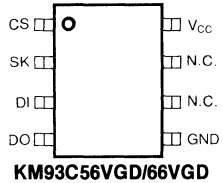




KM93C56V/66V



KM93C56VG/66VG (C56V/66V)



KM93C56VGD/66VGD (56VD/66VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	—	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		3.0	5.5	V
Operating Current	(DC)	I_{CC1}	CS = SK = V_{IH}		1	mA
	(AC)	I_{CC2}	CS = V_{IH}, SK = 1MHz		3	mA
Standby Current	(TTL)	I_{SB1}	V_{CC} = 5.5, CS = V_{IL}		250	μA
	(CMOS)	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}		100	μA
Input Low Voltage Levels		V_{IL}		−0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	V_{CC} + 0.3	V
Output Voltage Levels		V_{OL1}	I_{OL} = 2.1mA		0.4	V
(4.5<V_{CC}<5.5)		V_{OH1}	I_{OH} = −400μA	2.4		V
Output Voltage Levels		V_{OL2}	I_{OL} = 10μA		0.2	V
(3.0<V_{CC}<4.5)		V_{OH2}	I_{OH} = −10μA	2.0		V
Input Leakage Current		I_{LI}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{LO}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A7A6A5A4A3A2A1A0	D_{OUT}	Read register at specified address
WRITE	1	01	A7A6A5A4A3A2A1A0	D_{15}-D_0	Write the data at specified address
ERASE	1	11	A7A6A5A4A3A2A1A0	—	Erase the data at specified address
EWEN	1	00	11XXXXXX	—	Erase/Write enable
EWDS	1	00	00XXXXXX	—	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	Write all registers
ERAL	1	00	10XXXXXX	—	Erase all registers

Note: 1. A7 is a "don't care" address for KM93C56V.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.2V to 2.6V
Input Rise and Fall Times	20ns
Timing Measurement Reference Level	0.8V and 2.0V
Output Load	1 TTL GATE and CL = 100pF

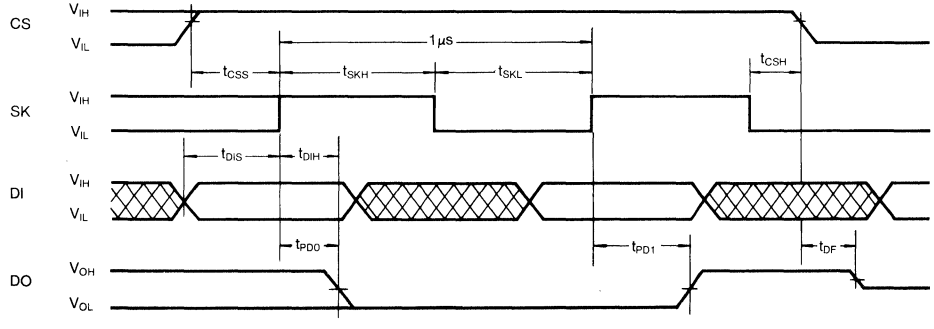
AC OPERATING CHARACTERISTICS (V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output delay to data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

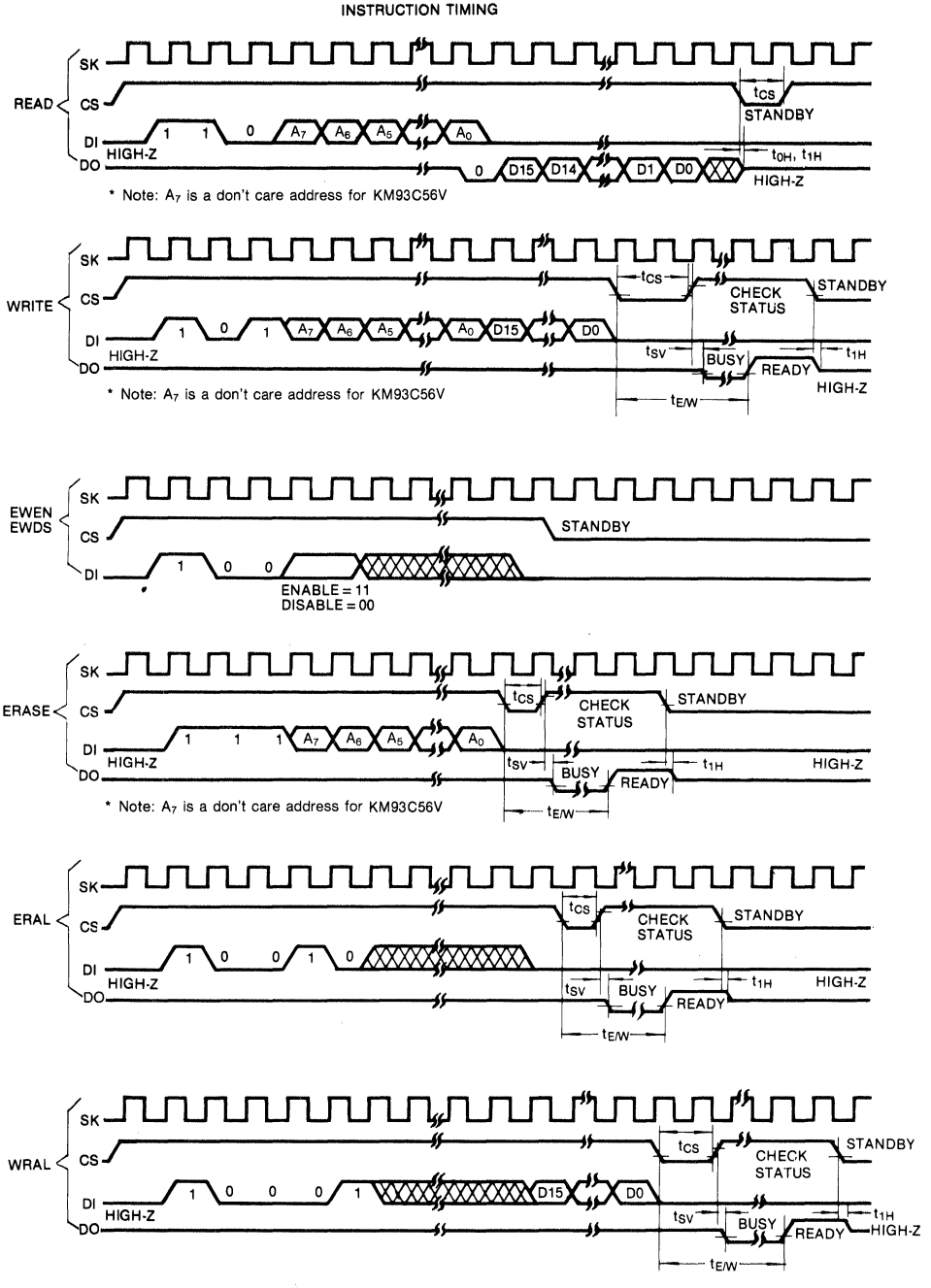
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



INTRODUCTION

The KM93C56V/66V is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a 3.0V to 5.5V single power supply. The write cycle of the KM93C56V/66V is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C56V/66V is at the write disable(EWDS) state during the power-up period to protect against accidental distubance. After the power-up period, the write operation must be preceded by an write enable(EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are written simultaneously with given data.

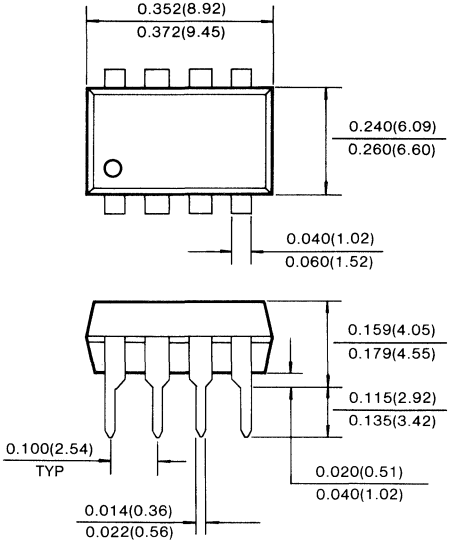
ERAL

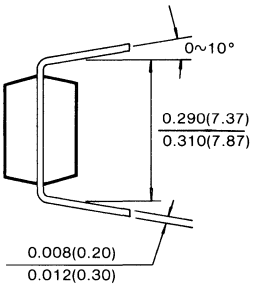
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

PACKAGE DIMENSIONS

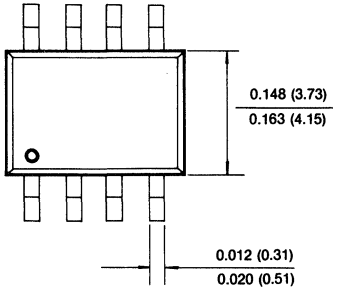
8 PIN PLASTIC DUAL IN LINE PACKAGE

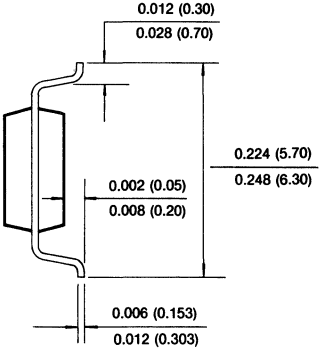
unit; inches (millimeters)

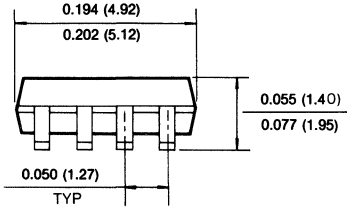




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **User selectable memory organization**
  - **— 256 x 16 or 512 x 8 for KM93C67**
  - **— 128 x 16 or 256 x 8 for KM93C57**
- **System Clock Frequency: 1 MHz (max.)**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

GENERAL DESCRIPTION

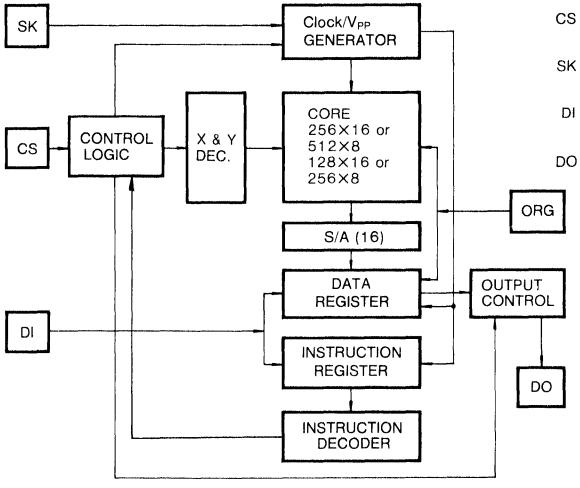
The KM93C57/67 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

The KM93C57/67 can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

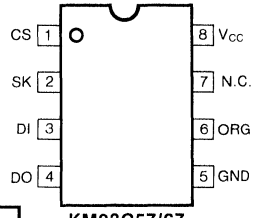
The KM93C57/67 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

2

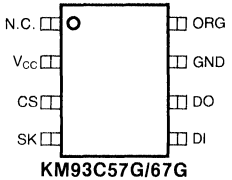
FUNCTIONAL BLOCK DIAGRAM



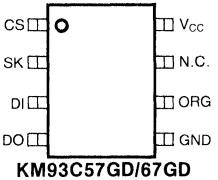
PIN CONFIGURATION



KM93C57/67



KM93C57G/67G (SC57/67)



KM93C57GD/67GD (C57D/67D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	250	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	100	μA
Input Low Voltage Levels		V_{IL}		-0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	Vcc+0.3	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

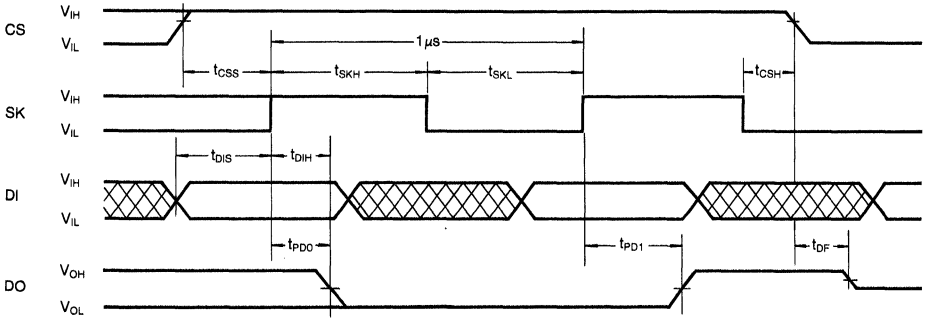
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 x 16 *(128 x 16)	512 x 8 (256 x 8)	256 x 16	512 x 8	
READ	1	10	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{OUT} (16 bit)	D_{OUT} (8 bit)	Read register at specified address
WRITE	1	01	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{15}~D_0	D_8~D_0	Write the data at specified address
ERASE	1	11	A7~A0 (A6~A0)	A8~A0 (A7~A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	D_8~D_0	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '( )' is appliable to KM93C57

TIMING DIAGRAMS

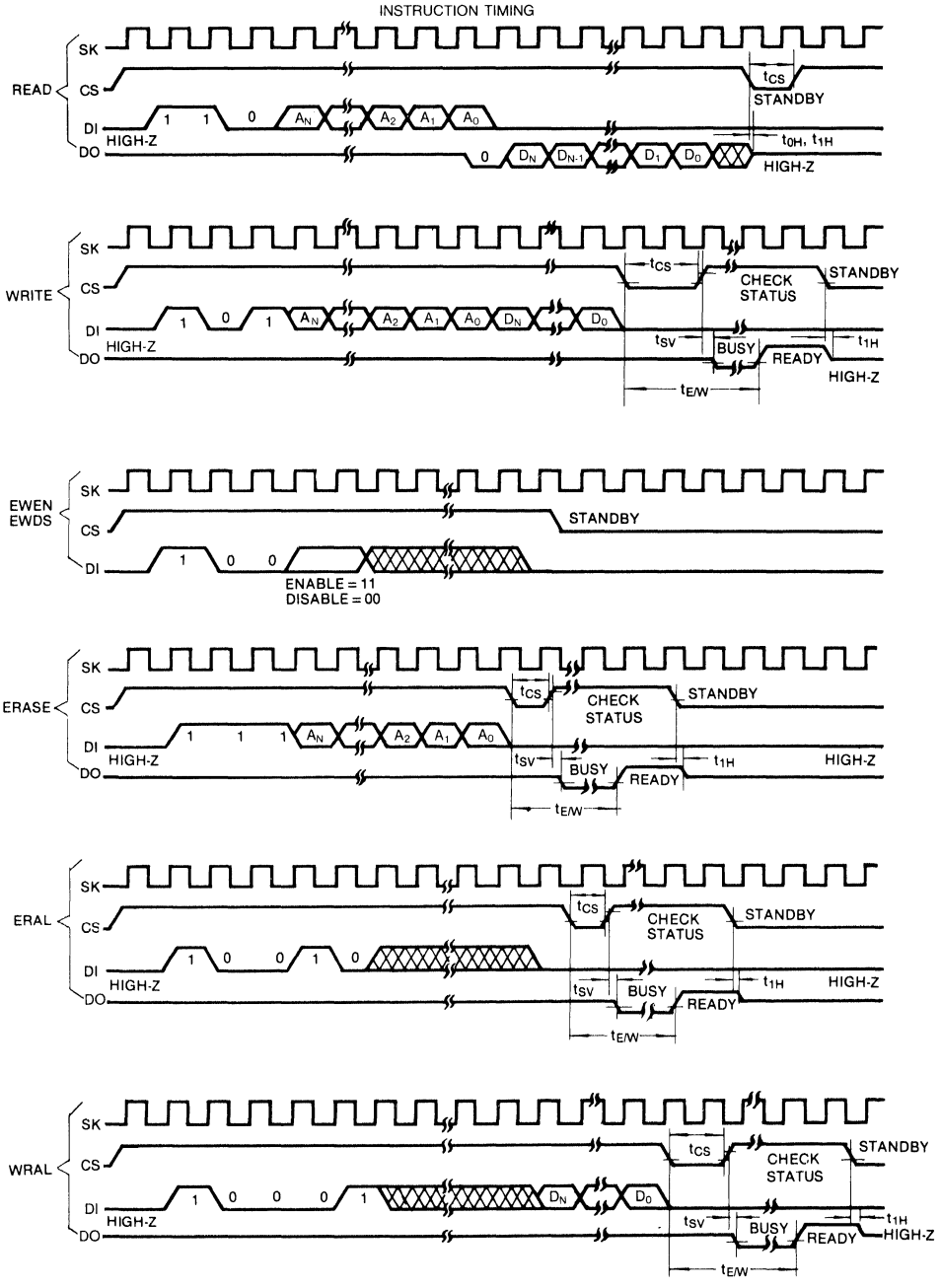
SYNCHRONOUS DATA TIMING



ORGANIZATION

P/N	Organization	AN	DN
KM93C67	512X 8	A_8	D_7
	256X16	A_7	D_{15}
KM93C57	256X 8	A_7	D_7
	128X16	A_6	D_{15}

TIMING DIAGRAMS (Continued)



INTRODUCTION

The KM93C57/67 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93C57/67 is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

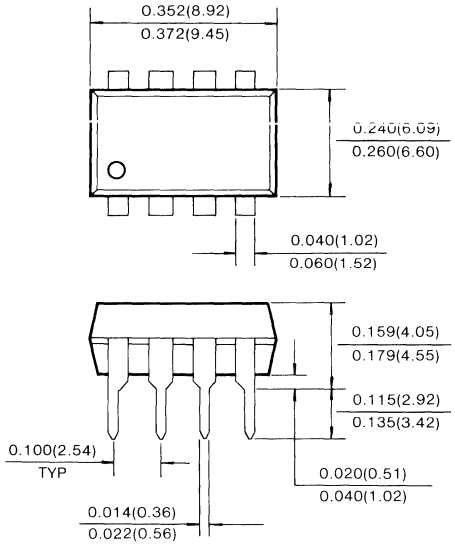
ERAL

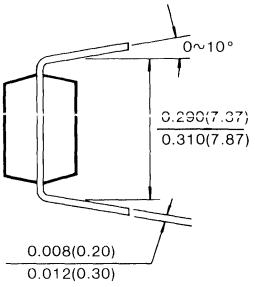
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

PACKAGE DIMENSIONS

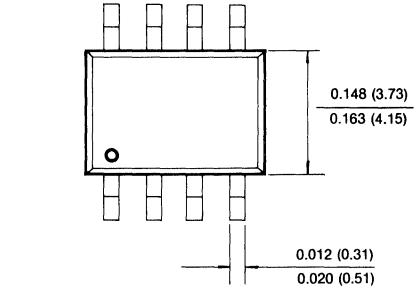
8 PIN PLASTIC DUAL IN LINE PACKAGE

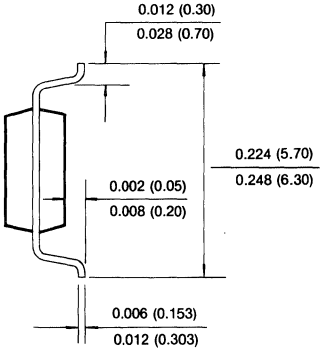
unit; inches (millimeters)

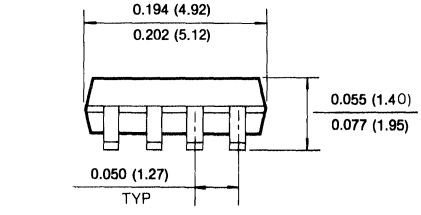




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Enhanced extended operating voltage: 3.0V~5.5V**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **User selectable memory organization**
  - **— 256 x 16 or 512 x 8 for KM93C67 V**
  - **— 128 x 16 or 256 x 8 for KM93C57 V**
- **System Clock Frequency: 1 MHz (max.)**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

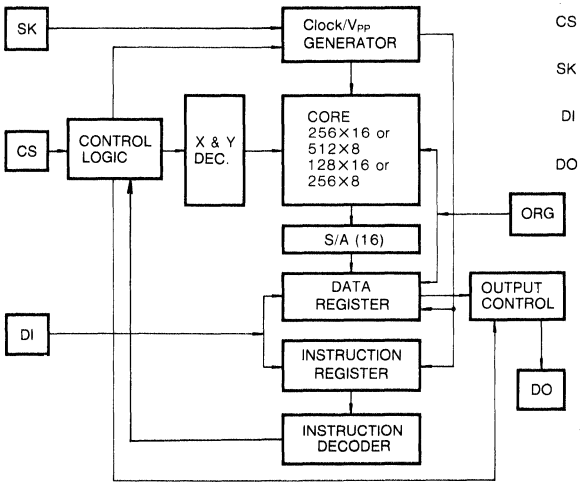
GENERAL DESCRIPTION

The KM93C57V/67V is a extended voltage 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

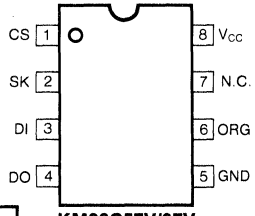
The KM93C57V/67V can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

The KM93C57V/67V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

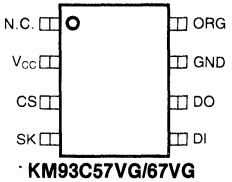
FUNCTIONAL BLOCK DIAGRAM



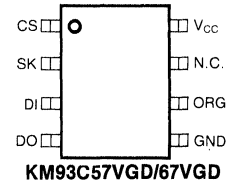
PIN CONFIGURATION



KM93C57V/67V



KM93C57VG/67VG (C57V/67V)



KM93C57VGD/67VGD (57VD/67VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	—	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		3.0	5.5	V
Operating Current	(DC)	I_{CC1}	CS = SK = V_{IH}		1	mA
	(AC)	I_{CC2}	CS = V_{IH}, SK = 1MHz		3	mA
Standby Current	(TTL)	I_{SB1}	V_{CC} = 5.5, CS = V_{IL}		250	μA
	(CMOS)	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}		100	μA
Input Low Voltage Levels		V_{IL}		−0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	V_{CC} + 0.3	V
Output Voltage Levels (4.5 < V_{CC} < 5.5)		V_{OL1}	I_{OL} = 2.1mA		0.4	V
		V_{OH1}	I_{OH} = −400μA	2.4		V
Output Voltage Levels (3.0 < V_{CC} < 4.5)		V_{OL2}	I_{OL} = 10μA		0.2	V
		V_{OH2}	I_{OH} = −10μA	2.0		V
Input Leakage Current		I_{LI}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{LO}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.2V to 2.6V
Input Rise and Fall Times	20ns
Timing Measurement Reference Level	0.8V and 2.0V
Output Load	1 TTL GATE and CL = 100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

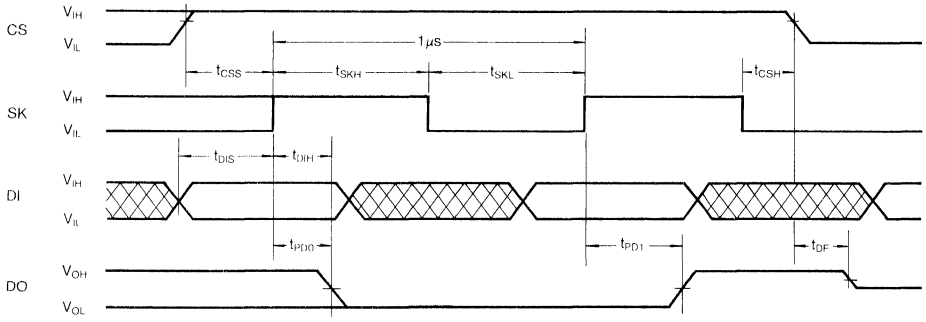
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 x 16 *(128 x 16)	512 x 8 (256 x 8)	256 x 16	512 x 8	
READ	1	10	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{OUT} (16 bit)	D_{OUT} (8 bit)	Read register at specified address
WRITE	1	01	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{15}~D_0	D_8~D_0	Write the data at specified address
ERASE	1	11	A7~A0 (A6~A0)	A8~A0 (A7~A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	D_8~D_0	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '( )' is appliable to KM93C57V

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

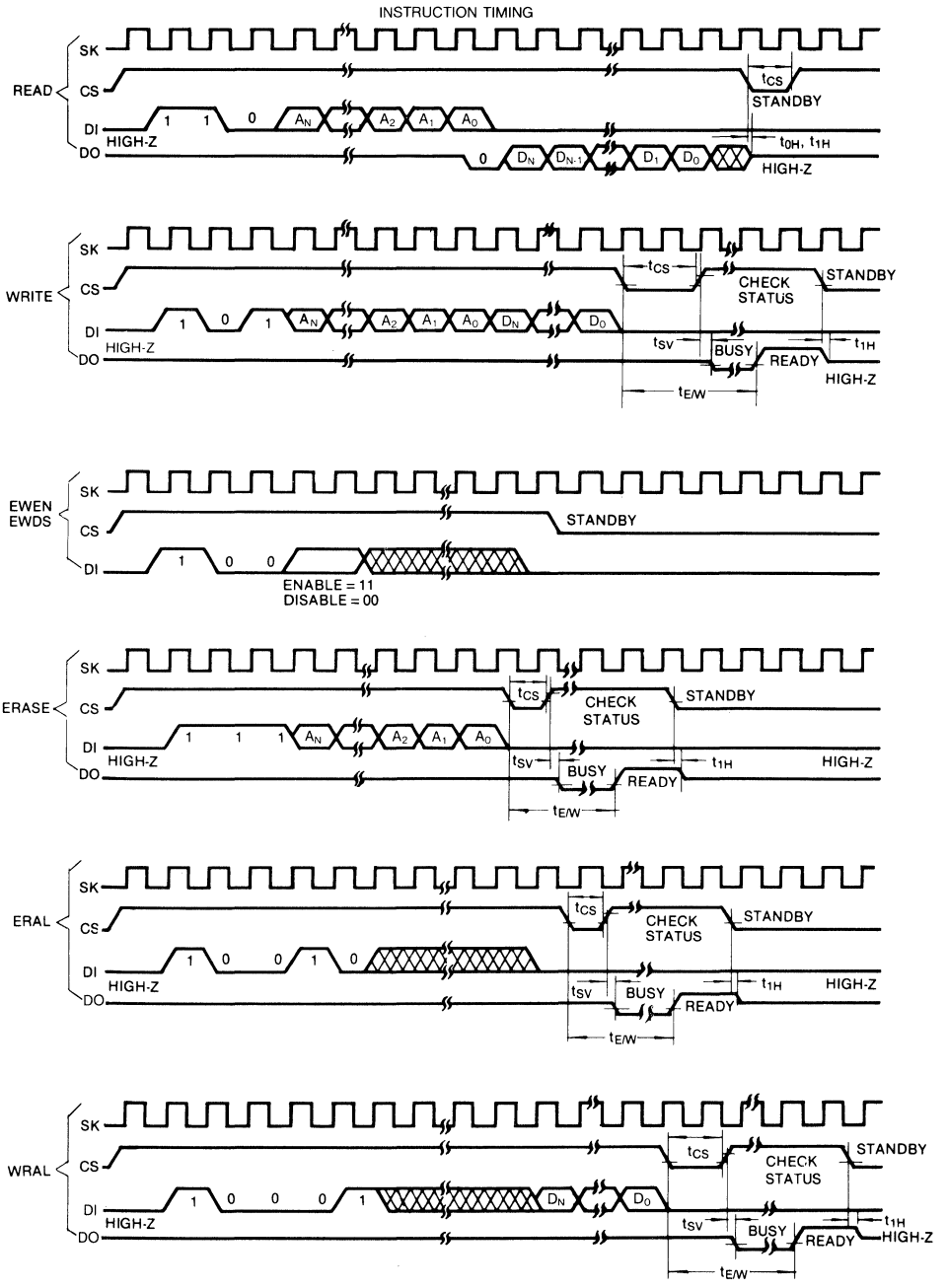


ORGANIZATION

P/N	Organization	AN	DN
KM93C67V	512× 8	A_8	D_7
	256×16	A_7	D_{15}
KM93C57V	256× 8	A_7	D_7
	128×16	A_6	D_{15}

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



INTRODUCTION

The KM93C57V/67V is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a3.0V to 5.5V single power supply. The write cycle of the KM93C57V/67V is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

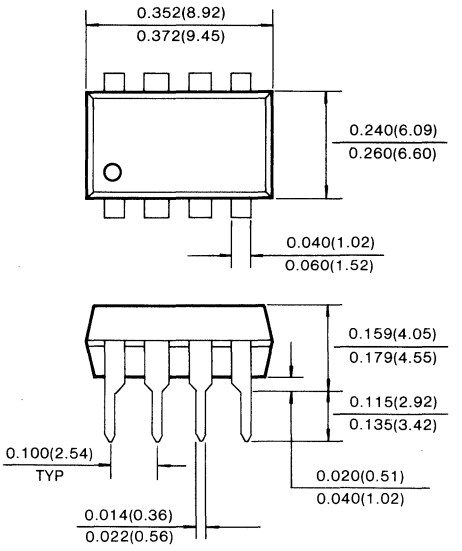
ERAL

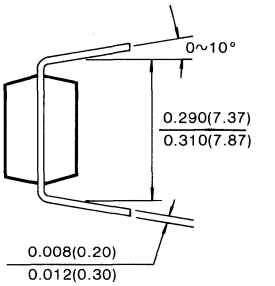
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

PACKAGE DIMENSIONS

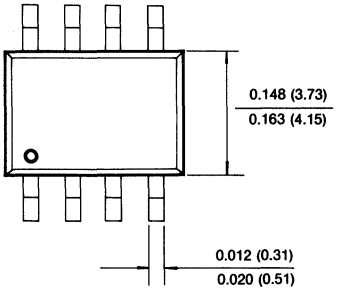
8 PIN PLASTIC DUAL IN LINE PACKAGE

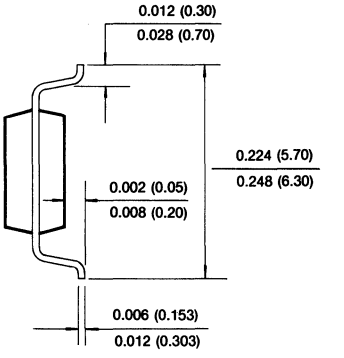
unit; inches (millimeters)

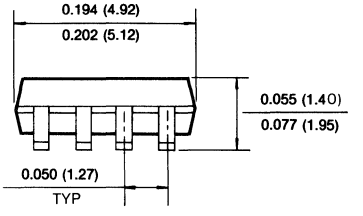




8 PIN PLASTIC SMALL OUT LINE PACKAGE







2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Write protection with memory pointer**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **Memory organization:**
  - **— 256 x 16 bits for KM93CS66**
  - **— 128 x 16 bits for KM93CS56**
- **System Clock Frequency: 1 MHz (max.)**
- **Self timed write cycle**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

GENERAL DESCRIPTION

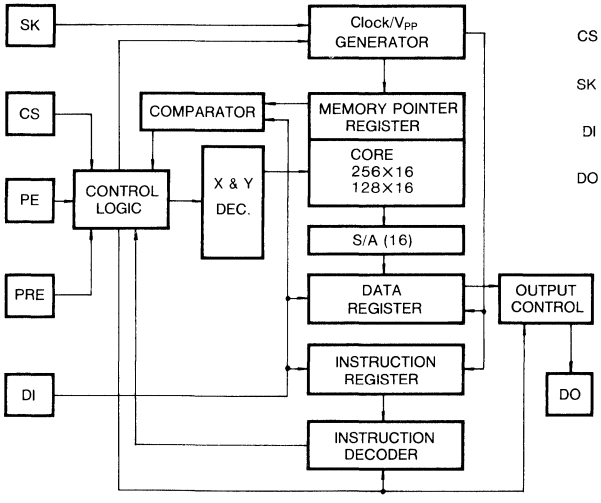
The KM93CS56/66 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

The KM93CS56/66 can be organized as 128/256 registers of 16 bits each, which can be read/written serially and provides data security feature with the memory pointer against the data modification. Besides, this memory pointer address can be locked permanetly.

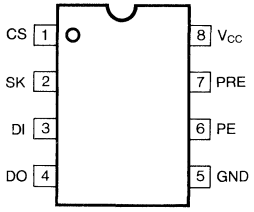
The KM93CS56/66 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

2

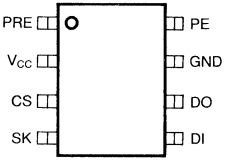
FUNCTIONAL BLOCK DIAGRAM



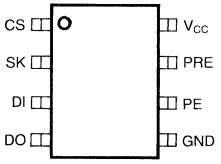
PIN CONFIGURATION



KM93CS56/66



KM93CS56G/66G (S56/66)



KM93CS56GD/66GD (S56D/66D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	250	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	100	μA
Input Low Voltage Levels		V_{IL}		-0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	Vcc+0.3	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and CL=100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
PRE Setup Time	t_{PRES}	Relative to SK	50	—	ns
PE Setup Time	t_{PES}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
PE Hold Time	t_{PEH}	Relative to CS	100	—	ns
PRE Hold Time	t_{PREH}	Relative to CS	100	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in Tri-state	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

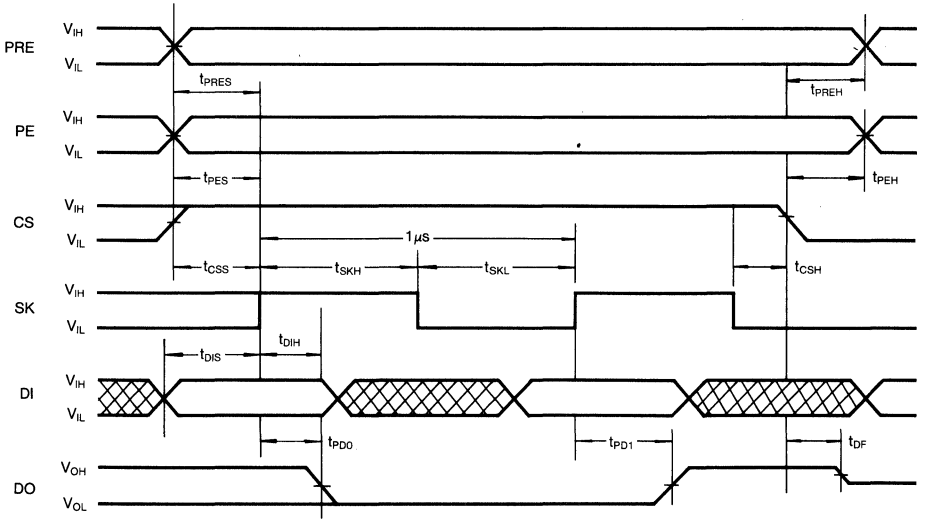
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	PRE	PE	Comment
READ	1	10	A7 - A0	D_{OUT}	0	X	Read register starting at specified address
WRITE	1	01	A7 - A0	D_{15}-D_0	0	1	Write data at memory
EWEN	1	00	11XXXXXX	—	0	1	Erase/Write enable
EWDS	1	00	00XXXXXX	—	0	X	Erase/Write disable
WRAL	1	00	01XXXXXX	D_{15}-D_0	0	1	Write all registers
MPRRD	1	10	XXXXXXXX	D_{OUT}	1	X	Read MPR*[1]
MPREN	1	00	11XXXXXX	—	1	1	Enable MPR write related instructions
MPRCLR	1	11	11111111	—	1	1	Clear the MPR
MPRWRT	1	01	A7 - A0	—	1	1	Write address in MPR*
MPRDS	1	00	00000000	—	1	1	One time only instruction to lock the MPR address permanently

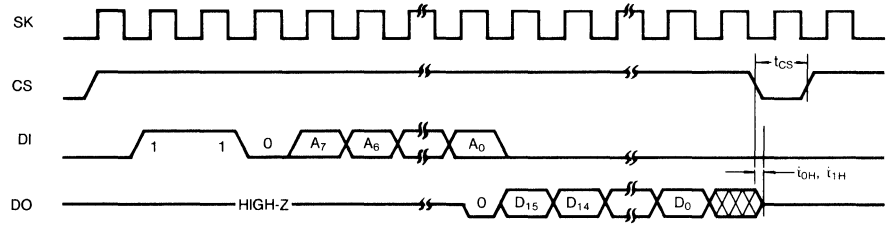
Note: 1. MPR: Memory Pointer Register
2. A7 is a "don't care" address for KM93CS56

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

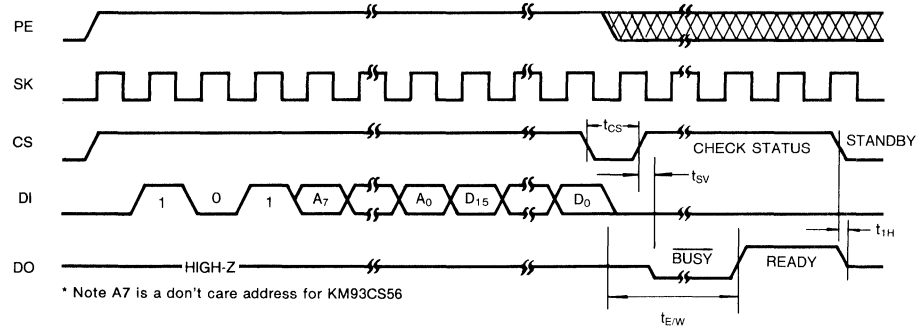


READ (PRE=V_{IL}, PE="Don't Care")



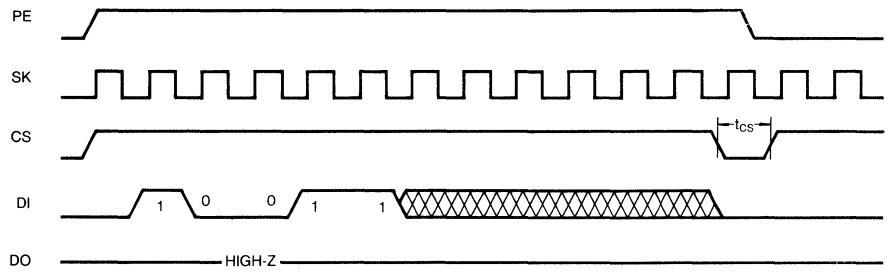
* Note A7 is a don't care address for KM93CS56

WRITE (PRE=V_{IL})

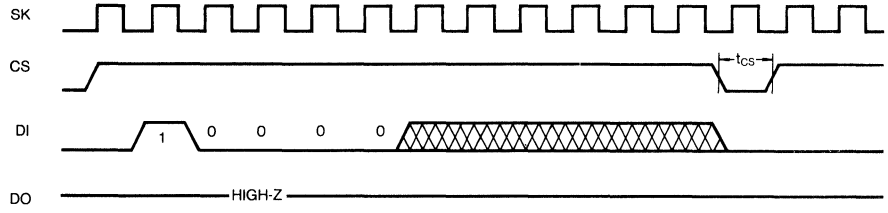


* Note A7 is a don't care address for KM93CS56

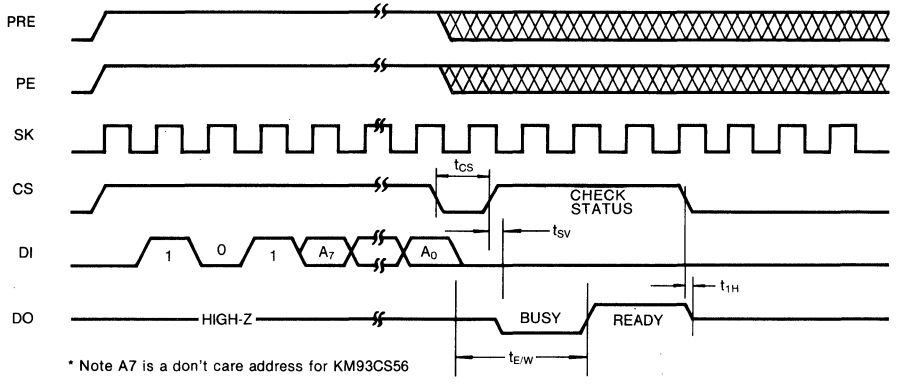
EWEN (PRE=V_{IL})



EWDS (PRE=V_{IL}, PE="Don't Care")

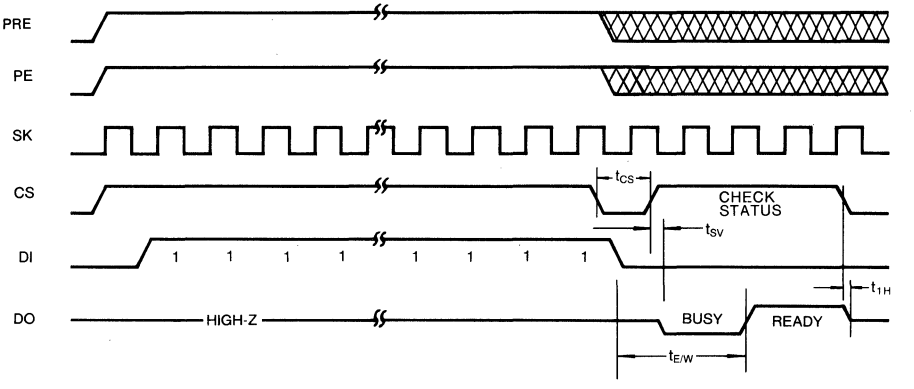


MPRWRT

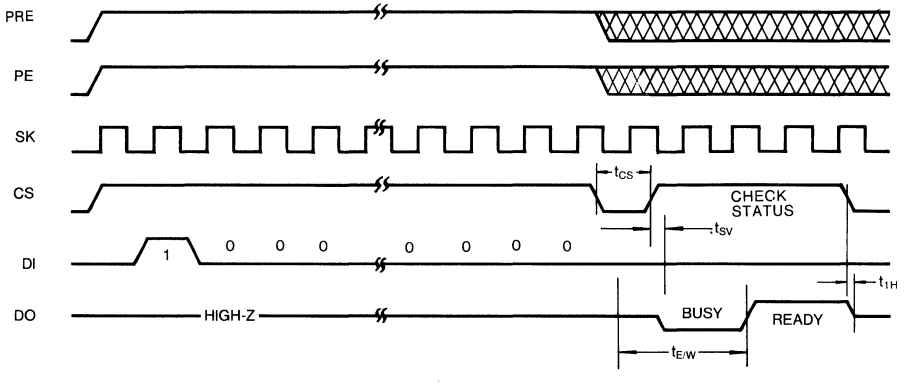


* Note A7 is a don't care address for KM93CS56

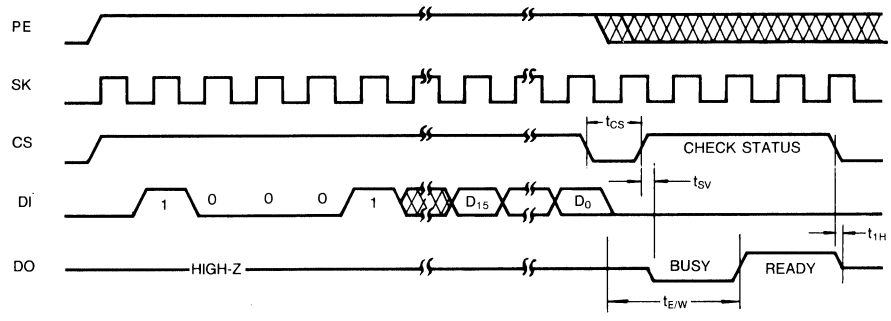
MPRCLR



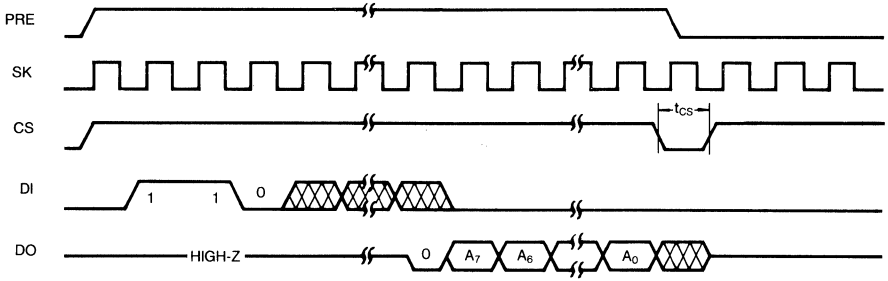
MPRDS



WRAL (PRE=V_{IL})

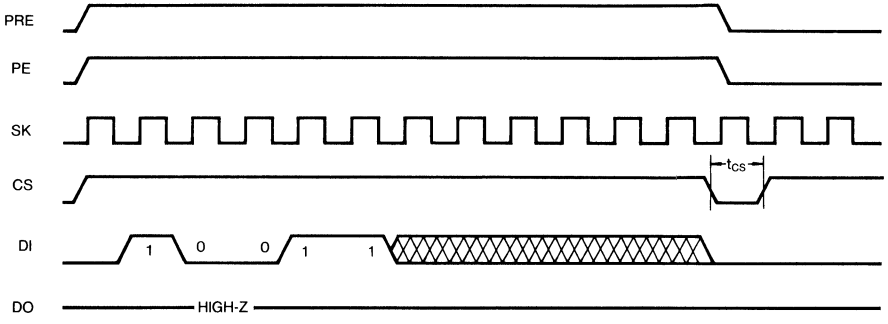


MPRRD (PE="Don't Care")



* Note A7 is a don't care address for KM93CS56

MPREN



INTRODUCTION

The KM93CS56/66 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93CS56/66 is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention. The KM93CS56/66 offers a data security feature with memory pointer to prevent the protected memory register. Once defined the memory pointer, the memory register is divided into a read/write area and read only area. The addresses equal to or greater than the memory pointer are protected from the Write operation unless clearing the memory pointer register.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string. After 16 bits are clocked out, the device read out the next address automatically. To terminate the read operation CS pin must be toggled high to low.

EWEN/EWDS

The KM93CS56/66 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle. During loading the WRITE instruction, the PE pin must be high, however after loading the WRITE instruction, the PE pin becomes "don't care".

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto chip erase. All cells are writen simultaneously with given data. The WRAL instruction is valid only when the memory pointer register has been cleared by executing a MPRCLR instruction and while loading the WRAL instruction, the PE pin must be held high, however after loading the WRAL instruction, the PE pin becomes "don't care"

MPRRD

The memory pointer register read (MPRRD) instruction outputs serial 8-bit address stored in the memory pointer register on the DO pin. Like the read operation, a dummy bit (logical "0") precedes the 8 bit address string. While loading the MPRRD instruction, PRE pin must be held high.

MPREN

The memory pointer register enable (MPREN) instruction is used to enable the MPRCLR. MPRWRT and MPRDS modes. The device must be in EWEN mode, before MPREN mode is executed. Both the PRE and PE pin must be held high while loading the MPREN instruction, however after loading the instruction, PE and PRE pins become "don't care". Note that MPREN instruction must be immediately preceded before executing a MPRCLR, MPRWRT, or MPRDS instruction.

MPRCLR

The memory pointer clear (MPRCLR) instruction reset the address stored in the memory pointer register. After executing the MPRCLR, the entire memory register can be programmed by using WRITE and WRAL instruction. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care".

MPRWRT

The memory pointer register write (MPRWRT) instruction program the memory pointer address into the memory pointer register. Once defined the memory pointer address, the memory registers, which has greater than or equal to the memory pointer address, are protected from the data modification. The memory pointer register must be reset before moving the memory pointer address, by executing the MPRCLR instruction. Both the PRE and PE pin must be held high while loading the MPWRT instruction. Once enabled this instruction, both the PE and PRE pins become "don't care"

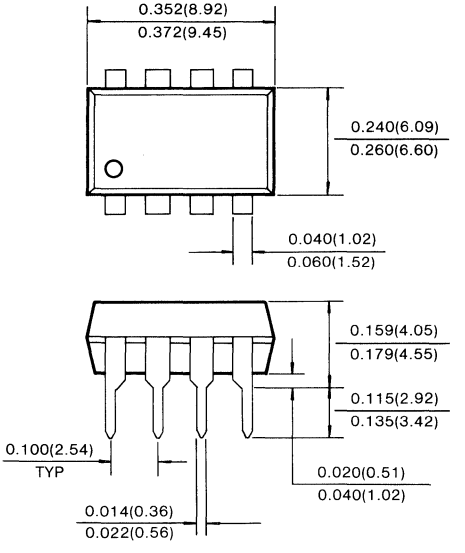
MPRDS

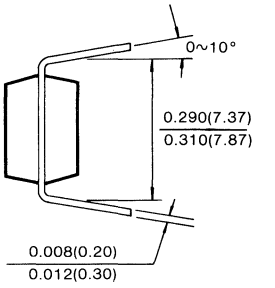
The memory pointer function disable (MPRDS) instruction is one time only instruction. The MPRWRT, MPRCLR, and MPREN instruction is disabled by executing this instruction. Therefore the address of the memory pointer register is permanently unalterable so that the memory registers whose address is greater than or equal to the memory pointer address, are not afford to modify the data permanetly. Both the PRE and PE pin must be held high while loading the MPRCLR instruction. Once enabled this instruction, both the PE and PRE pins become "don't care."

PACKAGE DIMENSIONS

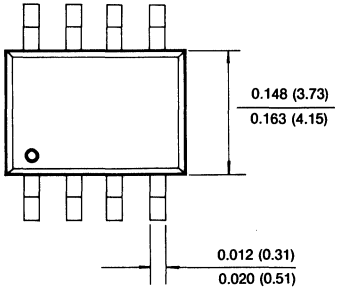
8 PIN PLASTIC DUAL IN LINE PACKAGE

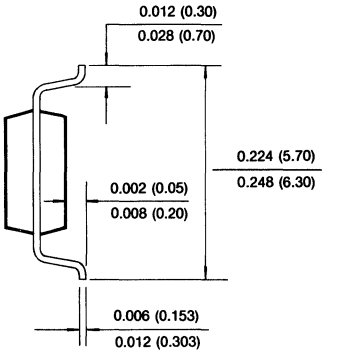
unit; inches (millimeters)

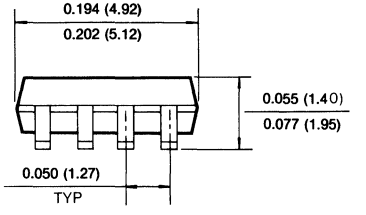




8 PIN PLASTIC SMALL OUT LINE PACKAGE







1,024-Bit Intelligent Serial EEPROM for Prepaid Card

FEATURES

- **Single 5V power supply**
- **Internal Memory organization : 128×8bit**
- **UART compatible asynchronous protocol with system clock 4.915 MHz**
- **Low power comsumption**
  - **Active Current : 5 mA**
  - **Standby Current : 100μA**
- **Fast write time : 10 ms/byte**
  - **Self-timed write**
  - **Automatic erase before write**
- **Main memory area 1024 bits, divided by logic into**
  - **4 bytes chip data**
  - **12 bytes card data**
  - **4 bytes count data and backup**
  - **108 bytes free area**
- **Maximally 65535 count units**
- **High perfomance CMOS floating-gate technology**
  - **Endurance : 10,000 cycle/byte**
  - **Data retension : 10 years**
- **Standard delivery : Wafer form and 8 pin COB**

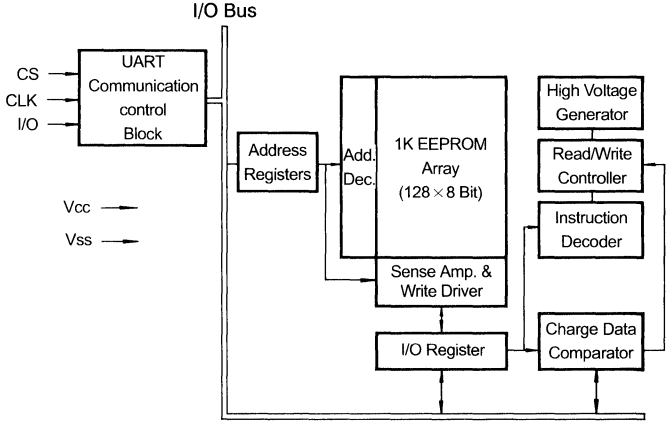
GENERAL DESCRIPTION

The KM28i01 is based on an EEPROM array containing 1024 bits. The main memory area is divided into 4 different section depending on the operating characteristics. It has EEPROM of 112 bytes, inhibitable EEPROM of 12 bytes by Lock-out and ROM of 4 bytes. Thus, by executing Lock instruction, the address bytes ranging 4 to 15 can be protected against write.
Spicial logic algorithm to secure the value data is included. The two bytes storing the value data is protected from write operation when the new value is equal to or higher than the stored value.
On delievery the memory content is at logic "1" except for ROM area, whose contents the customer is asked to notify to SAMSUNG.

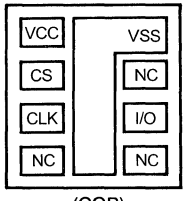
The KM28i01 is an ideal application for pre-paid cards such as telephone cards, using a UART-compatible asychronous protocol. The standard delivery of this product is performed either in dice or in 8 pin COB.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



(COB)

Pin Name	Pin Function
CS	Chip Select
CLK	Clock
I/O	Data In/Out
VCC	Power
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}	−0.3 to + 7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−65 to + 125	°C

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Voltage reference to Vss, T_A=−20℃ to + 70℃

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	—	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	—	4.5	—	5.5	V
Operating Current	I_{CC}	V_{CC}=5.5V, CS=5.5V	—	—	5	mA
Standby Current(Reset)	I_{SB}	V_{CC}=5.5V, CS=0V	—	—	100	μA
Input Voltage Levels	V_{IL}	—	2.4	—	Vcc	V
	V_{IH}	—	- 0.	—	0.8	V
Output Voltage Levels	V_{OL}	I_{OL}=2.1mA	3	—	0.4	V
	V_{OH}	I_{OH}= - 400μA	—	—	—	V
Input Leakage Current	I_{LC}	V_{IN}=5.5V, CS=V_{IH}	2.4	—	10	μA
Output Leakage Current	I_{LO}	V_{out}=CLK=V_{CC}=5.5V	—	—	10	μA
Clock Sink Current	I_{LS}	V_{IN}=5.5V, CS=V_{IL}*	—	10	—	μA
Write Inhibit Voltage Level	V_{WI}	—	3.0	—	—	V

Note 1) Sinking current of Clock pin when chip not selected.

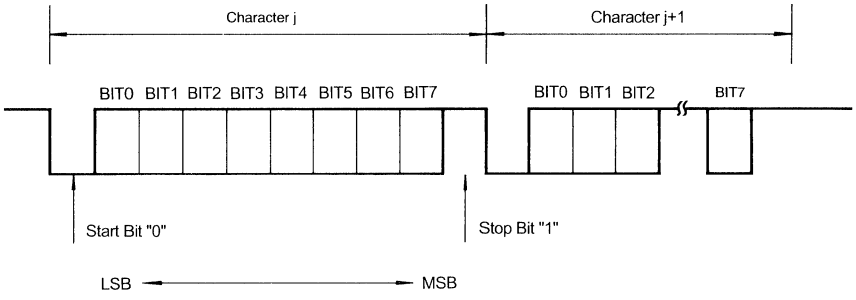
AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Timing Measurement Reference Level	0.8V and 2.0V
Output Load	1 TTL GATE and CL=100 pF

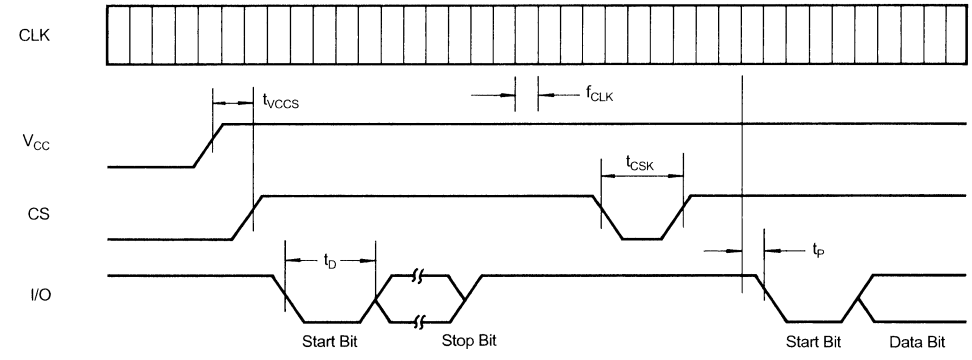
AC OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data bit Time	t_D	VIN=VIH or VIL Vout=VOH or VOL CL=100pF	—	104	—	μs
Clock to Dout Delay	t_P		—	—	150	ns
Erase/Write pulse width	$t_{E/W}$		—	—	10	ms
CS low pulse delay	t_{CSL}		100	—	—	ns
Vcc to CS setup time	t_{VCCS}	CL = 100pF	5	—	—	μs
Clock frequency	f_{CLK}	—	—	4.9152	—	MHz

ASYNCHRONOUS SERIAL COMMUNICATION PROTOCOL

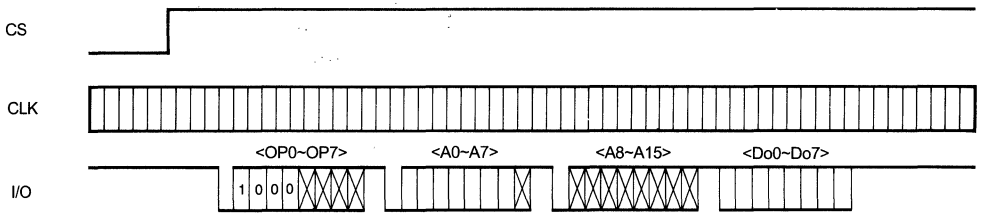


AC TIMING DIAGRAM

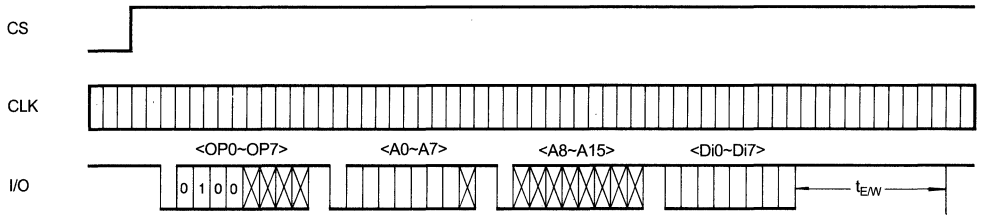


TIMING DIAGRAMS

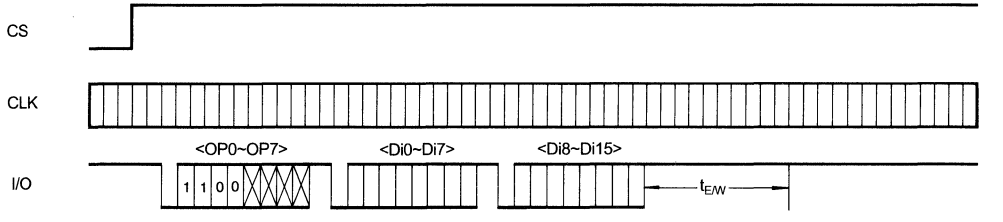
READ TIMING



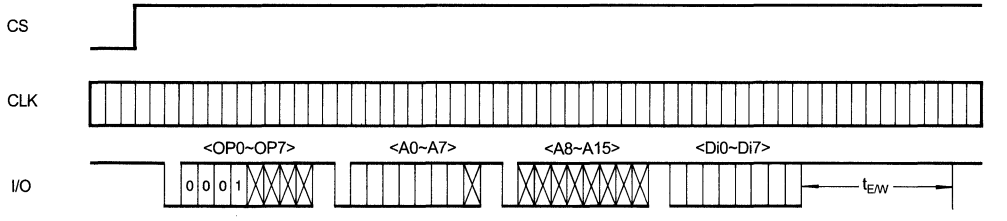
ISRWRT TIMING



VALWRT TIMING

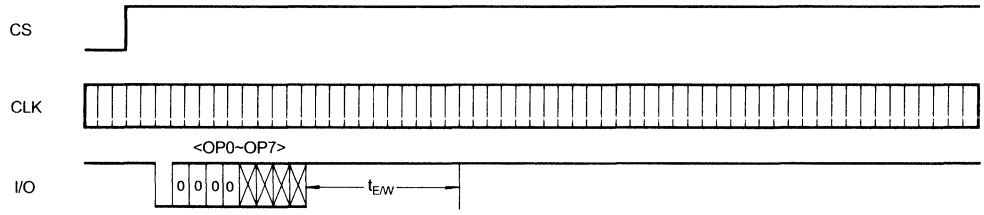


USRWRT TIMING

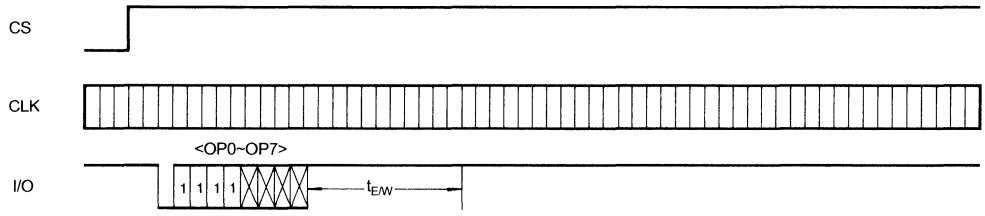


TIMING DIAGRAMS (Continued)

LOCK TIMING



NOP TIMING



INTRODUCTION

The KM28i01 is a value-card chip, internally organized as 128 × 8 bits, communicating with external devices via asynchronous serial communication protocol with 9600 BPS.
The operating characteristics of the memory are divided into different function areas :

* address 0-3 as ROM for chip data
* address 4-15 as inhibitible EEPROM for card data
* address 16-17 as EEPROM with security logic for value data
* address 18-19 as EEPROM with security logic for a back-up of value data
* address 20-127 as blank EEPROM for storing information

The address range 0-3 holds unalterable chip data, eg customer I.D. or intended application. The address range 4-15 is normally written during card initialization by the card issuer and secured against alteration by executing Lock instruction.
The address range 16 and 17 is EEPROM and stores the current status of the value. The two bytes comprise a word, 16 is low byte and 17 is high byte.
Address range 18-19 is an exact back-up of bytes 16-17. Executing VALWRT instruction writes the value data into the address range 16-19 altogether within the $t_{E/W}$ of 10ms. VALWRT operation is internally terminated when the new value is higher than or equal to the present value stored. Thus the number of write operation that is possible is restricted by chip logic to a maximum count of 65535 units.
The address range 20-127 is always accessible both in read and write mode.

PIN DESCRIPTION

CS (Chip Select)

The CS pin allows normal operation of device when set to high. When set to low, it resets the device to minimize the power consumption, terminating all I/O communication, and puts the output in high impedance state.

CS (Clock)

CLK is a system clock which allows operation of the device at the specified frequency. The KM28i01 has an internal clock divider to produce 9600 baud output using the input clock frequency of 4.9152 MHz. When CS is low, an internal pull-down device will sink a typical current of 10mA through clock pin.

I/O (Input/Output)

The data I/O accepts data and instruction and transfers data at the end of READ instruction in a serial format. It is in a high impedance state except during the output of data. Each byte must begin with "0" as start bit. The device will accept as many bits as an instruction requires, including both data and address bits.

Extra bits will be disregarded if they are "1's" and "0's" will be misinsterpreted as the start bit of the next byte. However, once the last byte of the instruction is accepted, the internal data-in buffer is disabled until the internal auto-timed write cycle is finished or the output of the stop bit of the accessed byte for read operation is finished.

DATA PROTECTION

Features have been designed into KM28i01 to prevent unwanted write cycles during power supply transitions and to protect from malfunction of command decoding during system noise periods.

The KM28i01 has a protection feature against I/O noises; the width of which shorter than 30ns(typ.) will be filtered out. Any inadvertent writes are inhibited when Vcc is less than V_{WI}=3.0V(min.), the write inhibit Vcc level. During power-up, the device automatically prevents any command operations for a period of 1ms after Vcc reaches the V_{WI} level. Holding CS low during power transitions will also suppress any command operation.

MEMORY MAP

Add	Information	Information	Memory Type	Remark
0 ~ 3	Producer Section	Read	ROM	Chip Data
4 ~ 15	Issuer Section	ISRWRT Read Lock	OTP ROM (by Lock Inst.)	Card Data
16	Count Section	VALWRT Read	EEPROM	Low Byte of count
17				High Byte of count
18	Count Back-up Section			Back-up of low count byte
19				Back-u[of high count byte
20 ~ 127	User Section	USRWRT Read		

DEVICE OPERATION

INSTRUCTION SET TABLE

INSTRUCTION	OP CODE				COMMENT
	SB	LBS	MSB	SP	
READ	0	1000 × × × ×		1	Read data
ISRWRT	0	0100 × × × ×		1	Write into issuer section
VALWRT	0	1100 × × × ×		1	Write amount of money information
USRWRT	0	0001 × × × ×		1	Write into unprotected section
LOCK	0	0000 × × × ×		1	Lock issuer section
NOP	0	1111 × × × ×		1	No operation

Note) × : Don't care, SB: Start bit, SP: Stop Bit

READ READ [ADDR1] [ADDR2]

After a read instruction and address set is received, the I/O pin outputs the contents of the specific addressed data bank serially. The entire 1024 bits are accessible for reading.

ISRWRT1 ISRWRT [ADDR1] [ARRD2] [DATA]

This instruction is used to write the issuer section of the memory. After the stop bit of data is loaded, the write cycle is initiated automatically.

VALWRT VALWRT [DATA1] [DATA2]

This instruction writes the value data into the two bytes of the count section. VALWRT operation is internally terminated when the new value data is higher than or equal to the present value stored. All of the address range 16-19 is written the given data in one write cycle. Data 1 is written into the low bytes of address 16 and 18 and data 2 into the high bytes of address 17 and 19.
After the stop bit of the data 2 is loaded, the self-timed write cycle is initiated automatically.

USRWRT USRWRT [ADDR1] [ADDR2] [DATA]

This instruction is used to write the address range of 20-127.

LOCK LOCK

Lock is one time only instruction. The ISRWRT instruction is disabled by executing Lock.
Therefore the issuer section(address range 4-15) is permanatly unalterable to become a ROM area.

NOP NOP

NOP is an idle instruction. While executing this instruction, the chip does not perform any operation.

2K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **KM28C16/KM28C17: Commercial**
  - **KM28C16I/KM28C17I: Industrial**
- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Write Timing**
  - **Automatic Internal Erase-Before-Write**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C17)**
  - **$\overline{\text{Data}}$-Polling and Verification**
- **32-byte page Write 2ms**
  - **Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **100,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

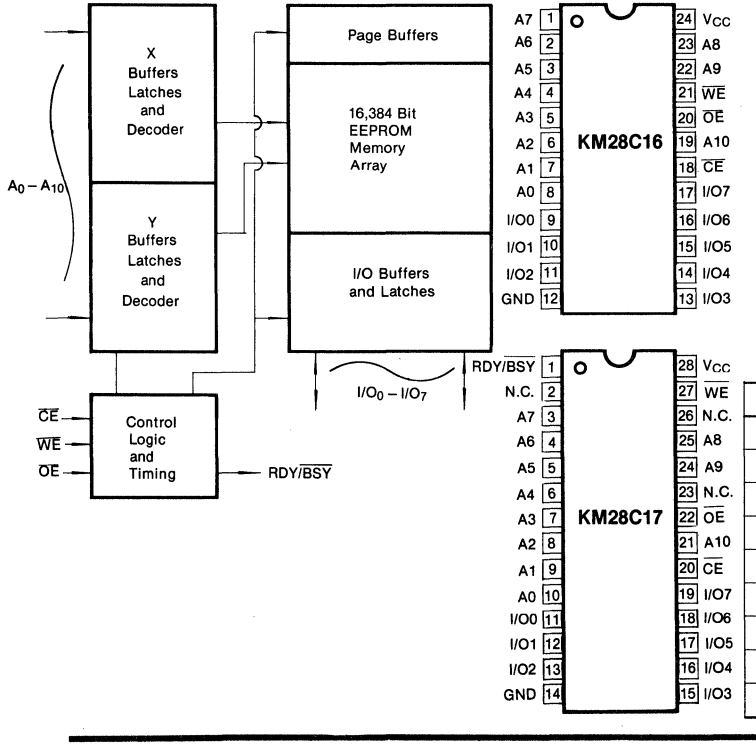
The KM28C16/C17 is a 2,048 x 8 bit Electrically Erasable Programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C16/C17 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 2ms write period. A 32-byte page write enables an entire chip written in 128ms.

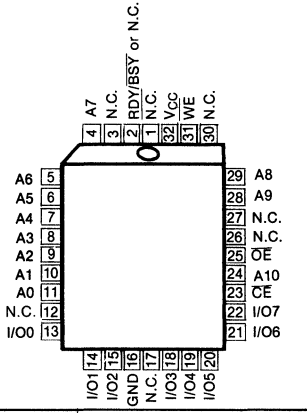
The KM28C16/C17 features $\overline{\text{Data}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM28C17 features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C16/C17 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

KM28C16/C17: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C16I/C17I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C16/C17: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C16I/C17I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C16-15 KM28C16I-15 KM28C17-15 KM28C17I-15		KM28C16-20 KM28C16I-20 KM28C17-20 KM28C17I-20		KM28C16-25 KM28C16I-25 KM28C17-25 KM28C17I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

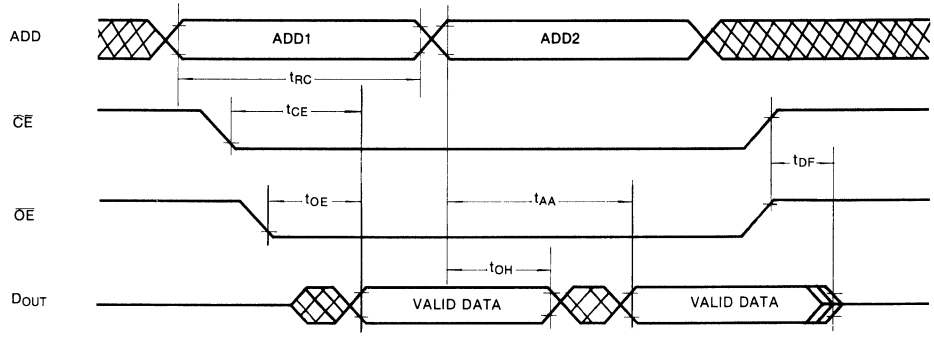
WRITE CYCLE

Parameter		Symbol	Min	Max	Unit
Write Cycle Time	Commercial	t_{WC}		2	ms
	Industrial			5	ms
Address Set-Up Time		t_{AS}	0		ns
Address Hold Time		t_{AH}	80		ns
Write Set-Up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
$\overline{CE}$ Pulse Width		t_{CW}	100		ns
Output Enable Set-Up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
$\overline{WE}$ Pulse Width		t_{WP}	100		ns
Data Set-Up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns
Time to Device Busy		t_{DB}		100	ns
Busy to Write Recovery Time		t_{BWR}	50		ns
Byte Load Cycle Time		t_{BLC}	0.2	100	μs
Last Byte Loaded to $\overline{Data}$ Polling		t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at a rising edge of $\overline{WE}$.

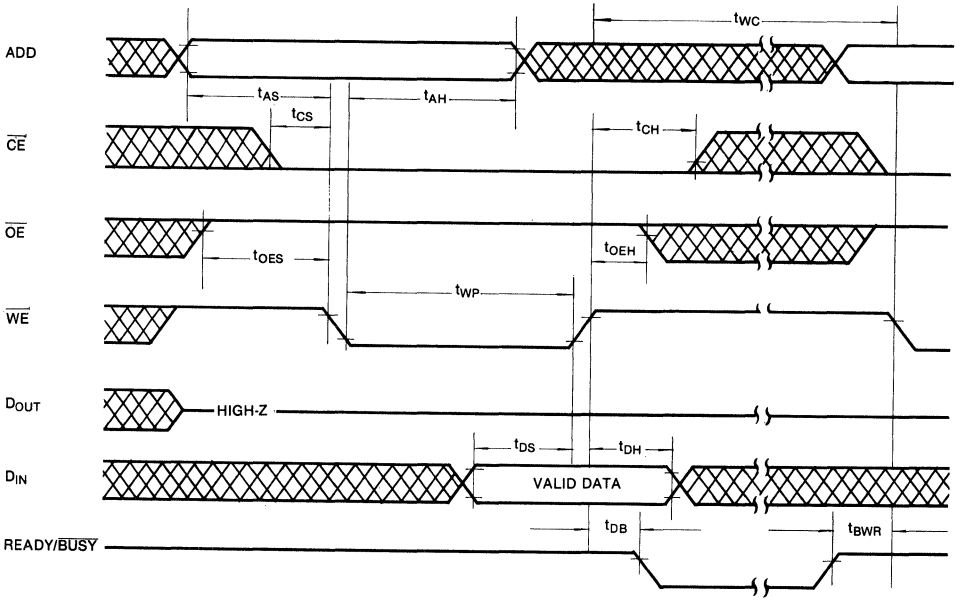
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

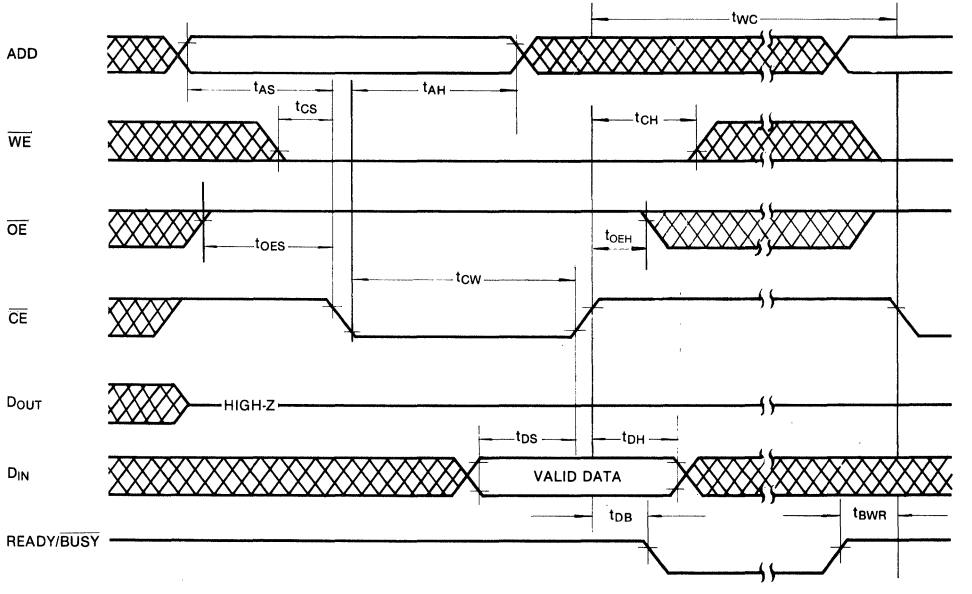


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

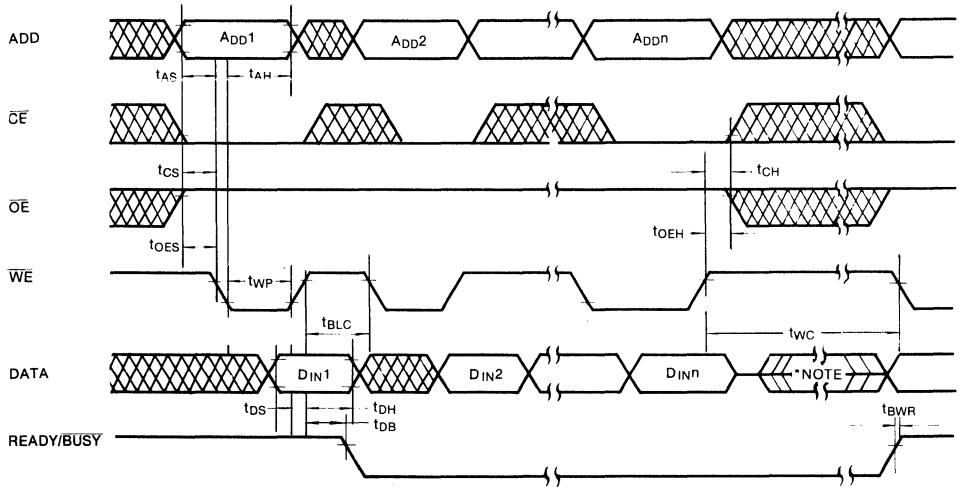


$\overline{CE}$ CONTROLLED WRITE

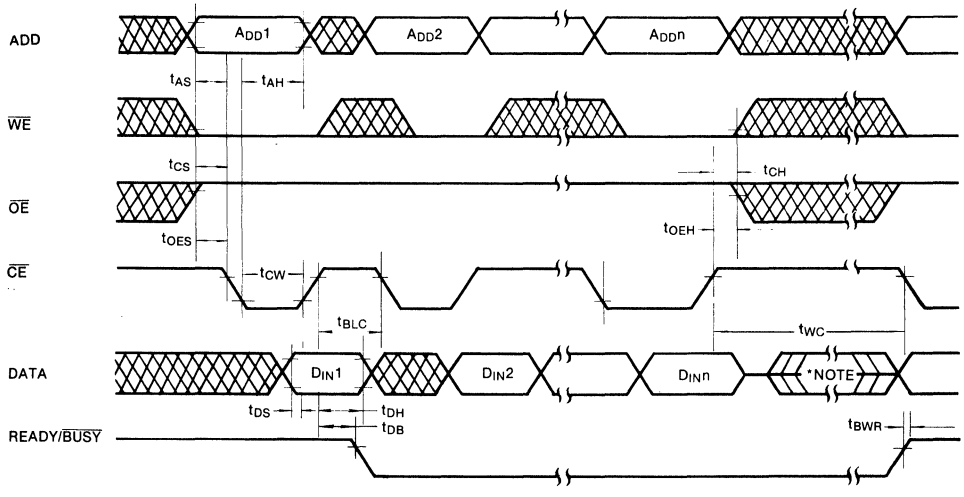


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $\overline{D_{IN}n}$ when the chip is read.
I/O_0-I/O_6 have high impedance.

SAMSUNG ELECTRONICS

DEVICE OPERATION

READ

Reading data from the KM28C16/C17 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C16/C17 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C16/C17 is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM28C16/C17.

**** PAGE WRITE MODE ****

The KM28C16/C17 allows up to 32 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 bytes of data are loaded into the KM28C16/C17 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C16/C17 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_4) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A_5-A_{10}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C16/C17 also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C16/C17 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C16/C17 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise, the width shorter than 20ns (typ.) will not start any unwanted write cycle.

Write cycles are also inhibited when V_{CC} is less than V_{WI} = 3.0 volts, the write inhibits V_{CC} level.

During power-up, the KM28C16/C17 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

DATA POLLING

The KM28C16C/C17 features Data polling at I/O_7 to detect the completion of a write cycle using a simple require any extemal hardware. During the write period, any data attempt to read of the last byte the EEPROM will produce, at I/O_7, an inverted value of the last I/O_7 data loaded in to the EEPROM (I/O_0-I/O_6 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION (Continued)

READY/BUSY

The KM28C17 has a Ready/Busy output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/Busy output is configured as an open-drain driver there-by allowing two or more Ready/Busy outputs to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready/Busy pin.

ENDURANCE AND DATA RETENTION

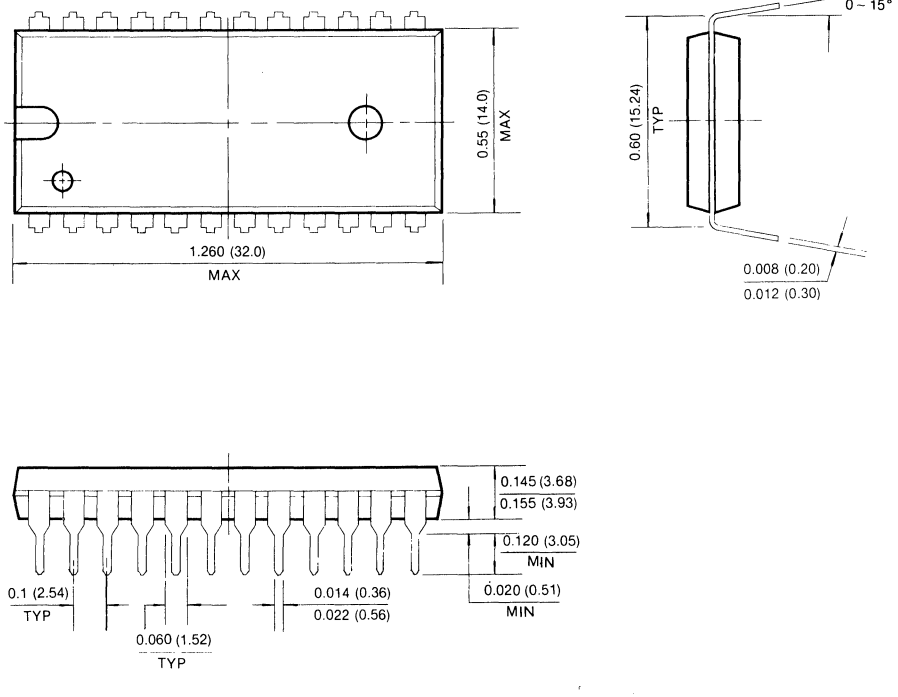
KM28C16/C17 is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation, and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

2

PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)

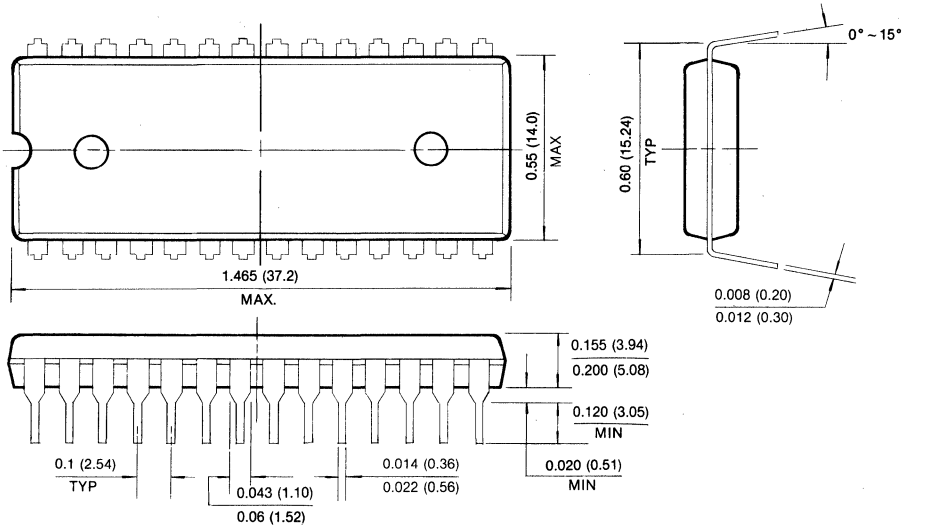


SAMSUNG ELECTRONICS

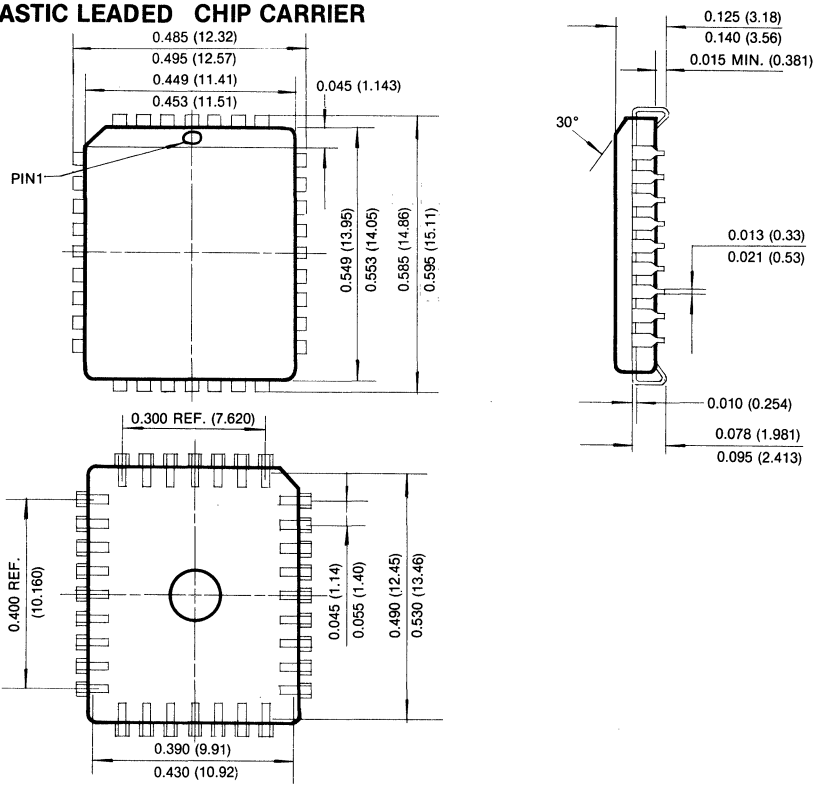
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



8K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C64A/65A: Commercial**
  - **— KM28C64AI/65AI: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Internal Erase-Before-Write**
  - **— Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65A)**
- **Fast Write Cycle Time**
  - **— 64-Byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 0.7 seconds**
- **$\overline{\text{Data}}$-Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 120ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating-Gate Technology**
  - **— Endurance: 100,000 Cycle**
  - **— Data Retention: 10 years**
- **JEDEC Byte-wide Memory Pinout**

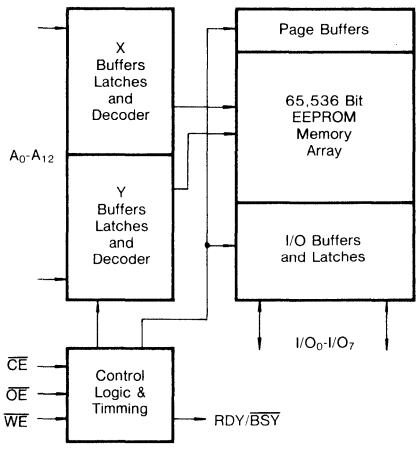
GENERAL DESCRIPTION

The KM28C64A/65A is a 8,192×8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

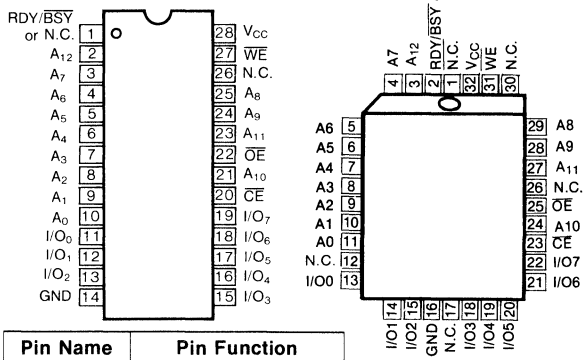
Writing data into the KM28C64A/65A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 0.7 seconds.

The KM28C64A/65A also features $\overline{\text{Data}}$-polling and a Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware. The KM28C65A features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.
The KM28C64A/65A is designed for applications up to 100,000 write cycles per byte. It's on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C64A/65A : Voltage reference to V_{SS}, T_A=0°C to +70°C
KM28C64AI/65AI : Voltage reference to V_{SS}, T_A=−40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, all I/O's open (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}-0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

Note 1: All address toggling from V_{IL} to V_{IH} at 8.4MHz.

CAPACITANCE (T_A=25°C, f=1.0 MHz))

Item	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{Data}$ Polling	$I/O_7=\overline{D_7}$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C64A/65A : T_A=0°C to +70°C V_{CC}=5V±10%, unless otherwise noted
KM28C64AI/65AI: T_A=−40°C to +85°C V_{CC}=5V±10%, unless otherwise noted

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM28C64A-12 KM28C65A-12		KM28C64A-15 KM28C64AI-15 KM28C65A-15 KM28C65AI-15		KM28C64A-20 KM28C64AI-20 KM28C65A-20 KM28C65AI-20		KM28C64A-25 KM28C64AI-25 KM28C65A-25 KM28C65AI-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		250		ns
Chip Enable Access Time	t_{CE}		120		150		200		250	ns
Address Access Time	t_{AA}		120		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

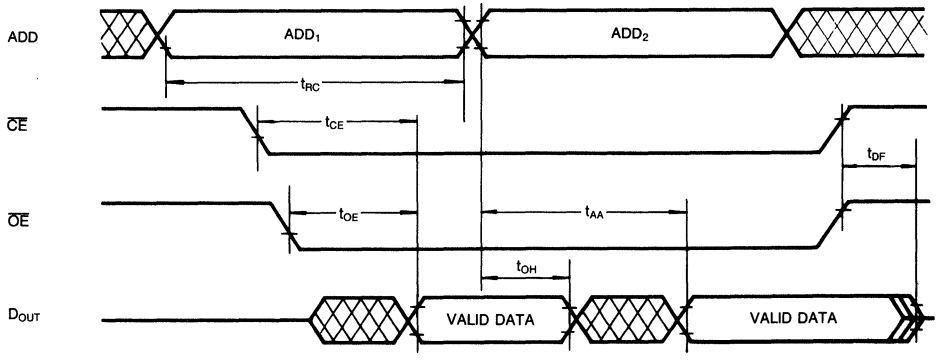
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		5	ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at rising edge of $\overline{WE}$.

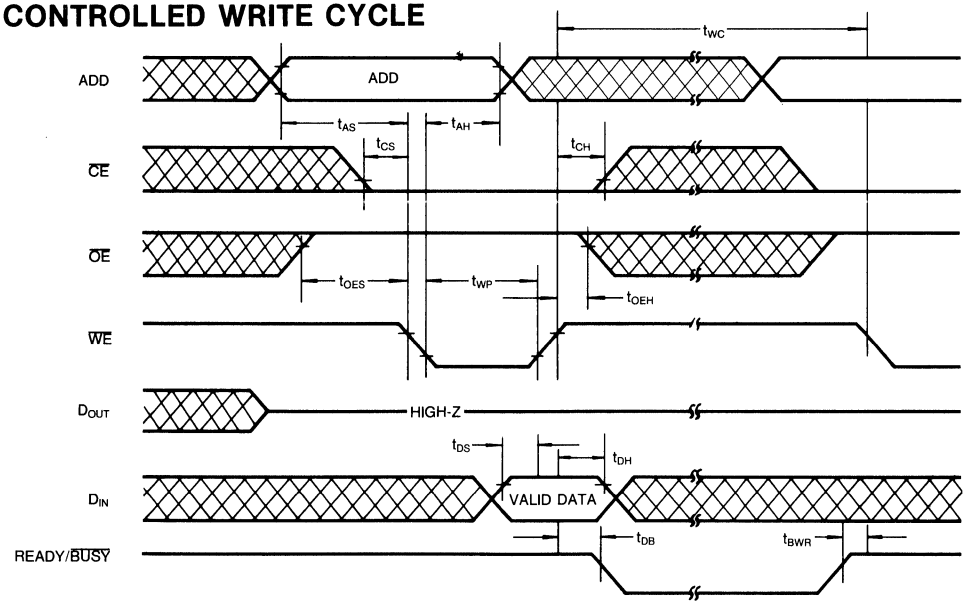
TIMING DIAGRAM

READ CYCLE ($\overline{WE}$=V_{IH})

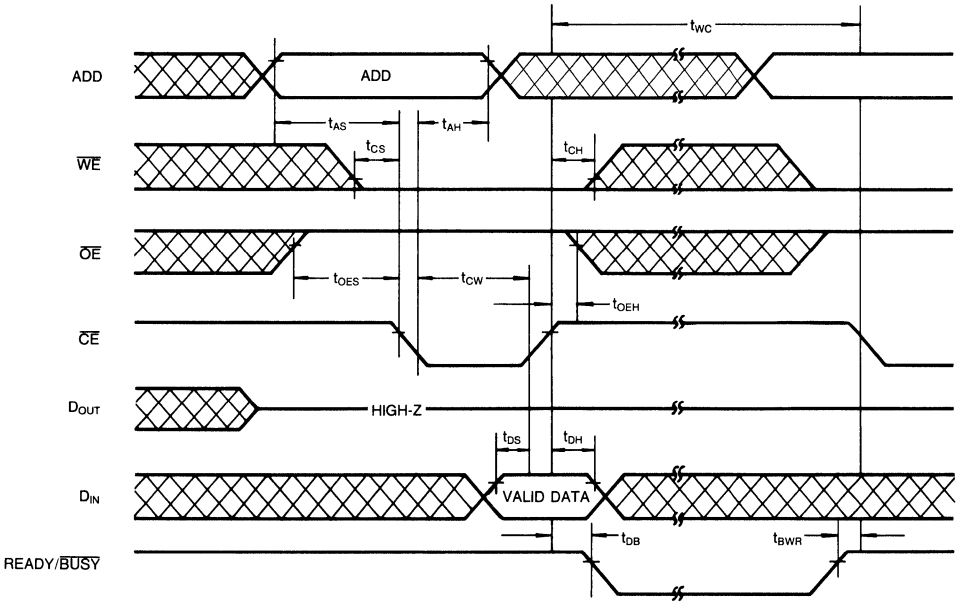


TIMING DIAGRAM (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

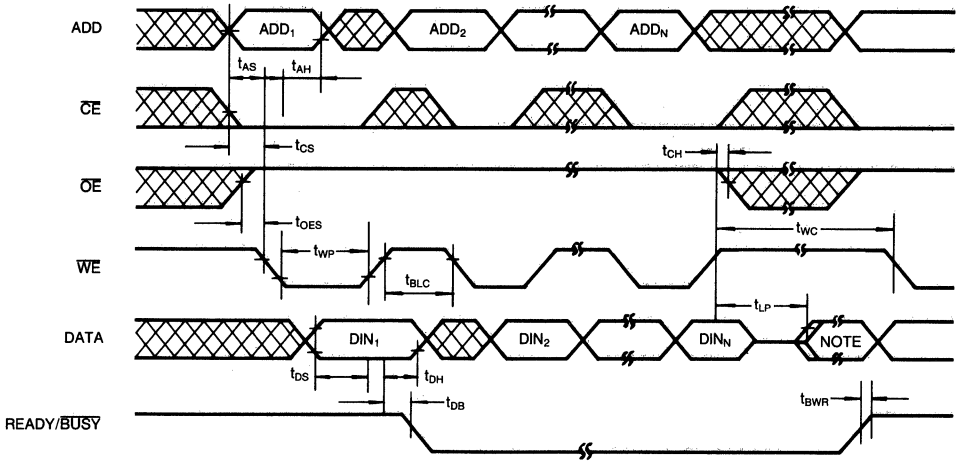


$\overline{CE}$ CONTROLLED WRITE CYCLE

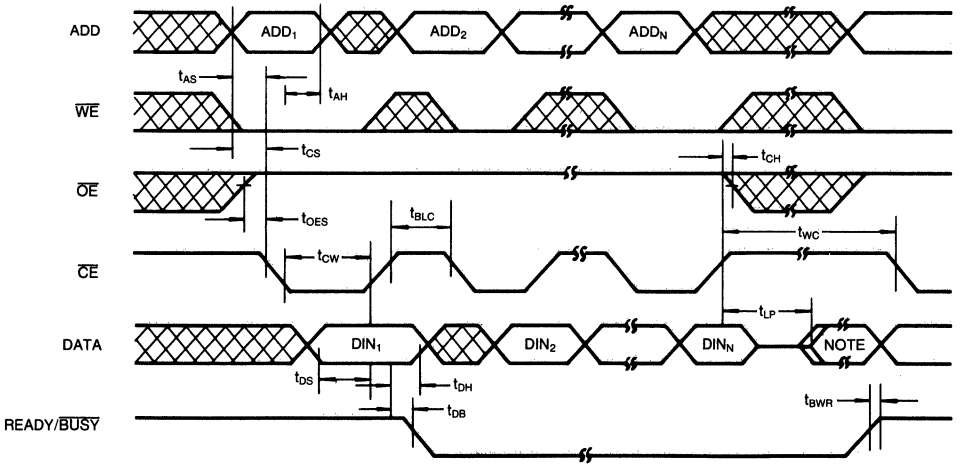


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



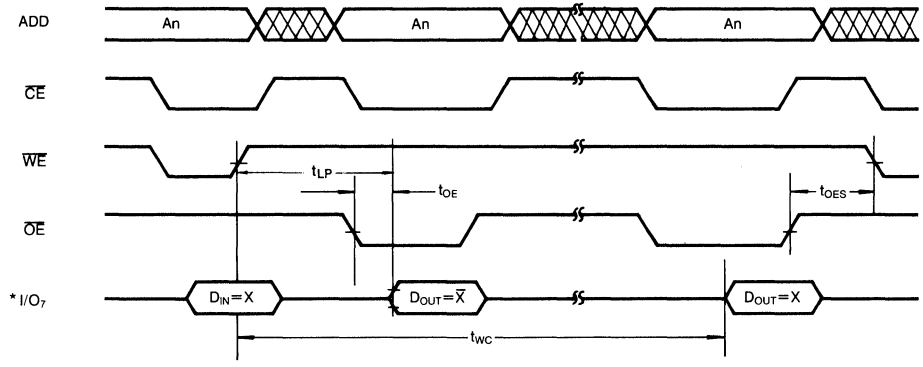
PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



* NOTE: I/O_7 output $\overline{DIN_N}$ when the chip is read.
I/O_6 is toggling between "1" and "0" when the chip is successively read.

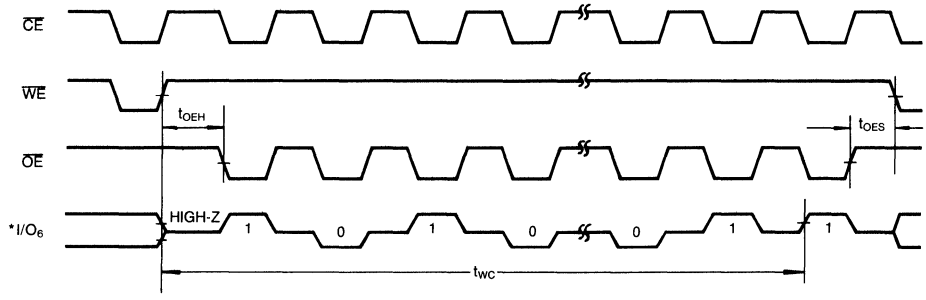
TIMING DIAGRAMS (Continued)

DATA POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the EEPROM.

TOGGLE BIT CYCLE



* During the write cycle, I/O_6 will toggle between "1" and "0".

SAMSUNG ELECTRONICS

DEVICE OPERATION

READ

Reading data from the KM28C64A/65A is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The DATA I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C64A/65A is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64A/65A is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolitile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C64A/65A allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C64A/65A internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C64A/65A by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for the data loading (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loding the data is that the interval between $\overline{WE}$ pulses dose not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low. The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A6-A12) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. the new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64A/65A also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power comsumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C64A/65A to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64A/65A has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than V_{WI}=3.0 volts, the write inhibits V_{CC} level. During power-up, the KM28C64A/65A automatically prevents any write operation for a period of 5ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C64A/65A has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm, followed by a write or page write operation. Once the protection mode is enabled, the KM28C64A/65A will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by exection a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

*** $\overline{\text{DATA}}$ POLLING ***

The KM28C64A/65A features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme dose not require any external hardware. During the write period, any attempt to read of the last byte the EEPROM will produce, at I/O_7. an inverted inverted value of the last I/O_7 data loaded to the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

*** TOGGLE BIT ***

The KM28C64A/65A also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 between "1" and "0". Once the write cycle is complete, the toggling will stop and valid data will be read.

*** READY/$\overline{\text{BUSY}}$ ***

The KM28C65A has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/$\overline{\text{Busy}}$ output is configured as an open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max)-V_{OL}(max)}{I_{OL}+\Sigma I_L} = \frac{5.1V}{2.1mA+\Sigma I_L}$$

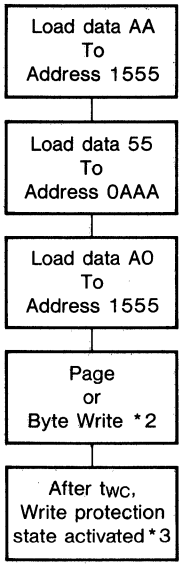
where ΣI_L is the sum of the input currents of all devices tied to the Ready/$\overline{\text{Busy}}$ pin.

ENDURANCE AND DATA RETENTION

KM28C64A/65A is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation. The device also featires an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

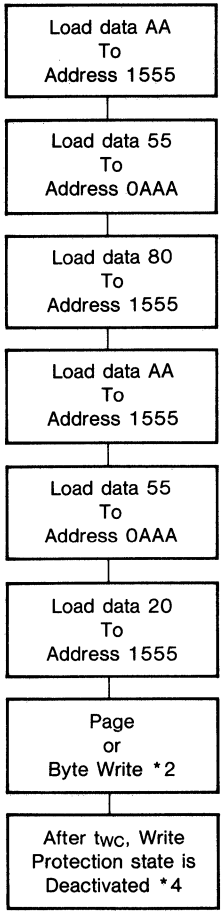
SOFTWARE DATA PROTECTION ALGORITHIM*[1]

SDP Enable Sequence



* Write mode enabled

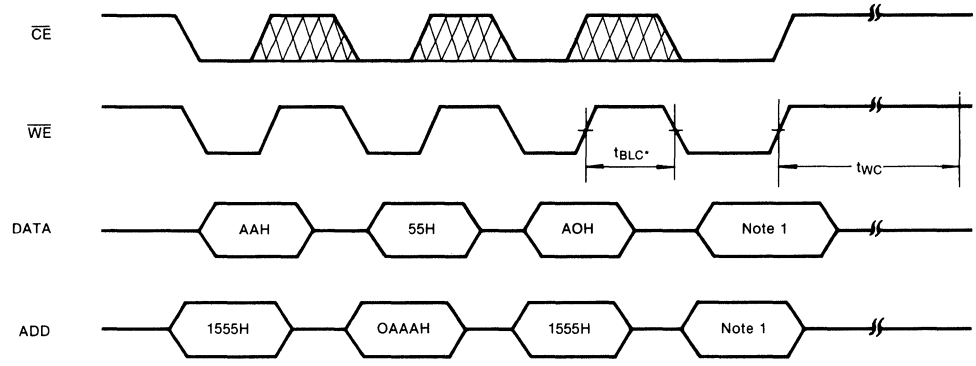
SDP Disable Sequance



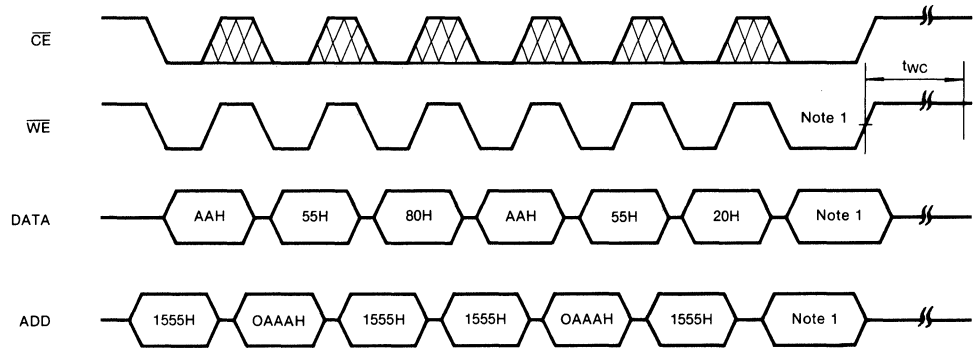
Note: 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{12}-A_0 (HEX)
2. 1 to 64 byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is writtern.
4. Write protection state will be deactived after.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



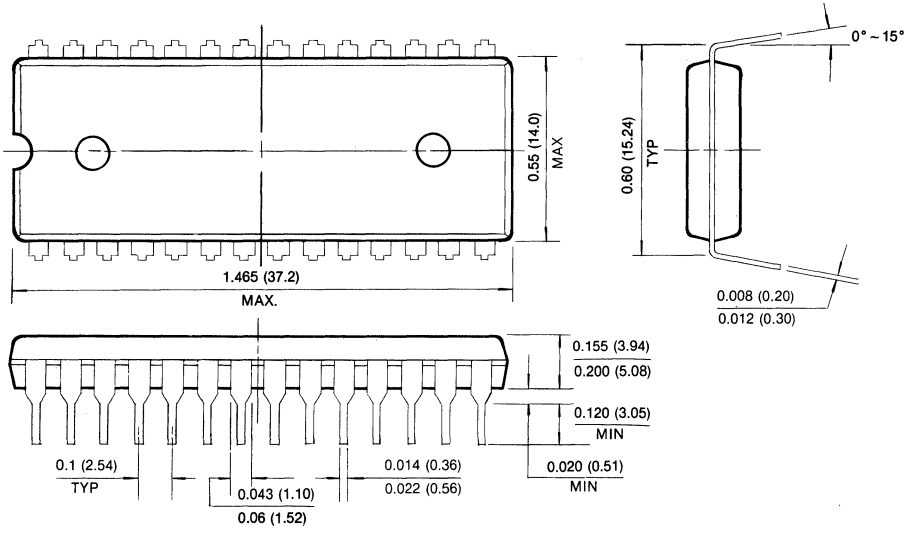
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

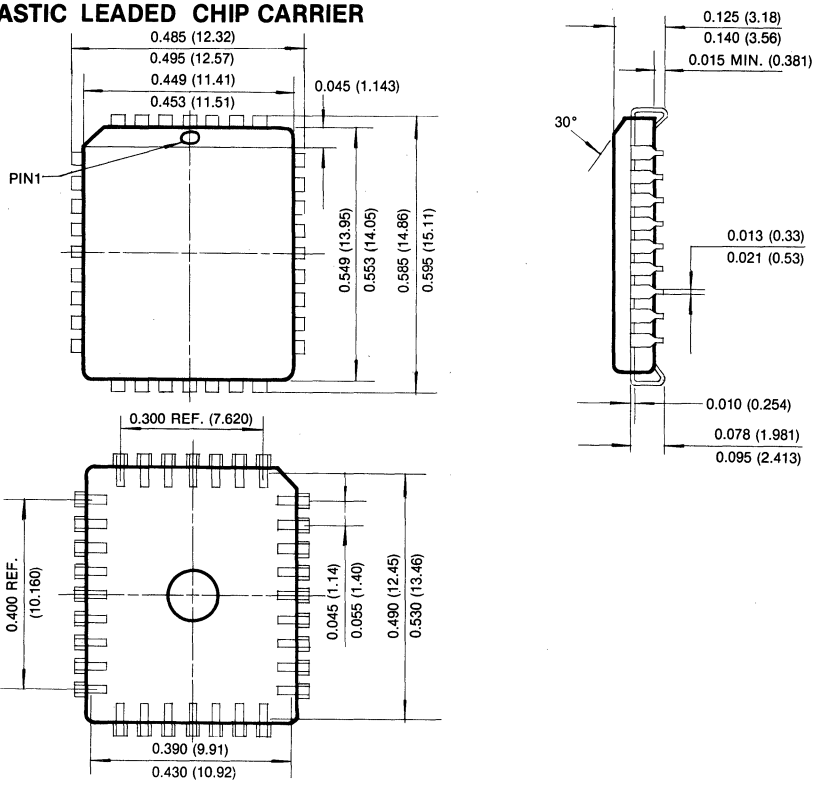
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



8K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C64B/65B: Commercial**
  - **— KM28C64B/65BI: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Internal Erase-Before-Write**
  - **— Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65B)**
- **Fast Write Cycle Time**
  - **— 64-Byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 0.7 seconds**
- **$\overline{\text{Data}}$-Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 90ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating-Gate Technology**
  - **— Endurance: 100,000 Cycle**
  - **— Data Retention: 10 years**
- **JEDEC Byte-wide Memory Pinout**

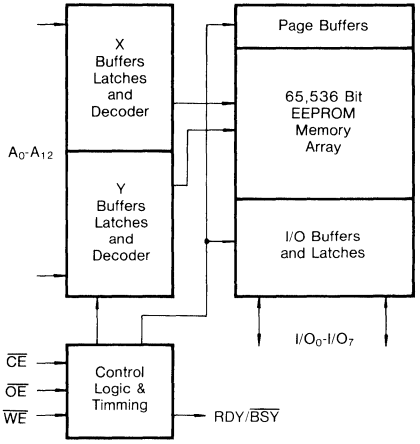
GENERAL DESCRIPTION

The KM28C64B/65B is a 8,192 x 8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

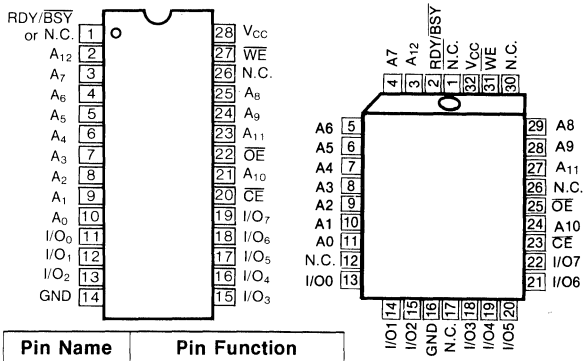
Writing data into the KM28C64B/65B is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 0.7 seconds.

The KM28C64B/65B also features $\overline{\text{Data}}$-polling and a Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware. The KM28C65B features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.
The KM28C64B/65B is designed for applications up to 100,000 write cycles per byte. It's on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{\text{Busy}}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	Com.	T_{bias}	−10 to +125	°C
	Ind.		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C64B/65B: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C64BI/65BI: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's open (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

Note 1: All address toggling from V_{IL} to V_{IH} at 10 MHz

CAPACITANCE ($T_A = 25°C$, f = 1.0 MHz))

Item	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{IL} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{Data}$ Polling	$I/O_7=\overline{D_7}$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

2

AC CHARACTERISTICS

KM28C64B/65B: T_A=0°C to +70°C V_{CC}=5V±10%, unless otherwise noted
KM28C64BI/65BI: T_A=−40°C to +85°C V_{CC}=5V±10%, unless otherwise noted

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM28C64B-09 KM28C65B-09 KM28C64BI-09 KM28C65BI-09		KM28C64B-12 KM28C65B-12 KM28C64BI-12 KM28C65BI-12		KM28C64B-15 KM28C65B-15 KM28C64BI-15 KM28C65BI-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		150		ns
Chip Enable Access Time	t_{CE}		90		120		150	ns
Address Access Time	t_{AA}		90		120		150	ns
Output Enable Access Time	t_{OE}		40		50		60	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	40	0	40	0	40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

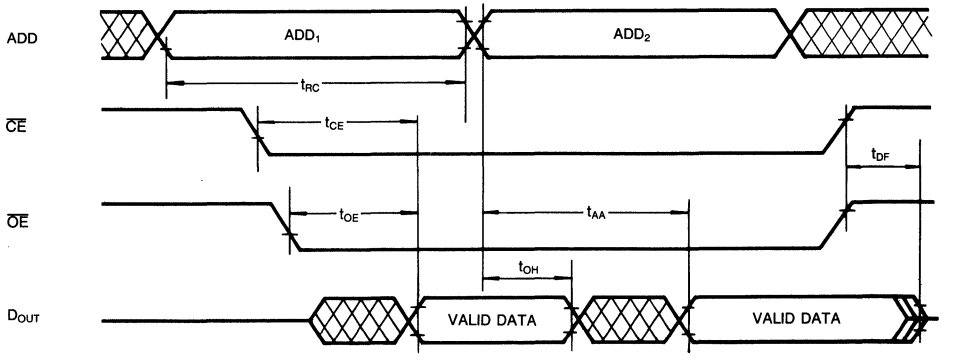
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		5	ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at rising edge of $\overline{WE}$.

TIMING DIAGRAM

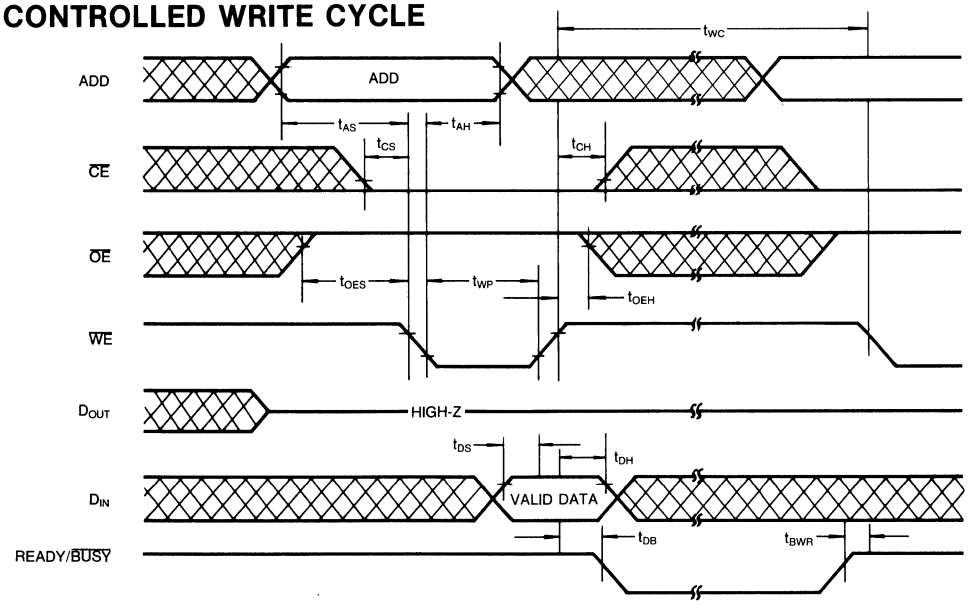
READ CYCLE ($\overline{WE}$=V_{IH})



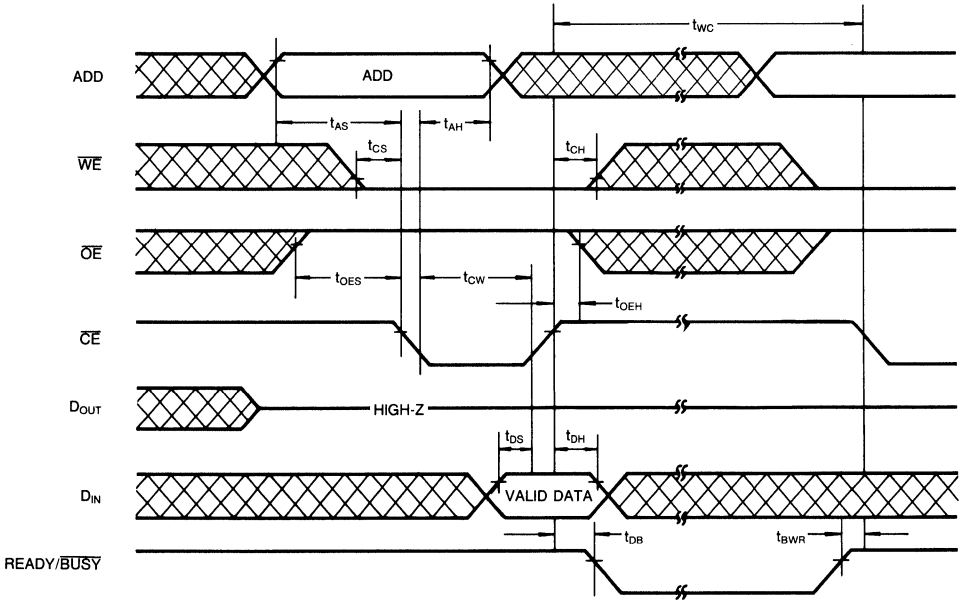
SAMSUNG ELECTRONICS

TIMING DIAGRAM (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

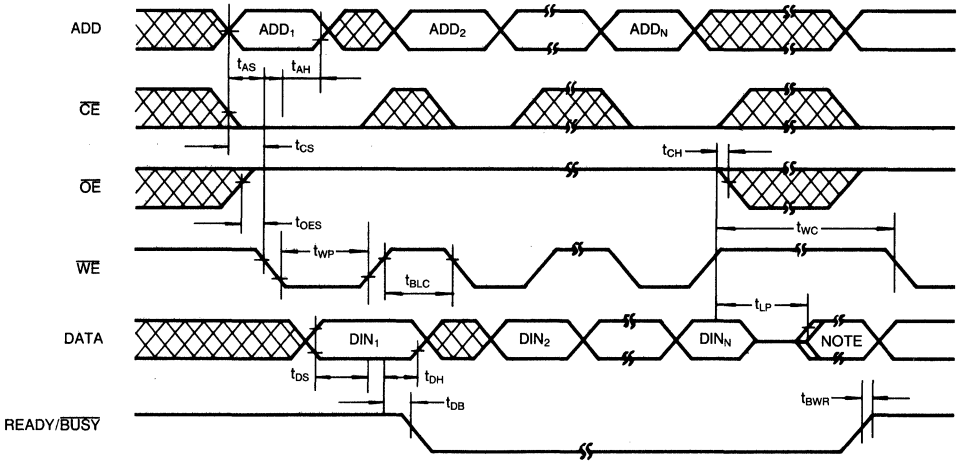


$\overline{CE}$ CONTROLLED WRITE CYCLE

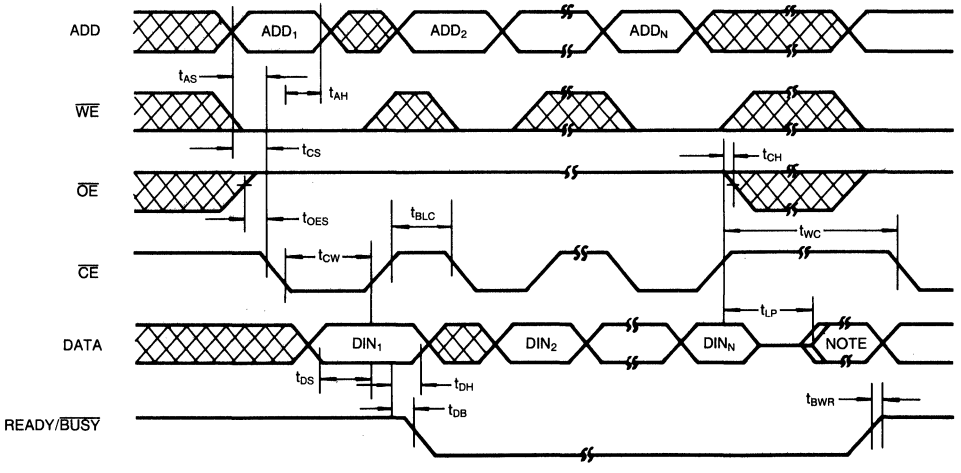


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



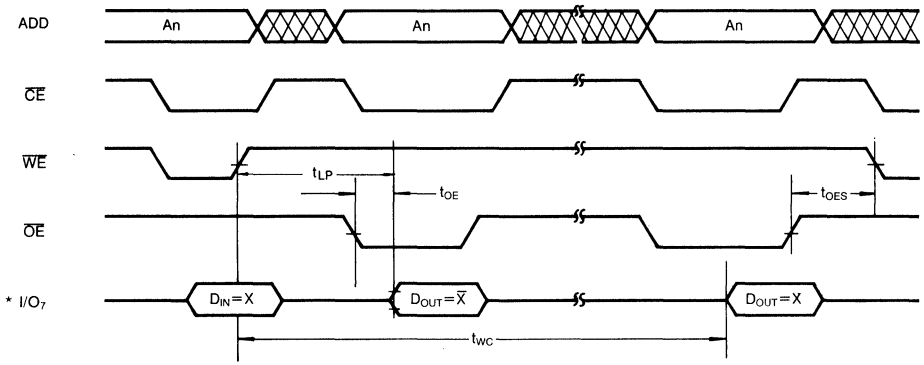
PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



* NOTE: I/O_7 output $\overline{DIN_N}$ when the chip is read.
I/O_6 is toggling between "1" and "0" when the chip is successively read.

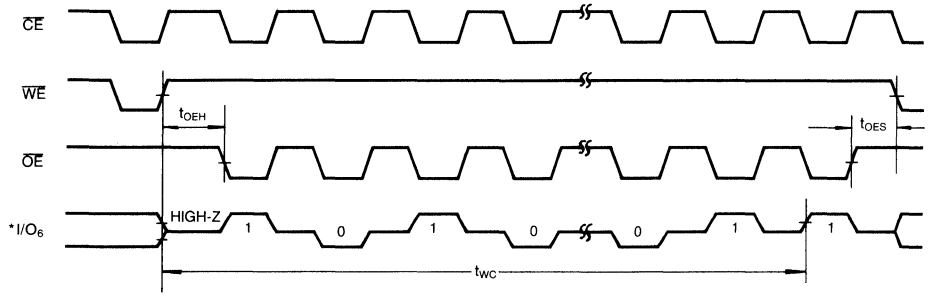
TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the EEPROM.

TOGGLE BIT CYCLE



* During the write cycle, I/O_6 will toggle between "1" and "0".

DEVICE OPERATION

READ

Reading data from the KM28C64B/65B is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The DATA I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C64B/65B is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64B/65B is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolitile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C64B/65B allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C64B/65B internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C64B/65B by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for the data loading (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loding the data is that the interval between $\overline{WE}$ pulses dose not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low. The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A6-A12) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. the new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64B/65B also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power comsumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C64B/65B to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64B/65B has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than V_{WI}=3.0 volts, the write inhibits V_{CC} level. During power-up, the KM28C64B/65B automatically prevents any write operation for a period of 5ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

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The KM28C64B/65B has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm, followed by a write or page write operation. Once the protection mode is enabled, the KM28C64B/65B will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by exection a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

*** $\overline{\text{DATA}}$ POLLING ***

The KM28C64B/65B features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme dose not require any external hardware. During the write period, any attempt to read of the last byte the EEPROM will produce, at I/O_7, an inverted inverted value of the last I/O_7 data loaded to the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

*** TOGGLE BIT ***

The KM28C64B/65B also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 between "1" and "0". Once the write cycle is complete, the toggling will stop and valid data will be read.

*** READY/$\overline{\text{BUSY}}$ ***

The KM28C65B has a Ready/$\overline{\text{Busy}}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/$\overline{\text{Busy}}$ output is configured as an open-drain driver there-by allowing two or more Ready/$\overline{\text{Busy}}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{2.1mA + \Sigma I_L}$$

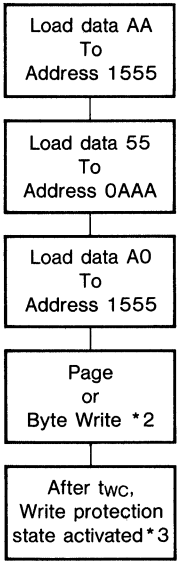
where ΣI_L is the sum of the input currents of all devices tied to the Ready/$\overline{\text{Busy}}$ pin.

ENDURANCE AND DATA RETENTION

KM28C64B/65B is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation. The device also featires an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

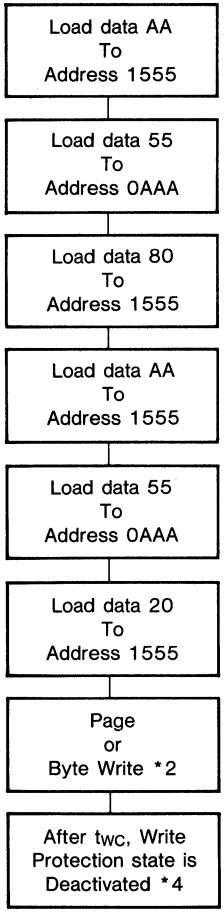
SOFTWARE DATA PROTECTION ALGORITHIM*[1]

SDP Enable Sequence



* Write mode enabled

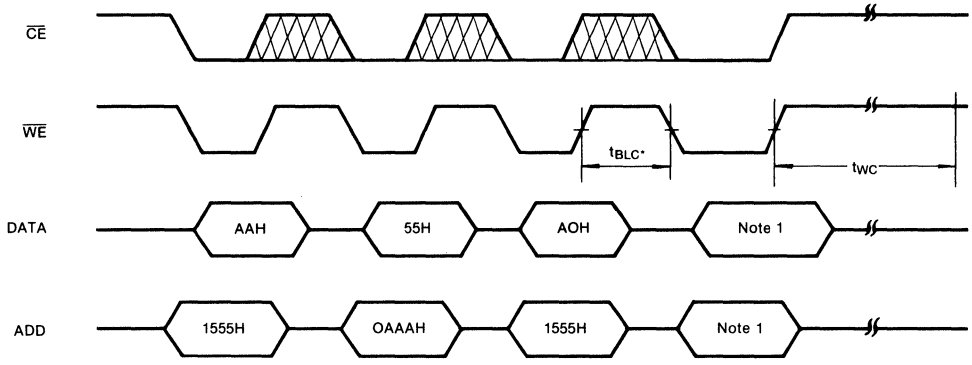
SDP Disable Sequance



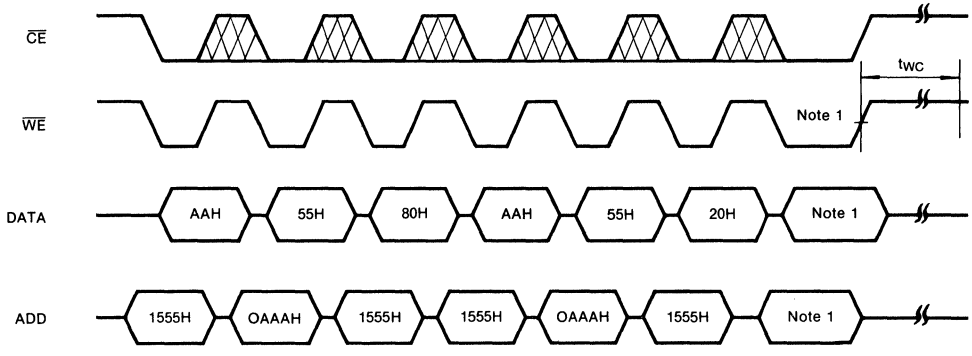
Note: 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{12}-A_0 (HEX)
2. 1 to 64 byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is writtern.
4. Write protection state will be deactived after.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



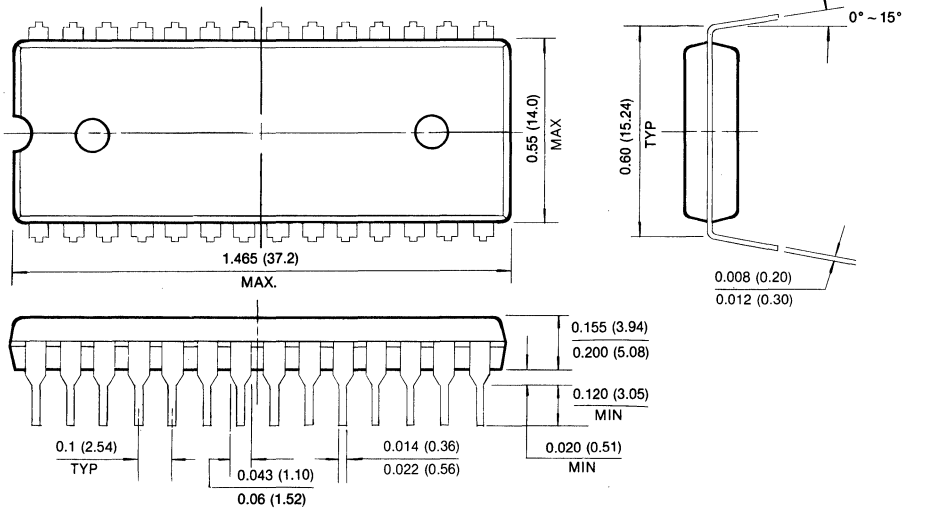
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

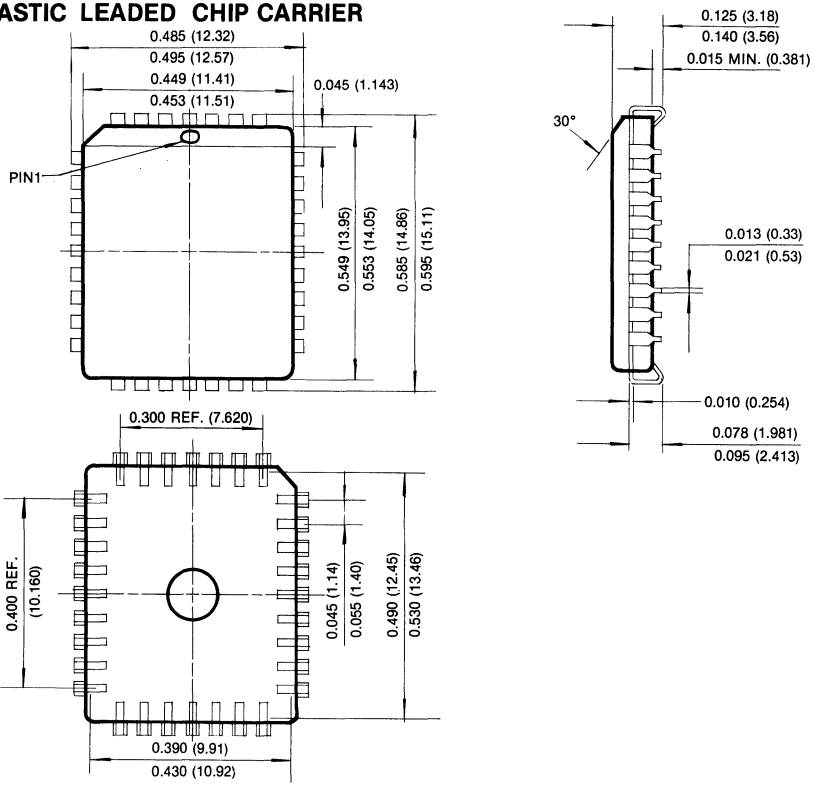
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



32K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C256: Commercial**
  - **— KM28C256I: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
- **Fast Write Cycle Time**
  - **— 64-byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 2.5 seconds**
- **Data Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating—Gate Technology**
  - **— Endurance: 100,000**
  - **— Data Retention: 10 years**
- **JEDEC Approved Byte-Wide Pinout**

GENERAL DESCRIPTION

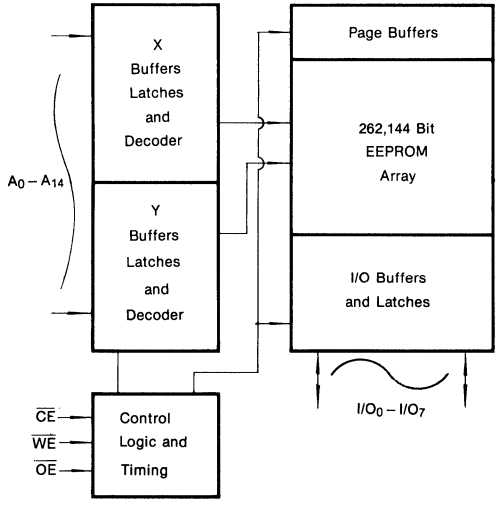
The KM28C256 is a 32,768 x 8 bit Electrically Erasable Programable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C256 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 2.5 seconds.

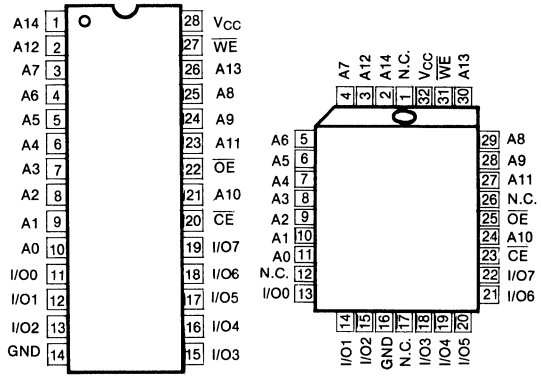
The KM28C256 also features Data polling and Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware.

The KM28C256 is designed for applications up to 100,000 write cycles per byte. Its on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C256: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C256I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open, all addresses* (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{\text{Data}}$-Polling	$I/O_7 = \overline{D_7}$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C256: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C256I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C256-15 KM28C256I-15		KM28C256-20 KM28C256I-20		KM28C256-25 KM28C256I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

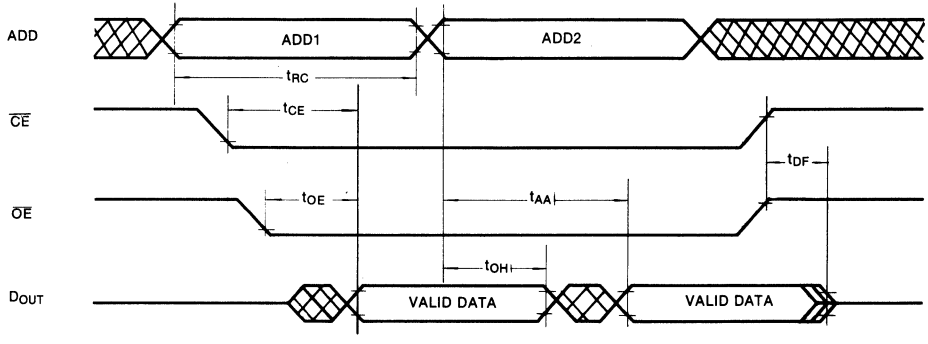
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		5	ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

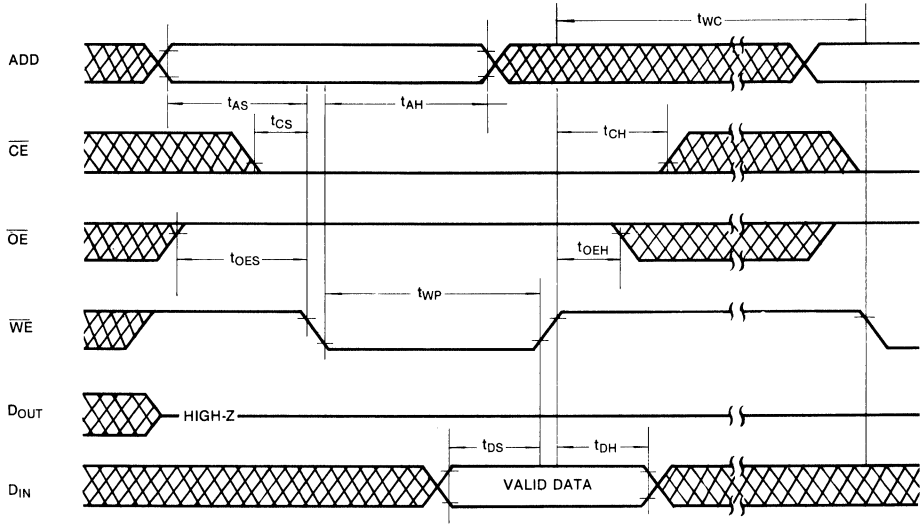
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

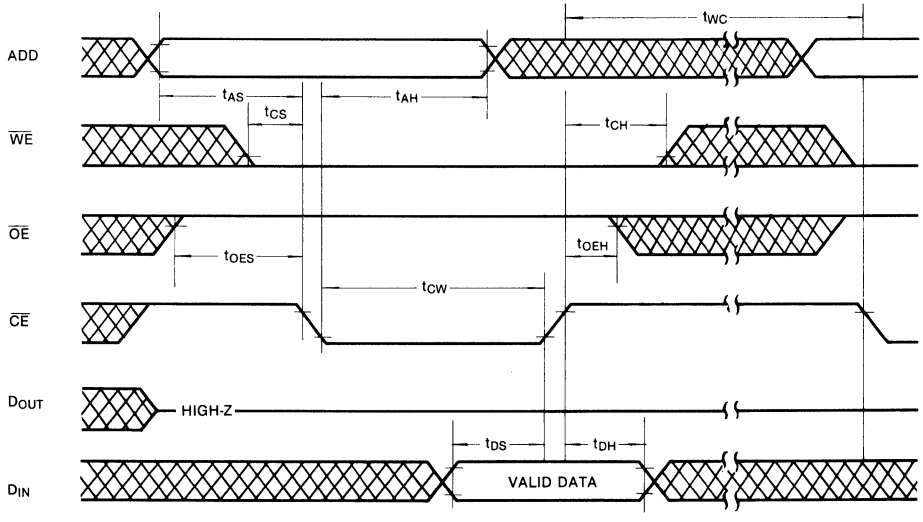


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

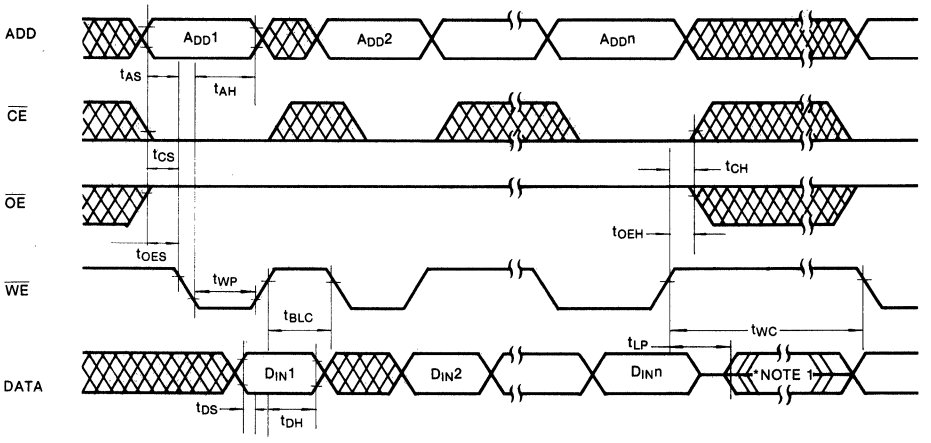


$\overline{CE}$ CONTROLLED WRITE CYCLE

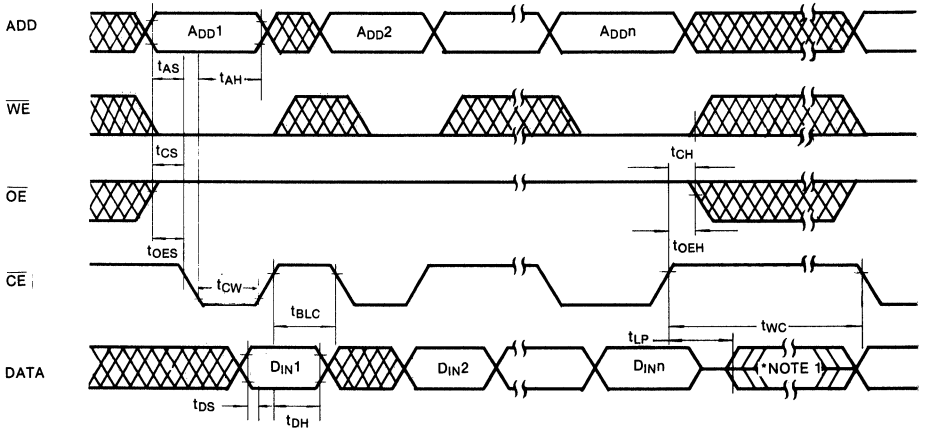


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



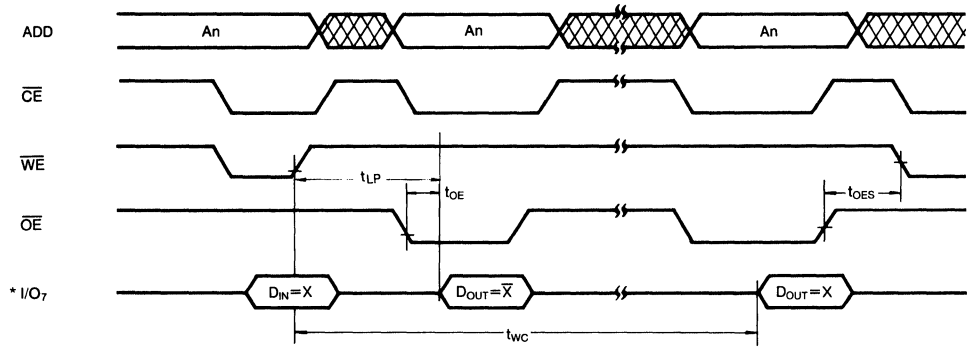
PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $\overline{D_{INn}}$ when the chip is read.
I/O_6 is toggling between "1" and "0" when
the chip is successively read

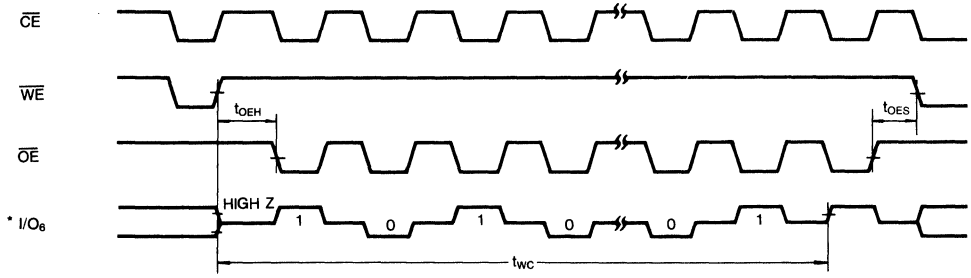
TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the EEPROM.

TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

SAMSUNG ELECTRONICS

DEVICE OPERATION

READ

Reading data from the KM28C256 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

WRITE

Writing data into the KM28C256 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C256 is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C256 allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C256 internal registers and a nonvolatile write period, in which the loaded data in the registers is written to the EEPROM cells of the selected page.

Data is loaded into the KM28C256 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A_6-A_{14}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C256 also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C256 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C256 has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.0$ volts, the write inhibit V_{CC} level. During power-up, the KM28C256 automatically prevents any write operation for a period of 5ms (min.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C256 has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operations if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing a short SDP enable software algorithm, followed by a write operation, either a single byte write or page write operation. Once the protection mode is enabled, the KM28C256 will not write any data if the SDP enable software algorithm is not preceded. The data protection function can be disabled by executing a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

**** DATA POLLING ****

The KM28C256 features DATA-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read of last byte the EEPROM will produce, at I/O_7, an inverted value of the last I/O_7 data loaded in to the EEPROM(I/O_0-IO_6 are at the high impedance state).

True data will be produced at all I/O's once the write cycle has been completed.

**** TOGGLE BIT ****

The KM28C256 also provides a toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, successive attempts to read the EEPROM will toggle I/O_6 between '1' and '0'. Once the write cycle is complete, the toggling will stop and valid data will be read.

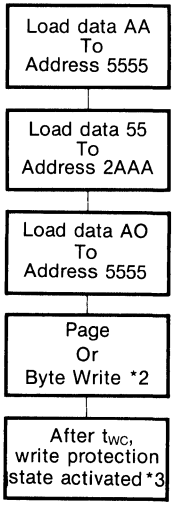
ENDURANCE AND DATA RETENTION

The KM28C256 is designed for applications requiring up to 100,000 write cycles per byte and ten years of data retention. This means that each byte can be reliably written 100,000 times without degrading device operation. The device also features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

2

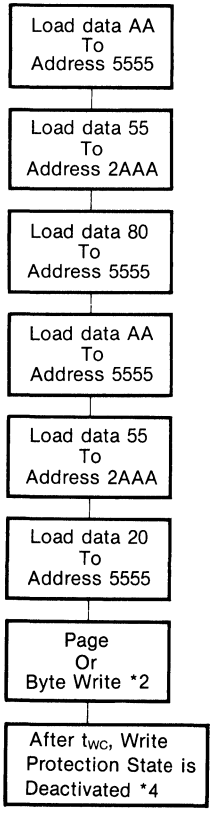
SOFTWARE DATA PROTECTION ALGORITHM*1

SDP Enable Sequence



*Write mode enabled

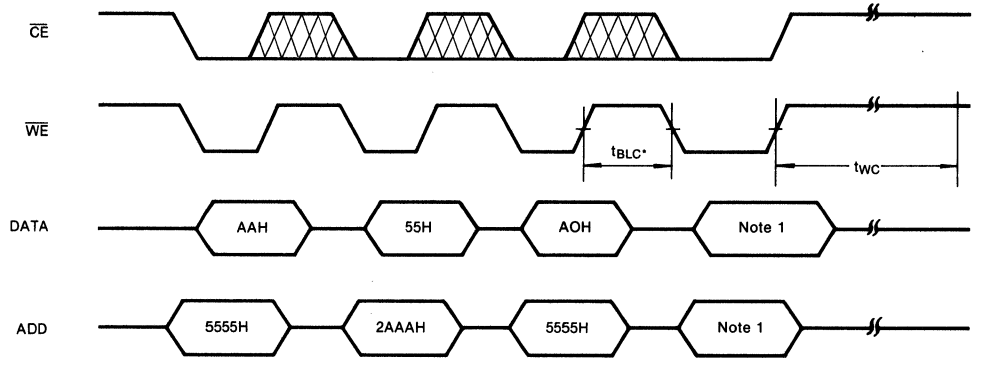
SDP Disable Sequence



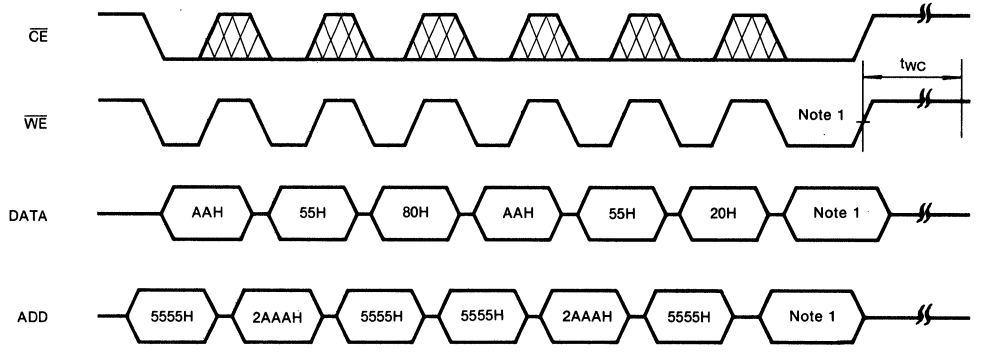
Notes 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{14}-A_0 (HEX)
2. 1 to 64-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is written.
4. Write protection state will be deactivated after t_{WC} even if no data is written.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



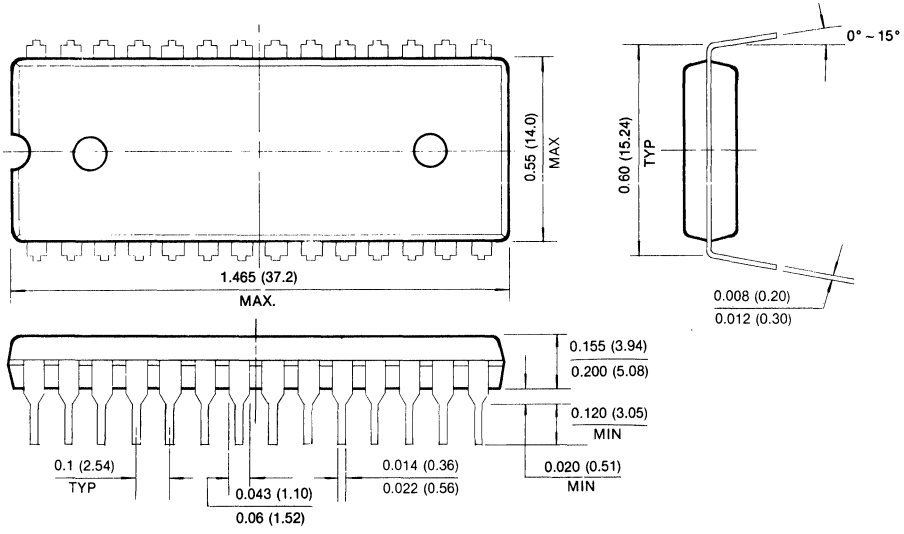
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

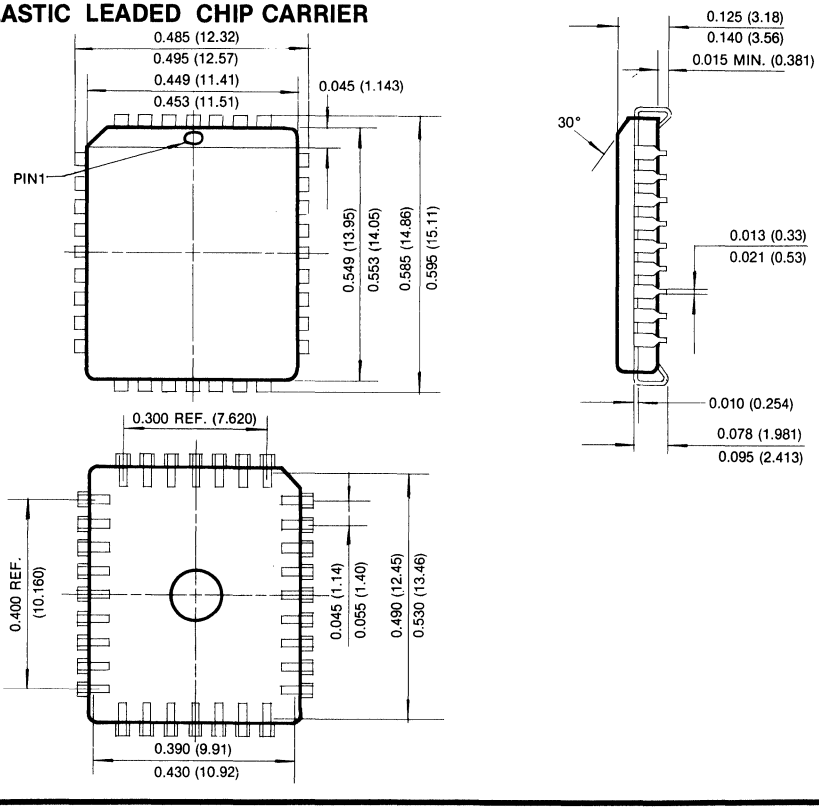
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



32K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C256A: Commercial**
  - **— KM28C256AI: Industrial**
- **Simple Byte Write & Page Write**
  - **— Single TTL Level Write Signal**
  - **— Internal Address and Data Latch**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
- **Fast Write Cycle Time**
  - **— 64-byte Page Write Operation**
  - **— 5ms Byte and Page Write Cycle Time**
  - **— Complete Memory Rewrite: 2.5 seconds**
- **$\overline{\text{Data}}$ Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 90ns**
- **Power: 100μA—Standby (max.)**
  40mA—Operating (max.)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating—Gate Technology**
  - **— Endurance: 100,000**
  - **— Data Retention: 10 years**
- **JEDEC Approved Byte-Wide Pinout**

GENERAL DESCRIPTION

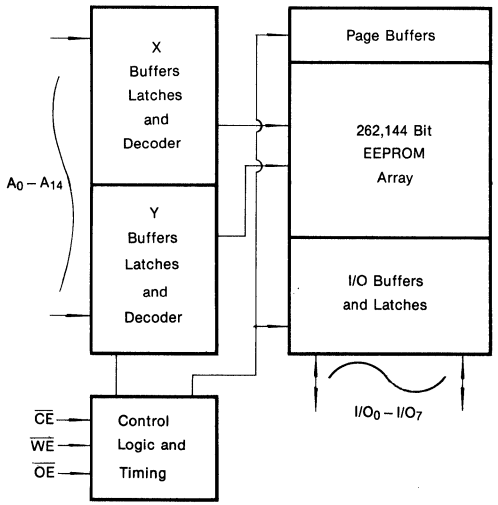
The KM28C256A is a 32,768 x 8 bit Electrically Erasable Programable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C256A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 2.5 seconds.

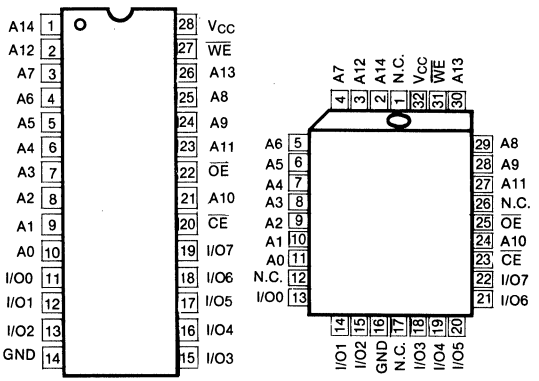
The KM28C256A also features $\overline{\text{Data}}$ polling and Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware.

The KM28C256A is designed for applications up to 100,000 write cycles per byte. Its on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

KM28C256A: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C256AI: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open, all addresses* (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$, all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 10 MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{Data}$-Polling	$I/O_7 = \overline{D_7}$	Active
			Toggle Bit	I/O_6	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C256A: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C256AI: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C256A-09 KM28C256AI-09		KM28C256A-12 KM28C256AI-12		KM28C256A-15 KM28C256AI-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		150		ns
Chip Enable Access Time	t_{CE}		90		120		150	ns
Address Access Time	t_{AA}		90		120		150	ns
Output Enable Access Time	t_{OE}		40		50		60	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	50	0	50	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

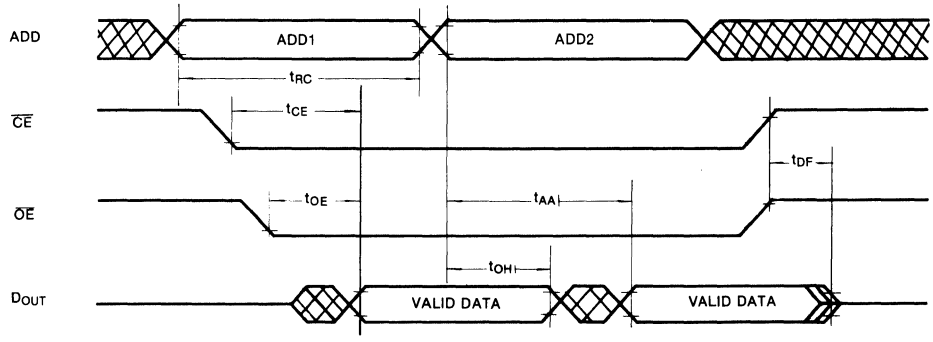
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		5	ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

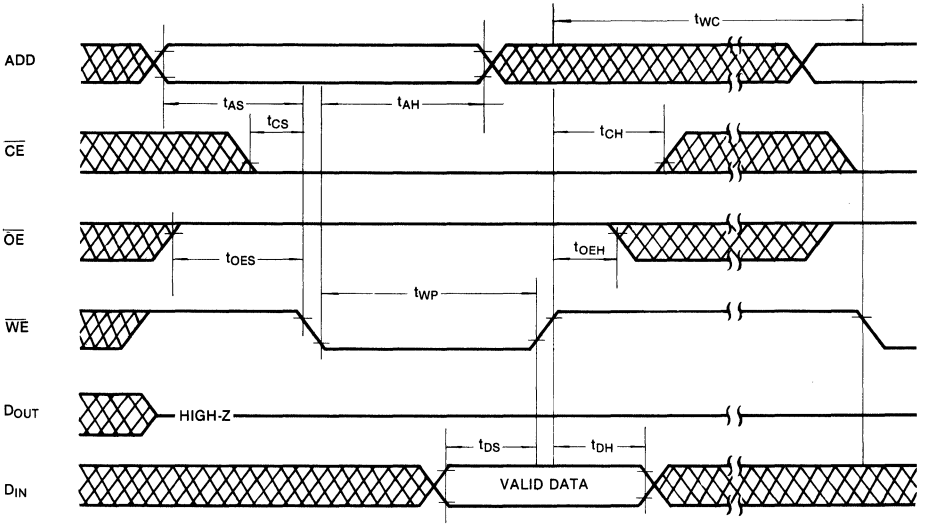
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

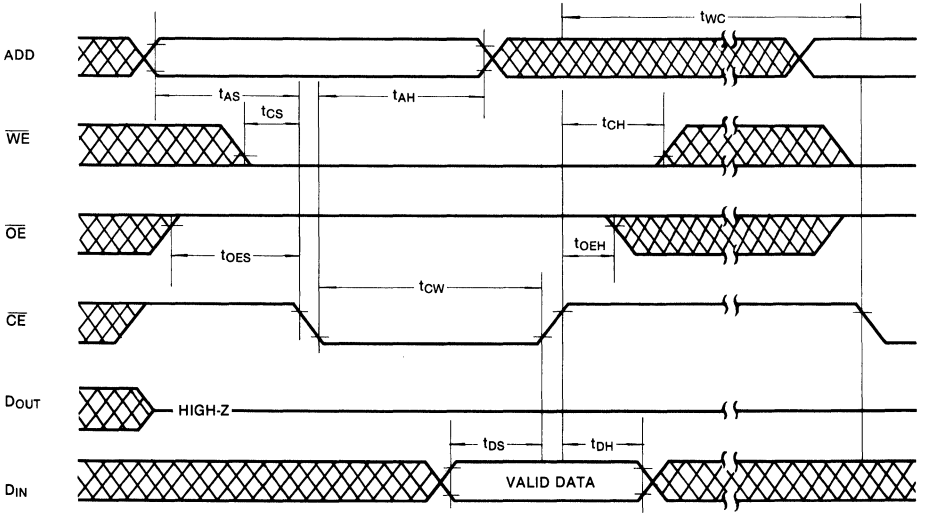


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

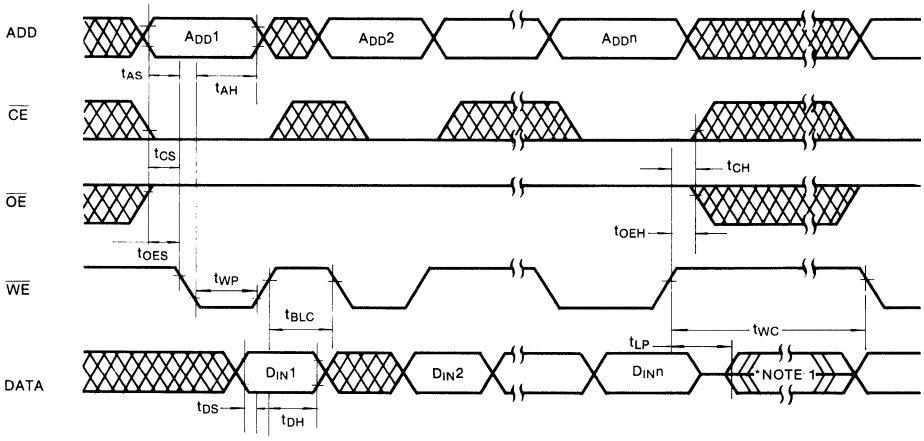


$\overline{CE}$ CONTROLLED WRITE CYCLE

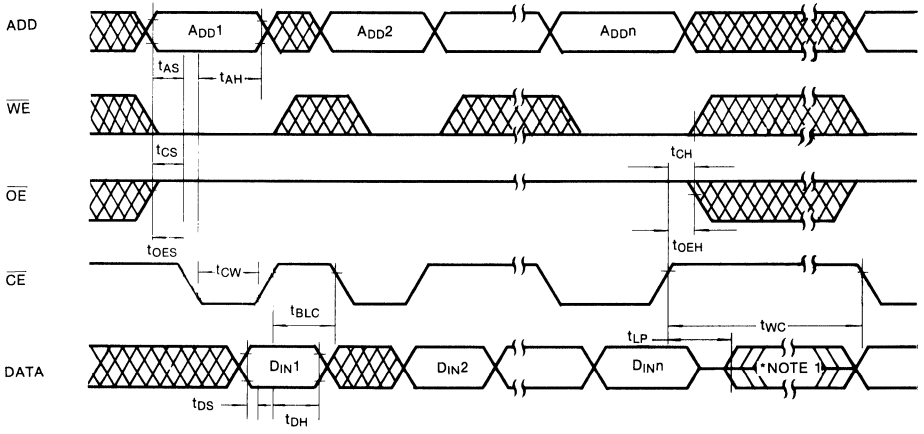


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



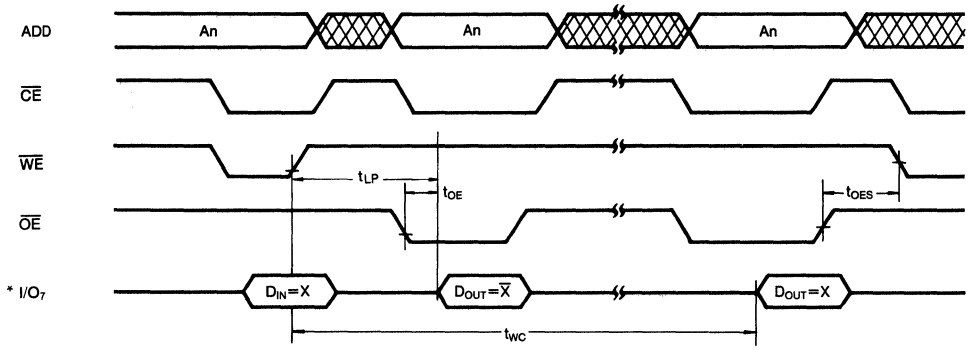
PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $\overline{D_{INn}}$ when the chip is read.
I/O_6 is toggling between "1" and "0" when
the chip is successively read

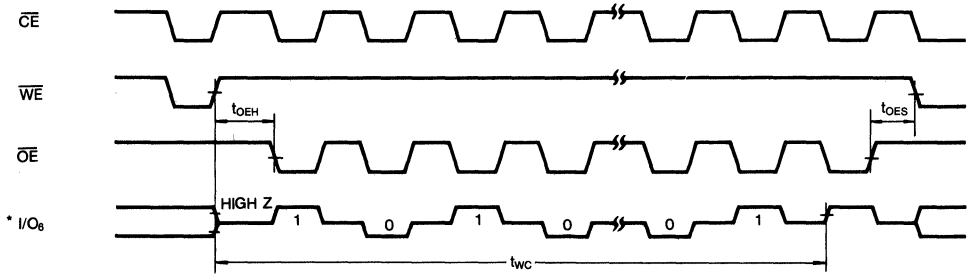
TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the EEPROM.

TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM28C256A is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

WRITE

Writing data into the KM28C256A is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C256A is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C256A allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C256A internal registers and a nonvolatile write period, in which the loaded data in the registers is written to the EEPROM cells of the selected page.

Data is loaded into the KM28C256A by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_5) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The nonvolatile write starts if $\overline{WE}$ stays high for at least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A_6-A_{14}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C256A also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C256 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C256A has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.0$ volts, the write inhibit V_{CC} level. During power-up, the KM28C256 automatically prevents any write operation for a period of 5ms (min.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C256A has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operations if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing a short SDP enable software algorithm, followed by a write operation, either a single byte write or page write operation. Once the protection mode is enabled, the KM28C256A will not write any data if the SDP enable software algorithm is not preceded. The data protection function can be disabled by executing a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

DEVICE OPERATION (Continued)

WRITE COMPLETION INDICATORS

**** DATA POLLING ****

The KM28C256A features DATA-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read of last byte the EEPROM will produce, at I/O_7, an inverted value of the last I/O_7 data loaded into the EEPROM True data will be produced at all I/O's once the write cycle has been completed.

**** TOGGLE BIT ****

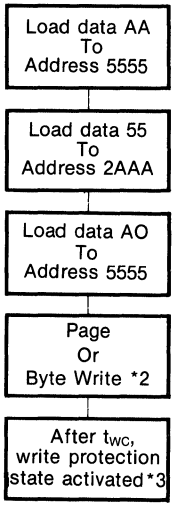
The KM28C256A also provides a toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, successive attempts to read the EEPROM will toggle I/O_6 between '1' and '0'. Once the write cycle is complete, the toggling will stop and valid data will be read.

ENDURANCE AND DATA RETENTION

The KM28C256A is designed for applications requiring up to 100,000 write cycles per byte and ten years of data retention. This means that each byte can be reliably written 100,000 times without degrading device operation. The device also features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

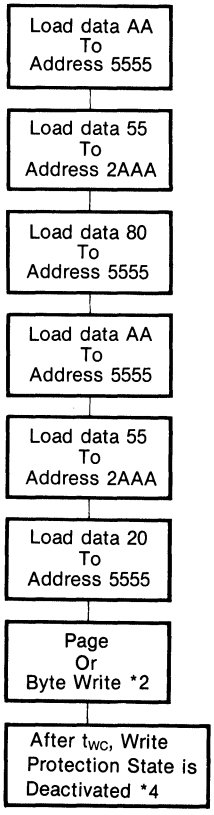
SOFTWARE DATA PROTECTION ALGORITHM*1

SDP Enable Sequence



*Write mode enabled

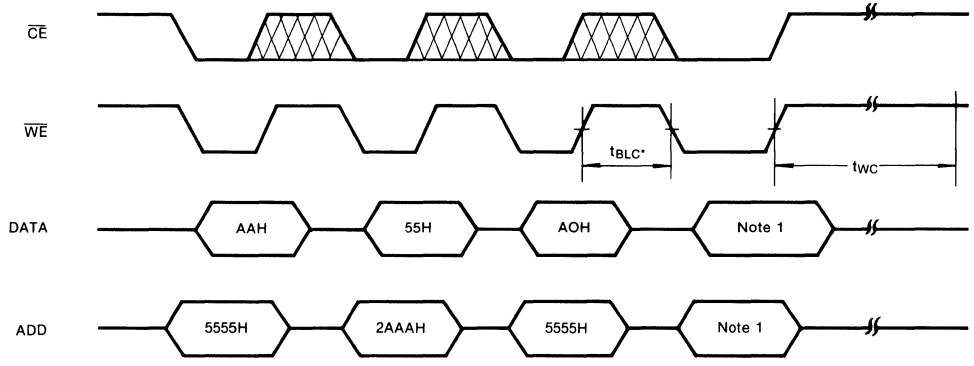
SDP Disable Sequence



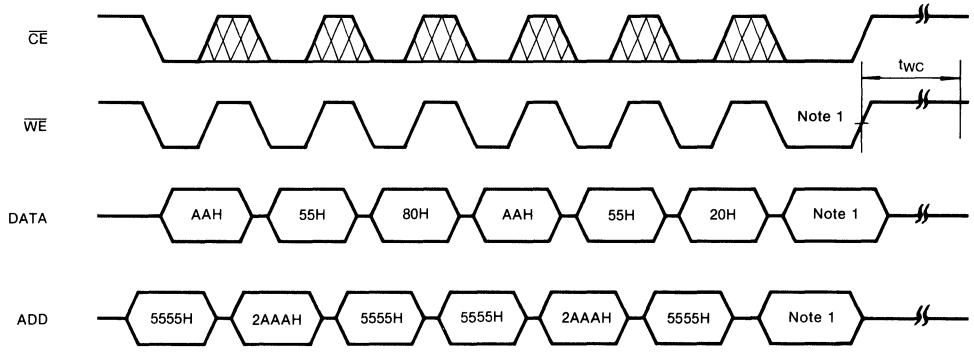
Notes 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{14}-A_0 (HEX)
2. 1 to 64-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is written.
4. Write protection state will be deactivated after t_{WC} even if no data is written.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



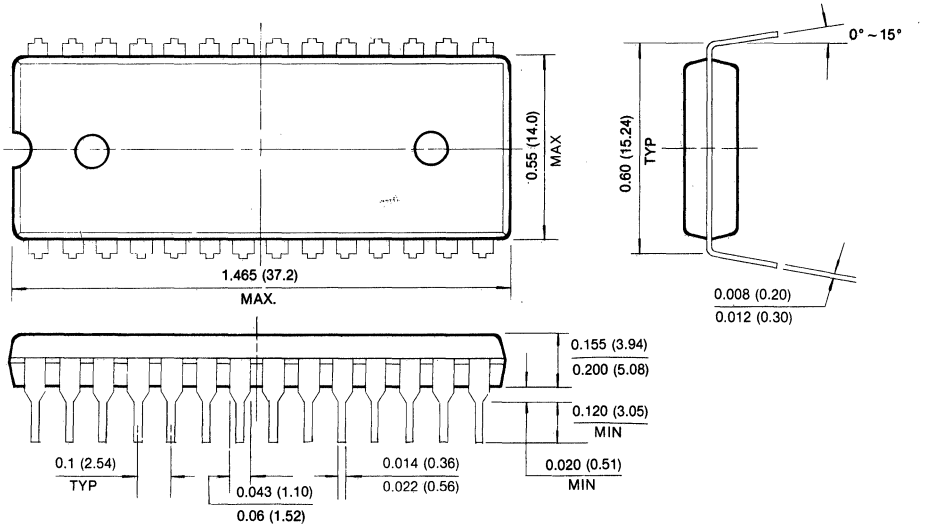
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 64 byte of data maybe loaded in random order.

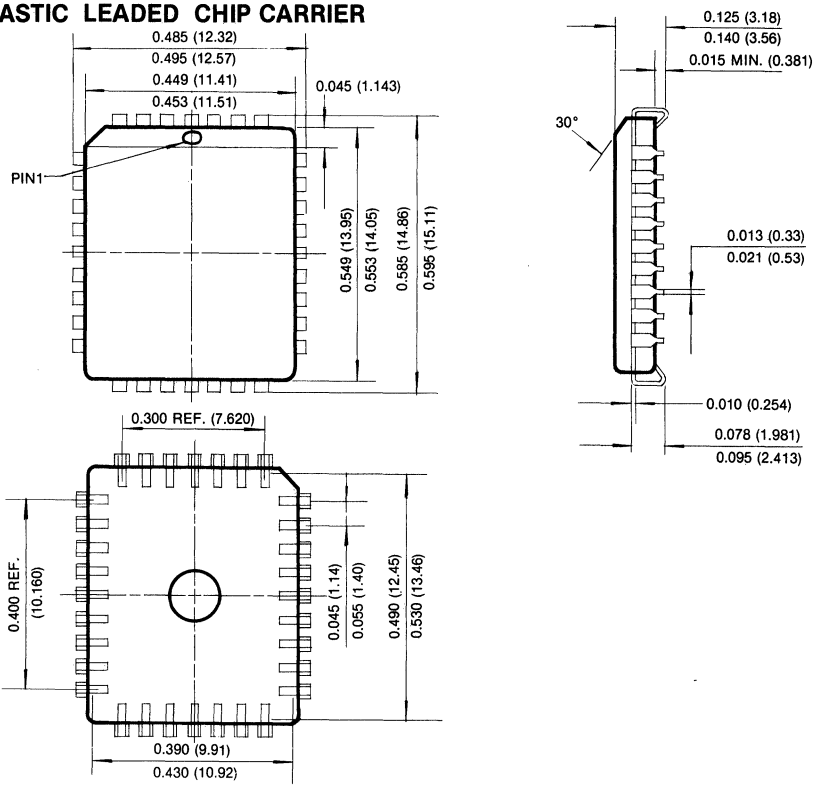
PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER



128K x 8 Bit CMOS Flash Memory

FEATURES

- **Fast Read Access Time: 90ns**
- **Single 5 Voltage Supply**
- **128 Byte Page Write Operation**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Write Timing**
  - **Automatic Page Erase Before Write**
- **Fast Write Cycle Time**
  - **Page Write Time: 10ms**
  - **Chip Erase Time: 10ms**
- **Low Power Dissipation**
  - **100μA: Standby (max)**
  - **40mA: Operating (max)**
- **Hardware and Software Data Protection**
- **$\overline{\text{Data}}$ Polling and Toggle Bit**
- **Reliable CMOS Floating-Gate Technology**
  - **Endurance: 100,000**
  - **Data Retention: 10 Years**
- **JEDEC Standard Byte-wide Pinout**
  - **32-Pin DIP/PLCC/TSOP1**

GENERAL DESCRIPTION

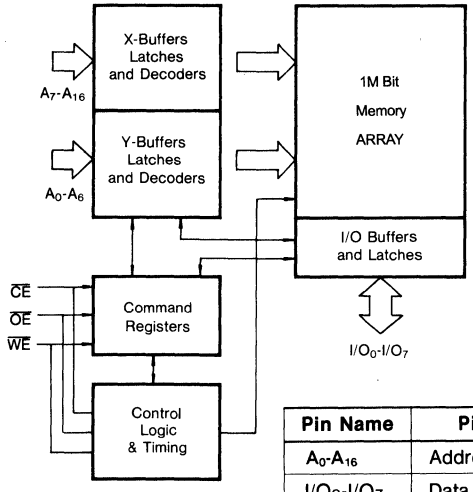
The KM29C010 is a 131,072×8 bit Flash Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM29C010 is very simple. Writing the KM29C010 is performed on a page basis; 128 bytes of data are loaded into the page buffer and then simultaneously written into the array.

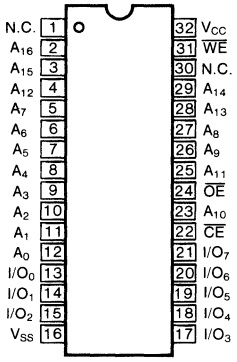
The KM29C010 features $\overline{\text{Data}}$ polling and Toggle bit schemes that signal the processor an early completion of a write cycle without requiring any external hardware.

2

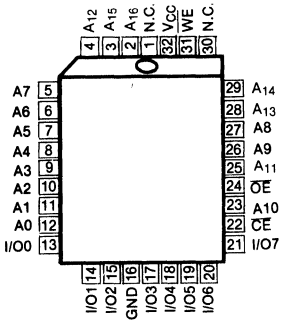
BLOCK DIAGRAM



PIN CONFIGURATION

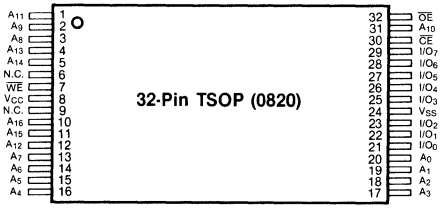


KM29C010



KM29C010J

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection*
V_{CC}	+5V
GND	Ground



KM29C010T

* Don't Care

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Short Circuit Output Current	I_{OS}	5	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Note: Voltage reference to V_{SS}, T_A=0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, all addresses* (Note 1)	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all I/O's=open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}−0.2, all I/O's=open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to 5.5V	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0		V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 8.4MHz.
2. V_{IL}(min) = −3.0V for ≤10ns Pulse.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IO}=0V	—	6	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7=\overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	Toggle Bit	I/O_6	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

Note: $T_A=0°C$ to $70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted.

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L=100pF$

READ CYCLE

Parameter	Symbol	KM29C010-09*		KM29C010-10		KM29C010-12		KM29C010-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		100		120		150		ns
Chip Enable Access Time	t_{CE}		90		100		120		150	ns
Address Access Time	t_{AA}		90		100		120		150	ns
Output Enable Access Time	t_{OE}		40		40		50		60	ns
Output or Chip Disable to Output High-Z	t_{DF}	0	30	0	30	0	40	0	50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

*Preliminary Product

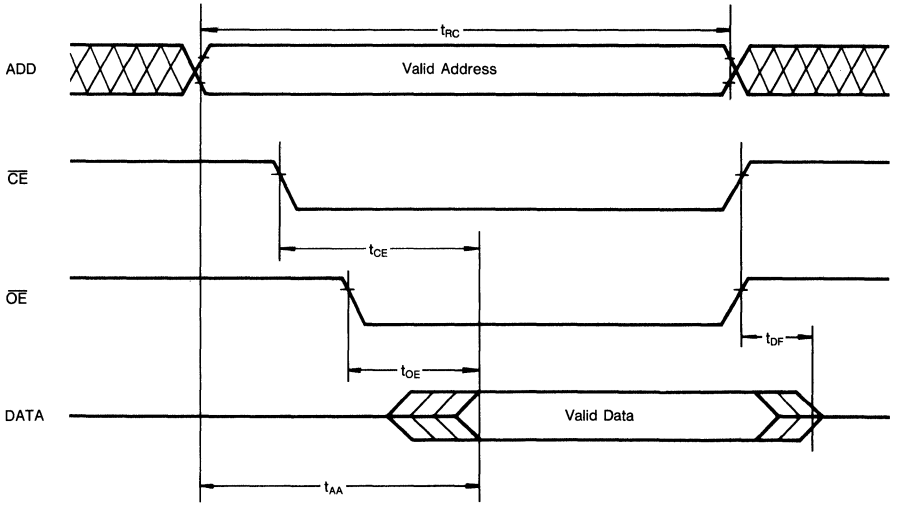
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}		10	ms
Address Set-Up Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Write Set-Up Time	t_{CS}	0	—	ns
Write Hold Time	t_{CH}	0	—	ns
$\overline{CE}$ Pulse Width	t_{CW}	90	—	ns
Output Enable Set-Up Time	t_{OES}	0	—	ns
Output Enable Hold Time	t_{OEH}	0	—	ns
$\overline{WE}$ Pulse Width	t_{WP}	90	—	ns
Data Set-Up Time	t_{DS}	50	—	ns
Data Hold Time	t_{DH}	0	—	ns
Byte Load Cycle Time	t_{BLC}	0.1	150	μs
Last Byte Loaded to Data Polling	t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a raising edge of $\overline{WE}$.

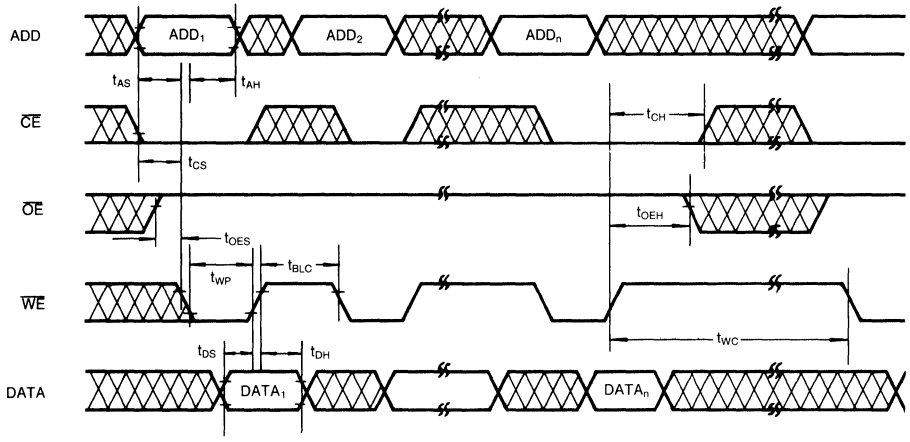
TIMING DIAGRAMS

READ CYCLE ($\overline{WE}$=V_{IH})

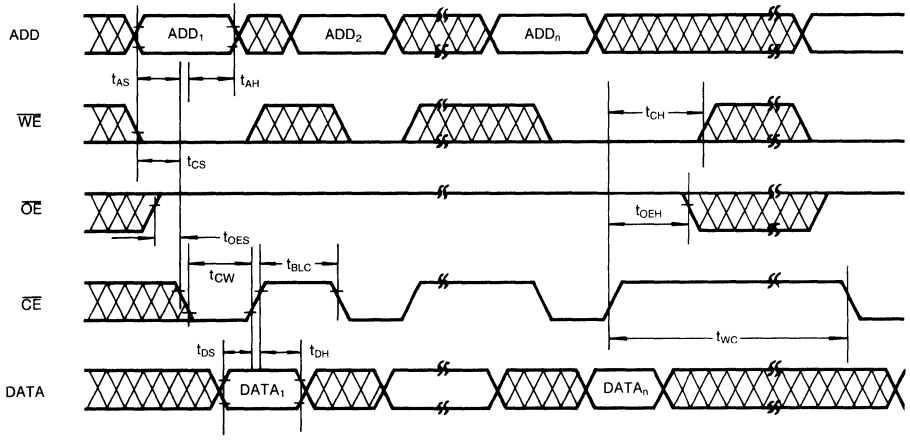


TIMING DIAGRAM (Continued)

PAGE PROGRAM CYCLE ($\overline{WE}$ Controlled Write Cycle)

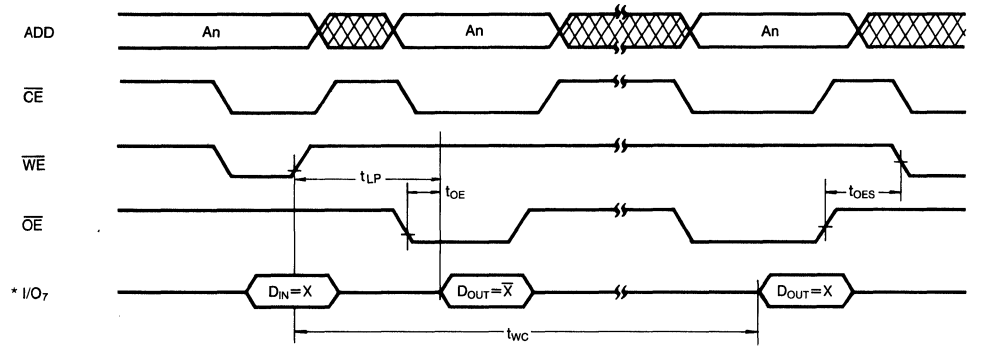


PAGE PROGRAM CYCLE ($\overline{CE}$ Controlled Write Cycle)



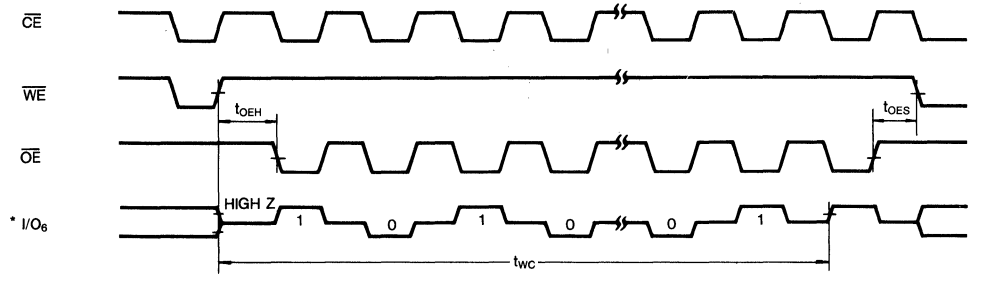
TIMING DIAGRAMS (Continued)

$\overline{\text{DATA}}$ POLLING CYCLE



* During the write cycle, I/O_7 will produce an inverted data of the last I/O_7 data, loaded into the Flash.

TOGGLE BIT CYCLE



*During the write cycle, I/O_6 will toggle between '1' and '0'

DEVICE OPERATION

READ

Reading data from the KM29C010 is similar to reading data from a SRAM. Read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high a read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Current consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and $I/O_0 \sim I/O_7$ are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA LOADING

A byte load is performed by appling a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_6) order and can be renewed in a data loading period.

PAGE WRITE

The KM29C010 is renewed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the write of its page will be erased to read data FFh. Once the bytes of a page are loaded into the device, they are simultaneously written during the internal write period. After the first byte data have been loaded into the device, successive bytes are entered in the same manner.

The nonvolatile write starts if $\overline{WE}$ stay high for the least t_{BLC} maximum (150μs) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address ($A_7 \sim A_{16}$) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase period and a program cycle. During the erase period, the existing data of the locations being addressed during the loading period are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page.

The KM29C010 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM29C010 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM29C010 has a protection feature against $\overline{WE}$ noises; a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when Vcc is less than V_{WI}=3.0V(min), the write inhibit Vcc level. During power-up, the KM29C010 automatically prevents any write operation for a period of 10ms(max.) after Vcc reaches the V_{WI} level. This will protect the chip from a false write during power up transiention. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit from inadvertent writings.

** SOFTWARE DATA PROTECTION **

The KM29C010 has the JEDEC standard software data protection scheme for enhanced protection of stored data.

The shceme does not affect normal write operation if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by executing short SDP enable software alogrithm, followed by a page write operation. Once the protection mode is enabled, the KM29C010 will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by excuting a SDP disable software algorithm. Power transitions will not reset the SDP-feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

$\overline{DATA}$ POLLING

The KM29C010 features $\overline{DATA}$-polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read of the last byte loaded the EEPROM will produce, at I/O_7, an inverted data of the last I/O_7 data loaded into the EEPROM. True data will be produced at all I/O's once the write cycle has been completed.

TOGGLE BIT

The KM29C010 also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 from "1" to "0" and "0" to "1". Once the write cycle is complete, the toggling will stop and valid data will be read.

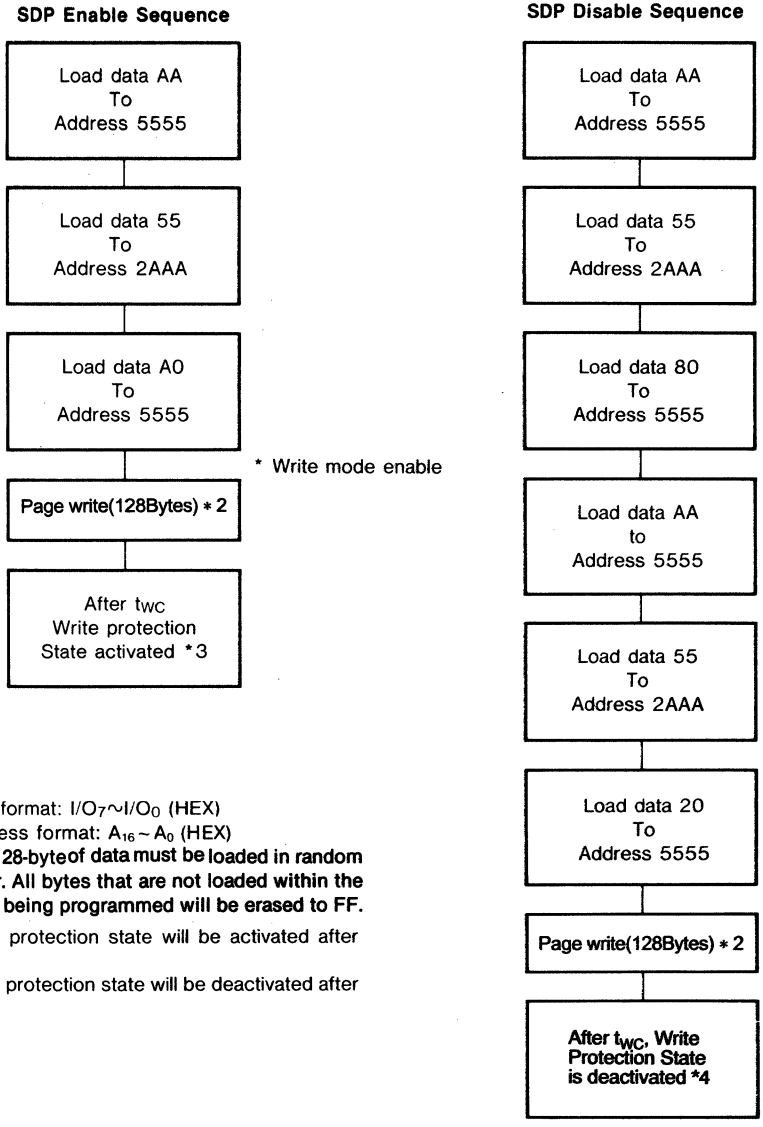
ENDURANCE AND DATA RETENTION

The KM29C010 is designed for applications requiring up to 100,000 write cycles per page and ten years of data retention. This means that each bit can be reliably written 100,000 times without degrading device opera-

DEVICE OPERATION (Continued)

tion, and this device features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in 32 bits. And hence, significant improvements in the endurance and data retention characteristics are achieved.

SOFTWARE DATA PROTECTION ALGORITHM *1



Note 1. Data format: $I/O_7 \sim I/O_0$ (HEX)
Address format: $A_{16} \sim A_0$ (HEX)

2. **1 to 128-byte of data must be loaded in random order. All bytes that are not loaded within the page being programmed will be erased to FF.**
3. Write protection state will be activated after t_{WC}.
4. Write protection state will be deactivated after t_{WC}.

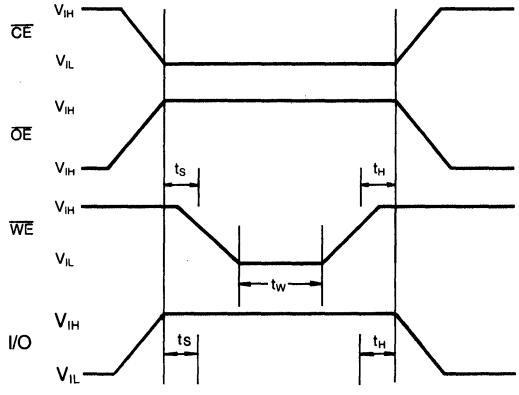
SOFTWARE CHIP ERASE

The KM29C010 may be erased at one time by using a six byte software command code. The erase code consists of six byte load commands to specific address location and specific data patterns. Once the code has been entered the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally auto-timed the erase operation so that external clocks are not required.

HIGH VOLTAGE CHIP ERASE

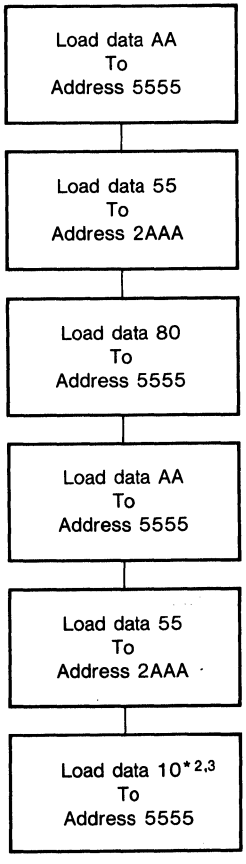
The contents of the KM29C010 may be set to the high state (FFh) by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high: When $\overline{WE}$ pulsed low for a minimum of 10ms, the contents of the KM29C010 is erased.

HIGH VOLTAGE CHIP ERASE WAVEFORMS



$t_S=t_H=5\mu sec$ (min)
$t_W=10msec$ (min)
$V_H=12.0V$

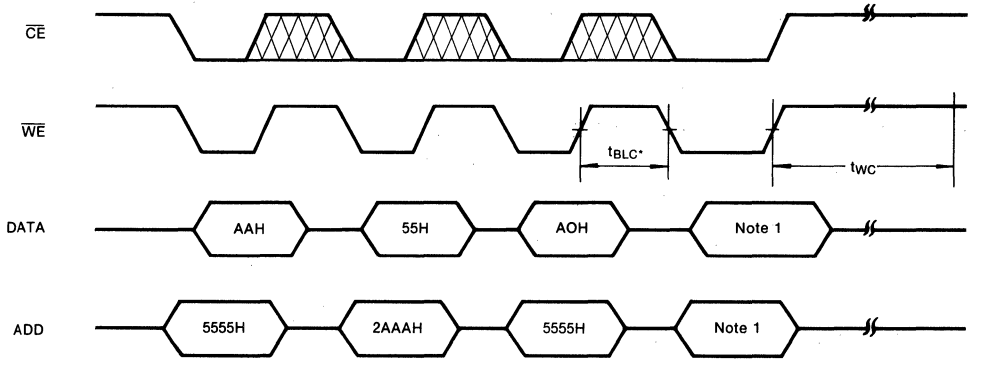
SOFTWARE CHIP ERASE ALGORITHM*1



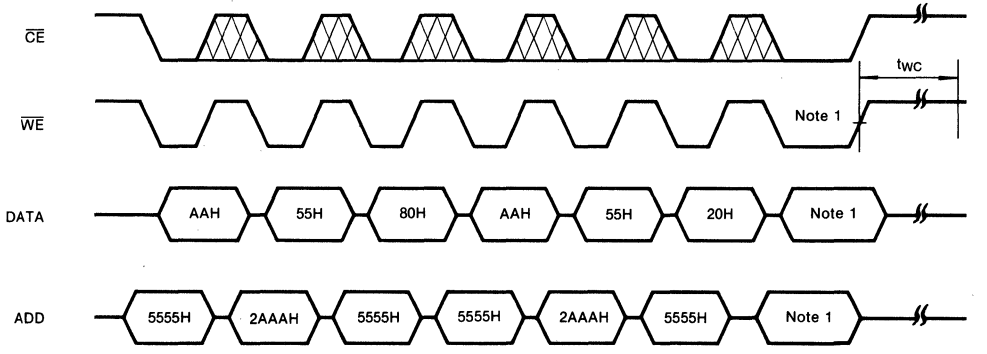
Notes for software ship erase code;
1. Data format: $I/O_7 \sim I/O_0$ (Hex.)
   Address format: $A_{14} \sim A_0$ (Hex.)
2. Data polling may be used to determine the end of the erase cycle by checking any address for data equal to FFh.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

TIMING DIAGRAM OF SOFTWARE DATA PROTECTION

SDP ENABLE TIMING SEQUENCE



SDP DISABLE TIMING SEQUENCE



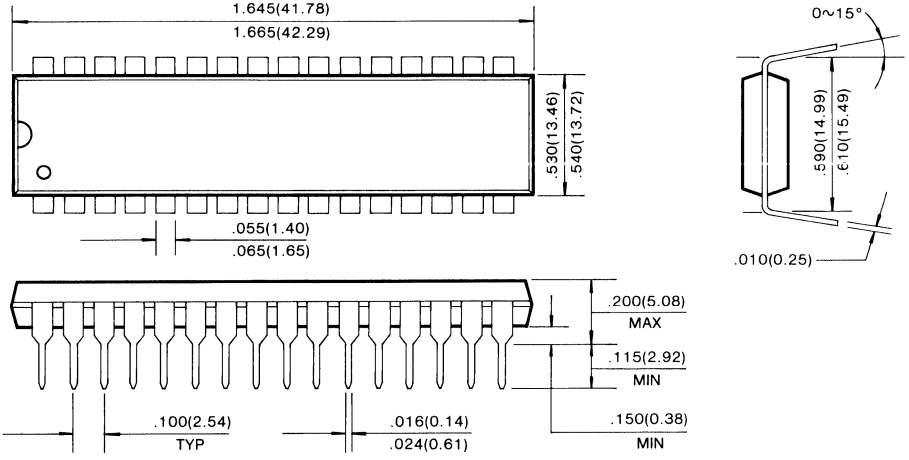
* $\leqslant t_{BLC}$ max.

Note 1: 1 to 128 byte to data maybe loaded in random order.

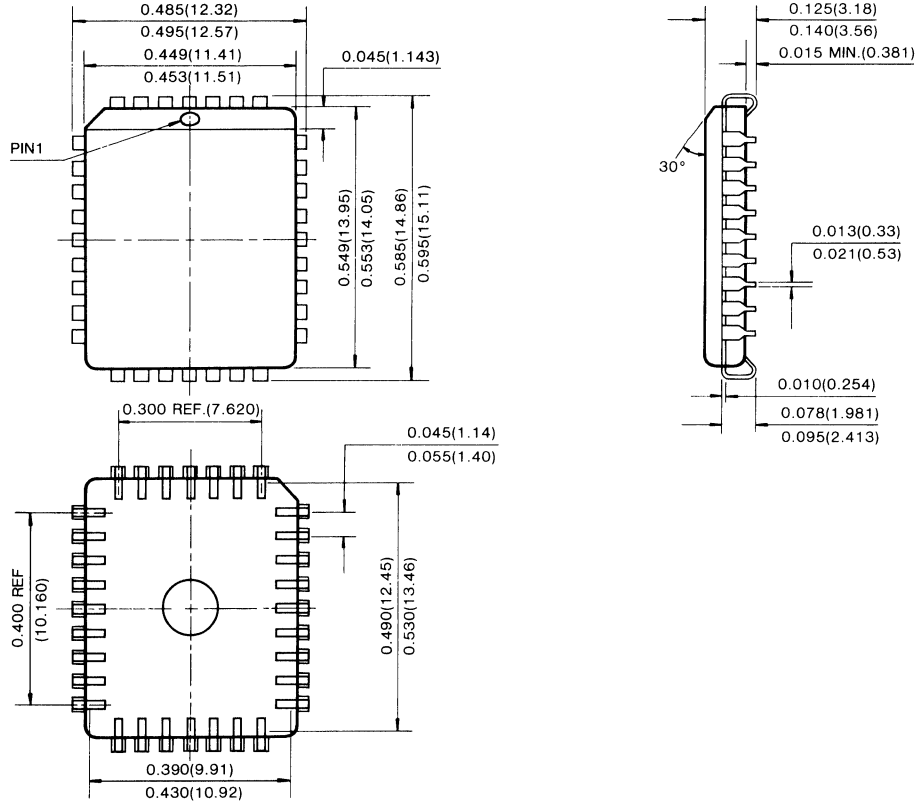
PACKAGE DIEMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



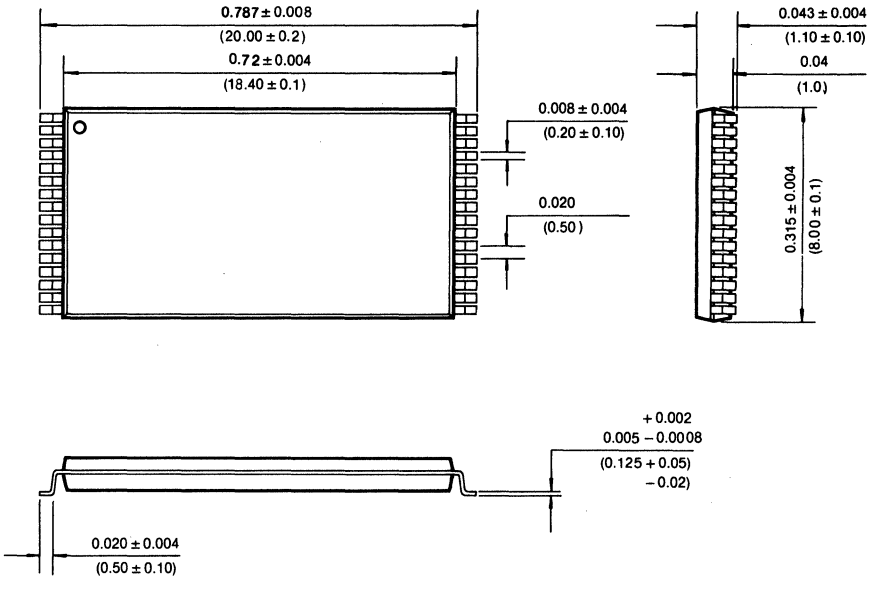
32 PIN PLASTIC LEADED CHIP CARRIER



SAMSUNG ELECTRONICS

32 PIN THIN SMALL OUTINE PACKAGE (Forward Type)

Unit: Inches (millimeters)



MASK ROM DATA SHEETS 3

SAMSUNG ROM DATA INFORMATION

1. HARD MEDIA

There are many kinds of hard media to deliver ROM Code as follows, and SEC defined the priority numbers for easy access to SEC's ROM Code generation tool.

* Priority #1: EPROM
  #2: Floppy Diskette (3.5 or 5.25 inch)
  #3: Reel Tape (6250 bpi. 9 track etc.)
  #4: Cartridge (150MB Quad Cartridge etc.)

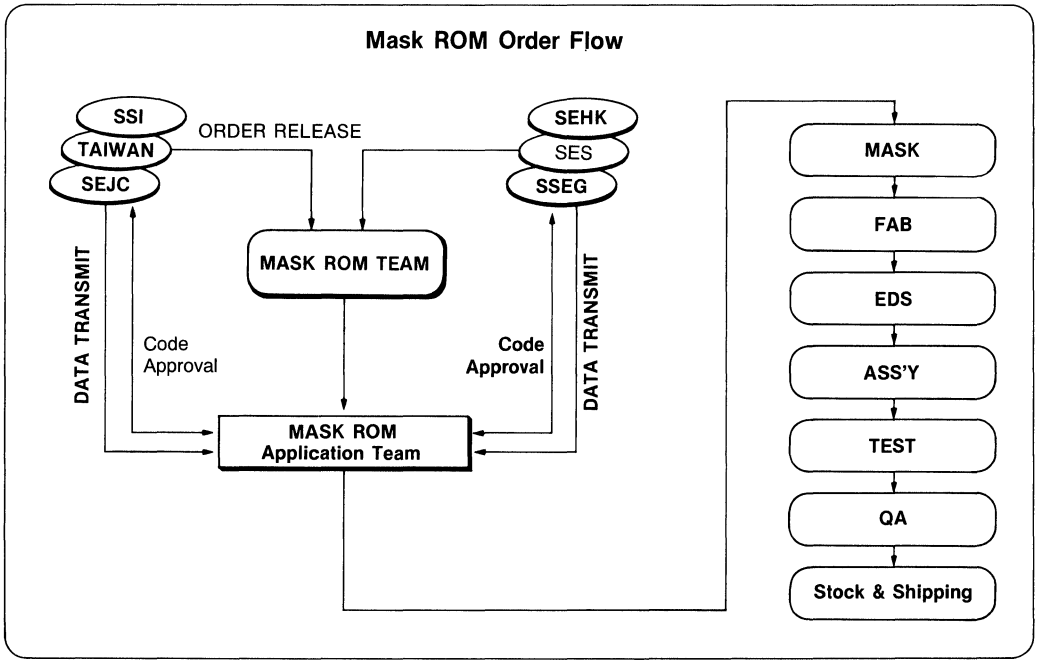
2. DATA FORMAT

In the event of providing ROM Code by cartridge, reel tape, or floppy diskette, SEC likes data format to be provide according to following priority.

* Priority #1: Extended Tek. Hexa format
  #2: Absolutely binary format
  #3: Intel-86 format
  #4: Intel-8 format

3. ROM CODE TRANSPORTATION VIA SATELLITE

SEC offers ROM Code transmission through satellite and it is very much competitive way in terms of TAT compare to ROM Code exchange by mail just like DHL or SPEED POST.



256K-Bit (32K x 8) CMOS MASK ROM

FEATURES

- **KM23C256: 28-pin DIP (Polarity programmable chip enable pin and output enable pin)**
- **KM23C256G: 32-pin SOP (Polarity programmable chip enable pin and output enable pin)**
- **32,768 x 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

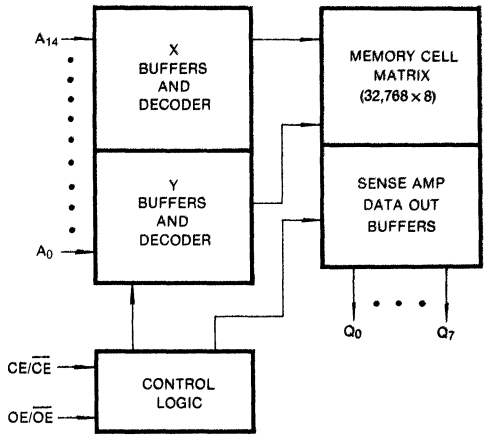
The KM23C256 is a fully static mask programmable ROM organized 32,768 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

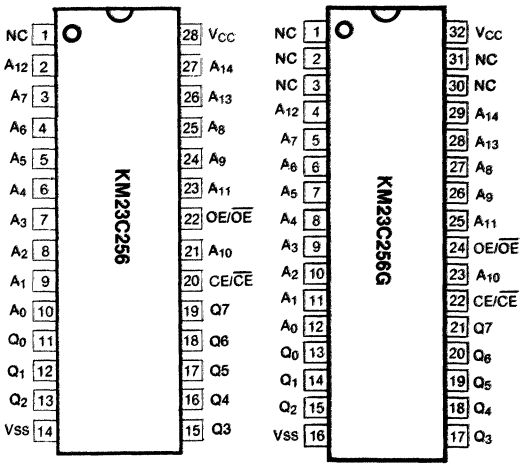
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C256 is packaged in a 28-DIP and the KM23C256G in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N C	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=5.0MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

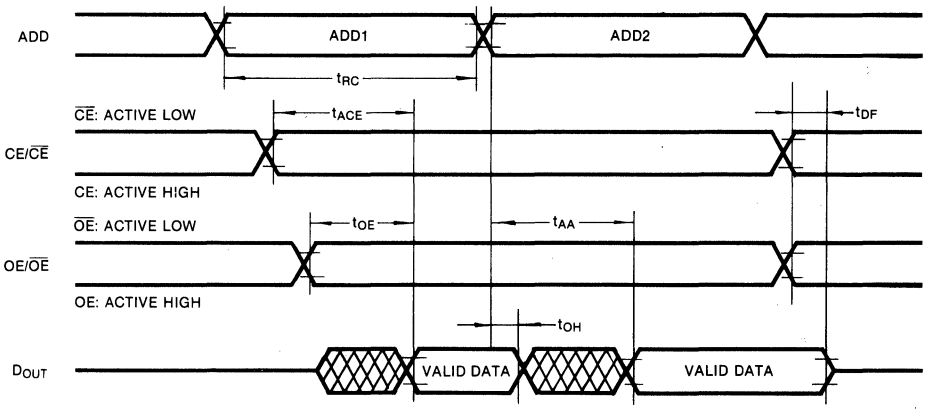
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C256(G)-12		KM23C256(G)-15		KM23C256(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

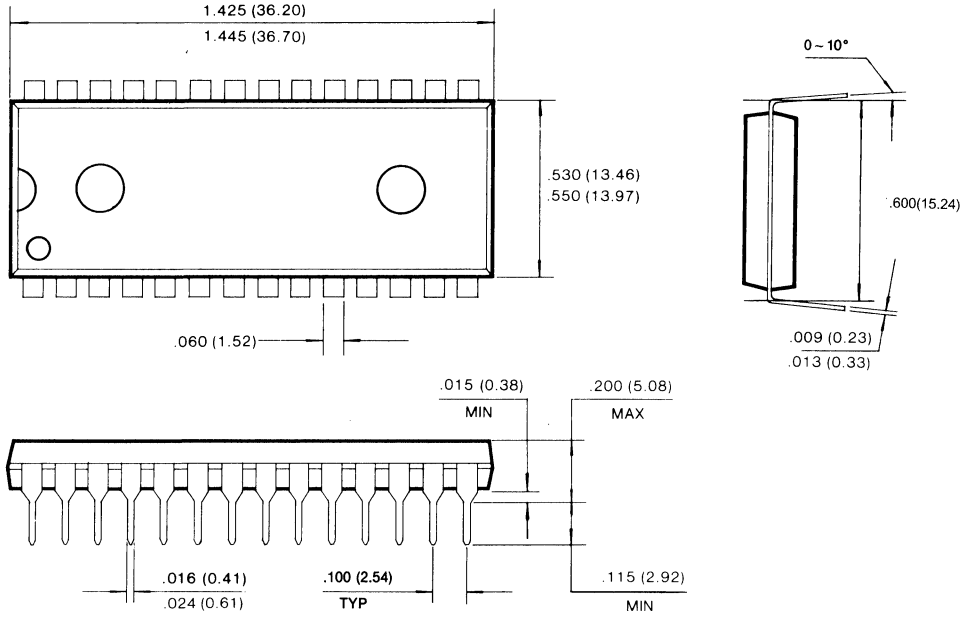
READ



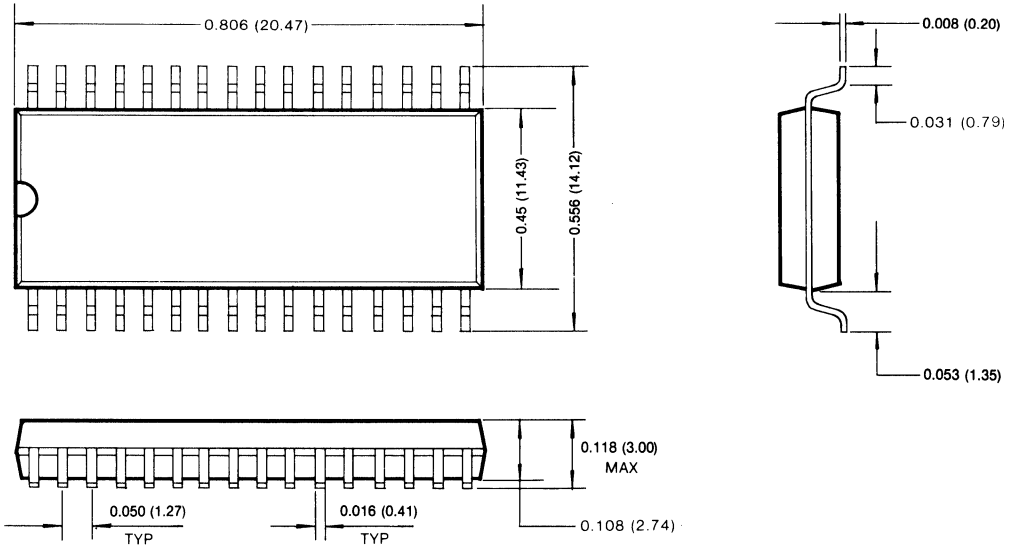
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C256)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C256G)



512K-Bit (64K x 8) CMOS MASK ROM

FEATURES

- **KM23C512: 28-pin DIP (Polarity programmable chip enable pin and output enable pin)**
- **KM23C512G: 32-pin SOP (Polarity programmable chip enable pin and output enable pin)**
- **65,536 x 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 30mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **600 mil, plastic DIP (JEDEC standard)**
  525 mil, plastic SOP

GENERAL DESCRIPTION

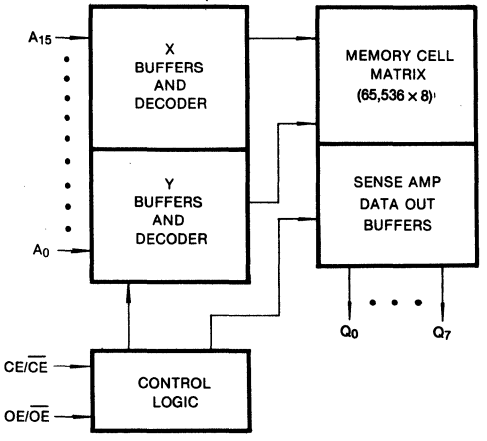
The KM23C512 is a fully static mask programmable ROM organized 65,536 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

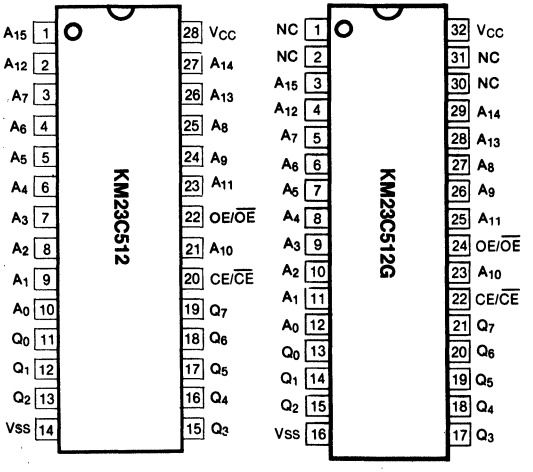
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C512 is packaged in a 28-DIP, provides polarity programmable CE and OE buffer as user option mode, the KM23C512G in a 32-SOP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f = 5.0MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

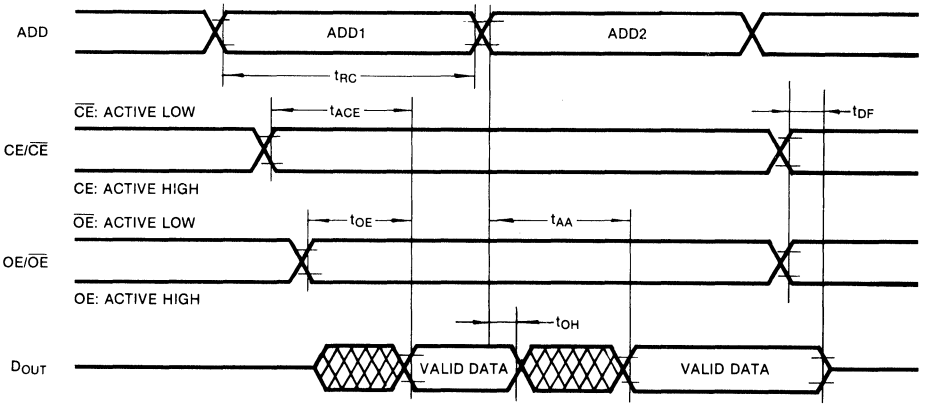
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C512(G)-12		KM23C512(G)-15		KM23C512(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

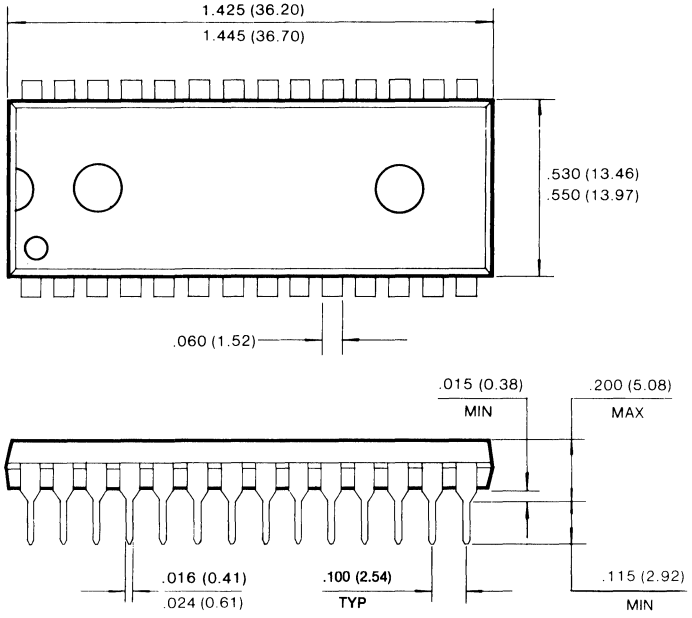
READ

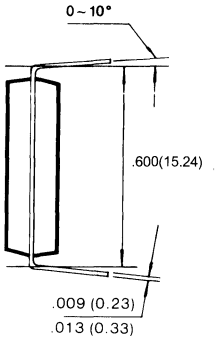


PACKAGE DIMENSIONS

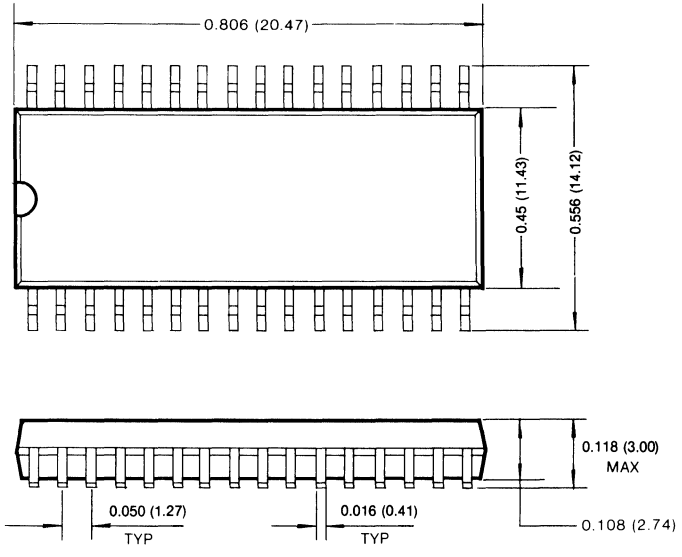
28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C512)

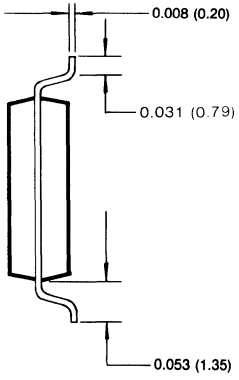
Units: Inches (millimeters)





32 LEAD SMALL OUTLINE PACKAGE (KM23C512G)





SAMSUNG ELECTRONICS

1M-Bit (128K×8) CMOS MASK ROM

FEATURES

- **131,072×8 bit organization**
- **Fast access time : 120ns(max).**
- **Supply voltage : single+5V**
- **Current consumption**
  Operating : 30 mA(max.)
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 28-pin, 600mil, plastic DIP**
  32-pin, 600mil, plastic DIP (JEDEC standard)
  32-pin, 525mil, plastic SOP
  32-pin, PLCC

GENERAL DESCRIPTION

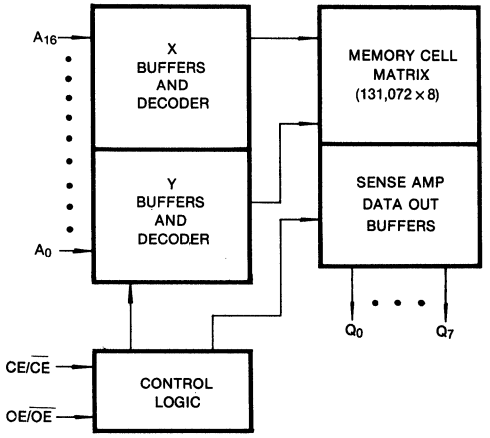
The KM23C1000/1010 is a fully static mask programmable ROM organized 131,072×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C1000 is packaged in a 28-DIP, the KM23C1010 in a 32-DIP, the KM23C1010G in a 32-SOP, and the KM23C1010J in a 32-PLCC, provides polarity programmable CE and OE buffer as user option mode.

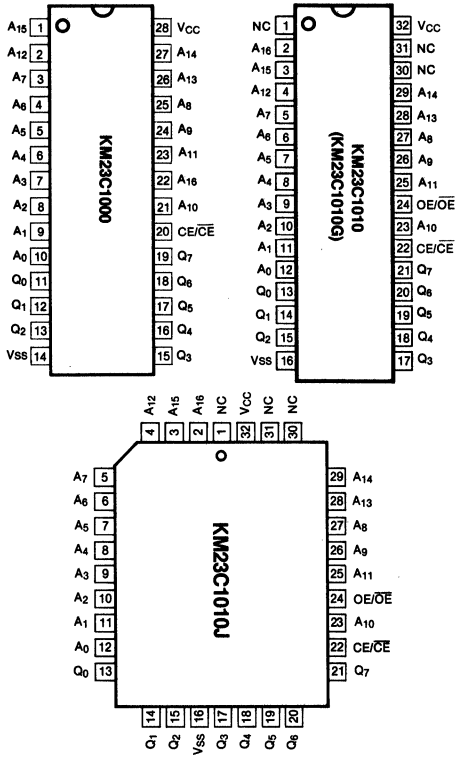
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=5.0MHz all output open	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION (KM23C1000)

$CE/\overline{CE}$	Mode	Data	Power
L/H	Standby	High-Z	Standby
H/L	Operating	D_{OUT}	Active

MODE SELECTION (KM23C1010)

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

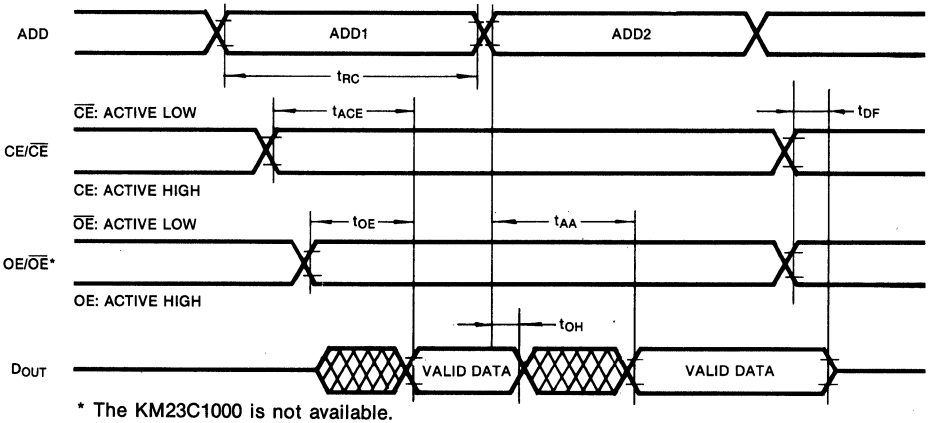
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C 1000-12 KM23C1010(G/J)12		KM23C 1000-15 KM23C1010(G/J)-15		KM23C 1000-20 KM23C 1010(G/J)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

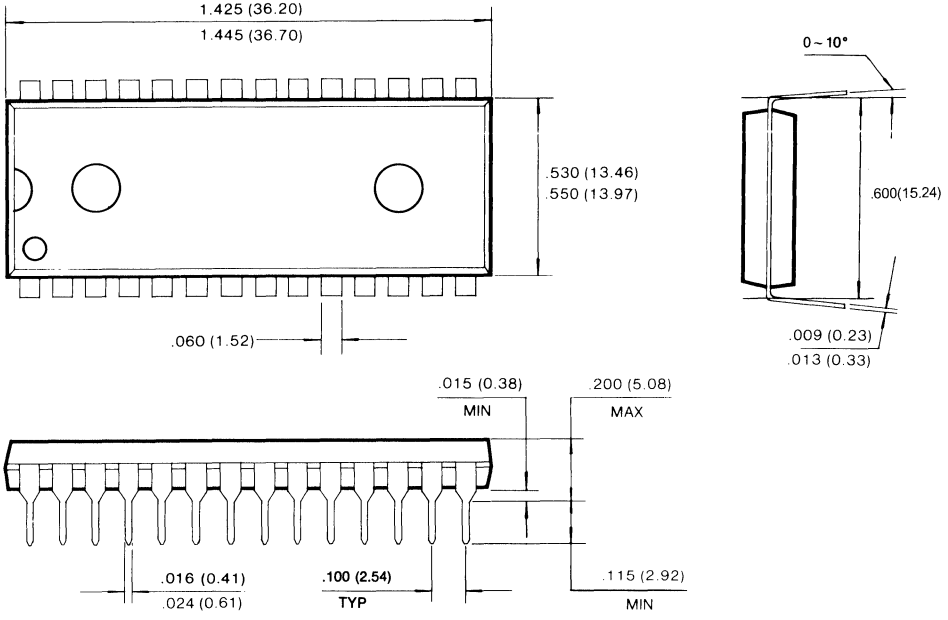


* The KM23C1000 is not available.

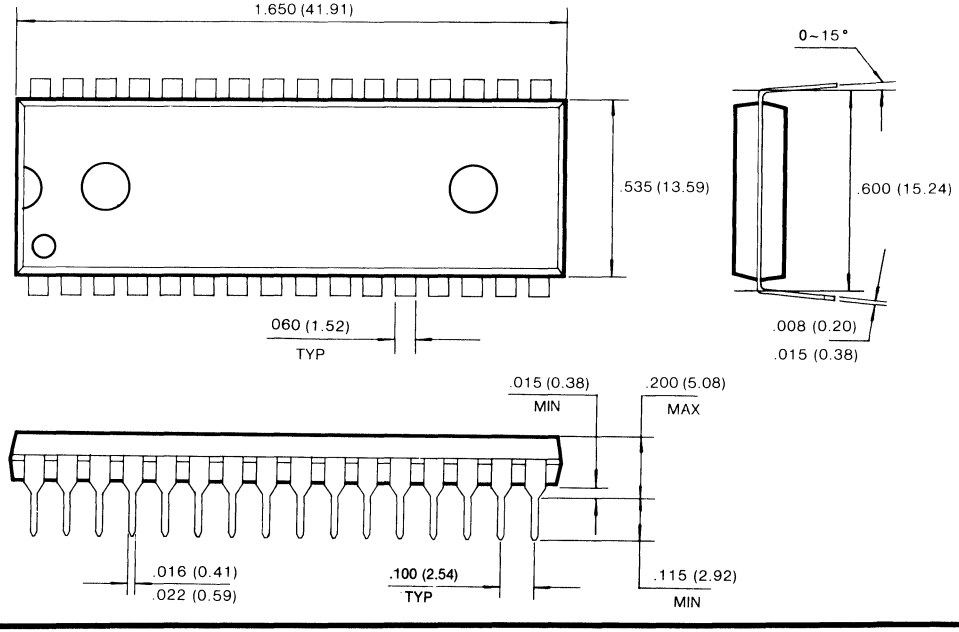
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1000)

Units: Inches (millimeters)



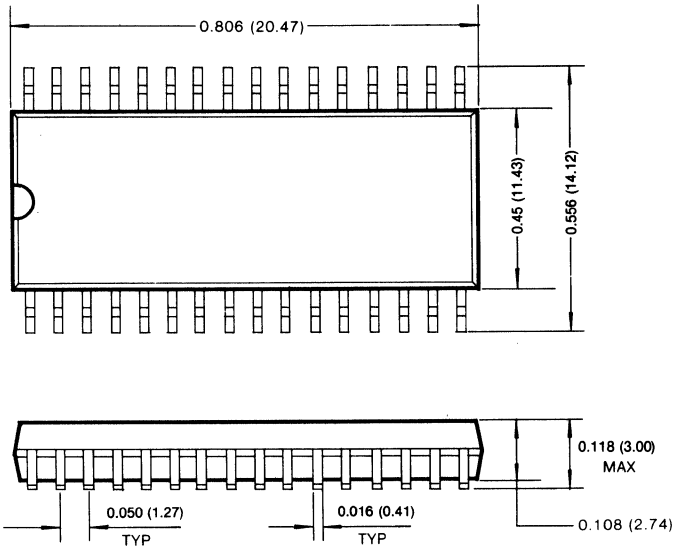
32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1010)



PACKAGE DIMENSIONS (Continued)

32 LEAD SMALL OUTLINE PACKAGE (KM23C1010G)

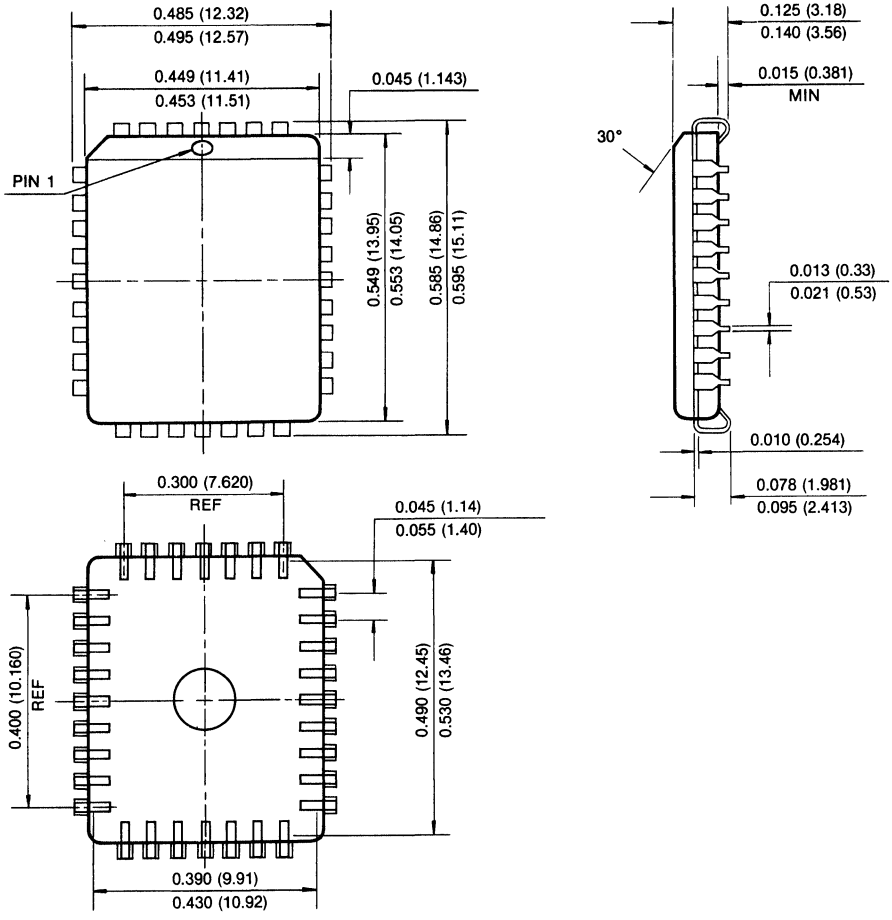
Units: Inches (millimeters)



PACKAGE DIMENSIONS

32 PIN PLASTIC LEADED CHIP CARRIER (KM23C1010J)

Units: Inches (millimeters)



3

1M-Bit (128K x 8) CMOS MASK ROM

FEATURES

- **131,072×8 bit organization**
- **Fast access time : 120ns(max).**
- **Supply voltage : single+5V**
- **Current consumption**
  Operating : 30 mA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package : 28-pin, 600mil, plastic DIP**
  32-pin, 600mil, plastic DIP
  (JEDEC standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

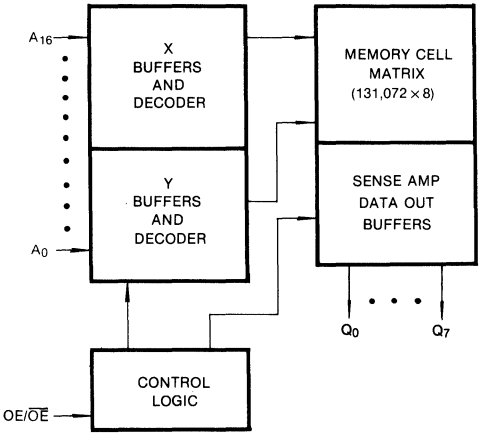
The KM23C1001/1011 is a fully static mask programmable ROM organized 131,072 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

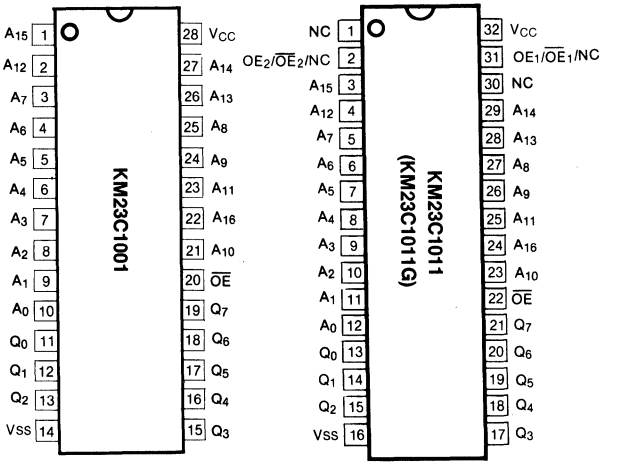
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C1001 is packaged in a 28-DIP, the KM23C1011 in a 32-DIP, the KM23C1011G in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE}$ = V_{IL}, f = 5.0MHz all output open	—	40	mA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$OE/\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

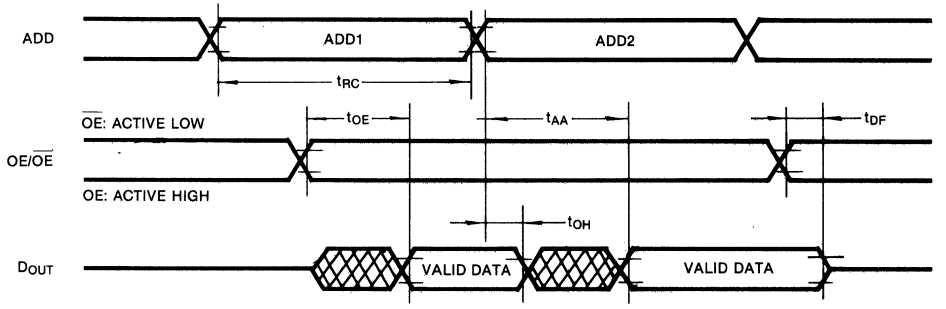
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C1001-12 KM23C1011(G)-12		KM23C1001-15 KM23C1011(G)-15		KM23C1001-20 KM23C1011(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

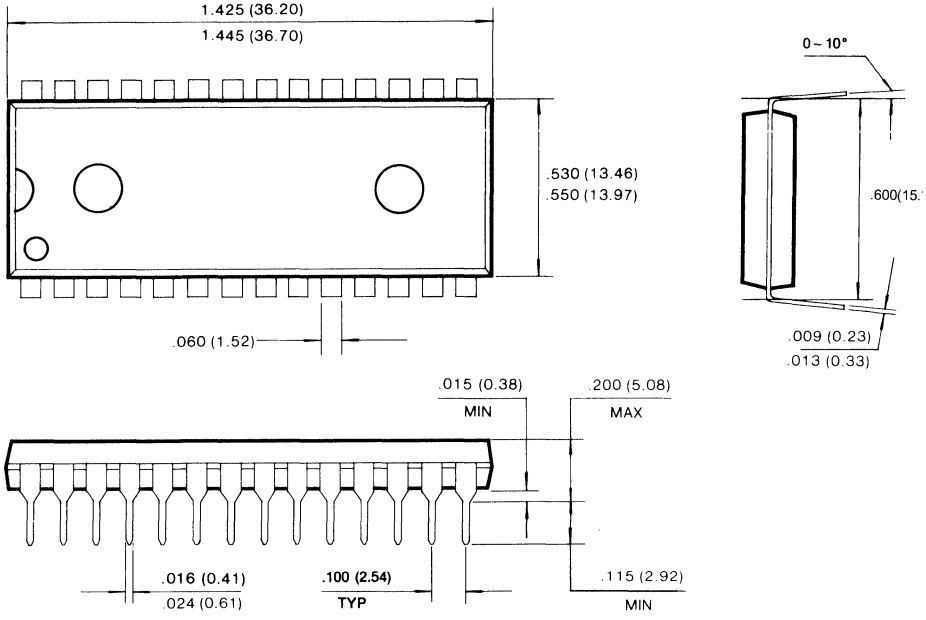
READ



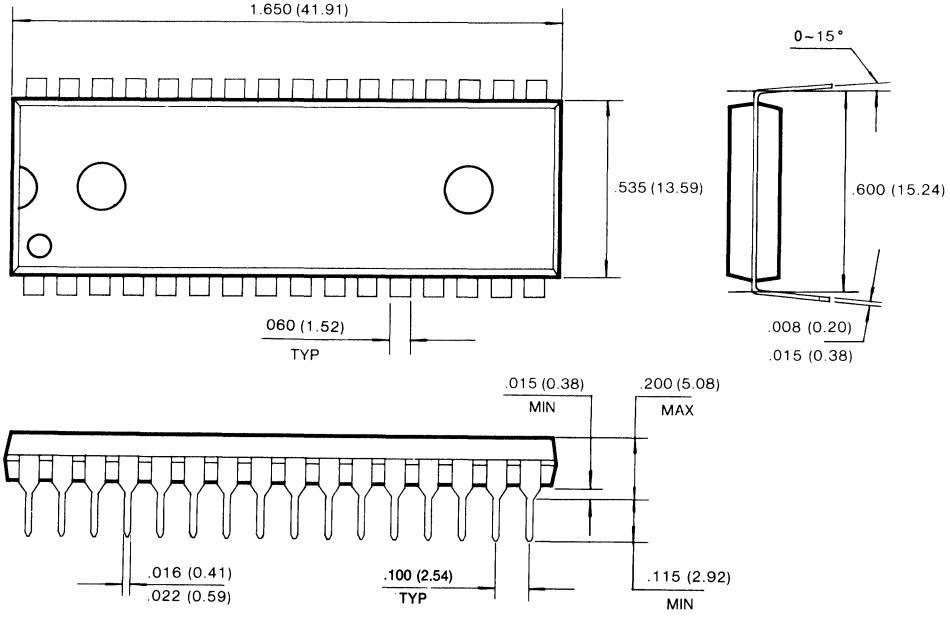
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1001)

Units: Inches (millimeters)



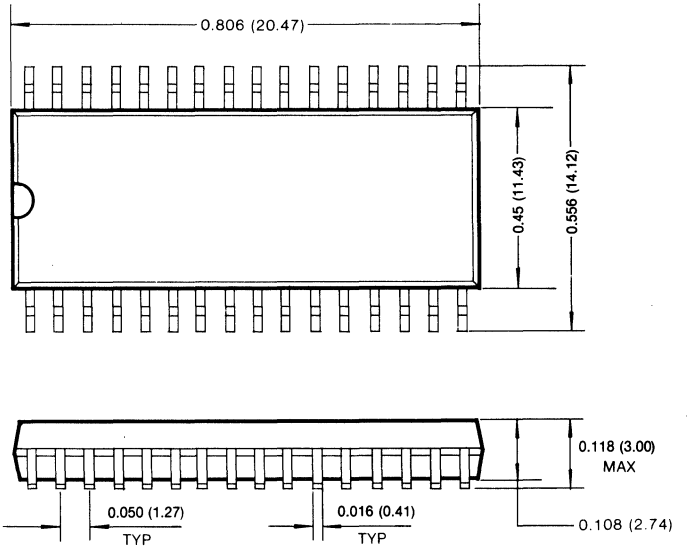
32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C1011)



PACKAGE DIMENSIONS (Continued)

32 LEAD SMALL OUTLINE PACKAGE (KM23C1011G)

Units: Inches (millimeters)



2M-Bit (256K x 8) CMOS MASK ROM

FEATURES

- **262,144 x 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C2000 is a fully static mask programmable ROM organized 262,144 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

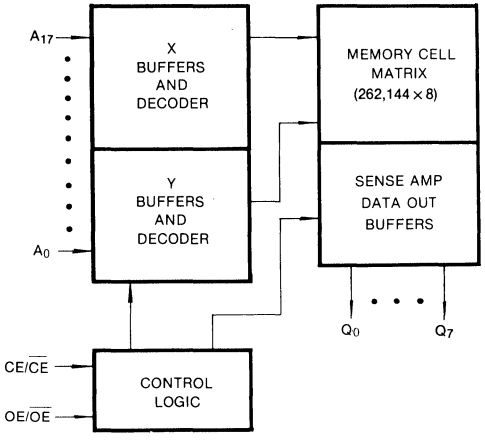
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

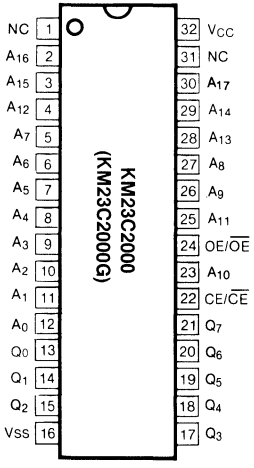
The KM23C2000 is packaged in a 32-DIP, and the KM23C2000G in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

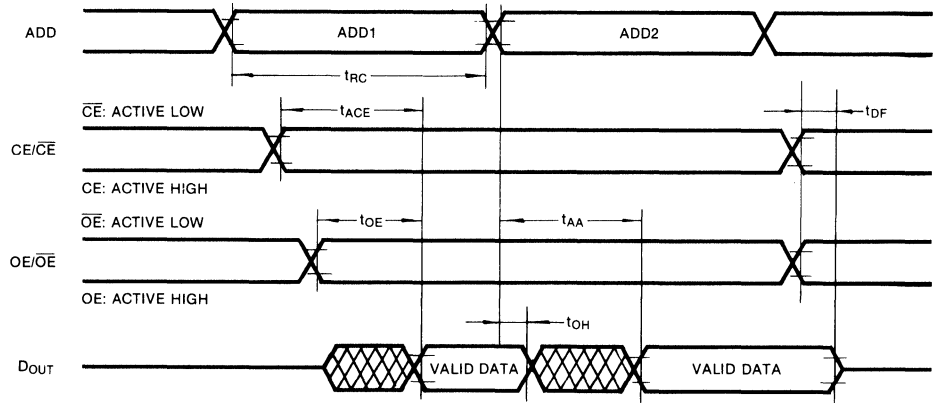
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C2000G-15		KM23C2000G-20		KM23C2000G-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

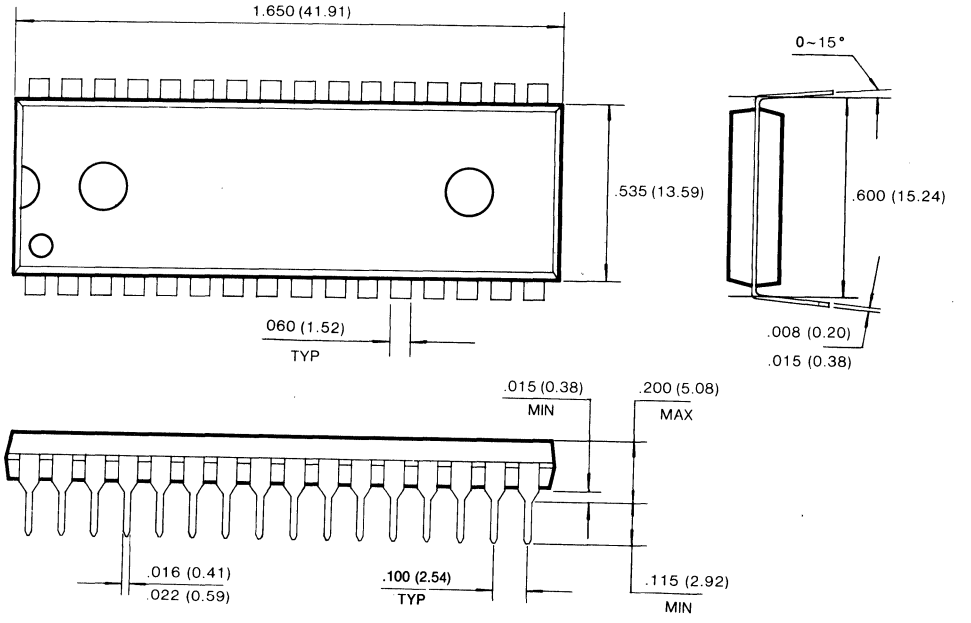
READ



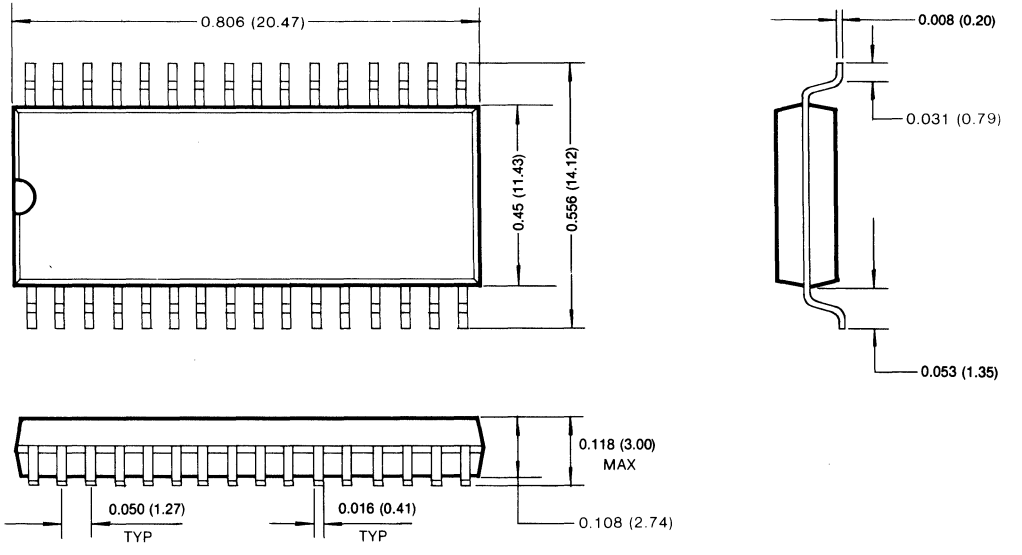
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2000)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2000G)



2M-Bit (256K x 8) CMOS MASK ROM

FEATURES

- **262,144 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 40mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C2000A is a fully static mask programmable ROM organized 262,144 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

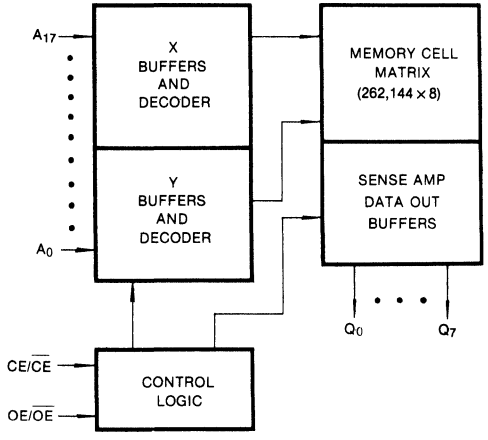
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

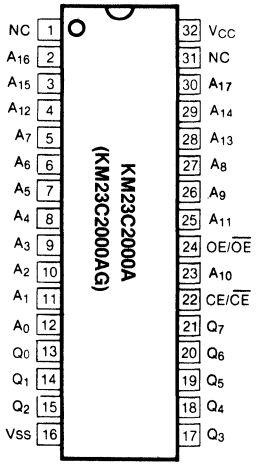
The KM23C2000A is packaged in a 32-DIP, and the KM23C2000AG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

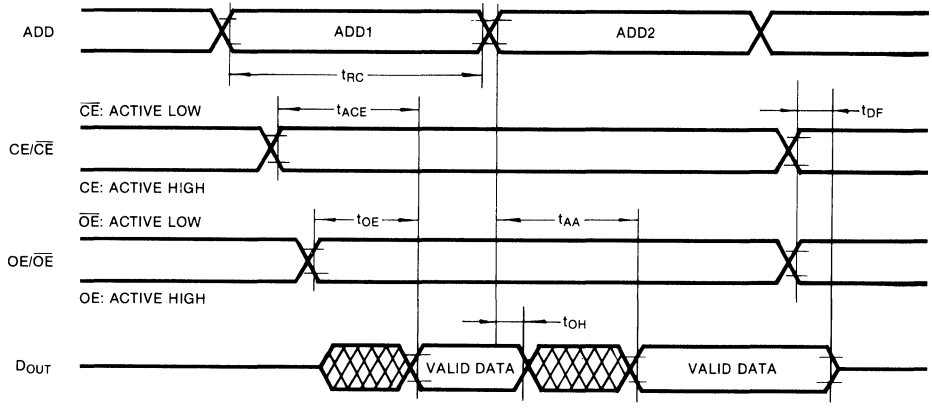
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C2000A(G)-10		KM23C2000A(G)-12		KM23C2000A(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

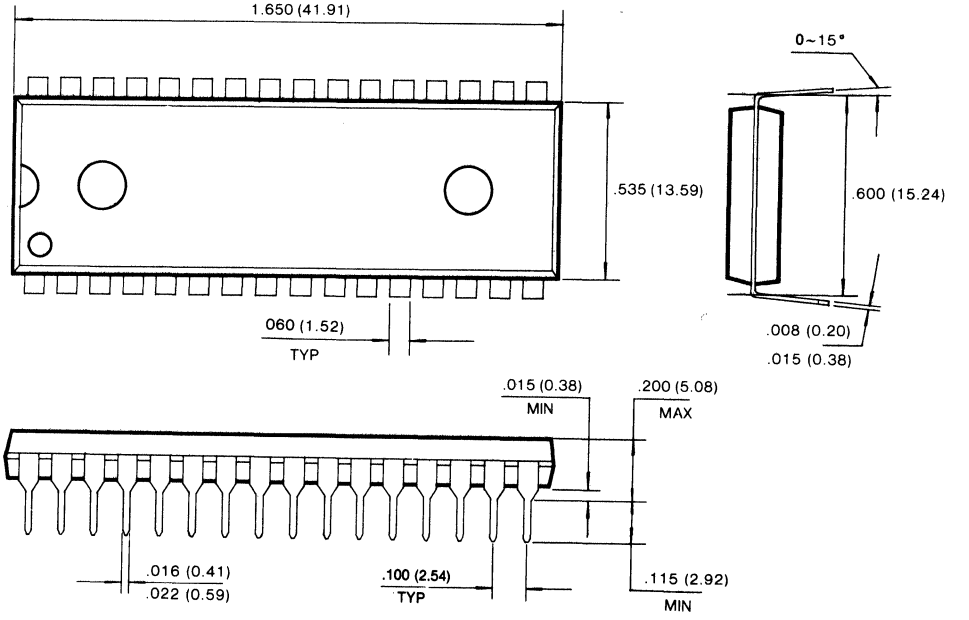
READ



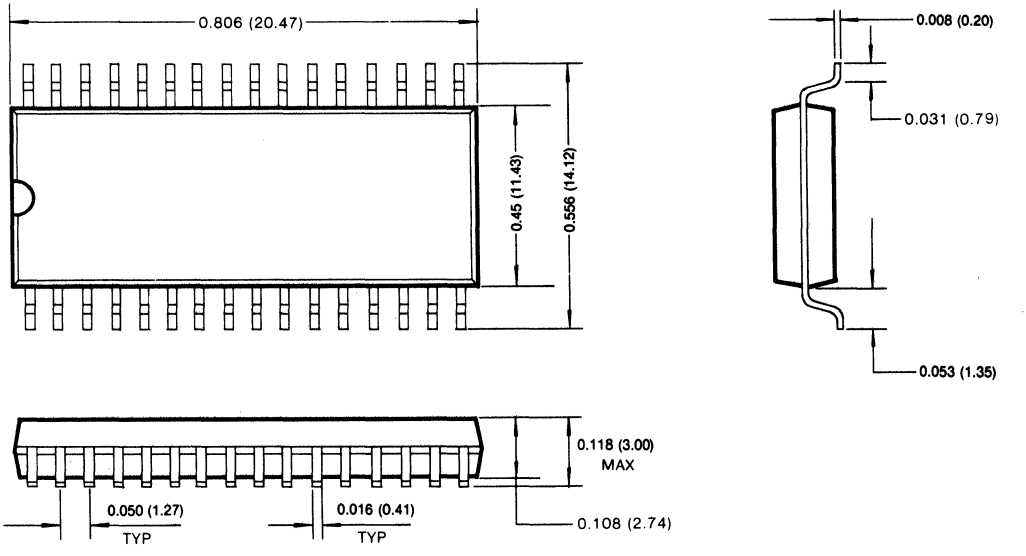
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2000A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2000AG)



2M-Bit (256K x 8) CMOS MASK ROM

FEATURES

- **262,144 x 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Package: 32-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

The KM23C2001 is a fully static mask programmable ROM organized 262,144 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

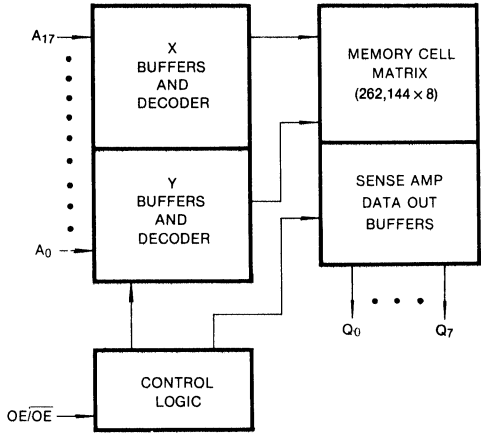
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

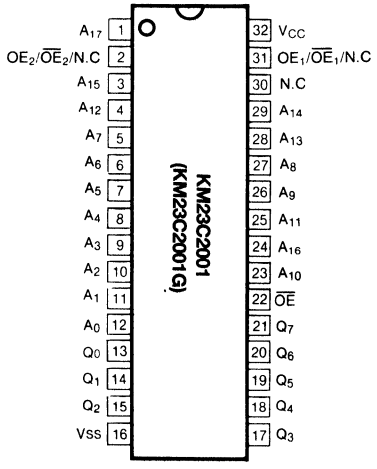
The KM23C 2001 is packaged in a 32-DIP, and the KM23C2001G in a 32SOP, provides polarity programmable OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

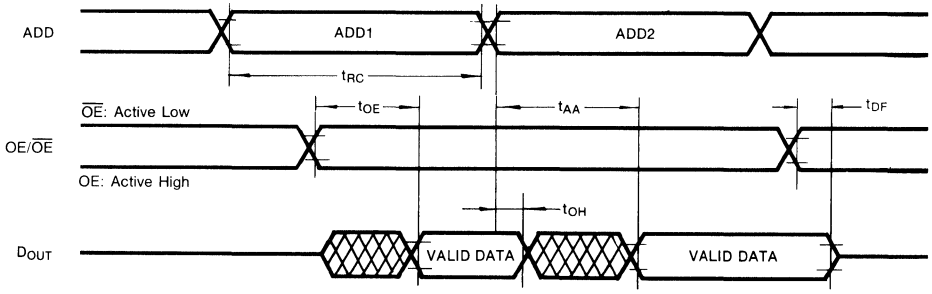
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C2001-15		KM23C2001-20		KM23C2001-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

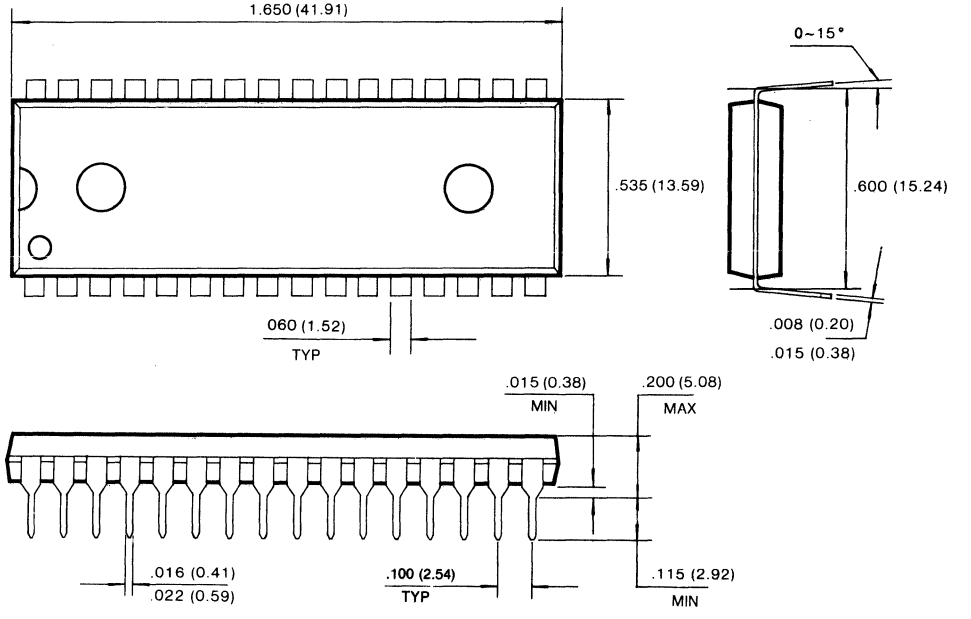
READ



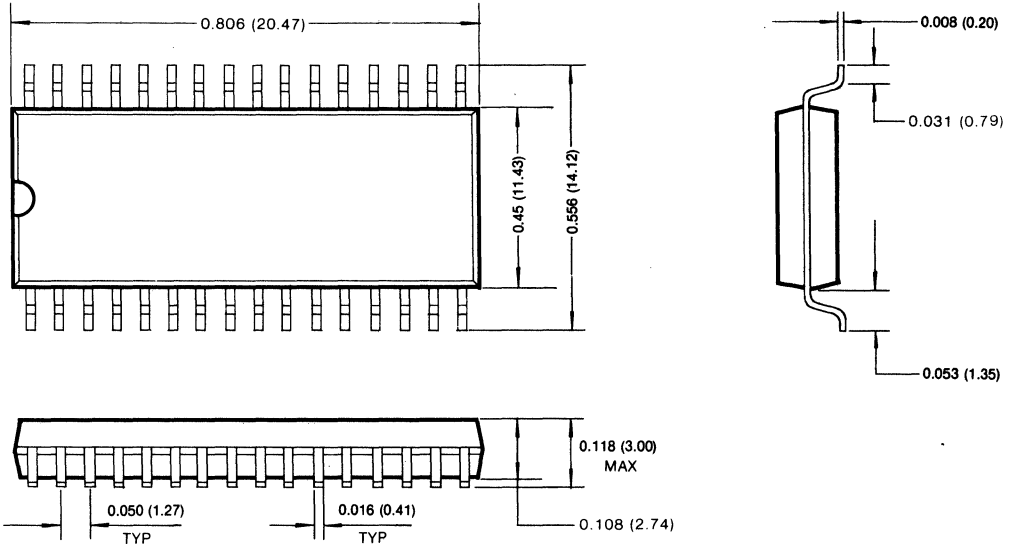
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2001)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2001G)



SAMSUNG ELECTRONICS

2M-Bit (256K x 8) CMOS MASK ROM

FEATURES

- **262,144 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 40mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Package: 32-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

The KM23C2001A is a fully static mask programmable ROM organized 262,144 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

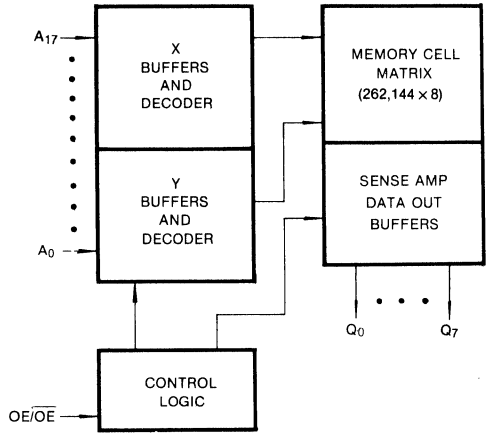
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

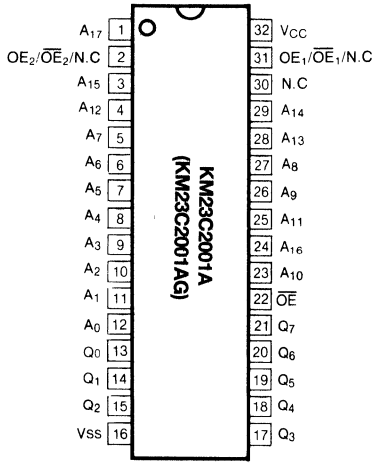
The KM23C2001A is packaged in a 32-DIP, and the KM23C2001AG in a 32SOP, provides polarity programmable OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 5.0MHz all output open	—	40	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

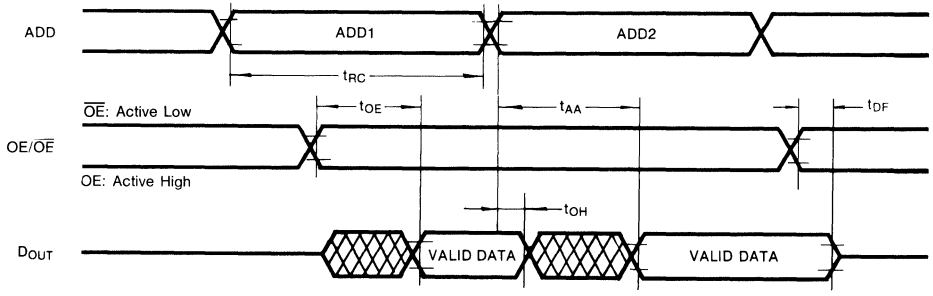
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C 2001A(G)-10		KM23C2001A(G)-12		KM23C2001A(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

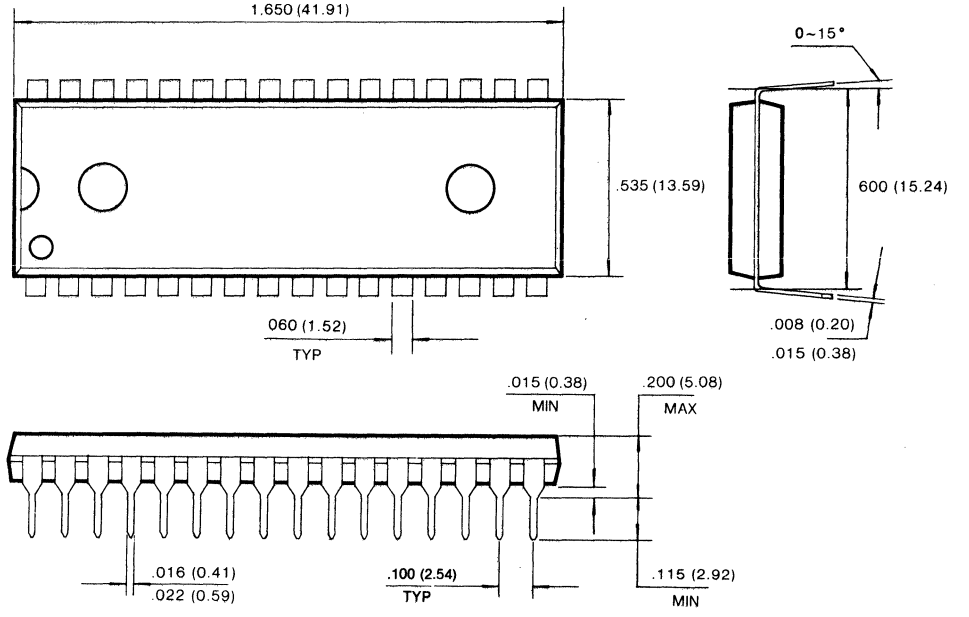
READ



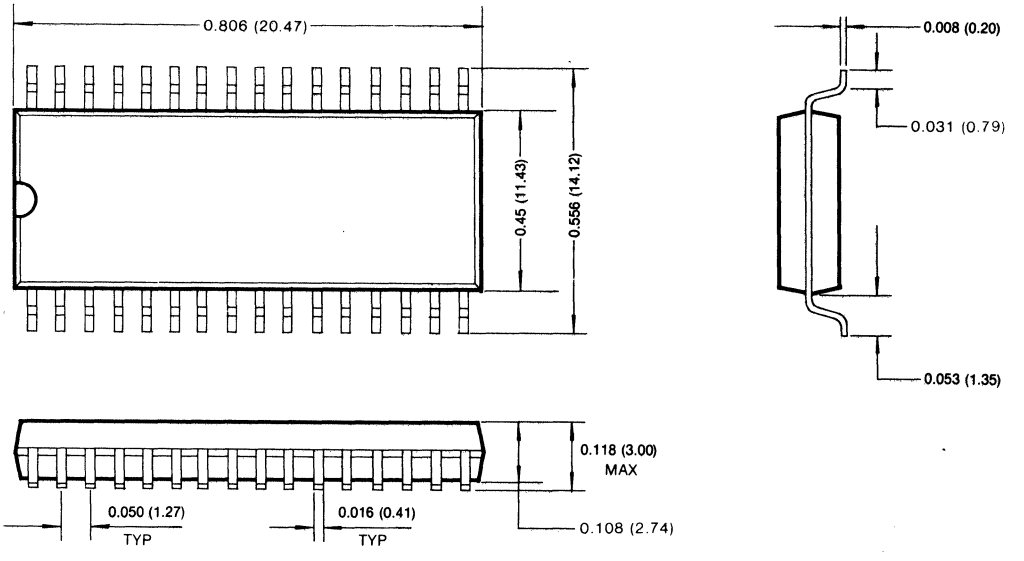
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2001A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C2001AG)



2M-Bit (256K x 8/128K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 262,144 x 8
  Word Mode: 131,072 x 16
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**

GENERAL DESCRIPTION

The KM23C2100 is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 262,144 x 8 bit (byte mode) or as 131,072 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

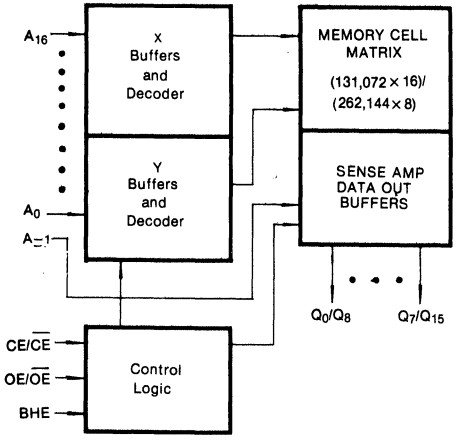
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C2100 is packaged in a 40-DIP, provides polarity programmable CE and OE buffer as user option mode.

3

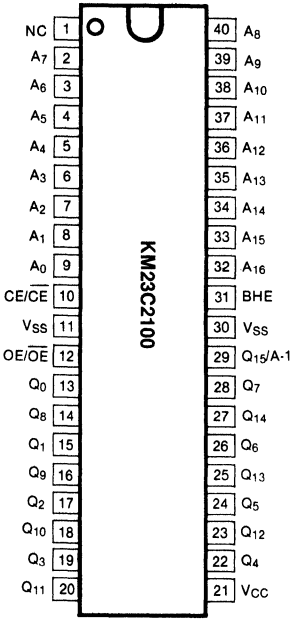
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5.0MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all output open	—	100	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

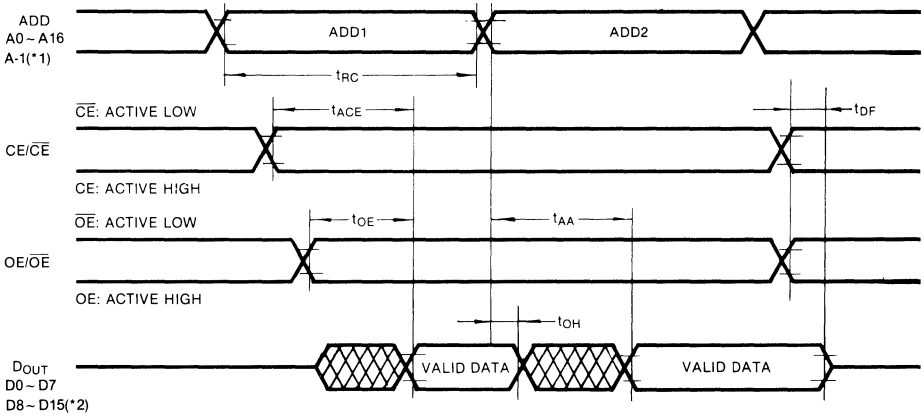
READ CYCLE

Parameter	Symbol	KM23C2100-15		KM23C2100-20		KM23C2100-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

3

TIMING DIAGRAM

READ

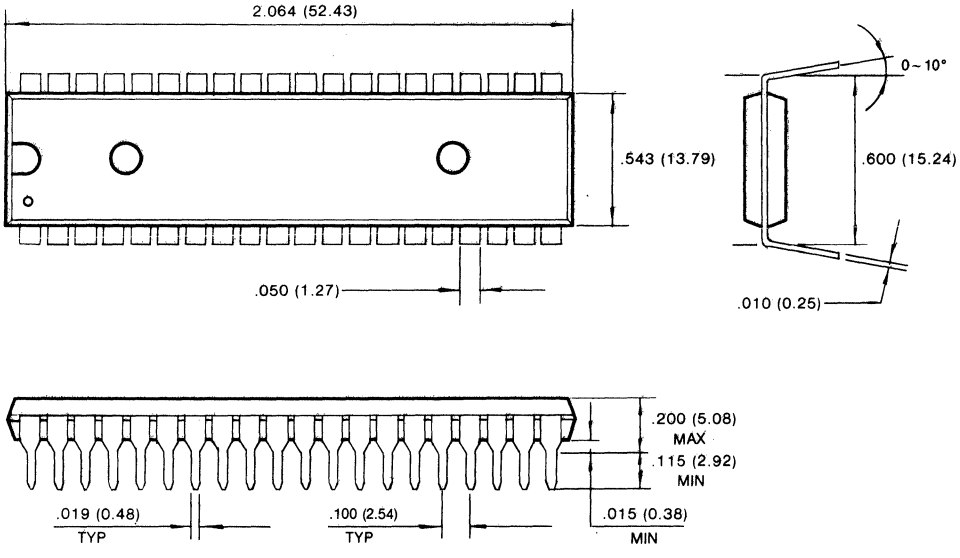


(*1) Byte Mode only. A-1 is Least Significant Bit Address. ($BHE = V_{IL}$)
(*2) Word Mode only. ($BHE = V_{IH}$)

PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2100)

Units: Inches (millimeters)



SAMSUNG ELECTRONICS

2M-Bit (256K x 8/128K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 262,144 x 8
  Word Mode: 131,072 x 16
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 40mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**

GENERAL DESCRIPTION

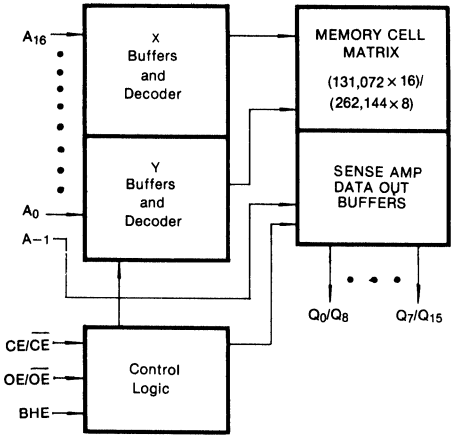
The KM23C2100A is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 262,144 x 8 bit (byte mode) or as 131,072 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C2100A is packaged in a 40-DIP, provides polarity programmable CE and OE buffer as user option mode.

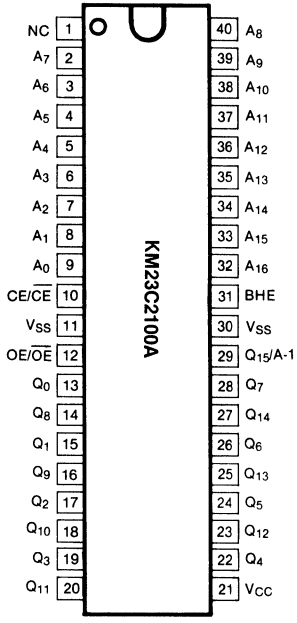
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5.0MHz all output open	—	40	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

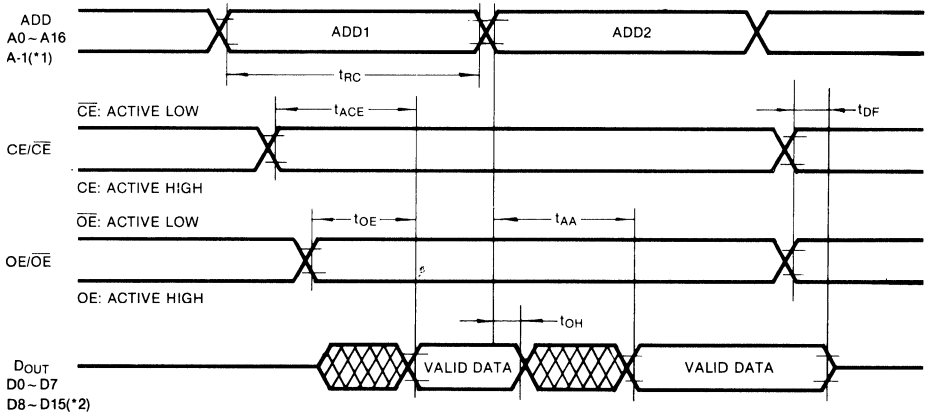
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C2100A-10		KM23C2100A-12		KM23C2100A-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

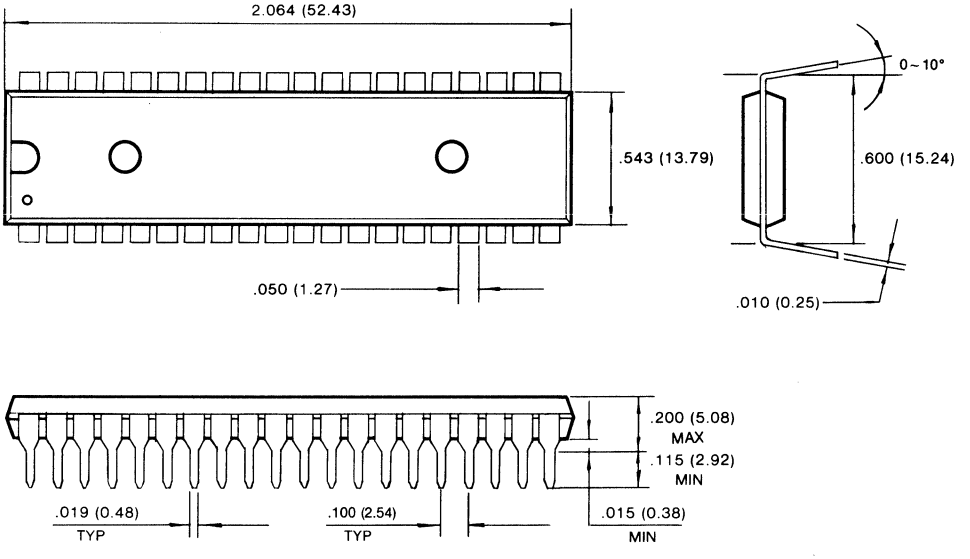


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C2100A)

Units: Inches (millimeters)



4M-Bit (512K x 8) CMOS MASK ROM

FEATURES

- **524,288 x 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 60 mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C4000B is a fully static mask programmable ROM organized 524,288 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

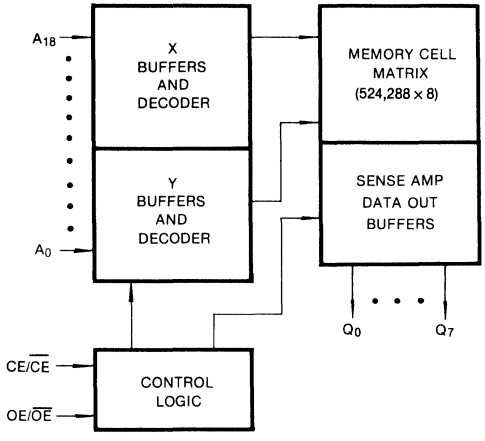
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

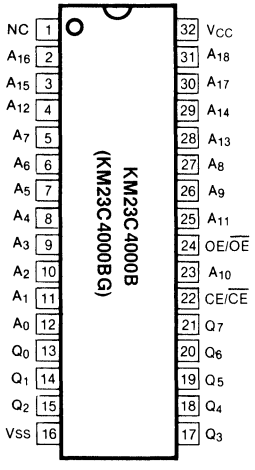
The KM23C4000B is packaged in a 32-DIP, and the KM23C4000BG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

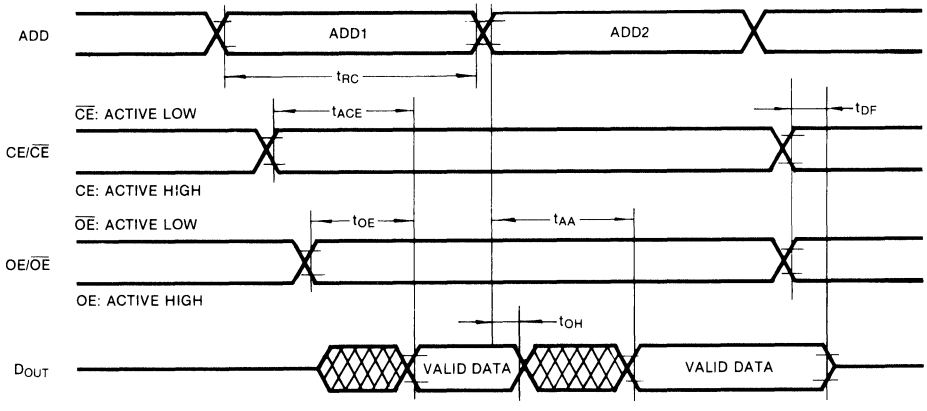
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4000B(G)-12		KM23C4000B(G)-15		KM23C4000B(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

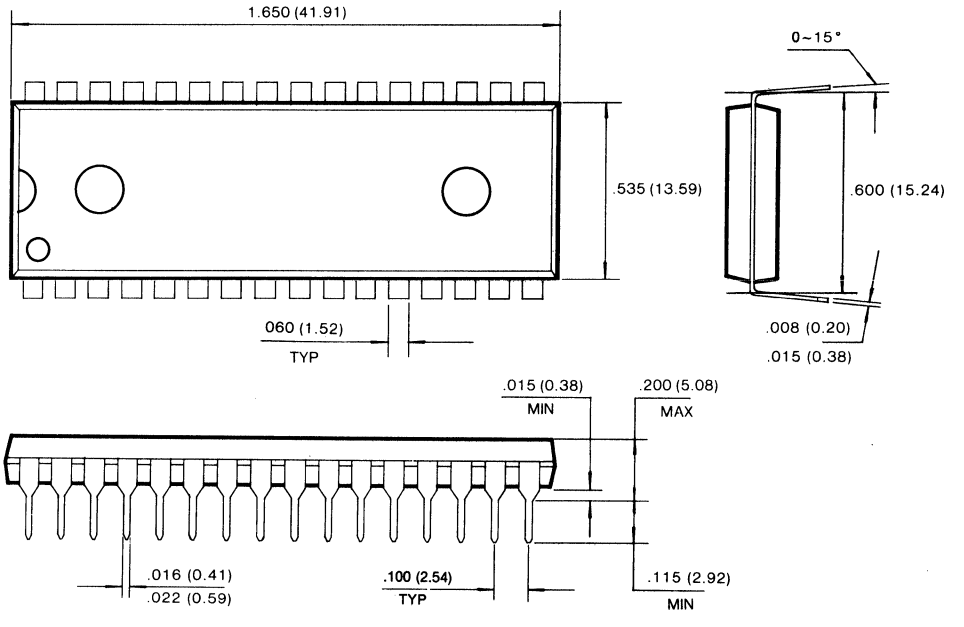


SAMSUNG ELECTRONICS

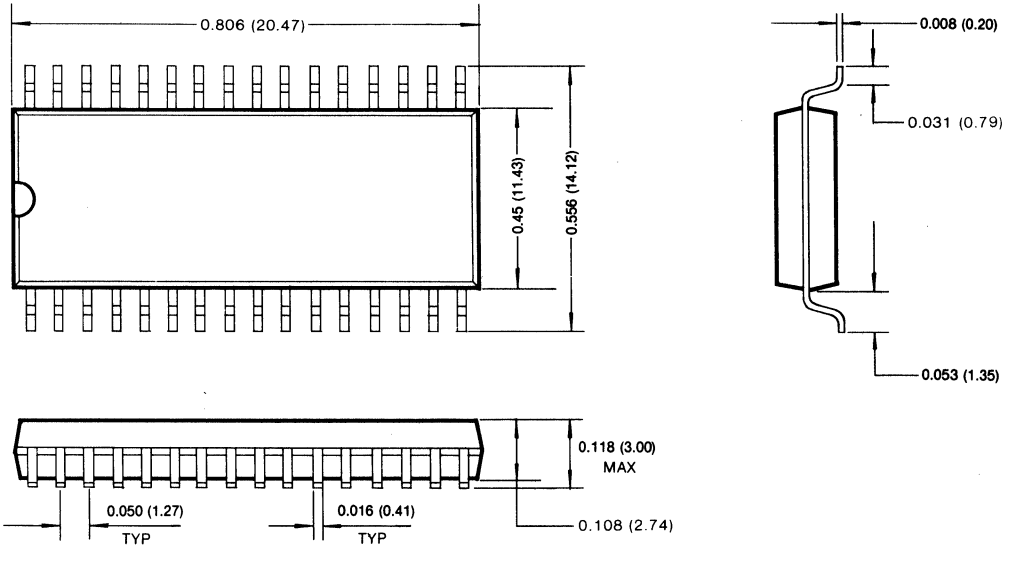
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4000B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4000BG)



4M-Bit (512K x 8) CMOS MASK ROM

FEATURES

- **524,288 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin 600 mil, plastic DIP**
  (JEDEC Standard)
  32-pin 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C4000H is a fully static mask programmable ROM organized 524,288 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

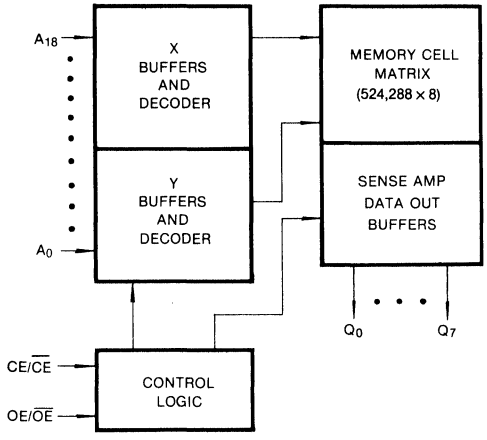
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

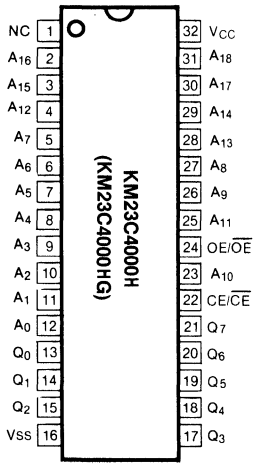
The KM23C4000H is packaged in a 32-DIP, and the KM23C4000HG packaged in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

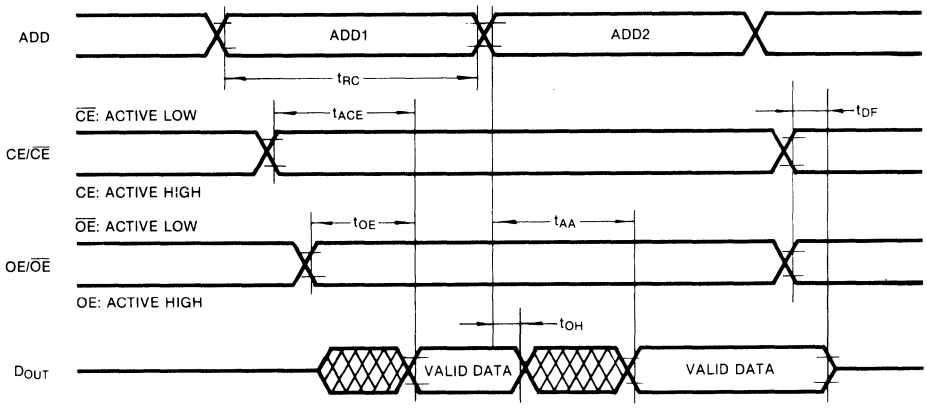
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4000H(G)-10		KM23C4000H(G)-12		KM23C4000H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

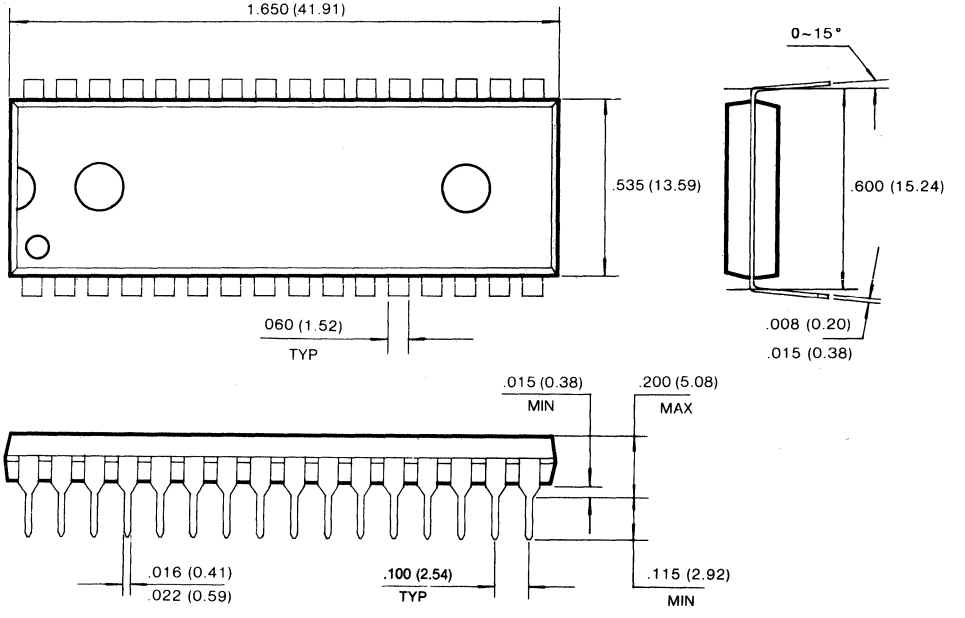


★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

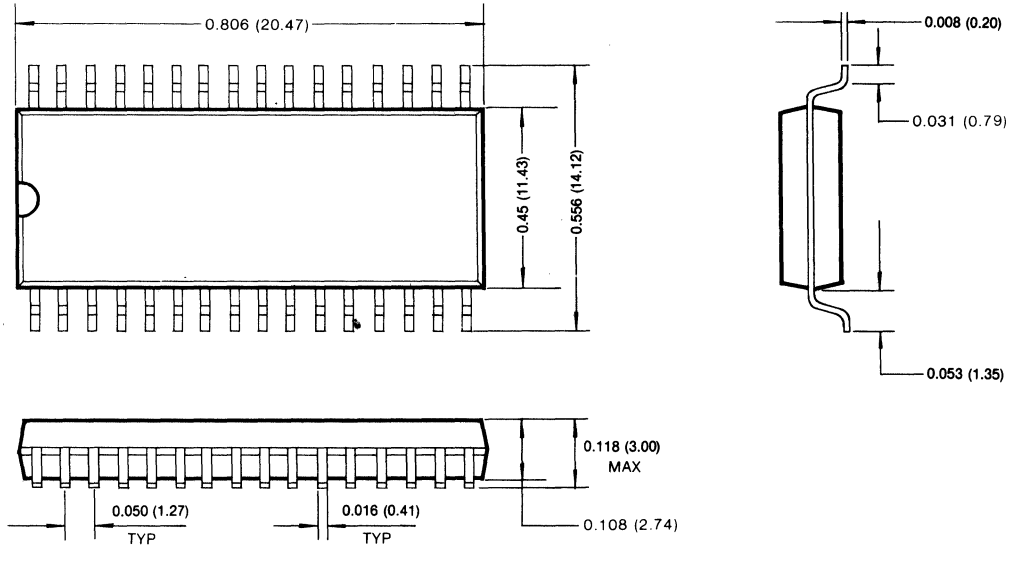
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4000H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4000HG)



SAMSUNG ELECTRONICS

4M-Bit (512K ×8) CMOS MASK ROM

FEATURES

- **524,288×8 bit organization**
- **Fast access time : 150ns(max).**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 32-pin, 600mil, plastic DIP**
  (JEDEC standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

The KM23V4000B is a fully static mask programmable ROM organized 524,288 8bit. It is fabricated using silicon-gate CMOS process technology.

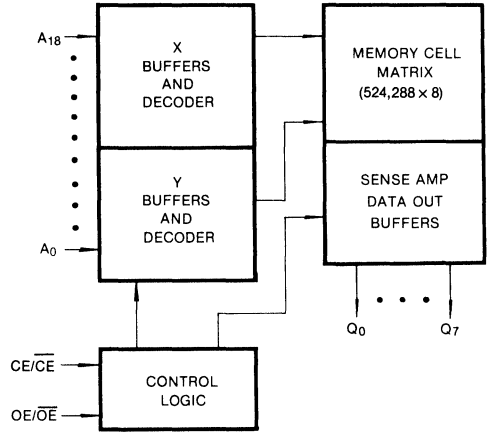
This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

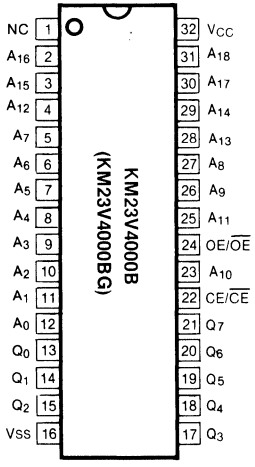
The KM23V4000B is packaged in a 32-DIP, and the KM23V4000BG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			- 0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V± 0.3)

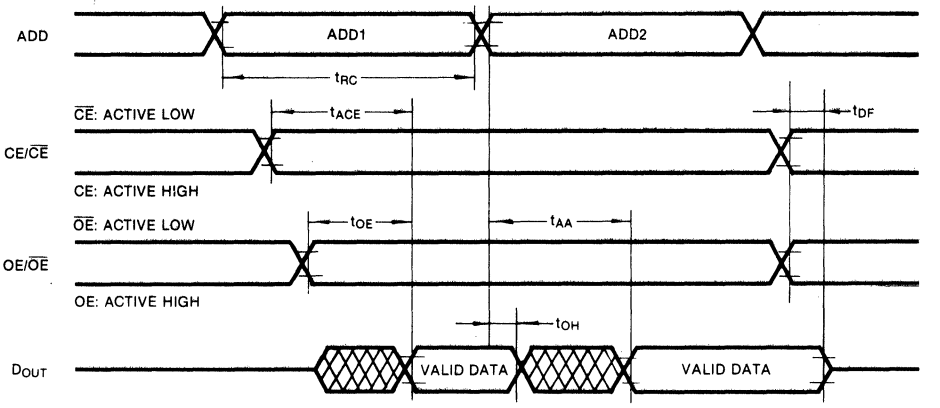
Parameter	Symbol	KM23V4000B(G)-20		KM23V4000B(G)-25		KM23V4000B(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V4000B(G)-15		KM23V4000B(G)-20		KM23V4000B(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

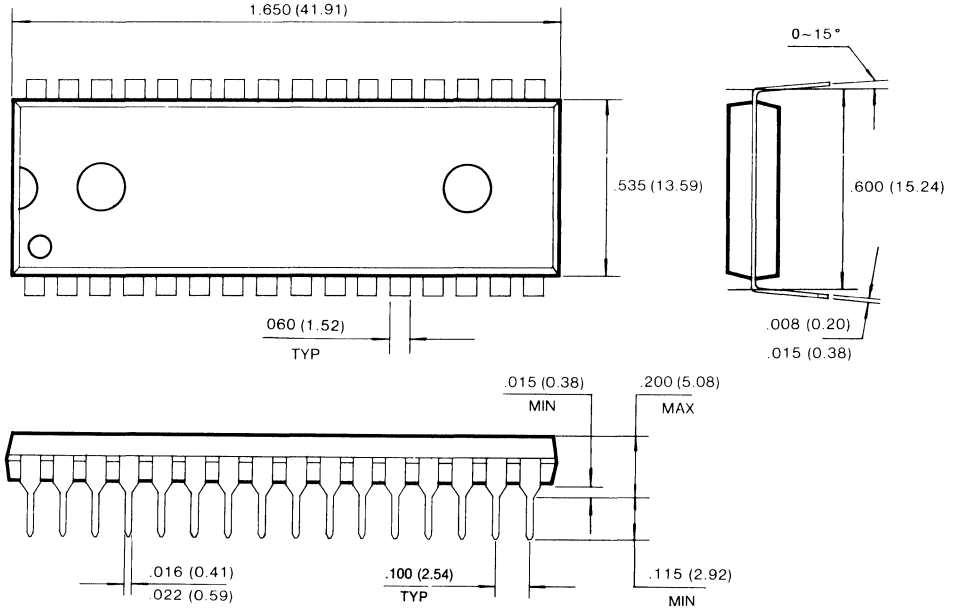
READ



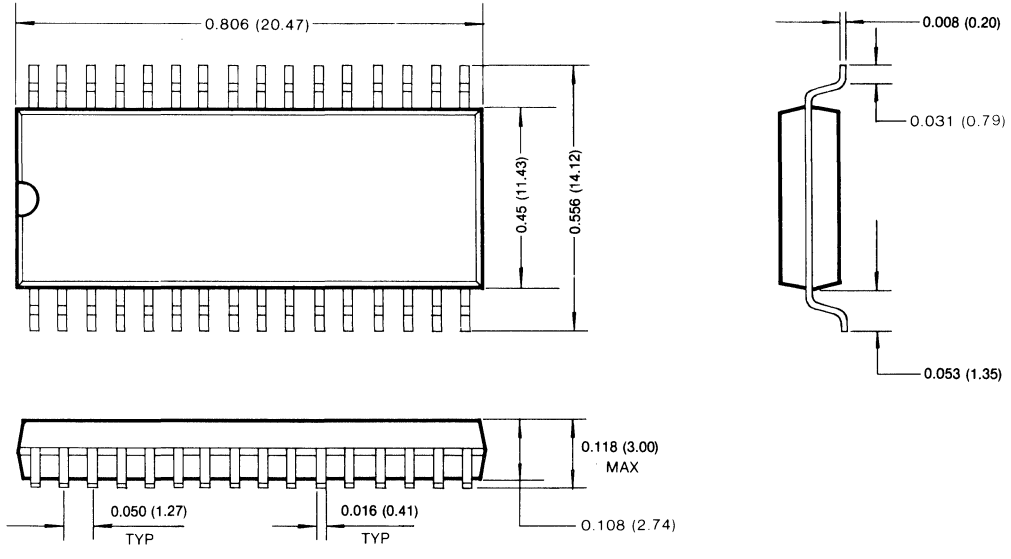
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V4000B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23V4000BG)



4M-Bit (512K x 8) CMOS MASK ROM

FEATURES

- **524,288 x 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**

  Operating: 60 mA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three-state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

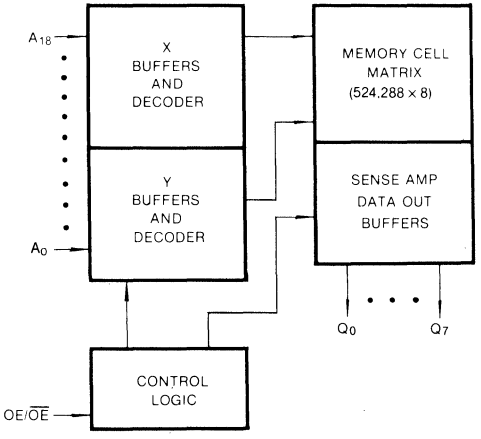
The KM23C4001B is a fully static mask programmable ROM organized 524,288 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

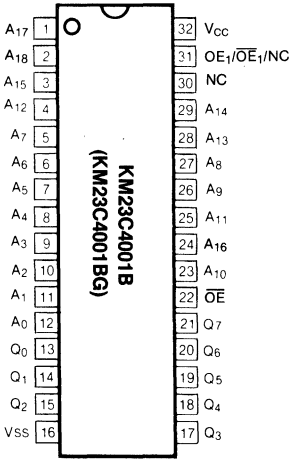
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4001B is packaged in a 32-DIP and the KM23C4001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$. $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

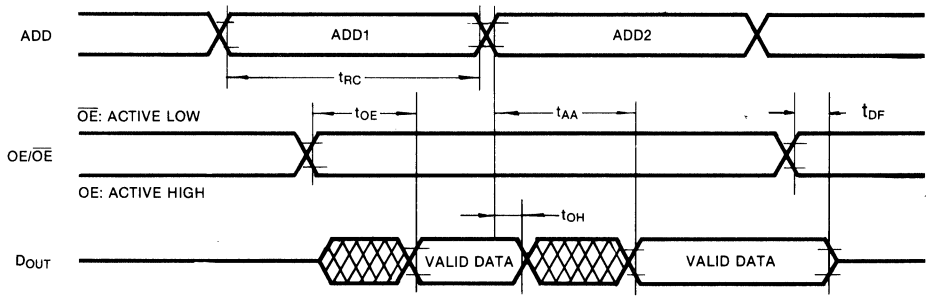
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4001B(G)-12		KM23C4001B(G)-15		KM23C4001B(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

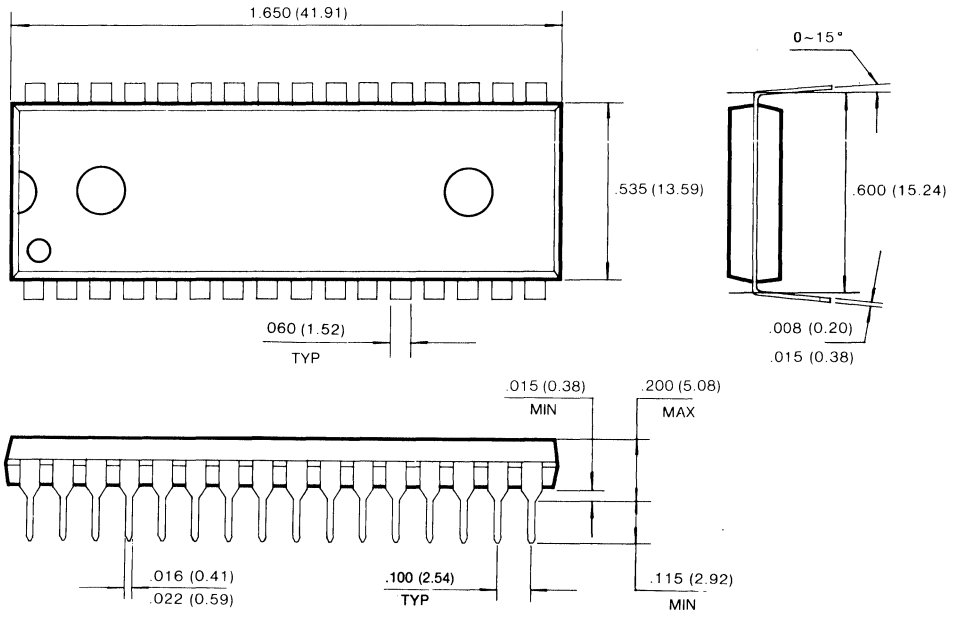
READ



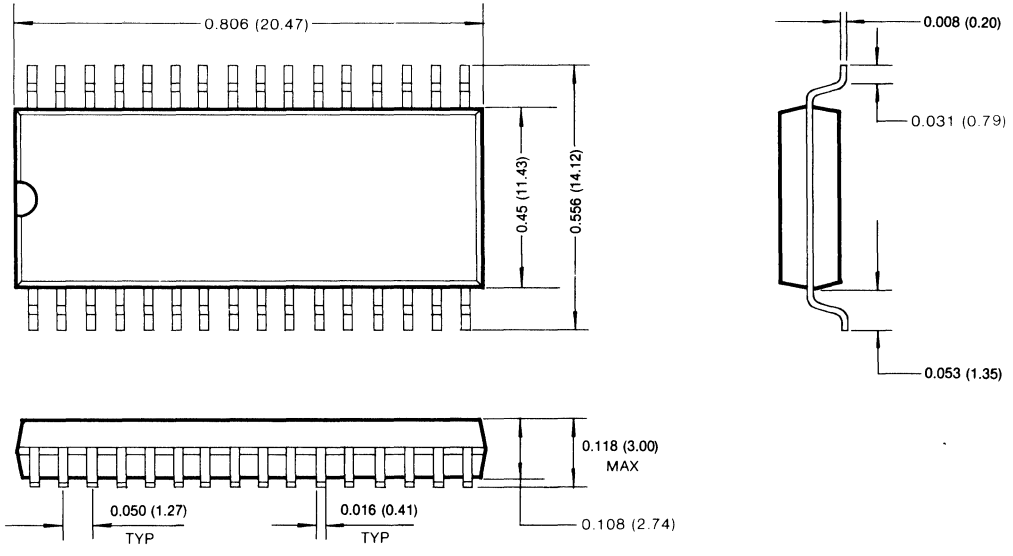
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4001B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4001BG)



4M-Bit (512K x 8) CMOS MASK ROM

FEATURES

- **524,288 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**

  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three-state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

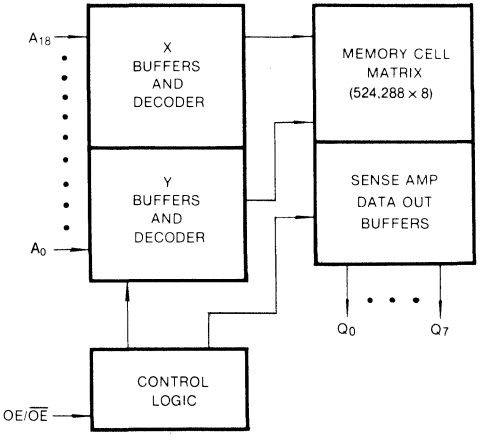
The KM23C4001H is a fully static mask programmable ROM organized 524,288 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

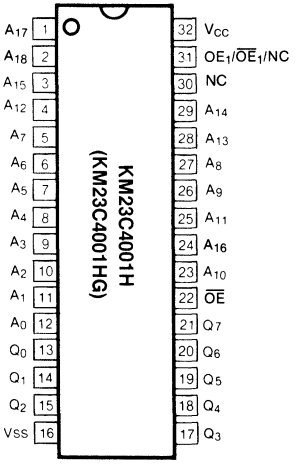
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4001H is packaged in a 32-DIP and the KM23C4001HG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	50	mA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

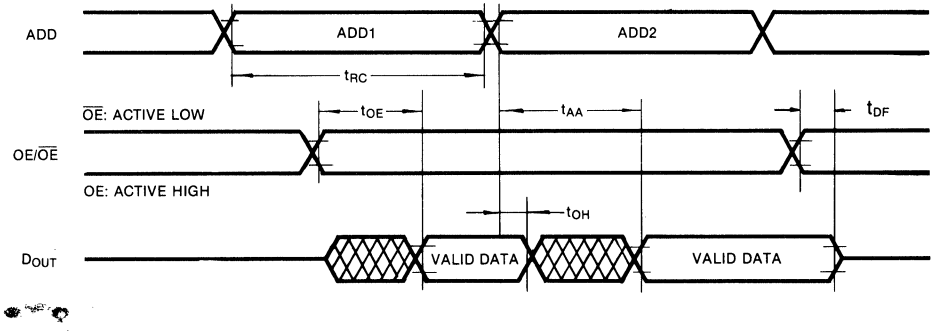
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4001H(G)-10		KM23C4001H(G)-12		KM23C4001H(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

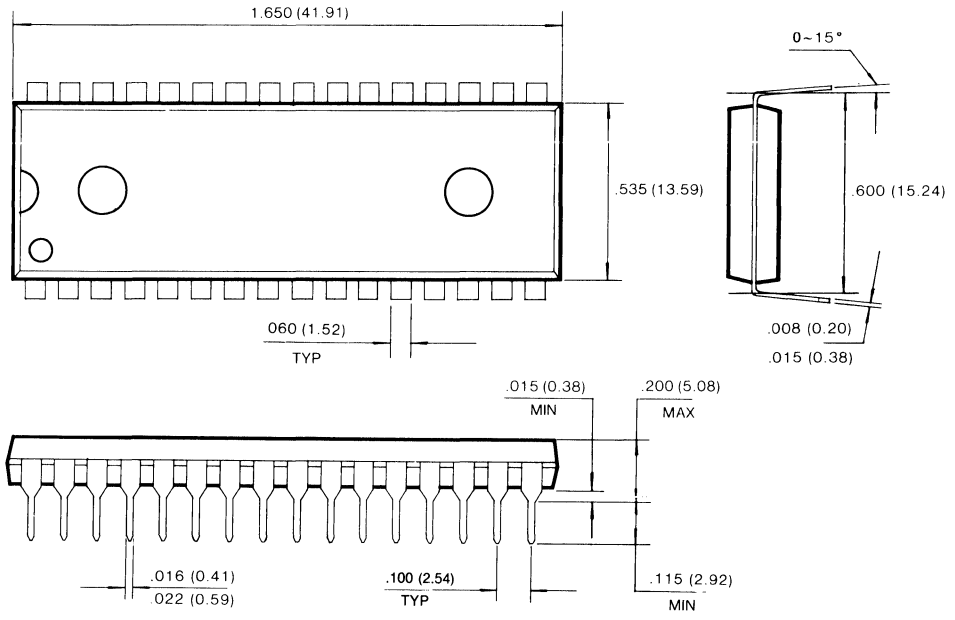


★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

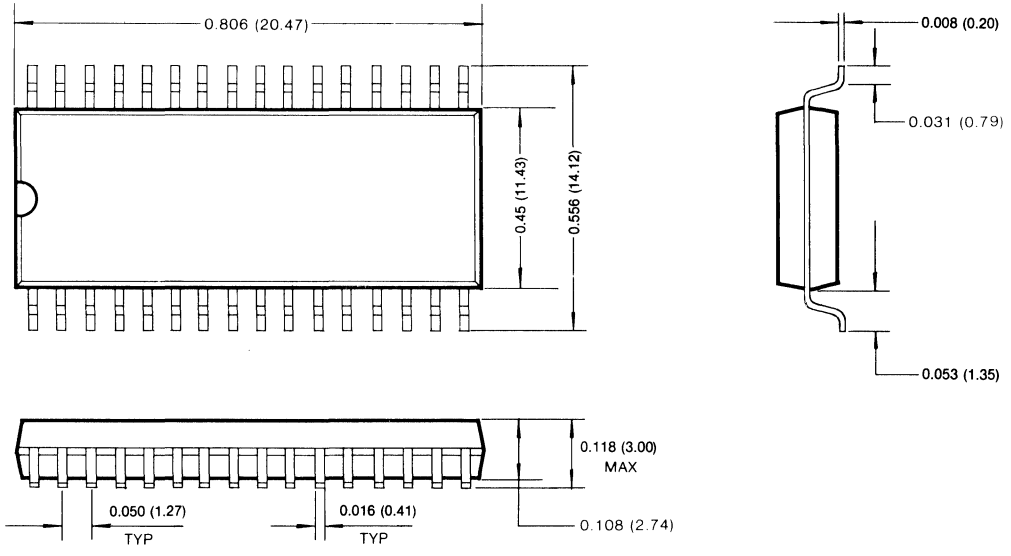
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4001H)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C4001HG)



4M-Bit (512K×8) CMOS MASK ROM

FEATURES

- **524,288×8 bit organization**
- **Fast access time : 150ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package : 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

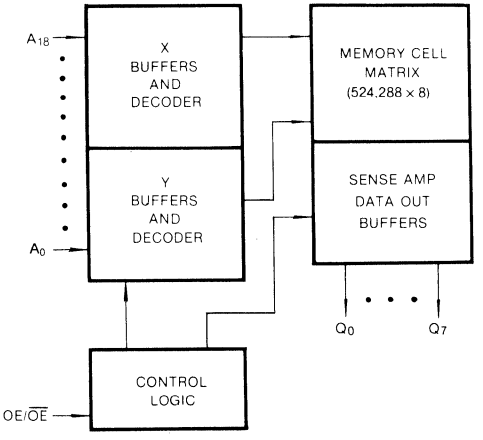
The KM23V4001B is a fully static mask programmable ROM organized 524,288×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

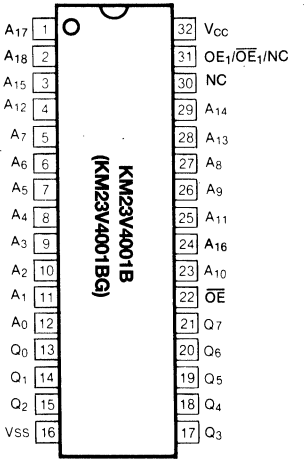
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V4001B is packaged in a 32-DIP, and the KM23V4001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			- 0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/OE	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V± 0.3)

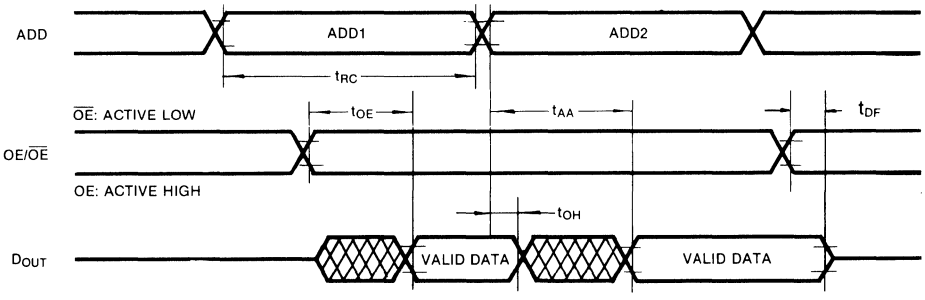
Parameter	Symbol	KM23V4001B(G)-20		KM23V4001B(G)-25		KM23V4001B(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V4001B(G)-15		KM23V4001B(G)-20		KM23V4001B(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

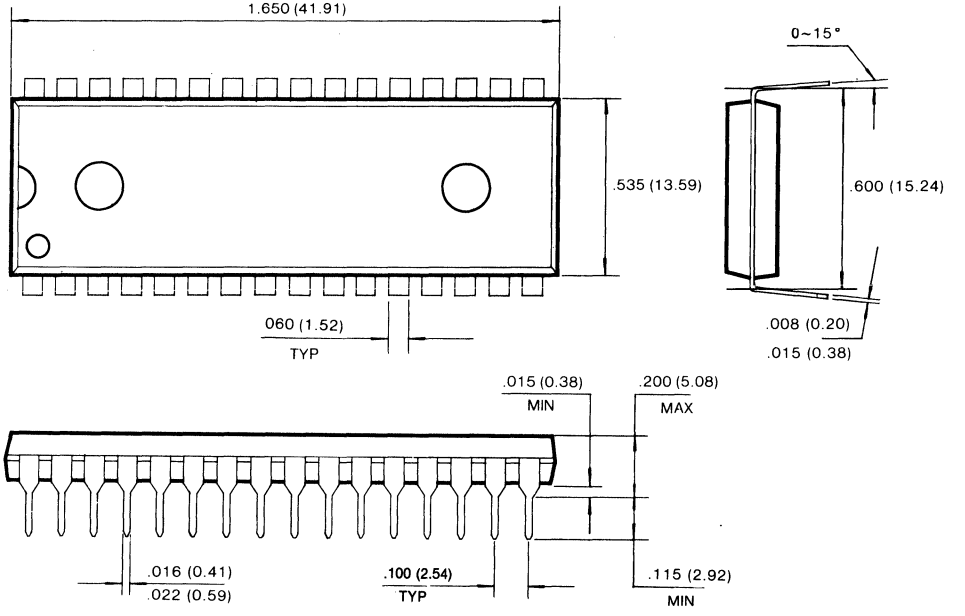
READ



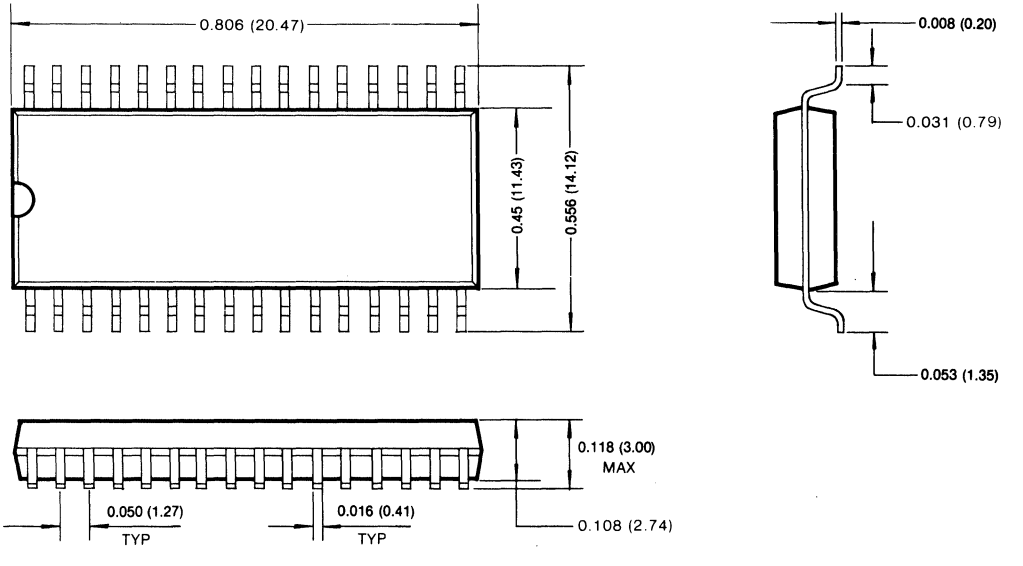
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V4001B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23V4001BG)



SAMSUNG ELECTRONICS

4M-Bit (512K x 8/256K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 x 8
  Word Mode: 262,144 x 16
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60 mA(max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  40-pin (525 mil, plastic SOP)
  44-pin QFP (14 x 14)

GENERAL DESCRIPTION

The KM23C4100B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 x 8 bit (byte mode) or as 262,144 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

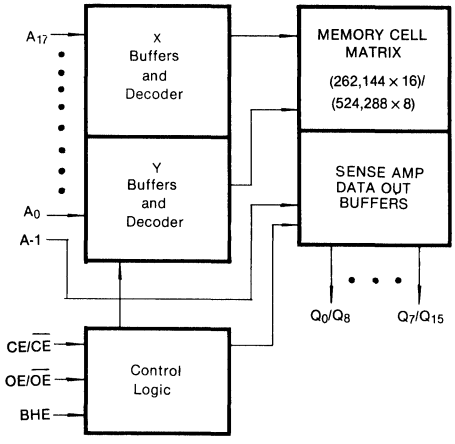
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

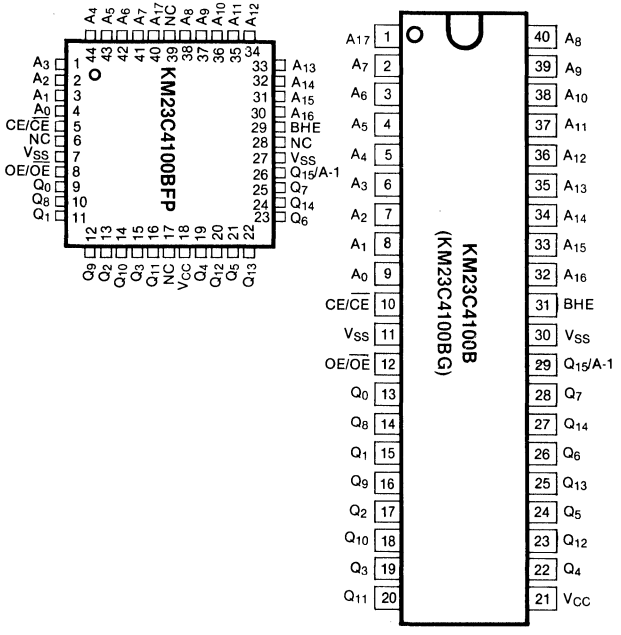
The KM23C4100B is packaged in a 40-DIP, and the KM23C4100BG in 40-SOP, and the KM23C4100BFP in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

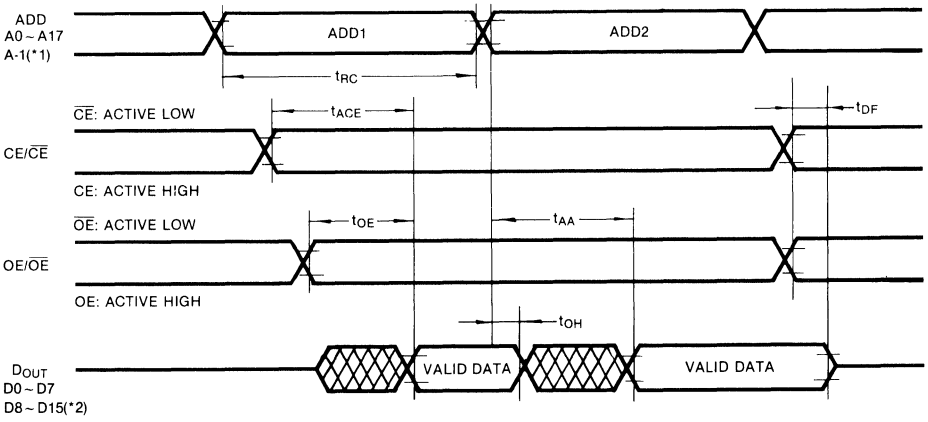
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4100B(G/FP)-12		KM23C4100B(G/FP)-15		KM23C4100B(G/FP)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

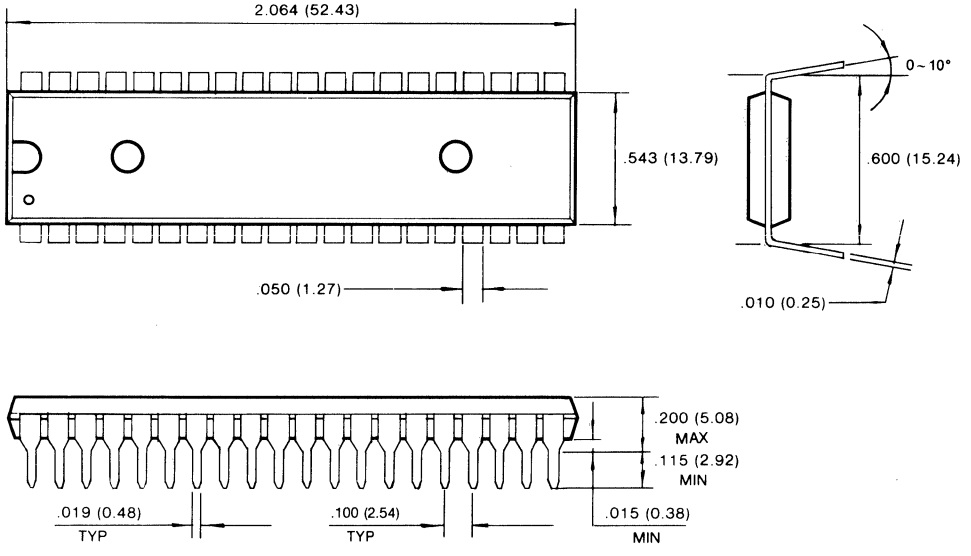


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

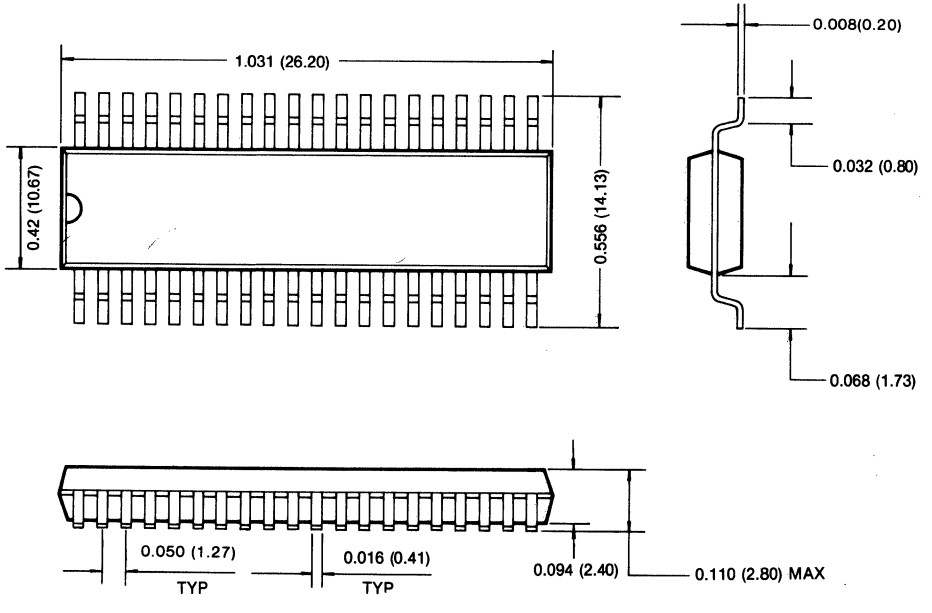
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4100B)

Units: Inches (millimeters)



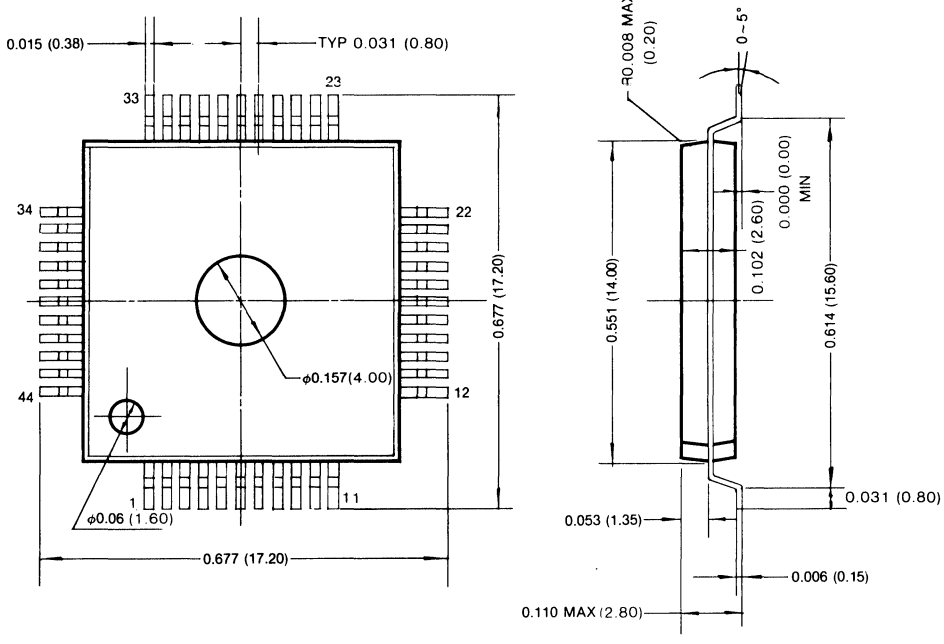
40 LEAD SMALL OUTLINE PACKAGE (KM23C4100BG)



PACKAGE DIMENSIONS (Continued)

Units: Inches (millimeters)

44 LEAD QUAD FLAT PACKAGE (KM23C4100BFP)



4M-Bit (512K x 8/256K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 x 8
  Word Mode: 262,144 x 16
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 100μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  44-pin QFP (14 x 14)

GENERAL DESCRIPTION

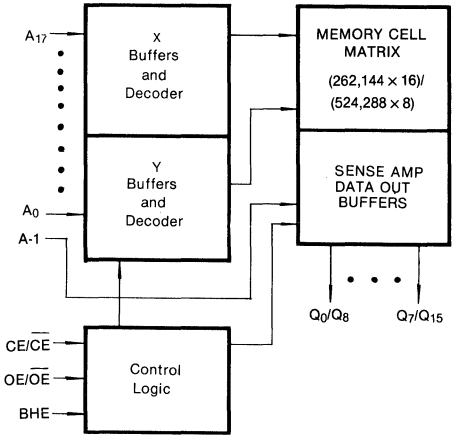
The KM23C4100H is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 x 8 bit (byte mode) or as 262,144 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

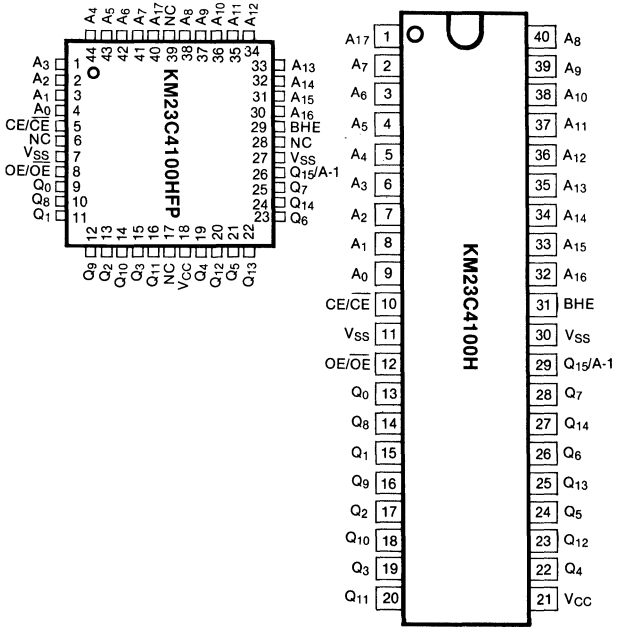
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C4100H is packaged in a 40-DIP, and the KM23C4100HFP in a 44-QFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	10.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

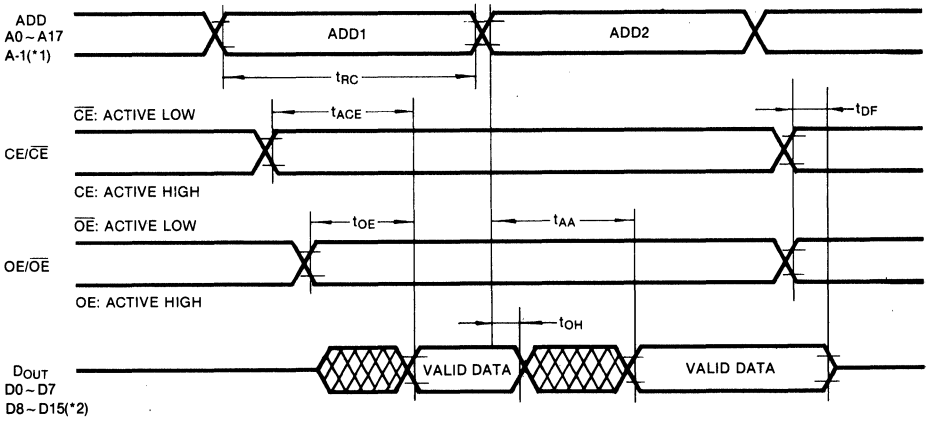
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C4100H(FP)-10		KM23C4100H(FP)-12		KM23C4100H(FP)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



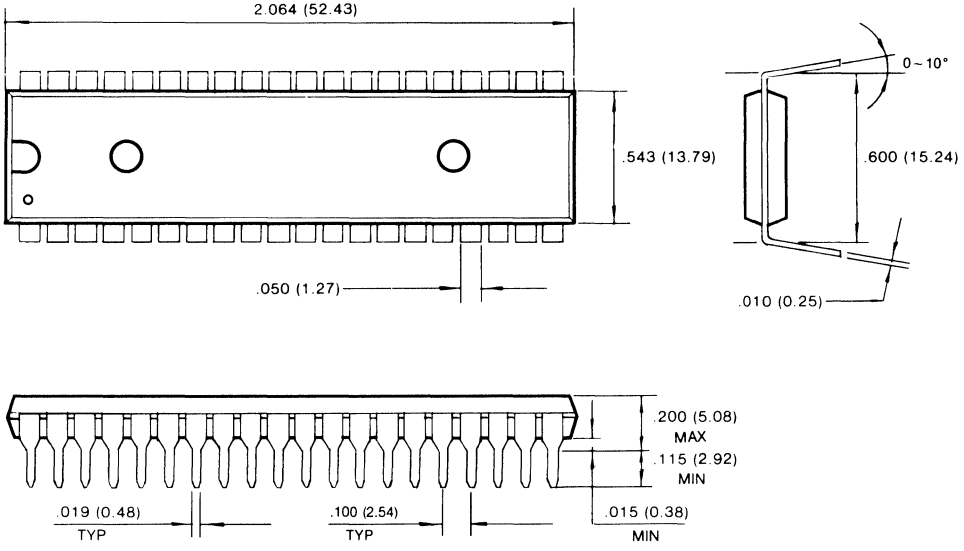
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

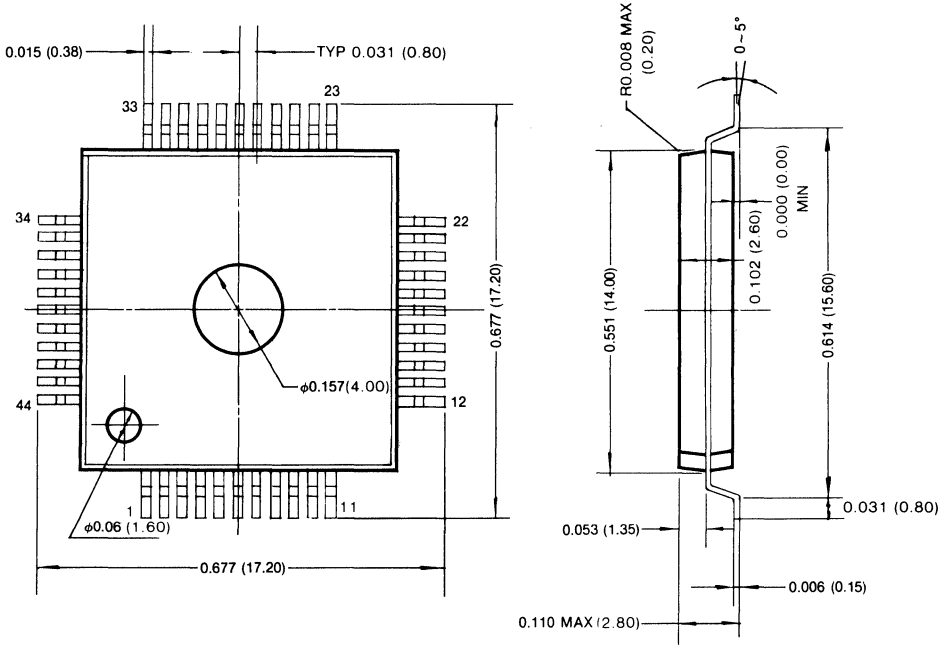
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4100H)

Units: Inches (millimeters)



44 LEAD QUAD FLAT PACKAGE (KM23C4100HFP)



4M-Bit (512K×8/256K×16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  524,288×8(byte mode)
  262,144×16(word mode)
- **Fast access time : 150ns(max.)**
- **Supply voltage : single+3.0V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 40-pin, 600mil, plastic DIP**
  (JEDEC Standard)

GENERAL DESCRIPTION

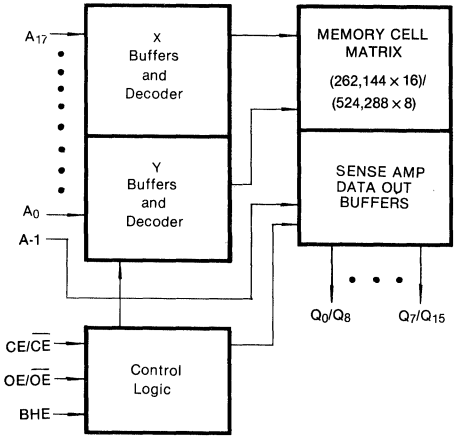
The KM23V4100B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is a organized either as 524,288×8 bit(byte mode)or as 262,144×16 bit(word mode)depending on BHE voltage level.(See mode selection table).

This device operates with a 3.0V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

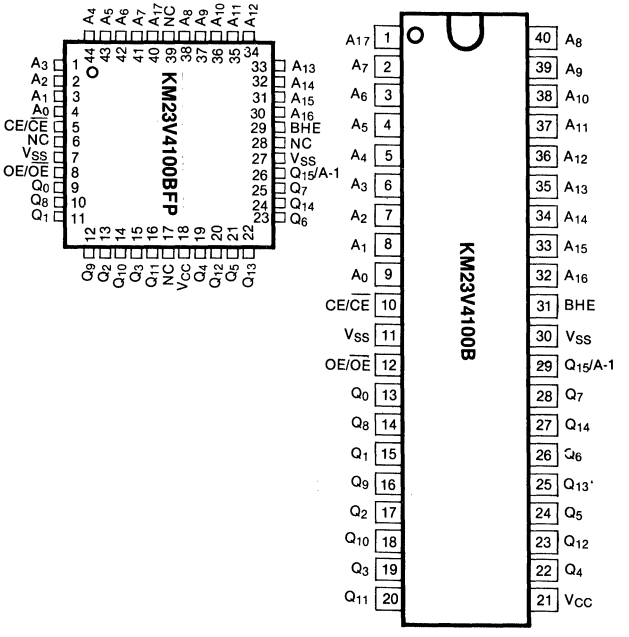
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V4100B is packaged in a 40-DIP, and the KM23V4100BFP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3.0V or 3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7 : D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to +70℃, V_{CC}=3.0V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

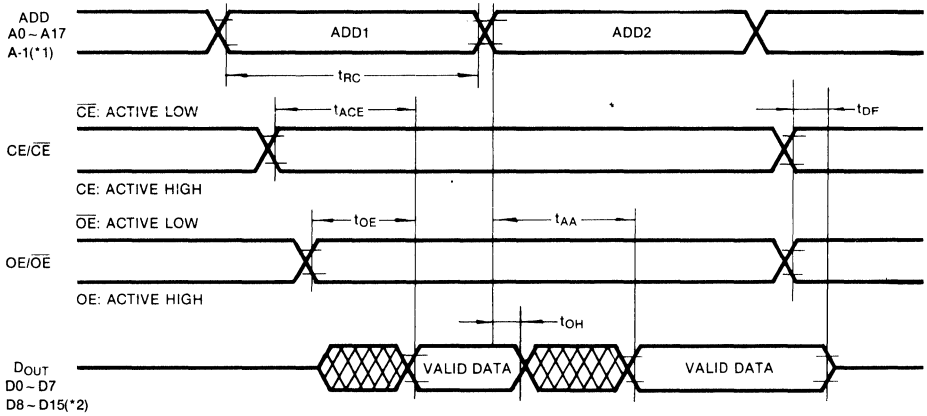
Parameter	Symbol	KM23V4100B(FP)-20		KM23V4100B(FP)-25		KM23V4100B(FP)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V4100B(FP)-15		KM23V4100B(FP)-20		KM23V4100B(FP)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



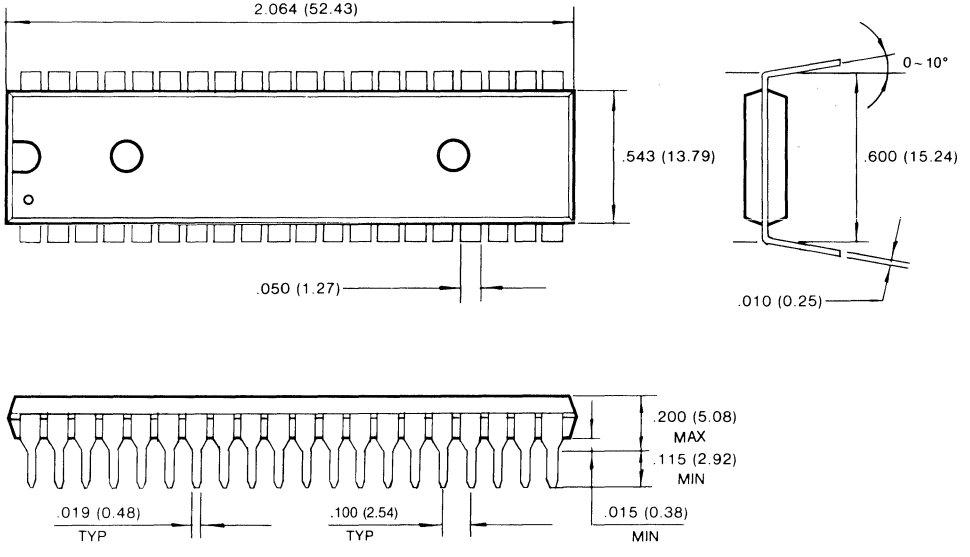
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

3

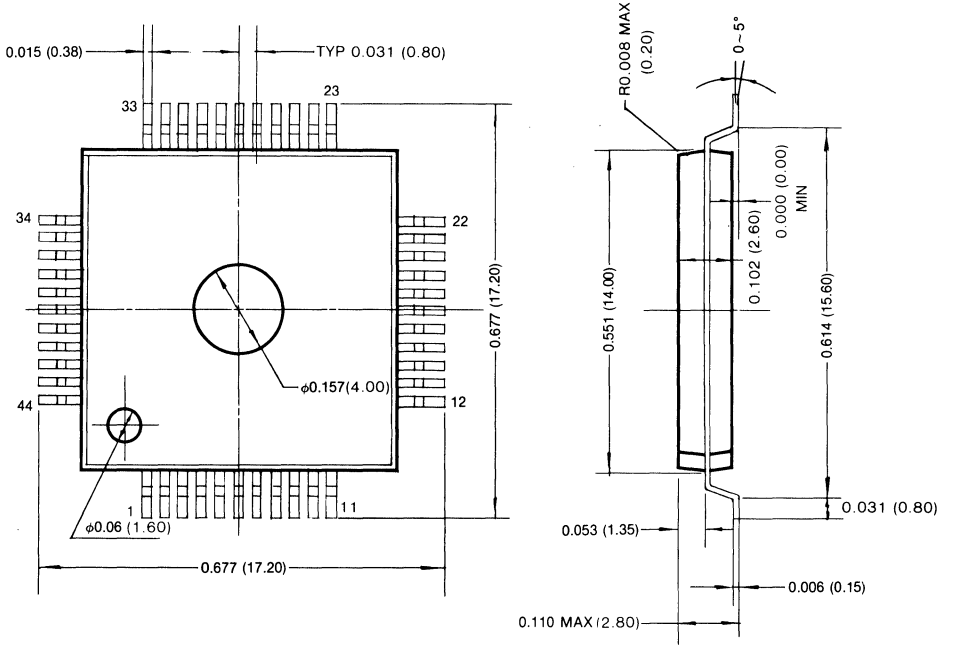
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V4100B)

Units: Inches (millimeters)



44 LEAD QUADFLAT PACKAGE (KM23V4100BFP)



4M-Bit (512K x 8/256K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  Byte Mode: 524,288 x 8
  Word Mode: 262,144 x 16
- **Fast access time: 120ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60 mA(max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 40-pin (600 mil, plastic DIP)**
  (JEDEC Standard)
  44-pin, PLCC

GENERAL DESCRIPTION

The KM23C4200B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is organized either as 524,288 x 8 bit (byte mode) or as 262,144 x 16 bit (word mode) depending on BHE (pin 1) voltage level. (See mode selection table).

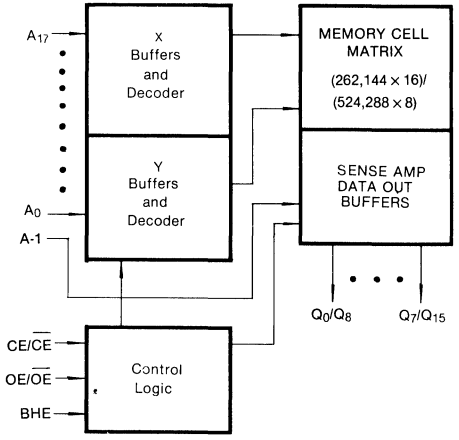
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

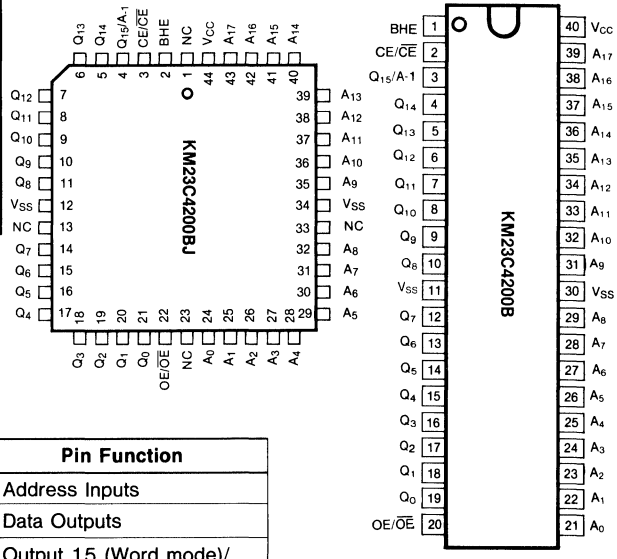
The KM23C 4200B is packaged in a 40-DIP, and the KM23C4200BJ in a 44 PLCC, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur If "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

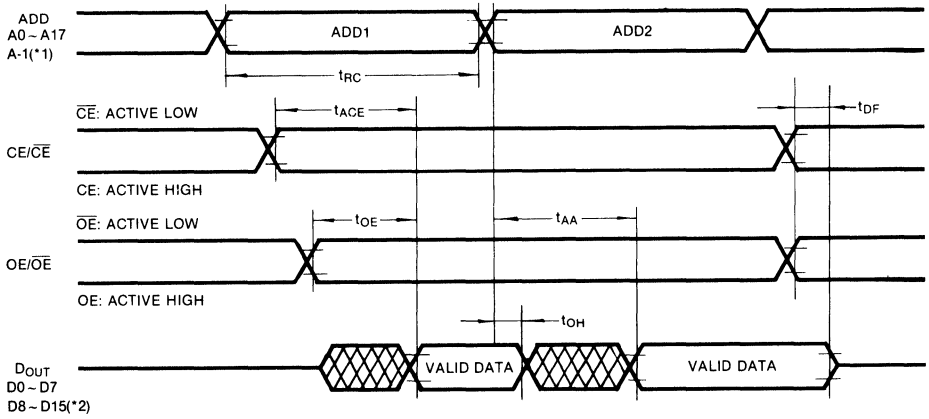
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C 4200B(J)-12		KM23C 4200B(J)-15		KM23C 4200B(J)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

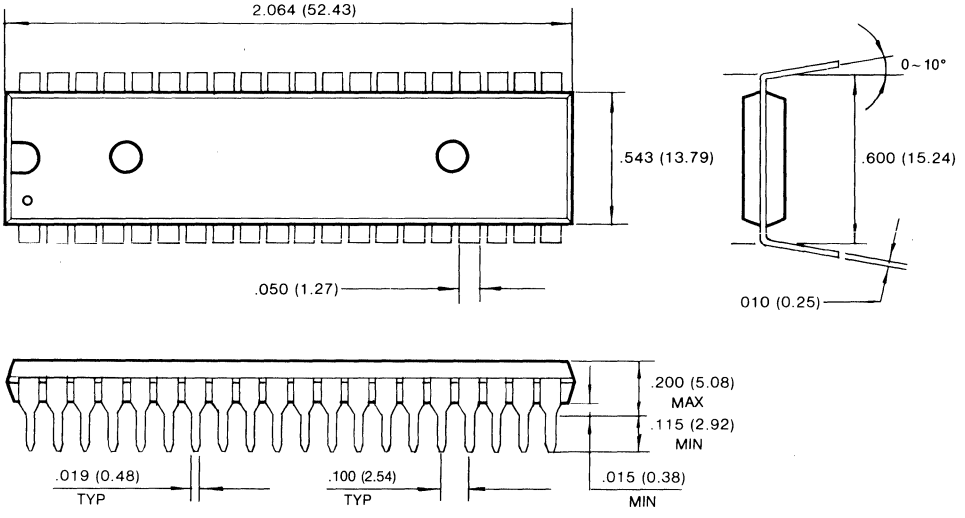


(*1) Byte Mode only. A-1 is Least Significant Bit Address. ($BHE = V_{IL}$)
(*2) Word Mode only. ($BHE = V_{IH}$)

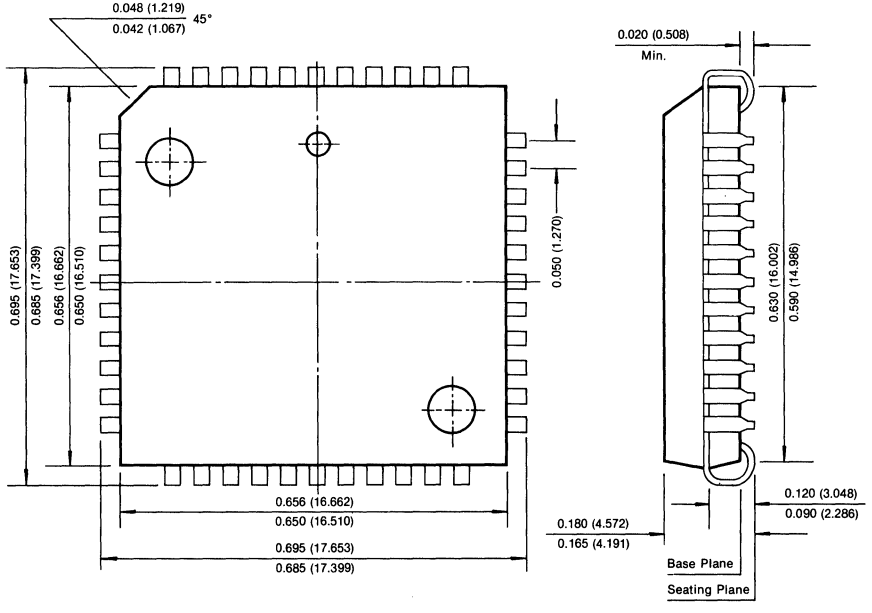
PACKAGE DIMENSIONS

40 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C4200B)

Units: Inches (millimeters)



44 PIN PLASTIC LEADED CHIP CARRIER (KM23C4200BJ)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 x 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  - **Operating: 50mA (max.)**
  - **Standby : 50μA (max.)**
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8000A is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

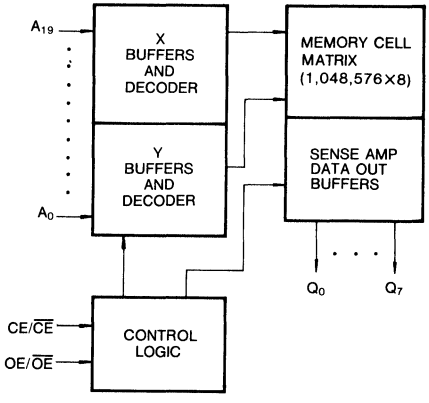
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

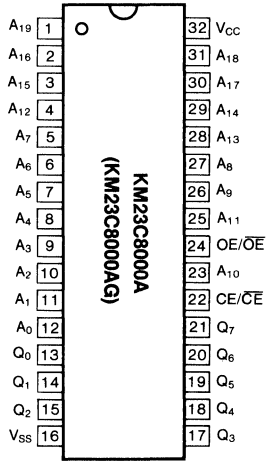
The KM23C8000A is packaged in a 32-DIP and the KM23C8000AG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

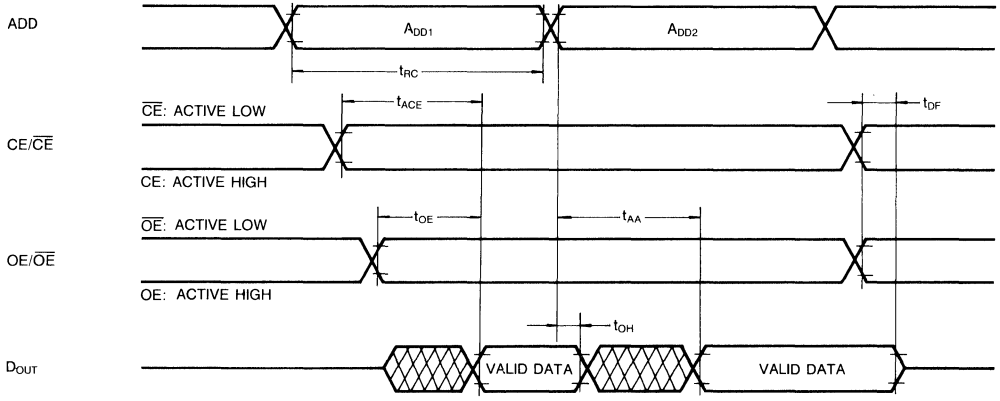
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM23C8000A(G)-15		KM23C8000A(G)-20		KM23C8000A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

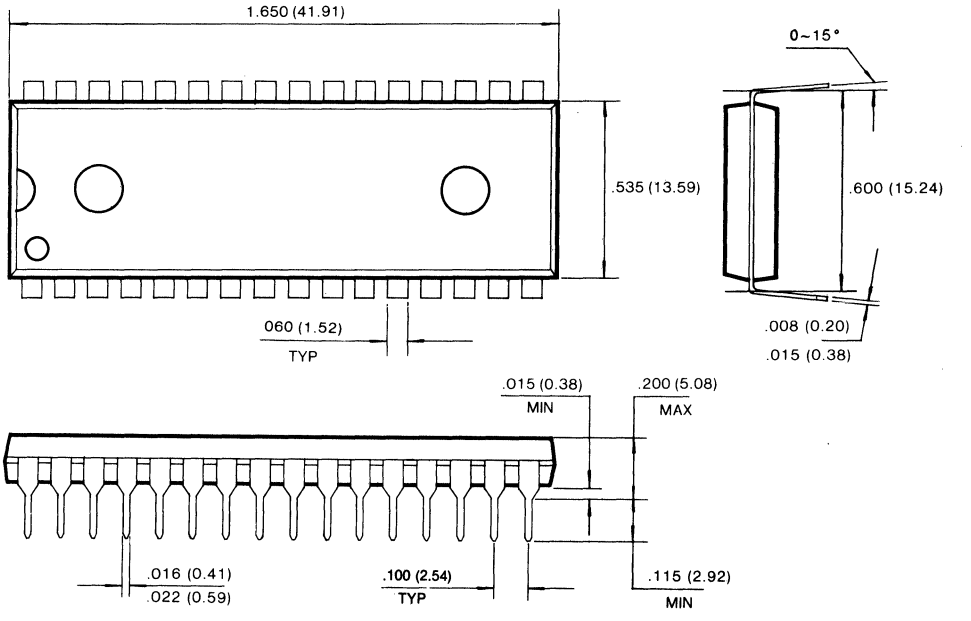


★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

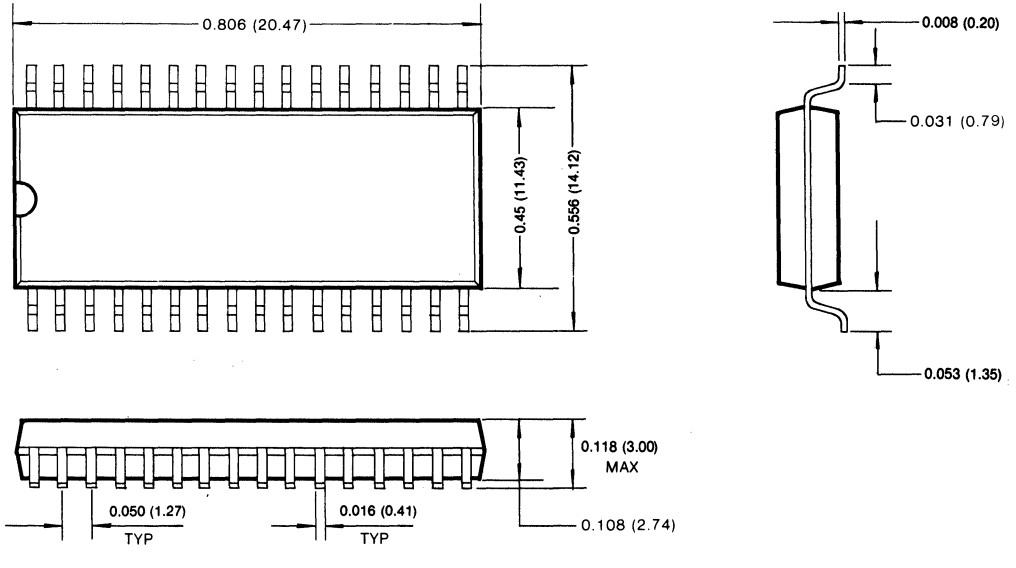
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8000AG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  - **Operating: 60mA (max.)**
  - **Standby : 50μA (max.)**
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8000B is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

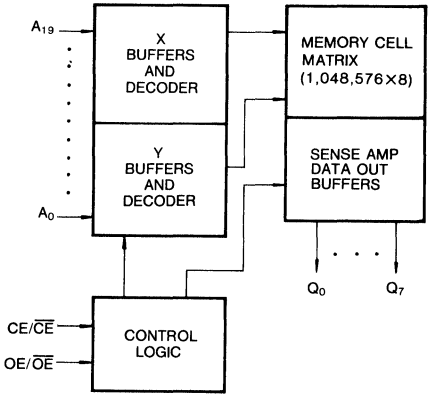
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

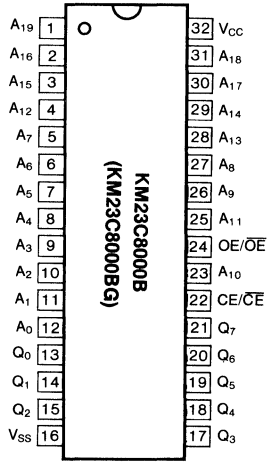
The KM23C8000B is packaged in a 32-DIP and the KM23C8000BG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

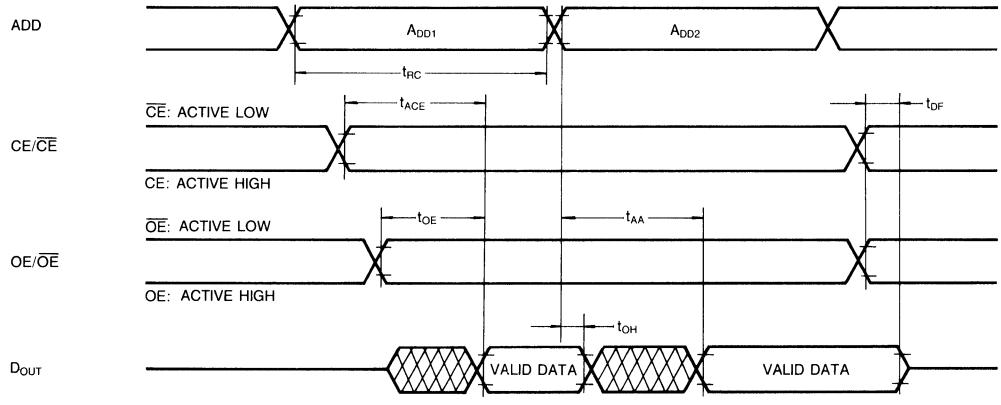
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C8000B(G)-10		KM23C8000B(G)-12		KM23C8000B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

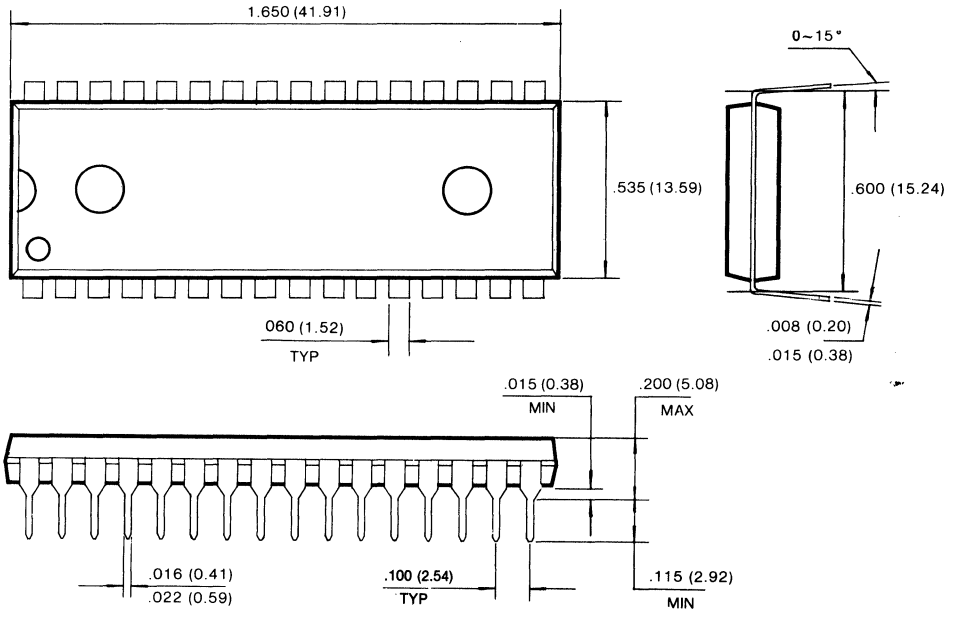


SAMSUNG ELECTRONICS

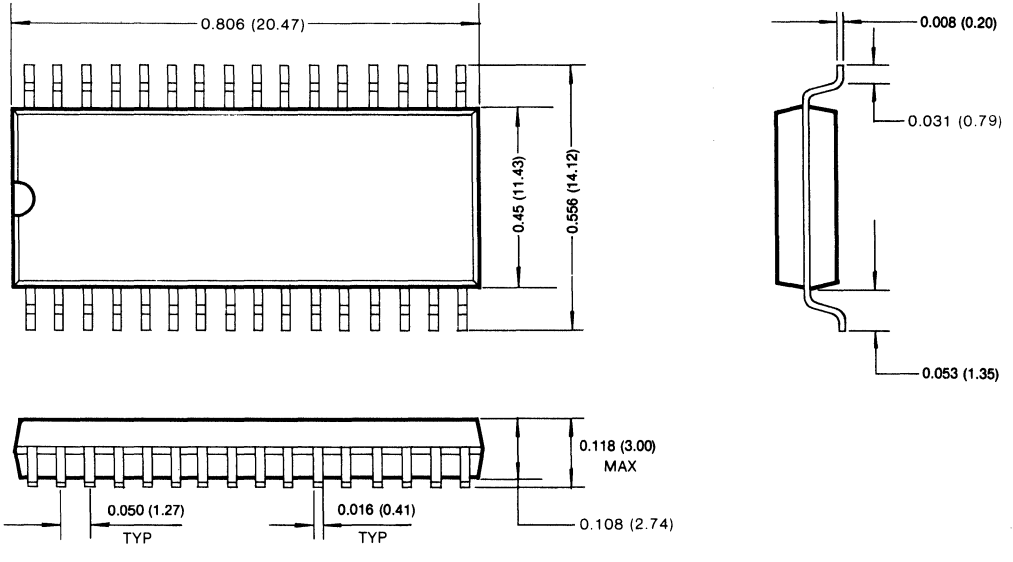
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8000B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8000BG)



8M-Bit (1M x 8) CMOS MASK ROM

FEATURES

- **1,048,576 x 8 bit organization**
- **Fast access time**
  Random access: 100ns (max.)
  Page access: 50ns (max.)
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 80 mA(max.)
  Standby: 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8005B is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576 x 8 bit.

This device is includes PAGE read mode function, page read mode allows two to four words of data to be read fast in the same page, CE and A_2-A_{19} should not be changed.

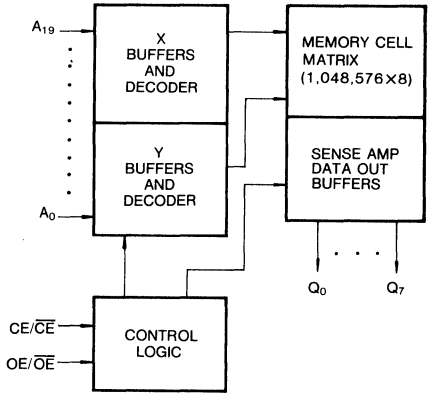
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

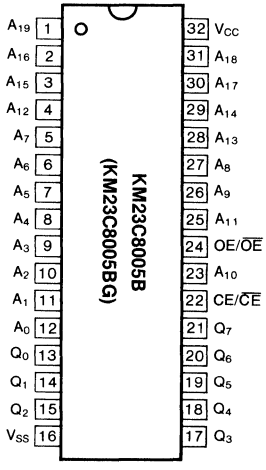
The KM23C8005B is packaged in a 32-DIP and the KM23C8005B in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_1	Page Address Inputs
A_2-A_{19}	Address Inputs
Q_0-Q_8	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	80	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

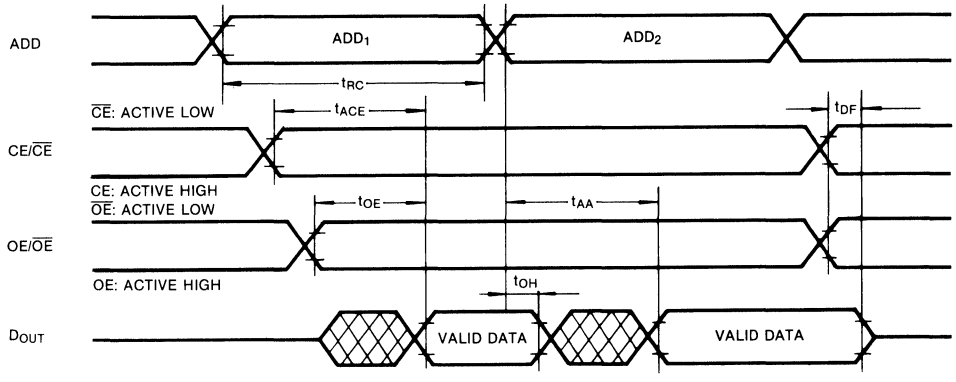
READ CYCLE

Parameter	Symbol	KM23C8005B(G)-10		KM23C8005B(G)-12		KM23C8005B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Page Address Access Time	t_{PA}		50		60		70	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

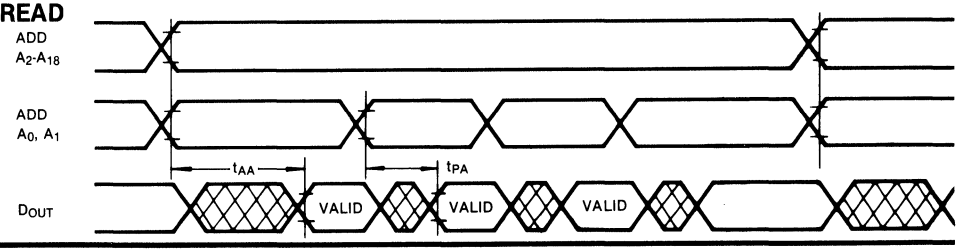
* Page Address: A_0, A_1

TIMING DIAGRAM

READ



PAGE READ

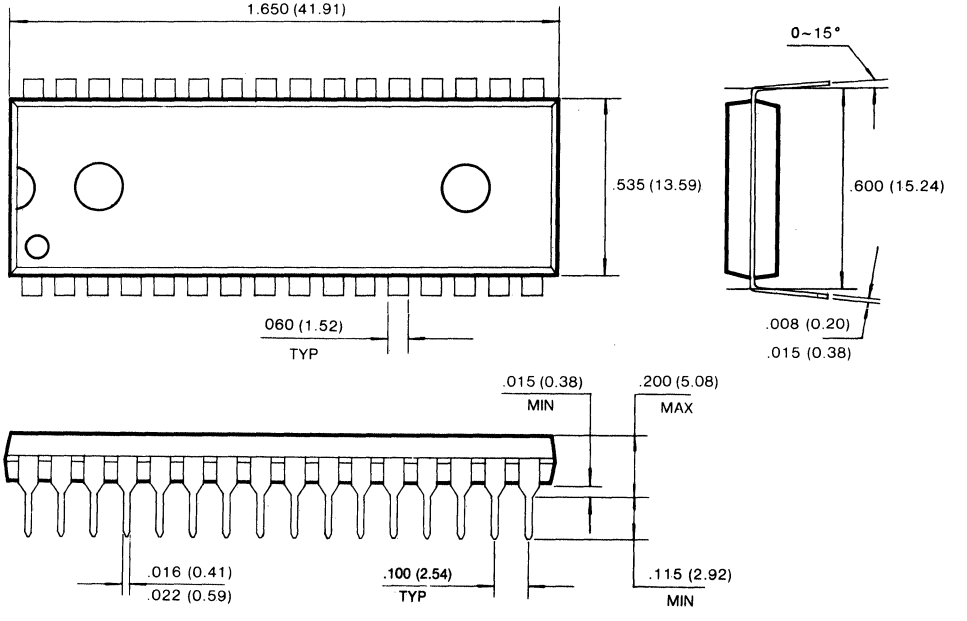


SAMSUNG ELECTRONICS

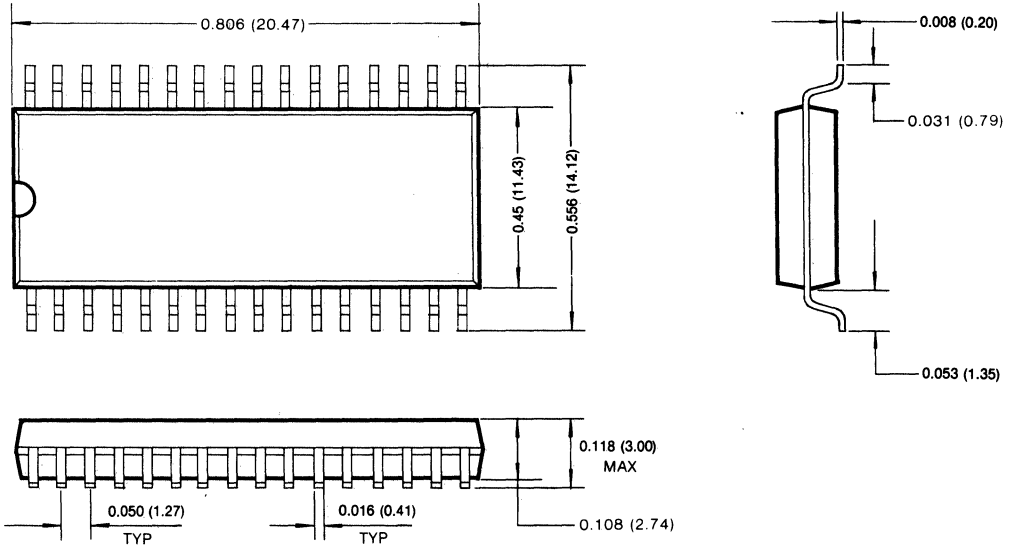
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8005B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8005BG)



8M-Bit (1M ×8) CMOS MASK ROM

FEATURES

- **1,048,576×8 bit organization**
- **Fast access time : 150ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

The KM23V8000B is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

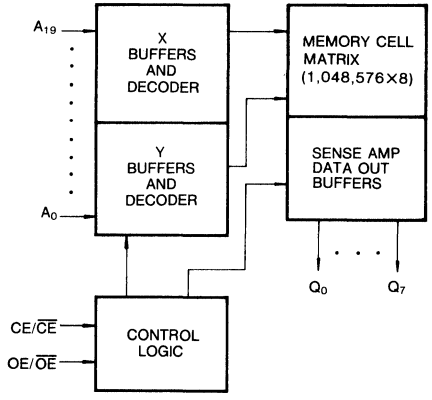
This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

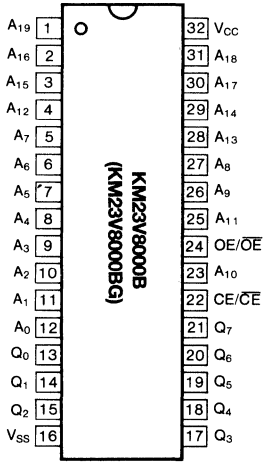
The KM23V8000B is packaged in a 32-DIP, and the KM23V8000BG in a 32-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground

* User Selectable Polarity

MODE SELECTION

CE/CE	OE/OE	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

Parameter	Symbol	KM23V8000B(G)-20		KM23V8000B(G)-25		KM23V8000B(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V8000B(G)-15		KM23V8000B(G)-20		KM23V8000B(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			- 0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

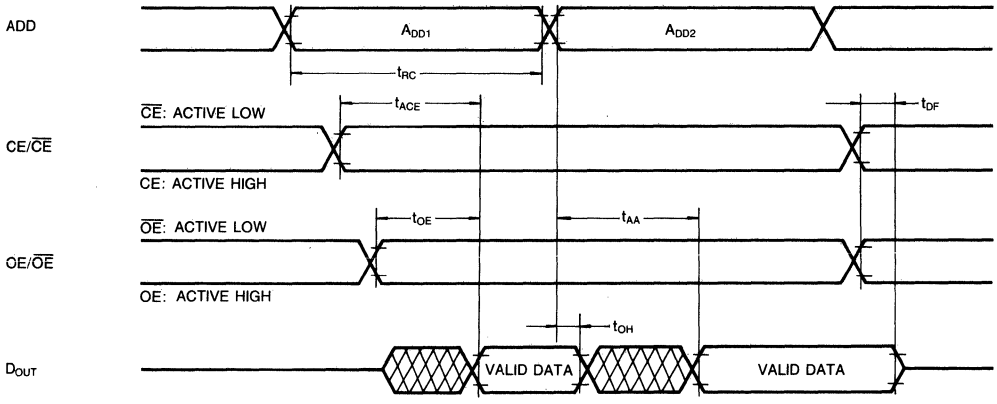
CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

TIMING DIAGRAM

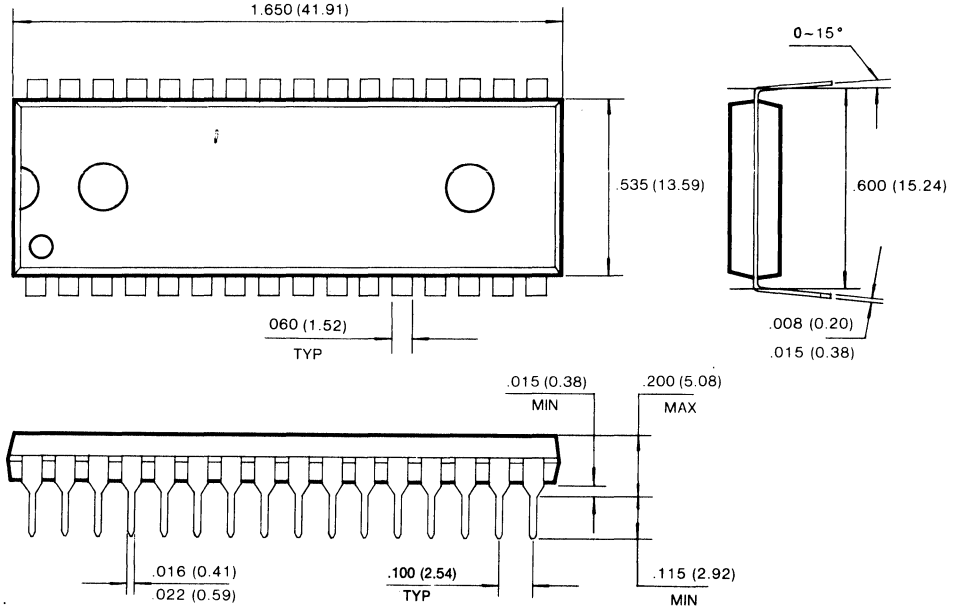
READ



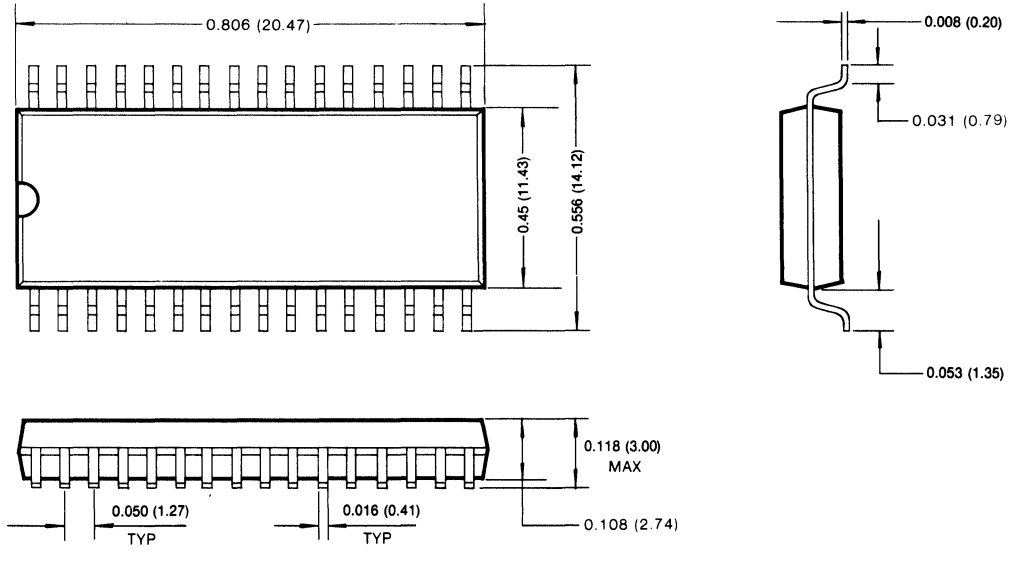
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V8000B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23V8000BG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 x 8 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 50mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

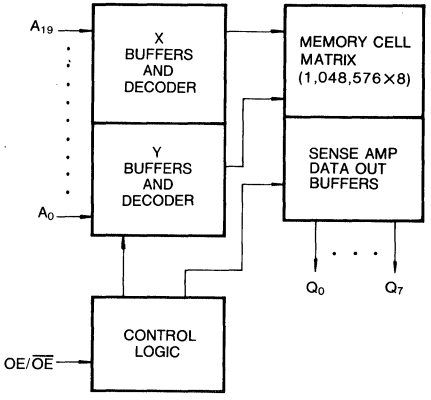
The KM23C8001A is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

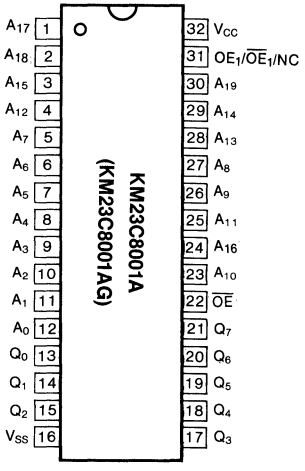
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8001A is packaged in a 32-DIP and the KM23C8001AG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	50	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}= −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

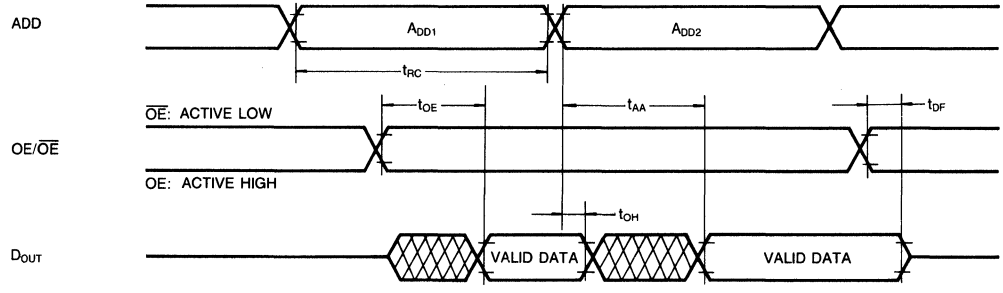
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C8001A(G)-15		KM23C8001A(G)-20		KM23C8001A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

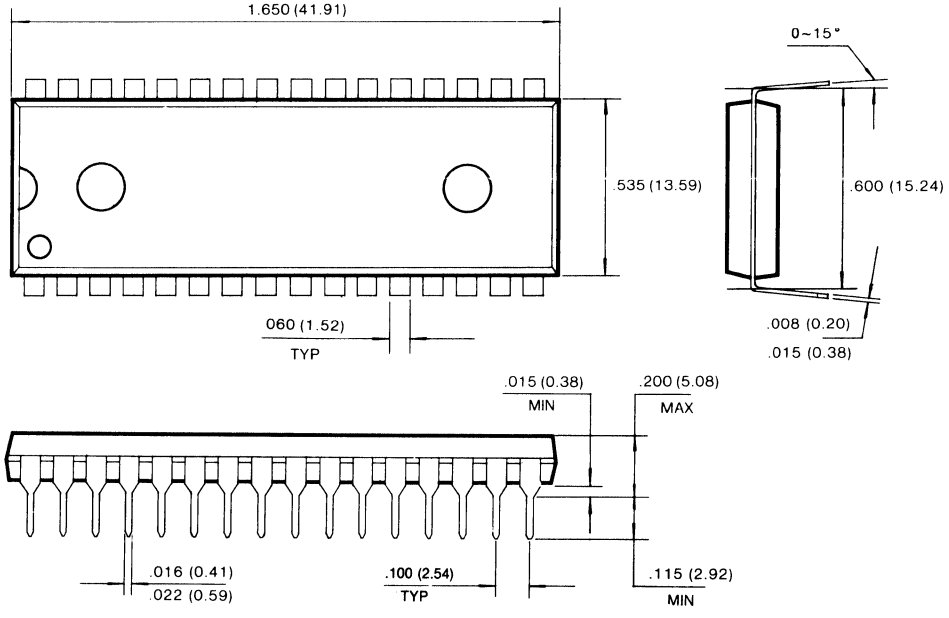


★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

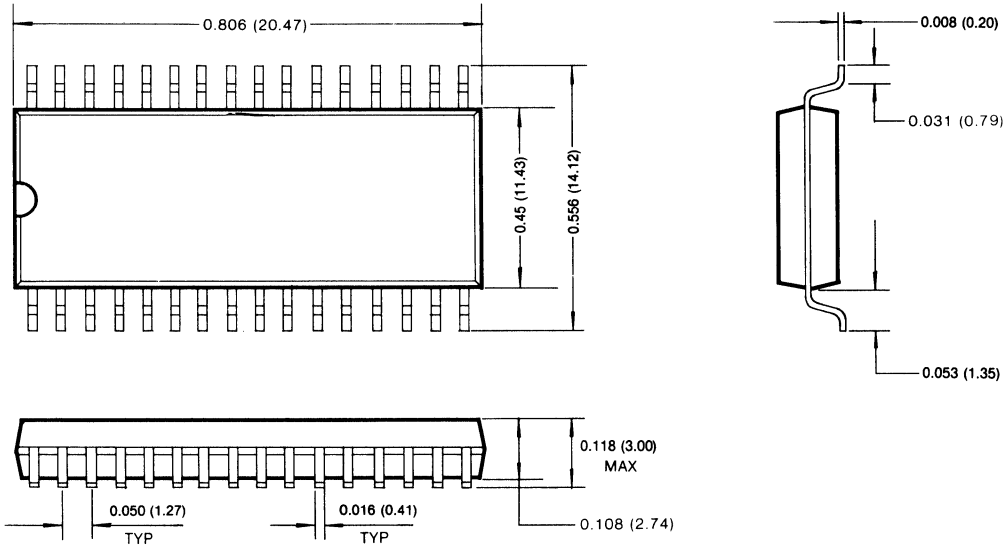
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8001A)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8001AG)



8M-Bit (1M X 8) CMOS MASK ROM

FEATURES

- **1,048,576 x 8 bit organization**
- **Fast access time: 100ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60 mA(max.)

- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package: 32-pin, 600 mil, plastic DIP (JEDEC standard)**
  32-pin, 525 mil, plastic SOP

GENERAL DESCRIPTION

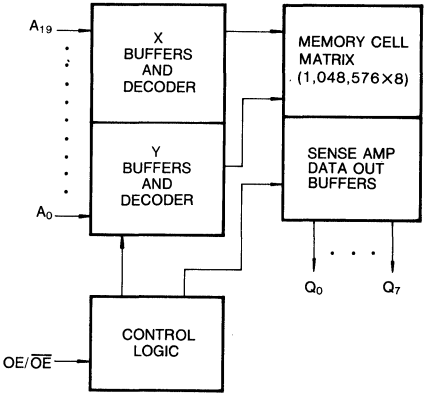
The KM23C8001B is a fully static mask programmable ROM organized 1,048,576×8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

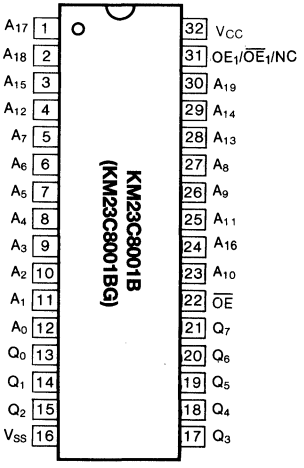
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8001B is packaged in a 32-DIP and the KM23V8001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/$\overline{OE}$	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS (Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

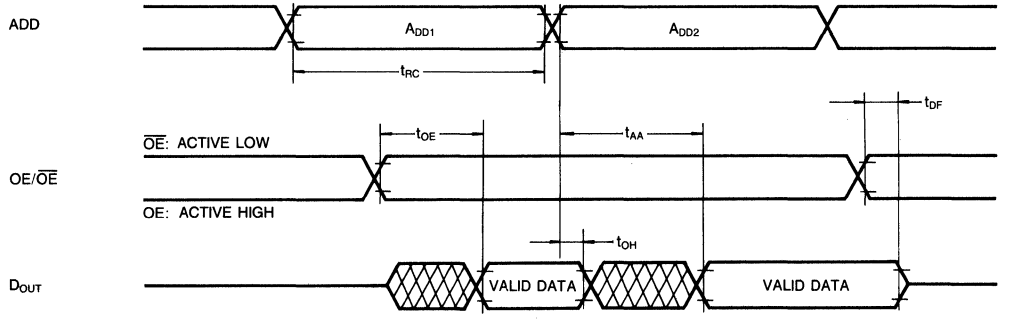
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C8001B(G)-10		KM23C8001B(G)-12		KM23C8001B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

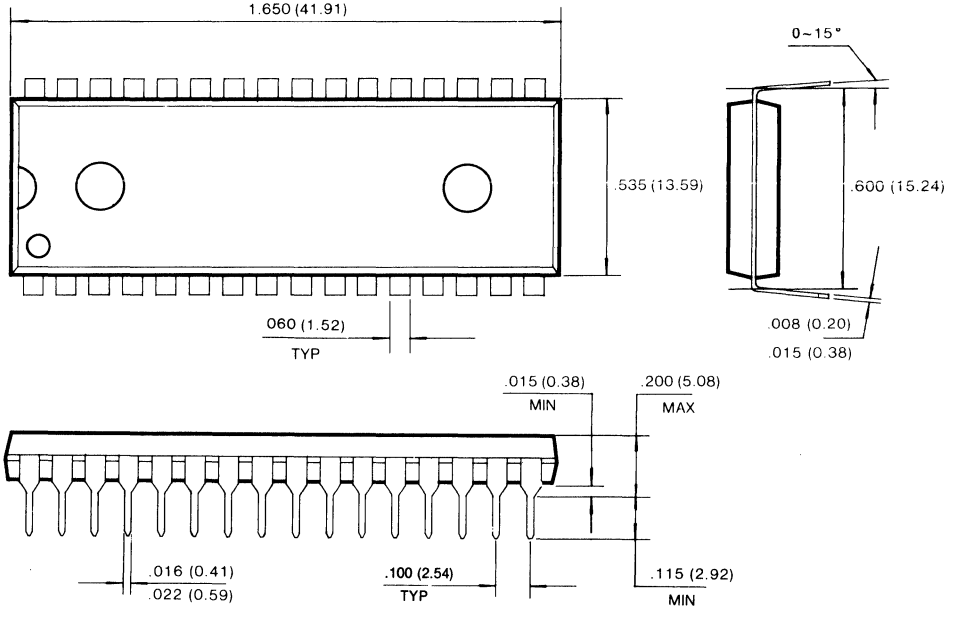
READ



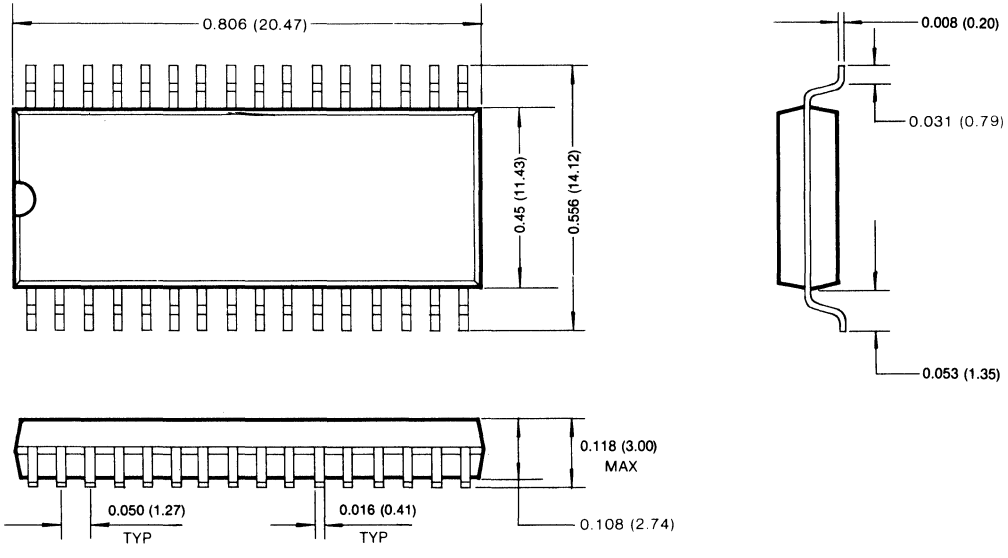
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8001B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23C8001BG)



8M-Bit (1M ×8) CMOS MASK ROM

FEATURES

- **1,048,576×8 bit organization**
- **Fast access time : 150ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable output enable pin**
- **Package : 32-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  32-pin, 525mil, plastic SOP

GENERAL DESCRIPTION

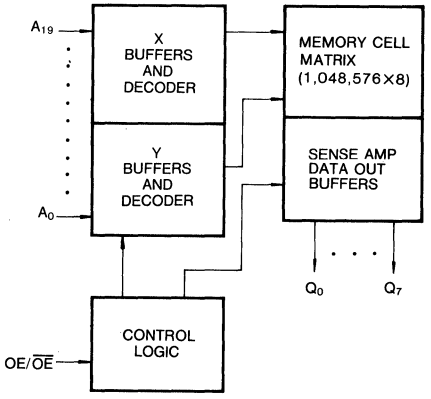
The KM23V8001B is a fully static mask programmable ROM organized 1,048,576 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

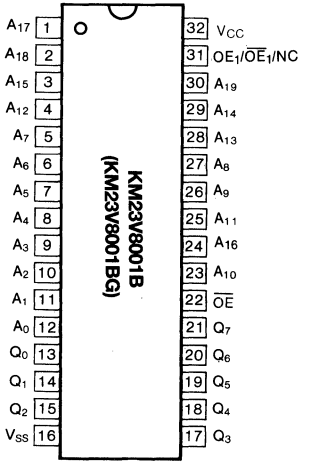
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V8001B is packaged in a 32-DIP, and the KM23V8001BG in a 32-SOP, provides polarity programmable OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			- 0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/OE	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

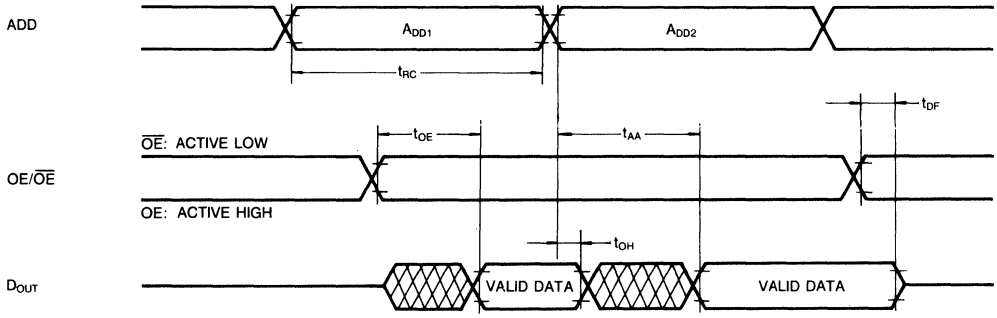
Parameter	Symbol	KM23V8001B(G)-20		KM23V8001B(G)-25		KM23V8001B(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V8001B(G)-15		KM23V8001B(G)-20		KM23V8001B(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



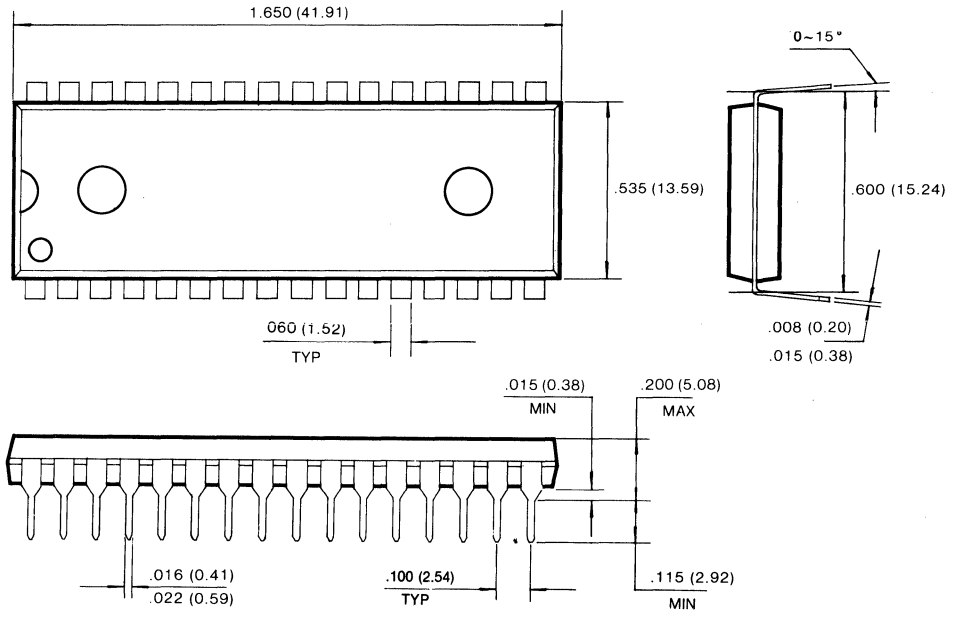
3

SAMSUNG ELECTRONICS

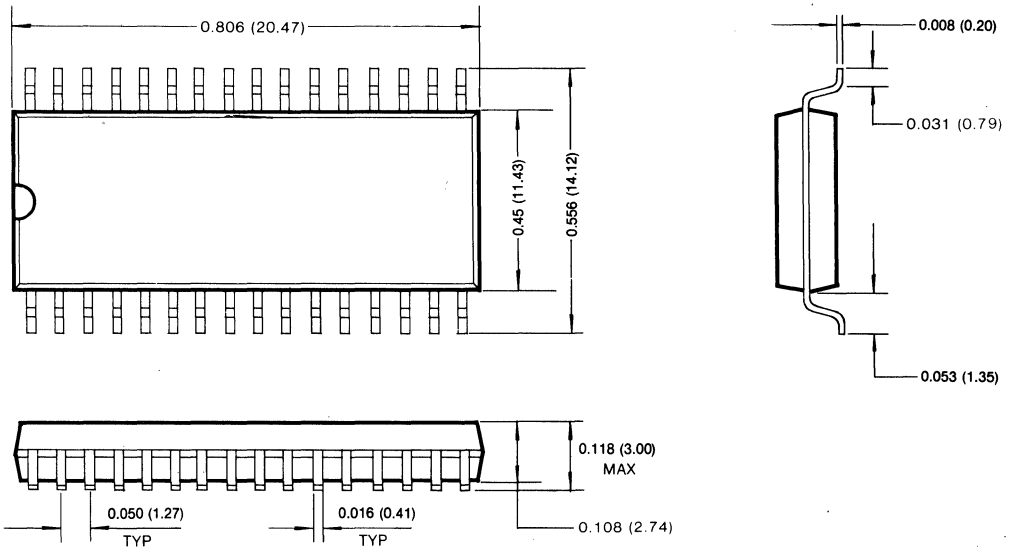
PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V8001B)

Units: Inches (millimeters)



32 LEAD SMALL OUTLINE PACKAGE (KM23V8001BG)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 x 8 (byte mode)
  524,288 x 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8100A is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576×8 bit (byte mode) or as 524,288×16 bit (word mode) depending on BHE voltage level. (See mode selection table).

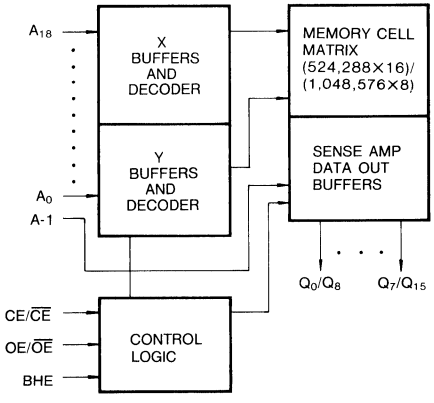
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100A is packaged in a 42-DIP and the KM23C8100AG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

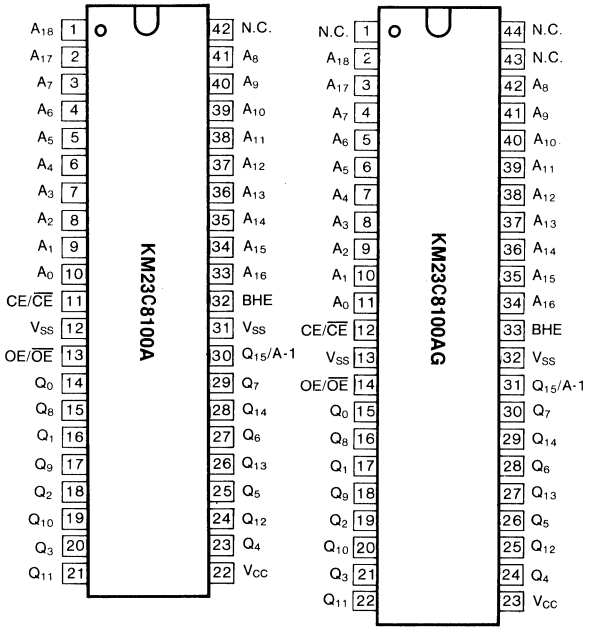
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}= −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

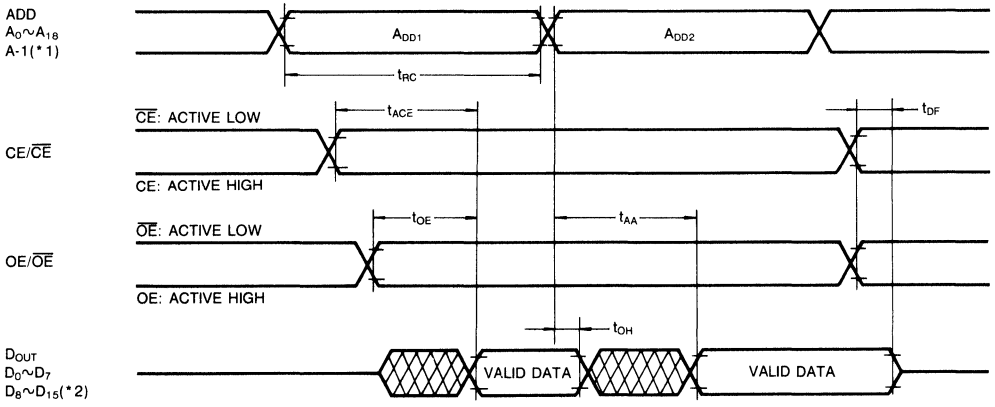
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C8100A(G)-15		KM23C8100A(G)-20		KM23C8100A(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



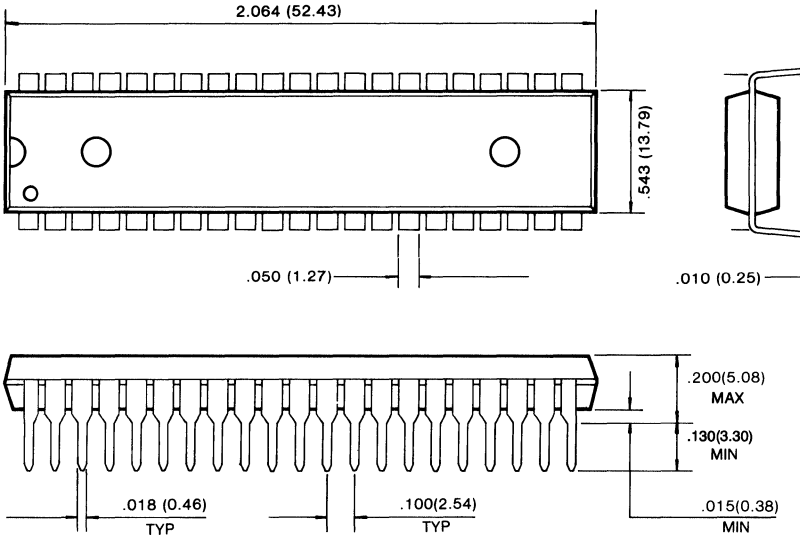
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

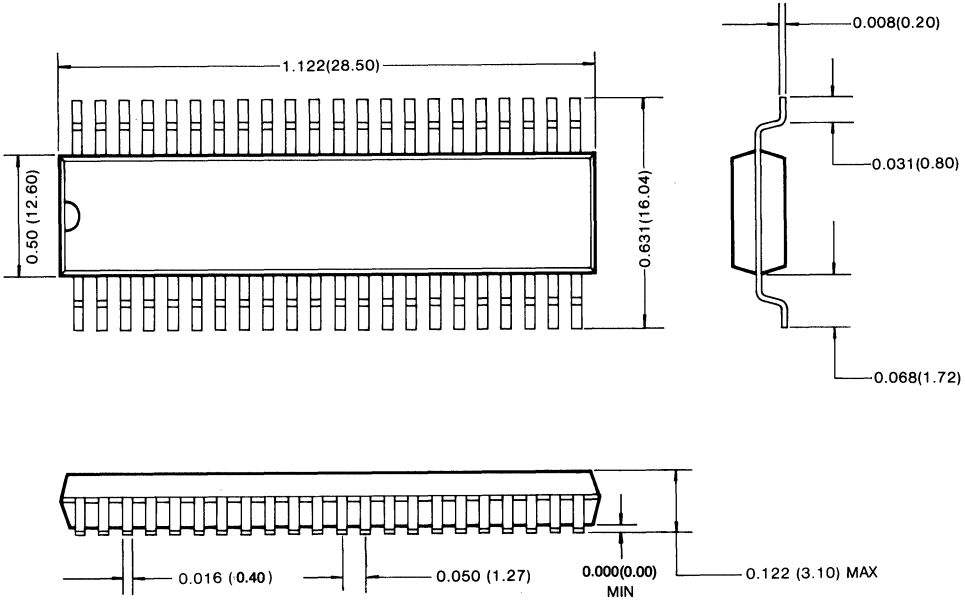
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8100A)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C8100AG)



8M-Bit (1M X 8/512K X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 x 8 (byte mode)
  524,288 x 16 (word mode)
- **Fast access time: 100ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8100B is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576X8 bit (byte mode) or as 524,288X16 bit (word mode) depending on BHE voltage level. (See mode selection table).

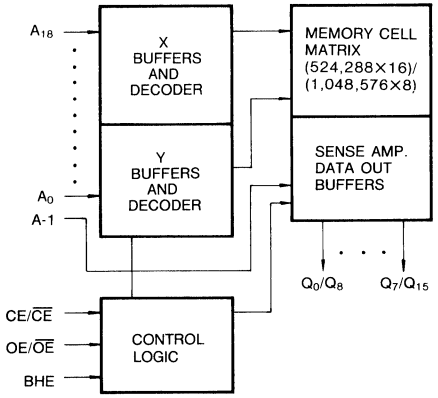
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8100B is packaged in a 42-DIP and the KM23C8100BG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

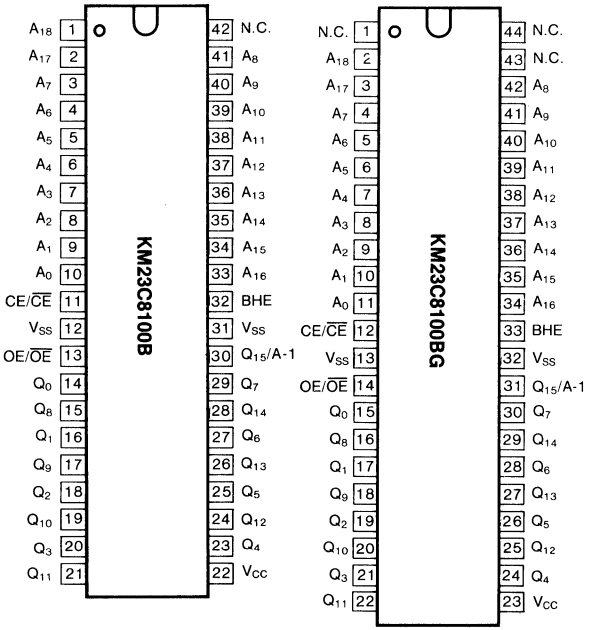
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

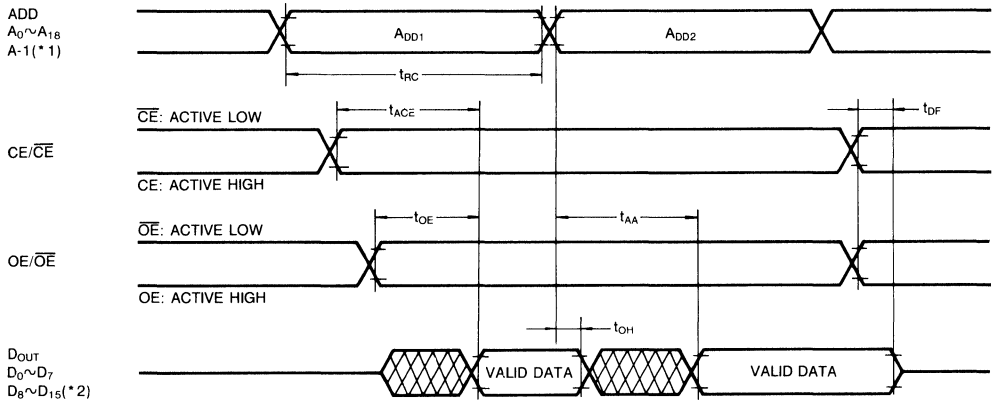
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C8100B(G)-10		KM23C8100B(G)-12		KM23C8100B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

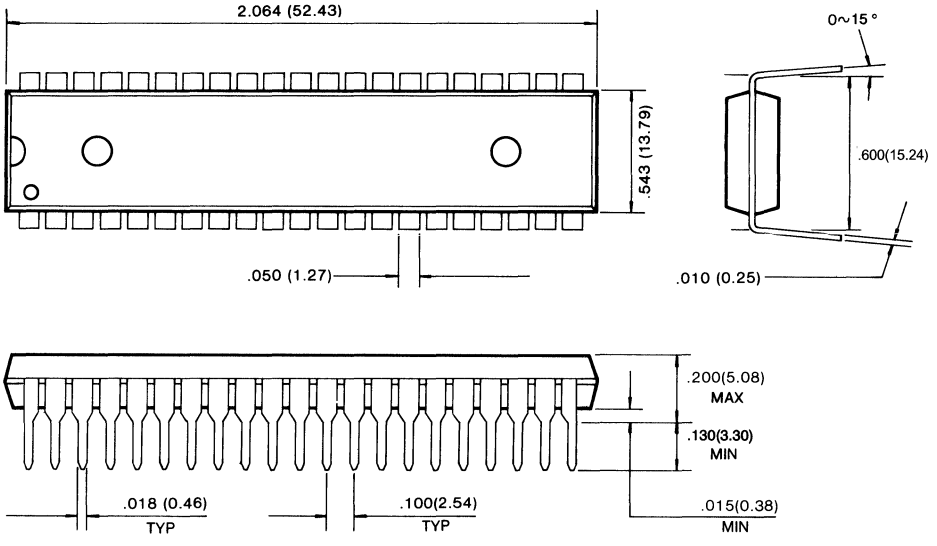


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

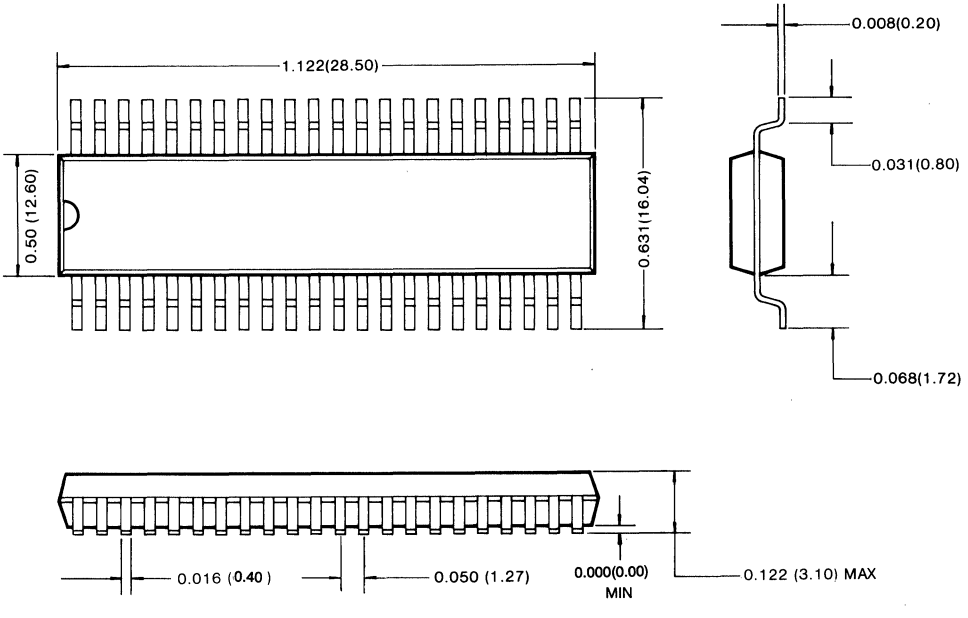
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8100B)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C8100BG)



8M-Bit (1M x 8/512K x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576 x 8 (byte mode)
  524,288 x 16 (word mode)
- **Fast access time**
  Random access: 100ns (max.)
  Page access: 50ns (max.)
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 80 mA(max.)
  Standby: 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)**
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C8105B is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576 x 8 bit (byte mode) or as 524,288 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table)

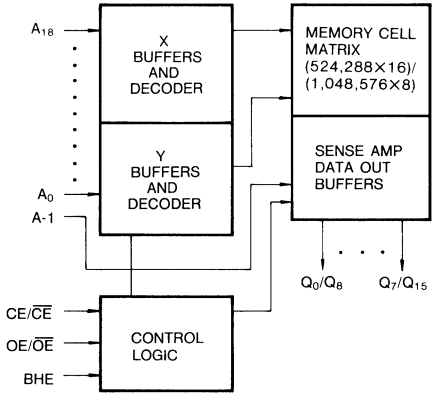
This device is includes PAGE read mode function, page read mode allows two to four words of data to be read fast in the same page, CE and A_2-A_{18} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C8105B is packaged in a 42-DIP and the KM23C8105BG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

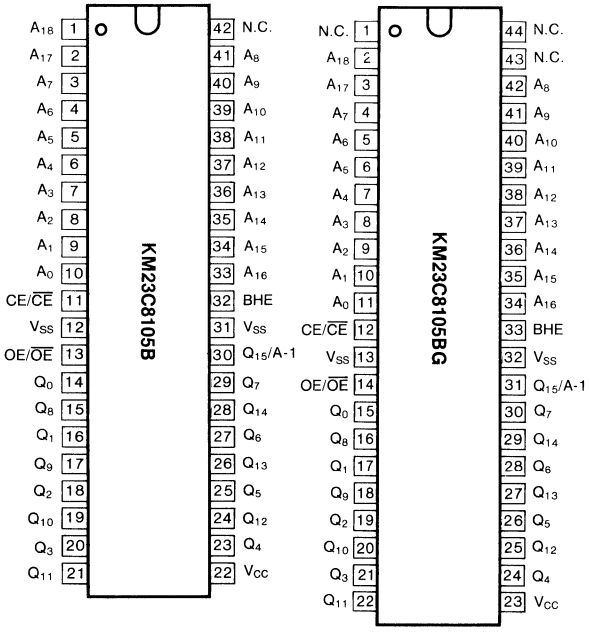
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_1	Page Address Inputs
A_2-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 6.7MHz all output open	—	80	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

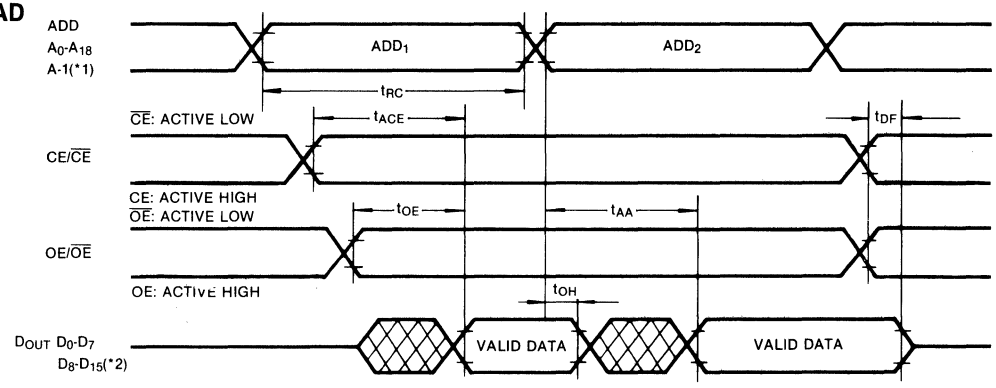
READ CYCLE

Parameter	Symbol	KM23C8105B(G)-10		KM23C8105B(G)-12		KM23C8105B(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Chip Enable Access Time	t_{ACE}		100		120		150	ns
Address Access Time	t_{AA}		100		120		150	ns
Page Address Access Time	t_{PA}		50		60		70	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20		30	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

* Page Address: A_0, A_1

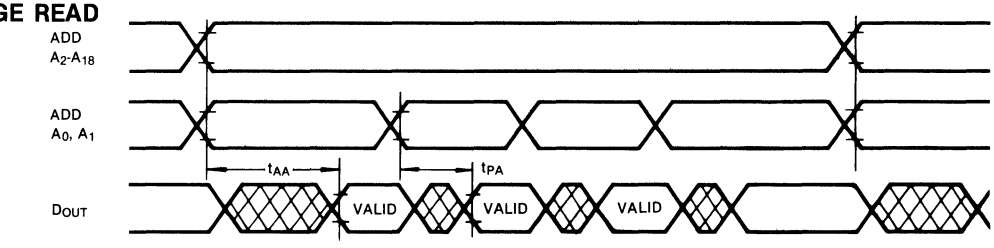
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

PAGE READ

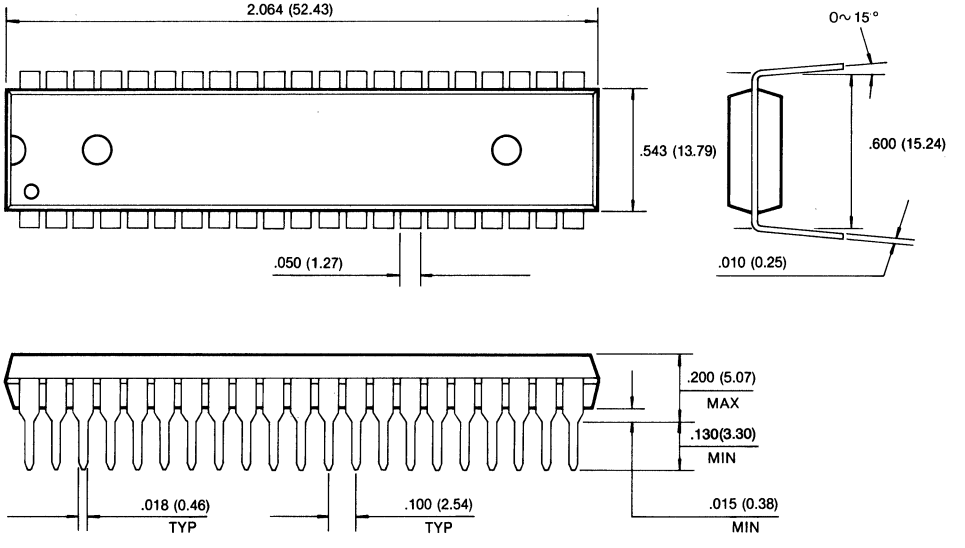


SAMSUNG ELECTRONICS

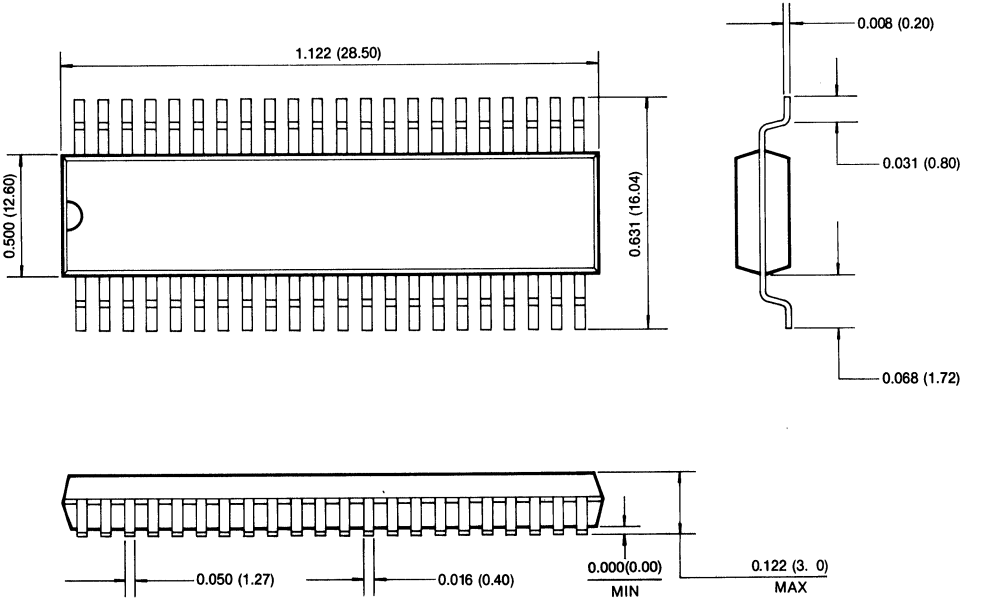
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C8105B)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C8105BG)



8M-Bit (1M×8/512K×16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  1,048,576×8(byte mode)
  524,288×16(word mode)
- **Fast access time : 150ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 42-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  44-pin, 600mil, plastic SOP

GENERAL DESCRIPTION

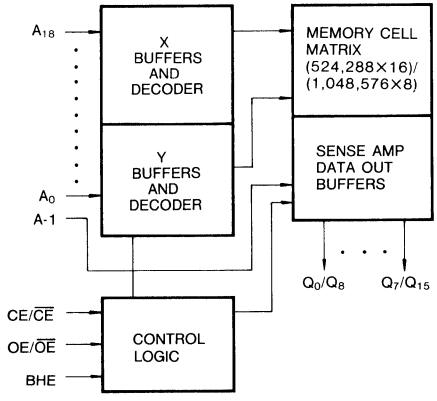
The KM23V8100B is a fully static mask programmable ROM fabricated using silicon-gate CMOS process technology, and is a organized either as 1,048,576×8 bit (byte mode)or as 524,288×16 bit(word mode)depending on BHE voltage level.(See mode selection table).

This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V8100B is packaged in a 42-DIP, and the KM23V8100BG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

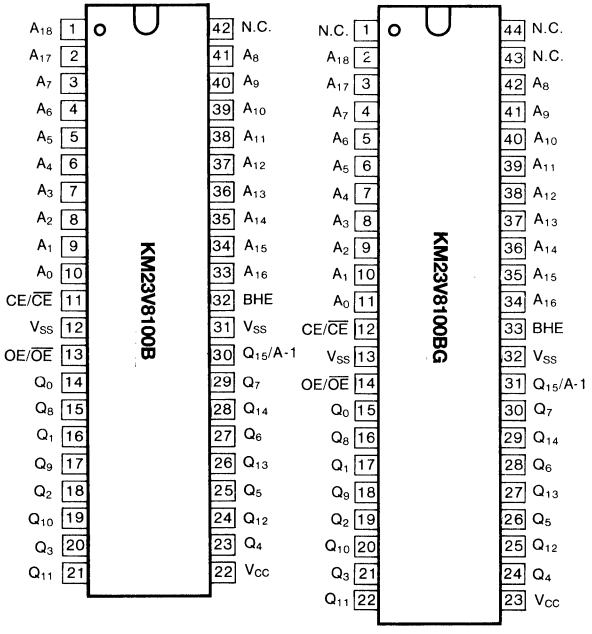
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7 : D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

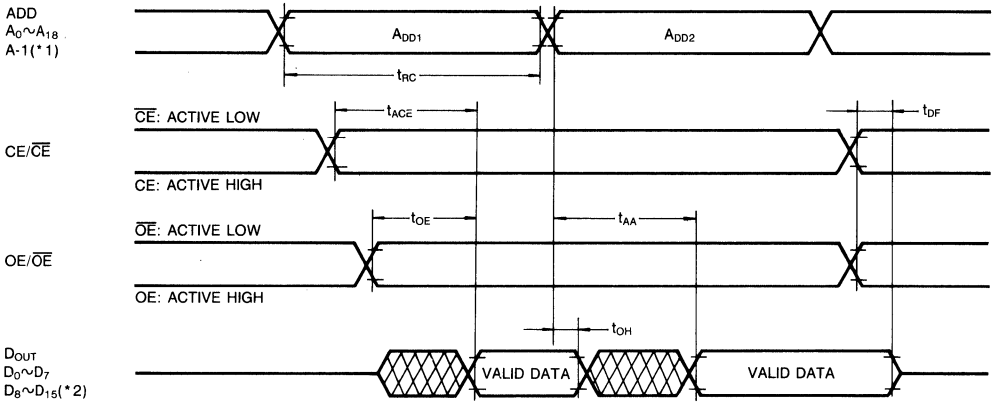
Parameter	Symbol	KM23V8100B(G)-20		KM23V8100B(G)-25		KM23V8100B(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V8100B(G)-15		KM23V8100B(G)-20		KM23V8100B(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

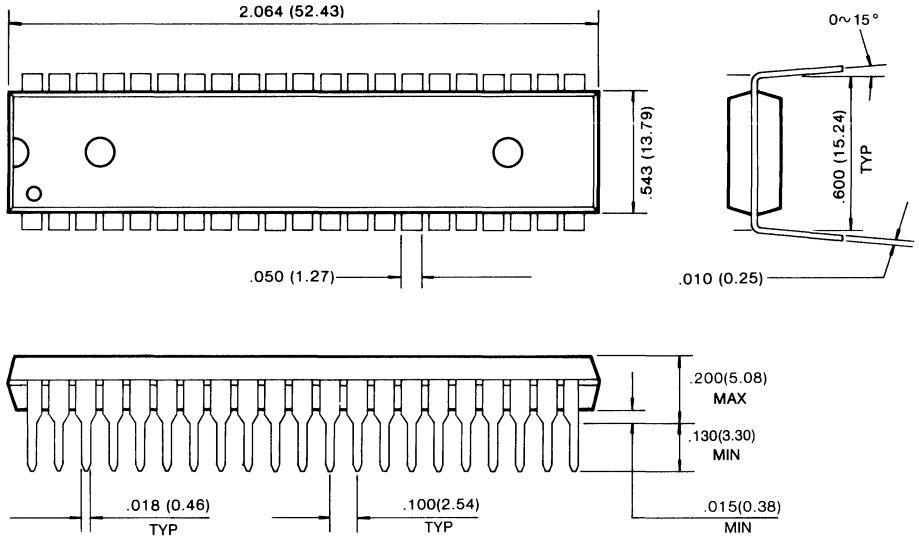


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

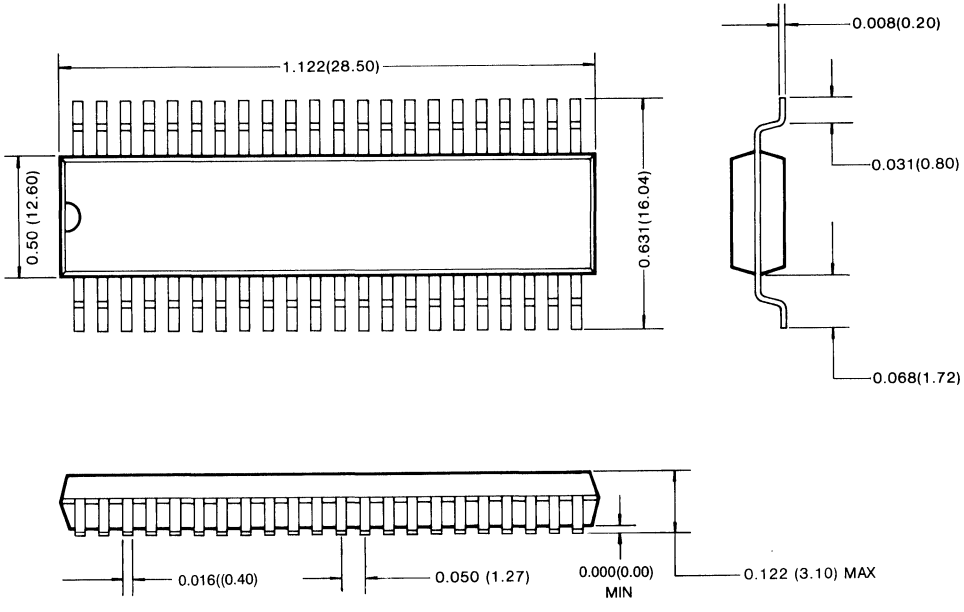
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V8100B)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23V8100BG)



16M-Bit (2M x 8) CMOS MASK ROM

FEATURES

- 2,097,152 x 8 bit organization
- Fast access time: 120ns(max).
- Supply voltage: single + 5V
- Current consumption
  Operating: 60mA (max.)
  Standby: 50μA (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package: 36-pin, 600 mil, plastic DIP
  (JEDEC standard)

GENERAL DESCRIPTION

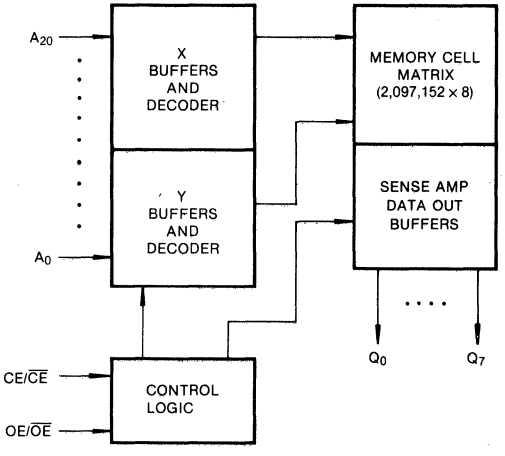
The KM23C16100A is a fully static mask programmable ROM organized 2,097,152 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

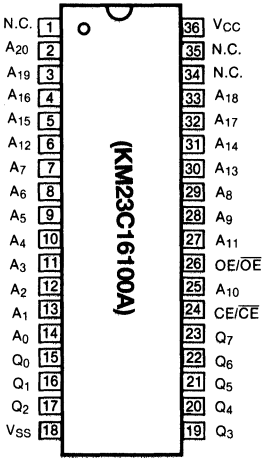
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16100A is packaged in a 36-DIP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_7	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

3

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}	—	2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}	—	−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

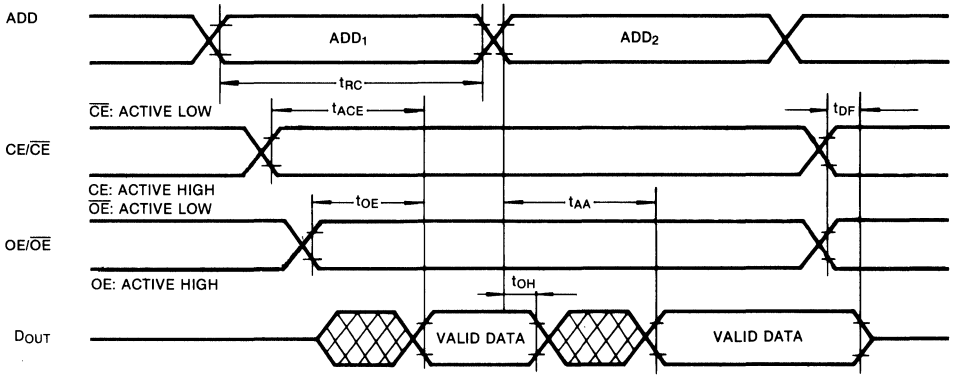
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C16100A-12		KM23C16100A-15		KM23C16100A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

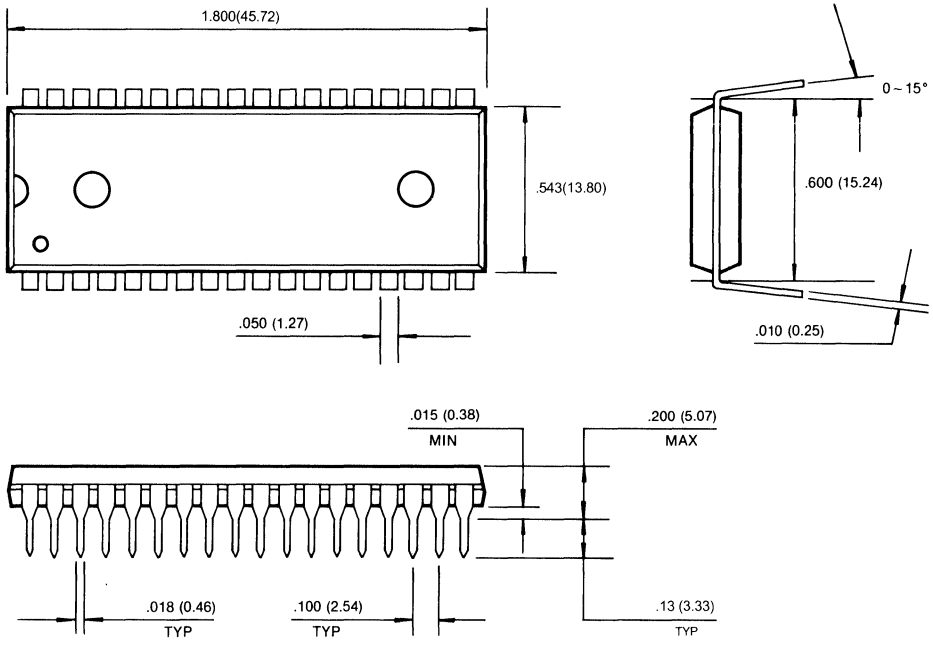
READ



PACKAGE DIMENSIONS

36 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16100A)

Unit: Inches (millimeters)



16M-Bit (2M ×8) CMOS MASK ROM

FEATURES

- **2,097,152×8 bit organization**
- **Fast access time : 200ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 36-pin, 600mil, plastic DIP**
  (JEDEC Standard)

GENERAL DESCRIPTION

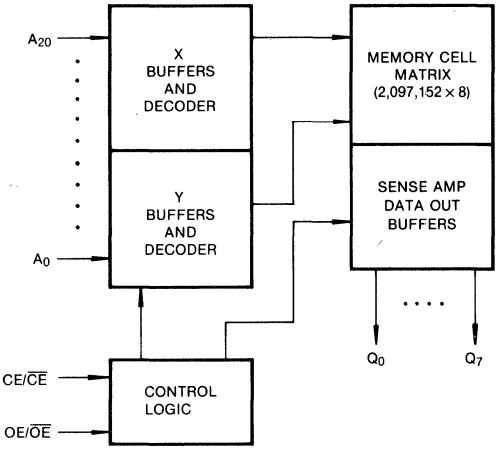
The KM23V16100A is a fully static mask programmable ROM organized 2,097,152 × 8 bit. It is fabricated using silicon-gate CMOS process technology.

This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

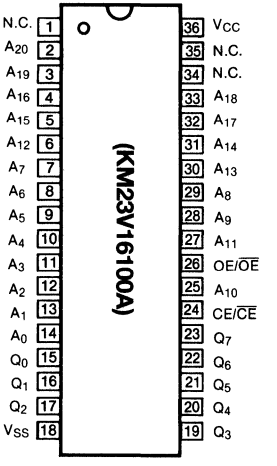
It is suitable for use In program memory of microprocessor, and data memory, character generator.

The KM23V16100A is packaged in a 36-DIP, provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V± 0.3)

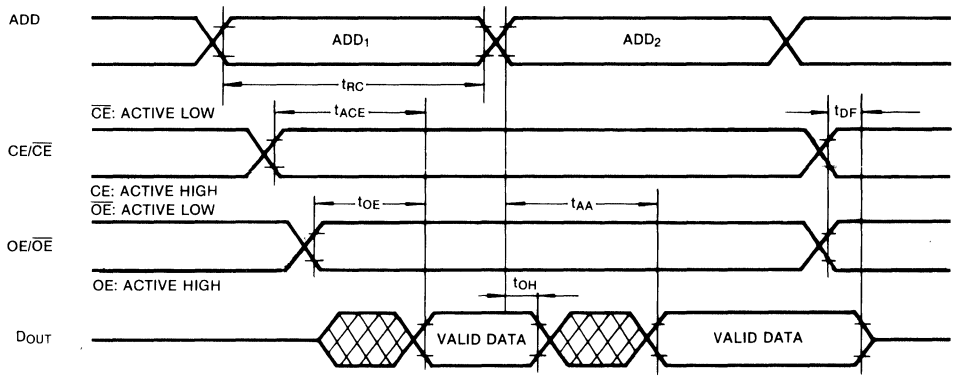
Parameter	Symbol	KM23V16100A-25		KM23V16100A-30		KM23V16100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		300		350		ns
Chip Enable Access Time	t_{ACE}		250		300		350	ns
Address Access Time	t_{AA}		250		300		350	ns
Output Enable Access Time	t_{OE}		110		130		150	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V16100A-20		KM23V16100A-25		KM23V16100A-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

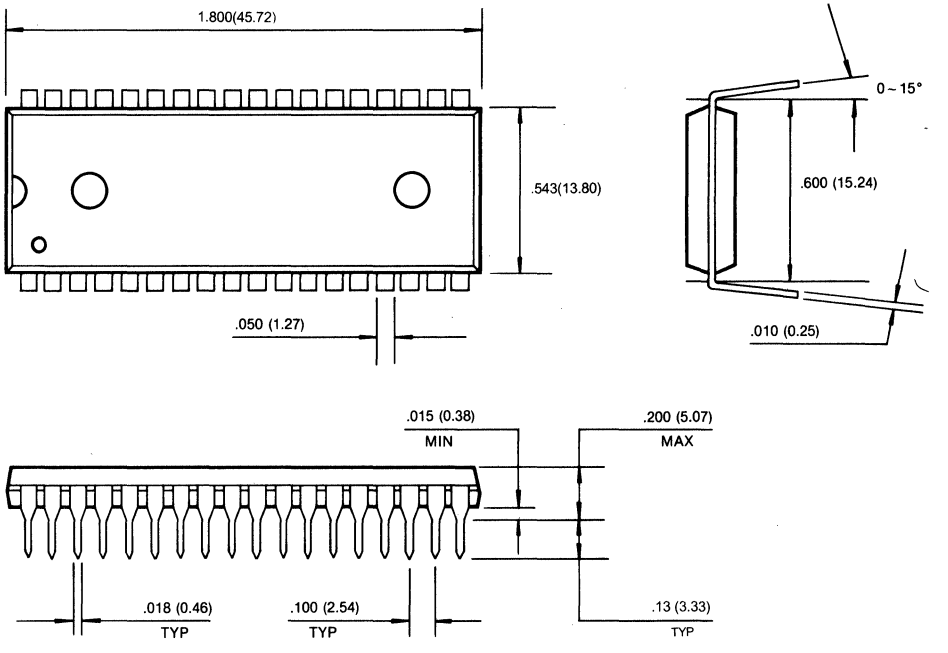
READ



PACKAGE DIMENSIONS

36 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V16100A)

Unit: Inches (millimeters)



16M-Bit (2M x 8) CMOS MASK ROM

FEATURES

- **2,097,152 x 8 bit organization**
- **Fast access time: 120ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 60mA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 36-pin, 600 mil, plastic DIP**
  (JEDEC standard)

GENERAL DESCRIPTION

The KM23C16101A is a fully static mask programmable ROM organized 2,097,152 x 8 bit. It is fabricated using silicon-gate CMOS process technology.

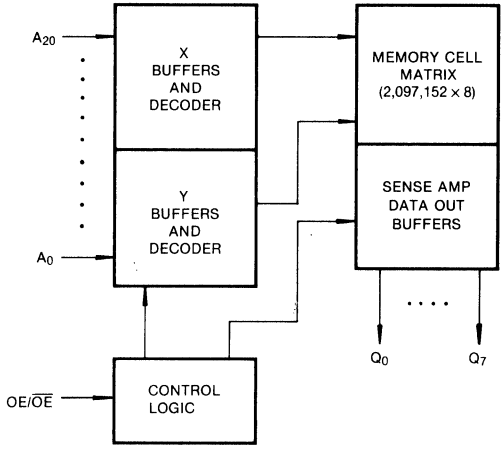
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

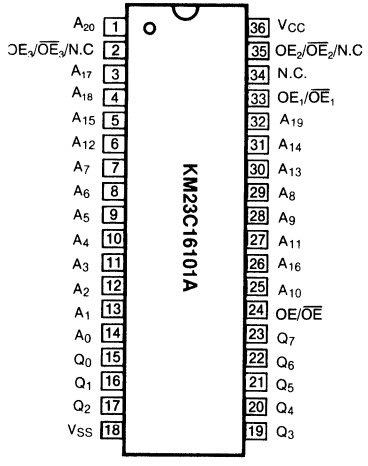
The KM23C16101A is packaged in a 36-DIP, provides polarity programmable OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

* User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}	—	2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}	—	−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/OE	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

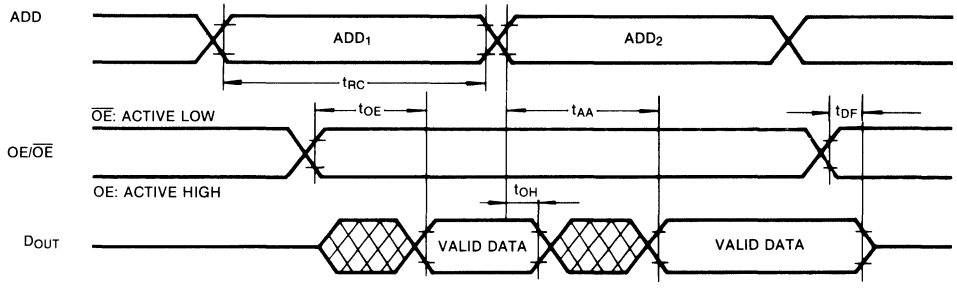
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM23C16101A-12		KM23C16101A-15		KM23C16101A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

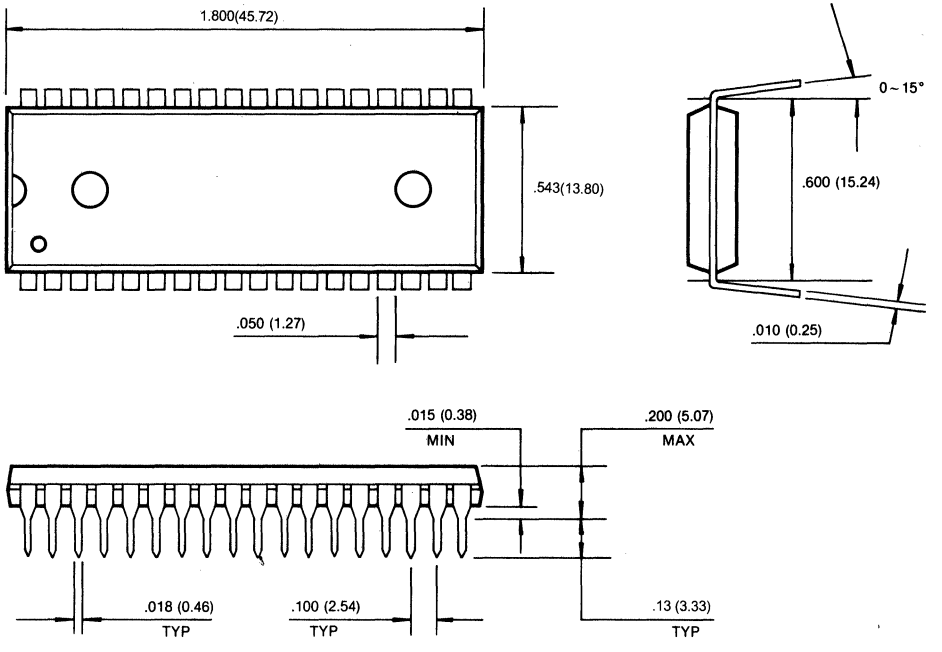


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

36 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16101A)

Unit: Inches (millimeters)



SAMSUNG ELECTRONICS

16M-Bit (2M ×8) CMOS MASK ROM

FEATURES

- **2,097,152×8 bit organization**
- **Fast access time : 200ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V± 0.3
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 36-pin, 600mil, plastic DIP**
  (JEDEC Standard)

GENERAL DESCRIPTION

The KM23V16101A is a fully static mask programmable ROM organized 2,097,152×8 bit. It is fabricated using silicon-gate CMOS process technology.

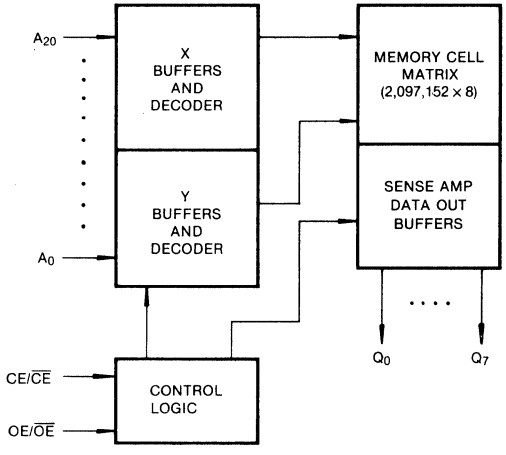
This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

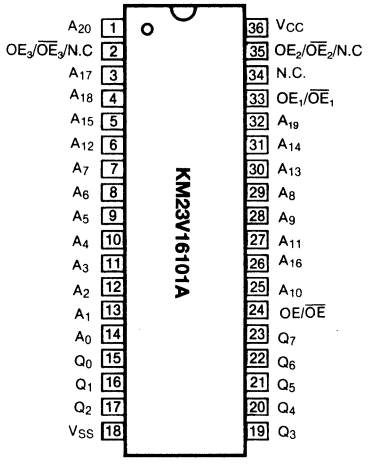
The KM23V16101A is packaged in a 36-DIP, provides polarity programmable OE buffer as user option mode.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_7	Data Outputs
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(+3V or +3.3V)
V_{SS}	Ground

*User Selectable Polarity

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			- 0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

OE/OE	Mode	Data	Power
L/H	Operating	High-Z	Active
H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to +70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

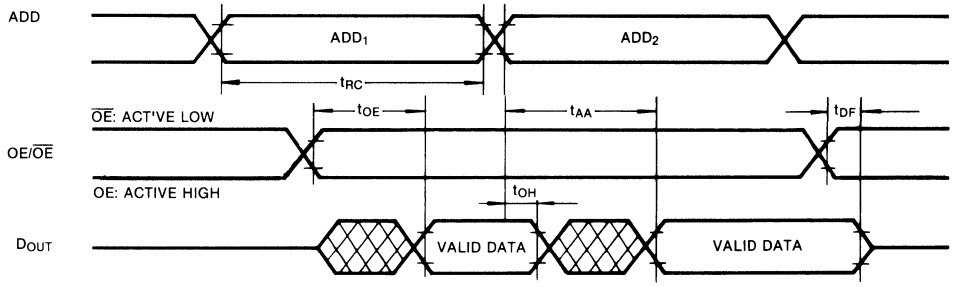
Parameter	Symbol	KM23V16101A-25		KM23V16101A-30		KM23V16101A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		300		350		ns
Address Access Time	t_{AA}		250		300		350	ns
Output Enable Access Time	t_{OE}		110		130		150	ns
Output Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V16101A-20		KM23V16101A-25		KM23V16101A-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

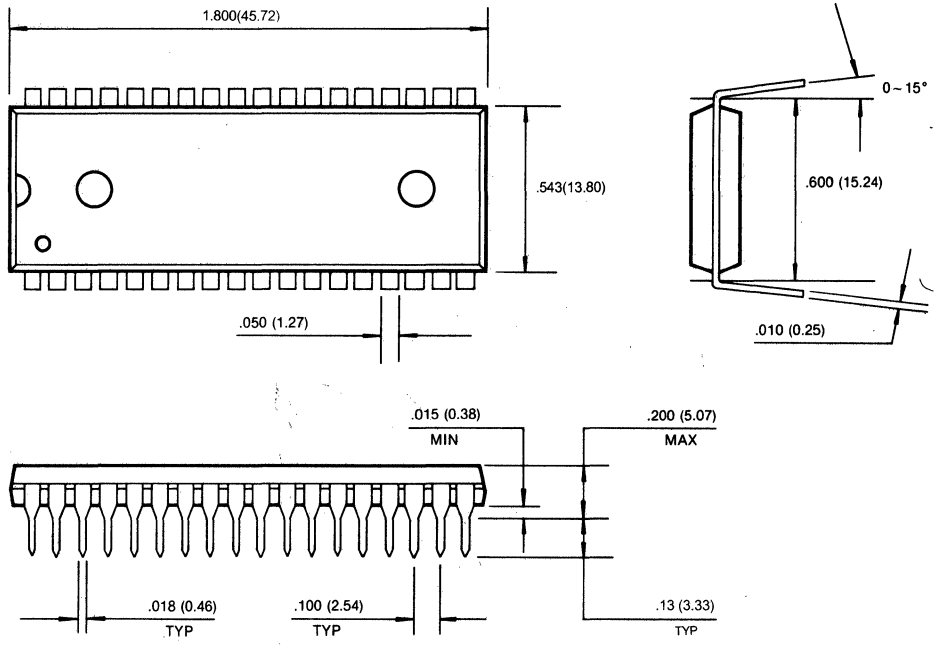
READ



PACKAGE DIMENSIONS

36 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V16101A)

Unit: Inches (millimeters)



16M-Bit (2M X 8/1M X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 x 8 (byte mode)
  1,048,576 x 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating: 50mA (max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

The KM23C16000 is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organization either as 2,097,152X8 bit (byte mode) or as 1,048,576X16 bit (word mode) depending on BHE voltage level. (See mode selection table).

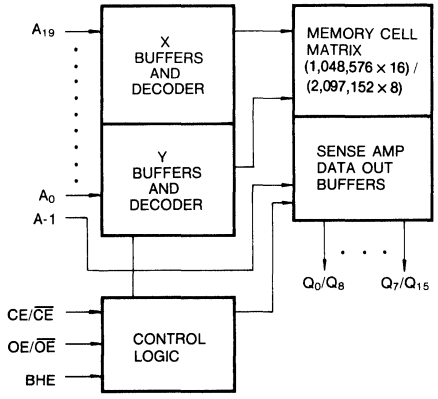
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16000 is packaged in a 42-DIP, and the KM23C16000G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

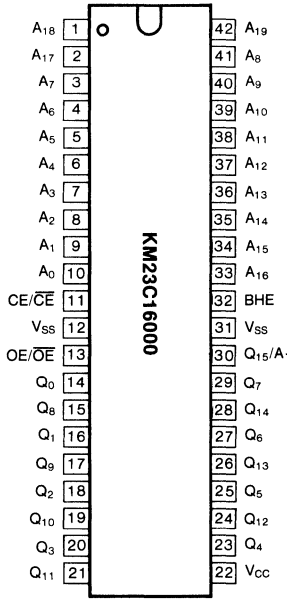
FUNCTIONAL BLOCK DIAGRAM

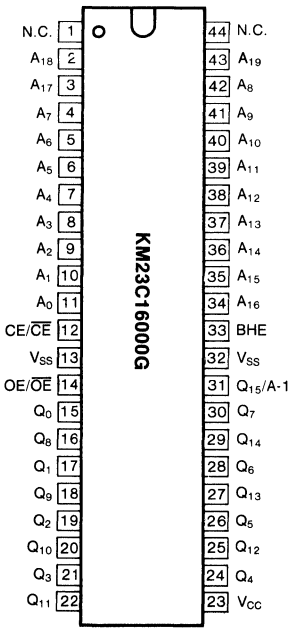


Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	50	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}= −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	10.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

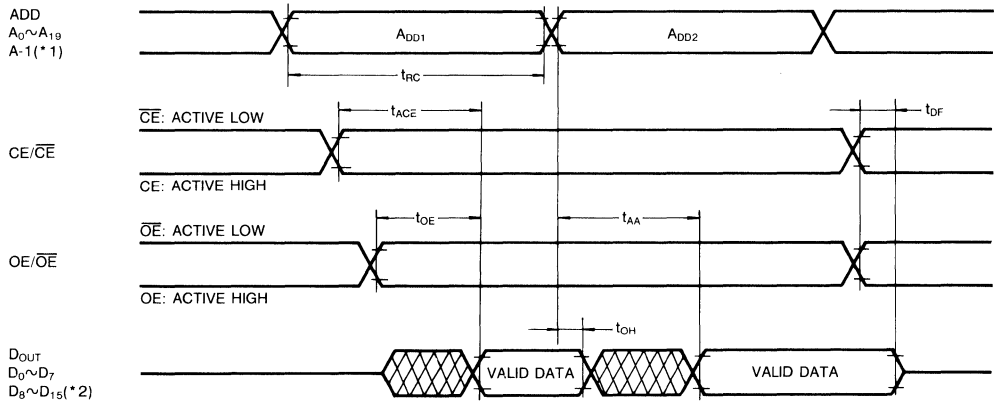
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM23C16000(G)-15		KM23C16000(G)-20		KM23C16000(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



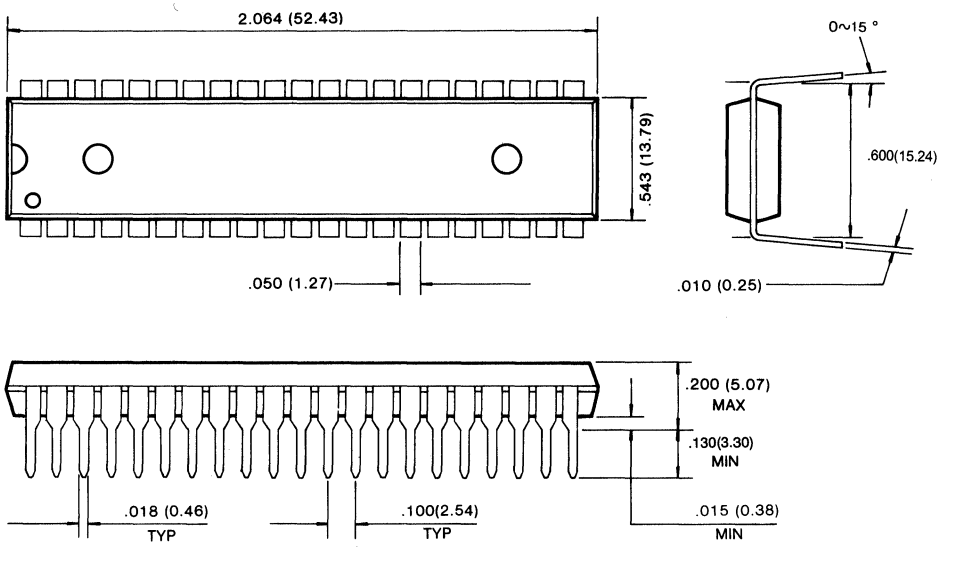
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

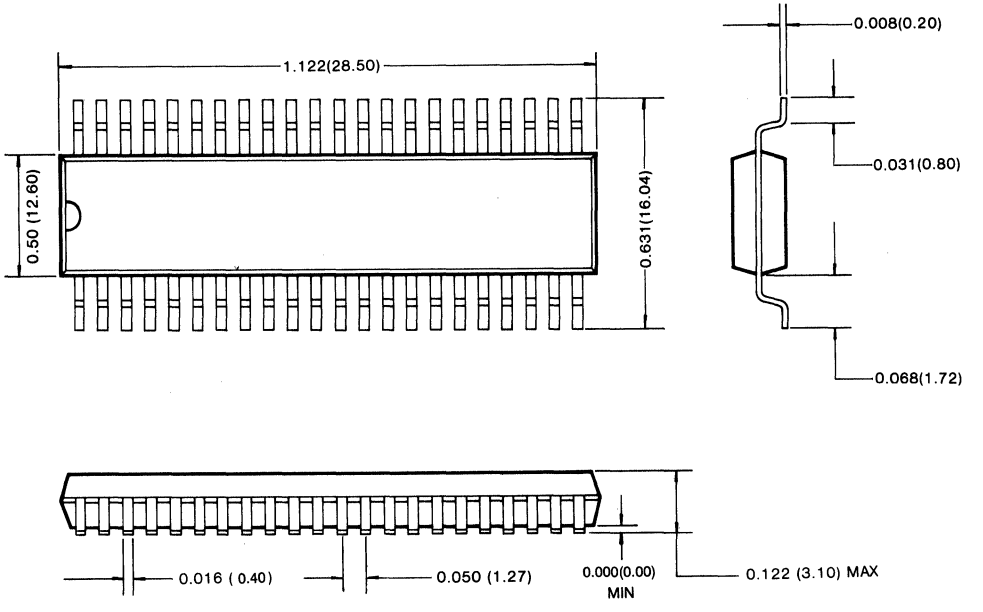
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16000)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C16000G)



16M-Bit (2M X 8/1M X 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 x 8 (byte mode)
  1,048,576 x 16 (word mode)
- **Fast access time: 120ns (max.)**
- **Supply voltage: single + 5V**
- **Current consumption**
  Operating : 60 mA(max.)
  Standby : 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

GENERAL DESCRIPTION

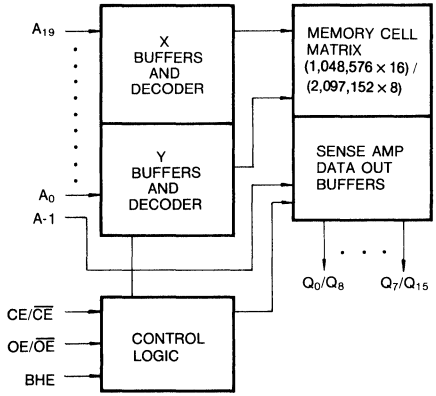
The KM23C16000A is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organization either as 2,097,152X8 bit (byte mode) or as 1,048,576X16 bit (word mode) depending on BHE voltage level. (See mode selection table).

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16000A is packaged in a 42-DIP, and the KM23C16000AG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

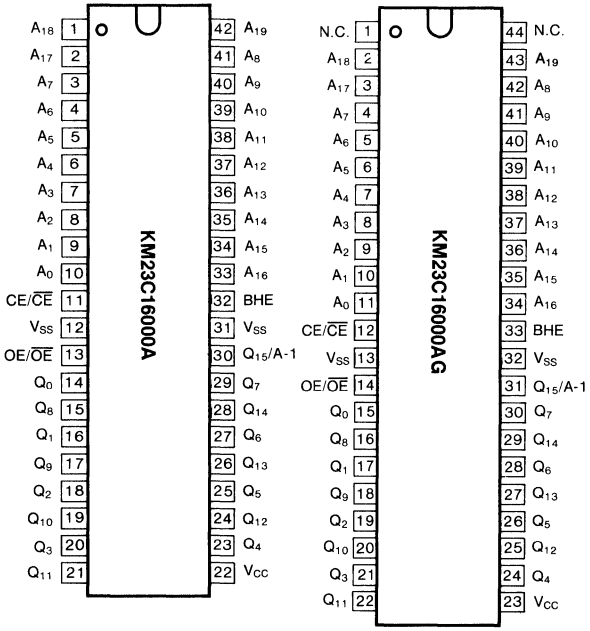
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, f=6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=−400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA	—	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

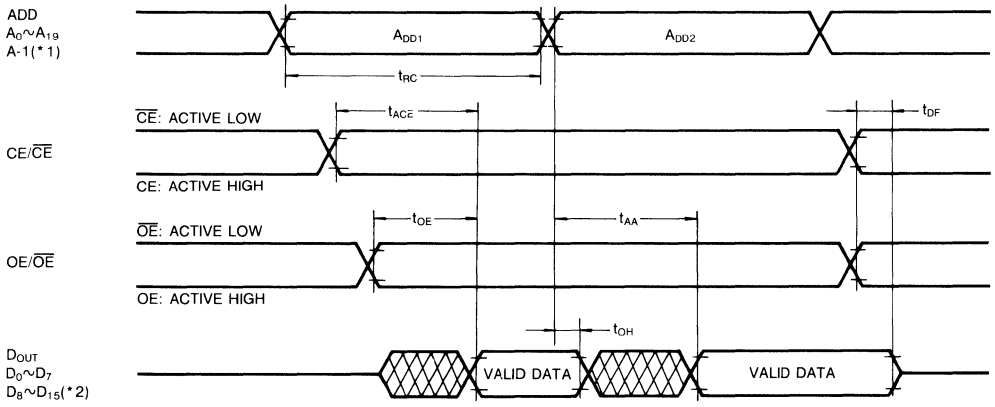
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C16000A(G)-12		KM23C16000A(G)-15		KM23C16000A(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Output Enable Access Time	t_{OE}		60		70		90	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ

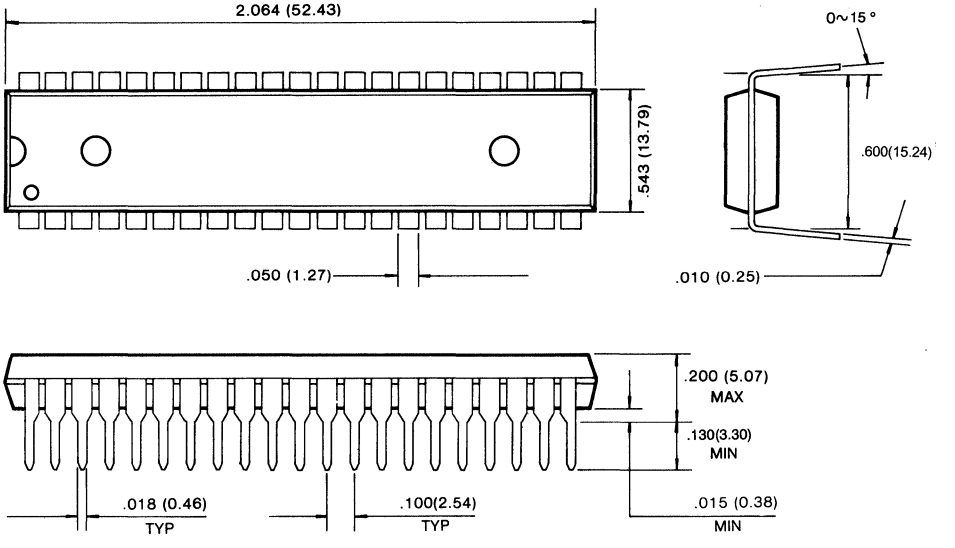


(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

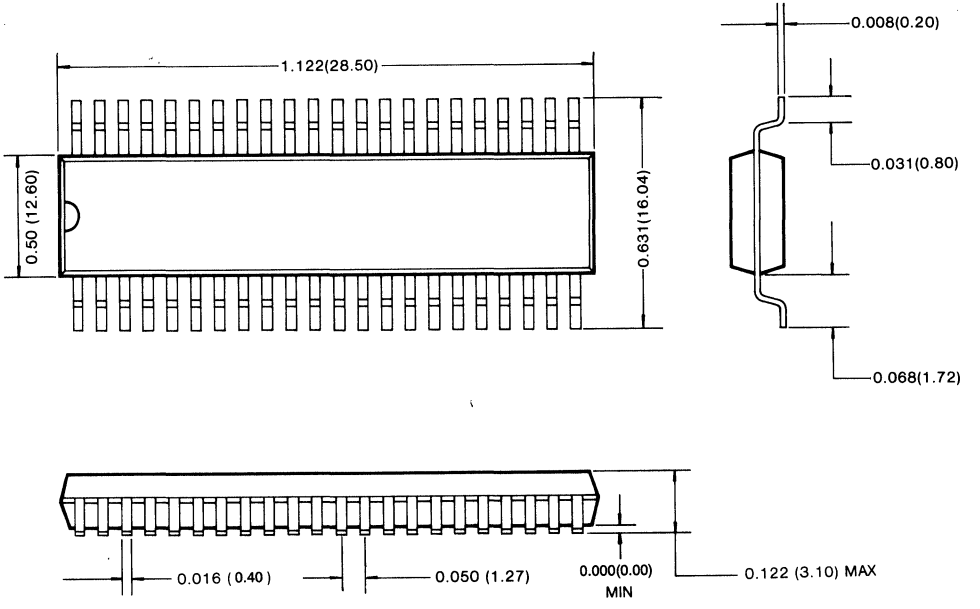
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16000A)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C16000AG)

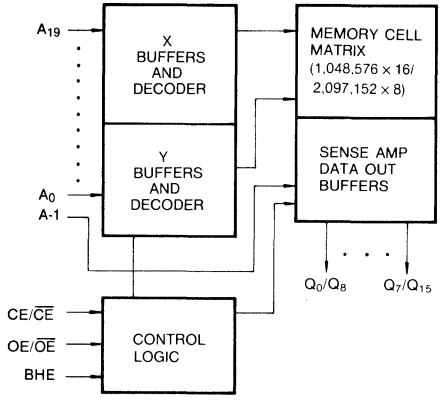


16M-Bit (2M x 8/1M x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152 x 8 (byte mode)
  1,048,576 x 16 (word mode)
- **Fast access time**
  Random access: 120ns (max.)
  Page access: 50ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)
  44-pin, 600 mil, plastic SOP

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

GENERAL DESCRIPTION

The KM23C16005A is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152 x 8 bit (byte mode) or as 1,048,576 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table)

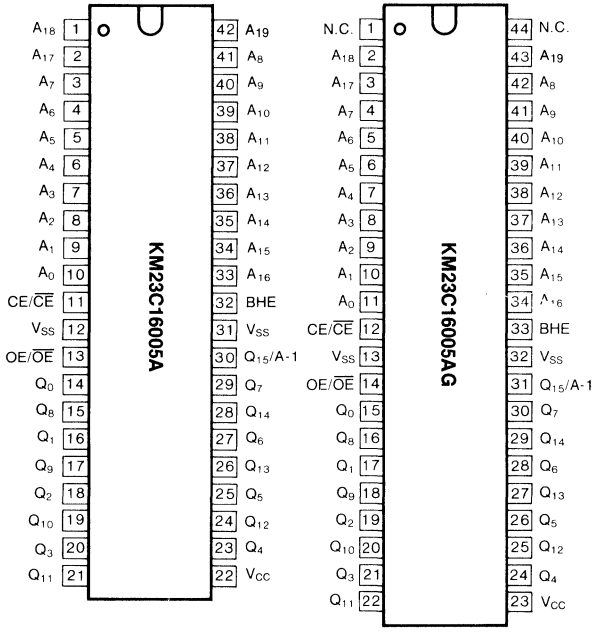
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{19} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C16005A is packaged in a 42-DIP and the KM23C16005AG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	100	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

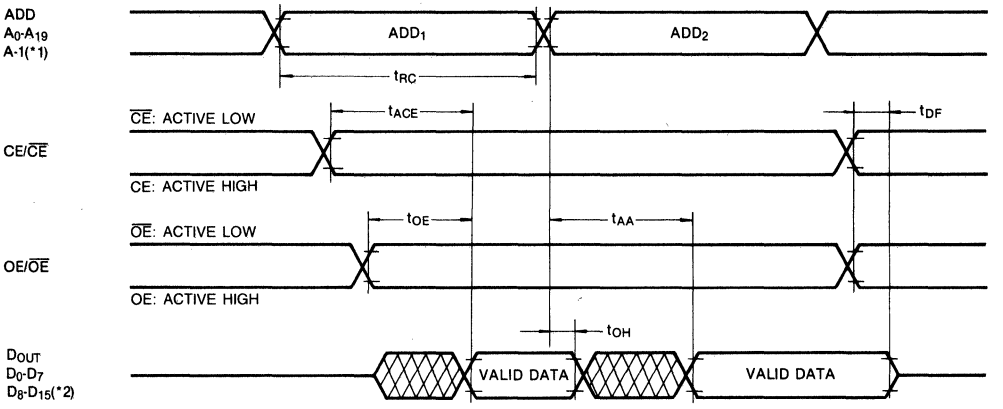
READ CYCLE

Parameter	Symbol	KM23C16005A(G)-12		KM23C16005A(G)-15		KM23C16005A(G)-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Chip Enable Access Time	t_{ACE}		120		150		200	ns
Address Access Time	t_{AA}		120		150		200	ns
Page Address Access Time	t_{PA}		50		60		70	ns
Output Enable Access Time	t_{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		30		40	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

* Page Address: A_0, A_1, A_2

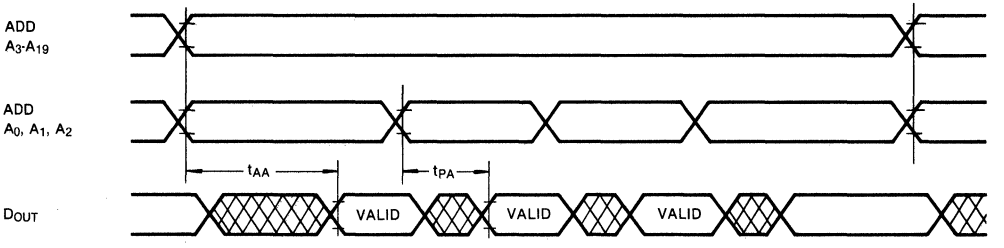
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

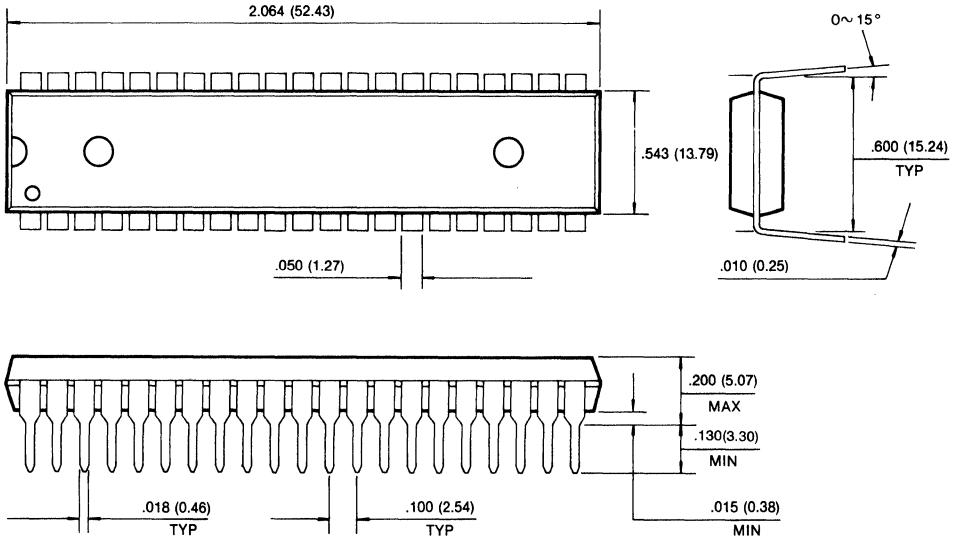
PAGE READ



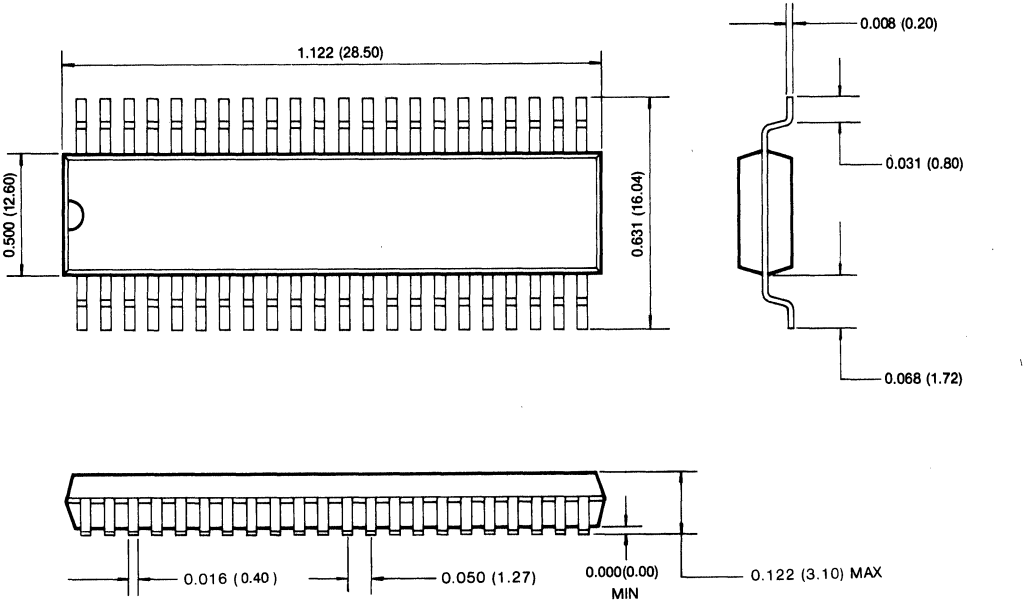
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C16005A)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23C16005AG)



16M-Bit (2M ×8/1M × 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  2,097,152×8(byte mode)
  1,048,578×16(word mode)
- **Fast access time : 200ns(max.)**
- **Supply voltage : single+3V or +3.3V**
- **Current consumption**
  Operating : 25 mA(max.) at V_{CC}=3.0V± 0.3
  30 mA(max.) at V_{CC}=3.3V±0.3
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package : 42-pin, 600mil, plastic DIP**
  (JEDEC Standard)
  44-pin, 600mil, plastic SOP

GENERAL DESCRIPTION

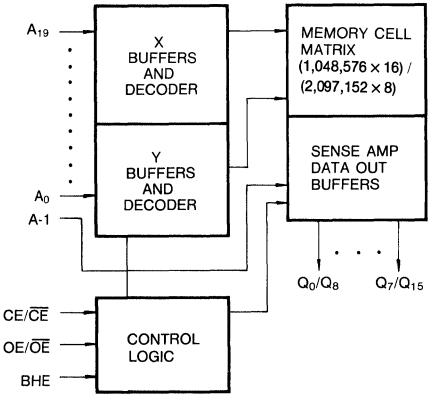
The KM23V16000A is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology and is a organized either as 2,097,152×8 bit (byte mode)or as 1,048,576×16 bit(word mode) depending on BHE voltage level.(See mode selection table).

This device operates with a 3V or 3.3V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V16000A is packaged in a 42-DIP, and the KM23V16000AG in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

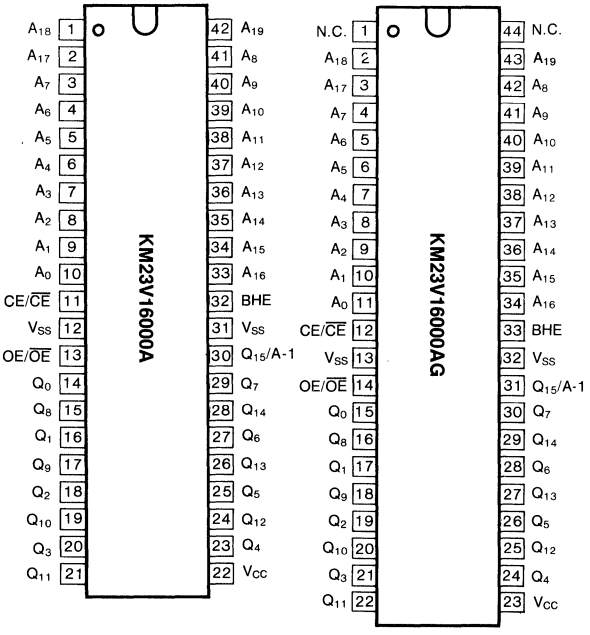
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power(3V or 3.3V)
V_{SS}	Ground
N.C	No Connection

*User Selectable Polarity

PIN CONFIGURATION



MODE SELECTION

CE/CE	OE/OE	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7 : D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0℃ to + 70℃, V_{CC}=3V±0.3/V_{CC}=3.3V±0.3, unless otherwise noted.)

Item	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE (V_{CC}=3.0V±0.3)

Parameter	Symbol	KM23V16000A(G)-25		KM23V16000A(G)-30		KM23V16000A(G)-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		300		350		ns
Chip Enable Access Time	t_{ACE}		250		300		350	ns
Address Access Time	t_{AA}		250		300		350	ns
Output Enable Access Time	t_{OE}		110		130		150	ns
Output or Chip Disable to Output High-Z	t_{DF}		50		60		70	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

READ CYCLE (V_{CC}=3.3V±0.3)

Parameter	Symbol	KM23V16000A(G)-20		KM23V16000A(G)-25		KM23V16000A(G)-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		300		ns
Chip Enable Access Time	t_{ACE}		200		250		300	ns
Address Access Time	t_{AA}		200		250		300	ns
Output Enable Access Time	t_{OE}		90		110		130	ns
Output or Chip Disable to Output High-Z	t_{DF}		40		50		60	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to + 4.5	V
Temperature Under Bias	T_{bias}	-10 to + 85	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0/3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}(V_{CC}=3.0V±0.3)	CE=OE=V_{IL}	f=5.0MHz	—	25	mA
	I_{CC}(V_{CC}=3.3V±0.3)	all output open	f=5.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	CE=V_{IH}, all output open		—	1	mA
Standby Current (CMOS)	I_{SB2}	CE=V_{CC}, all output open		—	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		—	10	μA
Input High Voltage, All Inputs	V_{IH}			2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}=-400μA		2.4		V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		—	0.4	V

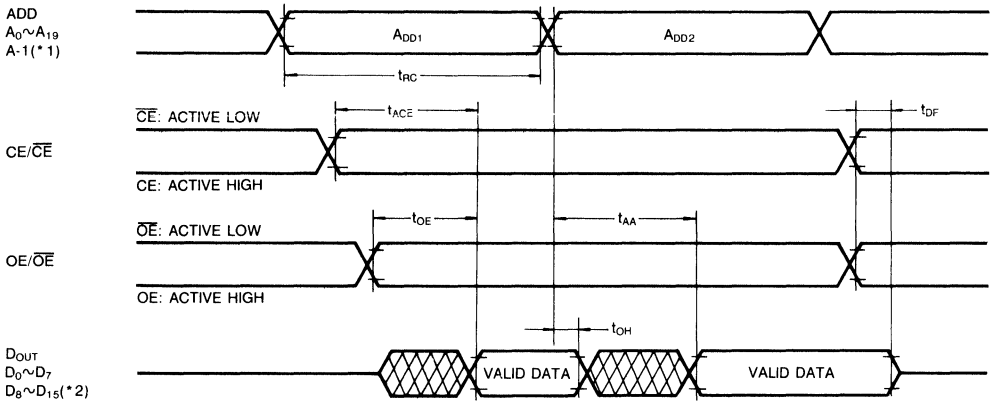
CAPACITANCE (T_A=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN}=0V	—	12.0	pF

Note; Capacitance is periodically sampled and not 100% tested.

TIMING DIAGRAM

READ



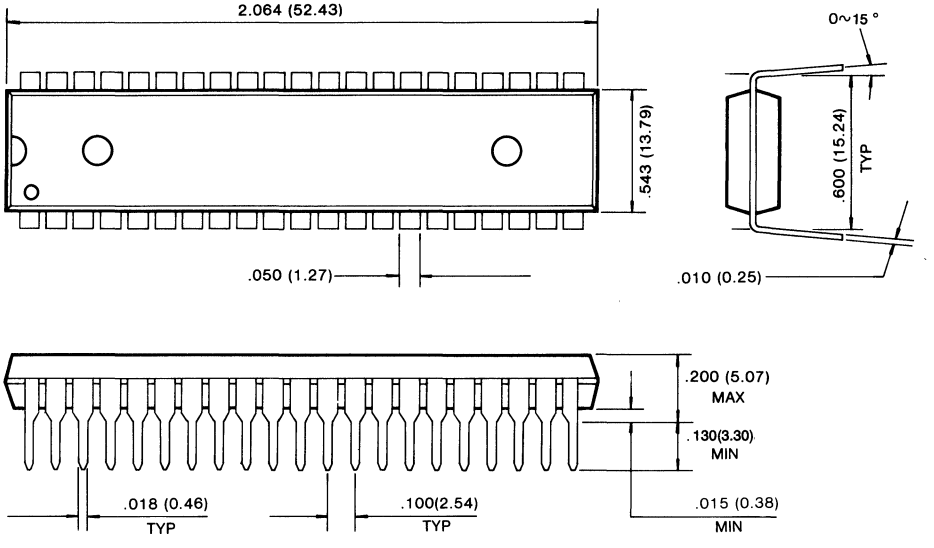
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

3

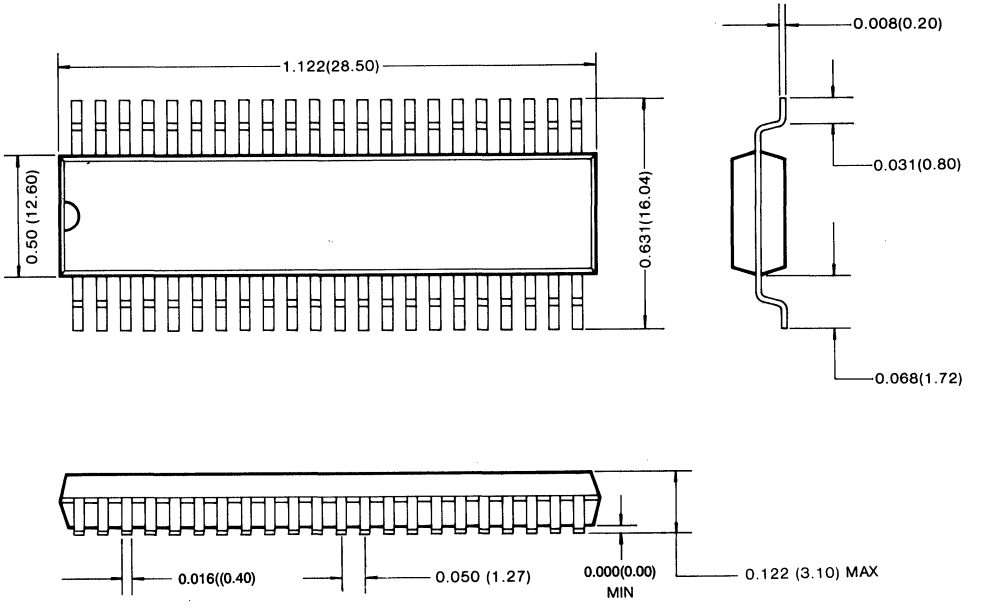
PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23V16000A)

Unit: Inches (mm)



44 LEAD SMALL OUTLINE PACKAGE (KM23V16000AG)



32M-Bit (2M x 16) CMOS MASK ROM

FEATURES

- **2,097,152 x 16 bit organization**
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)

GENERAL DESCRIPTION

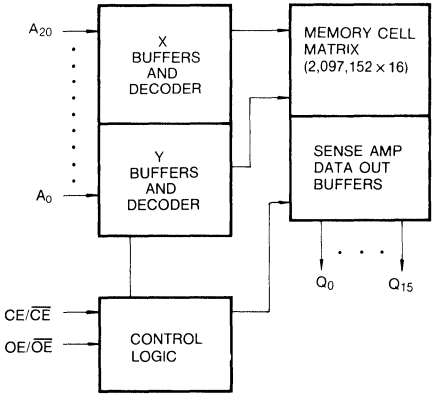
The KM23C32000 is a fully static mask programmable ROM organized 2,097,152 x 16 bit. It is fabricated using silicon gate CMOS process technolgy.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32000 is packaged in a 42-DIP, provides polarity programmable CE and OE buffer as user option mode.

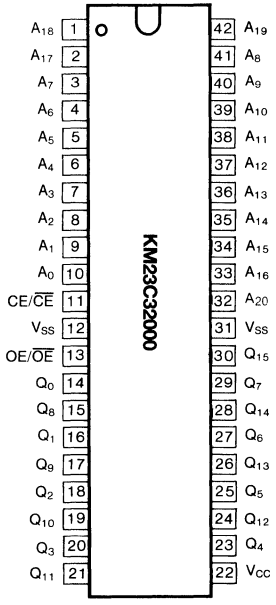
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_{15}	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

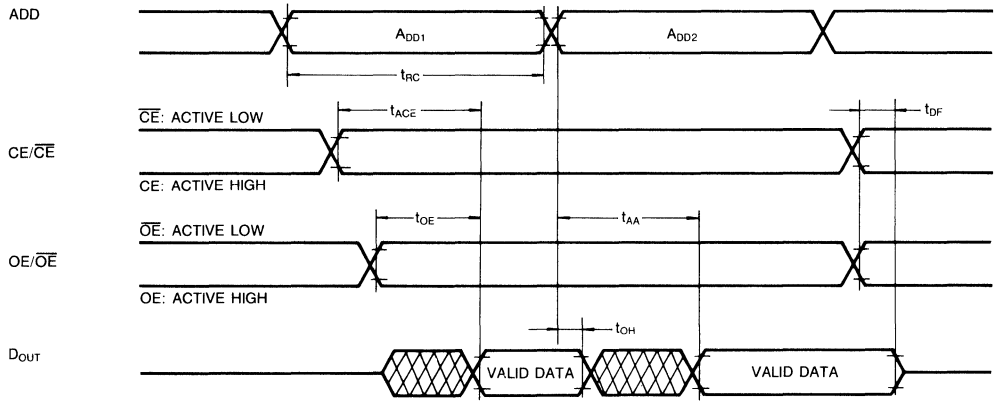
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L = 100pF

READ CYCLE

Parameter	Symbol	KM23C32000(G)-15		KM23C32000(G)-20		KM23C32000(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



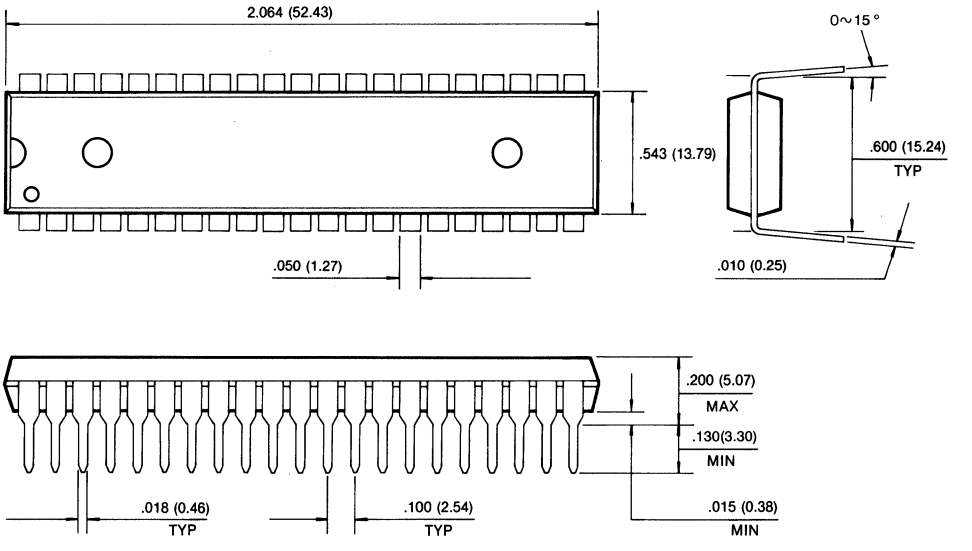
* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns)is required.

SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C32000)

Unit: Inches (mm)



SAMSUNG ELECTRONICS

32M-Bit (4M x 8/2M x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 x 8 (byte mode)
  2,097,152 x 16 (word mode)
- **Fast access time: 150ns (max.)**
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 60mA (max.)
  Standby: 50 μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin, 600 mil, plastic SOP**

GENERAL DESCRIPTION

The KM23C32000G is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organization either as 4,194,304 x 8 bit (byte mode) or as 2,097,152 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

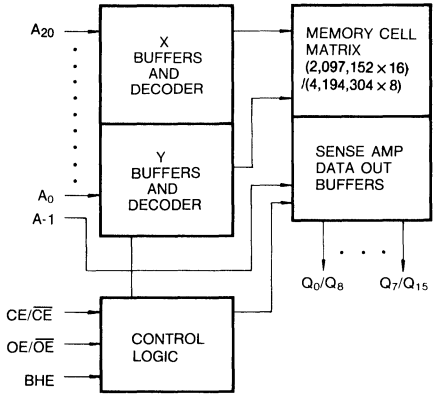
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32000G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

3

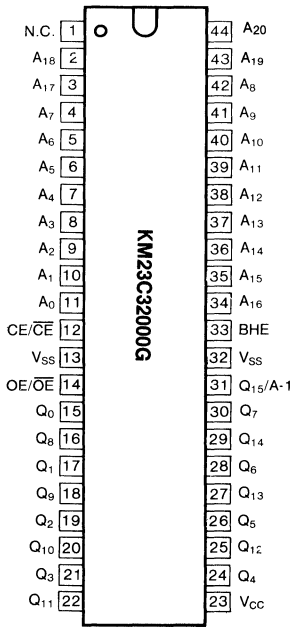
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to + 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
	H/L	H	Output	Operating	Q_0-Q_{15}: Dout	Active
		L	Input	Operating	Q_0-Q_7: Dout Q_8-Q_{14}: High-Z	Active

AC CHARCTERISTICS

(Ta=0° to +70°C, V_{CC}=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

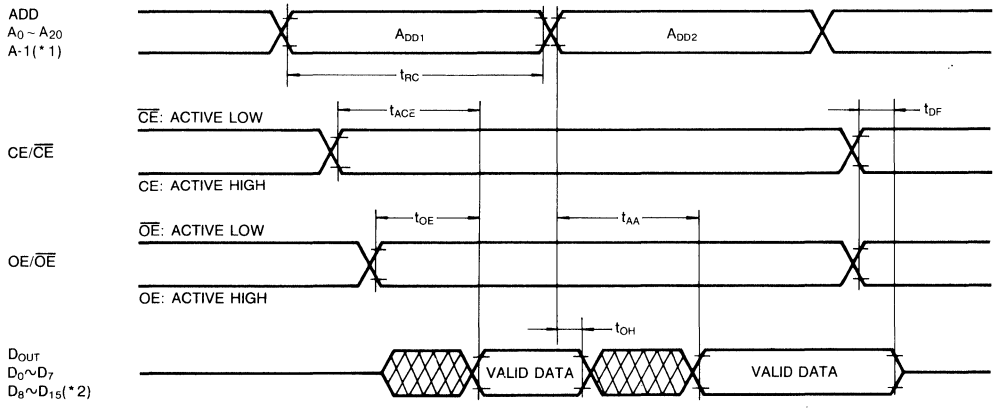
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

READ CYCLE

Parameter	Symbol	KM23C32000G-15		KM23C32000G-20		KM23C32000G-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

TIMING DIAGRAM

READ



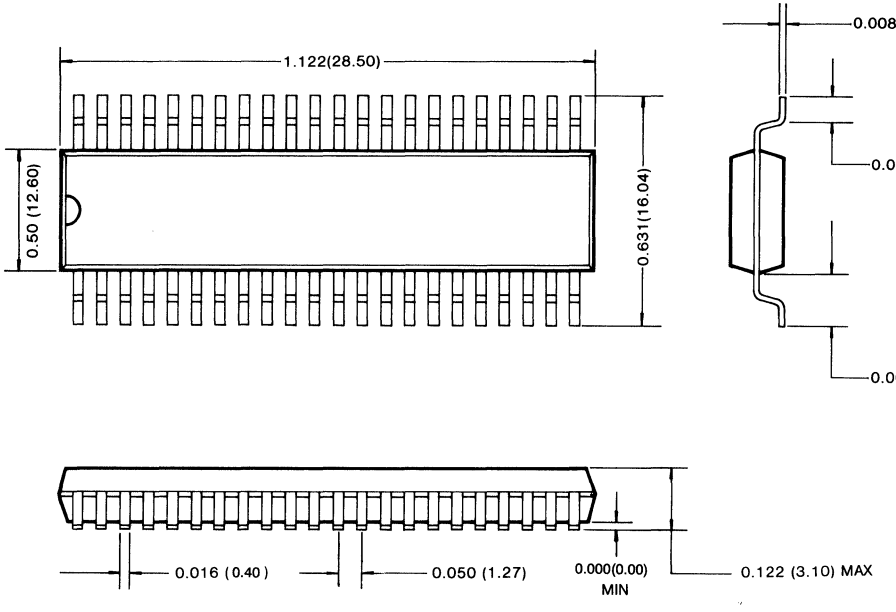
(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

SAMSUNG ELECTRONICS

44 LEAD SMALL OUTLINE PACKAGE (KM23C32000G)

Unit: Inches (mm)



32M-Bit (2M x 16) CMOS MASK ROM

FEATURES

- **2,097,152 x 16 bit organization**
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby: 50μA (max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 42-pin, 600 mil, plastic DIP**
  (JEDEC standard)

GENERAL DESCRIPTION

The KM23C32005 is a fully static mask programmable ROM organized 2,097,152 x 16 bit. It is fabricated using silicon gate CMOS process technology.

This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{20} should not be changed.

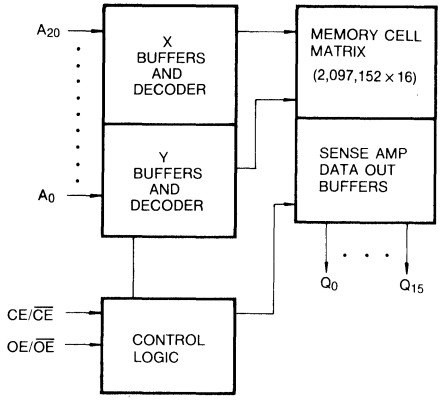
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32005 is packaged in a 42-DIP, provides polarity programmable CE and OE buffer as user option mode.

3

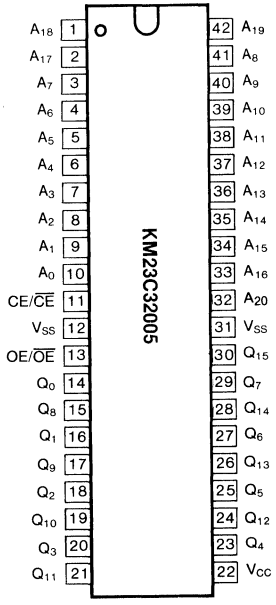
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{20}	Address Inputs
Q_0-Q_{15}	Data Outputs
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 6.7MHz all output open	—	100	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all output open	—	50	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH} = −400μA	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	12.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

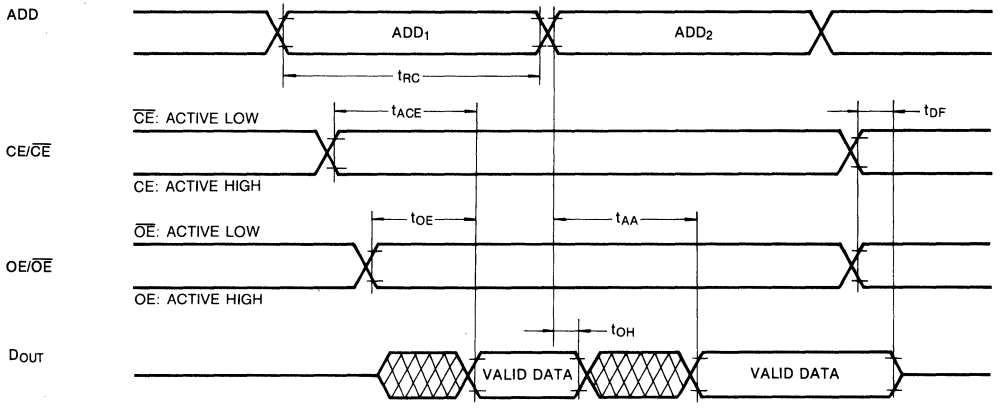
READ CYCLE

Parameter	Symbol	KM23C32005 -15		KM23C32005 -20		KM23C32005 -25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

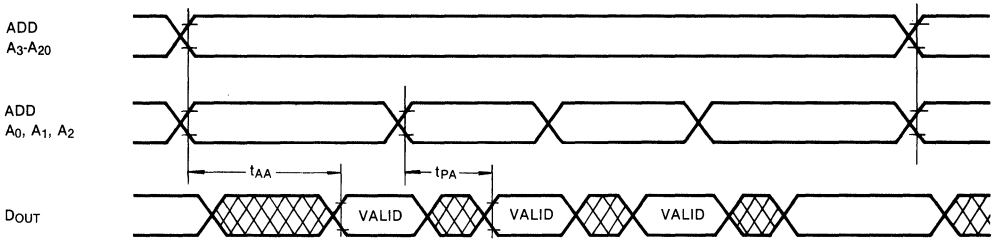
* Page Address: A_0, A_1, A_2

TIMING DIAGRAM

READ



PAGE READ

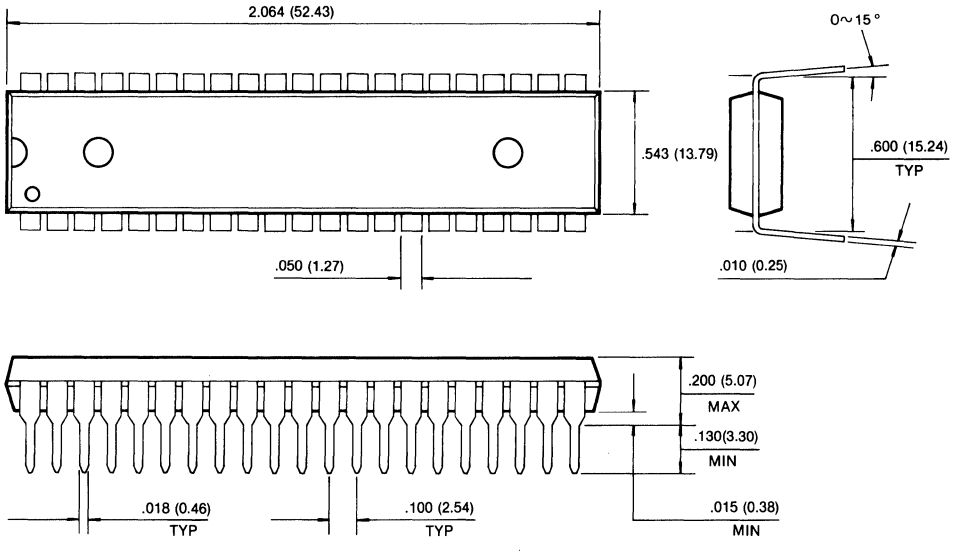


★ After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C32005)

Unit: Inches (mm)

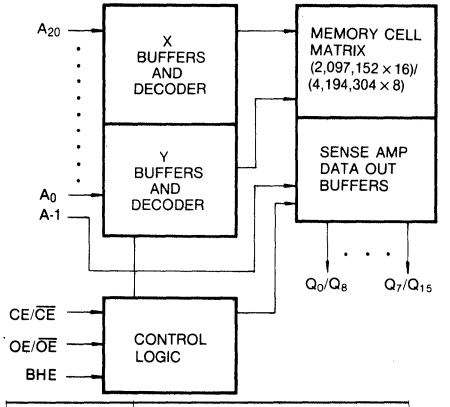


32M-Bit (4M x 8/2M x 16) CMOS MASK ROM

FEATURES

- **Switchable organization**
  4,194,304 x 8 (byte mode)
  2,097,152 x 16 (word mode)
- **Fast access time**
  Random access: 150ns (max.)
  Page access: 70ns (max.)
- **Supply voltage: single +5V**
- **Current consumption**
  Operating: 100mA (max.)
  Standby : 50μA(max.)
- **Fully static operation**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Polarity programmable chip enable and output enable pin**
- **Package: 44-pin, 600 mil, plastic SOP**

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_2	Page Address Inputs
A_3-A_{20}	Address Inputs
Q_0-Q_{14}	Data Outputs
Q_{15}/A-1	Output 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$*	Chip Enable
OE/$\overline{OE}$*	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

* User Selectable Polarity

GENERAL DESCRIPTION

The KM23C32005G is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 x 8 bit (byte mode) or as 2,097,152 x 16 bit (word mode) depending on BHE voltage level. (See mode selection table).

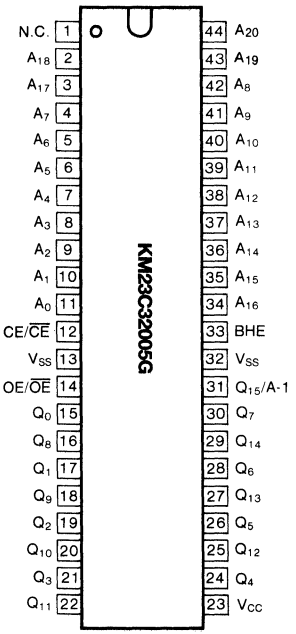
This device is includes PAGE read mode function, page read mode allows two or four to eight words of data to be read fast in the same page, CE and A_3-A_{20} should not be changed.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32005G in a 44-SOP, provides polarity programmable CE and OE buffer as user option mode.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz all output open	—	100	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, all output open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC}$, all output open	—	50	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to V_{CC}	—	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	$V_{CC}+0.3$	V
Input Low Voltage, All Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V

CAPACITANCE ($T_a = 25°C$, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	12.0	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	Q_{15}/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q_0-Q_{15}:D_{OUT}	Active
		L	Input	Operating	Q_0-Q_7: D_{OUT} Q_8-Q_{14}: High-Z	Active

AC CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L = 100pF$

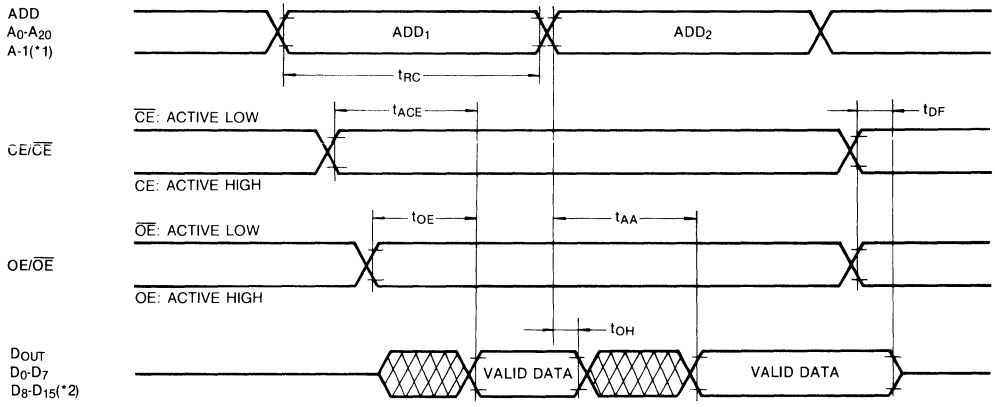
READ CYCLE

Parameter	Symbol	KM23C32005(G)-15		KM23C32005(G)-20		KM23C32005(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Page Address Access Time	t_{PA}		70		90		110	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

* Page Address: A_0, A_1, A_2

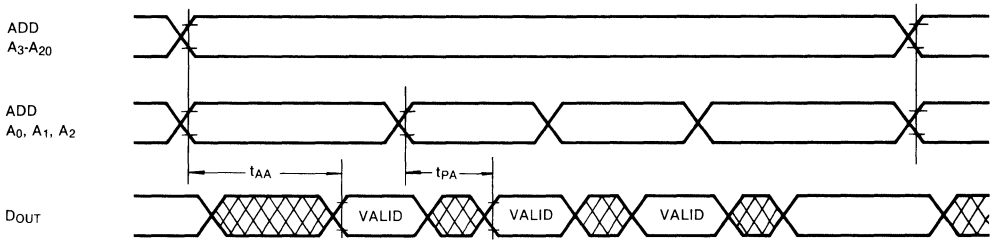
TIMING DIAGRAM

READ



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

PAGE READ

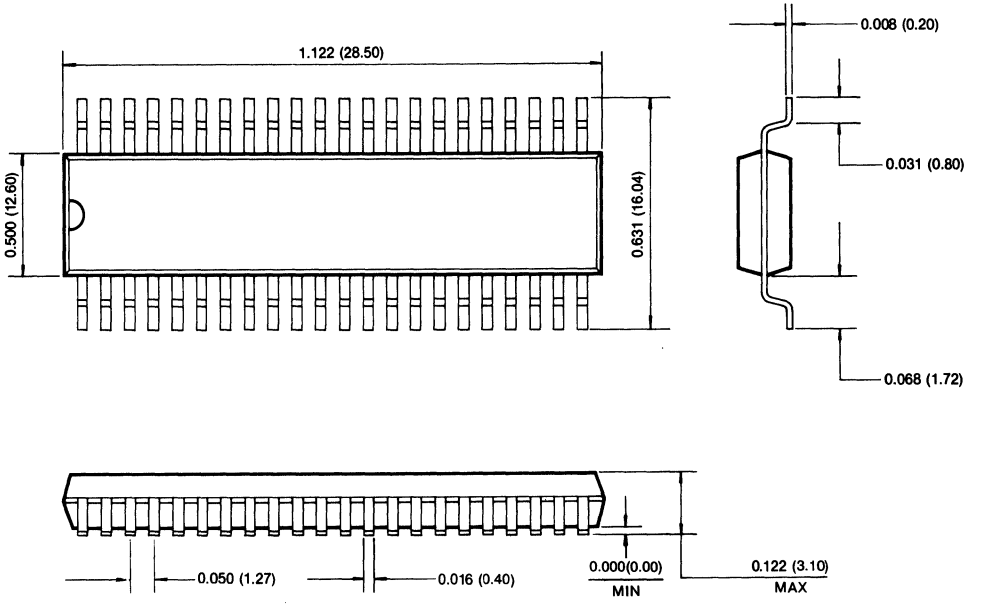


* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

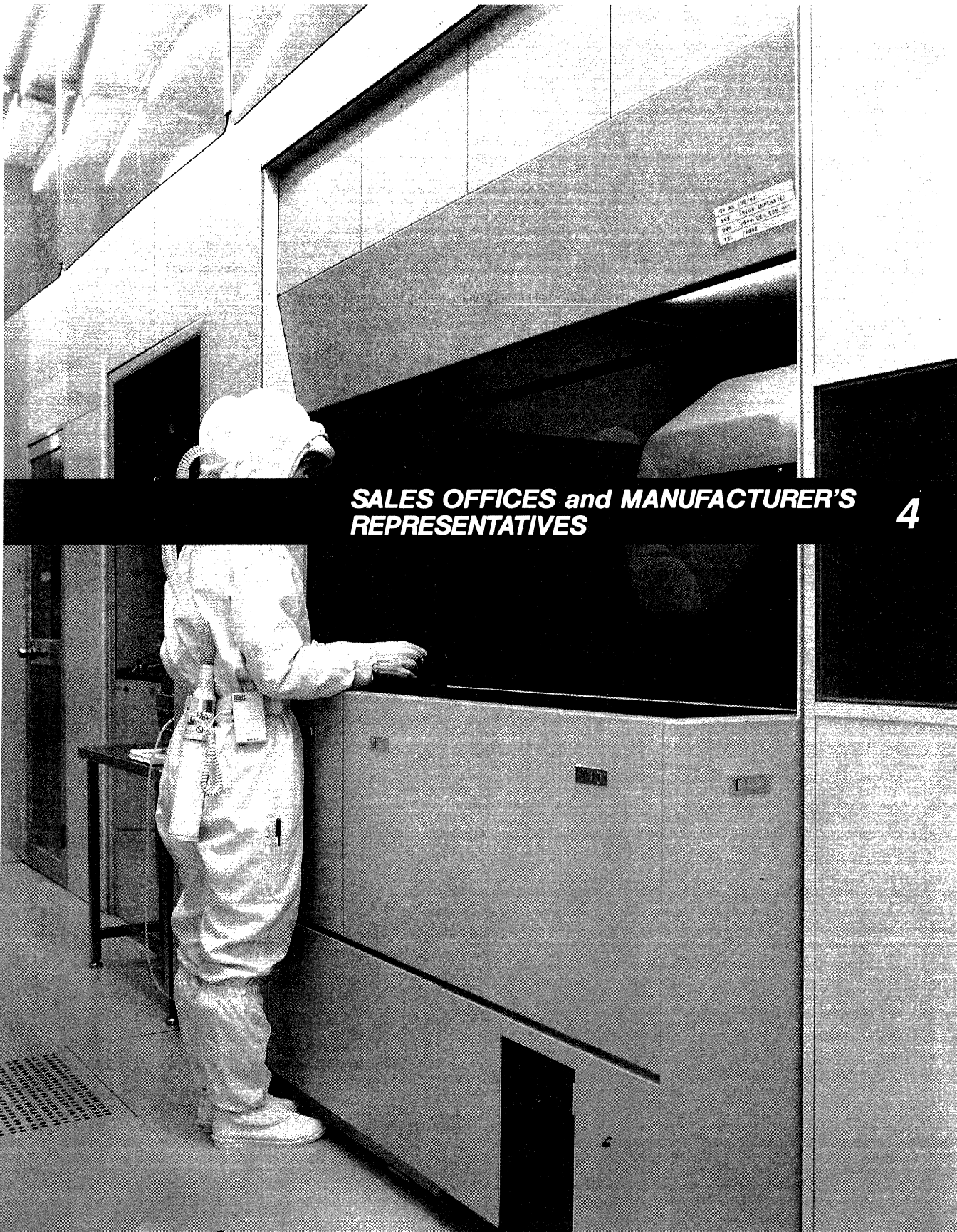
PACKAGE DIMENSIONS

44 LEAD SMALL OUTLINE PACKAGE (KM23C32005G)

Unit: Inches (mm)



SAMSUNG ELECTRONICS



SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

4

SAMSUNG SEMICONDUCTOR SALES OFFICES-U.S.A.

Northwest
3655 North First Street
San Jose, CA 95134
Tel: (408) 954-7000
Fax: (408) 954-7883

North Central
300 Park Boulevard
Suite 210
Itasca, IL 60143-2636
Tel: (708) 775-1050
Fax: (708) 775-1058

North East
20 Mall Road
Suite 410
Burlington, MA 01803
Tel: (617) 273-4888
Fax: (617) 273-9363

Southwest
16253 Laguna Canyon Road
Suite 100
Irvine, CA 92718
Tel: (714) 753-7530
Fax: (714) 753-7544

South Central
15851 Dallas Parkway
Suite 840
Dallas, TX 75248-3307
Tel: (214) 770-7970
Fax: (214) 770-7971

Southeast
802 Greenvalley Road
Suite 204
Greensboro, NC 27408
Tel: (919) 370-1600
Fax: (919) 370-1633

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SOUTH ATLANTIC COMPONENT SALES
1100 Jordon Lane — TEL: (205) 533-4229
Suite D — FAX: (205) 533-5008
Huntsville, AL 35816

SOUTHERN COMPONENT SALES
307 Clinton Avenue E, #413 — TEL: (205) 533-6500
Huntsville, AL 35801 — FAX: (205) 533-6578

ARIZONA

O'DONNELL ASSOCIATES — TEL: (602) 944-9542
2432 W. Peoria Ave. #1026 — FAX: (602) 861-2615
Phoenix, AZ 85029

CALIFORNIA

BESTRONICS — TEL: (619) 693-1111
9683 Tierra Grande Street, #102 — FAX: (619) 693-1963
San Diego, CA 92126

I-SQUARED — TEL: (408) 988-3400
3350 Scott Blvd. — FAX: (408) 988-2079
Building 10
Santa Clara, CA 95054

WESTAR REP COMPANY — TEL: (714) 453-7900
15265 Alton Parkway, #400 — FAX: (714) 453-7930
Irvine, CA 92718

WESTAR REP COMPANY — TEL: (818) 880-0594
26500 Agoura Rd., #204 — FAX: (818) 880-5013
Calabasas, CA 91302

CANADA

INTELATECH, INC. — TEL: (403) 230-3190
218 Third Avenue NE — FAX: (403) 230-3183
Calgary, Alberta, CanadaT2E 0H2

INTELATECH, INC. — TEL: (416) 629-0082
1115 Crestlawn Drive, #1 — FAX: (416) 629-1795
Mississauga, Ontario L4W1A7I

INTELATECH, INC. — TEL: (514) 630-6041
29 Charlevoix — FAX: (514) 630-5612
Kirkland, Quebec, Canada H9J 2S4

INTELATECH, INC. — TEL.:(613) 762-8014
275 Michael Copeland Drive — FAX:(416) 629-1795
Canata, Ontario, Canada K2M 2G2

COLORADO

FRONT RANGE MARKETING — TEL: (303) 443-4780
3100 Arapahoe Road, #404 — FAX: (303) 447-0371
Boulder, CO 80303

FLORIDA

B/B TECH SALES — TEL: (305) 477-0341
3900 N.W. 79th Avenue, #636 — FAX: (305) 477-0343
Miami, FL 33166

DYNE-A-MARK CORP. — TEL: (407) 835-2822
101 Sunnytown Road, #110 — FAX: (407) 834-4524
Casselberry, FL 32707

DYNE-A-MARK CORP. — TEL: (407) 724-7470
742 Penguin Avenue NE — FAX: (407) 984-2718
Palm Bay, FL 32905

DYNE-A-MARK CORP. — TEL: (305) 771-6508
1001 NW 62nd Street, #300N — FAX: (305) 772-0114
Fort Lauderdale, FL 33309

DYNE-A-MARK CORP. — TEL: (813) 345-9411
7884 Tent Avenue S — FAX: (813) 345-3731
St. Petersburg, FL 33707

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SOUTH ATLANTIC COMPONENT SALES
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Norcross, GA 30092 — FAX: (404) 447-6714

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DAVIX INTERNATIONAL LTD.
1655 N. Arlington Heights Rd. — TEL: (708) 259-5300
Suite 302 East — FAX: (708) 259-5428
Arlington Heights, IL 60004

INDIANA

GEN II MARKETING, INC. — TEL: (317) 848-3083
3003 E. 96th Street, #102 — FAX: (317) 848-1264
Indianapolis, IN 46240

GEN II MARKETING, INC — TEL: (219) 436-4485
1415 Magnavox Way, #130 — FAX: (219) 436-1977
Ft. Wayne, IN 46804

IOWA

ASSOCIATED ELECTRONIC MARKETING, INC.
4001 Shady Oak — TEL: (319) 377-1129
Marion, IA 52302 — FAX: (319) 377-1539

KANSAS

ASSOCIATED ELECTRONIC MARKETING, INC.
8843 Long St. — TEL: (913) 888-0022
Lenexa, KS 66215 — FAX: (913) 888-4848

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