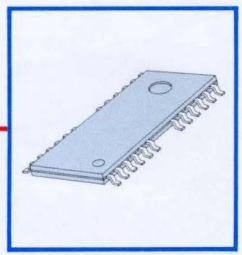
SAMSUNG

Data sheets

16M DRAM

JAN., 1994



- KM41C16000A/AL/ALL/ASL
- KM44C4000A/AL/ALL/ASL
- KM44C4100A/AL/ALL/ASL
- KM48C2000A/AL/ALL/ASL
- KM48C2100A/AL/ALL/ASL
- KM41V16000A/AL/ALL/ASL
- KM44V4000A/AL/ALL/ASL
- KM44V4100A/AL/ALL/ASL
- KM48V2000A/AL/ALL/ASL
- KM48V2100A/AL/ALL/ASL

PRINTED IN KOREA

Certified ISO 9001

Certificate No FM 24651

16M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C16000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Common I/O using Early Write**
- **Double+5.0V±10% power supply**
- **4096 cycles/64ms refresh**
- **4096 cycles/128ms (Low Power & Self Ref.)**
- **4096 cycles/256ms (Super Low Power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

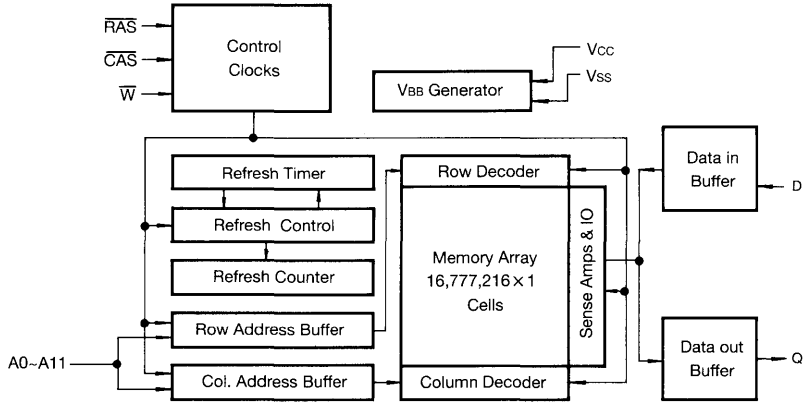
The Samsung KM41C16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41C16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

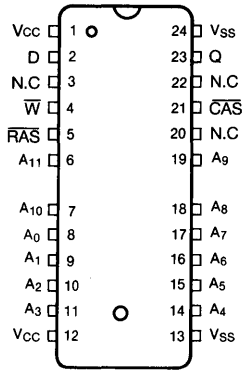
The KM41C16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



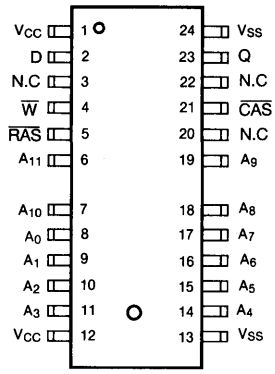
PIN CONFIGURATION (Top Views)

• **KM41C16000 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



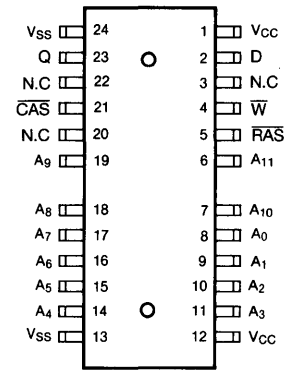
J : 400MIL
K : 300MIL

• **KM41C16000 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• **KM41C16000 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power(+5.0V)
VSS	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM41C16000A	I_{CC2}	-	2	mA
	KM41C16000AL			1	mA
	KM41C16000ALL			1	mA
	KM41C16000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM41C16000A/AL/ALL/ASL-6			70	mA
	KM41C16000A/AL/ALL/ASL-7			60	mA
	KM41C16000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM41C16000A	I_{CC5}	-	1	mA
	KM41C16000AL			300	μA
	KM41C16000ALL			200	μA
	KM41C16000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C16000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM41C16000A/AL/ALL/ASL-6			80	mA
	KM41C16000A/AL/ALL/ASL-7			70	mA
	KM41C16000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.5μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦min~300ns	KM41C16000AL	I_{CC7}	-	450	μA
	KM41C16000ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	KM41C16000ALL	ICCS	-	300	μA
Input Leakage Current (Any input 0≤VIN≤Vcc+0.5V, all other pins not under test=0 volts.)		II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤VOUT≤Vcc)		IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)		VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	CIN1	-	7	pF
Input Capacitance (A0-A11)	CIN2	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	CIN3	-	7	pF
Input Capacitance (Q)	COUT	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	5		5		5		5		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low Power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low Power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	13		15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	53		60		70		75		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

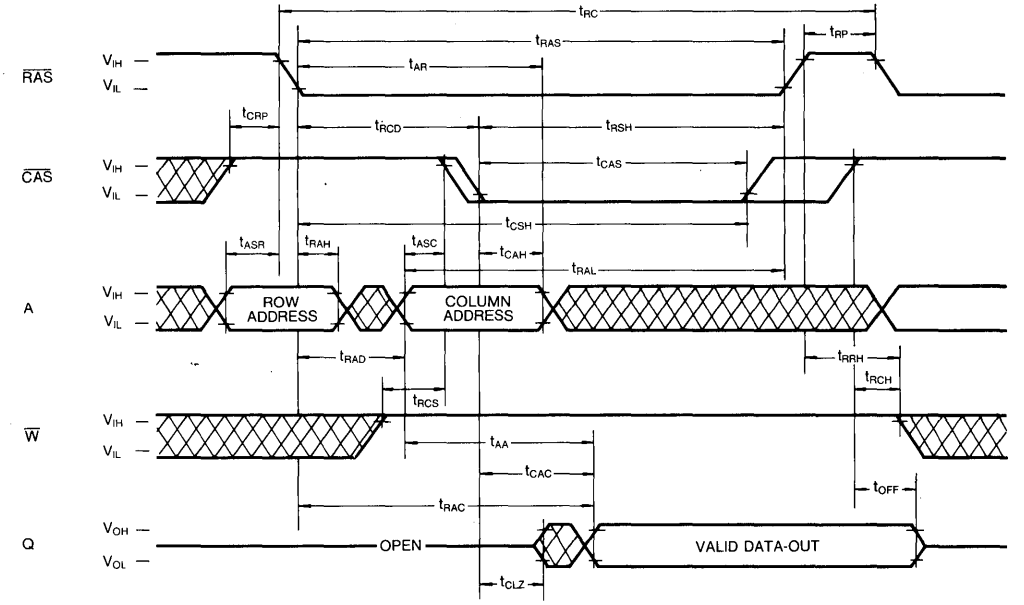
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	8
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	58		65		75		80		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

NOTES

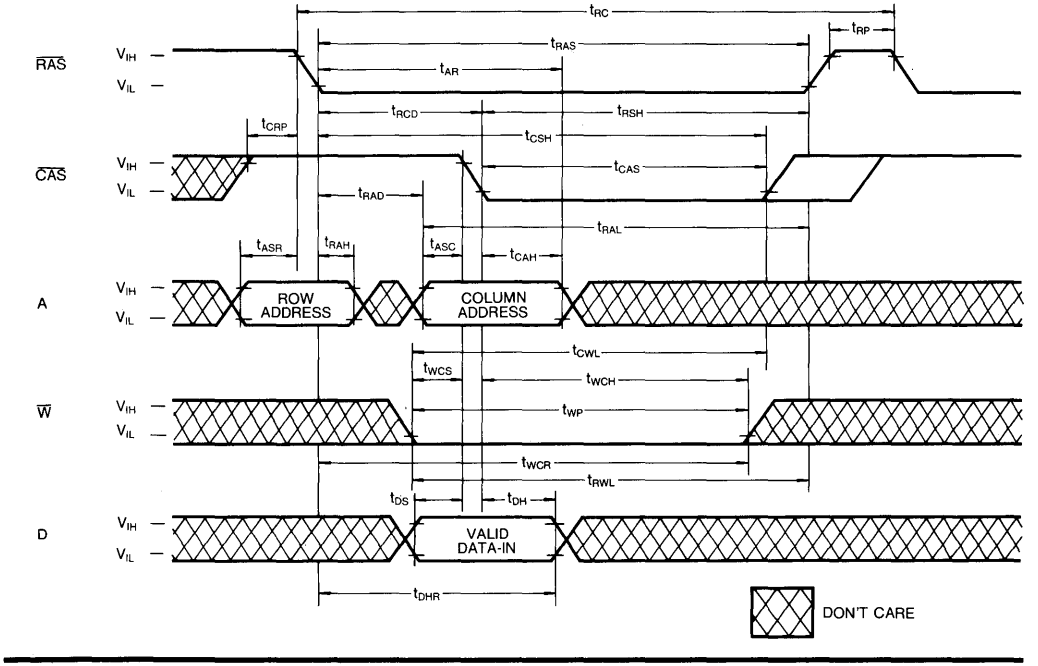
1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE

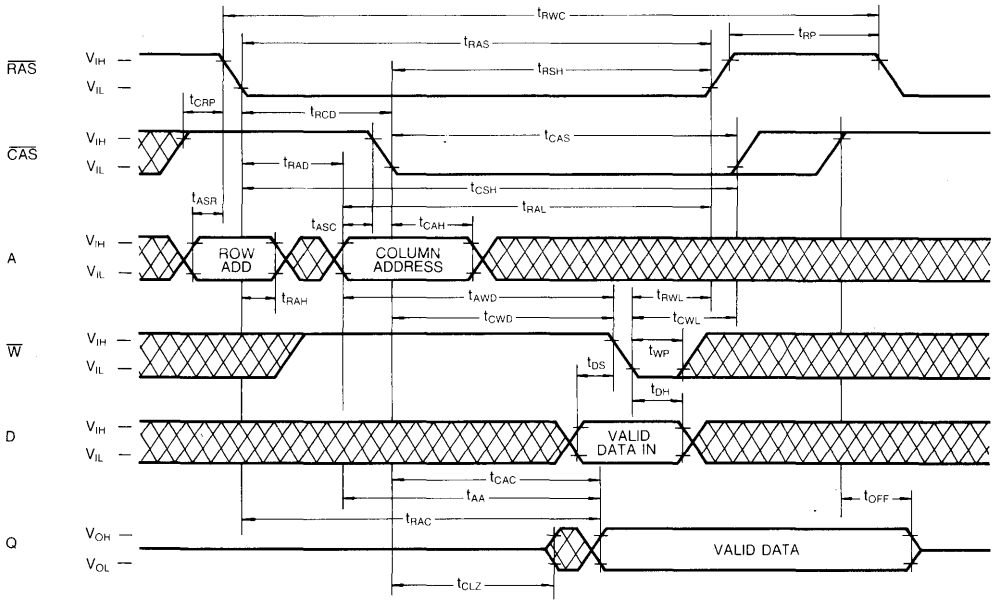


WRITE CYCLE (EARLY WRITE)

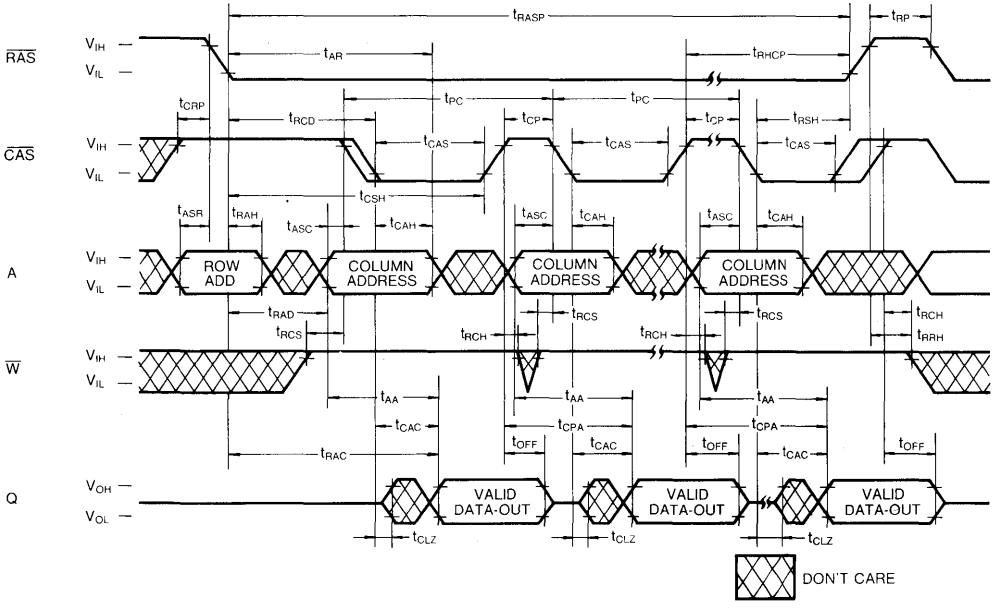


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

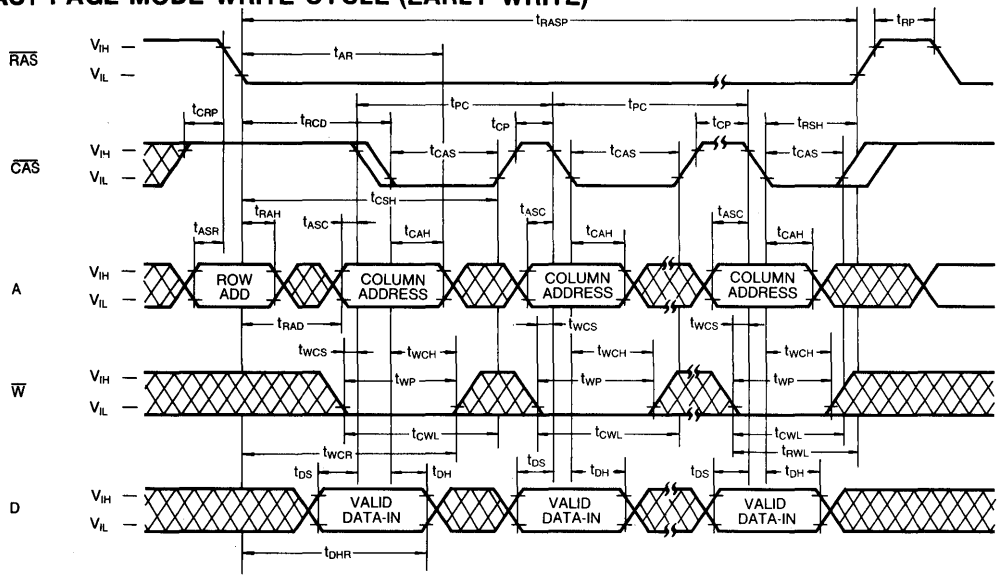


FAST PAGE MODE READ CYCLE

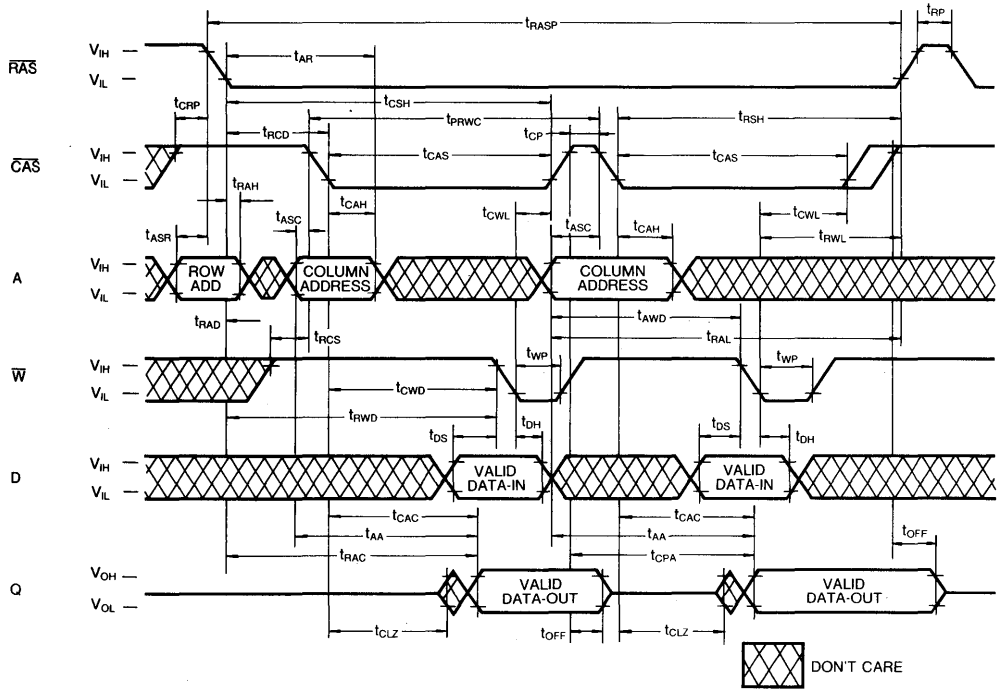


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



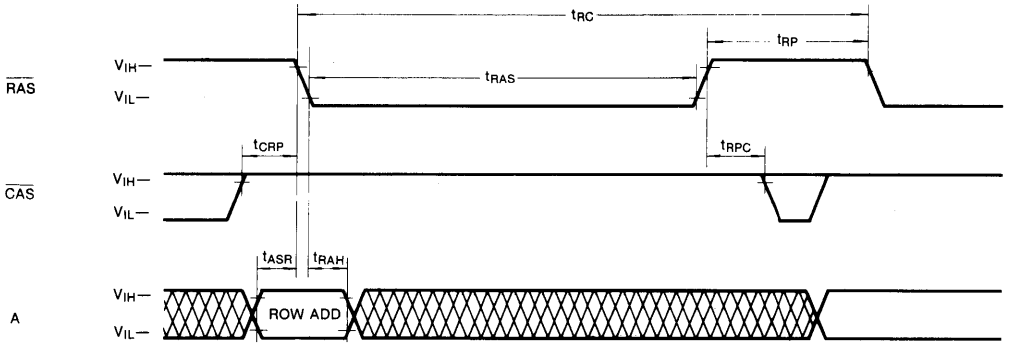
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

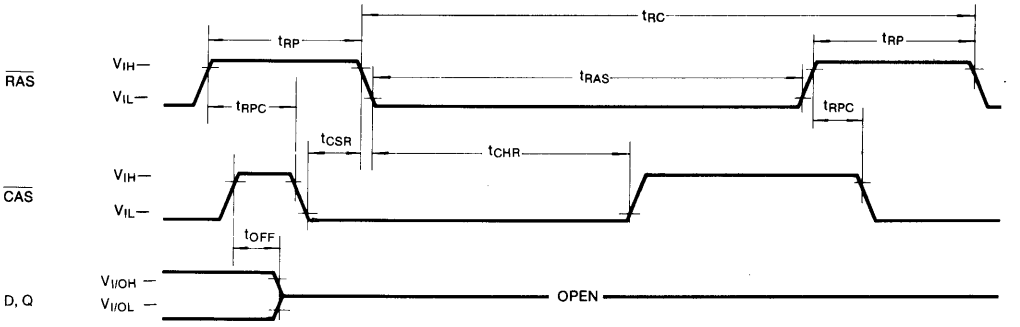
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



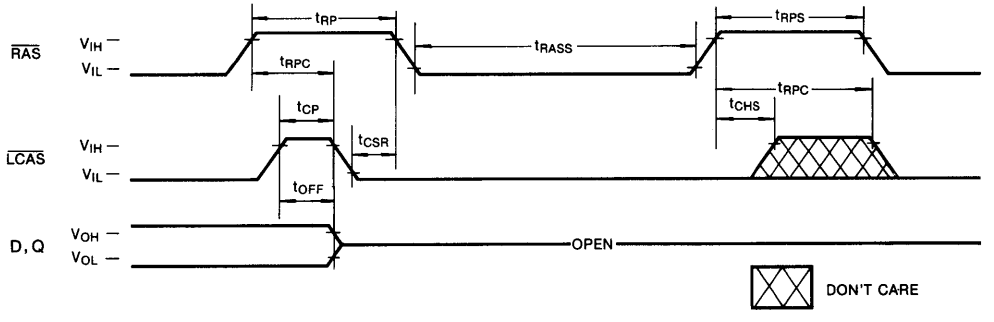
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



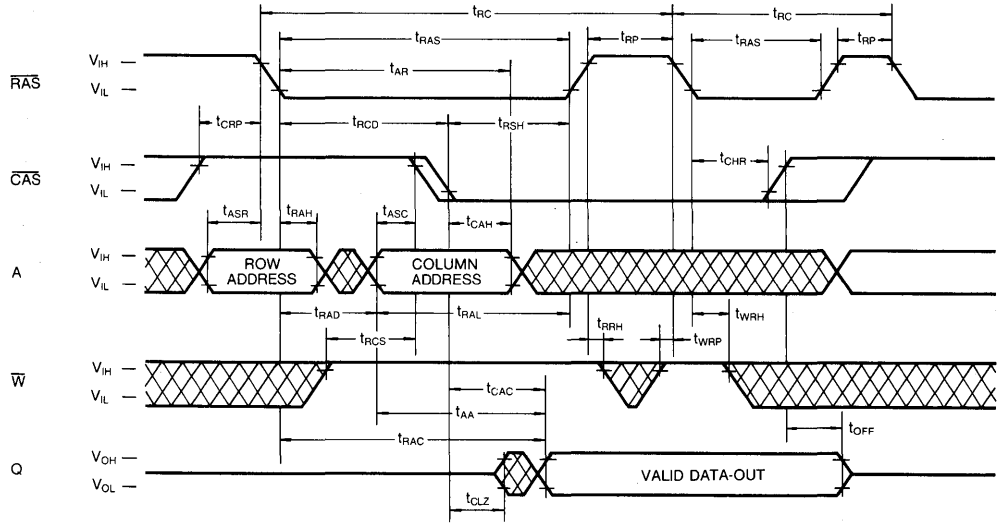
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

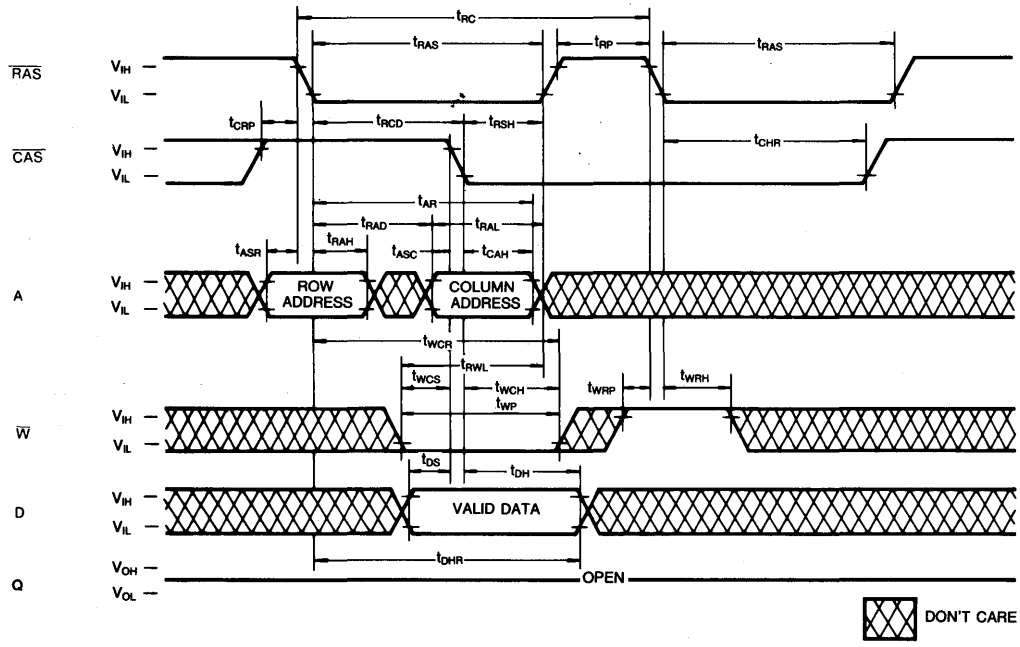


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

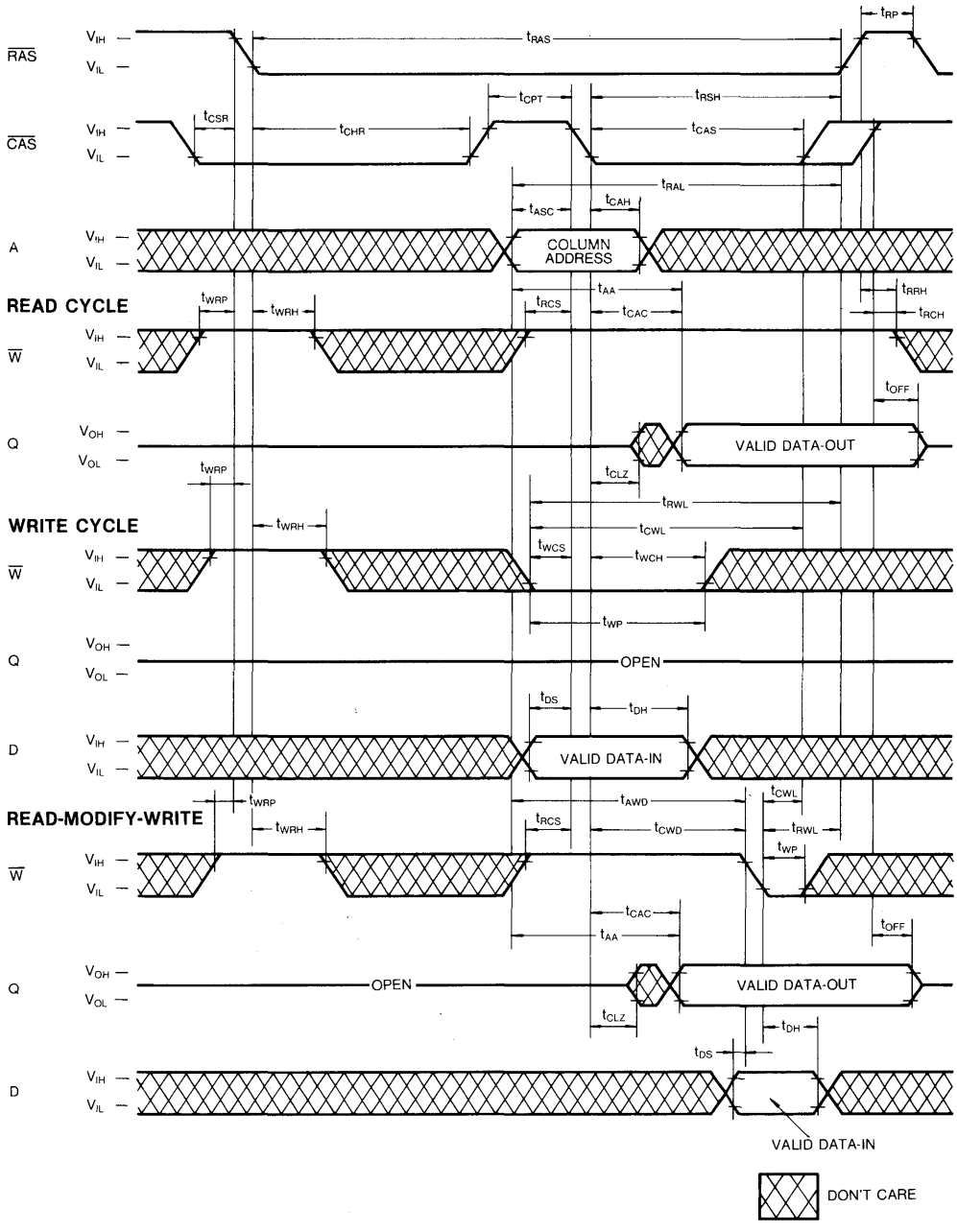


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

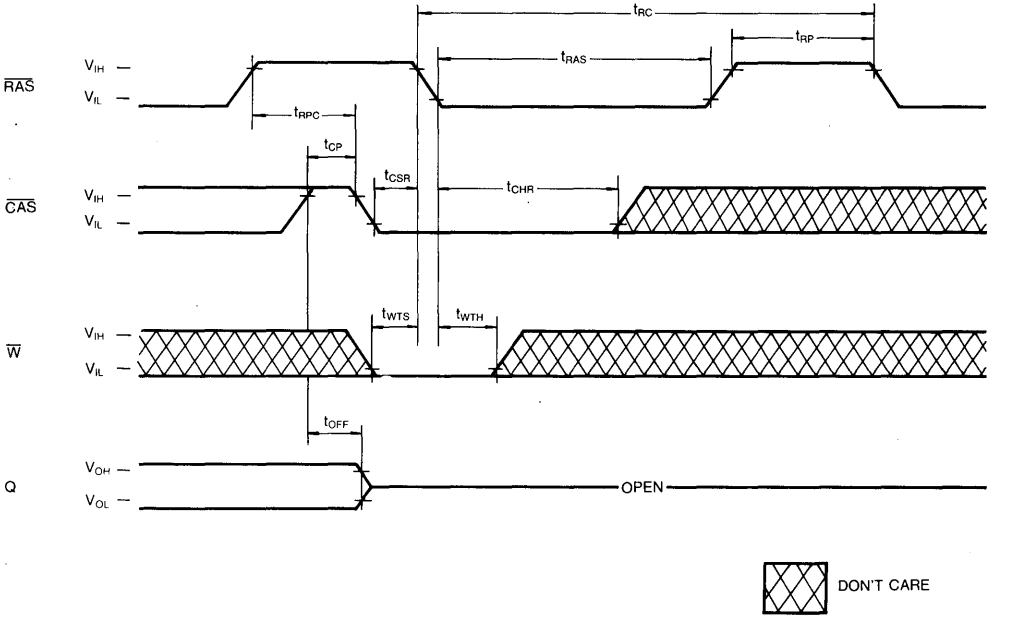


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



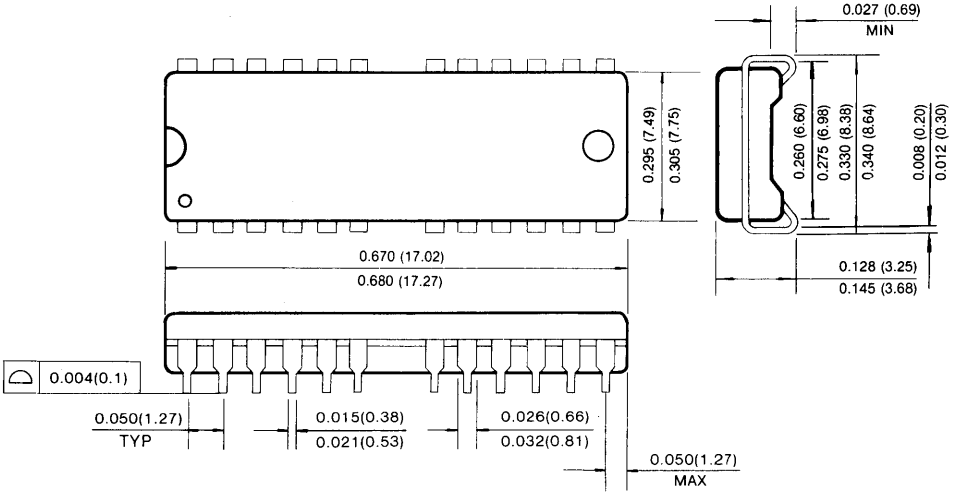
TEST MODE DESCRIPTION

The KM41C16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0". In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

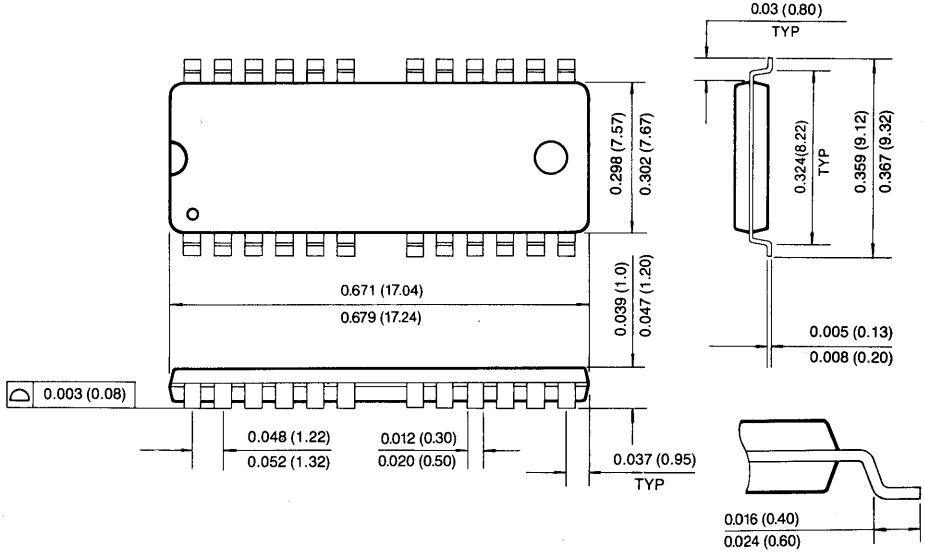
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

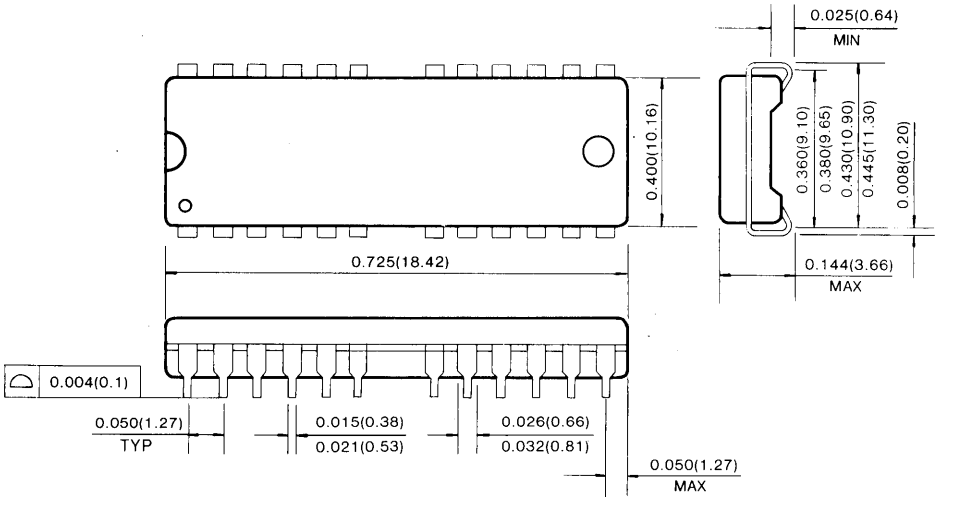


SAMSUNG ELECTRONICS

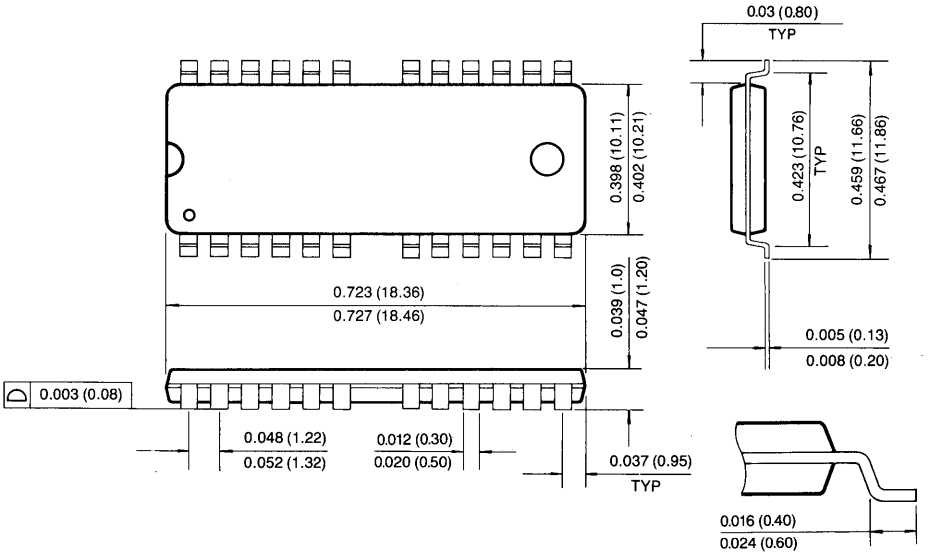
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

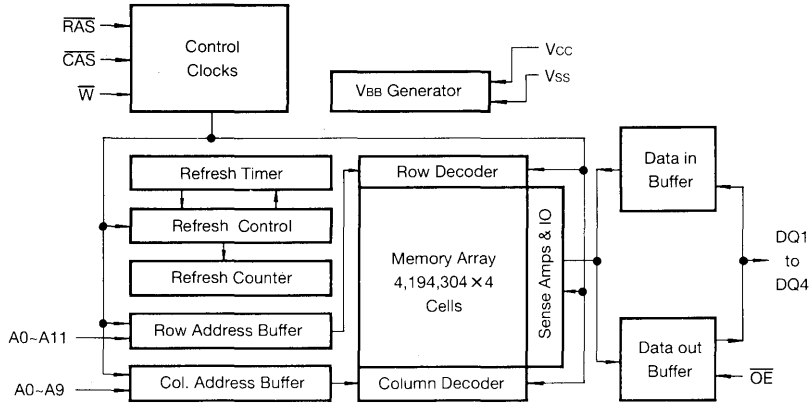
The Samsung KM44C4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

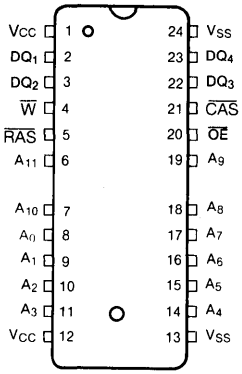
The KM44C4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



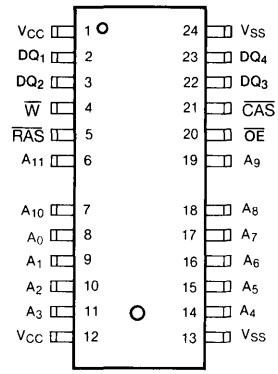
PIN CONFIGURATION (Top Views)

• KM44C4000 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



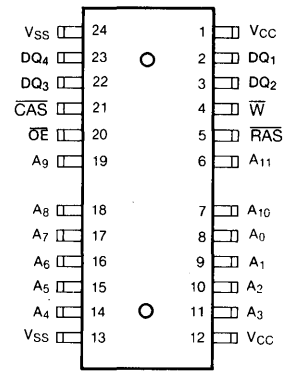
J : 400MIL
K : 300MIL

• KM44C4000 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4000 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VCC	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4000A	I_{CC2}	-	2	mA
	KM44C4000AL			1	mA
	KM44C4000ALL			1	mA
	KM44C4000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM44C4000A/AL/ALL/ASL-6			70	mA
	KM44C4000A/AL/ALL/ASL-7			60	mA
	KM44C4000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4000A	I_{CC5}	-	1	mA
	KM44C4000AL			300	μA
	KM44C4000ALL			200	μA
	KM44C4000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM44C4000A/AL/ALL/ASL-6			80	mA
	KM44C4000A/AL/ALL/ASL-7			70	mA
	KM44C4000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦min~300ns	KM44C4000AL	I_{CC7}	-	450	μA
	KM44C4000ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4000ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

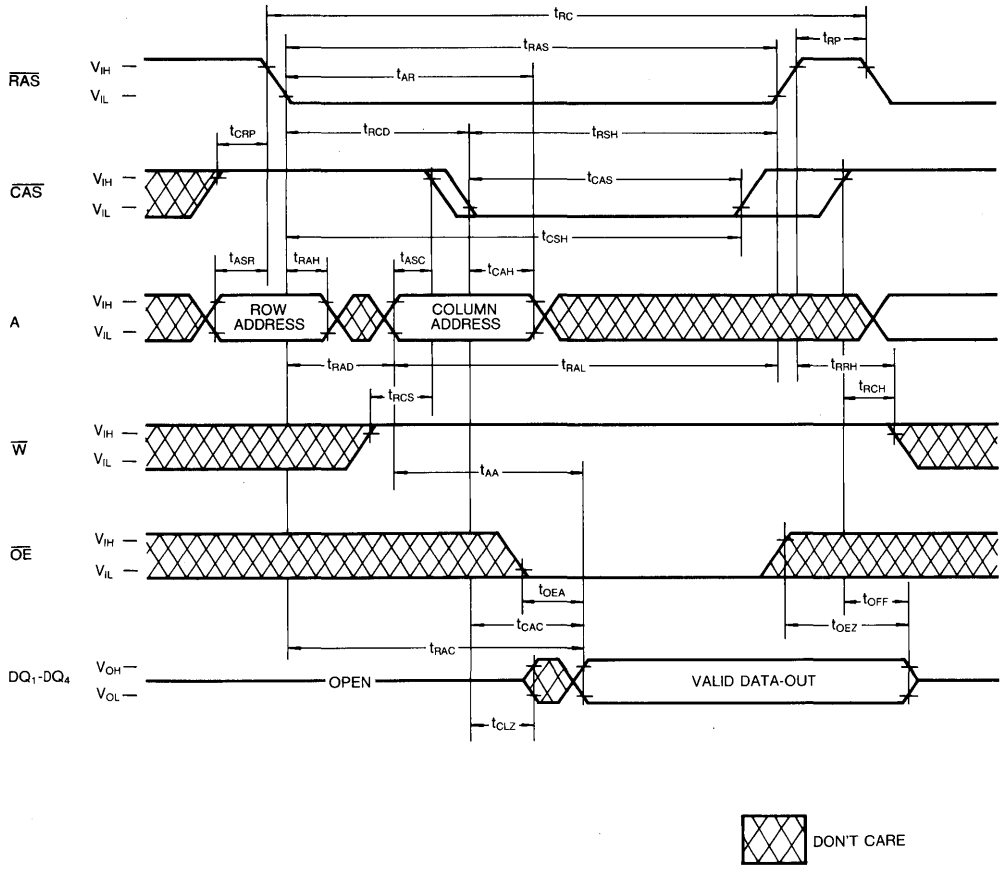
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

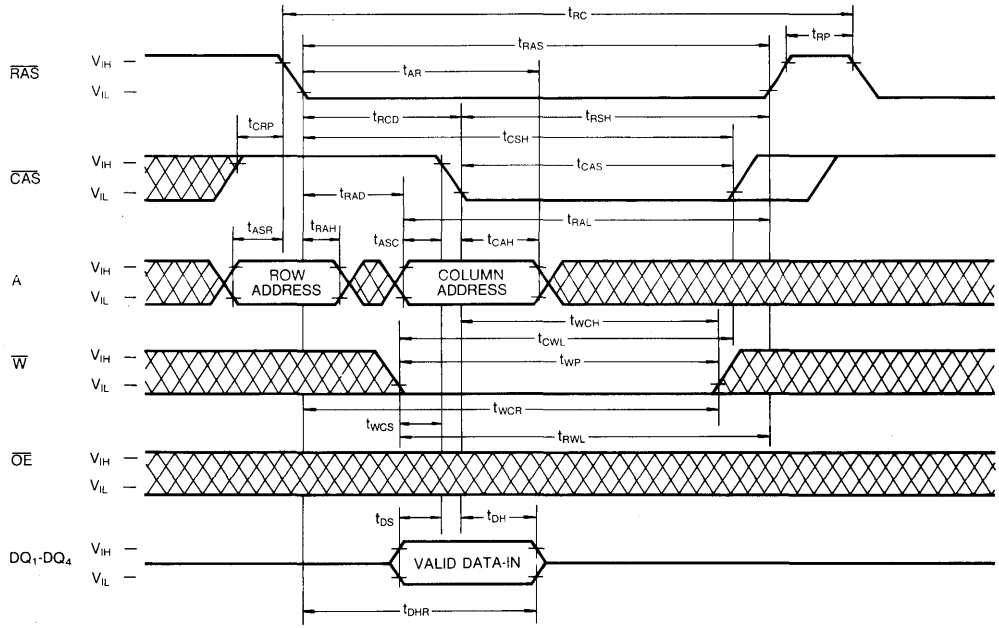
READ CYCLE



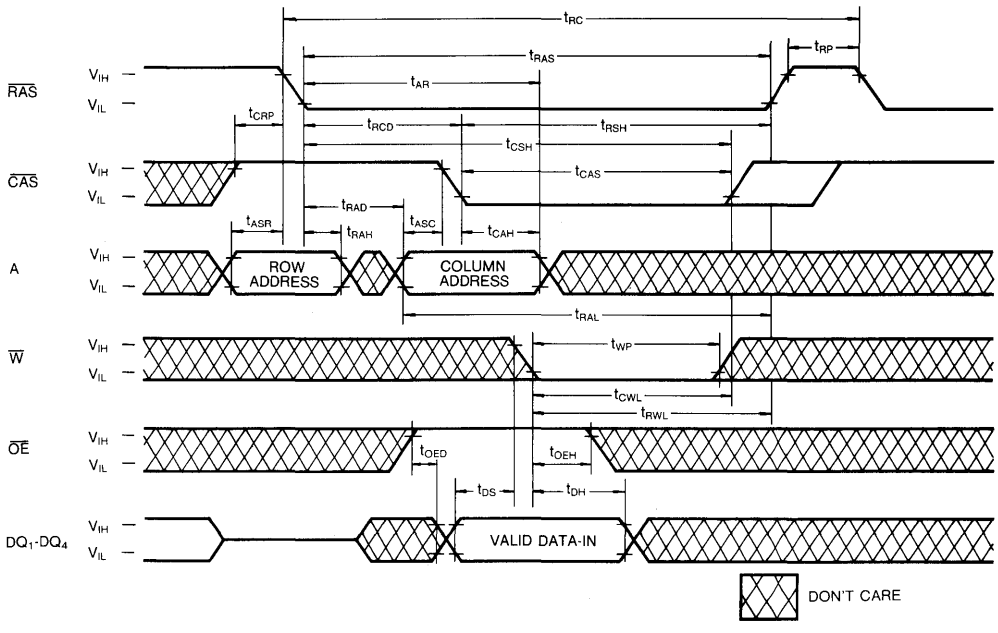
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

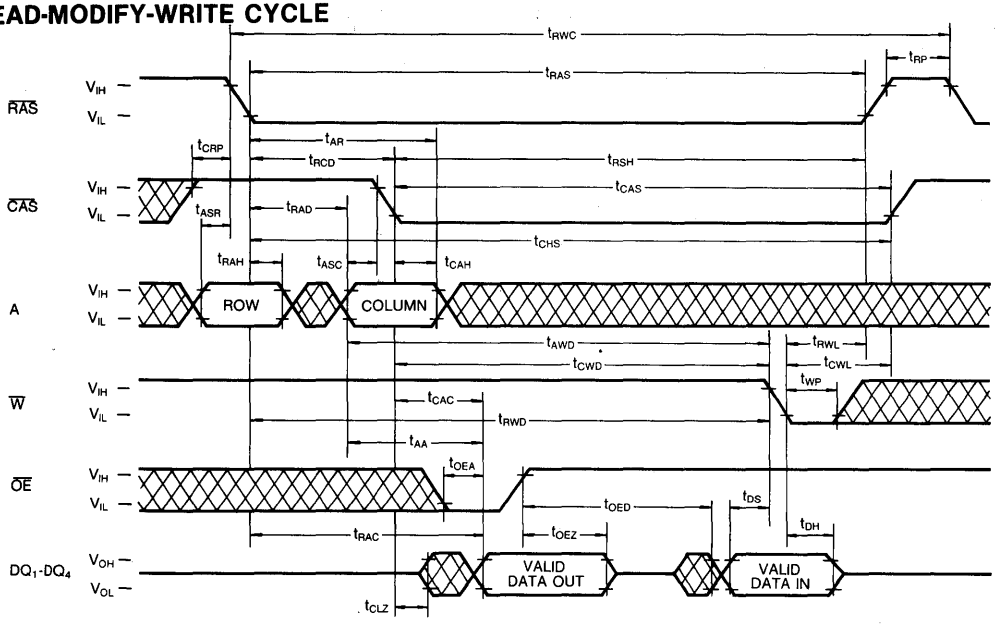


WRITE CYCLE (OE CONTROLLED WRITE)

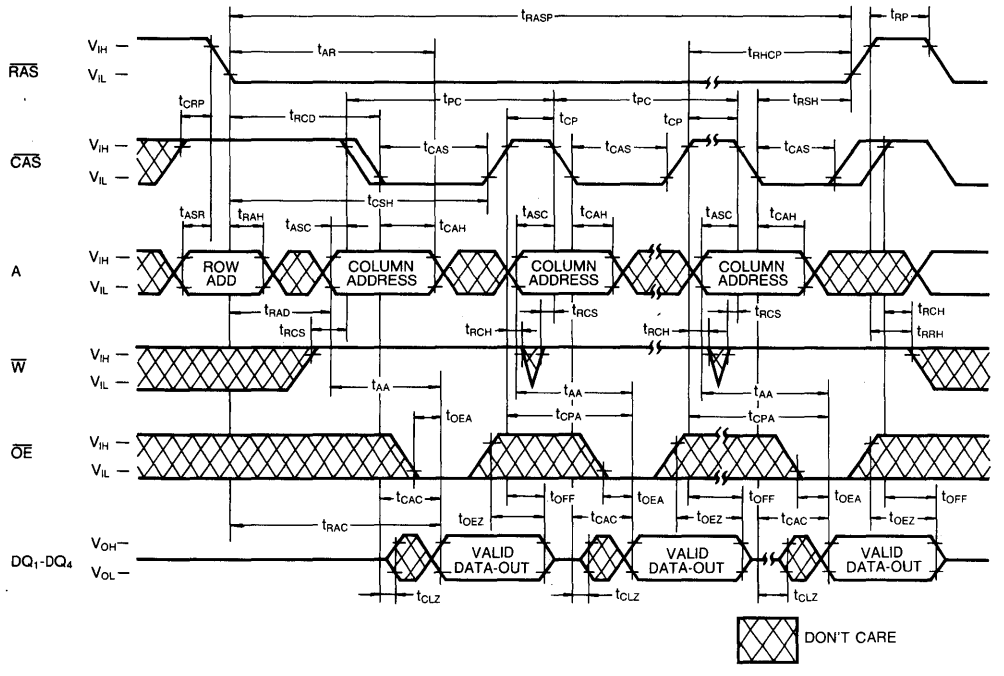


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



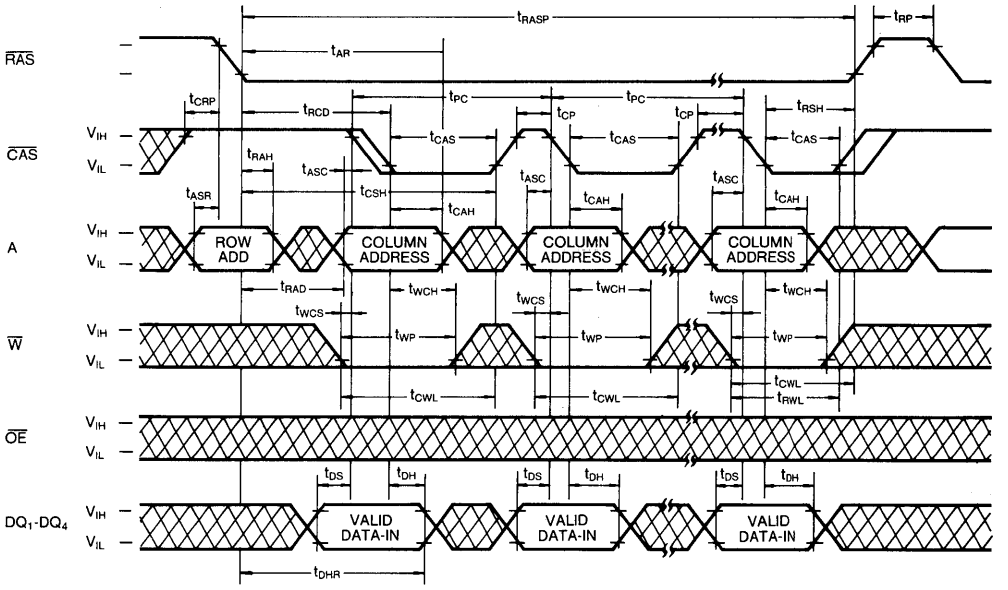
FAST PAGE MODE READ CYCLE



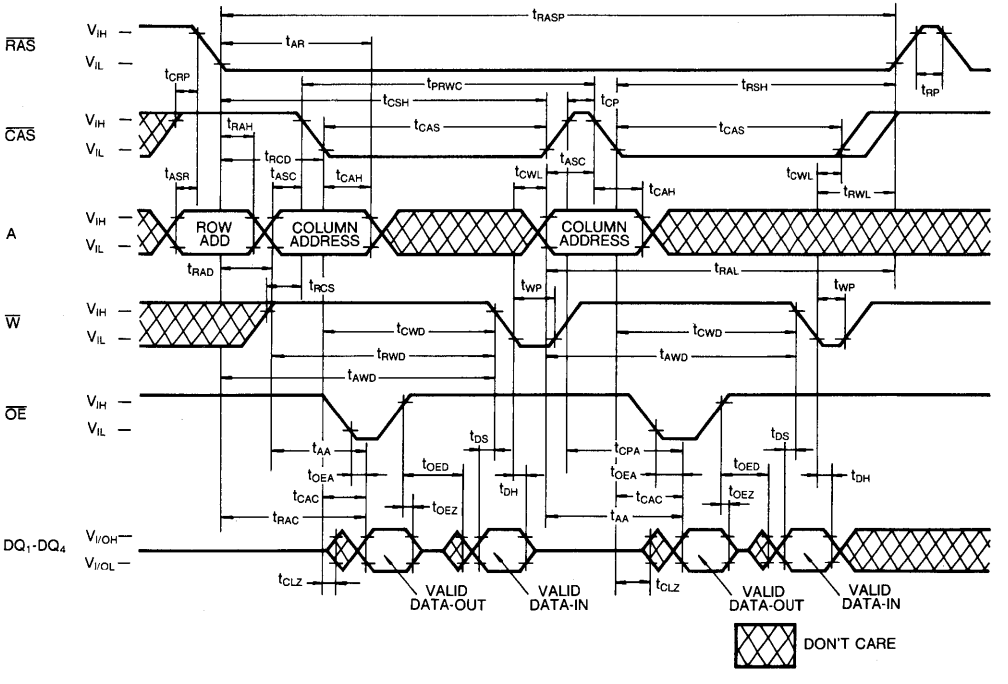
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



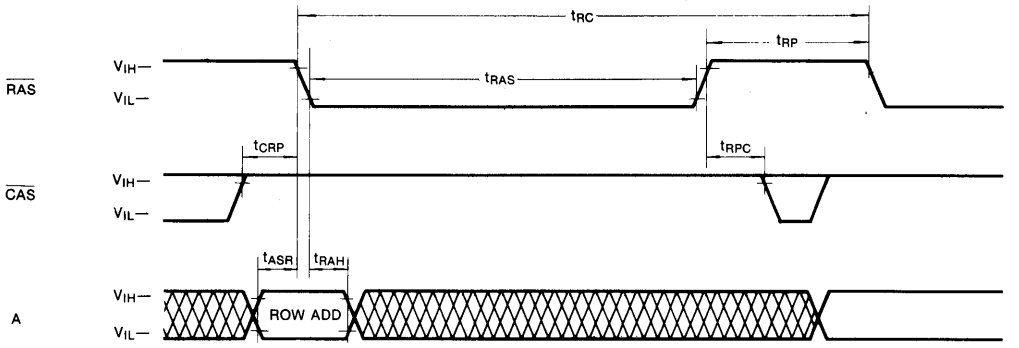
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

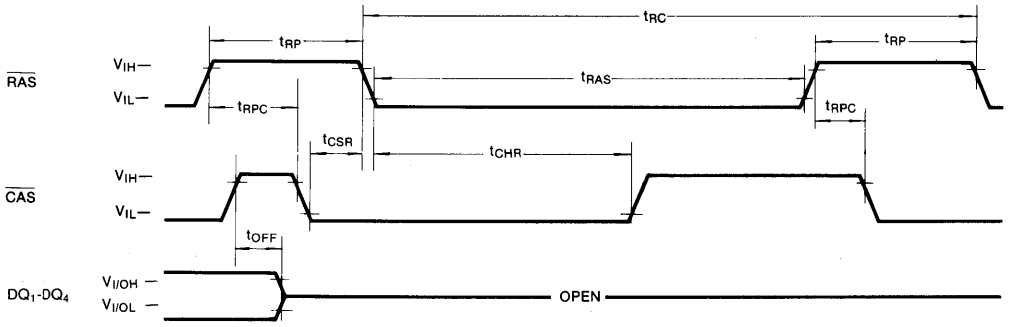
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



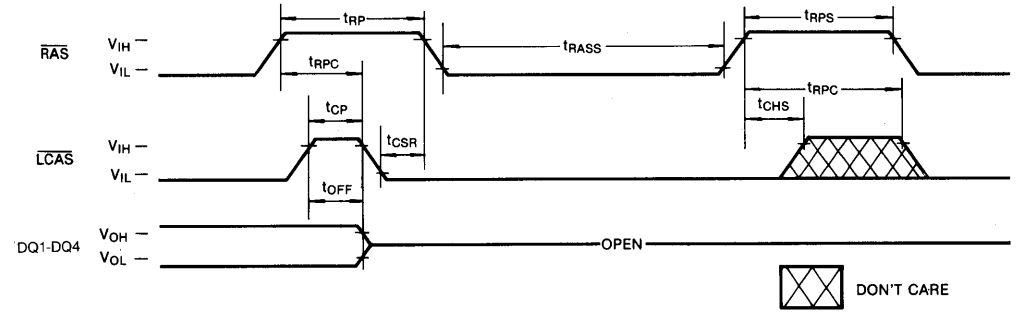
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



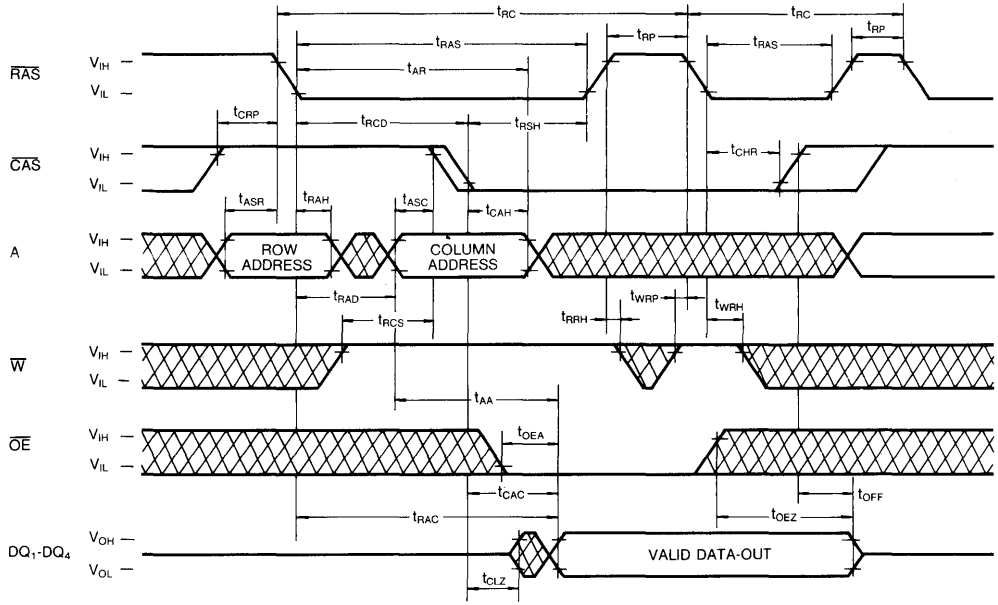
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

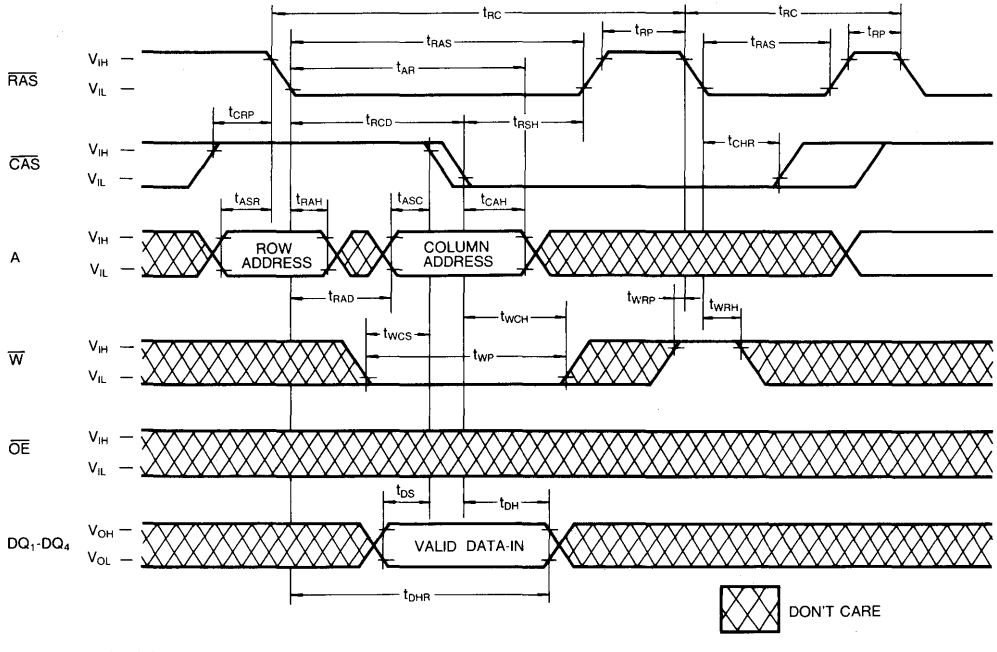


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

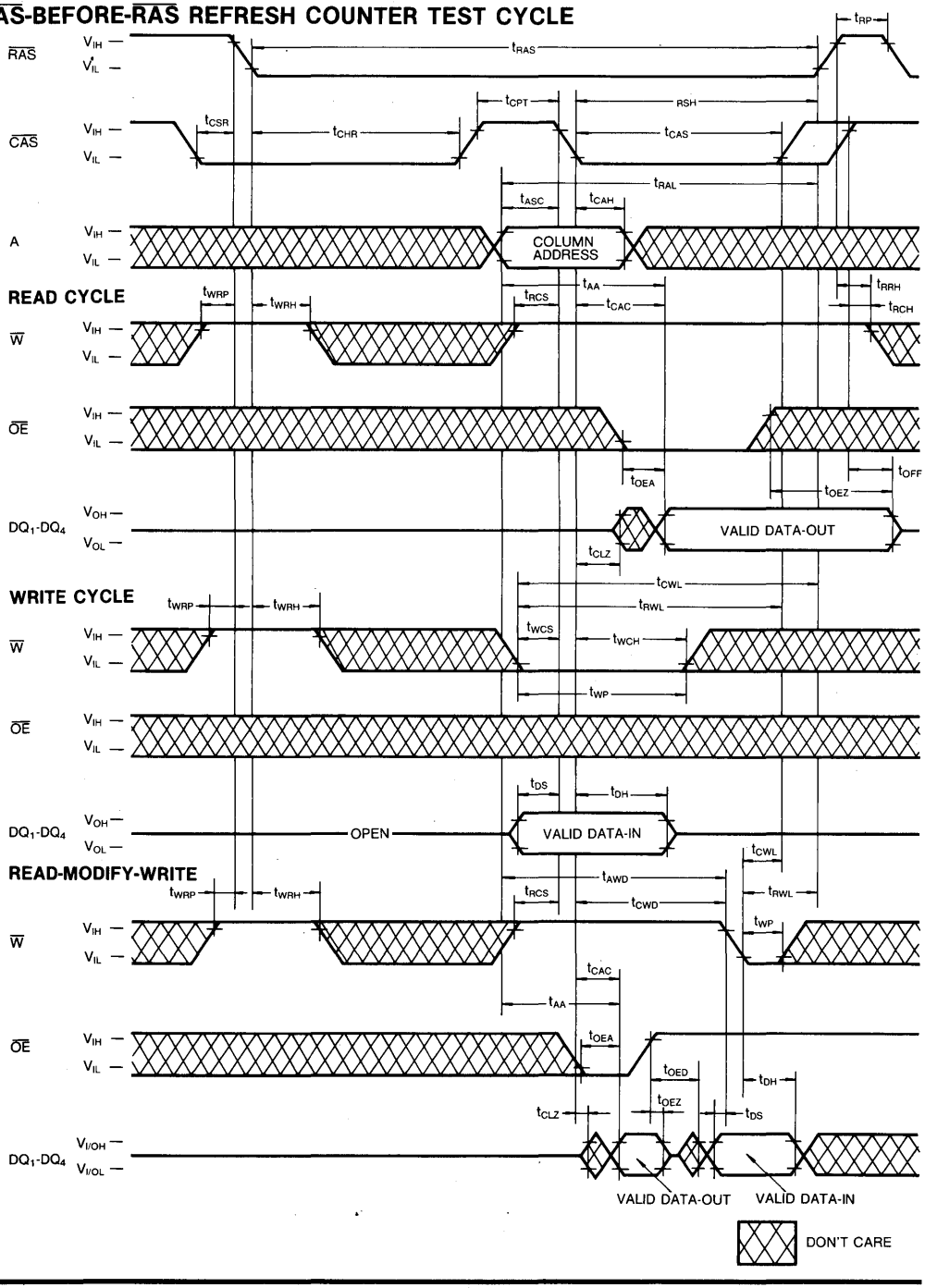


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

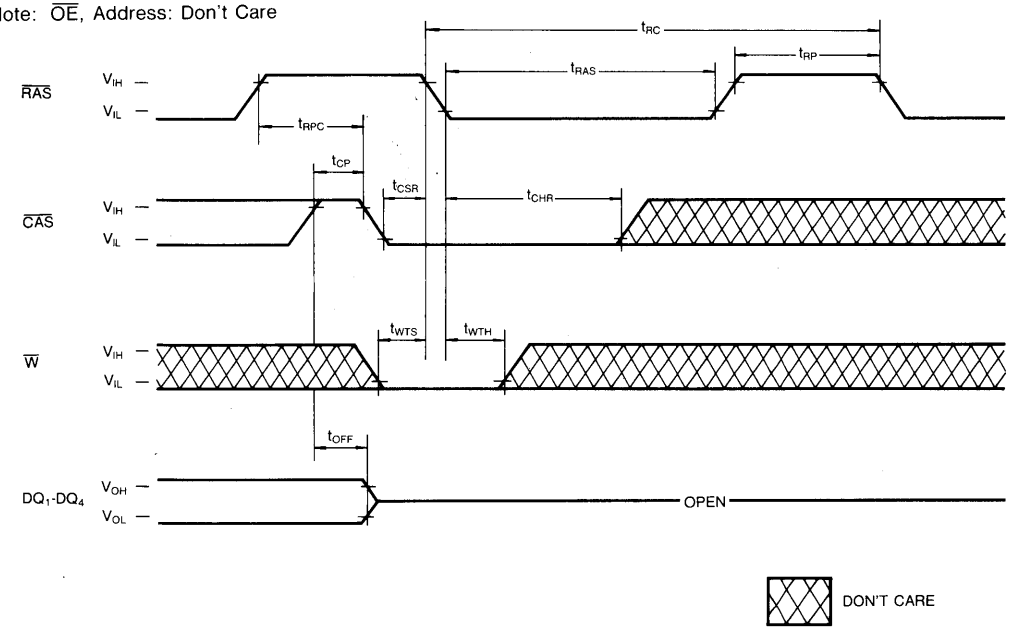


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



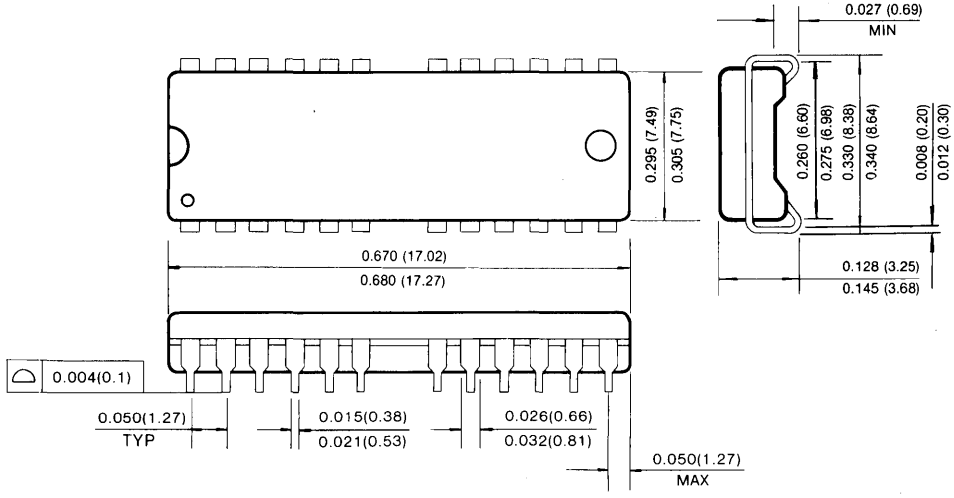
TEST MODE DESCRIPTION

The KM44C4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

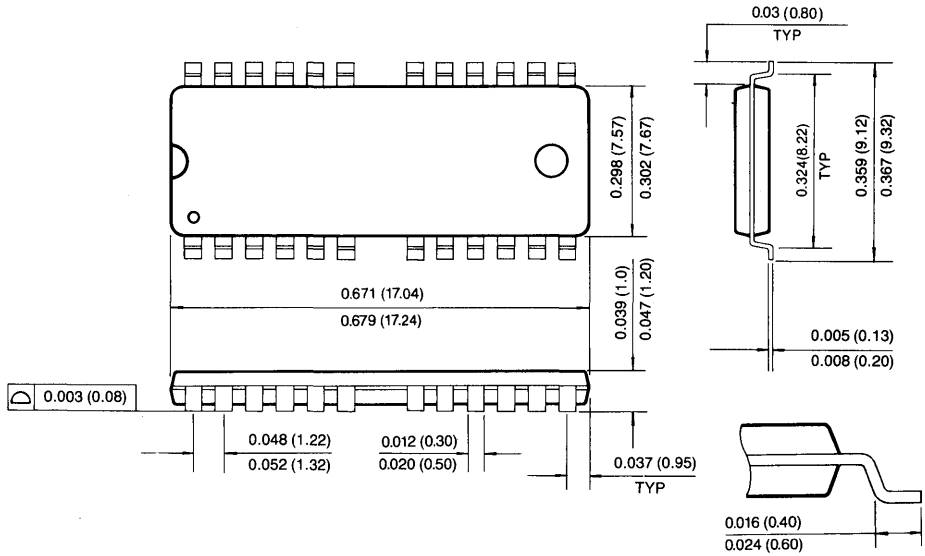
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

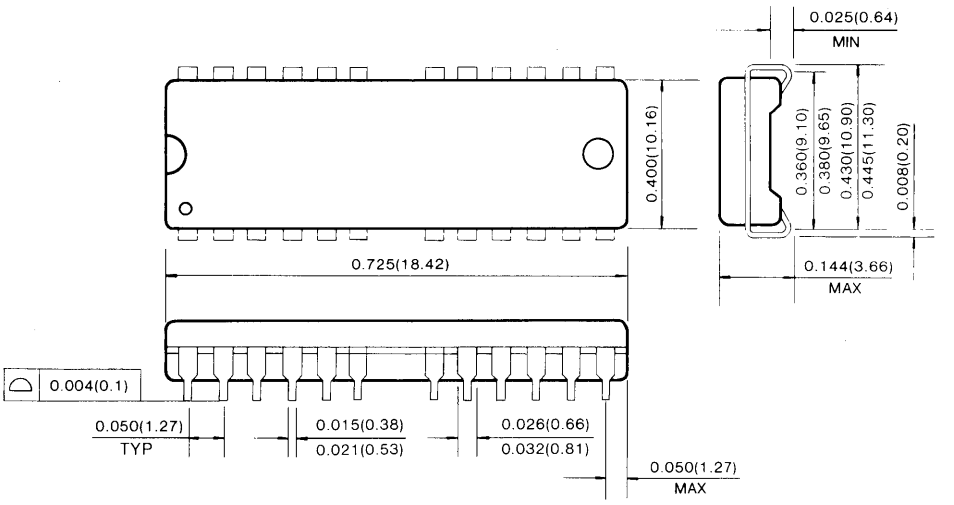


SAMSUNG ELECTRONICS

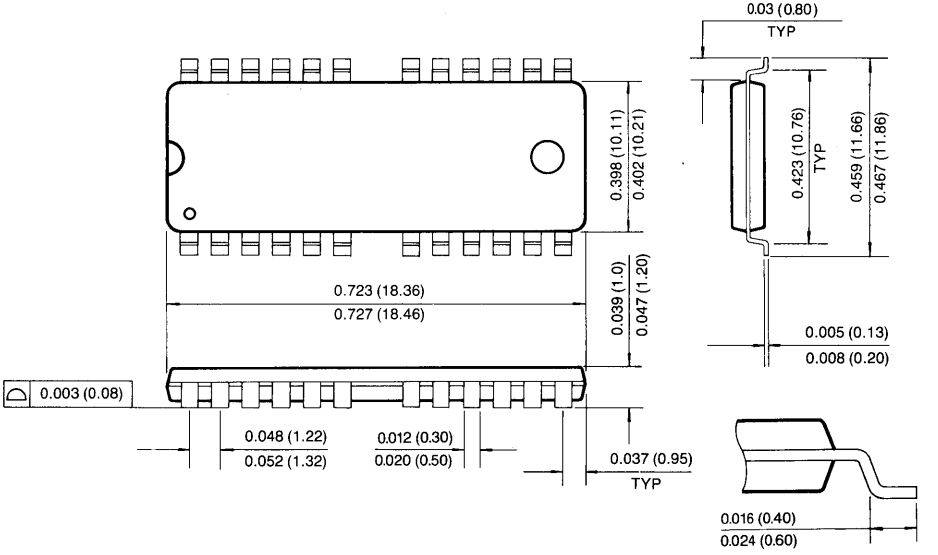
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C4100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double+5.0V±10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

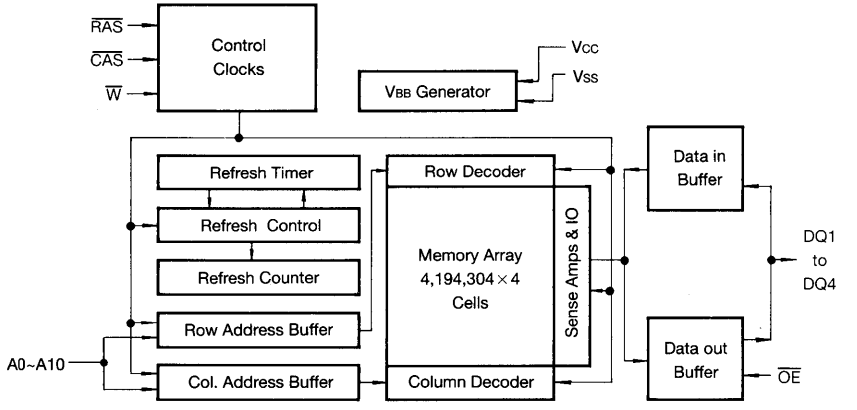
The Samsung KM44C4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

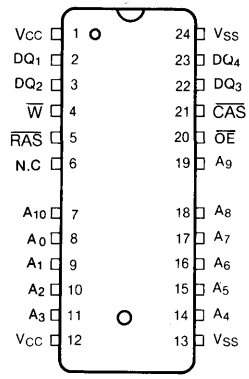
The KM44C4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



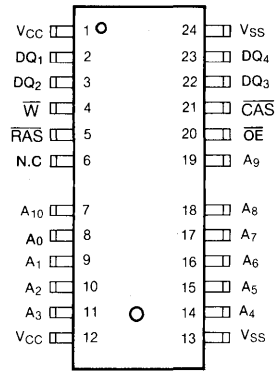
PIN CONFIGURATION (Top Views)

• **KM44C4100 AJ/ALJ/ALLJ/ASLJ**
AK/ALK/ALLK/ASLK



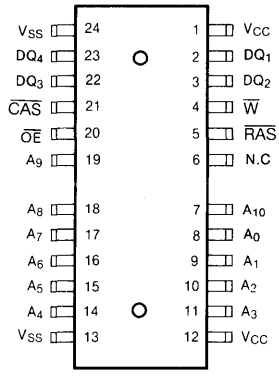
J : 400MIL
K : 300MIL

• **KM44C4100 AT/ALT/ALLT/ASLT**
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM44C4100 ATR/ALTR/ALLTR/ASLTR**
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C4100A	I_{CC2}	-	2	mA
	KM44C4100AL			1	mA
	KM44C4100ALL			1	mA
	KM44C4100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM44C4100A/AL/ALL/ASL-6			80	mA
	KM44C4100A/AL/ALL/ASL-7			70	mA
	KM44C4100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM44C4100A	I_{CC5}	-	1	mA
	KM44C4100AL			300	μA
	KM44C4100ALL			200	μA
	KM44C4100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C4100A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}≦min~300ns	KM44C4100AL	I_{CC7}	-	400	μA
	KM44C4100ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_4=V_{CC}-0.2V, 0.2V or Open	KM44C4100ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

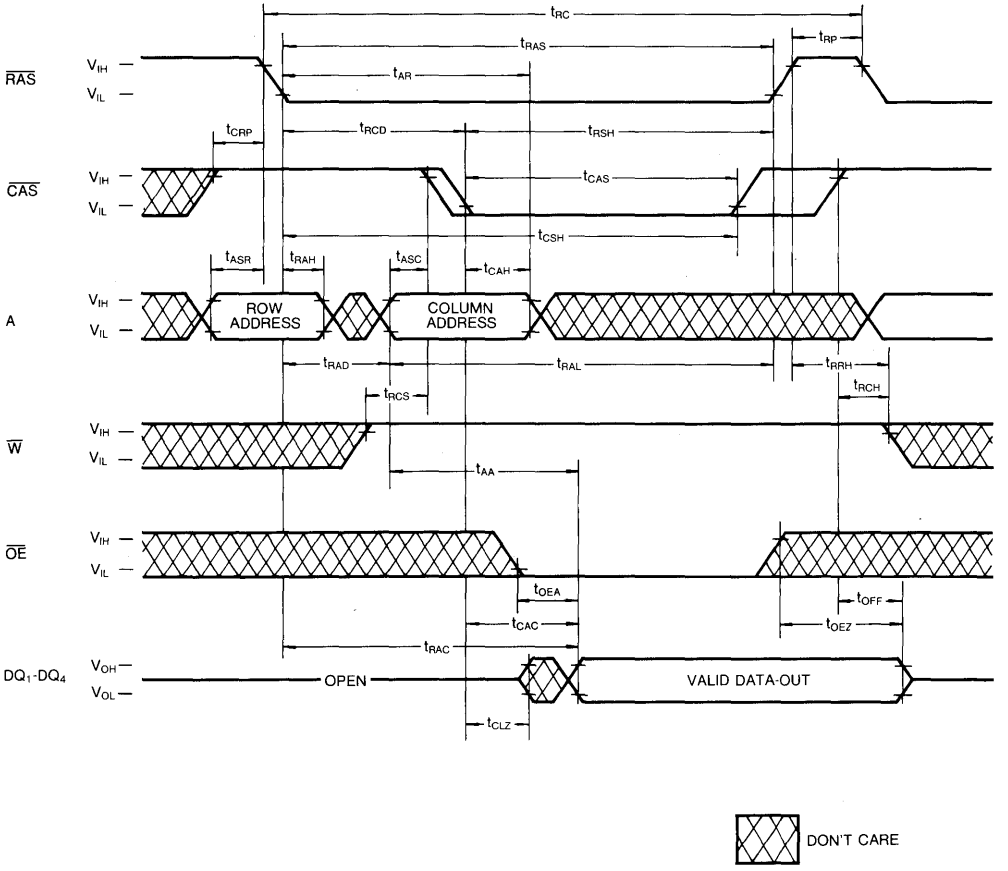
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

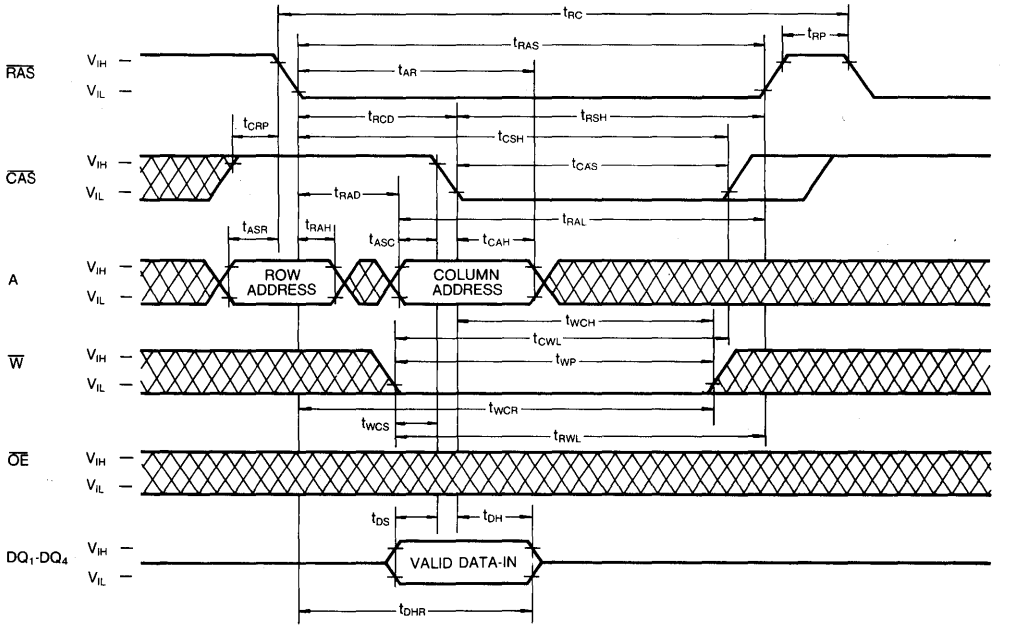
TIMING DIAGRAMS

READ CYCLE

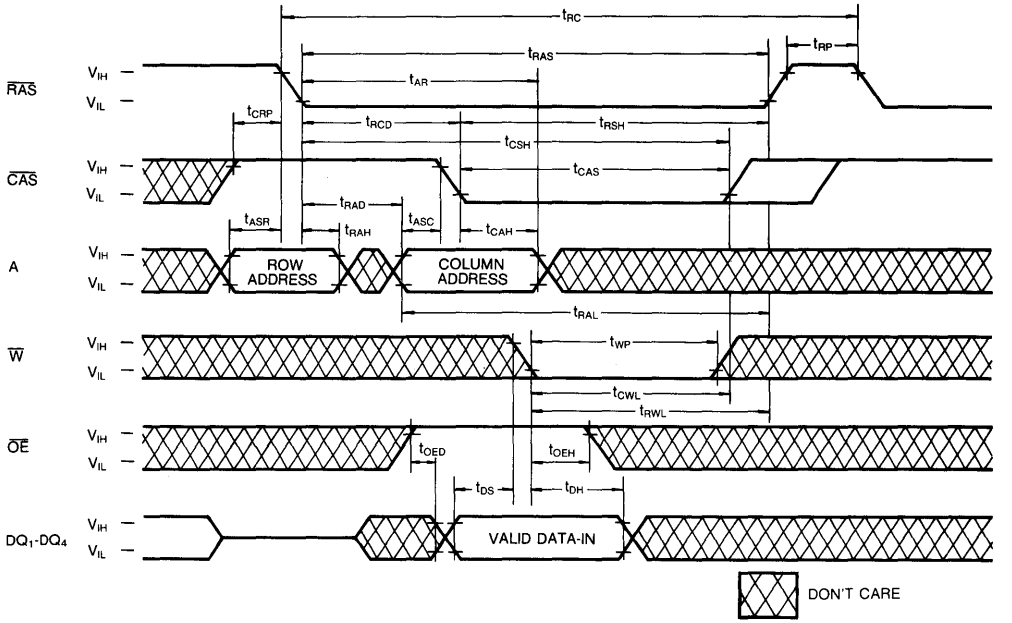


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



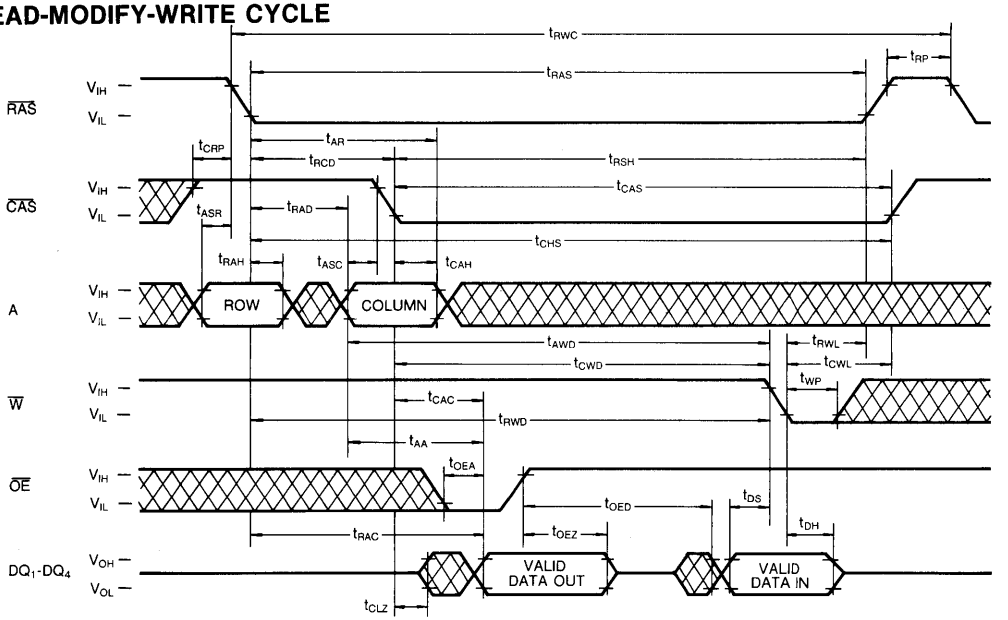
WRITE CYCLE (OE CONTROLLED WRITE)



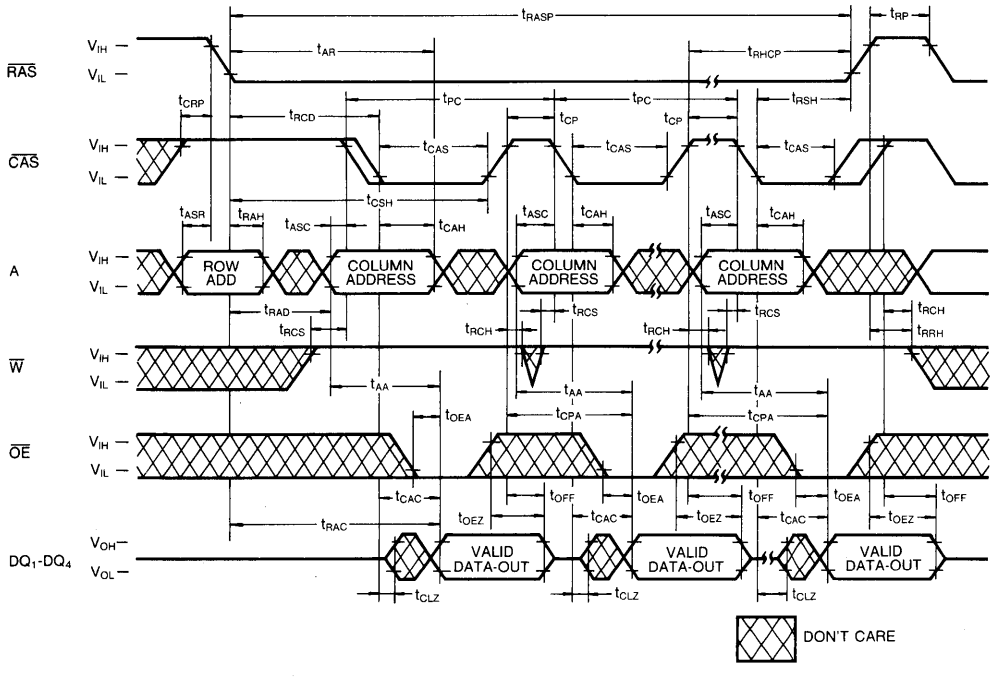
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



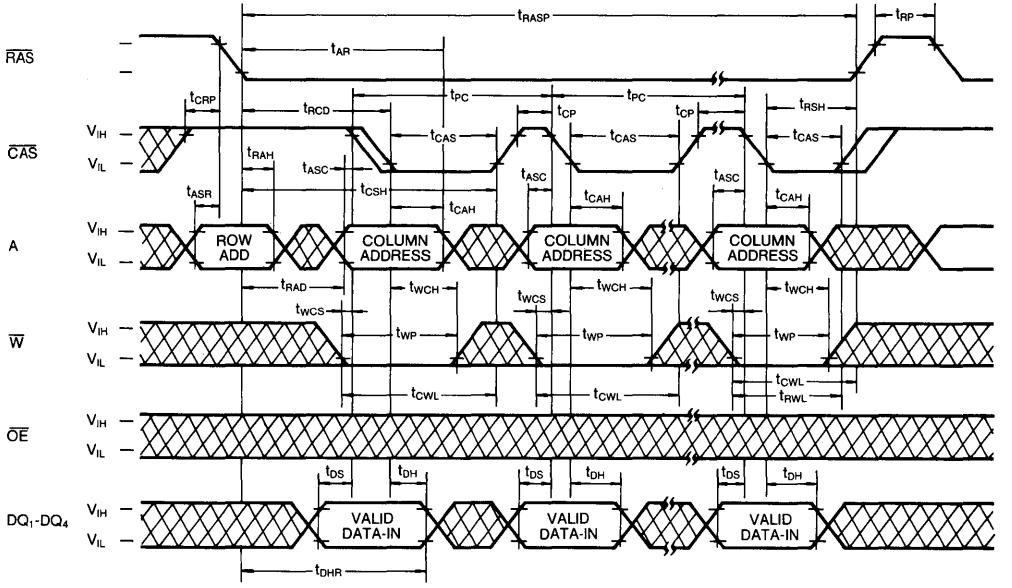
FAST PAGE MODE READ CYCLE



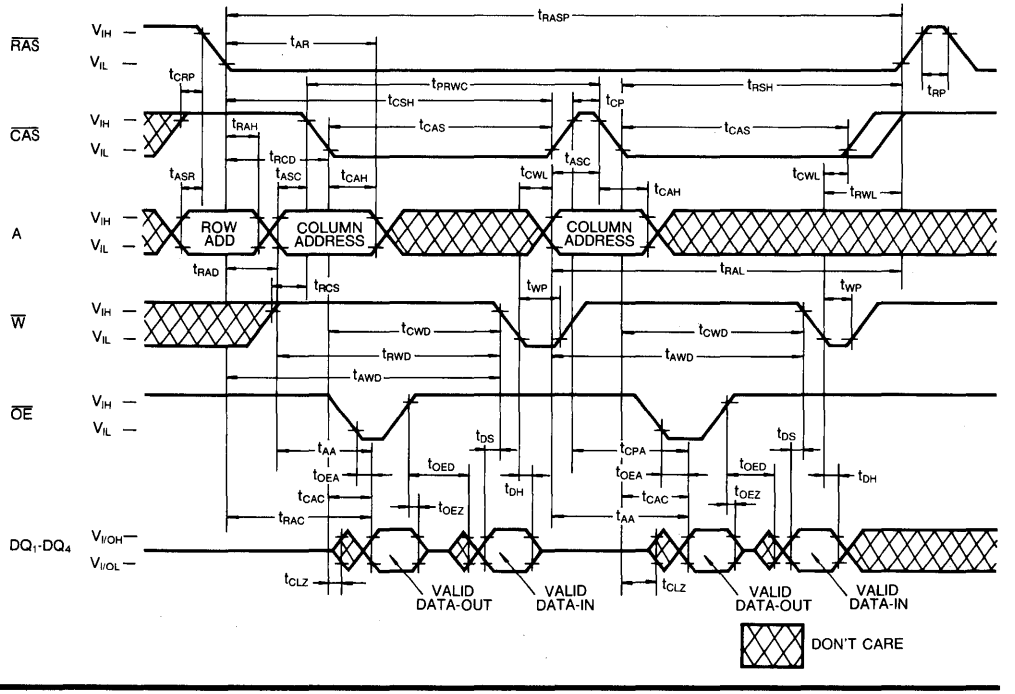
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



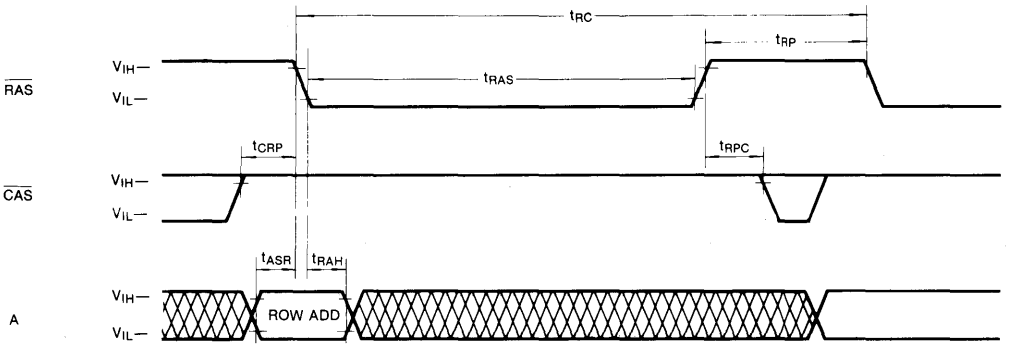
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

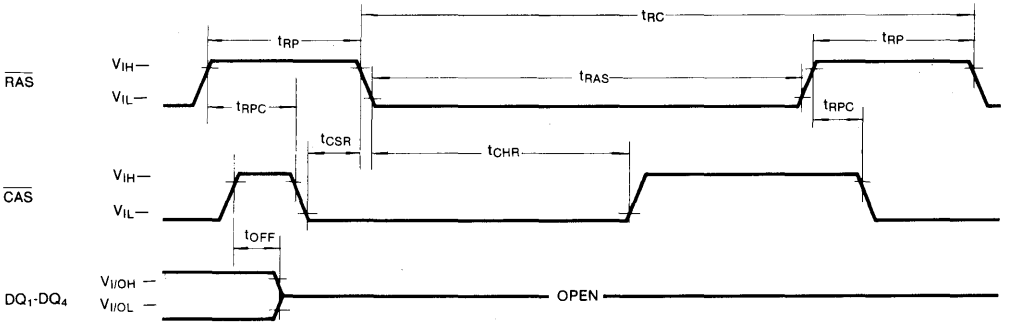
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



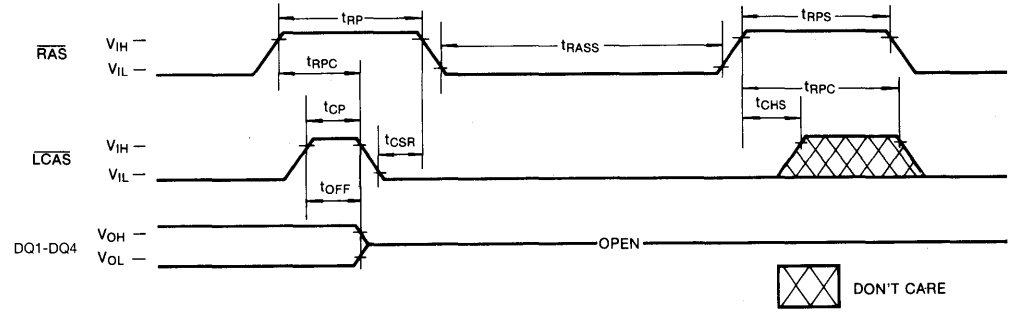
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



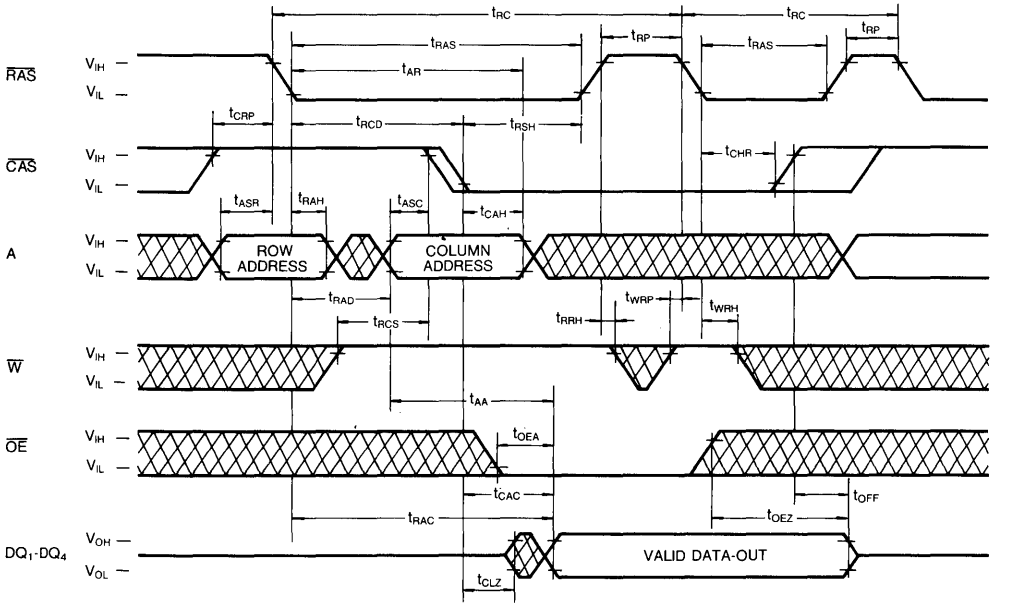
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

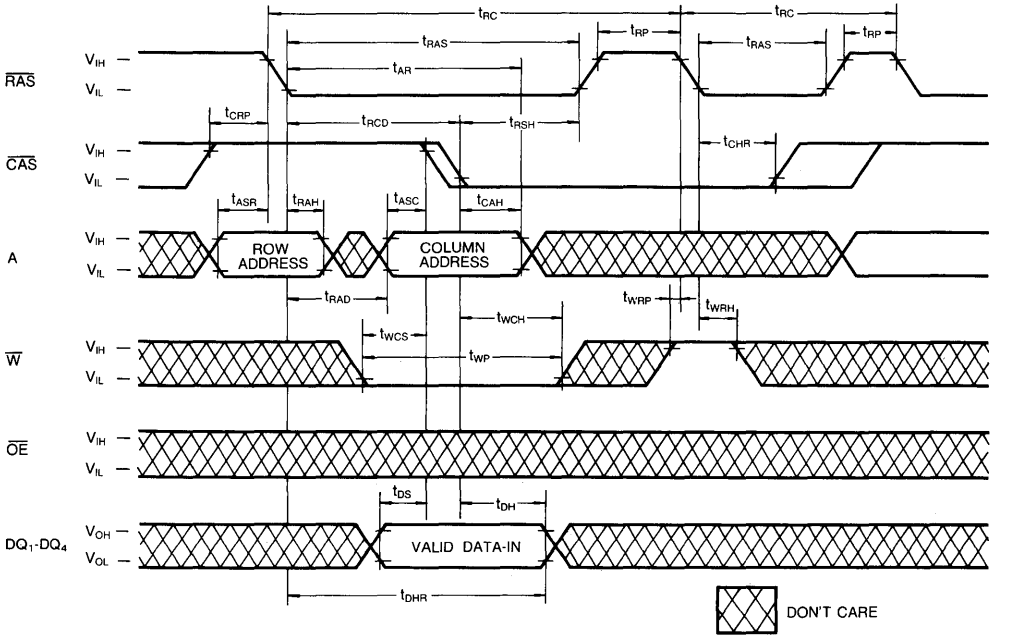


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

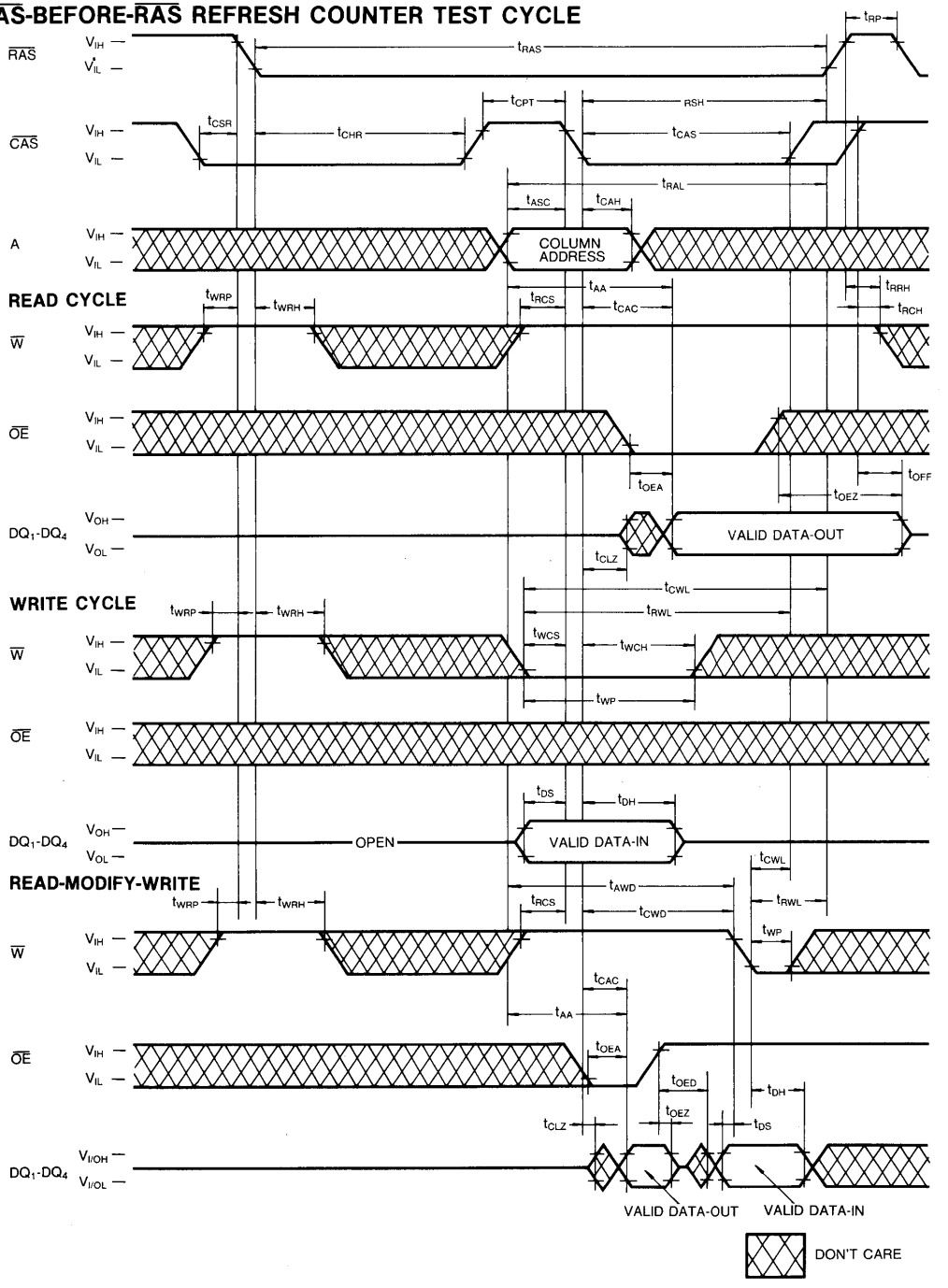


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

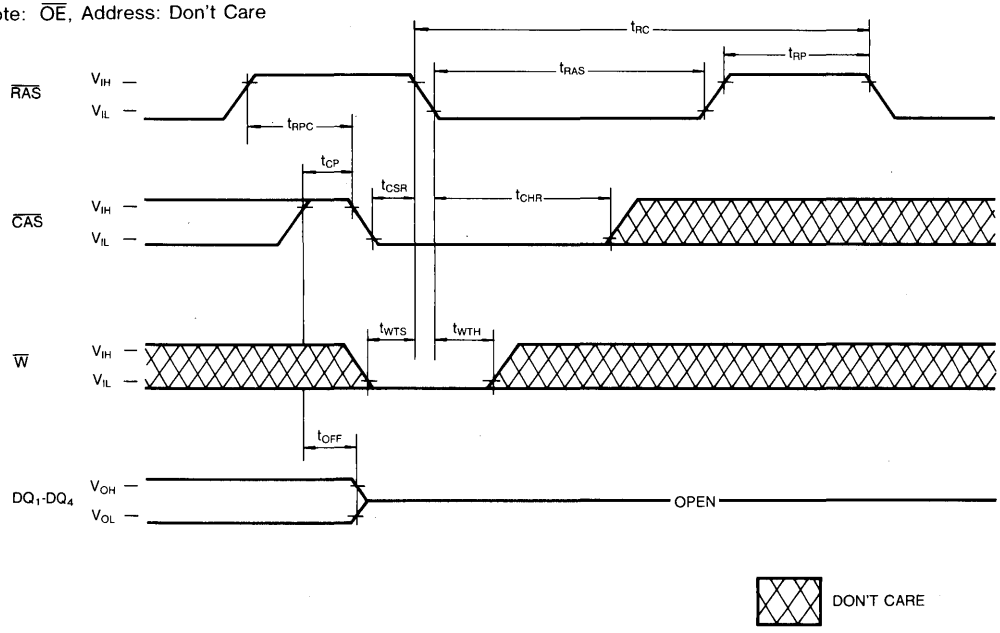


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



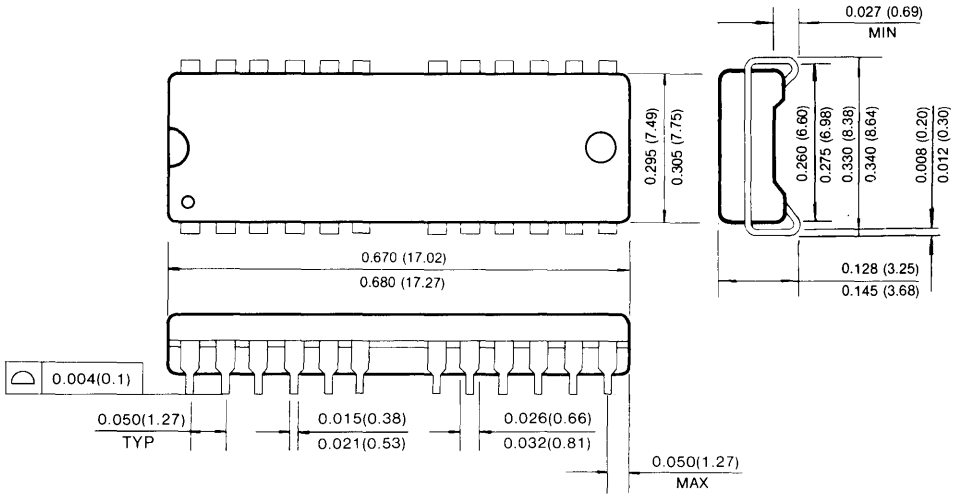
TEST MODE DESCRIPTION

The KM44C4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

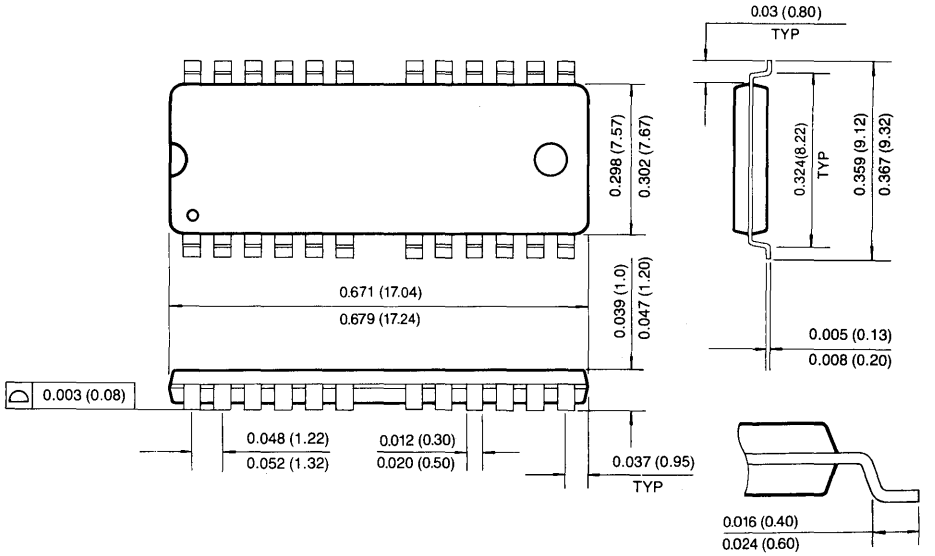
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



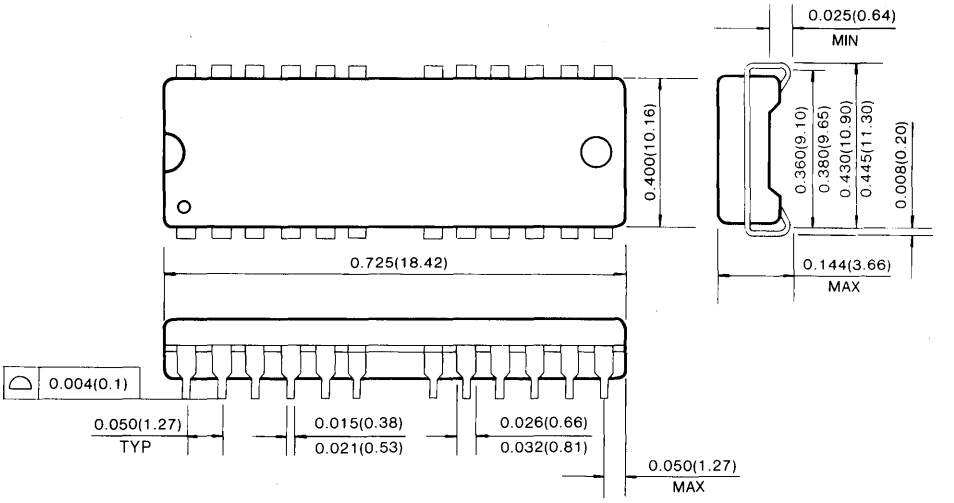
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



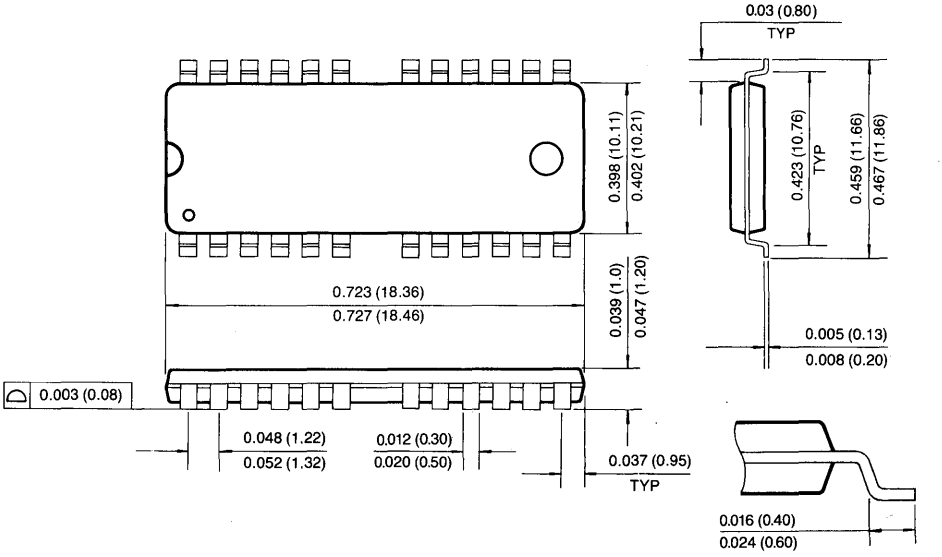
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48C2000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double+5.0V ± 10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

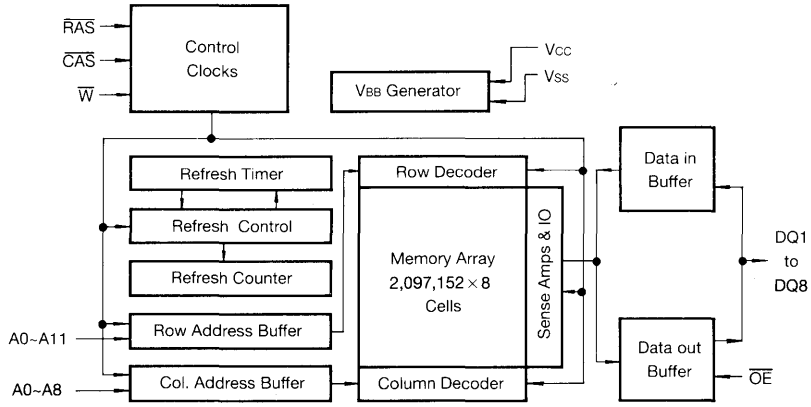
The Samsung KM48C2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

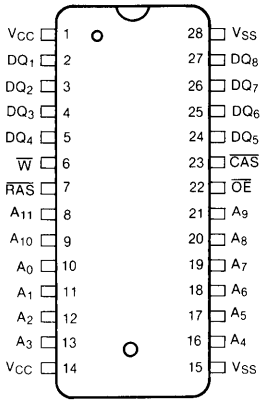
The KM48C2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

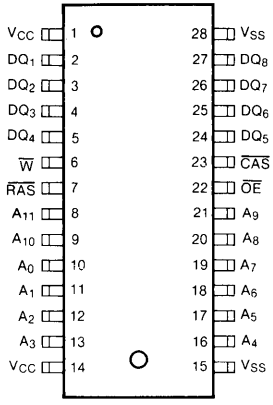


PIN CONFIGURATION (Top Views)

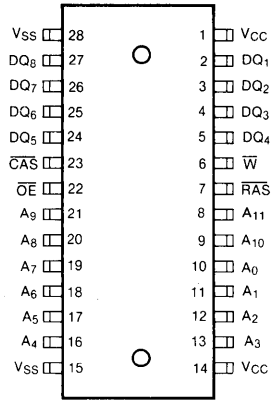
• KM48C2000 AJ/ALJ/ALLJ/ASLJ



• KM48C2000 AT/ALT/ALLT/ASLT



• KM48C2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2000A	I_{CC2}	-	2	mA
	KM48C2000AL			1	mA
	KM48C2000ALL			1	mA
	KM48C2000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM48C2000A/AL/ALL/ASL-6			70	mA
	KM48C2000A/AL/ALL/ASL-7			60	mA
	KM48C2000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2000A	I_{CC5}	-	1	mA
	KM48C2000AL			300	μA
	KM48C2000ALL			200	μA
	KM48C2000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM48C2000A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM48C2000A/AL/ALL/ASL-6			80	mA
	KM48C2000A/AL/ALL/ASL-7			70	mA
	KM48C2000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}≦300ns	KM48C2000AL	I_{CC7}	-	450	μA
	KM48C2000ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2000ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to W delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

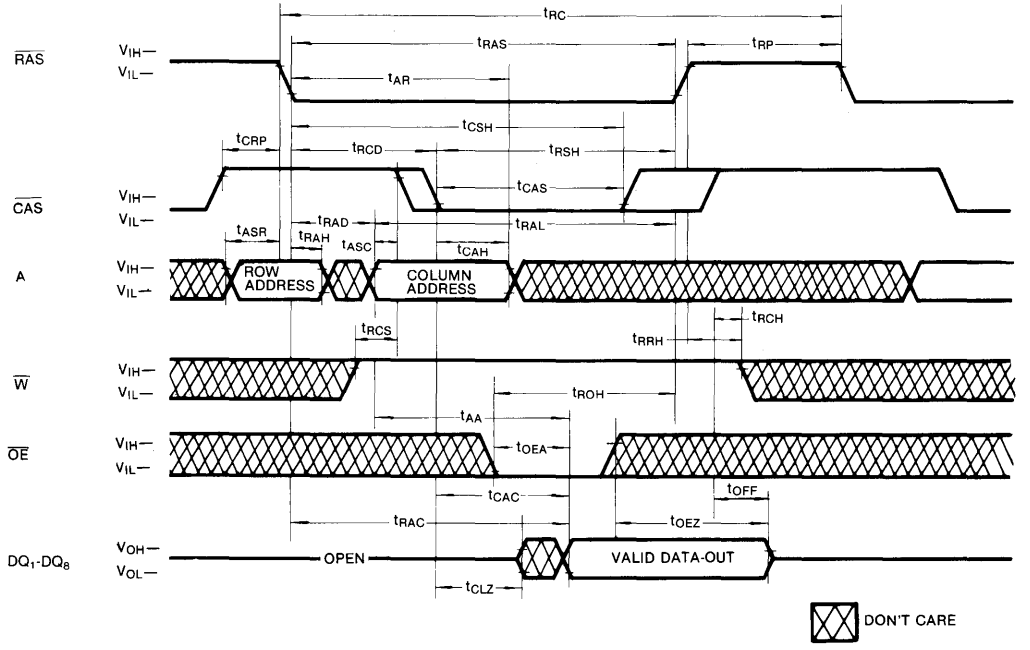
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

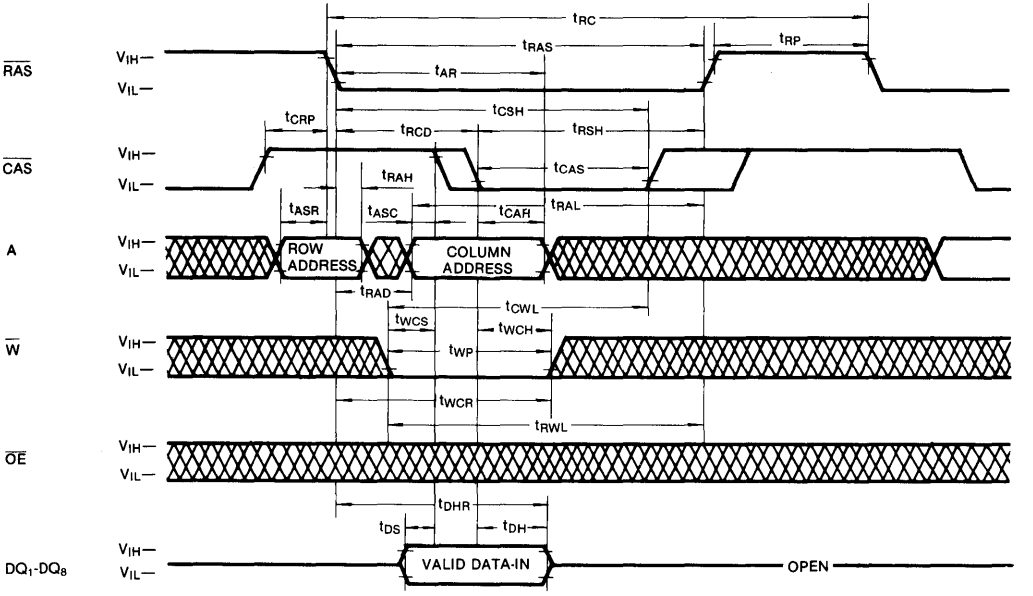
TIMING DIAGRAMS

READ CYCLE

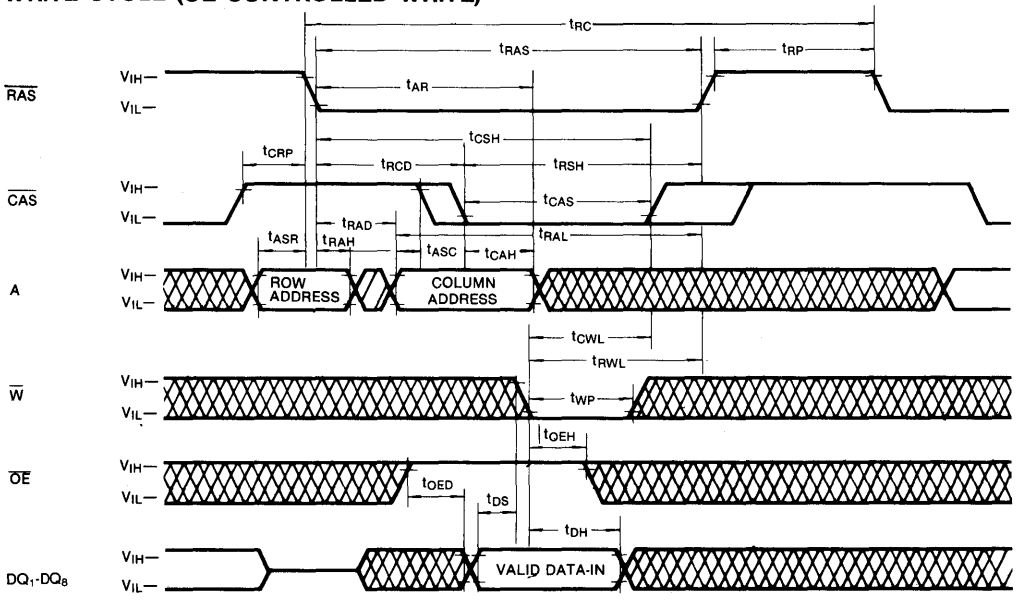


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



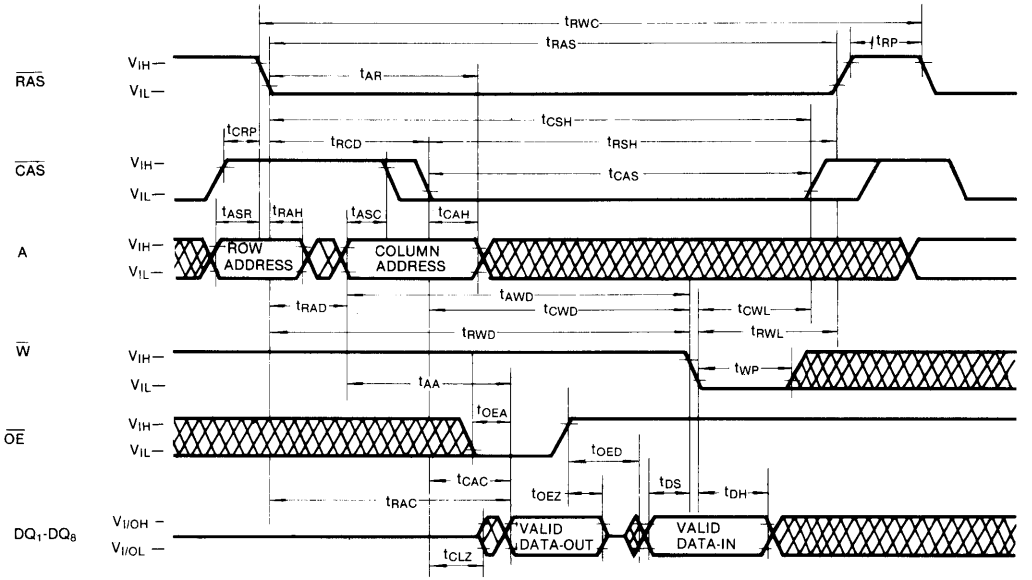
WRITE CYCLE (OE CONTROLLED WRITE)



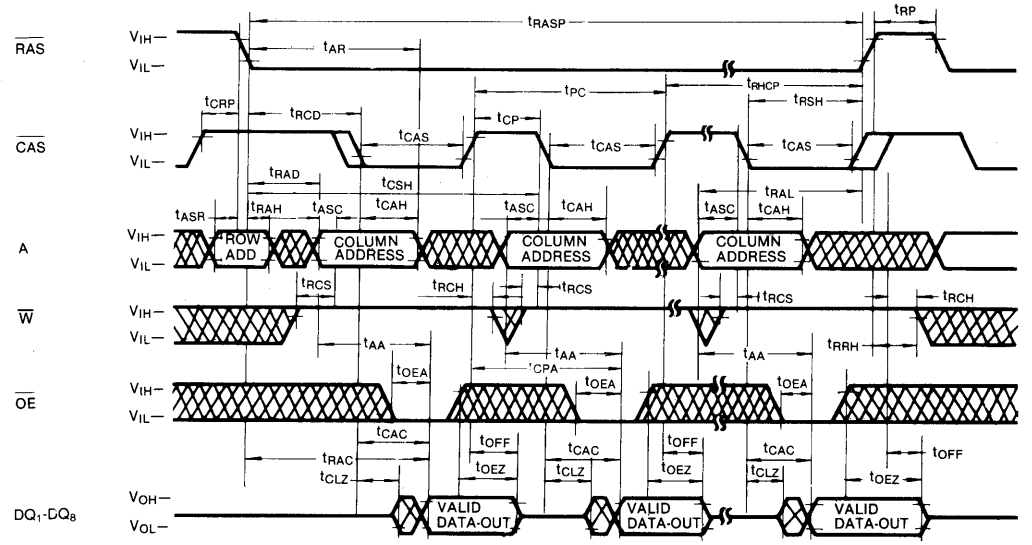
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



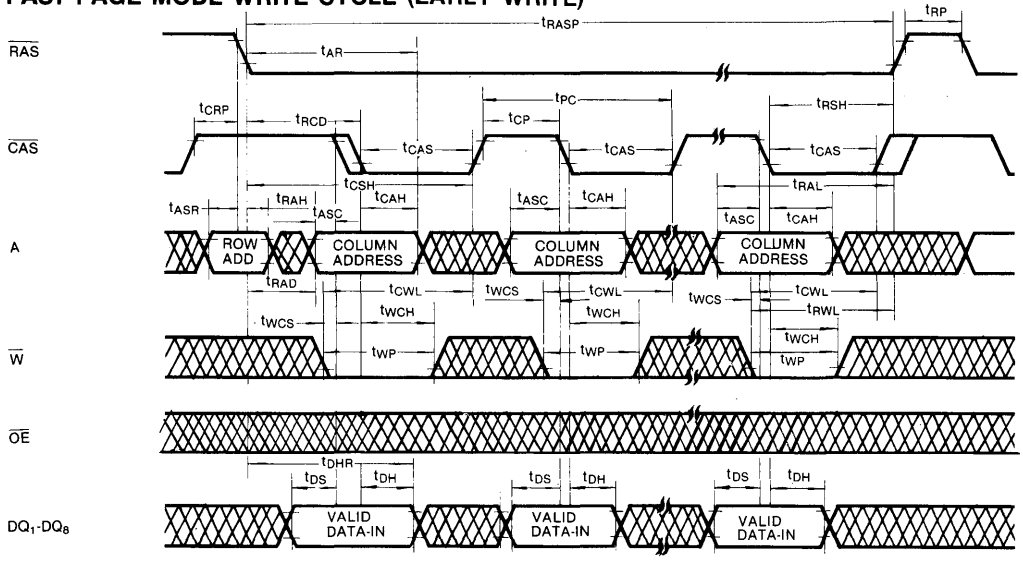
FAST PAGE MODE READ CYCLE



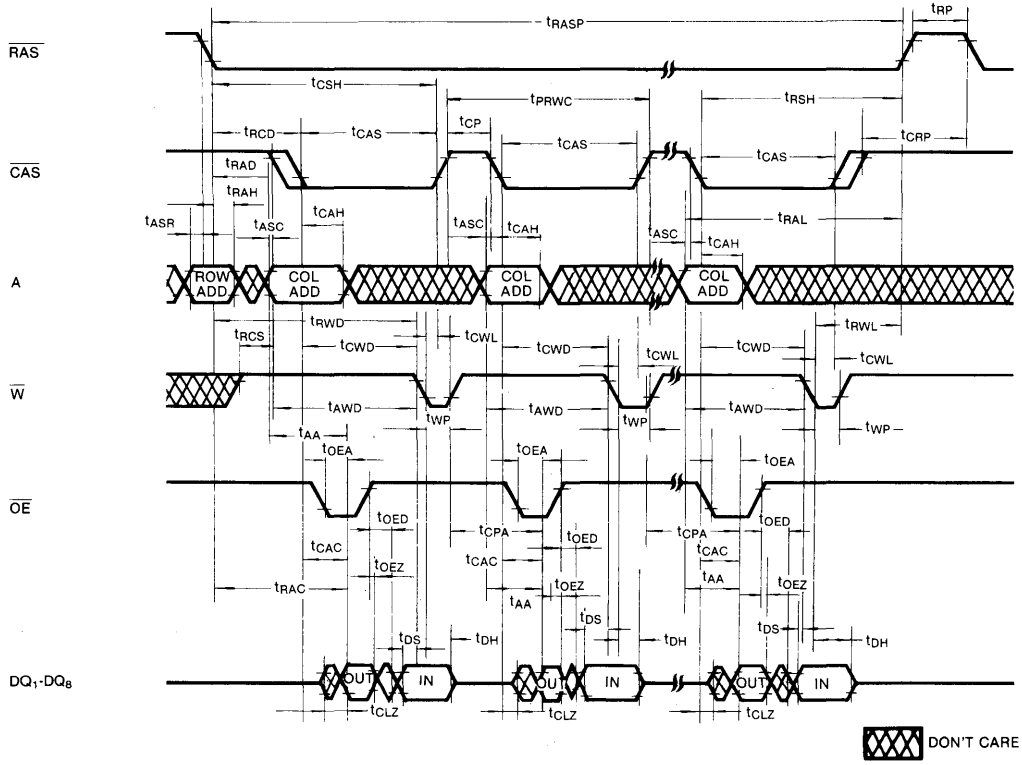
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



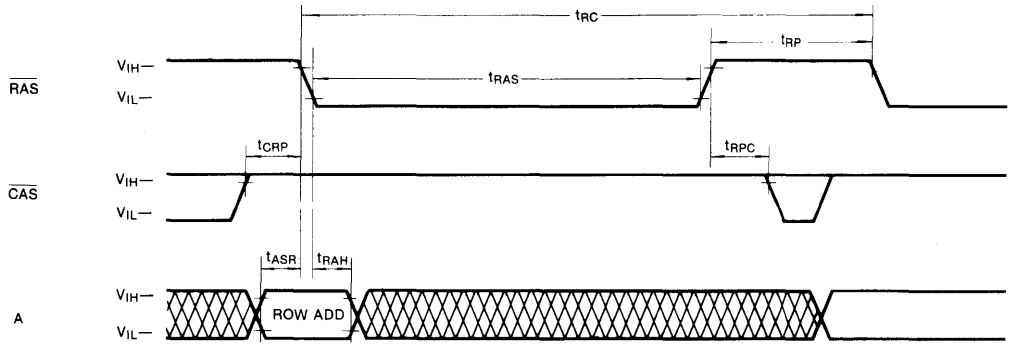
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

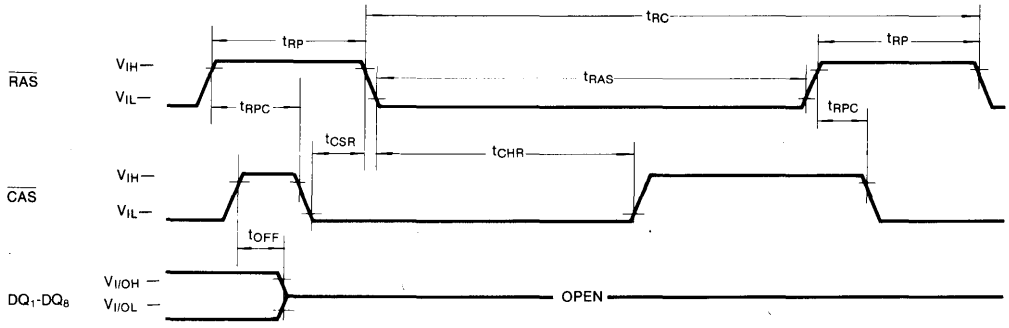
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



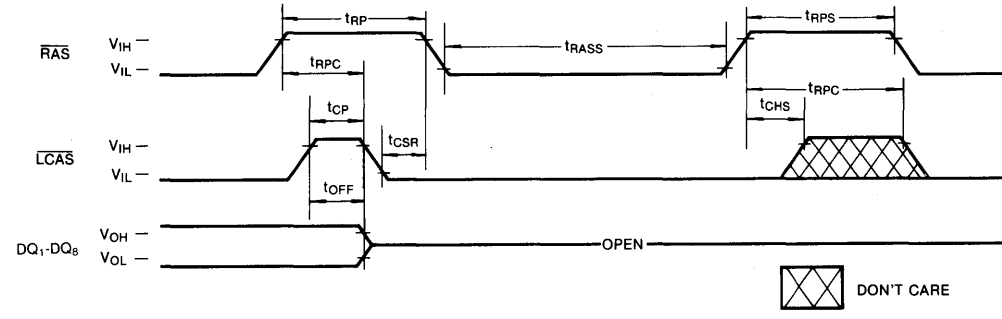
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



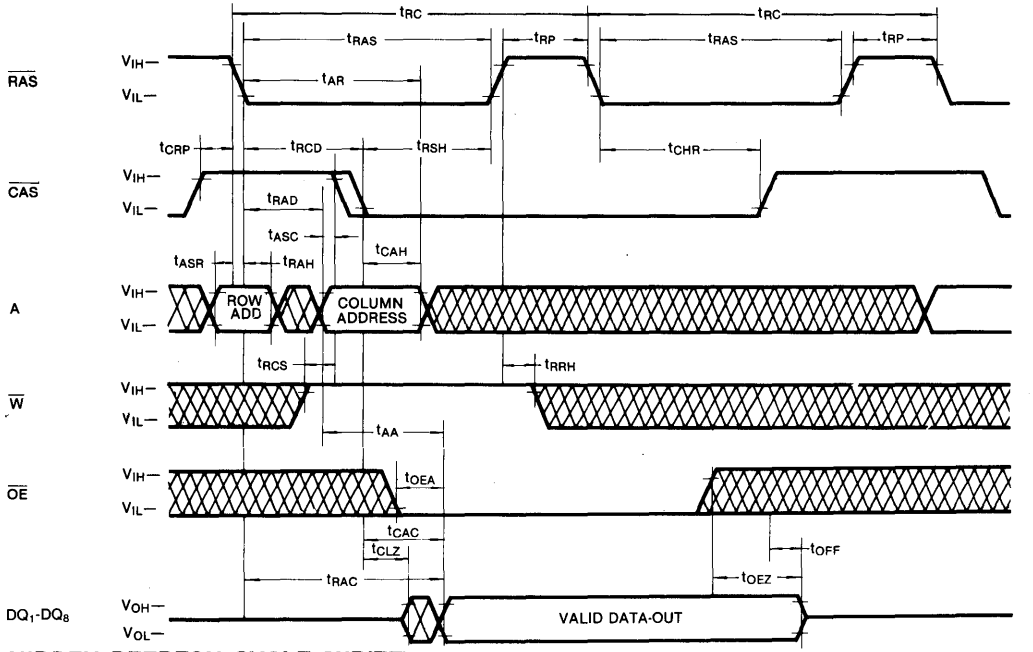
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

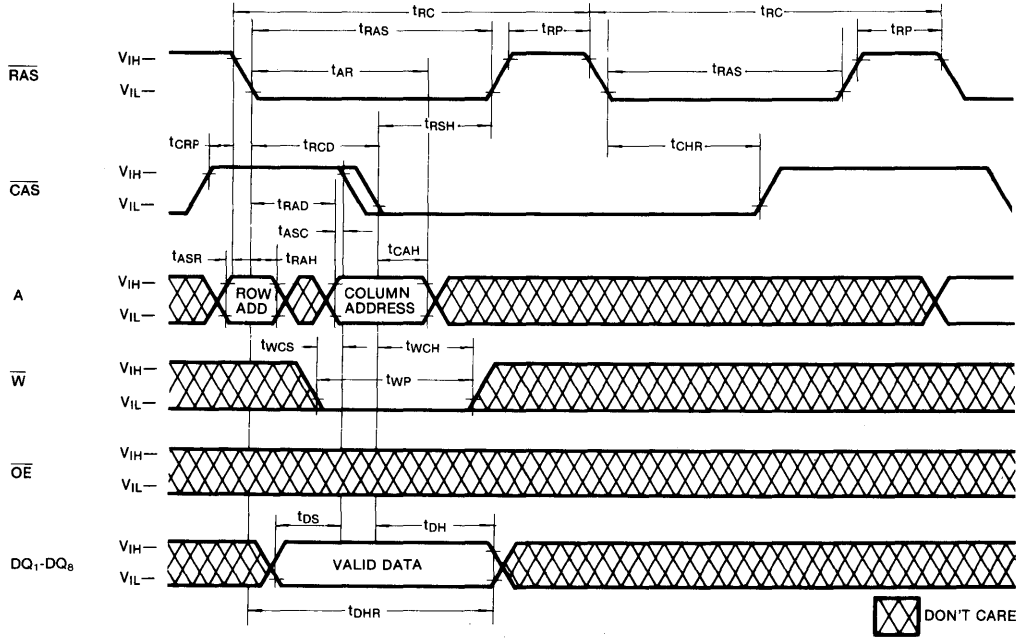


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

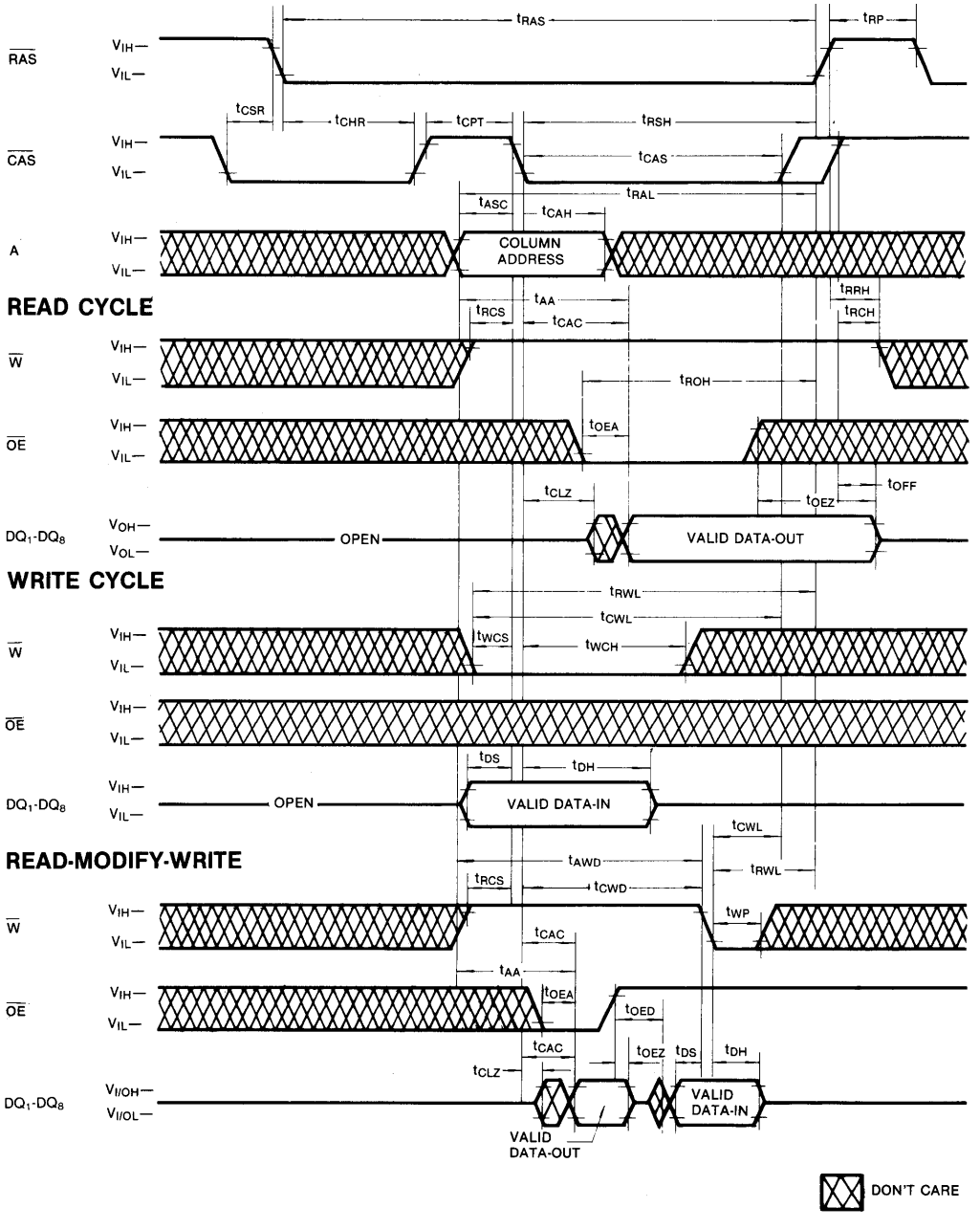


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

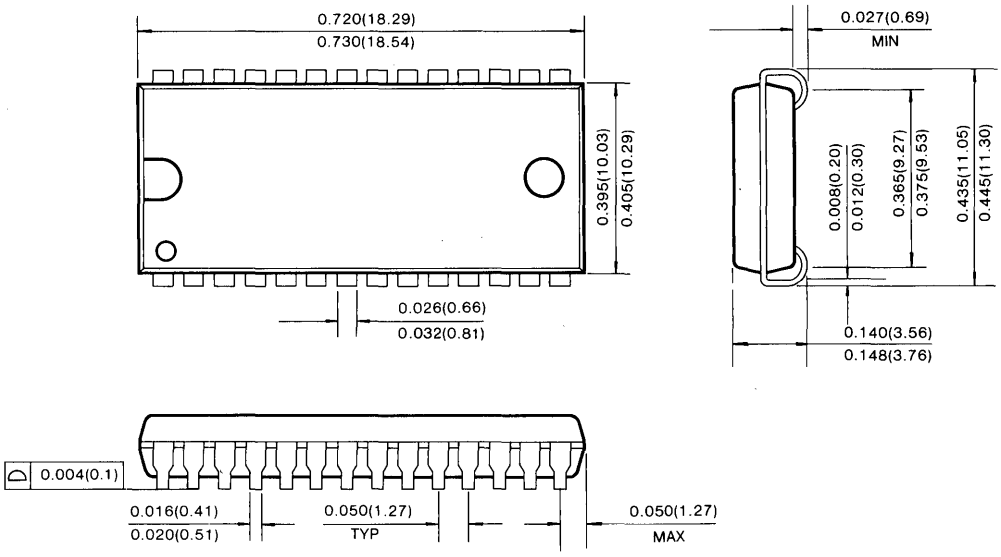
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

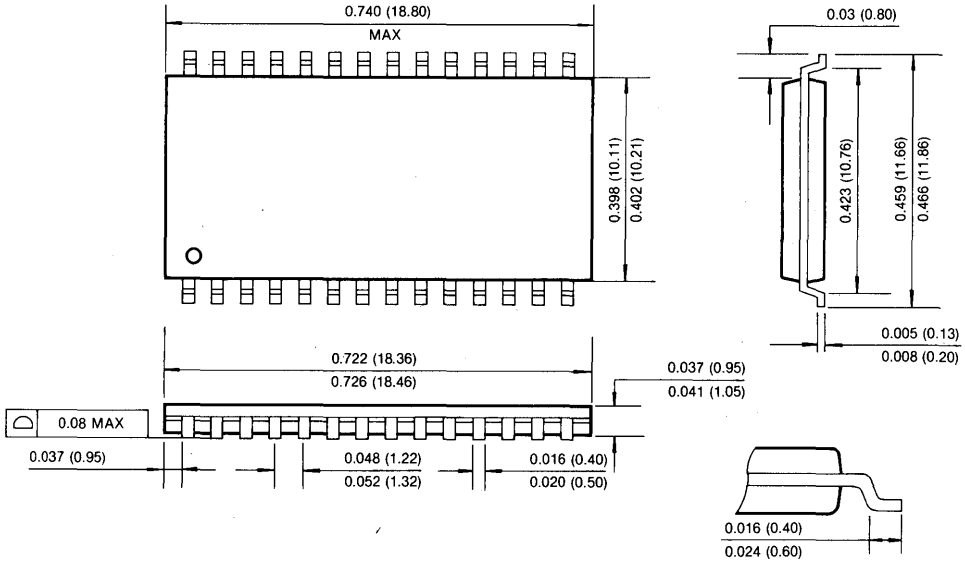
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C2100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double+5.0V ± 10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

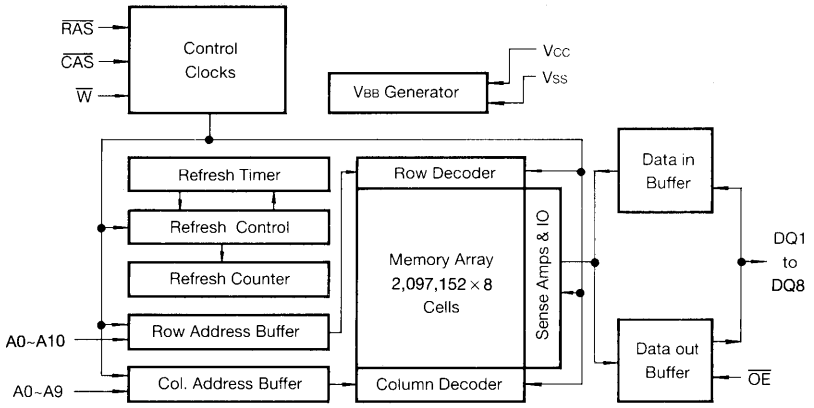
The Samsung KM48C2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

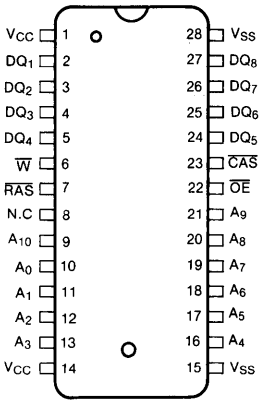
The KM48C2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

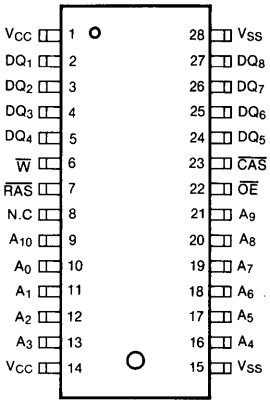


PIN CONFIGURATION (Top Views)

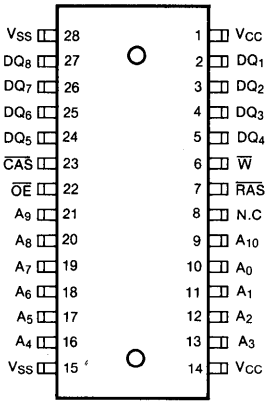
• KM48C2100 AJ/ALJ/ALLJ/ASLJ



• KM48C2100 AT/ALT/ALLT/ASLT



• KM48C2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ1~8	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC1}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C2100A	I_{CC2}	-	2	mA
	KM48C2100AL			1	mA
	KM48C2100ALL			1	mA
	KM48C2100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC3}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC4}	-	90	mA
	KM48C2100A/AL/ALL/ASL-6			80	mA
	KM48C2100A/AL/ALL/ASL-7			70	mA
	KM48C2100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C2100A	I_{CC5}	-	1	mA
	KM48C2100AL			300	μA
	KM48C2100ALL			200	μA
	KM48C2100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48C2100A/AL/ALL/ASL-5	I_{CC6}	-	110	mA
	KM48C2100A/AL/ALL/ASL-6			100	mA
	KM48C2100A/AL/ALL/ASL-7			90	mA
	KM48C2100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}≦300ns	KM48C2100AL	I_{CC7}	-	400	μA
	KM48C2100ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{CC}-0.2V or 0.2V DQ_1-DQ_8=V_{CC}-0.2V, 0.2V or Open	KM48C2100ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1-DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ pulse width(Fast Page mode)	t_{RASP}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		13		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

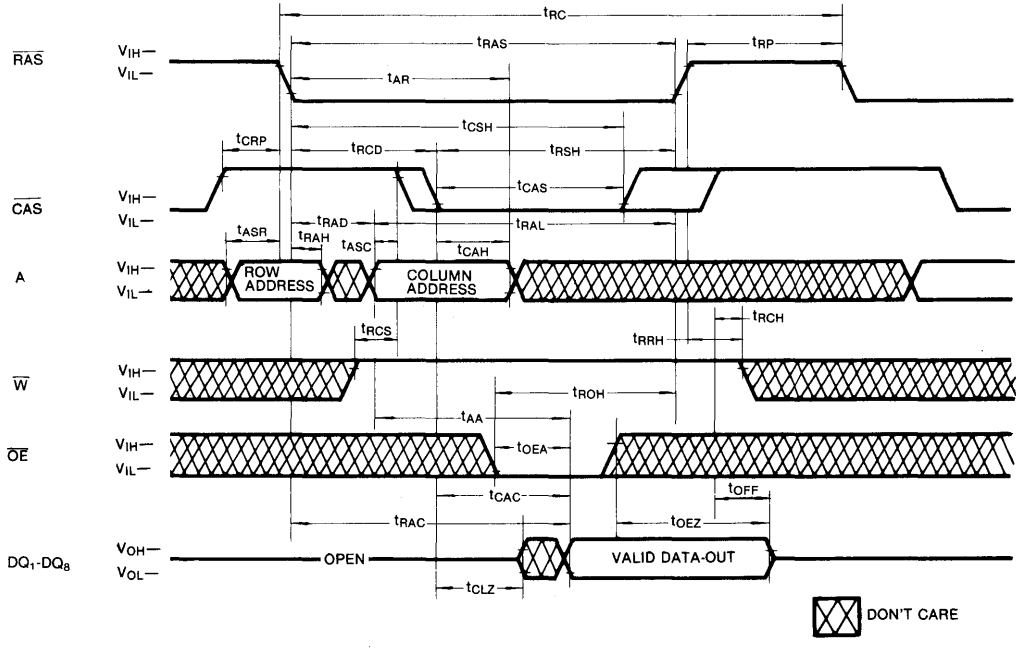
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

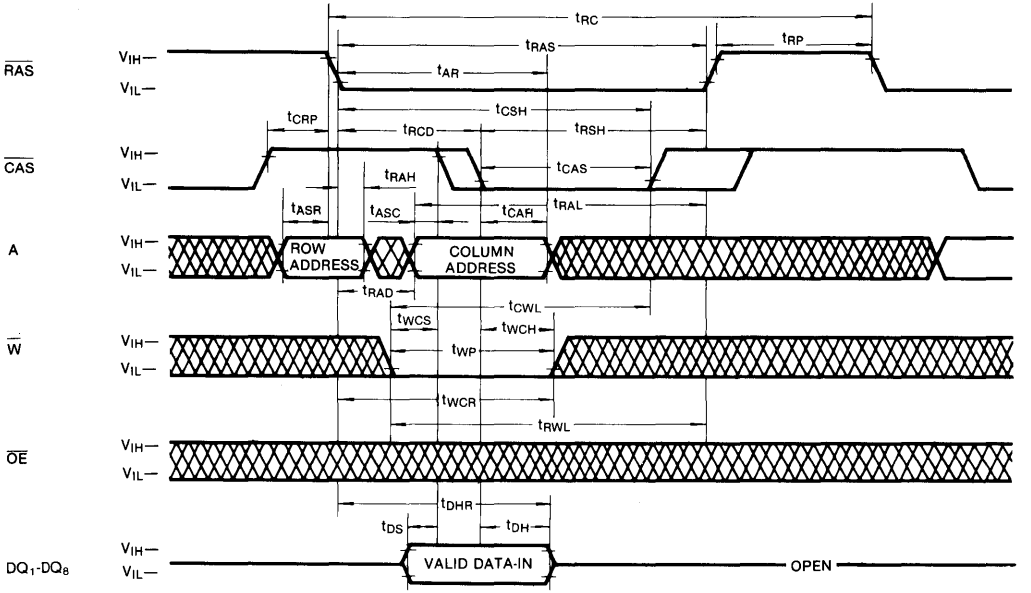
READ CYCLE



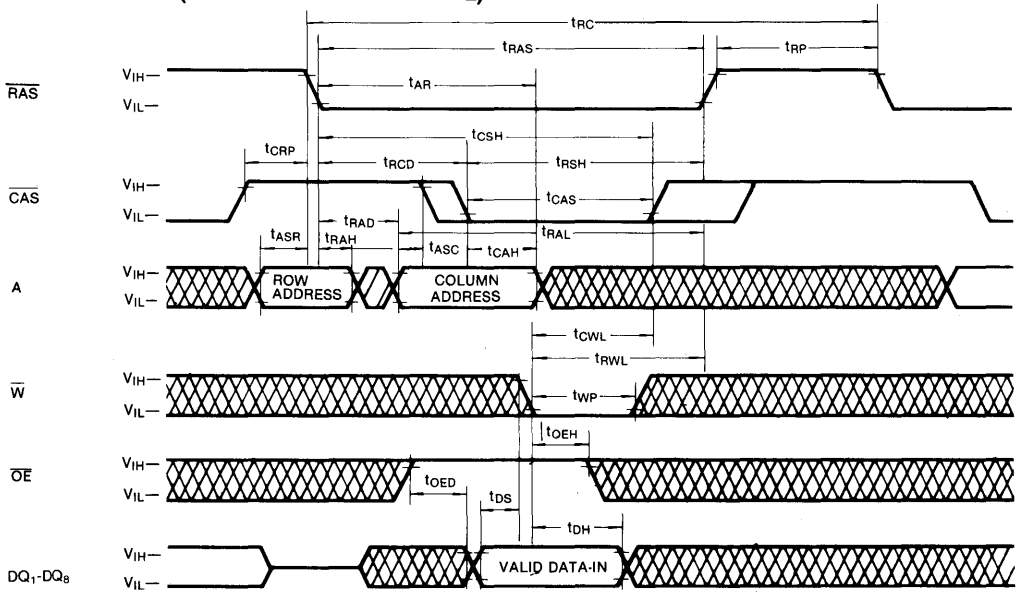
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



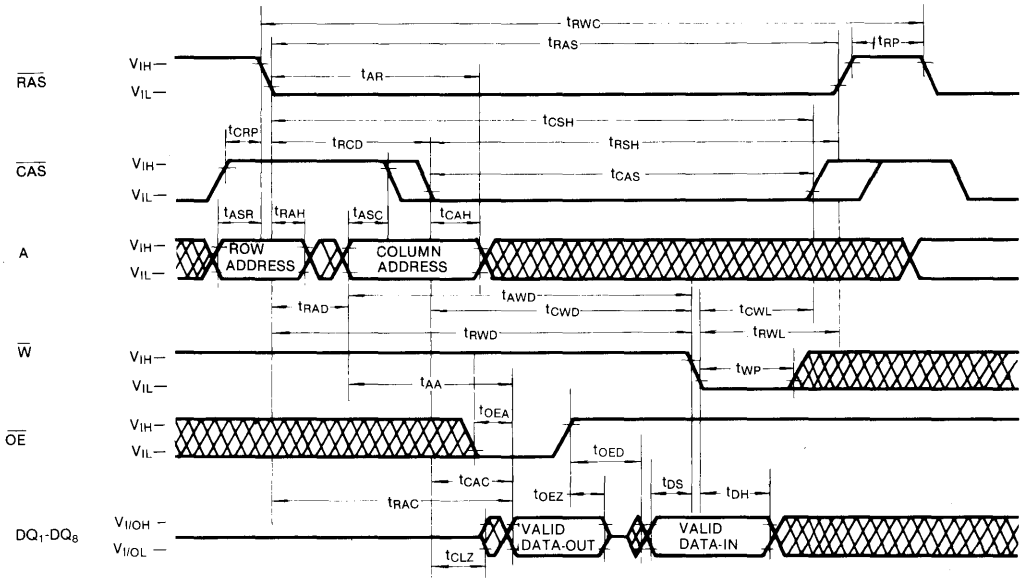
WRITE CYCLE (OE CONTROLLED WRITE)



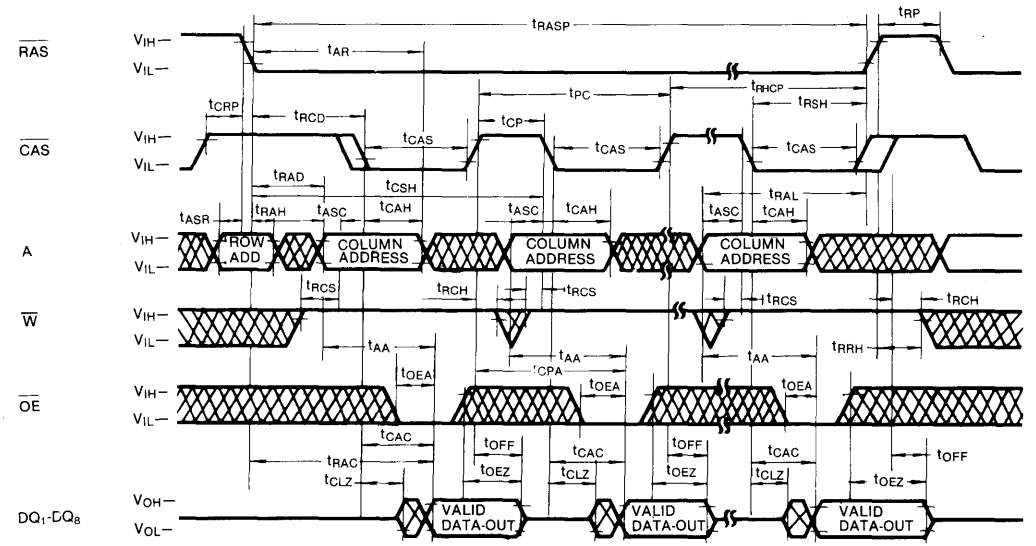
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



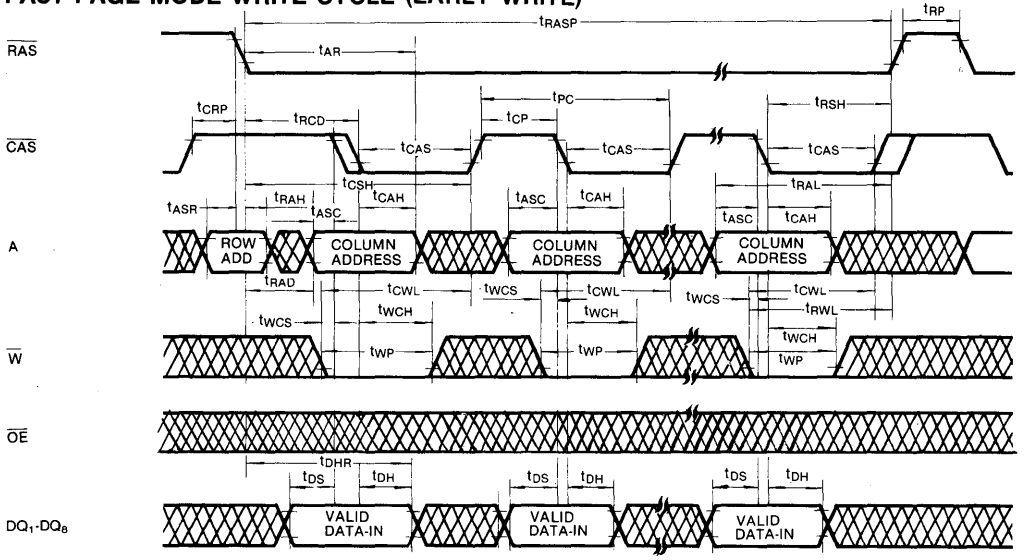
FAST PAGE MODE READ CYCLE



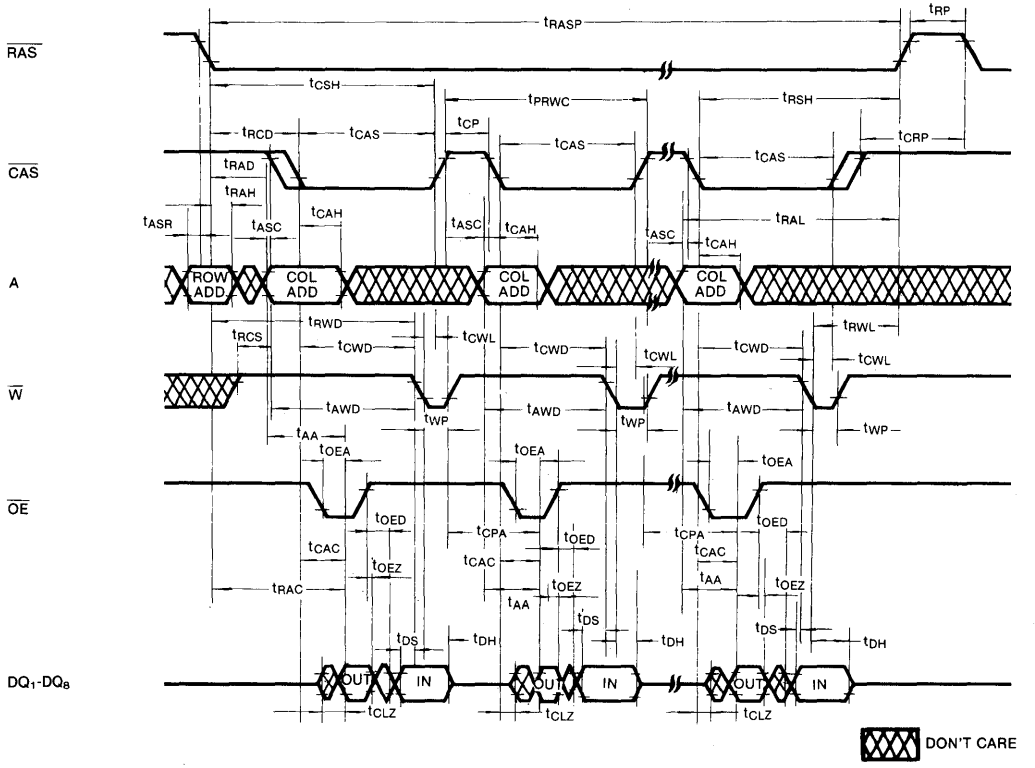
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



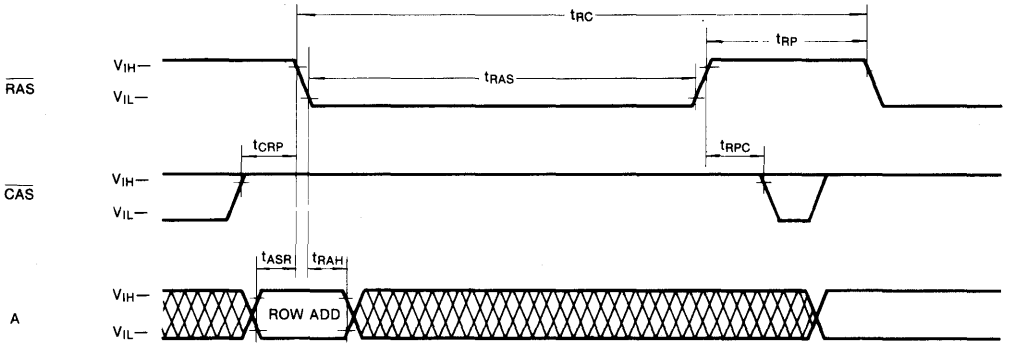
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

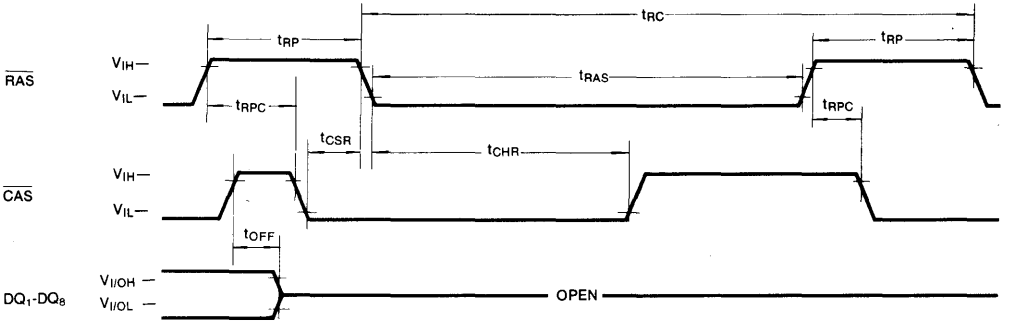
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



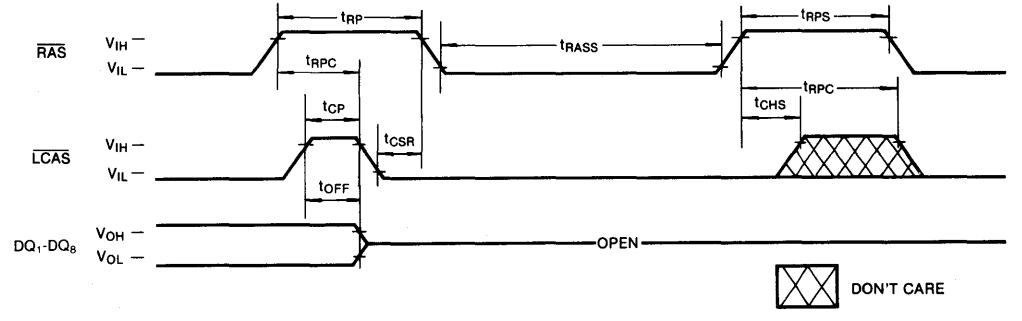
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



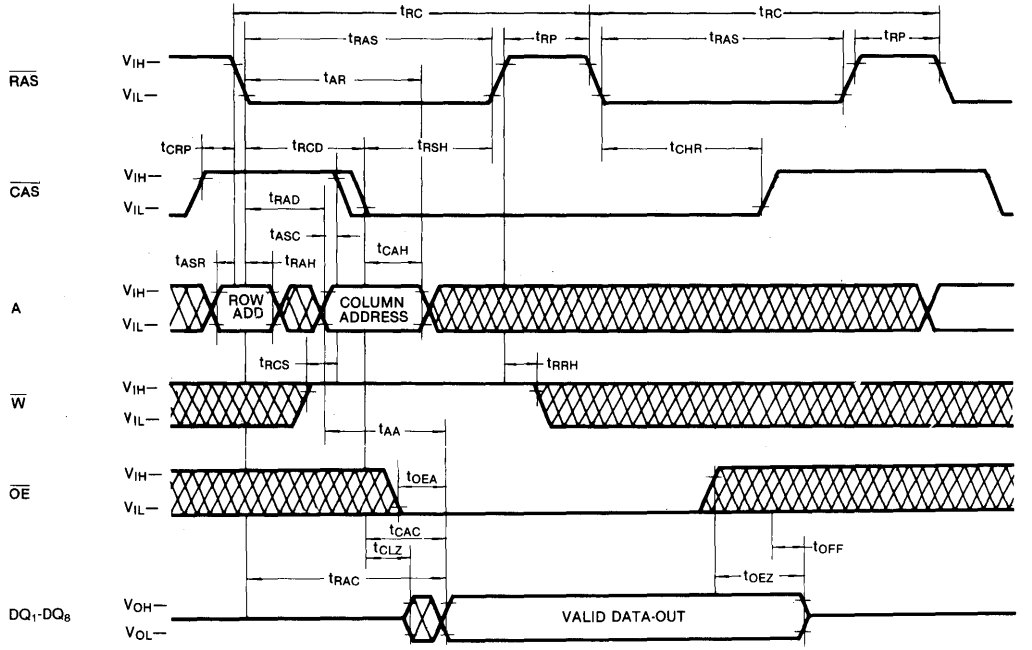
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

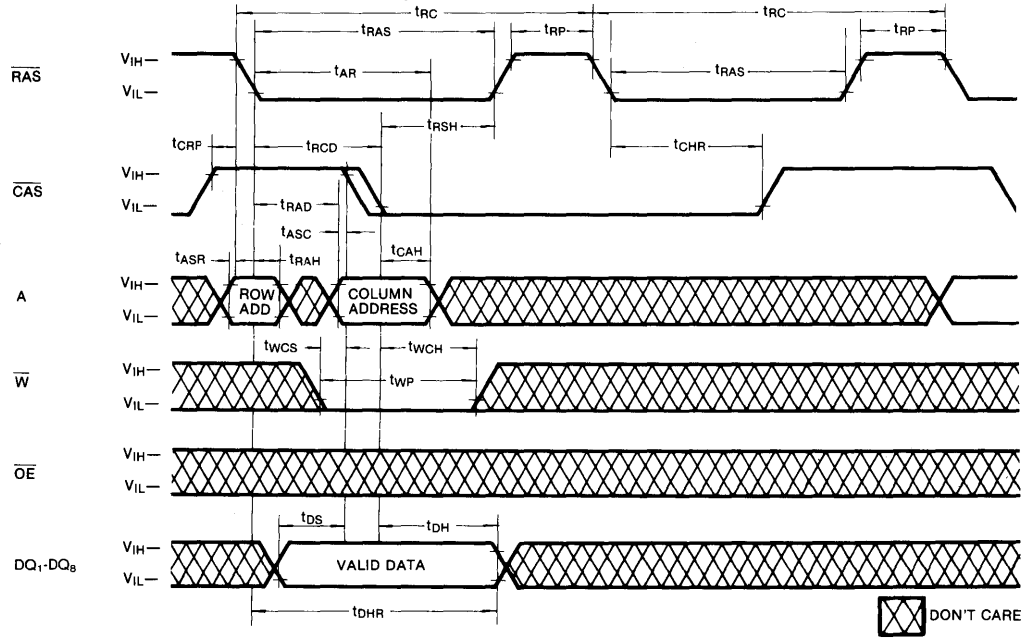


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



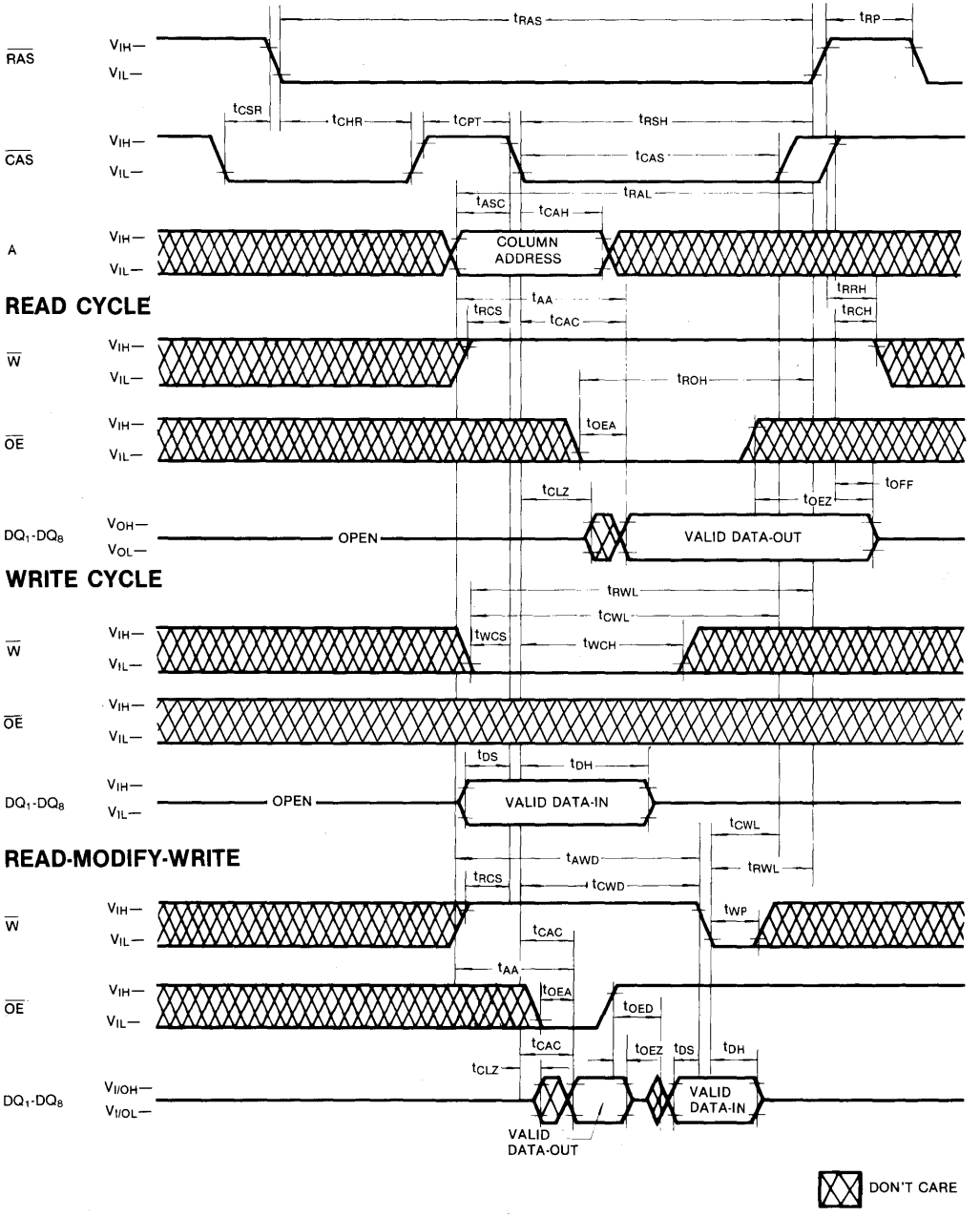
HIDDEN REFRESH CYCLE (WRITE)



SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

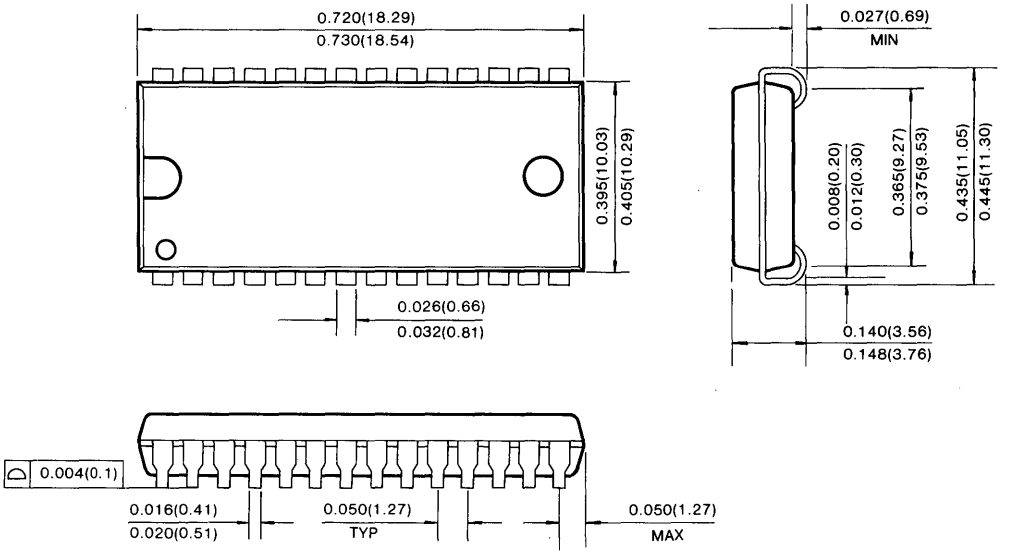
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

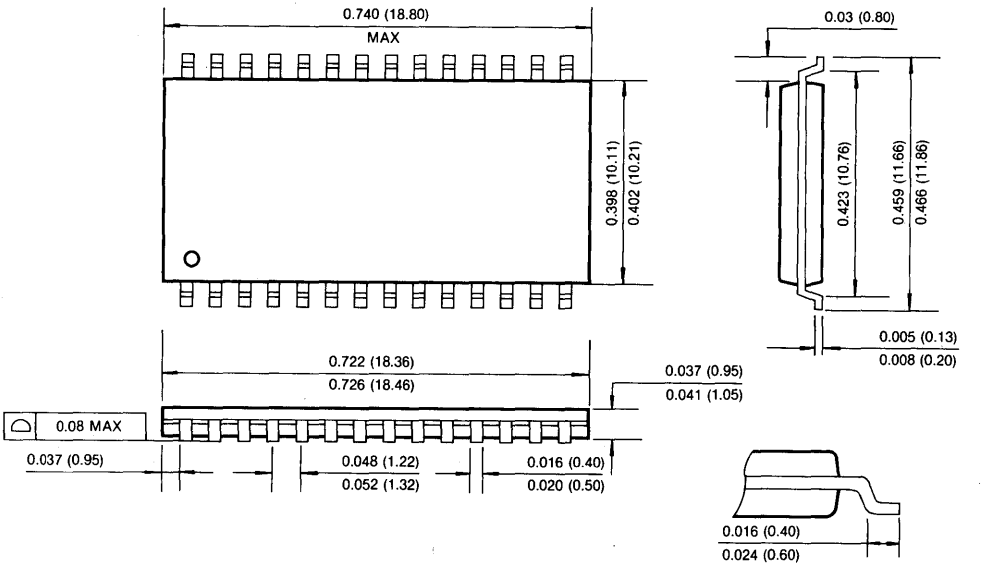
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



16M ×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41V16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41V16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41V16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Common I/O using Early Write**
- **Double+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh(Normal)**
- **4096 cycles/128ms refresh(Low power & Self Ref.)**
- **4096 cycles/256ms refresh(Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

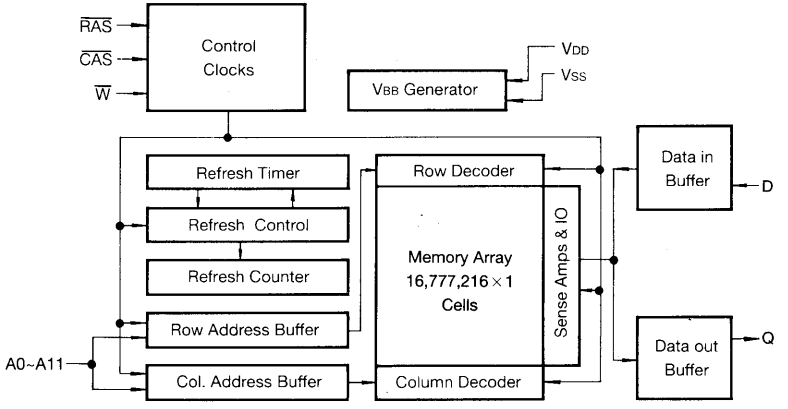
The Samsung KM41V16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit×1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41V16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

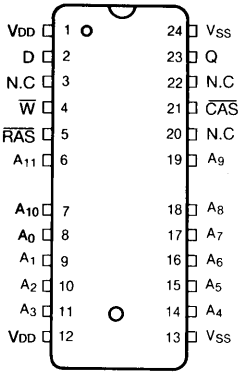
The KM41V16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



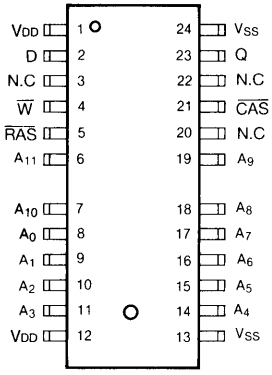
PIN CONFIGURATION (Top Views)

• **KM41V16000 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK**



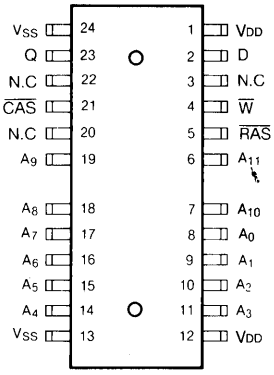
J : 400MIL
K : 300MIL

• **KM41V16000 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS**



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM41V16000 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR**



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power(+3.3V)
VDD	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC1}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM41V16000A	I_{CC2}	-	2	mA
	KM41V16000AL			1	mA
	KM41V16000ALL			1	mA
	KM41V16000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC3}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC4}	-	70	mA
	KM41V16000A/AL/ALL/ASL-7			60	mA
	KM41V16000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM41V16000A	I_{CC5}	-	1	mA
	KM41V16000AL			300	μA
	KM41V16000ALL			200	μA
	KM41V16000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41V16000A/AL/ALL/ASL-6	I_{CC6}	-	80	mA
	KM41V16000A/AL/ALL/ASL-7			70	mA
	KM41V16000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM41V16000AL	I_{CC7}	-	450	μA
	KM41V16000ASL			350	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V D, Q=V_{DD}-0.2V, 0.2V or Open	KM41V16000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	7	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ refresh)	t_{RASS}	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{RPS}	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHS}	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

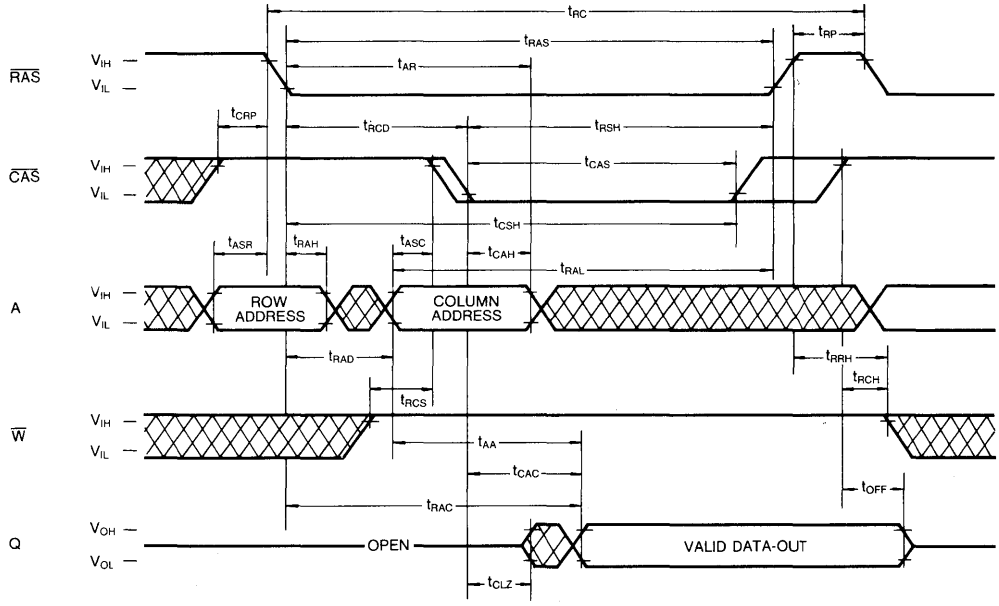
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		25		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	8
Fast Page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

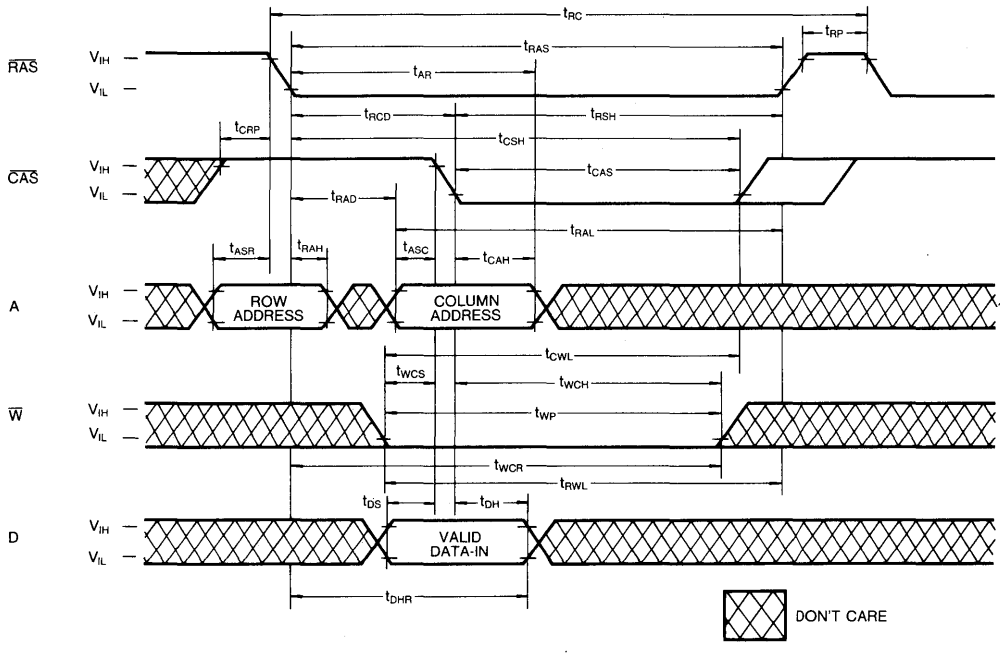
1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE

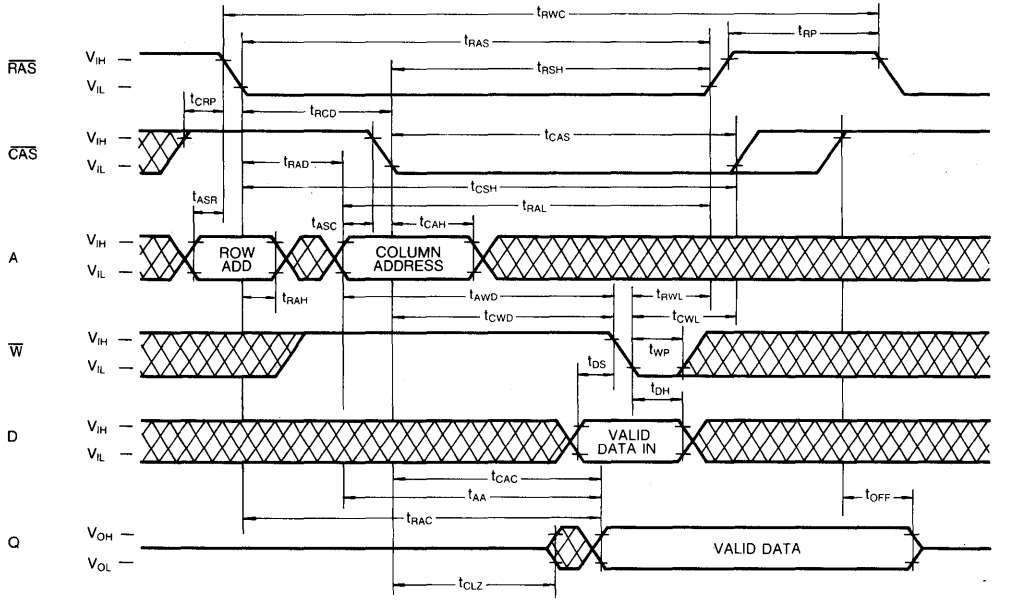


WRITE CYCLE (EARLY WRITE)

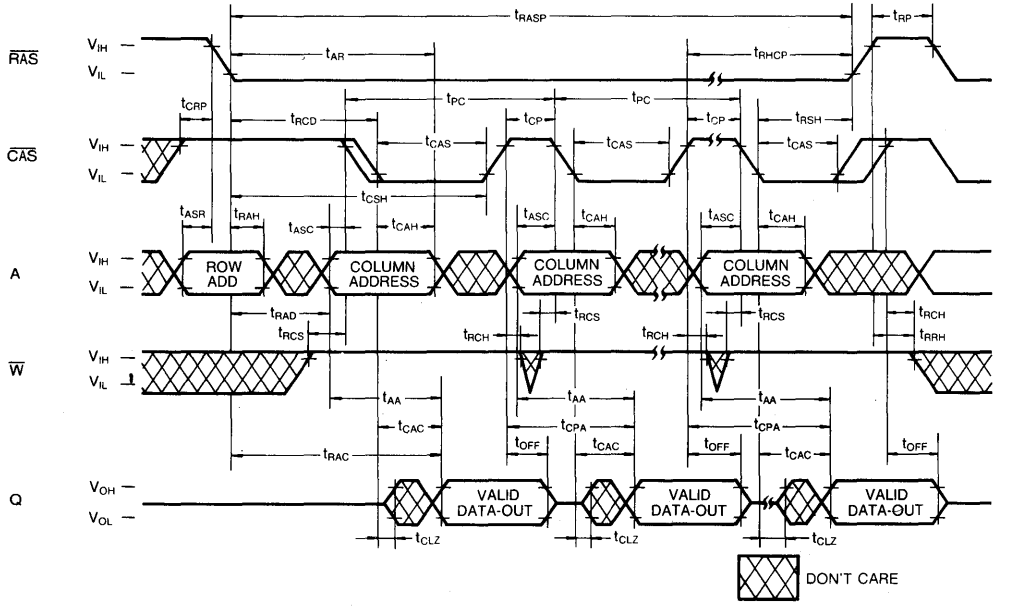


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

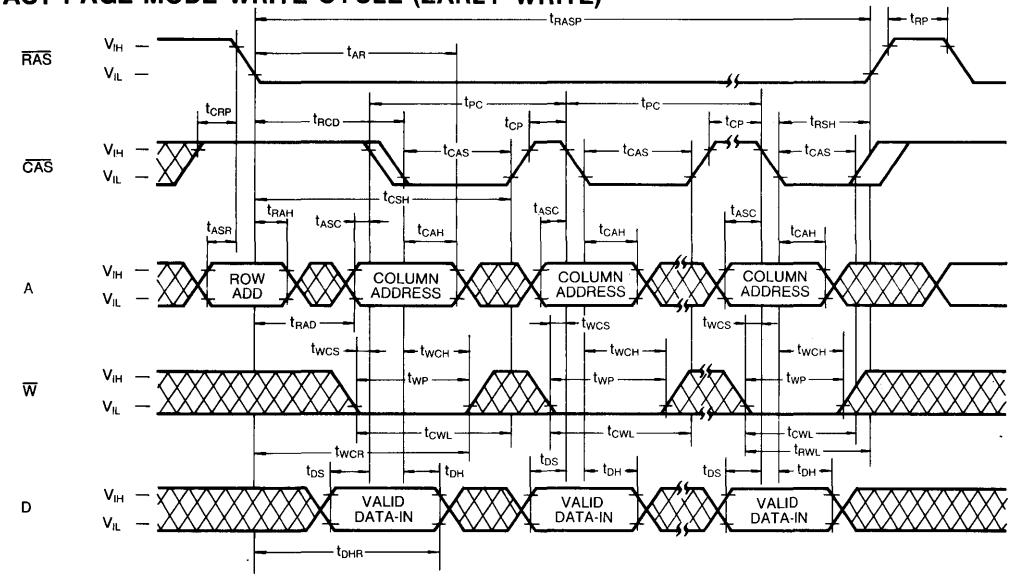


FAST PAGE MODE READ CYCLE

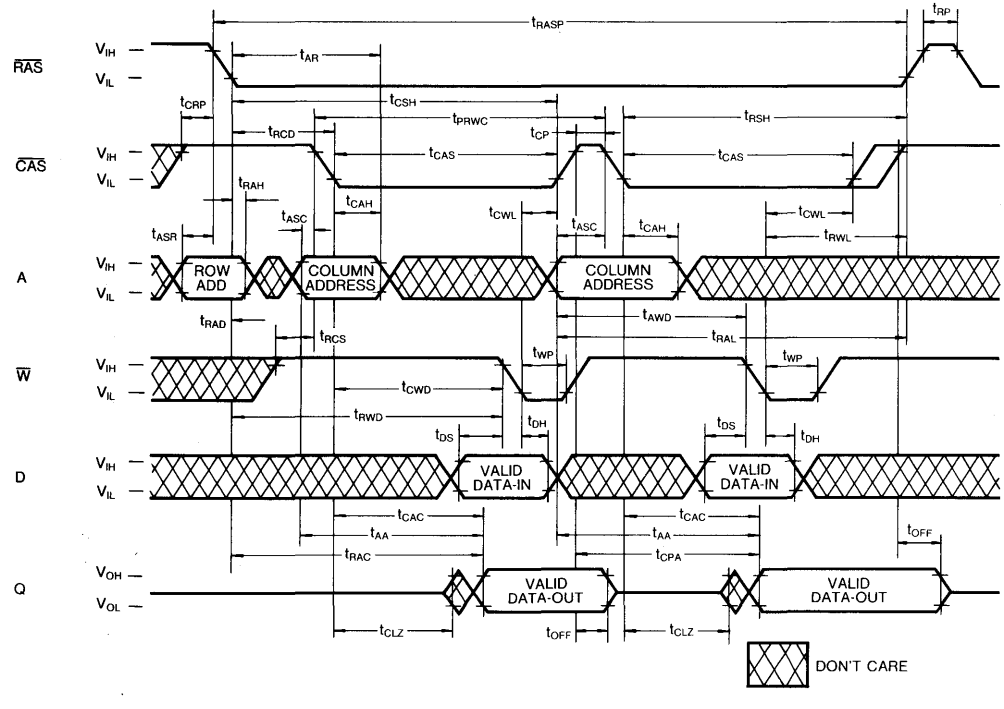


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



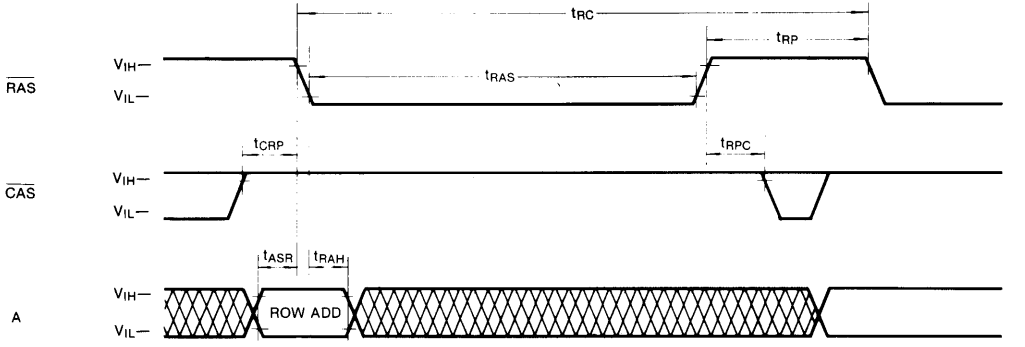
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

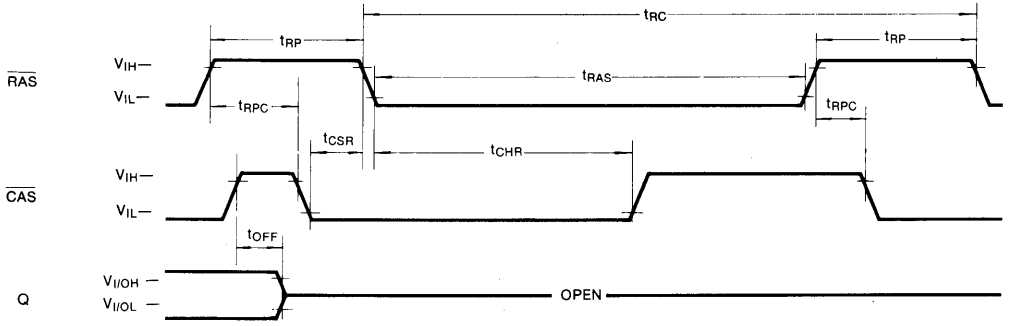
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



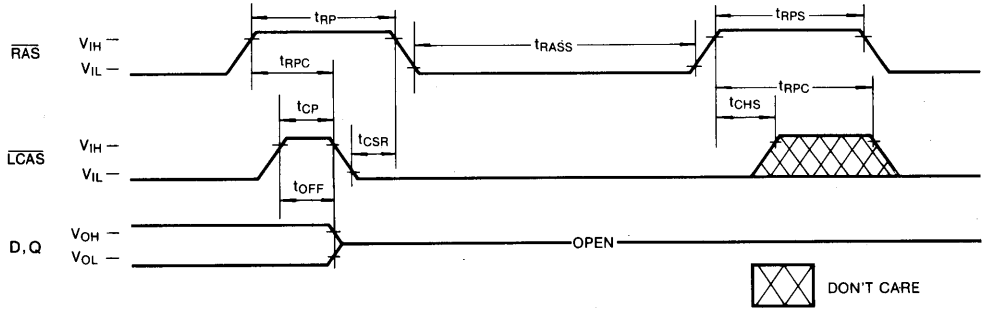
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



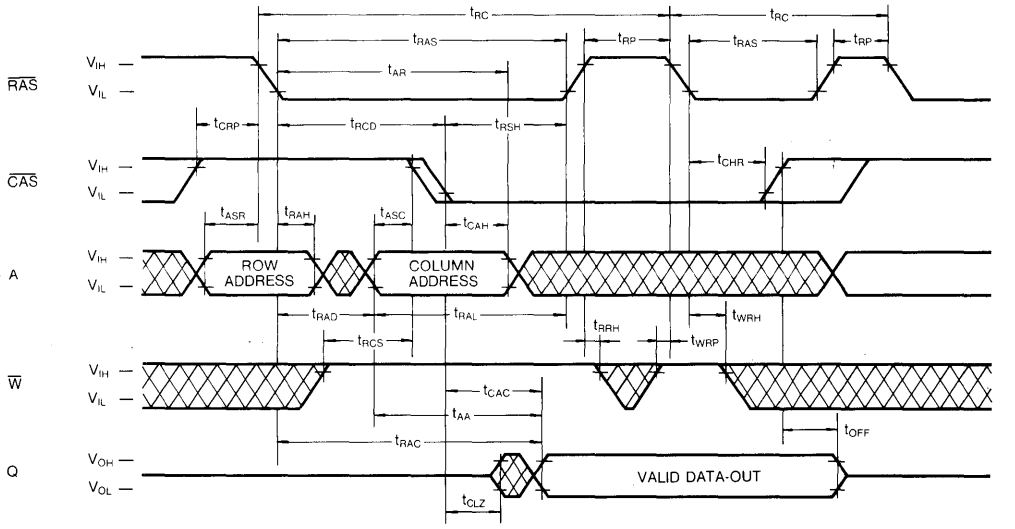
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

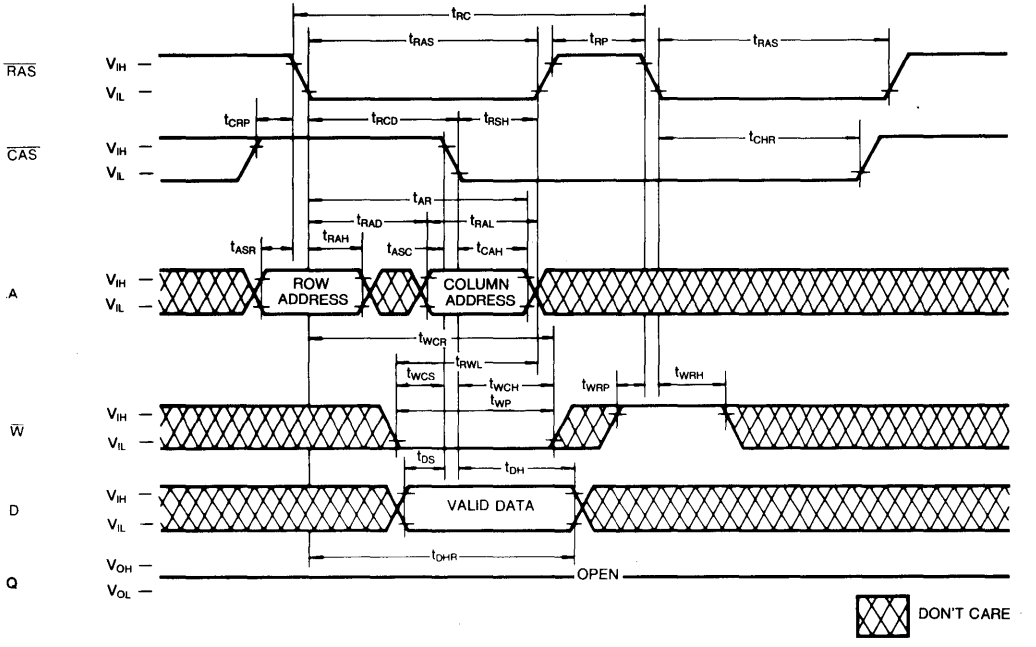


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

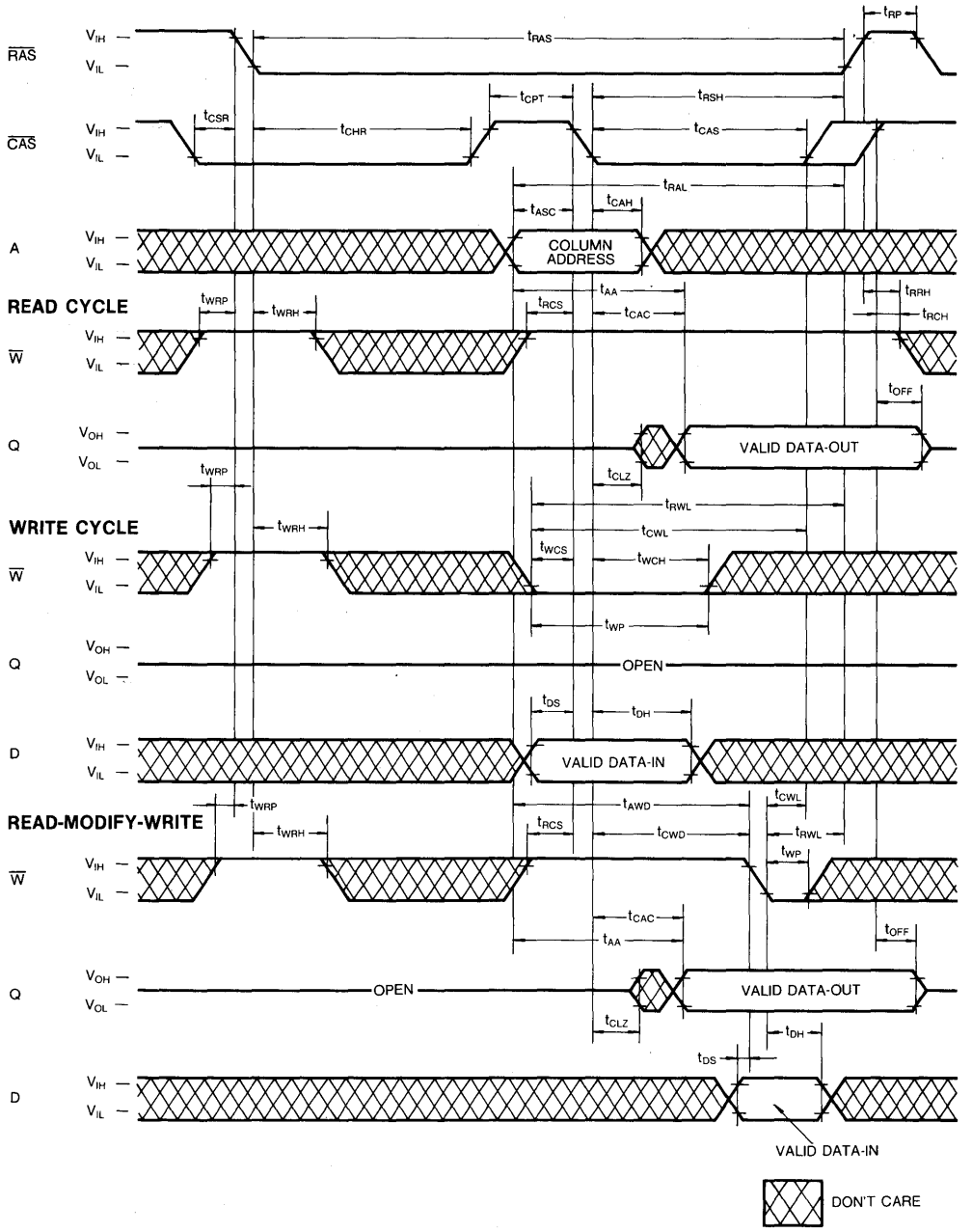


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

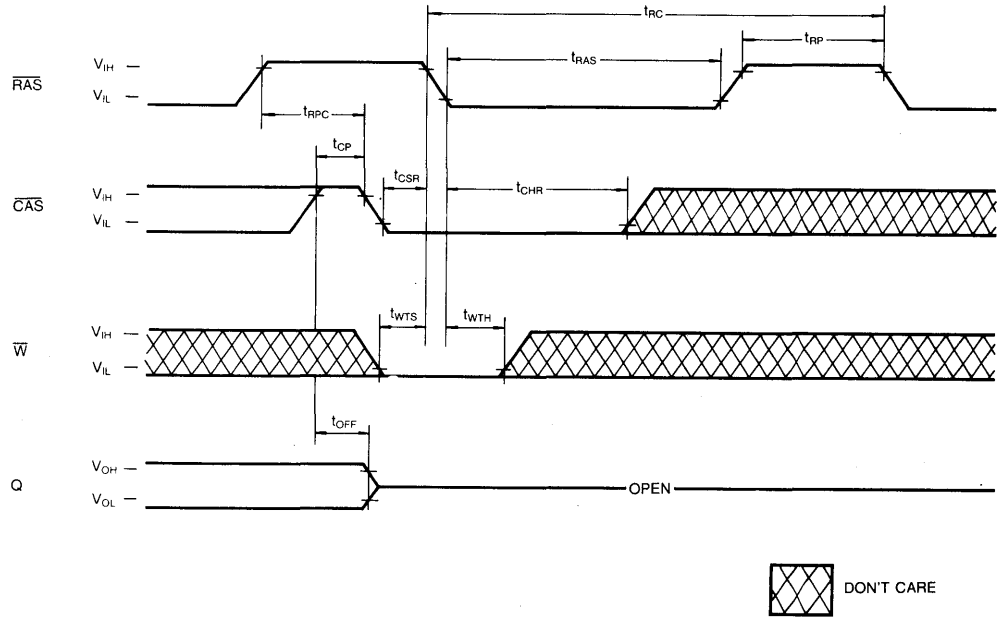
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



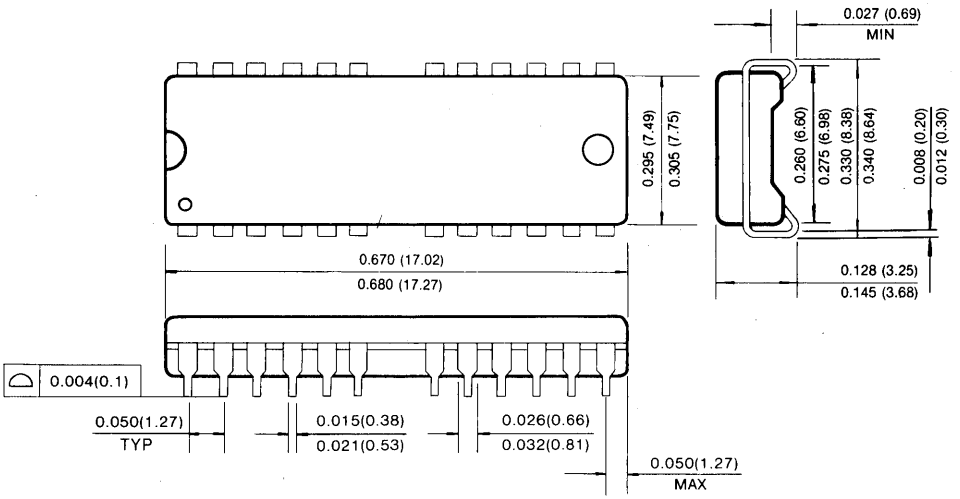
TEST MODE DESCRIPTION

The KM41V16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0". In "Test Mode", the 16M DRAM can be tested as if it were a 1M × 1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

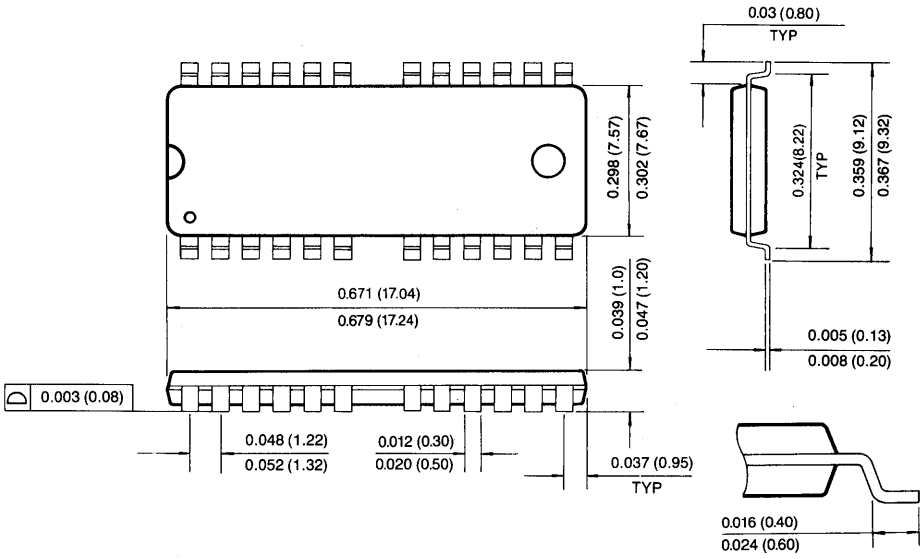
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



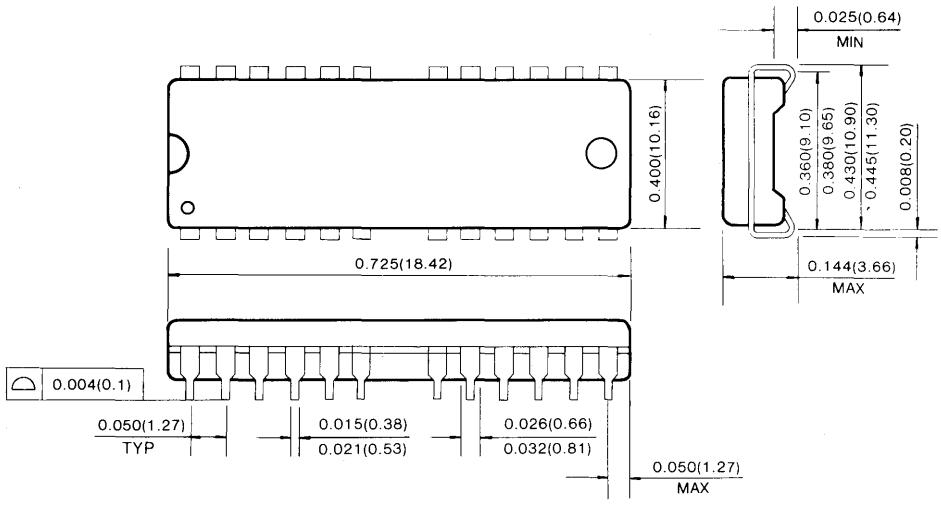
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



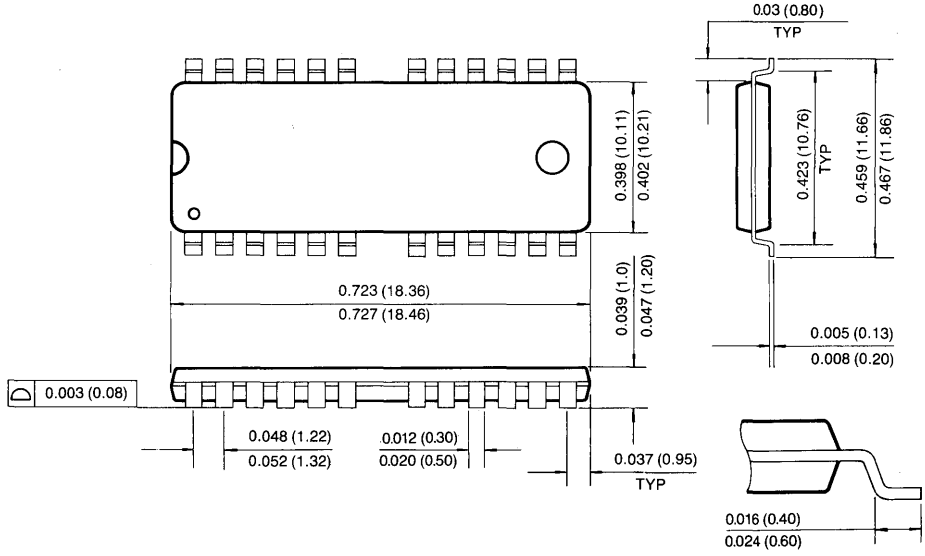
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44V4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Double+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal DRAM)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

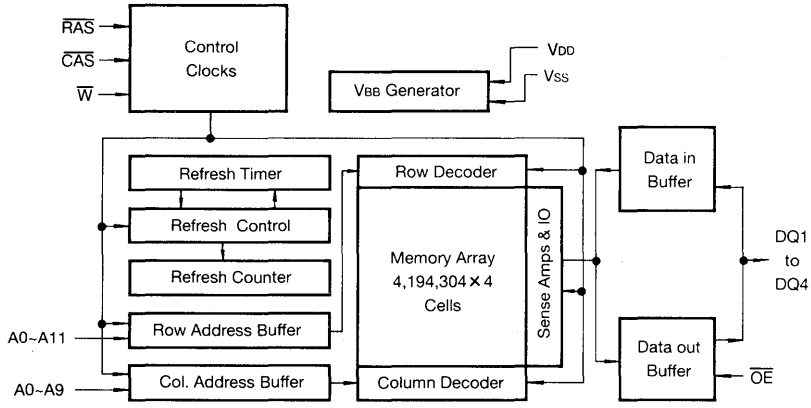
The Samsung KM44V4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

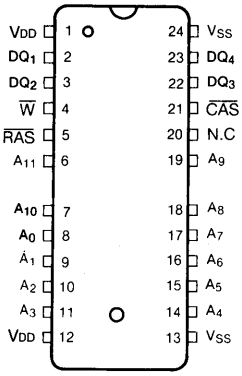
The KM44V4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



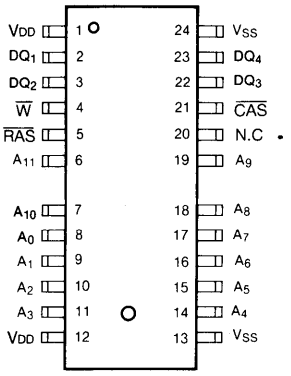
PIN CONFIGURATION (Top Views)

• KM44V4000 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK



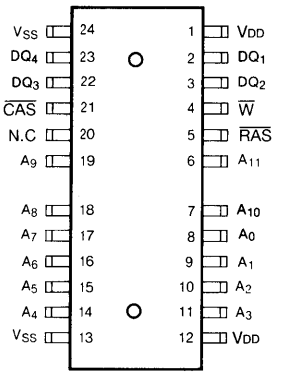
J : 400MIL
K : 300MIL

• KM44V4000 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4000 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1~4	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC1}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4000A	I_{CC2}	-	2	mA
	KM44V4000AL			1	mA
	KM44V4000ALL			1	mA
	KM44V4000ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC3}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC4}	-	70	mA
	KM44V4000A/AL/ALL/ASL-7			60	mA
	KM44V4000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4000A	I_{CC5}	-	1	mA
	KM44V4000AL			300	μA
	KM44V4000ALL			200	μA
	KM44V4000ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4000A/AL/ALL/ASL-6	I_{CC6}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM44V4000AL	I_{CC7}	-	450	μA
	KM44V4000ASL			350	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V, 0.2V or Open	KM44V4000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal DRAM only)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

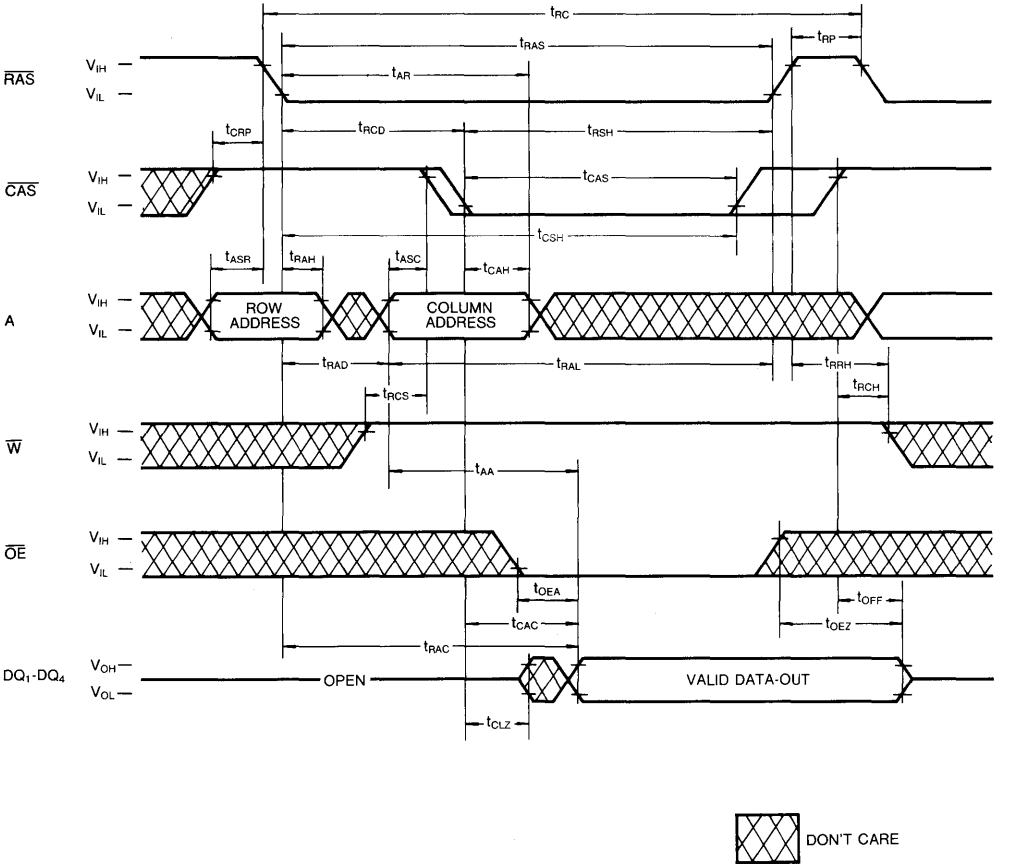
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

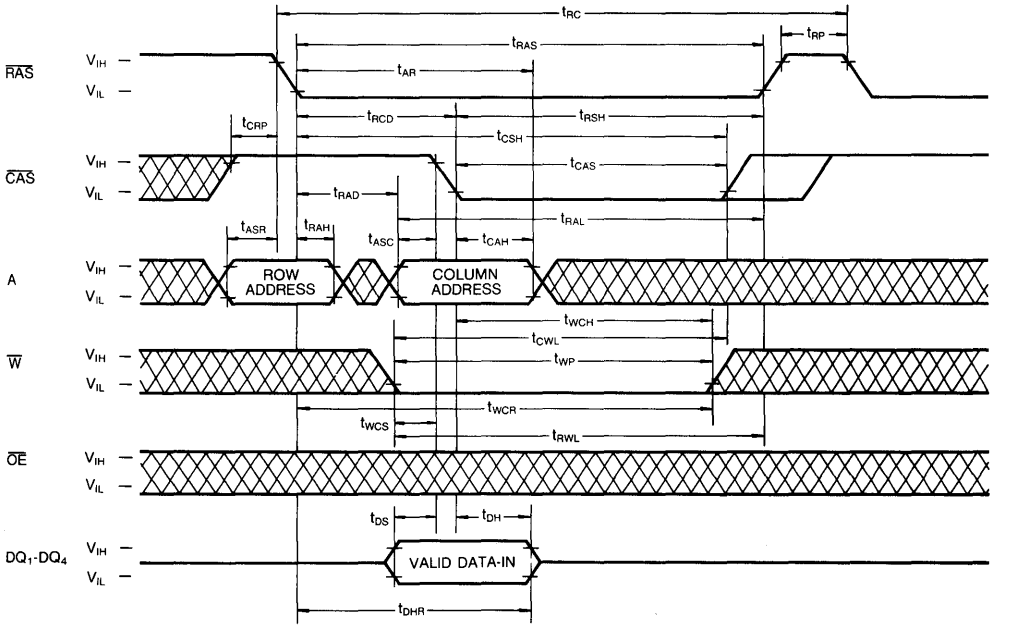
TIMING DIAGRAMS

READ CYCLE

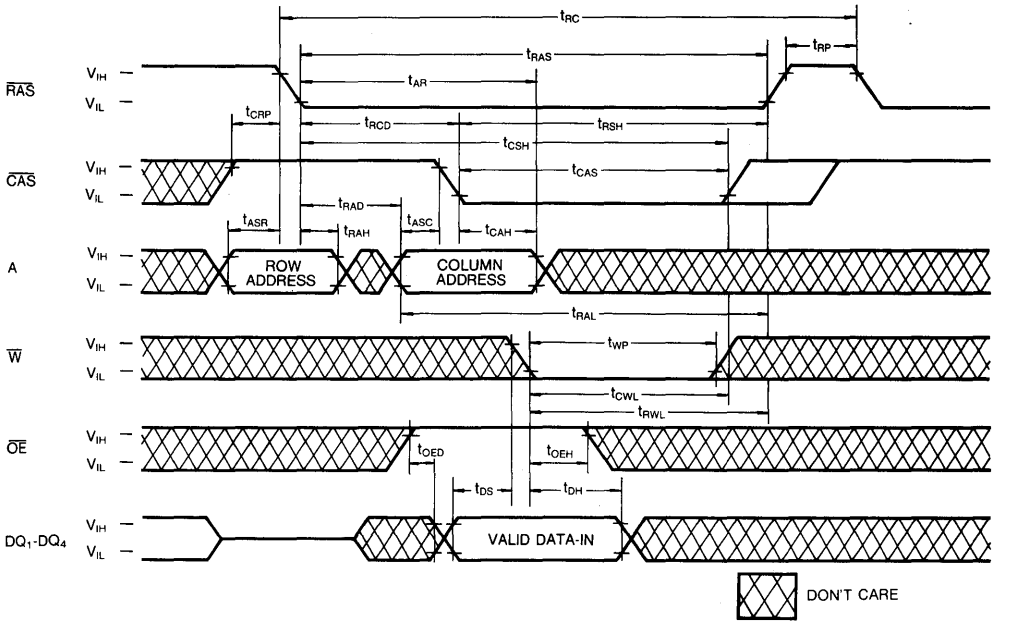


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

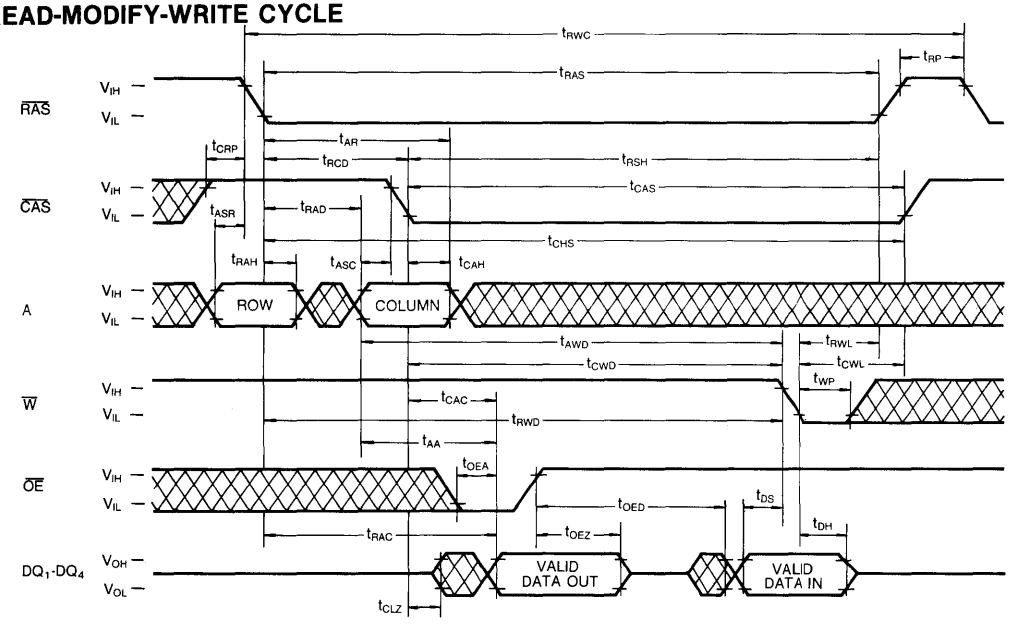


WRITE CYCLE (OE CONTROLLED WRITE)

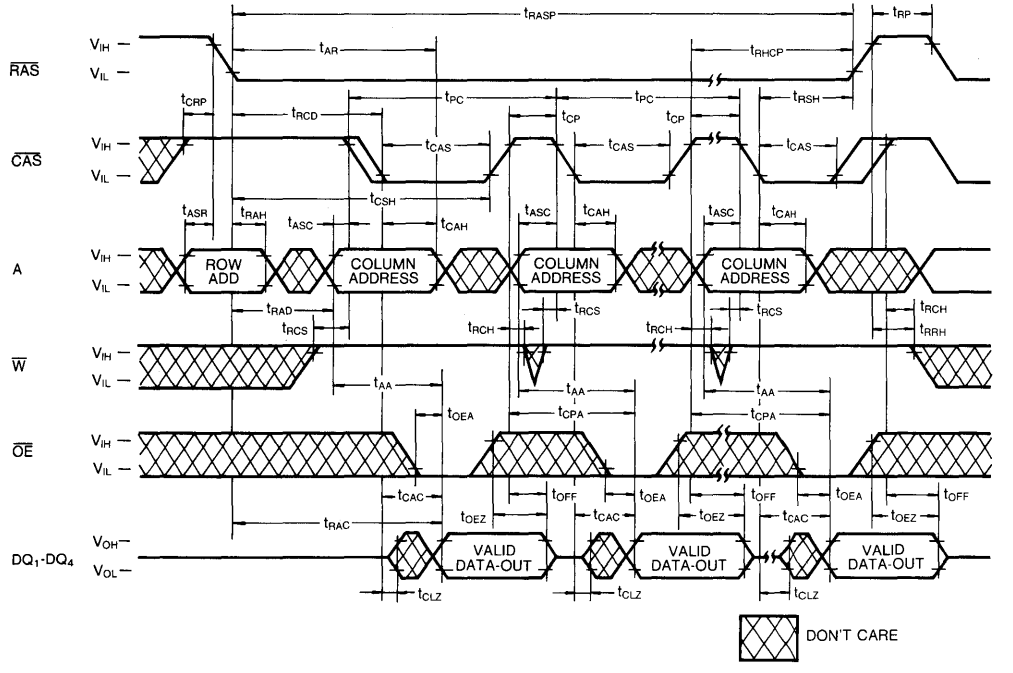


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



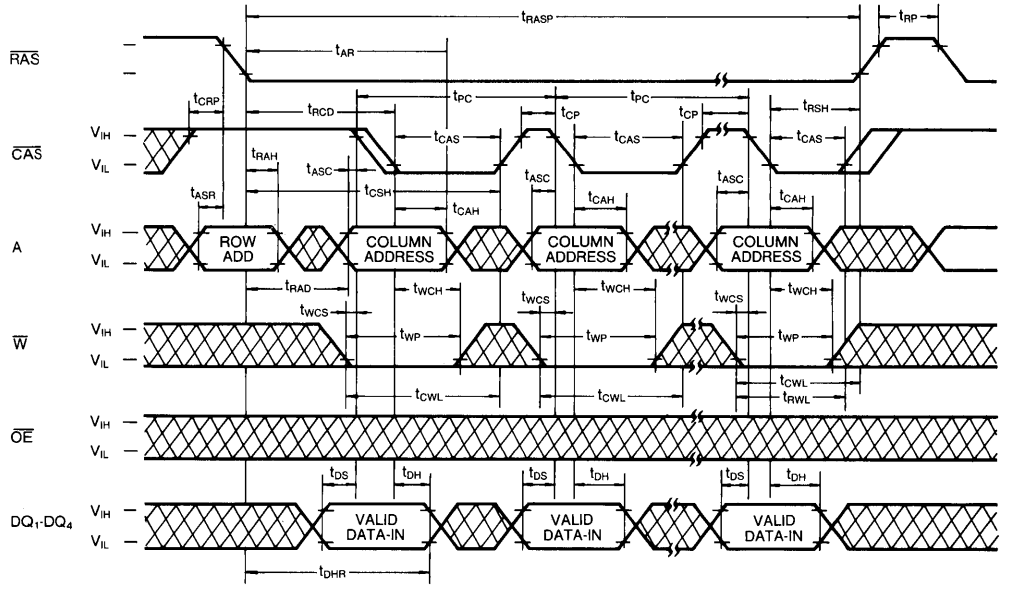
FAST PAGE MODE READ CYCLE



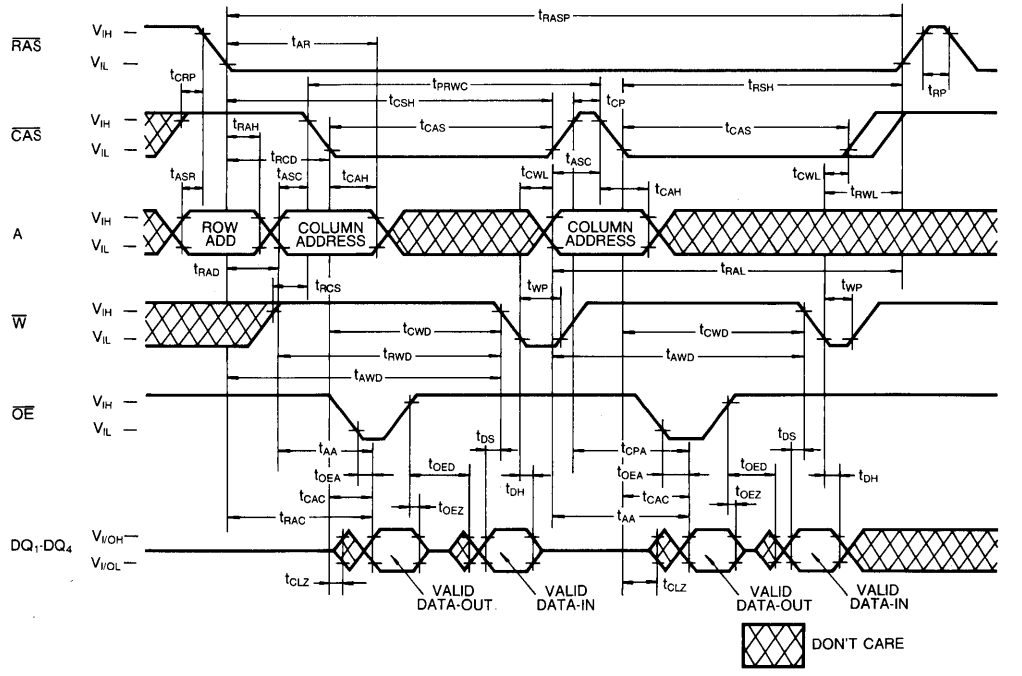
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

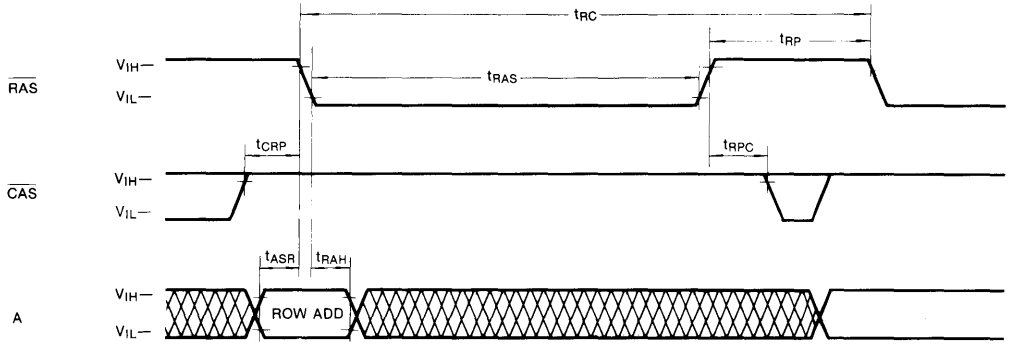


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

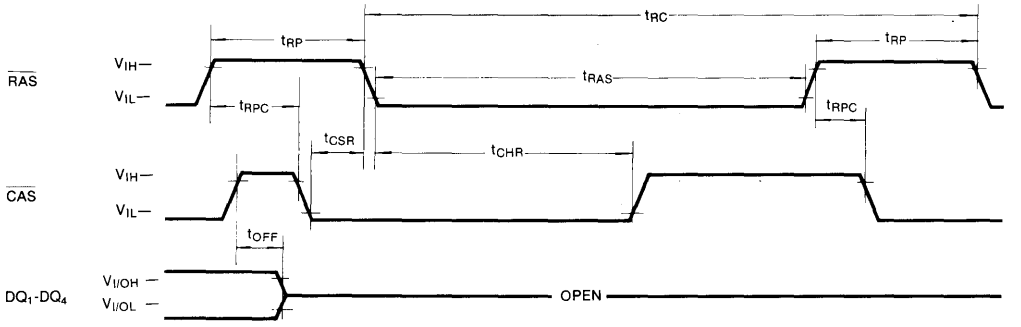
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



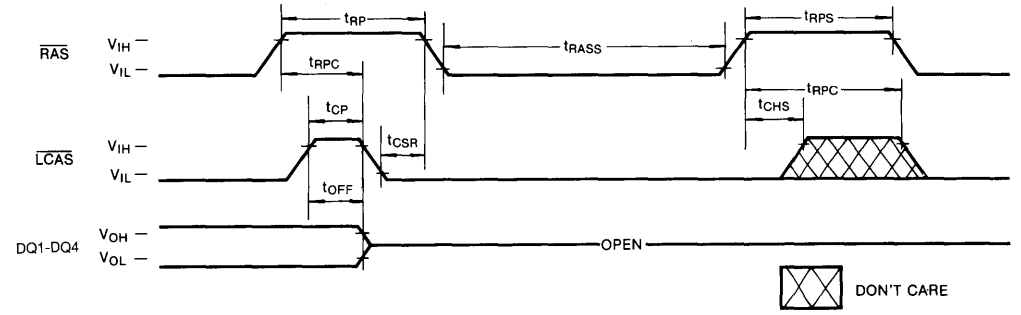
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



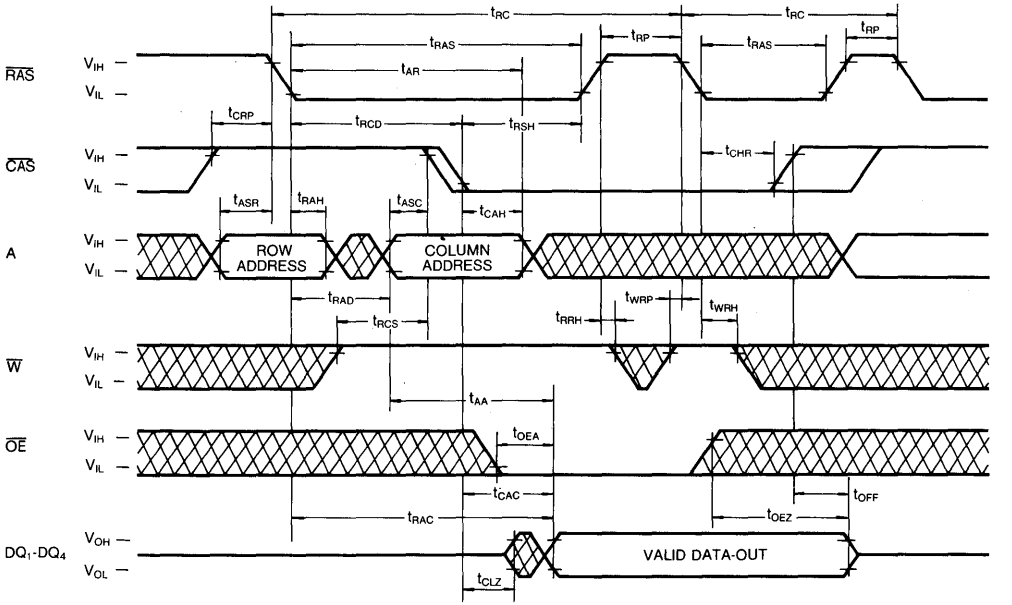
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

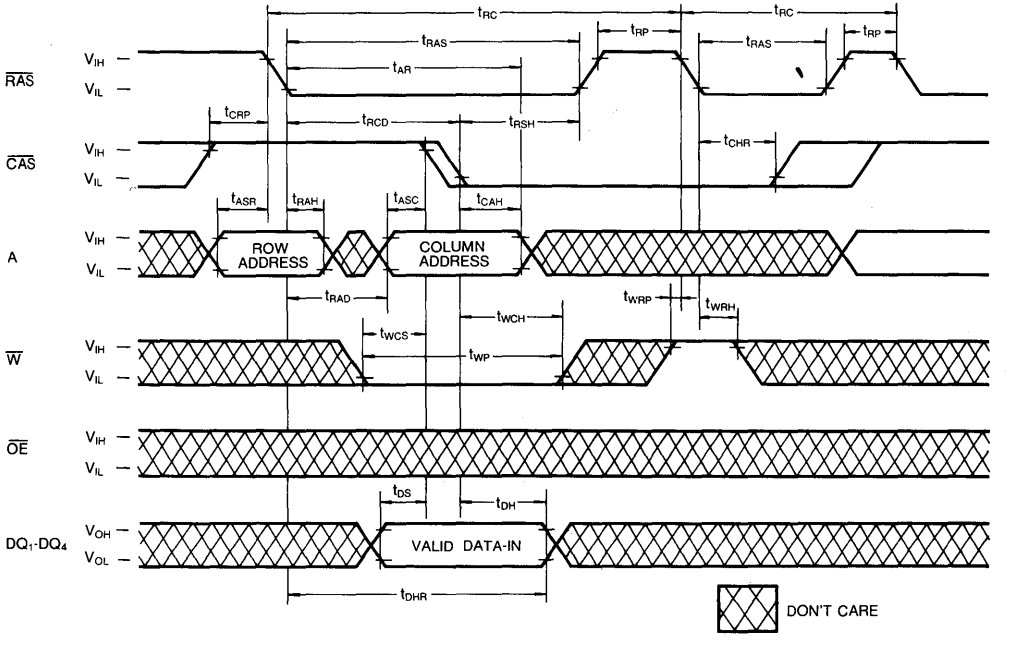


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

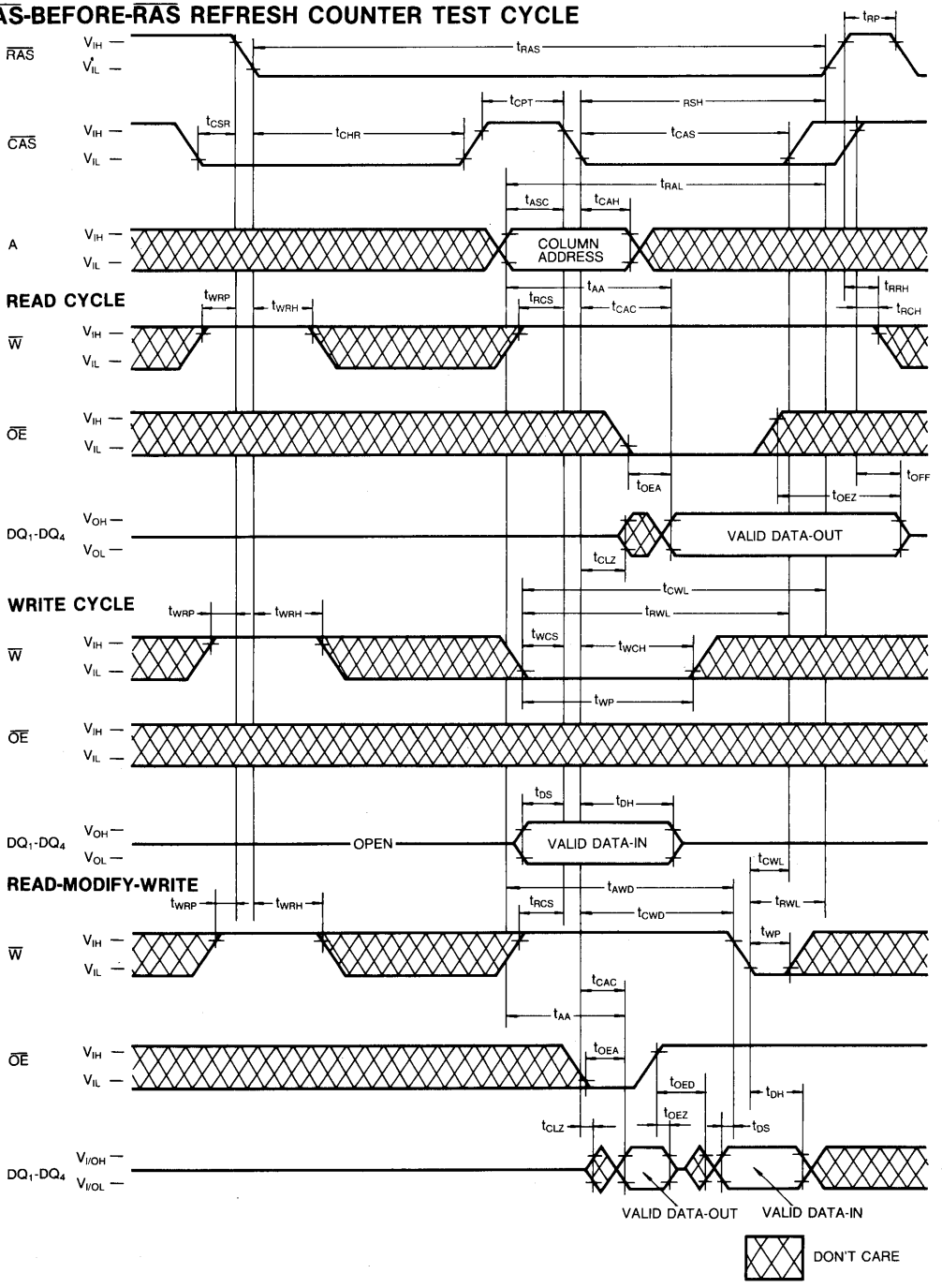


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

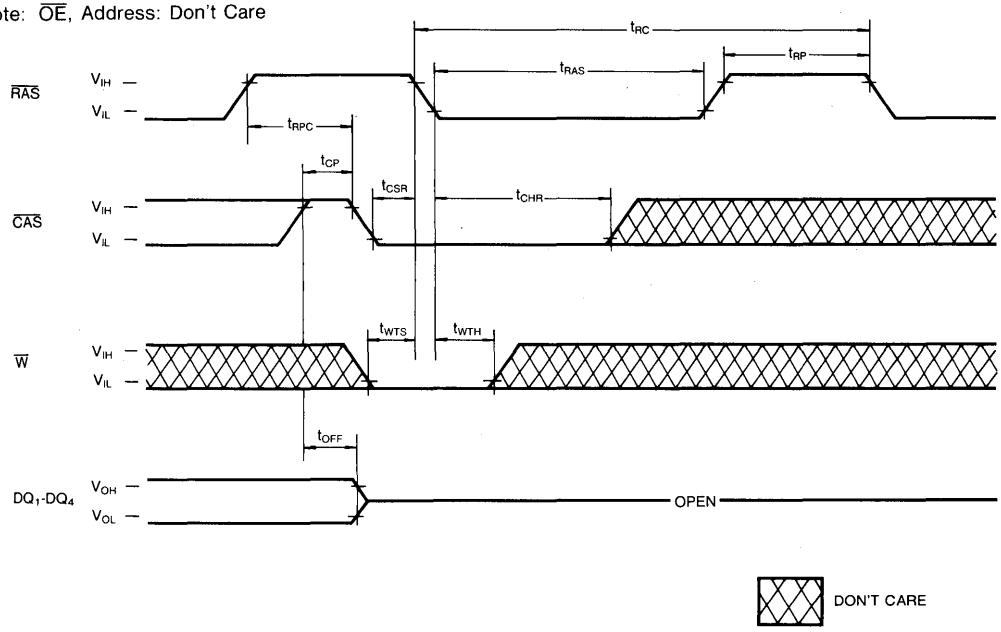


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



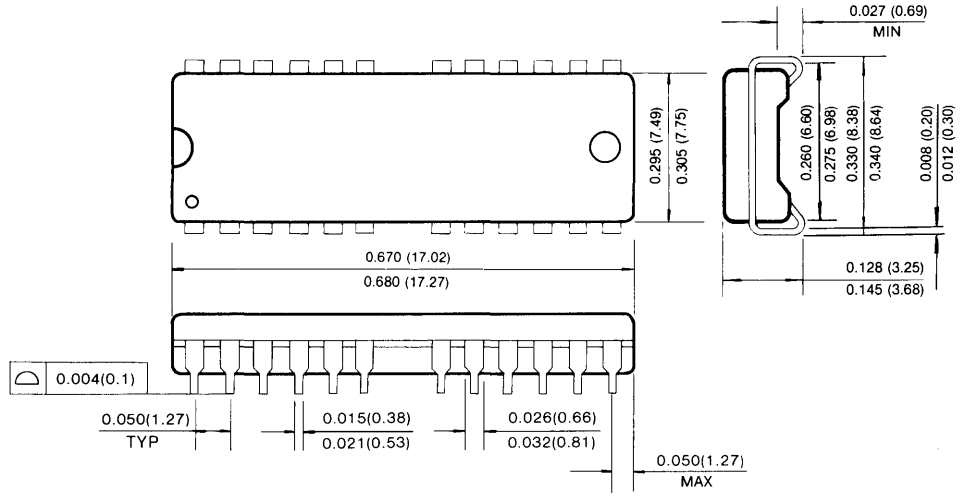
TEST MODE DESCRIPTION

The KM44V4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

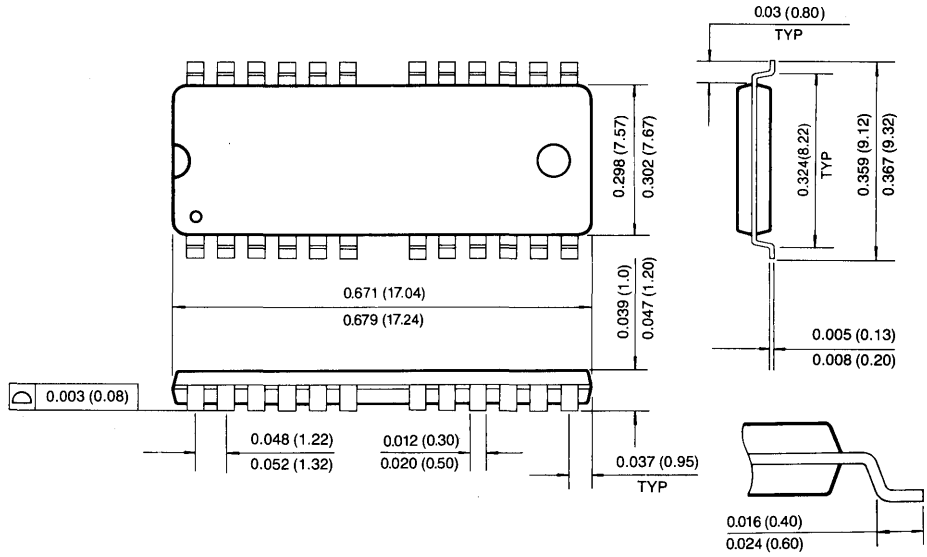
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



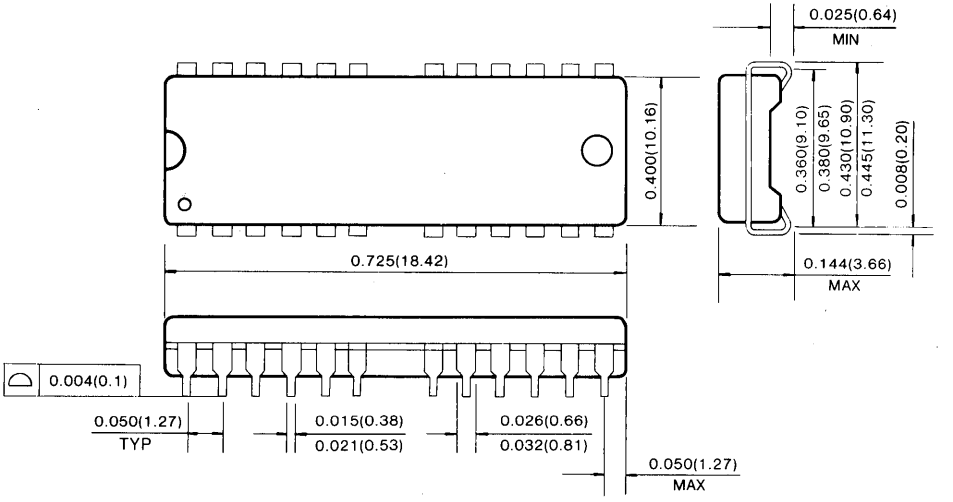
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



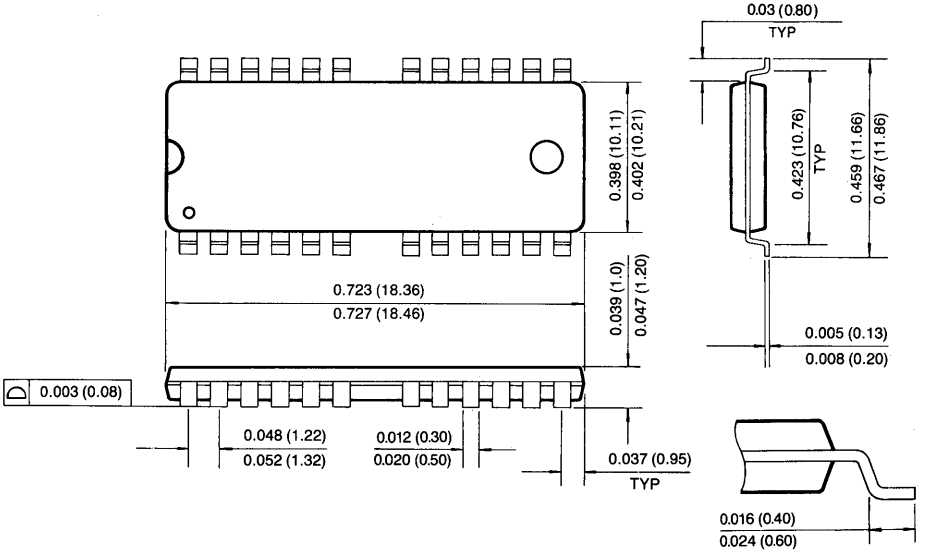
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M ×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44V4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Double+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal DRAM)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

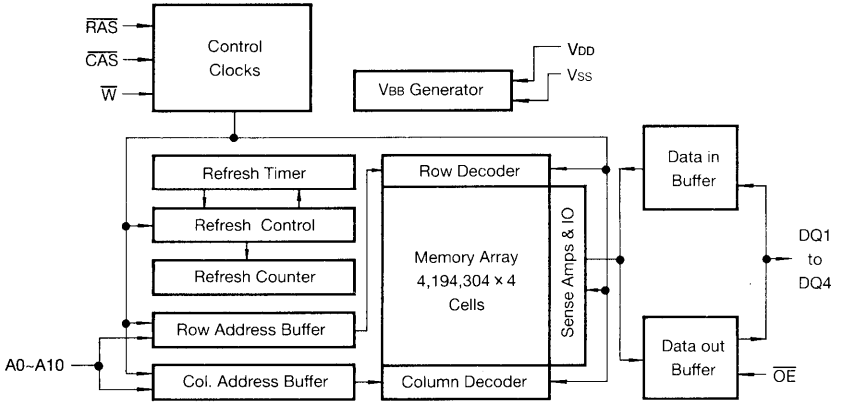
The Samsung KM44V4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

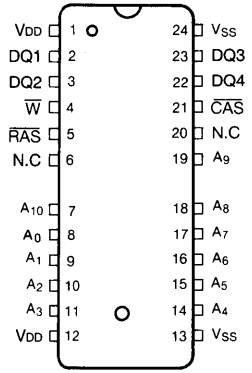
The KM44V4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



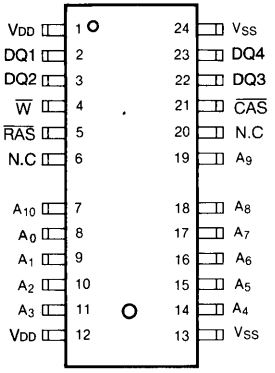
PIN CONFIGURATION (Top Views)

• **KM44V4100 AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK**



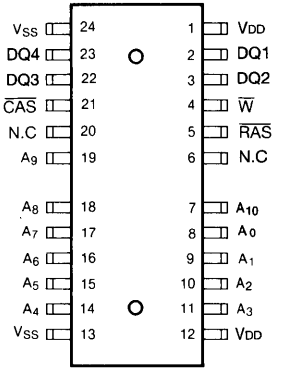
J : 400MIL
K : 300MIL

• **KM44V4100 AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS**



T : 400MIL(Forward)
S : 300MIL(Forward)

• **KM44V4100 ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR**



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
$DQ_{1\sim4}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V4100A	I_{CC2}	-	2	mA
	KM44V4100AL			1	mA
	KM44V4100ALL			1	mA
	KM44V4100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC4}	-	80	mA
	KM44V4100A/AL/ALL/ASL-7			70	mA
	KM44V4100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V4100A	I_{CC5}	-	1	mA
	KM44V4100AL			300	μA
	KM44V4100ALL			200	μA
	KM44V4100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44V4100A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM44V4100A/AL/ALL/ASL-7			90	mA
	KM44V4100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM44V4100AL	I_{CC7}	-	400	μA
	KM44V4100ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_4=V_{DD}-0.2V, 0.2V or Open	KM44V4100ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal DRAM only)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

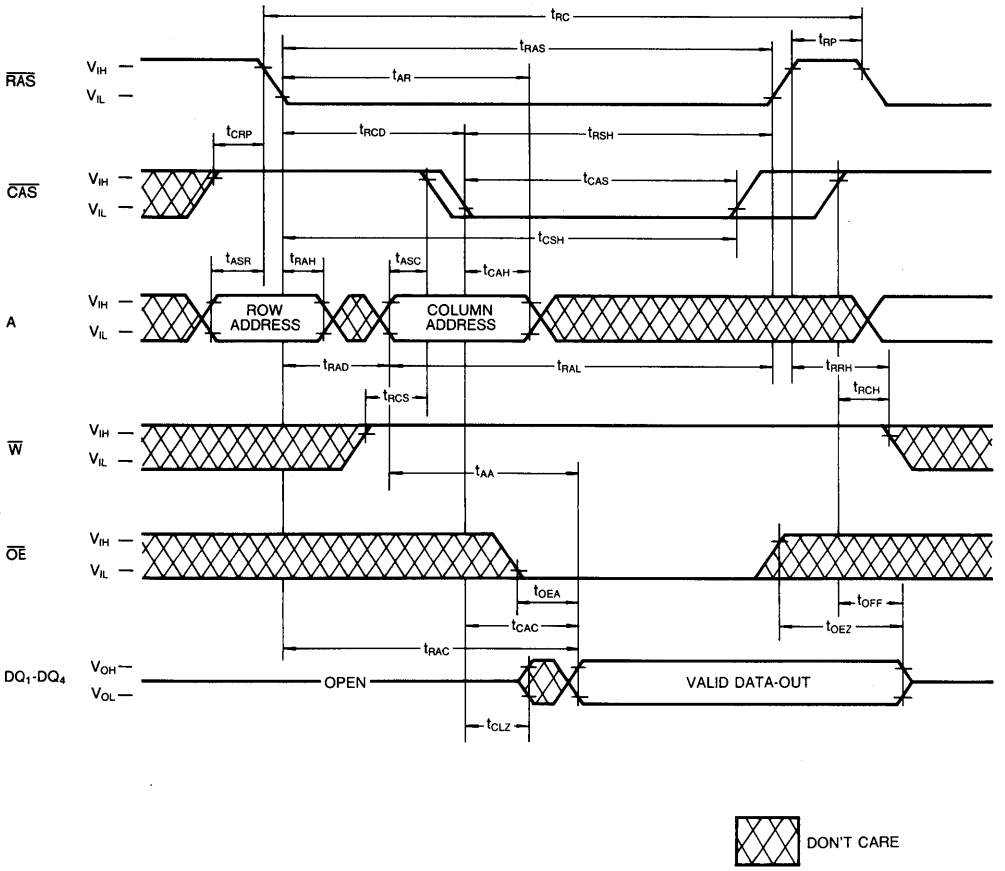
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

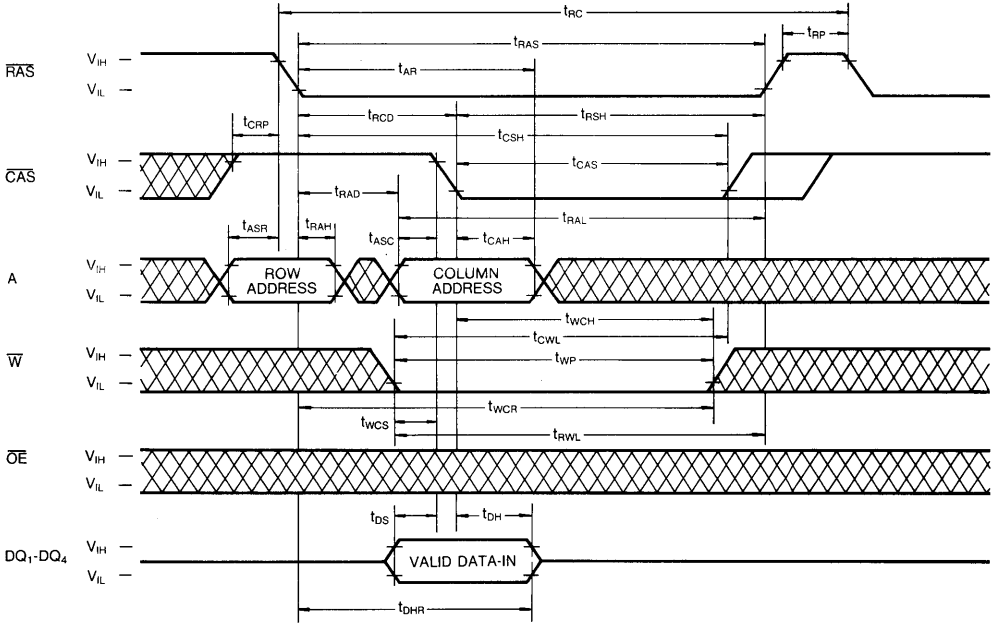
TIMING DIAGRAMS

READ CYCLE

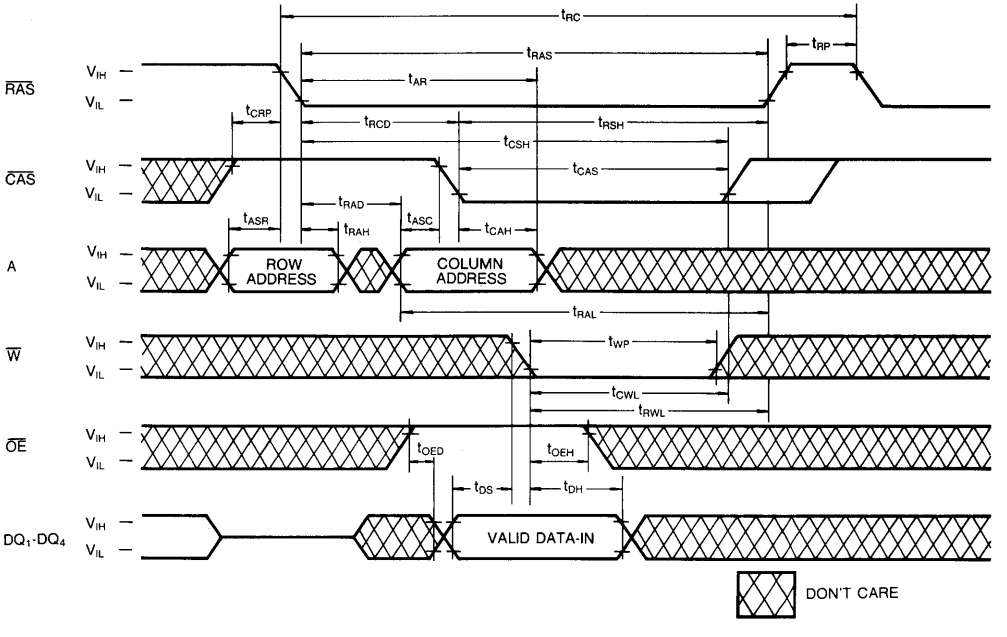


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

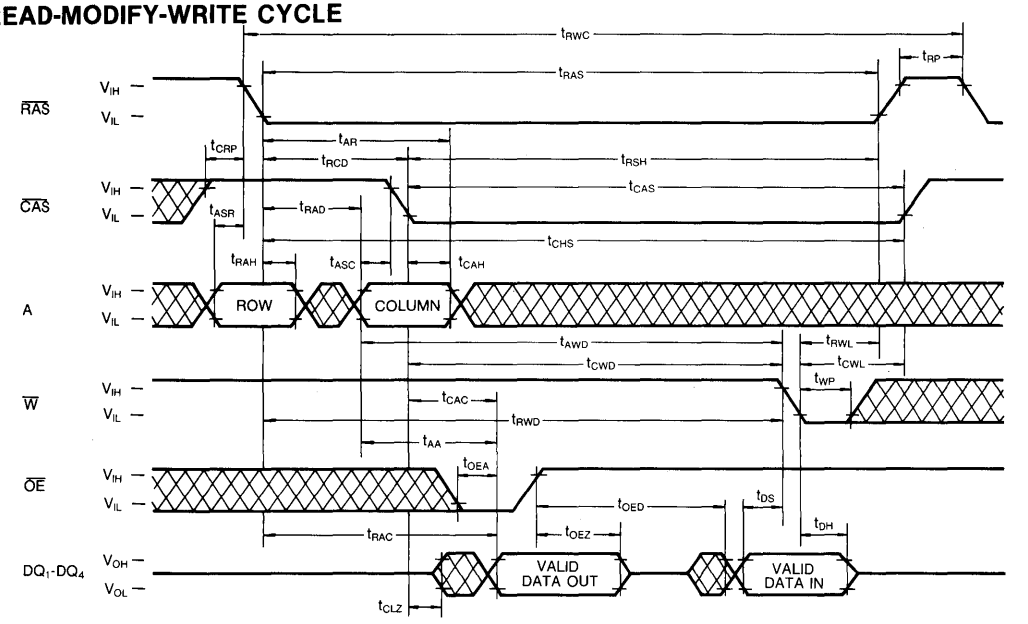


WRITE CYCLE (OE CONTROLLED WRITE)

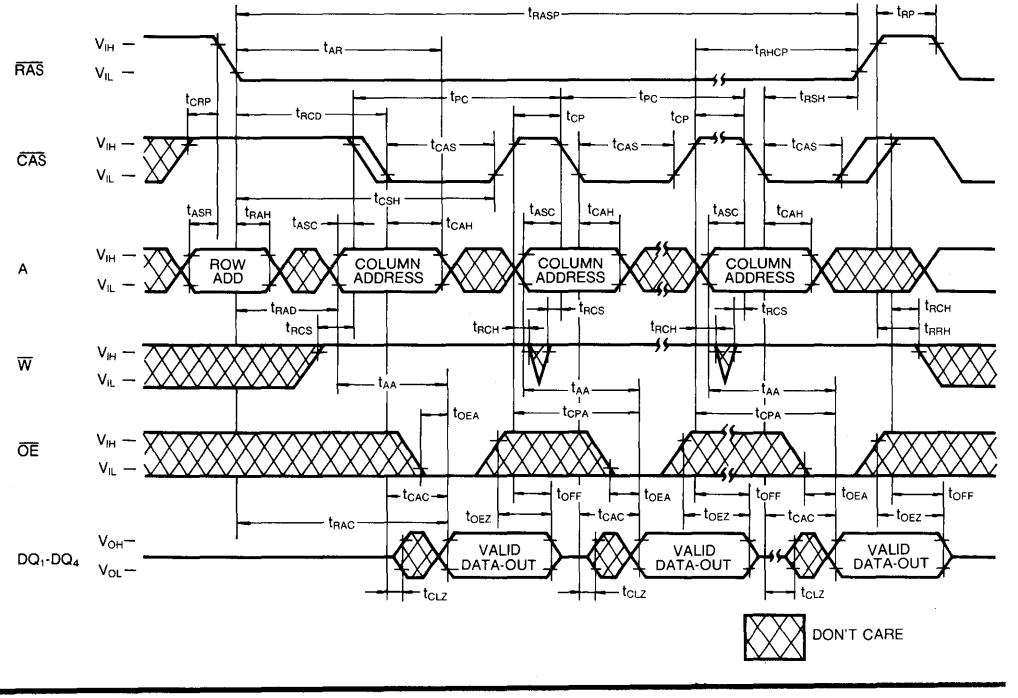


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



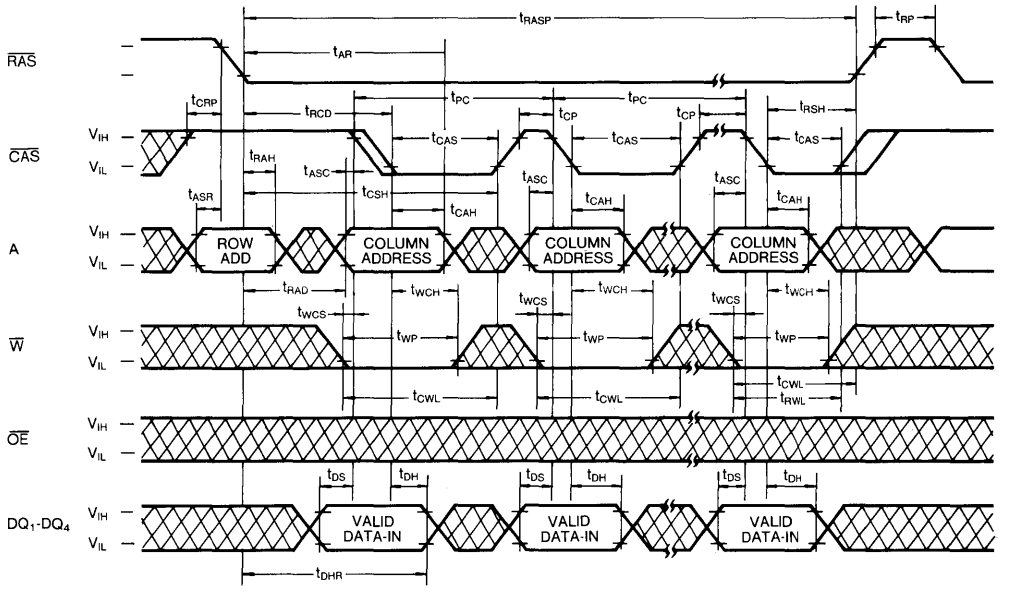
FAST PAGE MODE READ CYCLE



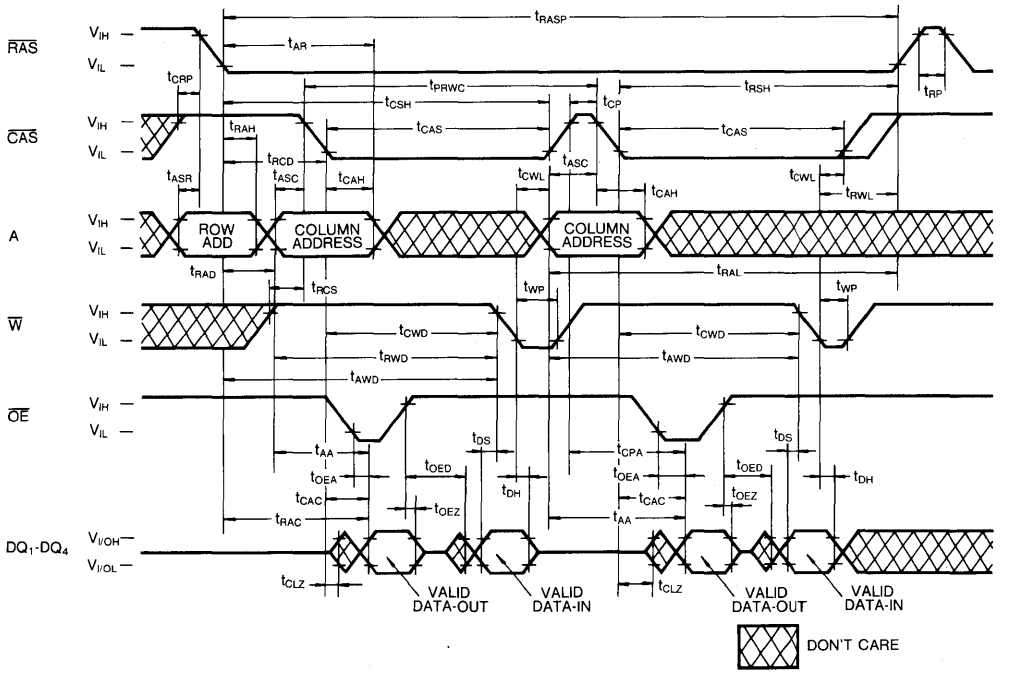
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

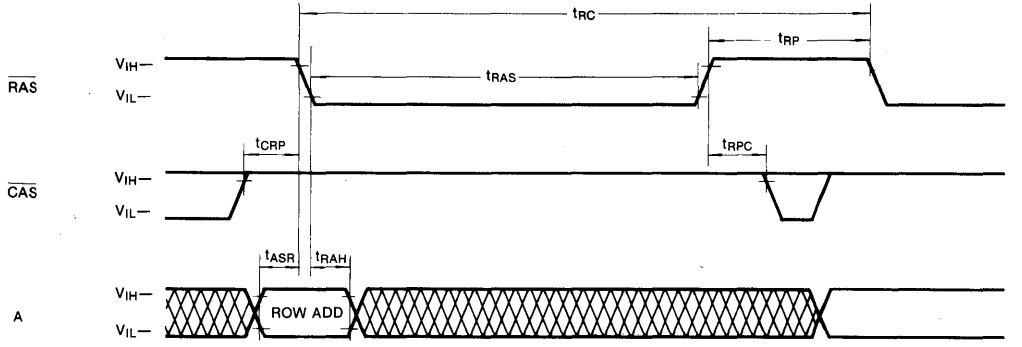


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

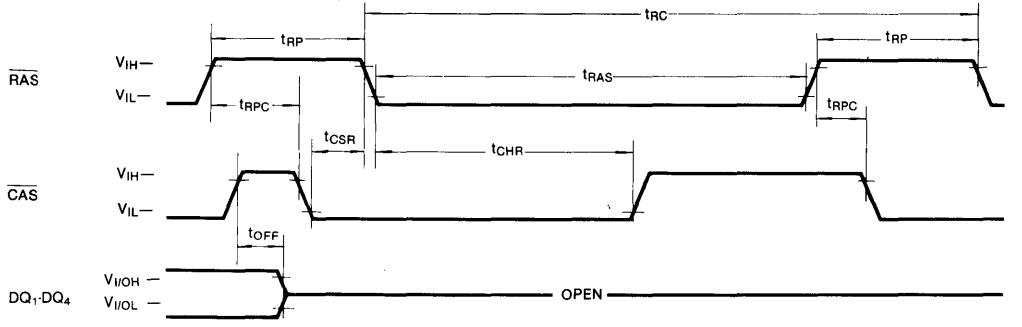
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



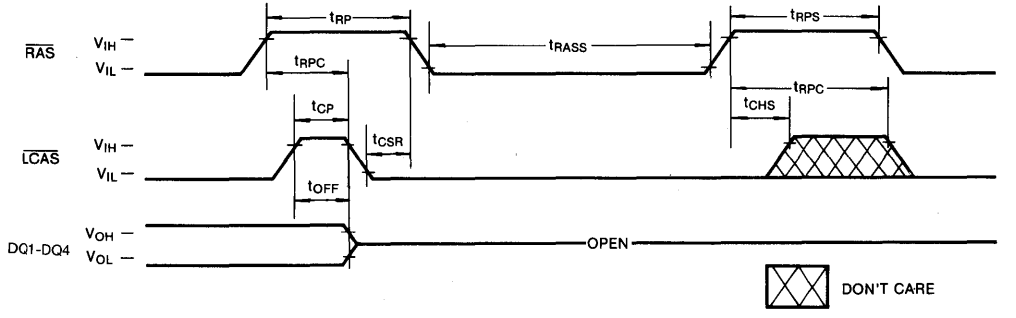
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



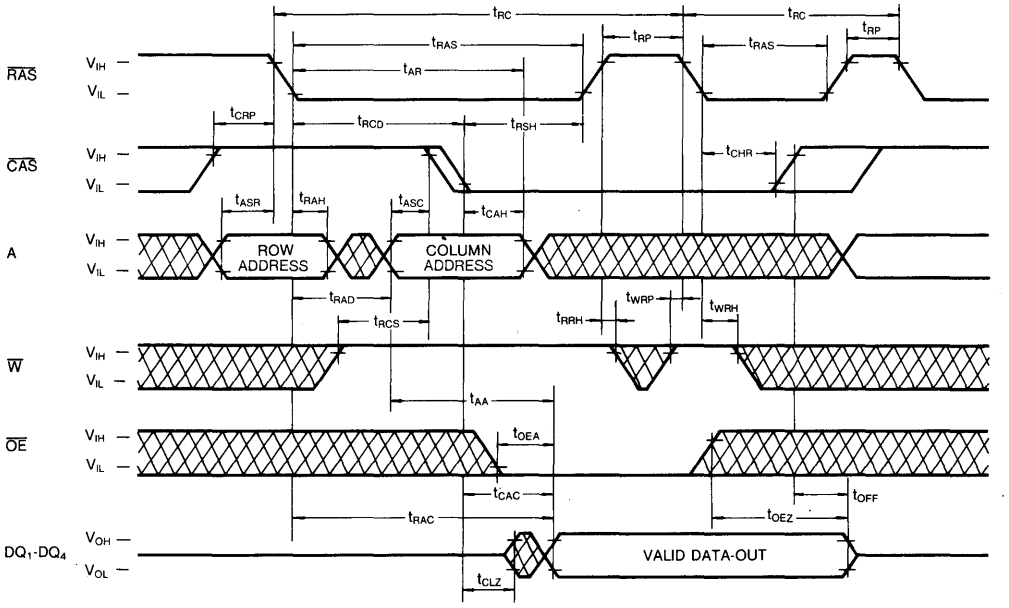
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

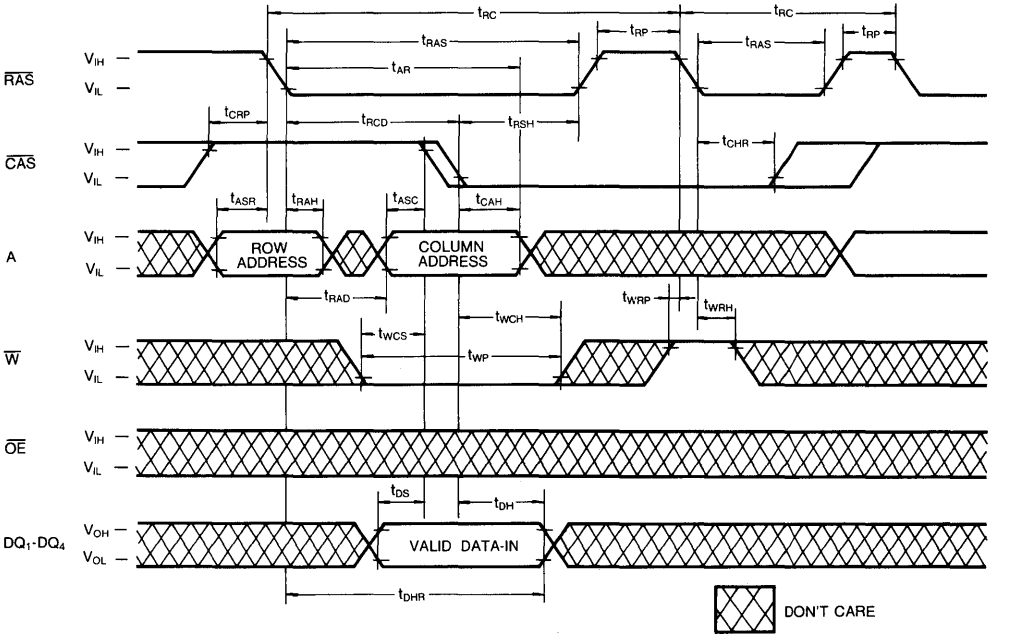


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

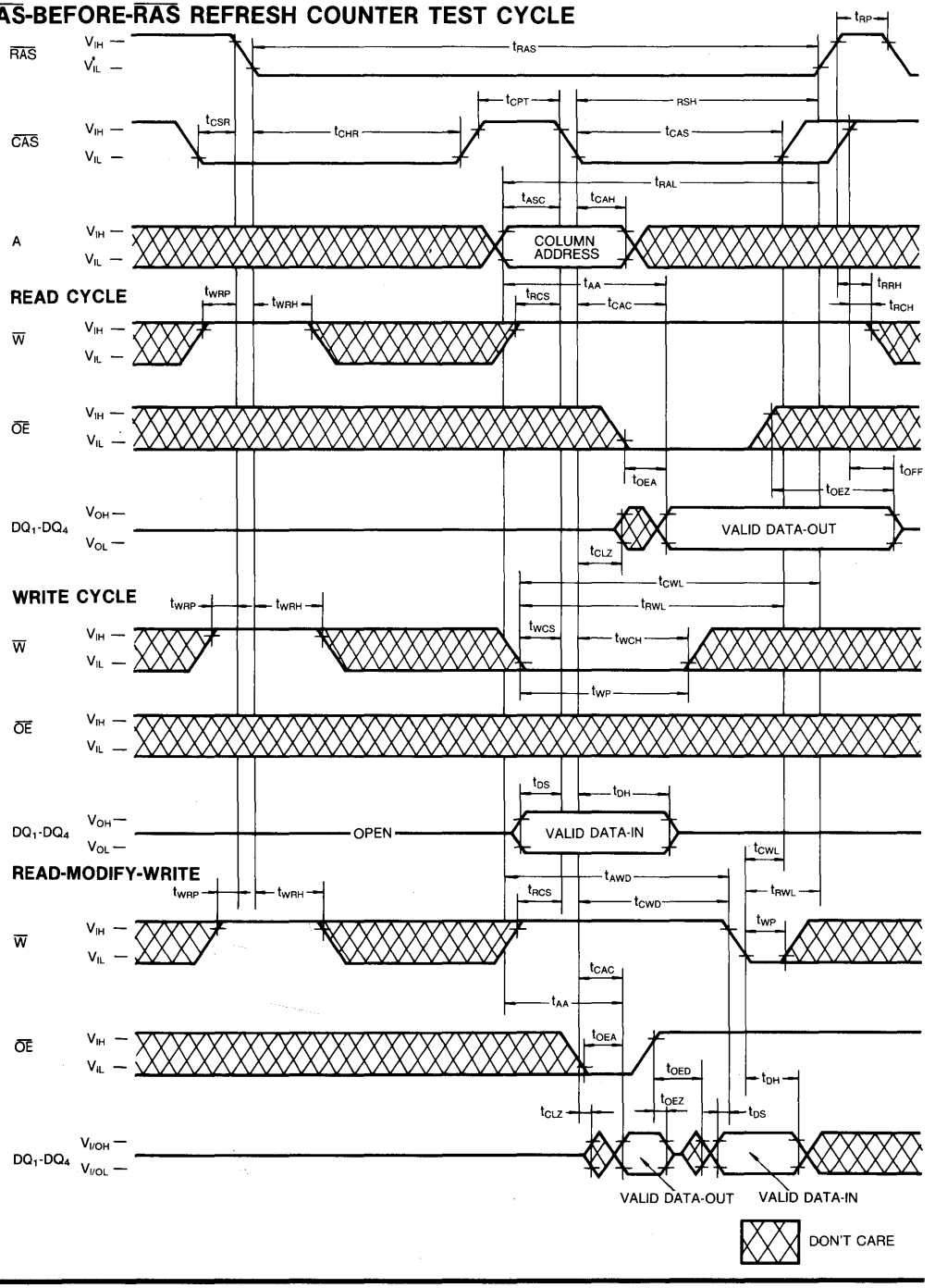


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

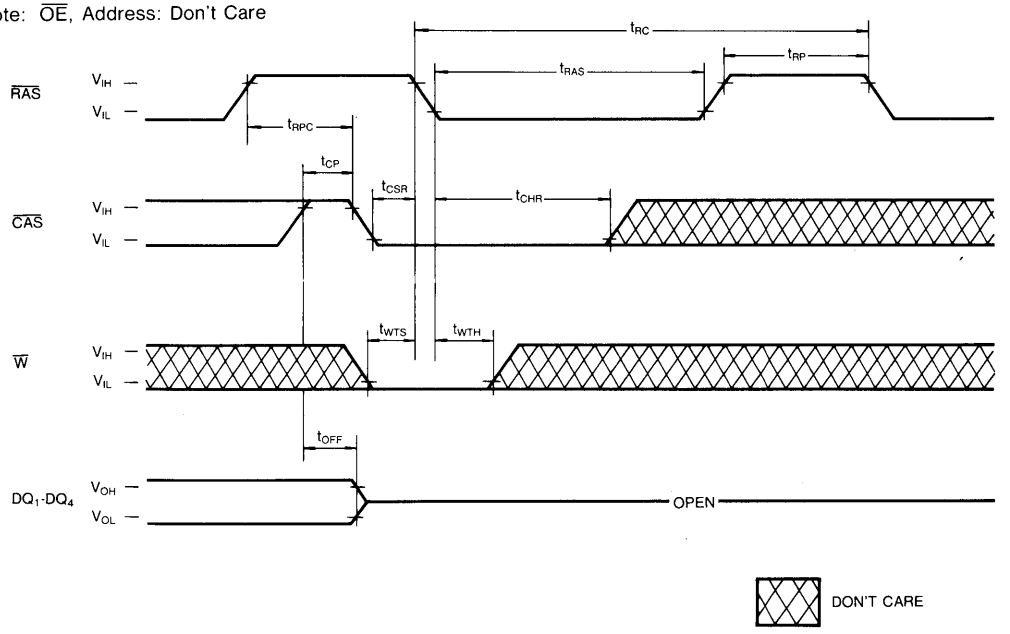
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



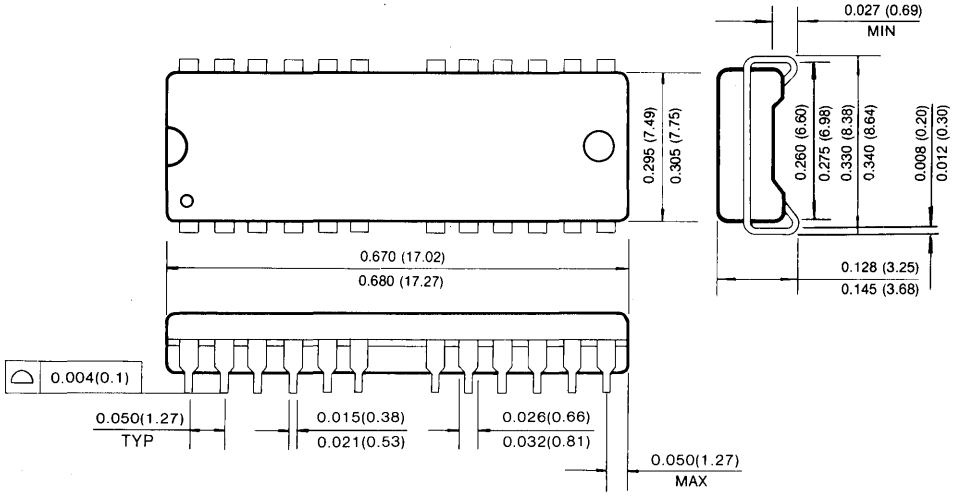
TEST MODE DESCRIPTION

The KM44V4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

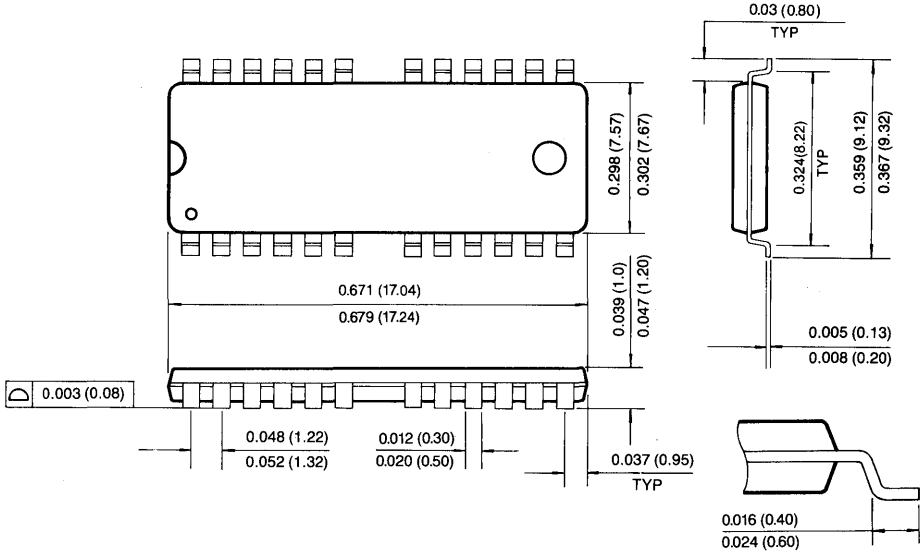
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

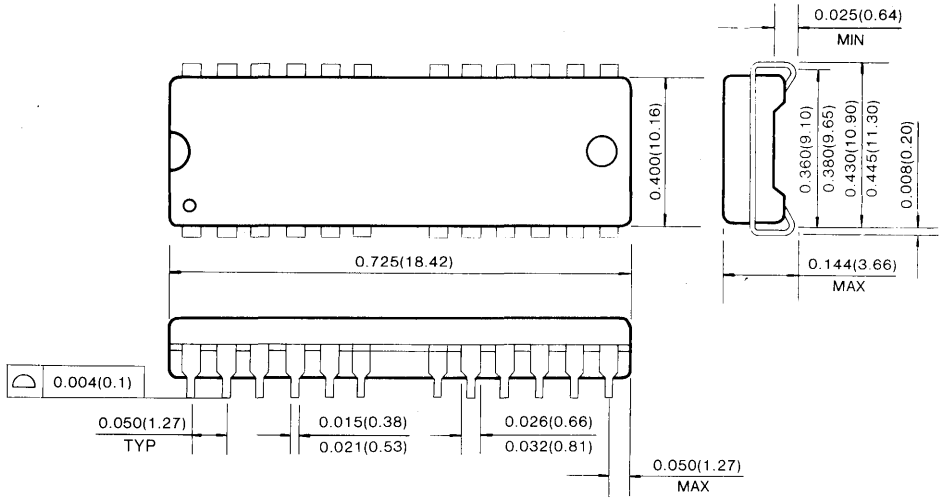


SAMSUNG ELECTRONICS

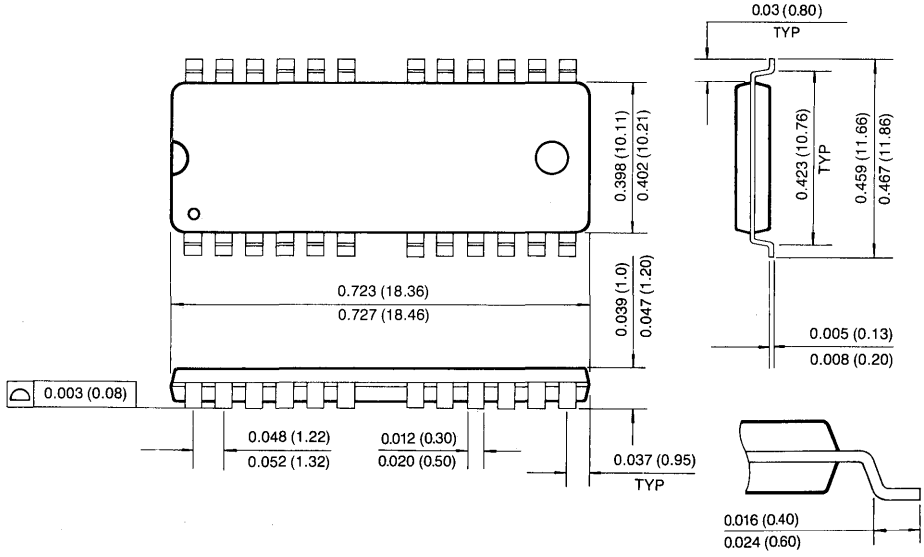
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48V2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Double+3.3V±0.3V power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

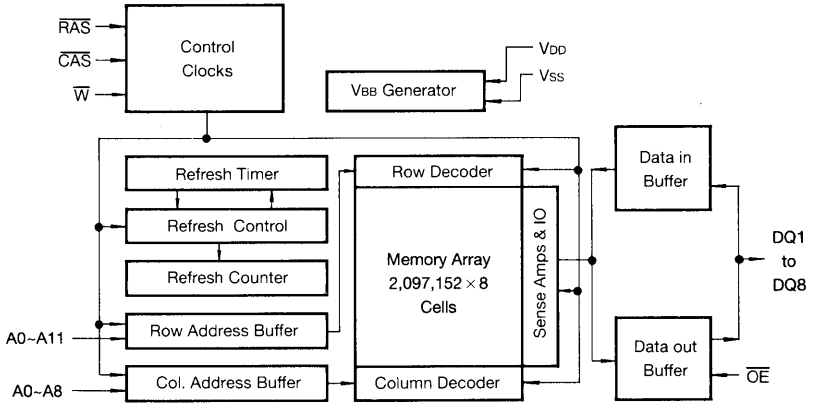
The Samsung KM48V2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

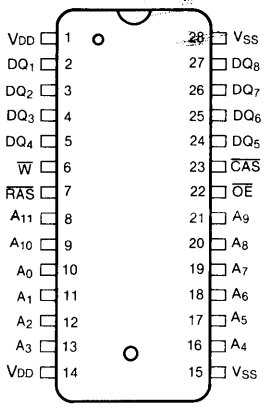
The KM48V2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

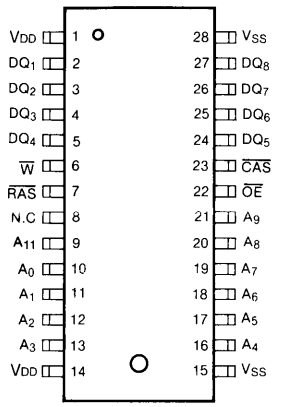


PIN CONFIGURATION (Top Views)

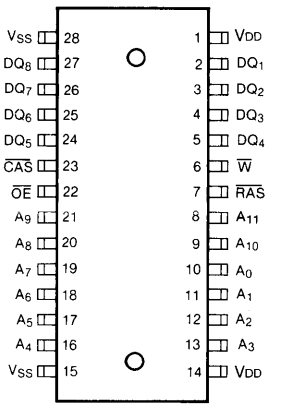
• KM48V2000 AJ/ALJ/ALLJ/ASLJ



• KM48V2000 AT/ALT/ALLT/ASLT



• KM48V2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A_0-A_{11}	Address Inputs
$DQ_{1\sim8}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC1}	-	80 70 60	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL	I_{CC2}	-	2 1 1 1	mA mA mA mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC3}	-	80 70 60	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC4}	-	70 60 50	mA mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL	I_{CC5}	-	1 300 200 200	mA μA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8	I_{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=31.25μS(L-Ver.) 62.5μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ms	KM48V2000AL KM48V2000ASL	I_{CC7}	-	450 350	μA μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2000ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

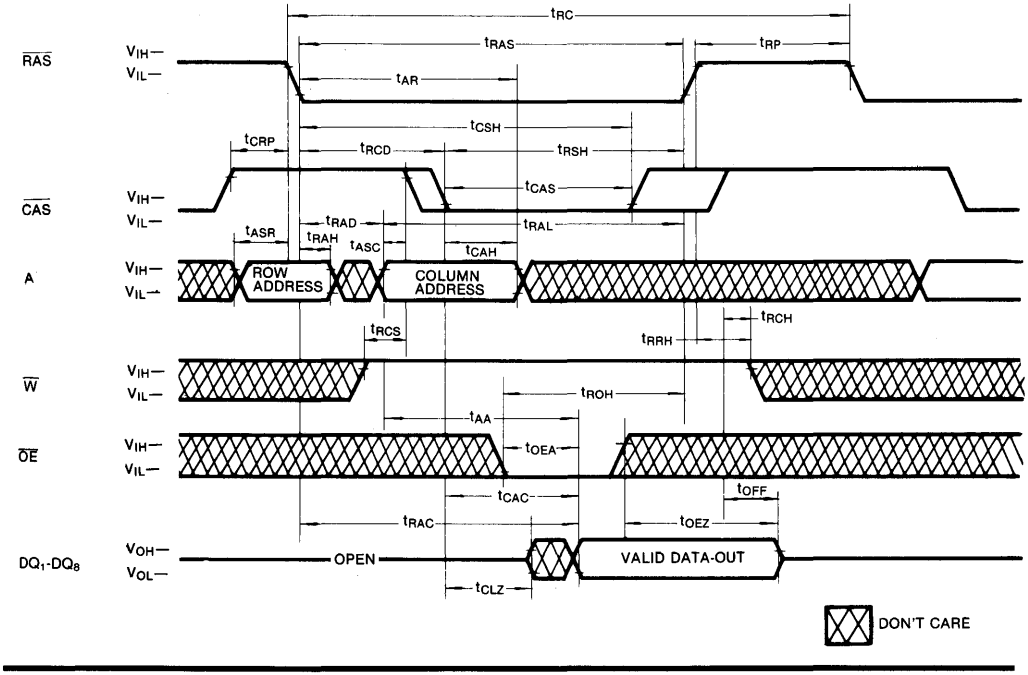
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

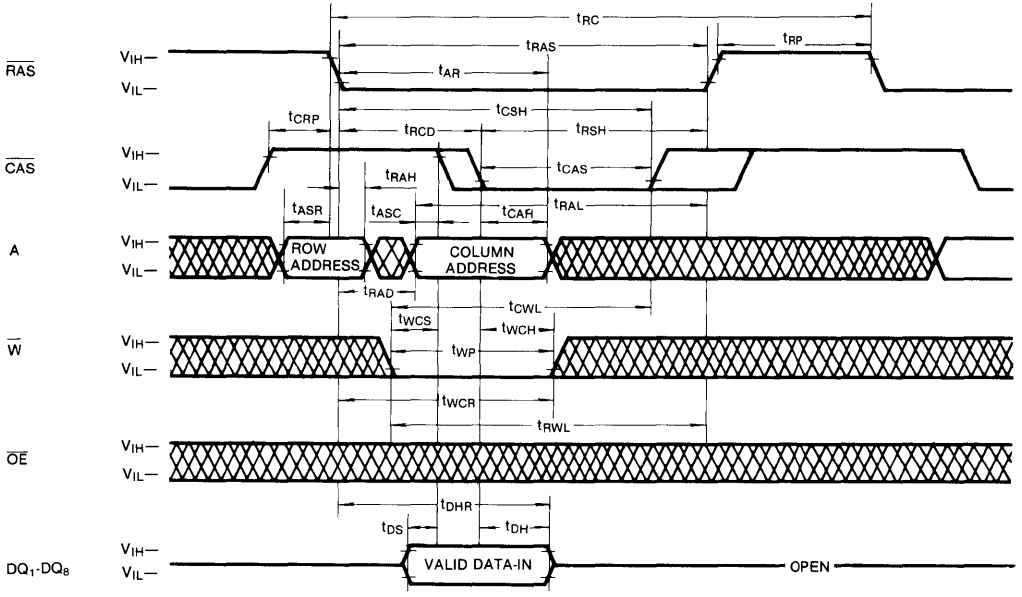
TIMING DIAGRAMS

READ CYCLE

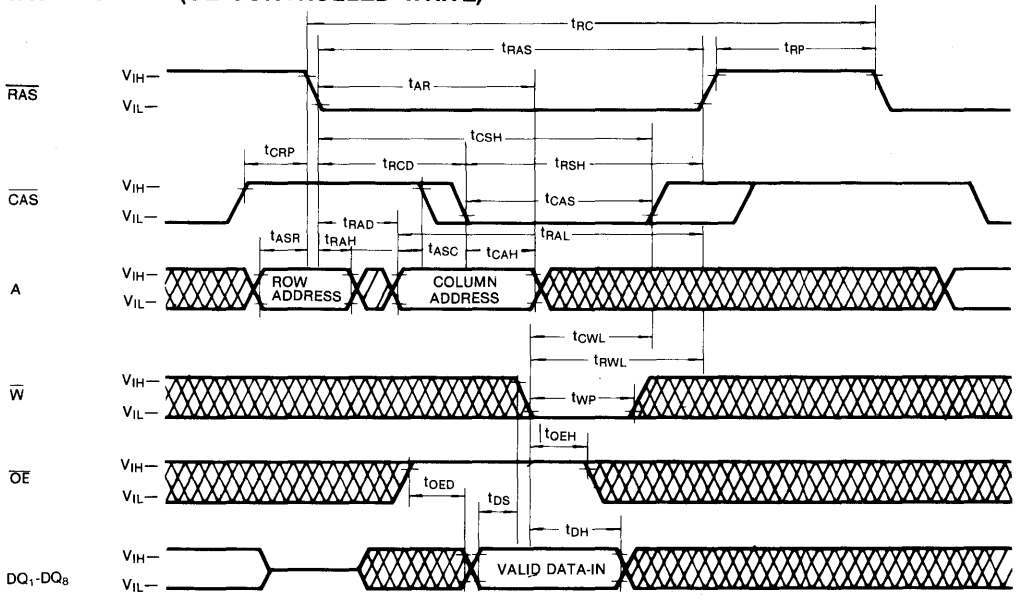


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



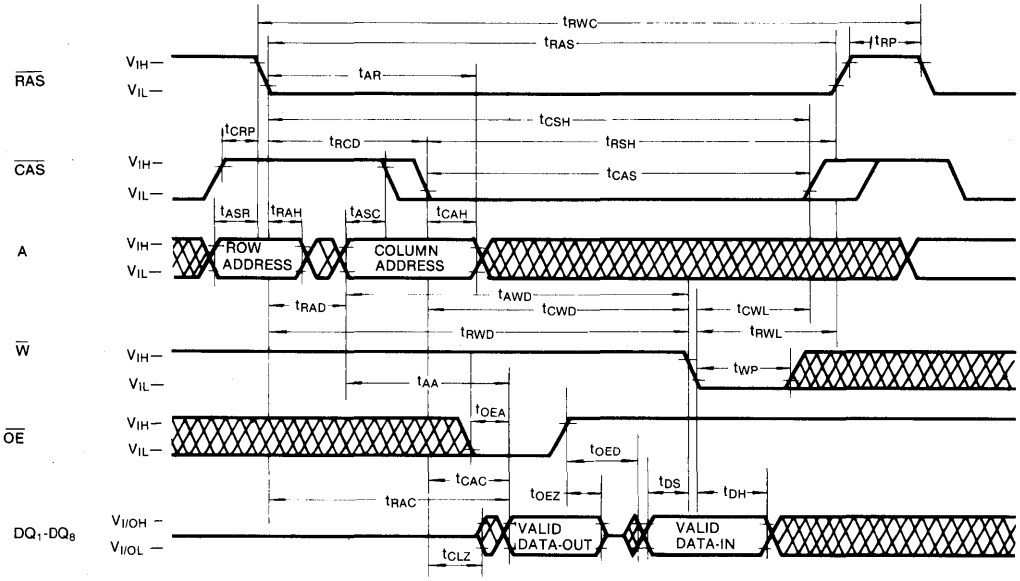
WRITE CYCLE (OE CONTROLLED WRITE)



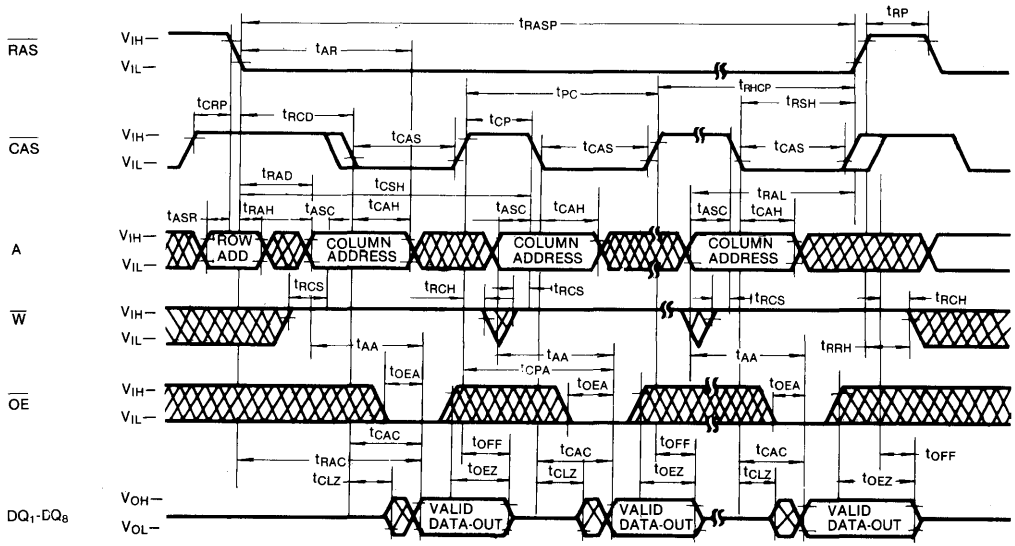
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



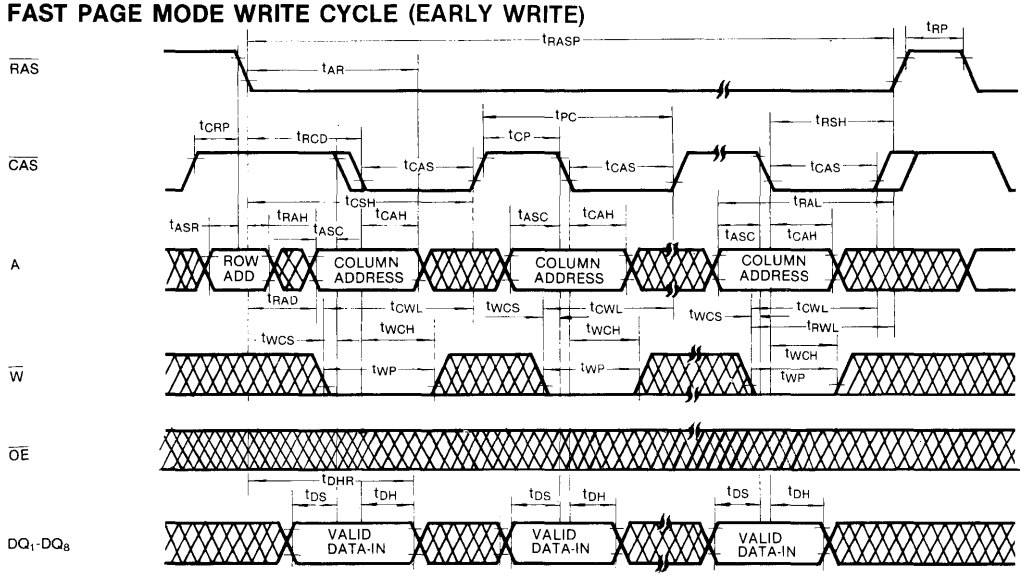
FAST PAGE MODE READ CYCLE



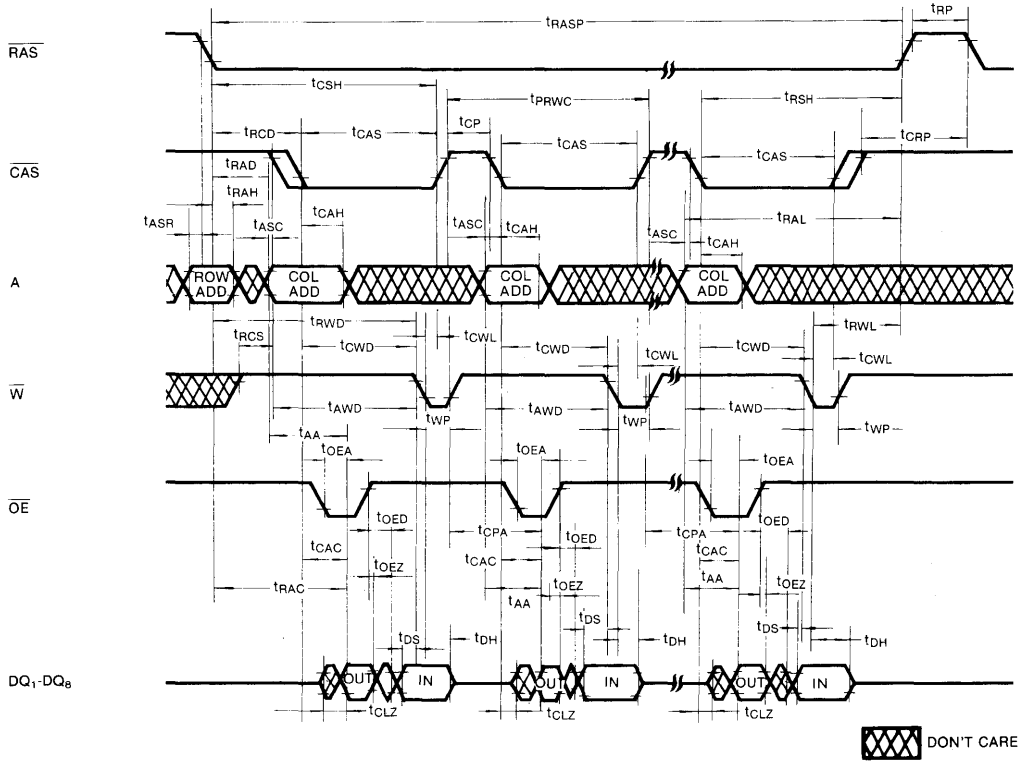
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



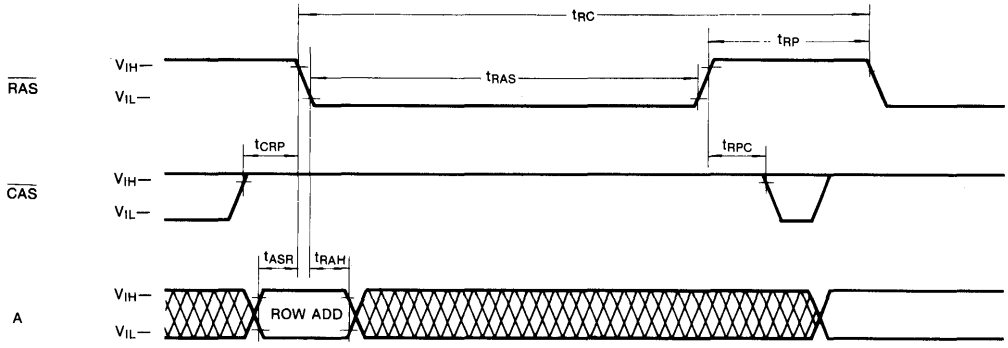
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

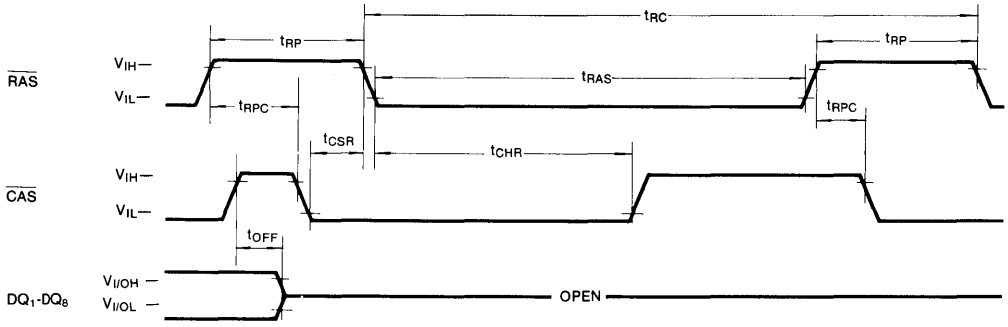
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



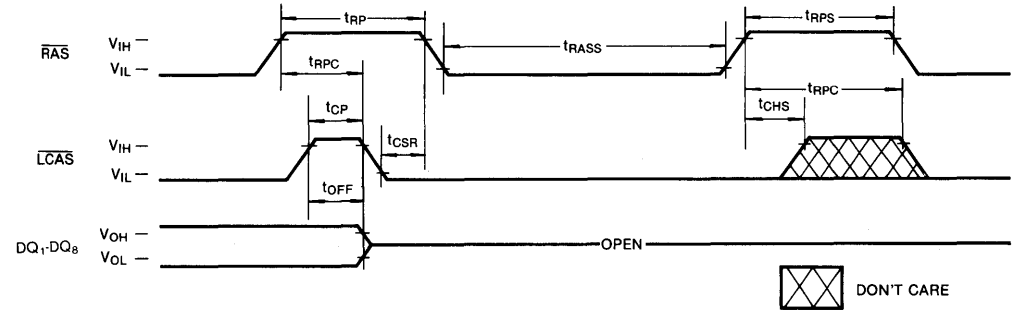
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



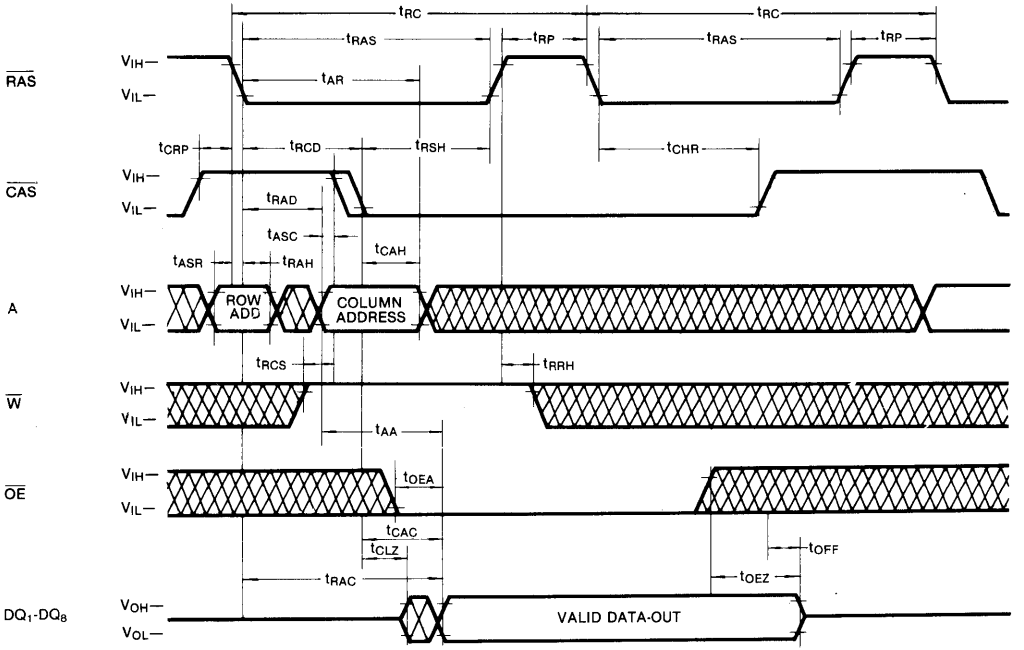
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

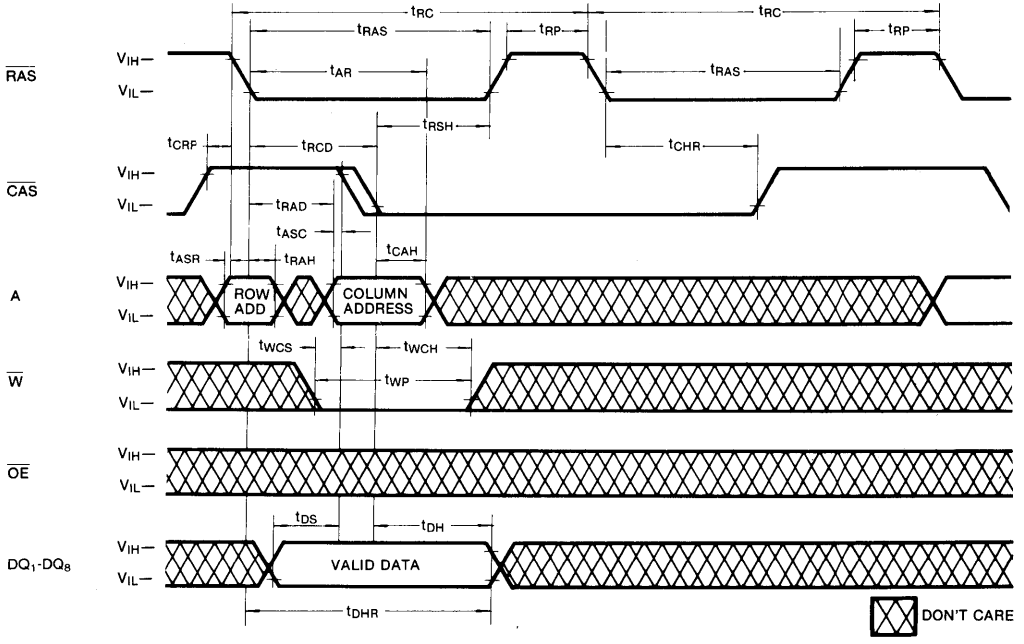


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

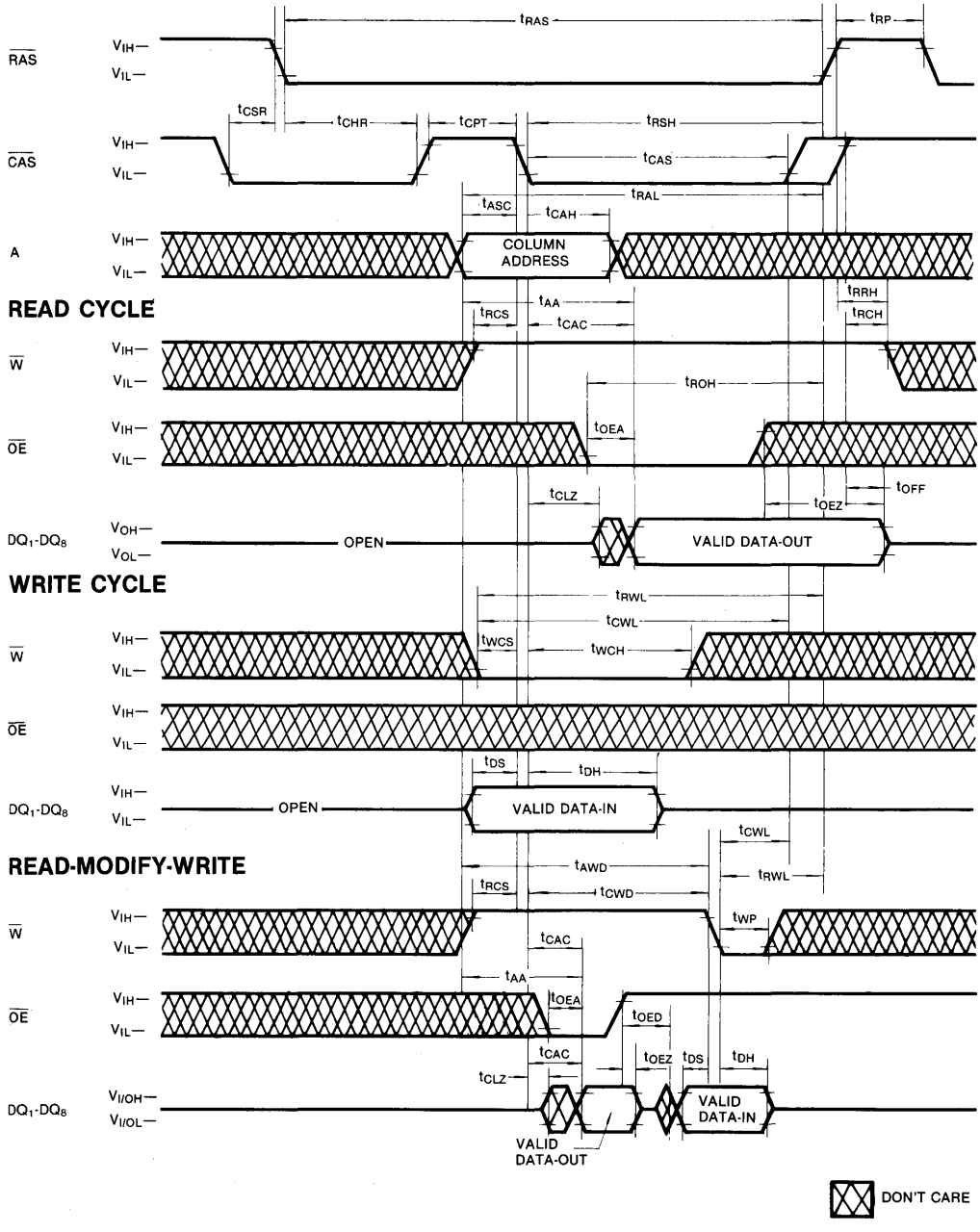


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

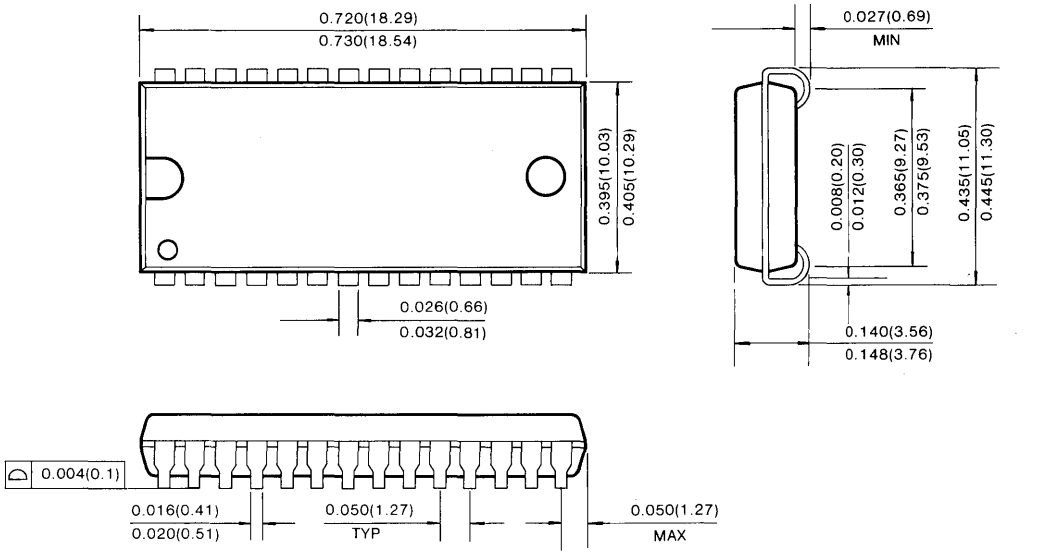
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

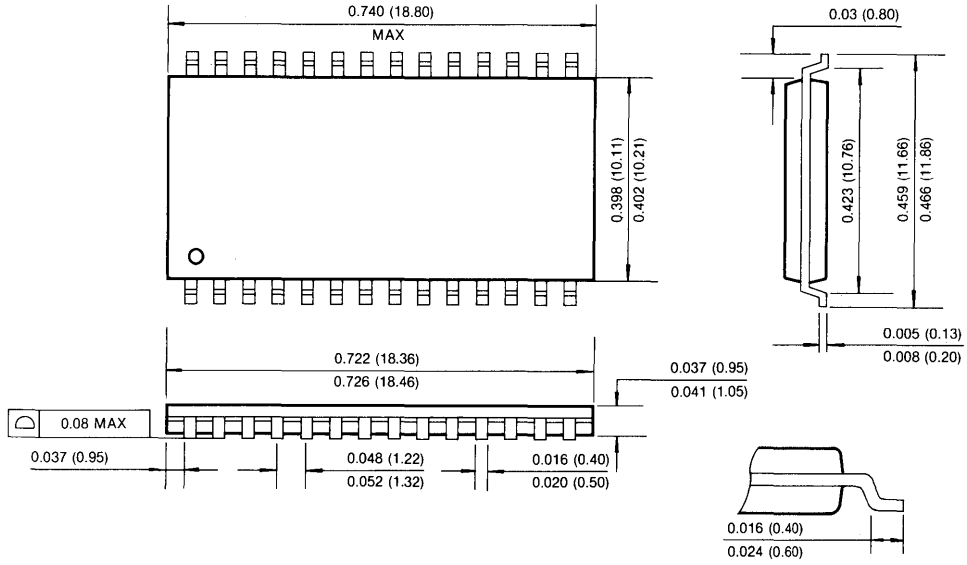
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M ×8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM48V2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Double+3.3V±0.3V power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

GENERAL DESCRIPTION

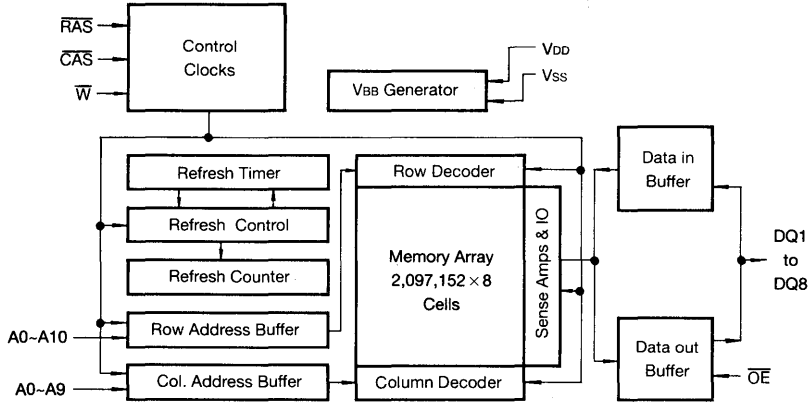
The Samsung KM48V2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

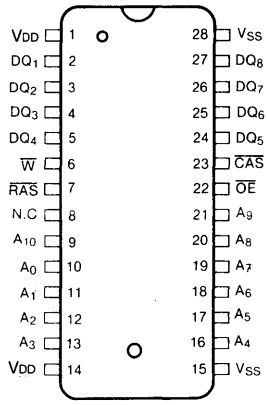
The KM48V2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

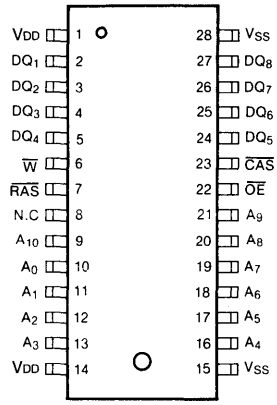


PIN CONFIGURATION (Top Views)

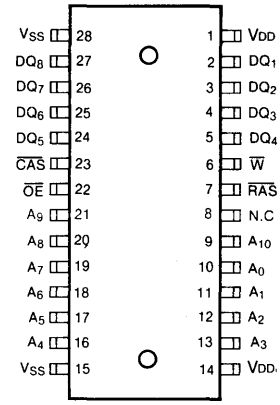
• KM48V2100 AJ/ALJ/ALLJ/ASLJ



• KM48V2100 AT/ALT/ALLT/ASLT



• KM48V2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM48V2100A/AL/ALL/ASL-7			90	mA
	KM48V2100A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2100A	I_{CC2}	-	2	mA
	KM48V2100AL			1	mA
	KM48V2100ALL			1	mA
	KM48V2100ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM48V2100A/AL/ALL/ASL-7			90	mA
	KM48V2100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2100A/AL/ALL/ASL-6	I_{CC4}	-	80	mA
	KM48V2100A/AL/ALL/ASL-7			70	mA
	KM48V2100A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2100A	I_{CC5}	-	1	mA
	KM48V2100AL			300	μA
	KM48V2100ALL			200	μA
	KM48V2100ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2100A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM48V2100A/AL/ALL/ASL-7			90	mA
	KM48V2100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=62.5μS(L-Ver.) 125μS(SL-Ver.), T_{RAS}=T_{RAS} min.~300ns	KM48V2100AL	I_{CC7}	-	400	μA
	KM48V2100ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2100ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{11})	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ commend hold time	t_{OEH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

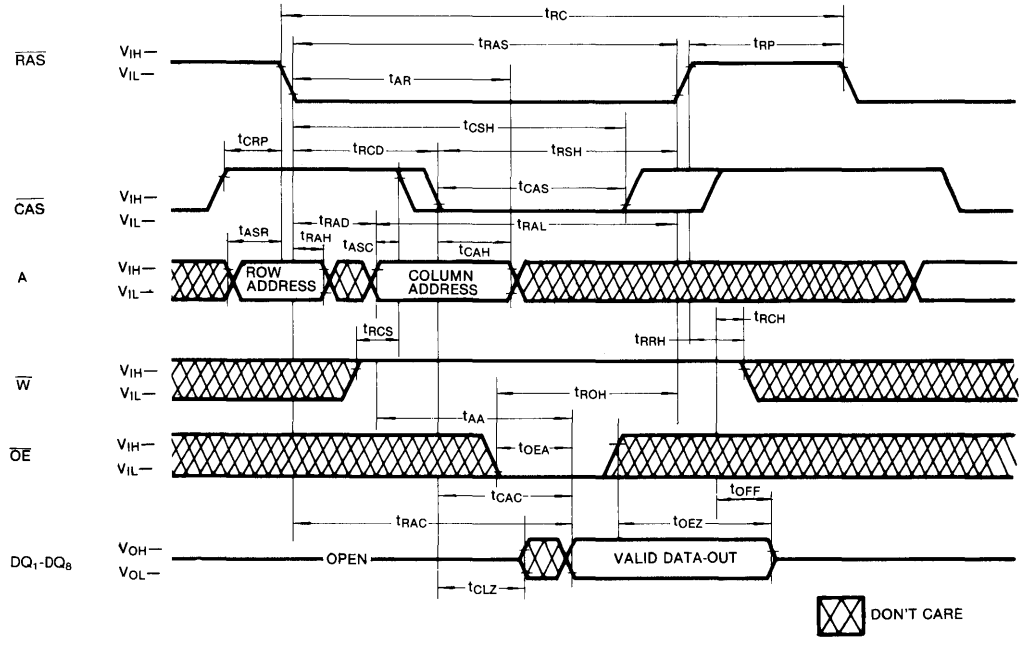
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

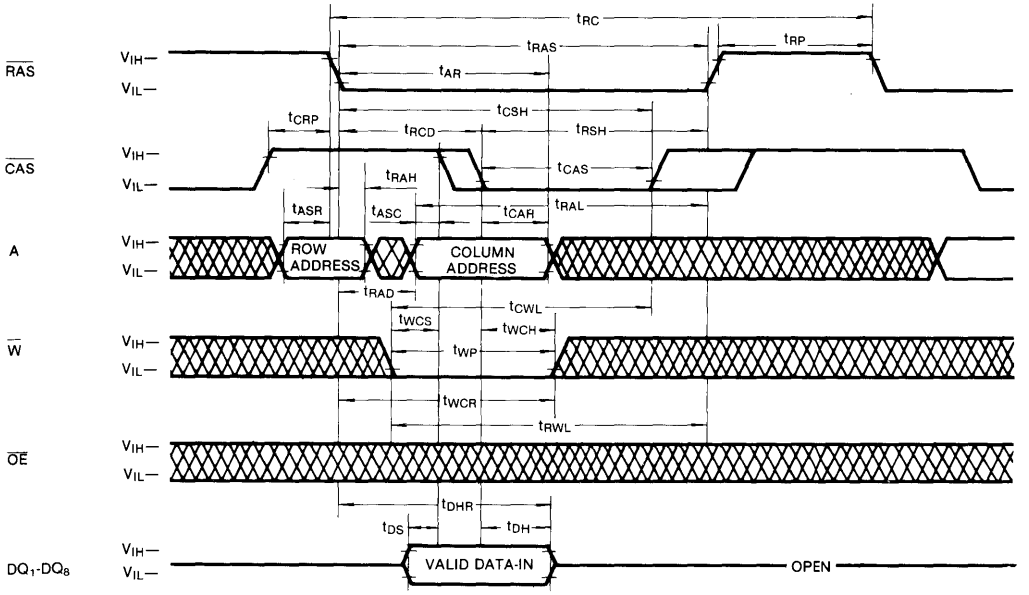
TIMING DIAGRAMS

READ CYCLE

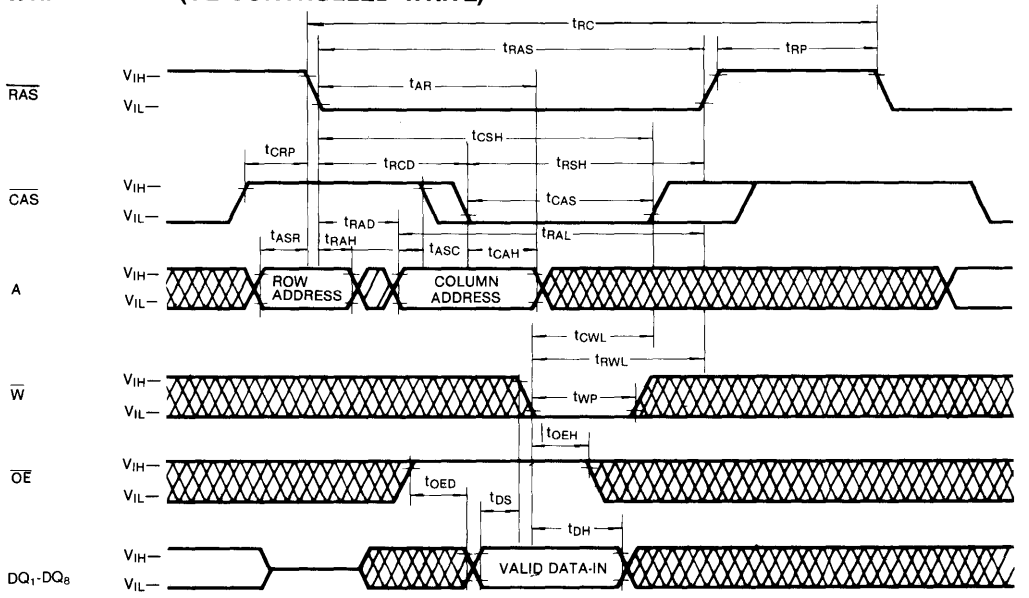


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



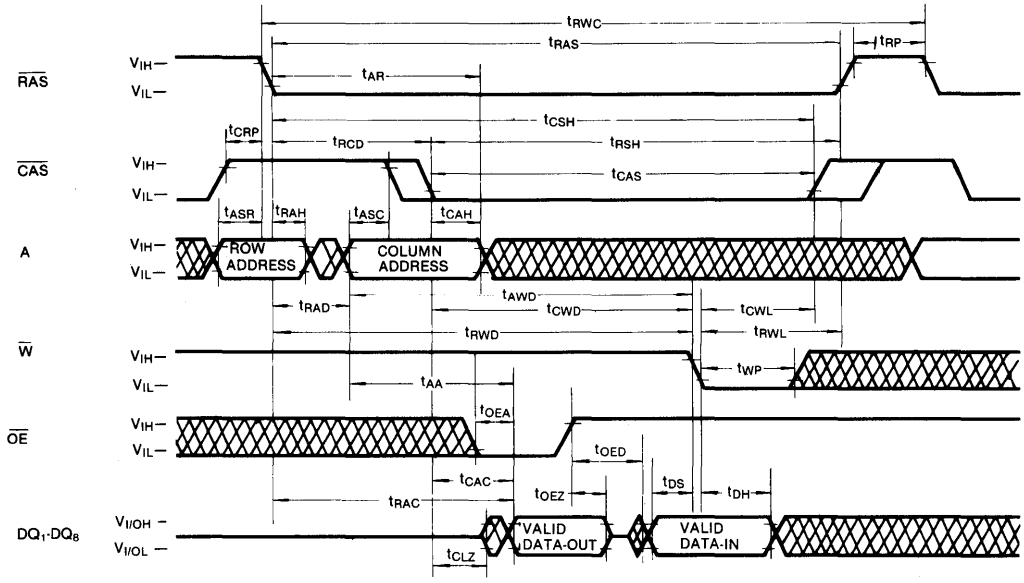
WRITE CYCLE (OE CONTROLLED WRITE)



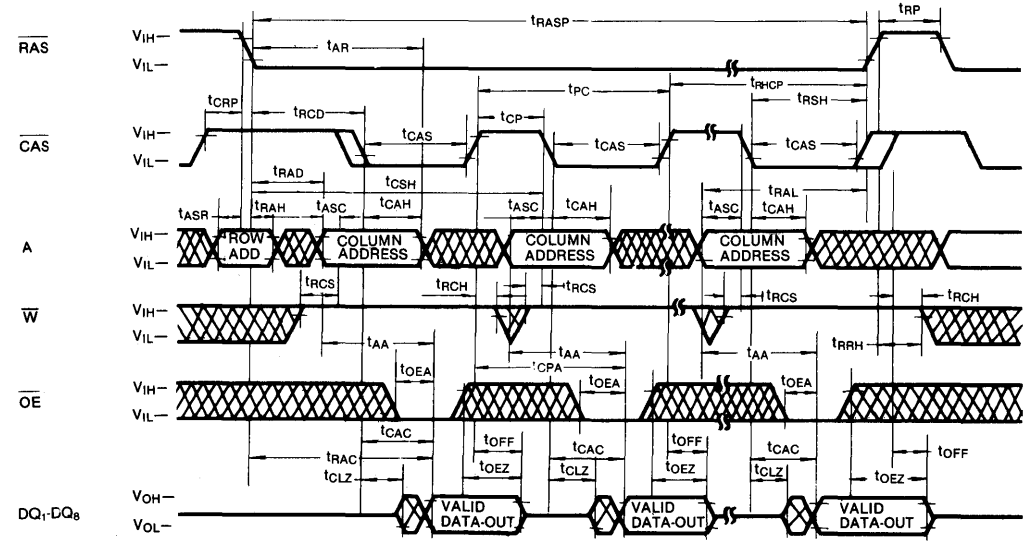
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



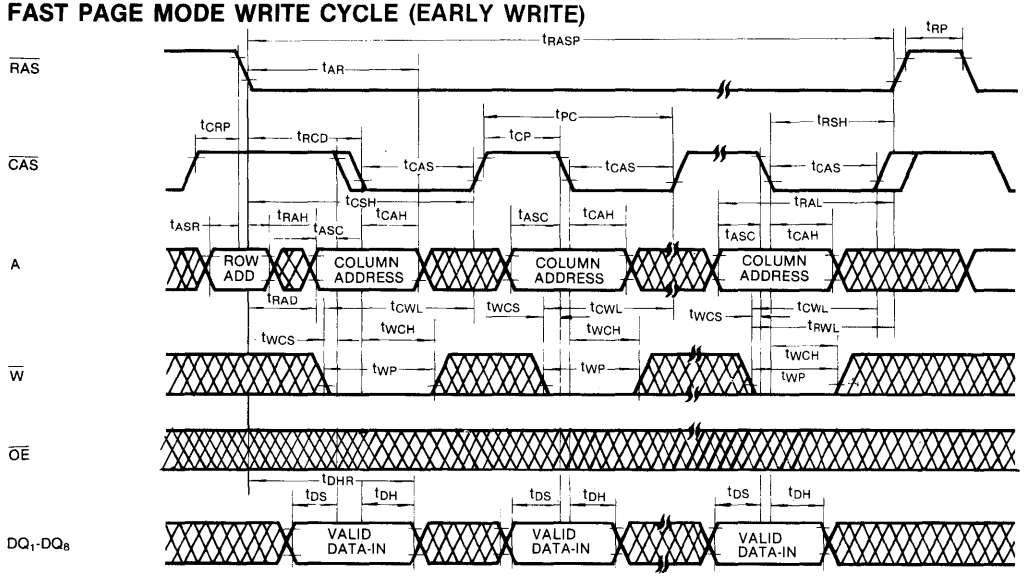
FAST PAGE MODE READ CYCLE



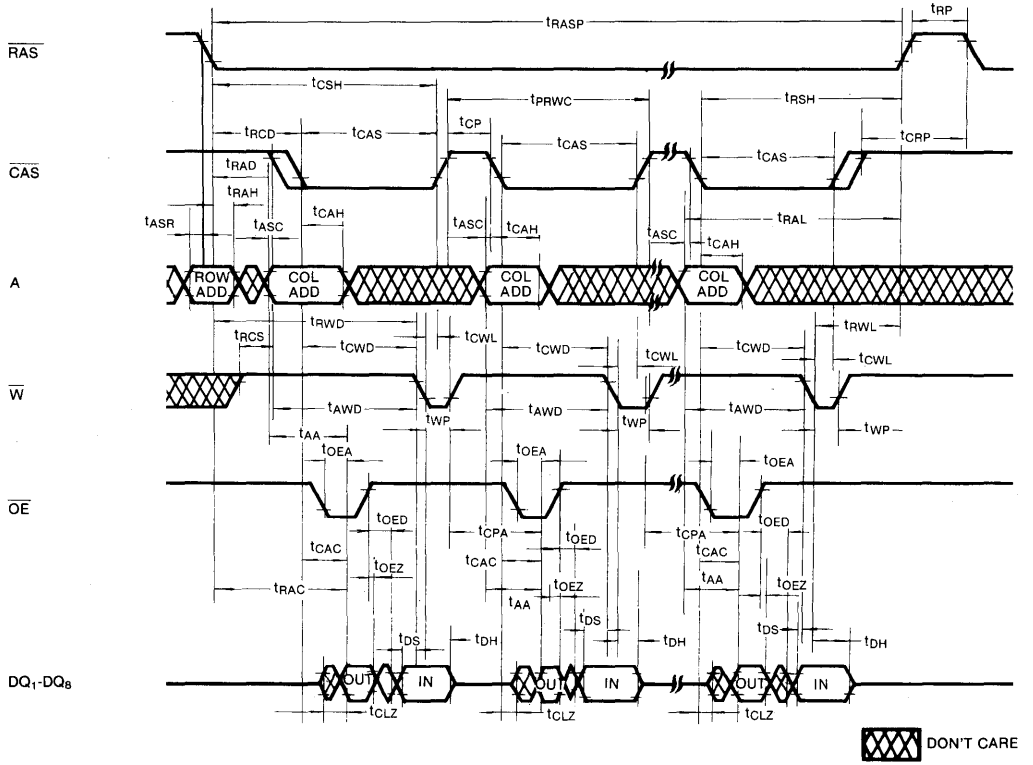
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



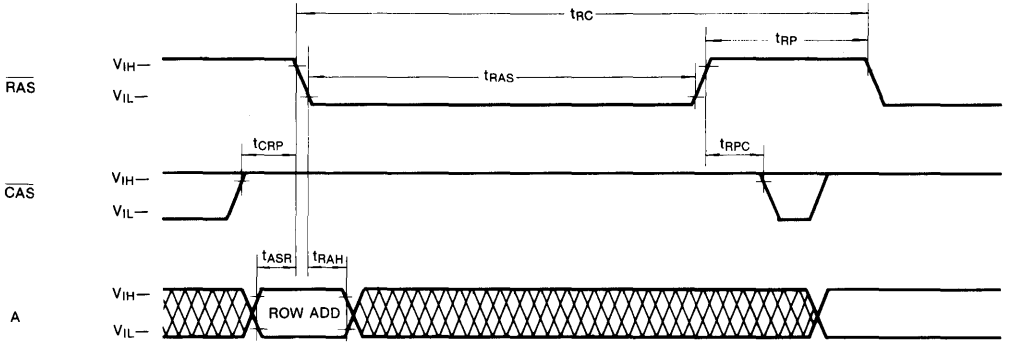
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

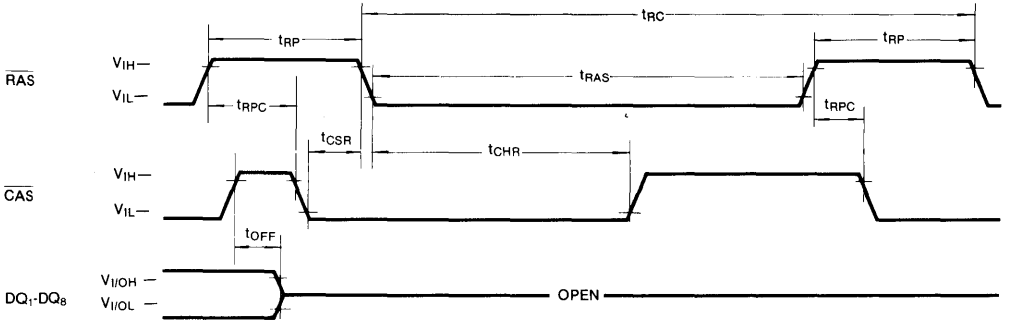
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



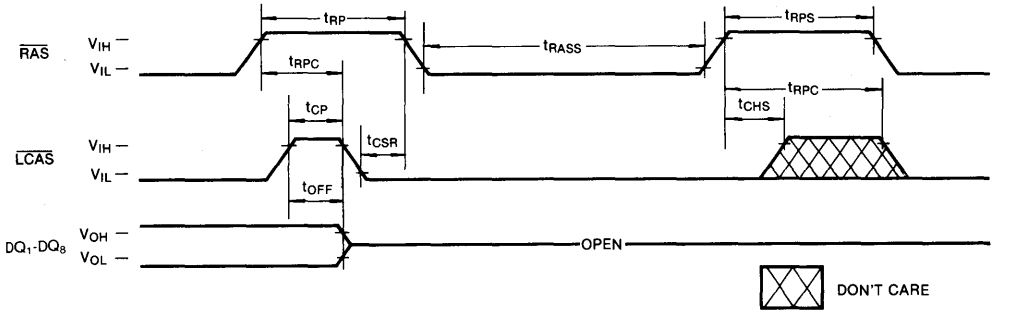
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



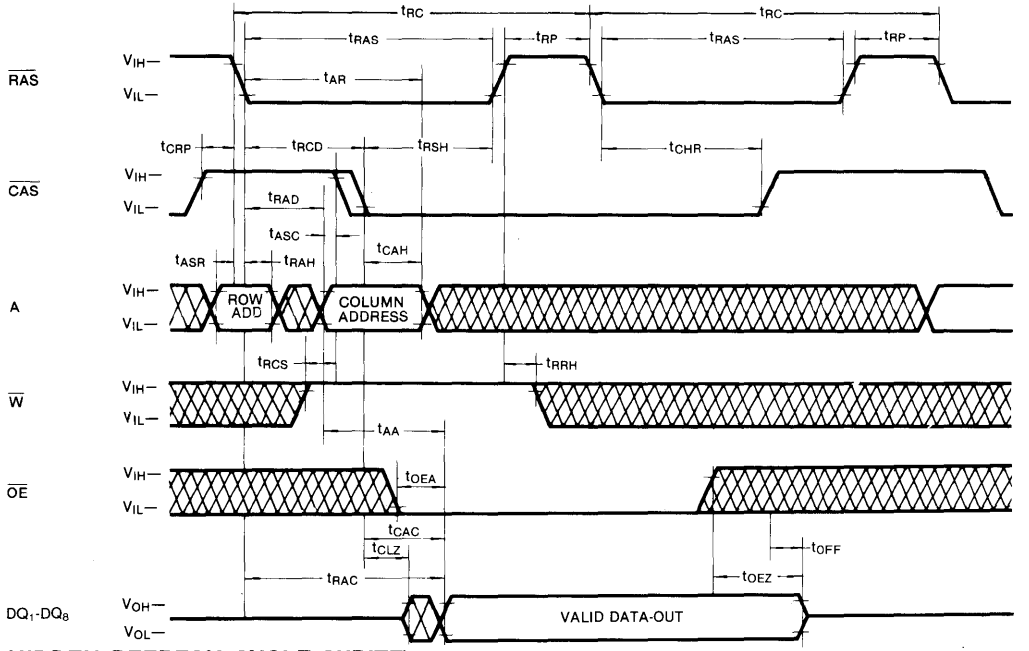
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

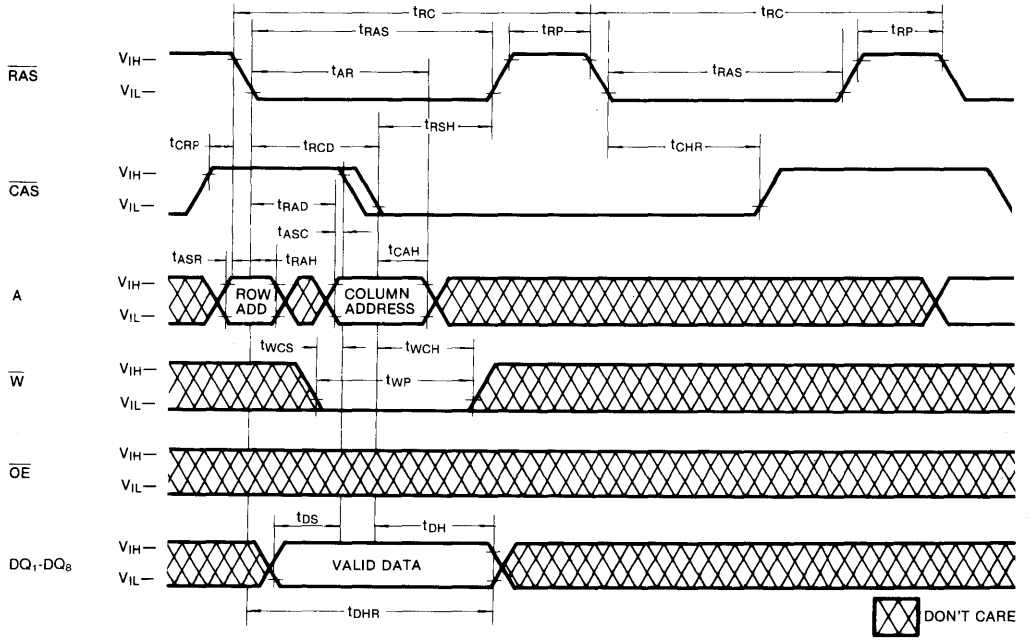


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

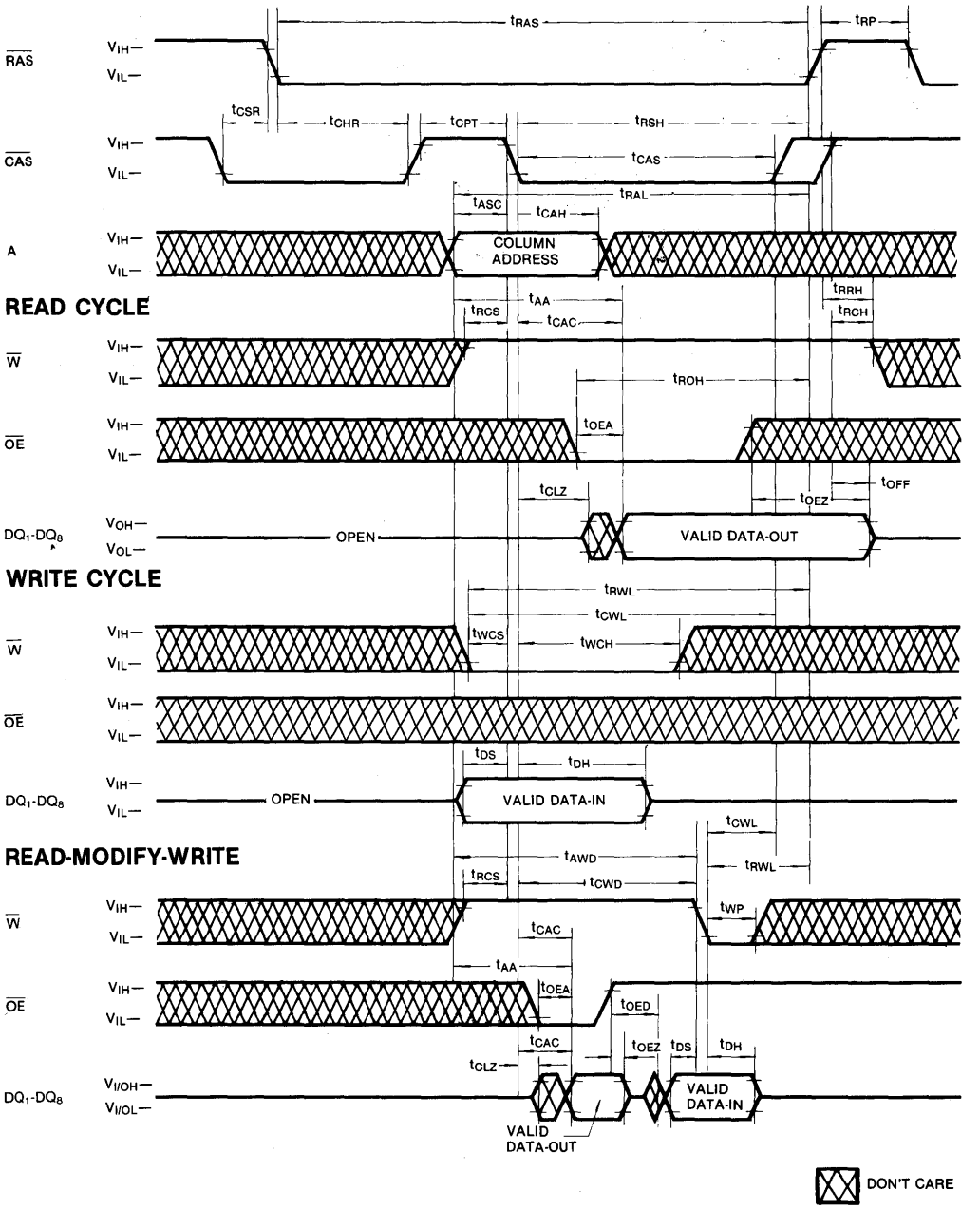


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

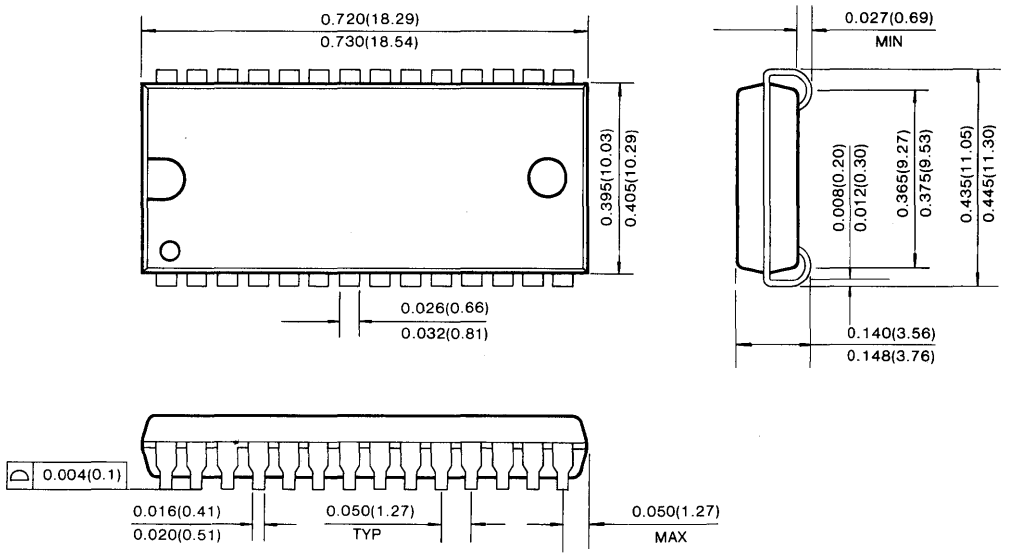
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

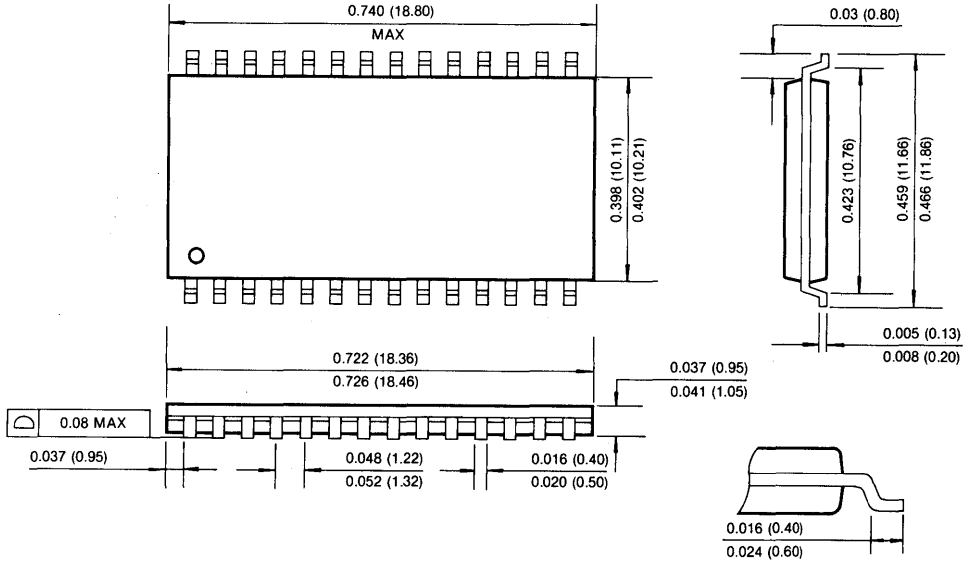
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



NOTES

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SAMSUNG ELECTRONICS CO., LTD. SHANGHAI OFFICE :

SUITE 4034,
SHERATON HUATING HOTEL,
1200 CAOXIBEILU, SHANGHAI
200030, CHINA
TEL : 021-4390707
FAX : 021-4393798

Printed in the Republic of Korea