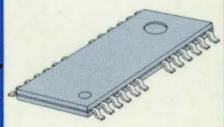
SAMSUNG

1130 - 4051

MOS Memory

1994



• Video RAM

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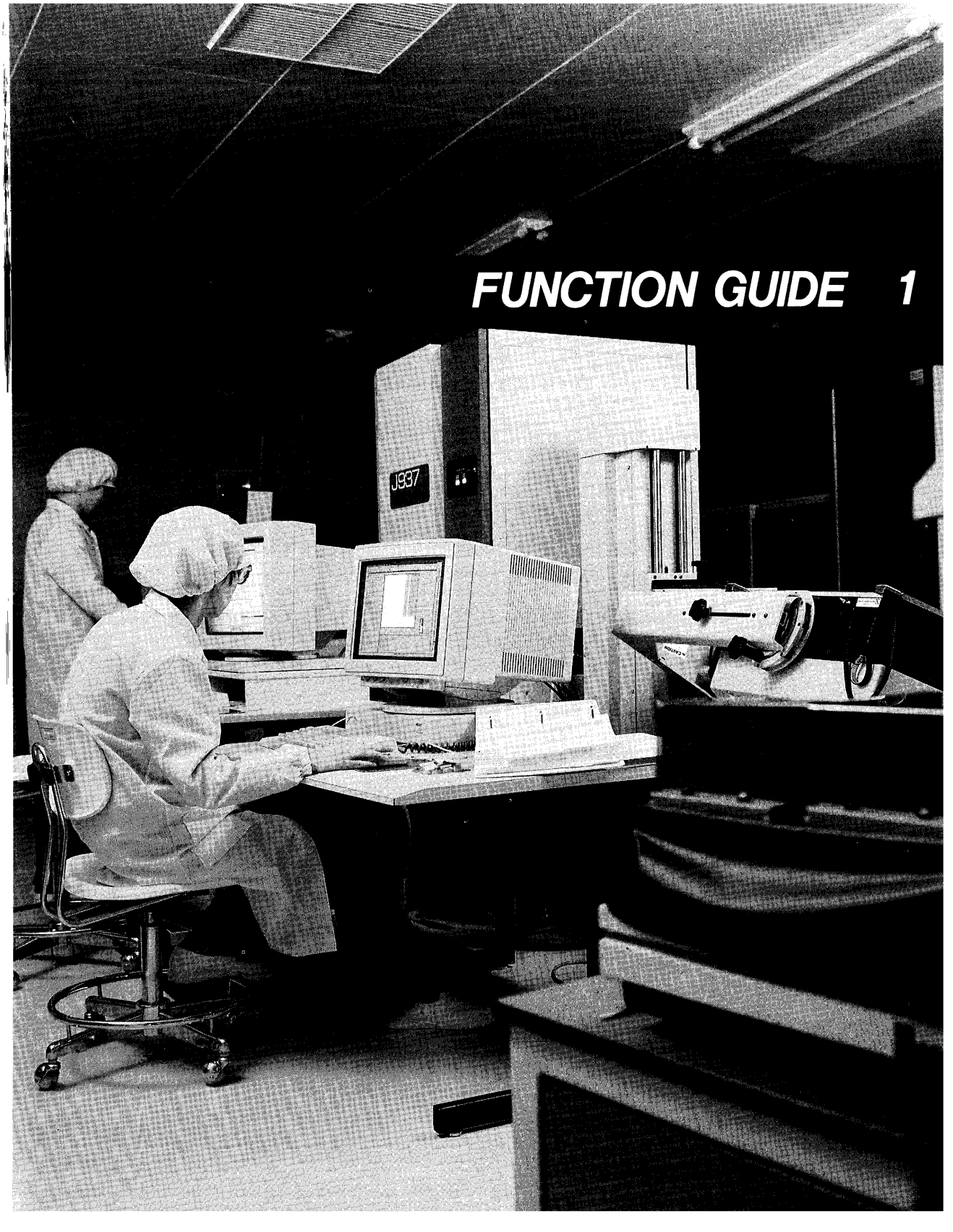
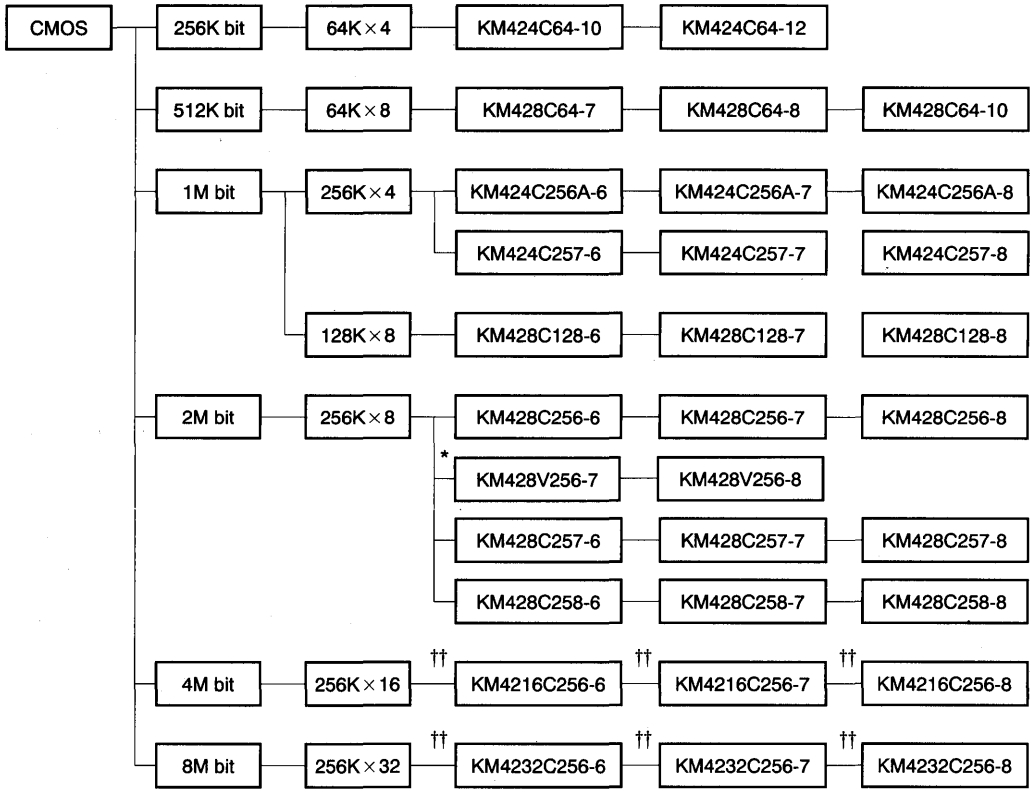


FUNCTION GUIDE 1

Video RAM



†† Under Development

Video RAM

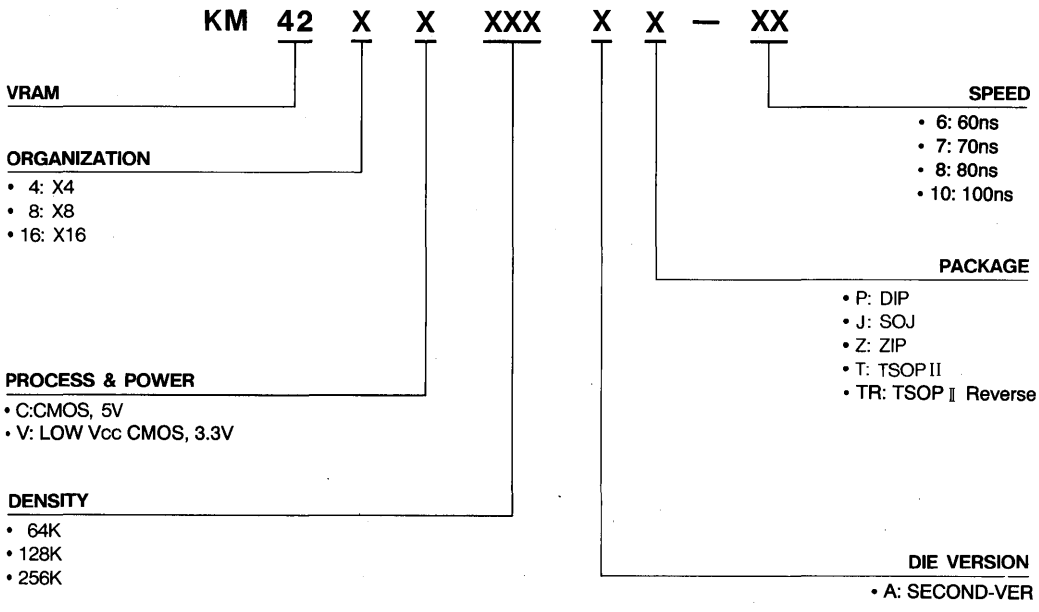
Capacity	Part Number	Orgnization	Speed(ns)	Technology	Features	Package	Remark
256K	KM424C64	64K×4	100/120	CMOS	M/F	24Pin DIP/ZIP	NOW
512K	KM428C64	64K×8	70/80/100	CMOS	M/F	40PIN SOJ	NOW
1M	KM424C256A	256K×4	60/70/80	CMOS	M/F	28Pin ZIP/SOJ	NOW
	KM424C257	256K×4	60/70/80	CMOS	E/F	28Pin ZIP/SOJ	NOW
	KM428C128	128K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
2M	KM428C256	256K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428V256	256K×8	70/80	CMOS	E/F(3.3V)	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C257	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C258	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
4M	† KM4216C256	256K×16	60/70/80	CMOS	F/F	64Pin SSOP/TSOP-Ⅱ	2Q '94

* : New Product † : Under Development

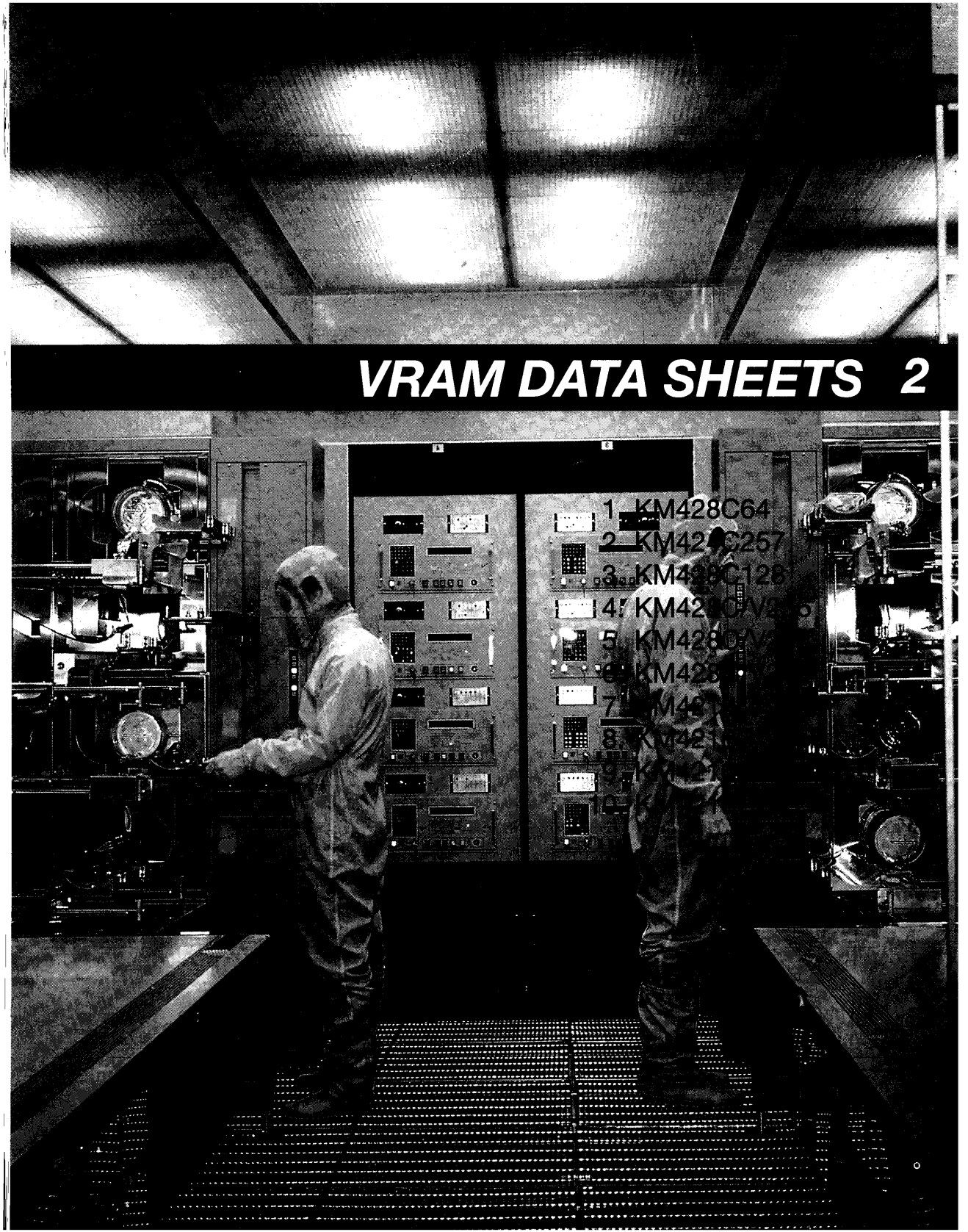
Video RAM

Density	Feature	Organization	Samsung	Micron	Toshiba	NEC	Hitachi	Ti
256K	Minimum	64K×4	KM424C64	MT42C4064		μPD41264 μPD42264	HM53461(2)	TMS4461
512K	Minimum	64K×8	KM428C64					
1M	Minimum	256K×4	KM424C256 KM424C256A		TC524256 TC524256A TC524256B TC524257	μPD42273	HM534251 HM534251A HM534252	TMS44C250 SMJ44C250
		128K×8			TC528126A TC528126B		HM538121 HM538121A	TMS48C121
	Extended	256K×4	KM424C257	MT42C4256 MT42C4255	TC524258A TC524258B TC524259B	μPD42274	HM534253A	TMS44C251 SMJ44C251 SMJ44C251A
		128K×8	KM428C128	MT42C8128 MT42C8128	TC528128A TC528128B TC528129B	μPD42275	HM538123A	
2M	Extended	256K×8	KM428C256	MT42C8255				
	Full	256K×8	KM428C257 KM428C258	MT42C8256 MT42C8254	TC528267	μPD482234 μPD482235	HM538253	
4M	Full	256K×32	KM4216C256	MT42C256K16A1				

VRAM


KM 42 X X XXX X X — XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
• V: LOW Vcc CMOS, 3.3V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 7: 70ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
• TR: TSOP II Reverse
DIE VERSION
• A: SECOND-VER

VRAM DATA SHEETS 2



64K X 8 Bit CMOS Video RAM

FEATURES

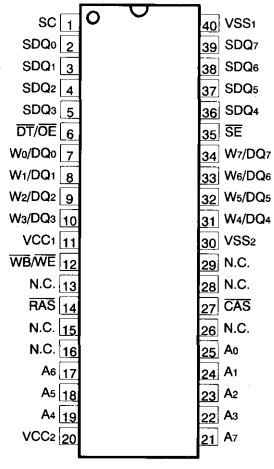
- **Dual port Architecture**
  64K x 8 bits RAM port
  256 x 8 bits SAM port
- **Performance range :**

Parameter \ Speed	-7	-8	-10
RAM access time (t_{RAC})	70ns	80ns	100ns
RAM access time (t_{CAC})	20ns	20ns	25ns
RAM cycle time (t_{RC})	130ns	150ns	180ns
RAM page mode cycle (t_{PC})	45ns	50ns	60ns
SAM access time (t_{SCA})	20ns	20ns	25ns
SAM cycle time (t_{SCC})	25ns	25ns	30ns
RAM active current	85mA	80mA	70mA
SAM active current	45mA	40mA	40mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read Transfer and Write Transfer**
- **Real time read transfer capability**
- **Write per bit masking on RAM write cycles**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 256 Cycle/4ms**
- **Single +5V± 10% Supply Voltage**
- **Plastic 40-Pin 400 mil SOJ**

PIN CONFIGURATION (TOP VIEWS)

40 Pin 400 mil SOJ



GENERAL DESCRIPTION

The Samsung KM428C64 is a CMOS 64K x 8 bit Dual Port DRAM. It consists of a 64K x 8 dynamic random access memory (RAM) port and 256 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 256 bit rows of 2048 bits. It operates like a conventional 64K x 8 CMOS DRAM. The RAM port has a write per bit mask capability.

The SAM port consists of four 256 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

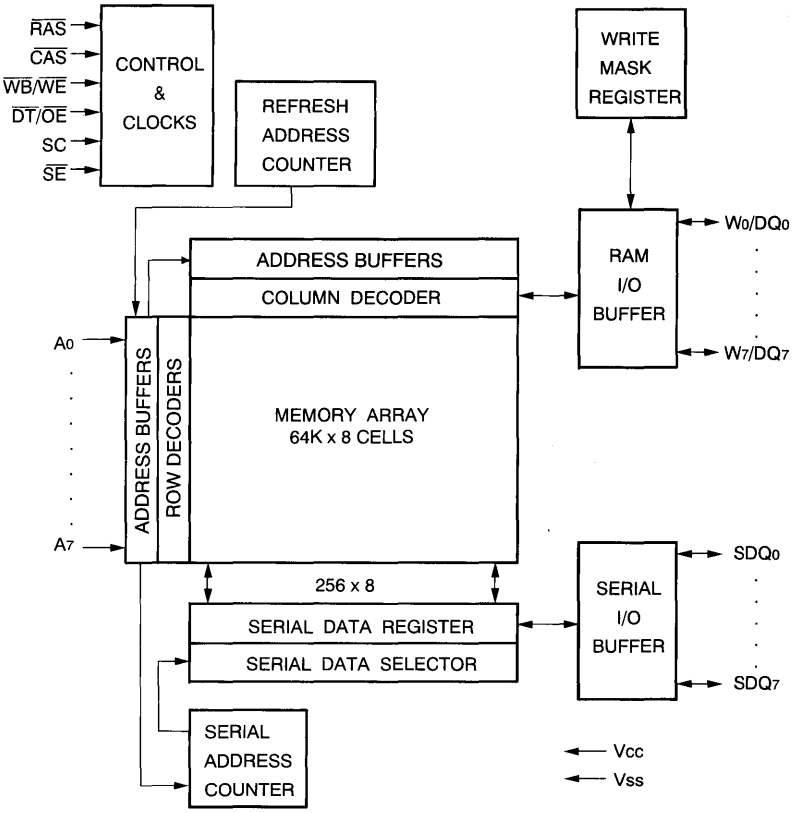
Refresh is accomplished by familiar DRAM refresh modes. The KM428C64 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN DESCRIPTION

Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ input is a multifunction pin. when $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
$\overline{SE}$	IN	In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", Serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "High"
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
V_{CC}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground
NC	—	No Connection

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code		RAS			Address*1		DQi Input*2		Write Mask	Function
	CAS	DT/OE	WE	SE	RAS	CAS	RAS	CAS/WE		
CBR	0	X	X	X	X	X	X	–	–	CBR Refresh
ROR	1	1	X	X	Row	-	X	–	–	RAS-Only Refresh
RW	1	1	1	X	Row	Col.	X	Data	No	Normal DRAM R/W(No Mask)
RW/NM	1	1	0	X	Row	Col.	WMi	Data	Use	Masked DRAM Write(New Mask)
RT	1	0	1	X	Row	Tap	X	X	–	Read Transfer
PWT	1	0	0	1	Row*3	Tap	x	X	–	Pesudo Write Transfer

X: Don't Care, -: Not Applicable, Tap: SAM Start(column)Address

Note

*1 : These column show what must be present on the A_0~A_7 inputs at the falling edge of RAS and CAS.

*2 : These column show what must be present on the DQ_0~DQ_7 outputs at the falling edge of RAS, CAS or WB/WE, whichever is later.

*3 : The Row that is addressed will be refreshed.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN},V_{OUT}	-1 to + 7.0	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	℃
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70° C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)			SAM port	Symbol	KM428C64			Unit
					-7	-8	-10	
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)			Standby	I_{CC1}	85	80	70	mA
			Active	I_{CC1A}	130	120	110	mA
Standby Current	$\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ =V_{IH}	$\overline{SE}$ = V_{IH}, SC= V_{IL}	Standby	I_{CC2}	5	5	5	mA
		$\overline{SE}$ = V_{IL}, SC= Cycling	Active	I_{CC2A}	45	40	40	mA
$\overline{RAS}$ Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ tRC=min)			Standby	I_{CC3}	85	80	70	mA
			Active	I_{CC3A}	130	120	110	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ tPC=min)			Standby	I_{CC4}	65	60	50	mA
			Active	I_{CC4A}	110	100	90	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)			Standby	I_{CC5}	85	80	70	mA
			Active	I_{CC5A}	130	120	110	mA
Data Transfer Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)			Standby	I_{CC6}	115	110	100	mA
			Active	I_{CC6A}	160	150	140	mA

*NOTE: Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open.

I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, address transition should be changed only while $\overline{RAS}$=V_{IL}

In I_{CC4} address transition should be changed only once while $\overline{CAS}$ = V_{IH}.

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$ +0.5V, all other pins not under test=0 volts)	I_{IL}	-10	10	μ A
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μ A
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_7)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, SE, SC)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF

AC CHARACTERISTICS (0 ℃≤T_A≤70 ℃, Vcc=5.0V±10%, See notes 1,2)

Parameter	Symbol	70ns		80ns		100ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	175		200		240		ns	
Fast page mode cycle time	t_{PC}	45		50		60		ns	
Fast page mode read-modify-write	t_{PRWC}	85		90		115		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3
Access time from column address	t_{AA}		35		40		50	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	3	15	3	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	25	10K	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	70ns		80ns		100ns		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR Counter Test)	t_{CPT}	10		10		15		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		20		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		45		50		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay(Fast Page mode)	t_{CPWD}	65		70		85		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	95		105		130		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	60		65		80		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		10		20		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from output enable	t_{OEA}		20		20		25	ns	
Output enable to data input delay	t_{OED}	15		15		20		ns	
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	3	15	3	20	ns	7
Output enable command hold time	t_{OEH}	15		15		20		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period(256 cycle)	t_{REF}		4		4		4	ms	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	70ns		80ns		100ns		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	10		15		15		ns	
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		15		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		15		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	tRTH	60		65		80		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	tCTH	20		25		30		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	tATH	25		30		35		ns	
$\overline{SE}$ set-up time referenced to $\overline{RAS}$	tESR	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	tREH	10		15		15		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	50		60		70		ns	
$\overline{DT}$ precharge time	tTP	20		25		30		ns	
$\overline{RAS}$ to first SC delay(read transfer)	tRSD	70		80		100		ns	
$\overline{CAS}$ to first SC delay(read transfer)	tCSD	30		35		50		ns	
Col. Addr.to first SC delay(read transfer)	tASD	40		40		55		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	tTSD	10		15		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	tSRS	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	tSRD	20		25		25		ns	
$\overline{RAS}$ to serial input delay time	tSDD	40		50		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	tSDZ	10	30	10	35	10	50	ns	7
Serial Input to first SC delay time	tSZS	0		0		0		ns	
SC cycle time	tSCC	25		25		30		ns	
SC pulse width(SC high time)	tSC	7		7		10		ns	
SC precharge(SC low time)	tSCP	7		7		10		ns	
Access time from SC	tSCA		20		20		25	ns	4
Serial output hold time from SC	tSOH	5		5		5		ns	
Serial input set-up time	tSDS	0		0		0		ns	
Serial input hold time	tSDH	15		15		20		ns	
Access time from $\overline{SE}$	tSEA		20		20		25	ns	4
$\overline{SE}$ pulse width	tSE	20		25		25		ns	
$\overline{SE}$ precharge time	tSEP	20		25		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	3	15	3	15	3	15	ns	7
Serial input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	

AC CHARACTERISTICS (Continued)

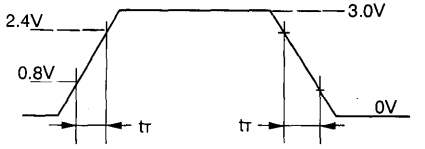
Parameter	Symbol	70ns		80ns		100ns		Units	Notes
		Min	Max	Min	Max	Min	Max		
Serial write enable set-up time	t_{SWS}	5		5		5		ns	
Serial write enable hold time	t_{SWH}	15		15		20		ns	
Serial write disable set-up time	t_{SWIS}	5		5		5		ns	
Serial write disable hold time	t_{SWIH}	15		15		20		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8SC cycles before proper device operation is achieved. If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level: V_{OH}/V_{OL}=2.0/0.8V
4. SAM port outputs are measured with a load equijalent to 1TTL load and 30pF
   D_{OUT} comparator level: V_{OH}/V_{OL}=2.0/0.8V
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), t_{SDZ}(max) and t_{SEZ}(max), define the time at which the output achieves the open circuit condition and are not reverenced to V_{OH} or V_{OL}.
8. The t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min)and $t_{RWD} \geq t_{RWD}$(min)and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycle.
11. Operation within the t_{RAD}(max) limit insured that t_{RCD}(max) can be met. The t_{RAD}(max) is specified as a reference point only. If the t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. During power-up $\overline{RAS}$, $\overline{DT/OE}$ must be held High or track with V_{CC}. After power-up, initial status of chip is described below.

PIN	STATUS
Tap Pointer	Invalid
Wi/DQi	Hi-Z
SAM Port	Input Mode
SDQi	Hi-Z

13. Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are reverenced from V_{IL} (max) and V_{IH}(min) with transition time=3.0ns



14. t_{WCR}, t_{DHR} are reverenced to t_{RAD}(max).

DEVICE OPERATION

The KM428C64 contains 524,288 memory locations. Sixteen address bits are required to address a particular 8bit word in the memory array. Since the KM428C64 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM428C64 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.
Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM428C64 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths.
In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C64 begin a complex sequence of events.
If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.
If $\overline{CAS}$ goes low before t_{RCD} (max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}.

The KM428C64 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Write

The KM428C64 can perform early write and read-modify -write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle. Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$, whichever is later.

Fast Page Mode

Fast page mode provides high speed read,write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Writer-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a "1" is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in table 1.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
↓	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

DEVICE OPERATION (Continued)

Data Output

The KM428C64 has a three-state output buffer which are controlled by $\overline{CAS}$ and $\overline{DT}/\overline{OE}$. When either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameter t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM428C64 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden refresh, Fast page mode Read, Fast Page Mode Read-Modify-Write.

Refresh

The data in the KM428C64 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 256 rows every 4 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter.
Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 256 row address,(A_0 ~ A_7).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM428C64 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$.

The KM428C64 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the preferred method.

Transfer Operation

1. Normal Write/Read Transfer.
   (SAM → RAM / RAM → SAM)
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM).
3. Real Time Read Transfer (On the fly Read Transfer Operation).

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register.
A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM.

The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the output mode.
In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$

Write Transfer Cycle

A write transfer cycle consist of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When consecutive write transfer operations are performed, there as a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has seen satisfied. A rising edge of the SC clock must not occur until after a specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

DEVICE OPERATION (Continued)

Table 2. Truth table for Transfer operation

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION	TRANSFER DIRECTION
↓	H	L	H	*	Read transfer cycle	RAM → SAM
	H	L	L	L	Write transfer cycle	SAM → RAM
	H	L	L	H	Pseudo write transfer cycle	—

Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A pseudo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

Serial Clock (SC)

All operation of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8 bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

Serial Input / Output (SDQ0 ~ SDQ7)

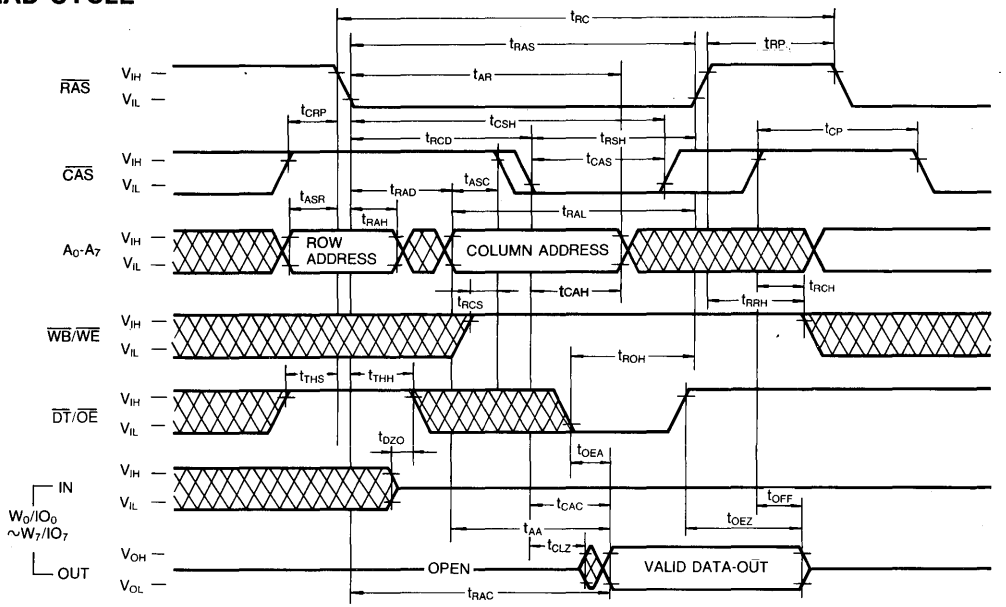
Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write transfer is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains is the input mode.

Power - up

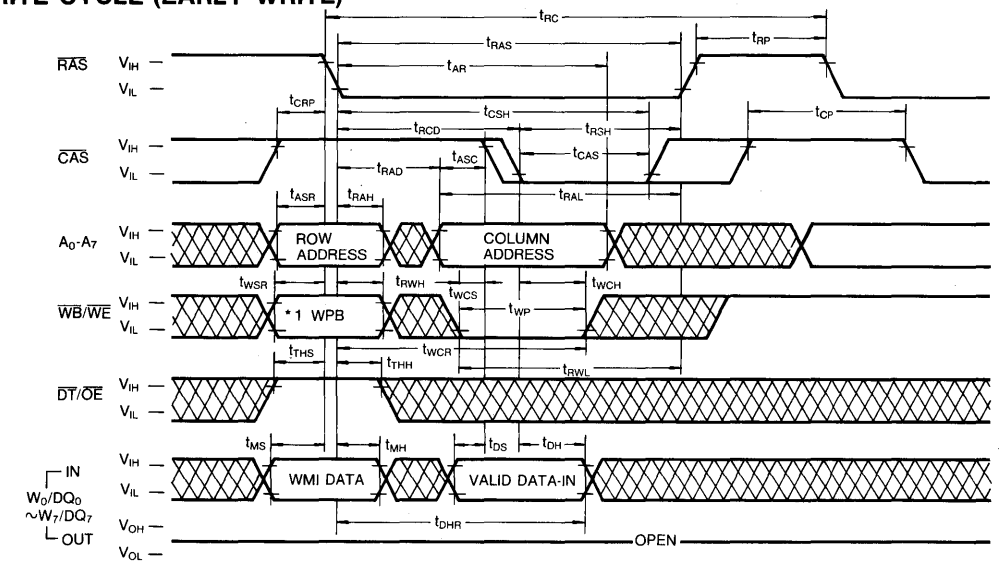
An initial pause of 200 μsec is required, after power-up followed by 8 initialization cycles before proper device operation is assured.

TIMING DIAGRAMS

READ CYCLE



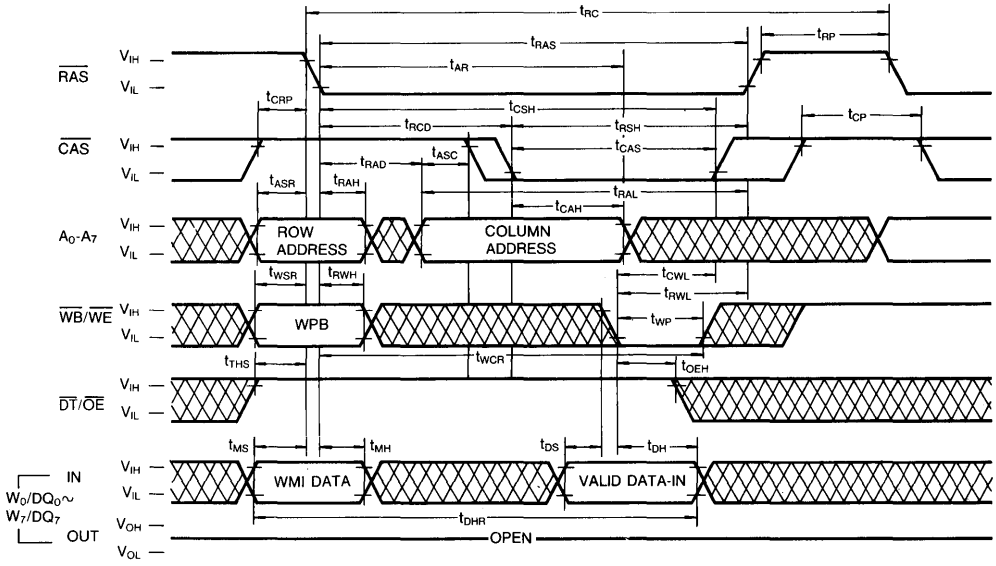
WRITE CYCLE (EARLY WRITE)



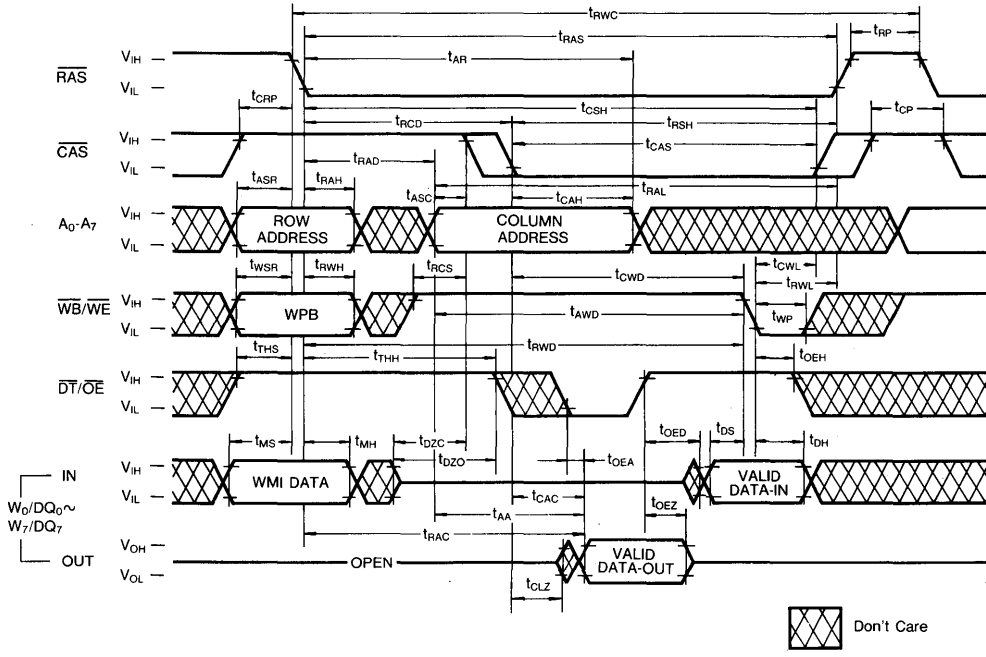
Don't Care

TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

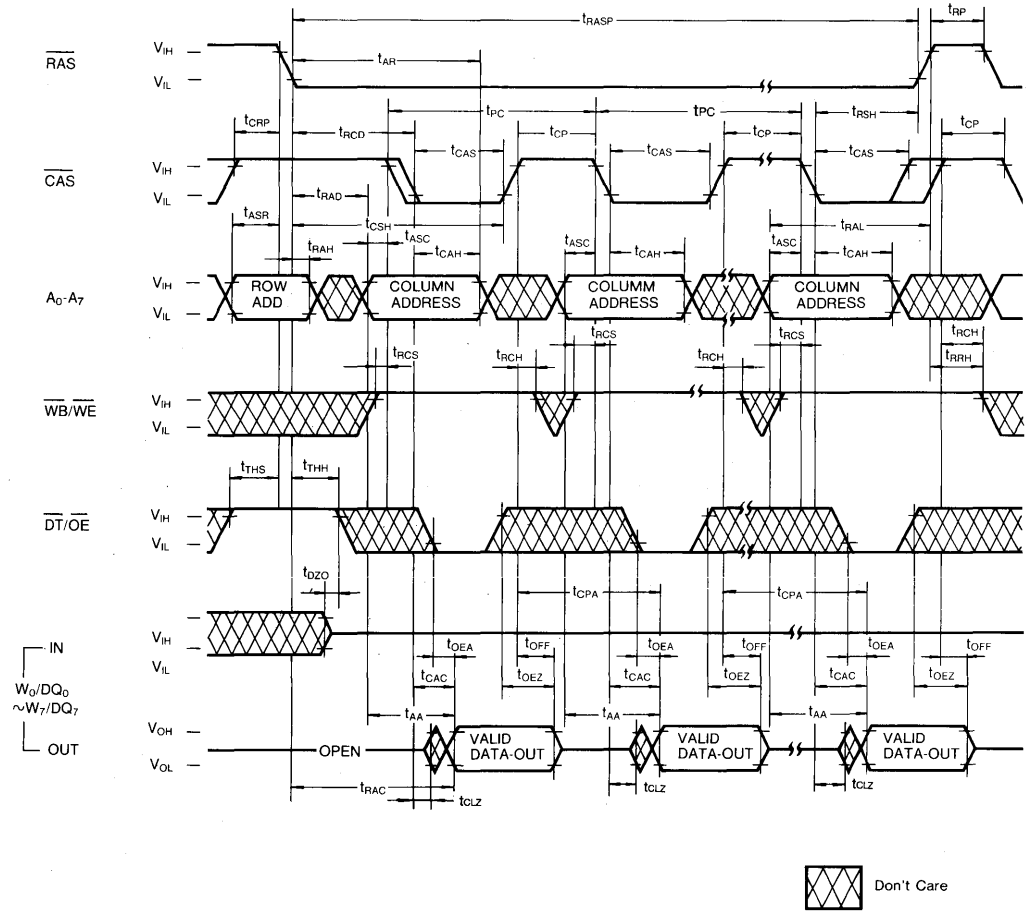


READ-WRITE/READ-MODIFY-WRITE CYCLE



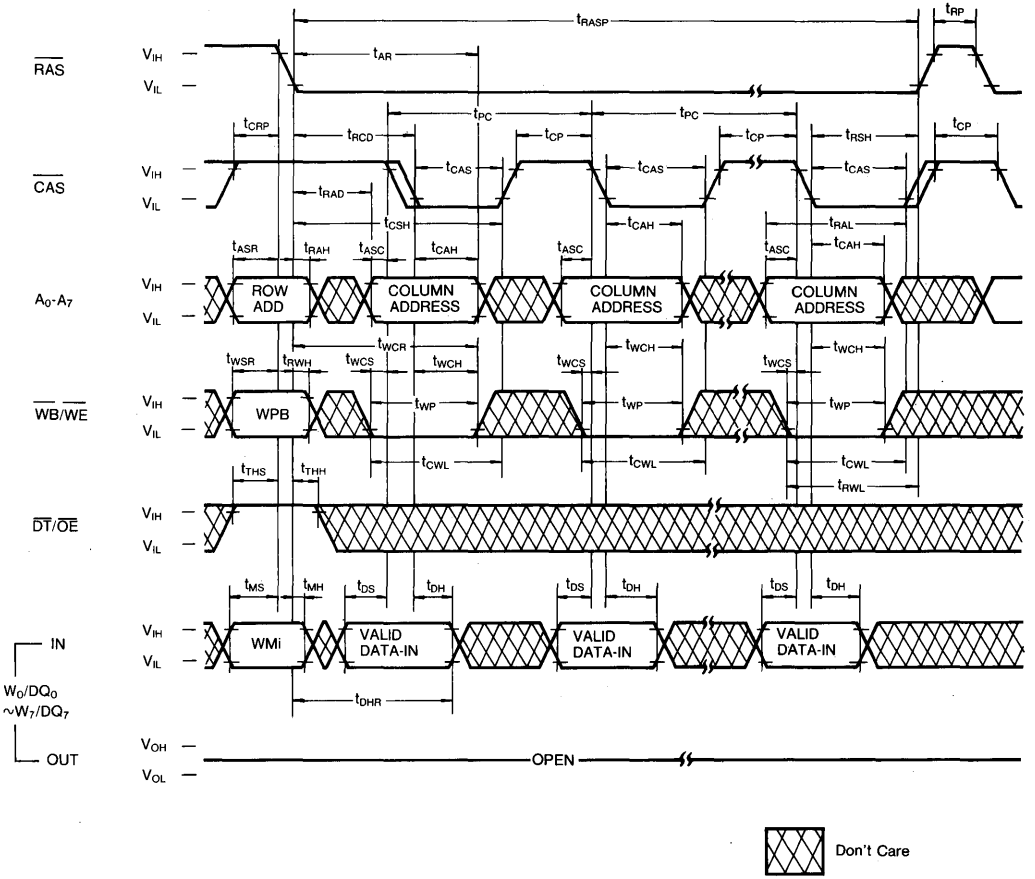
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



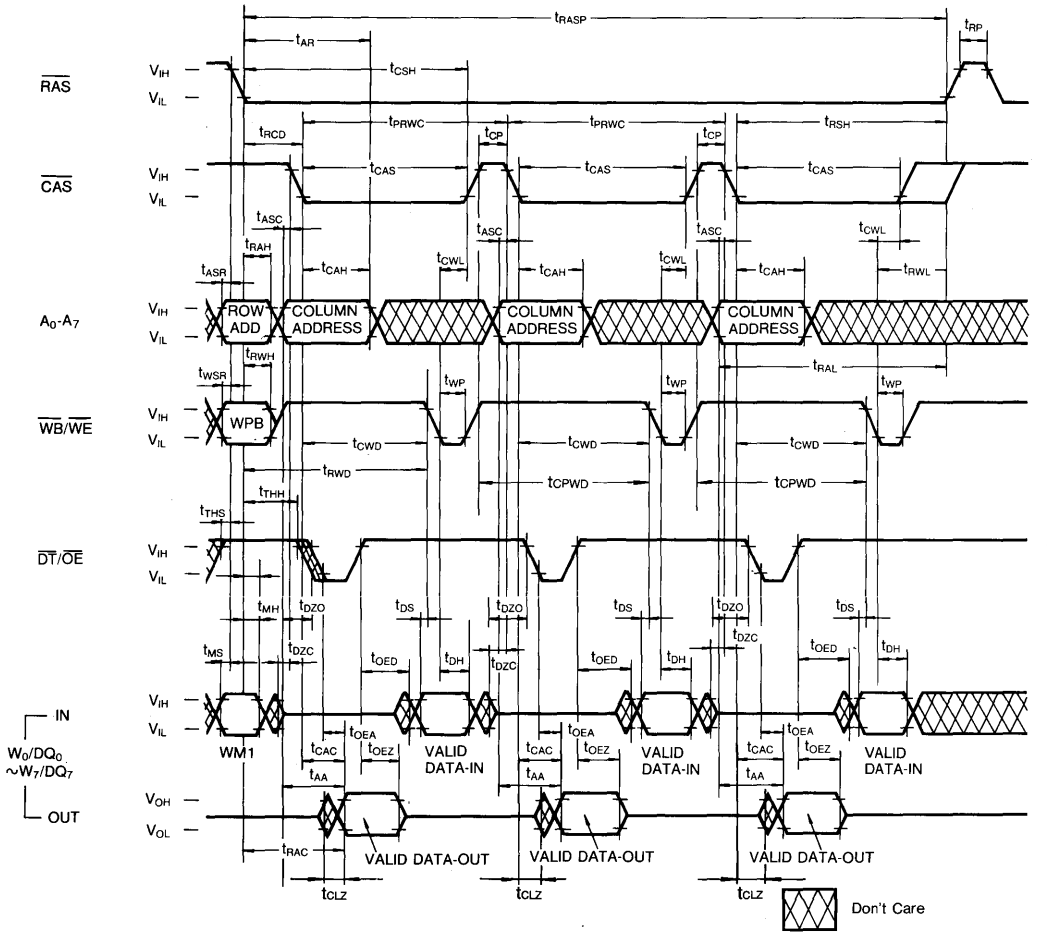
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE (EARLY WRITE)



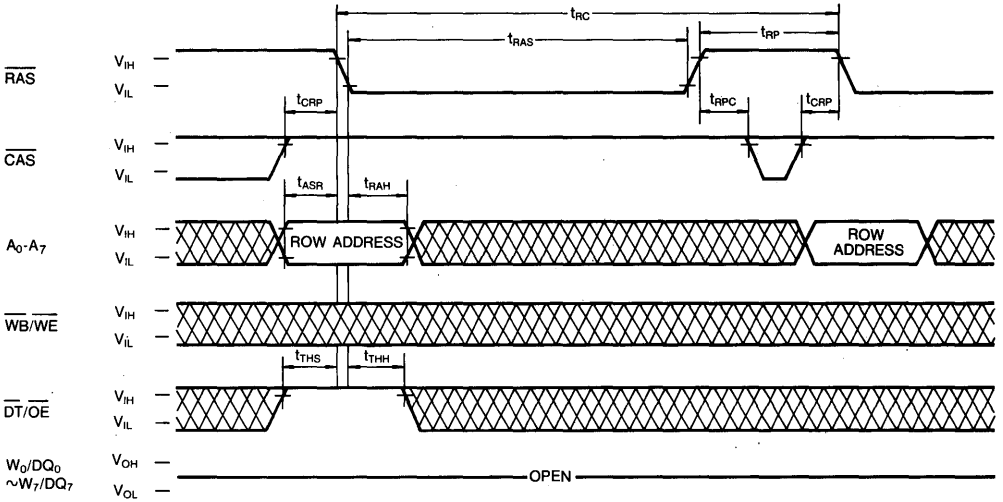
TIMING DIAGRAMS (Continued)

PAGE MODE READ-MODIFY-WRITY CYCLE

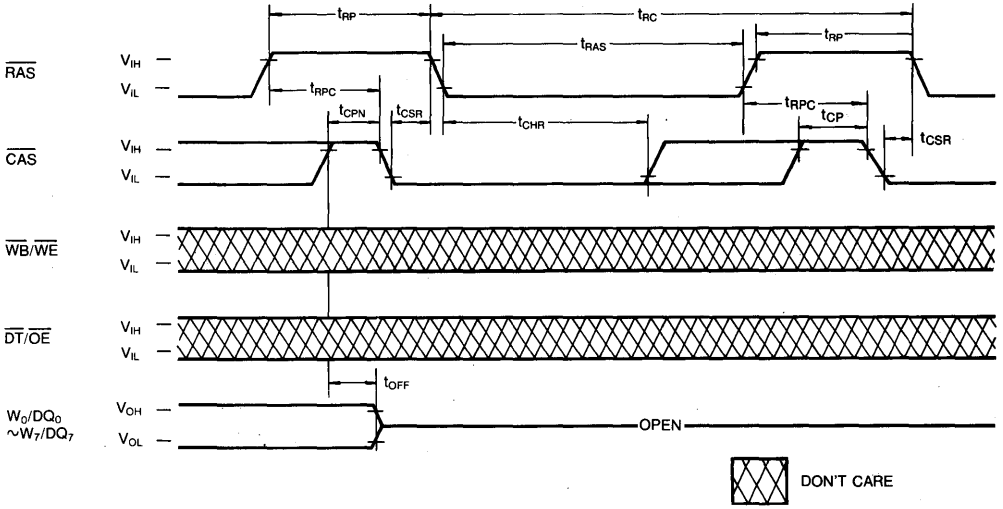


TIMING DIAGRAMS (Continued)

$\overline{RAS}$ ONLY REFRESH CYCLE

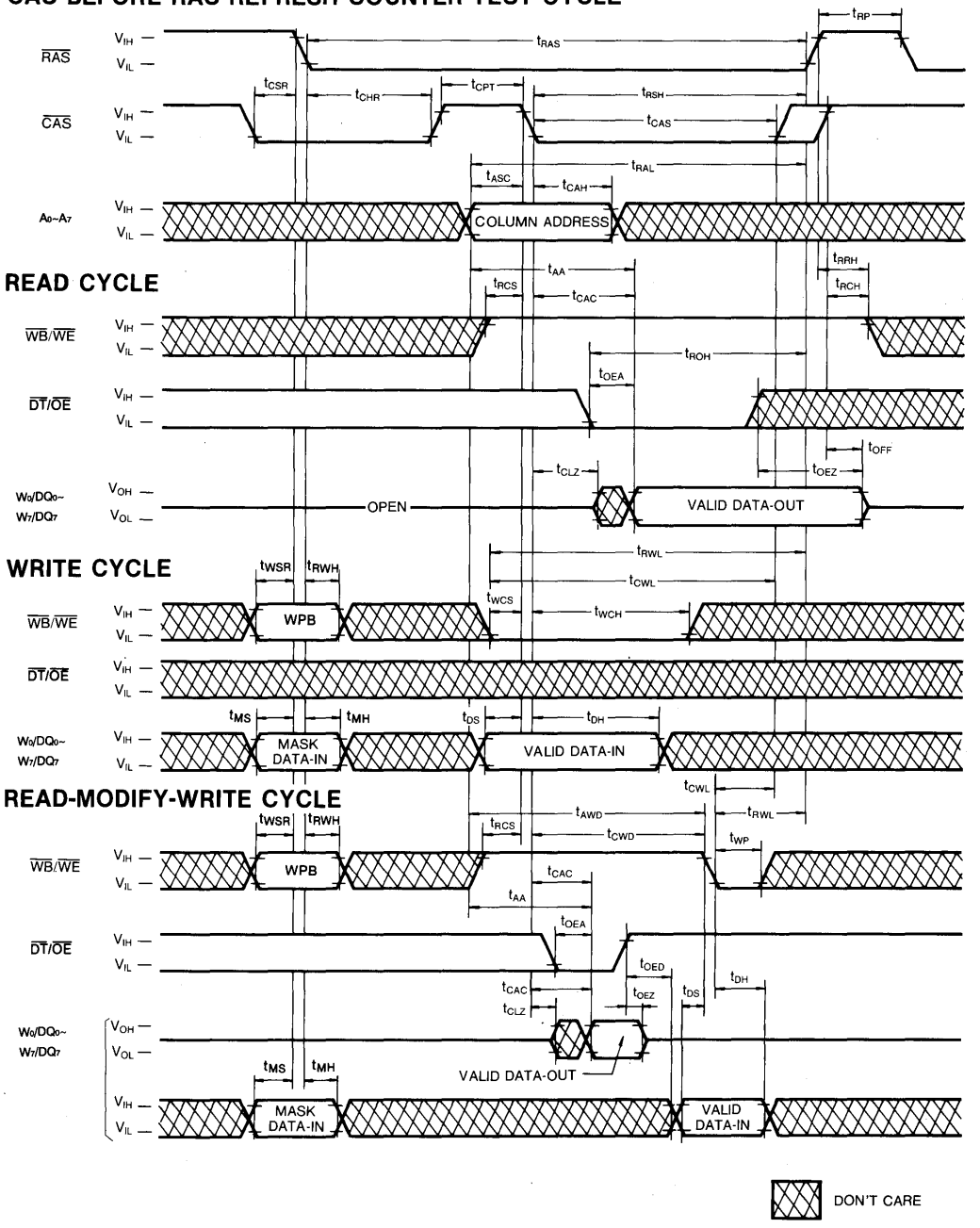


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH



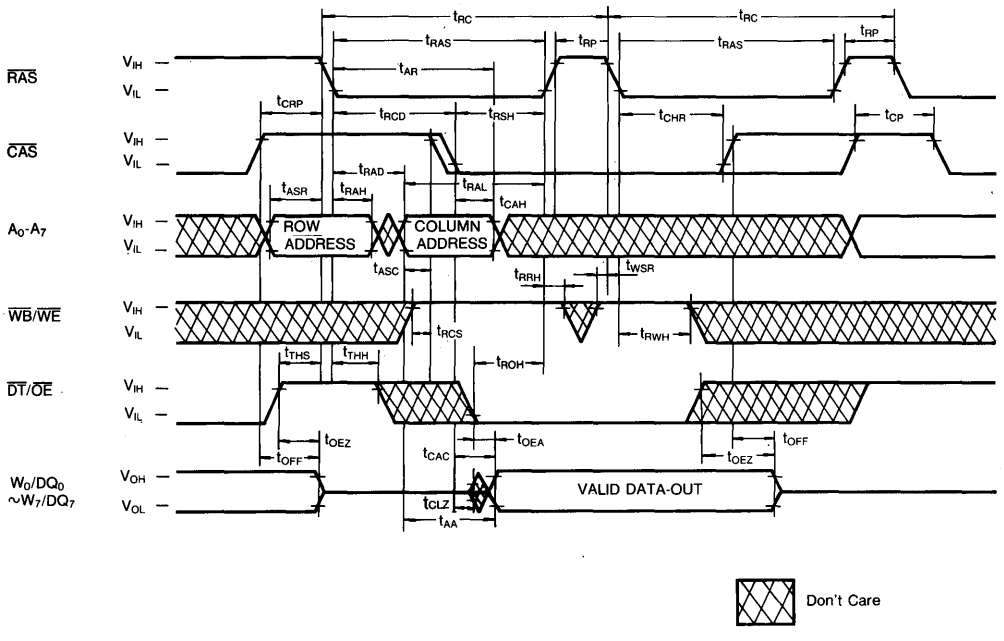
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



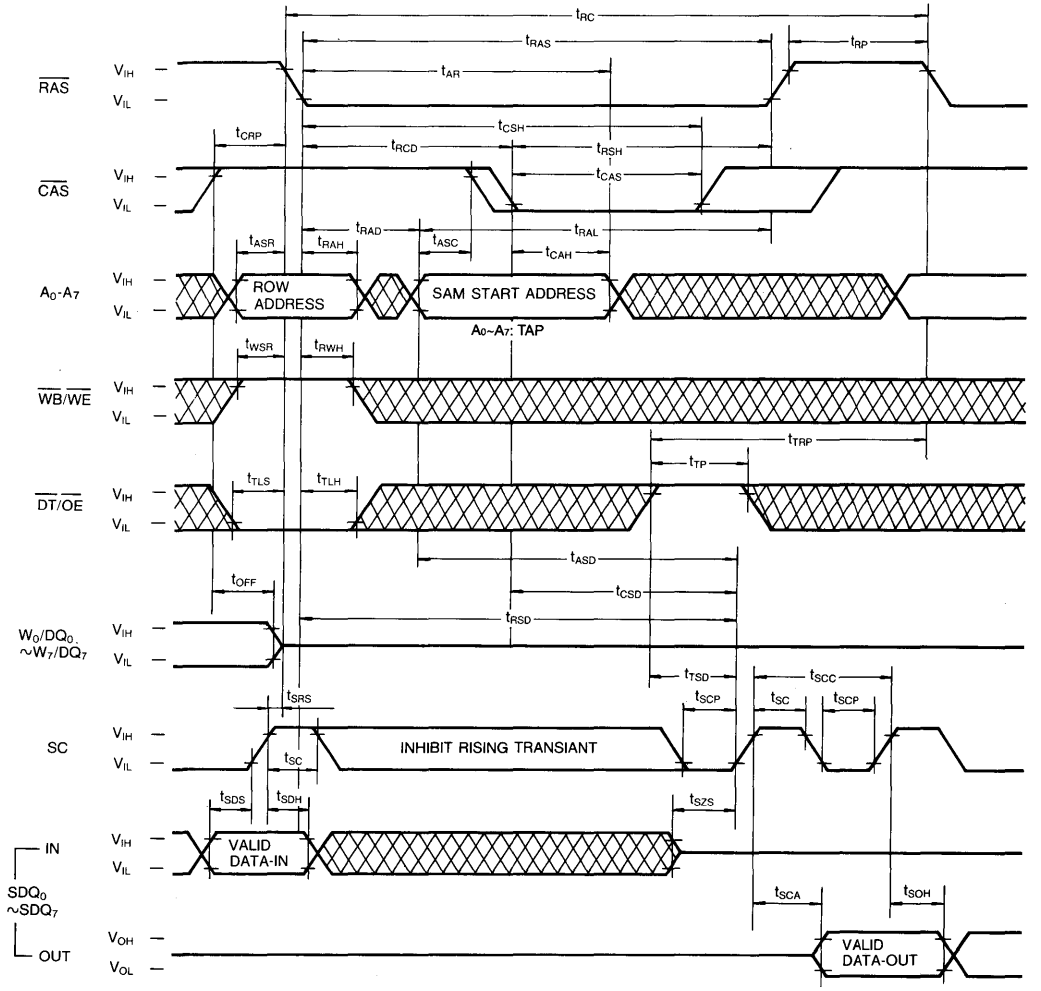
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



TIMING DIAGRAMS (Continued)

READ TRANSFER CYCLE

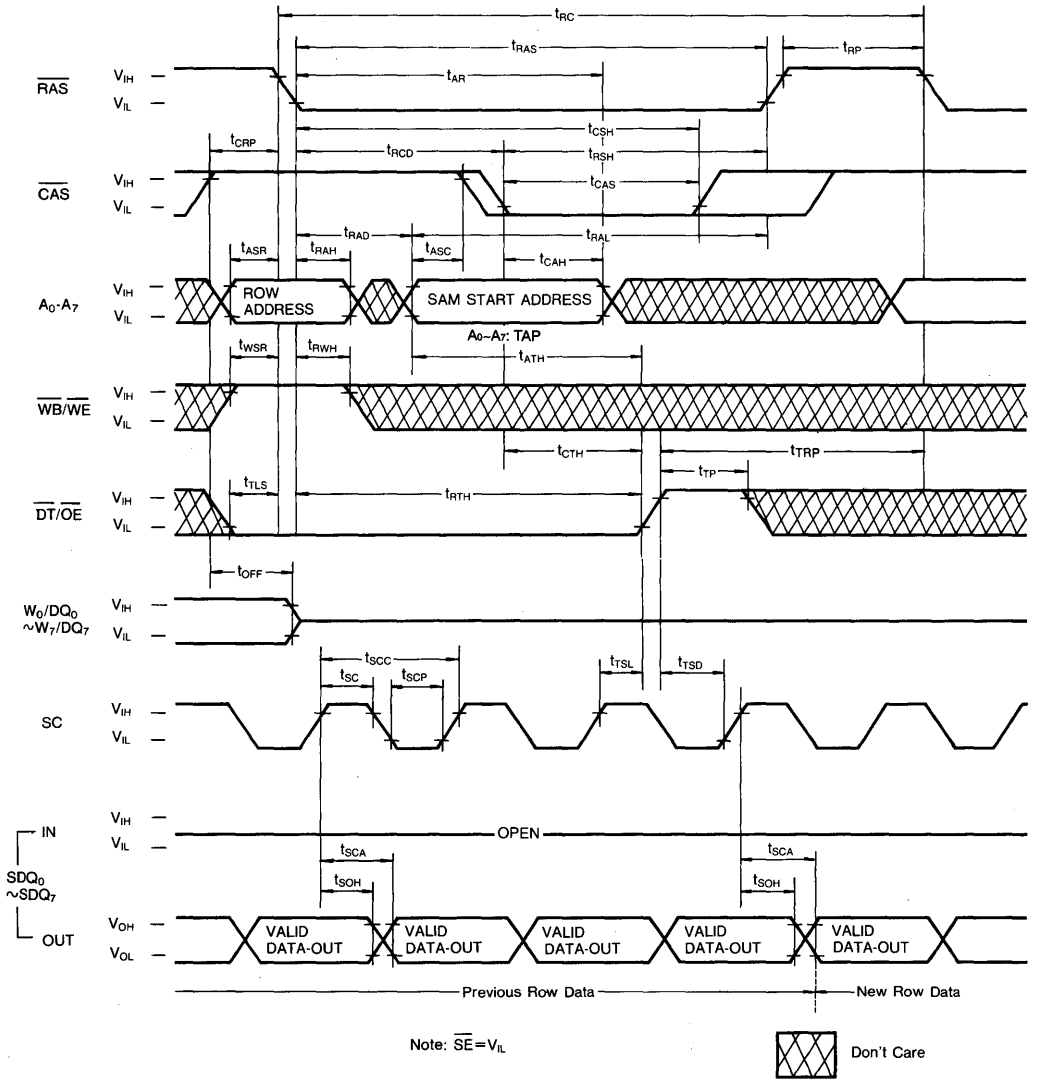


Note: $\overline{SE}=V_{IL}$

Don't Care

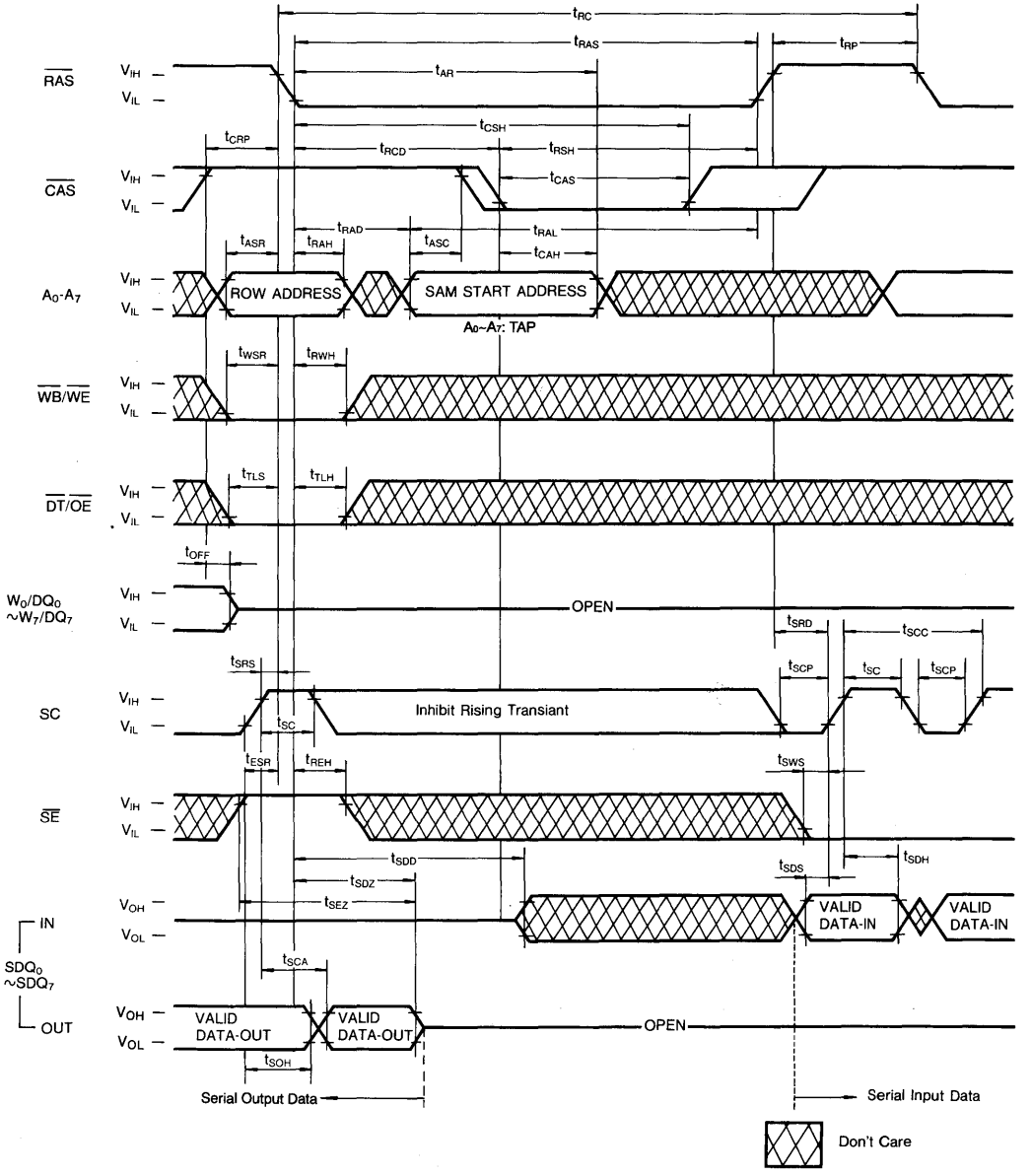
TIMING DIAGRAMS (Continued)

REAL TIME READ TRANSFER CYCLE



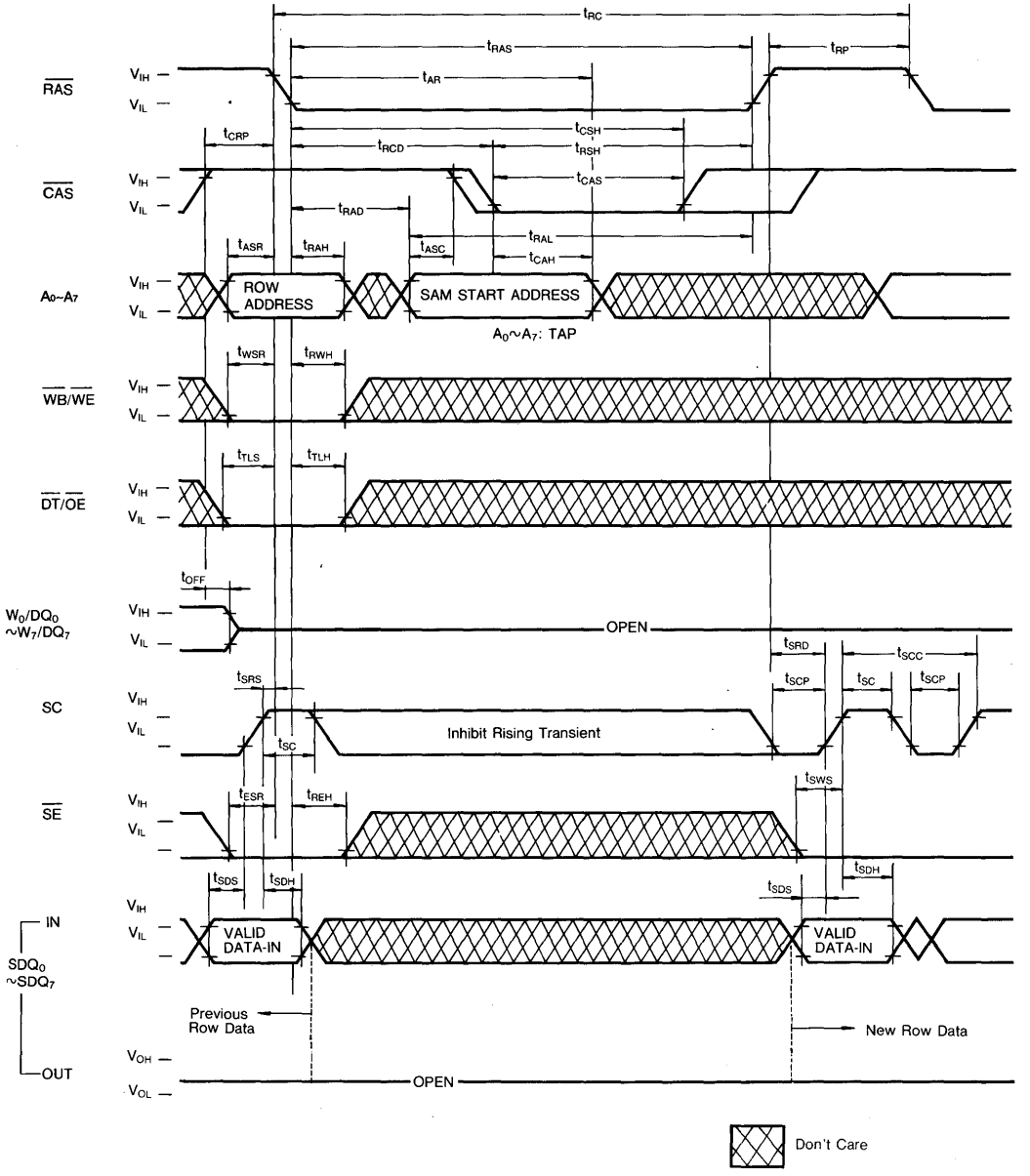
TIMING DIAGRAMS (Continued)

PSEUDO WRITE TRANSFER CYCLE



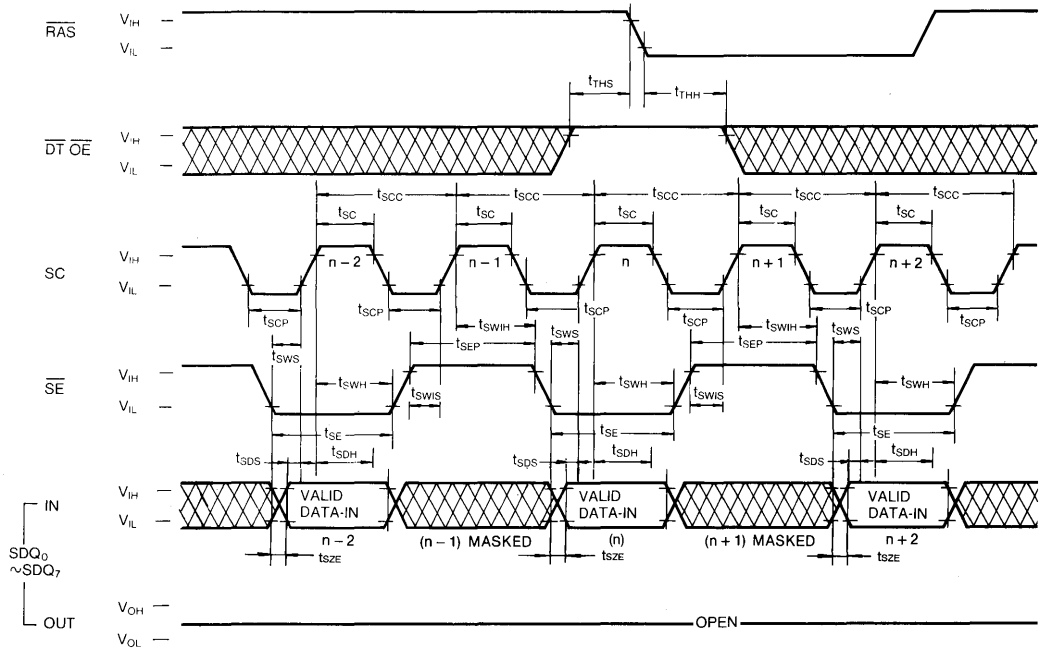
TIMING DIAGRAMS (Continued)

WRITE TRANSFER CYCLE

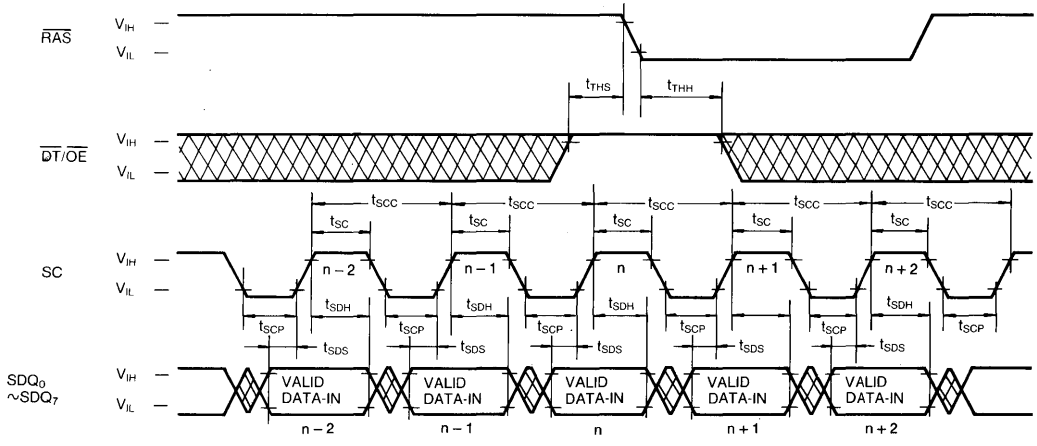


TIMING DIAGRAMS (Continued)

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



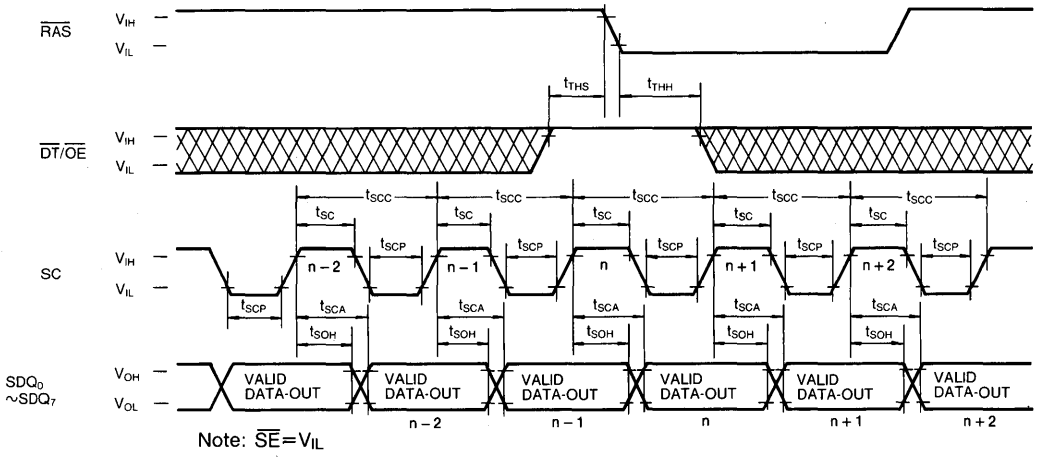
SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



Note: $\overline{SE} = V_{IL}$

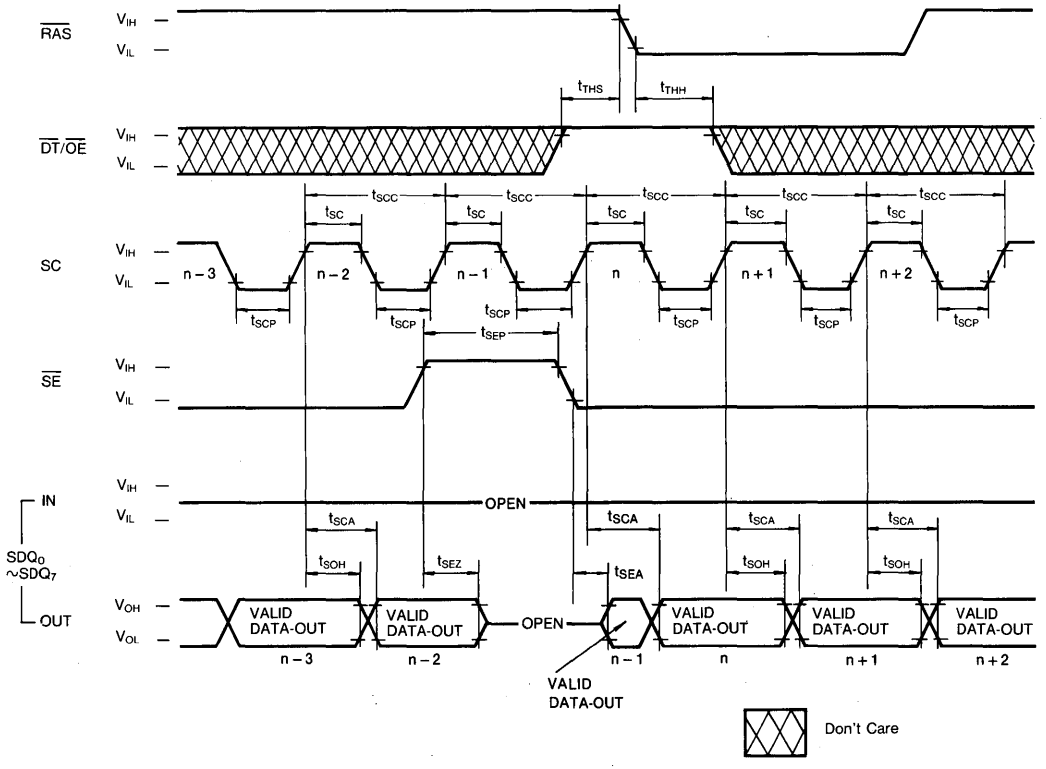
Don't Care

SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$=V_{IL}

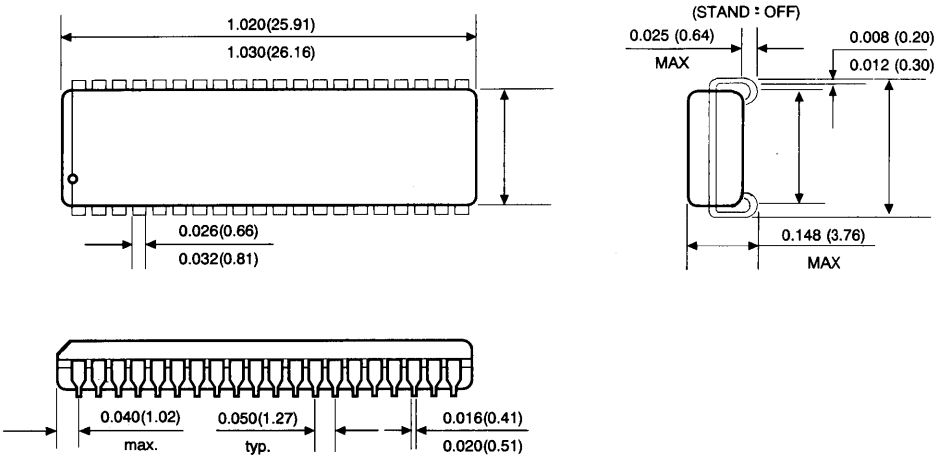
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



PACKAGES DIMENSION

40 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE

Unit : Inches (millimeters)



256KX4 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K x 4 bits RAM port
  512 x 4 bits SAM port
- **Performance**

Parameter \ Speed	-6	-7	-8
RAM access time (t_{RAC})	60ns	70ns	80ns
RAM access time (t_{CAC})	20ns	20ns	20ns
RAM cycle time (t_{RC})	110ns	130ns	150ns
RAM page mode cycle (t_{PC})	40ns	45ns	50ns
SAM access time (t_{SCA})	18ns	20ns	20ns
SAM cycle time (t_{SCC})	20ns	25ns	25ns
RAM active current	90mA	85mA	80mA
SAM active current	50mA	45mA	40mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read, Real Time Read and Split Read Transfer (RAM→SAM)**
- **Write, Split Write Transfer with Masking operation (New Mask)**
- **Block Write, Flash Write and Write per bit with Masking operation (New Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output Control**
- **All Inputs and outputs TTL compatible**
- **Refresh: 512 Cycle/8ms**
  Single +5V±10% Supply Voltage
- **Plastic 28-PIN 400 mil SOJ and ZIP**

GENERAL DESCRIPTION

The Samsung KM424C257 is a CMOS 256K×4 bit Dual Port DRAM. It consists of a 256K×4 dynamic random access memory (RAM) port and 512×4 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 2048 bits. It operates like a conventional 256K×4 CMOS DRAM. The RAM port has a write per bit mask capability.

The SAM port consists of four 512 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

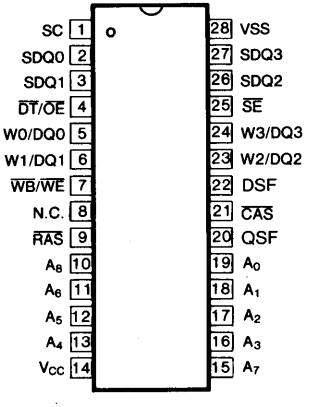
Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM424C257 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

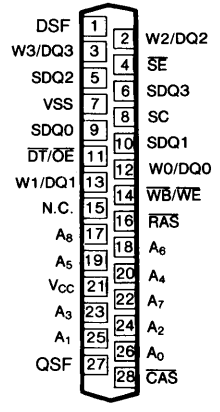
All inputs and I/O's are TTL level compatible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (Top Views)

28 Pin 400 mil SOJ



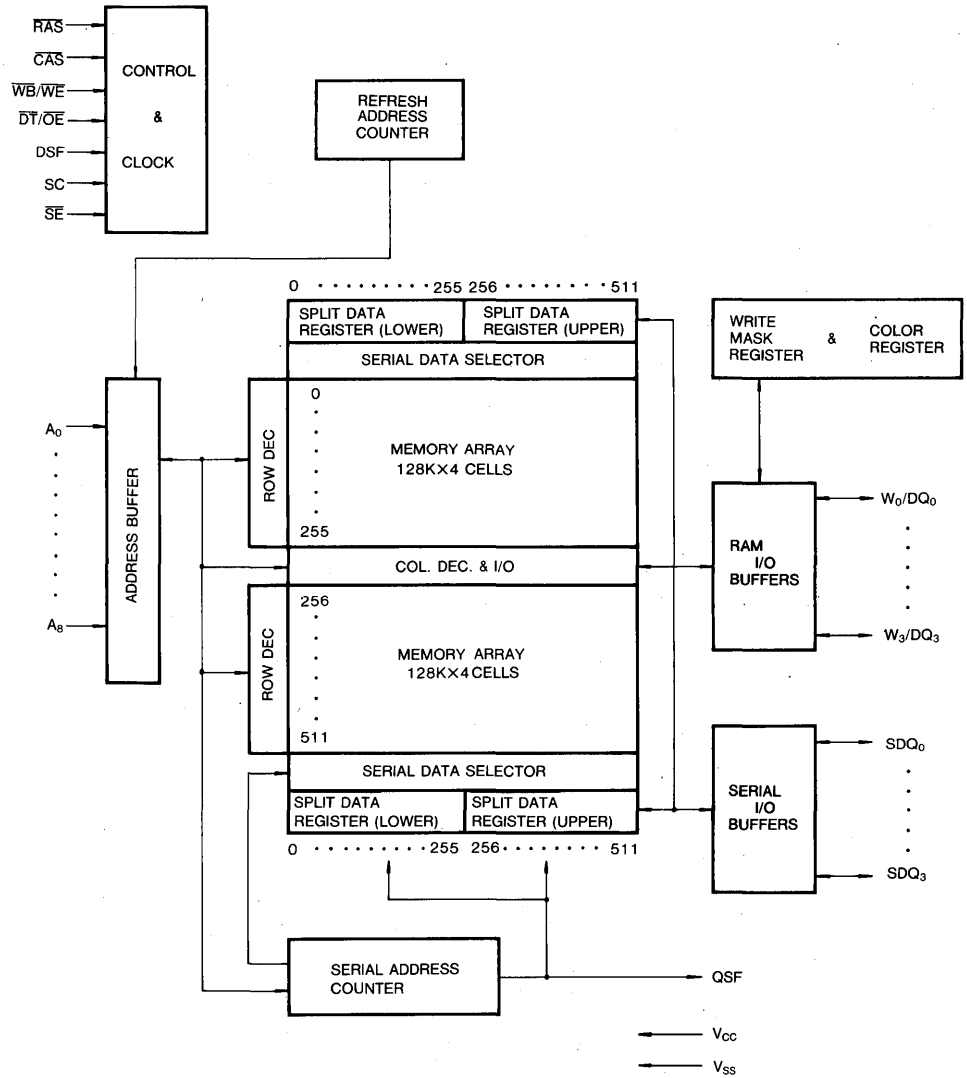
28 Pin 400 mil ZIP



PIN DESCRIPTION

Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ input is a multifunction pin. when $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions(BW, FW, Split Transfer, etc)are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0-255, High if address is 256-511.
SE	IN	In a serial read cycle. $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
V_{CC}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS					CAS	Address*1		DQi Input*2		Write Mask	Color Register	Function
	CAS	DT/OE	WE	DSF	SE	DSF	RAS	CAS	RAS	CAS/WE			
CBR	0	X	X	X	X	–	X	X	X	–	–	–	CBR Refresh
ROR	1	1	X	0	X	–	Row	X	X	–	–	–	RAS-only Refresh
RW	1	1	1	0	X	0	Row	Col.	X	Data	–	–	Normal DRAM Read/ Write(No. Mask)
RW/NM	1	1	0	0	X	0	Row	Col.	WMi	Data	Use	–	Masked DRAM Write (New Mask)
MFLW	1	1	0	1	X	X	Row	X	WMi	X	Use	Use	Masked Flash Write (New Mask)
BW	1	1	1	0	X	1	Row	Col. (A2~A8)	X	Col. Mask	–	Use	Block Write (No Mask)
BW/NW	1	1	0	0	X	1	Row	Col. (A2~A8)	WMi	Col. Mask	Use	Use	Masked Block Write (New Mask)
LCR	1	1	1	1	X	1	Row*3	•X	X	Coor Mask	–	Load	Load Color Register
RT	1	0	1	0	X	X	Row	Tap	X	X	–	–	Read Transfer
SRT	1	0	1	1	X	X	Row	Tap	X	X	–	–	Split Read Transfer
PWT	1	0	0	0	1	X	Row	Tap	X	X	–	–	Pseudo Write Transfer
MWT	1	0	0	0	0	X	Row*3	Tap	WMi	X	–	–	Masked Write Transfer(New Mask)
MSWT	1	0	0	1	X	X	Row	Tap	WMi	X	–	–	Masked Split Write Transfer(New Mask)

X: Don't Care, -: Not Applicable

Note

*1 : These column show what must be present on the A_0~A_8 outputs at the falling edge of RAS and CAS.

*2 : These column show what must be present on the DQ_0~DQ_3 outputs at the falling edge of RAS, CAS or WB/WE, whichever is later.

*3 : The Row that is addressed will be refreshed.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1V	V
Input Low Voltage	V_{IL}	−1.5	—	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \le V_{IN} \le V_{CC}$ +0.5V, all other pins not under test=0 volts)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OL}	−10	10	μA
Output High Voltage Level (RAM I_{OH}=−5mA, SAM I_{OH}=−2mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (RAM I_{OL}=4.2mA, SAM I_{OL}=2mA)	V_{OL}	—	0.4	V

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0-W_3/DQ_3)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0-SDQ_3)	C_{SDQ}	2	7	pF
Output Capacitance (QSF)	C_{QSF}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM424C257			Unit
			-6	-7	-8	
Operating Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC1}	90	85	80	mA
	Active	I_{CC1A}	140	130	120	mA
Standby Current*1 ($\overline{RAS}$=$\overline{CAS}$=$\overline{DT}$/$\overline{OE}$=$\overline{WB}$/$\overline{WE}$=V_{IH},DSF=V_{IL})	Standby	I_{CC2}	5	5	5	mA
	Active	I_{CC2A}	50	45	40	mA
$\overline{RAS}$ Only Refresh Current*1 ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC3}	90	85	80	mA
	Active	I_{CC3A}	140	130	120	mA
Fast Page Mode Current*1 ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @t_{PC}=min.)	Standby	I_{CC4}	70	65	60	mA
	Active	I_{CC4A}	120	110	100	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC5}	90	85	80	mA
	Active	I_{CC5A}	140	130	120	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC6}	120	115	110	mA
	Active	I_{CC6A}	170	160	150	mA
Flash Write Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC7}	90	85	80	mA
	Active	I_{CC7A}	140	130	120	mA
Block Write Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC8}	100	95	90	mA
	Active	I_{CC8A}	150	140	130	mA
Color Register Load or Read Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	Standby	I_{CC9}	90	85	80	mA
	Active	I_{CC9A}	140	130	120	mA

NOTE*1: Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open, Icc is Specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, I_{CC9} address transition should be changed only while $\overline{RAS}$=V_{IL}

In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, see notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		20		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		20	ns	4
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width(fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	20	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR Counter Test)	t_{CPT}	10		10		10		ns	
$\overline{CAS}$ precharge time(fast page mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$, See notes 1,2)

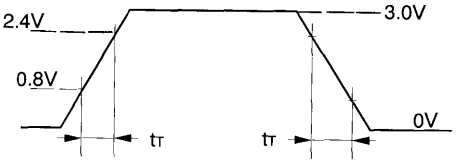
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay(Fast Page mode)	t_{CPWD}	60		65		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
Access time from output enable	t_{OEA}		20		20		20	ns	7
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period(512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$ (I)	t_{FHR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$ (I)	t_{FSR}	45		55		60		ns	
DSF hold time referenced to $\overline{RAS}$ (II)	t_{RFH}	10		10		15		ns	
DSF set-p time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up	t_{MS}	0		0		0		ns	
Write per bit mask data hold	t_{MH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{SE}$ setup referenced to $\overline{RAS}$	t_{ESR}	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	10		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ precharge time	t_{TRP}	40		50		60		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		25		ns	
$\overline{RAS}$ to first SC delay(read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	t_{CSD}	25		30		35		ns	
Col.Addr.to first SC delay(read transfer)	t_{ASD}	35		40		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	t_{TSD}	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	t_{SRS}	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	t_{SRD}	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	t_{SDD}	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	t_{SDZ}	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	20		25		25		ns	12
SC pulse width(SC high time)	t_{SC}	6		7		7		ns	
SC precharge(SC low time)	t_{SCP}	6		7		7		ns	
Access time from SC	t_{SCA}		18		20		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	10		15		15		ns	
Access time from $\overline{SE}$	t_{SEA}		15		20		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	5		5		5		ns	
Serial write enable hold time	t_{SWH}	10		15		15		ns	
Serial write disable set-up time	t_{SWIS}	5		5		5		ns	
Serial write disable hold time	t_{SWIH}	15		15		15		ns	
Split transfer set-up time	t_{STS}	25		25		25		ns	
Split transfer hold time	t_{STH}	25		25		25		ns	
SC-QSF delay time	t_{SQD}		25		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		25		25		25	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		30		35		40	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		60		70		80	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
   Inputs signal transition from 0 to 3V for AC Testing.
3. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.
   Dout comparator level:V_{OH}/V_{OL}=2.0/0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL loads and 50pF. Dout comparator level: V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
7. The parameters, $t_{OFF(max)}$, $t_{OEZ(max)}$, $t_{SDZ(max)}$ and $t_{SEZ(max)}$, define the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RCD(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Assume t_T=3ns
13. Recomended operating input condition.



Input pulse levels are from 0.0V to 3.0Volts.

All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 3.0ns

14. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max)

DEVICE OPERATION

The KM424C257 contains 1,048,576 memory locations. Eighteen addres bits are required to address a particular 4-bit word in the memory array. Since the KM424C257 has only 0 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM424C257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM424C257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM424C257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}.

The KM424C257 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Write

The KM424C257 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$, whichever is later.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Write-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in Table 1.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
⌐	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	INHIBIT WRITE

DEVICE OPERATION (Continued)

Block Write

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "Low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled as write per bit function. At the falling edge of $\overline{CAS}$, the starting column address pointer and column mask data must be provided. During a block write cycle, the 2 least significant column address (A_0 and A_1) are internally controlled and only the seven most significant column address (A_2~A_8) are latched at the falling edge of $\overline{CAS}$.

Flash Write

Flash write is mainly used for fast clear operations in frame buffer applications. A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "Low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the Wi/DQi lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks.

Data Output

The KM424C257 has a three state output buffers which are controlled by $\overline{CAS}$ and $\overline{DT}/\overline{OE}$. When either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM424C257 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modity-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write, Read Color Register.

Refresh

The data in the KM424C257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address, (A_0-A_8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM424C257 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM424C257 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM424C257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

1. Normal Write/Read Transfer (SAM→RAM/RAM→SAM.).
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM.).
3. Real Time Read Transfer (On the fly Read Transfer operation).
4. Split Write/Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred from/to the SAM while the other half is write to/read from the SDQ pins.).

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address

DEVICE OPERATION (Continued)

selected at the falling edge of $\overline{RAS}$ determines the RAM row to be trasferred into the SAM.

The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the otuput mode. In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Table 2. Truth table for Transfer operation

$\overline{RAS}$ Falling-Edge					Function	Transfer Direction	Transfer Data Bits	Sam port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM→SAM	512X4	Input→Output
H	L	L	L	L	Masked Write Transfer	SAM→RAM	512X4	Output→Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output→Input

*: Don't Care

Write Transfer Cycle

A write transfer cycle consists of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transfered. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When two consecutive write transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has seen satisfied. A rising edge of the SC clock until must not occur after a specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A psuedo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

Special Function Input (DSF)

In read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split register mode read transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of most significant column address bit (A_8) that is strobed in on the falling edge of $\overline{CAS}$. If A_8 is high, the transfer is to the high half of the register. If A_8 is low, the transfer is to the low half of the register. Use of the split register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{DT}/\overline{OE}$ to the serial clock. The transfer can be to either the active half or the inactive half register. If the transfer is to the active register, with an uninterrupted serial data stream, then the timings t_{TSL} and t_{TSD} must be met.

In write tranfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of a Split Register mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

DEVICE OPERATION(Continued)

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(512bit)to be transferred to the selected row in the DRAM array. masking is selected by latching Wi/DQi9i-0~7)inputs when $\overline{RAS}$ goes low.

The Column address defines defines the start address of serial input and its MSB(A_8)defines QSF level.

If A_8 is low, the QSF will be low level to designate that the start address is in positioned in the lower half of SAM.(For A_8=high, the QSF will be high and indicates that the start address will be positioned in the upper half of SAM) After write transfer cycle is completed. SAM ports is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$)because the transfer has to occur at the first rising edge of $\overline{DT}/\overline{OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state QSF.

A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WE}/\overline{WB}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of RAS

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_7) defines the starting address of the SAM port from which data will begin shifting out. column address pin A_8 is a "Don't Care".

The QSF pin indicates which SAM half is shifting out serial data(0=Lower, 1=Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary(e.g. 255th or 511th bit).

Masked Split Write Transfer(MSWT)

This transfer function is very similar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "Don't Care". The opening cycle of either MWT or PWT is needed before MSWT can be performed.

Split Register Active status Output(QSF)

QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low(least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher(most significant)256 bits of the SAM.

Serial clock9SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

DEVICE OPERATIONS (Continued)

Serial Input/Output(SDQ0~SDQ3)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains in the input mode.

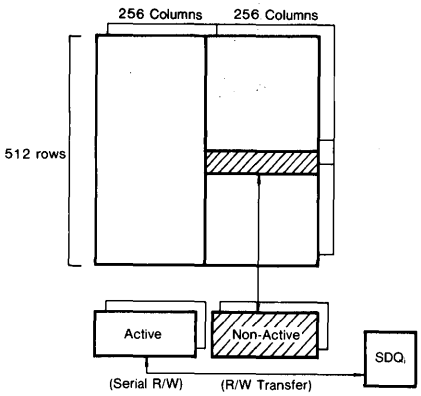
Tap Address Limitation

The Tap Address of non-split transfer cycle preceding split transfer cycle should be between 0 and 253 or between 256 and 509.

Power-up

During Power-up $\overline{RAS}$, $\overline{DT/OE}$, must be held High or track with Vcc.

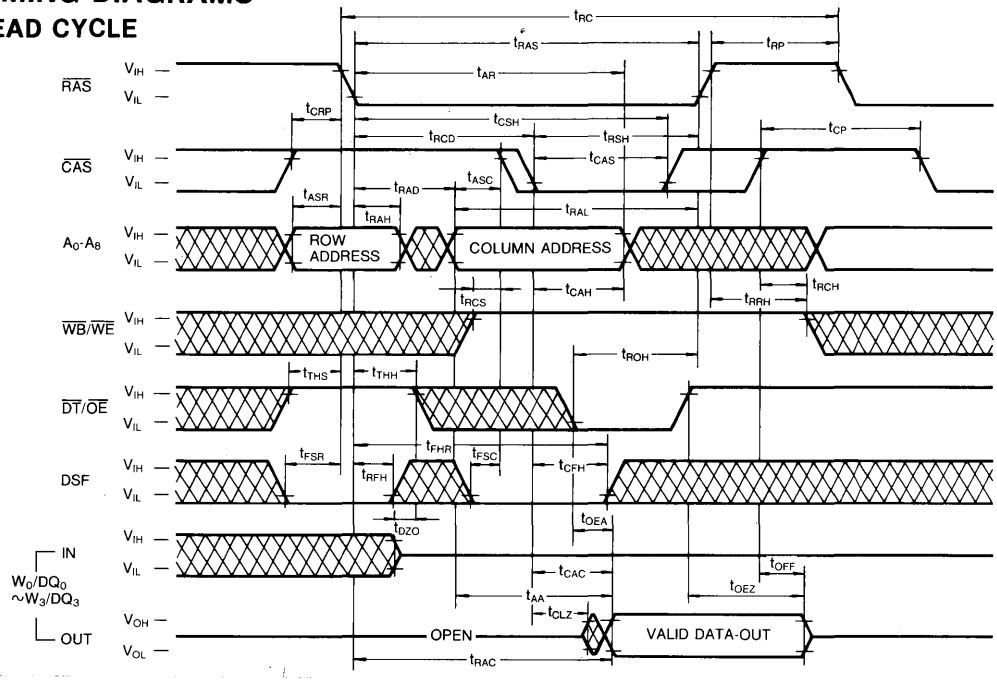
Table 3. SPLIT REGISTER MODE



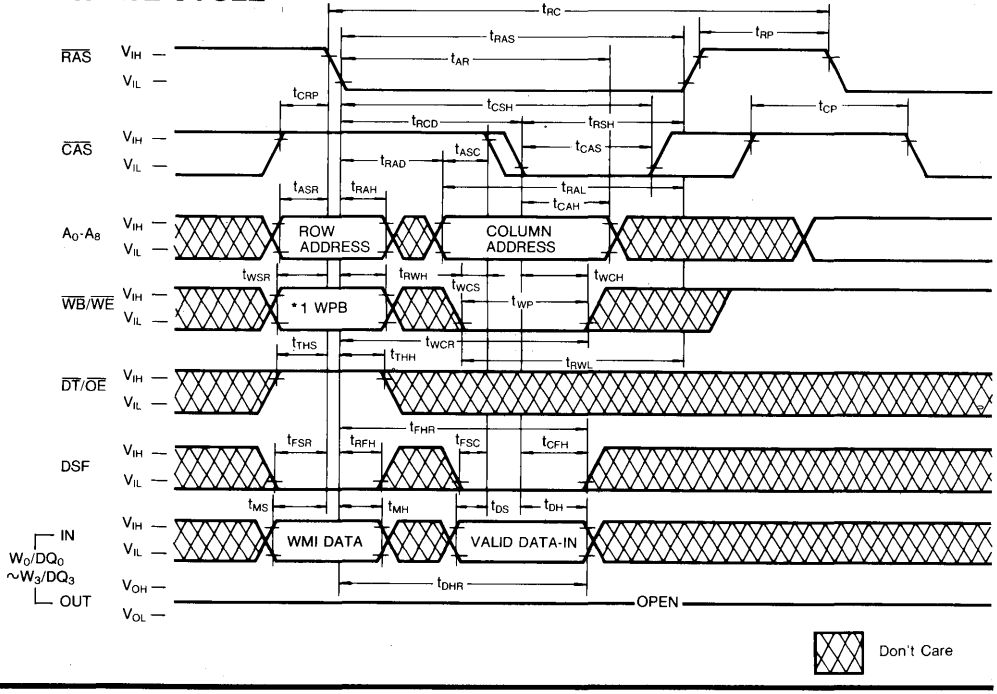
Active SAM	QSF Level
LOWER SAM	LOW
UPPER SAM	HIGH

TIMING DIAGRAMS

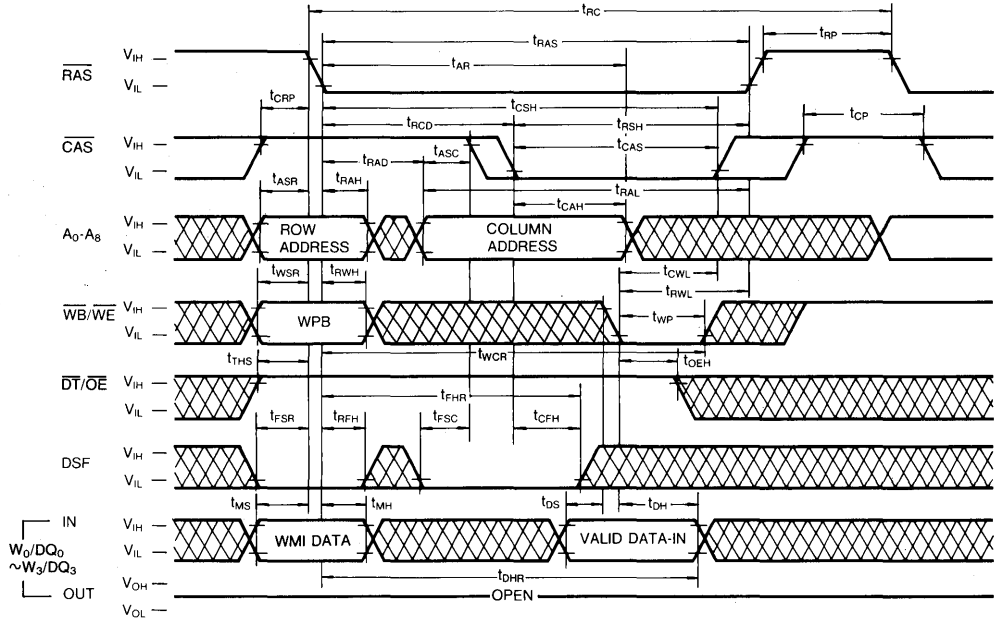
READ CYCLE



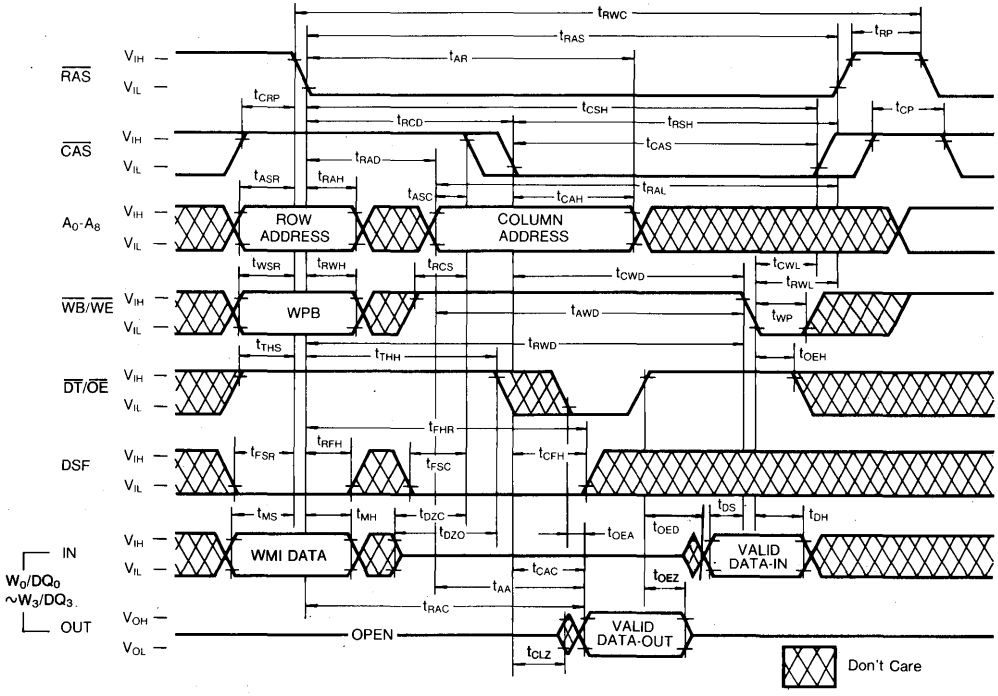
EARLY WRITE CYCLE



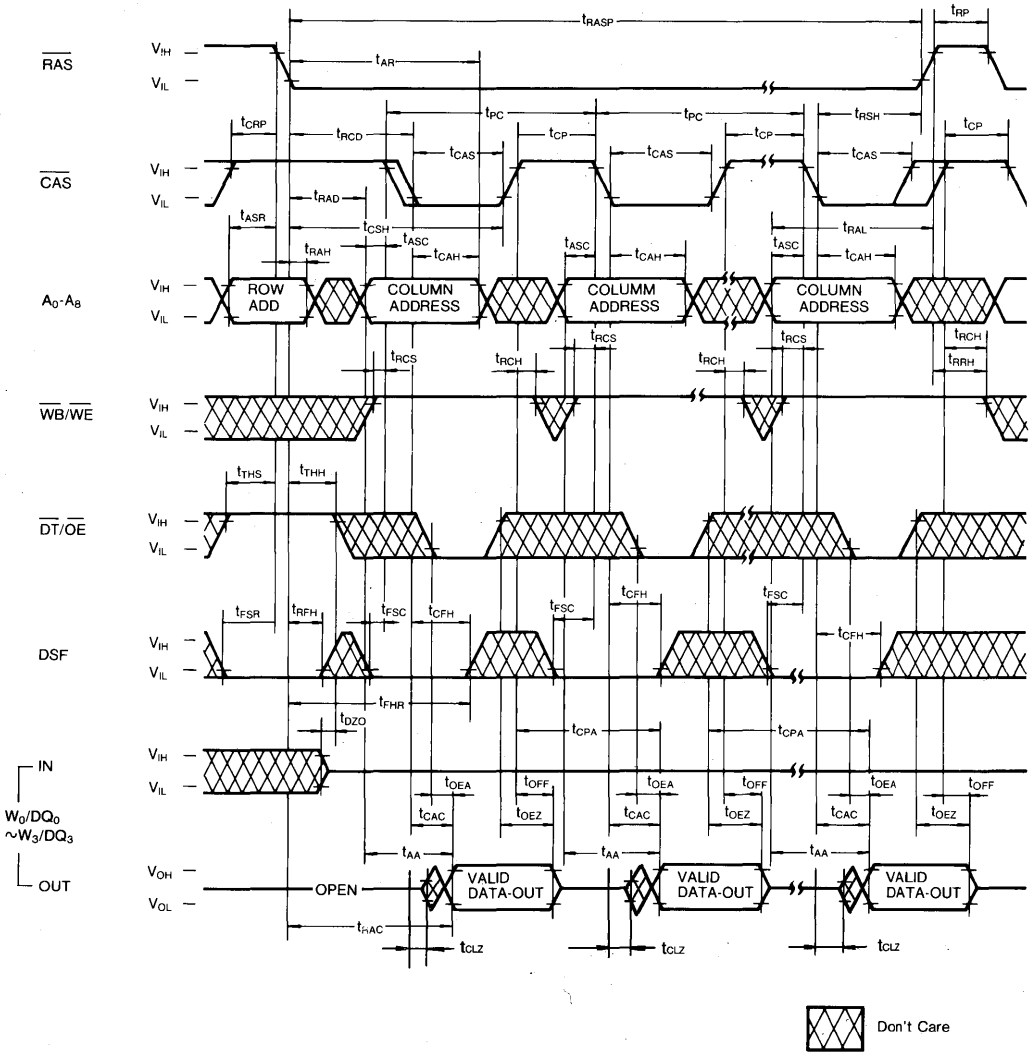
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



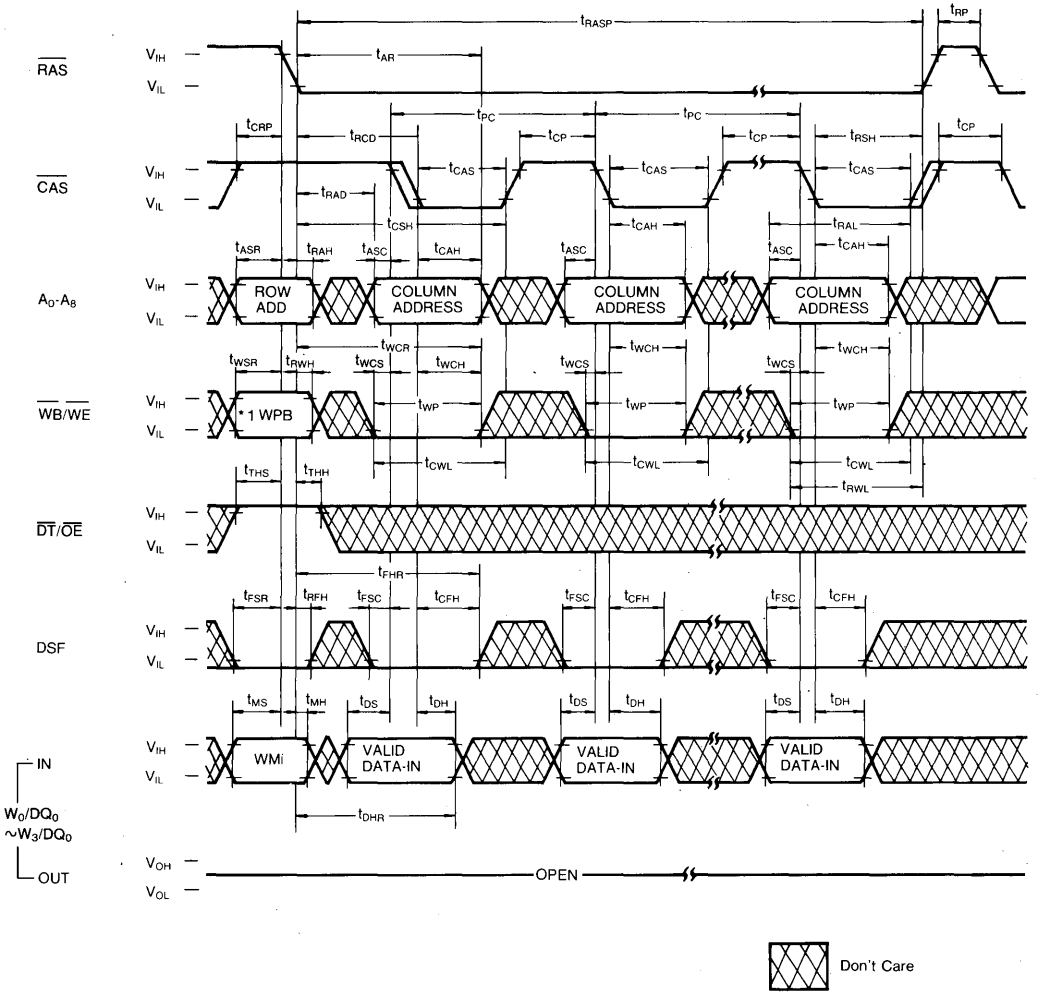
READ-WRITE/READ-MODIFY-WRITE CYCLE



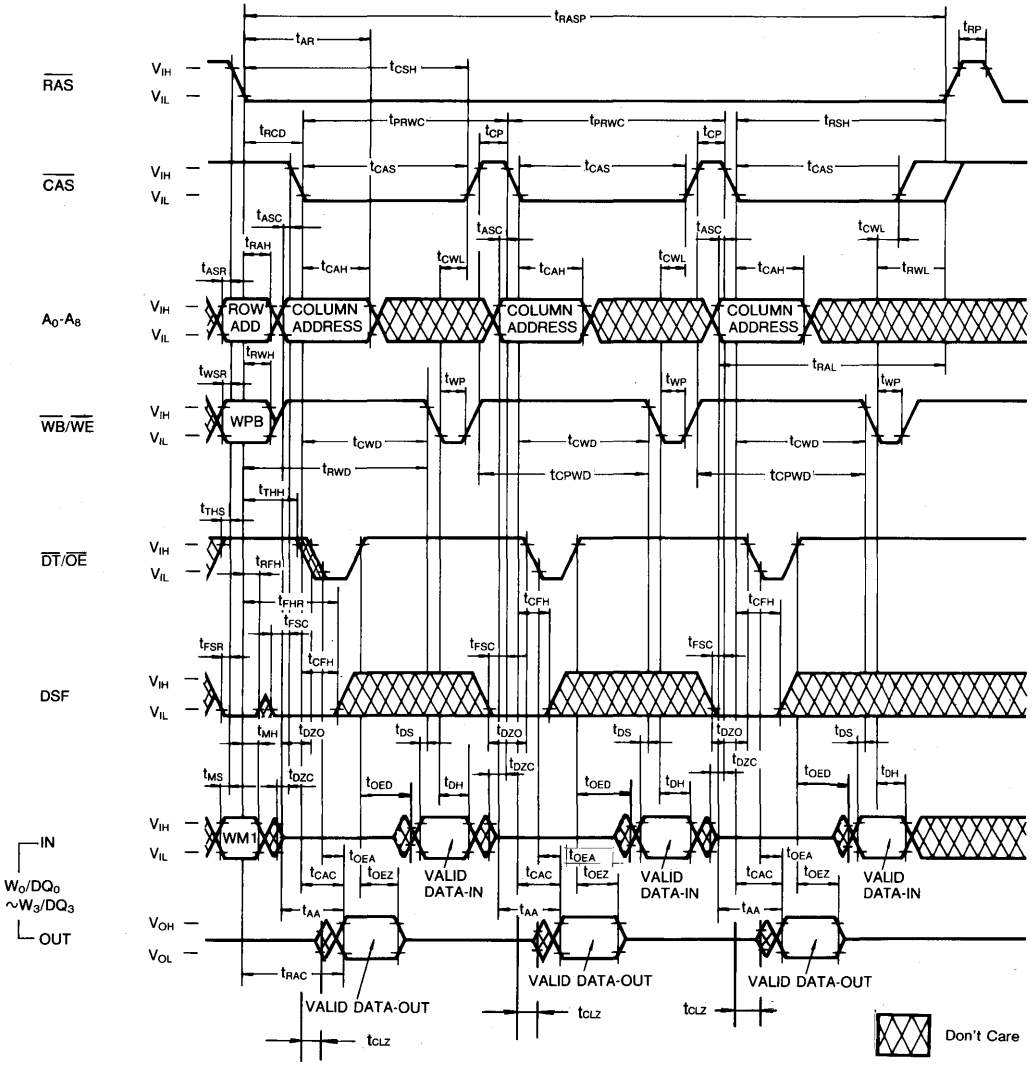
PAGE MODE READ CYCLE



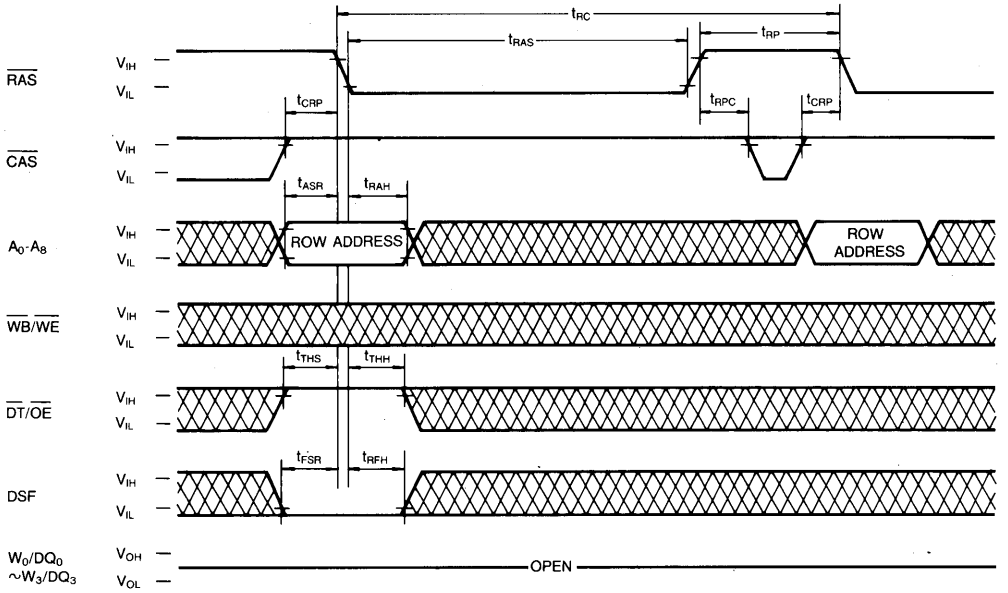
PAGE MODE WRITE CYCLE (EARLY WRITE)



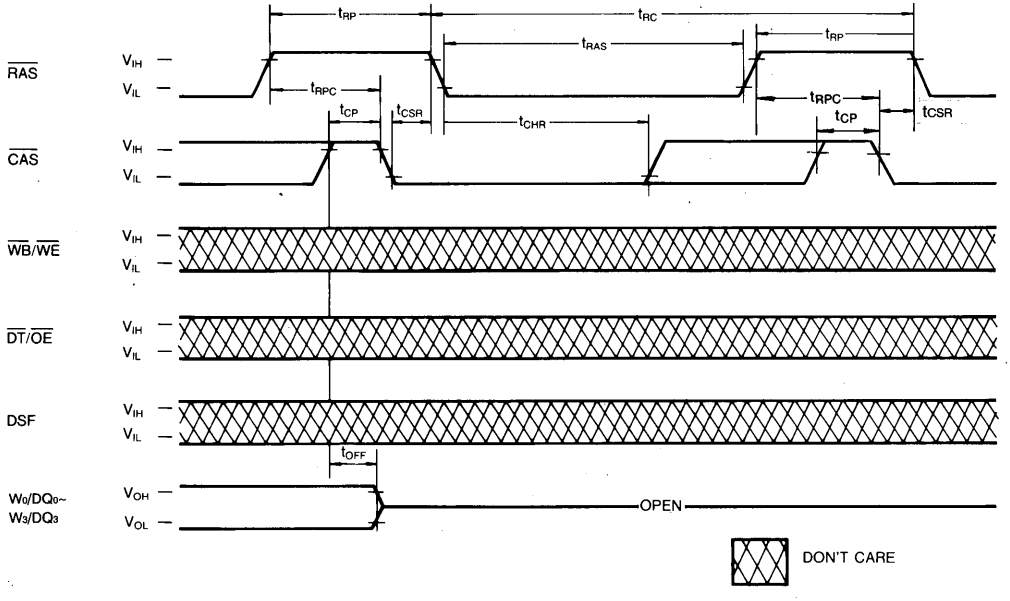
PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE

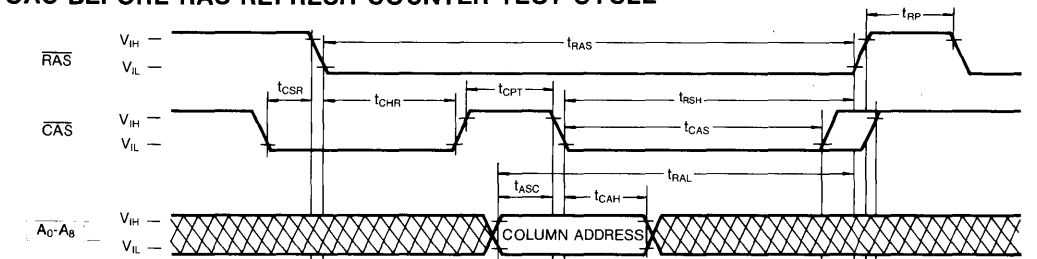


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

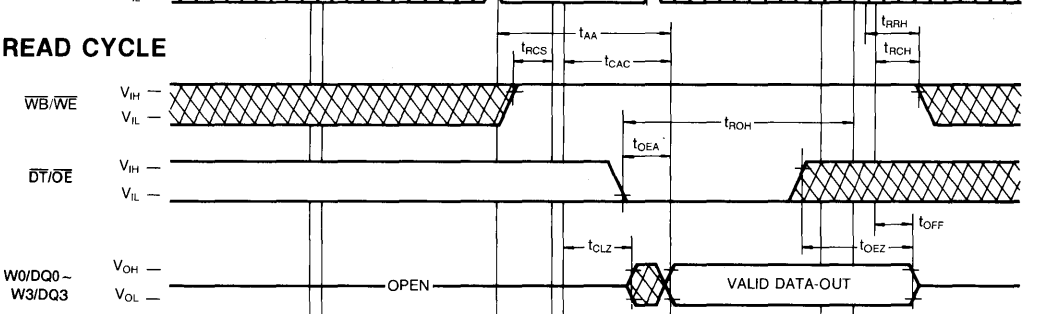


SAMSUNG ELECTRONICS

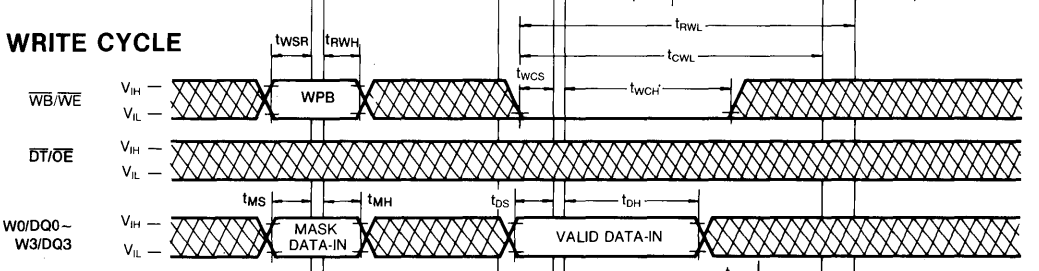
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



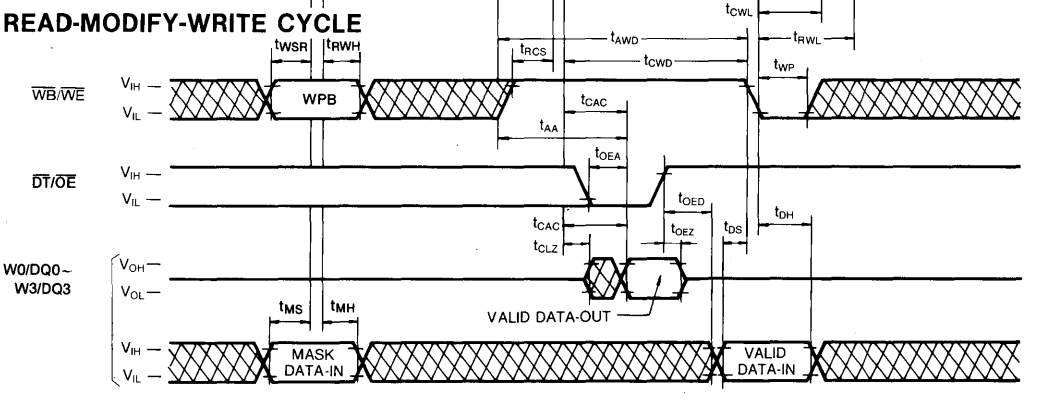
READ CYCLE



WRITE CYCLE



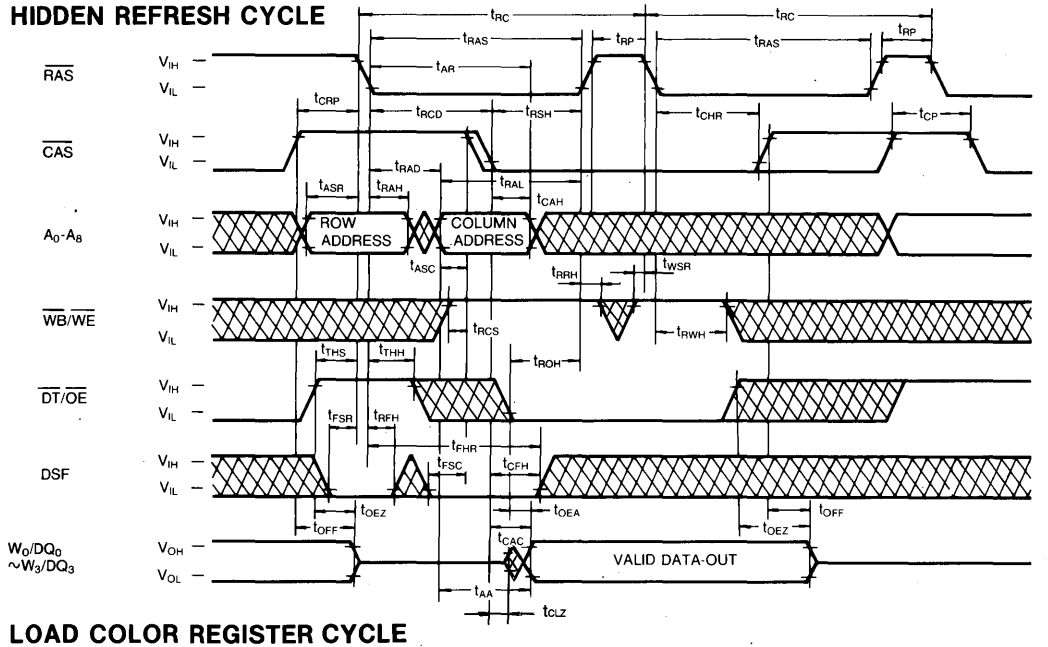
READ-MODIFY-WRITE CYCLE



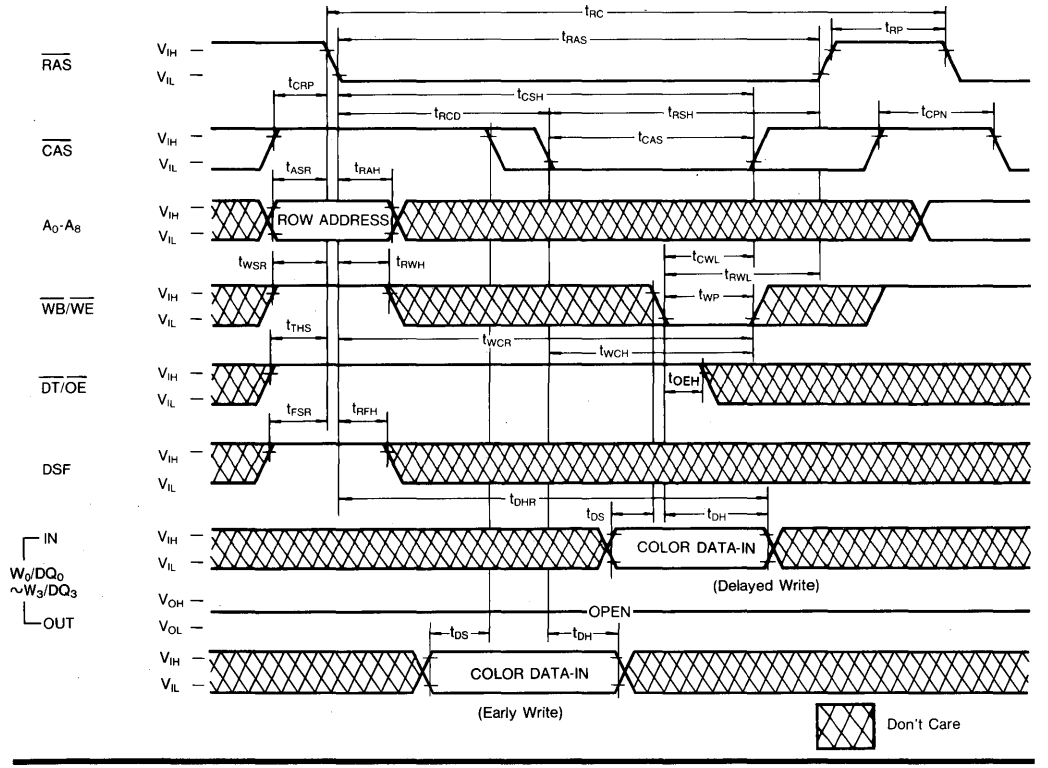
DSF = DON'T CARE

DON'T CARE

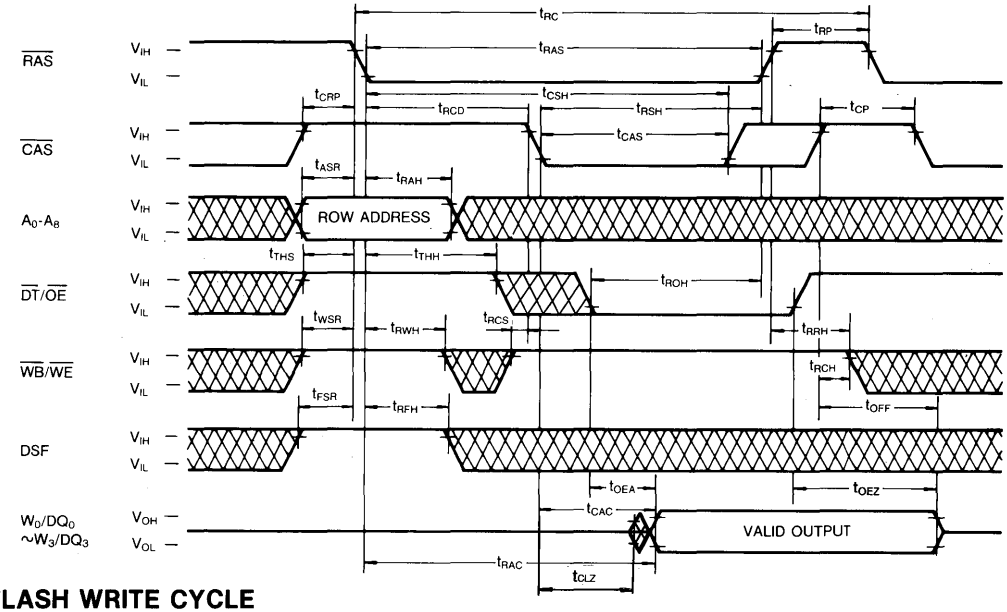
HIDDEN REFRESH CYCLE



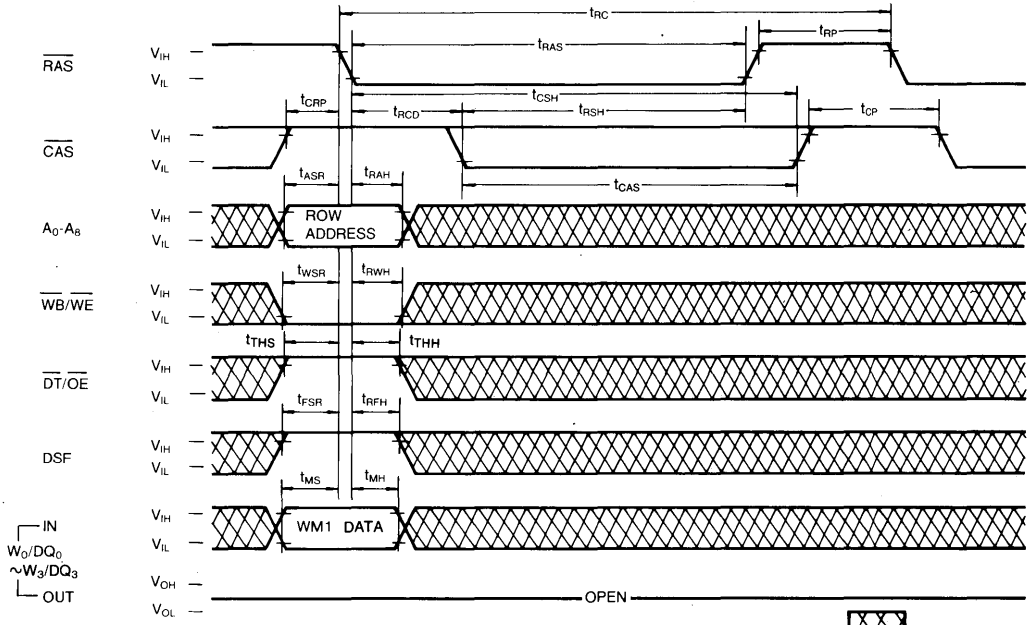
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE



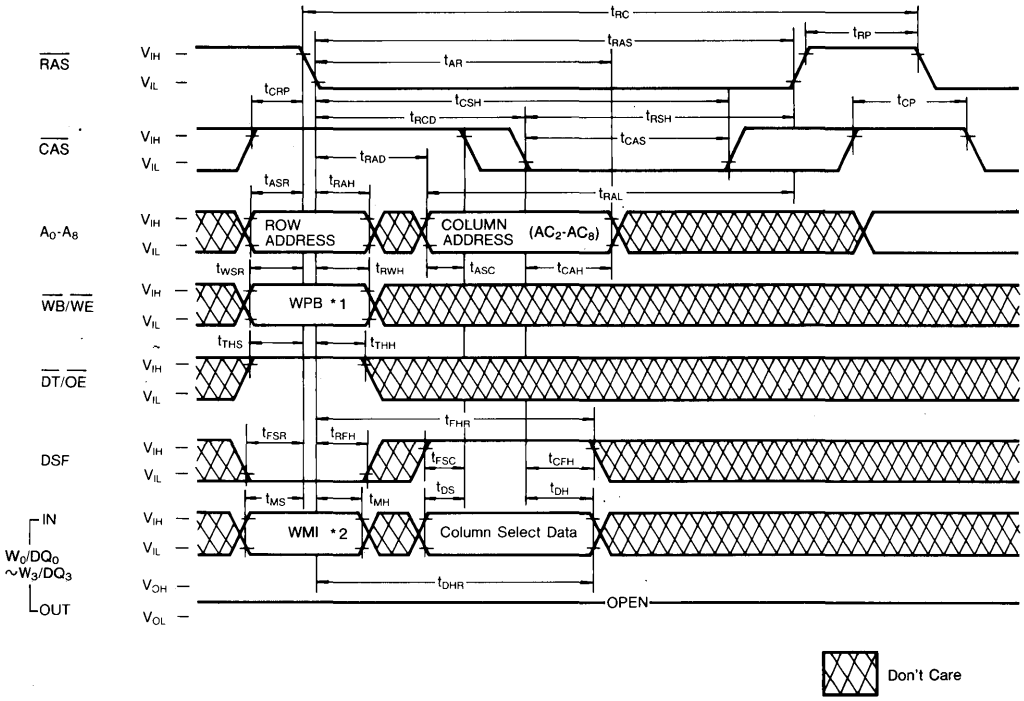
FLASH WRITE CYCLE



WM1 DATA	CYCLE
0	Flash write Disable
1	Flash write Enable

Don't Care

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_3/DQ_3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

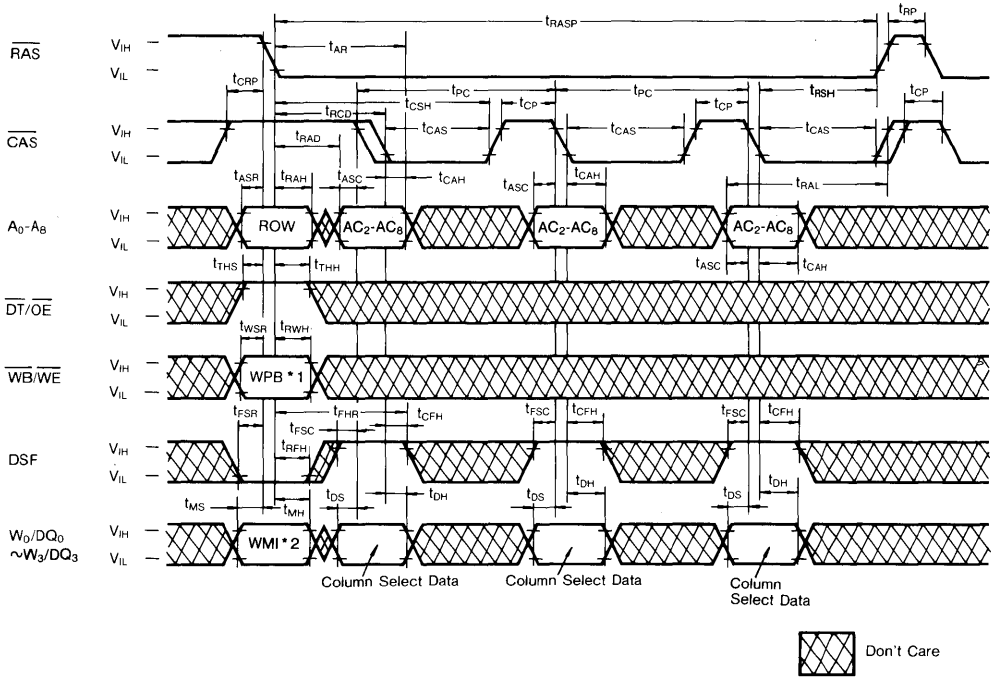
WM1 Data: 0: Write Disable
1: Write Enable

COLUMN SELECT DATA

W_0/DQ_0 — Column 0 (A_{IC}=0, A_{OC}=0)
W_1/DQ_1 — Column 1 (A_{IC}=0, A_{OC}=1)
W_2/DQ_2 — Column 2 (A_{IC}=1, A_{OC}=0)
W_3/DQ_3 — Column 3 (A_{IC}=1, A_{OC}=1)

Wn/DQn
= 0: Disable
= 1: Enable

PAGE MODE BLOCK WRITE CYCLE



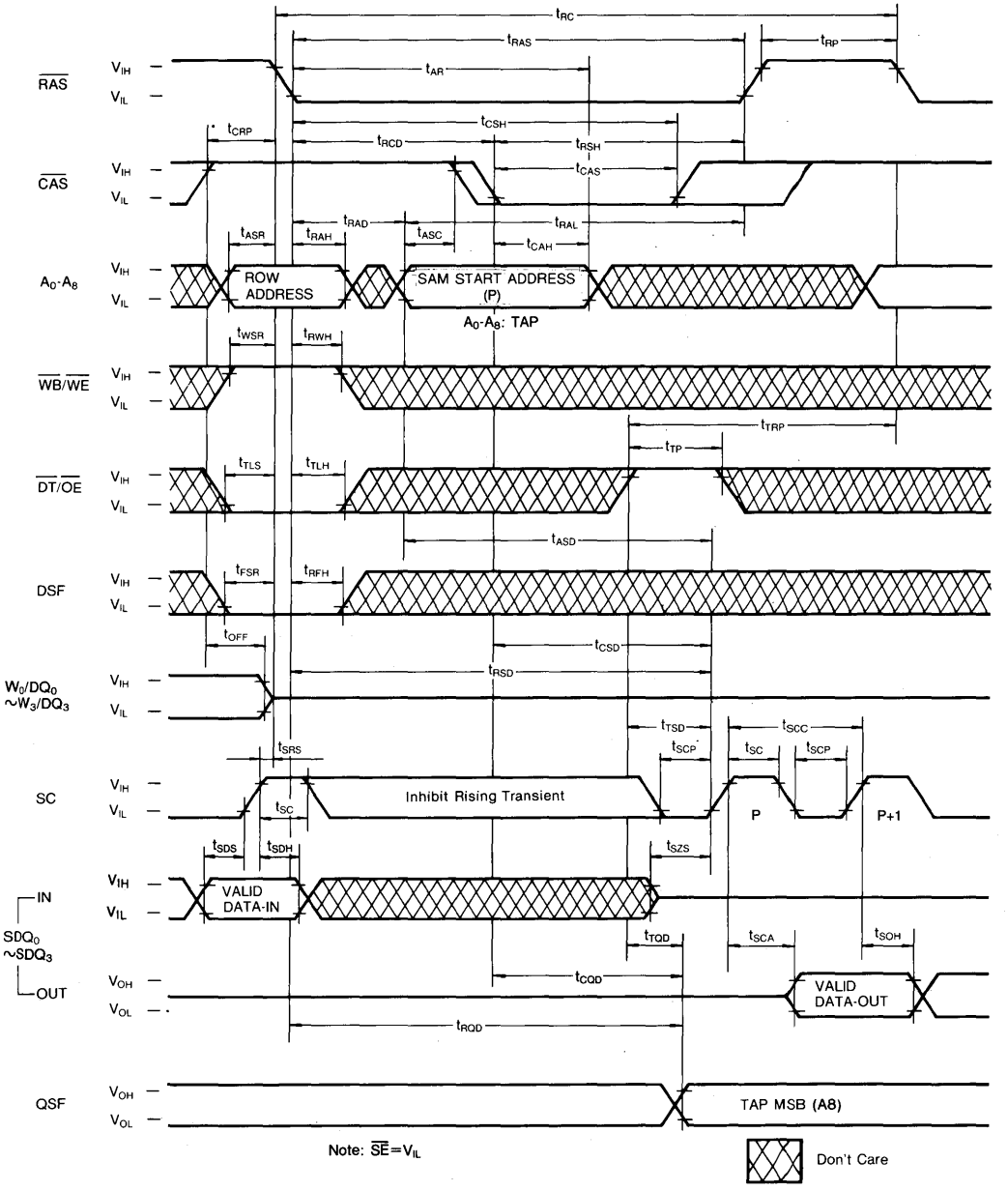
*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_3/DQ_3	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable
1: Write Enable

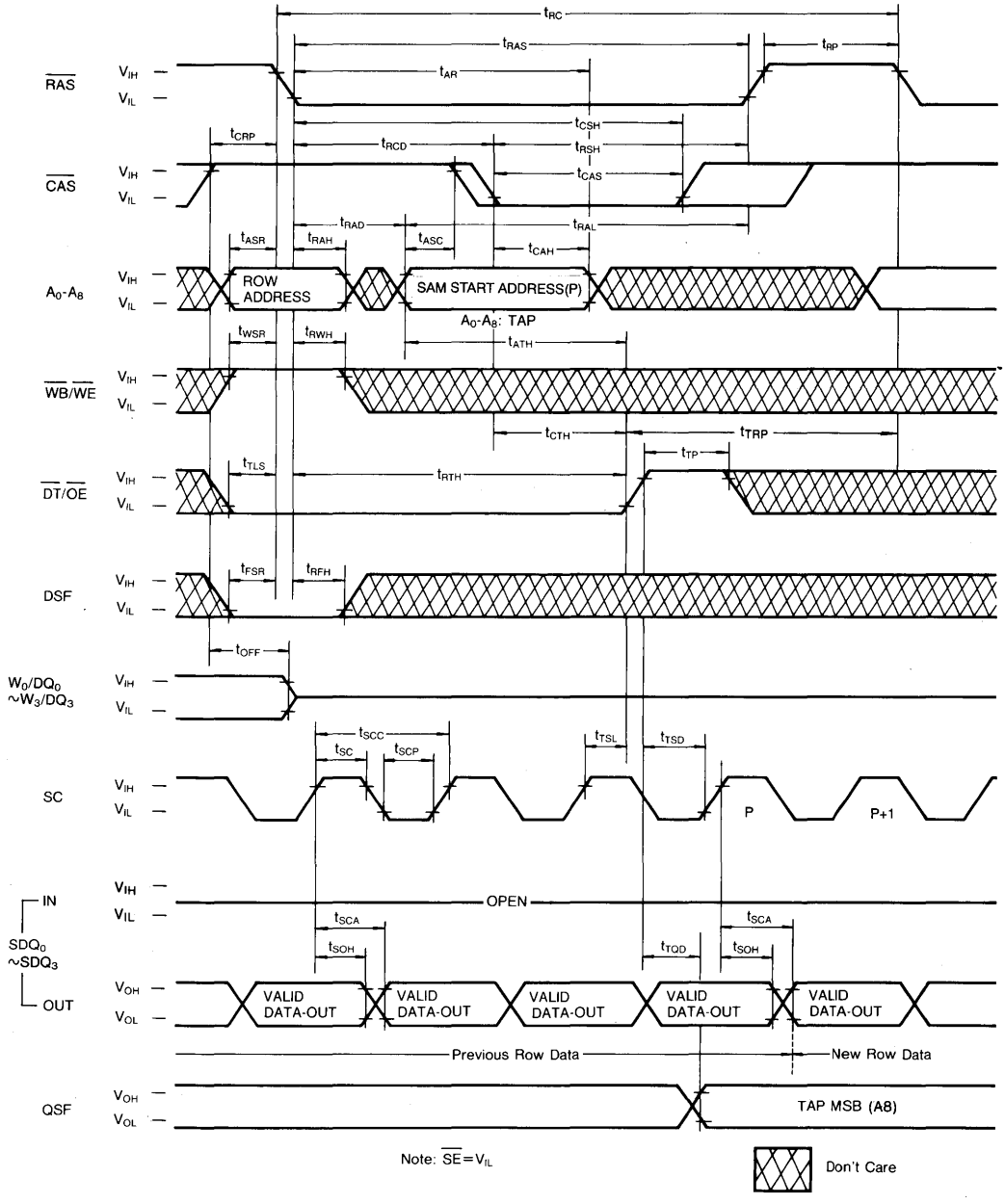
COLUMN SELECT DATA
W_0/DQ_0 — Column 0 (A_{IC}=0, A_{OC}=0)
W_1/DQ_1 — Column 1 (A_{IC}=0, A_{OC}=1)
W_2/DQ_2 — Column 2 (A_{IC}=1, A_{OC}=0)
W_3/DQ_3 — Column 3 (A_{IC}=1, A_{OC}=1)

Wn/DQn
= 0: Disable
= 1: Enable

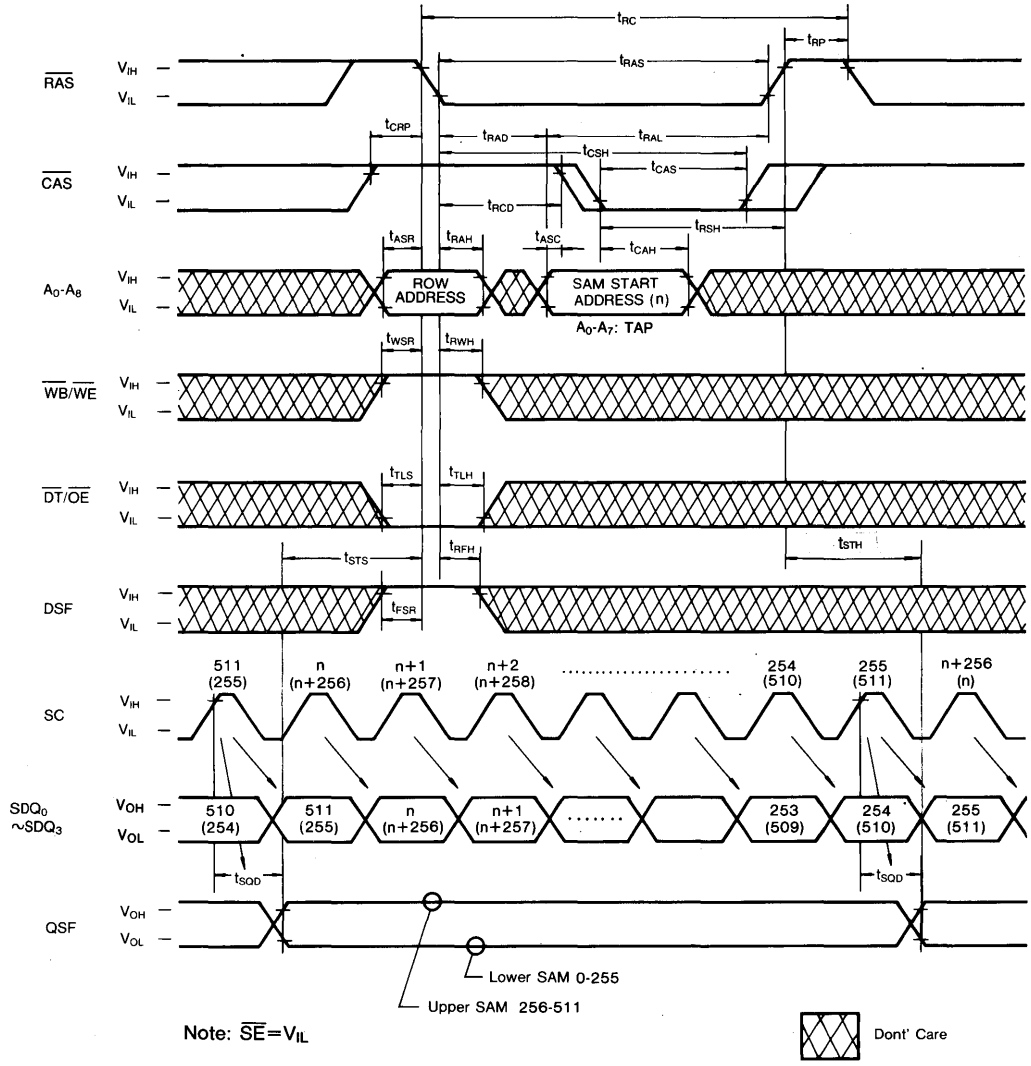
READ TRANSFER CYCLE



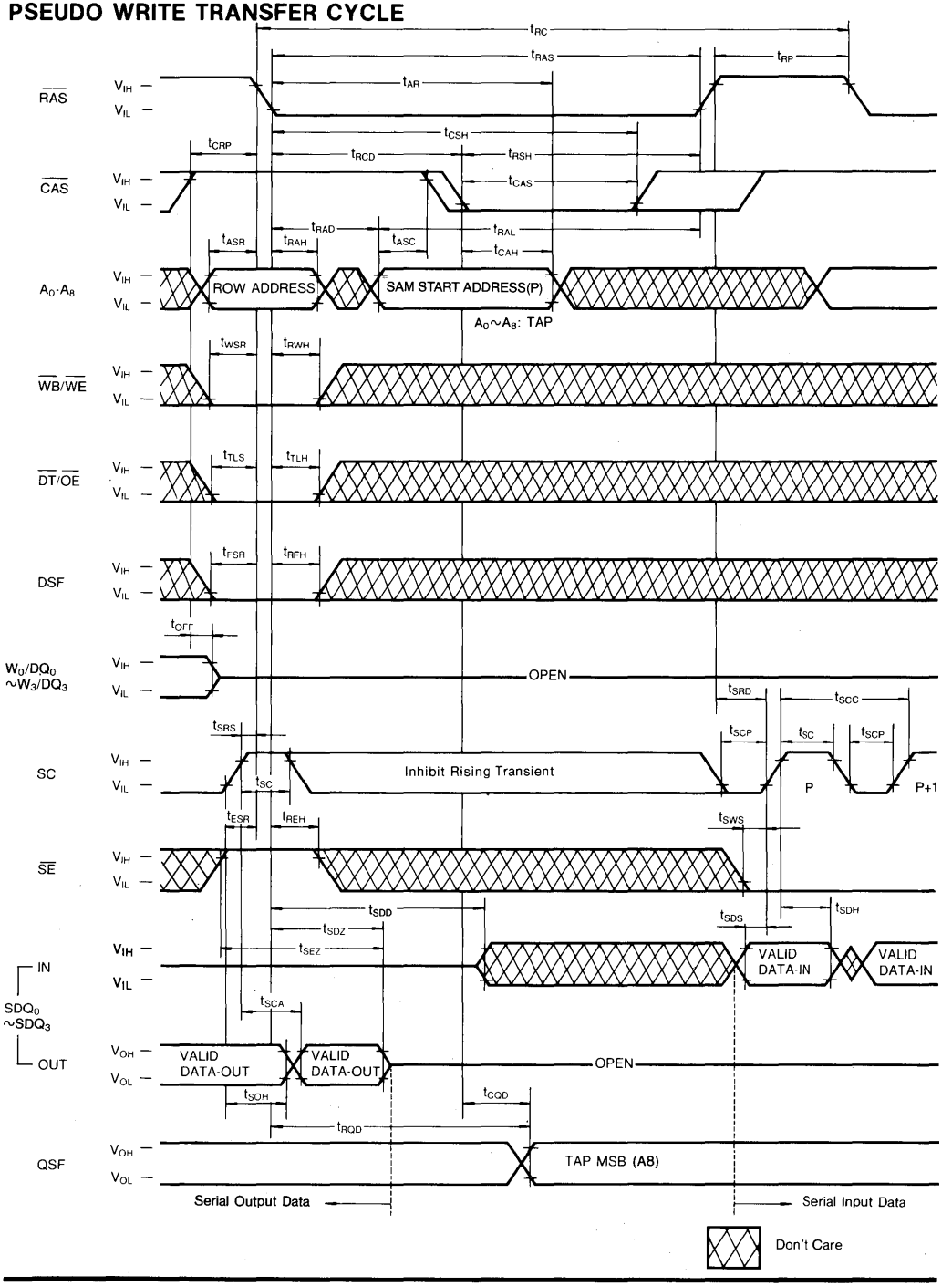
REAL TIME READ TRANSFER CYCLE



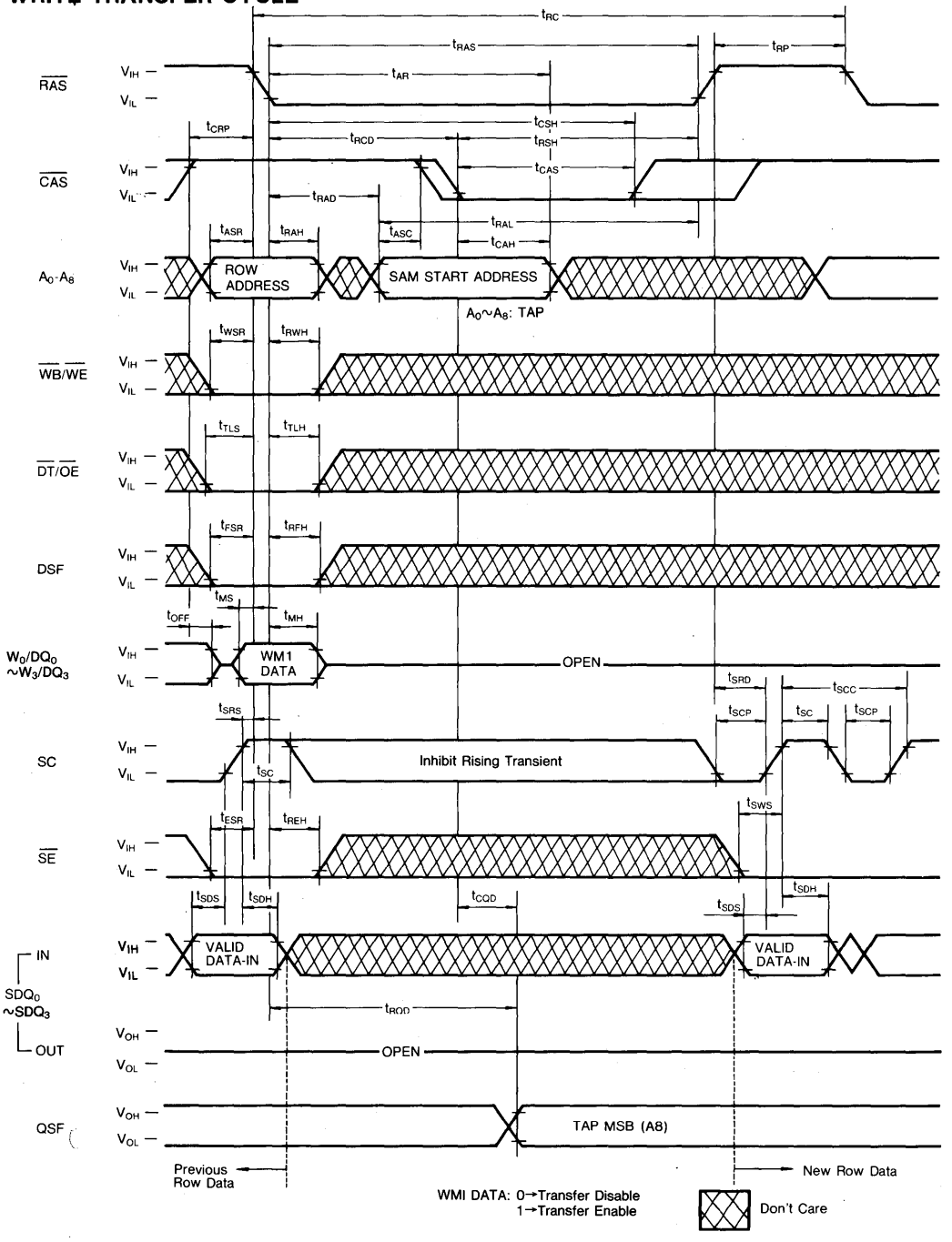
SPLIT READ TRANSFER CYCLE



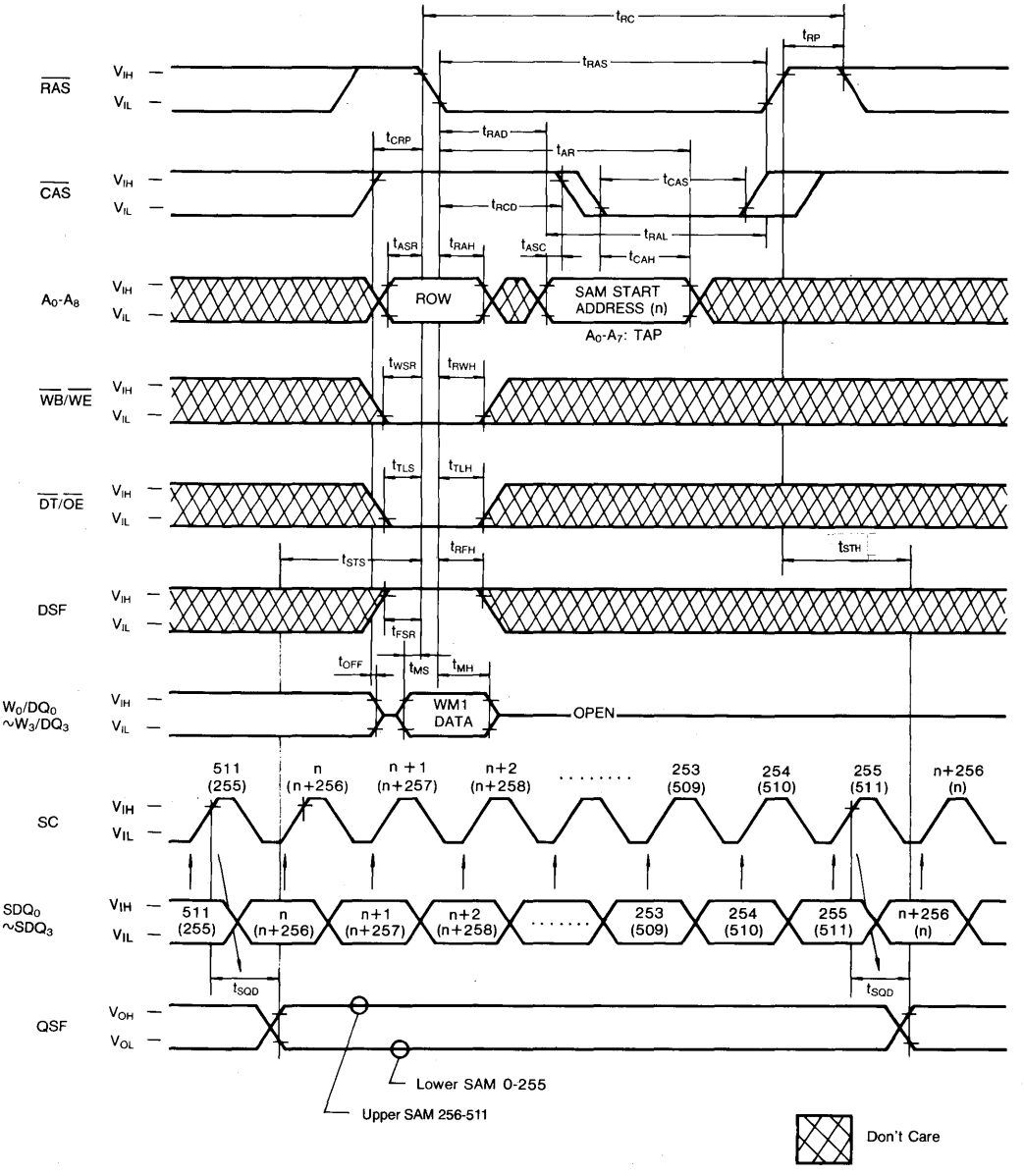
PSEUDO WRITE TRANSFER CYCLE



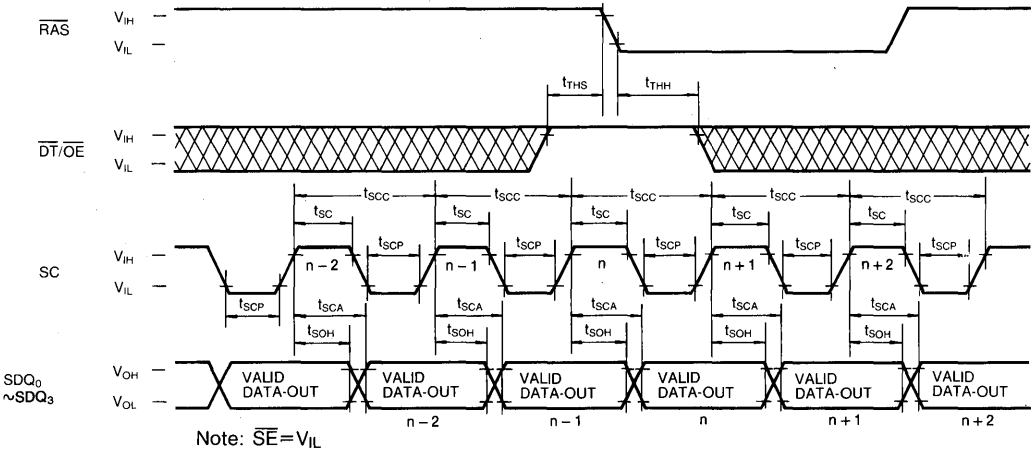
WRITE TRANSFER CYCLE



SPLIT WRITE TRANSFER CYCLE

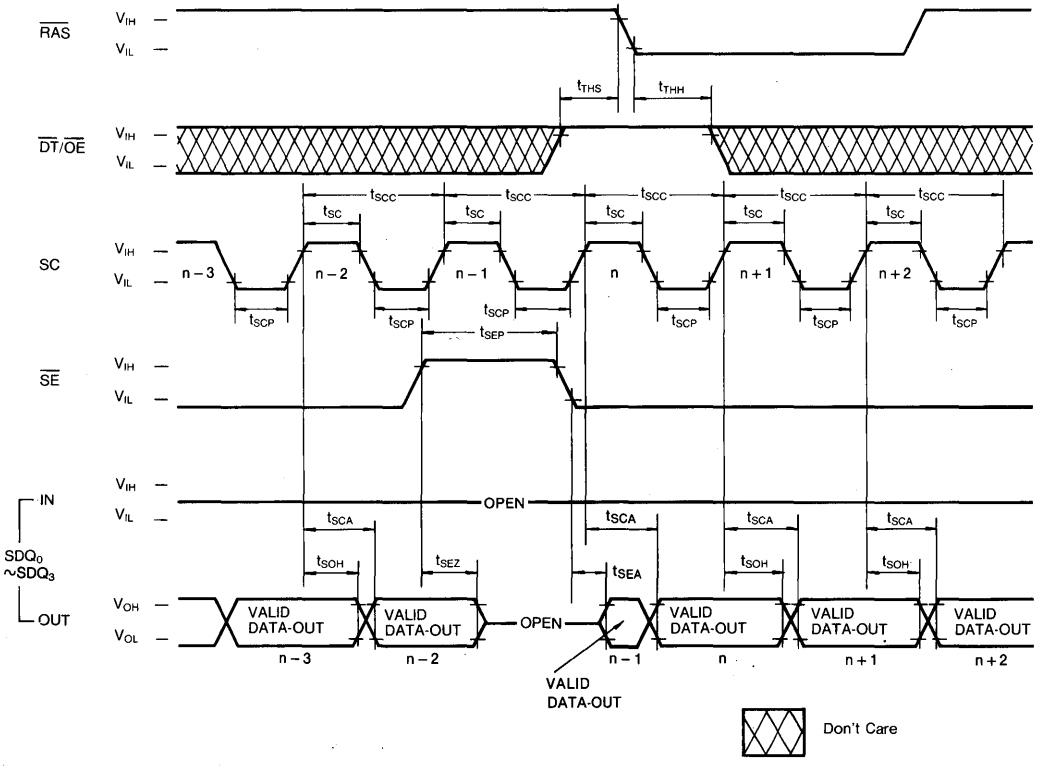


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

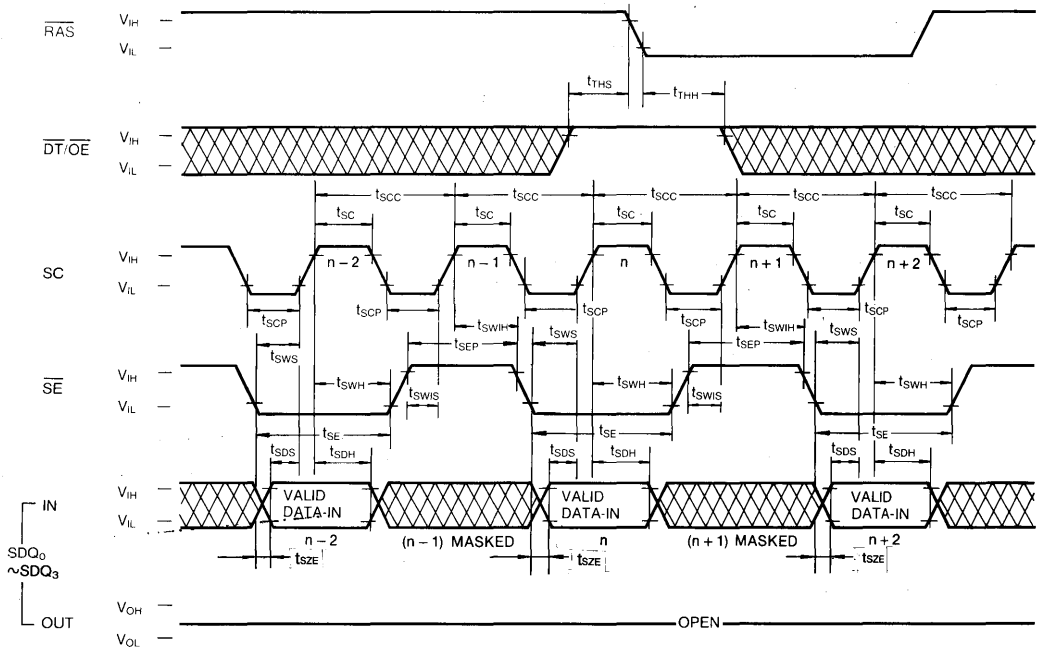


Note: $\overline{SE}$=V_{IL}

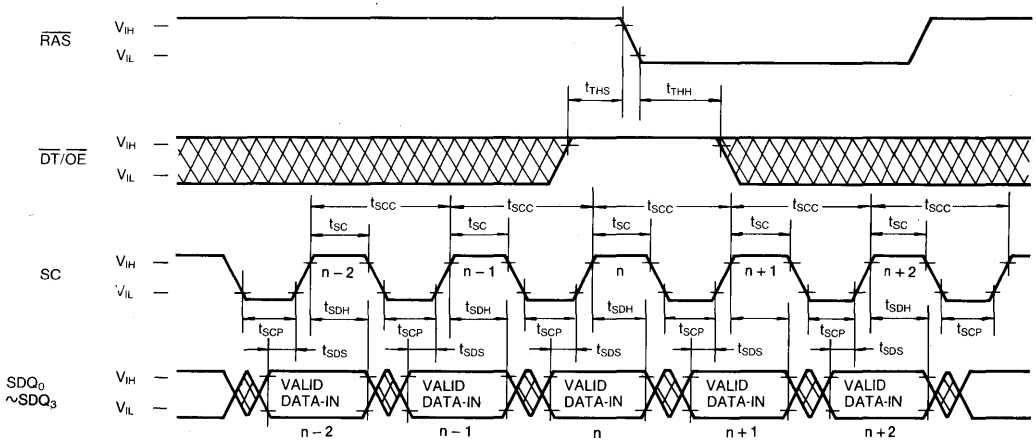
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



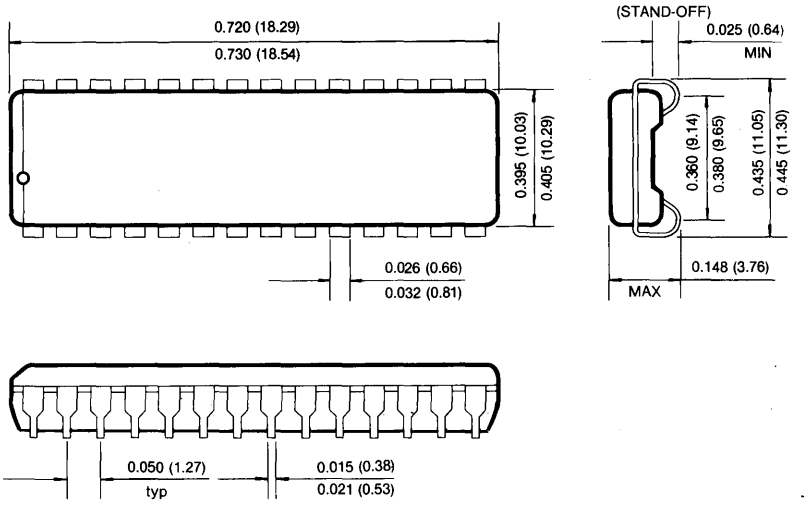
Note: $\overline{SE} = V_{IL}$

Don't Care

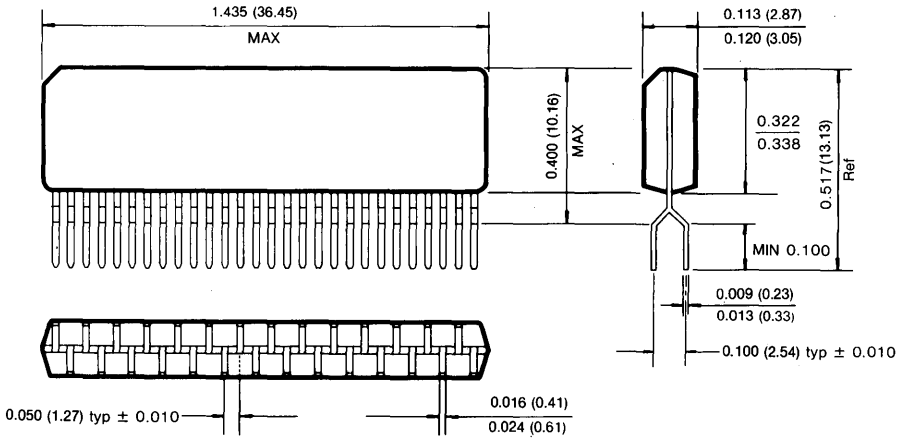
PACKAGE DIMENSIONS

28-PIN PLASTIC SOJ

Units Inches (millimeters)



28-PIN PLASTIC ZIP



128KX8 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  128K x 8 bits RAM port
  256 x 8 bits SAM port
- **Performance**

Parameter \ Speed	-6	-7	-8
RAM access time (t_{RAC})	60ns	70ns	80ns
RAM access time (t_{CAC})	20ns	20ns	20ns
RAM cycle time (t_{RC})	110ns	130ns	150ns
RAM page mode cycle (t_{PC})	40ns	45ns	50ns
SAM access time	18ns	20ns	20ns
SAM cycle time	20ns	25ns	25ns
RAM active current	90mA	85mA	80mA
SAM active current	50mA	45mA	40mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read, Real Time Read and Split Read Transfer (RAM→SAM)**
- **Write, Split Write Transfer with Masking operation (New Mask)**
- **Block Write, Flash Write and Write per bit with Masking operation (New Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output Control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single +5V±10% Supply Voltage**
- **Plastic 40-PIN 400 mil SOJ**

GENERAL DESCRIPTION

The Samsung KM428C128 is a CMOS 128KX8 bit Dual Port DRAM. It consists of a 128KX8 dynamic random access memory (RAM) port and 256X8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 2048 bits. It operates like a conventional 128KX8 CMOS DRAM. The RAM port has a write per bit mask capability.

The SAM port consists of eight 256 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

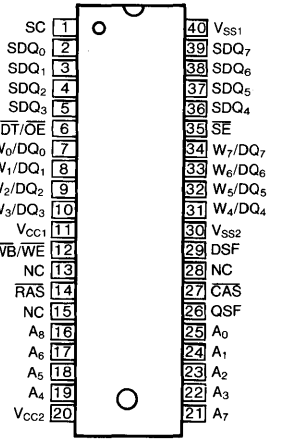
Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C128 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and Data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (Top Views)

40 Pin 400 mil SOJ

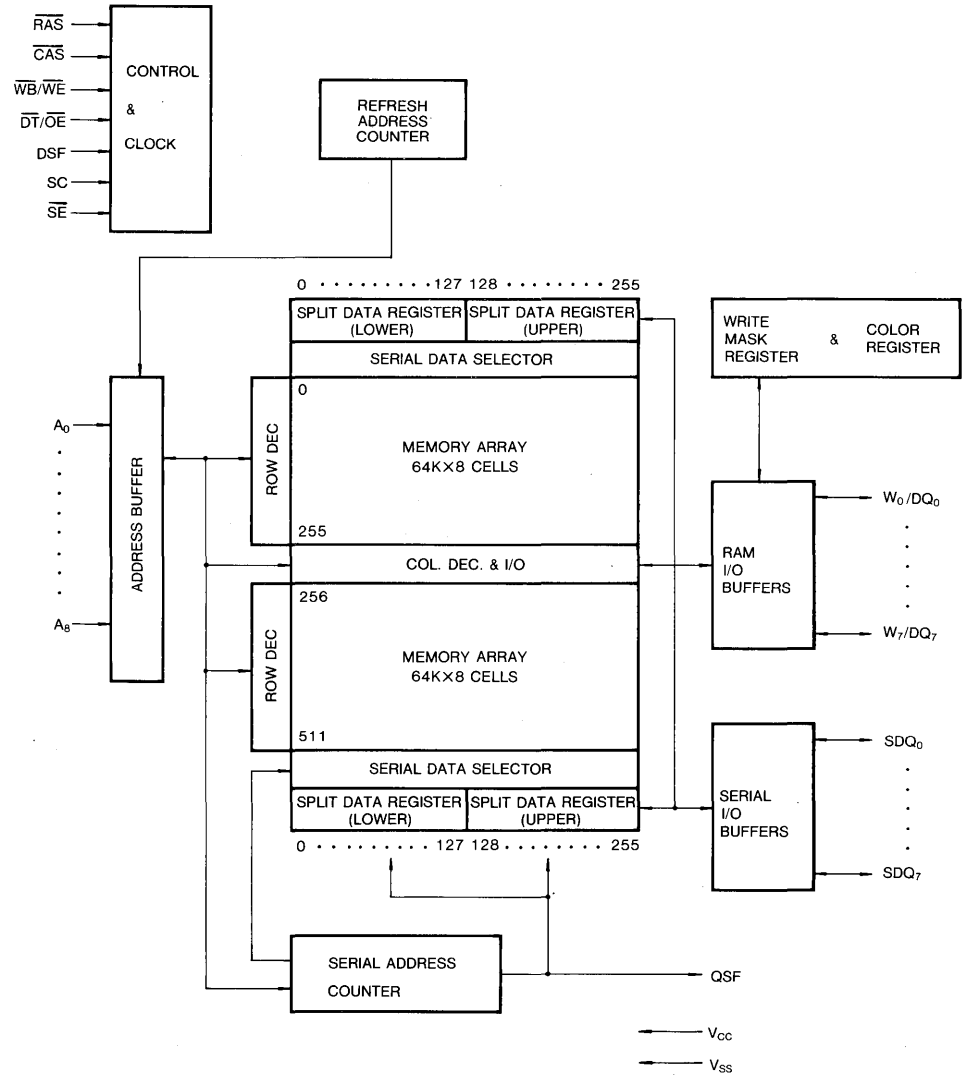


SAMSUNG ELECTRONICS

PIN DESCRIPTION

Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 8 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 8 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ input is a multifunction pin. when $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions(BW, FW, Split Transfer, etc)are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0-255, High if address is 256-511.
$\overline{SE}$	IN	In a serial read cycle. $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
V_{CC}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	$\overline{RAS}$					$\overline{CAS}$	Address*1		DQi Input*2		Write Mask	Color Register	Function
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS/WE}$			
CBR	0	X	X	X	X	–	X	X	X	–	–	–	CBR Refresh
ROR	1	1	X	0	X	–	Row	X	X	–	–	–	$\overline{RAS}$-only Refresh
RW	1	1	1	0	X	0	Row	Col.	X	Data	–	–	Normal DRAM Read/ Write(No. Mask)
RW/NM	1	1	0	0	X	0	Row	Col.	WMi	Data	Use	–	Masked DRAM Write (New Mask)
MFLW	1	1	0	1	X	X	Row	X	WMi	X	Use	Use	Masked Flash Write (New Mask)
BW	1	1	1	0	X	1	Row	Col. (A2~A7)	X	Col. Mask	–	Use	Block Write (No Mask)
BW/NW	1	1	0	0	X	1	Row	Col. (A2~A7)	WMi	Col. Mask	Use	Use	Masked Block Write (New Mask)
LCR	1	1	1	1	X	1	Row*3	X	X	Coor Mask	–	Load	Load Color Register
RT	1	0	1	0	X	X	Row	Tap	X	X	–	–	Read Transfer
SRT	1	0	1	1	X	X	Row	Tap	X	X	–	–	Split Read Transfer
PWT	1	0	0	0	1	X	Row*3	Tap	X	X	–	–	Pseudo Write Transfer
MWT	1	0	0	0	0	X	Row	Tap	WMi	X	Use	–	Masked Write Transfer(New Mask)
MSWT	1	0	0	1	X	X	Row	Tap	WMi	X	Use	–	Masked Split Write Transfer(New Mask)

X: Don't Care, -: Not Applicable

Note

*1 : These column show what must be present on the A_0~A_8 outputs at the falling edge of $\overline{RAS}$ and $\overline{CAS}$.

*2 : These column show what must be present on the DQ_0~DQ_3 outputs at the falling edge of $\overline{RAS}$, $\overline{CAS}$ or $\overline{WB/WE}$, whichever is later.

*3 : The Row that is addressed will be refreshed.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1V	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input 0≤V_{IN}≤V_{CC} +0.5V all other pins not under test=0 volts)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	I_{OL}	−10	10	μA
Output High Voltage Level (RAM I_{OH}=−5mA, SAM I_{OH}=−2mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (RAM I_{OL}=4.2mA, SAM I_{OL}=2mA)	V_{OL}	—	0.4	V

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0-W_3/DQ_3)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0-SDQ_3)	C_{SDQ}	2	7	pF
Output Capacitance (QSF)	C_{QSF}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM428C128			Unit
			-6	-7	-8	
Operating Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC1}	90	85	80	mA
	Active	I_{CC1A}	140	130	120	mA
Standby Current*1 ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$=$V_{IH}$,DSF=$V_{IL}$)	Standby	I_{CC2}	5	5	5	mA
	Active	I_{CC2A}	50	45	40	mA
$\overline{RAS}$ Only Refresh Current*1 ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @tRC=min.)	Standby	I_{CC3}	90	85	80	mA
	Active	I_{CC3A}	140	130	120	mA
Fast Page Mode Current*1 ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @tPC=min.)	Standby	I_{CC4}	70	65	60	mA
	Active	I_{CC4A}	120	110	100	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC5}	90	85	80	mA
	Active	I_{CC5A}	140	130	120	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC6}	120	115	110	mA
	Active	I_{CC6A}	170	160	150	mA
Flash Write Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC7}	90	85	80	mA
	Active	I_{CC7A}	140	130	120	mA
Block Write Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC8}	100	95	90	mA
	Active	I_{CC8A}	150	140	130	mA
Color Register Load or Read Cycle ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC9}	90	85	80	mA
	Active	I_{CC9A}	140	130	120	mA

Note*1 : Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as a average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, I_{CC9}, address transition should be changed only while $\overline{RAS}$=V_{IL}

In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, see notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		200		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		20	ns	4
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ Precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output butter turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ Precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width(fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	20	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR Counter Test)	t_{CPT}	10		10		10		ns	
$\overline{CAS}$ precharge time(fast page mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column address hold to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

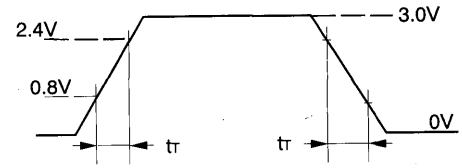
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay(Fast Page mode)	t_{CPWD}	60		65		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
Access time from output enable	t_{OEA}		20		20		20	ns	
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	7
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period(512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$ (I)	t_{FHR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$ (I)	t_{FSR}	45		55		60		ns	
DSF hold time referenced to $\overline{RAS}$ (II)	t_{RFH}	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{SE}$ setup referenced to $\overline{RAS}$	t_{ESR}	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	10		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ precharge time	t_{TRP}	40		50		60		ns	
$\overline{DT}$ precharge time	t_{rp}	20		20		25		ns	
$\overline{RAS}$ to first SC delay(read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	t_{CSD}	25		30		35		ns	
Col.Addr.to first SC delay(read transfer)	t_{ASD}	35		40		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay(read transfer)	t_{TSD}	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up(serial input)	t_{SRS}	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	t_{SRD}	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	t_{SDD}	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	t_{SDZ}	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	20		25		25		ns	12
SC pulse width(SC high time)	t_{SC}	6		7		7		ns	
SC precharge(SC low time)	t_{SCP}	6		7		7		ns	
Access time from SC	t_{SCA}		18		20		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	10		15		15		ns	
Access time from $\overline{SE}$	t_{SEA}		15		20		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial out butter turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	5		5		5		ns	
Serial write enable hold time	t_{SWH}	10		15		15		ns	
Serial write disable set-up time	t_{SWIS}	5		5		5		ns	
Serial write disable hold time	t_{SWIH}	15		15		15		ns	
Split transfer set-up time	t_{STS}	25		25		25		ns	
Split transfer hold time	t_{STH}	25		25		25		ns	
SC-QSF delay time	t_{SQD}		25		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		25		25		25	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		30		35		40	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		60		70		80	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. If the Internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ inltialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs. Inputs signal transition from 0V to 3V for AC Testing.
3. RAM port outputs are measured with a load equivalent to 1 TTL loads and 50pF. D_{OUT} comparator level: V_{OH}/V_{OL}=2.0/0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL loads and 30pF. D_{OUT} comparator level: V_{OH}/V_{OL}=2.0/0.8V
5. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), t_{SDZ}(max) and t_{SEZ}(max), define the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Assume t_T=3ns.
13. Recommended operating input condition. Input pulse levels are from 0.0V to 3.0 Volts. All timing measurements are referenced from V_{IL}(max) and V_{IH}(min) with transition=3.0ns



14. t_{WCR}, t_{DHR} are referenced to t_{RAD}. (max.)

DEVICE OPERATION

The KM428C128 contains 1,048,576 memory locations. Seventeen address bits are required to address a particular 8-bit word in the memory array. Since the KM428C128 has only 0 address input pins, time multiplexed addressing is used to input 9 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CAS}$)and the valid row and column address inputs.

Operation of the KM428C128 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM428C128 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C128 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}.

The KM428C128 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Write

The KM428C128 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$, whichever is later.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Write-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in Table 1.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
⎺_	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	INHIBIT WRITE

DEVICE OPERATION (Continued)

Block Write

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "Low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled as write per bit function. At the falling edge of $\overline{CAS}$, the starting column address pointer and column mask data must be provided. During a block write cycle, the 2 least significant column address(A_0 and A_1) are internally controlled and only the six most significant column address(A_2-A_7)are latched at the falling edge of $\overline{CAS}$.

Flash Write

Flash write is mainly used for fast clear operations in frame buffer applications. A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the Wi/DQi lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks.

Data Output

The KM428C128 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{DT}/\overline{OE}$. When either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM428C128 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modity-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write, Read Color Register.

Refresh

The data in the KM428C128 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address, (A_0-A_8).

$\overline{CAS}$ before-$\overline{RAS}$ Refresh: The KM428C128 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM428C128 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM428C128 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

1. Normal Write/Read Transfer (SAM→RAM/RAM→SAM.).
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM.).
3. Real Time Read Transfer (On the fly Read Transfer operation).
4. Split Write/Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred from/to the SAM while the other half is write to/read from the SDQ pins.).

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address

DEVICE OPERATION (Continued)

selected at the falling edge of $\overline{RAS}$ determines the RAM row to be trasferred into the SAM.

The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the otuput mode. In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the $\overline{SDQ}$ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Table 2. Truth table for Transfer operation

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bits	Sam port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM→SAM	256×8	Input→Output
H	L	L	L	L	Masked Write Transfer	SAM→RAM	256×8	Output→Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output→Input

*: Don't Care

Write Transfer Cycle

A write transfer cycle consists of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transfered. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When two consecutive write transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has seen satisfied, A rising edge of the SC clock until must not occur after a specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A psuedo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

Special Function Input (DSF)

In read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split register mode read transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of most significant column address bit(A_7) that is strobed in on the falling edge of $\overline{CAS}$. If A_7 is high, the transfer is to the high half of the register. If A_7 is low, the transfer is to the low half of the register. Use of the split register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{DT}/\overline{OE}$ to the serial clock. The transfer can be to either the active half or the inactive half register. If the transfer is to the active register, with an uninterrupted serial data stream, then the timings t_{TSL} and t_{TSD} must be met.

In write tranfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of a Split Register mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without performing a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

DEVICE OPERATION(Continued)

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(256bit)to be transferred to the selected row in the DRAM array. masking is selected by latching Wi/DQi(i-0~7) inputs when $\overline{RAS}$ goes low.

The Column address defines defines the start address of serial input and its MSB(A_8)defines QSF level.

If A_8 is low, the QSF will be low level to designate that the start address is in positioned in the lower half of SAM.(For A_8=high, the QSF will be high and indicates that the start address will be positioned in the upper half of(SAM) After write transfer cycle is completed. SAM ports is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$)because the transfer has to occur at the first rising edge of $\overline{DT}/\overline{OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 128 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state QSF.

A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WE}/\overline{WB}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_6) defines the starting address of the SAM port from which data will begin shifting out. column address pin A_7, A_8 are " Don't Care".

The QSF pin indicates which SAM half is shifting out serial data(0=Lower, 1=Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary(e.g. 127th or 255th bit).

Masked Split Write Transfer(MSWT)

This transfer function is very similar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "Don't Care". The opening cycle of either MWT or PWT is needed before MSWT can be performed.

Split Register Active status Output(QSF)

QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low(least significant) 128 bits of the SAM. If QSF is high, then the pointer is accessing the higher(most significant)128 bits of the SAM.

Serial clock(SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

DEVICE OPERATION(Continued)

Serial Input/Output(SDQ0~SDQ7)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains in the input mode.

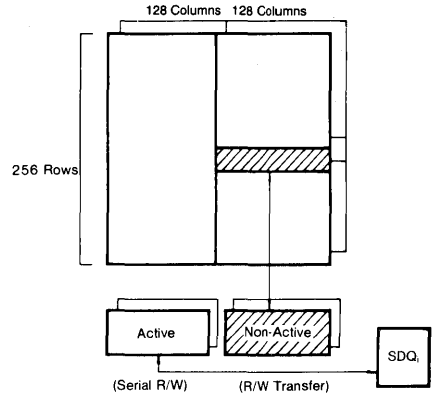
Tap Address Limitation

The Tap Address of non-split transfer cycle preceding split transfer cycle should be between 0 and 126 or between 128 and 254.

Power-up

During Power-up $\overline{RAS}$, $\overline{DT}/\overline{OE}$, must be held High or track with V_{CC}.

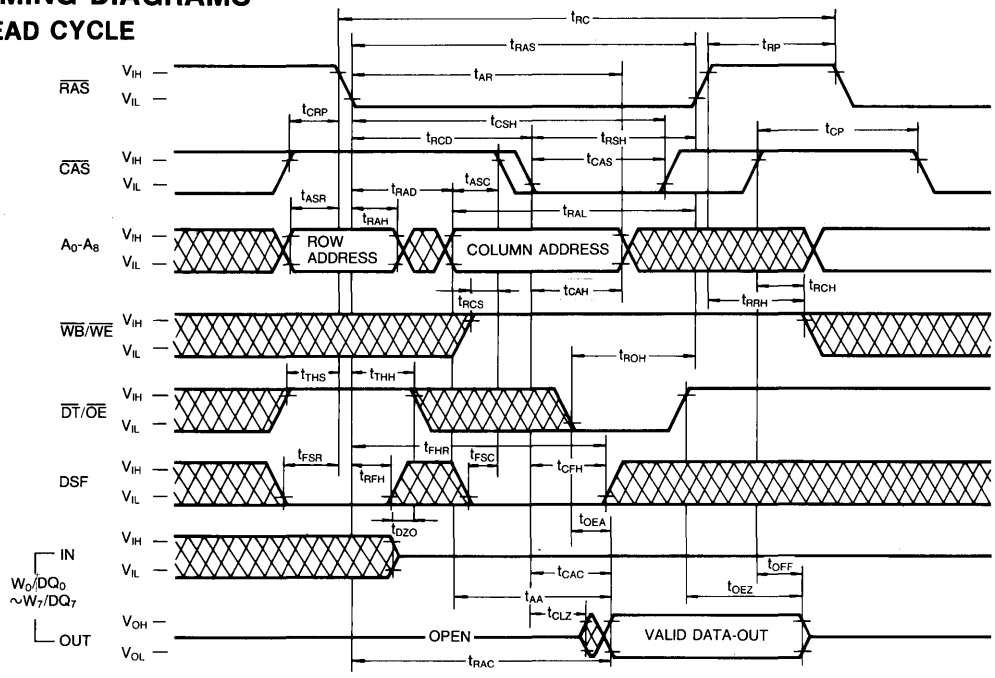
Table 3. SPLIT REGISTER MODE



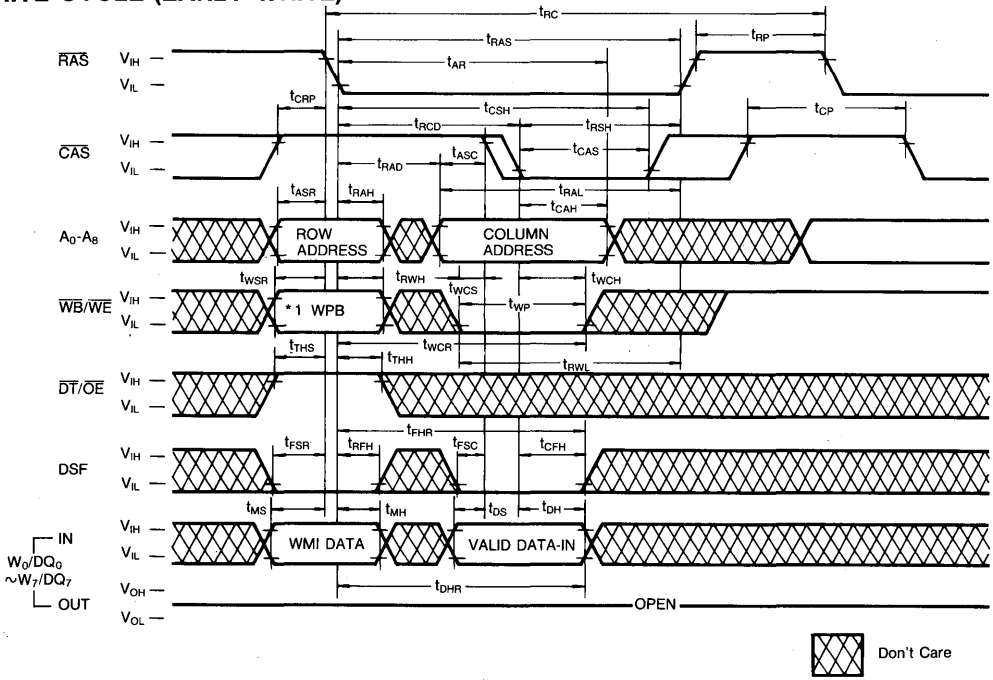
Active SAM	QSF Level
LOWER SAM	LOW
UPPER SAM	HIGH

TIMING DIAGRAMS

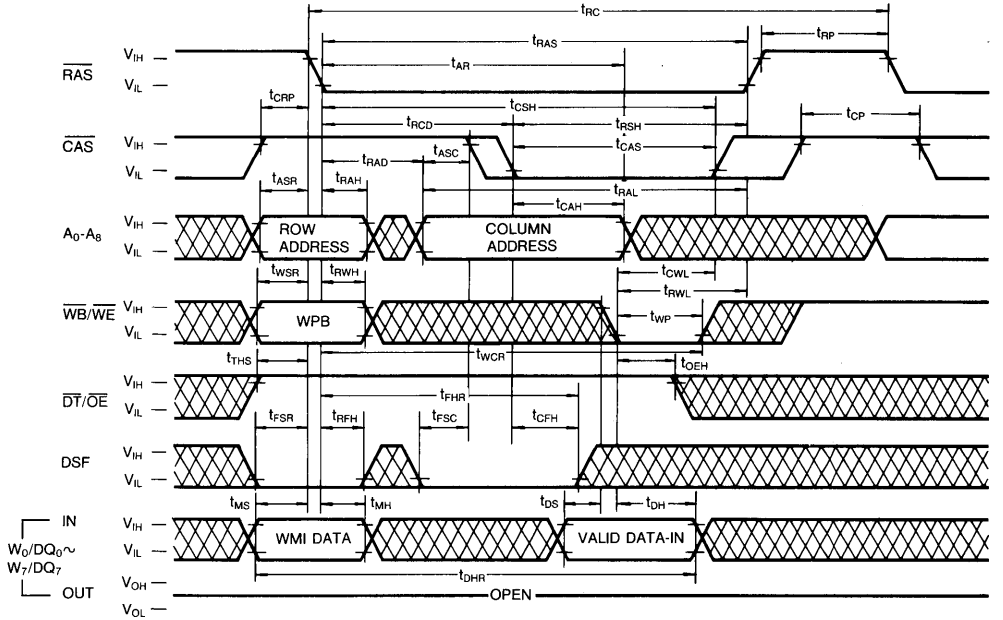
READ CYCLE



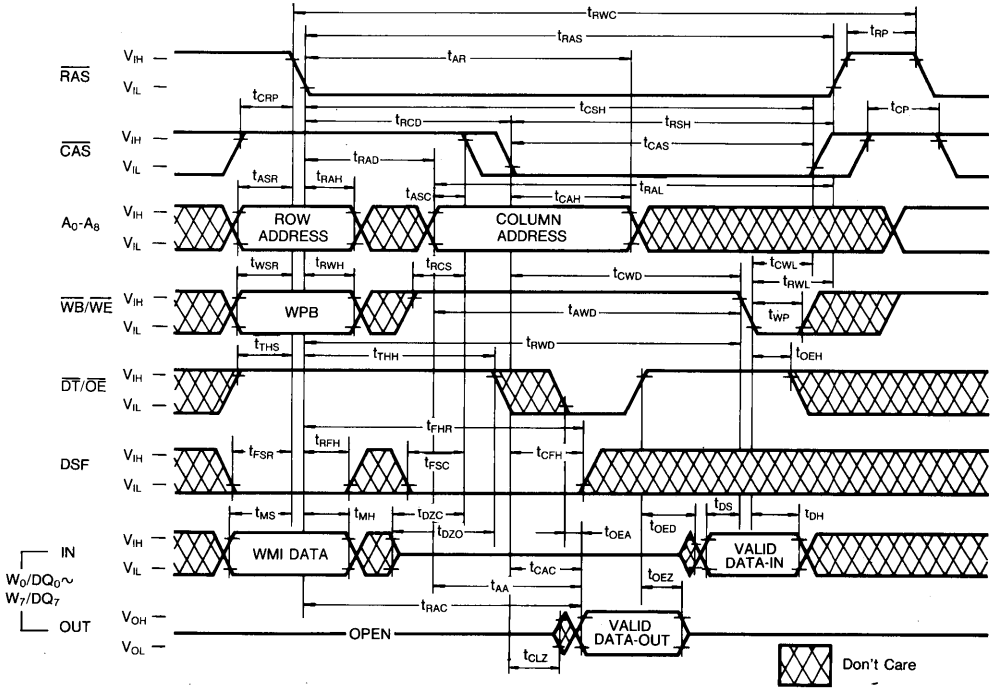
WRITE CYCLE (EARLY WRITE)



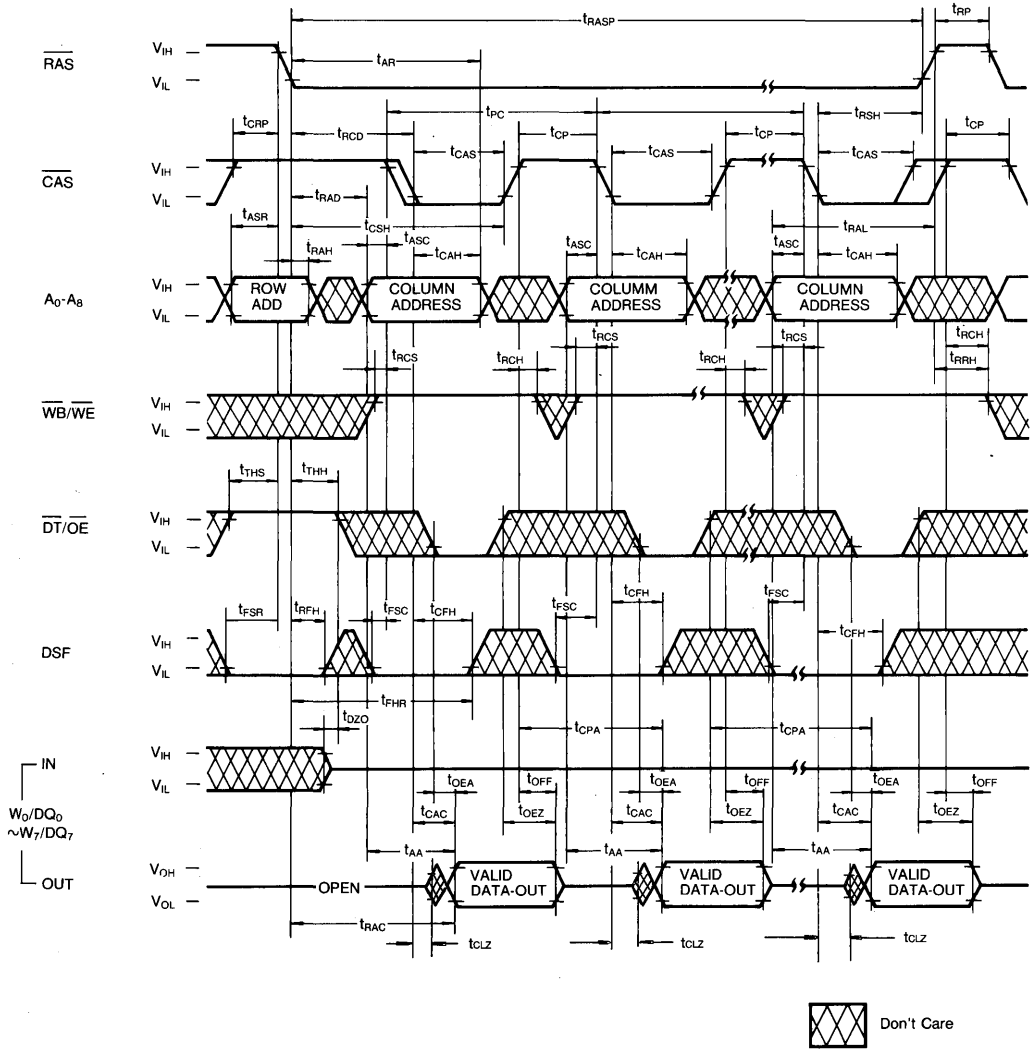
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



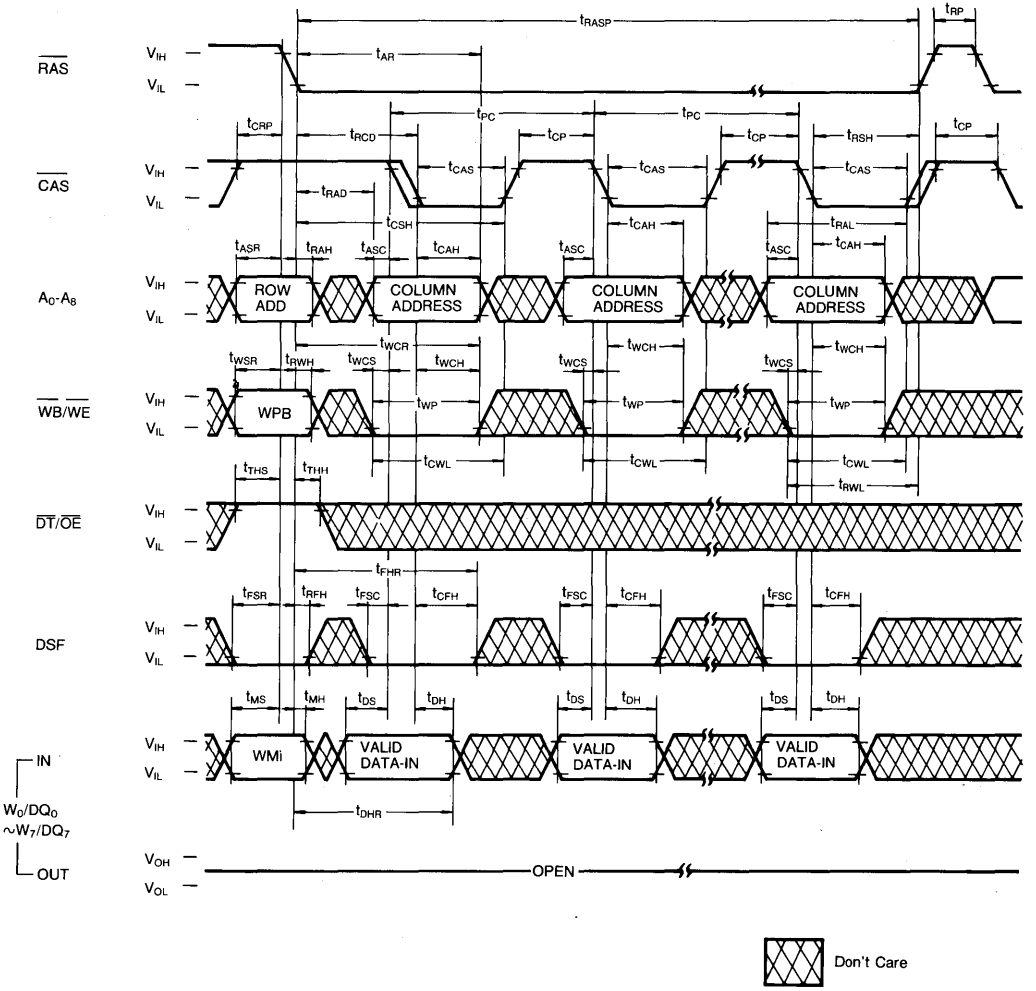
READ-WRITE/READ-MODIFY-WRITE CYCLE



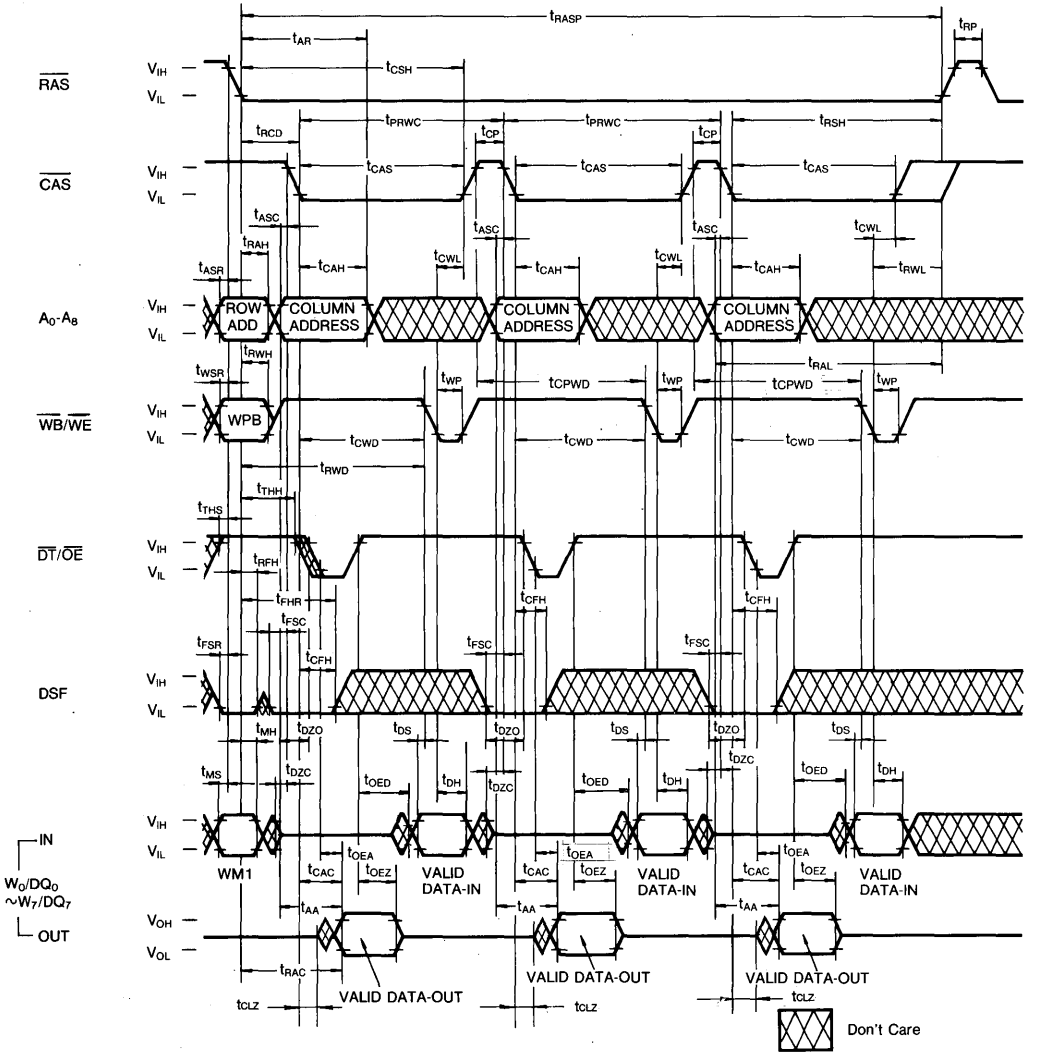
PAGE MODE READ CYCLE



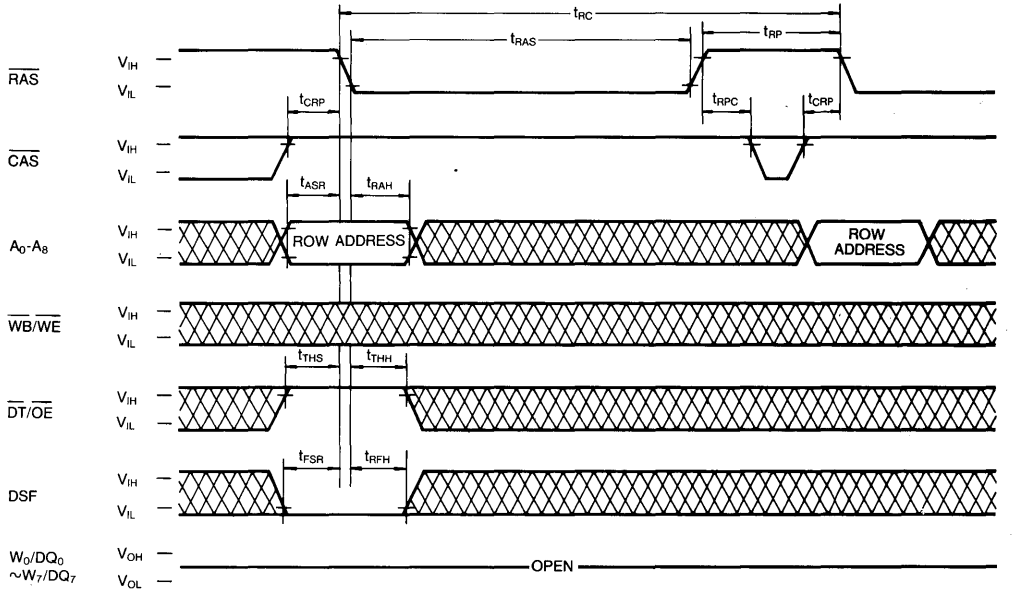
PAGE MODE WRITE CYCLE (EARLY WRITE)



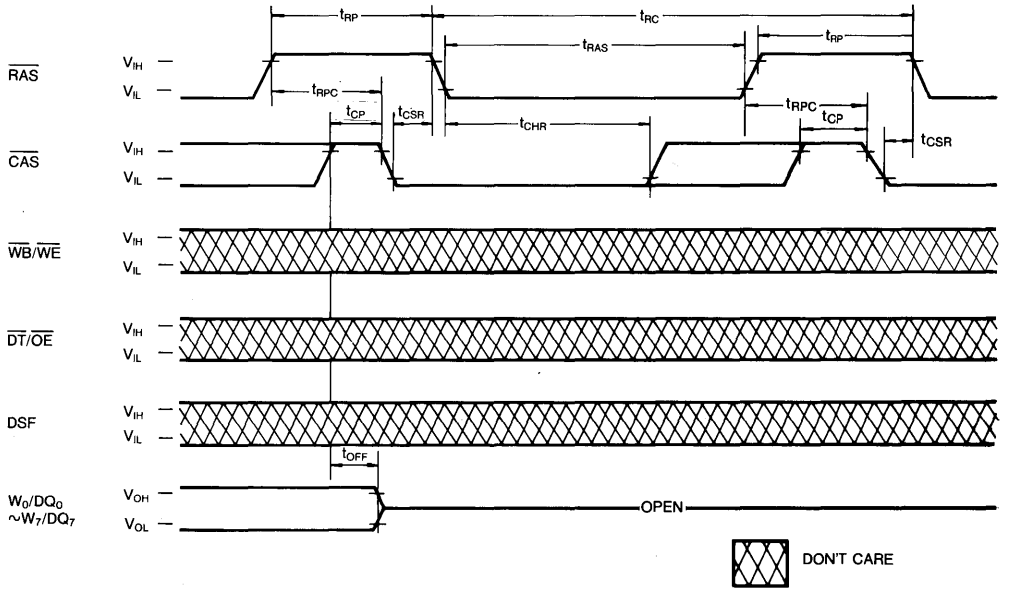
PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

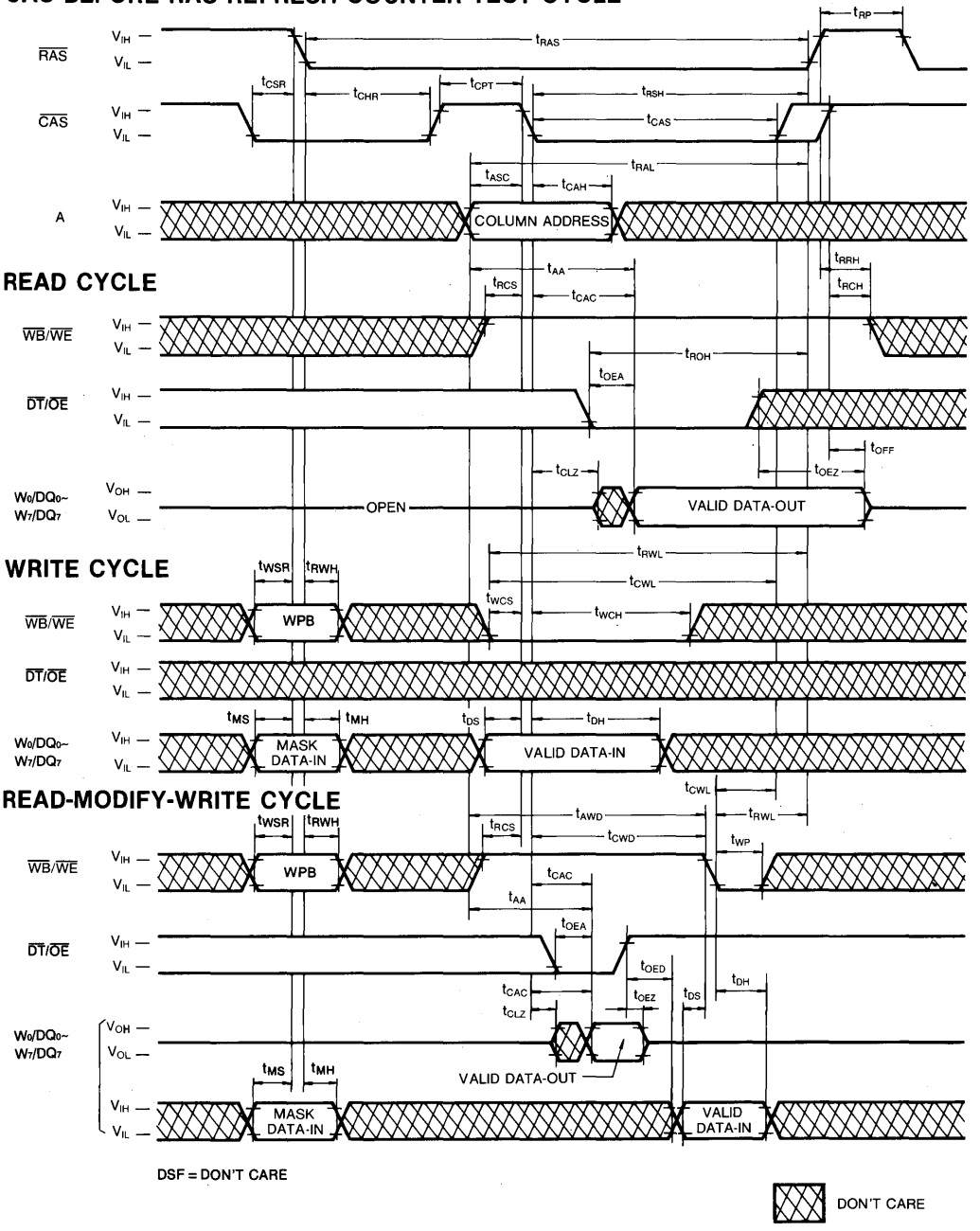


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

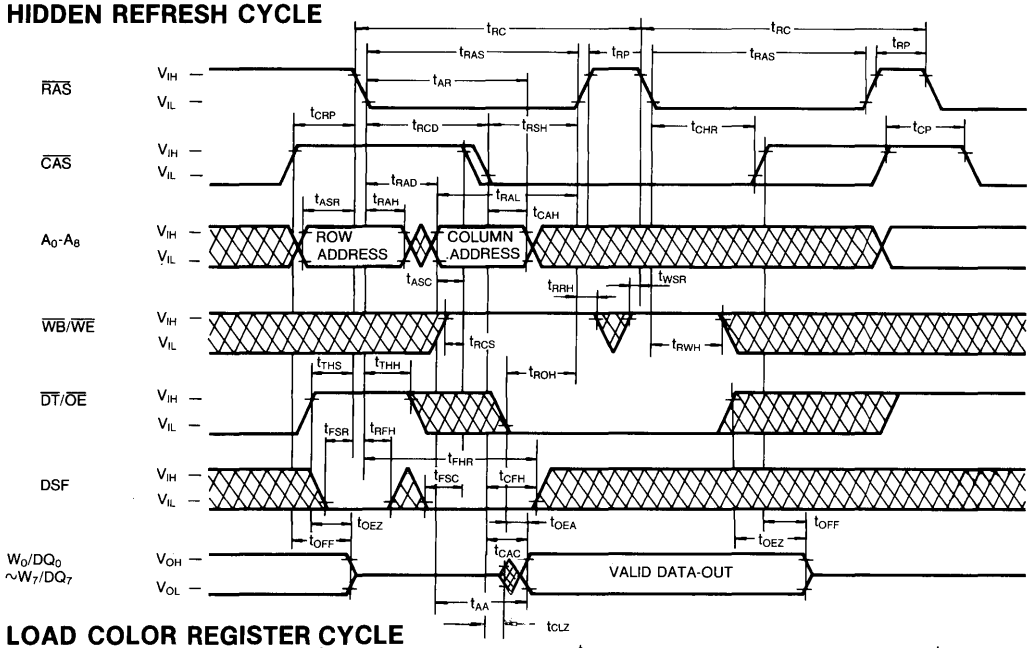
READ CYCLE

WRITE CYCLE

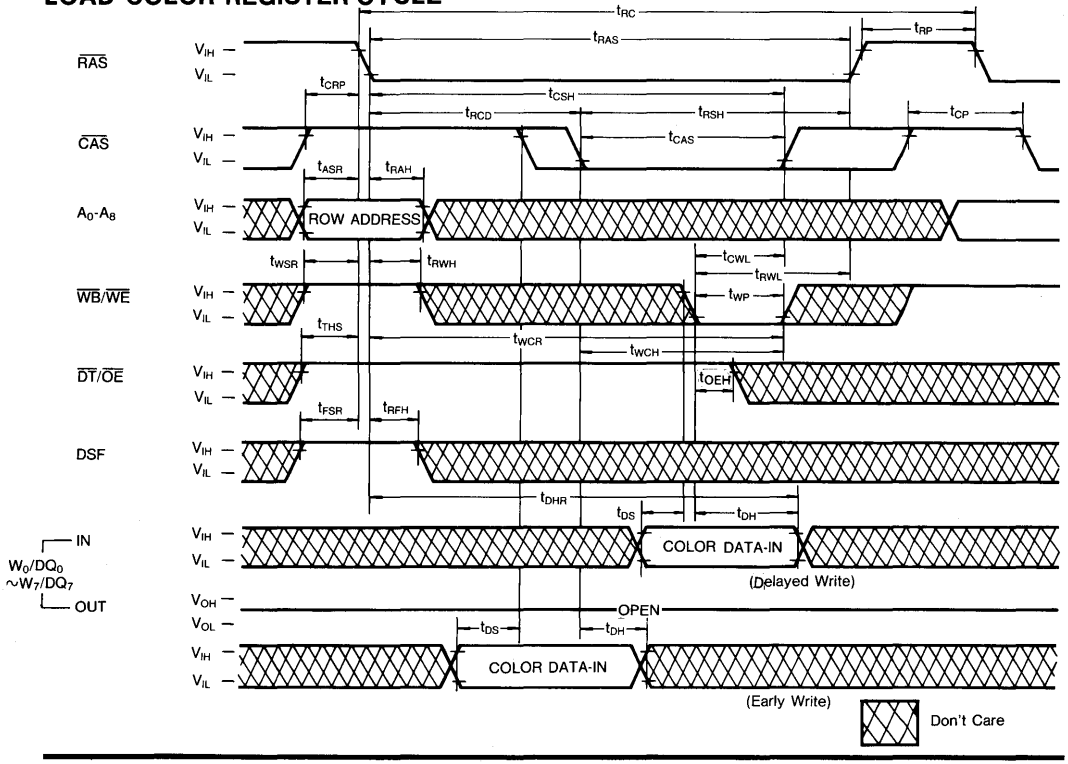
READ-MODIFY-WRITE CYCLE



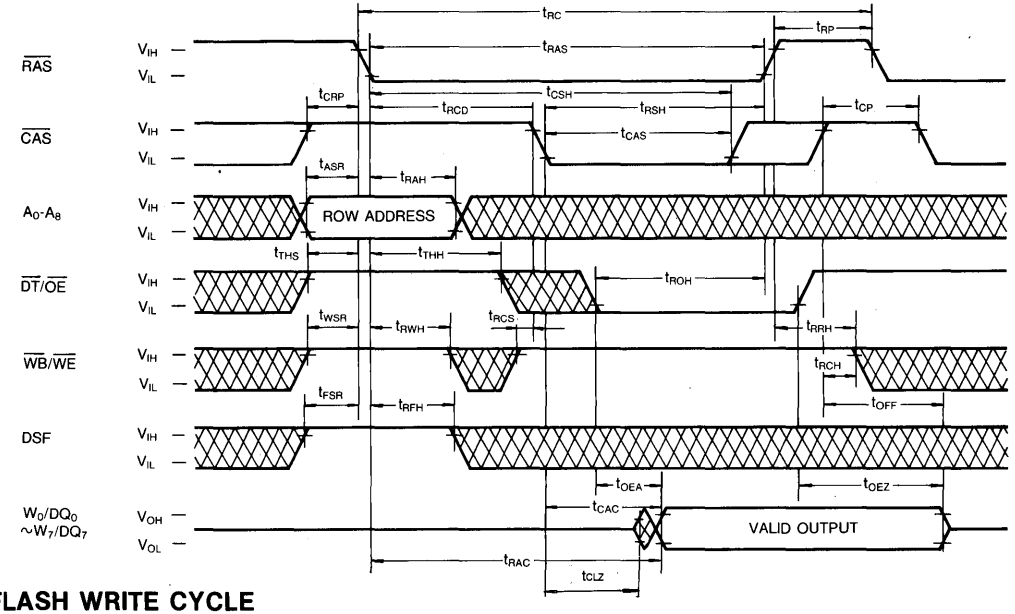
HIDDEN REFRESH CYCLE



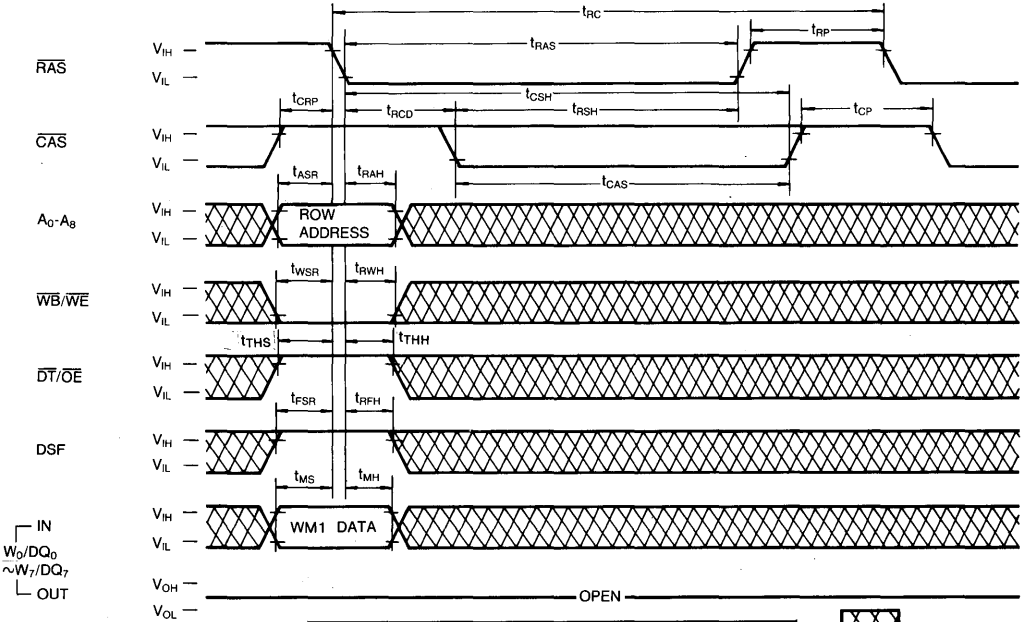
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE



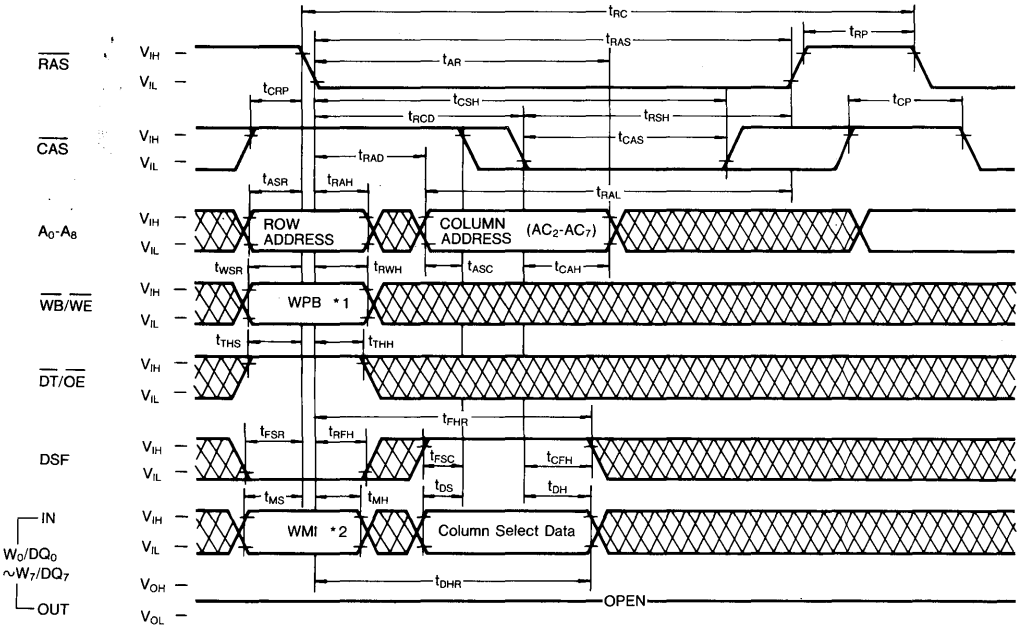
FLASH WRITE CYCLE



WM1 DATA	CYCLE
0	Flash write Disable
1	Flash write Enable

Don't Care

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_7/DQ_7	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

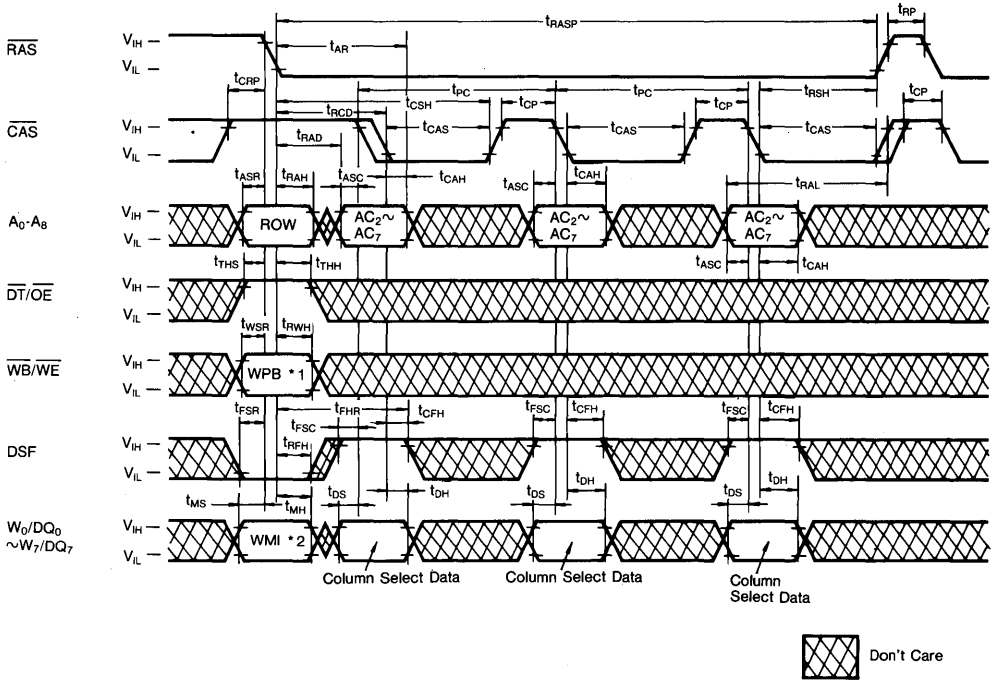
WM1 Data: 0: Write Disable
1: Write Enable

COLUMN SELECT DATA

W_0/DQ_0 - Column 0 (A_{1C}=0, A_{0C}=0)
W_1/DQ_1 - Column 1 (A_{1C}=0, A_{0C}=1)
W_2/DQ_2 - Column 2 (A_{1C}=1, A_{0C}=0)
W_3/DQ_3 - Column 3 (A_{1C}=1, A_{0C}=1)

Wn/DQn
= 0: Disable
= 1: Enable

PAGE MODE BLOCK WRITE CYCLE



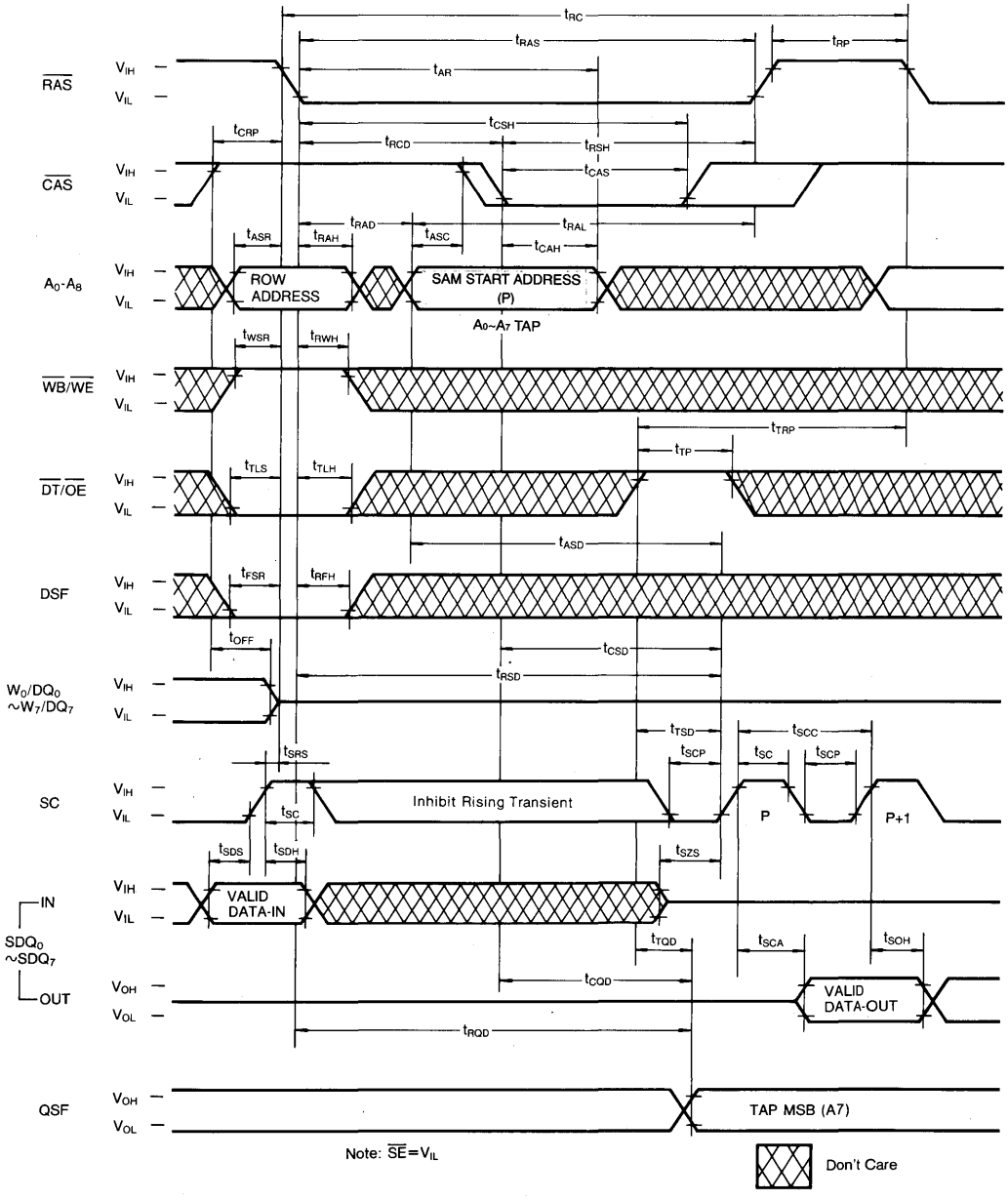
*1 $\overline{WB}/\overline{WE}$	*2 W_0/DQ_0-W_7/DQ_7	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 Data: 0: Write Disable
1: Write Enable

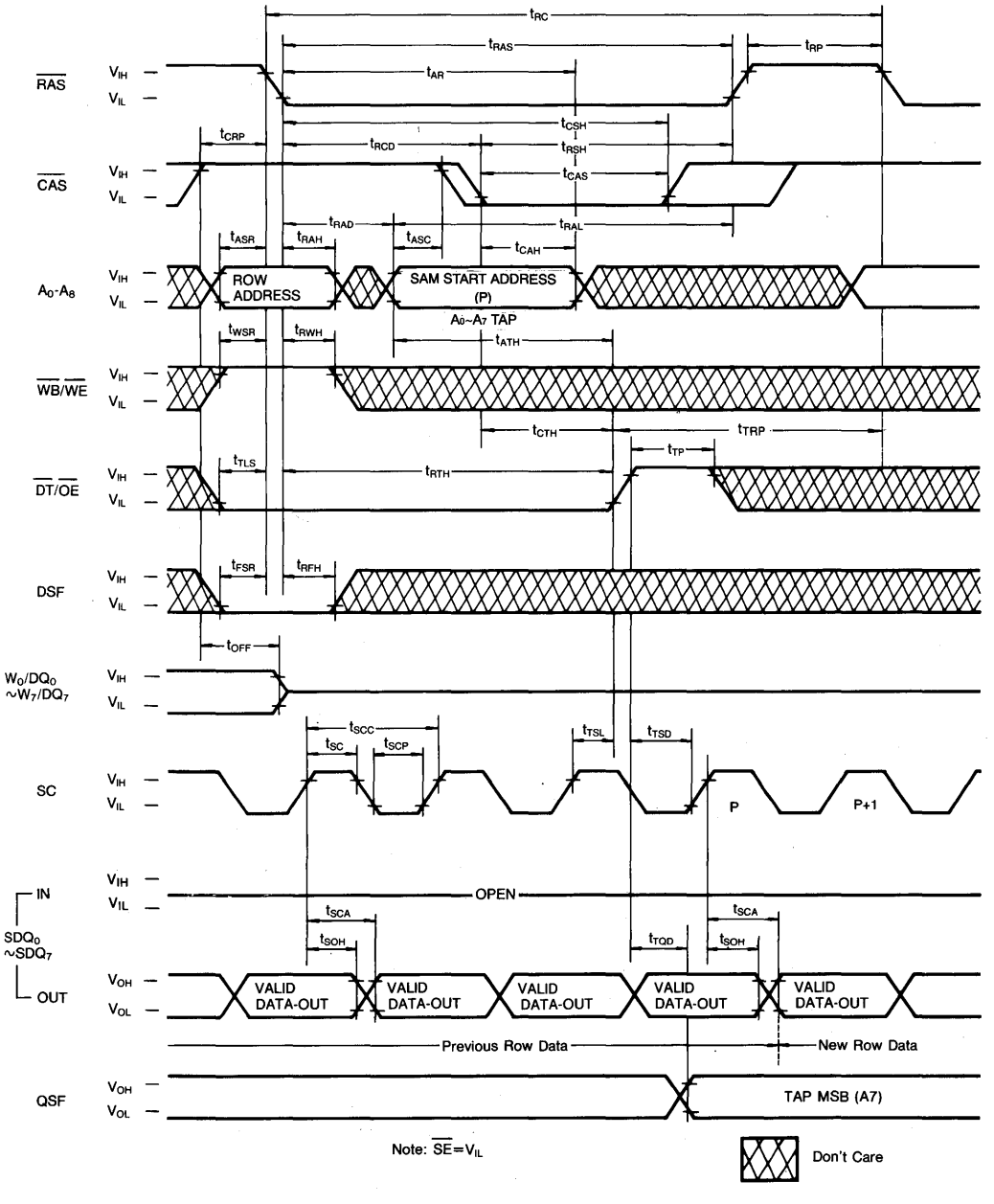
COLUMN SELECT DATA
W_0/DQ_0 - Column 0 (A_{1C}=0, A_{0C}=0)
W_1/DQ_1 - Column 1 (A_{1C}=0, A_{0C}=1)
W_2/DQ_2 - Column 2 (A_{1C}=1, A_{0C}=0)
W_3/DQ_3 - Column 3 (A_{1C}=1, A_{0C}=1)

Wn/DQn
= 0: Disable
= 1: Enable

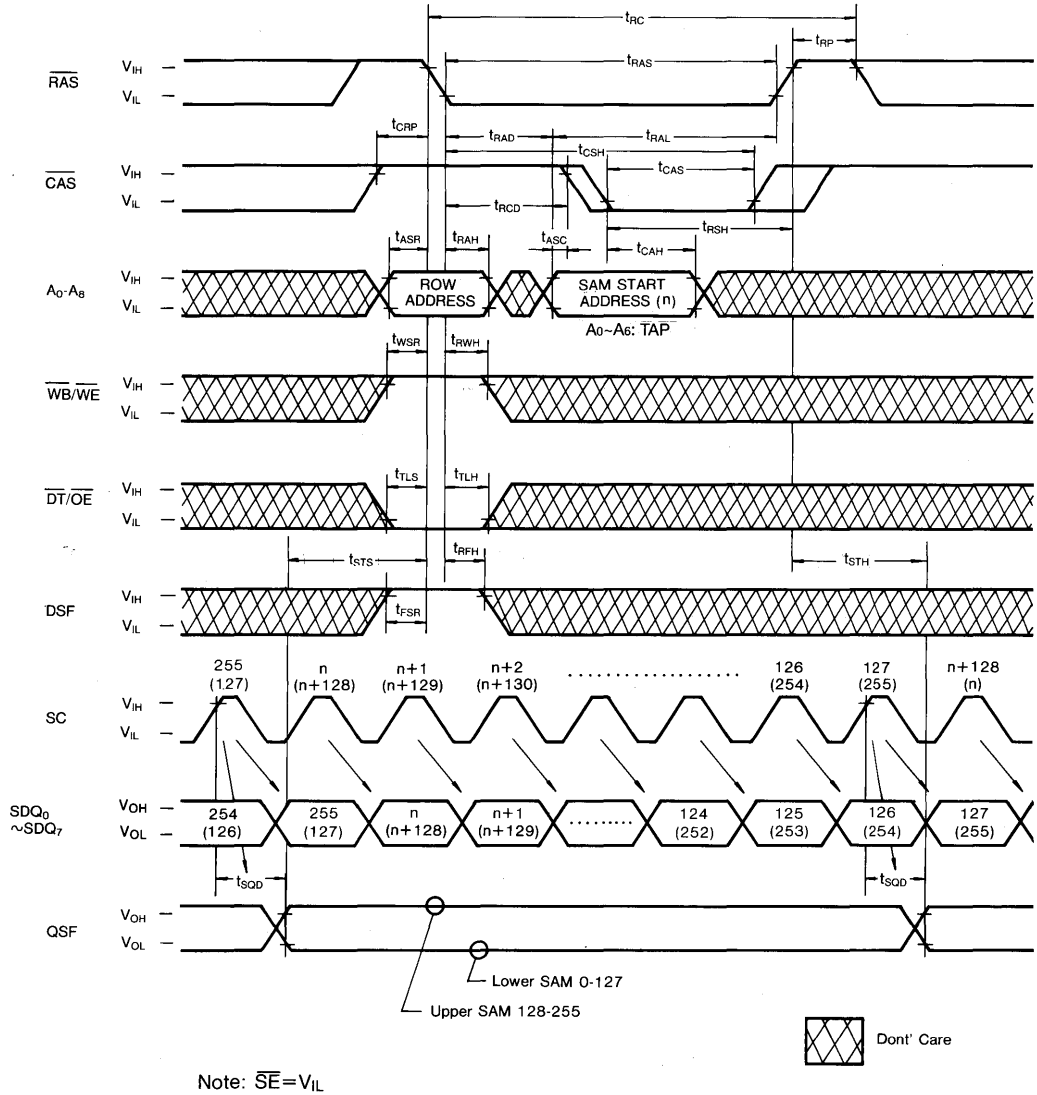
READ TRANSFER CYCLE



REAL TIME READ TRANSFER CYCLE

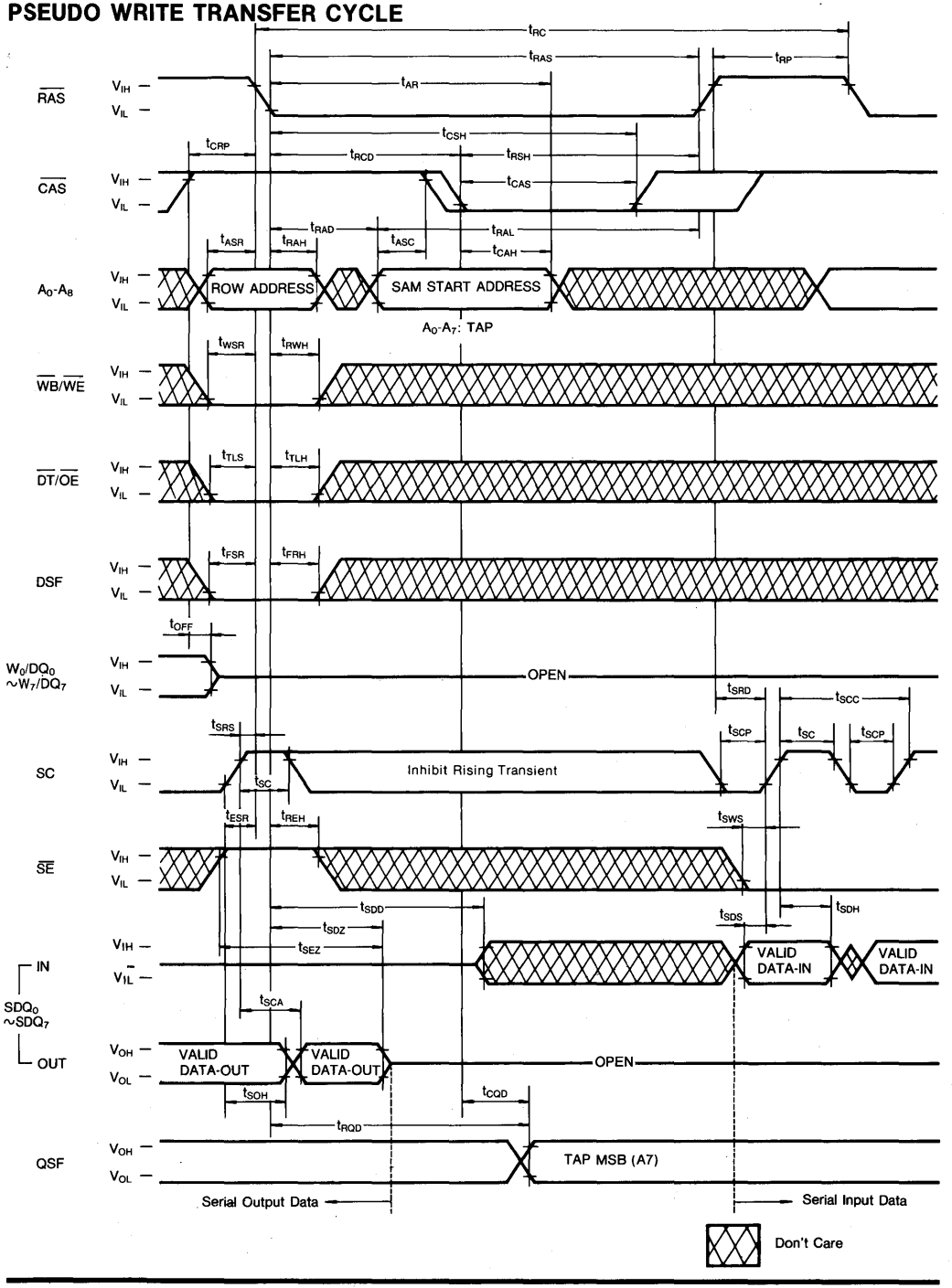


SPLIT READ TRANSFER CYCLE

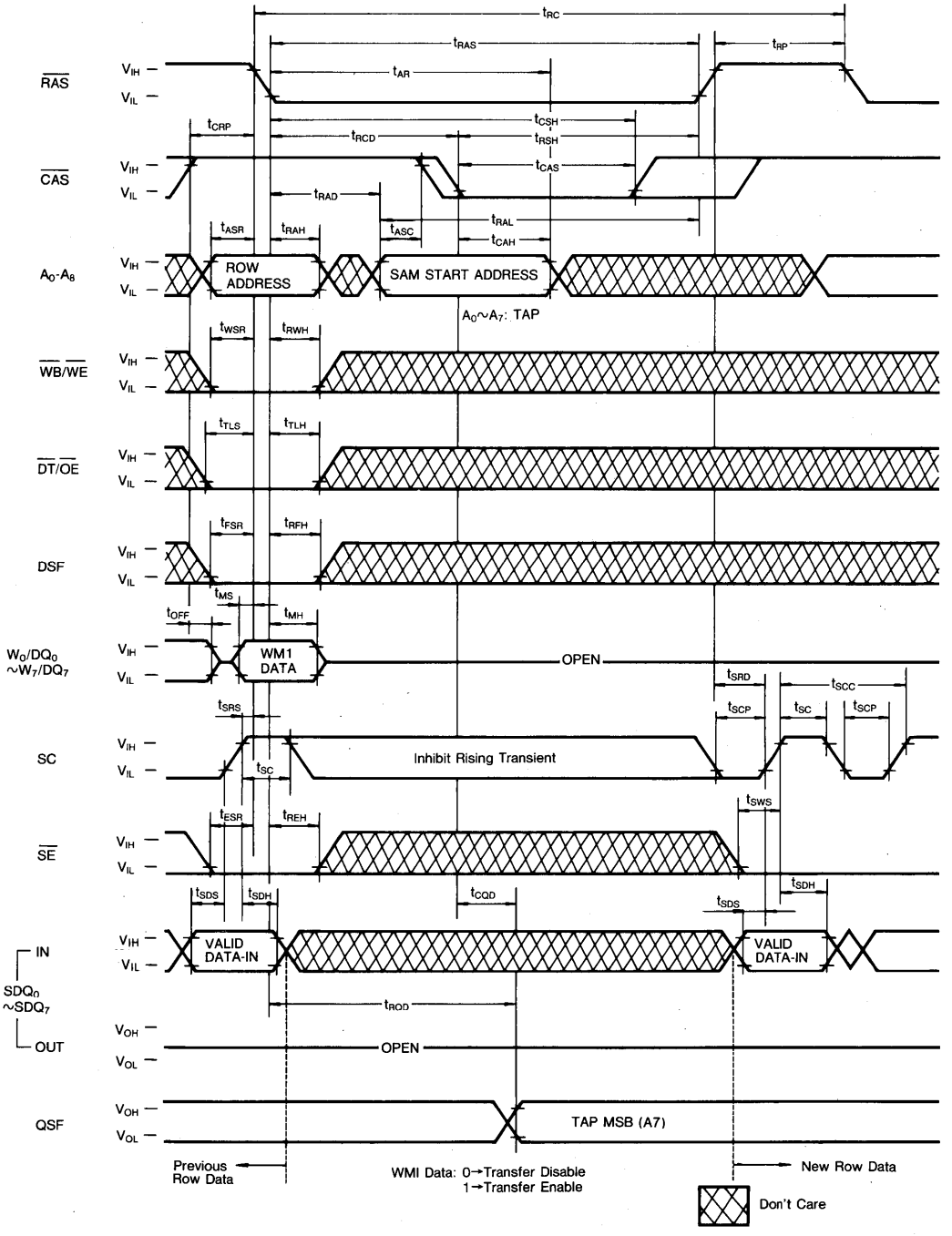


Note: $\overline{SE}=V_{IL}$

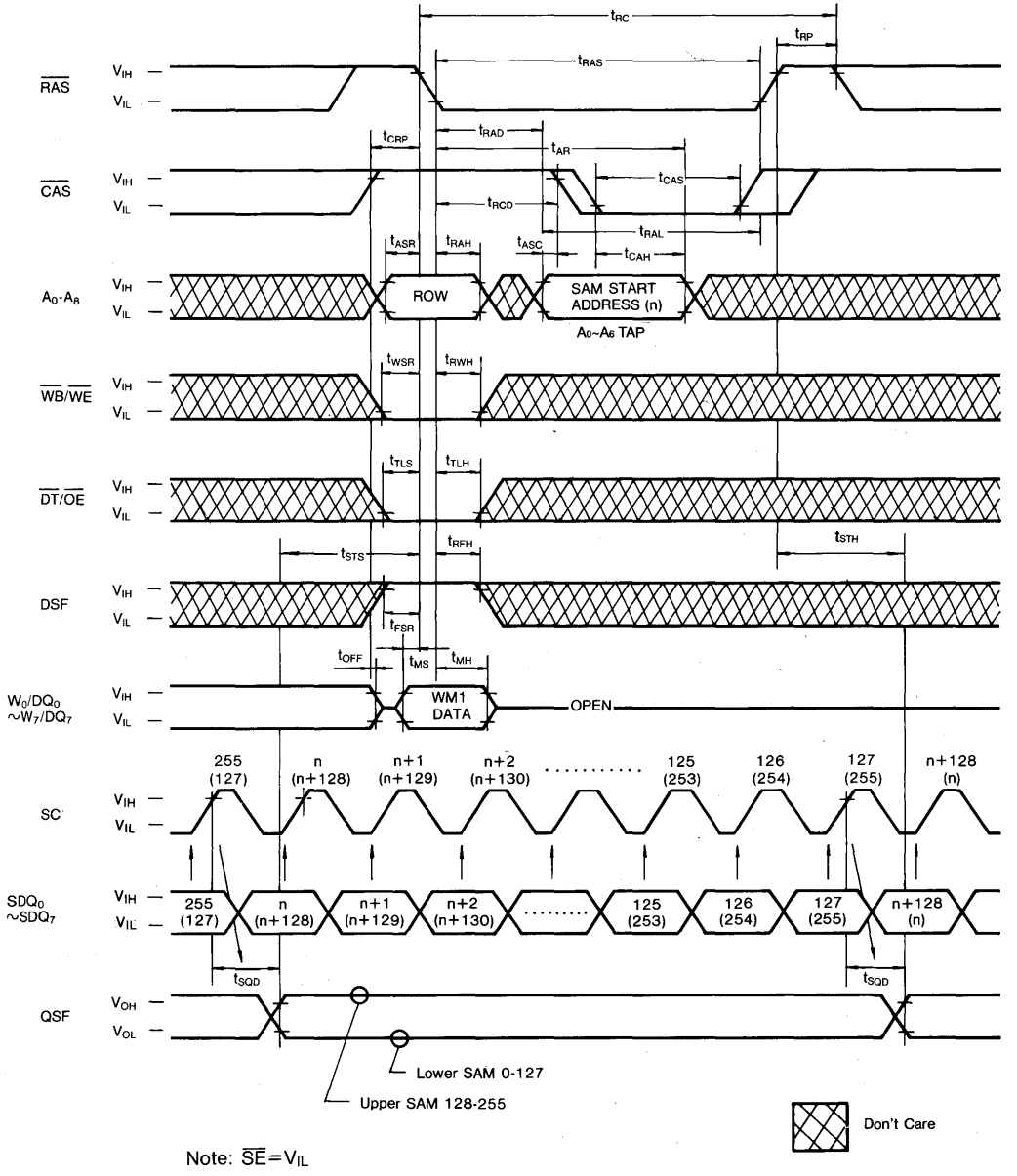
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE

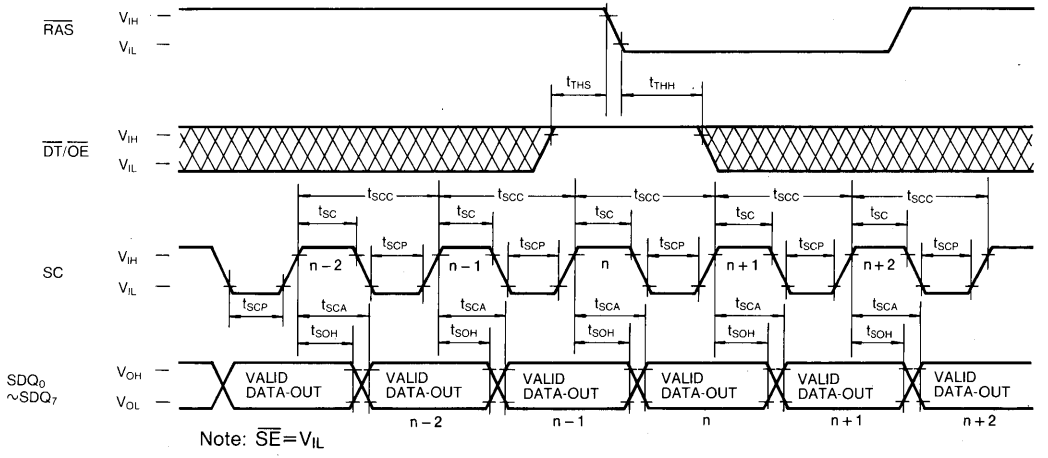


SPLIT WRITE TRANSFER CYCLE



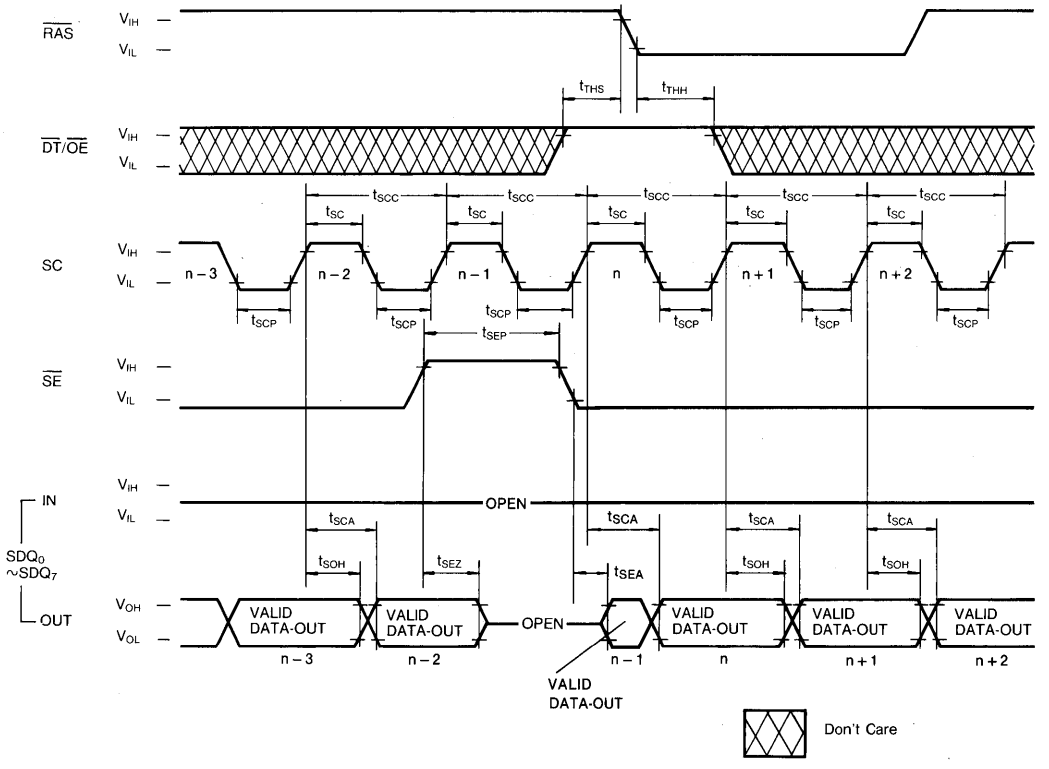
Note: $\overline{SE}=V_{IL}$

SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

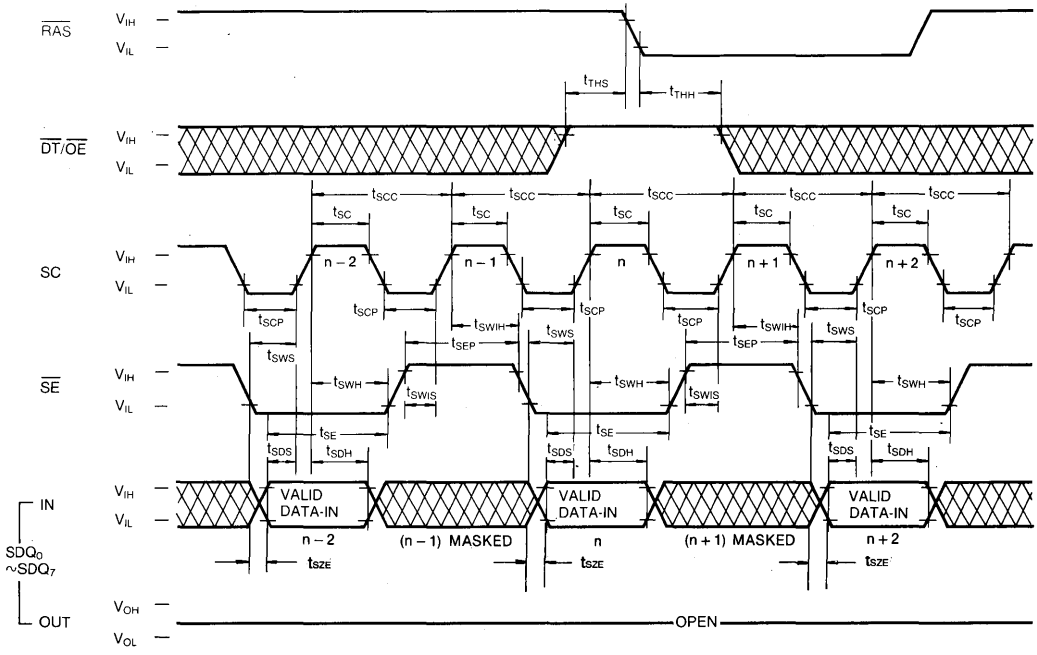


Note: $\overline{SE}$=V_{IL}

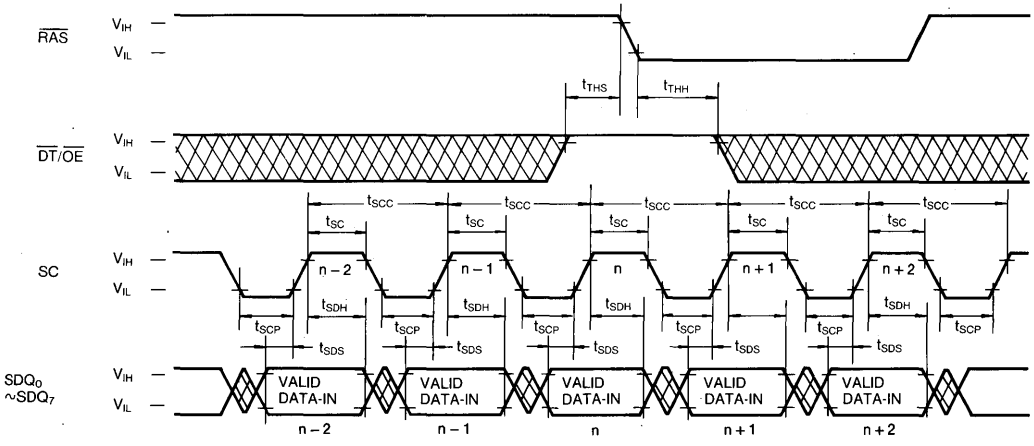
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



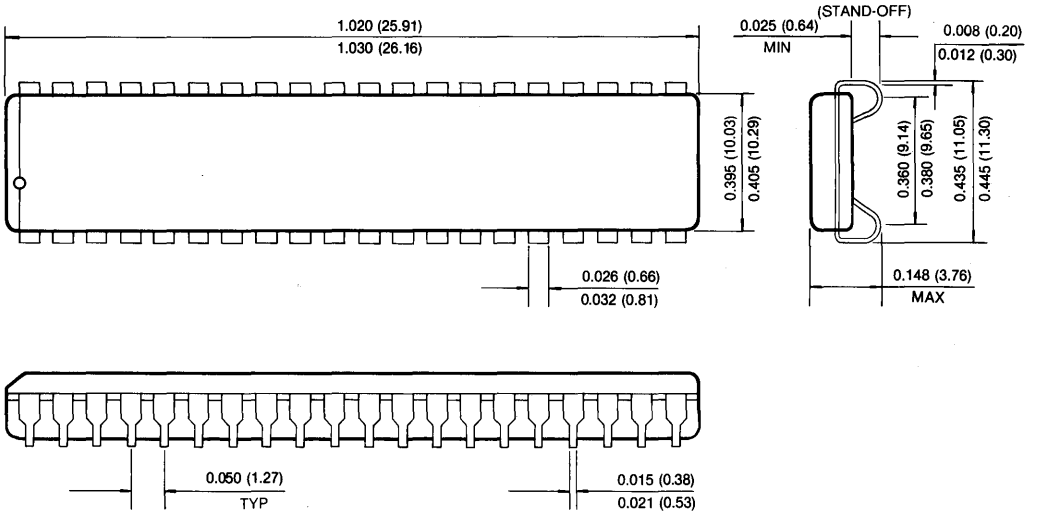
Note: $\overline{SE} = V_{IL}$

Don't Care

PACKAGE DIMENSIONS

40-PIN PLASTIC SOJ

Units Inches (millimeters)



256K X 8 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K x 8 bits RAM port
  512 x 8 bits SAM port
- **Performance range :**

Parameter \ Speed		-6	-7	-8
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page mode cycle (t_{PC})		40ns	45ns	50ns
SAM access time (t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	22ns	25ns
RAM active current	KM428C256	110mA	100mA	90mA
	KM428V256	-	60mA	55mA
SAM active current	KM428C256	55mA	50mA	45mA
	KM428V256	-	30mA	25mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR) and Serial Write (SW)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer (SRT)**
- **Pseudo Write Transfer(PWT)**
- **Write and Split Write Transfer with Masking Operation (New Mask), (WT,SWT)**
- **Block Write (BW) Flash Write (FLW) and Write-per-Bit with Masking Operation (New Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All inputs and Outputs TTL(5.0V) or LVTTL(3.3V) Compatible**
- **Refresh:512 Cycle/8ms**
- **Single +5V±10% Supply Voltage**
- **Single +3.3V±10% Supply Voltage**
- **Low Vcc(3.3V) Part Name: KM428V256**
- **KM428C256: 60, 70, 80ns**
- **KM428V256: 70, 80ns**
- **Plastic 40-Pin 400mil SOJ**
- **Plastic 40/44-Pin 400mil TSOP II (Forward and Reverse Type)**

GENERAL DESCRIPTION

The Samsung KM428C/V256 is a CMOS 256K x 8 bit Dual Port DRAM. It consists of a 256K x 8 dynamic random access memory (RAM) port and 512 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 4096 bits.
It operates like a conventional 256K x 8 CMOS DRAM.
The RAM port has a write per bit mask capability. Data may be written with New Mask. The RAM port has Fast Page mode access, Block Write and Flash Write Capabilities.

The SAM port consists of eight 512 bit high speed shift registers that are connected to the RAM array through a 4096 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read, write Split Transfers or normal Read, Write Transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C/V256 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$ -before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

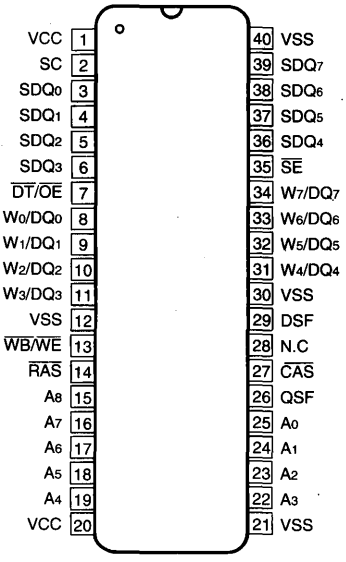
All inputs and I/O's are TTL(5.0V) or LVTTL(3.3V) level compatible. All address lines and data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN DESCRIPTION

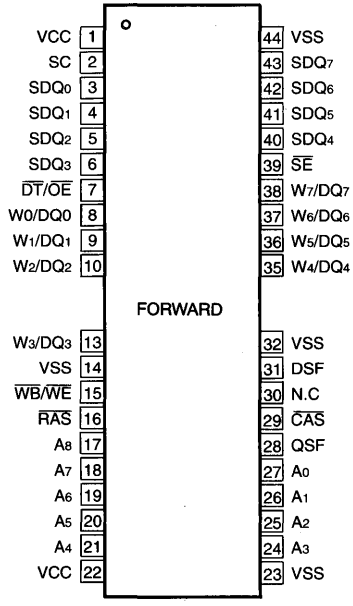
Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ input is a multifunction pin. when $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions(BW, FW, Split Transfer, etc)are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0-255, High if address is 256-511.
$\overline{SE}$	IN	In a serial read cycle. $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
V_{CC}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground

PIN CONFIGURATION (TOP VIEWS)

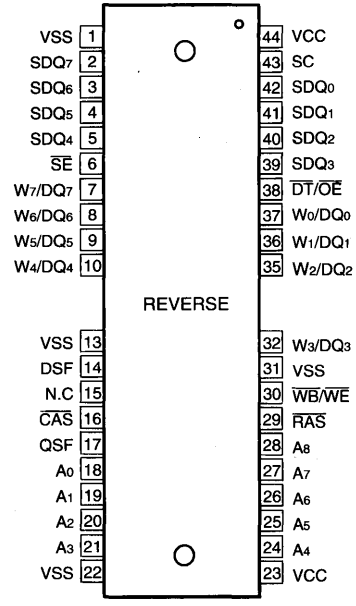
40 Pin 400 mil SOJ



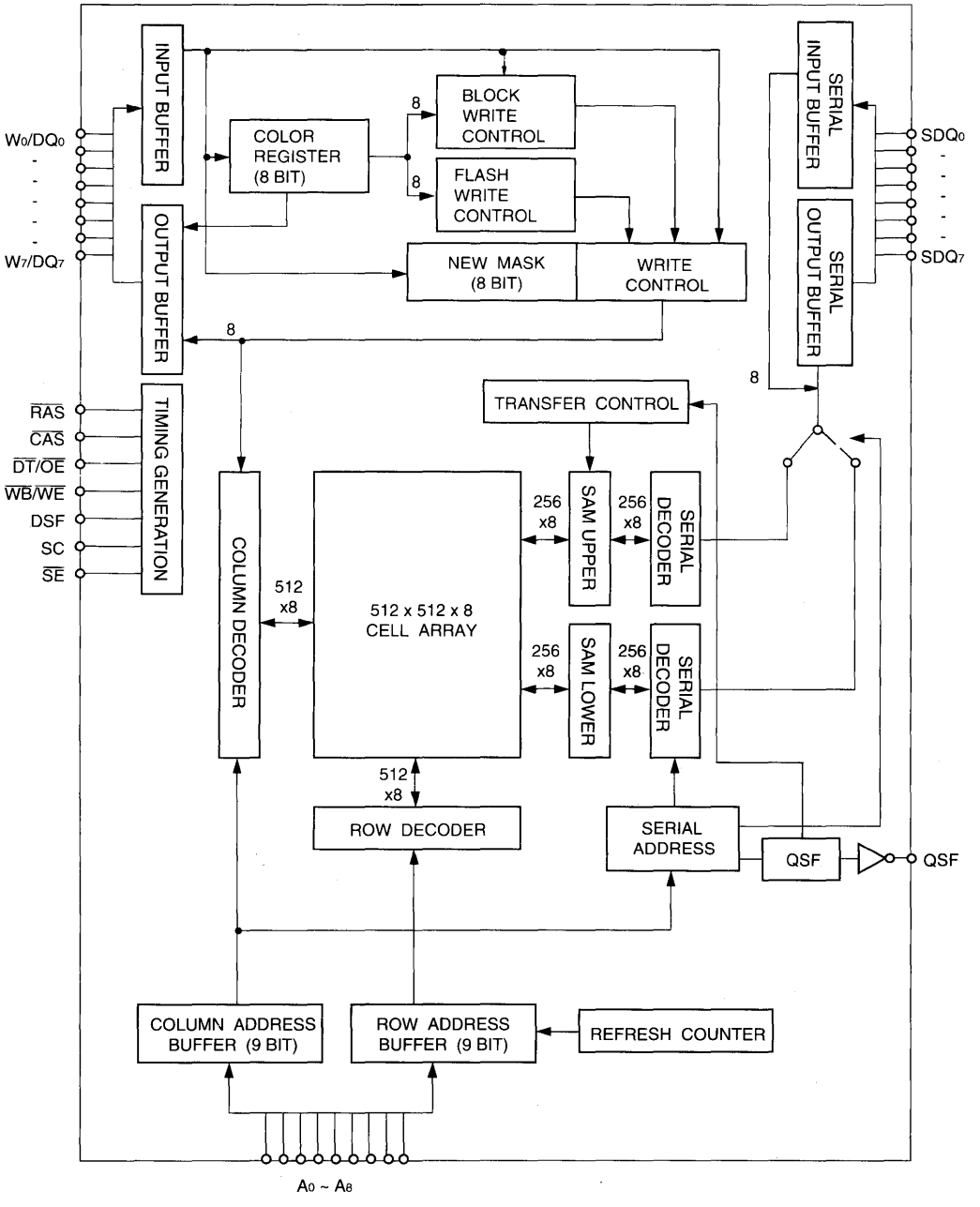
40/44 Pin 400 mil TSOP II



40/44 Pin 400 mil TSOP II



BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS falling edge					CAS	Address*1		DQi Input*2		Write Mask	Color Register	Function
	CAS	DT/OE	WE	DSF	SE	DSF	RAS	CAS	RAS	CAS/WE			
CBR	0	X	X	X	X	-	X	X	X	-	-	-	CBR Refresh
ROR	1	1	X	0	X	-	Row	X	X	-	-	-	RAS- only Refresh
RW	1	1	1	0	X	0	Row	Col.	X	Data	No	-	Normal DRAM Read/ Write (No. Mask)
RWNM	1	1	0	0	X	0	Row	Col.	WMi	Data	Use	-	Masked DRAM Write (New Mask)
MFLW	1	1	0	1	X	X	Row	X	WMi	X	Use	Use	Masked Flash Write (New Mask)
BW	1	1	1	0	X	1	Row	Col. (A2~A8)	X	Col. Mask	No	Use	Block Write (No Mask)
BWNW	1	1	0	0	X	1	Row	Col. (A2~A8)	WMi	Col. Mask	Use	Use	Masked Block Write (New Mask)
LCR	1	1	1	1	X	X	*3 Row	X	X	Color Data	-	Load	Load Color Register
RT	1	0	1	0	X	X	Row	Tap	X	X	-	-	Read Transfer
SRT	1	0	1	1	X	X	Row	Tap	X	X	-	-	Split Read Transfer
PWT	1	0	0	0	1	X	*3 Row	Tap	X	X	-	-	Pseudo Write Transfer
MWT	1	0	0	0	0	X	Row	Tap	WMi	X	Use	-	Masked Write Transfer (New Mask)
MSWT	1	0	0	1	X	X	Row	Tap	WMi	X	Use	-	Masked Split Write Transfer (New Mask)

X : Don't Care, - : Not Applicable , Tap: SAM Start(column)Address

Notes :

*1 : These columns show what must be present on the A_0~A_8 inputs at the falling edge of RAS and CAS.

*2 : These columns show what must be present on the DQ_0~DQ_7 outputs at the falling edge of RAS, CAS or WB/WE, whichever is later.

*3. The Row that is addressed will be refreshed.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM428C256	KM428V256	
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to Vcc + 0.5	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	-0.5 to + 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	-55 to + 150	℃
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70 ℃)

Item	Symbol	KM428C256			KM428V256			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	Vcc	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1V	2.0		Vcc + 0.3	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}+0.5V$*1, all other pins not under test=0 volts, $SE \geq V_{CC}-0.2V$)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$	I_{OL}	-10	10	μA
Output HIgh Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1: 3.6V in KM428V256

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25℃)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF
Output Capacitance (QSF)	C_{QSF}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM428C256			KM428V256		Unit
			-6	-7	-8	-7	-8	
Operating Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC1}	110	100	90	60	55	mA
	Active	I_{CC1A}	155	140	125	85	75	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$=VIH,DSF=VIL)	Standby	I_{CC2}	10	10	10	5	5	mA
	Active	I_{CC2A}	55	50	45	30	25	mA
$\overline{RAS}$ Only Refresh Current*1 ($\overline{CAS}$=VIH, $\overline{RAS}$ Cycling @tRC=min.)	Standby	I_{CC3}	100	90	80	55	50	mA
	Active	I_{CC3A}	145	130	115	80	70	mA
Fast Page Mode Current*1 ($\overline{RAS}$=VIL, $\overline{CAS}$ Cycling @tPC=min.)	Standby	I_{CC4}	80	75	70	45	40	mA
	Active	I_{CC4A}	125	115	105	70	65	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC5}	90	85	80	50	45	mA
	Active	I_{CC5A}	135	125	115	75	70	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC6}	140	125	110	75	70	mA
	Active	I_{CC6A}	185	165	145	100	90	mA
Flash Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC7}	90	85	80	50	45	mA
	Active	I_{CC7A}	135	125	115	75	70	mA
Block Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC8}	110	105	100	65	60	mA
	Active	I_{CC8A}	155	145	135	90	80	mA
Color Register Load or Read Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC9}	90	85	80	50	45	mA
	Active	I_{CC9A}	135	125	115	75	70	mA

Note *1 : Real values dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as average current. In Icc1, Icc3, Icc6, Icc7, Icc8, Icc9 address transition should be changed only once while $\overline{RAS}$=VIL. In Icc4 address transition should be changed only once while $\overline{CAS}$=VIH

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM428C256: $V_{CC}=5.0V \pm 10\%$, KM428V256: $V_{CC}=3.3V \pm 10\%$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		200		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,6
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width(fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time(fast page mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay(Fast Page mode)	t_{CPWD}	60		65		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from output enable	t_{OEA}		15		20		20	ns	
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	7
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period(512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF hold time(at $\overline{CAS}$ Low)referenced to $\overline{RAS}$	t_{FHR}	45		55		60		ns	
DSF set-up time referenced to $\overline{RAS}$	t_{FSR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	t_{RFH}	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	15		15		15		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ high set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{SE}$ setup referenced to $\overline{RAS}$	t_{ESR}	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	10		10		15		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	t_{TRP}	40		50		60		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		20		ns	

AC CHARACTERISTICS (Continued)

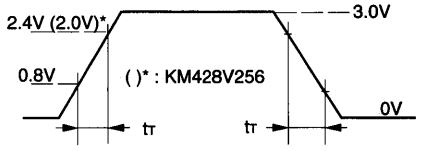
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to first SC delay(read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	t_{CSD}	25		30		35		ns	
Col. Addr.to first SC delay(read transfer)	t_{ASD}	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	t_{TSD}	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	t_{SRS}	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	t_{SRD}	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	t_{SDD}	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SDZ}	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	18		22		25		ns	15
SC pulse width(SC high time)	t_{SC}	6		7		7		ns	
SC precharge(SC low time)	t_{SCP}	6		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	10		15		15		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	0		0		0		ns	
Serial write enable hold time	t_{SWH}	10		15		15		ns	
Serial write disable set-up time	t_{SWIS}	0		0		0		ns	
Serial write disable hold time	t_{SWIH}	10		15		15		ns	
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	
SC-QSF delay time	t_{SQD}		20		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		20		25		25	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		60		70		80	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		20		35		40	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), and t_{SDZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. The t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below.

SAM PORT	INPUT MODE
QSF	Hi-Z
Color Register	Don't Care
Tap Pointer	Invalid
W_i/DQ_i	Hi-Z
SAM Port	Input Mode
SDQ_i	Hi-Z

13. Recommended operating input condition:



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=3.0ns.
14. Assume t_T=3ns.
15. t_{DHR}, t_{WCR} are referenced to t_{RAD}(max).

DEVICE OPERATION

The KM428C/V256 contains 2,097,152 memory locations. Eighteen address bits are required to address a particular 8-bit word in the memory array. Since the KM428C/V256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM428C/V256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This is the beginning of any KM428C/V256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C/V256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB/WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access time is specified by t_{CAC} or t_{AA}.

The KM428C/V256 has common data I/O pins. The $\overline{DT/OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT/OE}$ must be low for the period of time defined by t_{OEA}.

RAM Write

The KM428C/V256 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB/WE}$, $\overline{DT/OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{WB/WE}$.

New Mask Write Per Bit

The New Mask Write cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB/WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_7/DQ_7 pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the data bit remains unchanged. When the mask data is high, data is written into the RAM. The mask data is valid for only one cycle, defined by an active $\overline{RAS}$ period. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB/WE}$ low before $\overline{CAS}$ falling and Late Write cycle is achieved by $\overline{WB/WE}$ high at the falling edge of $\overline{CAS}$. During the Early or Late Write cycle, input data through W_0/DQ_0~W_7/DQ_7 must meet the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB/WE}$. When $\overline{WB/WE}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	Wi/DQi	FUNCTION
↓	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	INHIBIT WRITE

DEVICE OPERATION (Continued)

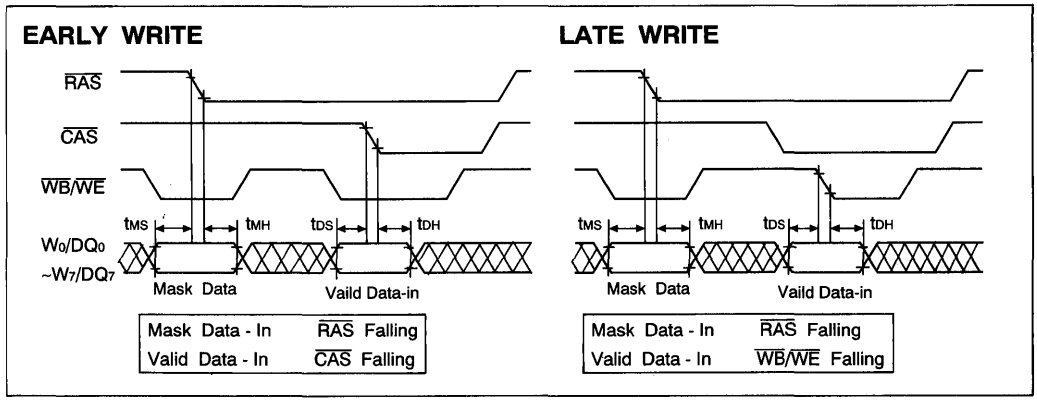


Figure 1. New Mask Write Cycle Example 1. (Early Write & Late Write)

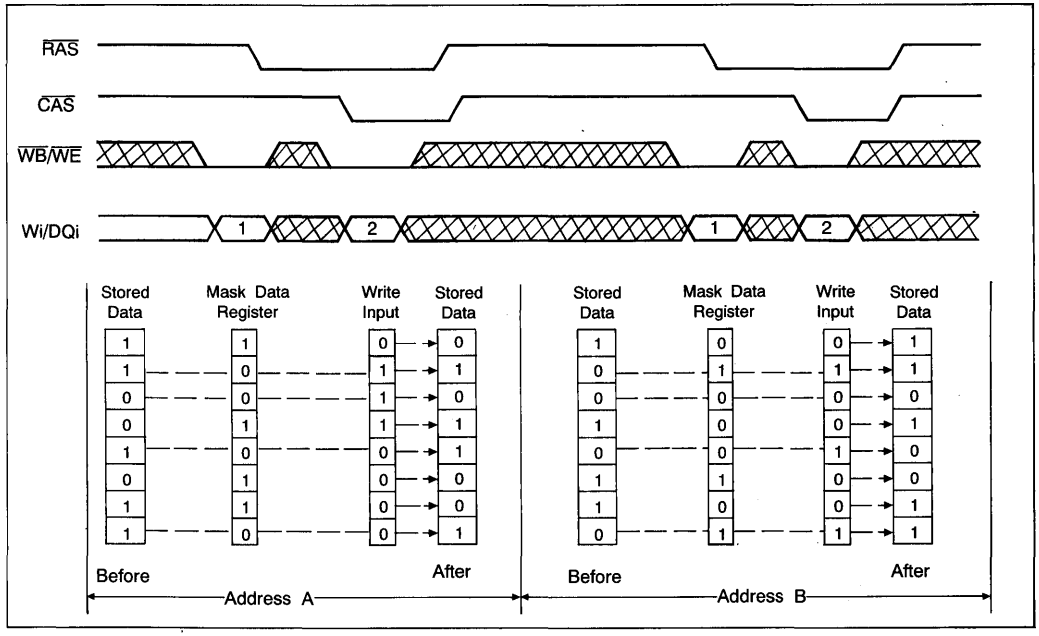


Figure 2. New Mask Write Cycle Example 2.

Fast Page Mode

Fast page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. In this cycle, read, write, read-modify write, and Block Write cycles can be mixed.

In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. Masking data stored at the $\overline{RAS}$ falling edge of the first Fast page write cycle remains valid for subsequent Fast page write cycles.

DEVICE OPERATION (Continued)

Load Color Register(LCR)

A Load Color Register cycle is performed by keeping DSF high on the falling edges of $\overline{RAS}$. Color data id loaded on the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$ (delayed write) via the W_0/DQ_0~W_7/DQ_7 pins. this data is used in Block Write and Flash Write cycles and remains unchanged until the next Load Color Register cycle.

Block Write

In a Block Write cycle four adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 8-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into four adjacent locations of the same row of each corresponding bit plane(8). This results in a total of 32-bits being written in a single Block Write cycle compared to 8-bits in a normal Write cycle.

The Block Write cycle is performed if DSF is low on the falling edge of $\overline{RAS}$ and high on the falling edge of $\overline{CAS}$.

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.

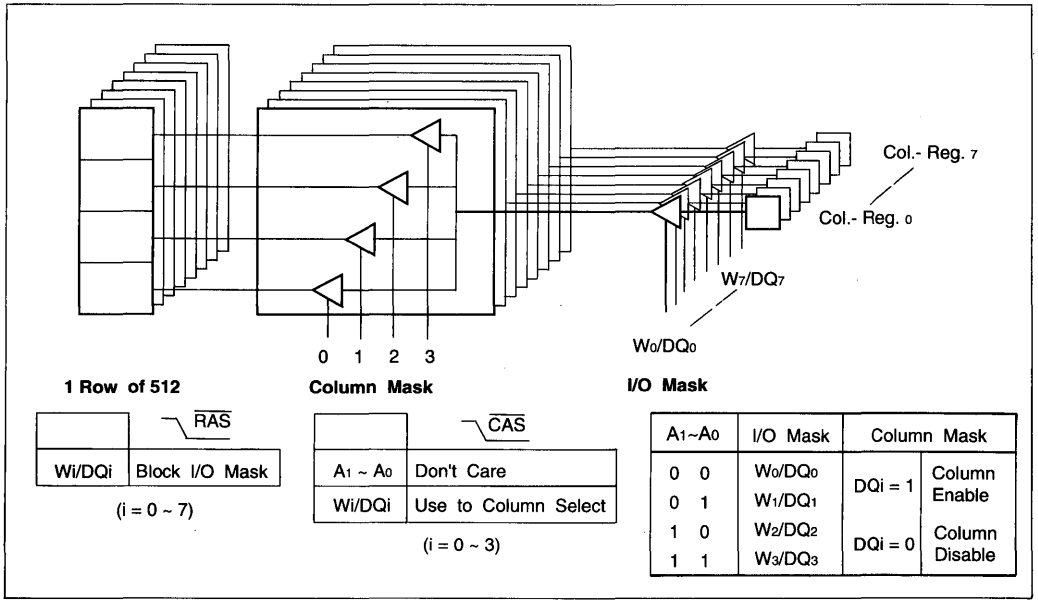
Since four bits are being written at a time, when the minimum increment required for the column address is four. Therefore, when the column address is latched on the falling edge of $\overline{CAS}$, the 2LSBs, A_0 and A_1 are ignored and only bits(A_2~A_8) are used to define the location of the first bit out of the four to be written.

Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_3/DQ_3 pins provideds column mask data. That is, for each of the four bits in all 8-bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0 = 1 and W_1/DQ_1 = 0, than the Color Register contents will be written into the first bit out of the four, but the second remains unchanged. Fig. 3 shows the correspondence of each data line to the column mask bits.

Masked Block Write(BWNM)

A Masked Block Write cycle is identical to a New Mask Write-per-bit cycle except that each of the 8-bit planes being masked is operating on 4 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high on the falling edge of $\overline{CAS}$. Mask data is latched into the device via the W_0/DQ_0~W_7/DQ_7 pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle.



	RAS
Wi/DQi	Block I/O Mask

(i = 0 ~ 7)

	CAS
A_1 ~ A_0	Don't Care
Wi/DQi	Use to Column Select

(i = 0 ~ 3)

A_1~A_0	I/O Mask	Column Mask	
0 0	W_0/DQ_0	DQi = 1	Column Enable
0 1	W_1/DQ_1		
1 0	W_2/DQ_2	DQi = 0	Column Disable
1 1	W_3/DQ_3		

Figure 3. Block Write Scheme

DEVICE OPERATION (Continued)

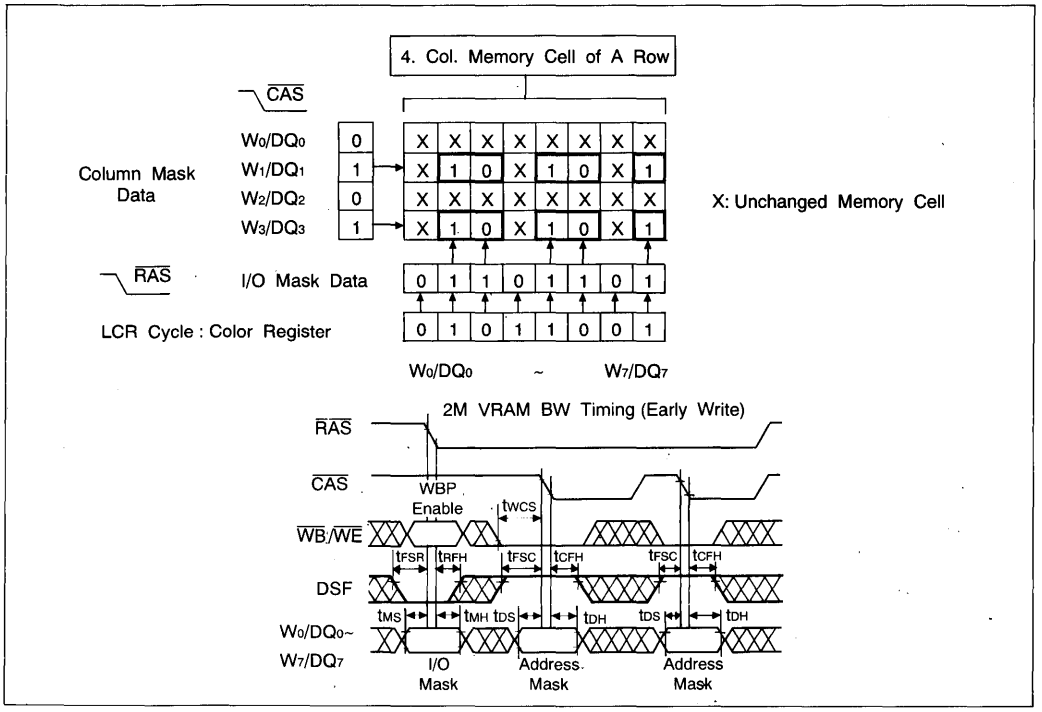


Figure 4. Block Write Example and Timing

Flash Write

The Flash Write cycle is a way of writing each bit of the Color Register into the whole row(512 columns) simultaneously. This function is used for fast screen clear or background color change. 512 columns in each bit plane are written, for a total of 4096 bits(512×8 bit planes) in one cycle. While this cycle writes significantly more data than the Block Write cycle, it is also less selective.

If $\overline{WB}/\overline{WE}$ is low and DSF is high on the falling edge of $\overline{RAS}$, a Flash Write cycle is performed. Also on this edge, the data present on the Wi/DQi pins is used as mask data and needs to be provided for every Flash Write cycle. A Load Color Register cycle must have been performed before initiating a Flash Write cycle.

Data Output

The KM428C/V256 has three state output buffers controlled by $\overline{DT}/\overline{OE}$, $\overline{CAS}$ and $\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ are high, the output state is in high impedance(High-z). In any cycle, the output goes low impedance state from the first $\overline{CAS}$ falling edge.

Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh).

Each of the KM428C/V256 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Refresh

The data in the KM428C/V256 is stored as a charge on a tiny capacitor within each memory cell. Due to leakage the data may be lost over a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 4096 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses (A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM428C/V256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM428C/V256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM428C/V256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

Transfer operation is initiated when $\overline{DT}/\overline{OE}$ is low at the falling edge of $\overline{RAS}$. The state of $\overline{WB}/\overline{WE}$ when $\overline{RAS}$ goes low indicates the direction of transfer (to or from DRAM) and DSF pin is used to designate the proper transfer mode like normal and Split Transfer. Each of the transfer cycle is described in the truth table of transfer operation.(Table2.)

Read Transfer(RT)

The Read Transfer operation is set if $\overline{DT}/\overline{OE}$ is low, $\overline{WB}/\overline{WE}$ is high, and DSF is low when $\overline{RAS}$ goes low. The row address bits in the read transfer cycle indicate which eight 512bit DRAM Row portions are transferred to the eight SAM data registers. The column address bits indicate the start address of the SAM registers when SAM data read operation is performed. If MSB bit of column address is low during Read transfer operation, the QSF state will be set low and this indicates the start address of the SAM register is present at the lower half of the SAM port.(If A_8 is high, QSF will be high meaning that the start address is in the upper half). Read Transfer may be achieved in two ways. If the transfer is to be synchronized with the SC, both SAM Read and Read transfer operation is possible simultaneously. The completion of transfer operation is determined by the timing relationship of first SC rising, $\overline{RAS}/\overline{CAS}$ falling edge and $\overline{DT}/\overline{OE}$ rising edge of transfer cycle. This is usually called "Real Time Read Transfer". The completion of Real time Read transfer is accomplished at the rising edge of $\overline{DT}/\overline{OE}$. Note that the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with the rising edge of SC to retain the continuity of serial read data output.

Table 2. Truth Table for Transfer Operation

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$				
H	L	H	L	*	Read Transfer	RAM → SAM	512×8	Input → Output
H	L	L	L	L	Masked Write Transfer	SAM → RAM	512×8	Output → Input
H	L	L	L	H	Pseudo Write Transfer	—	—	Output → Input
H	L	H	H	*	Split Read Transfer	RAM → SAM	256×8	Not Changed
H	L	L	H	*	Masked Split Write Transfer	SAM → RAM	256×8	Not Changed

DEVICE OPERATION (Continued)

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(512bit) to be transferred to the selected row in the DRAM array. Masking is selected by latching Wi/DQi(i=0~7)inputs when $\overline{RAS}$ goes low.

The column address defines the start address of serial input and its MSB(A_8)defines QSF level.

If A_8 is low, the QSF will be low level to designate that the start address is in positioned in the lower half of SAM. (For A_8=high, the QSF will be high and indicates that the start address will be positioned in the upper half of SAM) After write transfer cycle is completed, SAM port is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT}/\overline{OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. column address pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data(0=Lower, 1=Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary(e.g. 255th or 511th bit).

Example of SRT applications are shown in Fig. 5 through Fig.9.

The normal usage of Split Read Transfer cycle is described in Fig 5. When Read Transfer is executed, data from X1 row address is fully transferred to the SAM port and Serial Read is started from 0(Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255 SC. Note that in this case "0+256" Tap address instead of "0" is loaded.

The another example of SRT cycle is described in Fig. 6. When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 7 and 8 are the example of abnormal SRT cycle. If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig. 7, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 8. indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511. In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that the SRT limitation period during QSF transition designated as "Not Allowed Period" in which SRT is prohibit as shown in Fig. 9 due to uncertaining of which half SAM the data is transferred. This is also true in Masked Split Write Transfer.

A Split Read Transfer does not change the direction of the SAM I/O port.

Masked Split Write Transfer(MSWT)

This transfer function is very similiar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "don't care". The example of MSWT is described in Fig.10. The opening cycle of either MWT or PWT is needed before MSWT can be performed.

A pseudo write transfer Cycle(PWT)

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A pseudo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, DSF low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a serial write cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$.

DEVICE OPERATION (Continued)

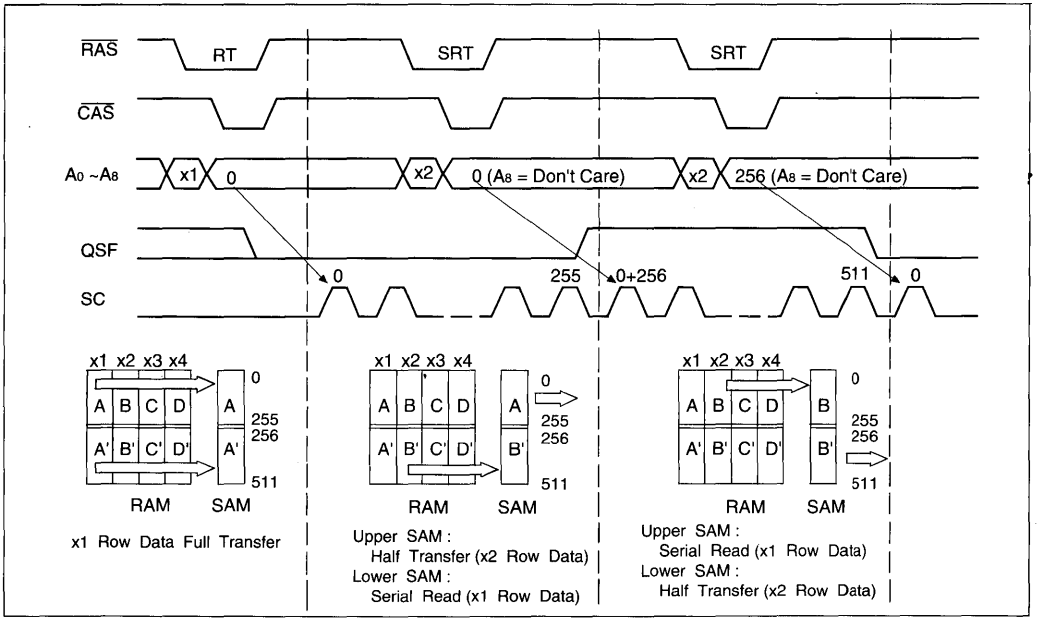


Figure 5. Split Read Transfer Normal Usage

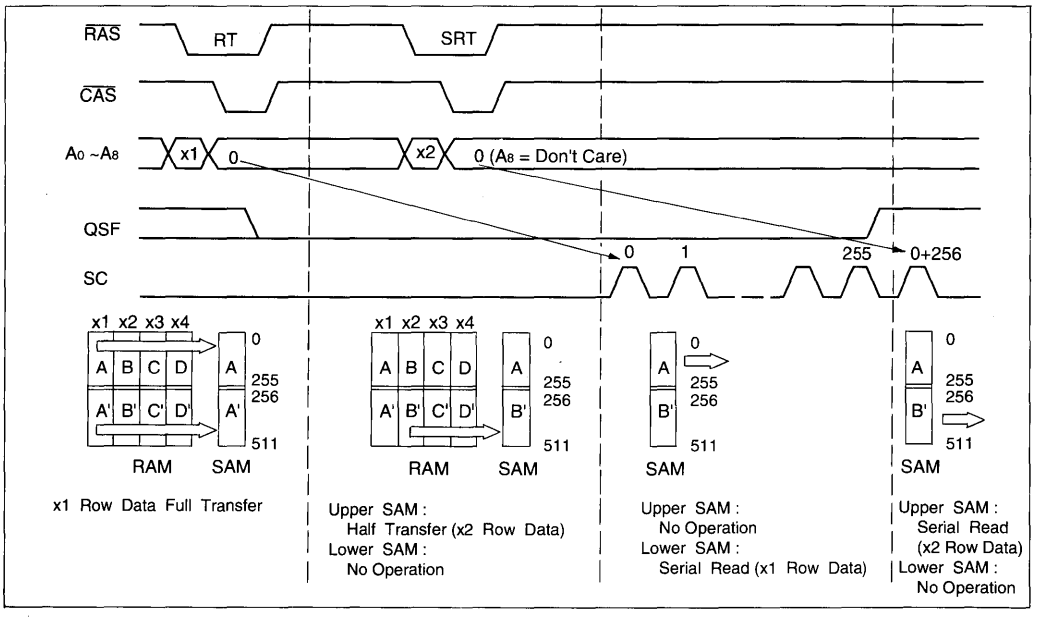


Figure 6. Split Read Transfer Normal Usage

DEVICE OPERATION (Continued)

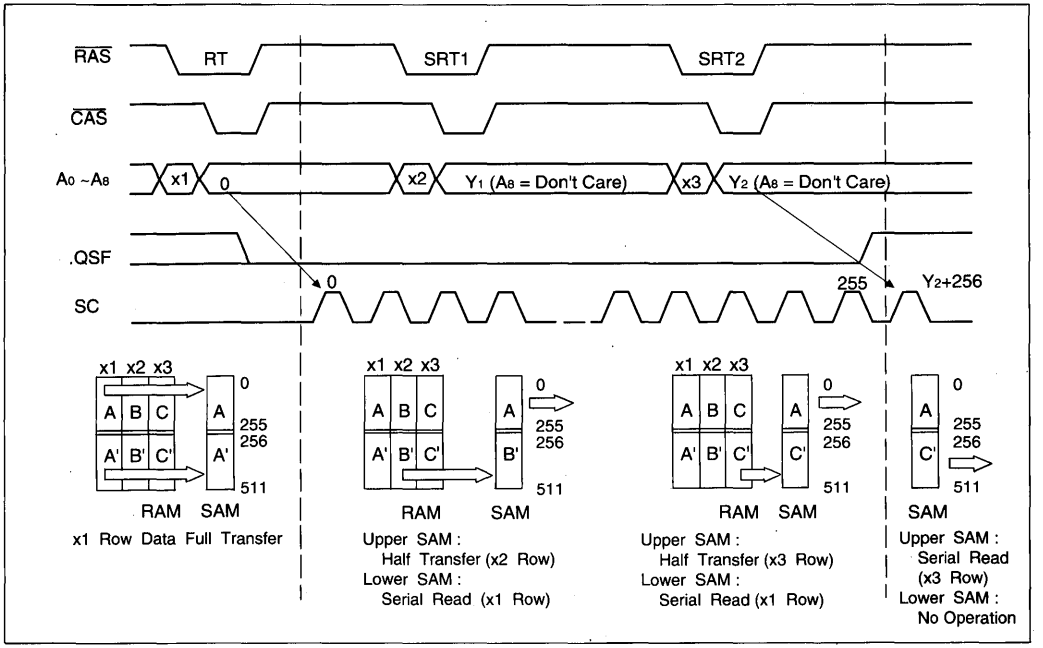


Figure 7. Split Read Transfer Abnormal Usage (Case 1)

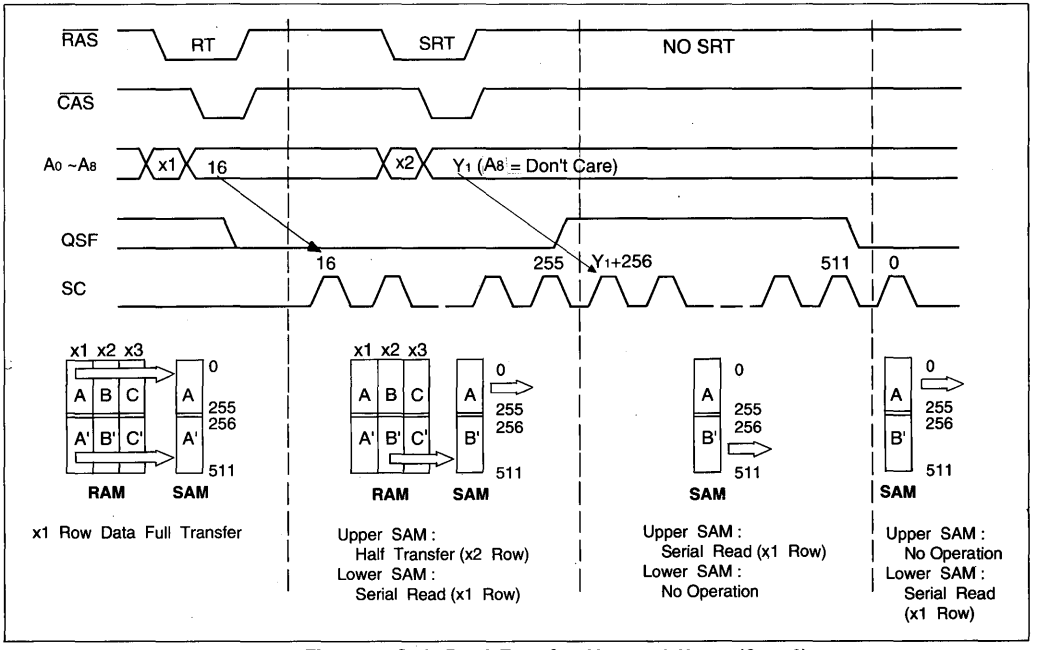


Figure 8. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATION (Continued)

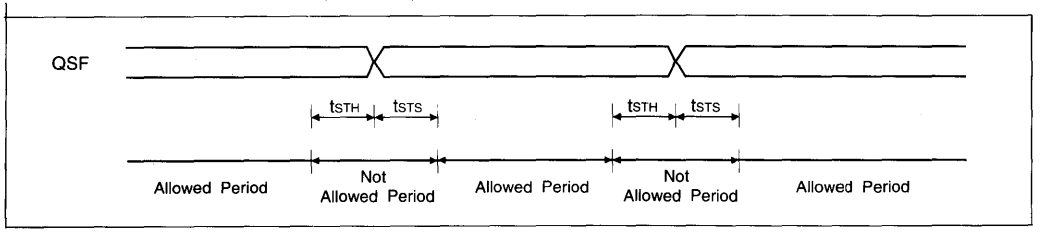


Figure 9. Split Transfer Cycle Limitation Period

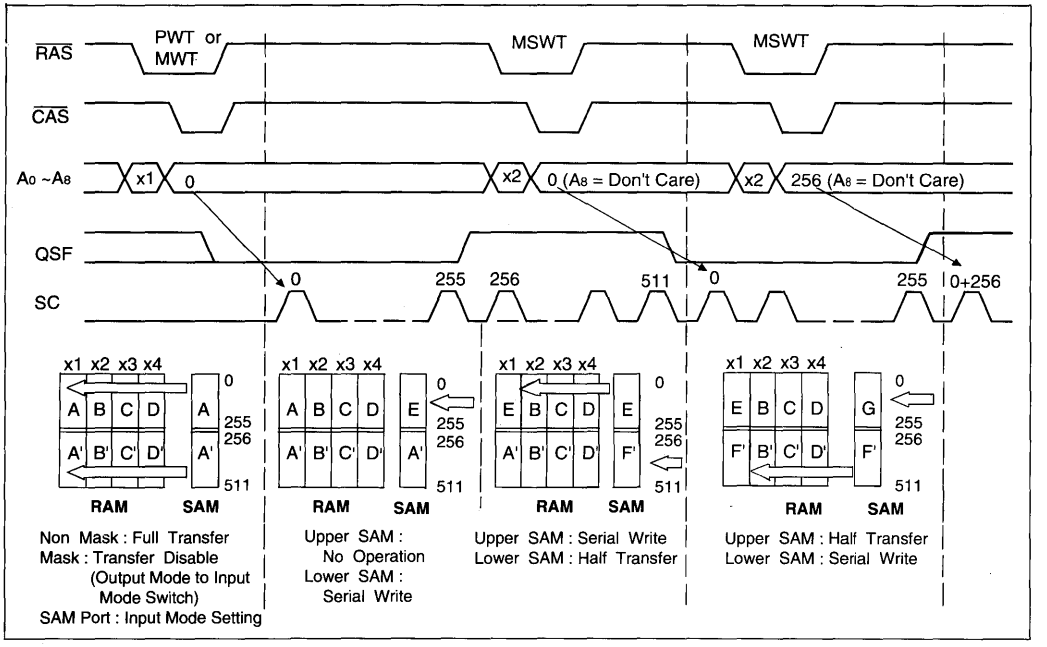
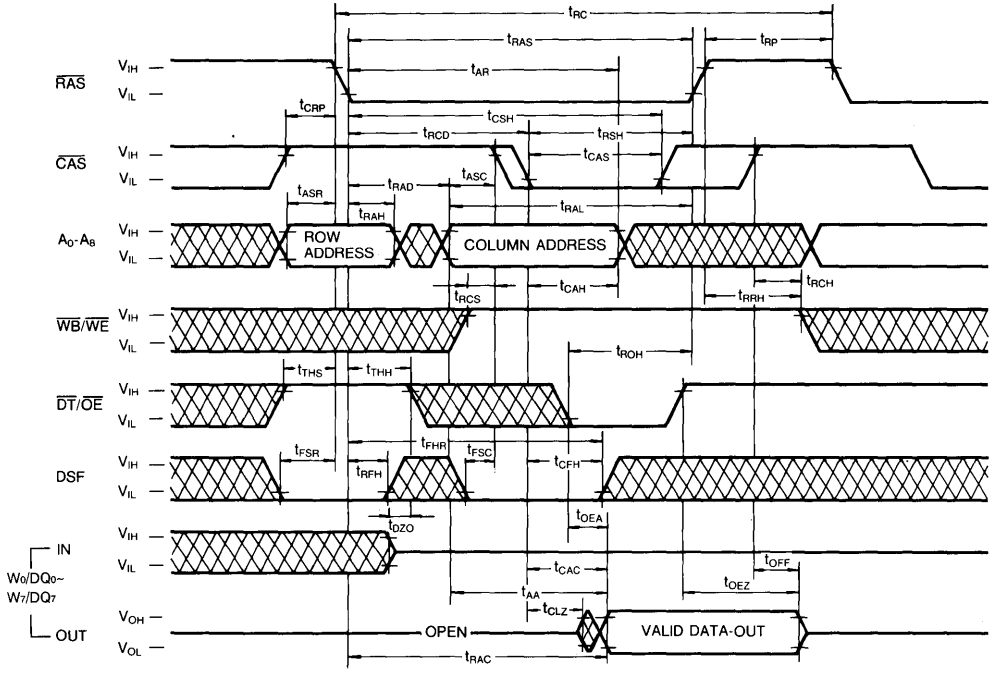


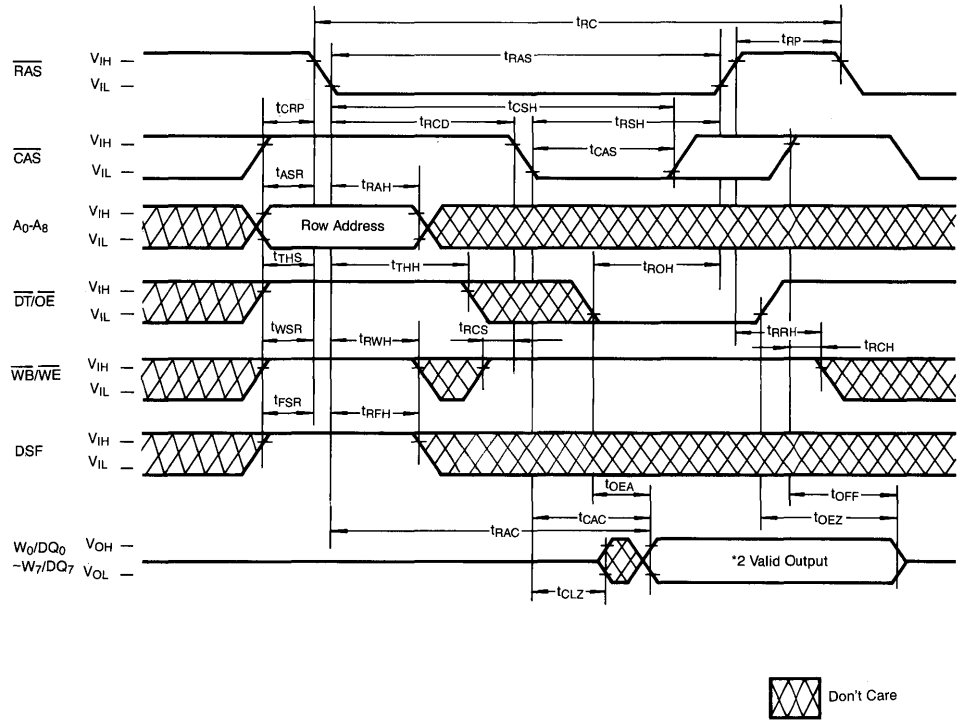
Figure 10. Masked Split Write Transfer Normal Usage

TIMING DIAGRAMS

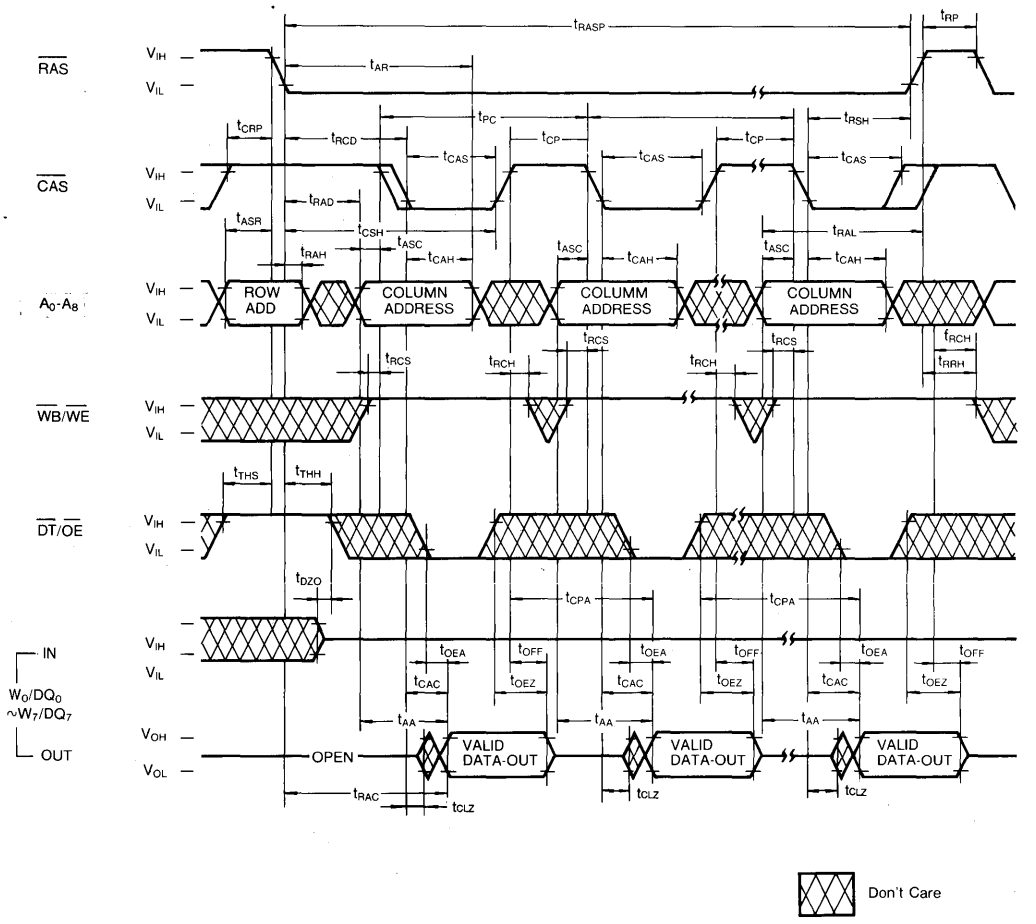
READ CYCLE



READ COLOR REGISTER CYCLE



FAST PAGE MODE READ CYCLE



TRUTH TABLE FOR WRITE CYCLE[1]

Function	RAS			CAS[2][3] or WB/WE (Early Write)(Late Write)	
	*1 WB/WE	*2 DSF	*3 Wi/DQi (New Mask)	*4 DSF	*5 Wi/DQi
Normal Write	1	0	X	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)[3]	1	0	X	1	Column Mask
Masked Block Write[3]	0	0	Write Mask	1	Column Mask
Masked Flash Write	0	1	Write Mask	X	X
Load Color Register	1	1	X	X	Color Data

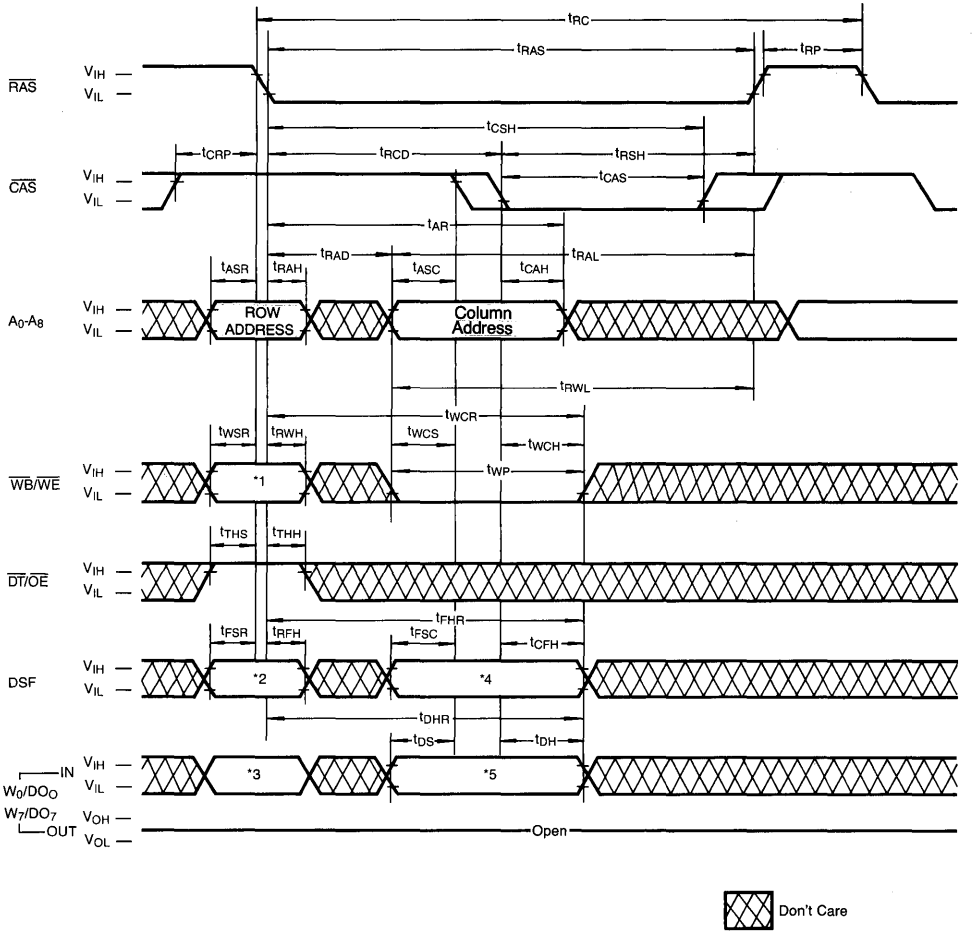
*NOTE: (1) Reference truth table to determine the input signal states of *1, *2, *3, *4 and *5 for the Write cycle timing diagram

(2) On the masked flash write cycle, all the signal inputs are don't care condition except $\overline{RAS}$ at the falling edge of $\overline{CAS}$.
On the Block Write cycle, Column Mask is latched only at the falling edge of $\overline{CAS}$ and $\overline{WB}/\overline{WE}$ is "Don't Care" at the falling edge of $\overline{CAS}$.
Lately Block Write and Read Modify Block Write are not allowed.

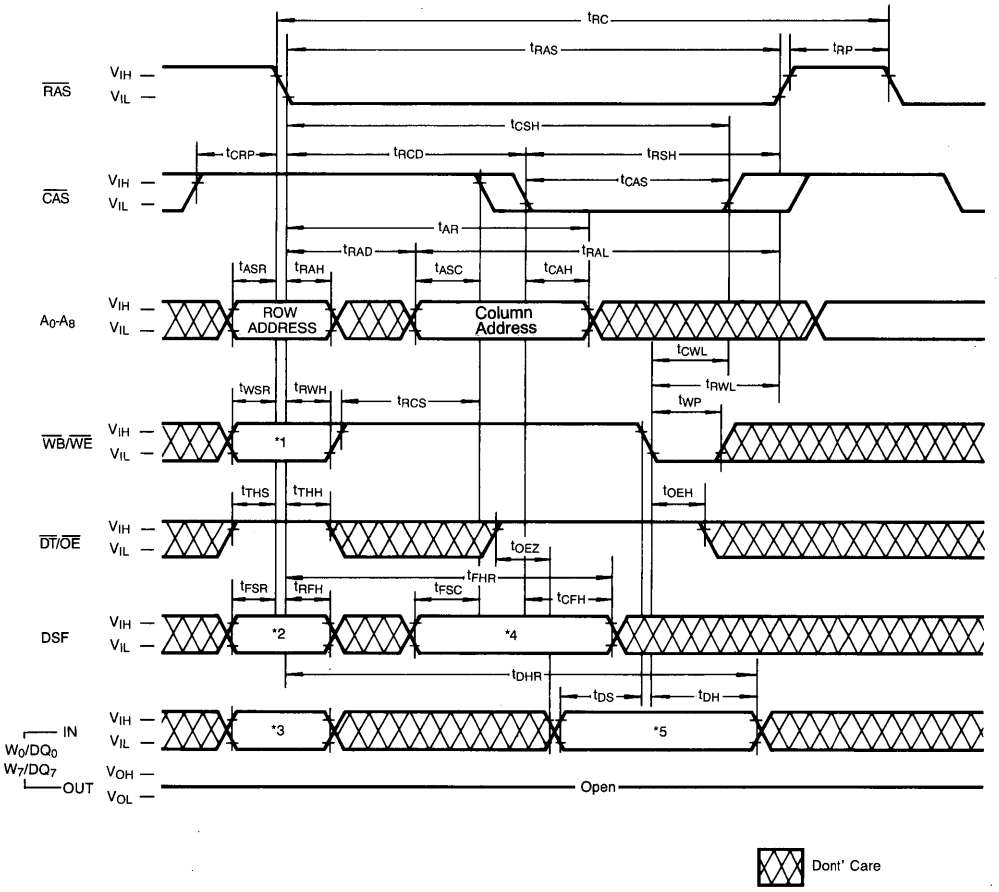
(3) Function Table for Block Write Column Address A_0., A_1 are "Don't Care" during Block Write.

Column Address		*5	If	
A_1	A_0	Wi/DQi	Wi/DQi=0	Wi/DQi=1
0	0	W_0/DQ_0	No Change the Internal Data	Color Register Data Are Written to The Corresponding Column Address Location
0	1	W_1/DQ_1		
1	0	W_2/DQ_2		
1	1	W_3/DQ_3		

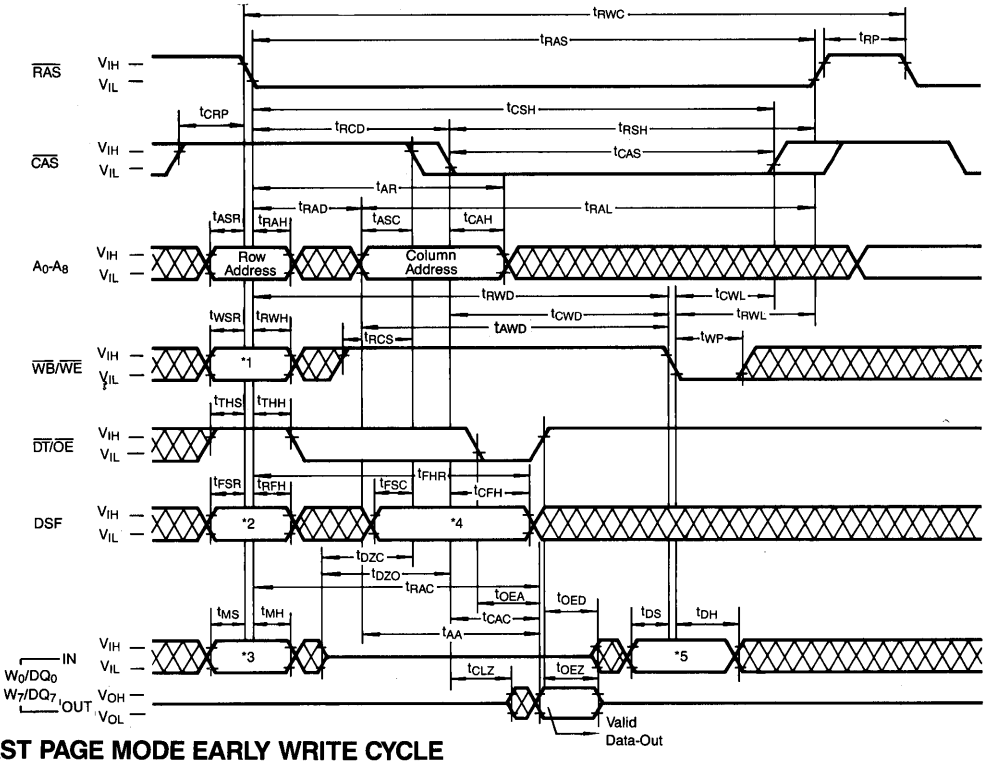
EARLY WRITE CYCLE



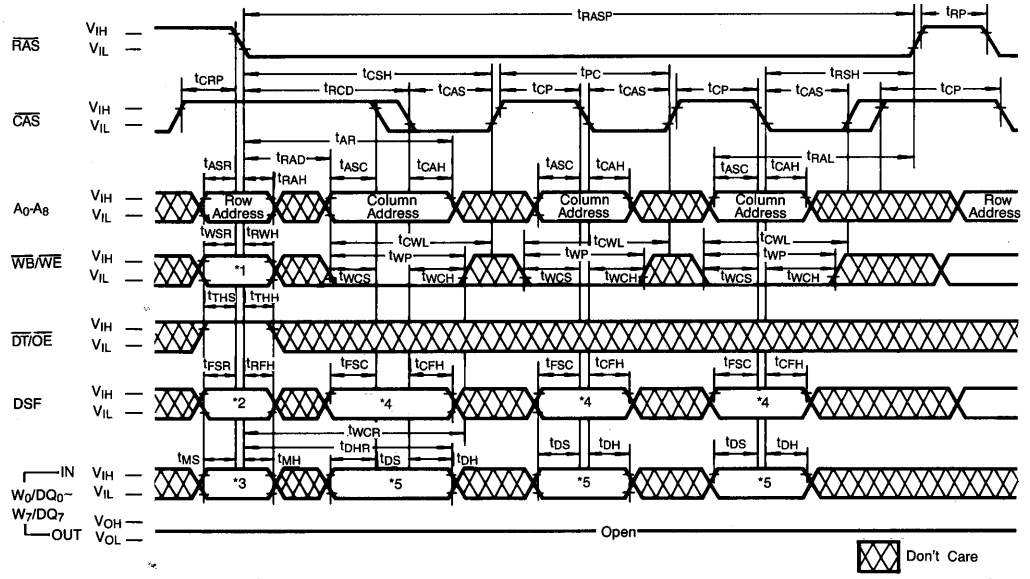
LATE WRITE CYCLE



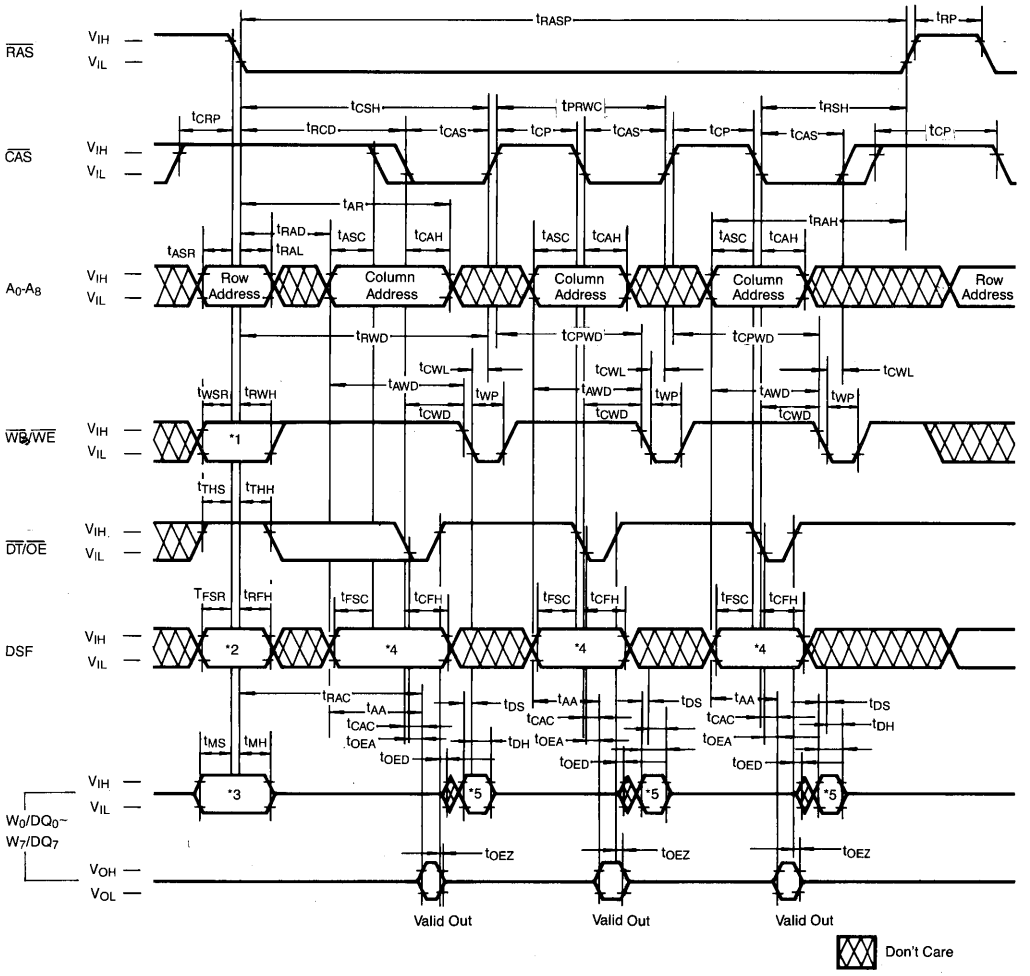
READ-WRITE/READ-MODIFY-WRITE CYCLE



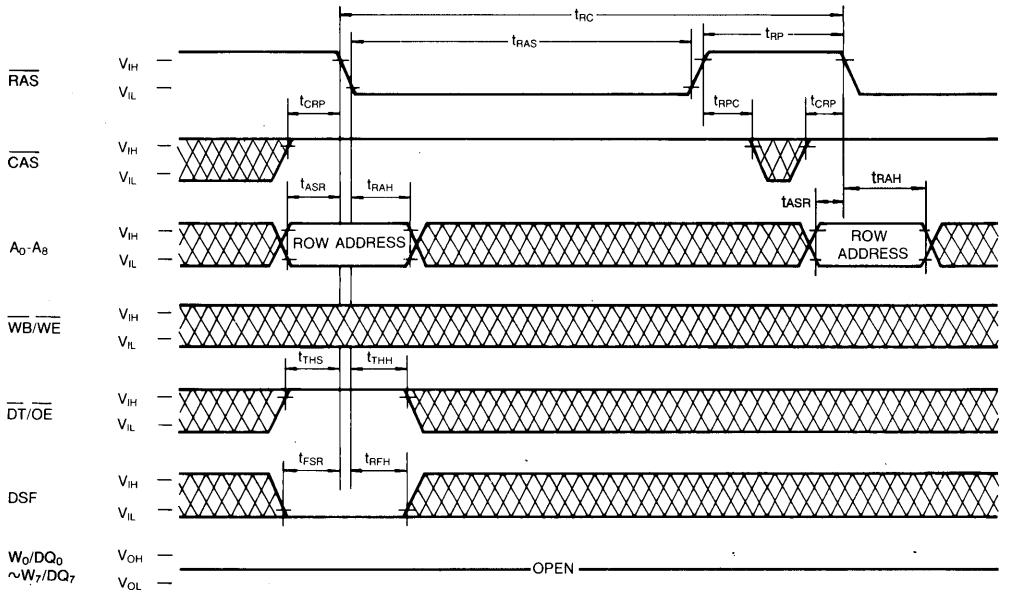
FAST PAGE MODE EARLY WRITE CYCLE



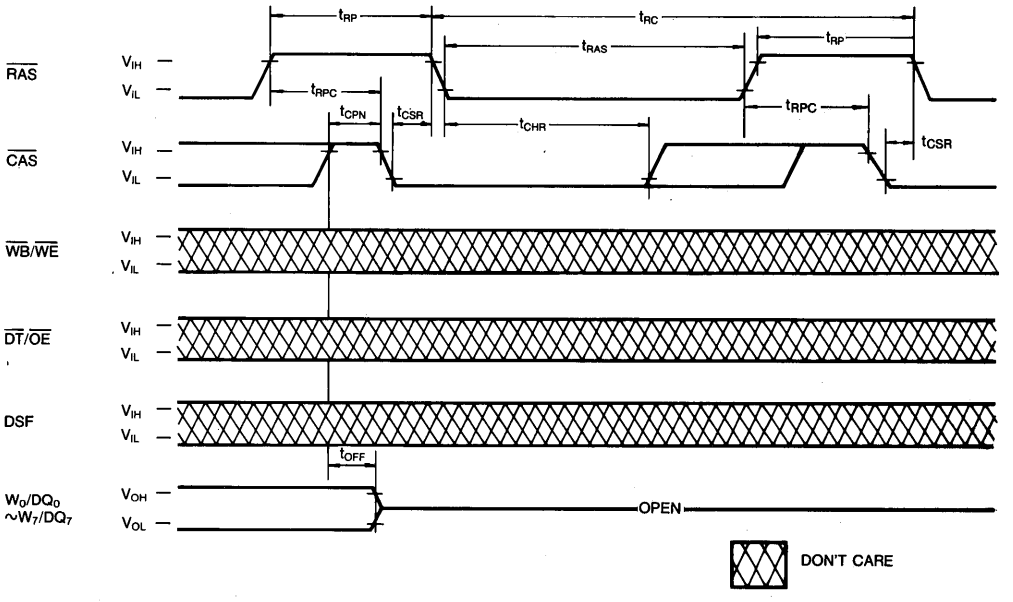
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



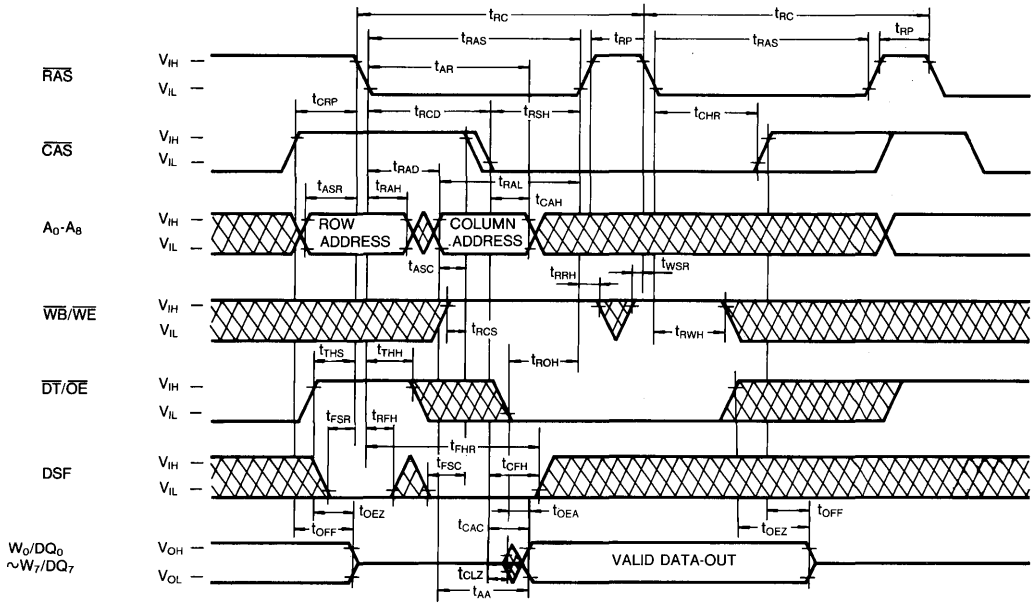
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

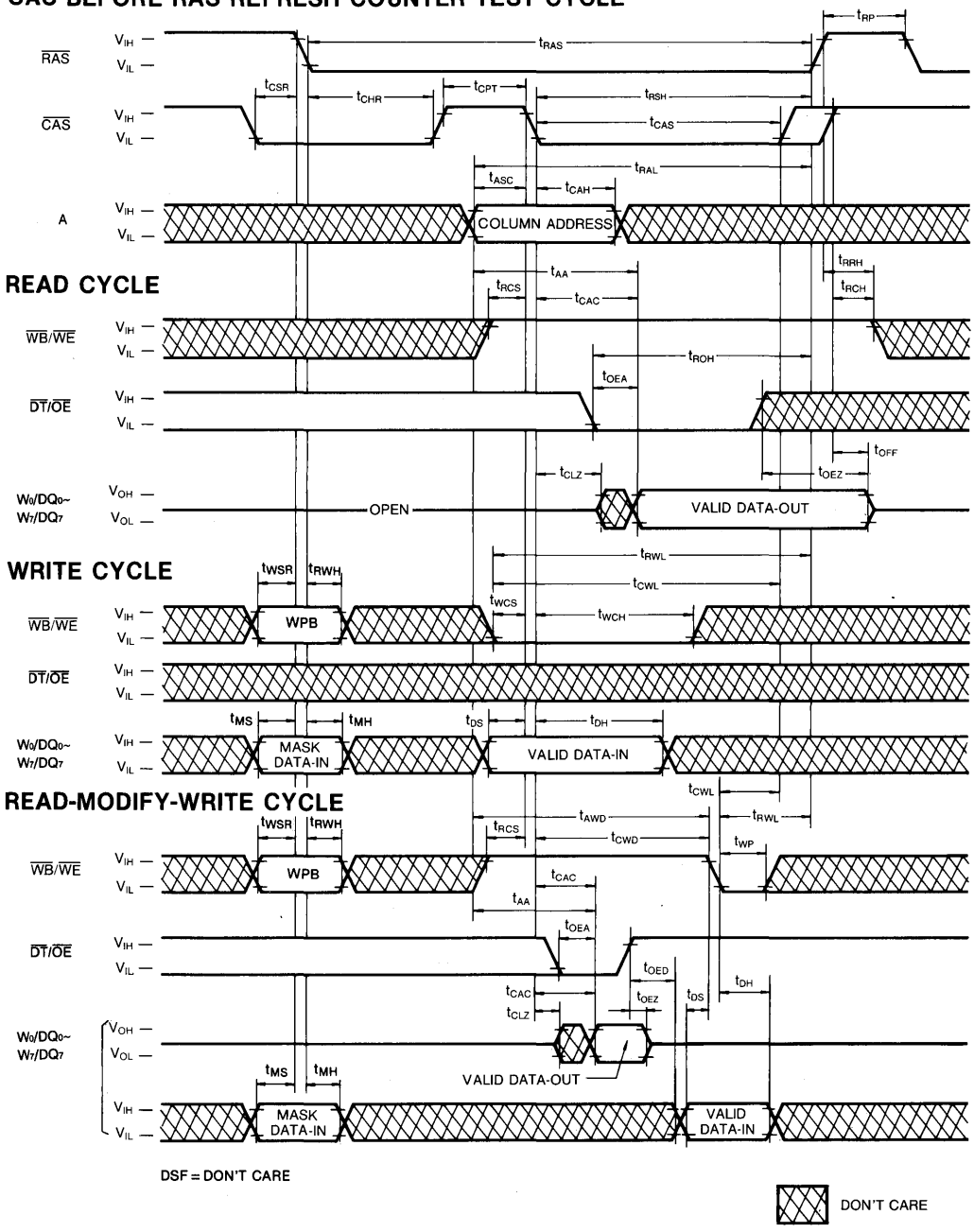


HIDDEN REFRESH CYCLE

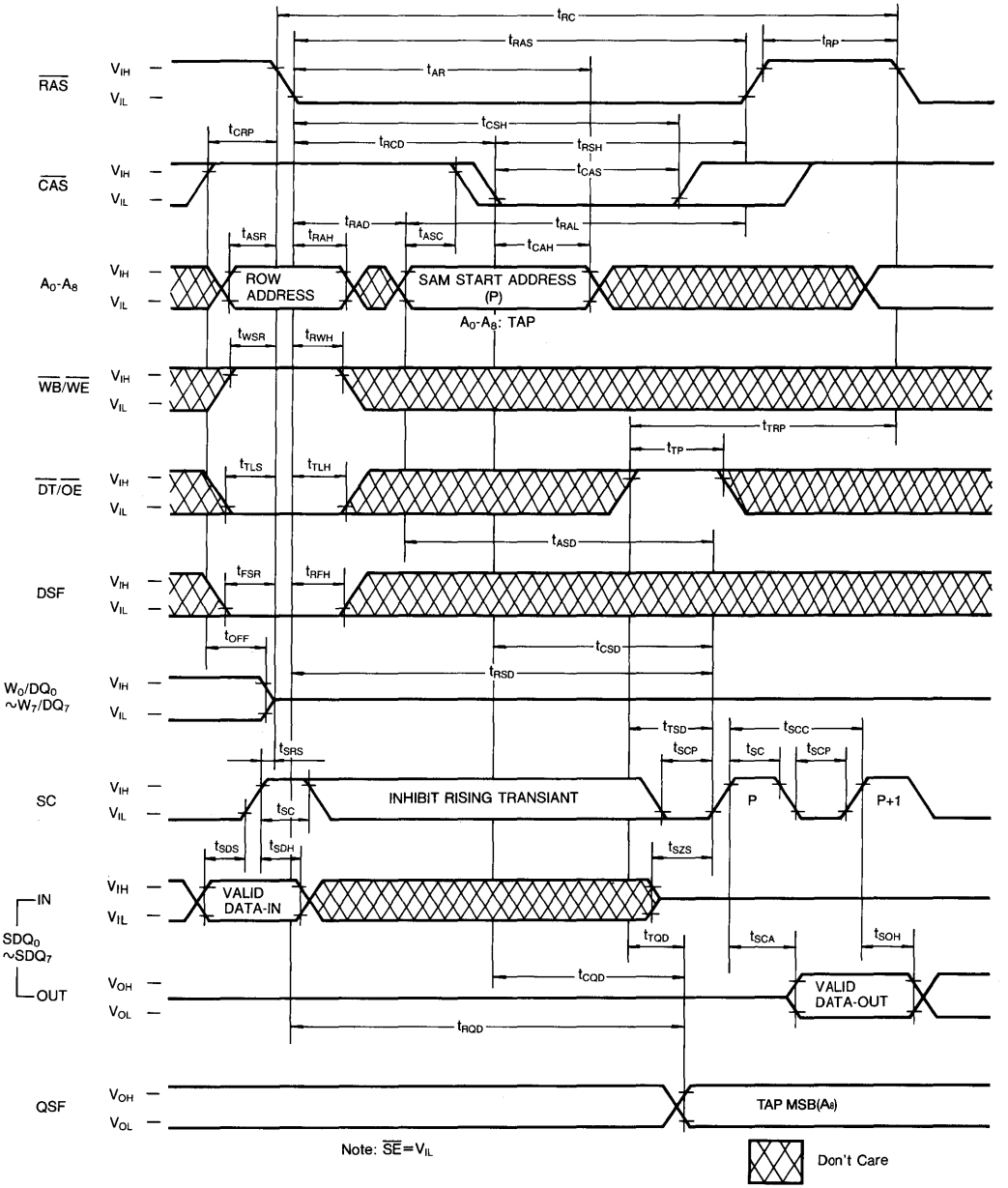


Don't Care

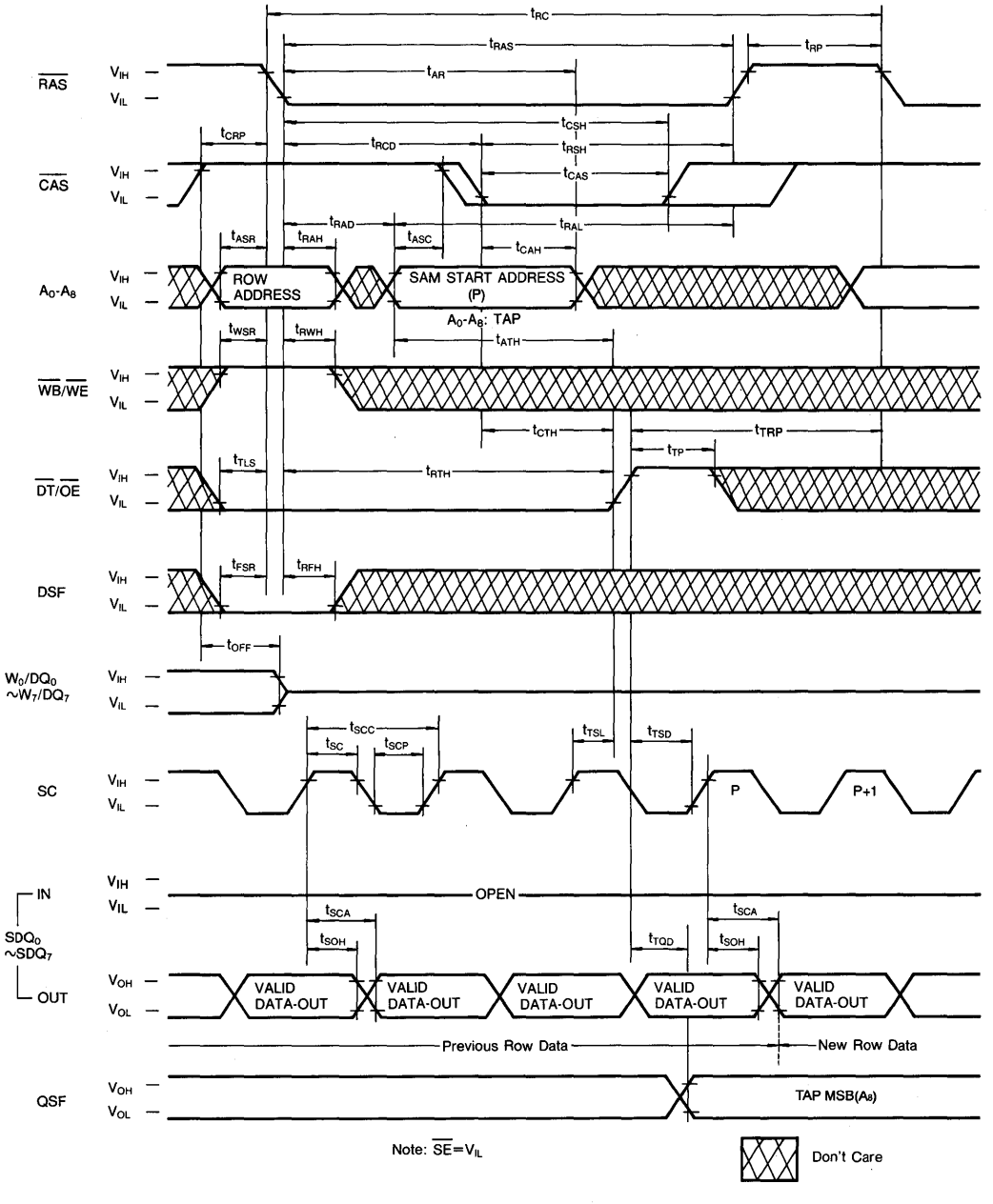
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



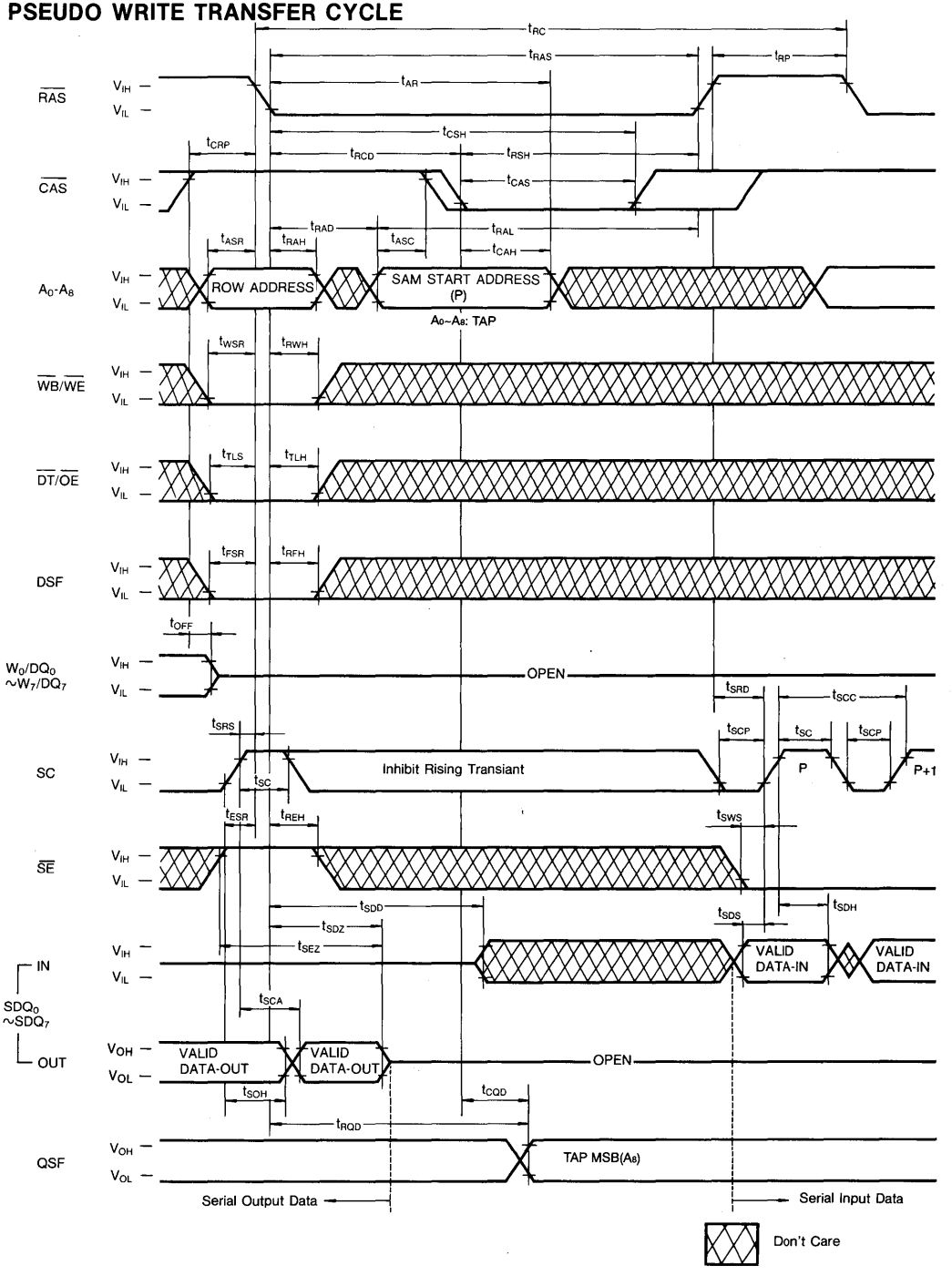
READ TRANSFER CYCLE



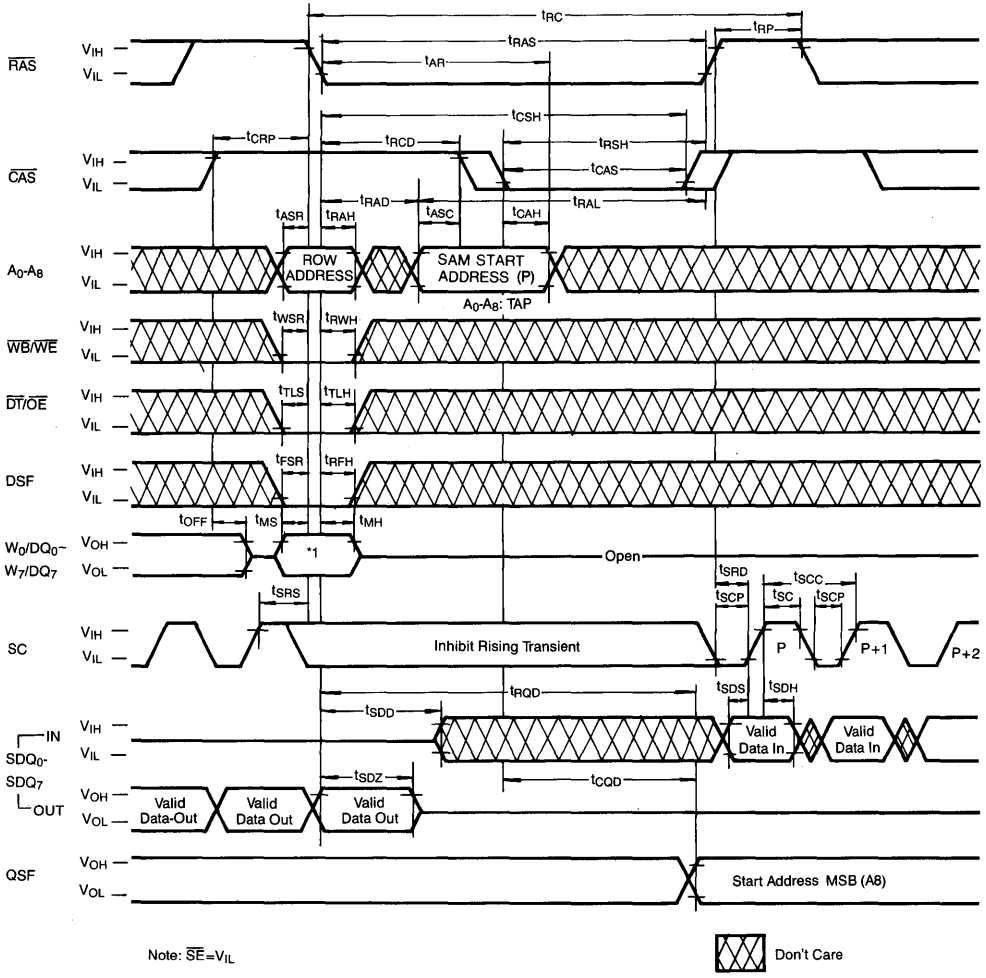
REAL TIME READ TRANSFER CYCLE



PSEUDO WRITE TRANSFER CYCLE

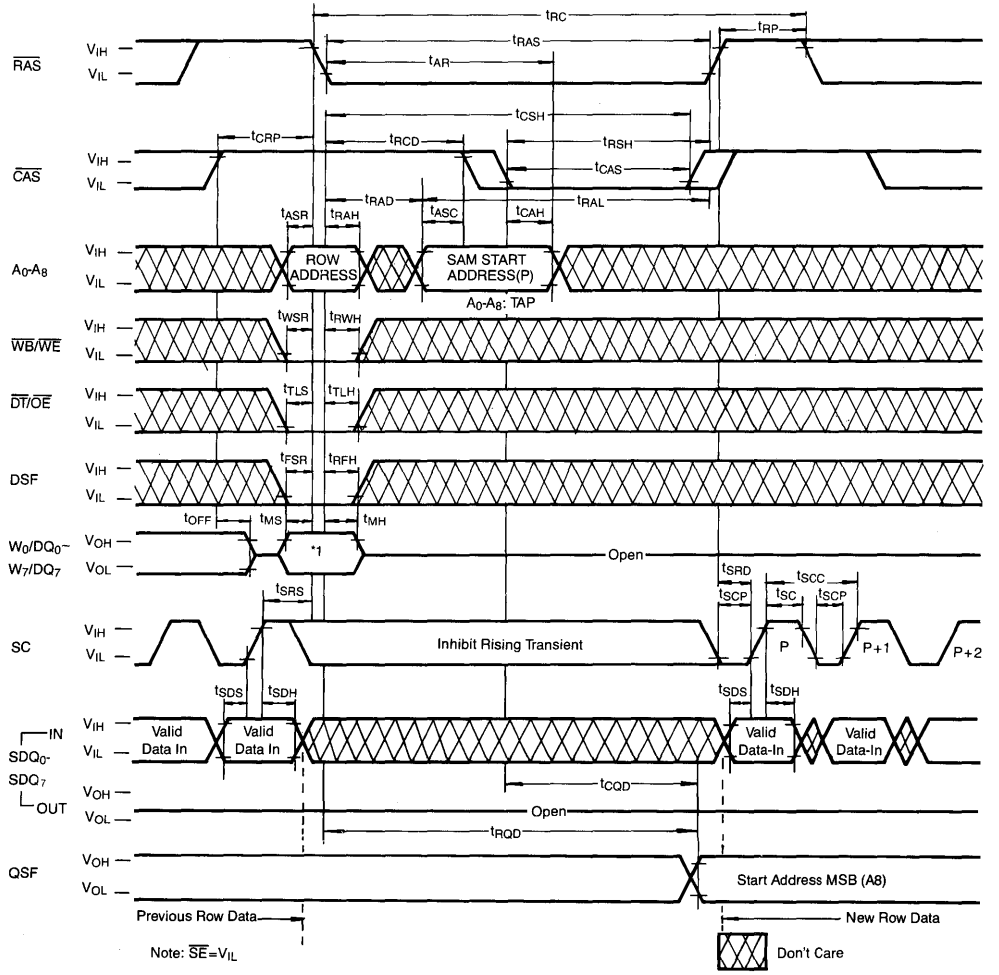


MASKED WRITE TRANSFER CYCLE (Output Mode to Input Mode Switch)



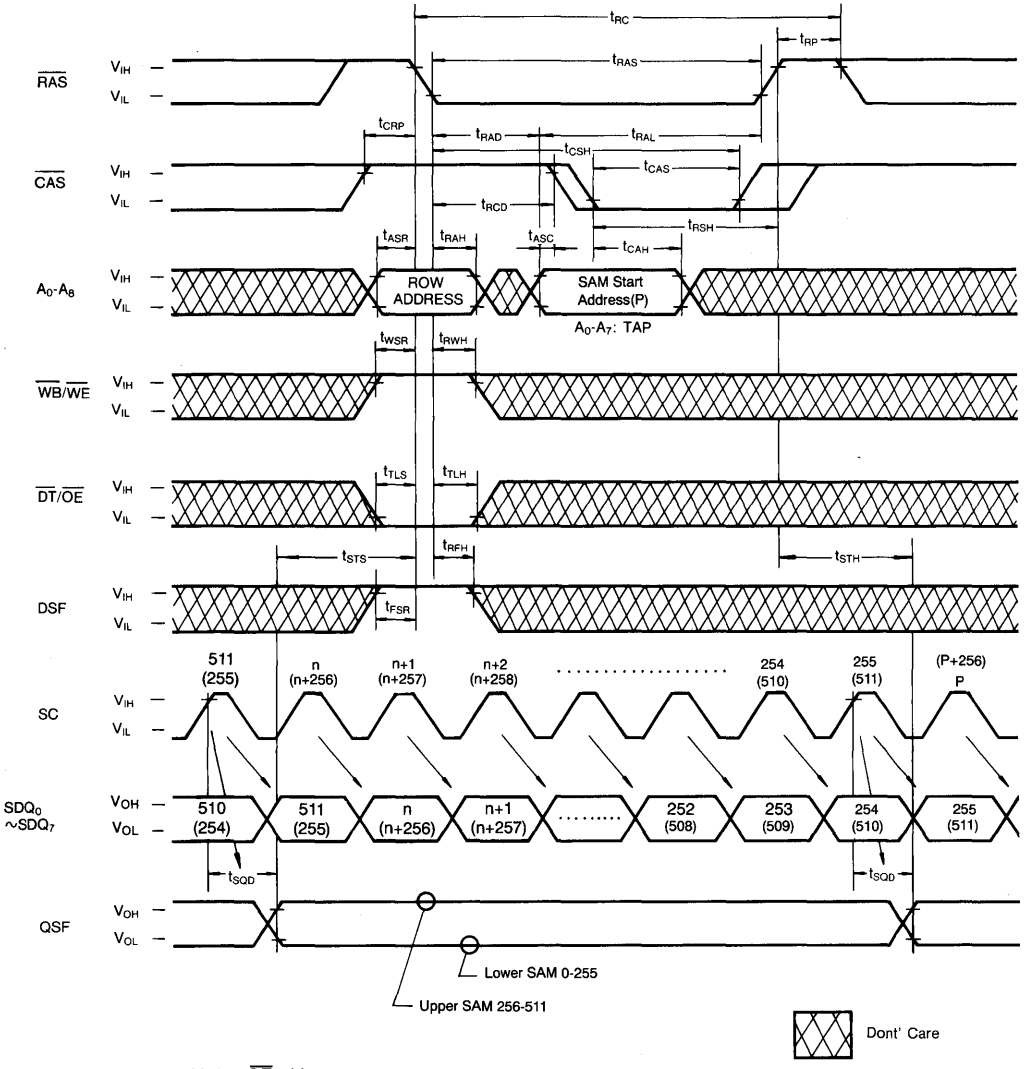
*1(WMi)	Transfer
0	Disable
1	Enable

MASKED WRITE TRANSFER CYCLE



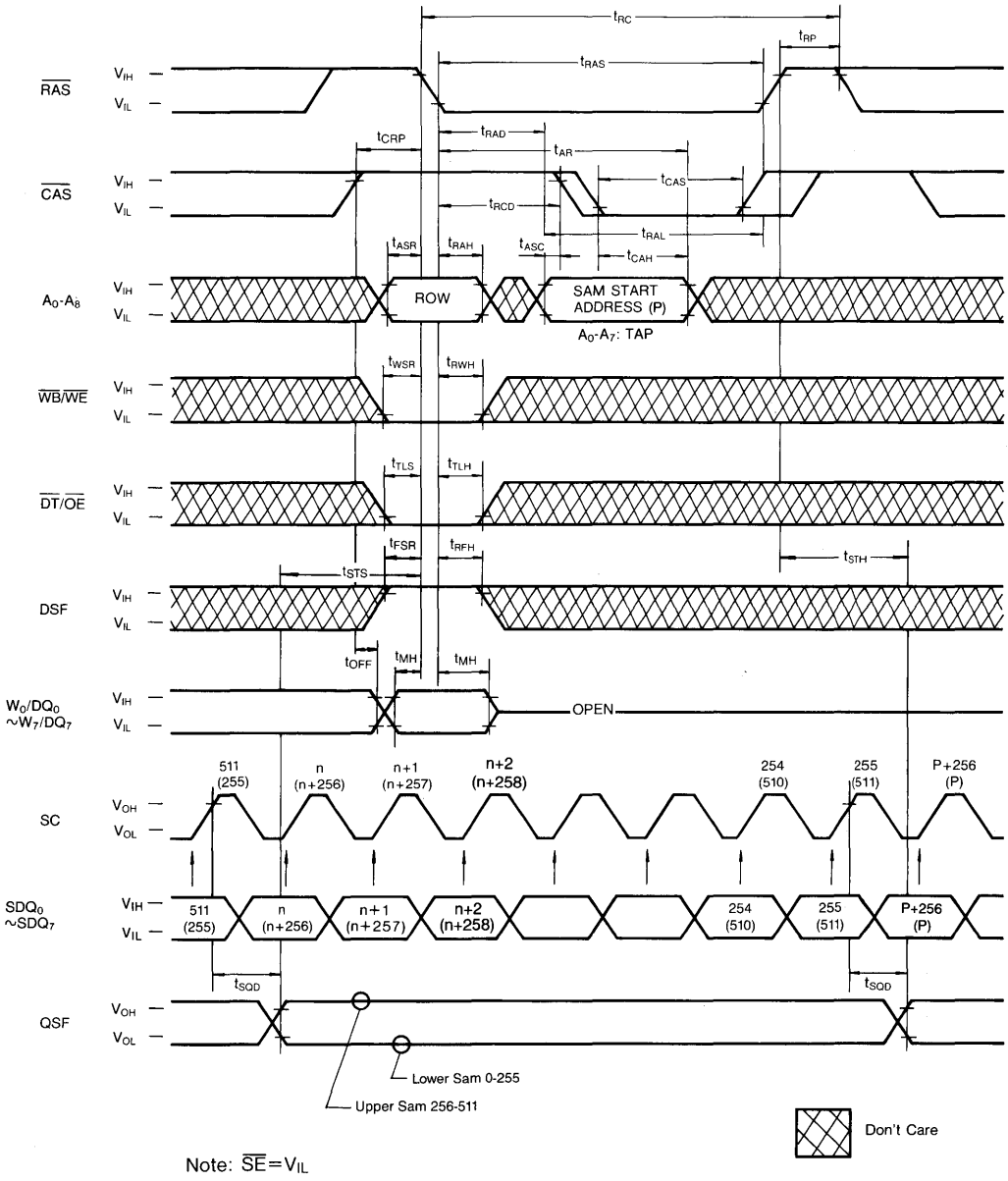
*1(WMi)	Transfer
0	Disable
1	Enable

SPLIT READ TRANSFER CYCLE



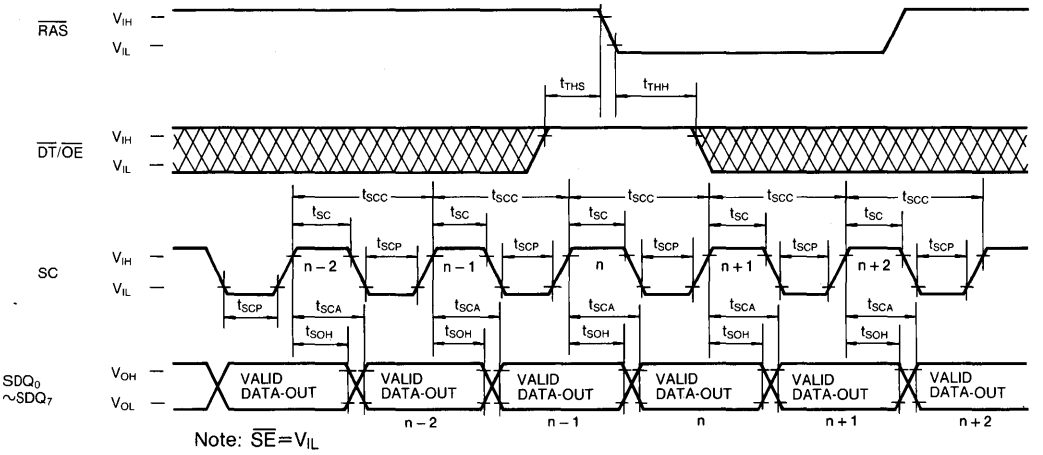
Note: $\overline{SE}=V_{IL}$

MASKED SPLIT WRITE TRANSFER CYCLE



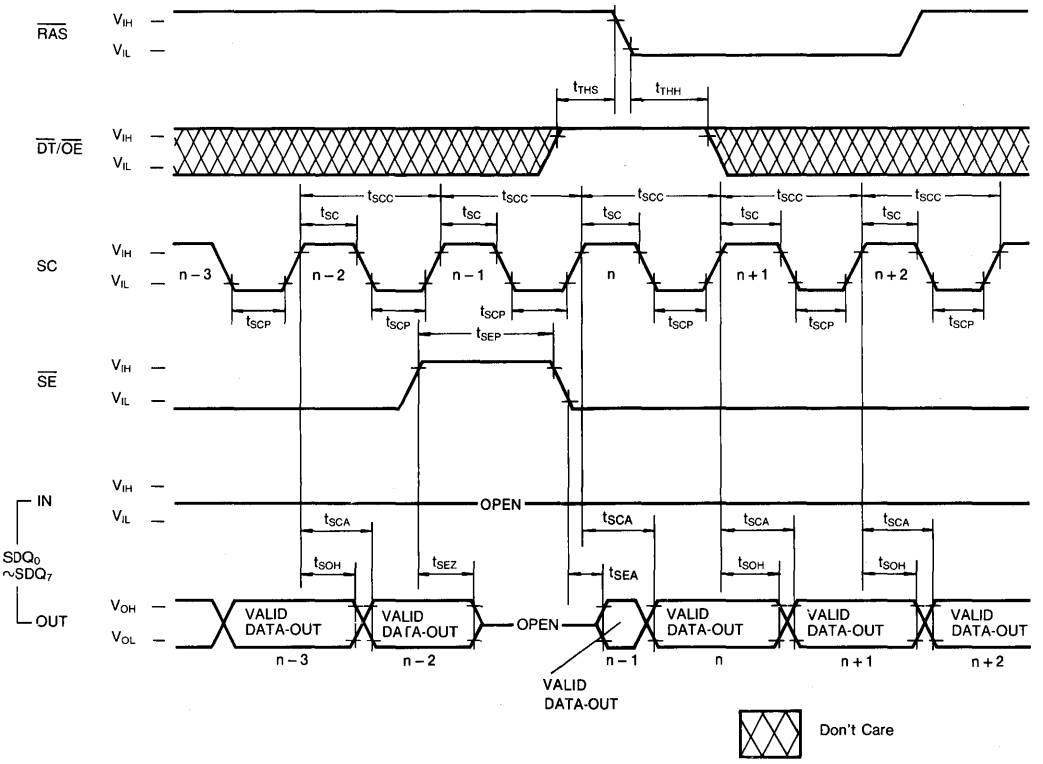
Note: $\overline{SE}=V_{IL}$

SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)

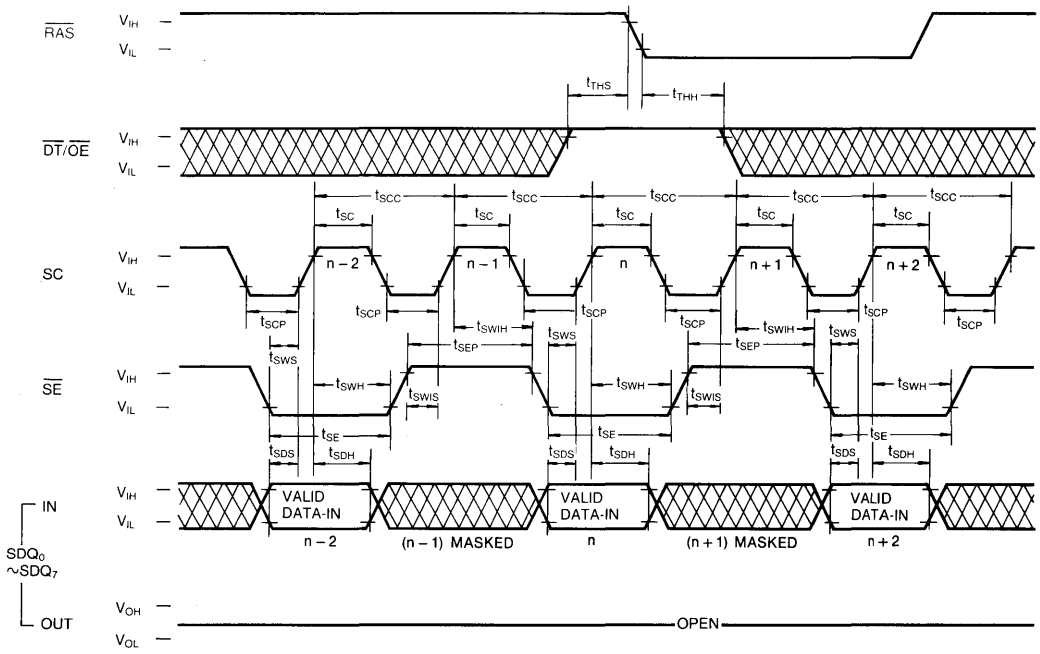


Note: $\overline{SE} = V_{IL}$

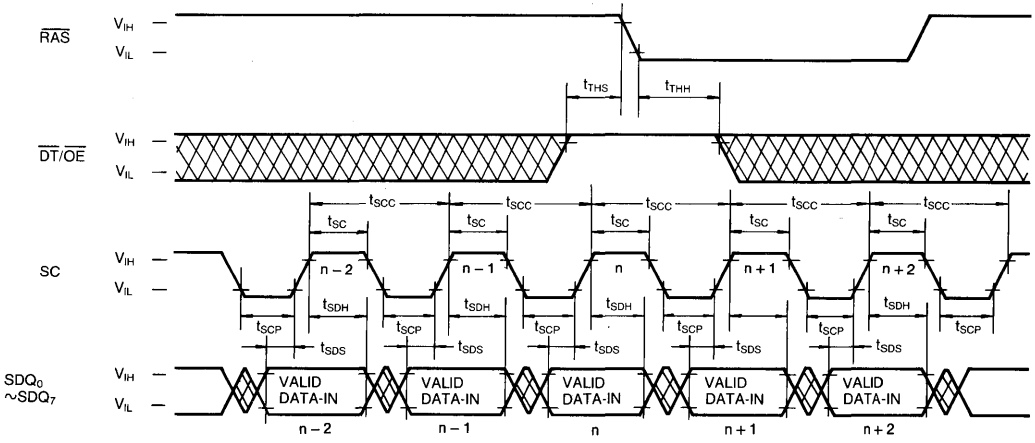
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



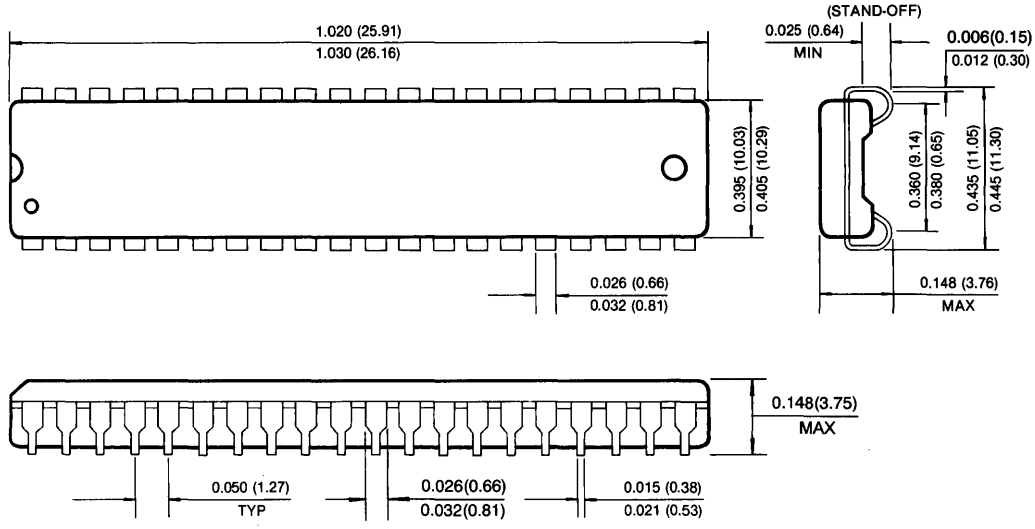
Note: $\overline{SE}=V_{IL}$

Don't Care

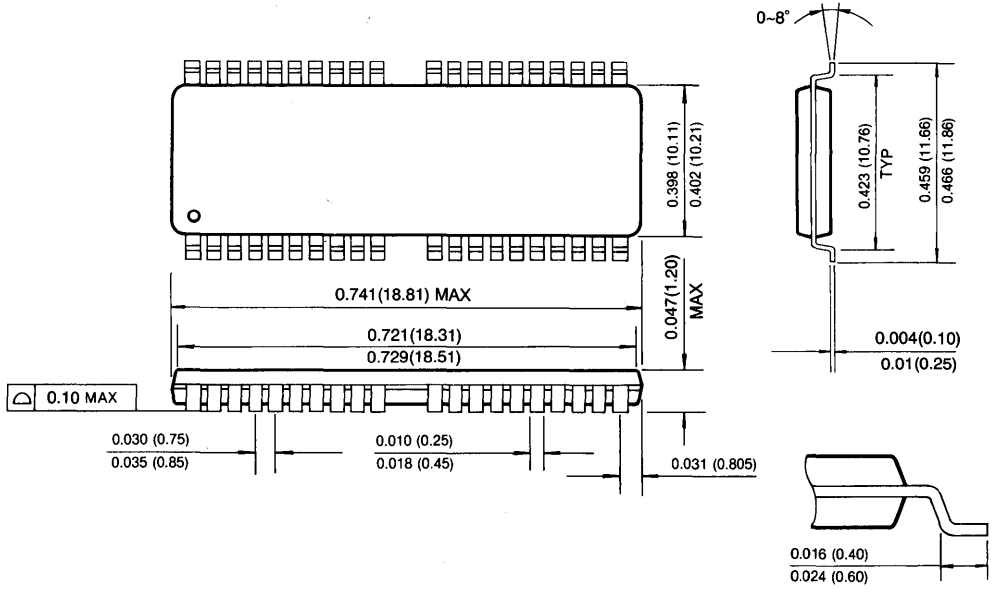
PACKAGE DIMENSIONS

40-PIN PLASTIC SOJ

Units: Inches (millimeters)



40/44-PIN PLASTIC TSOP-II (Forward Type)



256K X 8 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K x 8 bits RAM port
  512 x 8 bits SAM port
- **Performance range :**

Parameter \ Speed		-6	-7	-8
RAM access time(t_{RAC})		60ns	70ns	80ns
RAM access time(t_{CAC})		15ns	20ns	20ns
RAM cycle time(t_{RC})		110ns	130ns	150ns
RAM page mode cycle(t_{PC})		30ns	35ns	40ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time(t_{SCC})		18ns	22ns	25ns
SAM active current	KM428C257	110mA	100mA	90mA
	KM428V257	–	60mA	55mA
SAM active current	KM428C257	55mA	50mA	45mA
	KM428V257	–	30mA	25mA

- **Fast Page Mode with Extended Data Out**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR) and Serial Write (SW)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Register(SRT)**
- **Write and Split Write Transfer with Stop Register (New and Old Mask), (WT,SWT)**
- **Block Write (BW), Flash Write (FLW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single +5V$\pm$10% Supply Voltage**

Single +3.3V$\pm$10% Supply Voltage
Low Vcc (3.3V) Part Name: KM428V257
KM428C257: 60, 70, 80ns
KM428V257: 70, 80ns
Plastic 40-Pin 400mil SOJ
Plastic 40/44Pin 400mil TSOP II
(Forward and Reverse Type)

GENERAL DESCRIPTION

The Samsung KM428C/V257 is a CMOS 256K x 8 bit Dual Port DRAM. It consists of a 256K x 8 dynamic random access memory (RAM) port and 512 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 4096 bits.
It operates like a conventional 256K x 8 CMOS DRAM.
The RAM port has a write per bit mask capability.
Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Block Write and Flash Write capability.

The SAM port consists of eight 512 bit high speed shift registers that are connected to the RAM array through a 4096 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read, write and programmable (Stop Register) Split Transfers or normal Read/Write Transfer.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C/V257 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

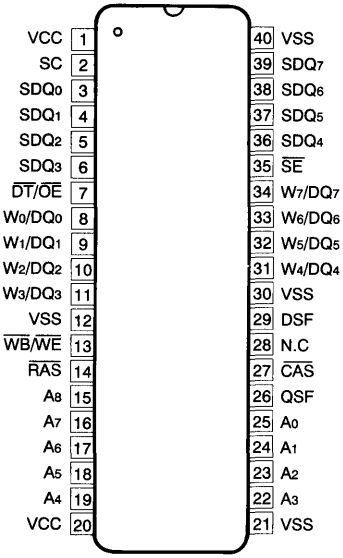
All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN DESCRIPTION

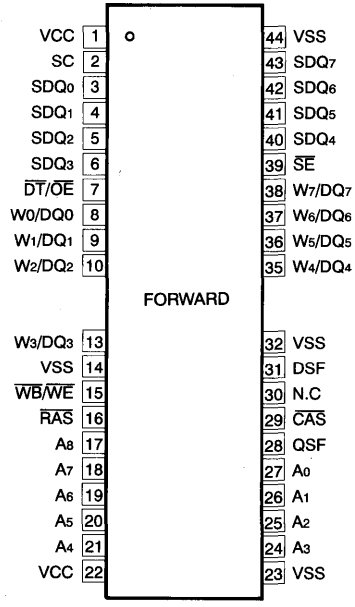
Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WB/WE}$	IN	The $\overline{WB/WE}$ input is a multifunction pin. when $\overline{WB/WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT/OE}$	IN	The $\overline{DT/OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions(BW, FW, Split Transfer, etc)are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0-255, High if address is 256-511.
$\overline{SE}$	IN	In a serial read cycle. $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
Vcc	SUPPLY	Power supply
Vss	SUPPLY	Ground

PIN CONFIGURATION (TOP VIEWS)

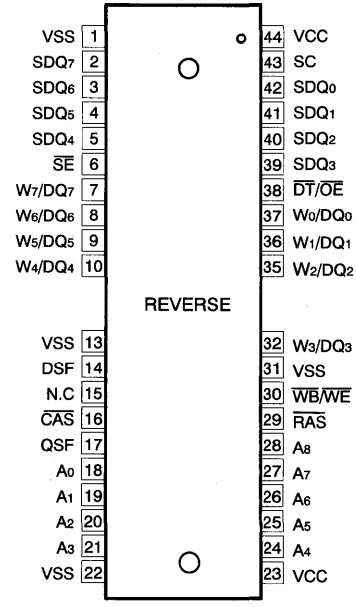
40 Pin 400 mil SOJ



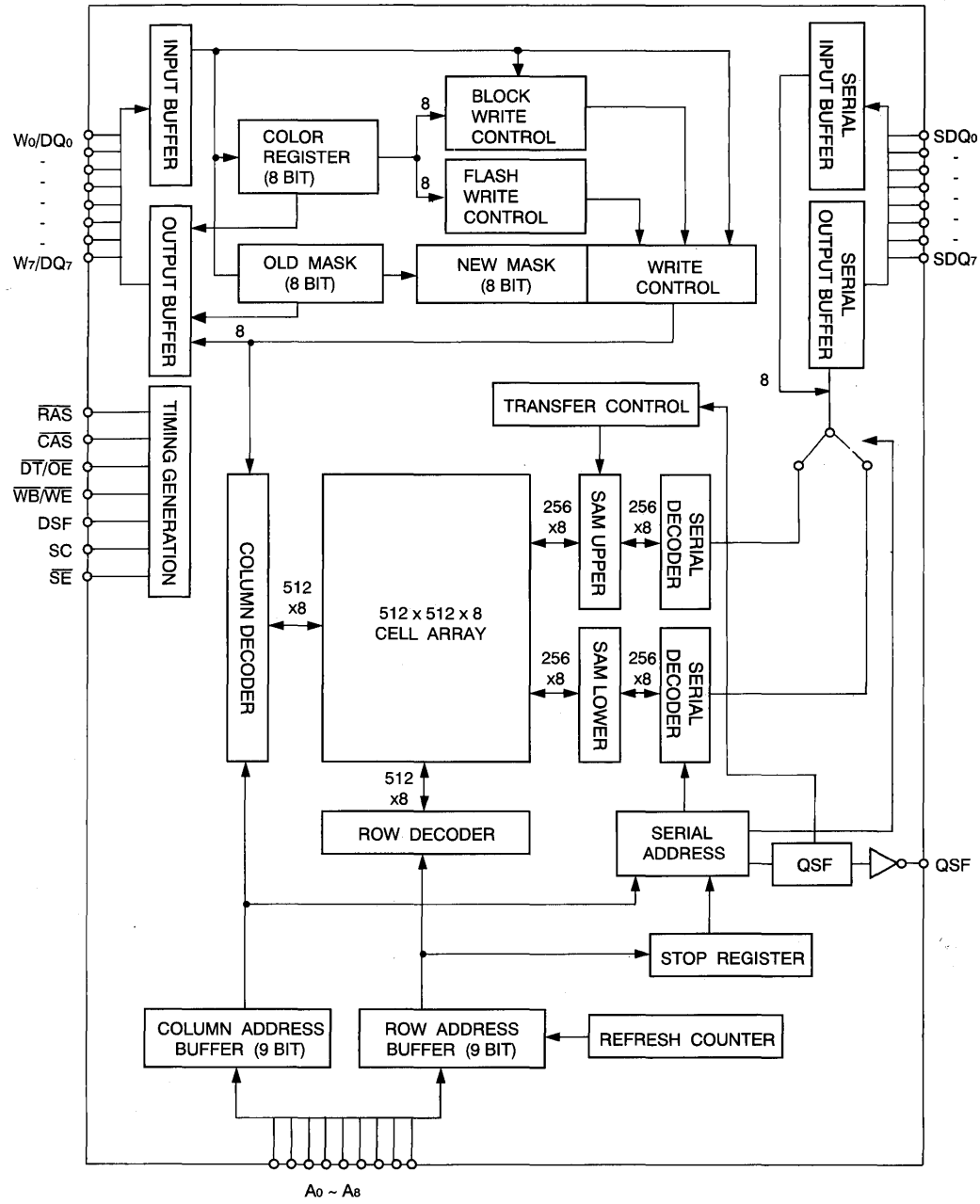
40/44 Pin 400 mil TSOP II



40/44 Pin 400 mil TSOP II



BLOCK DAIGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS				CAS	Address		DQi Input		Write Mask	Register		Function
	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE		Mask	Color	
CBRS (Note 1,3)	0	X	0	1	–	Stop (note4)	–	X	–	–	–	–	CBR Refresh/Stop (Register set)
CBRN (Note 1)	0	X	1	1	–	X	–	X	–	–	–	–	CBR Refresh (No reset)
CBRR (Note 1)	0	X	X	0	–	X	–	X	–	–	–	–	CBR Refresh (Option reset)
ROR	1	1	X	0	–	Row	–	X	–	–	–	–	RAS Only Refresh
MWT	1	0	0	0	X	Row	Tap	WMI	–	Yes	Use	–	Masked Write Transfer (New/Old)
MSWT	1	0	0	1	X	Row	Tap	WMI	–	Yes	Use	–	Masked Split Write Transfer(New/Old)
RT	1	0	1	0	X	Row	Tap	–	–	–	–	–	Read Transfer
SRT	1	0	1	1	X	Row	Tap	–	–	–	–	–	Split Read Transfer
RWM	1	1	0	0	0	Row	Col.	WMI	Data	Yes	Use	–	Read Write (New/Old Mask)
BWM	1	1	0	0	1	Row	Col. Mask	WMI	Col.	Yes	Use	Use	Block Write (New/Old Mask)
FWM	1	1	0	1	X	Row	X	WMI	X	Yes	Use	Use	Flash Write(New/Old mask)
RW	1	1	1	0	0	Row	Col	X	Data	No	–	–	Read Write (No Mask)
BW	1	1	1	0	1	Row	Col	X	Col Mask	No	–	Use	Block Write (No Mask)
LMR (Note 2)	1	1	1	1	0	Row (note6)	X	X	WMi	–	Load (Note5)	–	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	Row (note6)	X	X	Color	–	–	Load	Load Color Register

X: Don't Care, -: Not Applicable, Tap: SAM Start(column)Address, WMi: Write Mask Data (i=0~7)
RAS only refresh does not reset Stop or LMR functions.

Notes :

(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, FLW, MWT, MSWT, RWM and BWM use old mask. (CBRR reset to new mask. Use CBRS or CBRN to perform CAS- before-RAS refresh while using Old mask)
(3) With CBRS, split transfer operation uses stop Register as a boundary address
(4) Stop defines the column on which Shift out moves to the other half of the SAM.
(5) After LMR, WMi is only changed by the another LMR or CBRR cycle.
(6) The Row that is addressed will be refreshed, but a Row address is not required.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM428C257	KM428V257	
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	-0.5 to + 4.6	V
Storage Temperature	Tstg	-55 to + 150	-55 to + 150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70 °C)

Item	Symbol	KM428C257			KM428V257			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC}+1V	2.0	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	–	0.8	-0.3	–	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \le V_{IN} \le V_{CC}$+0.5V*1 all other pins not under test=0 volts, $\overline{SE} \ge V_{CC}$-0.2V)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)*1	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1: 3.6V in KM428V257

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25°C)

Item	Symbol	MIN	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF
Output Capacitance (QSF)	C_{QSF}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM428C257			KM428V257		Unit
			-6	-7	-8	-7	-8	
Operating current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC1	110	100	90	60	55	mA
	Active	ICC1A	155	140	125	85	75	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$=VIH, DSF=VIL)	Standby	ICC2	10	10	10	5	5	mA
	Active	ICC2A	55	50	45	30	25	mA
RAS Only Refresh Current*1 ($\overline{CAS}$=VIH, $\overline{RAS}$ Cycling @tRC=min.)	Standby	ICC3	100	90	80	55	50	mA
	Active	ICC3A	145	130	115	80	70	mA
Fast Page Mode Current*1 ($\overline{RAS}$=VIL, $\overline{CAS}$ Cycling @tPC=min.)	Standby	ICC4	80	75	70	45	40	mA
	Active	ICC4A	125	115	105	70	65	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC5	90	85	80	50	45	mA
	Active	ICC5A	135	125	115	75	70	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC6	140	125	110	75	70	mA
	Active	ICC6A	185	165	145	100	90	mA
Flash Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC7	90	85	80	50	45	mA
	Active	ICC7A	135	125	115	75	70	mA
Block Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC8	110	105	100	65	60	mA
	Active	ICC8A	155	145	135	90	80	mA
Color Register Load or Read Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	ICC9	90	85	80	50	45	mA
	Active	ICC9A	135	125	115	75	70	mA

Note *1 : Real values dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as average current. In ICC1, ICC3, ICC6, ICC7, ICC8, ICC9 address transition should be changed only once while $\overline{RAS}$=VIL. In ICC4 address transition should be changed only once while $\overline{CAS}$=VIH

AC CHARACTERISTICS

(0°C≤TA≤70°C, KM428C257: VCC=5.0V±10%, KM428V257: VCC=3.3V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		200		ns	
Fast page mode cycle time	tPC	30		35		40		ns	
Fast page mode read-modify-write	tPRWC	80		85		90		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	tCAC		12		15		20	ns	3,5,6
Access time from column address	tAA		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Write command pulse width	tWPZ	10		10		10		ns	
Write command output buffer turn-off delay	tWEZ		10		15		15	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5,6
$\overline{RAS}$ to column addr. delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time(CBR counter test cycle)	t_{CPT}	10		10		10		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
Output hold time from $\overline{CAS}$	t_{DOH}	5		5		5		ns	
Row addr. set-up time	t_{ASR}	0		0		0		ns	
Row Addr. hold time	t_{RAH}	10		10		10		ns	
Column addr. set-up time	t_{ASC}	0		0		0		ns	
Column addr. hold time	t_{CAH}	15		15		15		ns	
Column addr. hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column addr. to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	15
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	15
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column addr. to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output buffer turn-off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period(512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	15		15		15		ns	
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	tCTH	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	tATH	20		25		30		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay(read transfer)	tRSD	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	tCSD	25		30		35		ns	
Col. Addr.to first SC delay(read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	tTSD	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	tSRS	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	tSRD	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	tSDD	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	tSZS	0		0		0		ns	
SC cycle time	tSCC	18		22		25		ns	
SC pulse width(SC high time)	tSC	6		7		7		ns	14

AC CHARACTERISTICS (Continued)

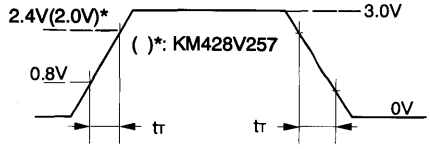
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
SC precharge(SC low time)	tSCP	6		7		7		ns	
Access time from SC	tSCA		15		17		20	ns	
Serial output hold time from SC	tSOH	5		5		5		ns	4
Serial input set-up time	tSDS	0		0		0		ns	
Serial input hold time	tSDH	10		15		10		ns	
Access time from $\overline{SE}$	tSEA		15		17		20	ns	
$\overline{SE}$ pulse width	tSE	20		20		25		ns	4
$\overline{SE}$ precharge time	tSEP	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	
Serial input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	7
Serial write enable set-up time	tSWS	0		0		0		ns	
Serial write enable hold time	tSWH	10		15		15		ns	
Serial write disable set-up time	tSWIS	0		0		0		ns	
Serial write disable hold time	tSWIH	10		15		15		ns	
Split transfer set-up time	tSTS	20		25		25		ns	
Split transfer hold time	tSTH	20		25		25		ns	
SC-QSF delay time	tSQD		20		25		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		25		25	ns	
$\overline{RAS}$-QSF delay time	tRQD		60		70		80	ns	
$\overline{CAS}$-QSF delay time	tCQD		20		35		40	ns	
$\overline{DT}/\overline{OE}$ high pulse width	tOEP	10		10		10		ns	
$\overline{DT}/\overline{OE}$ high hold time from $\overline{CAS}$ high	tOEHC	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), and t_{SDZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. During power-up $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ must be held High or track with V_{CC}. After power-up, initial status of chip is described below.

PIN or REGISTER	STATUS
Color Register	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
W_i/DQ_i	Hi-Z
SAM Port	Input Mode
SDQ_i	Hi-Z
QSF	Hi-Z

13. Recommended operating input condition:



   Input pulse levels are from 0.0V to 3.0Volts.
   All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 3.0ns
14. Assume t_T=3ns.
15. t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).

DEVICE OPERATION

The KM428C/V257 contains 2,097,152 memory locations. Eighteen address bits are required to address a particular 8bit word in the memory array. Since the KM428C/V257 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM428C/V257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This is the beginning of any KM428C/V257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C/V257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access time is specified by t_{CAC} or t_{AA}.

The KM428C/V257 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM read cycle, D_{OUT} buffer is designed to make turn-off by the rising edge of CAS even though $\overline{OE}$ is to be low. The KM428C/V258 offers an accelerated Fast Page Mode cycle by eliminating output disable from $\overline{CAS}$ high.

This is called "Extended Data out (or Hyper Page) mode", Data outputs are disabled at $\overline{WB}/\overline{WE}$=low, $\overline{DT}/\overline{OE}$=high and t_{OFF} time after $\overline{RAS}$ and $\overline{CAS}$ are high. The t_{OFF} time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs later(see Figure 1). What the output buffer is disabled during $\overline{DT}/\overline{OE}$=high is to use Bank selection in the frame buffer memory using common I/O line. Read, write and read-modify write cycles are available during the Extended data out mode.

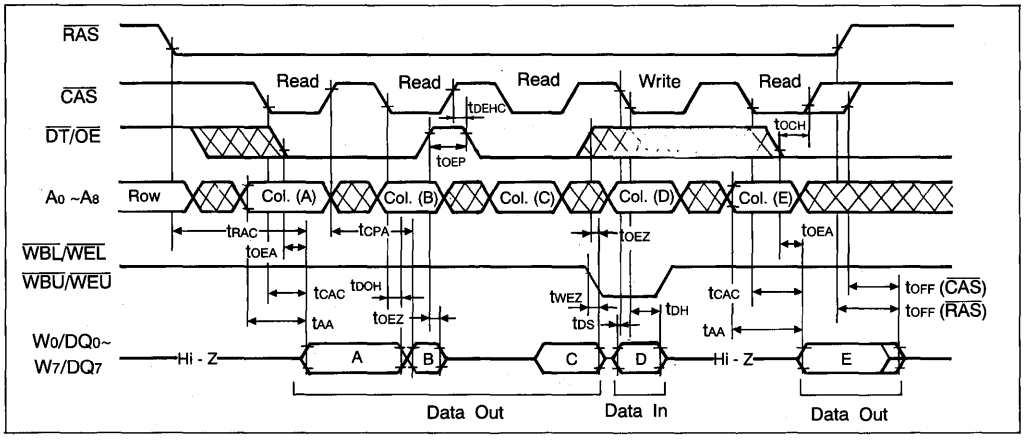


Figure 1. Extended Data Out Example

DEVICE OPERATION (Continued)

New Mask Write Per Bit

The New Mask Write cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB/WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_7/DQ_7 pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the data bit remains unchanged. When the mask data is high, data is written into the RAM. The mask data is valid for only one cycle, defined by an active $\overline{RAS}$ period. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB/WE}$ low before $\overline{CAS}$ falling and late Write cycle is achieved by $\overline{WB/WE}$ low after the falling edge of $\overline{CAS}$. During the Early or Late Write, cycle, input data through $W0/DQ_0$~W_7/DQ_7 must meet the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB/WE}$. When $\overline{WB/WE}$ is high at the falling edge of $\overline{RAS}$. no masking operation is performed.

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the wi/DQi pins into the Mask data Register at the falling edge of $\overline{CAS}$ or $\overline{WB/WE}$. The LMR cycle is performed if DSF high, $\overline{WB/WE}$ high at the falling edge of $\overline{RAS}$ and DSF Low at the $\overline{CAS}$ falling edge. If an LMR is done the KM428C/V257 is set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR)cycle. If an LMR is done, all Masked Write are Old Masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register(See Figure3). The mask data is applied in the same manner as in New Masked write-Per-Bit mode. Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After Power up, the KM428C/V257 initialized in the New Masked Write mode.

Fast Page Mode

Fast page mode cycle reads/writes the data of the same row address at high speed by togging $\overline{CAS}$ while $\overline{RAS}$ is low. In this cycle, read, write, read-modify write, and block write cycles can be mixed. In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column address.

This eliminates the time required to set up and strobe sequential row address for the same page

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	Wi/DQi	FUNCTION
↓	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	INHIBIT WRITE

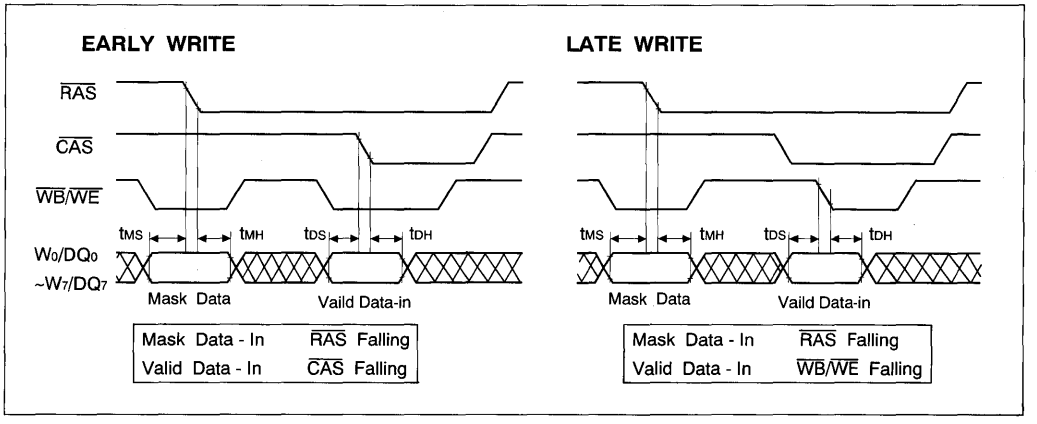


Figure 2. New Mask Write Cycle Example 1 (Early Write & Late Write)

DEVICE OPERATION (Continued)

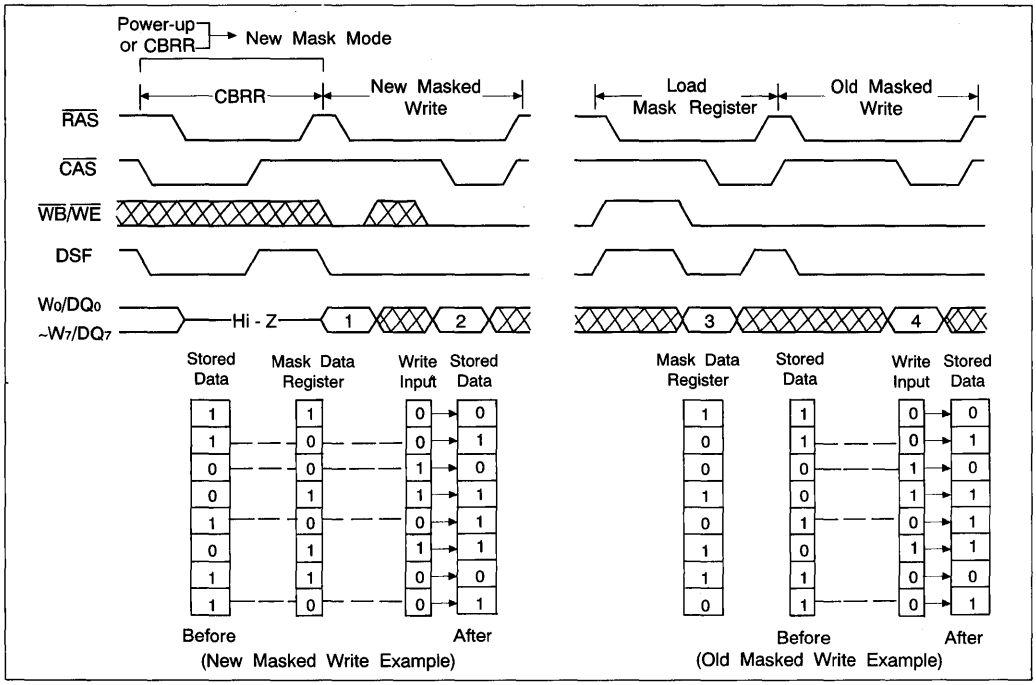


Figure 3. New Mask Write Cycle and Old Mask Write Cycle Example 2.

Load Color Register(LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(delayed write) via the W_0/DQ_0~W_7/DQ_7 pins. This data is used in Block Write and Flash Write cycles and remains unchanged until the next Load Color Register cycle.

Block Write

In a Block Write cycle four adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 8-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into four adjacent locations of the same row of each corresponding bit plane(8). This results in a total of 32-bits being written in a single Block Write cycle compared to 8-bits in a normal Write cycle.

The Block Write cycle is performed if DSF is low on the falling edge of $\overline{RAS}$ and high on the falling edge of $\overline{CAS}$.

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.

Since four bits are being written at a time, when the minimum increment required for the column address is four. Therefore, when the column address is latched on the falling edge of $\overline{CAS}$, the 2LSBs, A_0 and A_1 are ignored and only bits(A_2~A_8) are used to define the location of the first bit out of the four to be written.

Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_3/DQ_3 pins provideds column mask data. That is, for each of the four bits in all 8-bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the four, but the second remains unchanged. Fig. 4 shows the correspondence of each data line to the column mask bits.

Masked Block Write(MBW)

A Masked Block Write cycle is identical to a New Mask Write-per-bit cycle except that each of the 8-bit planes being masked is operating on 4 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB/WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high on the falling edge of $\overline{CAS}$. Mask data is latched into the device via the W_0/DQ_0~W_7/DQ_7 pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle.

DEVICE OPERATION (Continued)

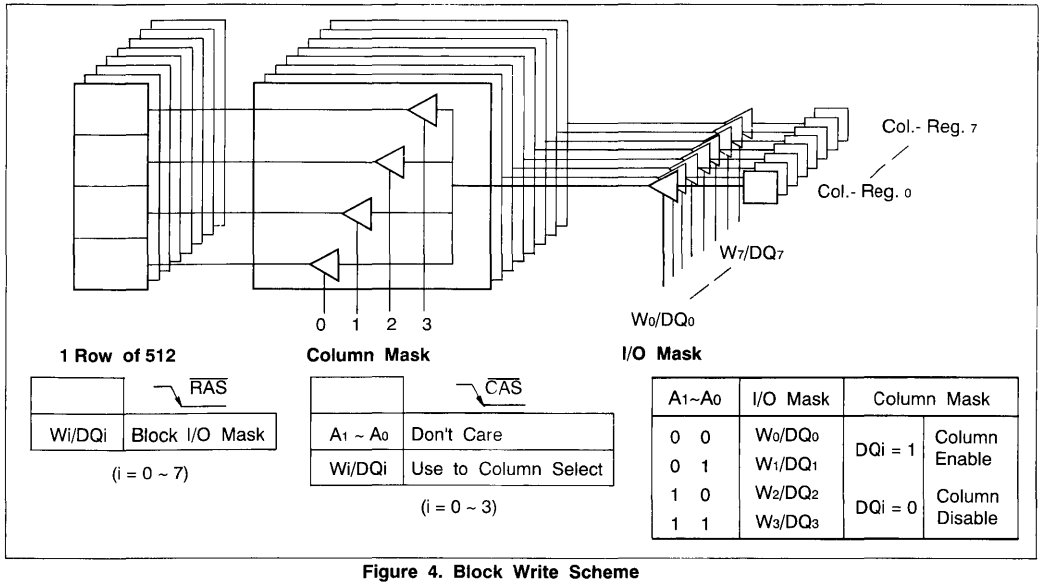


Figure 4. Block Write Scheme

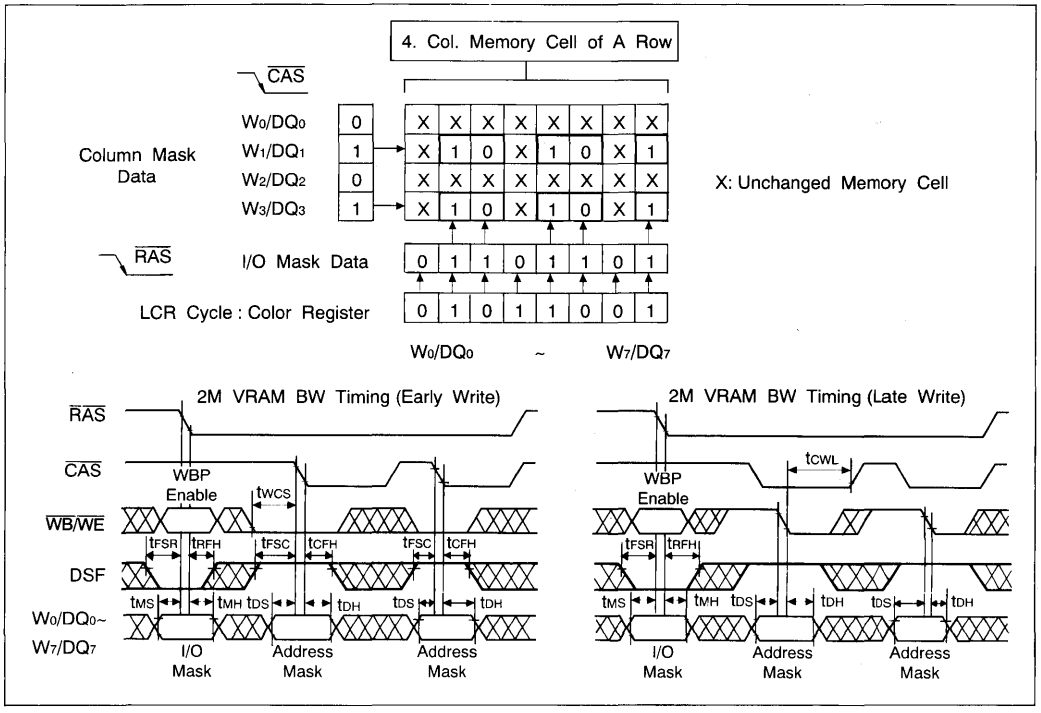


Figure 5. Block Write Example and Timing

DEVICE OPERATION (Continued)

Flash Write

The Flash Write cycle is a way of writing each bit of the Color Register into the whole row (512 columns) simultaneously. This function is used for fast screen clear or background color change. 512 columns in each bit plane are written, for a total of 4096 bits(512×8 bit planes) in one cycle. While this cycle writes significantly more data than the Block Write cycle, it is also less selective.

If $\overline{WB}/\overline{WE}$ is low and DSF is high on the falling edge of $\overline{RAS}$, a Flash Write cycle is performed. Also on this edge, the data present on the W_i/DQ_i pins is used as mask data and needs to be provided for every Flash Write cycle. A Load Color Register cycle must have been performed before initiating a Flash Write cycle.

Data Output

The KM428C/V257 has three state output buffers controlled by $\overline{DT}/\overline{OE}$, $\overline{CAS}$ and $\overline{RAS}$, $\overline{WB}/\overline{WE}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ are Low, the output state is in high impedance(High-z). In any cycle, the output goes low impedance state from the first $\overline{CAS}$ falling edge.
Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh).
Each of the KM428C/V257 operating cycles is listed below after the corresponding output state produced by the cycle.

Refresh

The data in the KM428C/V257 is stored as a charge on a tiny capacitor within each memory cell. Due to leakage the data may be lost over a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 4096 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses (A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM428C/V257 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. the refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
The KM428C257 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation; CBRR, CBRN, CBRS. CBRR(CBR Refresh with option reset)is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default value. CBRN(CBR Refresh without Reset)is set if DSF high when $\overline{WB}/\overline{WE}$ is high at the $\overline{RAS}$ falling edge and simply do only refresh operation. CBRS(CBR Refresh with stop register set)cycle is set if DSF high when $\overline{WB}/\overline{WE}$ is low and this mode is to set stop register's value.

Hidden Refresh: a hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM428C/V257 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM428C/V257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

Transfer operation is initiated when $\overline{DT}/\overline{OE}$ is low at the falling edge of $\overline{RAS}$. The state of $\overline{WB}/\overline{WE}$ when $\overline{RAS}$ goes low indicates the direction of transfer (to or from DRAM) and DSF pin is used to designated the proper transfer mode like normal and Split Transfer. Each of the transfer cycle is described in the truth table of transfer operation.(Table2.)

DEVICE OPERATION (Continued)

Table 2. Truth Table for Transfer Operation

RAS Falling Edge					Function	Transfer Direction	Transfer Data Bit	SAM Port Mode
CAS	DT/OE	WB/WE	DSF	SE				
H	L	H	L	*	Read Transfer	RAM → SAM	512 x 8	Input → Output
H	L	L	L	*	Masked Write Transfer	SAM → RAM	512 x 8	Output → Input
H	L	H	H	*	Split Read Transfer	RAM → SAM	256 x 8	Not Changed
H	L	L	H	*	Masked Split Write Transfer	SAM → RAM	256 x 8	Not Changed

2

Read Transfer(RT)

The Read Transfer operation is set if $\overline{DT}/\overline{OE}$ is low, $\overline{WB}/\overline{WE}$ is high, and DSF is low when $\overline{RAS}$ goes low. The row address bits in the read transfer cycle indicate which eight 512bit DRAM Row portions are transferred to the eight SAM data registers. The column address bits indicate the start address of the SAM registers when SAM data read operation is performed. If MSB bit of column address is low during Read transfer operation, the QSF state will be set low and this indicates the start address of the SAM register is present at the lower half of the SAM port.(If A_8 is high, QSF will be high meaning that the start address is in the upper half). Read Transfer may be achieved in two ways. If the transfer is to be synchronized with the SC, $\overline{DT}/\overline{OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with the rising edge of SC(t_{TSL}/t_{TSD})to retain the continuity of serial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT}/\overline{OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(512bit) to be transferred to the selected row in the DRAM array. Masking is selected by latching Wi/DQi(i=0~7)inputs when $\overline{RAS}$ goes low.

The column address defiiness the start address of serial input and its MSB(A_8)defines QSF level.

If A_8 is low, the QSF will be low level to designate that the start address is in positioned in the lower half of SAM. (For A_8=high, the QSF will be high and indicates that the start address will be positioned in the upper half of SAM) After write transfer cycle is completed, SAM port is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to be occured at the first rising edge of $\overline{DT}/\overline{OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is begun by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. Column address pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data(0-Lower, 1=Upper). A Split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary(e.g. 255th or 511th bit).

Example of SRT applications are shown in Fig. 6 through Fig 10.

The normal usage of Split Read Transfer cycle is described in Fig 6. When Read Transfer is executed,

DEVICE OPERATIONS (Continued)

data from X1 row address is fully transferred to the SAM port and Serial Read is started from 0(Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "0+256" Tap address instead of "0" is loaded.

The another example of SRT cycle is described in Fig. 7. When Serial Read is performed after executing RT and SRT in succession the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 8 and 9 are the example of abnormal SRT cycle.

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig. 8, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 9. indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511. In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during $t_{STH}+t_{STS}$ (See Figure 10). This is also true in Masked Split Write Transfer.

A Split Read Transfer does not change the direction of the SAM I/O port.

Masked Split Write Transfer(MSWT)

This transfer function is very similiar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when RAS goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "don't care". The example of MSWT is described in Fig. 11. The opening cycle MWT is needed before MSWT can be performed.

DEVICE OPERATION (Continued)

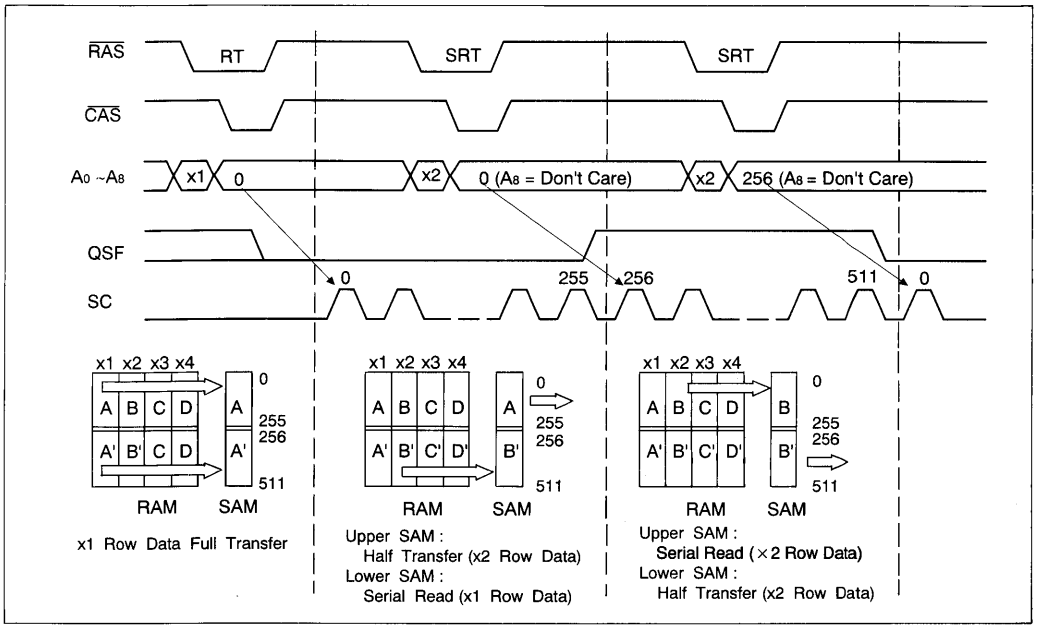


Figure 6. Split Read Transfer Normal Usage

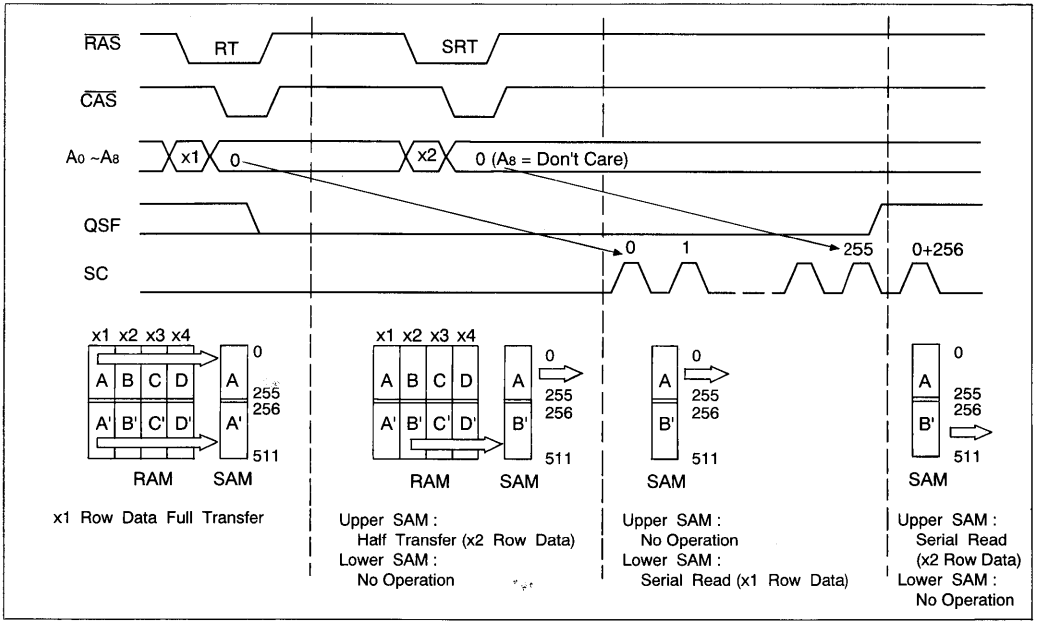


Figure 7. Split Read Transfer Normal Usage

DEVICE OPERATION (Continued)

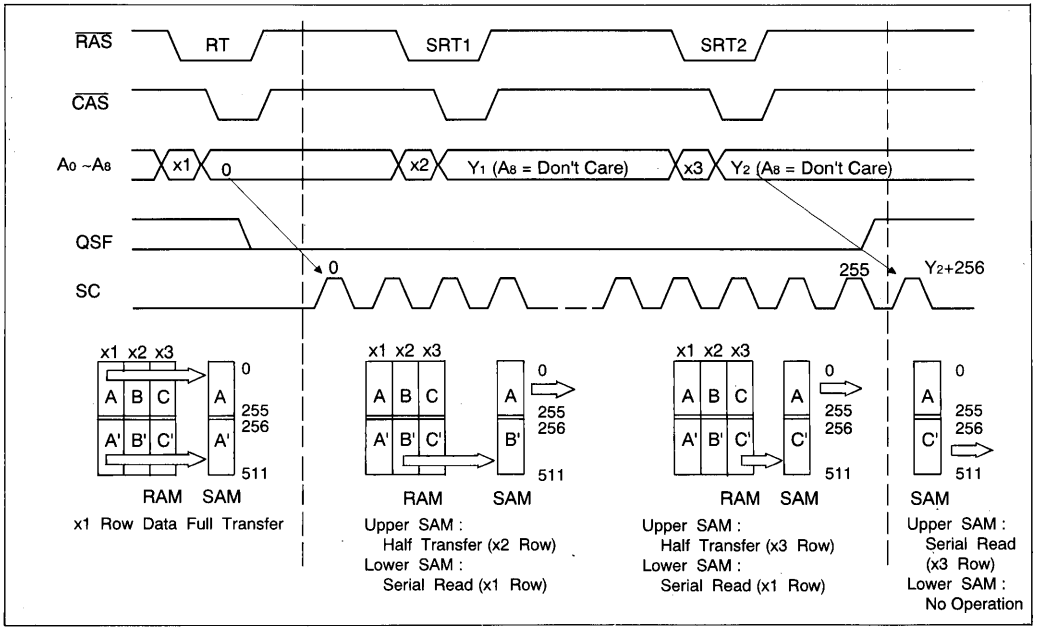


Figure 8. Split Read Transfer Abnormal Usage (Case 1)

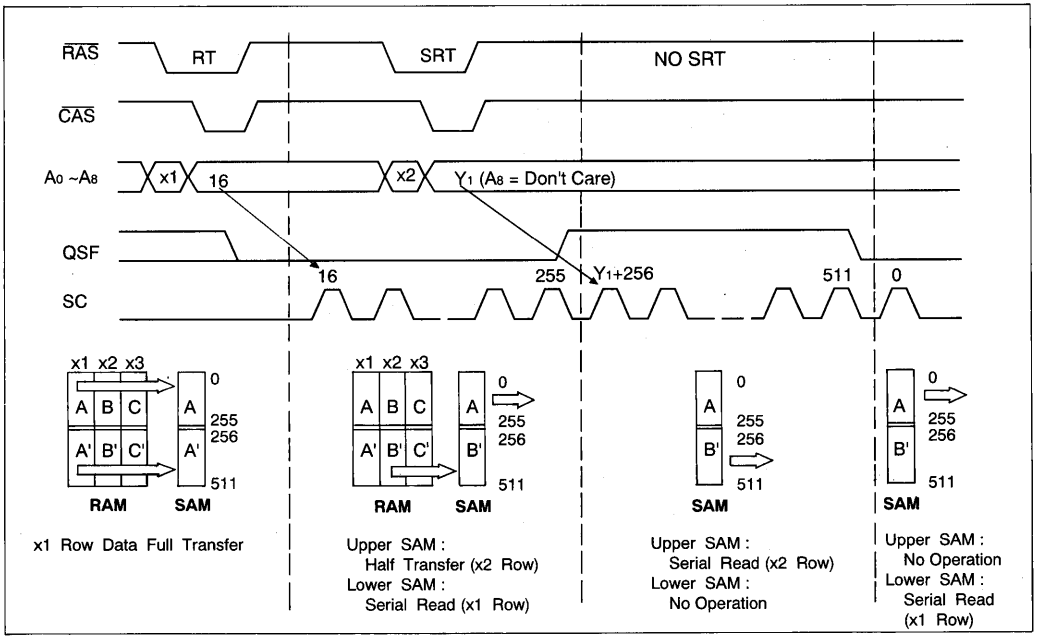


Figure 9. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATION (Continued)

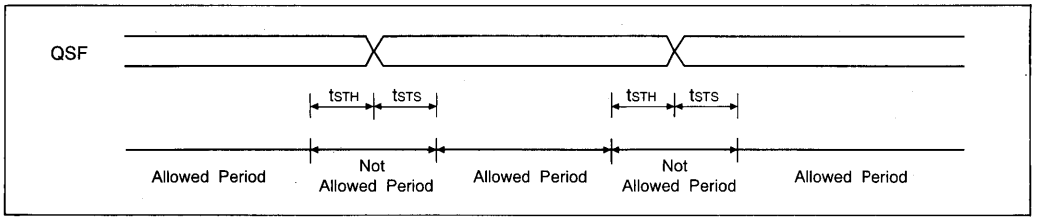


Figure 10. Split Transfer Cycle Limitation Period

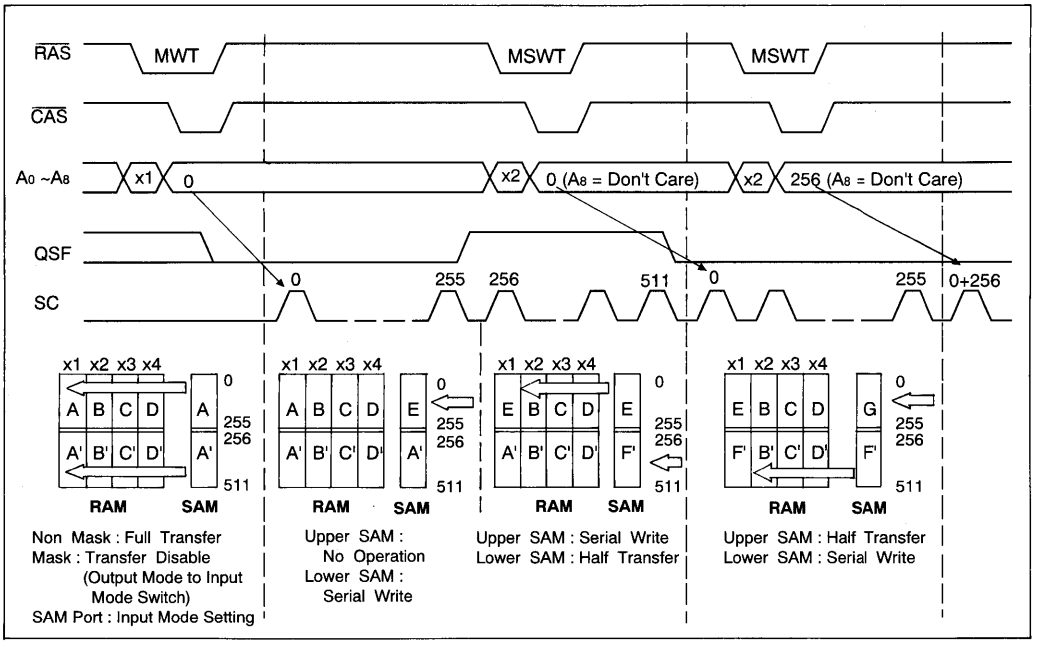


Figure 11. Masked Split Write Transfer Normal Usage

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half. After the last address of each half SAM(255 or 511)is accessed, the access will be changed one half of the SAM to the other half(at the loaded TAP address). This last address is called stop point.

The KM428C/V257 offers user-programmable Stop Point. The stop Points and size of the resulting partitions are shown in Table 3. The stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WB}/\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle

DEVICE OPERATION (Continued)

is done. The Stop Point do not effect to SAM in normal RT, RRT cycle. a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.

In Figure 12. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary(383), the access will jump to the TAP address (70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs or the SAM half boundary(255,511). Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed, To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$. The CBRR will take effect immediately; it does not require a SRT to become active valid.

Table 3. Stop Point Setting Address

Stop Register=Store the Address of Serial Access
Use on the Split Transfer Cycle
Stop Pointer Set → CBRS Cycle

Number of Stop Points /Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3~A_3
1	(1×256)×2	×	1	1	1	1	×
2	(2×128)×2	×	0	1	1	1	×
4	(4×64)×2	×	0	0	1	1	×
8	(8×32)×2	×	0	0	0	1	×
16	(16×16)×2	×	0	0	0	0	×
T	(T×Width)×2	Other Case=Inhibit					

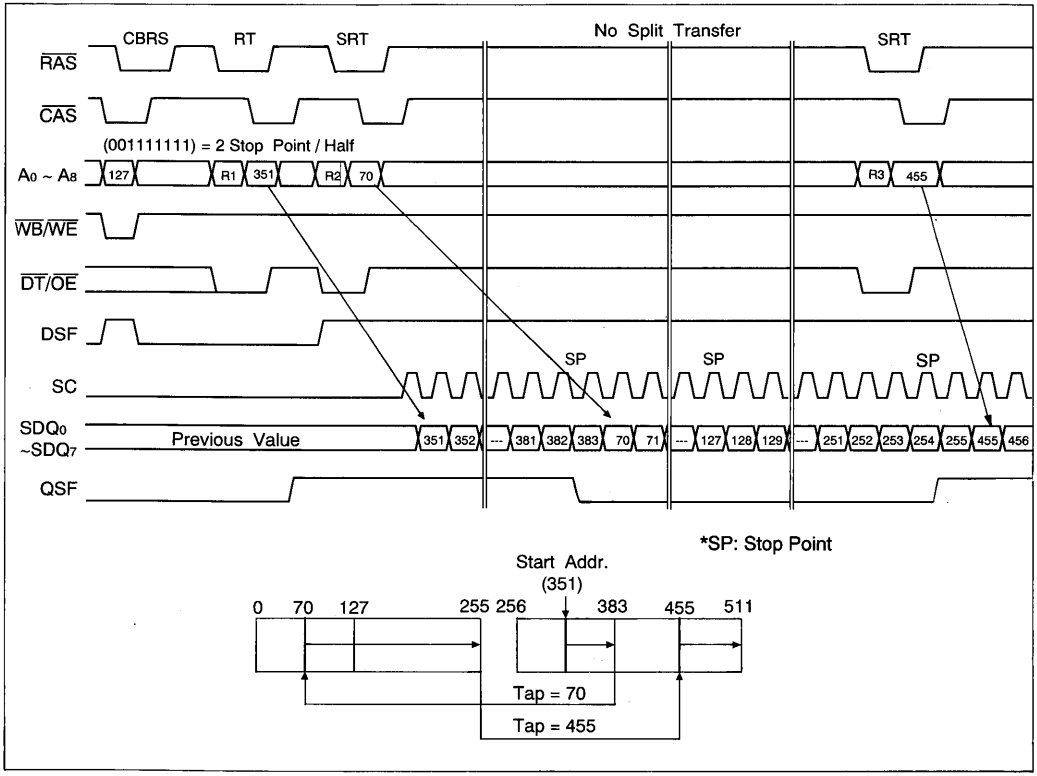
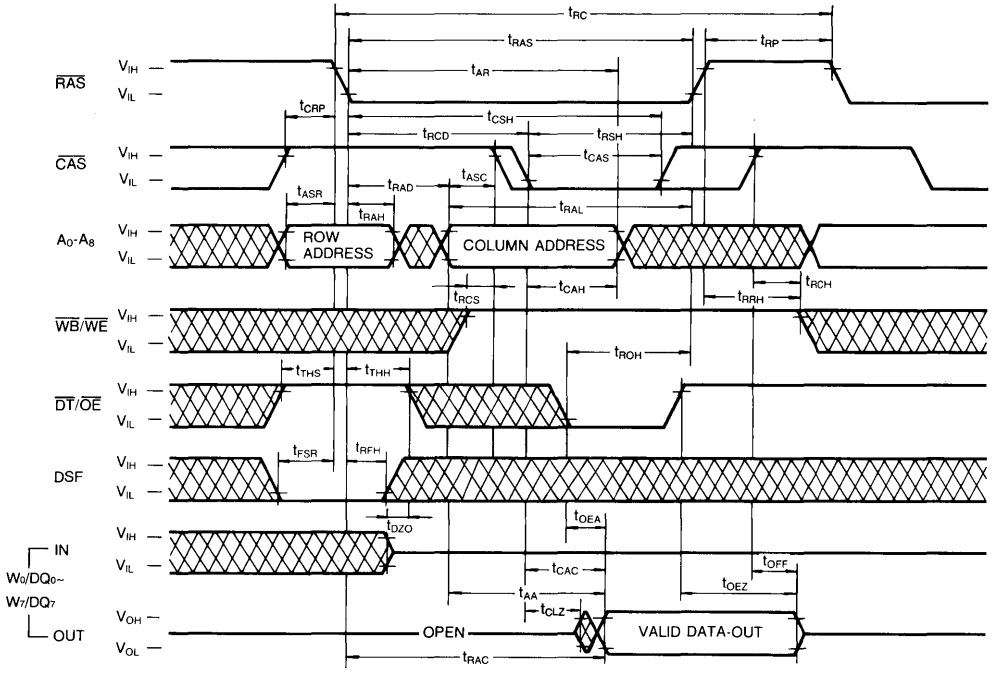


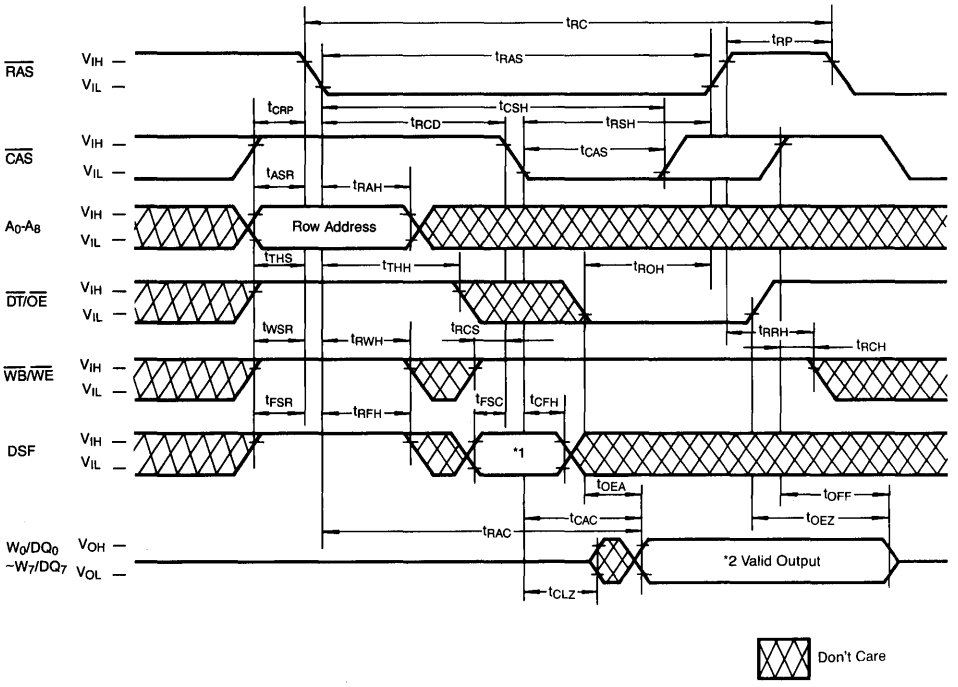
Figure 12. Stop Register Timing

TIMING DIAGRAMS

READ CYCLE

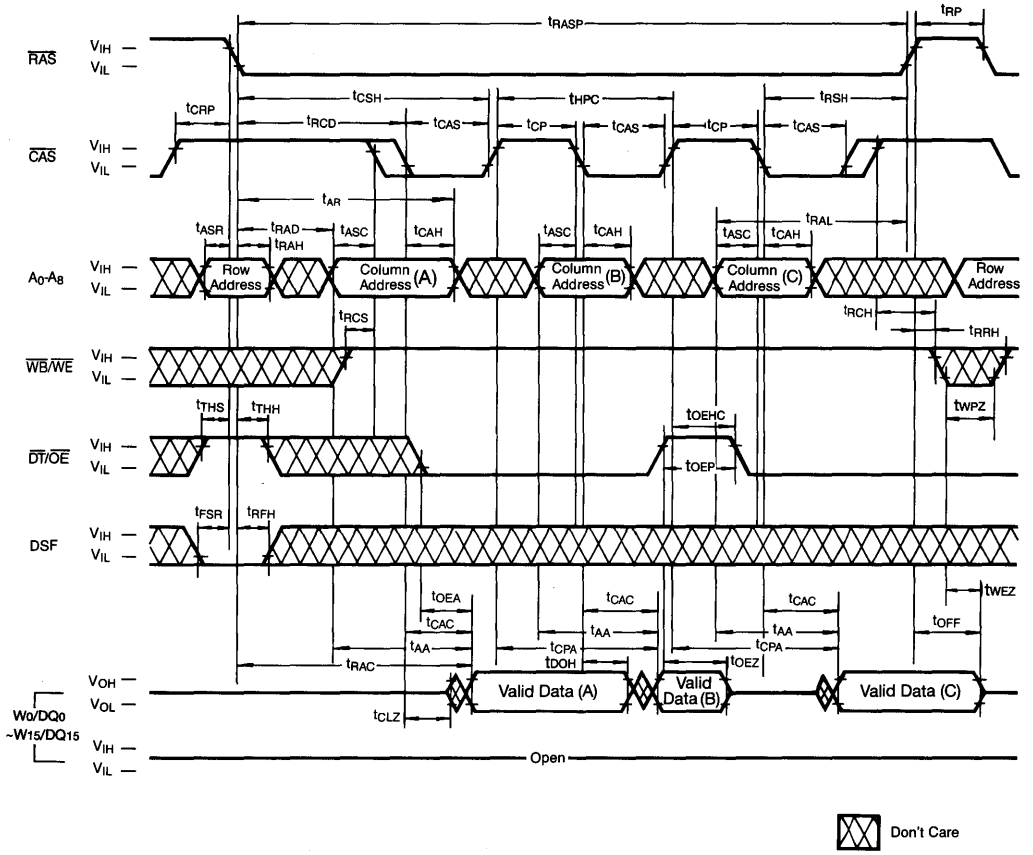


READ MASK/COLOR REGISTER CYCLE



*1	*2	Function
0	Mask data	Read Mask Register Cycle
1	Color data	Read Color Register Cycle

FAST PAGE MODE READ CYCLE (Extended Data Out)



TRUTH TABLE FOR WRITE CYCLE[1]

FUNCTION	RAS ↓			CAS ↓	CAS ↓ or WB/WE ↓
	*1 WB/WE	*2 DSF	*3 Wi/DQi[4] (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)[5]	1	0	×	1	Column Mask
Masked Block Write[5]	0	0	Write Mask	1	Column Mask
Masked Flash Write	0	1	Write Mask	×	×
Load Mask Data Register[2]	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram, on the following page.
(2) Old Mask data load
(3) On the masked flash write cycle. all the signal inputs are don't care condition except RAS at the falling edge of CAS.
(4) Function table for Old Mask and New Mask

IF		*1 WB/WB	*3 Wi/DQi	Note
LMR Cycle Executed	Yes	0	×	Write using mask register data (Old Mask Data)
		1	×	Non Masked Write
	No	0	Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	×	Non Masked Write

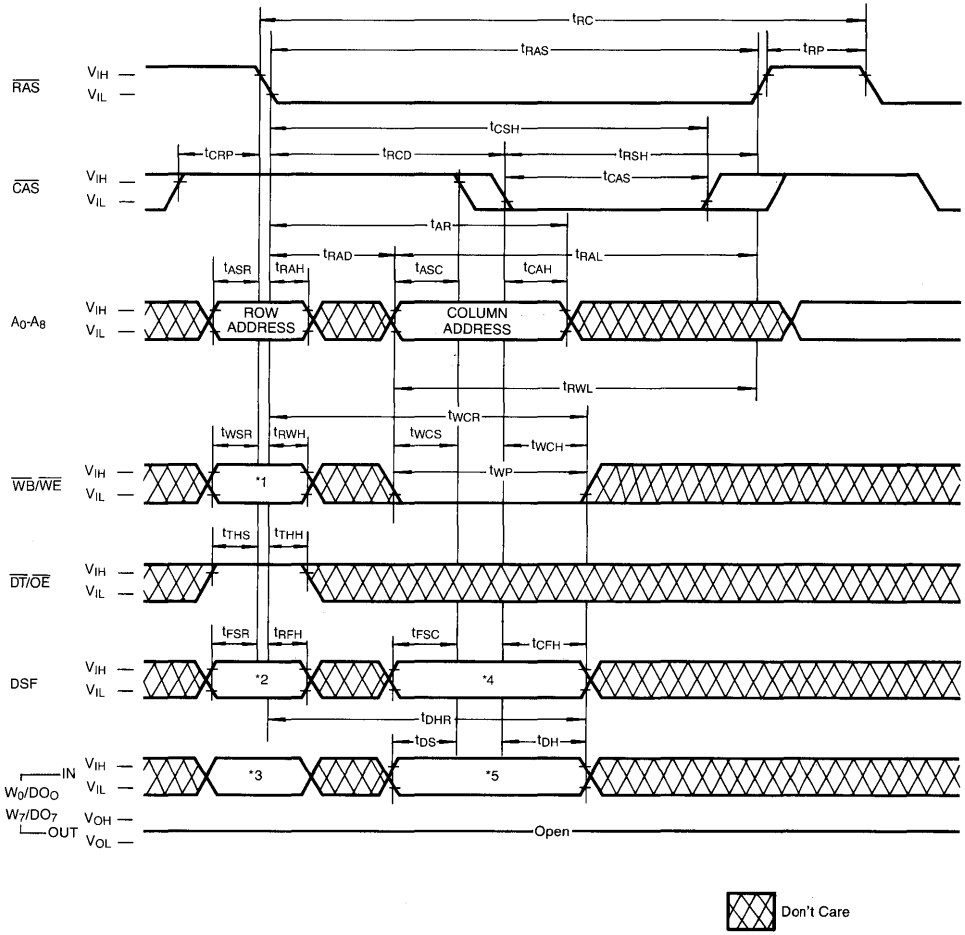
× : Don't Care

(5) Function Table for Block Write Column Mask

Column Address	
A1	A0
0	0
0	1
1	0
1	1

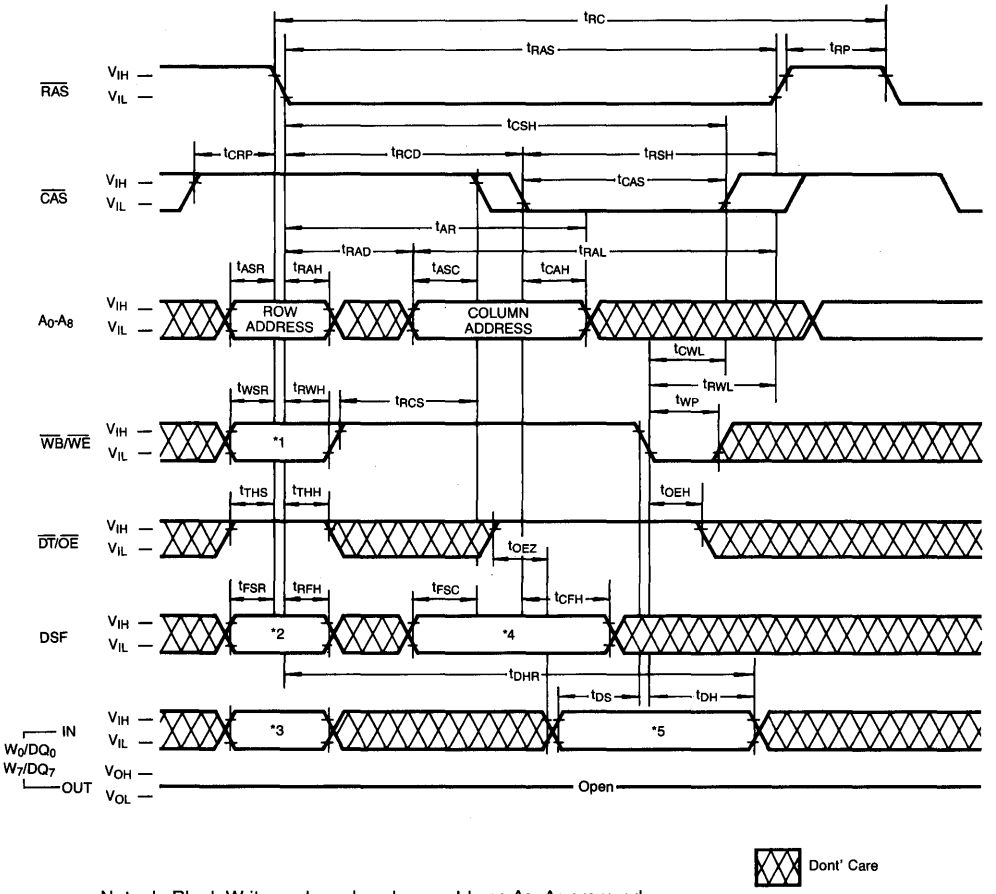
*5	IF	
Wi/DQi	Wi/DQi=0	Wi/DQi=1
W0/DQ0	No Change the Internal Data	Color Register Data Are Write to the Corresponding Column Address Location
W1/DQ1		
W2/DQ2		
W3/DQ3		

EARLY WRITE CYCLE



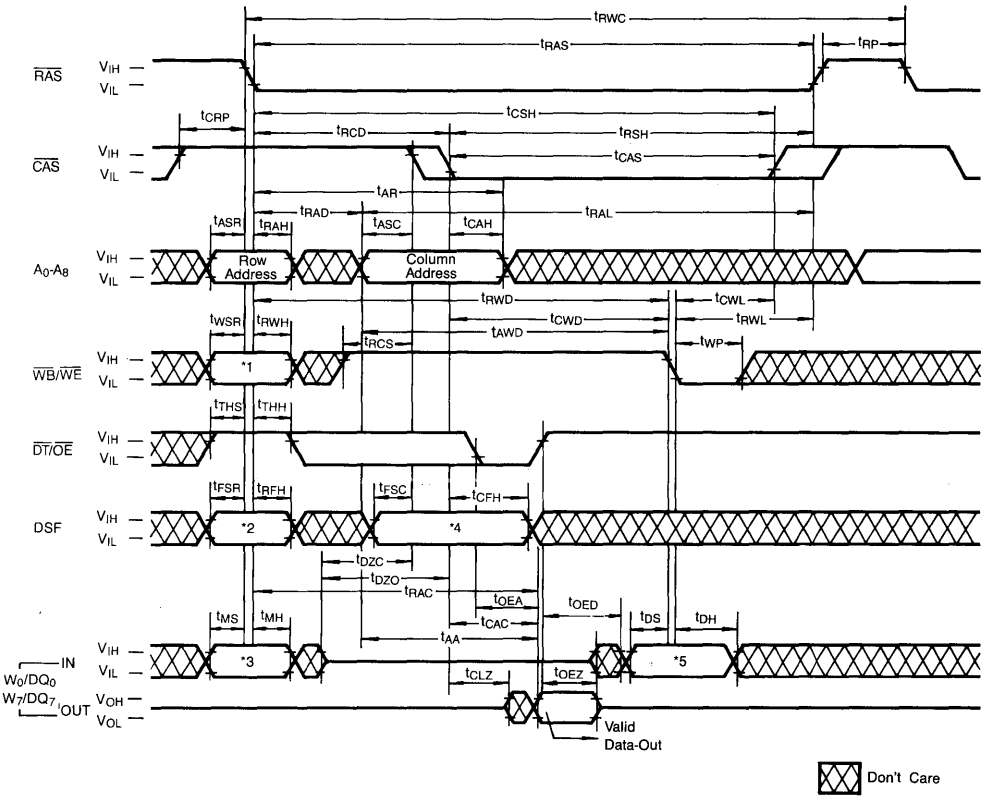
Note: In Block Write cycle, only column address A2~A8 are used.

LATE WRITE CYCLE



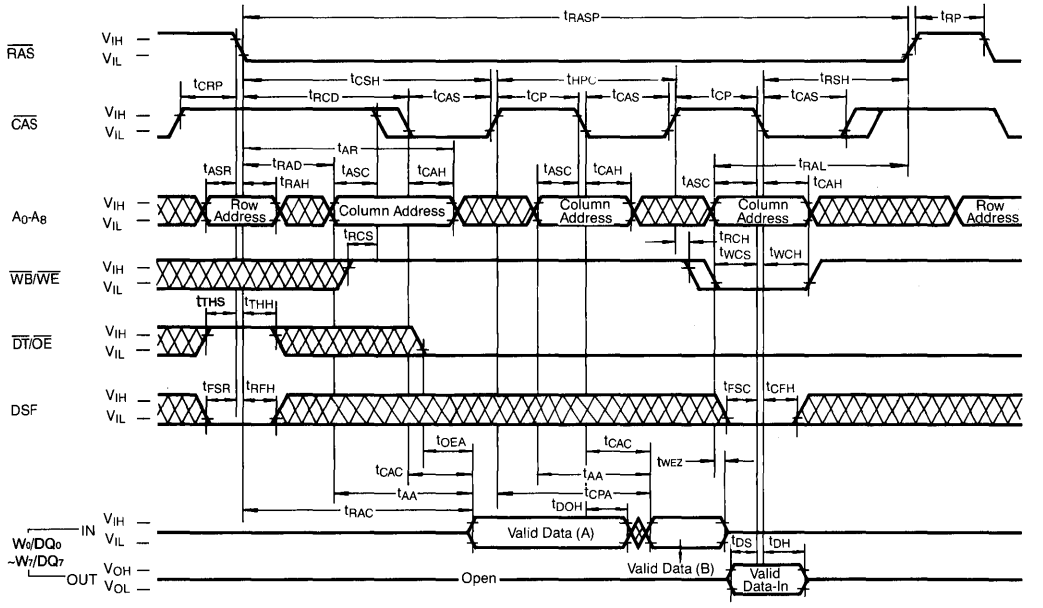
Note: In Block Write cycle, only column address A_2~A_8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE

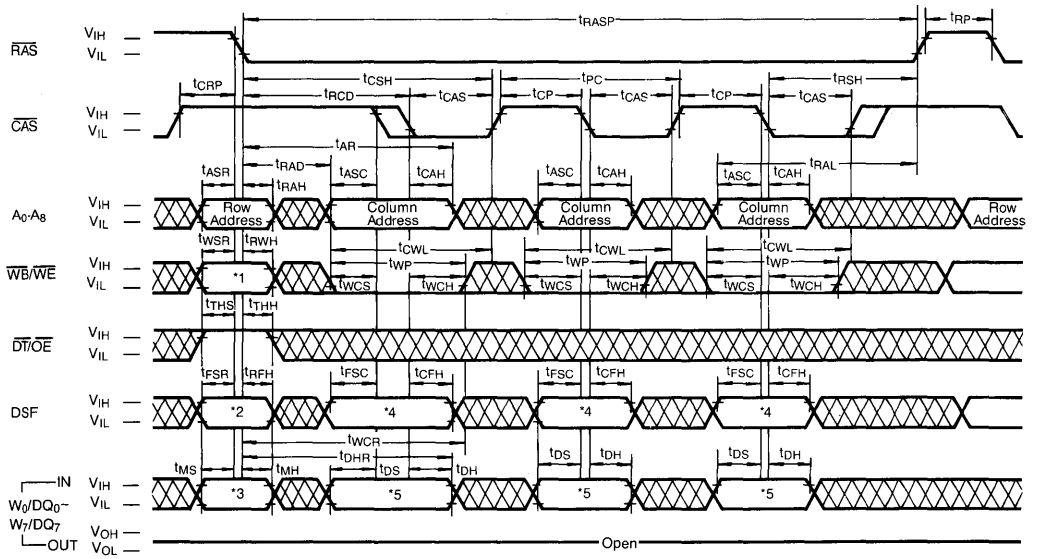


Note: In Block Write cycle, only column address A_2~A_8 are used.

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

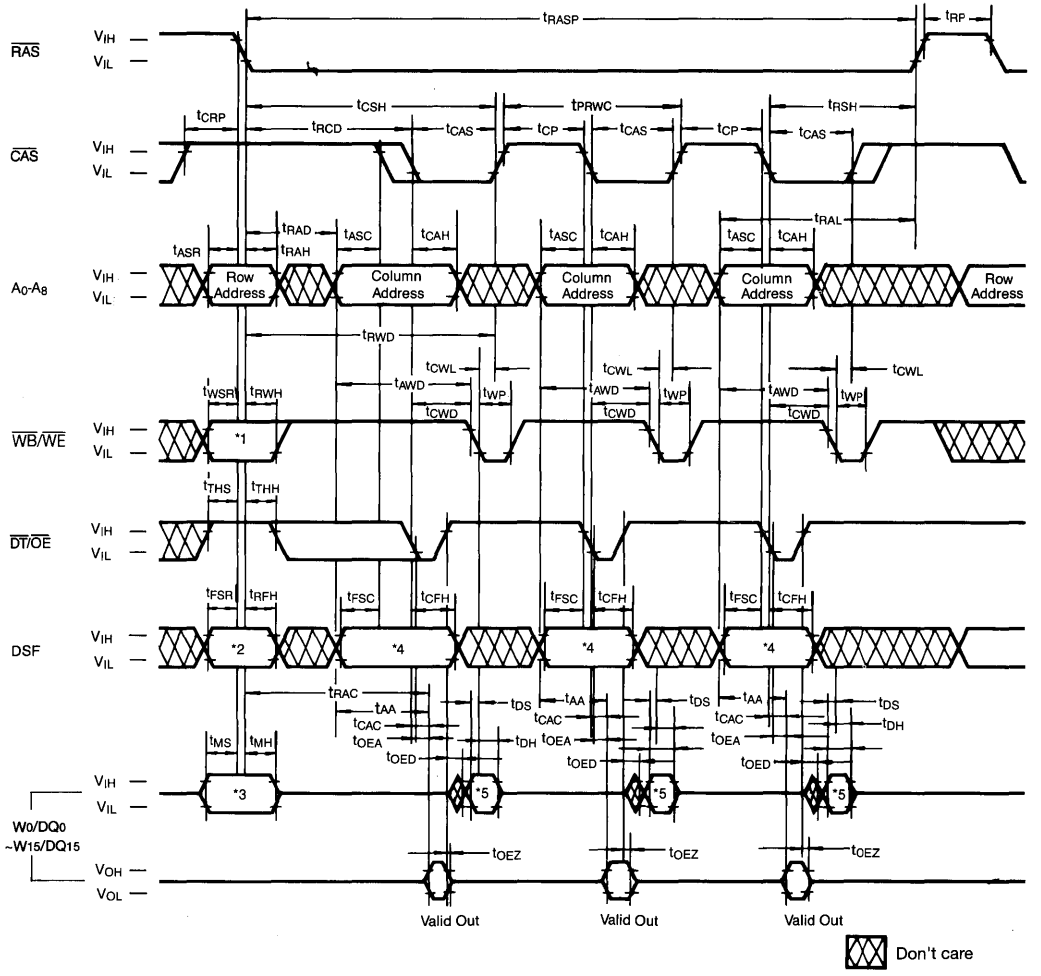


FAST PAGE MODE EARLY WRITE CYCLE



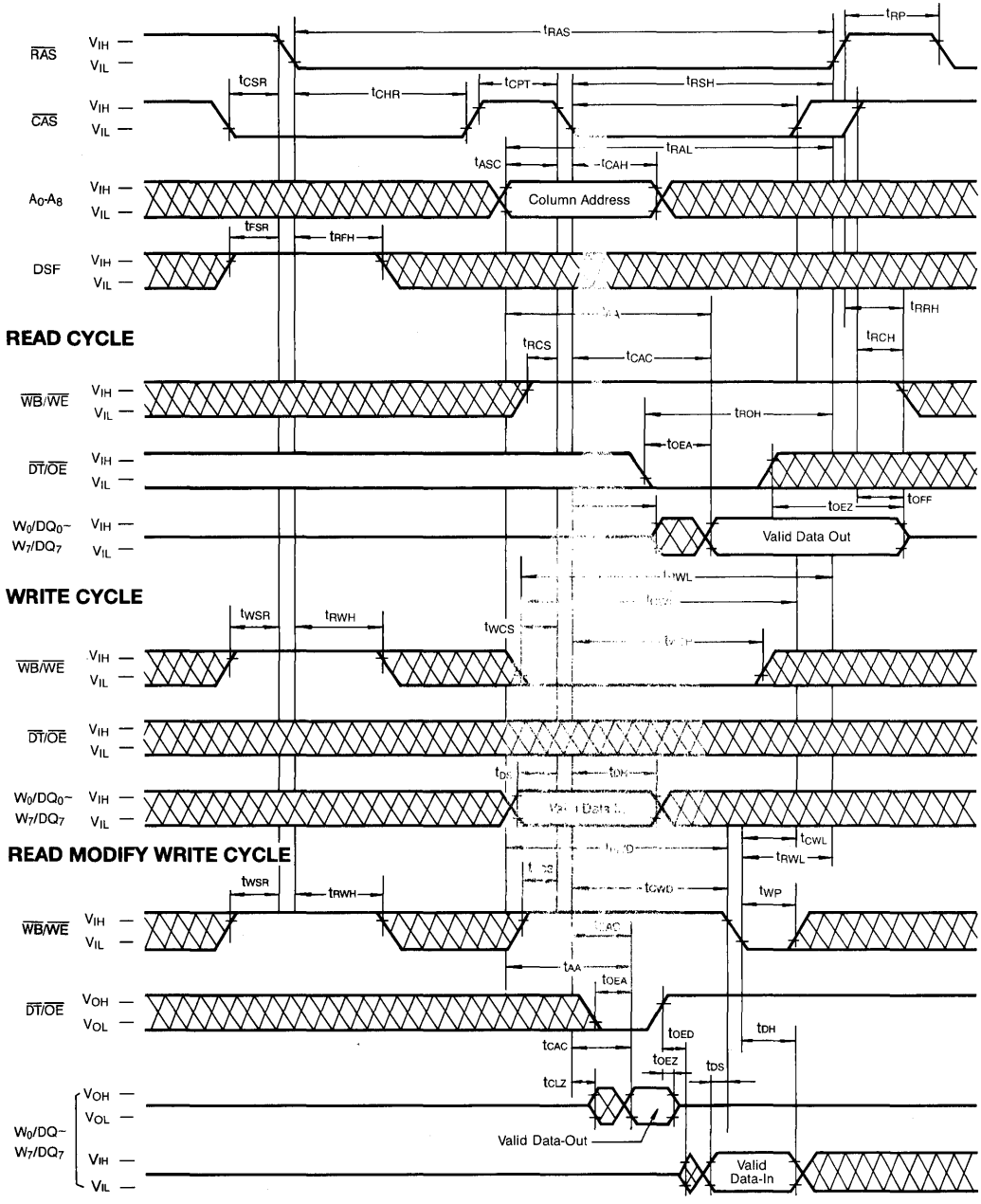
Note: In Block Write cycle, only column address A2~A8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

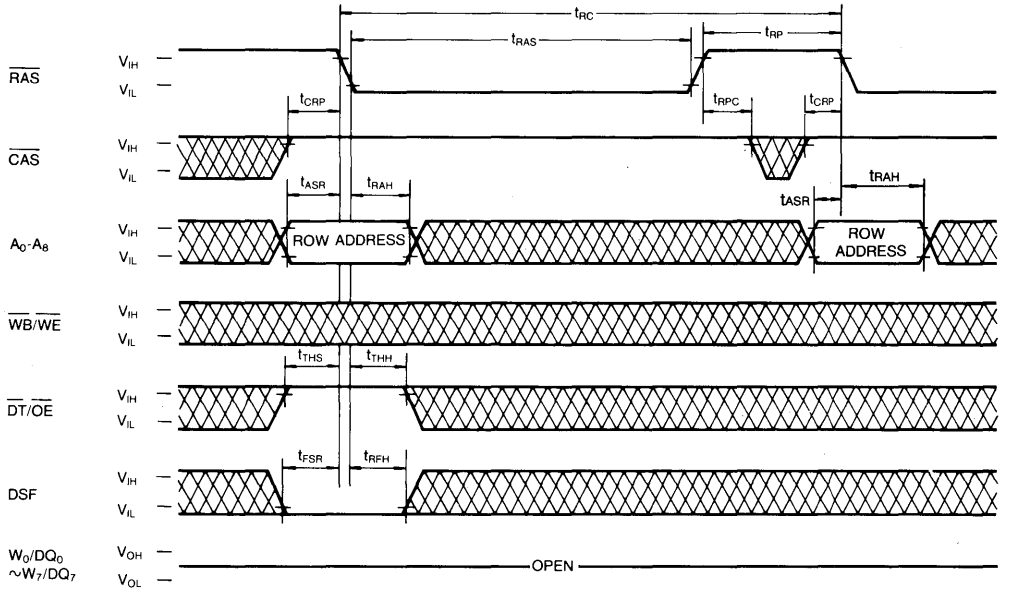


Note : In Block write cycle, only column address A3~A8 are used.

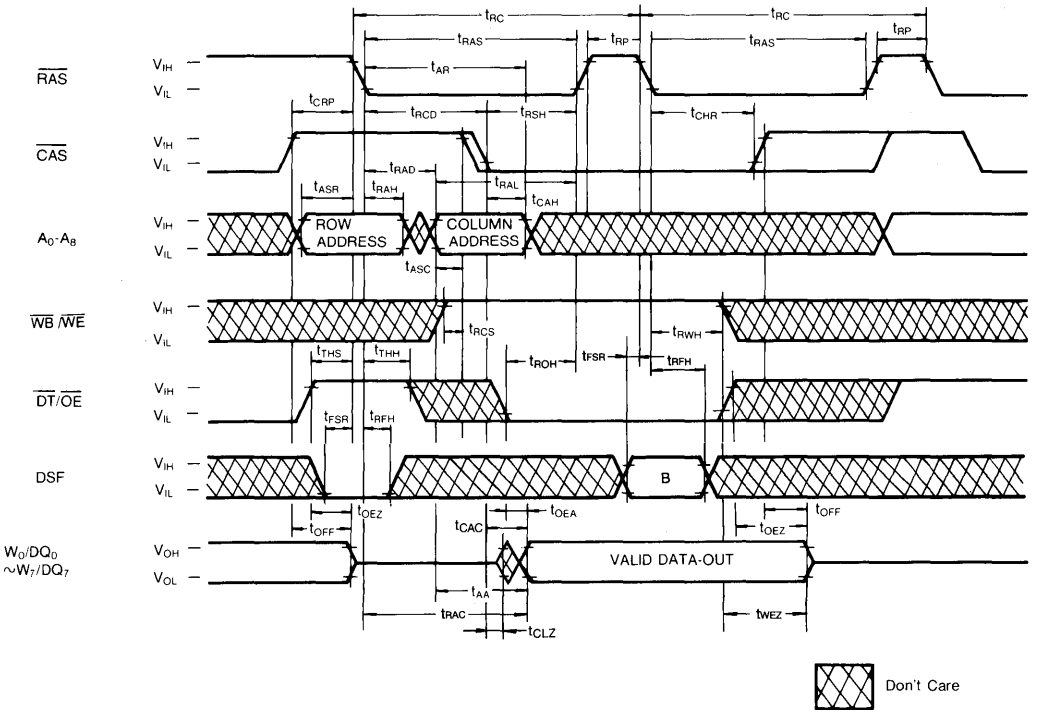
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



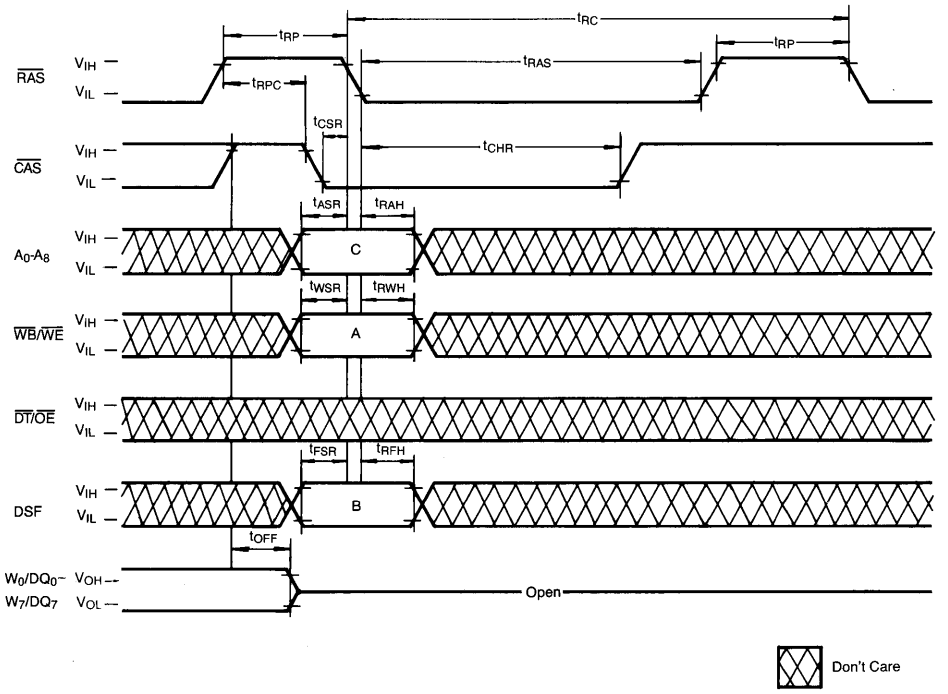
HIDDEN REFRESH CYCLE



HIDDEN REFRESH CYCLE FUNCTION TABLE

FUNCTION	Logic Status B
Hidden Refresh(Reset All Options)	0
Hidden Refresh(No Reset)	1

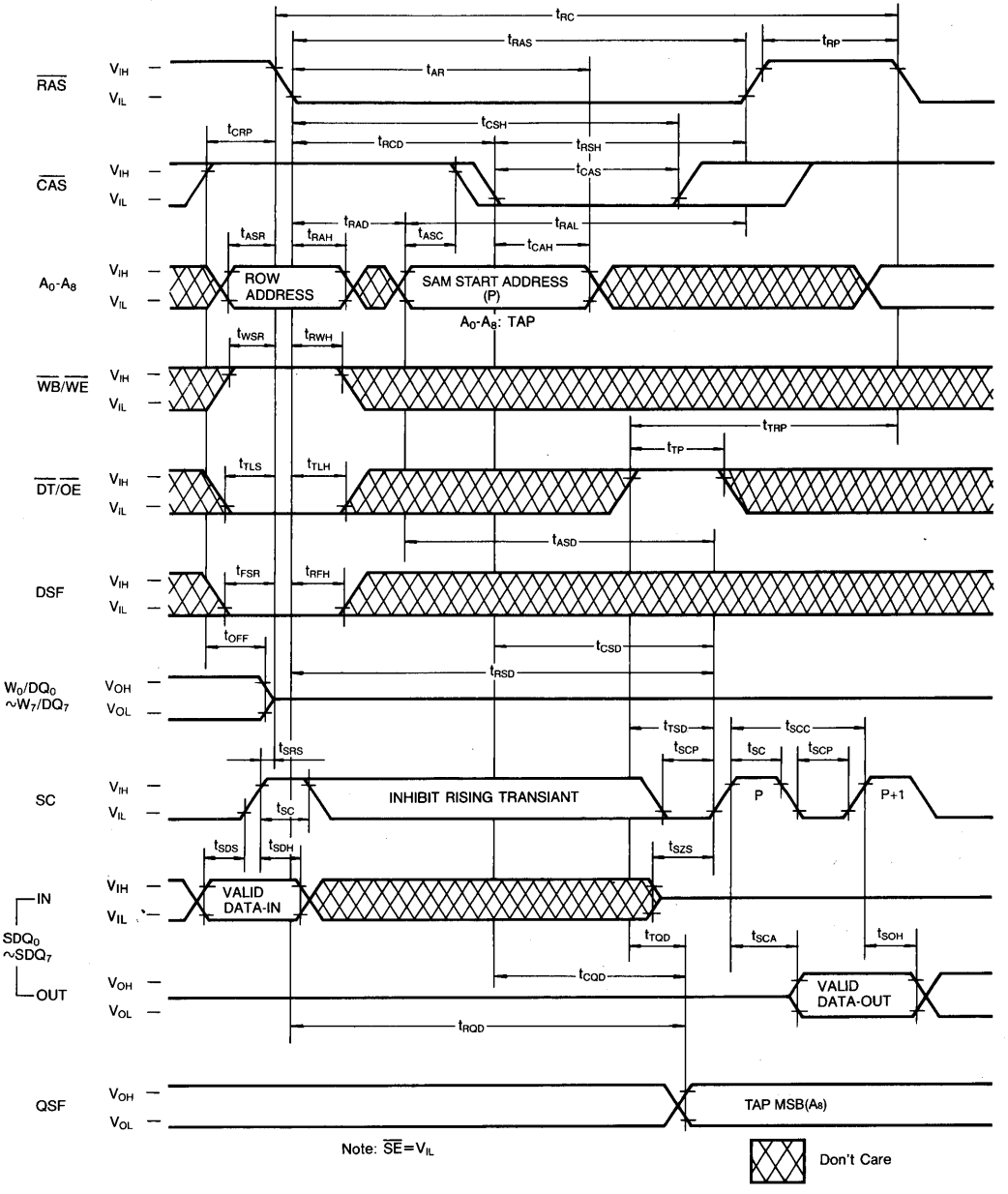
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



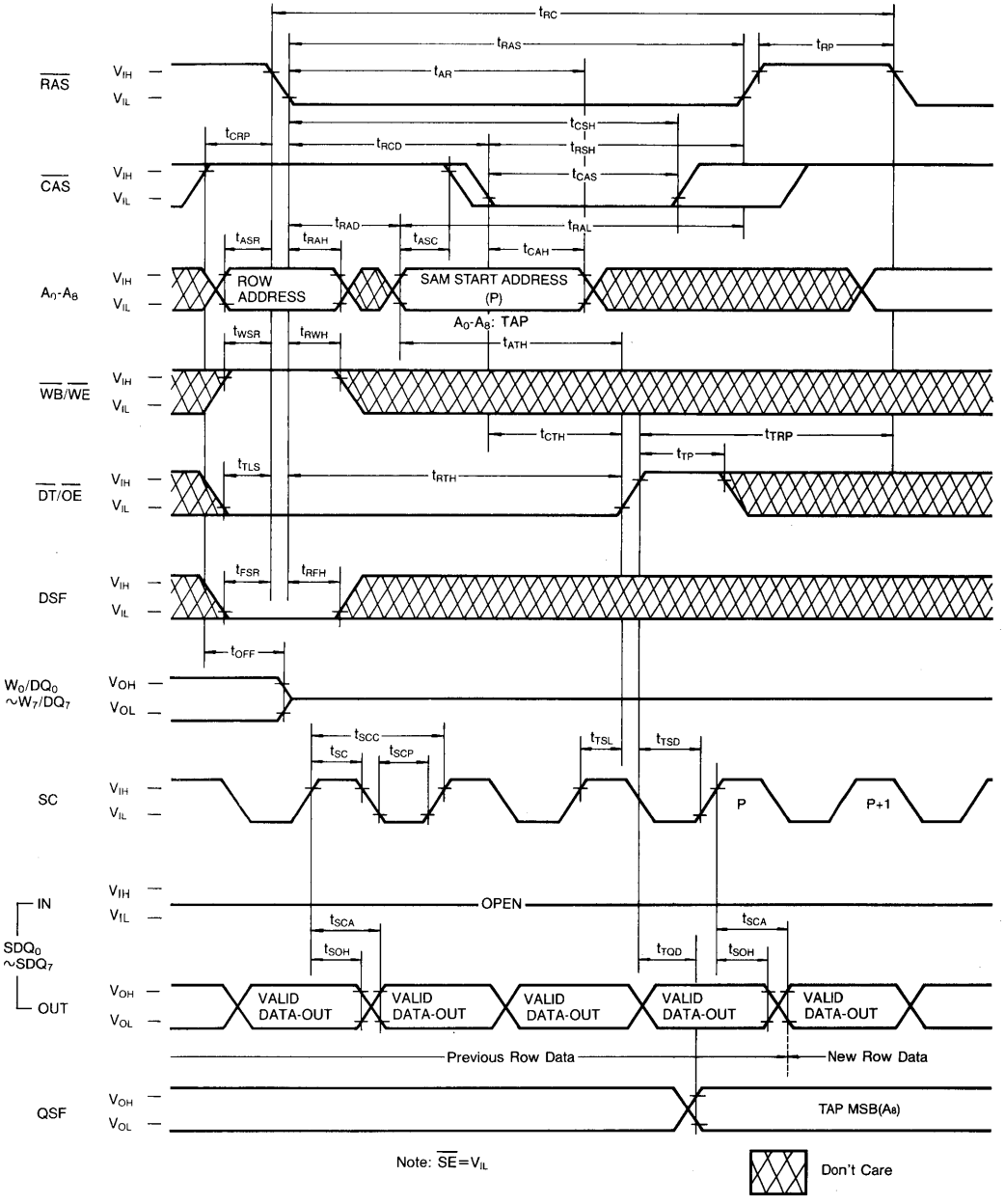
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	Stop Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

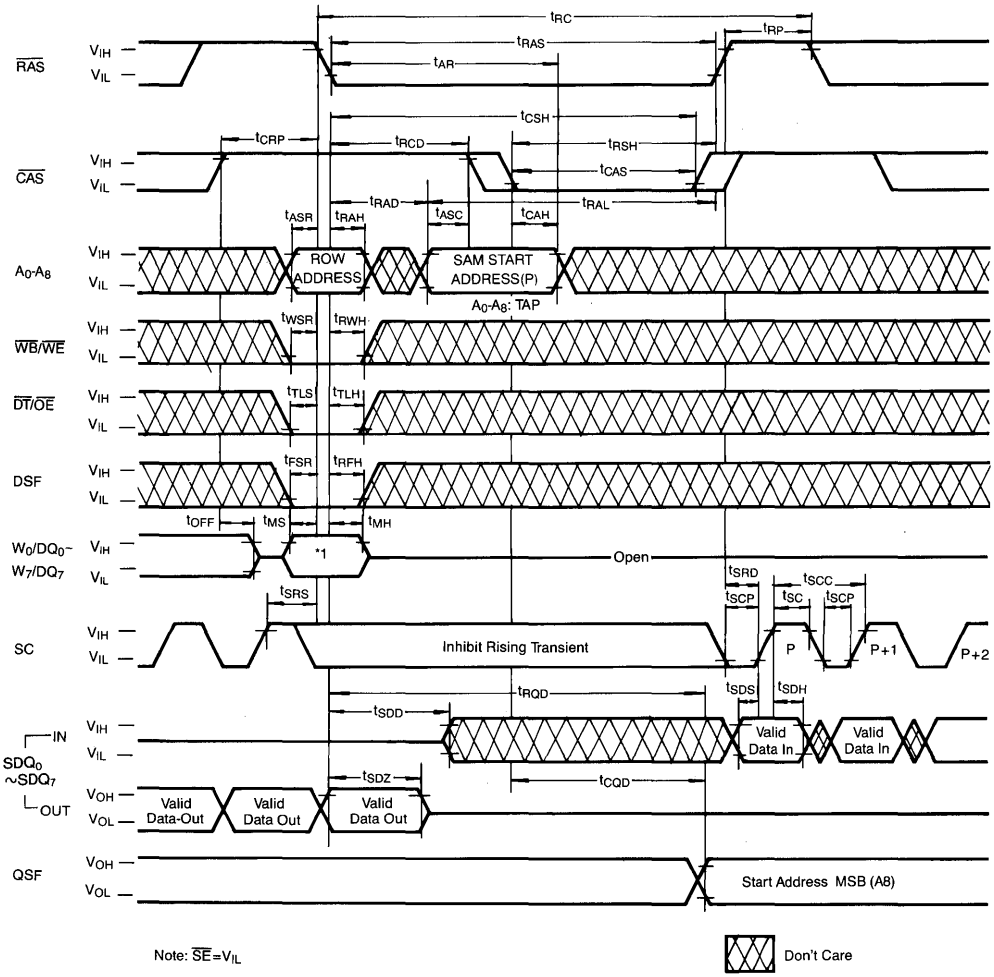
READ TRANSFER CYCLE



REAL TIME READ TRANSFER CYCLE



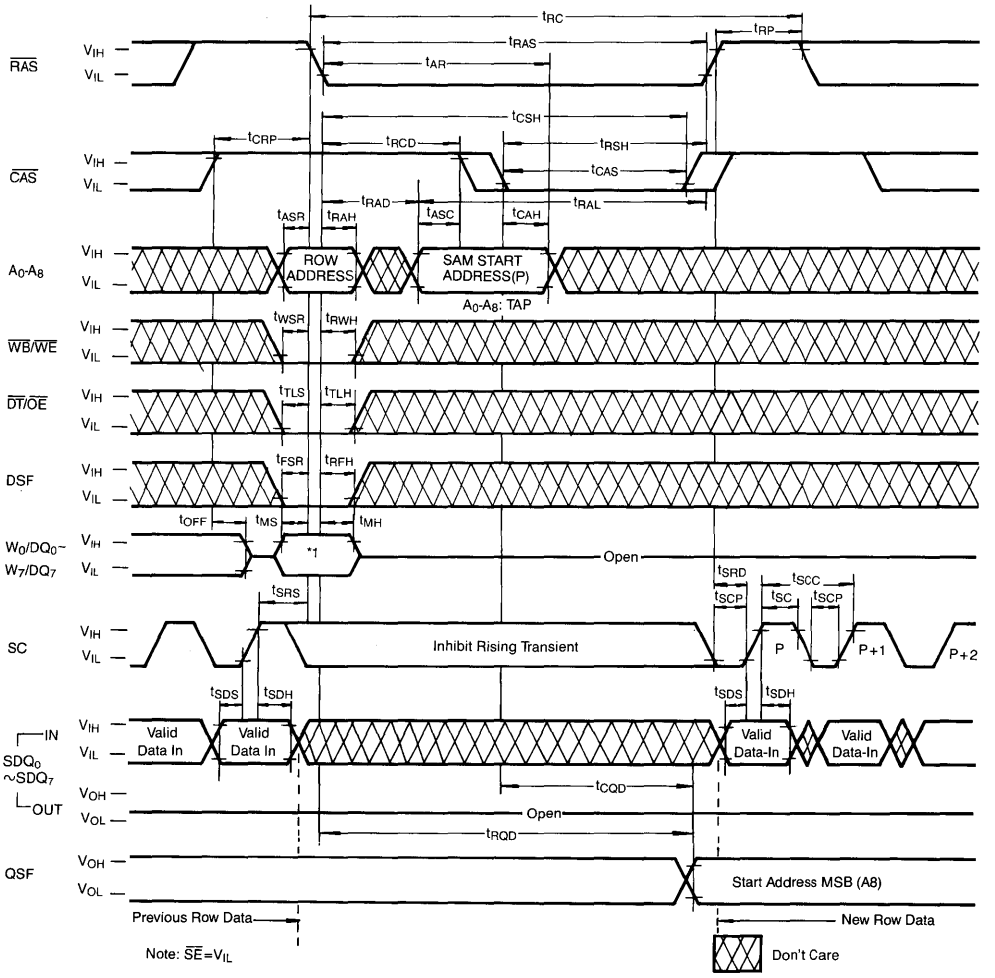
MASKED WRITE TRANSFER CYCLE (Output Mode to Input Mode Switch)



Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data 0: Transfer Disable
1: Transfer Enable

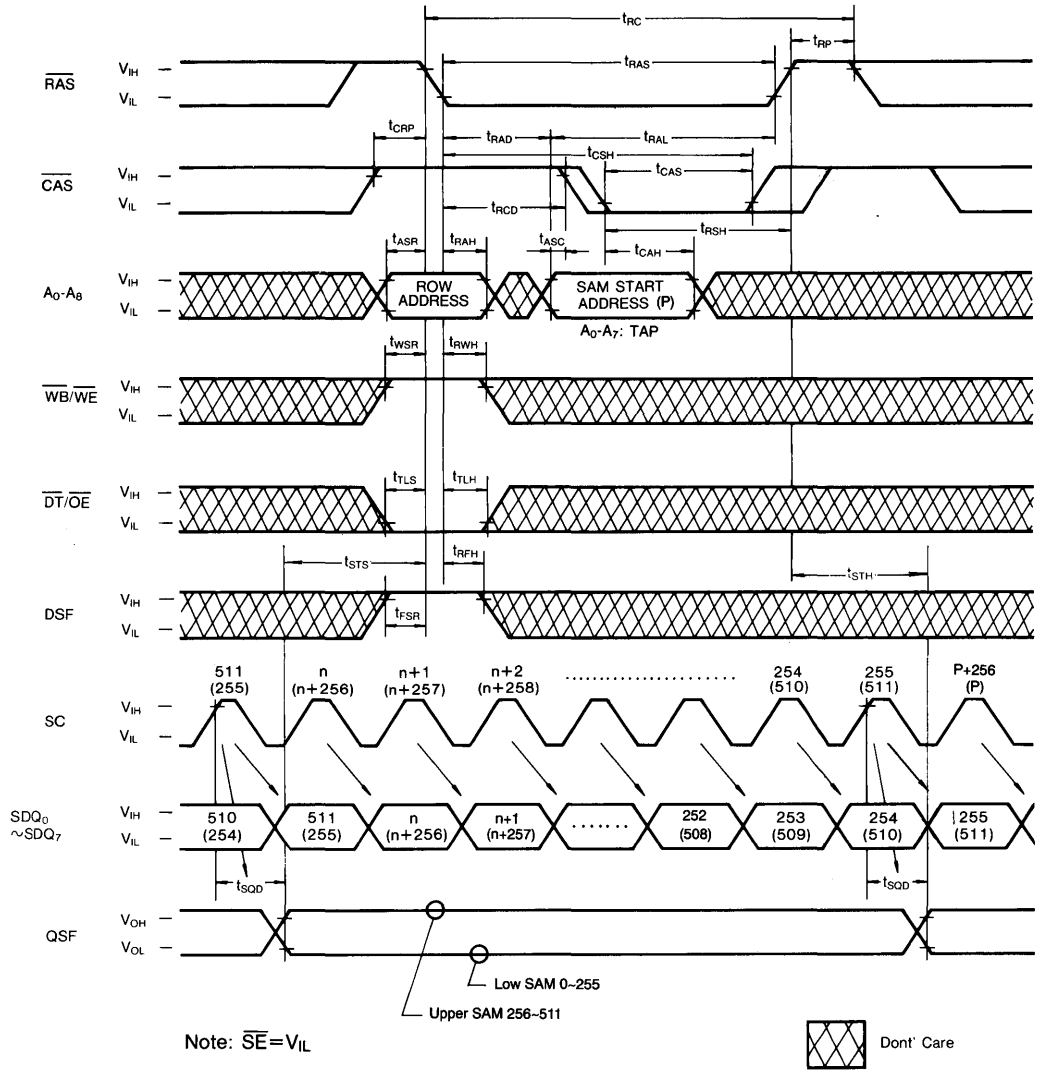
MASKED WRITE TRANSFER CYCLE



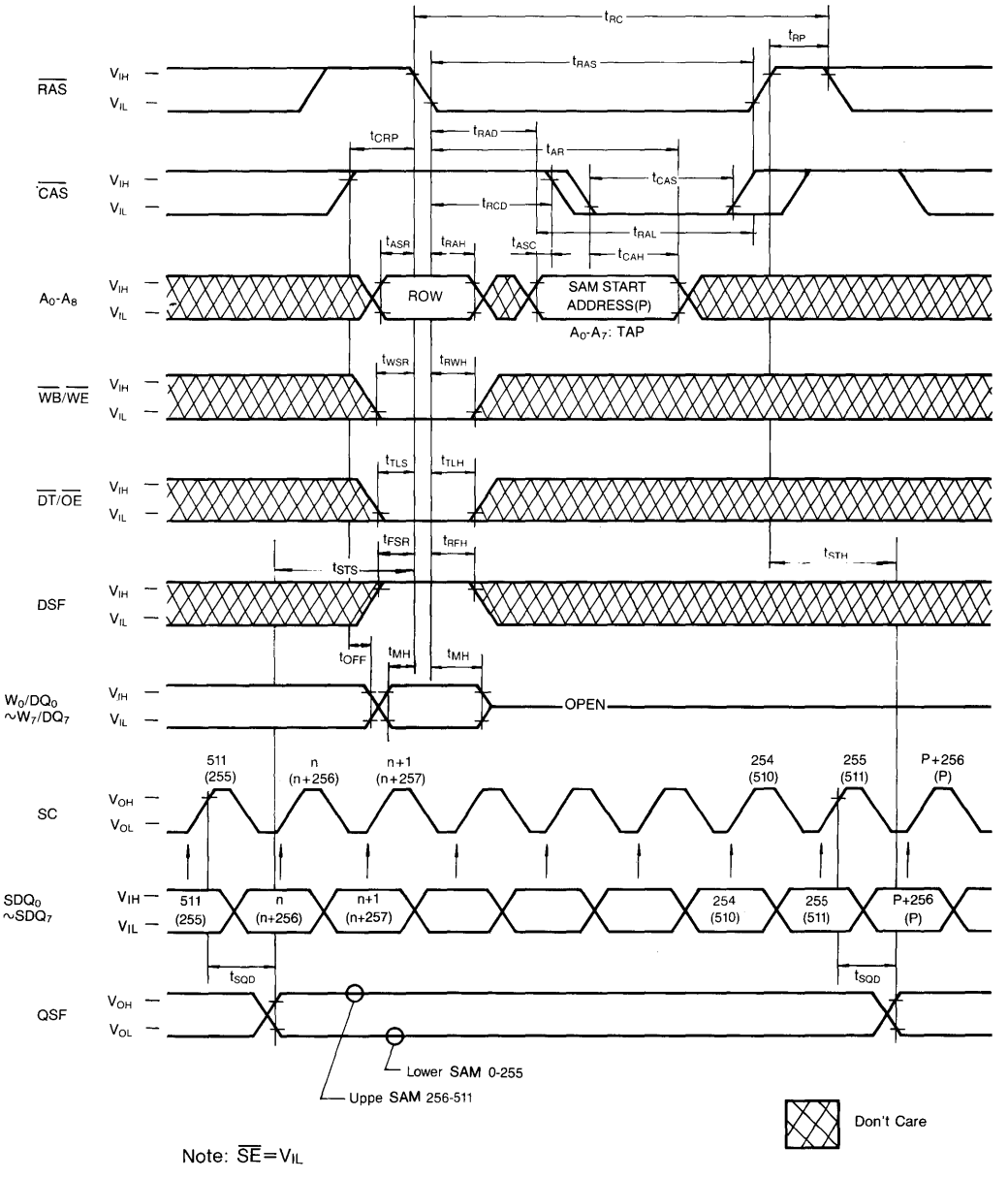
Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data 0 : Transfer Disable
1: Transfer Enable

SPLIT READ TRANSFER CYCLE

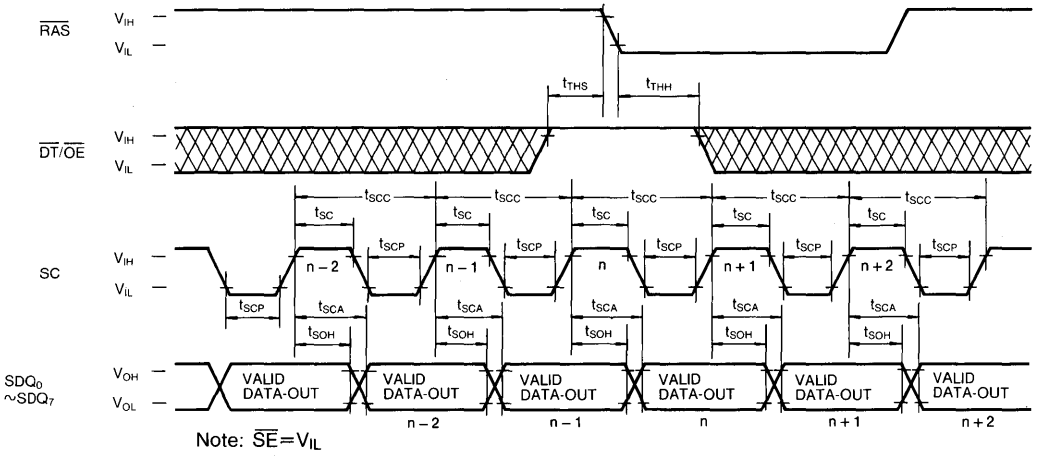


MASKED SPLIT WRITE TRANSFER CYCLE



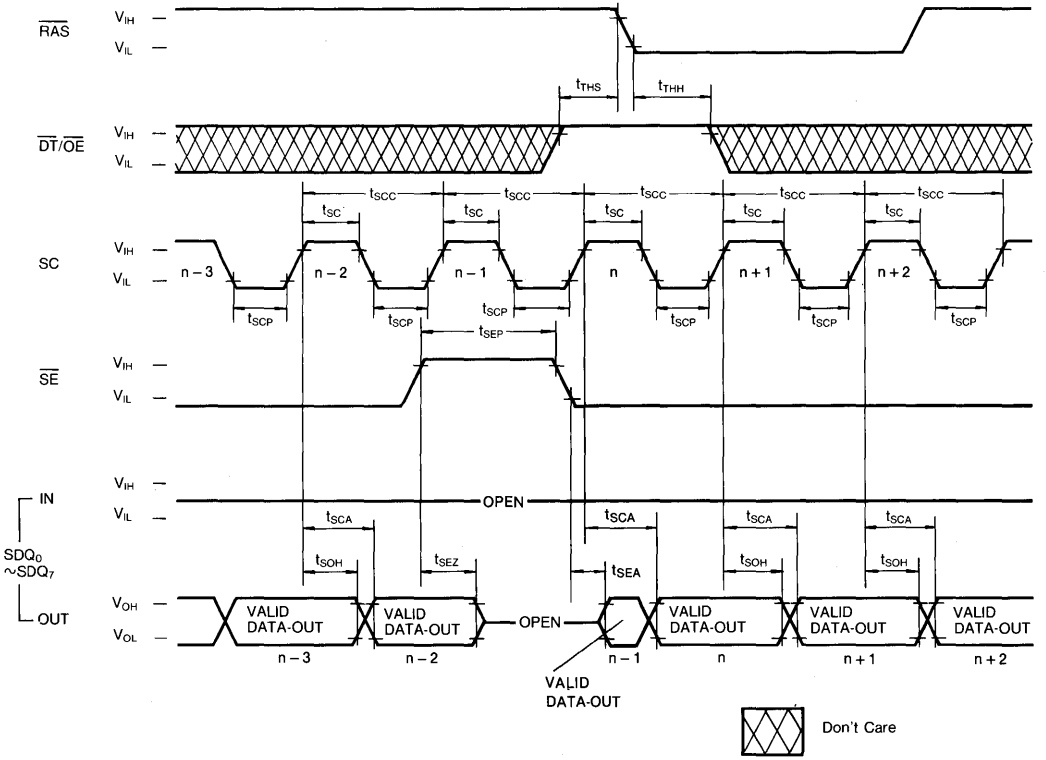
Note: $\overline{SE}=V_{IL}$

SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

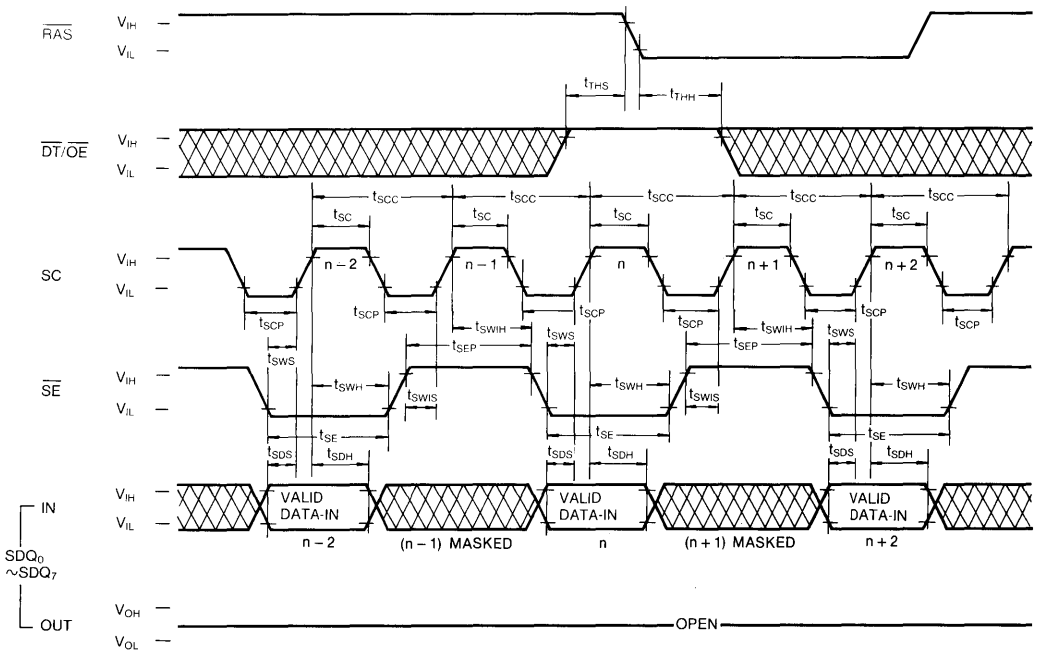


Note: $\overline{SE}$=V_{IL}

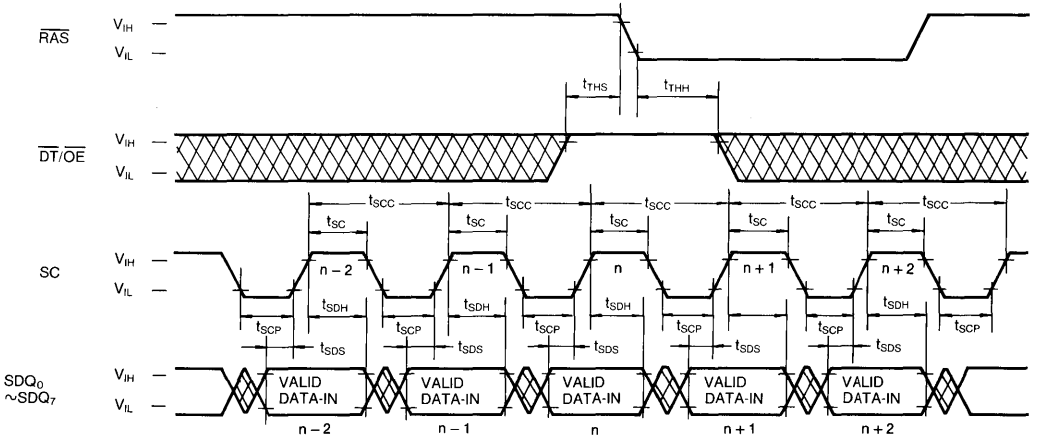
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



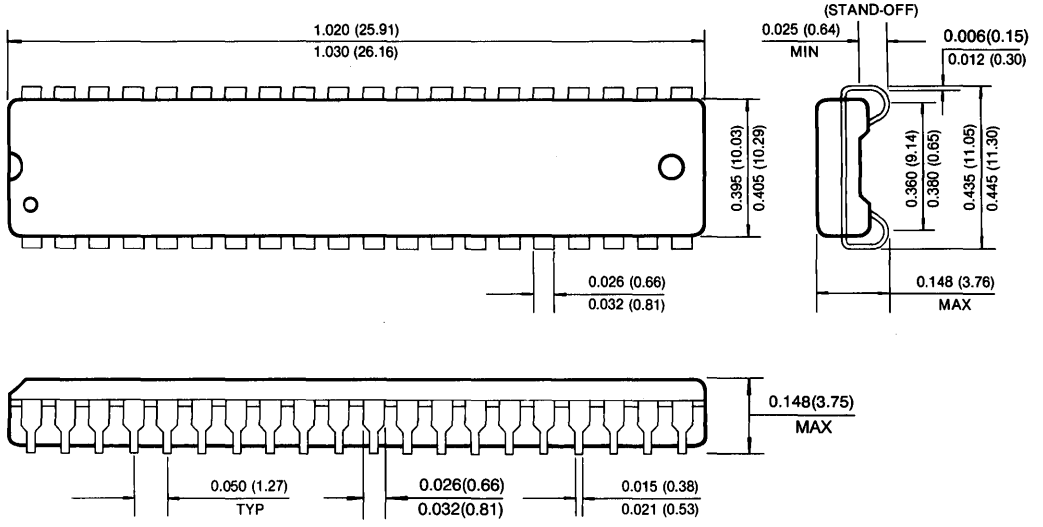
Note: $\overline{SE}$=V_{IL}

Don't Care

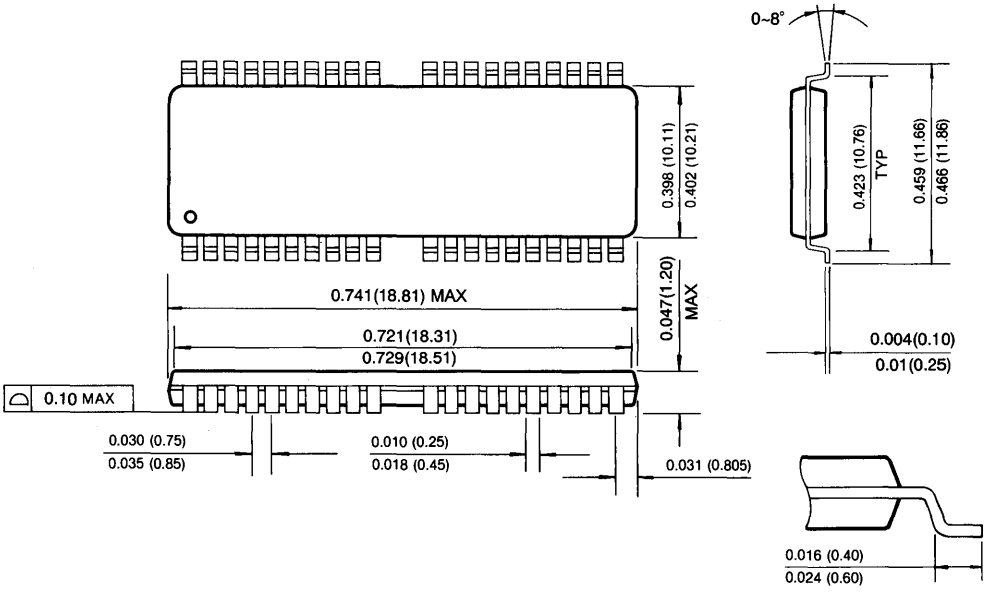
PACKAGE DIMENSIONS

40-PIN PLASTIC SOJ

Units: Inches (millimeters)



40/44-PIN PLASTIC TSOP-II (Forward Type)



256K X 8 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K x 8 bits RAM port
  512 x 8 bits SAM port
- **Performance range :**

Parameter \ Speed		-6	-7	-8
RAM access time(t_{RAC})		60ns	70ns	80ns
RAM access time(t_{CAC})		15ns	20ns	20ns
RAM cycle time(t_{RC})		110ns	130ns	150ns
RAM page mode cycle(t_{PC})		30ns	35ns	40ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time(t_{SCC})		18ns	22ns	25ns
SAM active current	KM428C258	110mA	100mA	90mA
	KM428V258	—	60mA	55mA
SAM active current	KM428C258	55mA	50mA	45mA
	KM428V258	—	30mA	25mA

- **Fast Page Mode with Extended Data Out**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR) and Serial Write (SW)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **Write and Split Write Transfer with Stop Register (New and Old Mask), (WT,SWT)**
- **Nibble Write Operation**
- **Block Write (BW), Flash Write (FLW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single +5V± 10% Supply Voltage**
- **Single +3.3V±10% Supply Voltage**
- **Low Vcc (3.3V) Part Name: KM428V258**
- **KM428C258: 60, 70, 80ns**
- **KM428V258: 70, 80ns**
- **Plastic 40-Pin 400mil SOJ**
- **Plastic 40/44Pin 400mil TSOP II (Forward and Reverse Type)**

GENERAL DESCRIPTION

The Samsung KM428C/V258 is a CMOS 256K×8 bit Dual Port DRAM. It consists of a 256K×8 dynamic random access memory(RAM) port and 512×8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 4096 bits. It operates like a conventional 256K x 8 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Block Write and Flash Write capability. Nibble write control can be applied in write, Block Write, Flash Write, Load Mask Register and Load Color Register cycles.

The SAM port consists of eight 512 bit high speed shift registers that are connected to the RAM array through a 4096 bit data transfer gate. The SAM port has serial read and write capabilities.

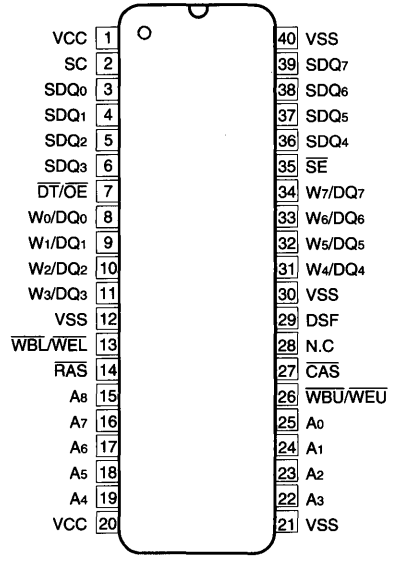
Data may be internally transferred bi-directionally between the RAM and SAM ports using read, write and programmable (Stop Register) Split Transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C/V258 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

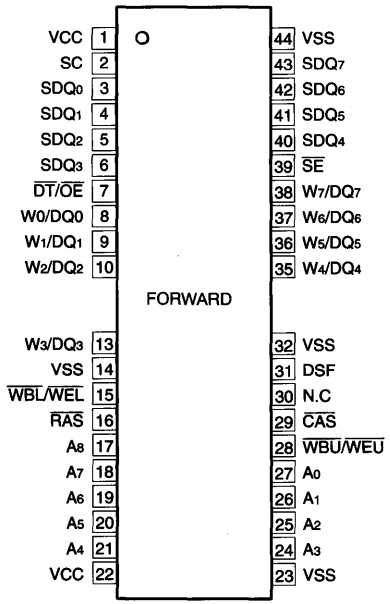
All inputs and I/O's are TTL level compatible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (TOP VIEWS)

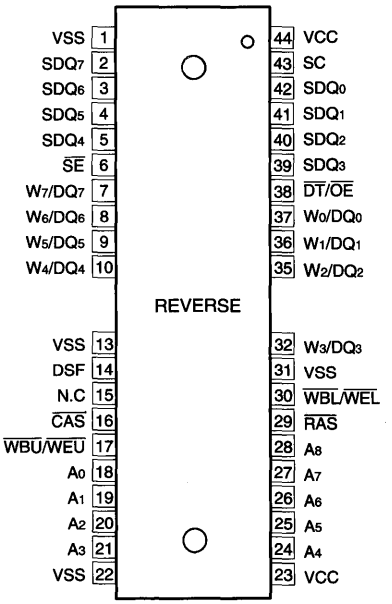
40 Pin 400 mil SOJ



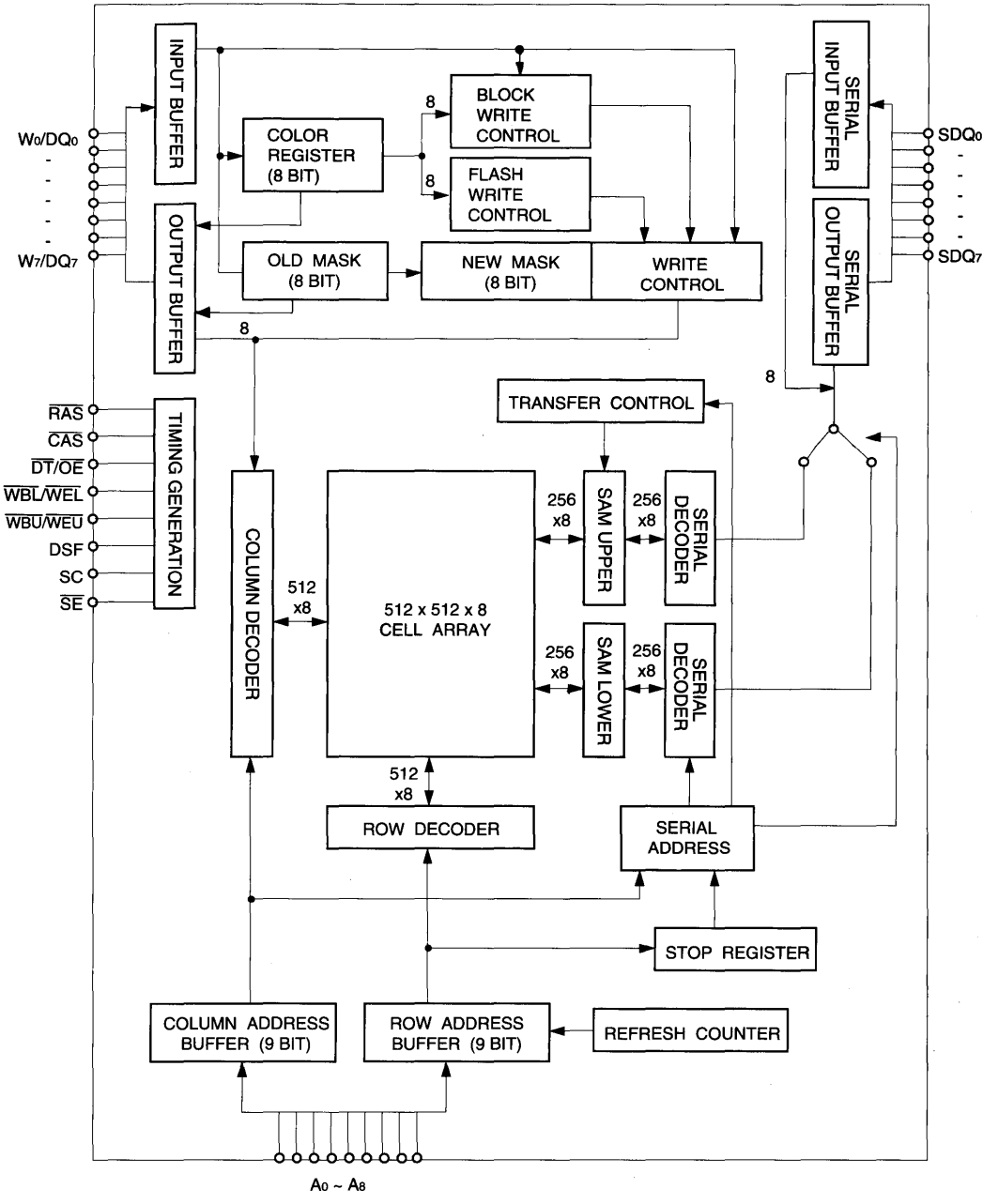
40/44 Pin 400 mil TSOP II



40/44 Pin 400 mil TSOP II



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Type	Description
$\overline{RAS}$	IN	Row Address Strobe. $\overline{RAS}$ is used to clock in the 9 row bits for another input signal. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High"
$\overline{CAS}$	IN	Column Address Strobe. $\overline{CAS}$ is used to clock in the 9 column address bits as a strobe for the DSF inputs
ADDRESS	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe($\overline{CAS}$).
$\overline{WBL}/\overline{WEL}$, $\overline{WBU}/\overline{WEU}$ (Lower /Upper)	IN	The $\overline{WBL}/\overline{WEL}$ input is a multifunction pin. when $\overline{WBX}/\overline{WEX}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WBX}/\overline{WEX}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions(BW, FW, Split Transfer, etc)are used for a particular access cycle.
Wi/DQi	IN/OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
$\overline{SE}$	IN	In a serial read cycle. $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
Vcc	SUPPLY	Power supply
Vss	SUPPLY	Ground

FUNCTION TRUTH TABLE

Mnemonic Code	RAS				CAS	Address		DQi Input		Write Mask	Register		Function
	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE		Mask	Color	
CBRS (Note 1,3)	0	X	0	1	–	Stop (note4)	–	X	–	–	–	–	CBR Refresh/Stop (Register set)
CBRN (Note 1)	0	X	1	1	–	X	–	X	–	–	–	–	CBR Refresh (No reset)
CBRR (Note 1)	0	X	X	0	–	X	–	X	–	–	–	–	CBR Refresh (Option reset)
ROR	1	1	X	0	–	Row	–	X	–	–	–	–	RAS Only Refresh
MWT	1	0	0	0	X	Row	Tap	WMI	–	Yes	Use	–	Masked Write Transfer (New/Old)
MSWT	1	0	0	1	X	Row	Tap	WMI	–	Yes	Use	–	Masked Split Write Transfer(New/Old)
RT	1	0	1	0	X	Row	Tap	–	–	–	–	–	Read Transfer
SRT	1	0	1	1	X	Row	Tap	–	–	–	–	–	Split Read Transfer
RWM	1	1	0	0	0	Row	Col.	WMI	Data	Yes	Use	–	Read Write (New/Old Mask)
BWM	1	1	0	0	1	Row	Col. Mask	WMI	Col.	Yes	Use	Use	Block Write (New/Old Mask)
FWM	1	1	0	1	X	Row	X	WMI	X	Yes	Use	Use	Flash Write(New/Old mask)
RW	1	1	1	0	0	Row	Col.	X	Data	No	–	–	Read Write (No Mask)
BW	1	1	1	0	1	Row	Col.	X	Col. Mask	No	–	Use	Block Write (No Mask)
LMR (Note 2)	1	1	1	1	0	Row (note6)	X	X	WMi	–	Load (Note5)	–	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	Row (note6)	X	X	Color	–	–	Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap: SAM Start (column) Address, WMi: Write Mask Data (i=0~7)
RAS only refresh does not reset Stop or LMR functions.

Notes :
(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, FLW, MWT, MSWT, RWM and BWM use old mask. (CBRR reset to new mask. Use CBRS or CBRN to perform CAS-before-RAS refresh while using Old mask).
(3) With CBRS, split transfer operation uses stop Register as a boundary address.
(4) Stop defines the column on which Shift out moves to the otehr half of the SAM.
(5) Ater LMR, WMi is only changed by the another LMR or CBRR cycle.
(6) The Row that is addressed will be refreshed, but a Row address is not required.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM428C258	KM428V258	
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	-0.5 to + 4.6	V
Storage Temperature	Tstg	-55 to + 150	-55 to + 150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70 °C)

Item	Symbol	KM428C258			KM428V258			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC}+1V	2.0	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	–	0.8	-0.3	–	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \le V_{IN} \le V_{CC}$+0.5V*1, all other pins not under test=0 volts, $SE \ge V_{CC}$-0.2V)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)*1	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

*1: 3.6V in KM428V258

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	MIN	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM428C258			KM428V258		Unit
			-6	-7	-8	-7	-8	
Operating current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC1}	110	100	90	60	55	mA
	Active	I_{CC1A}	155	140	125	85	75	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$=$V_{IH}$, DSF=$V_{IL}$)	Standby	I_{CC2}	10	10	10	5	5	mA
	Active	I_{CC2A}	55	50	45	30	25	mA
$\overline{RAS}$ Only Refresh Current*1 ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @tRC=min.)	Standby	I_{CC3}	100	90	80	55	50	mA
	Active	I_{CC3A}	145	130	115	80	70	mA
Fast Page Mode Current*1 ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @tPC=min.)	Standby	I_{CC4}	80	75	70	45	40	mA
	Active	I_{CC4A}	125	115	105	70	65	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC5}	90	85	80	50	45	mA
	Active	I_{CC5A}	135	125	115	75	70	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC6}	140	125	110	75	70	mA
	Active	I_{CC6A}	185	165	145	100	90	mA
Flash Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC7}	90	85	80	50	45	mA
	Active	I_{CC7A}	135	125	115	75	70	mA
Block Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC8}	110	105	100	65	60	mA
	Active	I_{CC8A}	155	145	135	90	80	mA
Color Register Load or Read Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @tRC=min.)	Standby	I_{CC9}	90	85	80	50	45	mA
	Active	I_{CC9A}	135	125	115	75	70	mA

Note *1 : Real values dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as average current. In Icc1, Icc3, Icc6, Icc7, Icc8, Icc9 address transition should be changed only once while $\overline{RAS}$=V_{IL}. In Icc4 address transition should be changed only once while $\overline{CAS}$=V_{IH}

AC CHARACTERISTICS

(0°C≤TA≤70°C, KM428C258: Vcc=5.0V±10%, KM428V258: Vcc=3.3V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		200		ns	
Fast page mode cycle time	tPC	30		35		40		ns	
Fast page mode read-modify-write	tPRWC	80		85		90		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	tCAC		12		15		20	ns	3,5,6
Access time from column address	tAA		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Write command pulse width	tWPZ	10		10		10		ns	
Write command output buffer turn-off delay	tWEZ		10		15		15	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5,6
$\overline{RAS}$ to column addr. delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time(CBR counter test cycle)	t_{CPT}	10		10		10		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
Output hold time from $\overline{CAS}$	t_{DOH}	5		5		5		ns	
Row addr. set-up time	t_{ASR}	0		0		0		ns	
Row Addr. hold time	t_{RAH}	10		10		10		ns	
Column addr. set-up time	t_{ASC}	0		0		0		ns	
Column addr. hold time	t_{CAH}	15		15		15		ns	
Column addr. hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column addr. to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	15
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	15
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column addr. to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output buffer turn-off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ms	
Refresh period(512 cycle)	tREF		8		8		8	ns	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	15		15		15		ns	
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	tCTH	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	tATH	20		25		30		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay(read transfer)	tRSD	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	tCSD	25		30		35		ns	
Col. Addr.to first SC delay(read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	tTSD	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	tSRS	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	tSRD	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	tSDD	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	10	30	10	30	10	35	ns	7
Serial Input to first SC delay time	tSZS	0		0		0		ns	
SC cycle time	tSCC	18		22		25		ns	
SC pulse width(SC high time)	tSC	6		7		7		ns	14

AC CHARACTERISTICS (Continued)

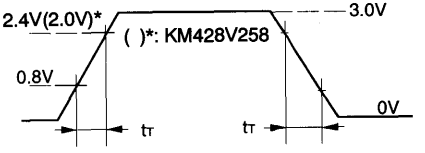
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
SC precharge(SC low time)	t_{SCP}	6		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	
Serial output hold time from SC	t_{SOH}	5		5		5		ns	4
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	10		15		10		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	4
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	7
Serial write enable set-up time	t_{SWS}	0		0		0		ns	
Serial write enable hold time	t_{SWH}	10		15		15		ns	
Serial write disable set-up time	t_{SWIS}	0		0		0		ns	
Serial write disable hold time	t_{SWIH}	10		10		15		ns	
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	
$\overline{DT}/\overline{OE}$ high pulse width	t_{OEP}	10		10		10		ns	
$\overline{DT}/\overline{OE}$ high hold time $\overline{CAS}$ high	t_{OEHC}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), and t_{SDZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. The t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. During power-up $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ must be held High or track with V_{CC}. After power-up, initial status of chip is described below.

PIN or REGISTER	STATUS
Color Register	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Input Mode
SDQi	Hi-Z

13. Recommended operating input condition:



   Input pulse levels are from 0.0V to 3.0Volts.
   All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 3.0ns
14. Assume t_T = 3.0ns
15. t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).

DEVICE OPERATION

The KM428C/V258 contains 2,097,152 memory locations. Eighteen address bits are required to address a particular 18bit word in the memory array. Since the KM428C/V258 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CAS}$)and the valid row and column address inputs.

Operation of the KM428C/V258, begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This is the beginning of any KM428C/V258 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C/V258 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access time is specified by t_{CAC} or t_{AA}.

The KM428C/V258 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM read cycle, D_{OUT} buffer is designed to make turn-off by the rising edge of $\overline{CAS}$ even though $\overline{OE}$ is to be low. The KM428C/V258 offers an accelerated Fast Page Mode cycle by eliminating output disable from $\overline{CAS}$ high.

This is called "Extended Data out (or Hyper Page) mode", Data outputs are disabled at $\overline{WB}/\overline{WE}$=low, $\overline{DT}/\overline{OE}$=high and t_{OFF} time after $\overline{RAS}$ and $\overline{CAS}$ are high. The t_{OFF} time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs later(see Figure 1). What the output buffer is disabled during $\overline{DT}/\overline{OE}$=high is to use Bank selection in the frame buffer memory using common I/O line. Read, write and read-modify write cycles are available during the Extended data out mode.

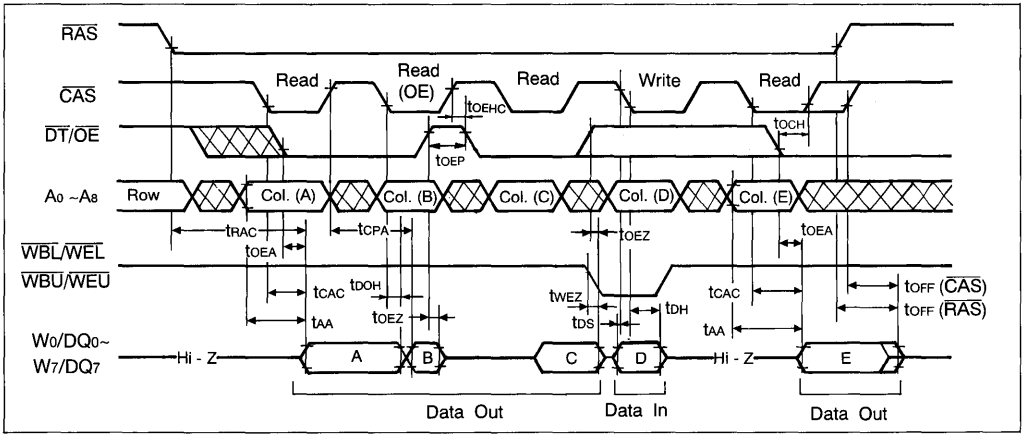


Figure 1. Extended Data Output Example

DEVICE OPERATION (Continued)

Nibble Write Operation

The KM428C/V258 has 2 write control Pin, $\overline{WBL}/\overline{WEL}$, $\overline{WBU}/\overline{WEU}$, and offers asynchronous write operation with Lower nibble(W_0/DQ_0~W_3/DQ_3)and upper nibble (W_4/DQ_4~W_7/DQ_7). This is called Nibble write operation. This operation can be performed in RAM write, Block Write, Load Mask Register and Load color Register.

New Mask Write Per Bit

The New Mask Write cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WBX}/\overline{WEX}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_7/DQ_7 pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data a low, writing is inhibited into the RAM and the data bit remains unchanged. When the mask data is high, data is written into the RAM. The mask data is valid for only one cycle, defined by an active $\overline{RAS}$ period. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WBX}/\overline{WEX}$ low before $\overline{CAS}$ falling and Late Write cycle is achieved by $\overline{WBX}/\overline{WEX}$ Low after the falling edge of $\overline{CAS}$. During the Early or Late Write cycle, input data through W_0/DQ_0~W_7/DQ_7 must meet the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WBX}/\overline{WEX}$. When $\overline{WBX}/\overline{WEX}$ is high at the falling edge of $\overline{RAS}$ no masking operation is performed.

2

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
↓	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

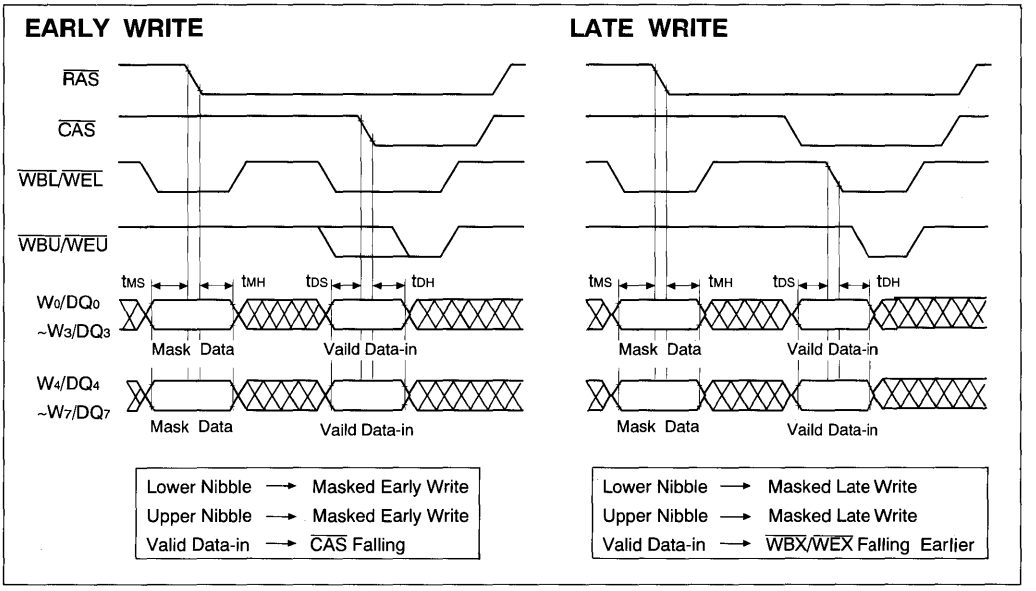


Figure 2. Nibble Write and New Masked Write Cycle Example 1 (Early Write & Late Write)

DEVICE OPERATION (Continued)

Load Mask register(LMR)

The Load Mask Register operation loads the data present on the wi/DQi pins into the Mask data Register at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$. The LMR cycle is performed if DSF high, $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$ and DSF Low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM428C/V258 is set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR)cycle. If an LMR is done, all Masked Writes are Old Masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register(See Figure3). The mask data is applied in the same manner as in New Masked write-Per-Bit mode. Mask Data Registers content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After Power up, the KM428C/V258 initialized in the New Masked Write mode.

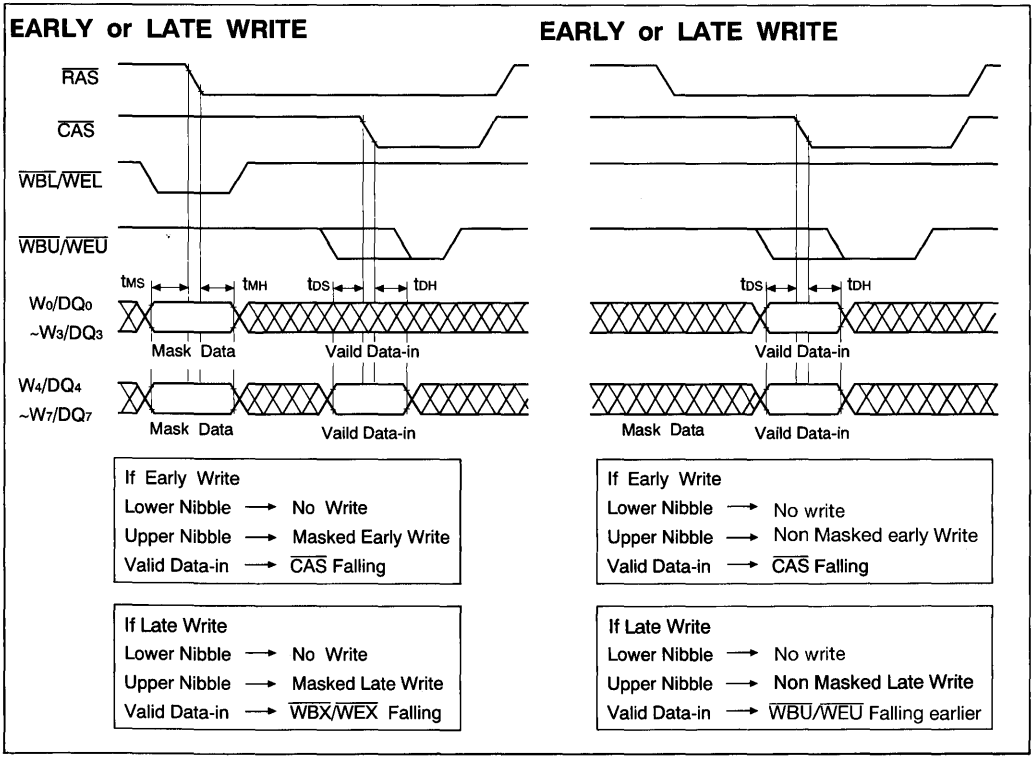


Figure 3. Nibble Write and New Mask Write Cycle Example 2

DEVICE OPERATION (Continued)

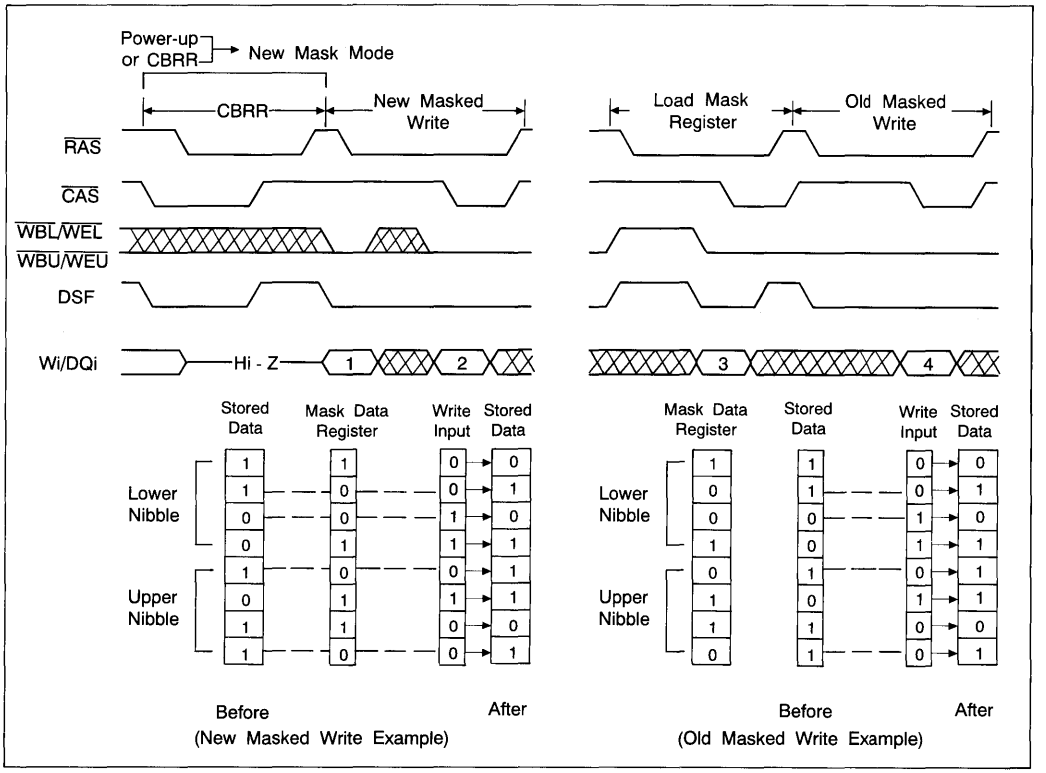


Figure 4. New Mask Write Cycle and Old Mask Write Cycle Example

Fast Page Mode

Fast page mode cycle reads/writes the data of the same row address at high speed by togging $\overline{CAS}$ while $\overline{RAS}$ is low. In this cycle, read, write, read-modify write, and block write cycles can be mixed. In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column address.

This eliminates the time required to set up and strobe sequential row address for the same page

Load Color Register(LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(delayed write) via the W_0/DQ_0~W_7/DQ_7 pins. This data is used in Block Write and Flash Write cycles and remains unchanged until the next Load Color Register cycle.

Block Write

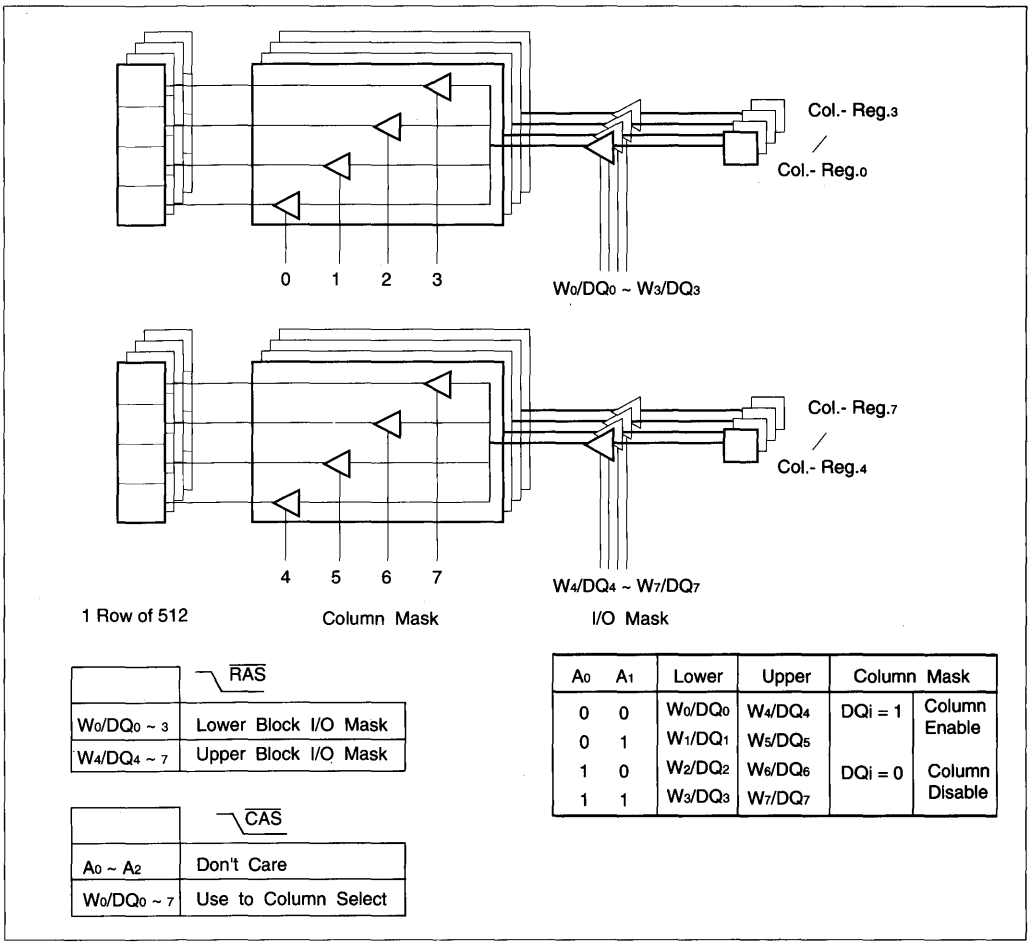
In a Block Write cycle four adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 8-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into four adjacent locations of the same row of each corresponding bit plane(8). This results in a total of 32-bits being written in a single Block Write cycle compared to 8-bits in a normal Write cycle.

The Block Write cycle is performed if DSF is low on the falling edge of $\overline{RAS}$ and high on the falling edge of $\overline{CAS}$.

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.

DEVICE OPERATION (Continued)



A0	A1	Lower	Upper	Column Mask	
0	0	W0/DQ0	W4/DQ4	DQi = 1	Column Enable
0	1	W1/DQ1	W5/DQ5		
1	0	W2/DQ2	W6/DQ6	DQi = 0	Column Disable
1	1	W3/DQ3	W7/DQ7		

Figure 5. Block Write Scheme

Since four bits are being written at a time, when the minimum increment required for the column address is four. Therefore, when the column address is latched on the falling edge of $\overline{CAS}$, the 2LSBs, A_0 and A_1 are ignored and only bits(A_2~A_8) are used to define the location of the first bit out of the four to be written.

Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_3/DQ_3 pins provideds column mask data. That is, for each of the four bits in all 8-bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_0/DQ_1=0, then the Color Register contents will be written into the first bit out of the four, but the second remains unchanged. Fig 5 shows the correspondence of each data line to the column mask bits.

Masked Block Write(MBW)

A Masked Block Write cycle is identical to a New Mask Write-per-bit cycle except that each of the 8-bit planes being masked is operating on 4 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high on the falling edge of $\overline{CAS}$. Mask data is latched into the device via the W_0/DQ_0~W_7/DQ_7 pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle.

DEVICE OPERATION (Continued)

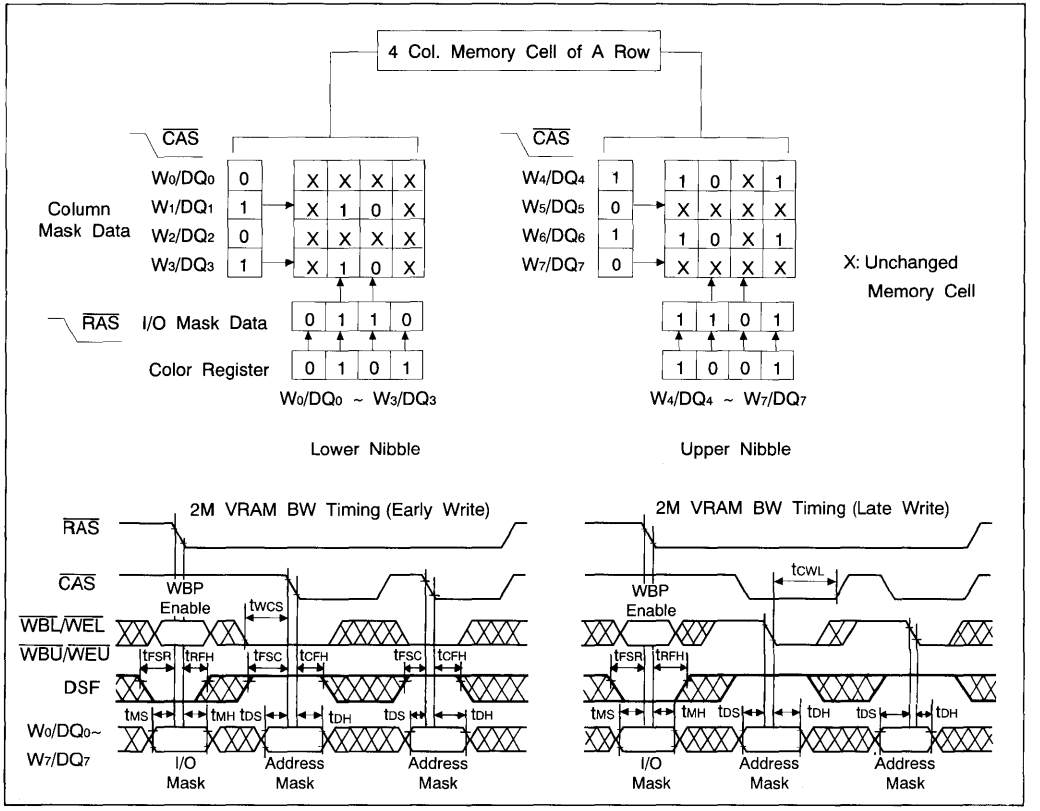


Figure 6. Block Write Example and Timing

Flash Write

The Flash Write cycle is a way of writing each bit of the Color Register into the whole row(512 columns) simultaneously. This function is used for fast screen clear or background color change. 512 columns in each bit plane are written, for a total of 4096 bits(512×8 bit planes) in one cycle. While this cycle writes significantly more data than the Block Write cycle, it is also less selective.

If $\overline{WBX}/\overline{WEX}$ is low and DSF is high on the falling edge of $\overline{RAS}$, a Flash Write cycle is performed. Also on this edge, the data present on the Wi/DQi pins is used as mask data and needs to be provided for every Flash Write cycle. A Load Color Register cycle must have been performed before initiating a Flash Write cycle.

Data Output

The KM428C/V258 has three state output buffers controlled by $\overline{DT}/\overline{OE}$, $\overline{CAS}$ and $\overline{RAS}$, $\overline{WB}/\overline{WE}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ are Low, the output state is in high impedance(Hi-z). In any cycle, the output goes low impedance state from the first $\overline{CAS}$ falling edge.

Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs(as in hidden refresh).

Each of the KM428C/V258 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Refresh

The data in the KM428C/V258 is stored as a charge on a tiny capacitor within each memory cell. Due to leakage the data may be lost over a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 4096 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses. (A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM428C/V258 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time(t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

The KM428C258 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation; CBRR, CBRN, CBRS. CBRR(CBR Refresh with option reset)is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default value. CBRN(CBR Refresh without Reset)is set if DSF high when $\overline{WB}/\overline{WE}$ is high at the $\overline{RAS}$ falling edge and simply do only refresh operation. CBRS(CBR Refresh with stop register set)cycle is set if DSF high when $\overline{WB}/\overline{WE}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM428C/V258 hidden refresh cycle is actually a $\overline{CAS}$ before-RAS refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM428C/V258 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

Transfer operation is initiated when $\overline{DT}/\overline{OE}$ is low at the falling edge of $\overline{RAS}$. The state of $\overline{WB}/\overline{WE}$ when $\overline{RAS}$ goes low indicates the direction of transfer (to or from DRAM) and DSF pin is used to designate the proper transfer mode like normal and Split Transfer. Each of the transfer cycle is described in the truth table of transfer operation.(Table2.)

Read Transfer(RT)

The Read Transfer operation is set if $\overline{DT}/\overline{OE}$ is low, $\overline{WB}/\overline{WE}$ is high, and DSF is low when $\overline{RAS}$ goes low. The row address bits in the read transfer cycle indicate which eight 512bit DRAM Row portions are transferred to the eight SAM data registers. The column address bits indicate the start address of the SAM registers when SAM data read operation is performed. If MSB bit of column address is low during Read transfer operation, the QSF state will be set low and this indicates the start address of the SAM register is present at the lower half of the SAM port.(If A_8 is high, QSF will be high meaning that the start address is in the upper half). Read Transfer may be achieved in two ways. If the transfer is to be synchronized with the SC, $\overline{DT}/\overline{OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer".

Note that the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with the rising edge of SC(t_{RSL}/t_{RSD})to retain the continuity of serial read data output.

If the transfer does not have to be synchronized with SC, $\overline{DT}/\overline{OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Table.2 Truth Table for Transfer Operation

* : Don't care

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$				
H	L	H	L	*	Read Transfer	RAM → SAM	512 x 8	Input → Output
H	L	L	L	*	Masked Write Transfer	SAM → RAM	512 x 8	Output → Input
H	L	H	H	*	Split Read Transfer	RAM → SAM	256 x 8	Not Changed
H	L	L	H	*	Masked Split Write Transfer	SAM → RAM	256 x 8	Not Changed

DEVICE OPERATION (Continued)

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(512bit) to be transferred to the selected ROW in the DRAM array. Masking is selected by latching Wi/DQi(i=0~7)inputs when $\overline{RAS}$ goes low.

The column address defines the start address of serial input.

If A_8 is low, the start address is positioned in the lower half of SAM.(For A_8=high, the start address will be positioned in the upper half of SAM) After write transfer cycle is completed, SAM port is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first clock of the new data.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, there by simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower op upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. The transfer is not synchronized with a 1μ s period while the other half is accessing data. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer. A Split Read Transfer cycle is begun by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. Address pin A_8 is a "Don't care".

A Split Read Transfer will load data into the other half. Example of SRT applications are shown in Fig. 7 through Fig 11.

The normal usage of Split Read Transfer cycle is described in Fig. 7. When Read Transfer is executed, data from X1 row address is fully transferred to the SAM port and Serial Read is started from 0(Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed.

The another example of SRT cycle is described in Fig. 8. When Serial Read is performed after executing RT and SRT in succession the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle. If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig. 9, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig.10, indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511. In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+t_{STS} (See Figure 11). This is also true in Masked Split Write Transfer.

A Split Read Transfer does not change the direction of the SAM I/O port.

Masked Split Write Transfer(MSWT)

This transfer function is very similiar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "Don't Care". The example of MSWT is described in fig. 10. The opening cycle MWT is needed before MSWT can be performed.

DEVICE OPERATION (Continued)

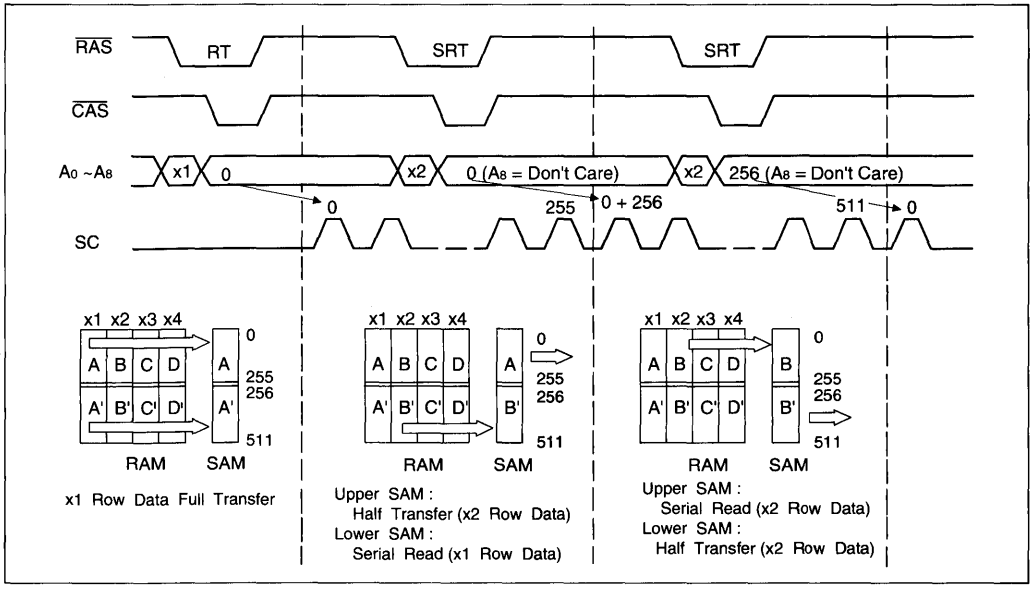


Figure 7. Split Read Transfer Normal Usage

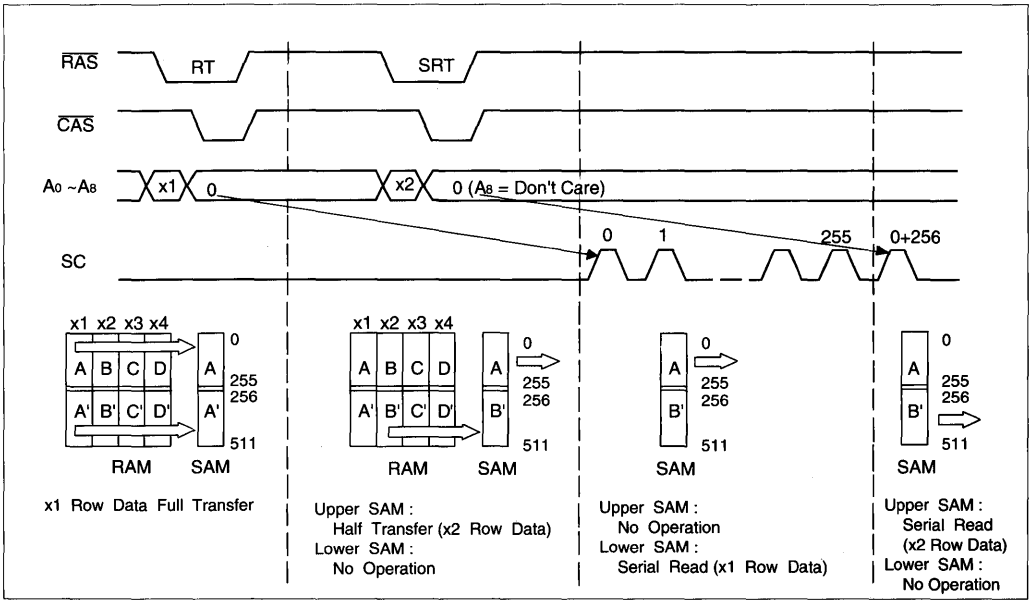


Figure 8. Split Read Transfer Normal Usage

DEVICE OPERATION (Continued)

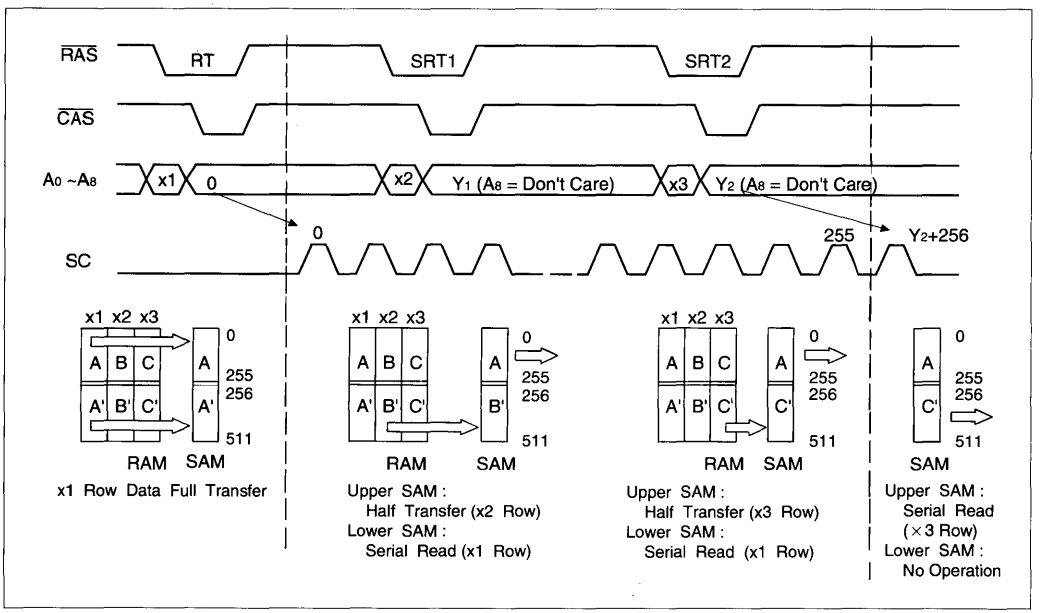


Figure 9. Split Read Transfer Abnormal Usage (Case 1)

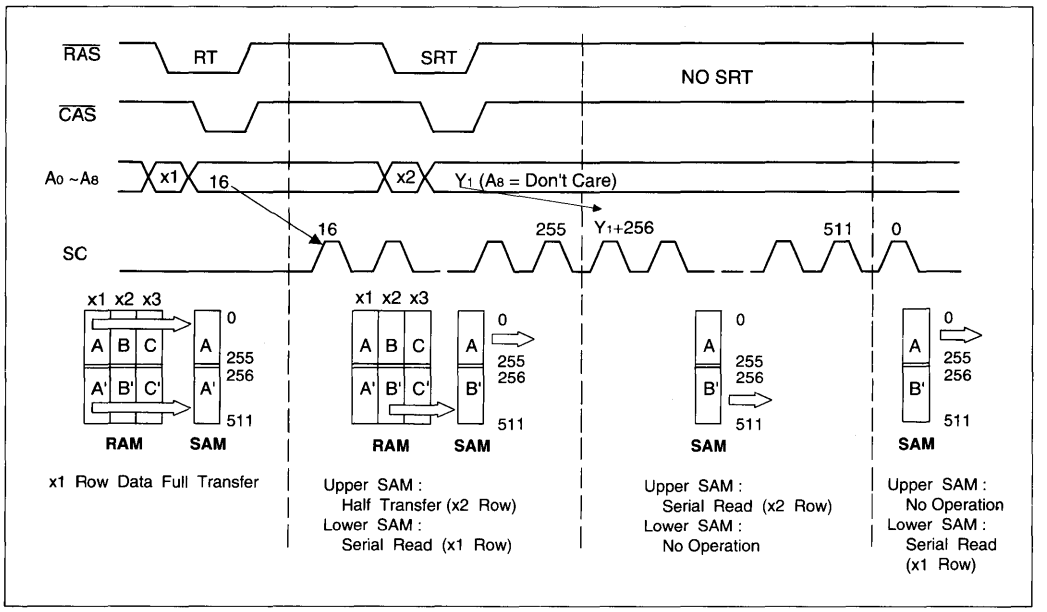


Figure 10. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATION (Continued)

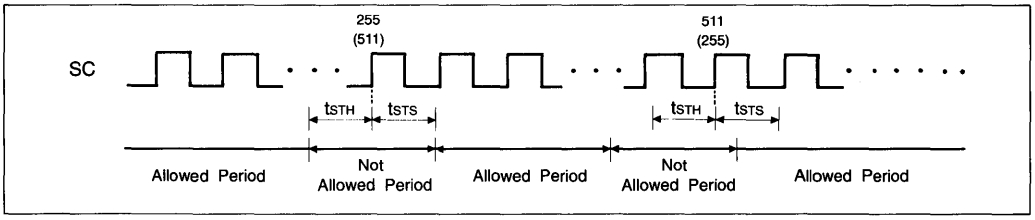


Figure 11. Split Transfer Cycle Limitation Period

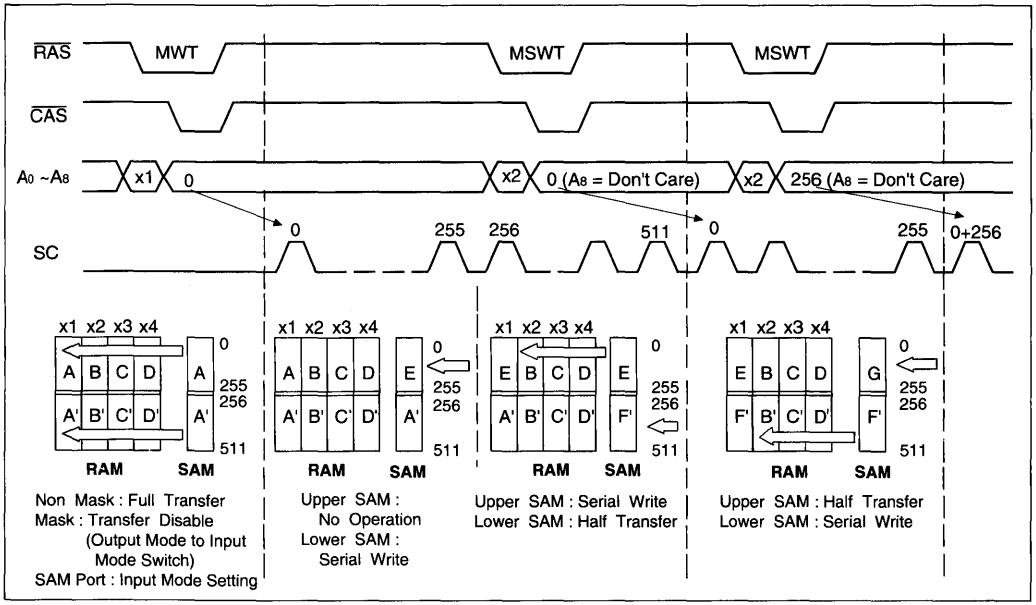


Figure 12. Masked Split Write Transfer Normal Usage

DEVICE OPERATION (Continued)

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half. After the last address of each half SAM(255 or 511)is accessed, the access will be changed one half of the SAM to the other half(at the loaded TAP address). This last address is called Stop Point.

The KM428C/V258 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 3. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.

In Figure 12. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary(383), the access will jump to the TAP address (70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs or the SAM half boundary(255,511). Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of RAS. The CBRR will take effect immediately; it does not require a SRT to become active valid.

Table 3. Stop Point Setting Address

Stop Register = Store the Address of Serial Access
Use on the Split Transfer Cycle
Stop Pointer Set ⟶ CBRS Cycle

Number Stop Points / Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3 ~A_0
1	(1x256)x2	X	1	1	1	1	X
2	(2x128)x2	X	0	1	1	1	X
4	(4x64)x2	X	0	0	1	1	X
8	(8x32)x2	X	0	0	0	1	X
16	(16x16)x2	X	0	0	0	0	X
T	(TxWidth)x2	Other Case = Inhibit					

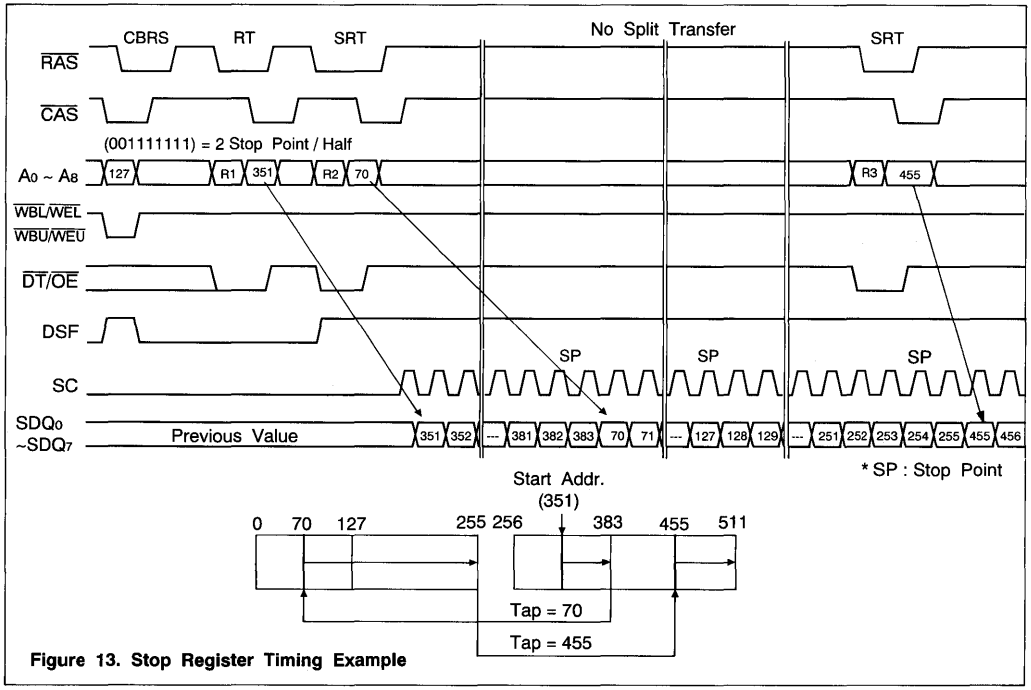
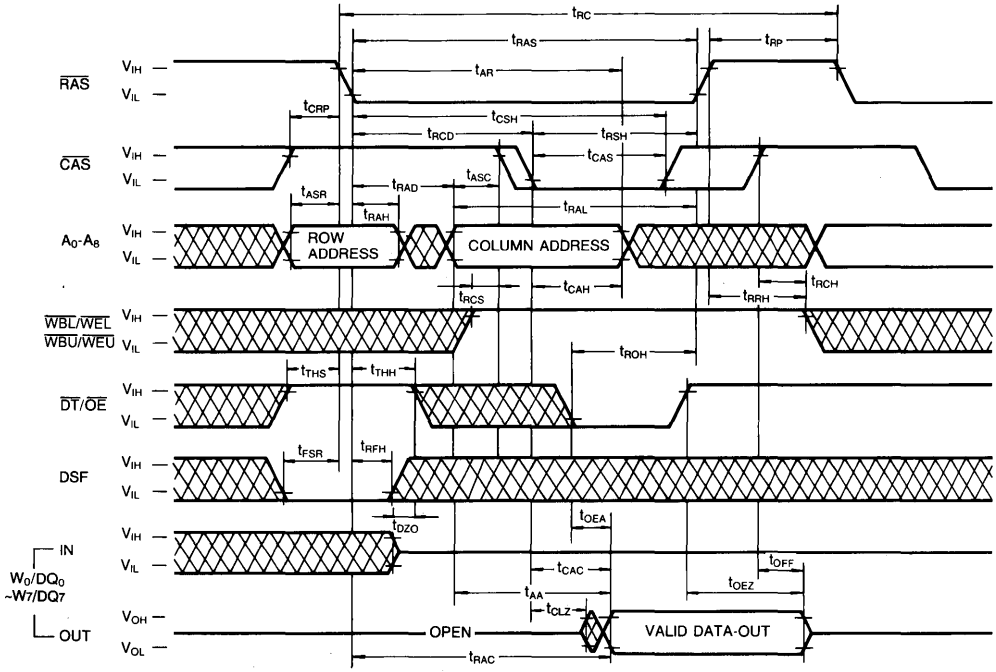


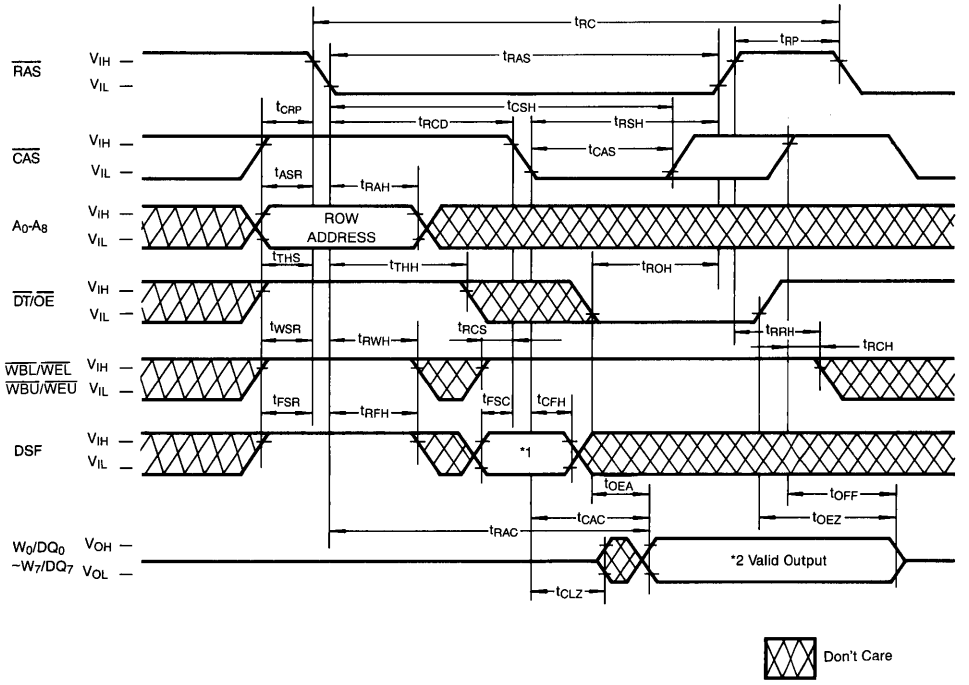
Figure 13. Stop Register Timing Example

TIMING DIAGRAMS

READ CYCLE

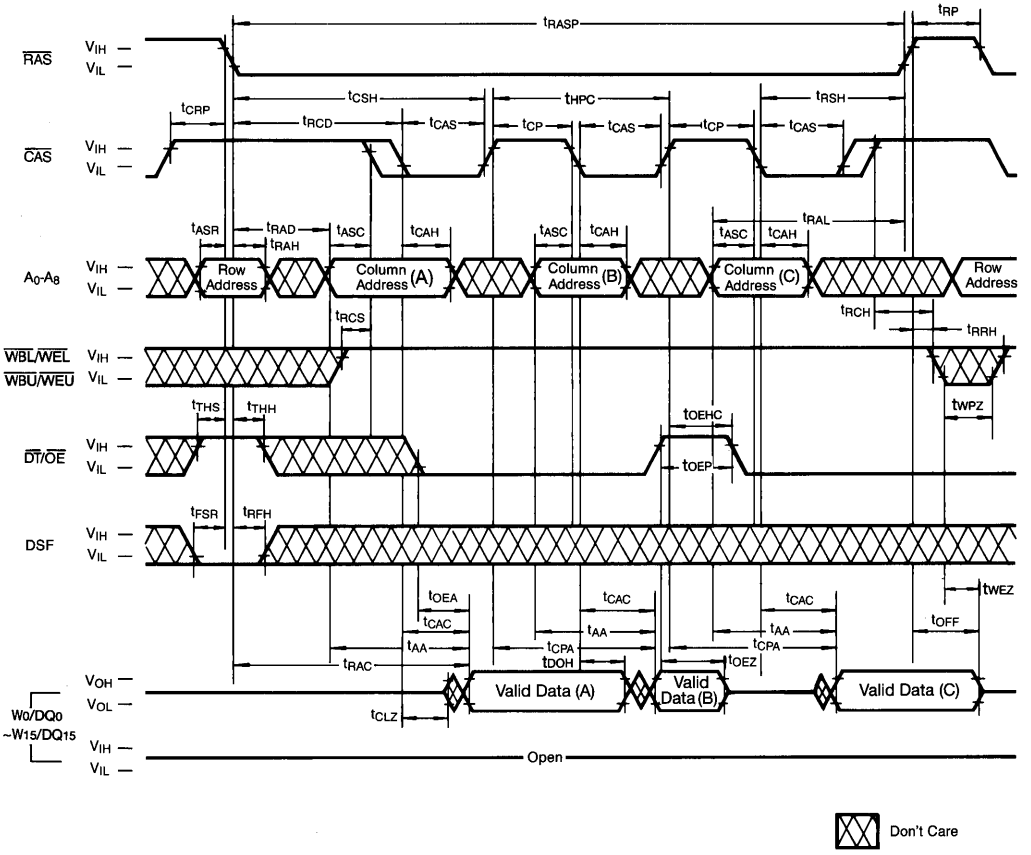


READ MASK/COLOR REGISTER CYCLE



*1	*2	Fuction
0	Mask data	Read Mask Register Cycle
1	Color data	Read Color Register Cycle

FAST PAGE MODE READ CYCLE (Extended Data Out)



TRUTH TABLE FOR WRITE CYCLE(1)

FUNCTION	RAS			CAS	CAS or WB/WE
	*1 WBL/WEL (WBU/WEU)	*2 DSF	*3 Wi/DQi[4] (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)[5]	1	0	×	1	Column Mask
Masked Block Write[5]	0	0	Write Mask	1	Column Mask
Masked Flash Write	0	1	Write Mask	×	×
Load Mask Data Register[2]	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram, on the following page.
(2) Old Mask data load
(3) On the masked flash write cycle. all the signal inputs are don't care condition except $\overline{RAS}$ at the falling edge of $\overline{CAS}$.
(4) Function table for Old Mask and New Mask

IF		*1		*3	Note
		WBL/WBL	WBU/WBU	Wi/DQi	
LMR Cycle Executed	Yes	0	0	×	Write using mask register data (Old Mask Data)
		1	1	×	Non Masked Write
	No	0	0	Write Mask	Write using New Mask Data
		0	1		Wi/DQi=0 Write Disable
		1	0		Wi/DQi=1 Write Enable
		1	1	×	Non Masked Write

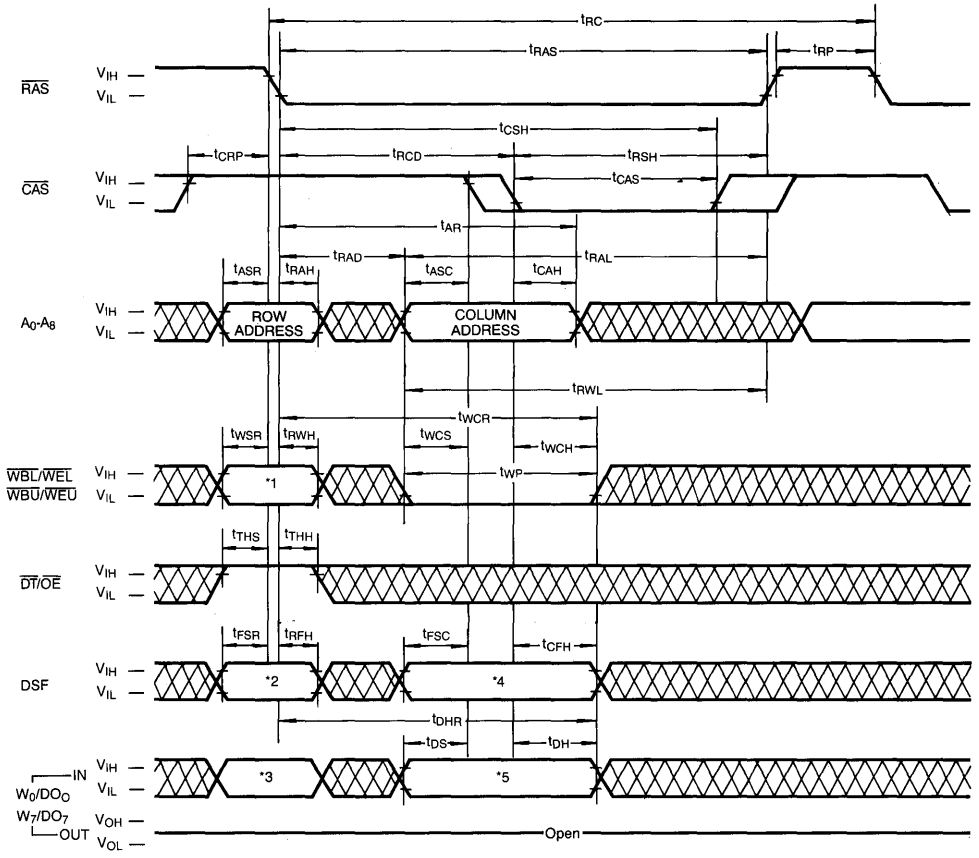
× : Don't Care

(5) Function Table for Block Write Column Mask

Column Address	
A1	A0
0	0
0	1
1	0
1	1

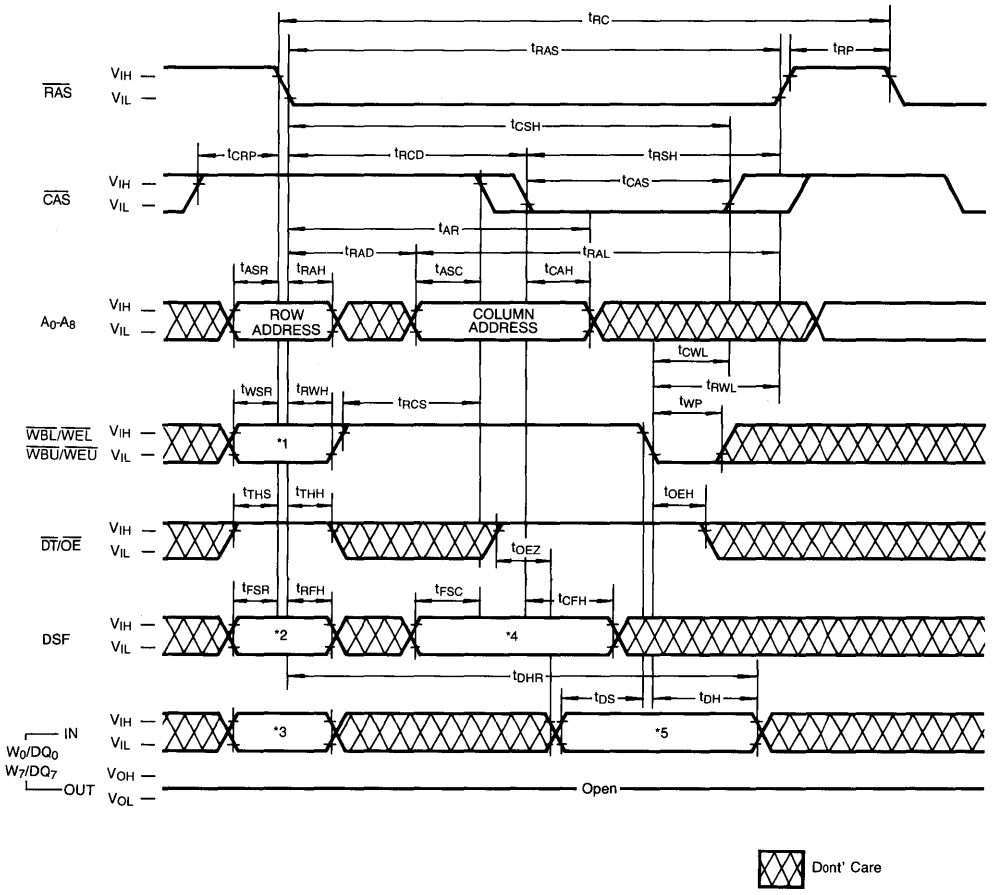
*5		IF	
Lower Nibble	Upper Nibble	Wi/DQi=0	Wi/DQi=1
W0/DQ0	W4/DQ4	No Change the Internal Data	Color Register Data Are Write to the Corresponding Column Address Location
W1/DQ1	W5/DQ5		
W2/DQ2	W6/DQ6		
W3/DQ3	W7/DQ7		

EARLY WRITE CYCLE



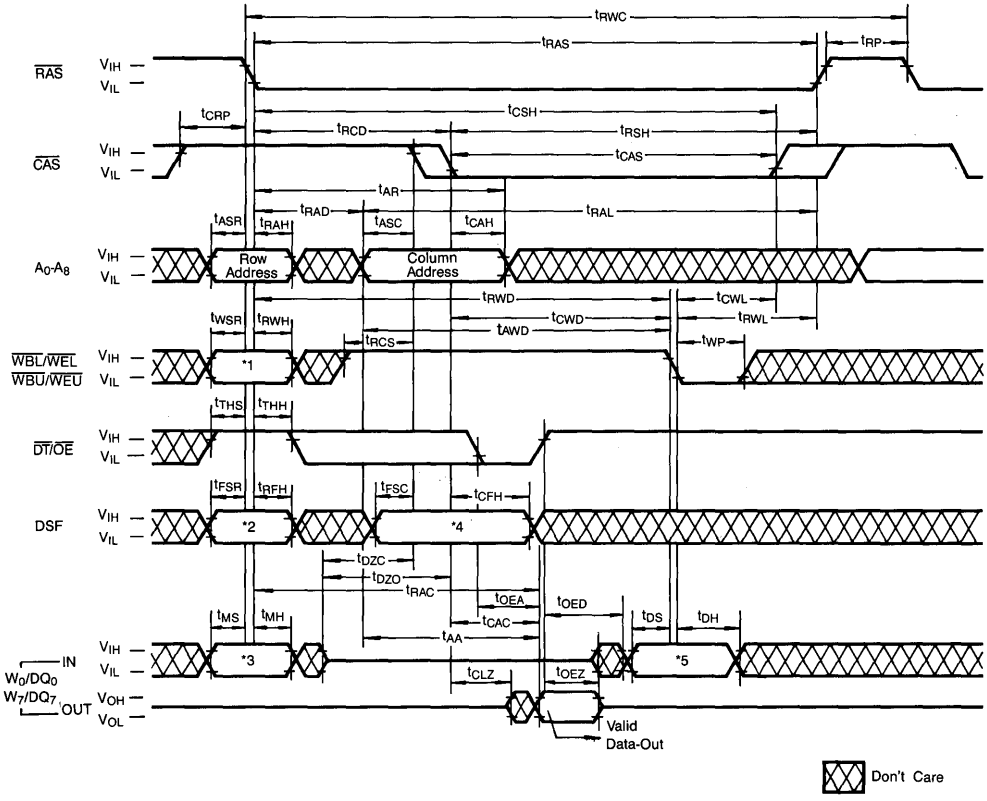
Note: In Block Write cycle, only column address A2~A8 are used.

LATE WRITE CYCLE



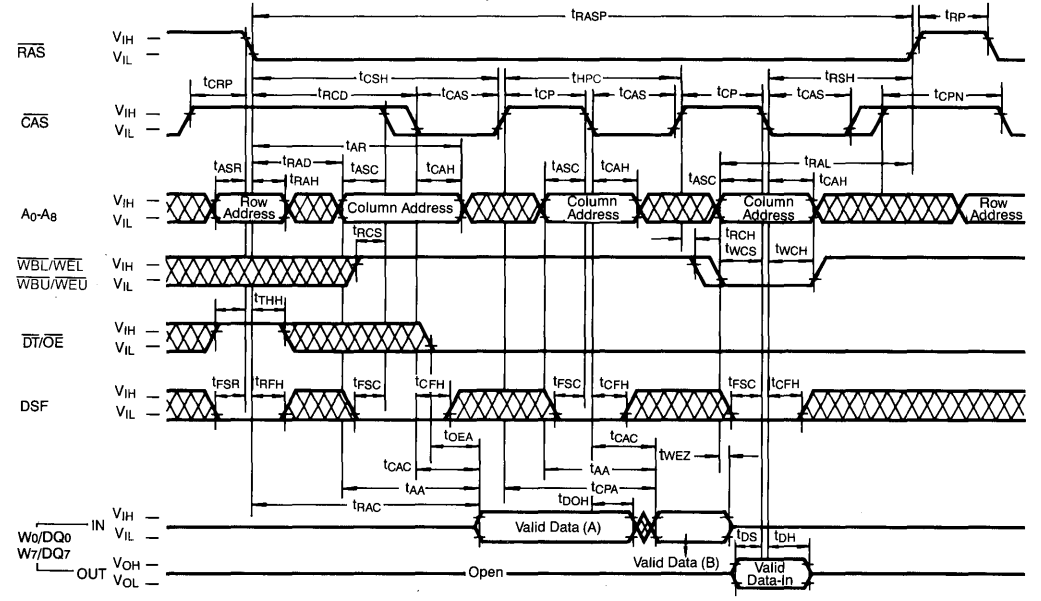
Note: In Block Write cycle, only column address A2~A8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE

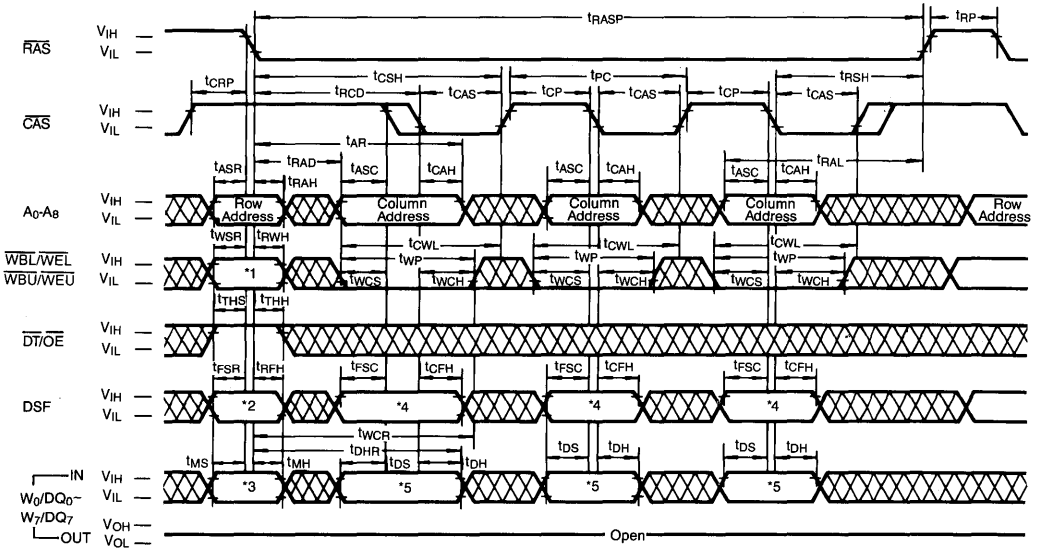


Note: In Block Write cycle, only column address A_2~A_8 are used.

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

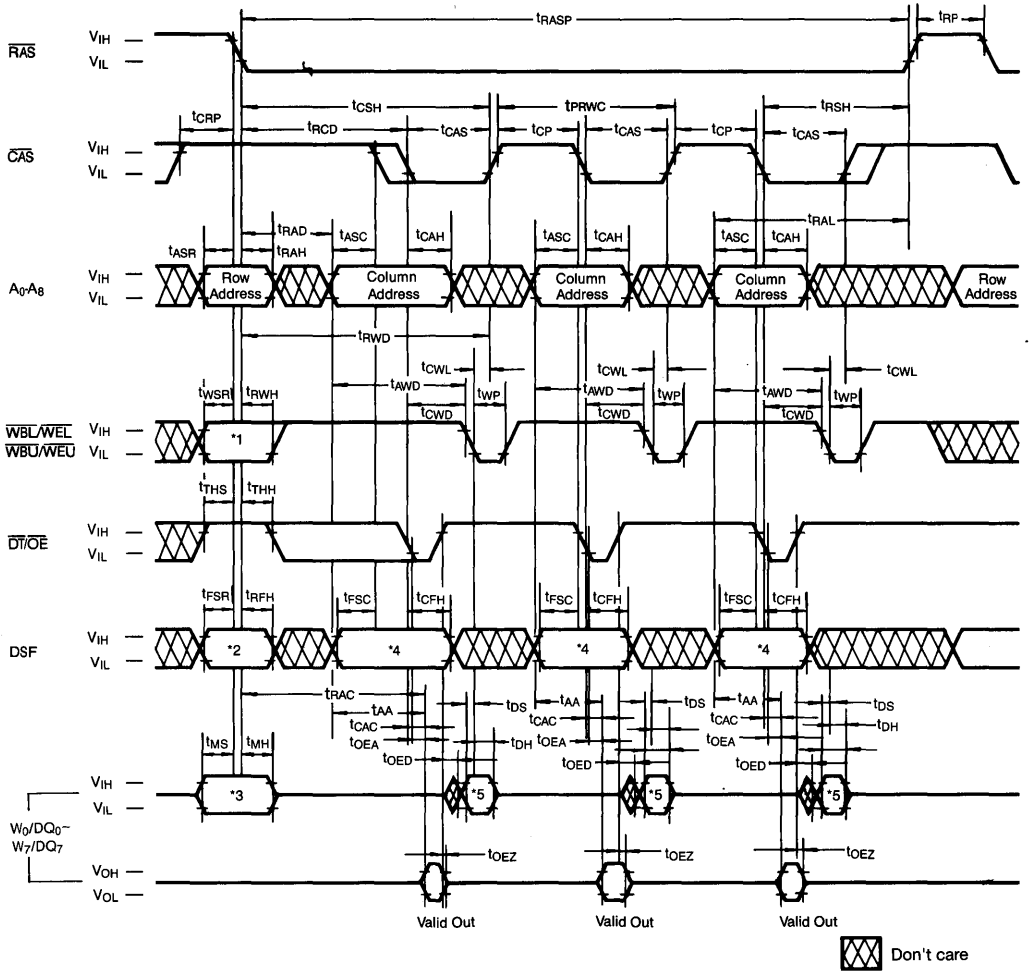


FAST PAGE MODE EARLY WRITE CYCLE



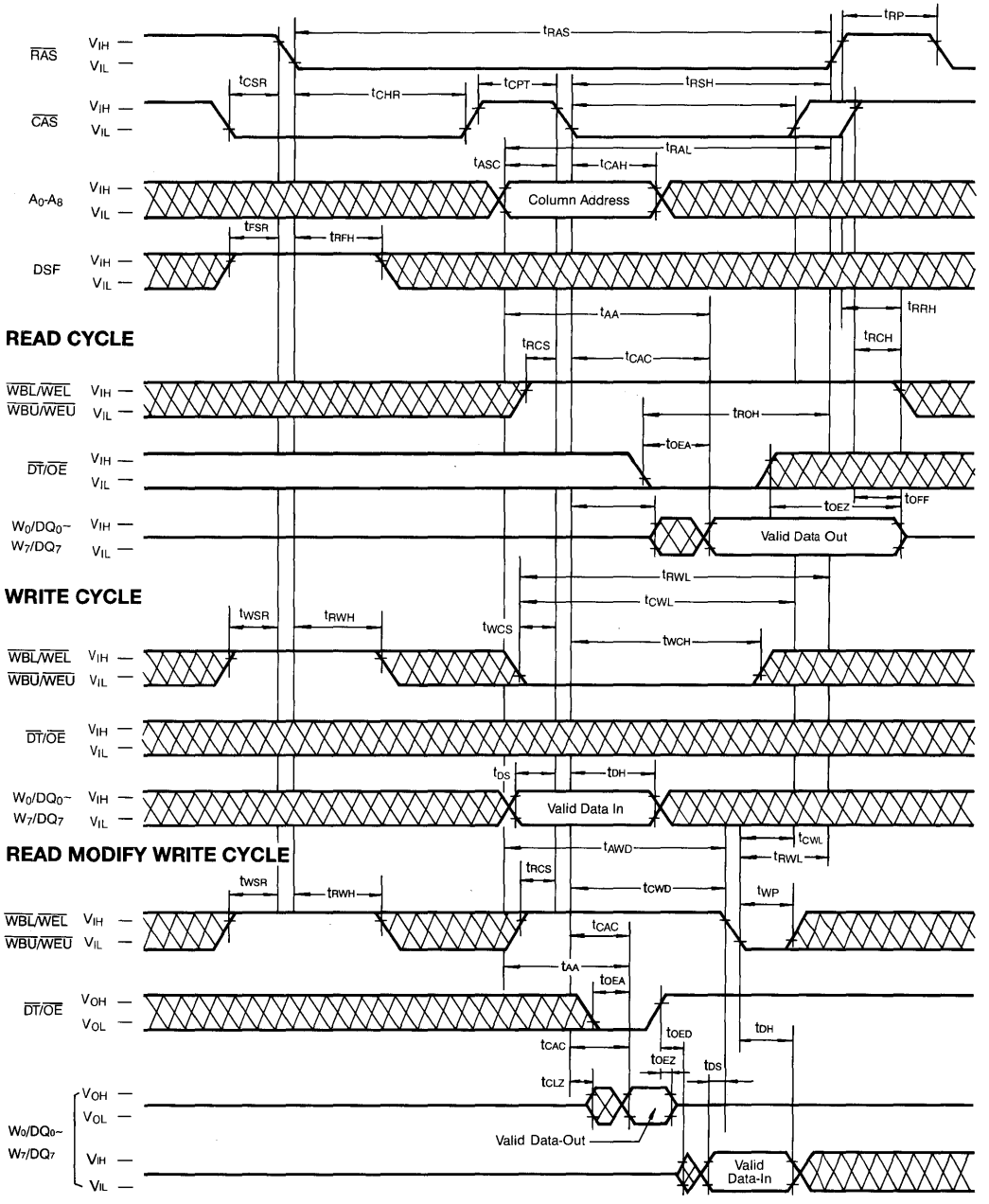
Note: In Block Write cycle, only column address A2~A8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

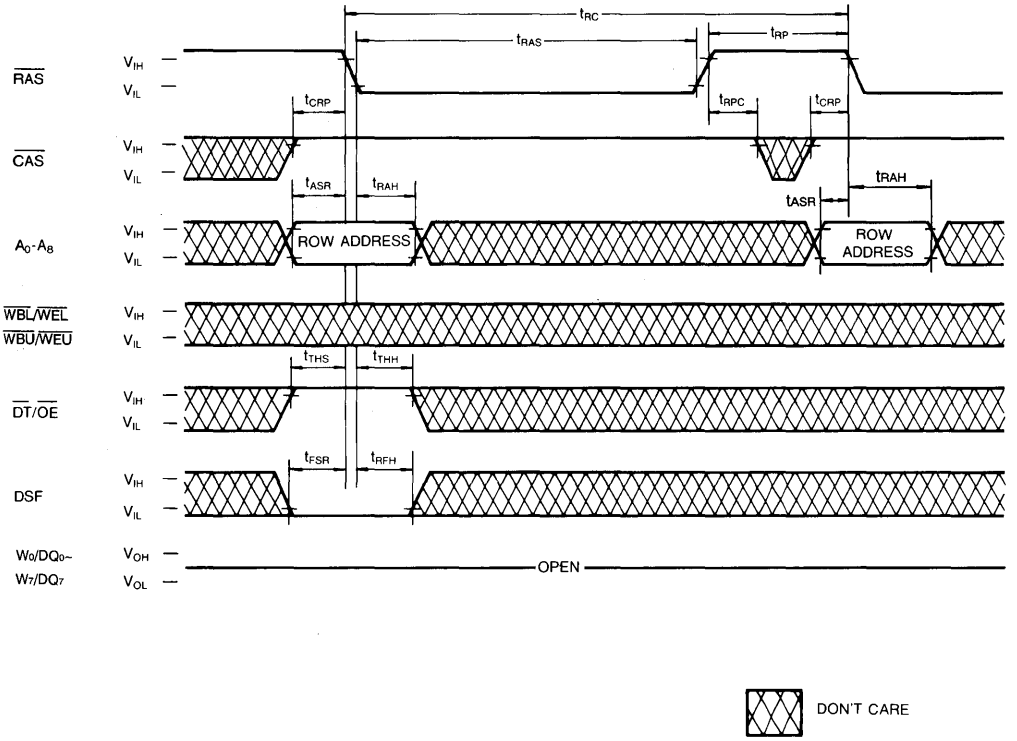


Note: In Block Write cycle, only column address A2~A8 are used.

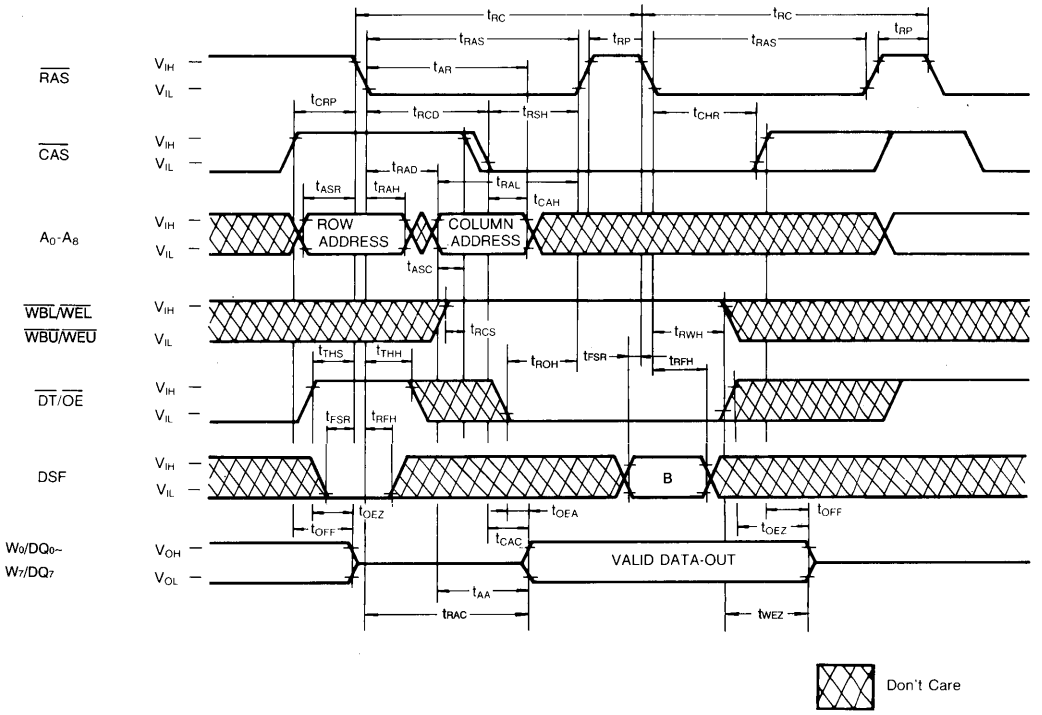
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



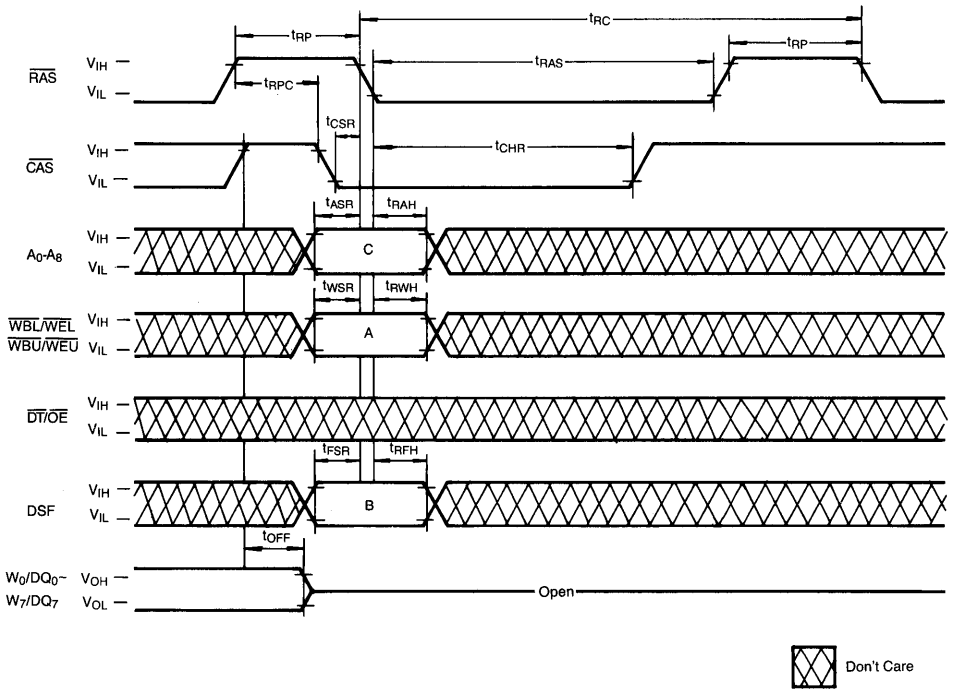
HIDDEN REFRESH CYCLE



HIDDEN REFRESH CYCLE FUNCTION TABLE

FUNCTION	Logic Status B
Hidden Refresh(Reset All Options)	0
Hidden Refresh(No Reset)	1

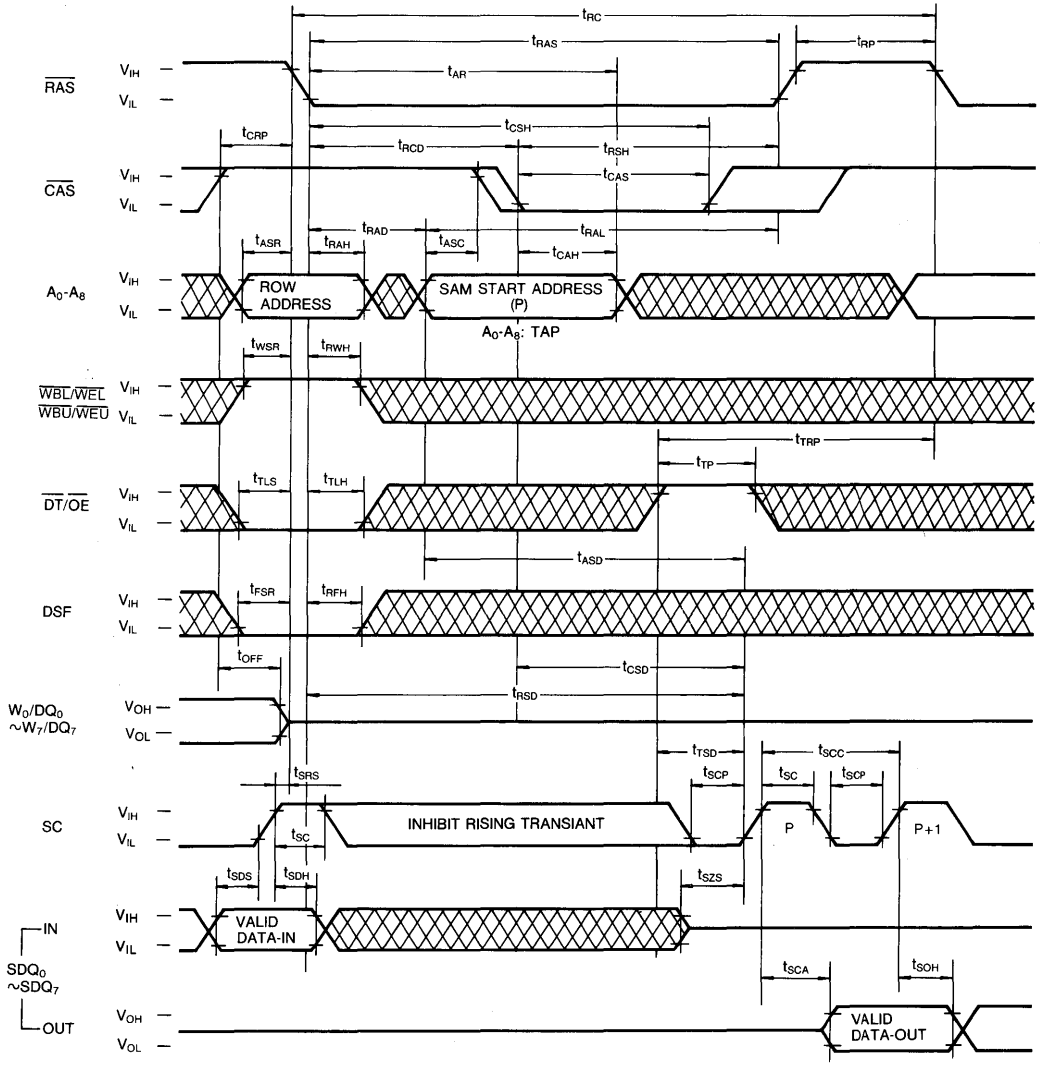
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE FUNCTION TABLE

FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	Stop Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

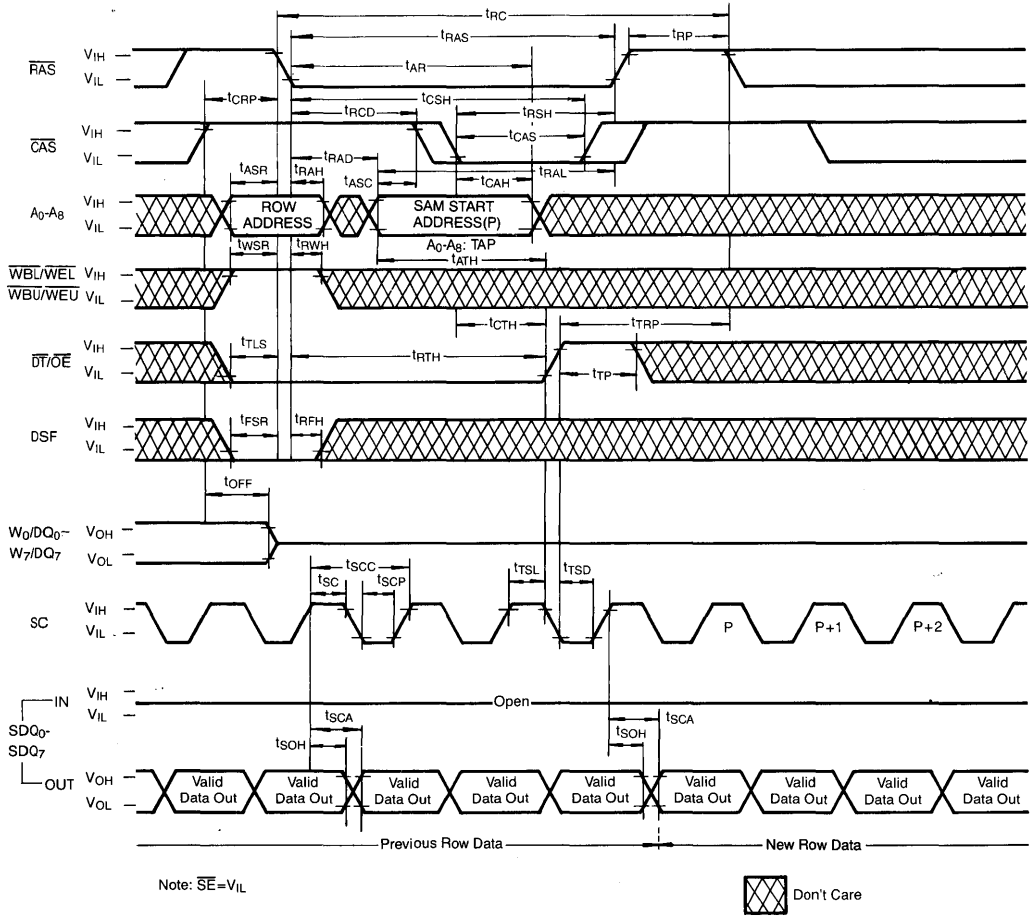
READ TRANSFER CYCLE



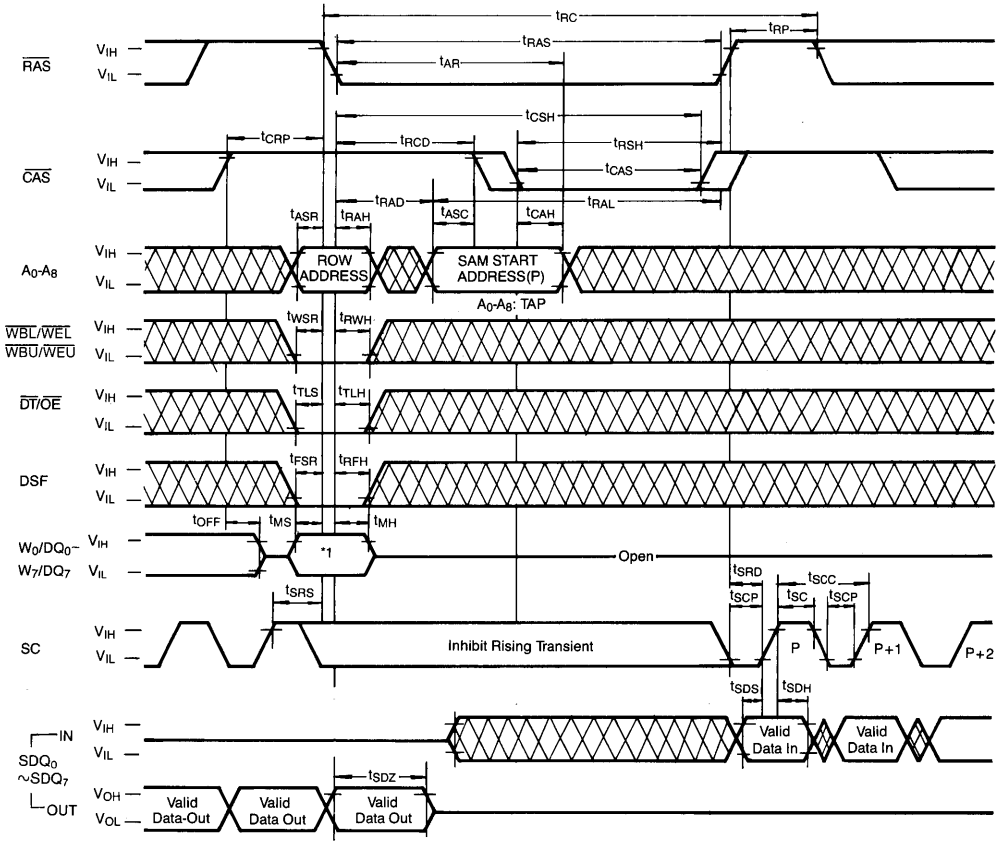
Note: $\overline{SE}$=VIL

Don't Care

REAL TIME READ TRANSFER CYCLE



MASKED WRITE TRANSFER CYCLE (Output Mode to Input Mode Switch)



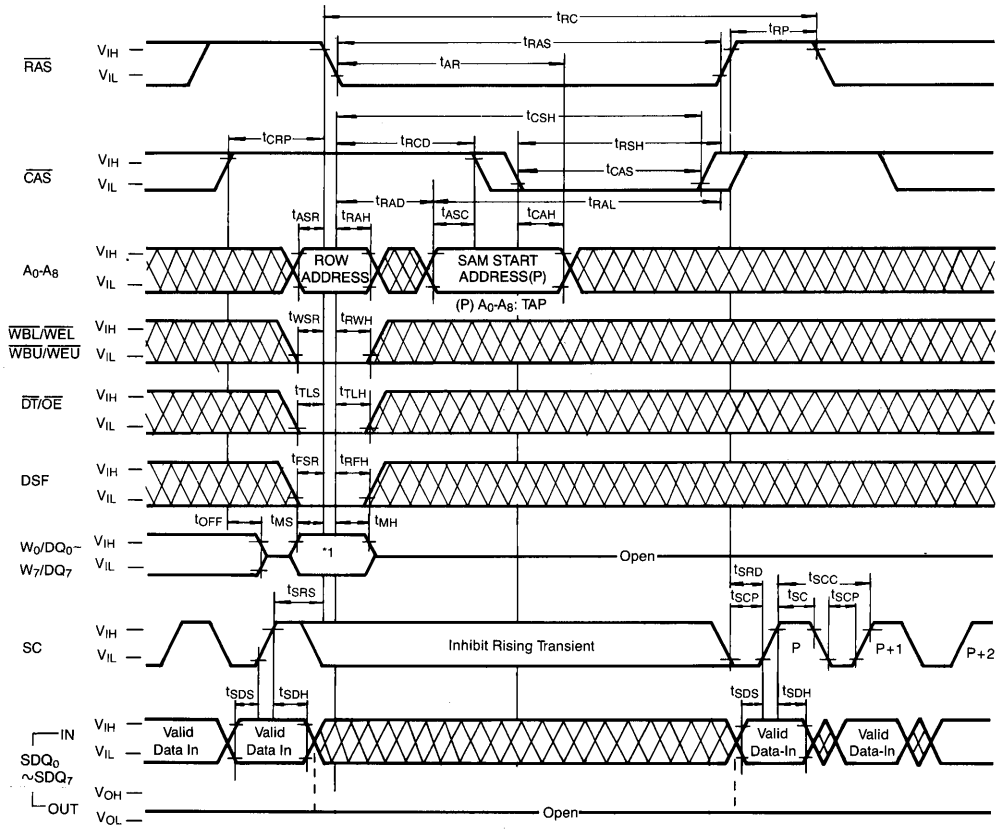
Note: $\overline{SE}=V_{IL}$

Don't Care

Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data 0: Transfer Disable
1: Transfer Enable

MASKED WRITE TRANSFER CYCLE



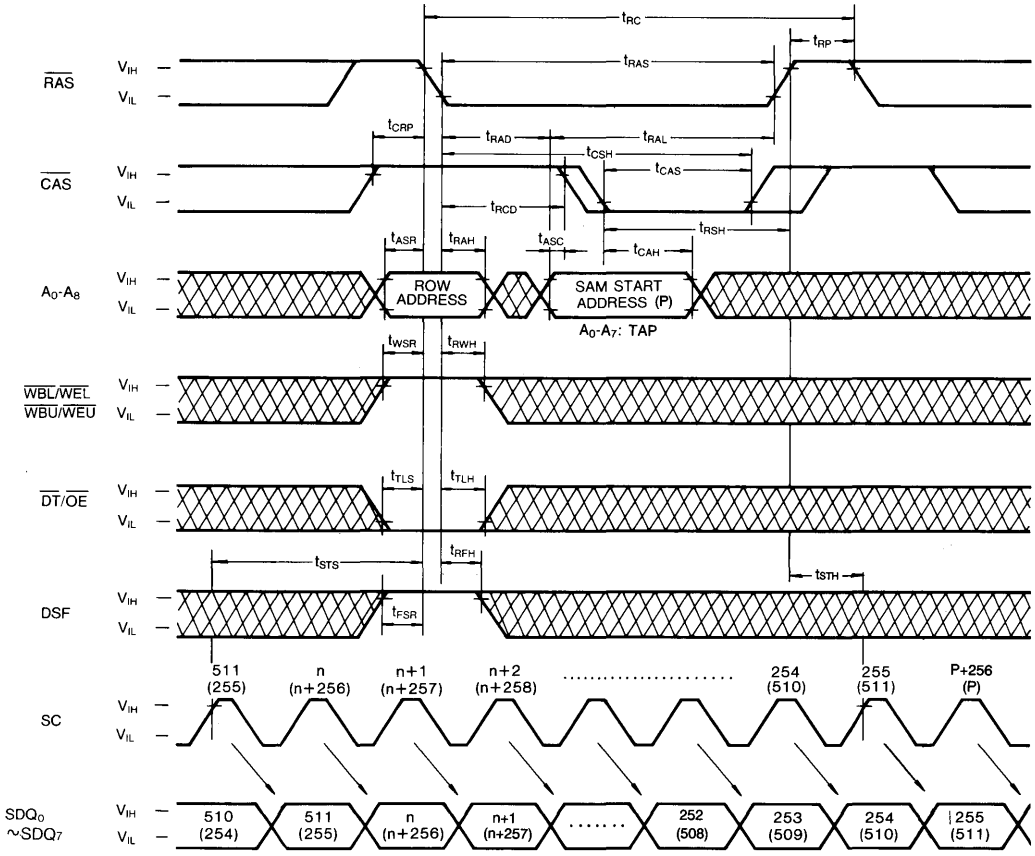
Note: $\overline{SE}=V_{IL}$

Don't Care

Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data 0: Transfer Disable
1: Transfer Enable

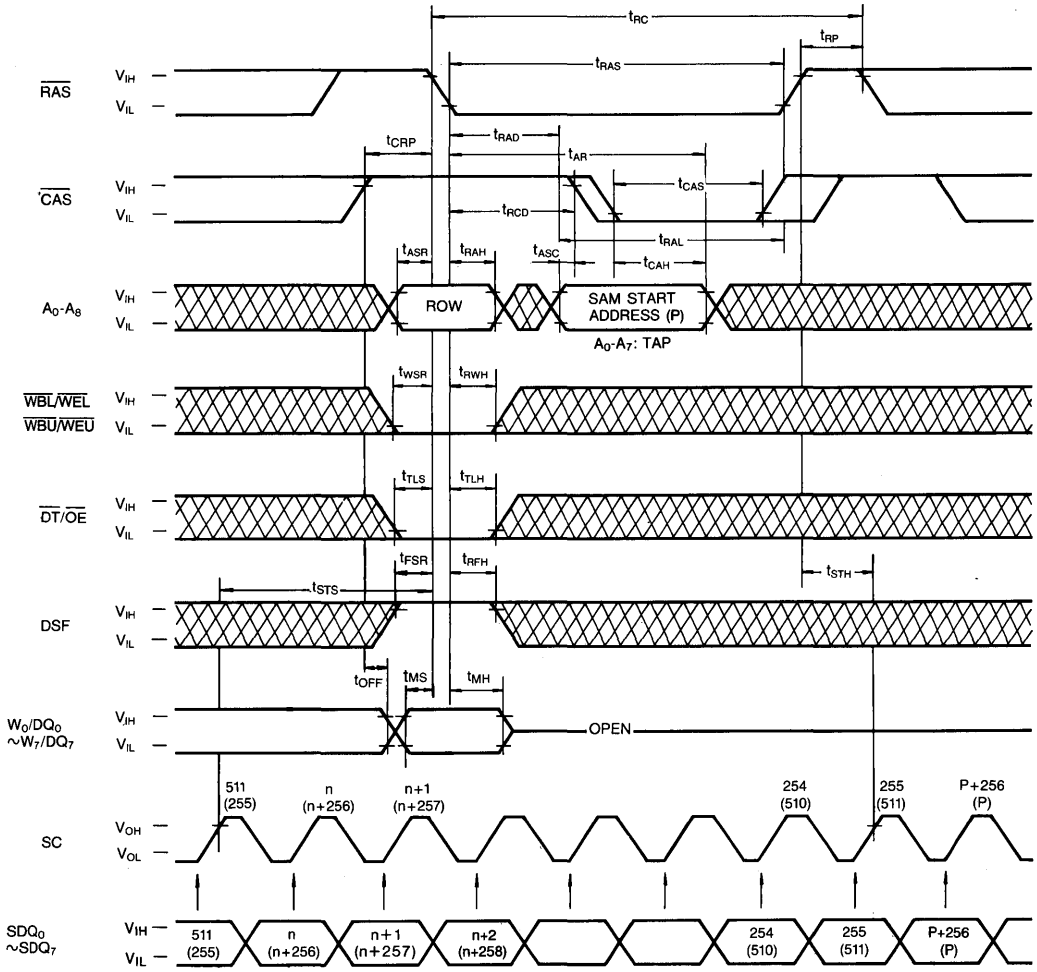
SPLIT READ TRANSFER CYCLE



Note: $\overline{SE}=V_{IL}$

Dont' Care

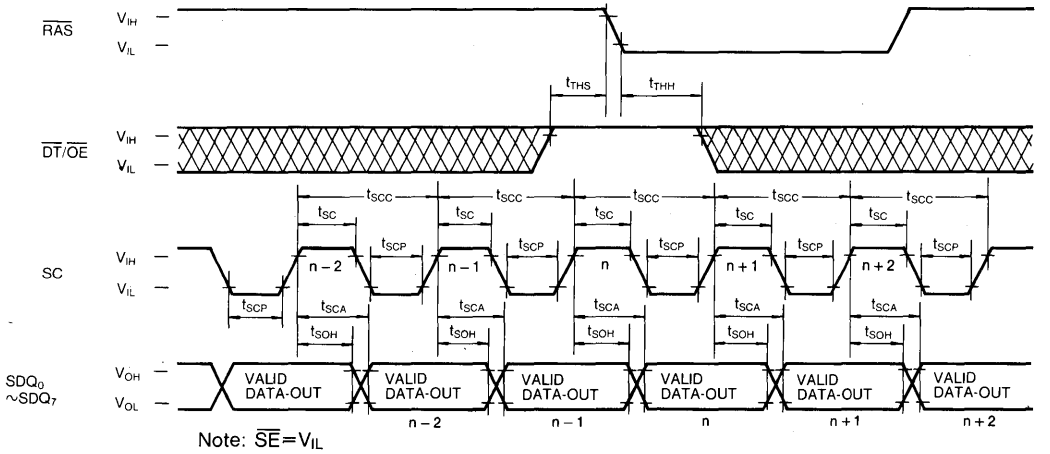
MASKED SPLIT WRITE TRANSFER CYCLE



$\overline{SE}$=VIL

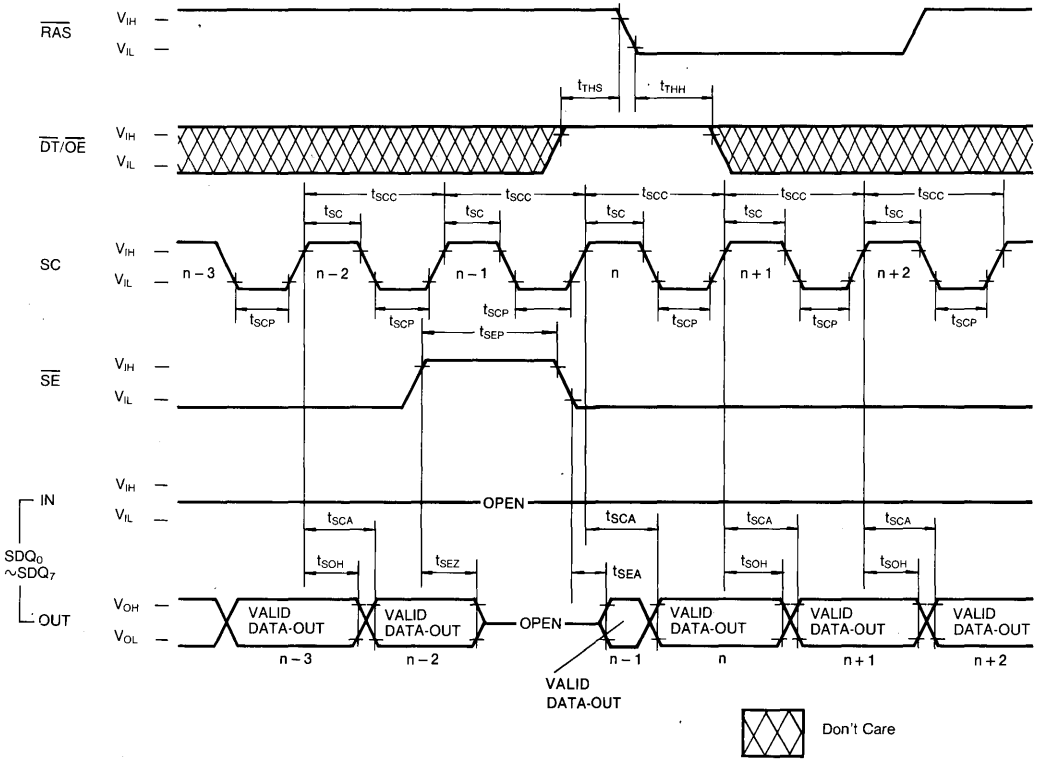
Don't Care

SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

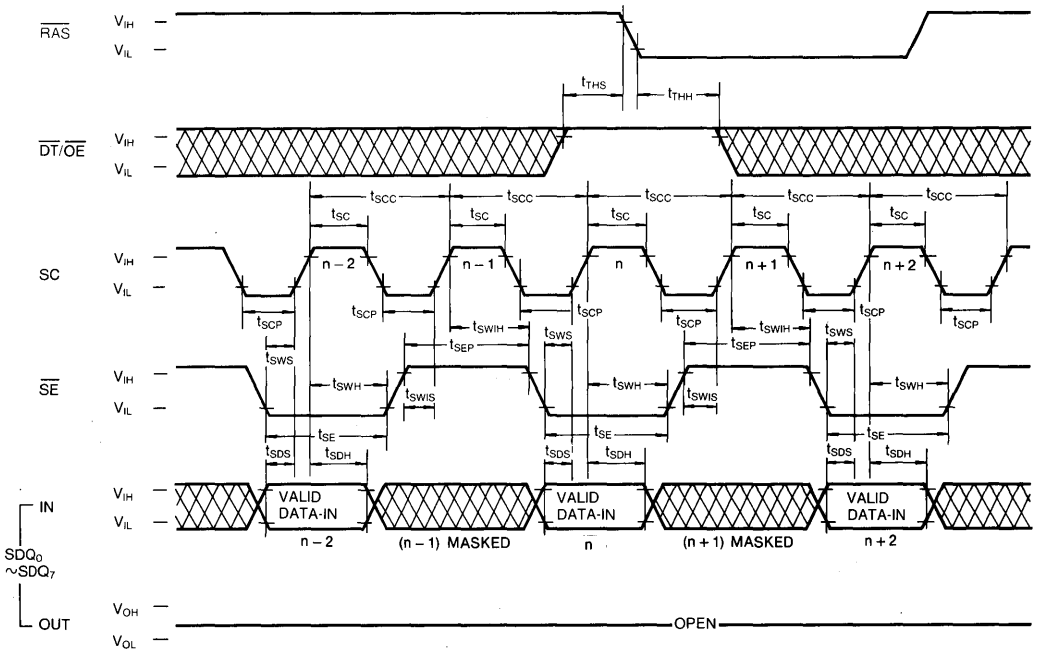


Note: $\overline{SE}$=V_{IL}

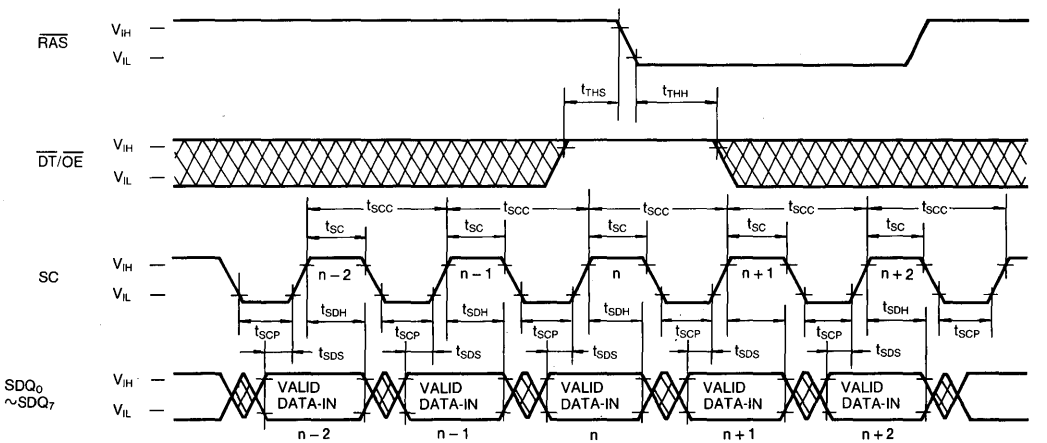
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



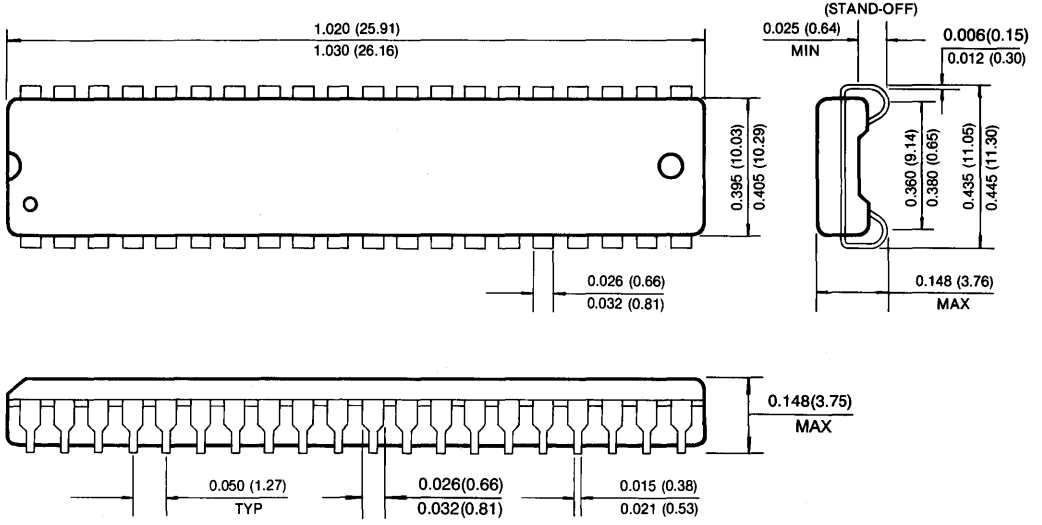
Note: $\overline{SE} = V_{IL}$

Don't Care

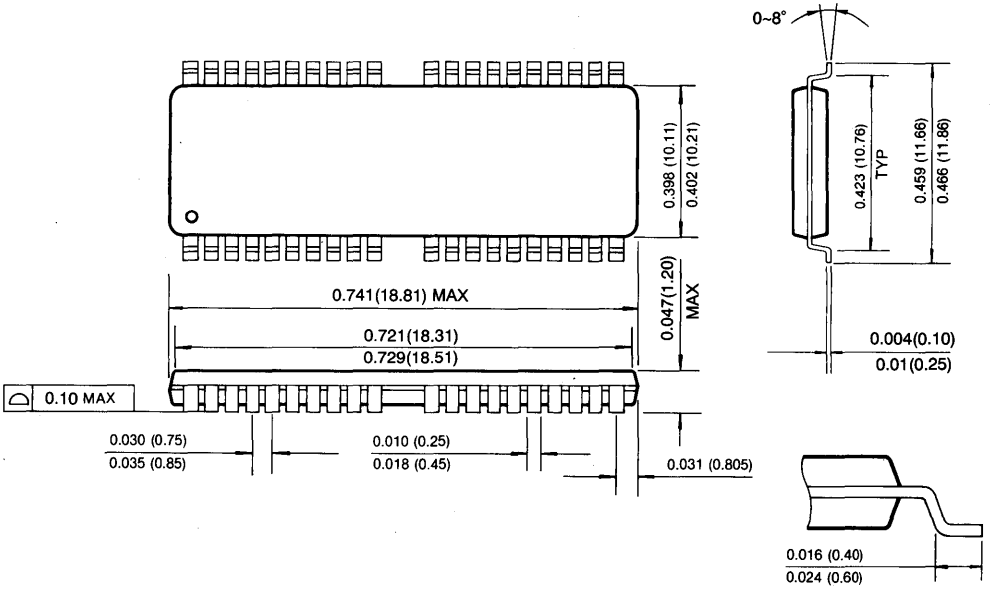
PACKAGE DIMENSIONS

40-PIN PLASTIC SOJ

Units: Inches (millimeters)



40/44-PIN PLASTIC TSOP-II (Forward Type)



256K × 16 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K × 16 bits RAM port
  512 × 16 bits SAM port
- **Performance range:**

Parameter \ Speed		-60	-70	-80
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{PC})	KM4216C255	40ns	45ns	50ns
	KM4216V255	40ns	45ns	50ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C255	120mA	110mA	100mA
	KM4216V255	110mA	100mA	90mA
SAM active current	KM4216C255	50mA	45mA	40mA
	KM4216V255	40mA	35mA	30mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **Byte/Word Write Operation**
- **8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single + 5V±10% Supply Voltage (KM4216C255)**
- **Single + 3.3V±10% Supply Voltage (KM4216V255)**
- **Plastic 64-Pin 525 mil SSOP (0.8mm pin pitch)**
- **Plastic 70-pin 400mil TSOP II(0.65mm pin pitch) (Forward and Reverse Type)**

- **Device Options** — **Part Marking**
  - **Low Power Dissipation**
    Extended CBR Refresh (64ms) — **L**
  - **Low Low Power Dissipation**
    Self Refresh (128ms) — **F**
- **Low Vcc(3.3V) Part Name: KM4216V255**

GENERAL DESCRIPTION

The Samsung KM4216C/V255 is a CMOS 256K × 16 bit Dual Port DRAM. It consists of a 256K × 16 dynamic random access memory (RAM) port and 512 × 16 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K × 16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access, Byte/word write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM ports using read, and programmable (Stop Register) Split Transfers.

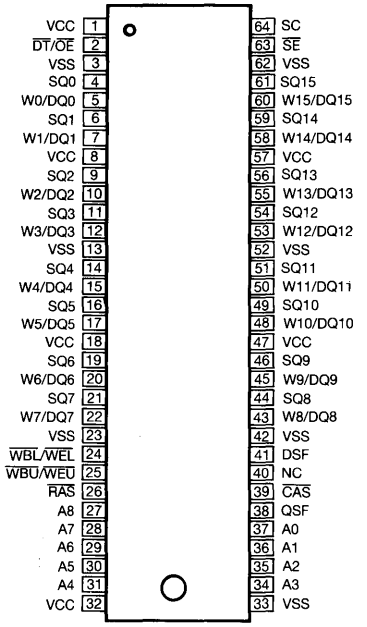
Refresh is accomplished by familiar DRAM refresh modes. The KM4216C/V255 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

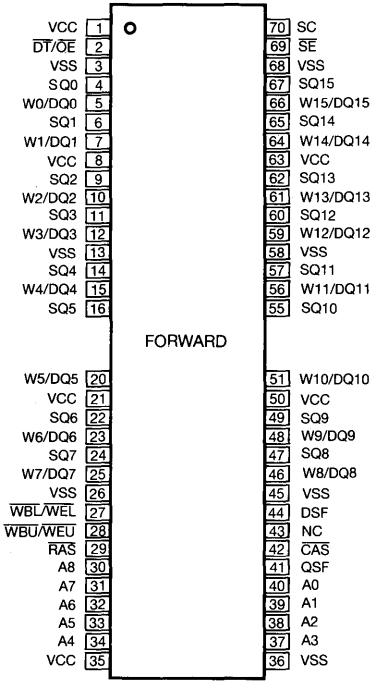
Pin Name		Pin Function
SC		Serial Clock
SQ_0-SQ_{15}		Serial Data Output
$\overline{DT/OE}$		Data Transfer/Output Enable
$\overline{WBL/WEL}$, $\overline{WBU/WEU}$		Write Per Bit/Write Enable (Lower /Upper)
$\overline{RAS}$		Row Address Strobe
$\overline{CAS}$		Column Address Strobe
W_0/DQ_0-W_{15}/DQ_{15}		Data Write Mask/Input/Output
$\overline{SE}$		Serial Enable
A_0-A_8		Address Inputs
DSF		Special Function Control
V_{CC}	KM4216C255	Power (+5V)
	KM4216V255	Power (+3.3V)
Vss		Ground
QSF		Special Flag Out
N.C		No Connection

PIN CONFIGURATION (TOP VIEWS)

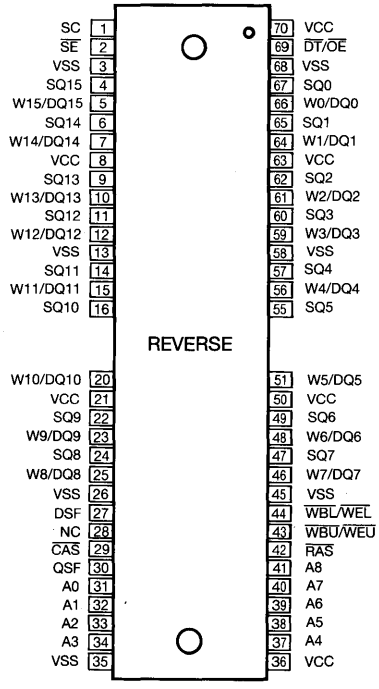
• **KM4216C/V255G/GL/GF**



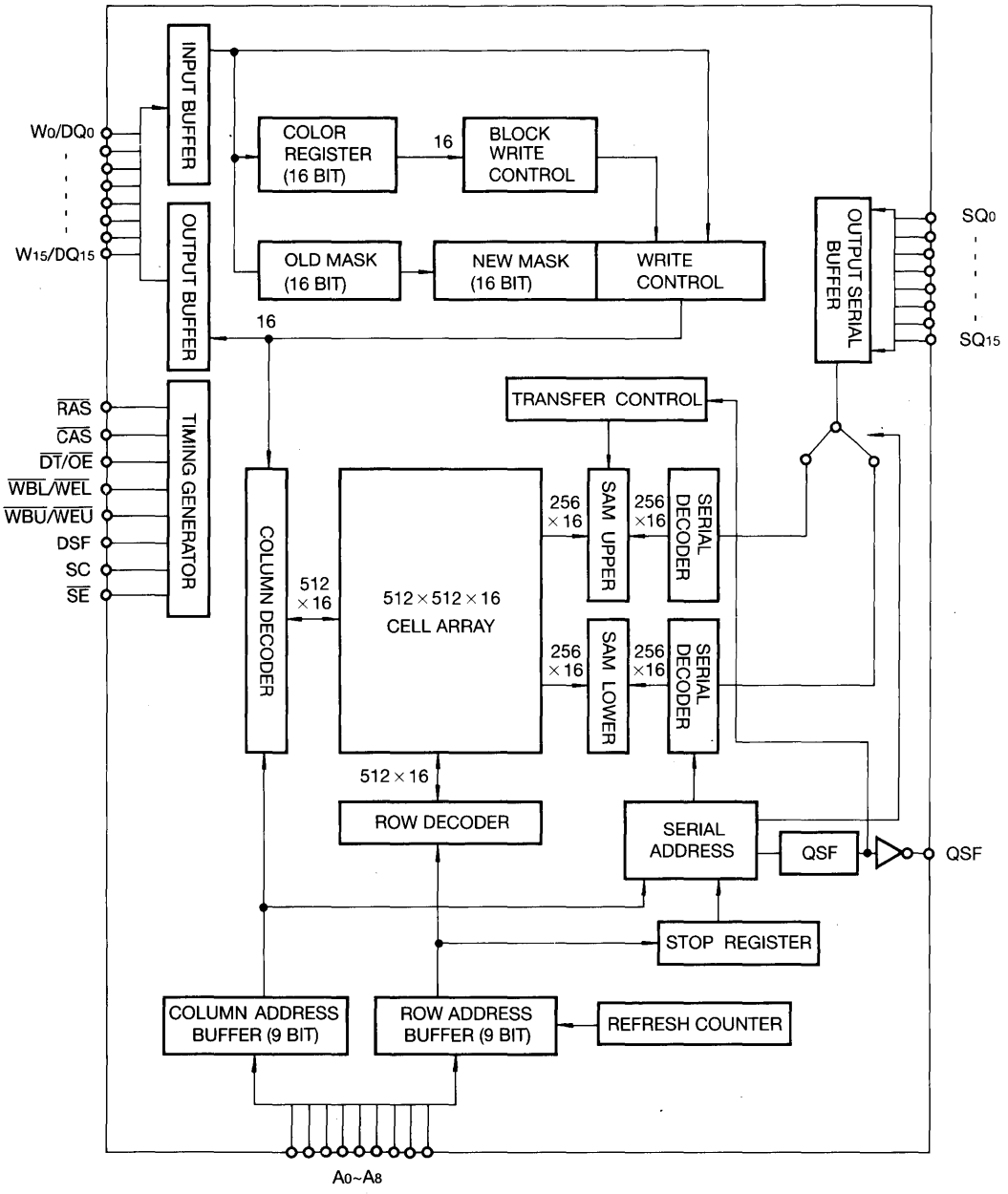
• **KM4216C/V255T/TL/TF**



• **KM4216C/V255R/RL/RF**



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS				CAS	Address		DQi Input		Register		Function
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS/WE}$	Mask	Color	
CBRS (Note 1.3)	0	×	0	1	-	Stop (Note4)	-	×	-	-	-	CBR Refresh/ Stop (No reset)
CBRN (Note 1)	0	×	1	1	-	×	-	×	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	×	×	0	-	×	-	×	-	-	-	CBR Refresh (Option reset)
ROR	1	1	×	0	-	ROW	-	×	-	-	-	RAS-only Refresh
RT	1	0	1	0	×	ROW	Tap	×	×	-	-	Read Transfer
SRT	1	0	1	1	×	ROW	Tap	×	×	-	-	Split Read Transfer
RWM	1	1	0	0	0	ROW	Col.	WMi	Data	Use	-	Masked write (New/Old Mask)
BWM	1	1	0	0	1	ROW	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New/Old Mask)
RW	1	1	1	0	0 (Note6)	ROW	Col.	×	Data	-	-	Read or Write
BW	1	1	1	0	1	ROW	Col.	×	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	ROW (Note7)	×	×	WMi	Load (Note5)	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	ROW (Note7)	×	×	Color		Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap:SAM Start (Column) Address, WMi : Write Mask Data (i=0~15)
RAS only refresh does not reset Stop or LMR functions.

Notes:
(1) CBRS, CBRN and CBRR all perform $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, CBRS or CBRN to perform $\overline{CAS}$-before-RAS refresh while using Old mask)
(3) After CBRS Cycle, SRT use STOP Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The ROW that is addressed will be refreshed, but a ROW address is not reguired.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C255	KM4216V255	
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to + 150	55 to +150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	KM4216C255			KM4216V255			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$+0.5(0.3*1) all other pins not under test=0 volts).	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V255

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless other wise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C255			KM4216V255			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1	Standby*4	I_{CC1}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)	Active	I_{CC1A}	160	145	130	140	125	110	mA
Standby Current	Standby*4	I_{CC2}	10	10	10	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$=$V_{IH}$	Active	I_{CC2A}	50	45	40	40	35	30	mA
DSF=V_{IL})	Standby*4	I_{CC2C}*2	200	200	200	200	200	200	μA
	Standby*4	I_{CC2C}*3	150	150	150	150	150	150	μA
$\overline{RAS}$ Only Refresh Current*1	Standby*4	I_{CC3}	120	110	100	110	100	90	mA
($\overline{CAS}$-V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min	Active	I_{CC3A}	160	145	130	140	125	110	mA
Fast Page Mode Current*1	Standby*4	I_{CC4}	110	100	90	100	90	80	mA
($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cyciing @t_{PC}=min	Active	I_{CC4A}	150	135	120	130	115	110	mA
$\overline{CAS}$ Before-$\overline{RAS}$ Refresh Current*1	Standby*4	I_{CC5}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min	Active	I_{CC5A}	160	145	130	140	125	110	mA
Data Transfer Current *1	Standby*4	I_{CC6}	140	130	120	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC6A}	180	165	150	160	145	130	mA
Block Write Cycle Current *1	Standby*4	I_{CC7}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC7A}	160	145	130	140	125	110	mA
Color Register Load Current *1	Standby*4	I_{CC8}	110	90	80	90	80	70	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC8A}	140	125	110	120	105	90	mA
Battery Back Up Current *2 $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycling or $\leq V_{IL}$ $\overline{RAS}$=t_{RAS}(min) to 1μs t_{RC}=125 μs (64ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF$\geq V_{IH}$ or$\leq V_{IL}$	Standby*4	I_{CC9}	300	300	300	300	300	300	μA
Self Refresh Current *3 $\overline{RAS}$,$\overline{CAS}\leq$0.2V(128ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, A_0~A_8, DSF$\geq V_{CC}$ - 0.2v or$\leq$0.2V DQ0~15=V_{CC}-0.2V, 0.2V or OPEN	Standby*4	I_{CC10}	250	250	250	250	250	250	μA

Note *1 Real values dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, adress transition should be changed only once while $\overline{RAS}$=V_{IL}.

In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$=V_{IH}

*2 KM4216C255L only : $V_{IH}\geq V_{CC}$-0.2V, $V_{IL}\leq$0.2V

*3 KM4216C255F only : $V_{IH}\geq V_{CC}$ -0.2V, $V_{IL}\leq$0.2V,

*4 SAM Standby Condition : $\overline{SE}\geq V_{IH}$, SC$\leq V_{IL}$ or $\geq V_{IH}$

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM4216C255 : V_{CC}=5.0V±10%, KM4216V255 : 3.3V±10%,)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		200		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,6
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		12		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		12		15		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	tAWD	50		55		60		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
$\overline{RAS}$ hold time referenced to OE	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output Buffer turn-off delay from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	10		10		15		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	0		0		0		ns	15
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (real time read transfer)	tCTH	15		20		25		ns	
$\overline{DT}$ low hold referenced to column address (real time read transfer)	tATH	20		25		30		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	tRSD	60		70		80		ns	

AC CHARACTERISTICS (Continued)

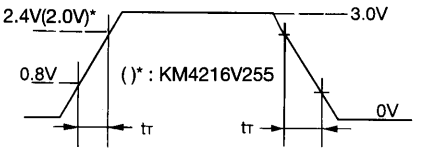
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to first SC delay (read transfer)	tCSD	25		30		35		ns	
Col. Address to first SC delay (read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	tTSD	10		10		15		ns	
LAST SC to $\overline{RAS}$ set-up time	tSRS	20		20		20		ns	
SC cycle time	tSCC	18		20		25		ns	14
SC pulse width (SC high time)	tSC	5		7		7		ns	
SC precharge (SC low time)	tSCP	5		7		7	20	ns	
Access time from SC	tSCA		15		17			ns	4
Serial output hold time from SC	tSOH	5		5		5	20	ns	
Access time from $\overline{SE}$	tSEA		15		17			ns	4
$\overline{SE}$ pulse width	tSE	20		20		25		ns	
$\overline{SE}$ precharge time	tSEP	20		20		25	15	ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0		ns	7
Split transfer set-up time	tSTS	20		25		25		ns	
Split transfer hold time	tSTH	20		25		25	25	ns	
SC-QSF delay time	tSQD		20		25		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		25		80	ns	
$\overline{RAS}$-QSF delay time	tRQD		70		75		40	ns	
$\overline{CAS}$-QSF delay time	tCQD		35		35			ns	
$\overline{DT}$ to $\overline{RAS}$ Prechange time	tTRP	40		50		60		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ 8 SC cycles before proper device operation is achieved.($\overline{DT}/\overline{OE}$=High) if the intenal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required in stead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input siganl transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1TTL load and 50pF.
   D_{OUT} Comparator level : V_{OH}/V_{OL}=2.0V/0.8V.
4. SAM port outputs are measured with a load equivalent to 1TTL load and 30pF.
   D_{OUT} comparator level:V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below

Pin or REGISTER	STATUS
QSF	Hi-Z
Color Registe	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SDQi	Hi-Z

13. Recommended operating input condition.



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=5.0ns
14. Assume t_T=3ns.
15. Self refresh parameter (KM4216C/V255F)
    512K cycle of burst refresh must be executed within 8ms before and after self-refresh in order to meet refresh specification.

DEVICE OPERATION

The KM4216C/V255 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V255 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$). the column address strobe($\overline{CAS}$) and the valid row and coumn address inputs.

Operation of the KM4216C/V255 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This the beginning of any KM4216C/V255 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V255 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$,$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.
If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then tne access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}
The KM4216C/V255 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Byte Write Operation

The KM4216C/V255 has 2 write control pin, $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$, and offers asynchronous write operation with lower byte (W_0/DQ_0~W_7/DQ_7) and upper byte (W_8/DQ_8~W_{15}/DQ_{15}). This is called Byte Write operation. This operation can be performed in RAM write, Block write, Load Mask register, and Load Color register.

Fast Page Mode

The KM4216C/V255 has Fast Page mode capbility provides high speed read, write or read-modify-write access to all memory locations Within a selected row. In this cycle, read, write, read-modify write, and block write cycles can be mixed in any order.
In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequental addresses for the same page.

New Masked Write Per Bit

The New Masked Write Per Bit cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low. writing is inhibited into the RAM and the mask data is high, data is written into the RAM.
The mask data is valid for only one cycle. Mask data must be provided in every write cycle that a masking operation is desired.
The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ low after $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

If $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed (see Figure1, 2). And If $\overline{WBL}/\overline{WEL}$ is high during $\overline{CAS}$ low, write operation of lower byte do not perform and if $\overline{WBU}/\overline{WEU}$ is high, write operation of upper byte do not execute.

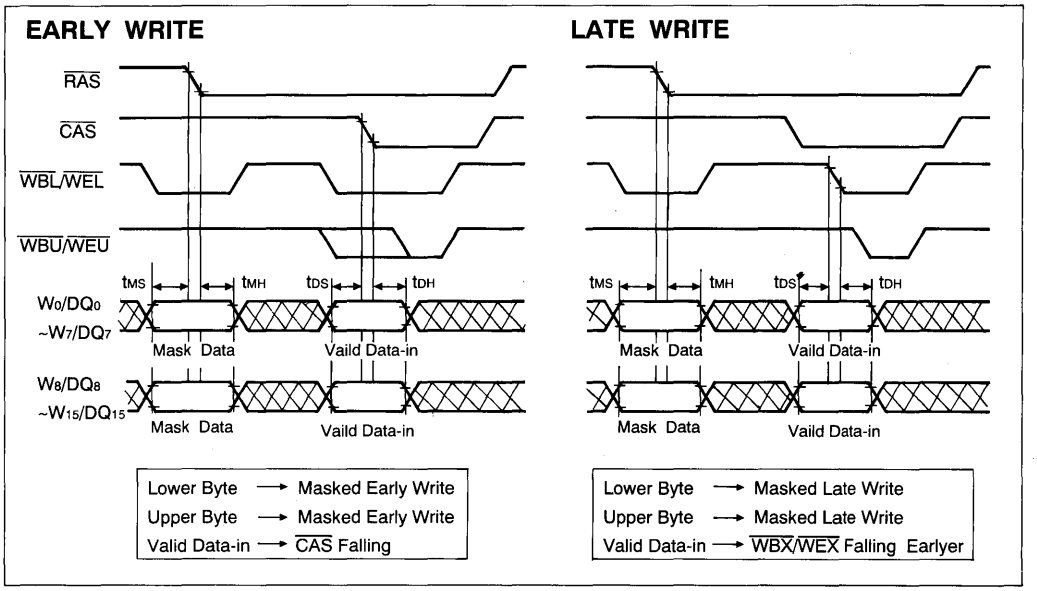


Figure 1. Byte Write and New Masked Write Cycle Example 1. (Early Write & Late Write)

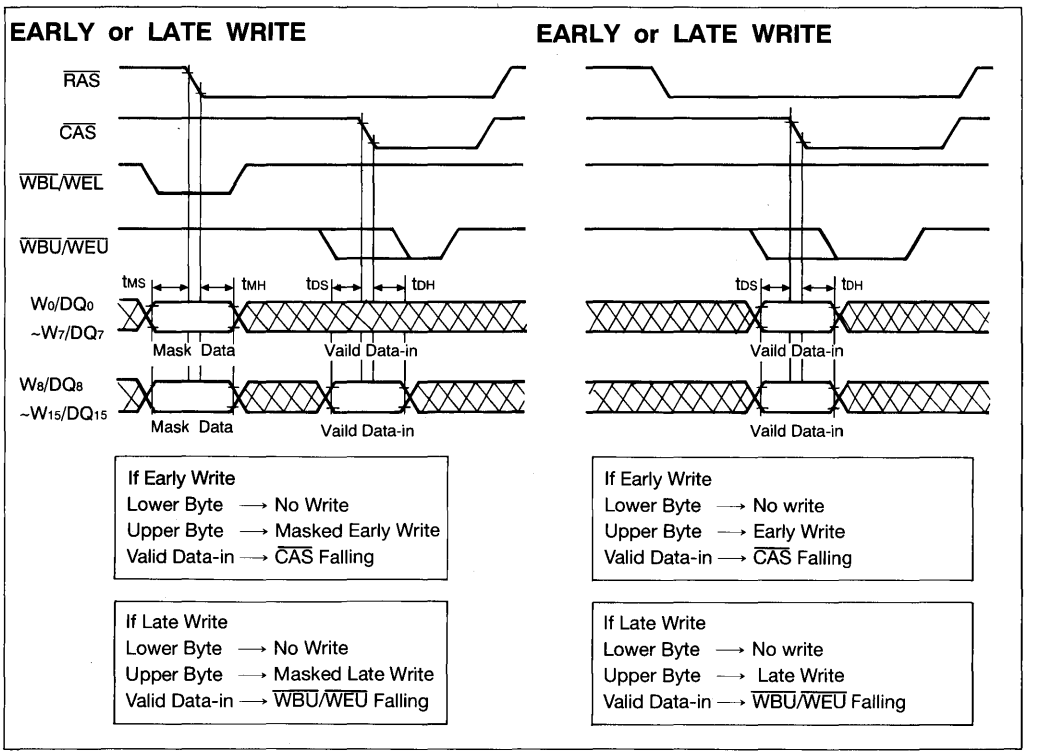


Figure 2. Byte Write and New Masked Write Cycle Example 2.

DEVICE OPERATION (continued)

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

The LMR cycle is performed if DSF high, $\overline{WB}/\overline{WE}$ high at the $\overline{RAS}$ falling edge and DSF low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM4216C/V255 are set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked write are Old Masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register (See Figure 3.)

The mask data is applied in the same manner as in New Masked write Per Bit mode.

Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After power-up, the KM4216C/V255 initializes in the New Masked write mode.

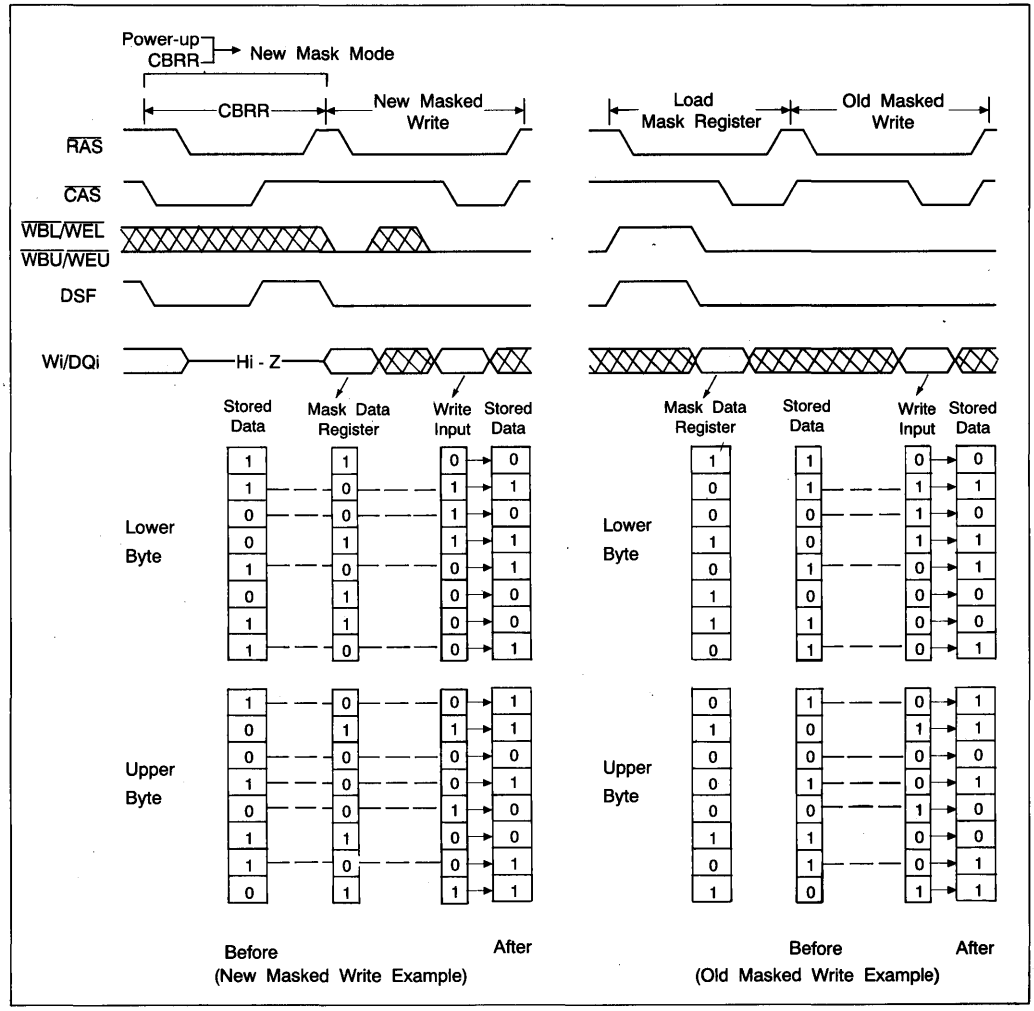


Figure 3. New Masked Write Cycle and Old Masked Write Cycle Example

DEVICE OPERATION (continued)

Load Color Register(LCR)

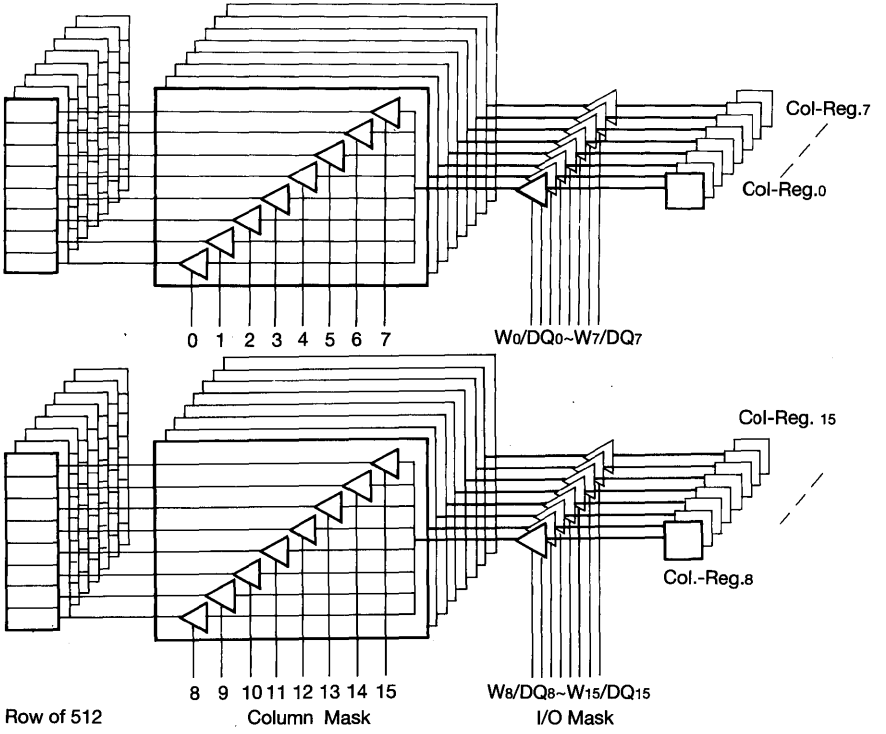
A Load Color register cycle is performed by keeping DSF high on the both falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded in the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(late write) via the W_0/DQ_0~w_7/DQ_7(Lower Byte), W_8/DQ_8~W_{15}/DQ_{15} (Upper Byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register Cycle.

Block Write

In a Block write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each corresponding bit plane(16). This results in a total of of 128-bits being written in a single Block write cycle campared to 16-bits in a normal write cycle.

The Block write cycle is performed if DSF is low at the falling edge of $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



	$\overline{RAS}$
W_0/DQ_0~7	Lower Block I/O Mask
W_8/DQ_8~15	Upper Block I/O Mask

	$\overline{CAS}$
A_0~A_2	Don't Care
W_0/DQ_0~7	Lower Block Column Select
W_8/DQ_8~15	Upper Block Column Select

A_2~A_0	Lower	Upper	Column Mask	
0 0 0	W_0/DQ_0	W_8/DQ_8		
0 0 1	W_1/DQ_1	W_9/DQ_9	DQi=1	Column
0 1 0	W_2/DQ_2	W_{10}/DQ_{10}		Enable
0 1 1	W_3/DQ_3	W_{11}/DQ_{11}		
1 0 0	W_4/DQ_4	W_{12}/DQ_{12}		
1 0 1	W_5/DQ_5	W_{13}/DQ_{13}	DQi=0	Column
1 1 0	W_6/DQ_6	W_{14}/DQ_{14}		Disable
1 1 1	W_7/DQ_7	W_{15}/DQ_{15}		

Figure 4. Block Write Scheme

DEVICE OPERATION (continued)

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.
Since 8 columns are being written at a time, the minimum increment required for the column address is latched on the falling edge of $\overline{CAS}$, the 3 LSBs, A_0, A_1, and A_2 are ignored and only bits (A_3~A_8) are used to define the location of the first bit out of the eight to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16 -bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the eight, but the second remains unchanged. Fig. 4 shows the correspondence of each data line to the column mask bits.
A Masked Block Write cycle is identical to a New/old Masked Write-Per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. And DSF must be high on the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0~W_{15}/DQ_{15} pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. In old mask mode, I/O mask data will be provided by the Mask Data Register.

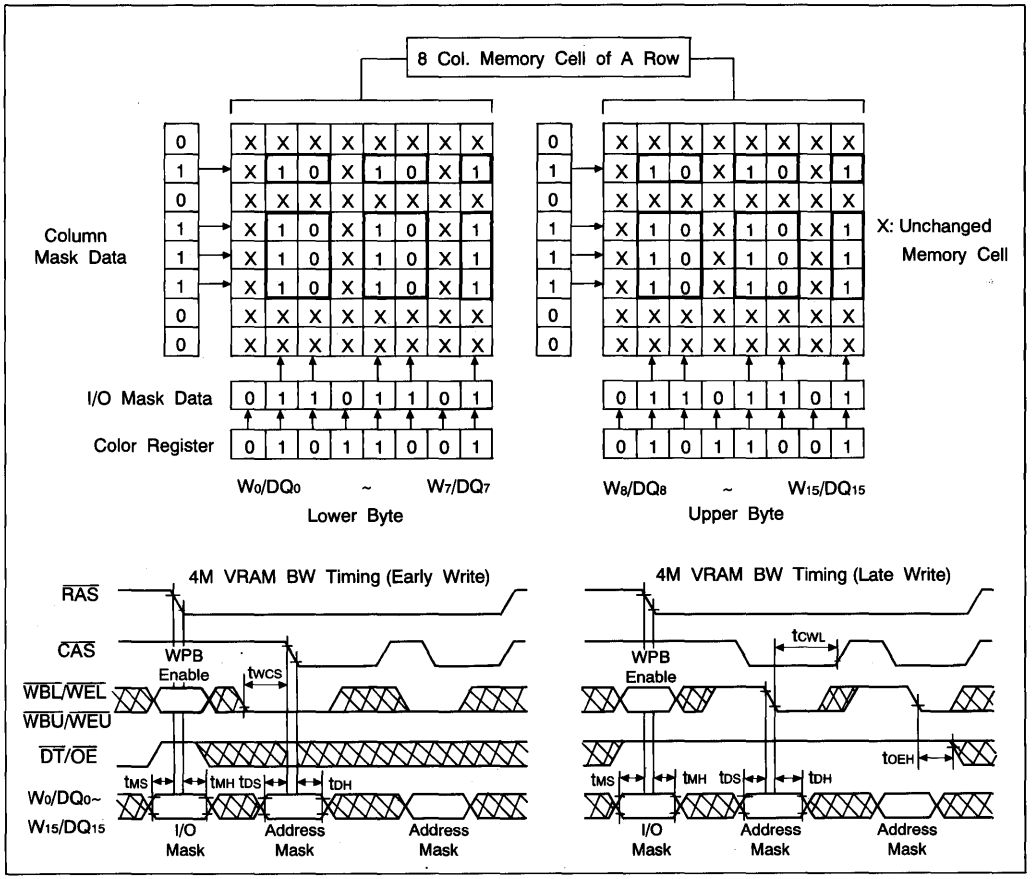


Figure 5. Block Write Example and Timing

DEVICE OPERATIONS (Continued)

Data Output

The KM4216C/V255 has three state output buffer Controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}$,$\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is in high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output duing the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V255 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM4216C/V255 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled.
An internal refresh operatian occurs automatically. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
The KM4216C/V255 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation ; CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default valuse.
CBRN (CBR refresh without reset) is set if DSF high when $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$ is high at the falling edge of $\overline{RAS}$ and simply do only refresh operation.
CRRS(CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V255 hidden refresh cycle is actually a $\overline{CAS}$-beford-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Self Refresh *(Only KM4216C/V255F)*: The Self Refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for longer periods of standby, such as a battery back-up. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If $\overline{RAS}$ is low more than 100μs at the condition of CBR, Self Refresh function is accomplished. In this state, the external refresh address do not need to supply additionally on-chip because the refresh counter on-chip gives that addresses needed to refresh. Please note that the ending point of Self Refresh is when $\overline{RAS}$ and $\overline{CAS}$ is high and t_{RPS} of Self Refresh is the time requiring to complete the last refresh of Self Refresh.

Other Refresh Methods : It is also possible to refresh the KM4216C/V255 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS (Continued)

Table 1. Truth Table for Transfer Operation *: Don't care

RAS Falling Edgd					Function	Transfer Direction	Transfer Data Bit
CAS	DT/OE	WB/WE	DSF	SE			
H	L	H	L	*	Read Transfer	RAM→SAM	512 × 16
H	L	H	H	*	Split Read Transfer	RAM→SAM	256 × 16

Transfer Operation

Transfer operation is initiated when $\overline{DT/OE}$ is low at the falling edge of $\overline{RAS}$. The state of DSF when $\overline{RAS}$ goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation. (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT/OE}$ is low, $\overline{WB/WE}$ is high, and DSF is low at the falling edge of $\overline{RAS}$. The row address bits in the read transfer cycle indicate which sixteen 512 bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operationn, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half). Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC, $\overline{DT/OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT/OE}$ must be Synchronized with the rising edge of SC (t_{TSL}/t_{TSD}) to retain the continuity of Serial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT/OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, $\overline{DT/OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT/OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT/OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$.

DEVICE OPERATIONS (Continued)

Address: The row address is latched in the falling edge of $\overline{RAS}$. The column address defined by (A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. column addrress pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1= Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g.255th or 511th bit).

Example of SRT applications are shown in Fig.6 through Fig. 9

The normal usage of Split Read Transfer cycle is described in Fig.6. When Read Transfer is executed, data from X_1 row address is fully transferred to the SAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X_2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y_0" Tap address instead of "Y_0" is loaded.

The another example of SRT cycle is described in Fig.7 When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 8 and 10 are the exanple of abnormal SRT cycle.

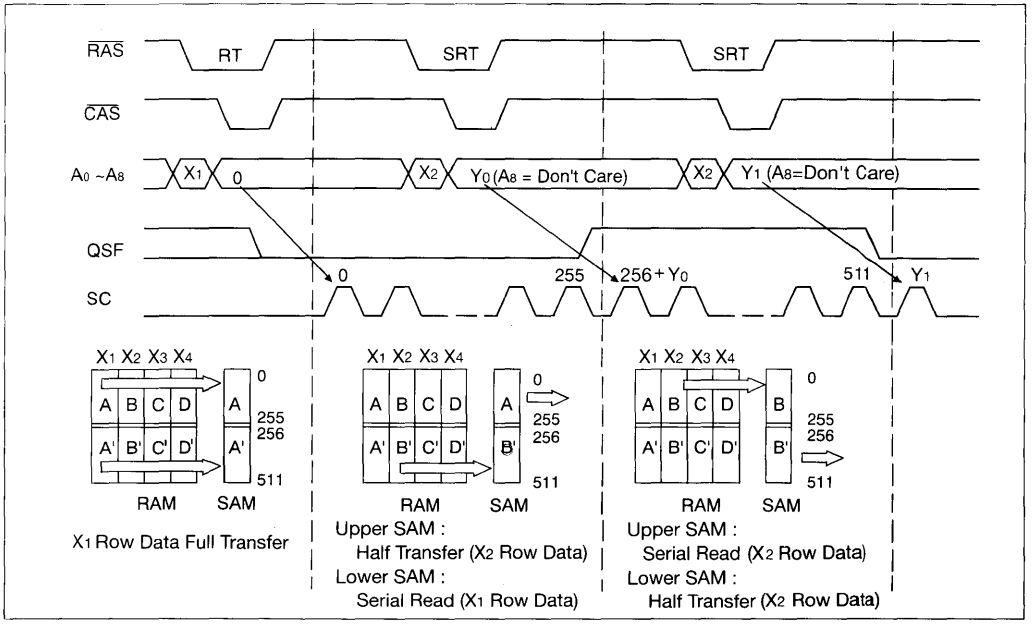


Figure 6. Split Read Transfer Normal Usage (Case1)

DEVICE OPERATIONS (Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig.8, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 9 indicates that SRT cycle is not performed until Serial Read is completed to the boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+ t_{STS}(See Figure 10.)

A split Read Transfer does not change the direction of the SAM I/O port.

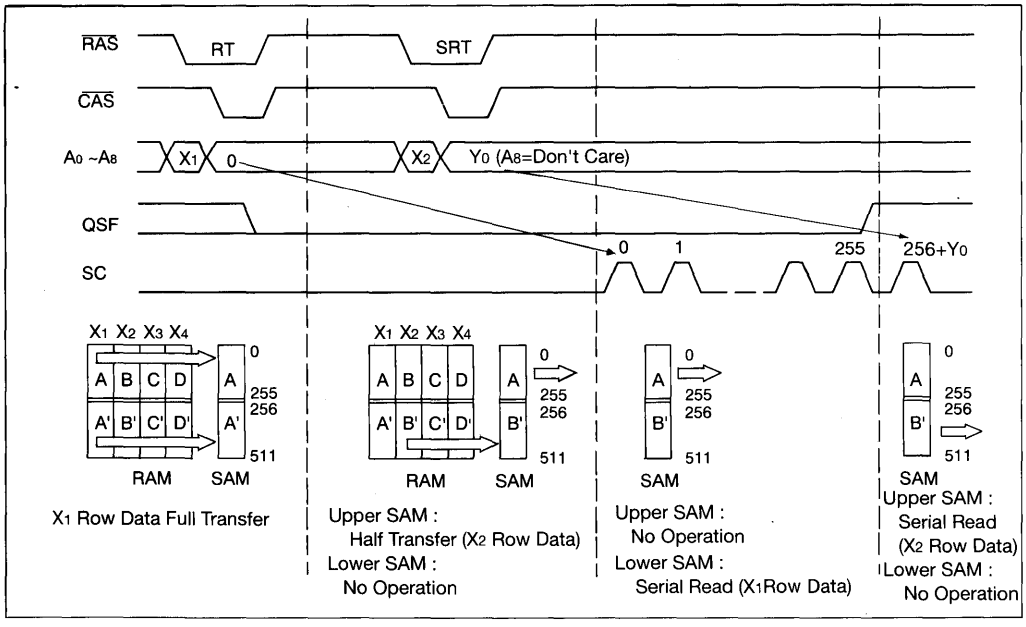


Figure 7. Split Read Transfer Normal Usage (Case 2)

DEVICE OPERATIONS (Continued)

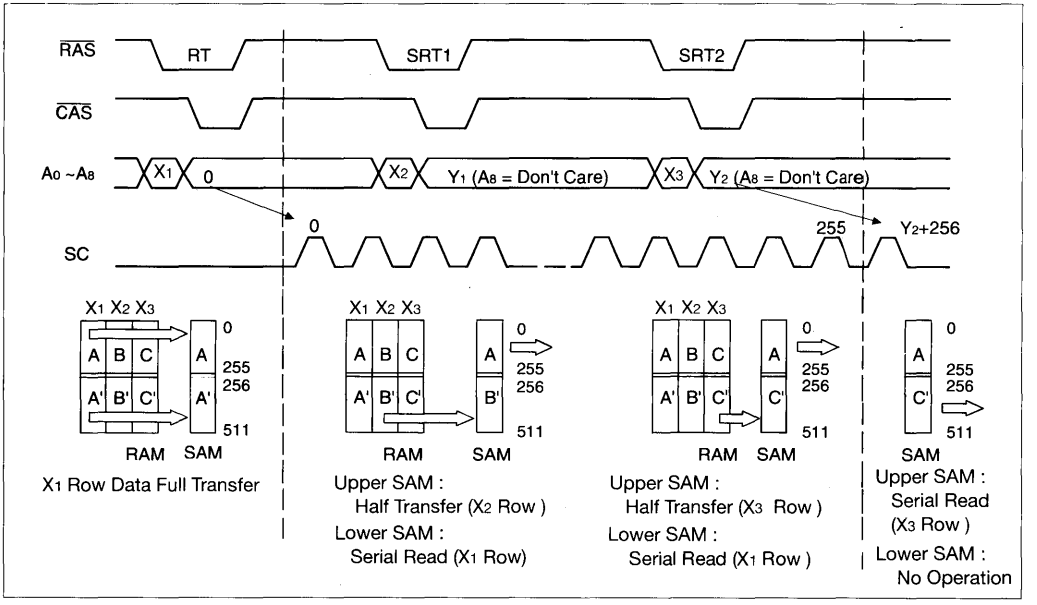


Figure 8. Split Read Transfer Abnormal Usage (Case 1)

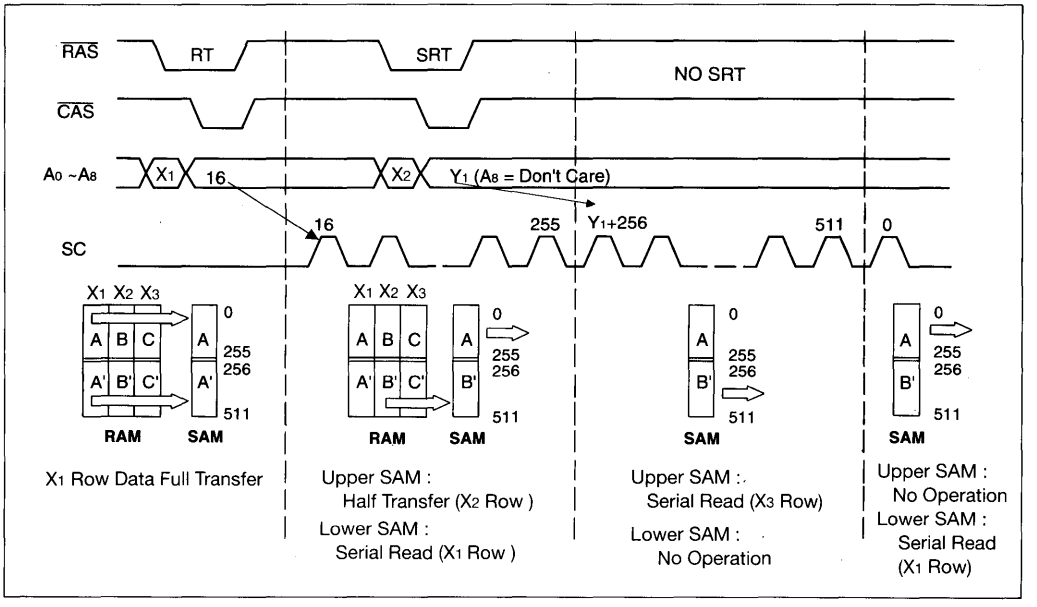


Figure 9. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATIONS (Continued)

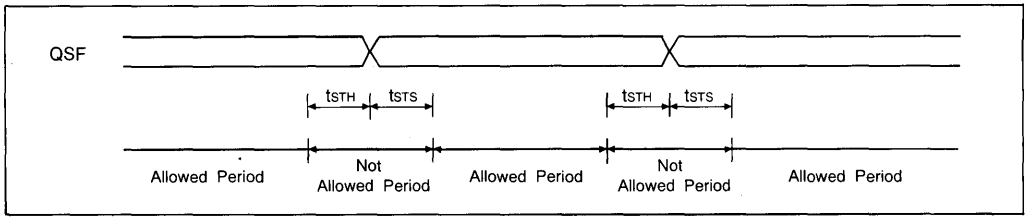


Figure 10. Split Transfer Cycle Limitation Period

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half.
After the last address of each half SAM(255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded TAP address).
This last address is called Stop Point.
The KM4216C/V255 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is WBL/WEL or WBU/WEU low, DSF high at the falling edge of RAS in CBR cycle and the Stop Point is determined by row address entering at this time.
The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.
In Figure 11. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address(70) of the next half. Otherwise, the axxess will continue in the same half until a SRT occurs or the SAM half boundary (255, 511).
Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. DBRR is a CBR cycle with DSF low at the falling edge of RAS. The CBRR wil take effect immediately; it does not require a SRT to become active valid.

Table 2. Stop Point Setting Address

Stop Register= Store Address of Serial Access
Use on the Split Transter Cycle
Stop Pointer Set → CBRS Cycle

Number of Stop Points/Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3-A_0
1	(1×256)×2	x	1	1	1	1	x
2	(2×128)×2	x	0	1	1	1	x
4	(4×64)×2	x	0	0	1	1	x
8	(8×32)×2	x	0	0	0	1	x
16	(16×16)×2	x	0	0	0	0	x

*Other Case=Inhibit
X=Don't Care

DEVICE OPERATIONS (Continued)

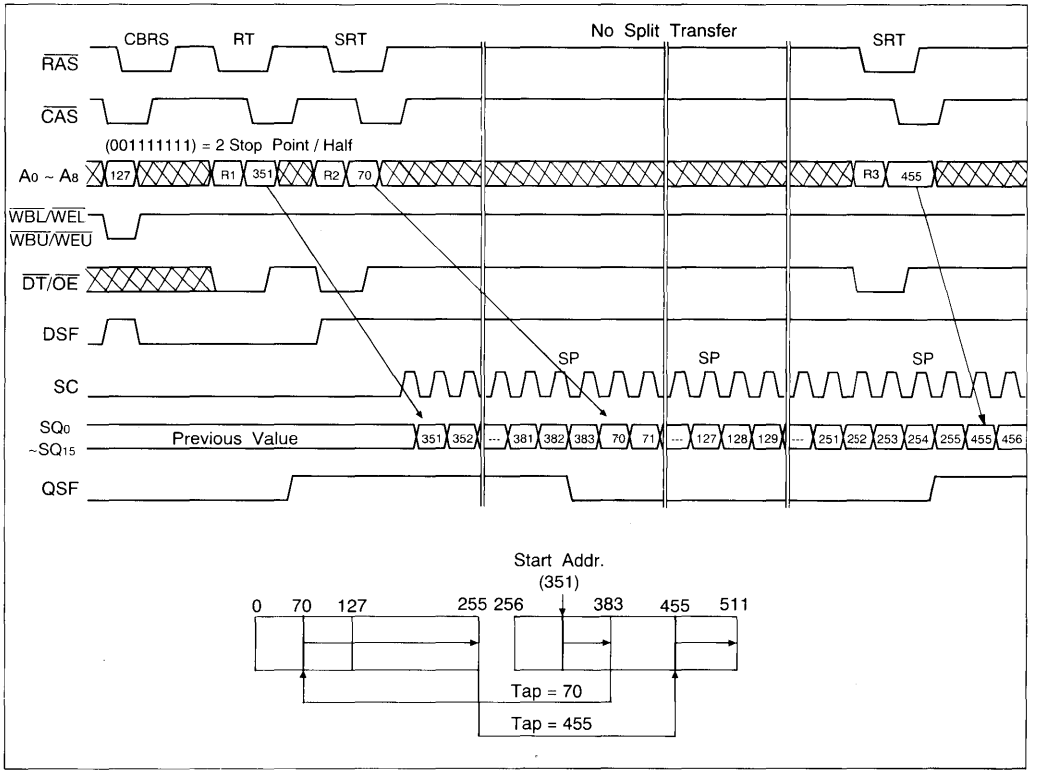
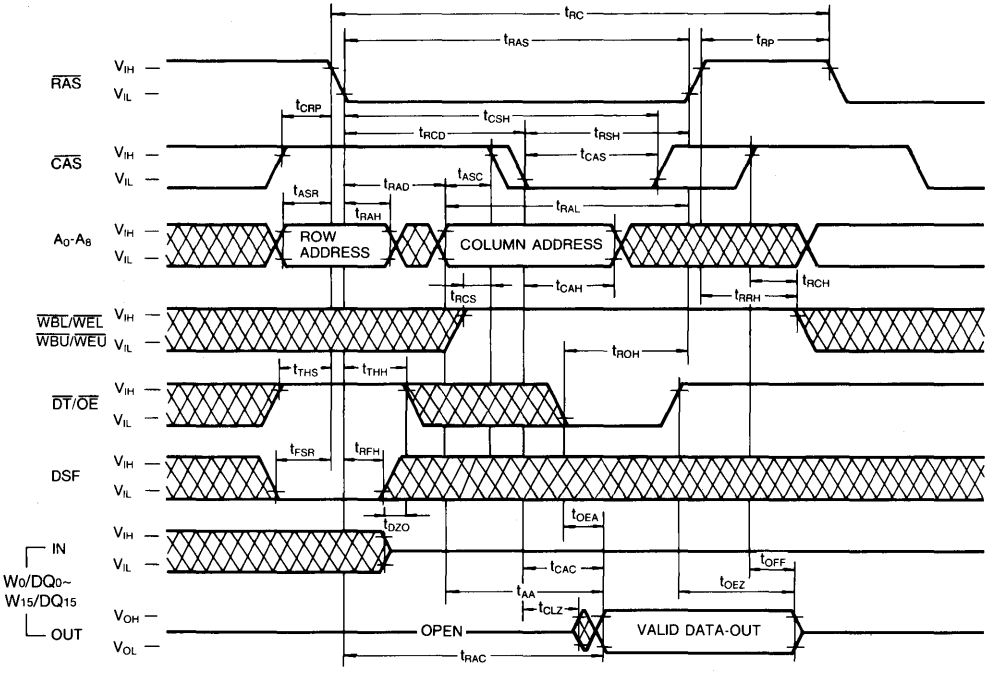


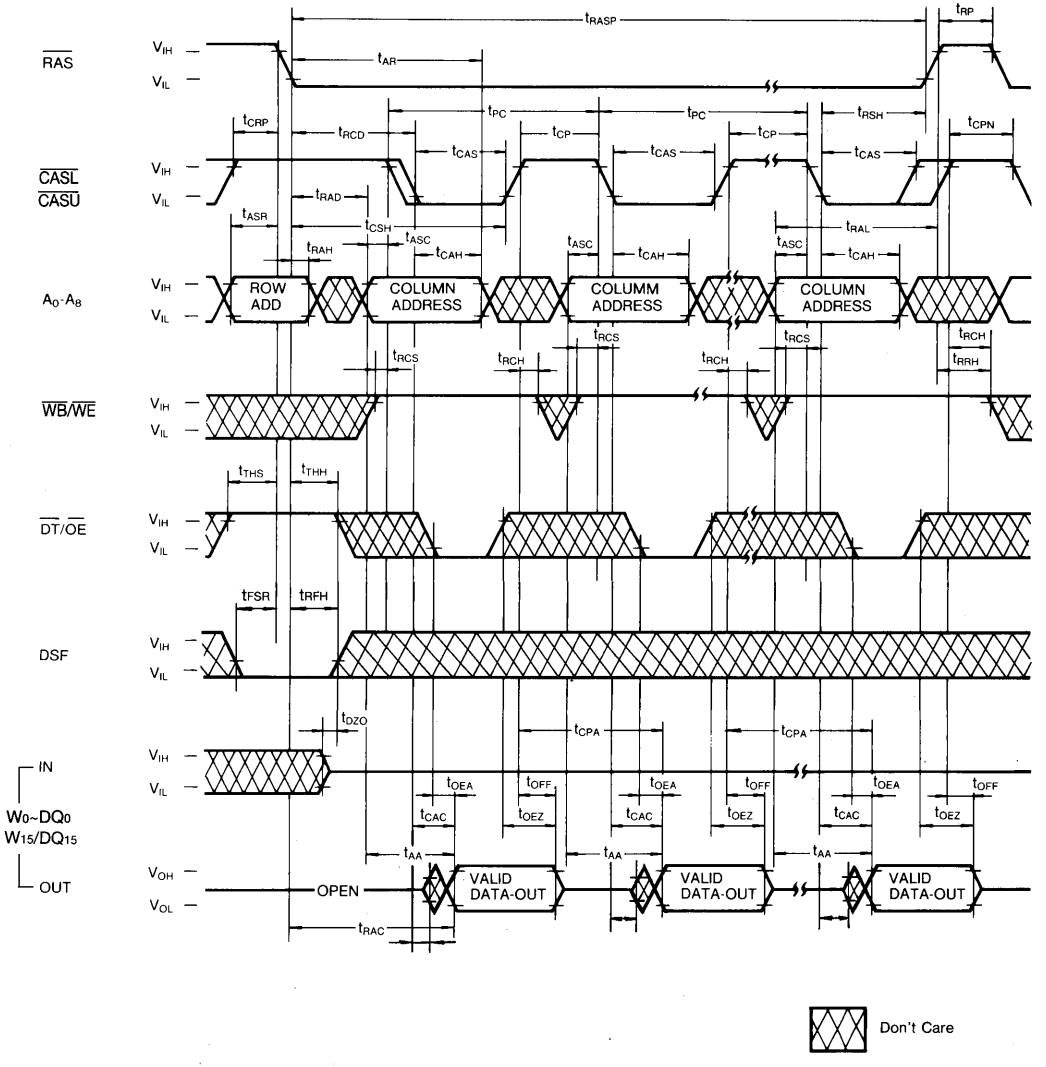
Figure 11. Programmable Split SAM operation

TIMING DIAGRAMS

READ CYCLE



FAST PAGE MODE READ CYCLE



Truth Table for Write Cycle(1)

FUNCTION	RAS ↓			CAS ↓	CAS ↓ or WBL(U)/WEL(U)
	*1 WBL/WEL (WBU/WEU)	*2 DSF	*3 Wi/DQi (3) (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask) (4)	1	0	×	1	Column Mask
Masked Block Write (4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register (2)	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram on the following pages
(2) Old Mask data load
(3) Function table for Old Mask and New Mask

IF		*1		*3	Note
		WBL/WEL	WBU/WEU	Wi/DQi	
LMR Cycle Executed	Yes	0	0	×	Write using mask register data (Old Mask Data)
		0	1	×	
		1	0	×	
		1	1	×	Non Masked Write
	No	0	0	Write Mask	Write using New Mask Data
		0	1		Wi/DQi=0 Write Disable
		1	0		Wi/DQi=1 Write Enable
		1	1	×	Non Masked Write

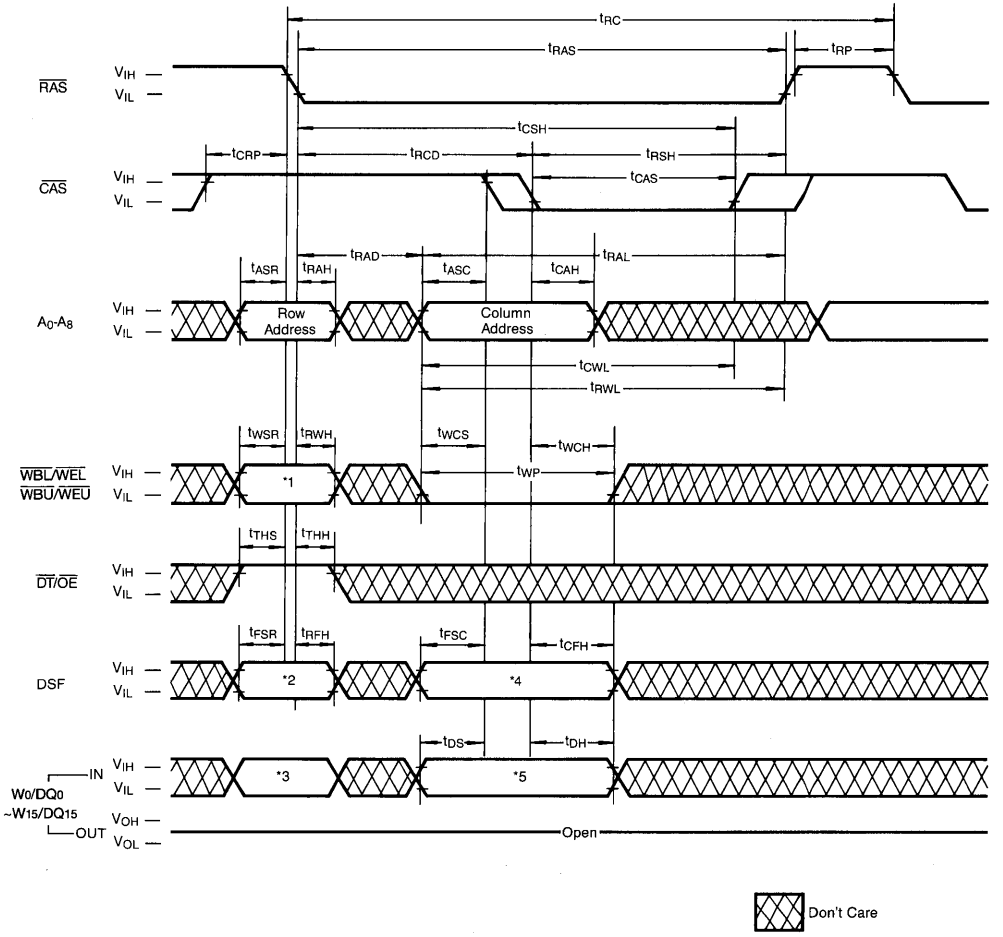
× : Don't Care

(4) Function Table for Block Write Column Mask

Column Address		
A2	A1	A0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

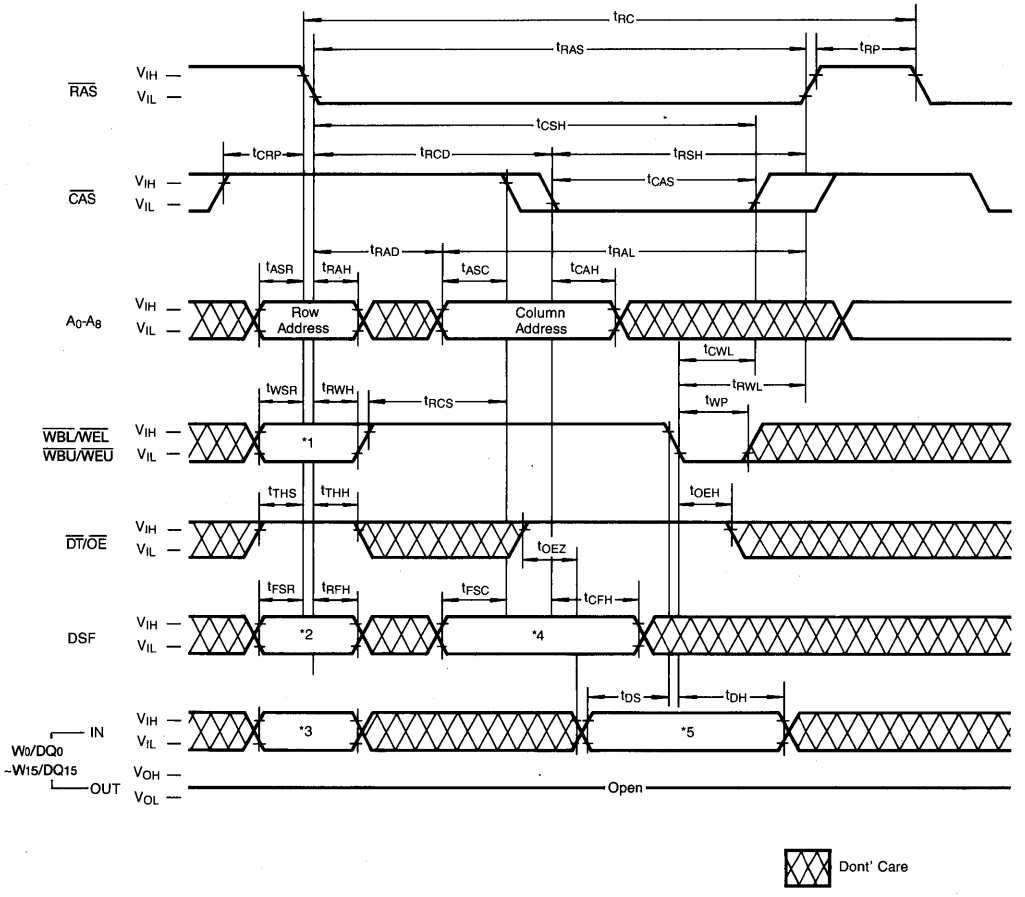
*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W0/DQ0	W8/DQ8	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
W1/DQ1	W9/DQ9		
W2/DQ2	W10/DQ10		
W3/DQ3	W11/DQ11		
W4/DQ4	W12/DQ12		
W5/DQ5	W13/DQ13		
W6/DQ6	W14/DQ14		
W7/DQ7	W15/DQ15		

EARLY WRITE CYCLE



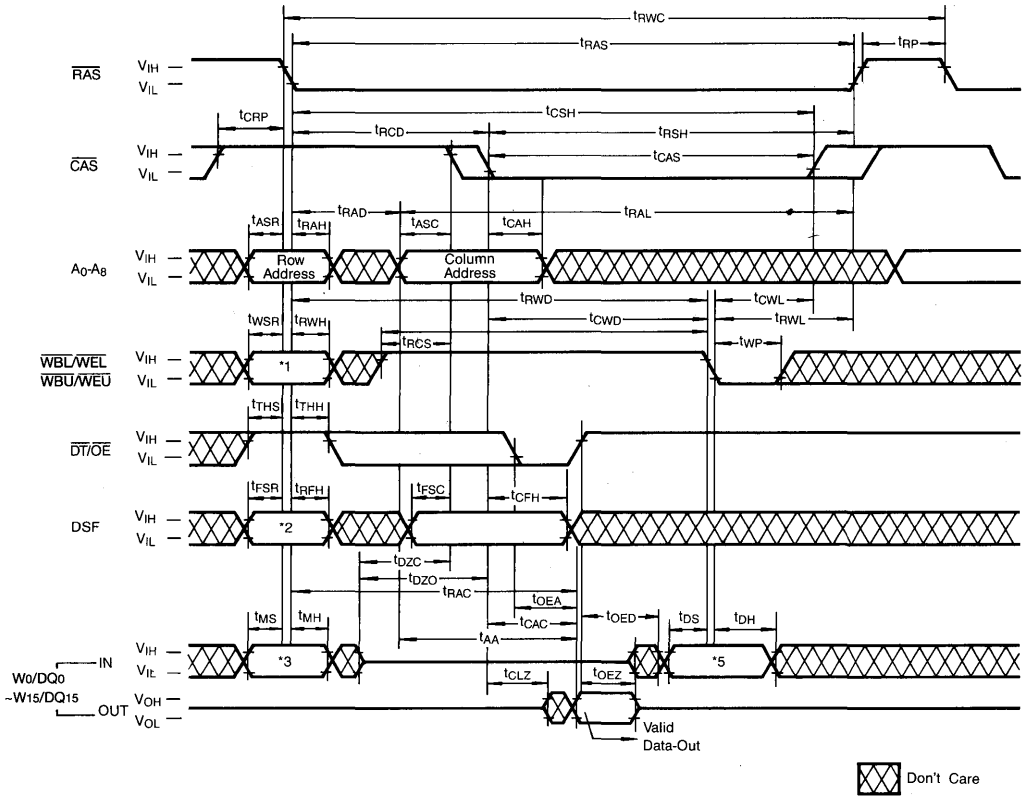
Note : In Block write cycle, only column address A3~A8 are used.

LATE WRITE CYCLE



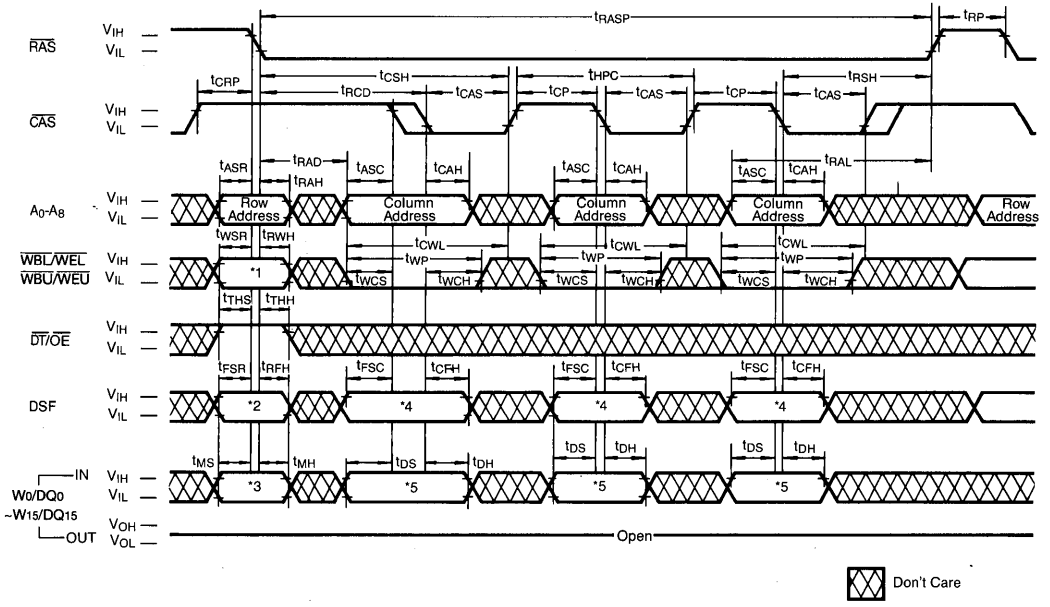
Note : In Block write cycle, only column address A_3~A_8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE



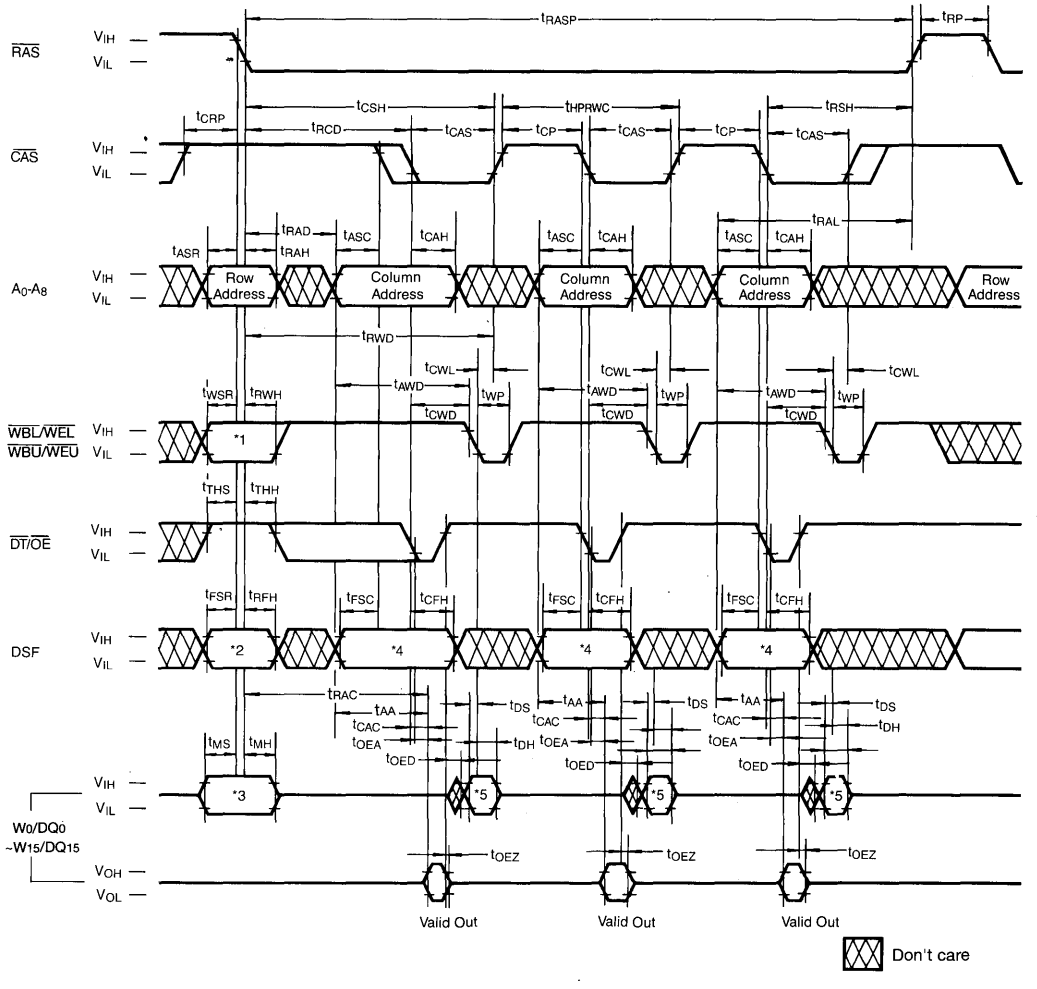
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE EARLY WRITE CYCLE



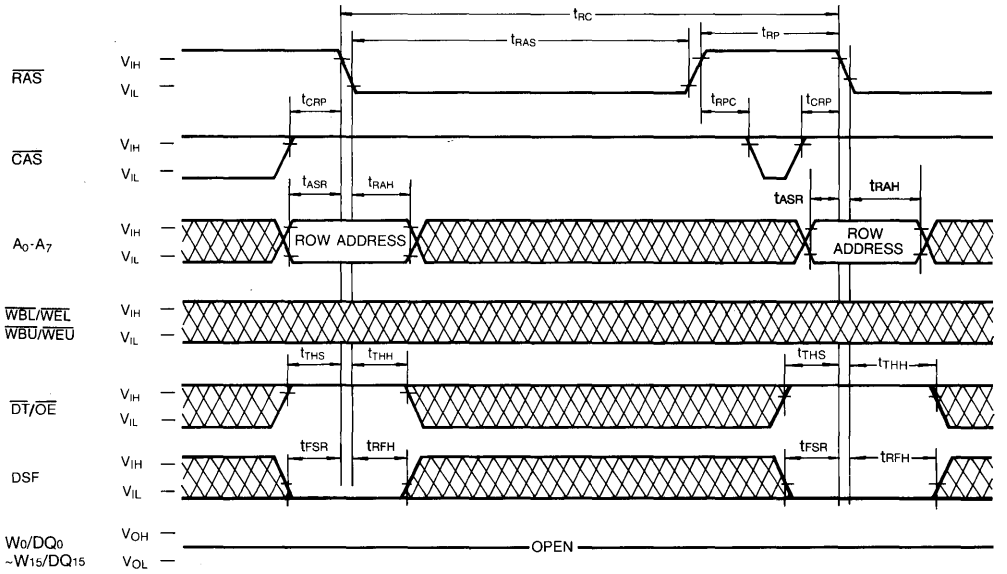
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

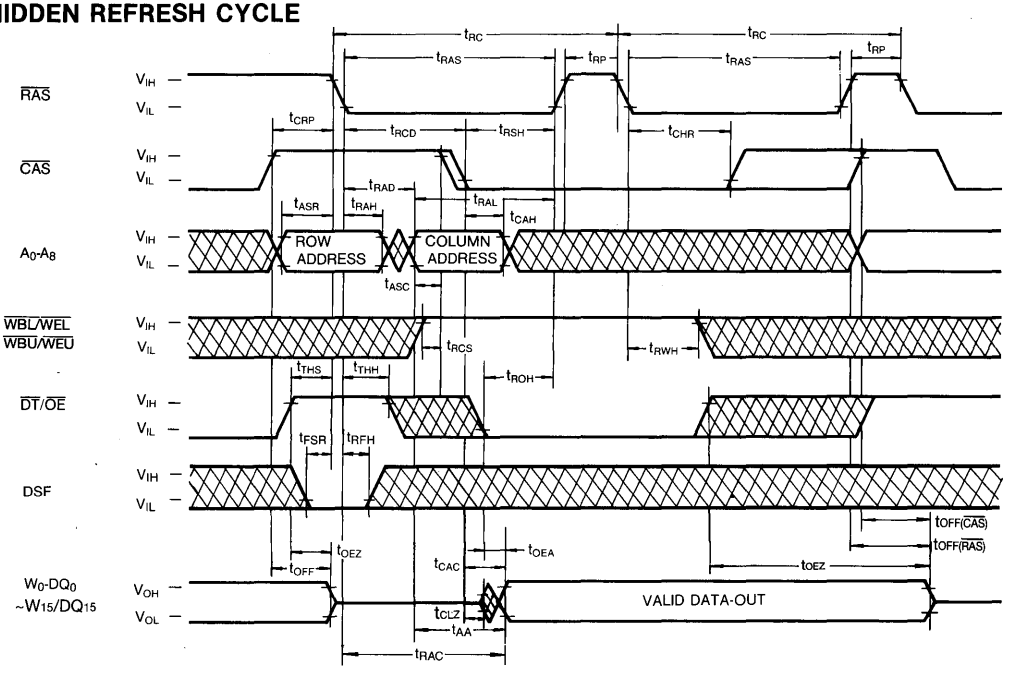


Note : In Block write cycle, only column address A_3~A_8 are used.

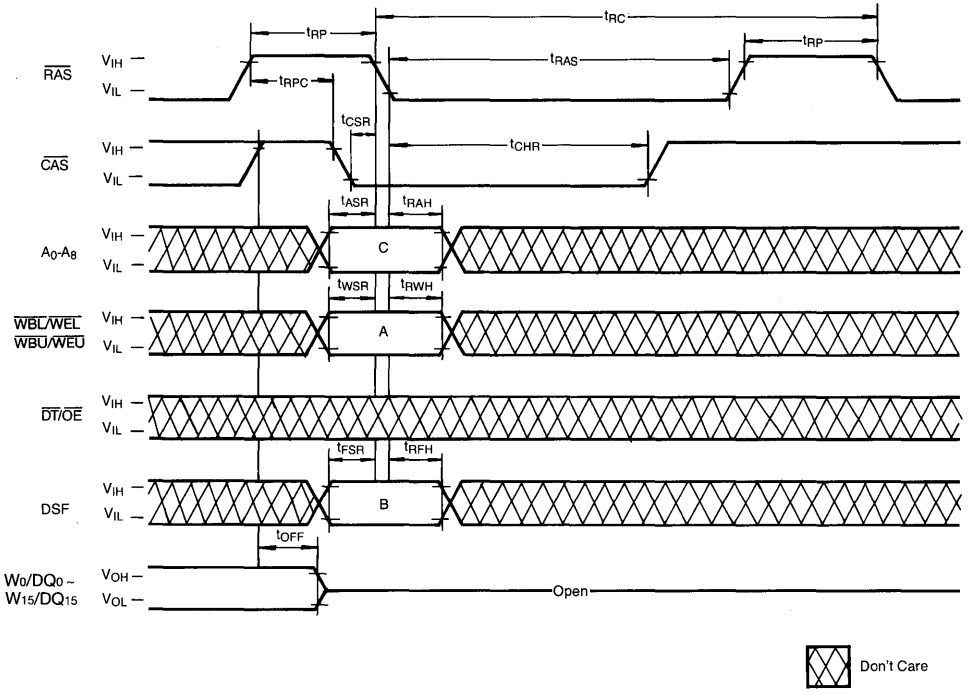
$\overline{RAS}$ ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE



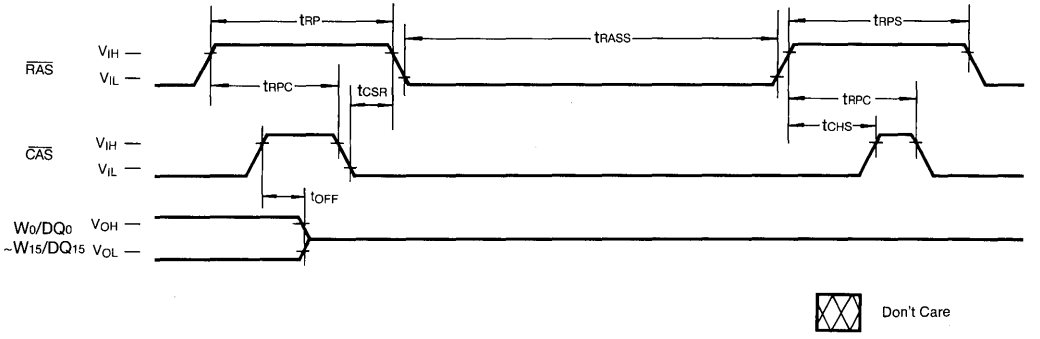
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE FUNCTION TABLE

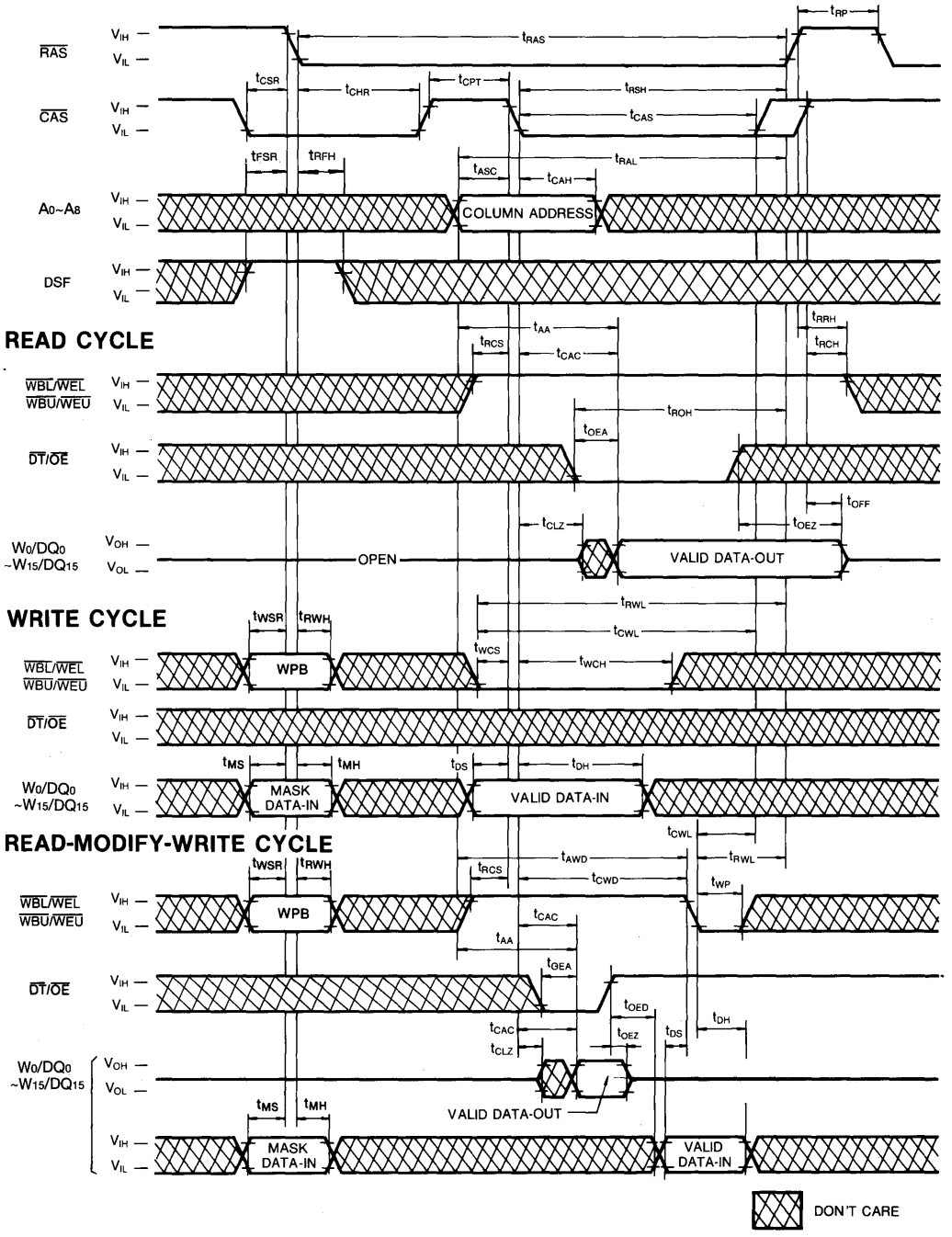
FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	STOP Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

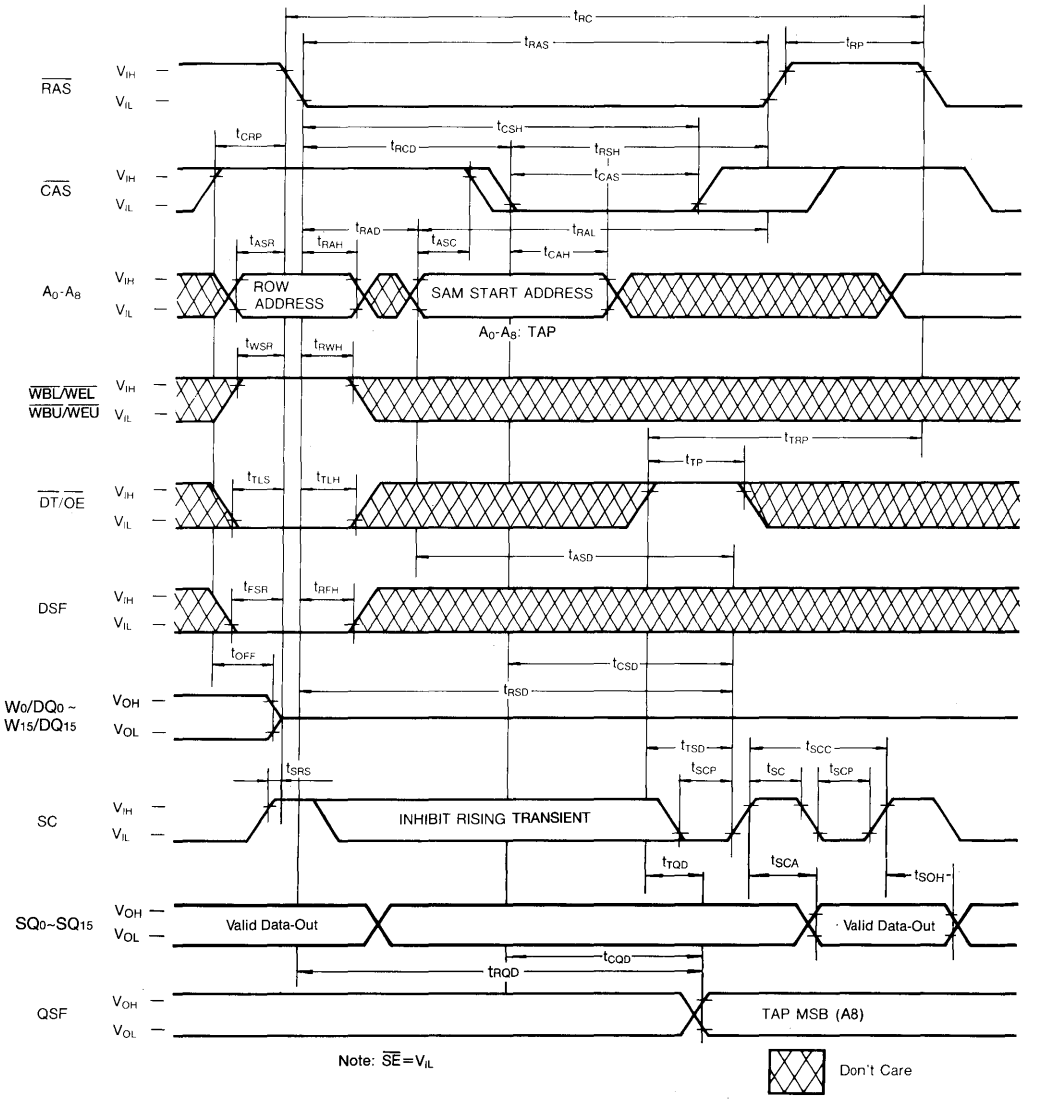


*CBR SELF REFRESH CYCLE IS APPLICABLE WITH CBRR, CBRS, OR CBRN CYCLE

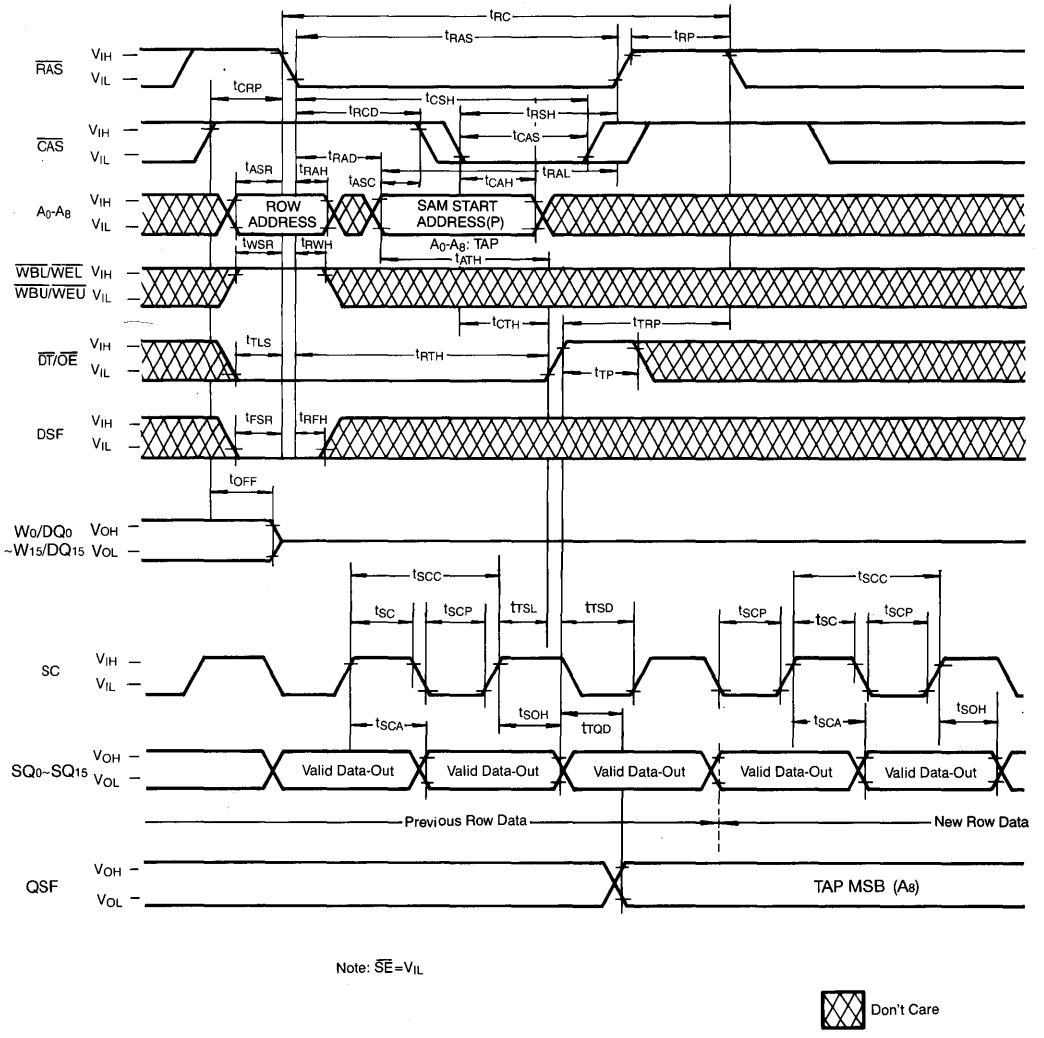
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



READ TRANSFER CYCLE



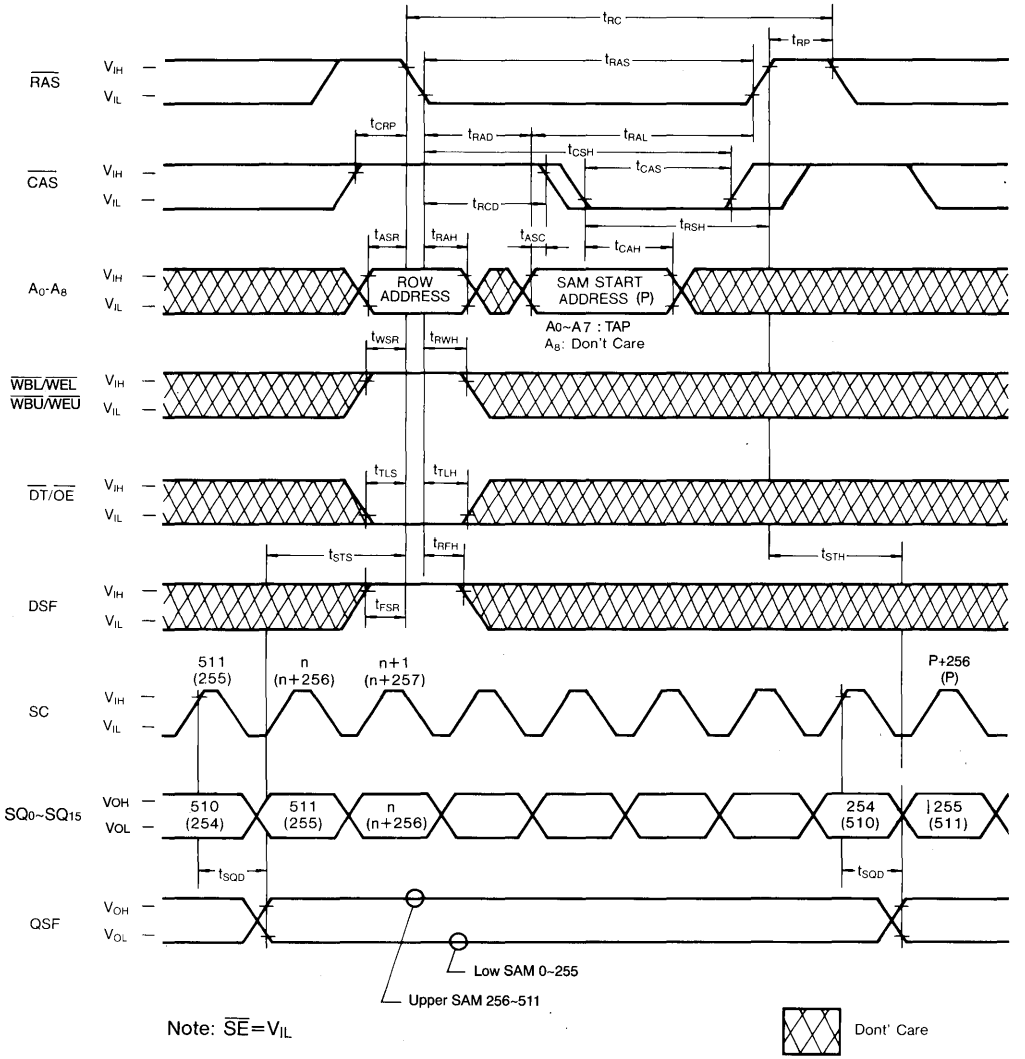
REAL TIME READ TRANSFER CYCLE



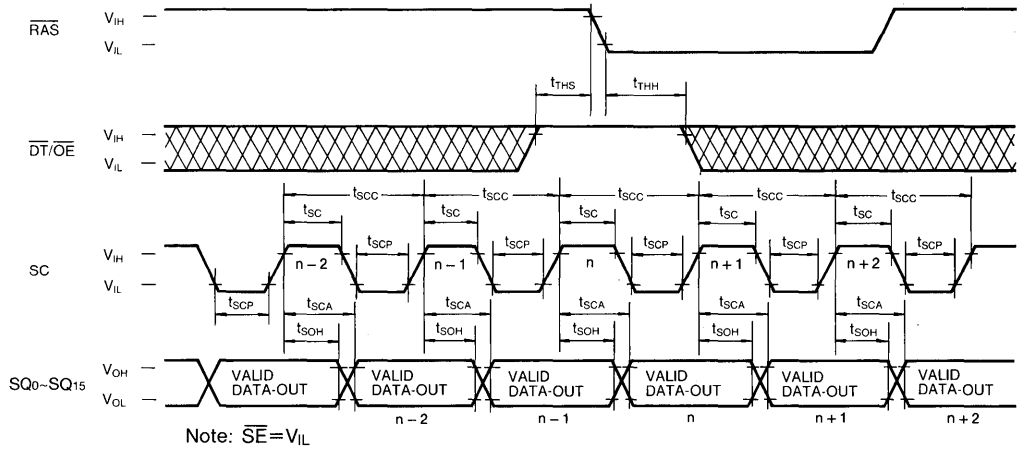
Note: $\overline{SE}$=V_{IL}

Don't Care

SPLIT READ TRANSFER CYCLE

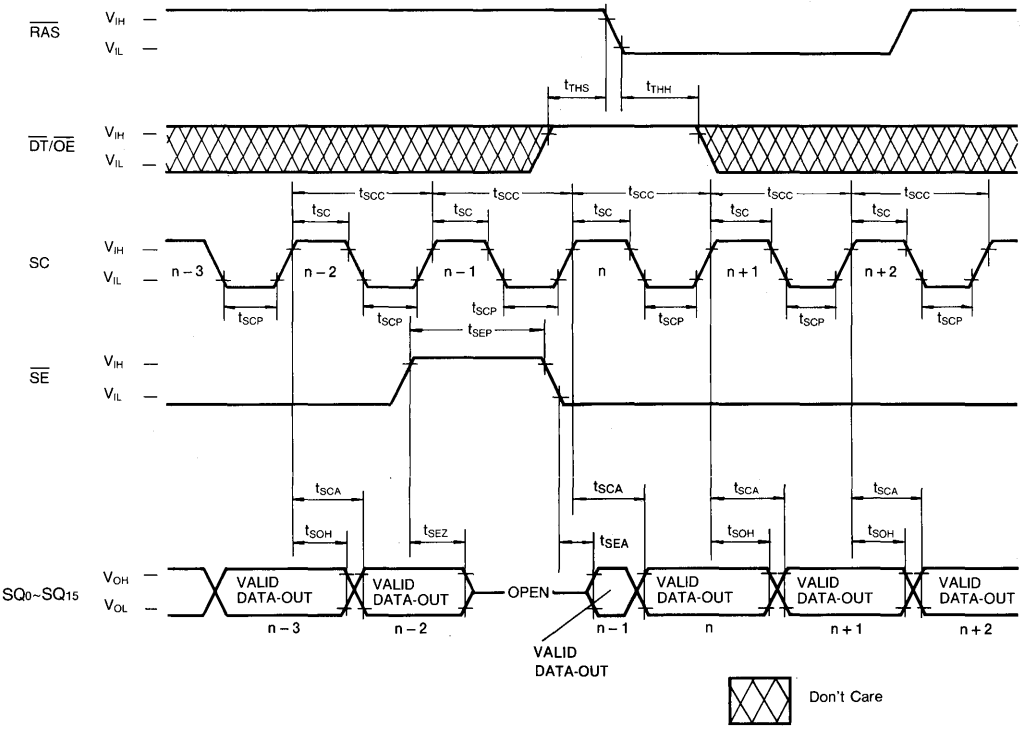


SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



Note: $\overline{SE} = V_{IL}$

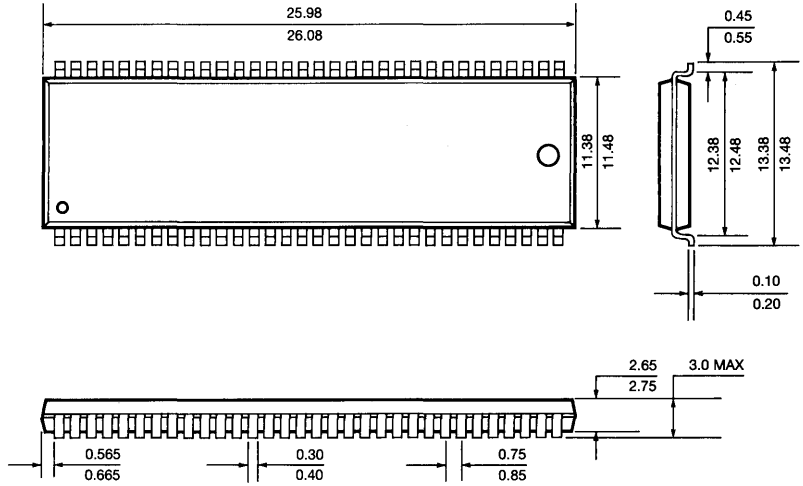
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



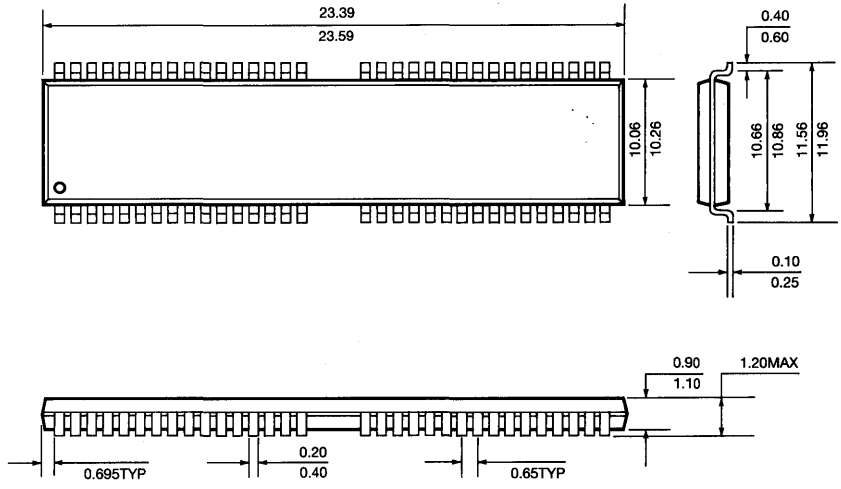
PACKAGE DIMENSIONS

Units: Millimeters

64 Pin Plastic Shrink Small Out Line Package



70(64) Pin Plastic Thin Small Out Line Package (Type II Forward)



256K × 16 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K × 16 bits RAM port
  512 × 16 bits SAM port
- **Performance range:**

Parameter \ Speed		-60	-70	-80
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{HPC})	KM4216C256	24ns	28ns	33ns
	KM4216V256	24ns	28ns	33ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C256	120mA	110mA	100mA
	KM4216V256	110mA	100mA	90mA
SAM active current	KM4216C256	50mA	45mA	40mA
	KM4216V256	40mA	35mA	30mA

- **Fast Page Mode with Extended Data out**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **Byte/Word Write Operation**
- **8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single + 5V±10% Supply Voltage (KM4216C256)**
- **Single + 3.3V±10% Supply Voltage (KM4216V256)**
- **Plastic 64-Pin 525 mil SSOP (0.8mm pin pitch)**
- **Plastic 70-pin 400mil TSOP II(0.65mm pin pitch) (Forward and Reverse Type)**

- **Device Options** — **Part Marking**
  -. Low Power Dissipation
  Extended CBR Refresh (64ms) — **L**
  -. Low Low Power Dissipation
  Self Refresh (128ms) — **F**
- **Low Vcc(3.3V) Part Name: KM4216V256**

GENERAL DESCRIPTION

The Samsung KM4216C/V256 is a CMOS 256K×16 bit Dual Port DRAM. It consists of a 256K ×16 dynamic random access memory (RAM) port and 512 ×16 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K×16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Byte/word write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM ports using read, and programmable (Stop Register) Split Transfers.

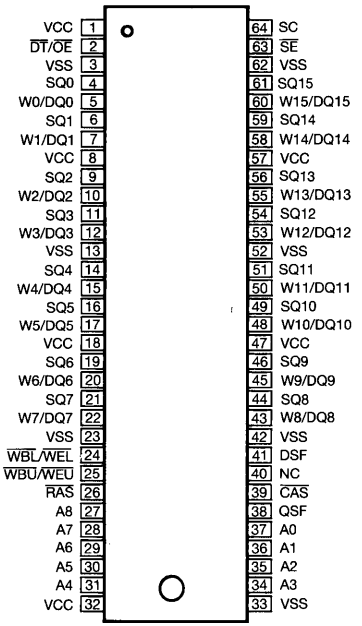
Refresh is accomplished by familiar DRAM refresh modes. The KM4216C/V256 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

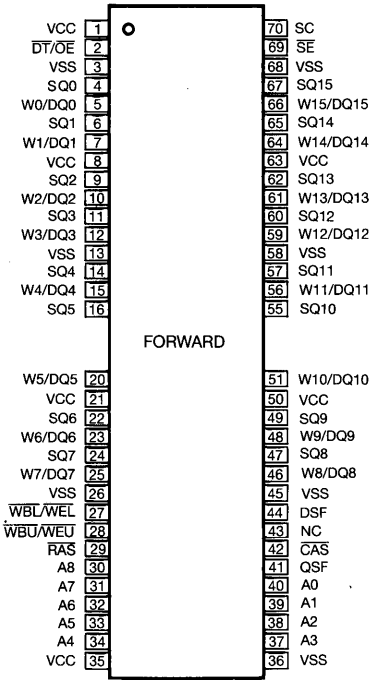
Pin Name		Pin Function
SC		Serial Clock
SQ_0-SQ_{15}		Serial Data Output
$\overline{DT}/\overline{OE}$		Data Transfer/Output Enable
$\overline{WBL}/\overline{WEL}$, $\overline{WBU}/\overline{WEU}$		Write Per Bit/Write Enable (Lower /Upper)
$\overline{RAS}$		Row Address Strobe
$\overline{CAS}$		Column Address Strobe
W_0/DQ_0-W_{15}/DQ_{15}		Data Write Mask/Input/Output
$\overline{SE}$		Serial Enable
A_0-A_8		Address Inputs
DSF		Special Function Control
V_{CC}	KM4216C256	Power (+5V)
	KM4216V256	Power (+3.3V)
V_{SS}		Ground
QSF		Special Flag Out
N.C		No Connection

PIN CONFIGURATION (TOP VIEWS)

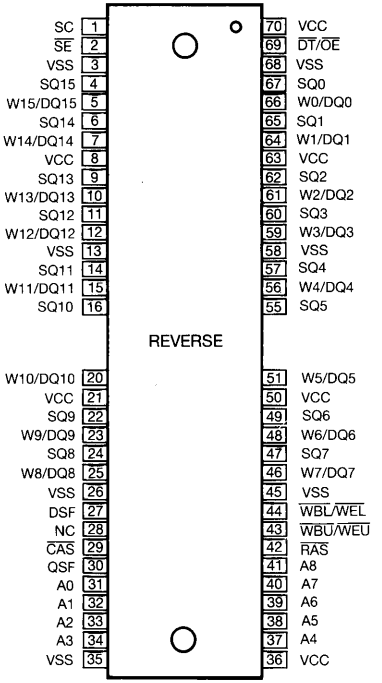
• **KM4216C/V256G/GL/GF**



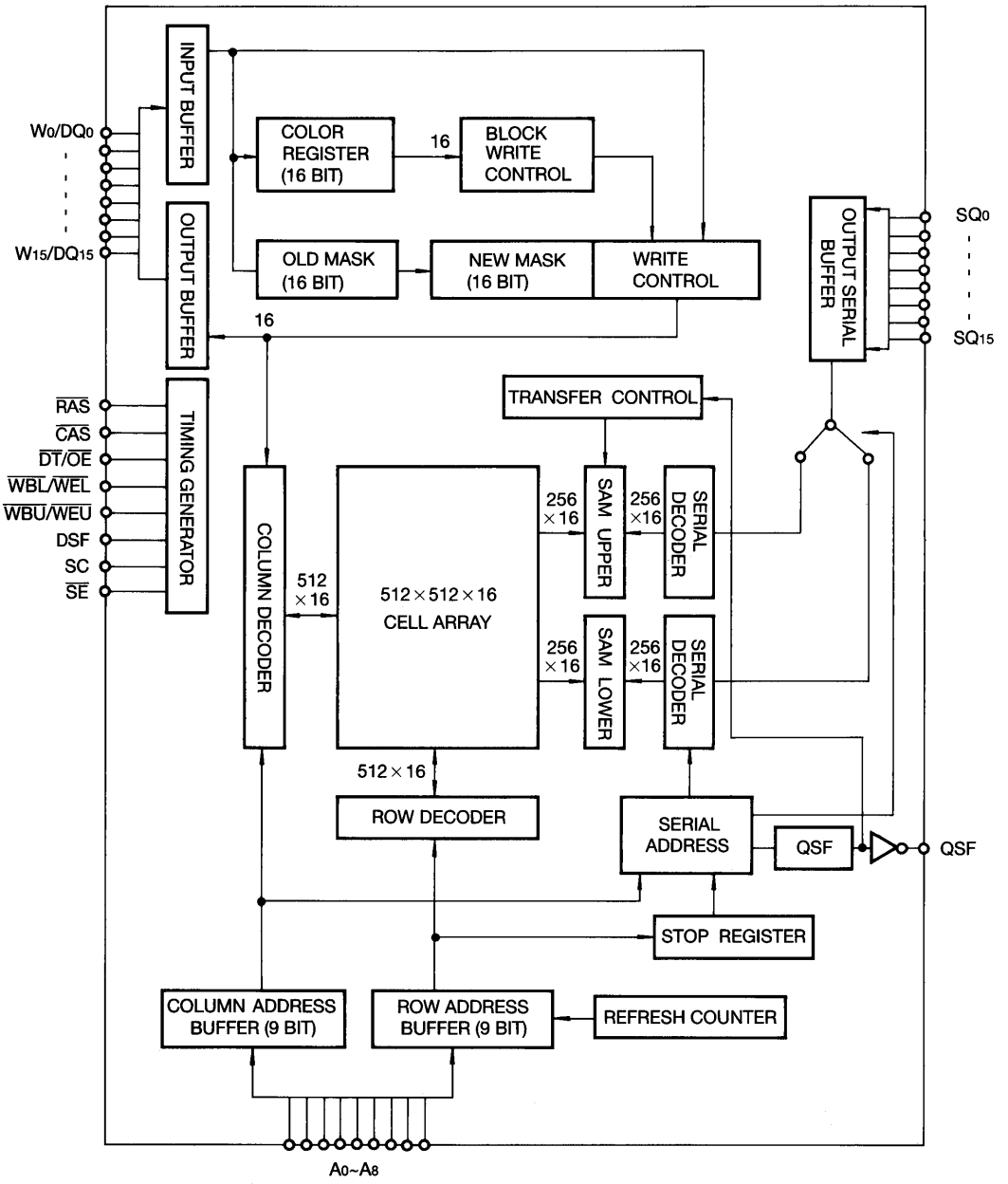
• **KM4216C/V256T/TL/TF**



• **KM4216C/V256R/RL/RF**



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic	RAS ↓				CAS ↓	Address		DQi Input		Register		Function
Code	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1.3)	0	×	0	1	-	Stop (Note4)	-	×	-	-	-	CBR Refresh/ Stop (No reset)
CBRN (Note 1)	0	×	1	1	-	×	-	×	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	×	×	0	-	×	-	×	-	-	-	CBR Refresh (Option reset)
ROR	1	1	×	0	-	ROW	-	×	-	-	-	RAS-only Refresh
RT	1	0	1	0	×	ROW	Tap	×	×	-	-	Read Transfer
SRT	1	0	1	1	×	ROW	Tap	×	×	-	-	Split Read Transfer
RWM	1	1	0	0	0	ROW	Col.	WMi	Data	Use	-	Masked write (New/Old Mask)
BWM	1	1	0	0	1	ROW	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New/Old Mask)
RW	1	1	1	0	0 (Note6)	ROW	Col.	×	Data	-	-	Read or Write
BW	1	1	1	0	1	ROW	Col.	×	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	ROW (Note7)	×	×	WMi	Load (Note5)	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	ROW (Note7)	×	×	Color		Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap:SAM Start (Column) Address, WMi : Write Mask Data (i=0~15)
RAS only refresh does not reset Stop or LMR functions.

Notes:
(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask.(Use CBRR reset to new mask, use CBRS or CBRN to perform CAS-before-RAS refresh while using Old mask)
(3) After CBRS Cycle, SRT use STOP Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The ROW that is addressed will be refreshed, but a ROW address is not reguired.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C256	KM4216V256	
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to + 150	55 to +150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	KM4216C256			KM4216V256			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$+0.5(0.3*1) all other pins not under test=0 volts).	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V256

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless other wise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C256			KM4216V256			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1	Standby*4	I_{CC1}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)	Active	I_{CC1A}	160	145	130	140	125	110	mA
Standby Current	Standby*4	I_{CC2}	10	10	10	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$=V_{IH}	Active	I_{CC2A}	50	45	40	40	35	30	mA
DSF=V_{IL})	Standby*4	I_{CC2C}*2	200	200	200	200	200	200	μA
	Standby*4	I_{CC2C}*3	150	150	150	150	150	150	μA
$\overline{RAS}$ Only Refresh Current*1	Standby*4	I_{CC3}	120	110	100	110	100	90	mA
($\overline{CAS}$-V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min	Active	I_{CC3A}	160	145	130	140	125	110	mA
Extended Fast Page Mode Current*1	Standby*4	I_{CC4}	110	100	90	100	90	80	mA
($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cyciing @t_{PC}=min	Active	I_{CC4A}	150	135	120	130	115	110	mA
$\overline{CAS}$ Before-$\overline{RAS}$ Refresh Current*1	Standby*4	I_{CC5}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min	Active	I_{CC5A}	160	145	130	140	125	110	mA
Data Transfer Current *1	Standby*4	I_{CC6}	140	130	120	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC6A}	180	165	150	160	145	130	mA
Block Write Cycle Current *1	Standby*4	I_{CC7}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC7A}	160	145	130	140	125	110	mA
Color Register Load Current *1	Standby*4	I_{CC8}	110	90	80	90	80	70	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC8A}	140	125	110	120	105	90	mA
Battery Back Up Current *2 $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycling or $\leq V_{IL}$ $\overline{RAS}$=t_{RAS}(min) to 1μs t_{RC}=125 μs (64ms for 512 rows) $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, DSF$\geq V_{IH}$ or$\leq V_{IL}$	Standby*4	I_{CC9}	300	300	300	300	300	300	μA
Self Refresh Current *3 $\overline{RAS}$,$\overline{CAS}\leq$0.2V(128ms for 512 rows) $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, DSF$\geq V_{CC}$ -0.2V or$\leq$0.2V DQ0~15=V_{CC}-0.2V, 0.2V or OPEN	Standby*4	I_{CC10}	250	250	250	250	250	250	μA

Note *1 Real values dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, adress transition should be changed only once while $\overline{RAS}$=V_{IL}.

In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$=V_{IH}

*2 KM4216C/V256L only : $V_{IH}\geq V_{CC}$-0.2V, $V_{IL}\leq$0.2V

*3 KM4216C256F only : $V_{IH}\geq V_{CC}$ -0.2V, $V_{IL}\leq$0.2V

*4 SAM standby condition : $\overline{SE}\geq V_{IH}$, SC$\leq V_{IL}$ or $\geq V_{IH}$

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM4216C256 : V_{CC}=5.0V±10%, KM4216V256 : 3.3V±10%,)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		200		ns	
Hyper page cycle time	t_{HPC}	30		35		40		ns	17
		24		28		33		ns	16
Hyper page read-modify-write cycle time	t_{HPRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,6
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Hyper page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		55		65		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	15	10K	20	10K	ns	17
		10		10		12		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time (Hyper page mode)	t_{CP}	10		10		10		ns	
Output hold time from $\overline{CAS}$	t_{DOH}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		12		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Output buffer turn off delay from $\overline{WBX}$/$\overline{WEX}$	t_{WEZ}	0	15	0	15	0	15	ns	7
Write command pulse width	t_{WPZ}	10		10		10		ns	7
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		12		15		ns	10
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	tAWD	50		55		60		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output Buffer turn-off delay from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	10		10		15		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	0		0		0		ns	15
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (real time read transfer)	tCTH	15		20		25		ns	

AC CHARACTERISTICS (Continued)

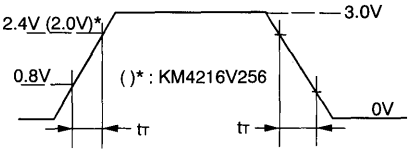
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ low hold referenced to column address (real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay (read transfer)	t_{CSD}	25		30		35		ns	
Col. Address to first SC delay (read transfer)	t_{ASD}	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	t_{TSD}	10		10		15		ns	
LAST SC to $\overline{RAS}$ set-up time	t_{SRS}	20		20		20		ns	
SC cycle time	t_{SCC}	18		20		25		ns	14
SC pulse width (SC high time)	t_{SC}	5		7		7		ns	
SC precharge (SC low time)	t_{SCP}	5		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	
SC-QSF delay time	t_{SQD}		20		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		20		25		25	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		70		75		80	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		35		35		40	ns	
$\overline{DT}$ to $\overline{RAS}$ Prechange time	t_{TRP}	40		50		60		ns	
$\overline{OE}$ high pulse width	t_{OEP}	10		10		10		ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	10		10		10		ns	
$\overline{OE}$ to $\overline{CAS}$ high set-up time	t_{OCH}	5		5		5		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved.($\overline{DT}/\overline{OE}$=High) if the intenal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required in stead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input siganl transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1TTL load and 50pF.
   D_{OUT} Comparator level : V_{OH}/V_{OL}=2.0V/0.8V.
4. SAM port outputs are measured with a load equivalent to 1TTL load and 30pF.
   D_{OUT} comparator level:V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below

Pin or REGISTER	STATUS
QSF	Hi-Z
Color Registe	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SQi	Hi-Z

13. Recommended operating input condition.



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=5.0ns
14. Assume t_T=3ns.
15. Self refresh parameter (KM4216C/V256F)
    512K cycle of burst refresh must be executed within 8ms before and after self-refresh in order to meet refresh specification.
16. $t_{ASC} \geq t_{CP}$(min) at normal cycle assume t_T=2ns.
17. $t_{ASC} < t_{CP}$(min) at normal cycle or any condition at Block write cycle assume t_T=2ns.

DEVICE OPERATION

The KM4216C/V256 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$). the column address strobe($\overline{CAS}$) and the valid row and coumn address inputs.

Operation of the KM4216C/V256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This the beginning of any KM4216C/V256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$,$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.
If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then tne access time to valid data is specified by t_{RAC}. However, if $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}
The KM4216C/V256 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM Read cycle, D_{OUT} buffer is designed to make turn-off by the rising edge fo $\overline{CAS}$. The KM4216C/V256 offers an accelerated Fast Page Mode Cycle by eliminating output disable from $\overline{CAS}$ high.
This is called Extended Data Output (or Hyper Page mode)
Data output are disabled at $\overline{WB}/\overline{WE}$=low, $\overline{DT}/\overline{OE}$=high and t_{OFF} time after $\overline{RAS}$ and $\overline{CAS}$ are high. The t_{OFF} time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs laters (See Figure 1). What the output buffer is disabling during $\overline{DT}/\overline{OE}$ = high is to use bank selection in the frame buffer memory using common I/O line. Read, write and read-modify-write cycles are available during the extended data out mode.

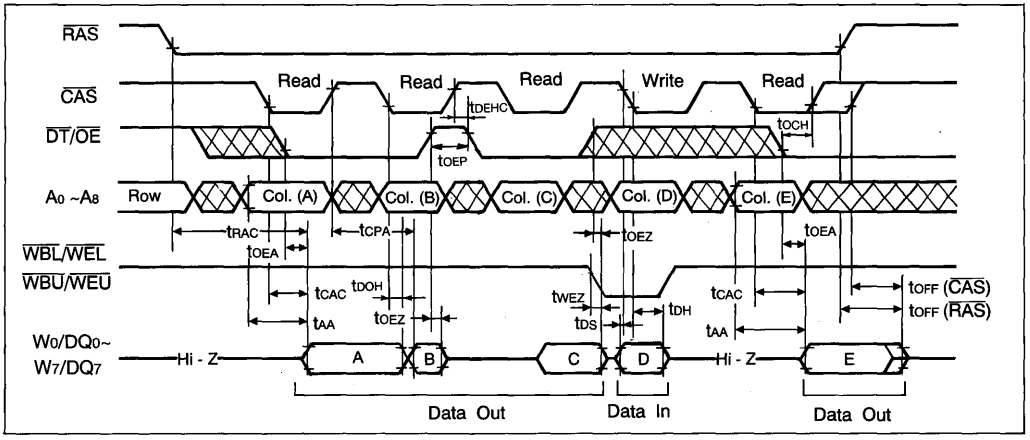


Figure 1. Extended Data Output Example

DEVICE OPERATION (continued)

Byte Write Operation

The KM4216C/V256 has 2 write control pin, $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$, and offers asynchronous write operation with lower byte (W_0/DQ_0~W_7/DQ_7) and upper byte (W_8/DQ_8~W_{15}/DQ_{15}). This is called Byte Write operation. This operation can be performed in RAM write, Block write, Load Mask register, and Load Color register.

New Masked Write Per Bit

The New Masked Write Per Bit cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM.

The mask data is valid for only one cycle. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ low after $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

If $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed (see Figure2, 3). And If $\overline{WBL}/\overline{WEL}$ is high during $\overline{CAS}$ low, write operation of lower byte do not perform and if $\overline{WBU}/\overline{WEU}$ is high, write operation of upper byte do not execute.

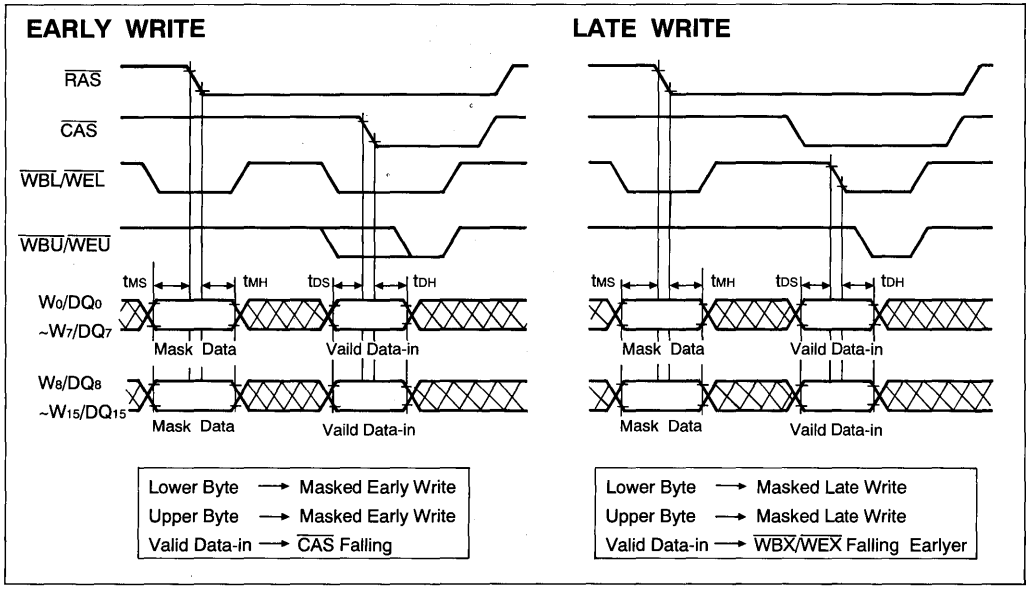


Figure 2. Byte Write and New Masked Write Cycle Example 1. (Early Write & Late Write)

DEVICE OPERATION (continued)

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.
The LMR cycle is performed if DSF high, $\overline{WB}/\overline{WE}$ high at the $\overline{RAS}$ falling edge and DSF low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM4216C/V256 are set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked write are Old Masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register (See Figure 4.)
The mask data is applied in the same manner as in New Masked write Per Bit mode.
Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After power-up, the KM4216C/V256 initializes in the New Masked write mode.

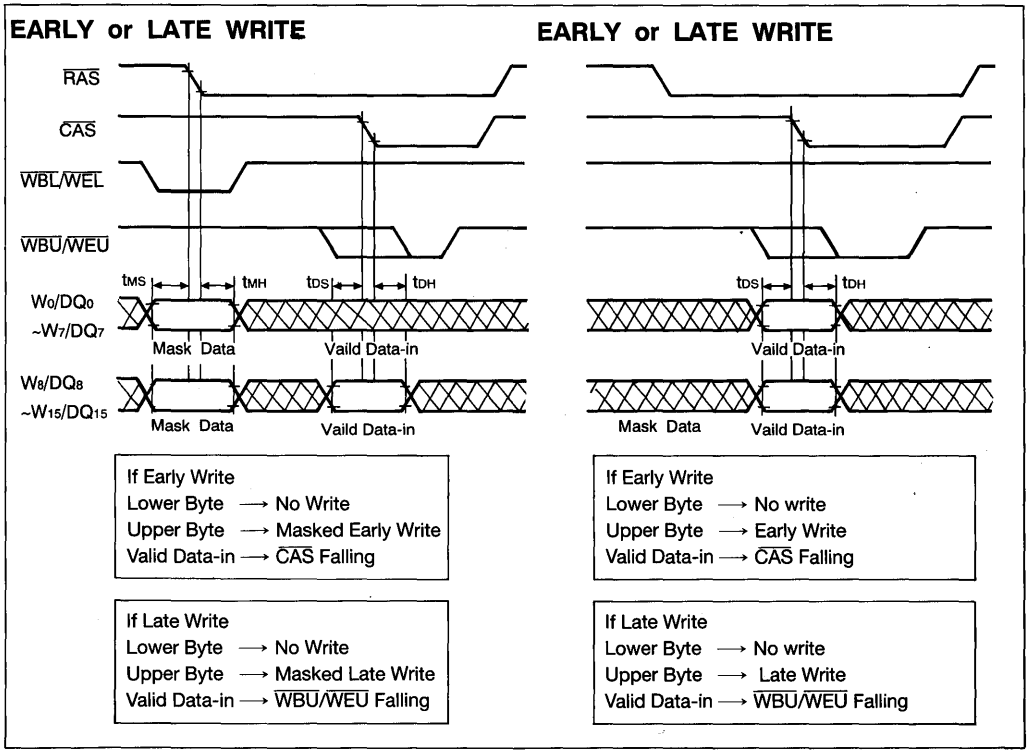


Figure 3. Byte Write and New Masked Write Cycle Example 2.

DEVICE OPERATION (continued)

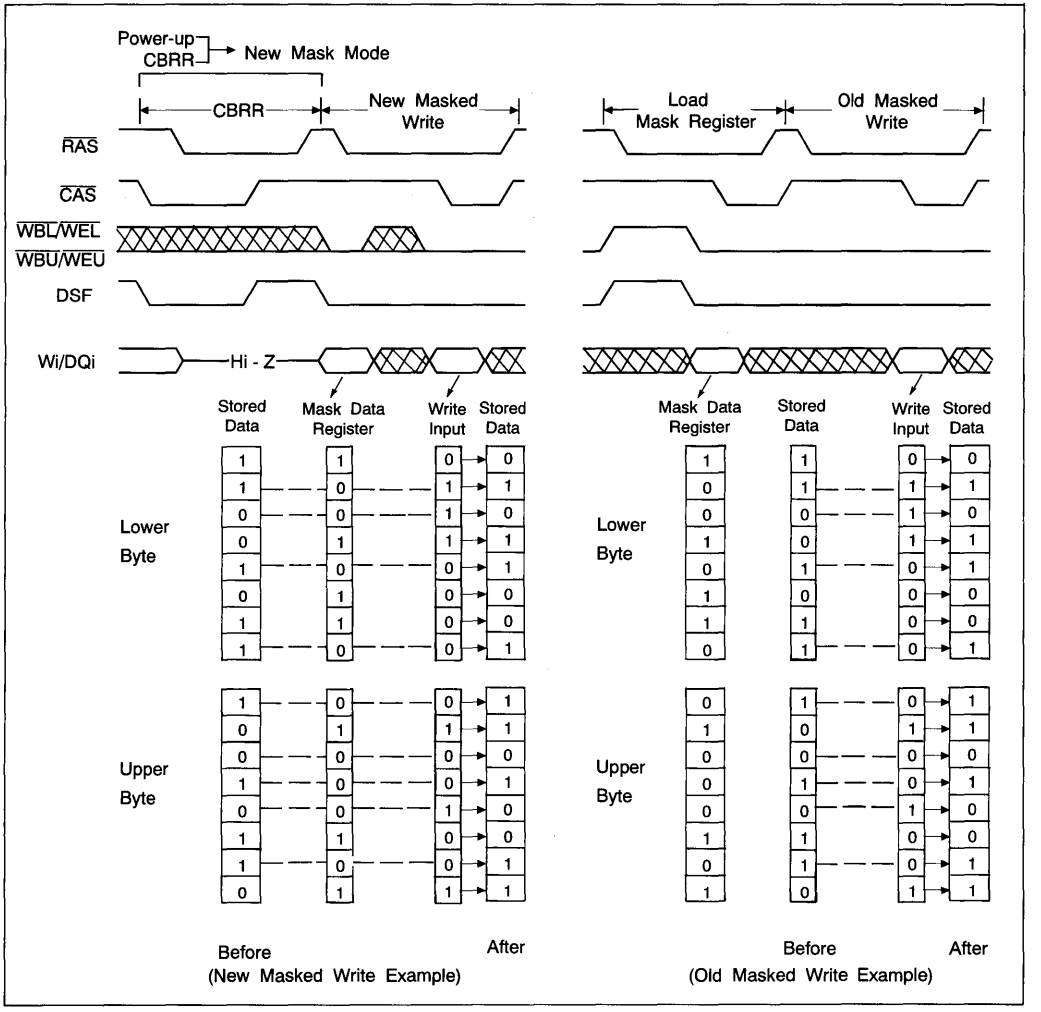


Figure 4. New Masked Write Cycle and Old Masked Write Cycle Example

Fast Page Mode

The KM4216C/V256 has Fast Page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. In this cycle, read, write, read-modify write, and block write cycles can be mixed in any order.
In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

DEVICE OPERATION (continued)

Load Color Register(LCR)

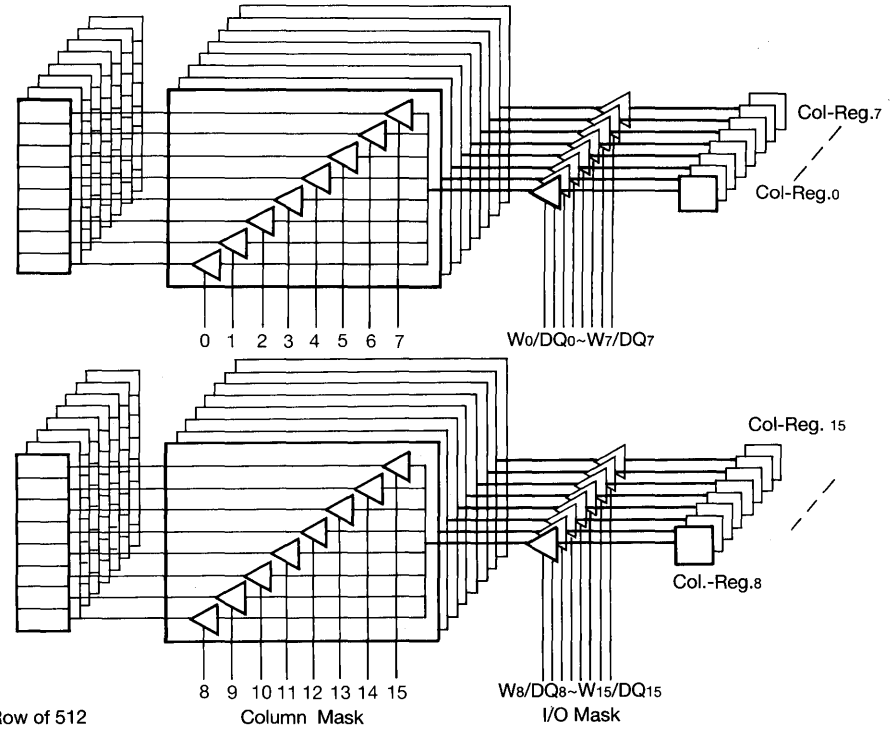
A Load Color register cycle is performed by keeping DSF high on the both falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded in the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(late write) via the W_0/DQ_0~W_7/DQ_7(Lower Byte), W_8/DQ_8~W_{15}/DQ_{15} (Upper Byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register Cycle.

Block Write

In a Block write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each corresponding bit plane(16). This result in a total of 128-bits being written in a single Block write cycle compared to 16-bits in a normal write cycle.

The Block write cycle is performed if DSF is low at the falling edge of $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



1 Row of 512

Column Mask

	$\overline{RAS}$
W_0/DQ_0~7	Lower Block I/O Mask
W_8/DQ_8~15	Upper Block I/O Mask

	$\overline{CAS}$
A_0~A_2	Don't Care
W_0/DQ_0~7	Lower Block Column Select
W_8/DQ_8~15	Upper Block Column Select

A_2~A_0	Lower	Upper	Column Mask	
0 0 0	W_0/DQ_0	W_8/DQ_8		
0 0 1	W_1/DQ_1	W_9/DQ_9	DQi=1	Column
0 1 0	W_2/DQ_2	W_{10}/DQ_{10}		Enable
0 1 1	W_3/DQ_3	W_{11}/DQ_{11}		
1 0 0	W_4/DQ_4	W_{12}/DQ_{12}		
1 0 1	W_5/DQ_5	W_{13}/DQ_{13}	DQi=0	Column
1 1 0	W_6/DQ_6	W_{14}/DQ_{14}		Disable
1 1 1	W_7/DQ_7	W_{15}/DQ_{15}		

Figure 5. Block Write Scheme

DEVICE OPERATION (continued)

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.
Since 8 columns are being written at a time, the minimum increment required for the column address is latched on the falling edge of $\overline{CAS}$, the 3 LSBs, A_0, A_1, and A_2 are ignored and only bits (A_3~A_8) are used to define the location of the first bit out of the eight to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16 -bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the eight, but the second remains unchanged. Fig. 5 shows the correspondence of each data line to the column mask bits.
A Masked Block Write cycle is identical to a New/old Masked Write-Per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high on the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0~W_{15}/DQ_{15} pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. In old mask mode, I/O mask data will be provided by the Mask Data Register.

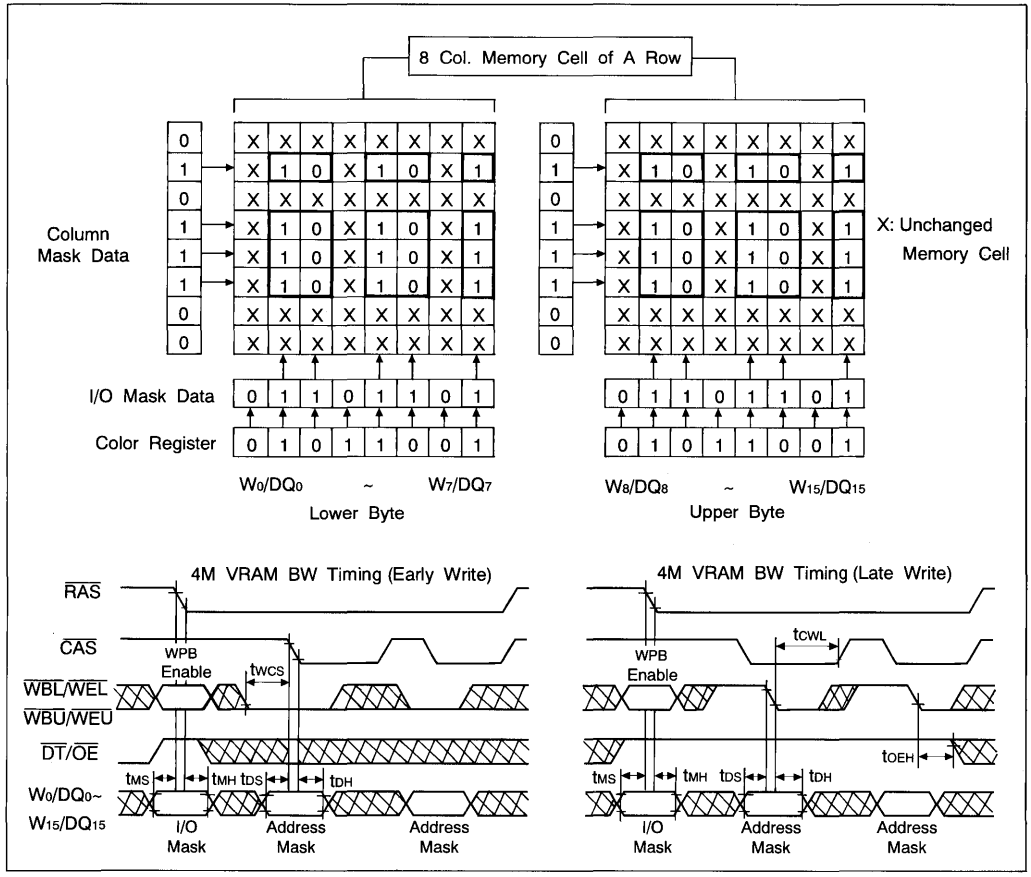


Figure 6. Block Write Example and Timing

DEVICE OPERATIONS (Continued)

Data Output

The KM4216C/V256 has three state output buffer Controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}/\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is in high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output duing the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V256 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM4216C/V256 has $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on chip refresh circuitry is enabled. An internal refresh operatian occurs automatically. The refresh address is supplied by the on chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
The KM4216C/V256 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation ; CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values
CBRN (CBR refresh without reset) is set if DSF high when $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$ is high at the falling edge of $\overline{RAS}$ and simply do only refresh operation.
CRRS(CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V256 hidden refresh cycle is actually a $\overline{CAS}$-beford-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Self Refresh *(Only KM4216C/V256F)* : The Self Refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for longer periods of standby, such as a battery back-up. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If $\overline{RAS}$ is low more than 100μs at the condition of CBR, Self Refresh function is accomplished. In this state, the external refresh address do not need to supply additionally on chip because the refresh counter on chip gives that addresses needed to refresh. Please note that the ending point of Self Refresh is when $\overline{RAS}$ and $\overline{CAS}$ is high and t_{RPS} of Self Refresh is the time reguiring to complete the last refresh of Self Refresh.

Other Refresh Methods : It is also possible to refresh the KM4216C/V256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS (Continued)

Table 1. Truth Table for Transfer Operation *: Don't care

RAS Falling Edgd					Function	Transfer Direction	Transfer Data Bit
CAS	DT/OE	WB/WE	DSF	SE			
H	L	H	L	*	Read Transfer	RAM→SAM	512 × 16
H	L	H	H	*	Split Read Transfer	RAM→SAM	256 × 16

Transfer Operation

Transfer operation is initiated when DT/OE is low at the falling edge of RAS. The state of DSF when RAS goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation. (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if DT/OE is low, WB/WE is high, and DSF is low at the falling edge of RAS. The row address bits in the read transfer cycle indicate which sixteen 512 bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half). Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC, DT/OE is taken high after CAS goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of DT/OE must be Synchronized with the rising edge of SC (t_{TSL}/t_{TSD}) to retain the continuity of serial read data output. If the transfer does not have to be synchronized with SC, DT/OE may go high before CAS goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, DT/OE, RAS and CAS) because the transfer has to occur at the first rising edge of DT/OE.

The Split Read Transfer cycle elinimates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between DT/OE and RAS, CAS, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and WB/WE high and DT/OE low at the falling edge of RAS.

2

DEVICE OPERATIONS (Continued)

Address: The row address is latched in the falling edge of $\overline{RAS}$. The column address defined by (A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. Column addrress pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1= Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g.255th or 511th bit).
Example of SRT applications are shown in Fig.7 through Fig. 10

The normal usage of Split Read Transfer cycle is described in Fig.7. When Read Transfer is executed, data from X_1 row address is fully transferred to the SAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X_2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y_0" Tap address instead of "Y_0" is loaded.
The another example of SRT cycle is described in Fig.8 When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle.

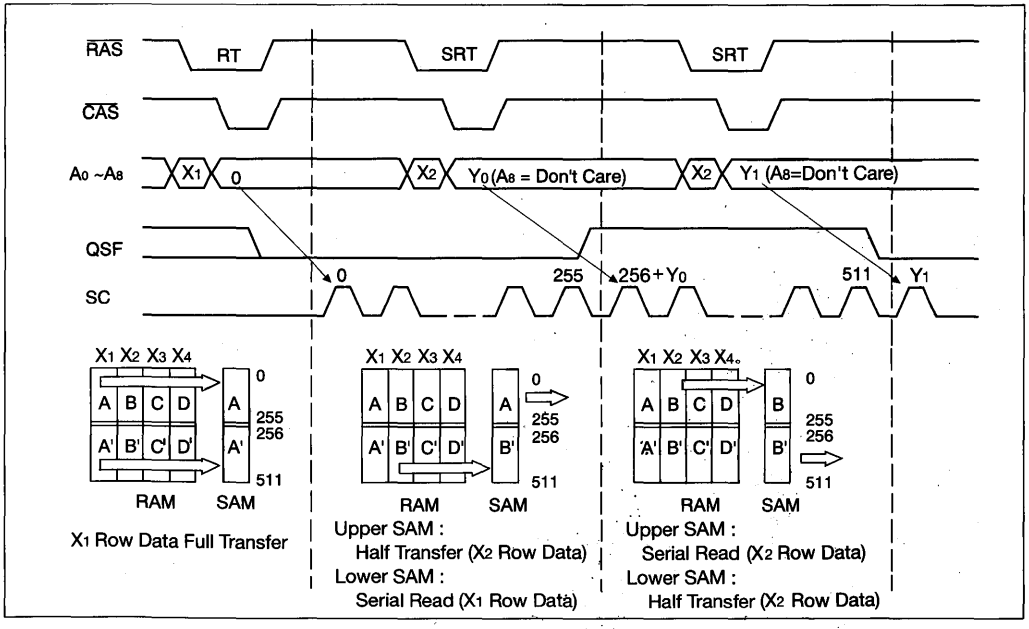


Figure 7. Split Read Transfer Normal Usage (Case1)

DEVICE OPERATIONS (Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig.9, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 10 indicates that SRT cycle is not performed until Serial Read is completed to the boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+ t_{STS}(See Figure 11.)

A split Read Transfer does not change the direction of the SAM I/O port.

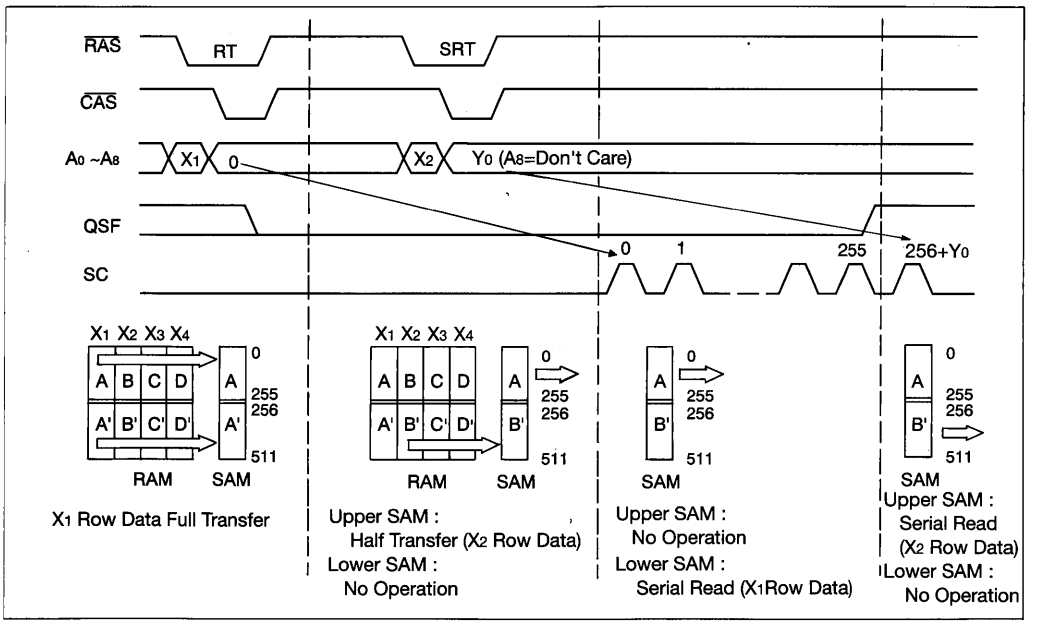


Figure 8. Split Read Transfer Normal Usage (Case 2)

DEVICE OPERATION (Continued)

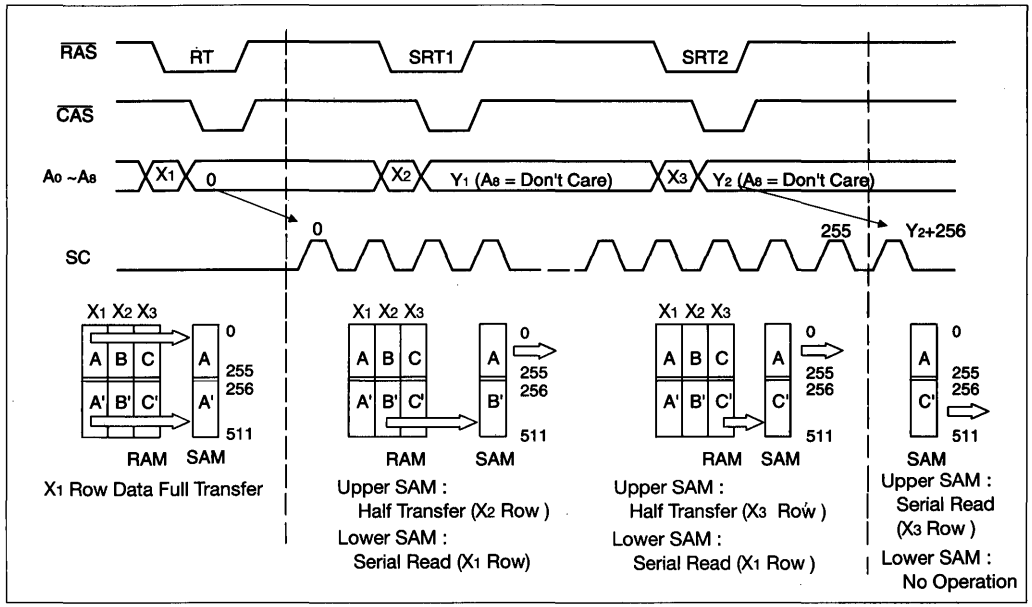


Figure 9. Split Read Transfer Abnormal Usage (Case 1)

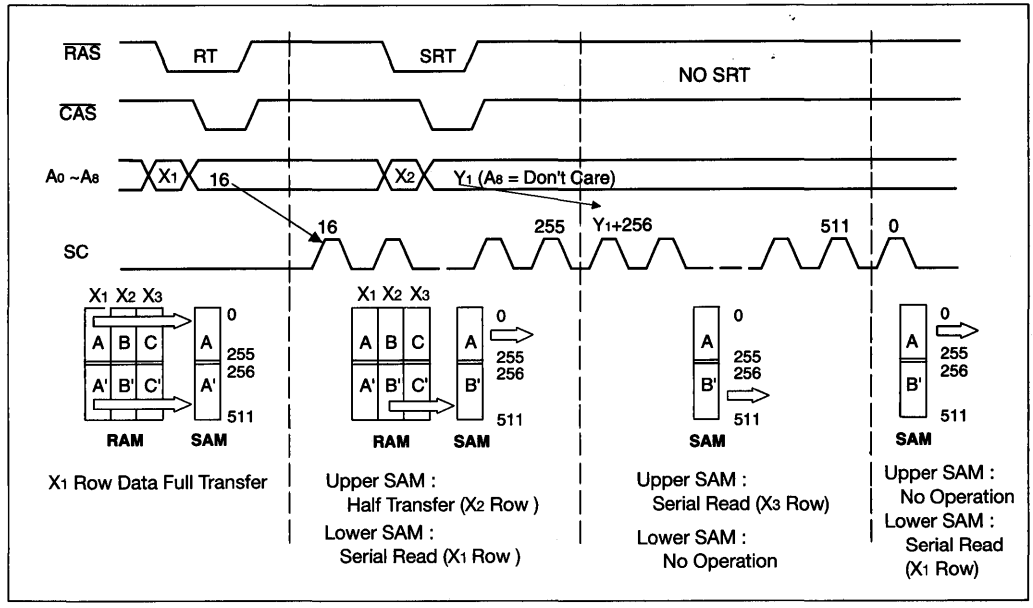


Figure 10. Split Read Transfer Abnormal Usage (Case 2)

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DEVICE OPERATION (Continued)

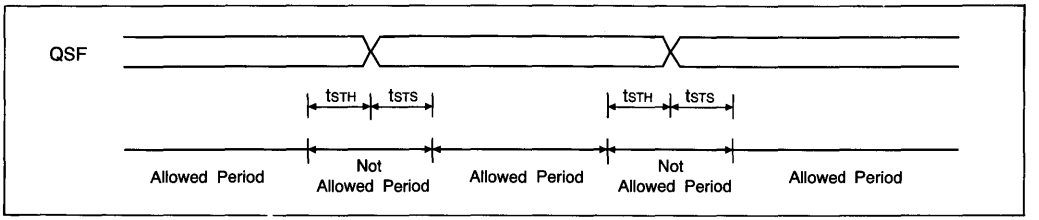


Figure 11. Split Transfer Cycle Limitation Period

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half.

After the last address of each half SAM(255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded TAP address).

This last address is called Stop Point.

The KM4216C/V256 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WBL}/\overline{WEL}$ or $\overline{WBU}/\overline{WEU}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.

In Figure 12. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address(70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs or the SAM half boundary (255, 511).

Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$. The CBRR wil take effect immediately; it does not require a SRT to become active valid.

Table 2. Stop Point Setting Address

Stop Register= Store Address of Serial Access Use on the Split Transter Cycle Stop Pointer Set → CBRS Cycle							
Number of stop Points/Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3-A_0
1	(1×256)×2	x	1	1	1	1	x
2	(2×128)×2	x	0	1	1	1	x
4	(4×64)×2	x	0	0	1	1	x
8	(8×32)×2	x	0	0	0	1	x
16	(16×16)×2	x	0	0	0	0	x

*Other Case=Inhibit
X=Don't Care

DEVICE OPERATION (Continued)

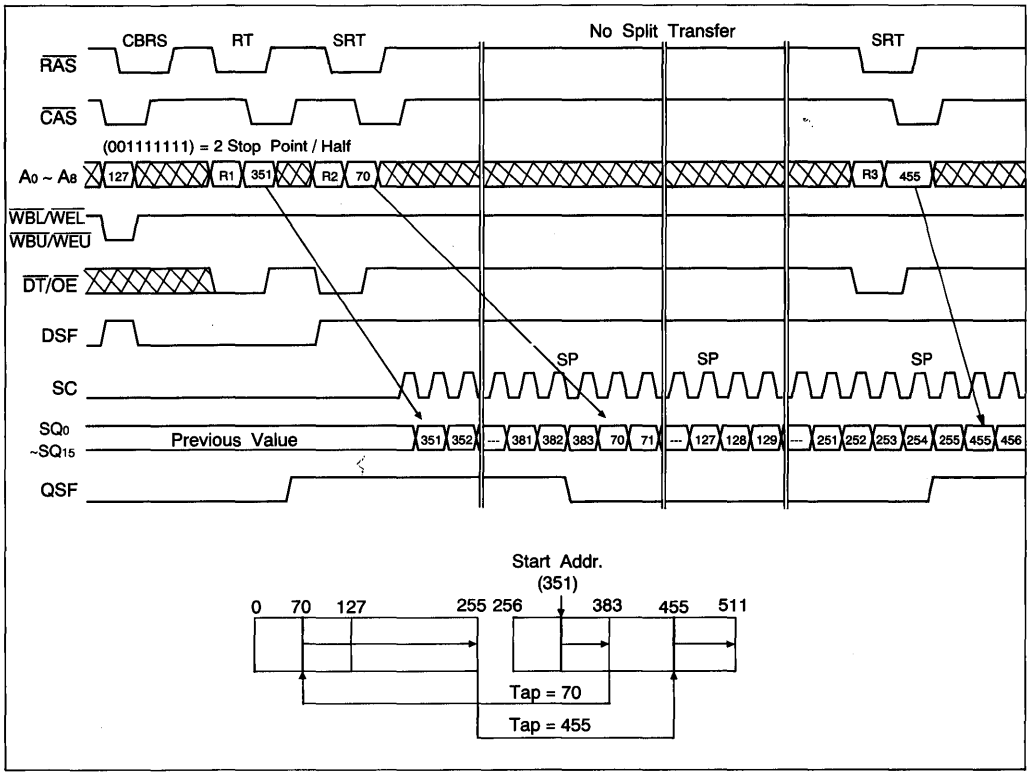
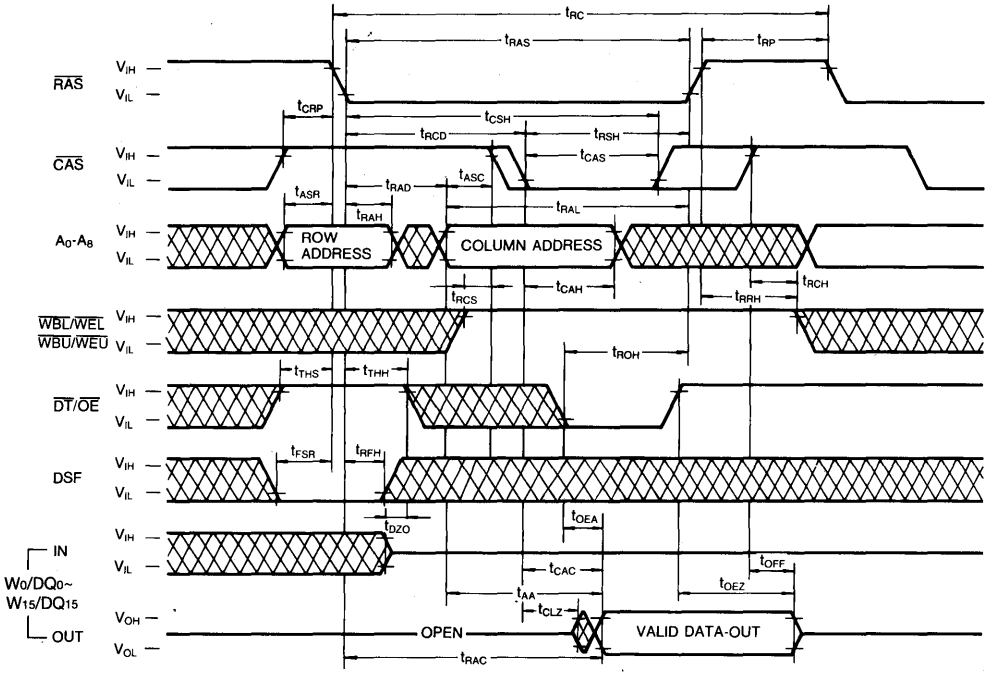


Figure 12. Programmable Split SAM operation

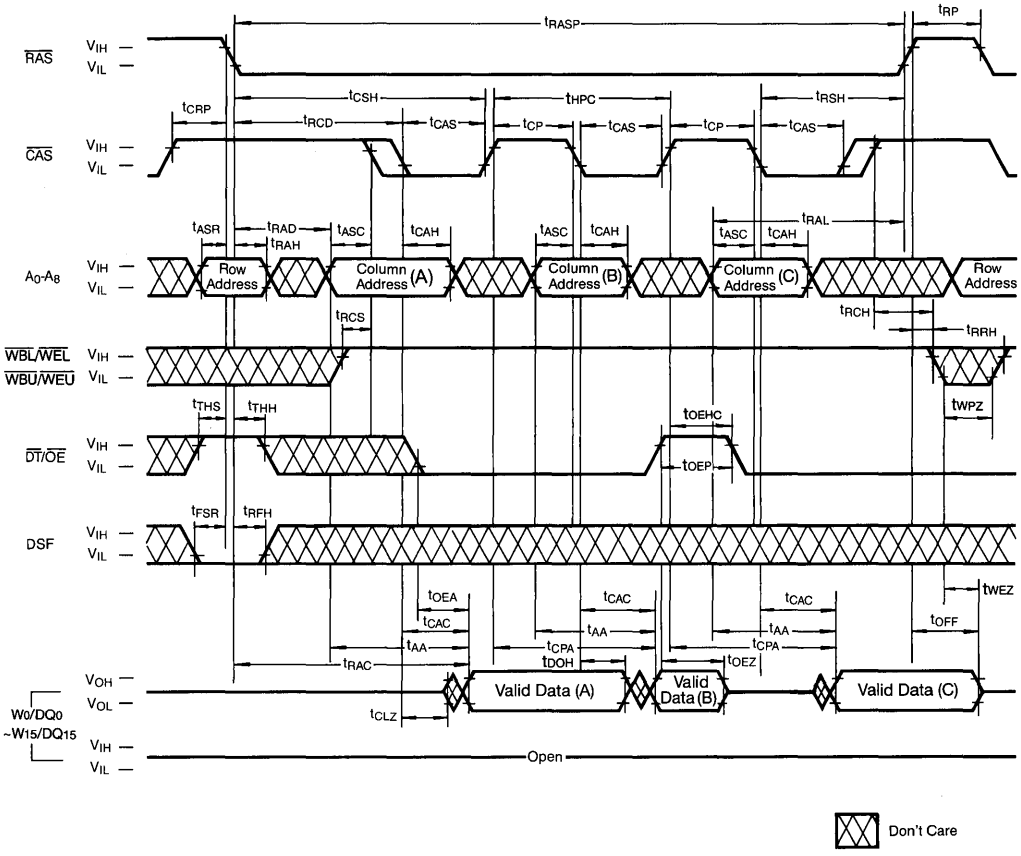
TIMING DIAGRAMS

READ CYCLE



Don't Care

FAST PAGE MODE READ CYCLE (Extended Data Out)



Truth Table for Write Cycle(1)

FUNCTION	RAS ↓			CAS ↓	CAS or WBL(U)/WEL(U)
	*1 WBL/WEL (WBU/WEU)	*2 DSF	*3 Wi/DQi (3) (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask) (4)	1	0	×	1	Column Mask
Masked Block Write (4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register (2)	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram on the following pages
(2) Old Mask data load
(3) Function table for Old Mask and New Mask

IF		*1 WBL/WEL	*1 WBU/WEU	*3 Wi/DQi	Note
LMR Cycle Executed	Yes	0	0	×	Write using mask register data
		0	1	×	(Old Mask Data)
		1	0	×	
		1	1	×	Non Masked Write
	No	0	0	Write Mask	Write using New Mask Data
		0	1		Wi/DQi=0 Write Disable
		1	0		Wi/DQi=1 Write Enable
		1	1	×	Non Masked Write

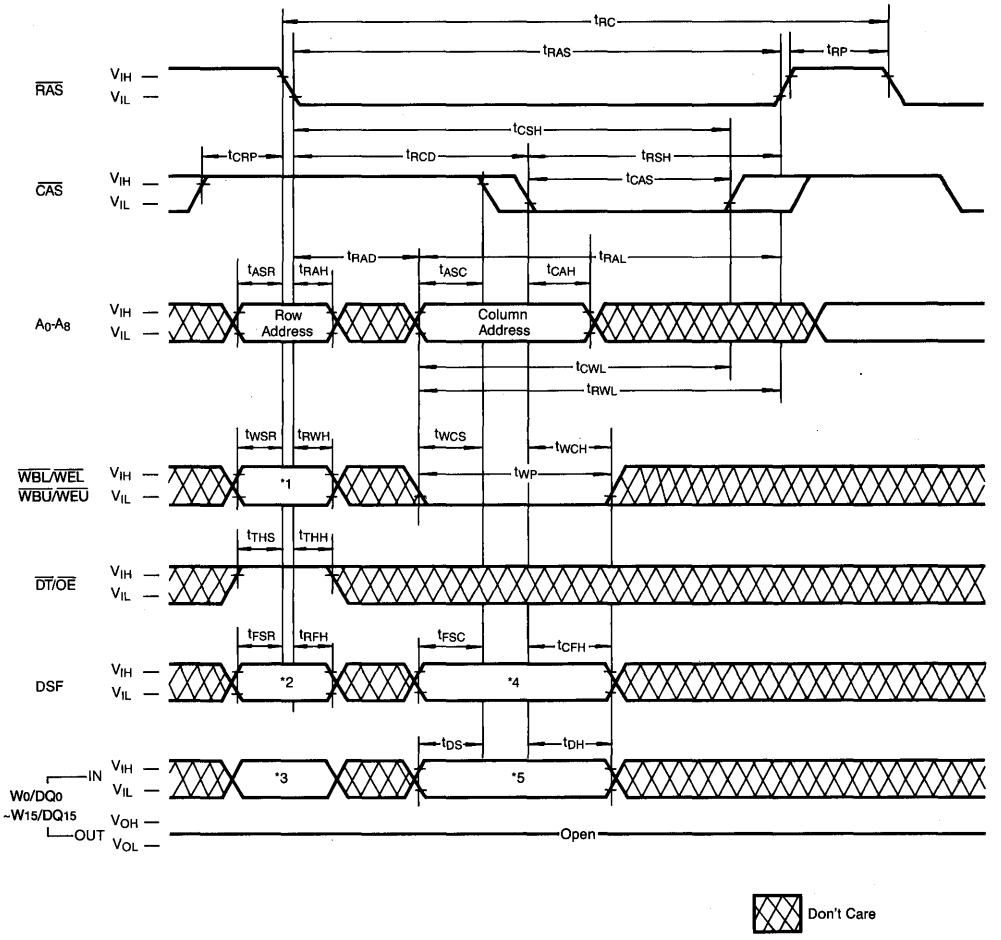
× : Don't Care

(4) Function Table for Block Write Column Mask

Column Address		
A2	A1	A0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

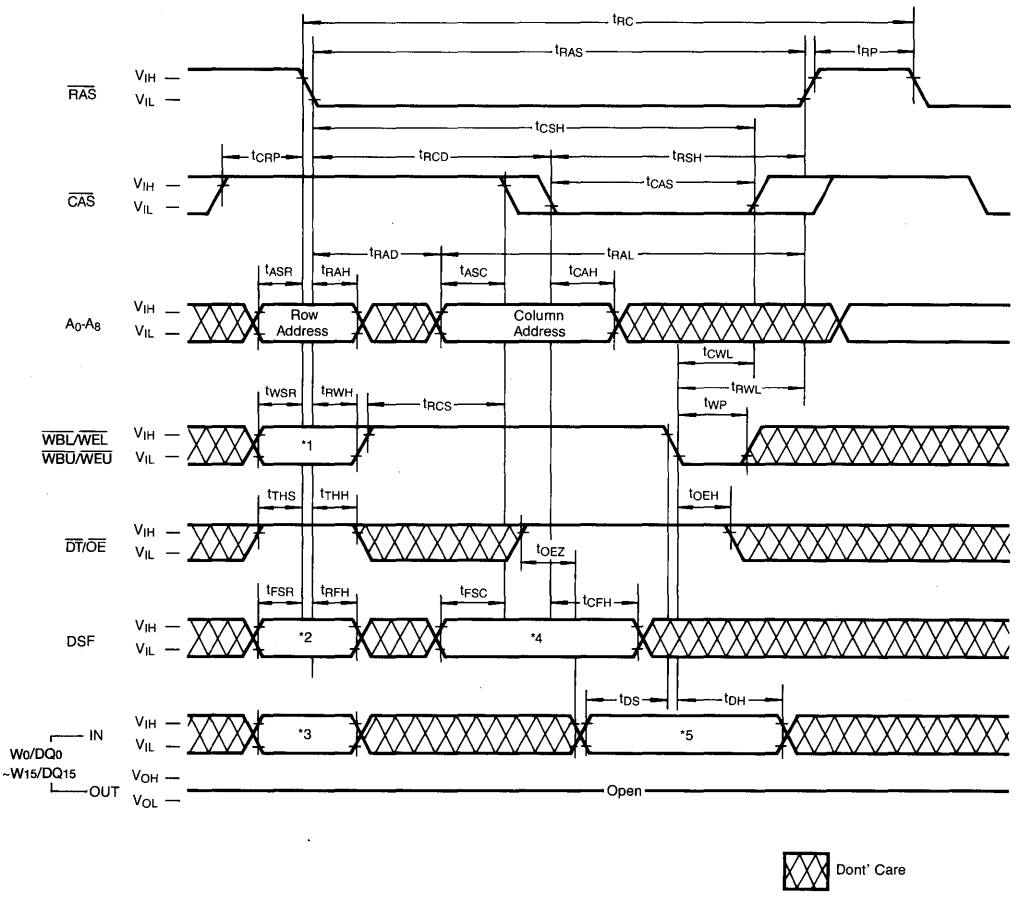
*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W0/DQ0	W8/DQ8	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
W1/DQ1	W9/DQ9		
W2/DQ2	W10/DQ10		
W3/DQ3	W11/DQ11		
W4/DQ4	W12/DQ12		
W5/DQ5	W13/DQ13		
W6/DQ6	W14/DQ14		
W7/DQ7	W15/DQ15		

EARLY WRITE CYCLE



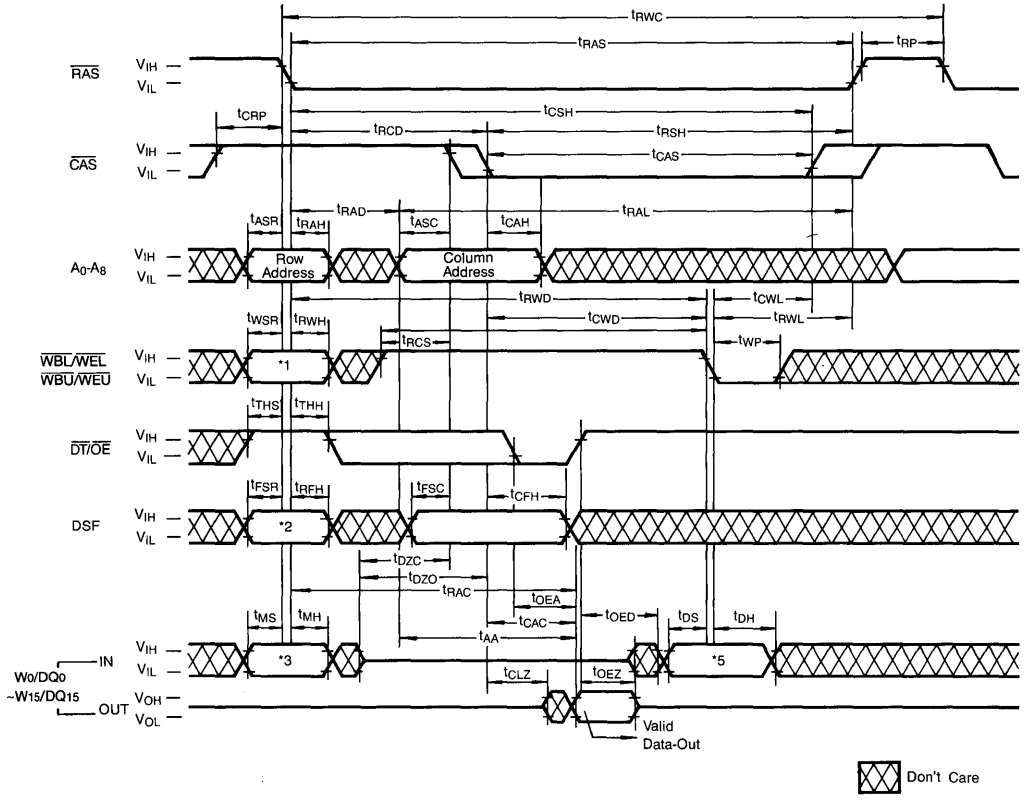
Note : In Block write cycle, only column address A_3~A_8 are used.

LATE WRITE CYCLE



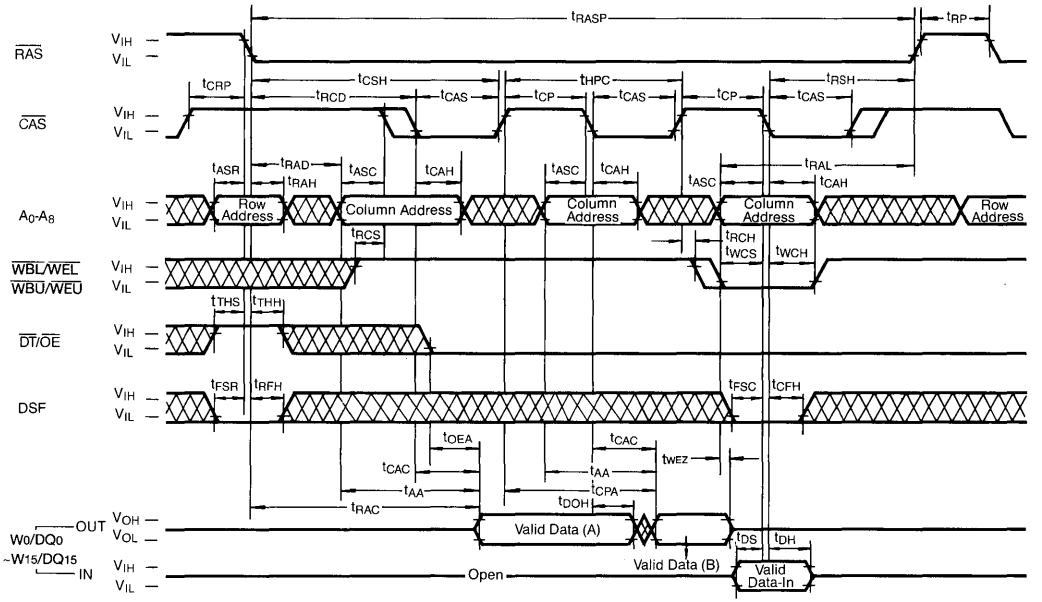
Note : In Block write cycle, only column address A_3~A_8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE

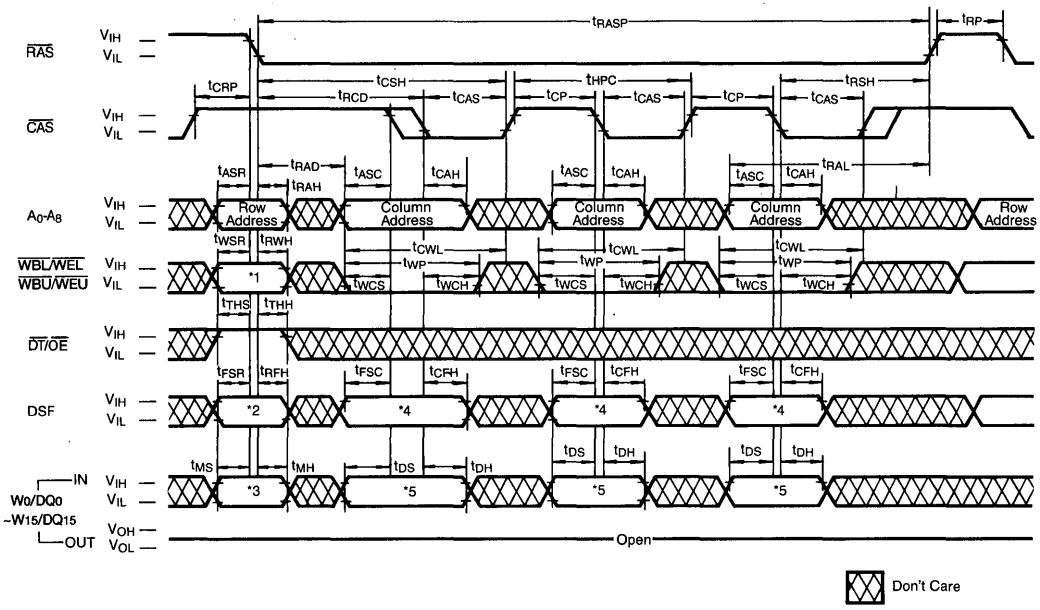


Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

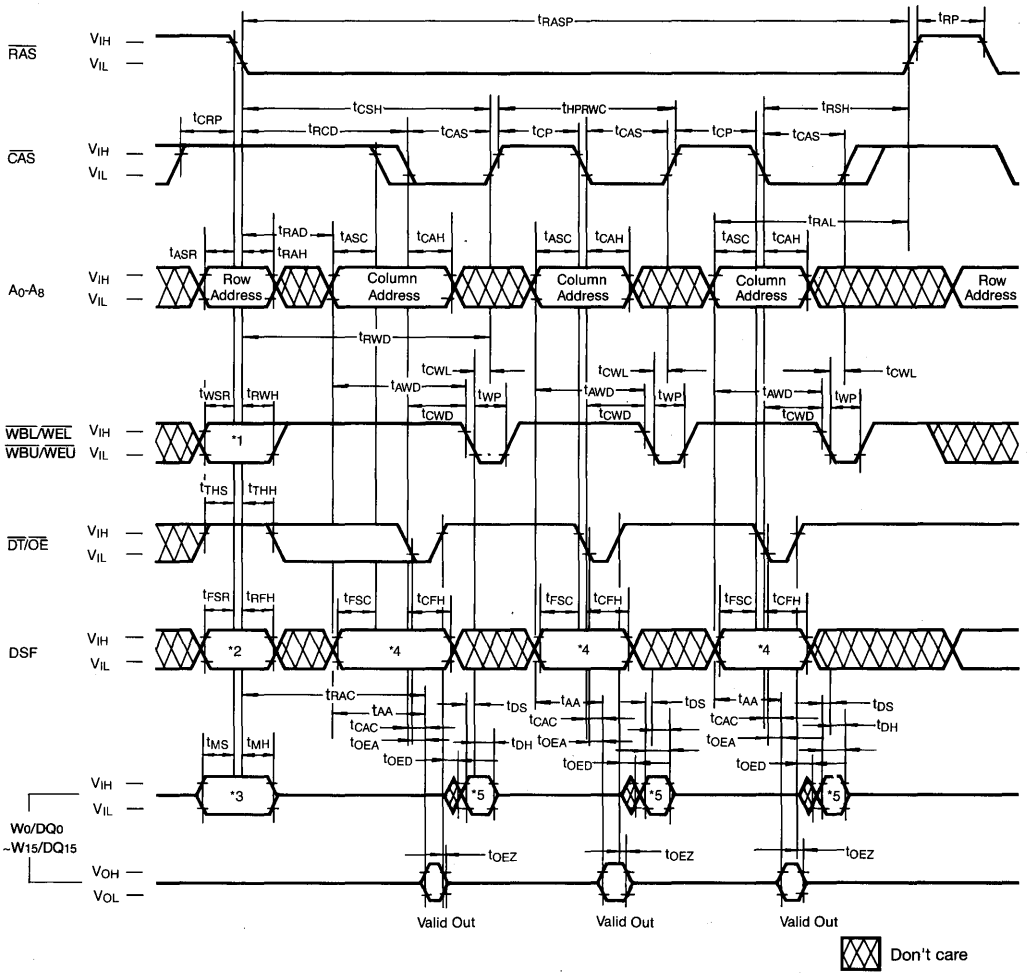


FAST PAGE MODE EARLY WRITE CYCLE



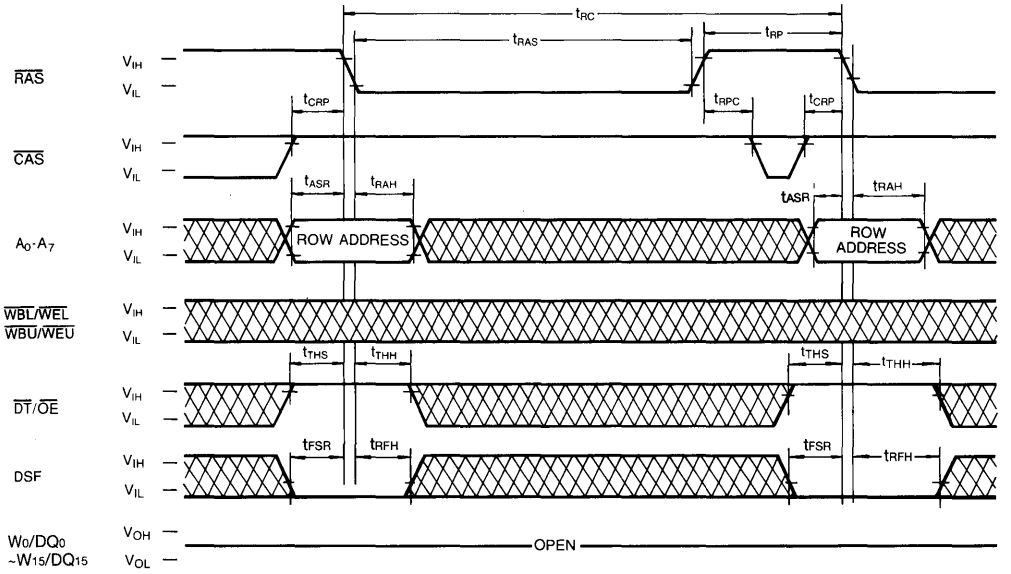
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



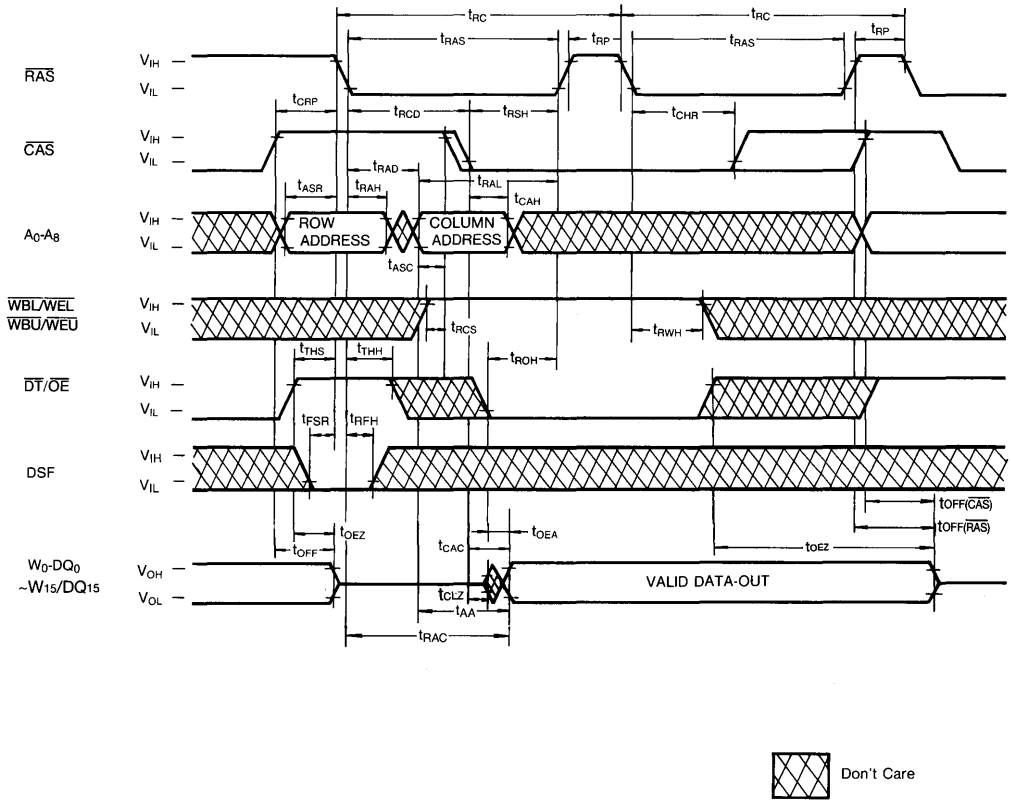
Note : In Block write cycle, only column address A3~A8 are used.

$\overline{RAS}$ ONLY REFRESH CYCLE

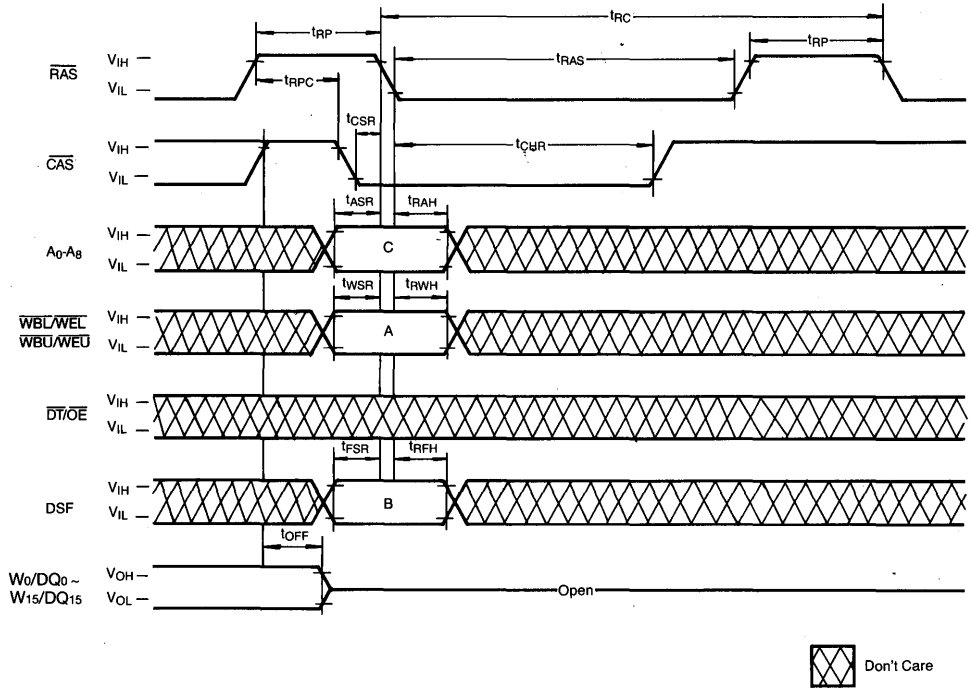


DON'T CARE

HIDDEN REFRESH CYCLE



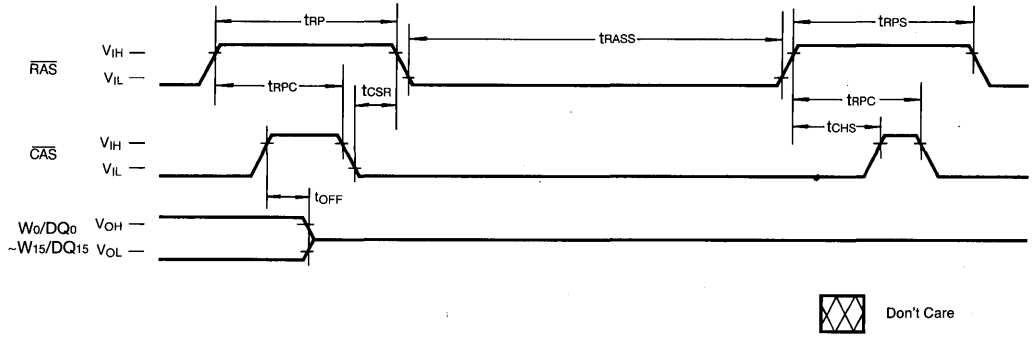
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE FUNCTION TABLE

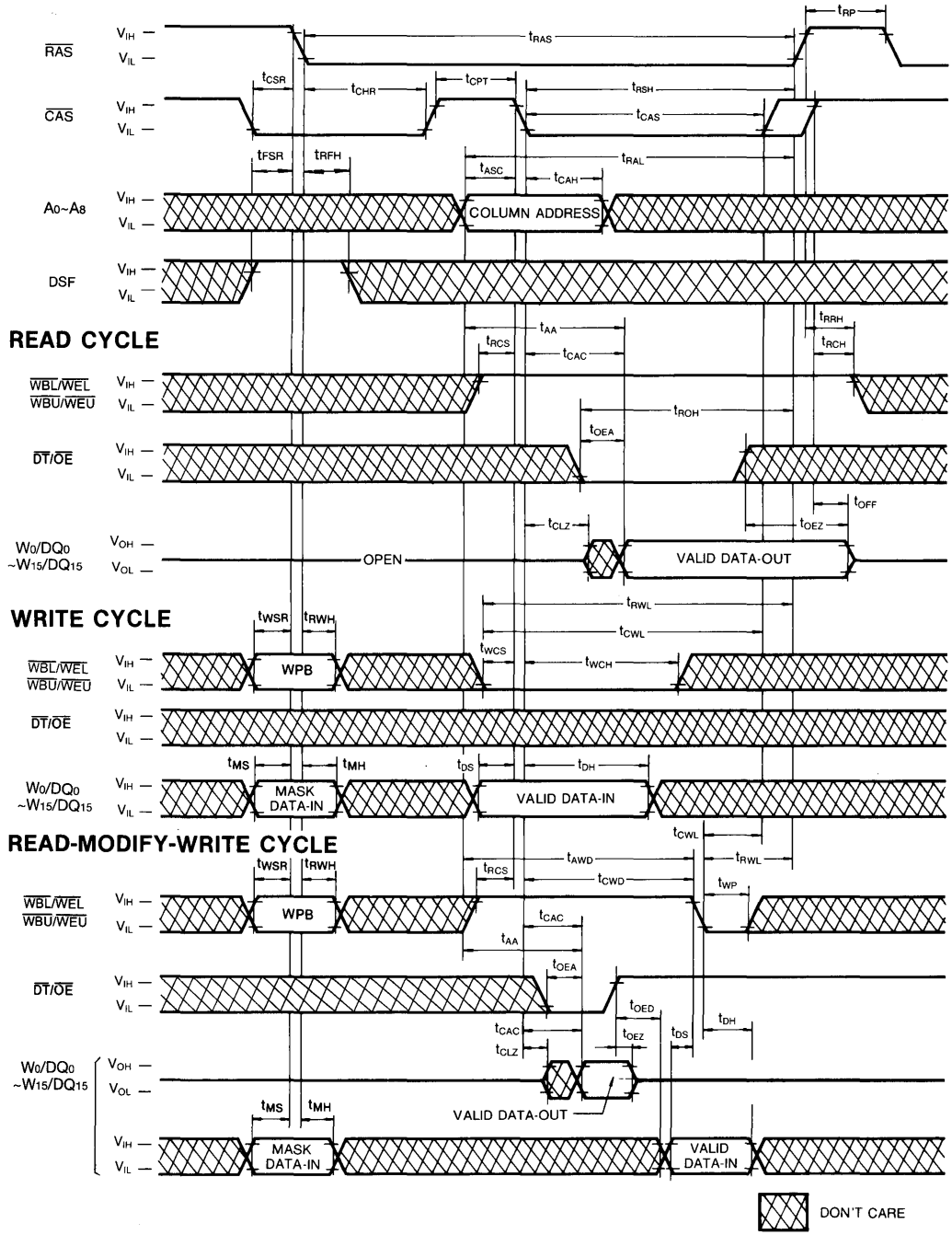
FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	STOP Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

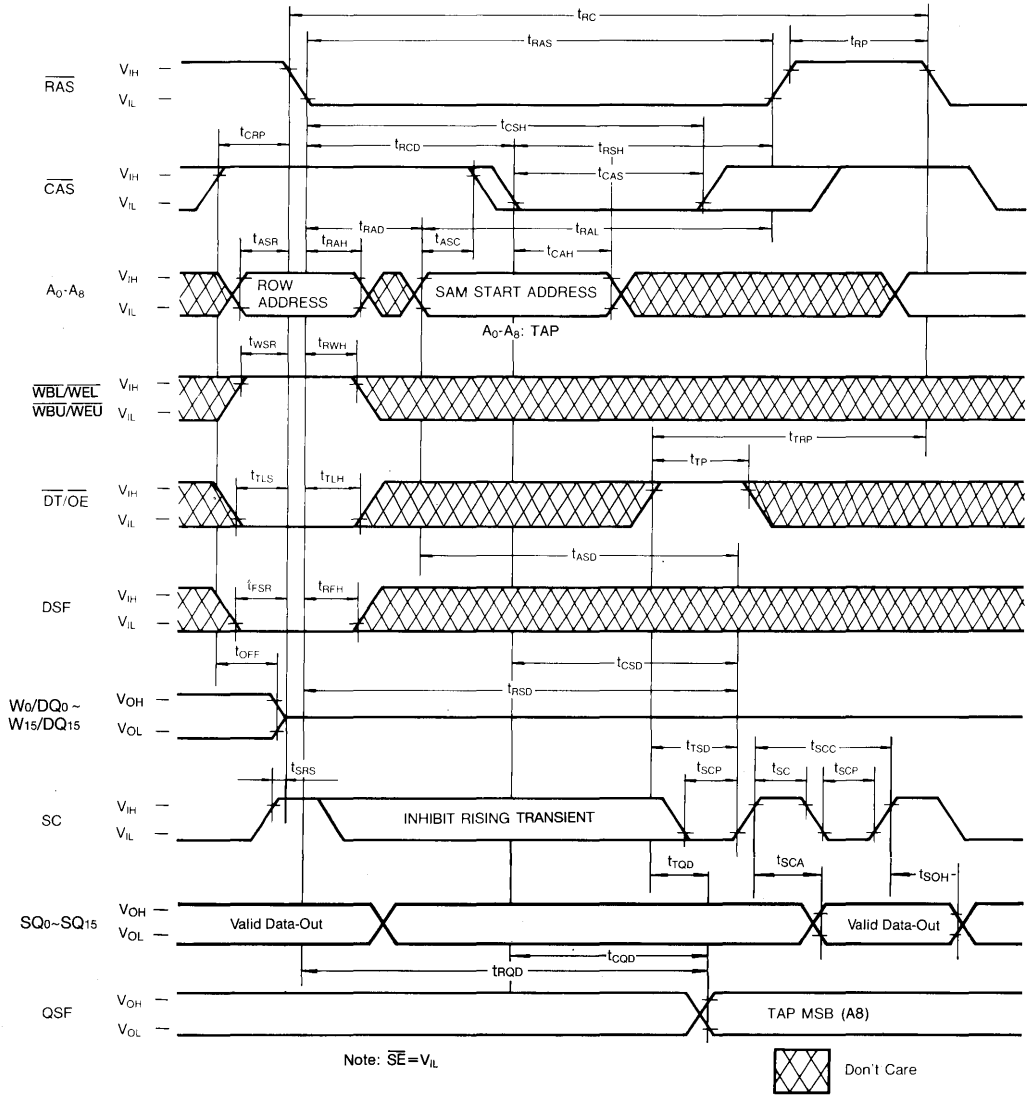


*CBR SELF REFRESH CYCLE IS APPLICABLE WITH CBRR, CBRS, OR CBRN CYCLE

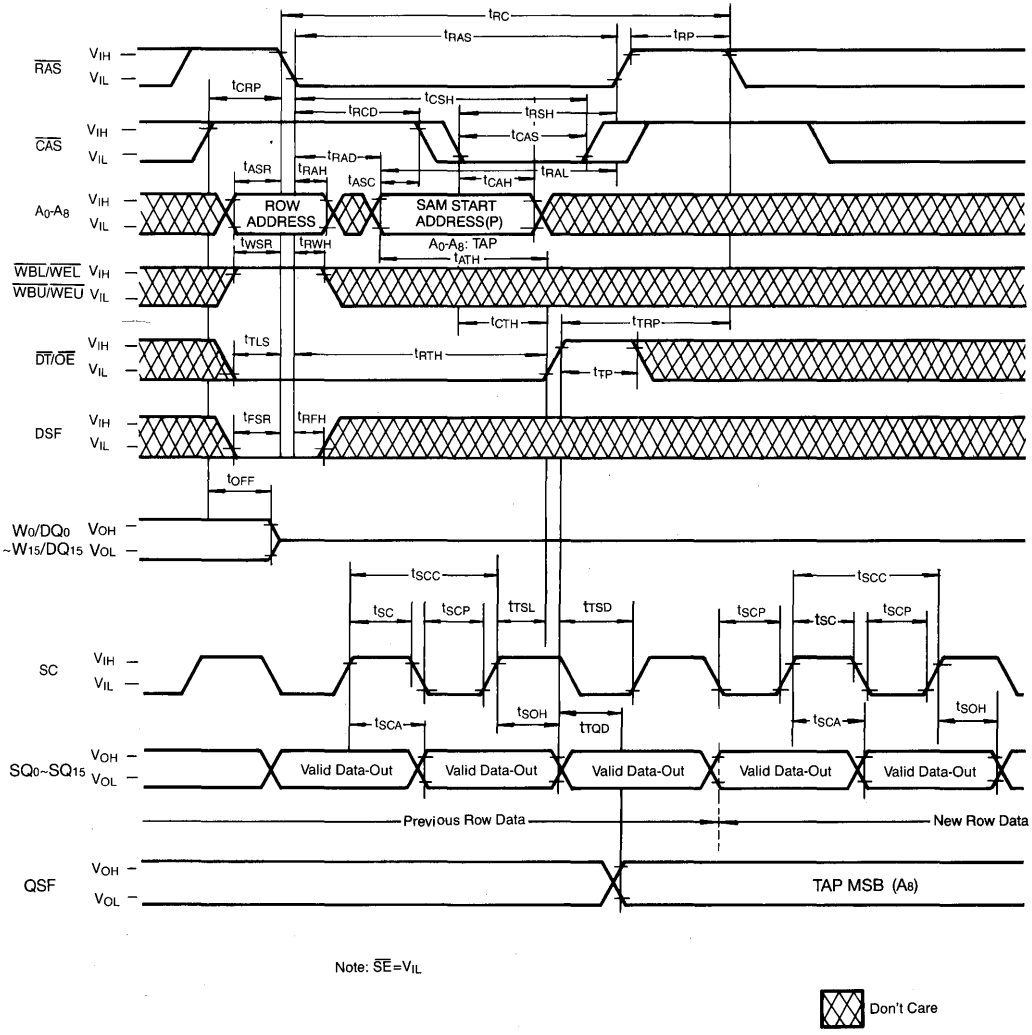
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



READ TRANSFER CYCLE



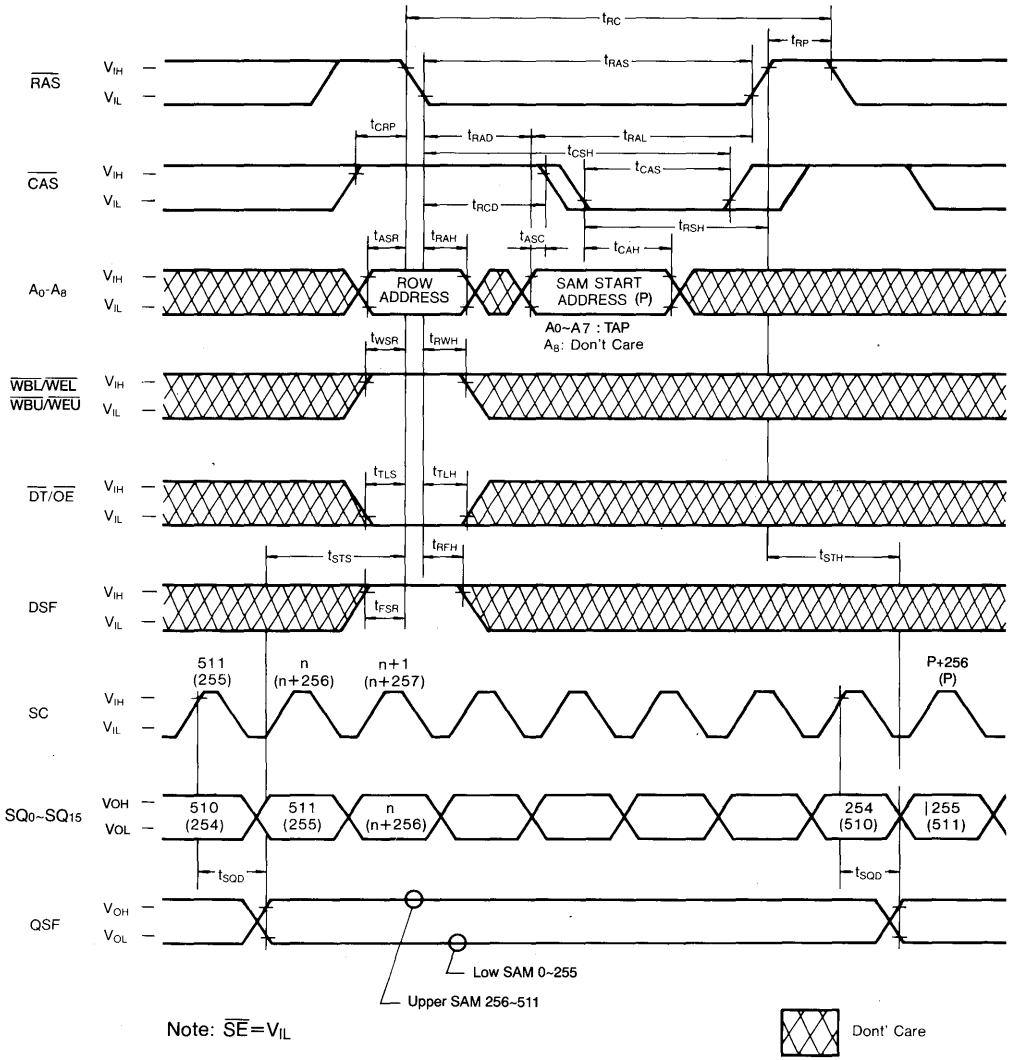
REAL TIME READ TRANSFER CYCLE



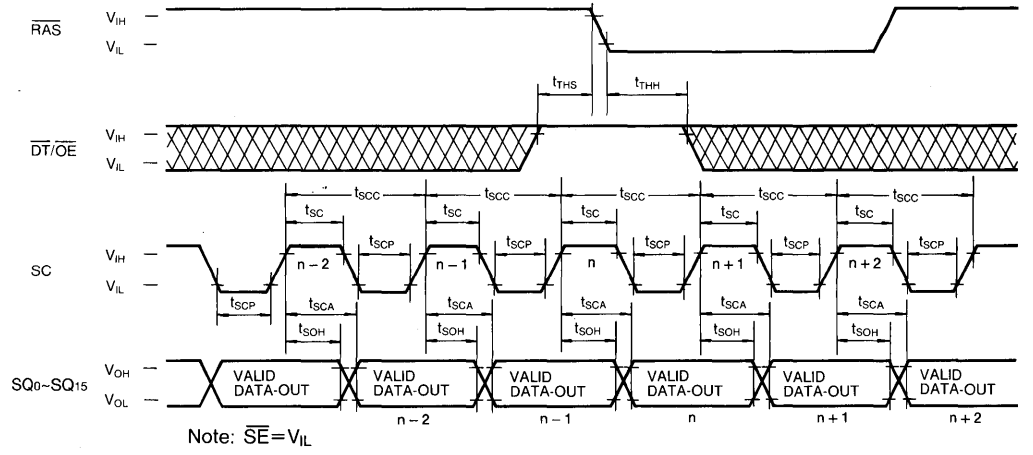
Note: $\overline{SE}$=V_{IL}

Don't Care

SPLIT READ TRANSFER CYCLE

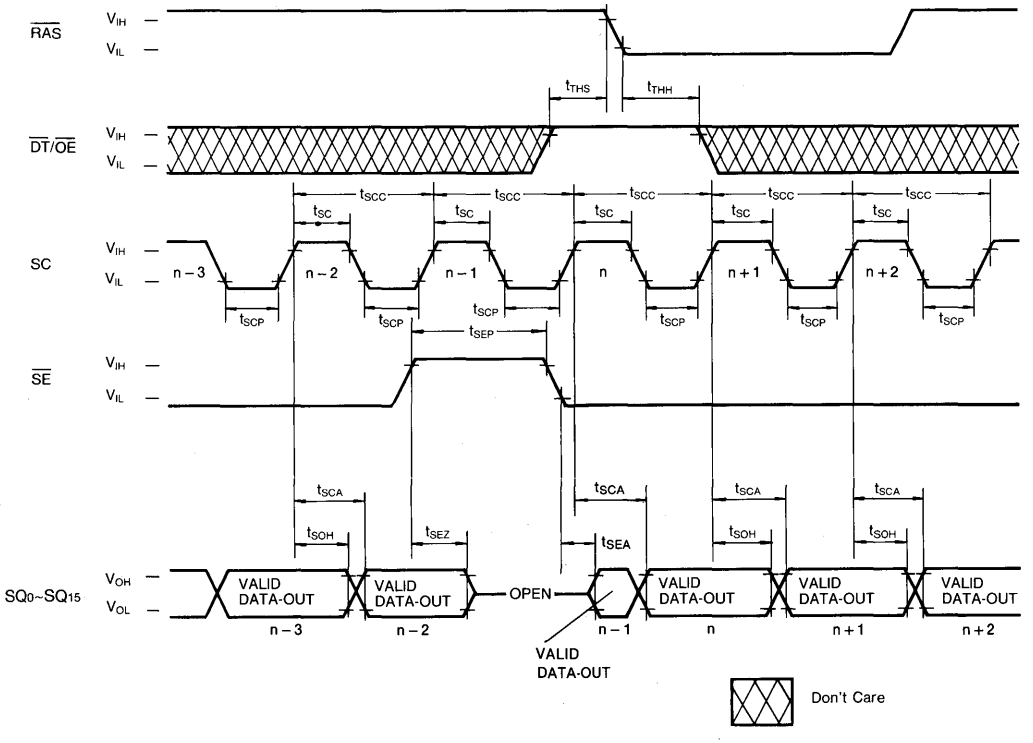


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$=V_{IL}

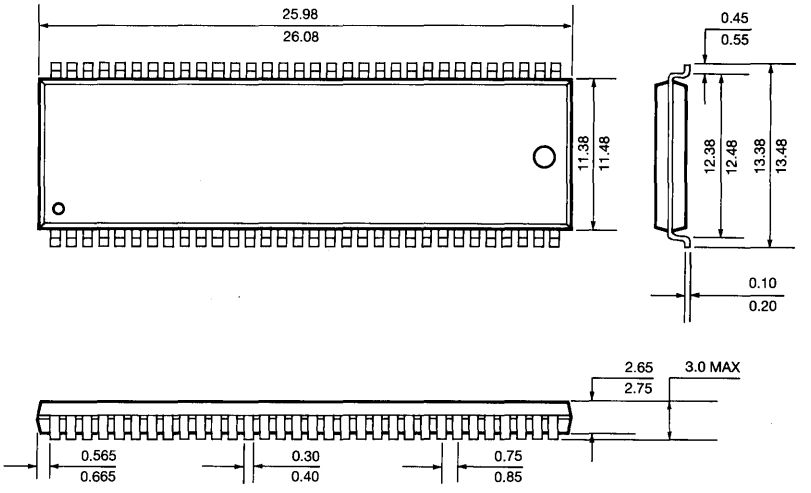
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



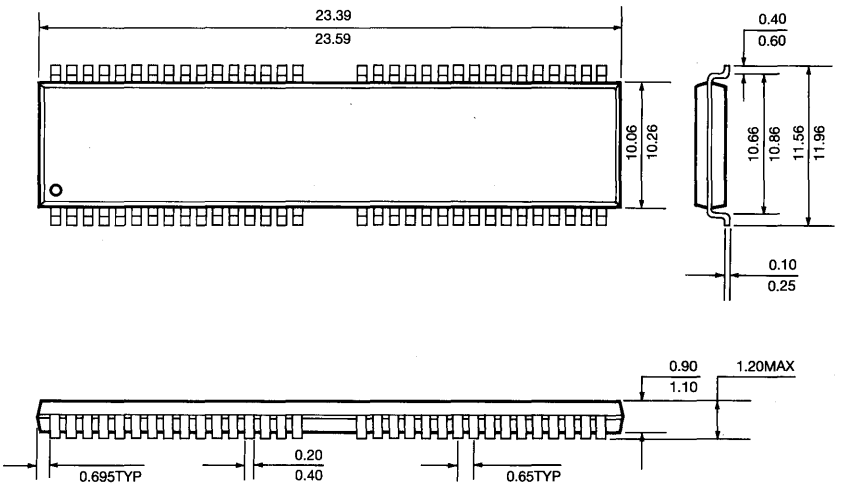
PACKAGE DIMENSIONS

Units: Millimeters

64 Pin Plastic Shrink Small Out Line Package



70(64) Pin Plastic Thin Small Out Line Package (Type II Forward)



256K × 16 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K × 16 bits RAM port
  512 × 16 bits SAM port
- **Performance range:**

Parameter \ Speed		-6	-70	-80
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{PC})	KM4216C257	40ns	45ns	50ns
	KM4216V257	40ns	45ns	50ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C257	120mA	110mA	100mA
	KM4216V257	110mA	100mA	90mA
SAM active current	KM4216C257	50mA	45mA	40mA
	KM4216V257	40mA	35mA	30mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **2 $\overline{CAS}$ Byte/Word Read/Write Operation**
- **8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single + 5V±10% Supply Voltage (KM4216C257)**
- **Single + 3.3V±10% Supply Voltage (KM4216V257)**
- **Plastic 64-Pin 525 mil SSOP (0.8mm pin pitch)**
- **Plastic 70-pin 400mil TSOP II(0.65mm pin pitch) (Forward and Reverse Type)**

- **Device Options** • **Part Marking**
  -. Low Power Dissipation
  Extended CBR Refresh (64ms) L
  -. Low Low Power Dissipation
  Self Refresh (128ms) F
- **Low Vcc(3.3V) Part Name: KM4216V257**

GENERAL DESCRIPTION

The Samsung KM4216C/V257 is a CMOS 256K × 16 bit Dual Port DRAM. It consists of a 256K × 16 dynamic random access memory (RAM) port and 512 × 16 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K × 16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access, 2 $\overline{CAS}$ Byte/word Read/write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM ports using read, and programmable (Stop Register) Split Transfers.

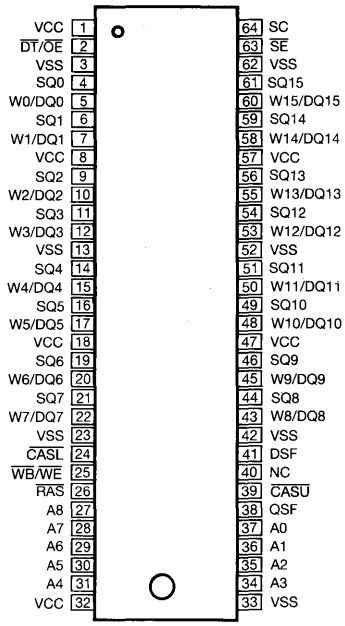
Refresh is accomplished by familiar DRAM refresh modes. The KM4216C/V257 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

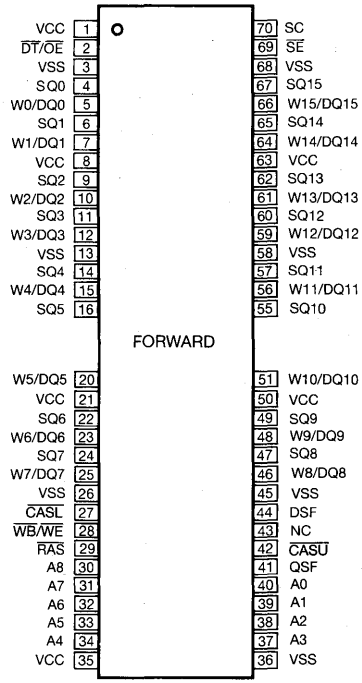
Pin Name		Pin Function
SC		Serial Clock
SQ_0-SQ_{15}		Serial Data Output
$\overline{DT}/\overline{OE}$		Data Transfer/Output Enable
$\overline{CASL}$, $\overline{CASU}$		Column Address Strobe (Lower /Upper)
$\overline{RAS}$		Row Address Strobe
$\overline{WB}/\overline{WE}$		Write Per Bit/Write Enable
W_0/DQ_0-W_{15}/DQ_{15}		Data Write Mask/Input/Output
$\overline{SE}$		Serial Enable
A_0-A_8		Address Inputs
DSF		Special Function Control
V_{CC}	KM4216C257	Power (+5V)
	KM4216V257	Power (+3.3V)
V_{SS}		Ground
QSF		Special Flag Out
N.C		No Connection

PIN CONFIGURATION (TOP VIEWS)

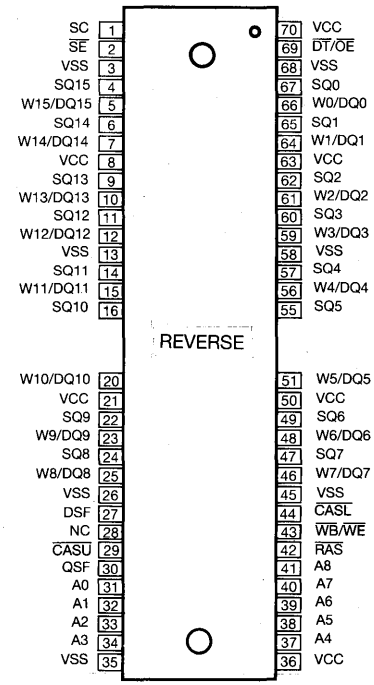
• **KM4216C/V257G/GL/GF**



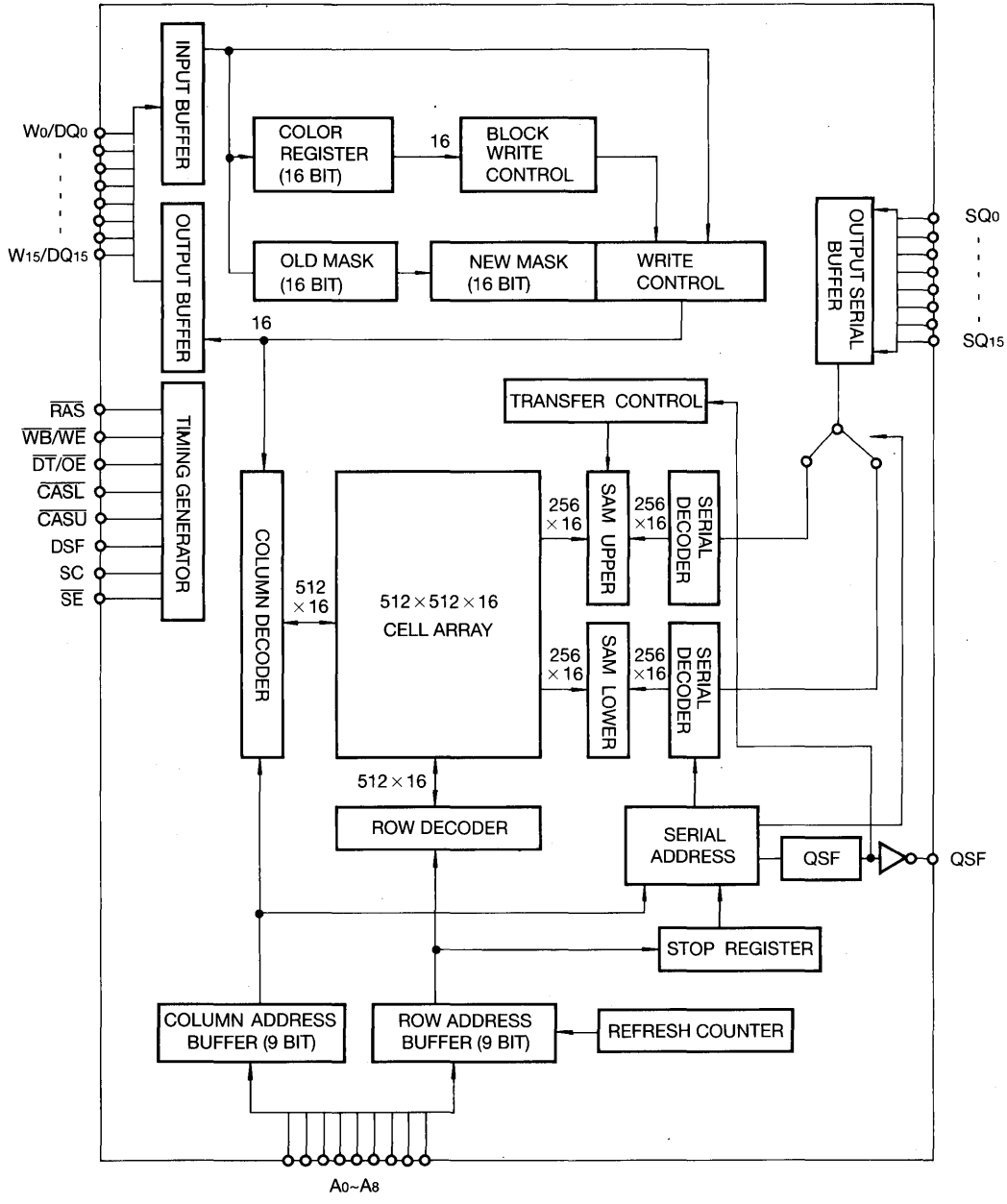
• **KM4216C/V257T/TL/TF**



• **KM4216C/V257R/RL/RF**



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic	RAS ↓				CAS ↓	Address		DQi Input		Register		Function
Code	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1.3)	0	×	0	1	-	Stop (Note4)	-	×	-	-	-	CBR Refresh/ Stop (No reset)
CBRN (Note 1)	0	×	1	1	-	×	-	×	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	×	×	0	-	×	-	×	-	-	-	CBR Refresh (Option reset)
ROR	1	1	×	0	-	ROW	-	×	-	-	-	RAS-only Refresh
RT	1	0	1	0	×	ROW	Tap	×	×	-	-	Read Transfer
SRT	1	0	1	1	×	ROW	Tap	×	×	-	-	Split Read Transfer
RWM	1	1	0	0	0	ROW	Col.	WMi	Data	Use	-	Masked write (New/Old Mask)
BWM	1	1	0	0	1	ROW	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New/Old Mask)
RW	1	1	1	0	0 (Note6)	ROW	Col.	×	Data	-	-	Read or Write
BW	1	1	1	0	1	ROW	Col.	×	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	ROW (Note7)	×	×	WMi	Load (Note5)	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	ROW (Note7)	×	×	Color		Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap:SAM Start (Column) Address, WMi : Write Mask Data (i=0~15)
RAS only refresh does not reset Stop or LMR functions.

Notes:
(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, CBRS or CBRN to perform CAS-before-RAS refresh while using Old mask)
(3) After CBRS Cycle, SRT use STOP Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The ROW that is addressed will be refreshed, but a ROW address is not reguired.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C257	KM4216V257	
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to + 150	55 to +150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	KM4216C257			KM4216V257			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$+0.5(0.3*1) all other pins not under test=0 volts).	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V257

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless other wise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C257			KM4216V257			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1	Standby*4	I_{CC1}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)	Active	I_{CC1A}	160	145	130	140	125	110	mA
Standby Current	Standby*4	I_{CC2}	10	10	10	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$=$V_{IH}$	Active	I_{CC2A}	50	45	40	40	35	30	mA
DSF=V_{IL})	Standby*4	I_{CC2C}*2	200	200	200	200	200	200	μA
	Standby*4	I_{CC2C}*3	150	150	150	150	150	150	μA
$\overline{RAS}$ Only Refresh Current*1	Standby*4	I_{CC3}	120	110	100	110	100	90	mA
($\overline{CAS}$-V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min	Active	I_{CC3A}	160	145	130	140	125	110	mA
Fast Page Mode Current*1	Standby*4	I_{CC4}	110	100	90	100	90	80	mA
($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cyciing @t_{PC}=min	Active	I_{CC4A}	150	135	120	130	115	110	mA
CAS Before-RAS Refresh Current*1	Standby*4	I_{CC5}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min	Active	I_{CC5A}	160	145	130	140	125	110	mA
Data Transfer Current *1	Standby*4	I_{CC6}	140	130	120	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC6A}	180	165	150	160	145	130	mA
Block Write Cycle Current *1	Standby*4	I_{CC7}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC7A}	160	145	130	140	125	110	mA
Color Register Load Current *1	Standby*4	I_{CC8}	110	90	80	90	80	70	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC8A}	140	125	110	120	105	90	mA
Battery Back Up Current *2 $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycling or $\leq V_{IL}$ $\overline{RAS}$=t_{RAS}(min) to 1μs t_{RC}=125 μs (64ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF$\geq V_{IH}$ or$\leq V_{IL}$	Standby*4	I_{CC9}	300	300	300	300	300	300	μA
Self Refresh Current *3 $\overline{RAS}$,$\overline{CAS}\leq$0.2V(128ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, A_0~A_8, DSF$\geq V_{CC}$ - 0.2v or$\leq$0.2V DQ0~15=Vcc-0.2V, 0.2V or OPEN	Standby*4	I_{CC10}	250	250	250	250	250	250	μA

Note *1 Real values dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, adress transition should be changed only once while RAS=V_{IL}.

In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$=V_{IH}

*2 KM4216C257L only : $V_{IH}\geq V_{CC}$-0.2V, $V_{IL}\leq$0.2V

*3 KM4216C257F only : $V_{IH}\geq V_{CC}$ -0.2V, $V_{IL}\leq$0.2V,

*4 SAM standby condition : $\overline{SE}\geq V_{IH}$, SC $\leq V_{IL}$ or $\geq V_{IL}$

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM4216C257 : V_{CC}=5.0V±10%, KM4216V257 : 3.3V±10%,)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		200		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,11
Access time from column address	t_{AA}		30		35		40	ns	3,5,6
Access time from CAS precharge	t_{CPA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	3
Transition time(rise and fall)	t_T	2	50	2	50	2	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	2
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	17
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	16
Column address hold time	t_{CAH}	10		12		15		ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	19
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		12		15		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		45		45		ns	8,18
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	tAWD	50		55		60		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	tCSR	10		10		10		ns	20
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHR	10		10		10		ns	21
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output Buffer turn-off delay from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	10		10		15		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	0		0		0		ns	15
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (real time read transfer)	tCTH	15		20		25		ns	
$\overline{DT}$ low hold referenced to column address (real time read transfer)	tATH	20		25		30		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	tRSD	60		70		80		ns	

AC CHARACTERISTICS (Continued)

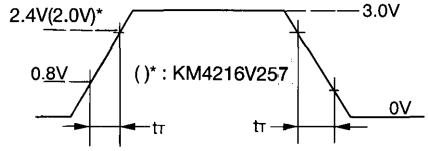
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to first SC delay (read transfer)	tCSD	25		30		40		ns	
Col. Address to first SC delay (read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	tTSD	10		10		15		ns	
LAST SC to $\overline{RAS}$ set-up time	tSRS	20		20		20		ns	
SC cycle time	tSCC	18		20		25		ns	14
SC pulse width (SC high time)	tSC	5		7		7		ns	
SC precharge (SC low time)	tSCP	5		7		7		ns	
Access time from SC	tSCA		15		17		20	ns	4
Serial output hold time from SC	tSOH	5		5		5		ns	
Access time from $\overline{SE}$	tSEA		15		17		20	ns	4
$\overline{SE}$ pulse width	tSE	20		20		25		ns	
$\overline{SE}$ precharge time	tSEP	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	7
Split transfer set-up time	tSTS	20		25		25		ns	
Split transfer hold time	tSTH	20		25		25		ns	
SC-QSF delay time	tSQD		20		25		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		25		25	ns	
$\overline{RAS}$-QSF delay time	tRQD		70		75		80	ns	
$\overline{CAS}$-QSF delay time	tCQD		35		35		40	ns	
$\overline{DT}$ to $\overline{RAS}$ Prechange time	tTRP	40		50		60		ns	

NOTES

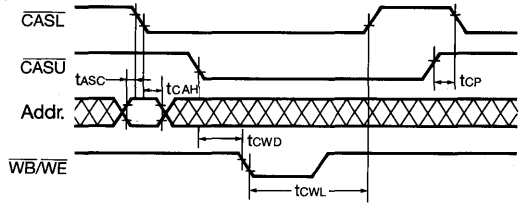
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ 8 SC cycles before proper device operation is achieved.($\overline{DT}/\overline{OE}$=High) if the intenal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required in stead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input siganl transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1TTL load and 50pF.
   D_{OUT} Comparator level : V_{OH}/V_{OL}=2.0V/0.8V.
4. SAM port outputs are measured with a load equivalent to 1TTL load and 30pF.
   D_{OUT} comparator level:V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the first $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below

Pin or REGISTER	STATUS
QSF	Hi-Z
Color Registe	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SDQi	Hi-Z

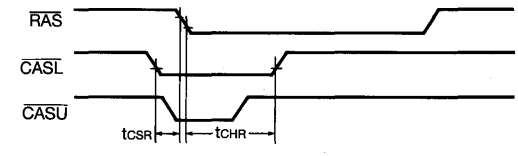
13. Recommended operating input condition.



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=5.0ns
14. Assume t_T=3ns.
15. Self refresh parameter (KM4216C/V257F)
    512K cycle of burst refresh must be executed within 8ms before and after self-refresh in order to meet refresh specification.
16. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
17. t_{CP} is specified from the last $\overline{CAS}$ rising edge in tne previous cycle to the first $\overline{CAS}$ falling edge in the next cycle
18. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
19. t_{CWL} is specified from $\overline{WB}/\overline{WE}$ faliing edge to the earlier $\overline{CAS}$ rising edge.



20. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
21. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



DEVICE OPERATION

The KM4216C/V257 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V257 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$). the column address strobe($\overline{CAS}$) and the valid row and coumn address inputs.

Operation of the KM4216C/V257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This the beginning of any KM4216C/V257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum RAS precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then tne access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}

The KM4216C/V257 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

DEVICE OPERATION (continued)

2$\overline{CAS}$ Byte/Word Read/Write Operation

The KM4216C/V257 has 2 $\overline{CAS}$ control pin, $\overline{CASL}$ and $\overline{CASU}$, and offers asynchronous Read/Write operation with lower byte (W_0/DQ_0~W_7/DQ_7) and upper bybe (W_8/DQ_8~W_{15}/DQ_{15}). This is called 2$\overline{CAS}$ Byte/Word Read/Write operation. This operation can be performed RAM Read in RAM write, Block write, Load Mask register, and Load Color register.

New Masked Write Per Bit

The New Masked Write Per Bit cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM.

The mask data is valid for only one cycle. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ low after $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

If $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed (see Figure2, 3). And If $\overline{CASL}$ is high during $\overline{WB}/\overline{WE}$ low, write operation of lower byte do not perform and if $\overline{CASU}$ is high, write operation of upper byte do not execute.

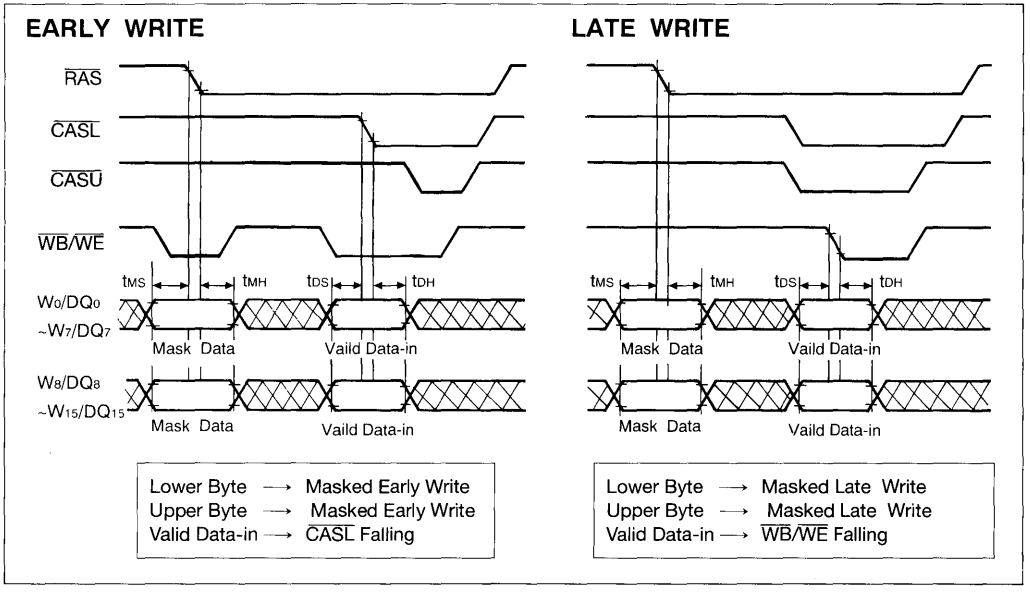


Figure 1. Byte Write and New Masked Write Cycle Example 1. (Early Write & Late Write)

DEVICE OPERATION (continued)

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of $\overline{CAS}$ or $\overline{WB/WE}$.

The LMR cycle is performed if DSF high, $\overline{WB/WE}$ high at the $\overline{RAS}$ falling edge. And DSF low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM4216C/V257 are set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked write are Old Masked Write Per Bit and the I/O mask data wil be provided by the Mask Data Register (See Figure 4.)

The mask data is applied in the same manner as in New Masked write Per Bit mode.

Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After power-up, the KM4216C/V257 Initializes in the New Masked write mode.

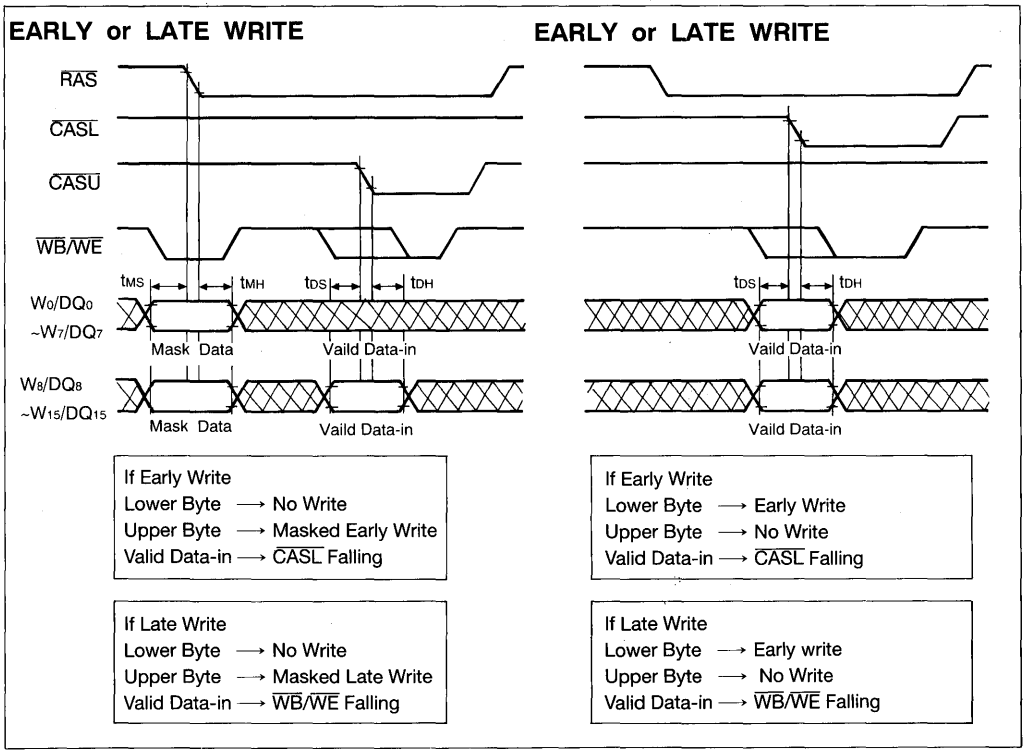


Figure 2. Byte Write and New Masked Write Cycle Example 2.

DEVICE OPERATION (continued)

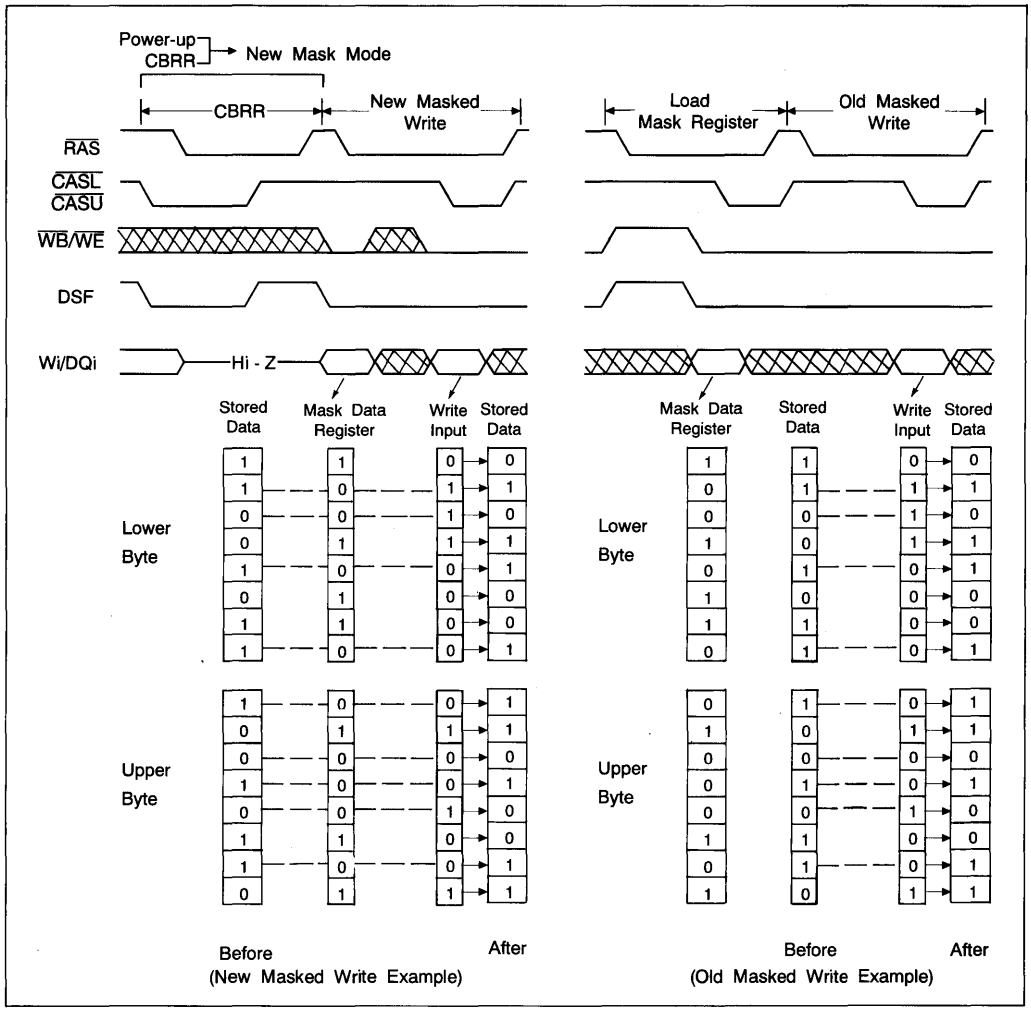


Figure 3. New Masked Write Cycle and Old Masked Write Cycle Example

Fast Page Mode

The KM4216C/V257 has Fast Page mode capability provides high speed read, write or read-modify-write access to all memory locations Within a selected row. In this cycle, read, write, read-modify write, and block write cycles can be mixed in any order.
In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

DEVICE OPERATION (continued)

Load Color Register(LCR)

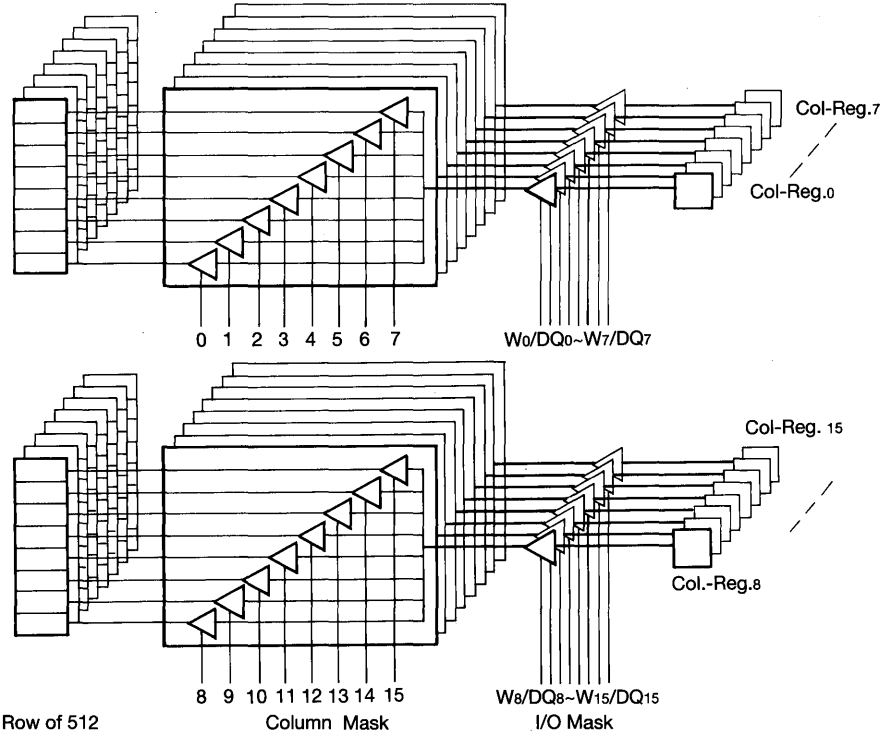
A Load Color register cycle is performed by keeping DSF high on the both falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded in the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(late write) via the W_0/DQ_0~w_7/DQ_7(Lower Byte), W_8/DQ_8~W_{15}/DQ_{15} (Upper Byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register Cycle.

Block Write

In a Block write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each correspeonding bit plane(16). This result in a total of 128-bits Written in a single Block write cycle compared to 16-bit in a normal write cycle.

The Block write cycle is performed if DSF is low at the falling edge of $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



	$\overline{RAS}$
W_0/DQ_0~7	Lower Block I/O Mask
W_8/DQ_8~15	Upper Block I/O Mask

	$\overline{CAS}$
A_0~A_2	Don't Care
W_0/DQ_0~7	Lower Block Column Select
W_8/DQ_8~15	Upper Block Column Select

A_2~A_0	Lower	Upper	Column Mask	
0 0 0	W_0/DQ_0	W_8/DQ_8		
0 0 1	W_1/DQ_1	W_9/DQ_9	DQi=1	Column
0 1 0	W_2/DQ_2	W_{10}/DQ_{10}		Enable
0 1 1	W_3/DQ_3	W_{11}/DQ_{11}		
1 0 0	W_4/DQ_4	W_{12}/DQ_{12}		
1 0 1	W_5/DQ_5	W_{13}/DQ_{13}	DQi=0	Column
1 1 0	W_6/DQ_6	W_{14}/DQ_{14}		Disable
1 1 1	W_7/DQ_7	W_{15}/DQ_{15}		

Figure 4. Block Write Scheme

DEVICE OPERATION (continued)

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.
Since 8 columns are being written at a time, the minimum increment required for the column address is latched on the falling edge of $\overline{CAS}$, the 3 LSBs, A_0, A_1, and A_2 are ignored and only bits (A_3~A_8) are used to define the location of the first bit out of the eight to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16 -bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the eight, but the second remains unchanged. Fig. 4 shows the correspondence of each data line to the column mask bits.
A Masked Block Write cycle is identical to a New/old Masked Write-Per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB/WE}$ must be low at the falling edge of $\overline{RAS}$. And DSF must be high on the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0~W_{15}/DQ_{15} pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. In Old mask mode, I/O mask data will be provided by the Mask Data Register.

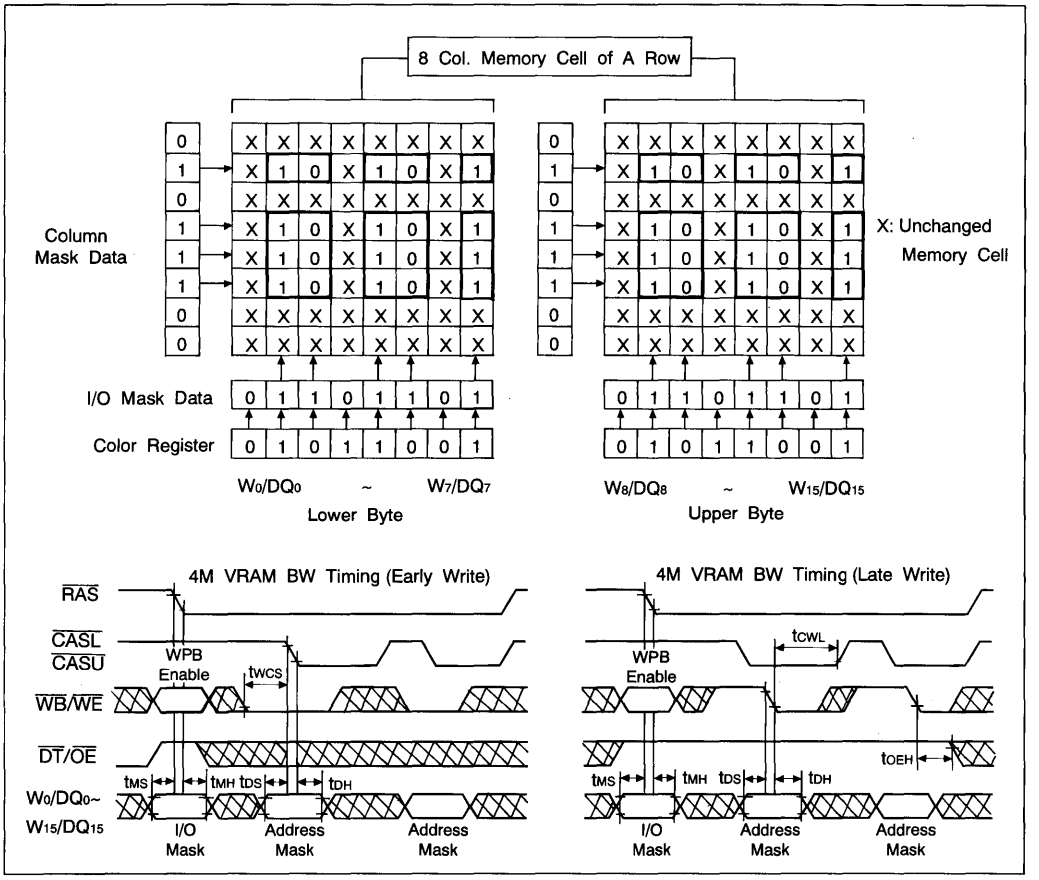


Figure 5. Block Write Example and Timing

DEVICE OPERATIONS (Continued)

Data Output

The KM4216C/V257 has three state output buffer Controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}$,$\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is in high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output duing the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM4216C/V257 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) befor $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled.
An internal refresh operatian occurs automatically. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
The KM4216C/V257 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation ; CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values.
CBRN (CBR refresh without reset) is set if DSF high when $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$ and simply do only refresh operation.
CRRS(CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WB}/\overline{WE}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V257 hidden refresh cycle is actually a $\overline{CAS}$-beford-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh *(Only KM4216C/V257F)* : The Self Refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for longer periods of standby, such as a battery back-up. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If $\overline{RAS}$ is low more than 100μs at the condition of CBR, Self Refresh function is accomplished. In this state, the external refresh address do not need to supply additionally on-chip because the refresh counter on-chip gives that addresses needed to refresh. Please note that the ending point of Self Refresh is when $\overline{RAS}$ and $\overline{CAS}$ is high and t_{RPS} of Self Refresh is the time reguiring to complete the last refresh of Self Refresh.

Other Refresh Methods : It is also possible to refresh the KM4216C/V257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS (Continued)

Table 1. Truth Table for Transfer Operation *: Don't care

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bit
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	$\overline{SE}$			
H	L	H	L	*	Read Transfer	RAM→SAM	512 × 16
H	L	H	H	*	Split Read Transfer	RAM→SAM	256 × 16

Transfer Operation

Transfer operation is initiated when $\overline{DT/OE}$ is low at the falling edge of $\overline{RAS}$. The state of DSF when $\overline{RAS}$ goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation. (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT/OE}$ is low, $\overline{WB/WE}$ is high, and DSF is low at the falling edge of $\overline{RAS}$. The row address bits in the read transfer cycle indicate which sixteen 512 bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half). Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC, $\overline{DT/OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT/OE}$ must be Synchronized with the rising edge of SC (t_{TSL}/t_{TSD}) to retain the continuity of Sevial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT/OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, $\overline{DT/OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT/OE}$.

The Split Read Transfer cycle elinimates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT/OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

DEVICE OPERATIONS (Continued)

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched in the falling edge of $\overline{RAS}$. The column address defined by (A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. column addrress pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1= Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g.255th or 511th bit).
Example of SRT applications are shown in Fig.6 through Fig. 9

The normal usage of Split Read Transfer cycle is described in Fig.6. When Read Transfer is executed, data from X_1 row address is fully transferred to the SAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X_2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y_0" Tap address instead of "Y_0" is loaded.
The another example of SRT cycle is described in Fig.7 When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 8 and 10 are the exanple of abnormal SRT cycle.

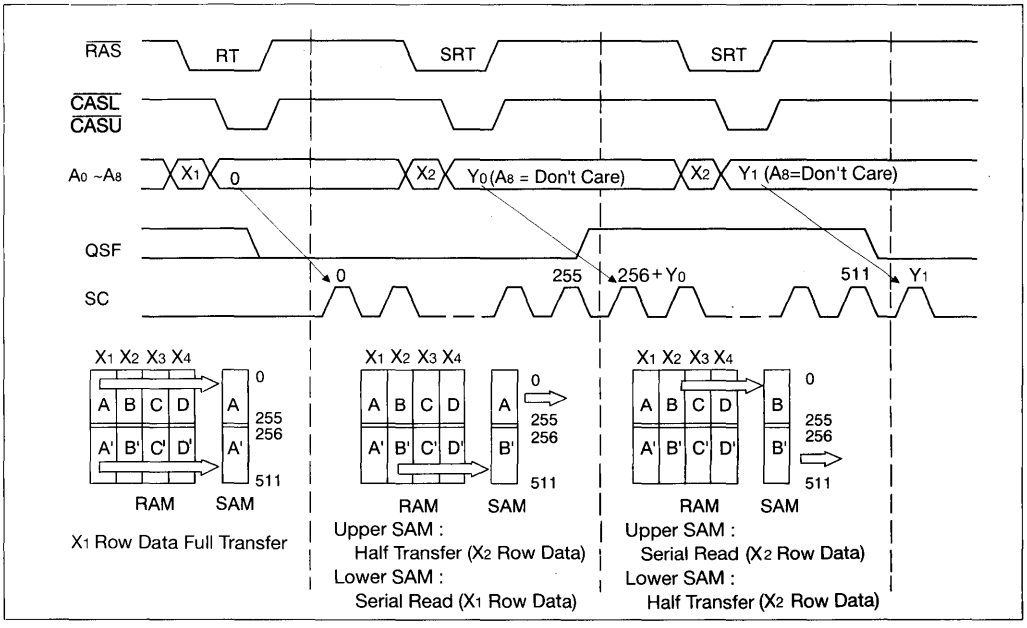


Figure 6. Split Read Transfer Normal Usage (Case1)

DEVICE OPERATIONS (Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig.8, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 9 indicates that SRT cycle is not performed until Serial Read is completed to the boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+ t_{STS}(See Figure 10)

A split Read Transfer does not change the direction of the SAM I/O port.

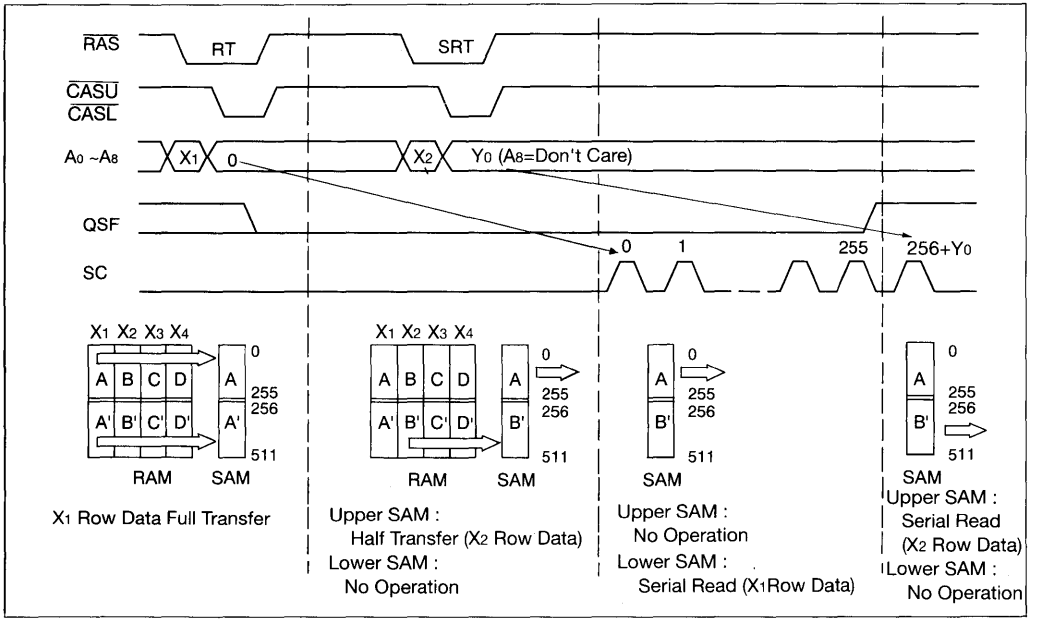


Figure 7. Split Read Transfer Normal Usage (Case 2)

DEVICE OPERATIONS (Continued)

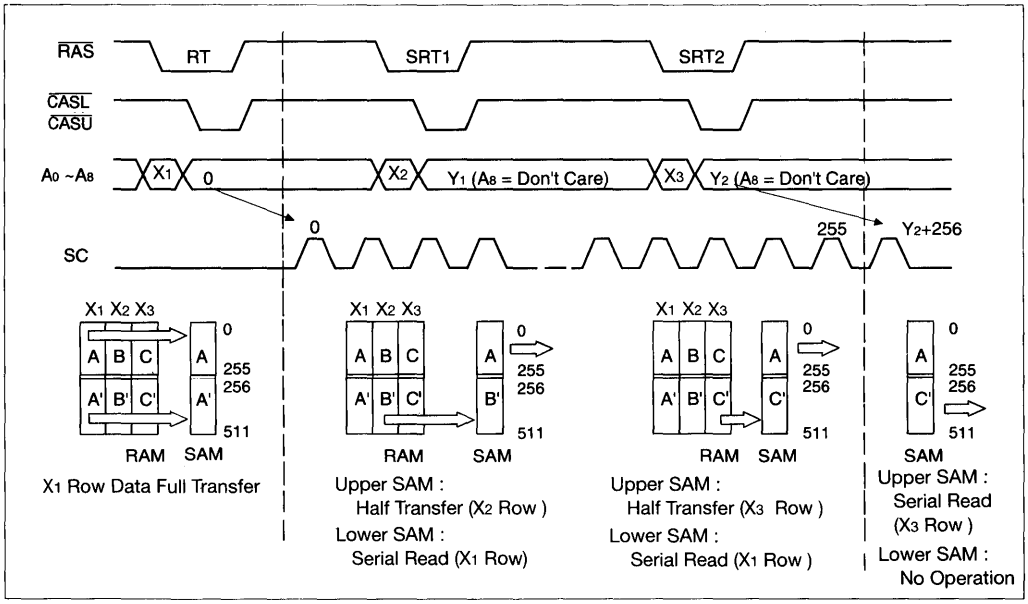


Figure 8. Split Read Transfer Abnormal Usage (Case 1)

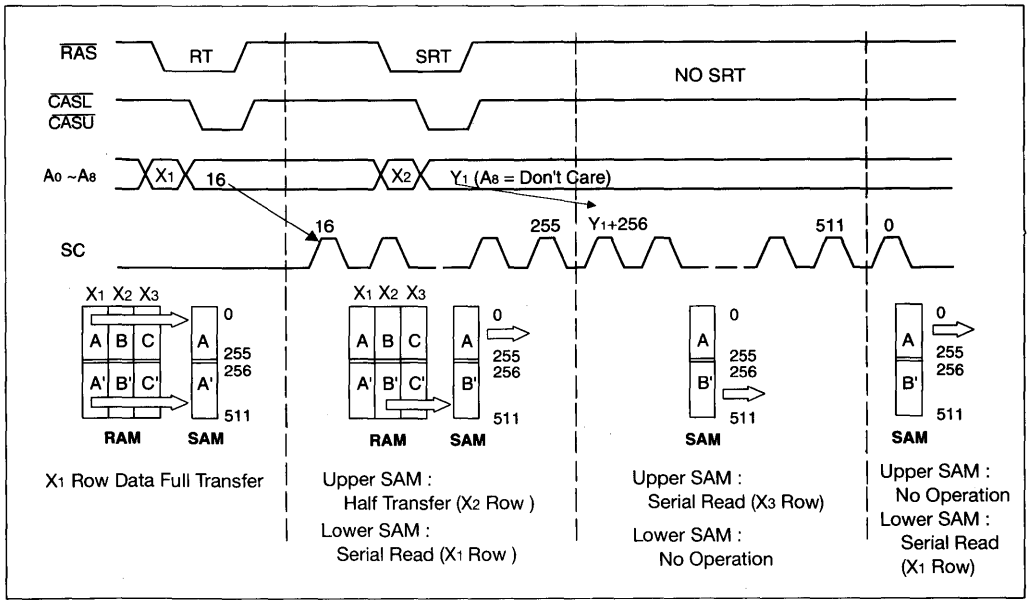


Figure 9. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATIONS (Continued)

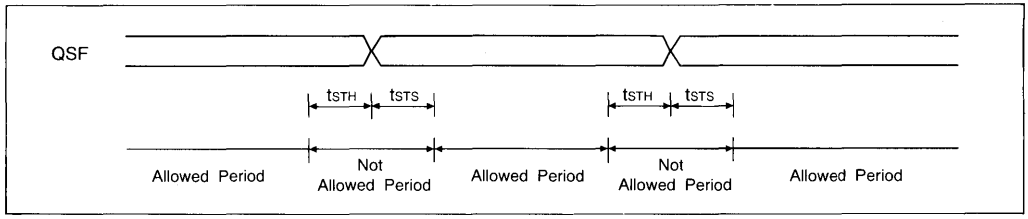


Figure 10. Split Transfer Cycle Limitation Period

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half.
After the last address of each half SAM(255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded TAP address).
This last address is called Stop Point.
The KM4216C/V257 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WB}/\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.
The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.
In Figure 11. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address(70) of the next half. Otherwise, the axxess will continue in the same half until a SRT occurs or the SAM half boundary (255, 511).
Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. DBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$. The CBRR wil take effect immediately; it does not require a SRT to become active valid.

Table 2. Stop Point Setting Address

Stop Register= Store Address of Serial Access Use on the Split Transter Cycle Stop Pointer Set → CBRS Cycle							
Number of Stop Points/Half	**Partition**	**Stop Point Setting Address**					
		A_8	**A_7**	**A_6**	**A_5**	**A_4**	**A_3~A_0**
1	(1×256)×2	x	1	1	1	1	x
2	(2×128)×2	x	0	1	1	1	x
4	(4×64)×2	x	0	0	1	1	x
8	(8×32)×2	x	0	0	0	1	x
16	(16×16)×2	x	0	0	0	0	x

*Other Case=Inhibit
X=Don't Care

DEVICE OPERATION (continued)

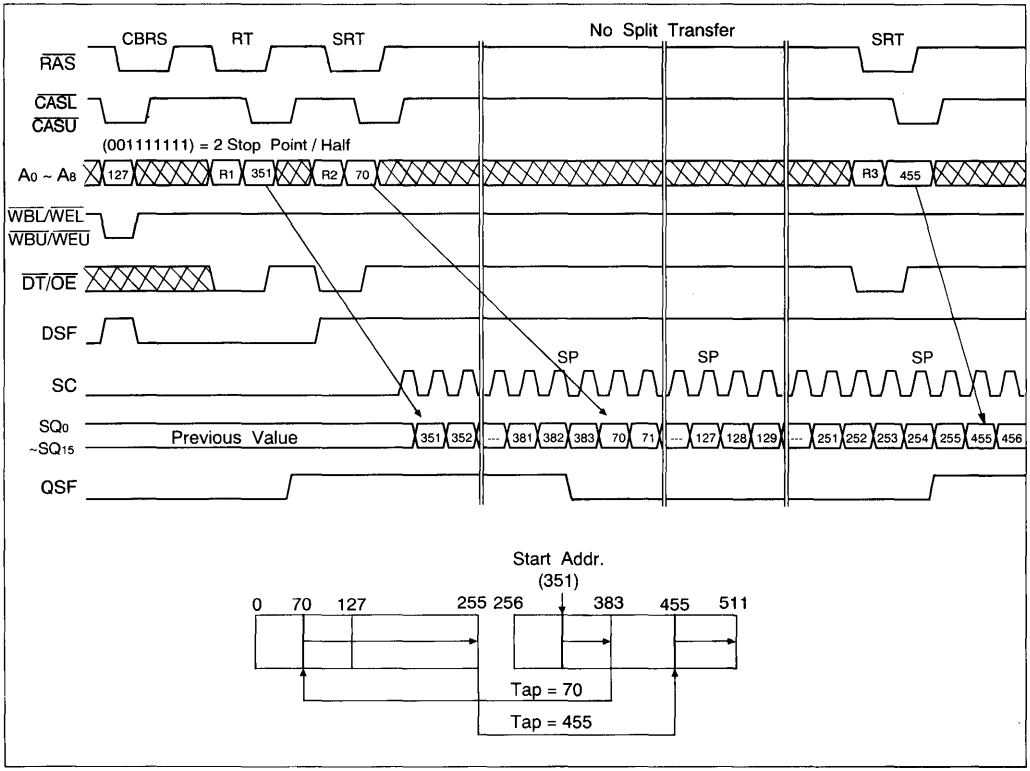
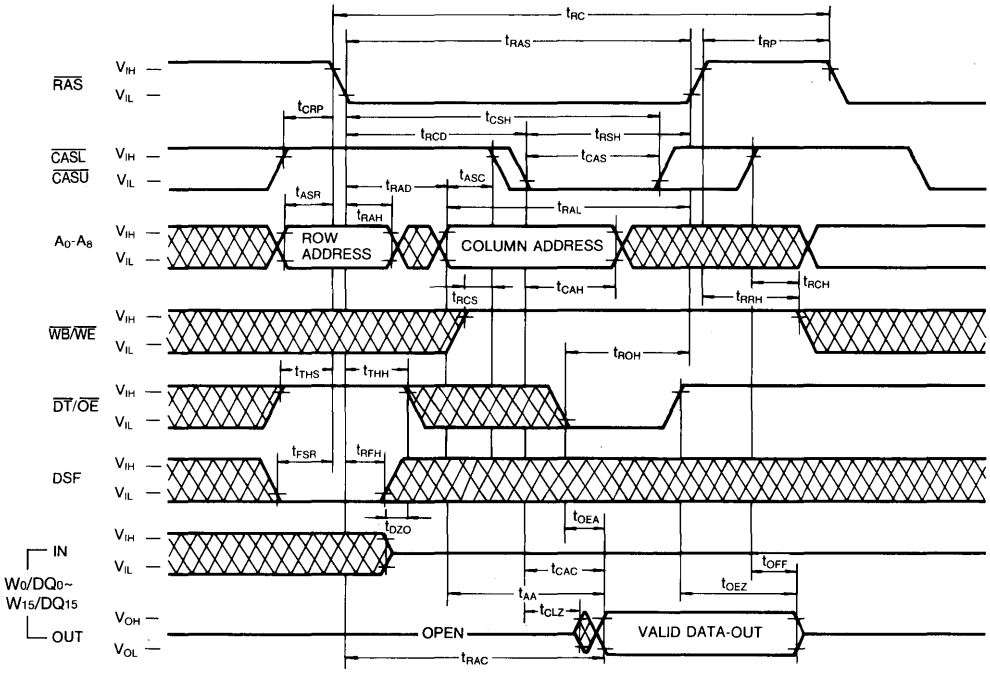


Figure 11. Programmable Split SAM operation

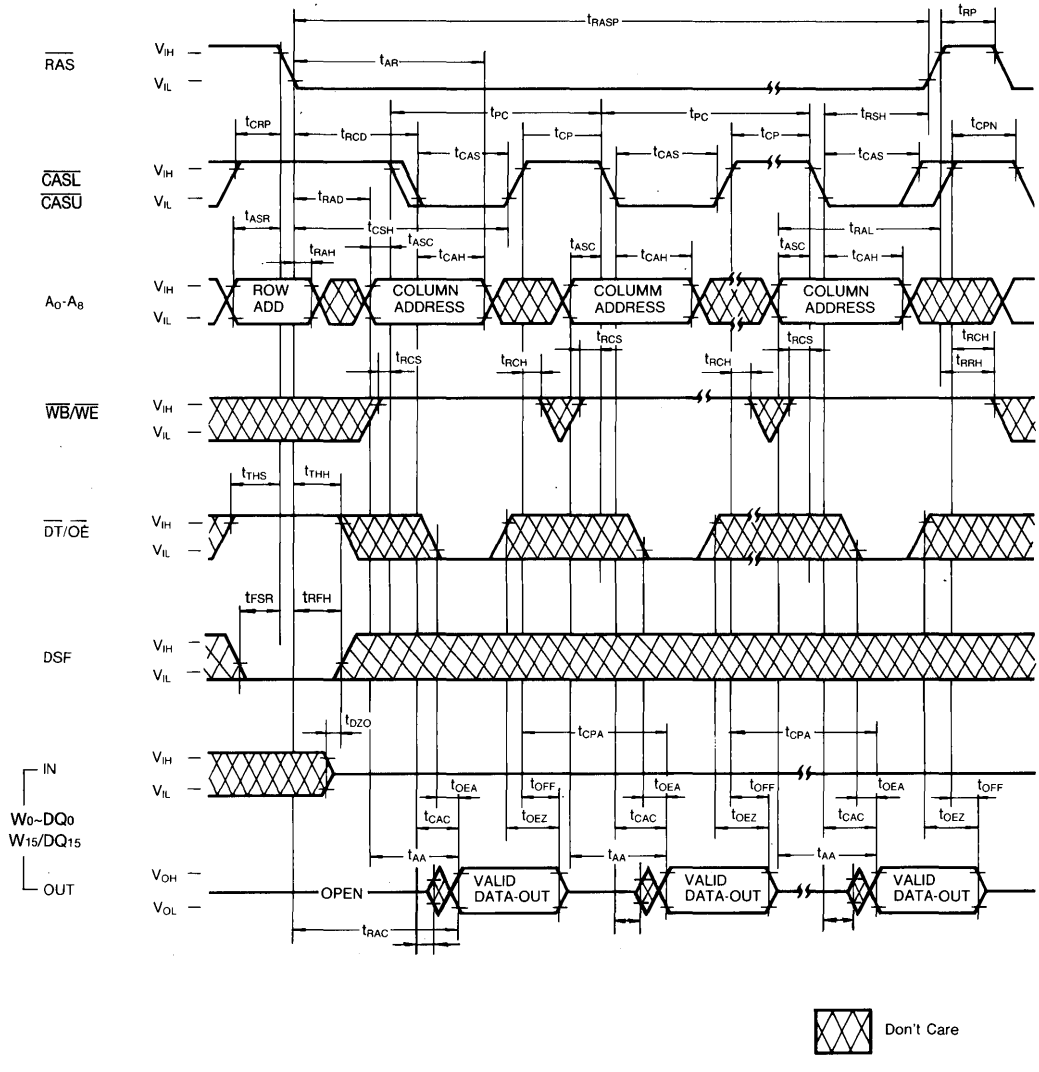
TIMING DIAGRAMS

READ CYCLE



Don't Care

FAST PAGE MODE READ CYCLE



Truth Table for Write Cycle(1)

FUNCTION	RAS			CAS	CAS↘ or WBL(U)/WEL(U)
	*1 WB/WE	*2 DSF	*3 Wi/DQi (3) (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask) (4)	1	0	×	1	Column Mask
Masked Block Write (4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register (2)	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram on the following pages
(2) Old Mask data load
(3) Function table for Old Mask and New Mask

IF		*1 WB/WE	*3 Wi/DQi	Note
LMR Cycle Executed	Yes	0	×	Write using mask register data (Old Mask Data)
		1	×	Non Masked Write
	No	0	Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	×	Non Masked Write

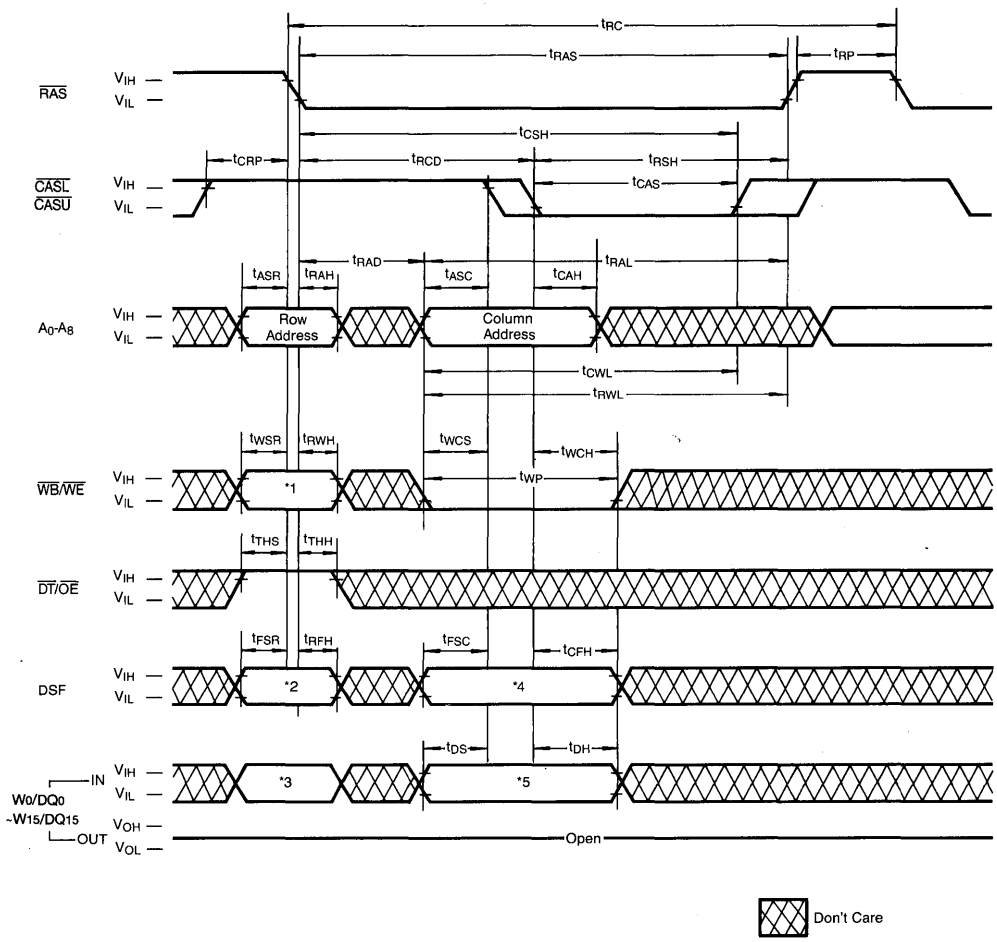
× : Don't Care

(4) Function Table for Block Write Column Mask

Column Address		
A2	A1	A0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

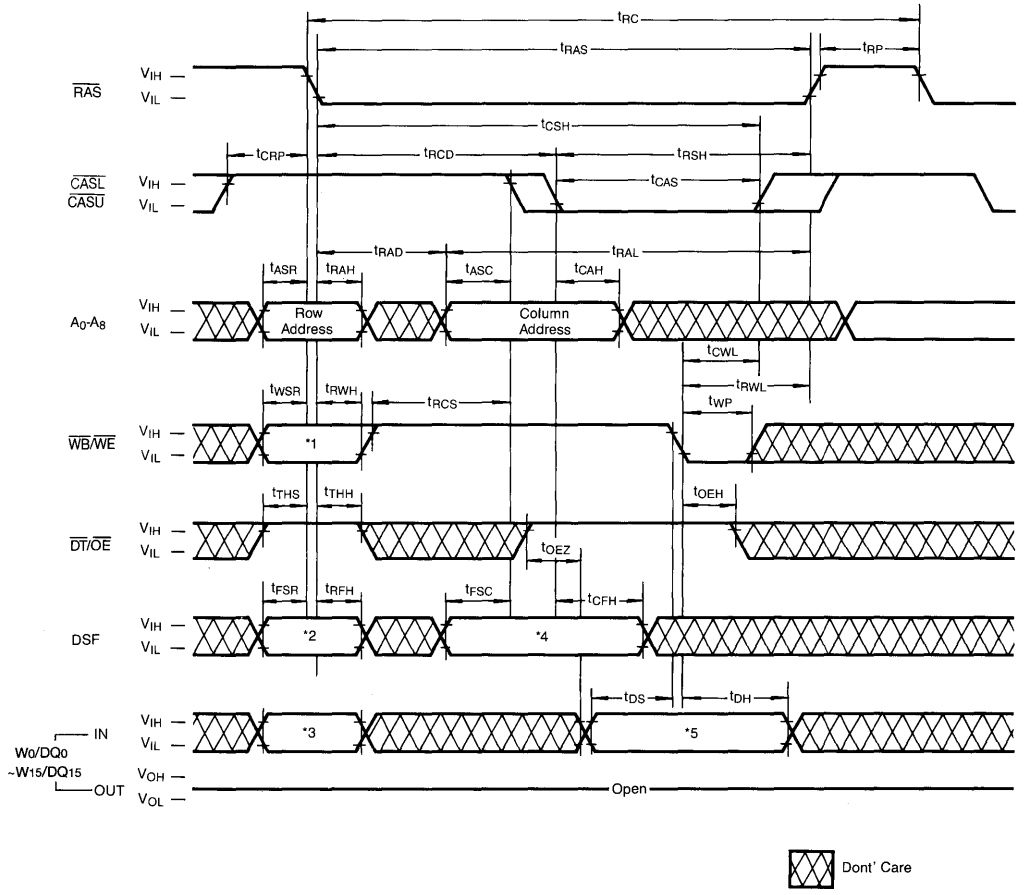
*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W_0/DQ_0	W_8/DQ_8	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
W_1/DQ_1	W_9/DQ_9		
W_2/DQ_2	W_{10}/DQ_{10}		
W_3/DQ_3	W_{11}/DQ_{11}		
W_4/DQ_4	W_{12}/DQ_{12}		
W_5/DQ_5	W_{13}/DQ_{13}		
W_6/DQ_6	W_{14}/DQ_{14}		
W_7/DQ_7	W_{15}/DQ_{15}		

EARLY WRITE CYCLE



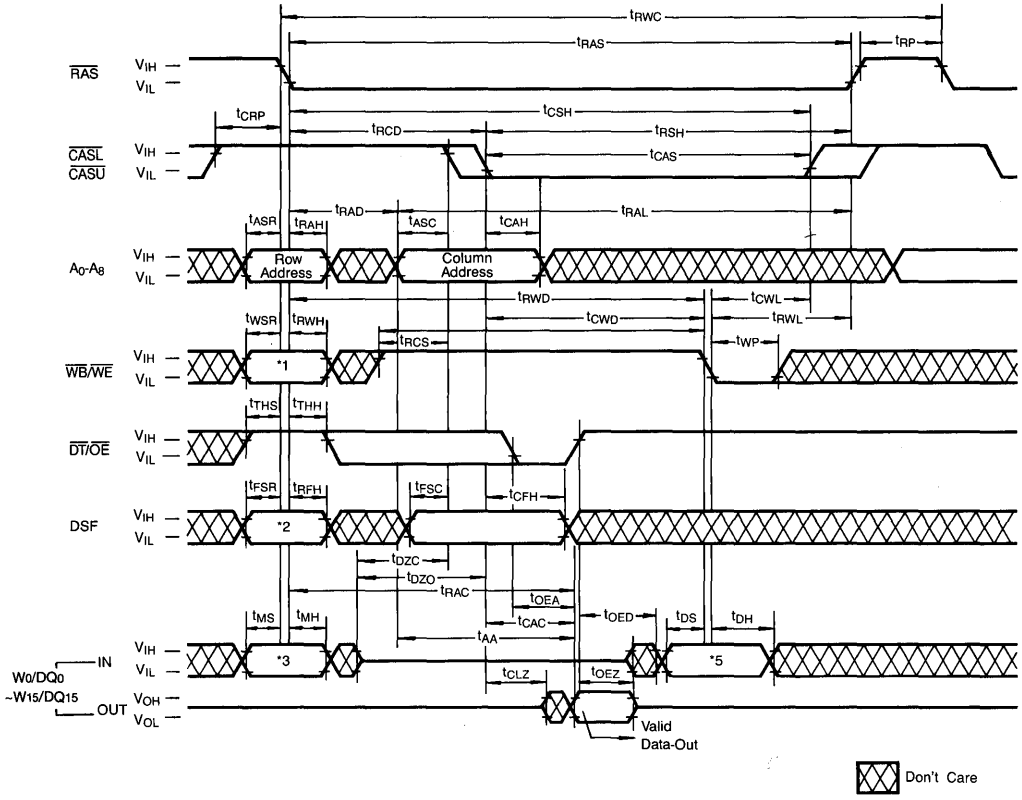
Note : In Block write cycle, only column address A3~A8 are used.

LATE WRITE CYCLE



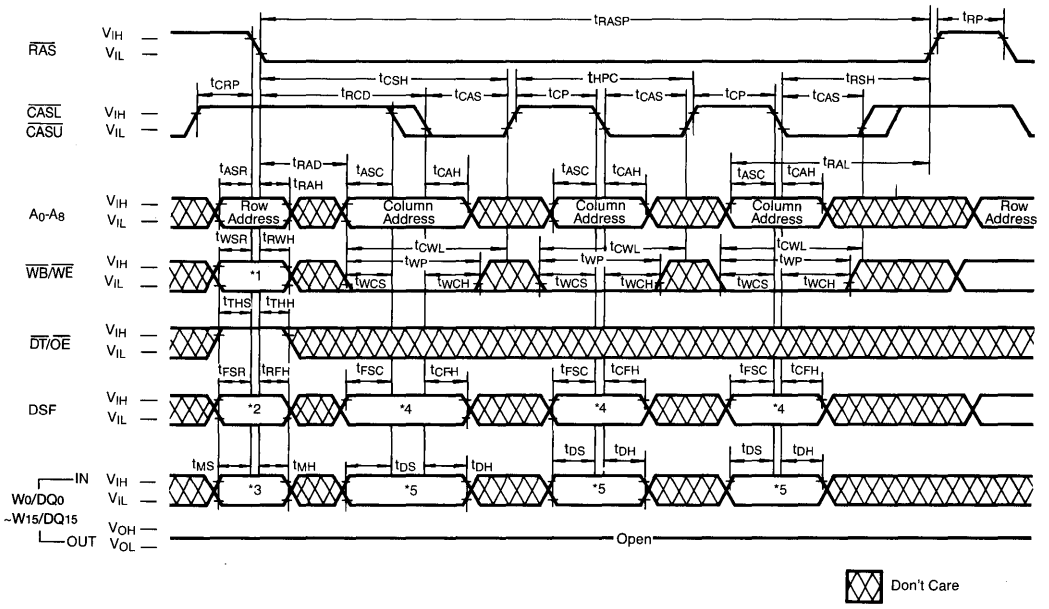
Note : In Block write cycle, only column address A3~A8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE



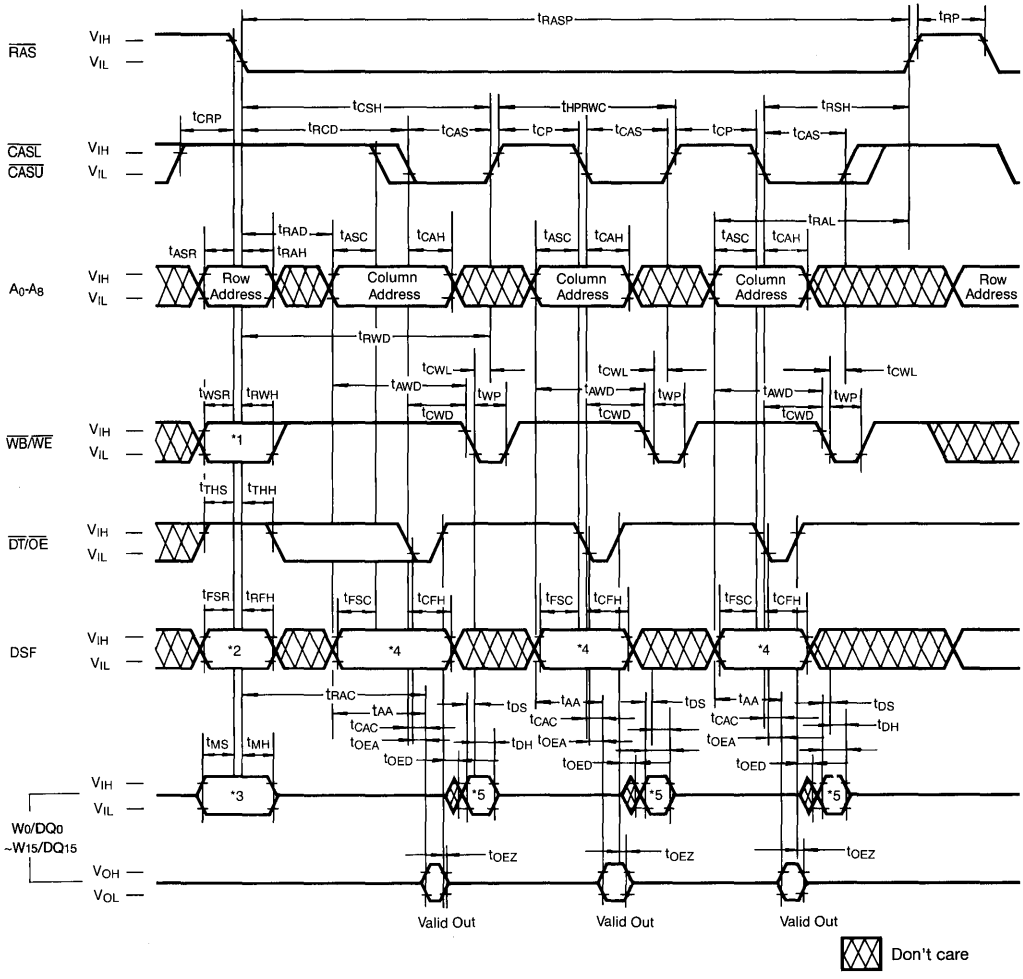
Note : In Block write cycle, only column address A3~A8 are used.

FAST PAGE MODE EARLY WRITE CYCLE



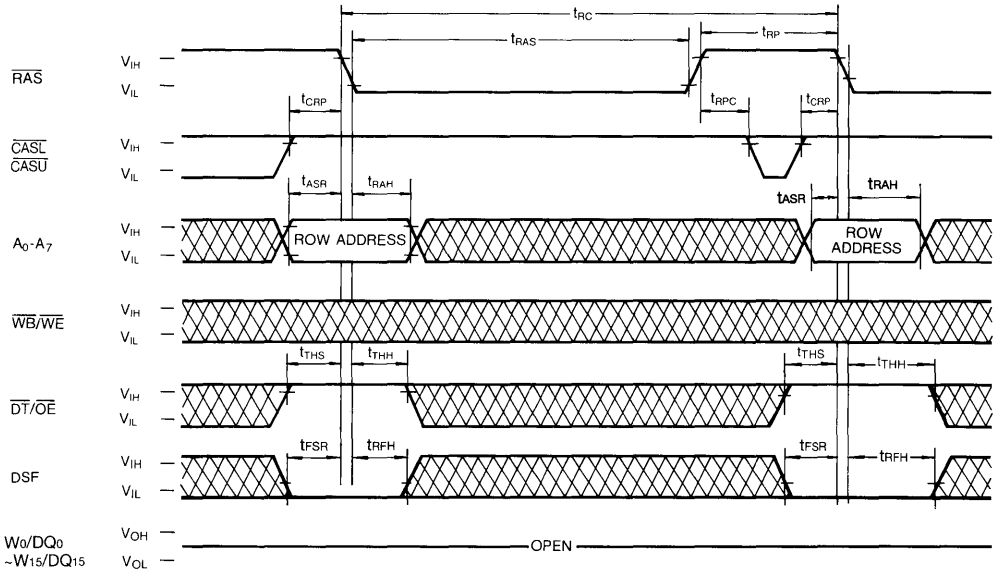
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



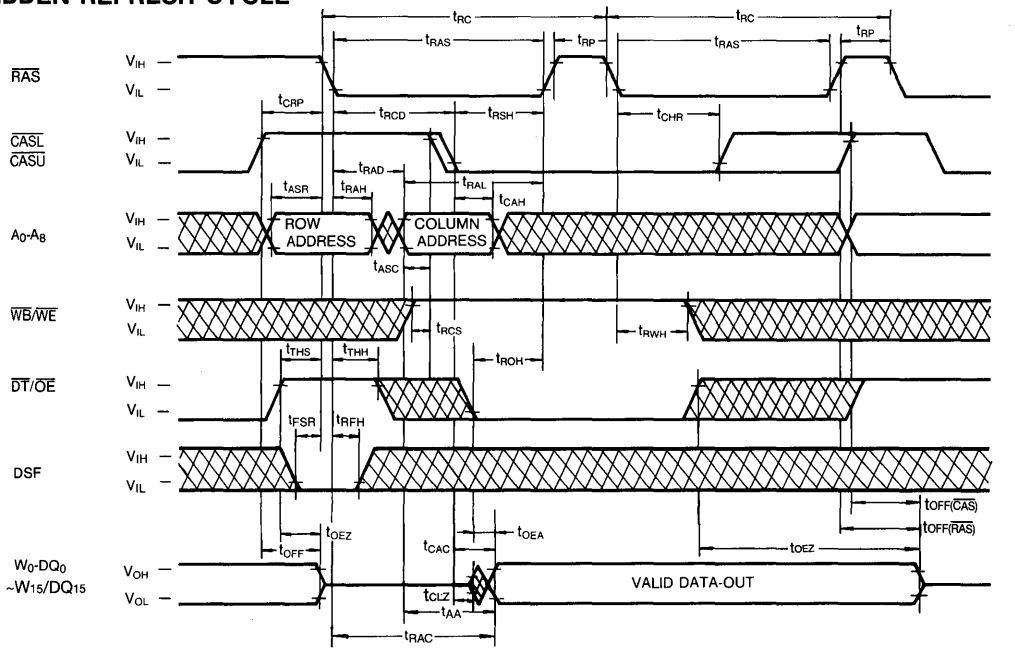
Note : In Block write cycle, only column address A3~A8 are used.

$\overline{RAS}$ ONLY REFRESH CYCLE

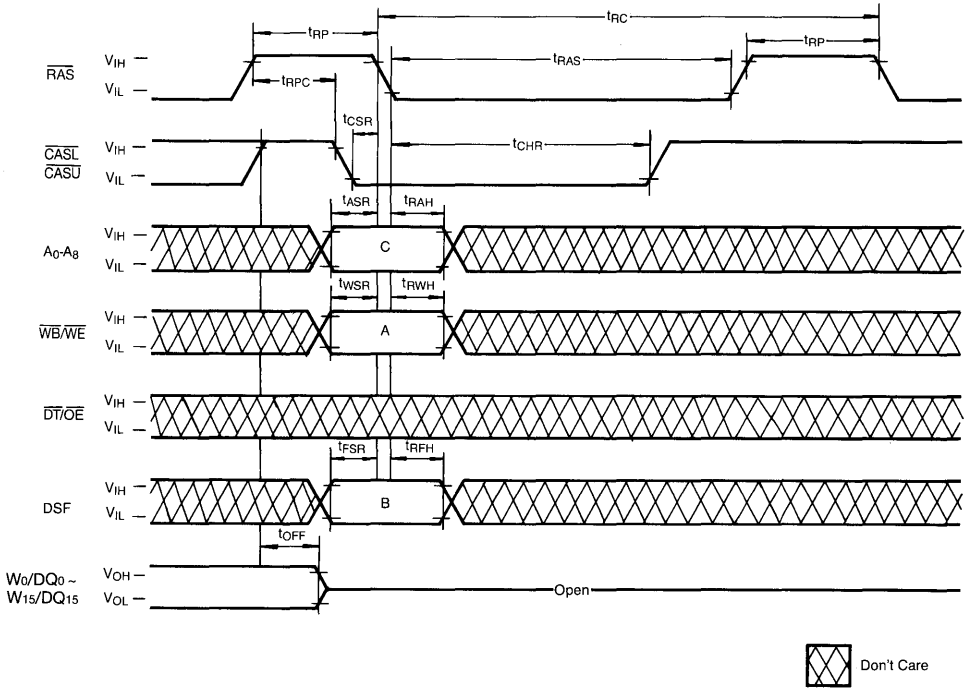


DON'T CARE

HIDDEN REFRESH CYCLE



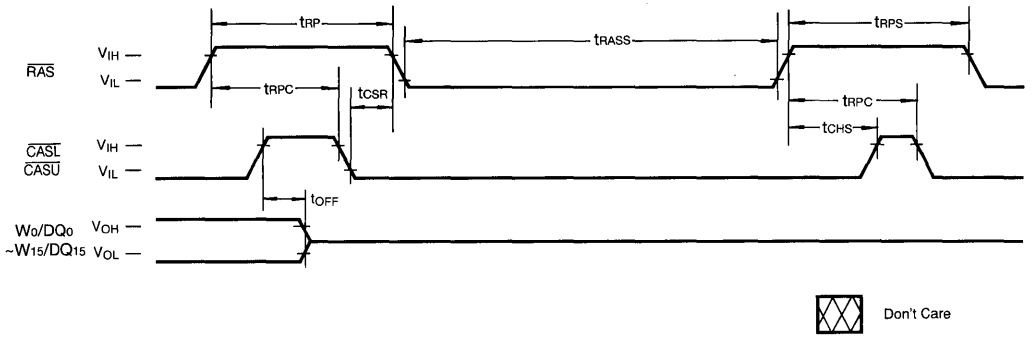
CAS BEFORE RAS REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE FUNCTION TABLE

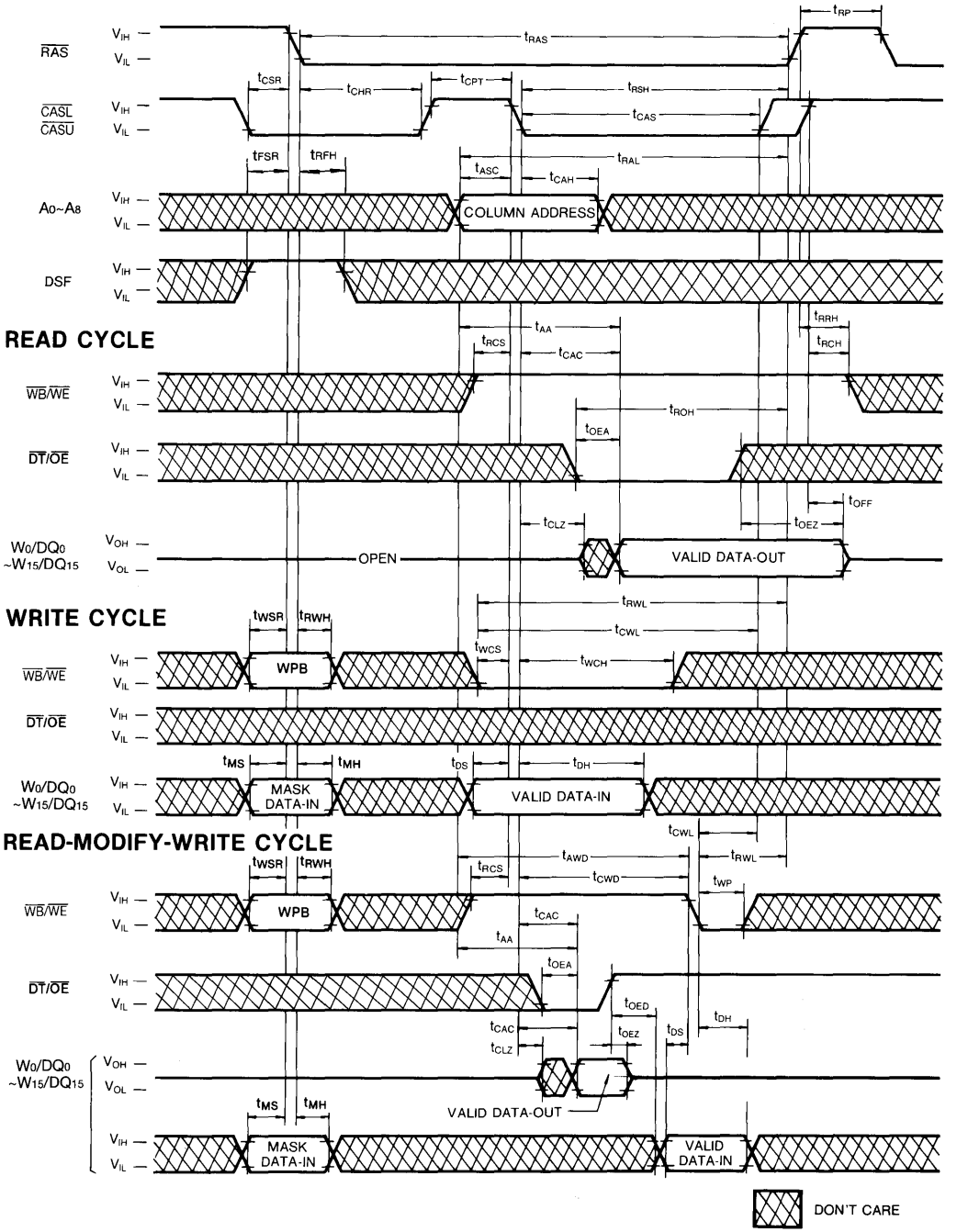
FUNCTION	CODE	LOGIC STATES		
		A	B	C
CAS-BEFORE-RAS REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
CAS-BEFORE-RAS REFRESH CYCLE (Stop Register Set)	CBRS	0	1	STOP Address
CAS-BEFORE-RAS REFRESH CYCLE (No Reset)	CBRN	1	1	X

CAS-BEFORE-RAS SELF REFRESH CYCLE

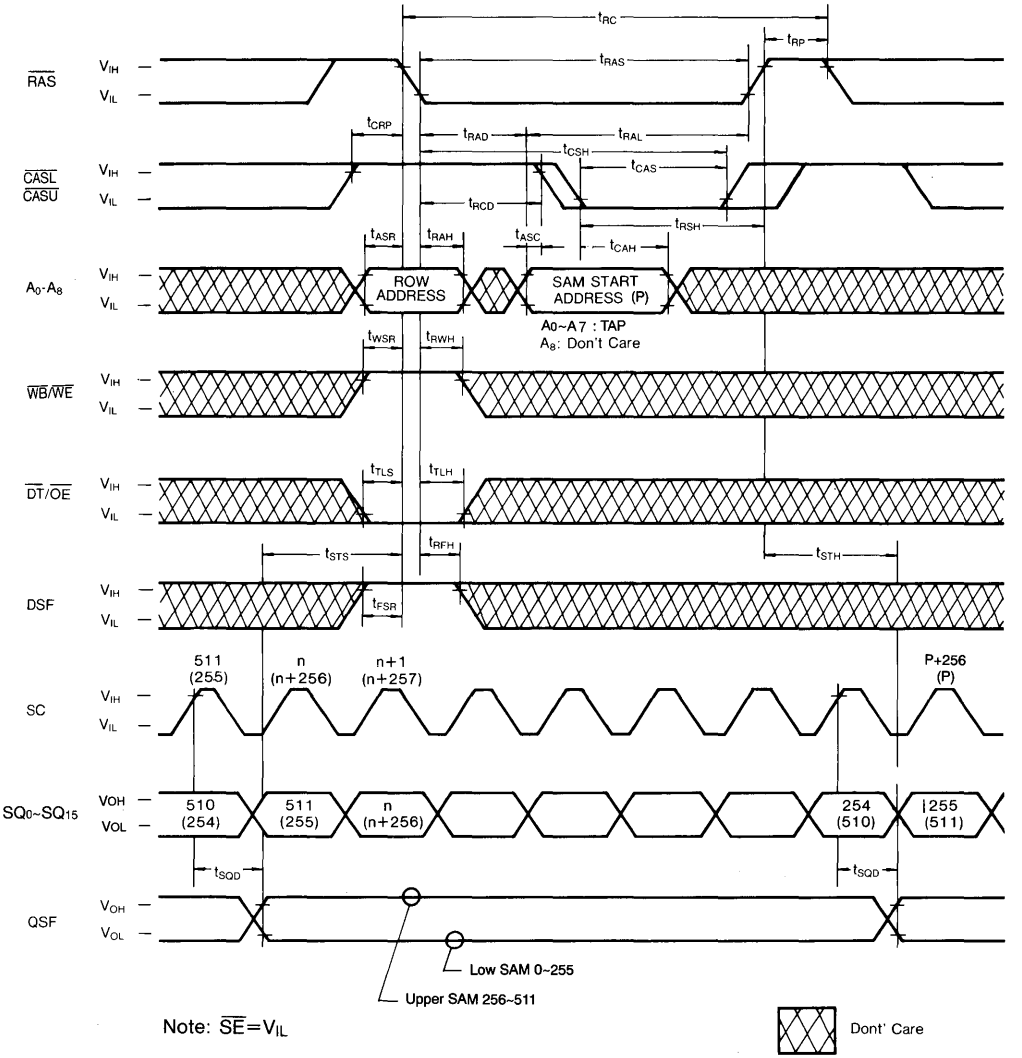


*CBR SELF REFRESH CYCLE IS APPLICABLE WITH CBRR, CBRS, OR CBRN CYCLE

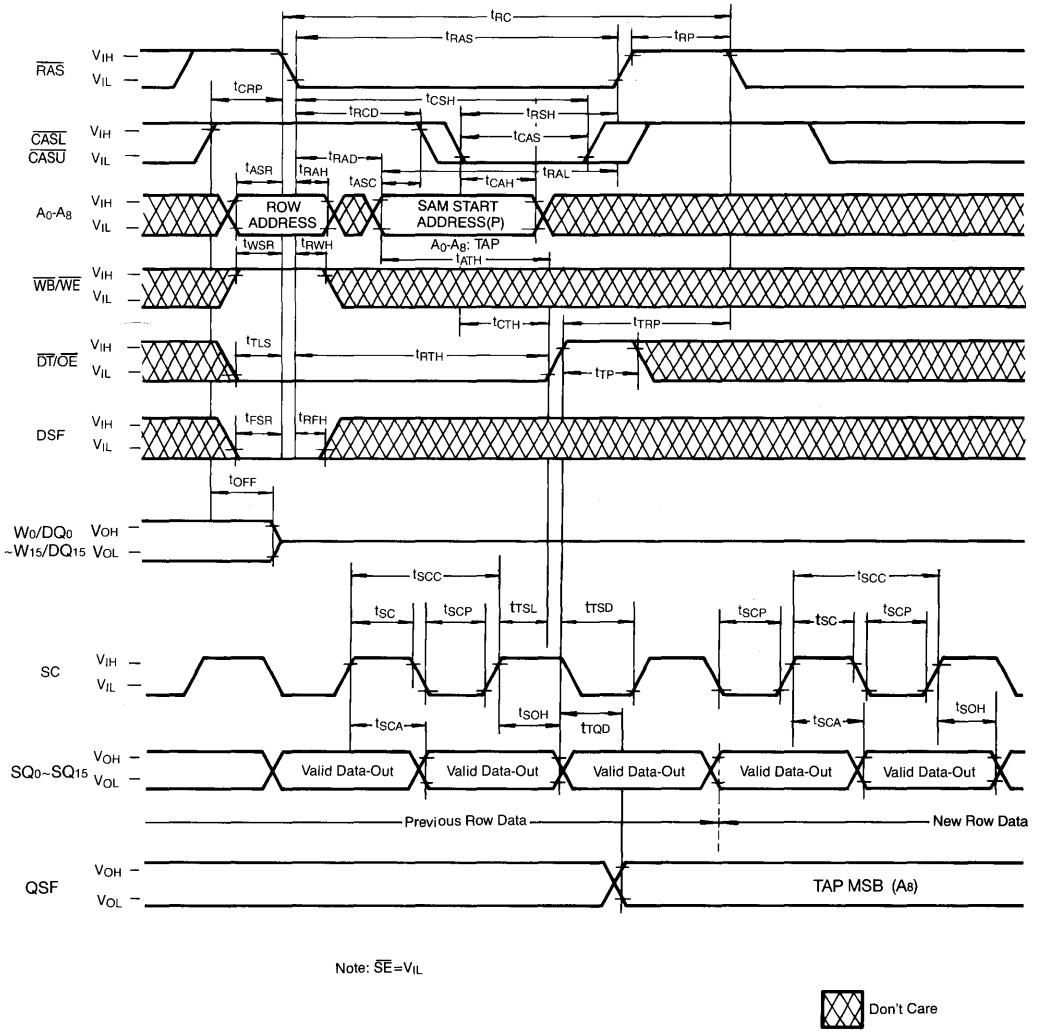
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SPLIT READ TRANSFER CYCLE



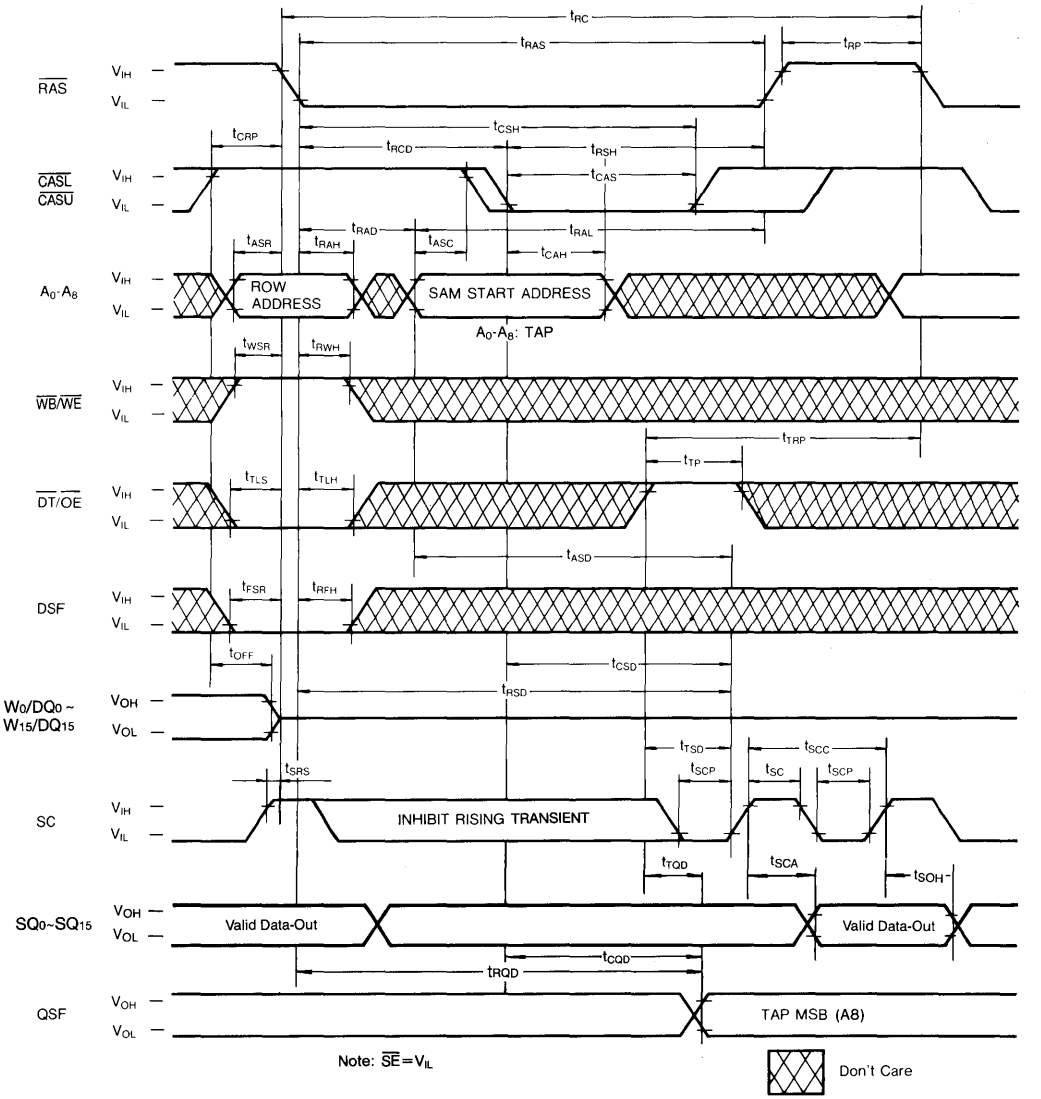
REAL TIME READ TRANSFER CYCLE



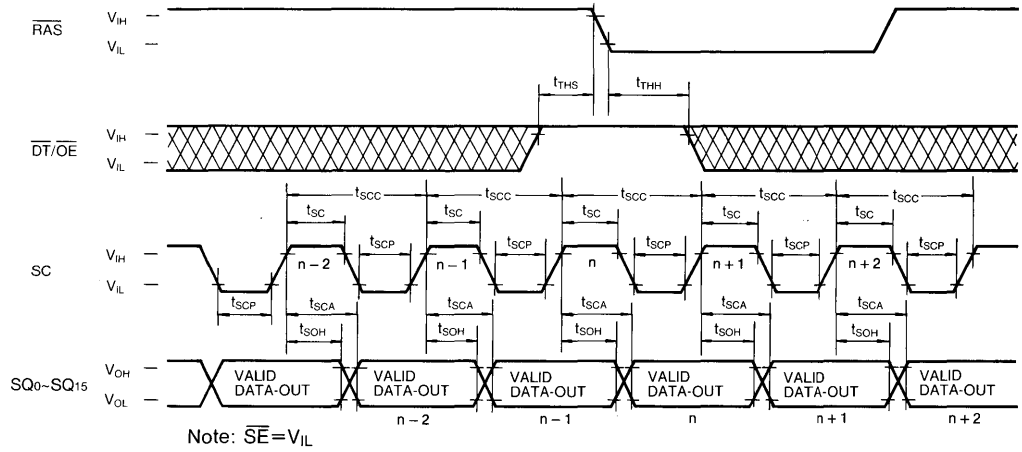
Note: $\overline{SE}$=V_{IL}

Don't Care

READ TRANSFER CYCLE

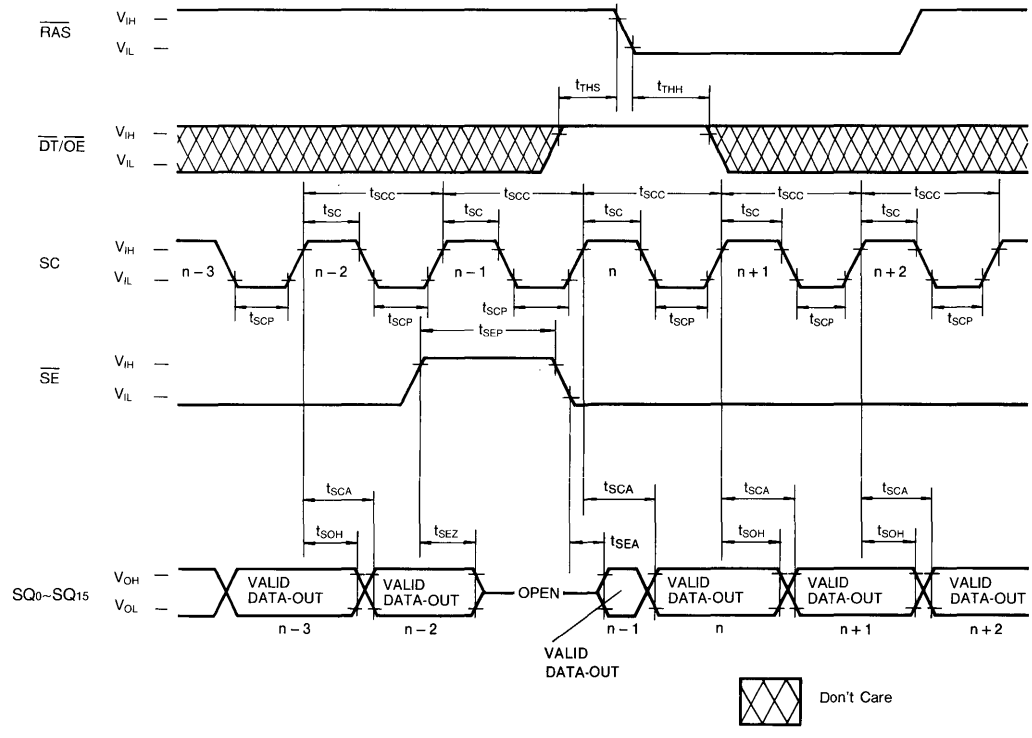


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$=V_{IL}

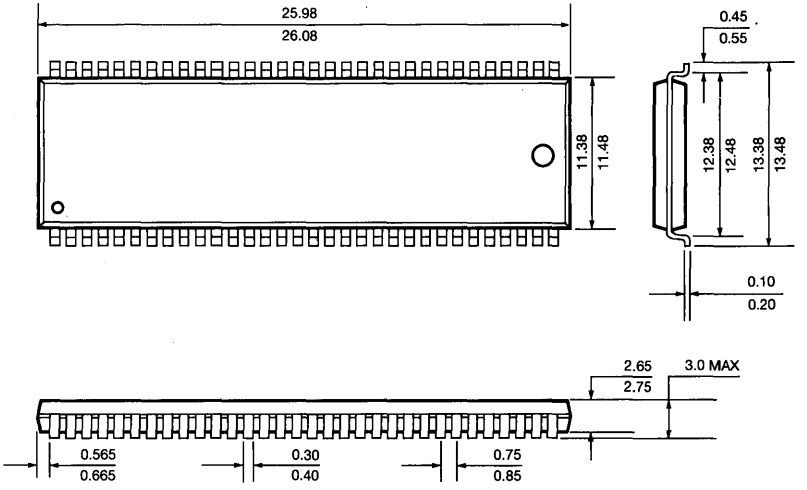
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



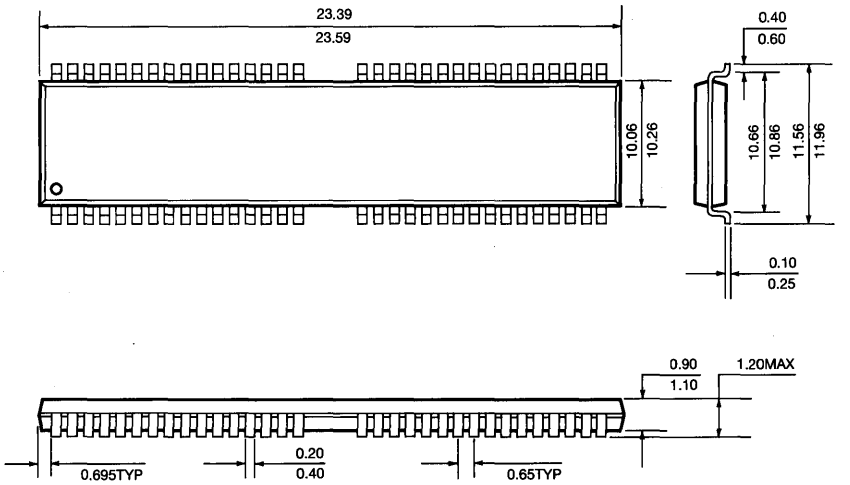
PACKAGE DIMENSIONS

Units: Millimeters

64 Pin Plastic Shrink Small Out Line Package



70(64) Pin Plastic Thin Small Out Line Package (Type II Forward)



256K × 16 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K × 16 bits RAM port
  512 × 16 bits SAM port
- **Performance range:**

Parameter \ Speed		-60	-70	-80
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{HPC})	KM4216C258	24ns	28ns	33ns
	KM4216V258	24ns	28ns	33ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C258	120mA	110mA	100mA
	KM4216V258	110mA	100mA	90mA
SAM active current	KM4216C258	50mA	45mA	40mA
	KM4216V258	40mA	35mA	30mA

- **Fast Page Mode with Extended Data out**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **2 $\overline{CAS}$ Byte/Word Read/Write Operation**
- **8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single + 5V±10% Supply Voltage (KM4216C258)**
- **Single + 3.3V±10% Supply Voltage (KM4216V258)**
- **Plastic 64-Pin 525 mil SSOP (0.8mm pin pitch)**
- **Plastic 70-pin 400mil TSOP II(0.65mm pin pitch) (Forward and Reverse Type)**

• Device Options	• Part Marking
-. Low Power Dissipation Extended CBR Refresh (64ms)	L
-. Low Low Power Dissipation Self Refresh (128ms)	F

- **Low Vcc(3.3V) Part Name: KM4216V258**

GENERAL DESCRIPTION

The Samsung KM4216C/V258 is a CMOS 256K × 16 bit Dual Port DRAM. It consists of a 256K × 16 dynamic random access memory (RAM) port and 512 × 16 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K × 16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, 2 $\overline{CAS}$ Byte/word Read/write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM ports using read, and programmable (Stop Register) Split Transfers.

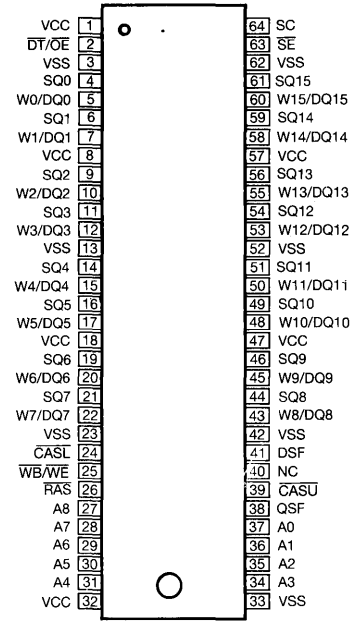
Refresh is accomplished by familiar DRAM refresh modes. The KM4216C/V258 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

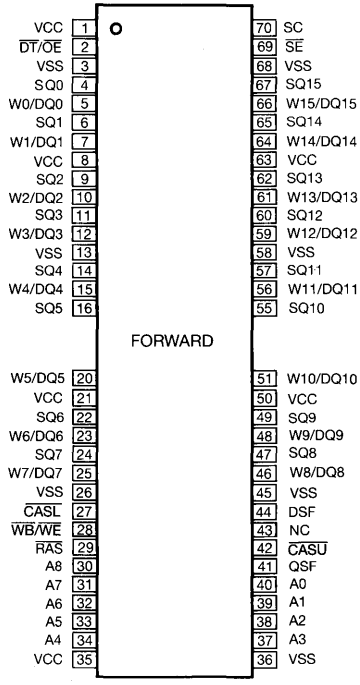
Pin Name		Pin Function
SC		Serial Clock
SQ_0-SQ_{15}		Serial Data Output
$\overline{DT}/\overline{OE}$		Data Transfer/Output Enable
$\overline{CASL}$, $\overline{CASU}$		Column Address Strobe (Lower /Upper)
$\overline{RAS}$		Row Address Strobe
$\overline{WB}/\overline{WE}$		Write Per Bit/Write Enable
W_0/DQ_0-W_{15}/DQ_{15}		Data Write Mask/Input/Output
$\overline{SE}$		Serial Enable
A_0-A_8		Address Inputs
DSF		Special Function Control
V_{CC}	KM4216C258	Power (+5V)
	KM4216V258	Power (+3.3V)
V_{SS}		Ground
QSF		Special Flag Out
N.C		No Connection

PIN CONFIGURATION (TOP VIEWS)

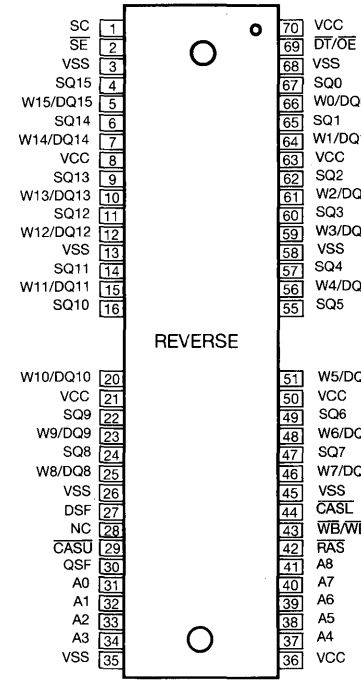
• **KM4216C/V258G/GL/GF**



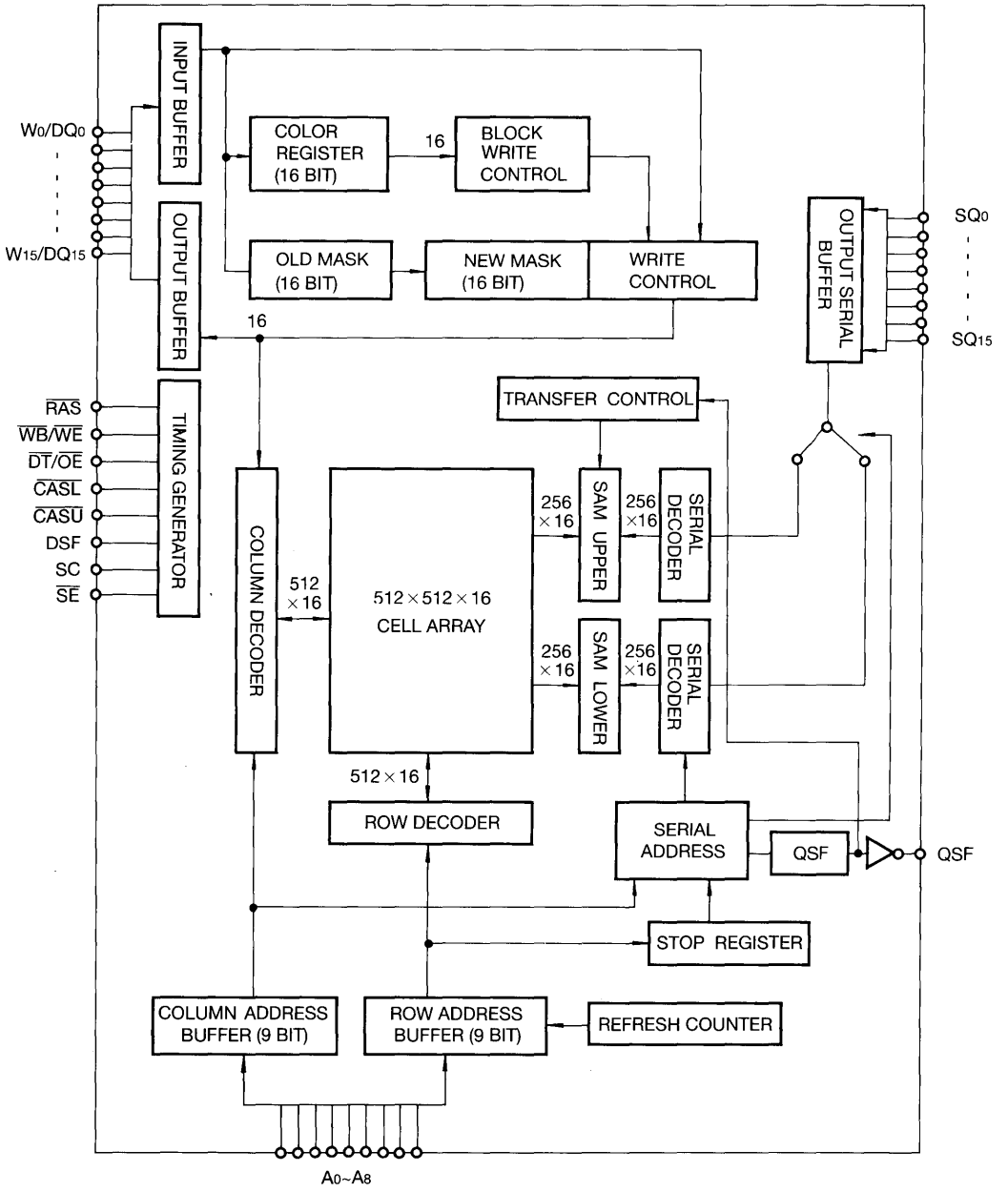
• **KM4216C/V258T/TL/TF**



• **KM4216C/V258R/RL/RF**



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic	RAS ↓				CAS ↓	Address		DQi Input		Register		Function
Code	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1.3)	0	×	0	1	-	Stop (Note4)	-	×	-	-	-	CBR Refresh/ Stop (No reset)
CBRN (Note 1)	0	×	1	1	-	×	-	×	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	×	×	0	-	×	-	×	-	-	-	CBR Refresh (Option reset)
ROR	1	1	×	0	-	ROW	-	×	-	-	-	RAS-only Refresh
RT	1	0	1	0	×	ROW	Tap	×	×	-	-	Read Transfer
SRT	1	0	1	1	×	ROW	Tap	×	×	-	-	Split Read Transfer
RWM	1	1	0	0	0	ROW	Col.	WMi	Data	Use	-	Masked write (New/Old Mask)
BWM	1	1	0	0	1	ROW	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New/Old Mask)
RW	1	1	1	0	0 (Note6)	ROW	Col.	×	Data	-	-	Read or Write
BW	1	1	1	0	1	ROW	Col.	×	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	ROW (Note7)	×	×	WMi	Load (Note5)	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	ROW (Note7)	×	×	Color		Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap:SAM Start (Column) Address, WMi : Write Mask Data (i=0~15)
$\overline{RAS}$ only refresh does not reset Stop or LMR functions.

Notes:
(1) CBRS, CBRN and CBRR all perform $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, CBRS or CBRN to perform $\overline{CAS}$-before-$\overline{RAS}$ refresh while using Old mask)
(3) After CBRS Cycle, SRT use STOP Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The ROW that is addressed will be refreshed, but a ROW address is not reguired.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C258	KM4216V258	
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to + 150	55 to +150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	KM4216C258			KM4216V258			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$+0.5(0.3*1) all other pins not under test=0 volts).	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V258

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless other wise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C258			KM4216V258			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1	Standby*4	I_{CC1}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)	Active	I_{CC1A}	160	145	130	140	125	110	mA
Standby Current	Standby*4	I_{CC2}	10	10	10	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$=V_{IH}	Active	I_{CC2A}	50	45	40	40	35	30	mA
DSF=V_{IL})	Standby*4	I_{CC2C}*2	200	200	200	200	200	200	μA
	Standby*4	I_{CC2C}*3	150	150	150	150	150	150	μA
$\overline{RAS}$ Only Refresh Current*1	Sandby*4	I_{CC3}	120	110	100	110	100	90	mA
($\overline{CAS}$-V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min	Active	I_{CC3A}	160	145	130	140	125	110	mA
Extended Fast Page Mode Current*1	Standby*4	I_{CC4}	110	100	90	100	90	80	mA
($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cyclinq @t_{PC}=min	Active	I_{CC4A}	150	135	120	130	115	110	mA
$\overline{CAS}$ Before-$\overline{RAS}$ Refresh Current*1	Standby*4	I_{CC5}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min	Active	I_{CC5A}	160	145	130	140	125	110	mA
Data Transfer Current *1	Standby*4	I_{CC6}	140	130	120	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC6A}	180	165	150	160	145	130	mA
Block Write Cycle Current *1	Standby*4	I_{CC7}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC7A}	160	145	130	140	125	110	mA
Color Register Load Current *1	Standby*4	I_{CC8}	110	90	80	90	80	70	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC8A}	140	125	110	120	105	90	mA
Battery Back Up Current *2 $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycling or $\leq V_{IL}$ $\overline{RAS}$=t_{RAS}(min) to 1μs t_{RC}=125 μs (64ms for 512 rows) $\overline{DT/OE}$, $\overline{WB/WE}$, DSF$\geq V_{IH}$ or$\leq V_{IL}$	Standby*4	I_{CC9}	300	300	300	300	300	300	μA
Self Refresh Current *3 $\overline{RAS}$,$\overline{CAS}$$\leq$0.2V(128ms for 512 rows) $\overline{DT/OE}$, $\overline{WB/WE}$, A_0~A_8, DSF$\geq V_{CC}$ - 0.2v or$\leq$0.2V DQ0~15=V_{CC}-0.2V, 0.2V or OPEN	Standby*4	I_{CC10}	250	250	250	250	250	250	μA

Note *1 Real values dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, adress transition should be changed only once while $\overline{RAS}$=V_{IL}.

In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$=V_{IH}

*2 KM4216C258L only : $V_{IH}\geq V_{CC}$-0.2V, $V_{IL}\leq$0.2V

*3 KM4216C258F only : $V_{IH}\geq V_{CC}$ -0.2V, $V_{IL}\leq$0.2V

*4 SAM standby condition : $\overline{SE}\geq V_{IH}$, SC$\leq V_{IL}$ or $\geq V_{IH}$

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM4216C258 : V_{CC}=5.0V±10%, KM4216V258 : 3.3V±10%,)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		200		ns	
Hyper page cycle time	t_{HPC}	30		35		40		ns	17
		24		28		33		ns	16
Hyper paage read-modify-write cycle time	t_{HPRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,6
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		5		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time(rise and fall)	t_T	2	50	3	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (Hyper page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		70		65		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	15	10K	20	10K	ns	17
		10		10		12		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		10		30		ns	
$\overline{CAS}$ precharge time (Hyper page mode)	t_{CP}	15		10		10		ns	17
Output hold time from $\overline{CAS}$	t_{DOH}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	16
Column address hold time	t_{CAH}	10		12		15		ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Output buffer turn off delay from $\overline{WB}$/$\overline{WE}$	t_{WEZ}	0	15	0	15	0	15	ns	7
Write command pulse width	t_{WPZ}	10		10		10		ns	7
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	19
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		12		15		ns	10
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		45		45		ns	8,18
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	tAWD	50		55		60		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	tCSR	10		10		10		ns	20
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tCHR	10		10		10		ns	21
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output Buffer turn-off delay from $\overline{OE}$	tOEZ	0	15	0	15	0	15	ns	7
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	tRFH	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	10		10		15		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	0		0		0		ns	15
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (real time read transfer)	tCTH	15		20		25		ns	

AC CHARACTERISTICS (Continued)

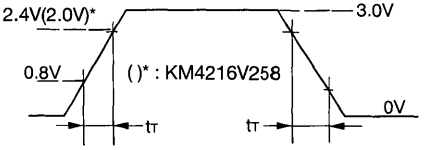
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{DT}$ low hold referenced to column address (real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay (read transfer)	t_{CSD}	25		30		35		ns	
Col. Address to first SC delay (read transfer)	t_{ASD}	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	t_{TSD}	10		10		15		ns	
LAST SC to $\overline{RAS}$ set-up time	t_{SRS}	20		20		20		ns	
SC cycle time	t_{SCC}	18		20		25		ns	14
SC pulse width (SC high time)	t_{SC}	5		7		7		ns	
SC precharge (SC low time)	t_{SCP}	5		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	
SC-QSF delay time	t_{SQD}		20		25		25	ns	
$\overline{DT}$-QSF delay time	t_{TQD}		20		25		25	ns	
$\overline{RAS}$-QSF delay time	t_{RQD}		70		75		80	ns	
$\overline{CAS}$-QSF delay time	t_{CQD}		35		35		40	ns	
$\overline{DT}$ to $\overline{RAS}$ Prechange time	t_{TRP}	40		50		60		ns	
$\overline{OE}$ high pulse width	t_{OEP}	10		10		10		ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	10		10		10		ns	
$\overline{OE}$ to $\overline{CAS}$ High set-up time	t_{OCH}	5		5		5		ns	

NOTES

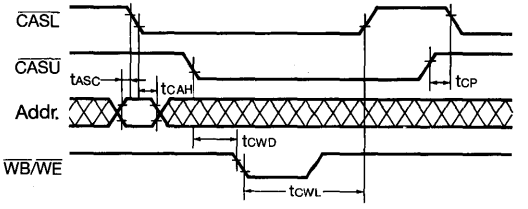
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ 8 SC cycles before proper device operation is achieved.($\overline{DT}/\overline{OE}$=High) if the intenal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required in stead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input siganl transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1TTL load and 50pF.
   D_{OUT} Comparator level : V_{OH}/V_{OL}=2.0V/0.8V.
4. SAM port outputs are measured with a load equivalent to 1TTL load and 30pF.
   D_{OUT} comparator level:V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the first $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below

Pin or REGISTER	STATUS
QSF	Hi-Z
Color Registe	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SDQi	Hi-Z

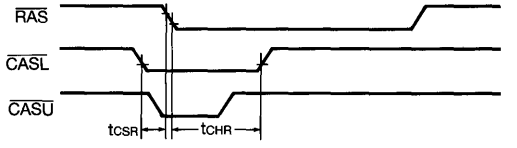
13. Recommended operating input condition.



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=5.0ns
14. Assume t_T=3ns.
15. Self refresh parameter (KM4216C/V258F)
    512K cycle of burst refresh must be executed within 8ms before and after self-refresh in order to meet refresh specification.
16. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
17. t_{CP} is specified from the last $\overline{CAS}$ rising edge in tne previous cycle to the first $\overline{CAS}$ falling edge in the next cycle
18. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
19. t_{CWL} is specified from $\overline{WB}/\overline{WE}$ faliing edge to the earlier $\overline{CAS}$ rising edge.



20. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
21. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



DEVICE OPERATION

The KM4216C/V258 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V258 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe($\overline{CAS}$) and the valid row and coumn address inputs.

Operation of the KM4216C/V258 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This the beginning of any KM4216C/V258 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V258 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$,$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.
If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then tne access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}
The KM4216C/V258 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM Read cycle, D_{OUT} buffer is designed to make turn-off by the rising edge fo $\overline{CAS}$. The KM4216C/V258 offers an accelerated Fast Page Mode Cycle by eliminating output disable from $\overline{CAS}$ high.
This is called Extended Data Output (or Hyper Page mode)
Data output are disabled at $\overline{WB}/\overline{WE}$=low, $\overline{DT}/\overline{OE}$=high and t_{OFF} time after $\overline{RAS}$ and $\overline{CAS}$ are high. The t_{OFF} time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs laters (See Figure 1). What the output buffer is disabling during $\overline{DT}/\overline{OE}$ = high is to use bank selection in the frame buffer memory using common I/O line. Read, write and read-modify-write cycles are available during the extended data out mode.

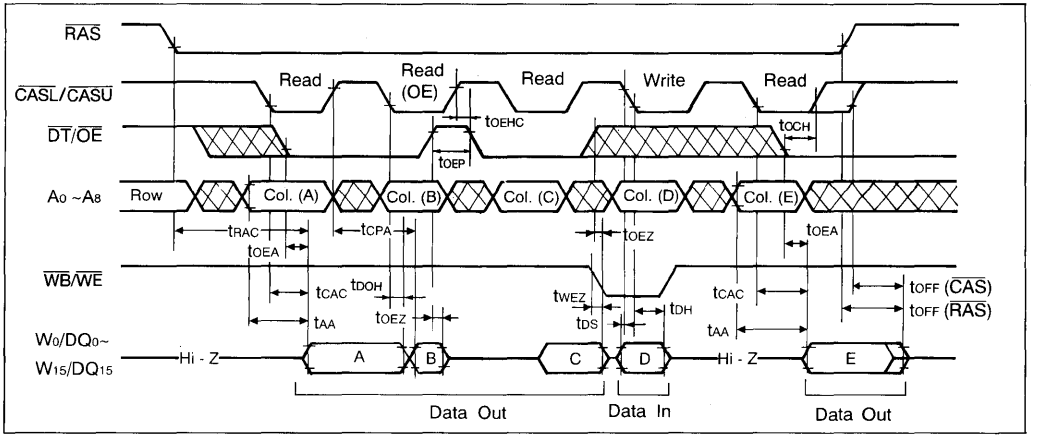


Figure 1. Extended Data Output Example

DEVICE OPERATION (continued)

2$\overline{CAS}$ Byte/Word Read/Write Operation

The KM4216C/V258 has 2 $\overline{CAS}$ control pin, $\overline{CASL}$ and $\overline{CASU}$, and offers asynchronous Read/Write operation with lower byte (W_0/DQ_0~W_7/DQ_7) and upper byte (W_8/DQ_8~W_{15}/DQ_{15}). This is called 2$\overline{CAS}$ Byte/Word Read/Write operation. This operation can be performed RAM Read in RAM write, Block write, Load Mask register, and Load Color register.

New Masked Write Per Bit

The New Masked Write Per Bit cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM.

The mask data is valid for only one cycle. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ low after $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

If $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed (see Figure2, 3). And If $\overline{CASL}$ is high during $\overline{WB}/\overline{WE}$ low, write operation of lower byte do not perform and if $\overline{CASU}$ is high, write operation of upper byte do not execute.

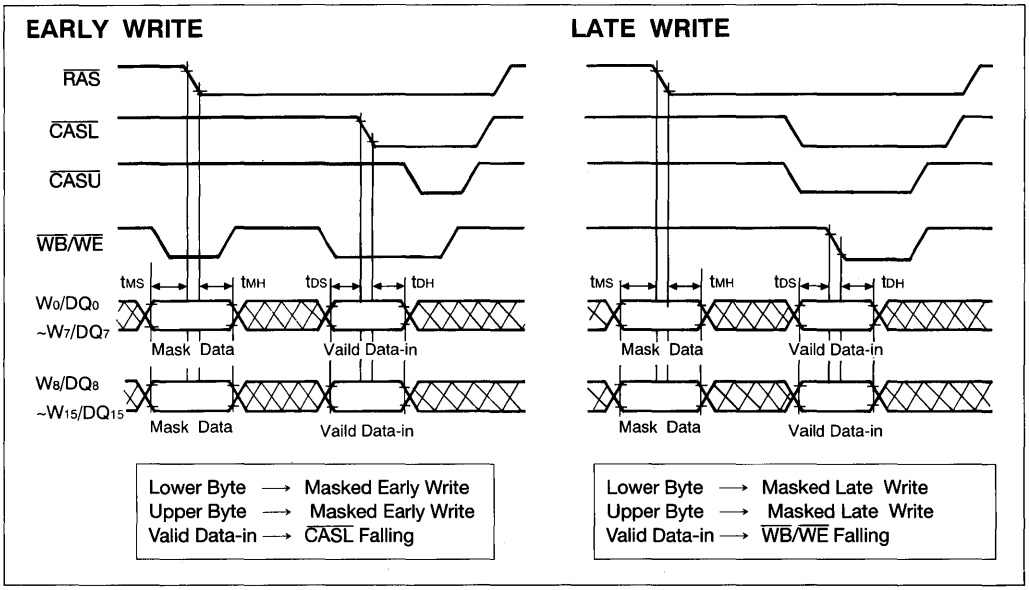


Figure 2. Byte Write and New Masked Write Cycle Example 1. (Early Write & Late Write)

DEVICE OPERATION (continued)

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

The LMR cycle is performed if DSF high, $\overline{WB}/\overline{WE}$ high at the $\overline{RAS}$ falling edge. And DSF low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM4216C/V258 are set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Registe (LMR) cycle. If an LMR is done, all Masked write are Old Masked Write Per Bit and the I/O mask data will be provided by the Mask Data Register (See Figure 4.)

The mask data is applied in the same manner as in New Masked write Per Bit mode.

Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After power-up, the KM4216C/V258 initializes in the New Masked write mode.

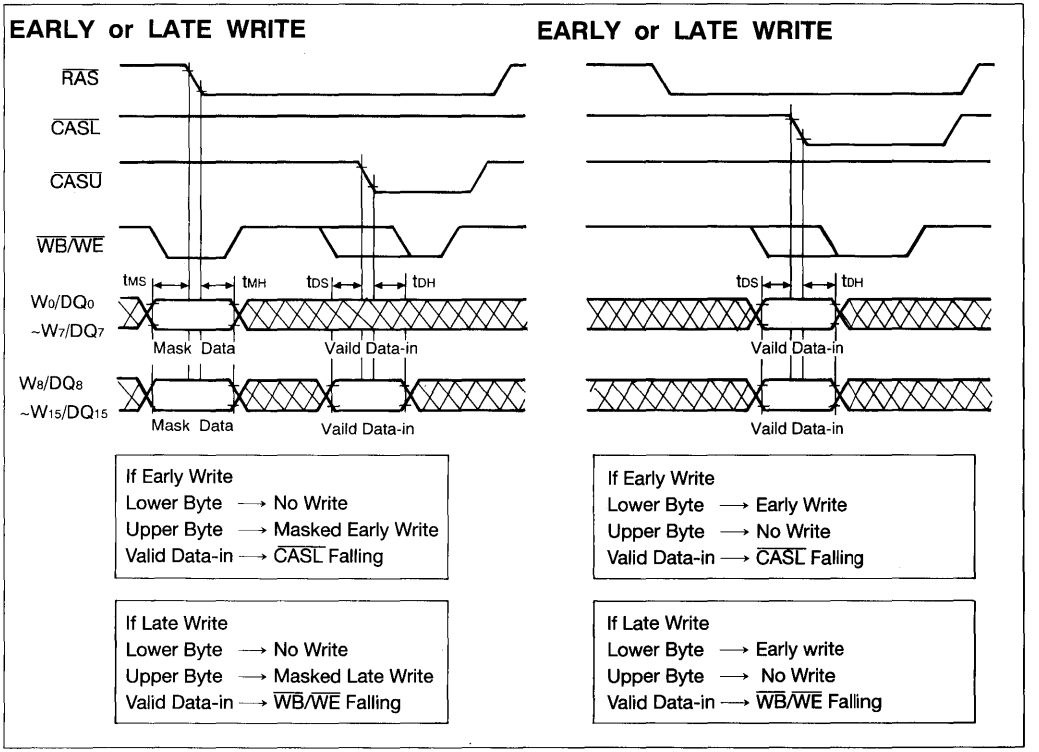


Figure 3. Byte Write and New Masked Write Cycle Example 2.

DEVICE OPERATION (continued)

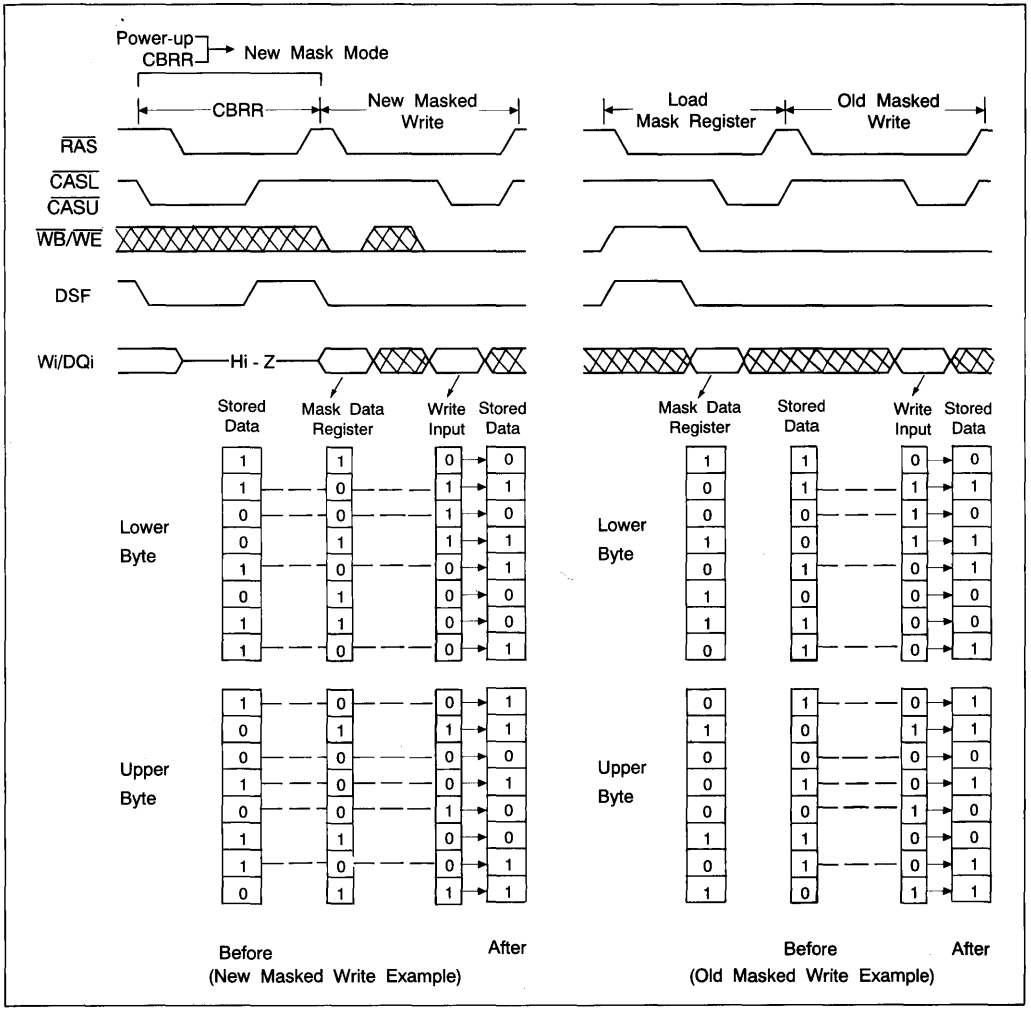


Figure 4. New Masked Write Cycle and Old Masked Write Cycle Example

Fast Page Mode

The KM4216C/V258 has Fast Page mode capability provides high speed read, write or read-modify-write access to all memory locations Within a selected row. In this cycle, read, write, read-modify write, and block write cycles can be mixed in any order.
In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

DEVICE OPERATION (continued)

Load Color Register(LCR)

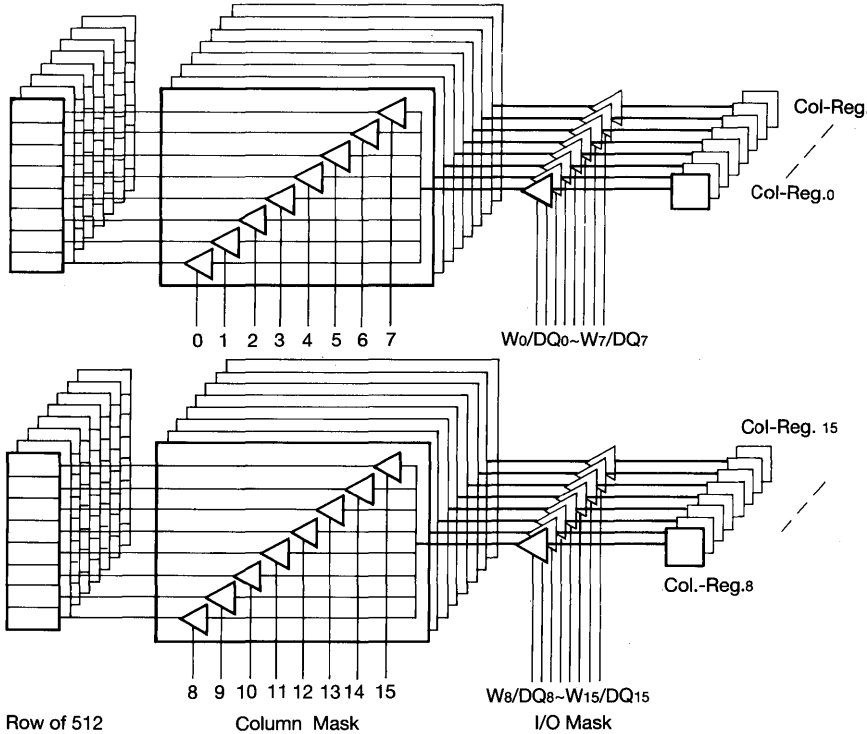
A Load Color register cycle is performed by keeping DSF high on the both falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded in the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(late write) via the W_0/DQ_0~W_7/DQ_7(Lower Byte), W_8/DQ_8~W_{15}/DQ_{15} (Upper Byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register Cycle.

Block Write

In a Block write cycle, 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each corresponding bit plane(16). This results in a total of 128-bits being written in a single Block write cycle compared to 16-bits in a normal write cycle.

The Block write cycle is performed if DSF is low at the falling edge of $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



	$\overline{RAS}$
W_0/DQ_0~7	Lower Block I/O Mask
W_8/DQ_8~15	Upper Block I/O Mask

	$\overline{CAS}$
A_0~A_2	Don't Care
W_0/DQ_0~7	Lower Block Column Select
W_8/DQ_8~15	Upper Block Column Select

A_2~A_0	Lower	Upper	Column Mask	
0 0 0	W_0/DQ_0	W_8/DQ_8	DQi=1	Column Enable
0 0 1	W_1/DQ_1	W_9/DQ_9		
0 1 0	W_2/DQ_2	W_{10}/DQ_{10}		
0 1 1	W_3/DQ_3	W_{11}/DQ_{11}		
1 0 0	W_4/DQ_4	W_{12}/DQ_{12}	DQi=0	Column Disable
1 0 1	W_5/DQ_5	W_{13}/DQ_{13}		
1 1 0	W_6/DQ_6	W_{14}/DQ_{14}		
1 1 1	W_7/DQ_7	W_{15}/DQ_{15}		

Figure 5. Block Write Scheme

DEVICE OPERATION (continued)

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.
Since 8 columns are being written at a time, the minimum increment required for the column address is latched on the falling edge of $\overline{CAS}$, the 3 LSBs, A_0, A_1, and A_2 are ignored and only bits (A_3~A_8) are used to define the location of the first bit out of the eight to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16 -bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the eight, but the second remains unchanged. Fig. 5 shows the correspondence of each data line to the column mask bits.
A Masked Block Write cycle is identical to a New/old Masked Write-Per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB/WE}$ must be low at the falling edge of $\overline{RAS}$. And DSF must be high on the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0~W_{15}/DQ_{15} pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. In Old mask mode, I/O mask data will be provided by the Mask Data Register.

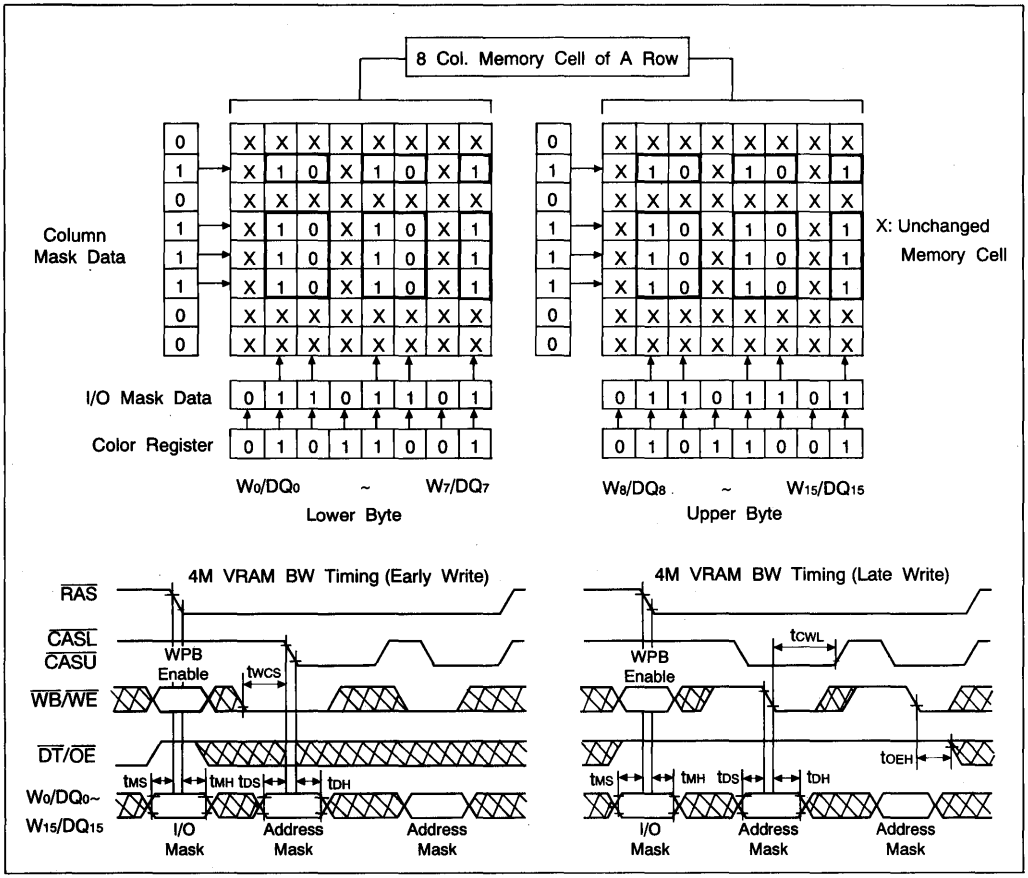


Figure 6. Block Write Example and Timing

DEVICE OPERATIONS (Continued)

Data Output

The KM4216C/V258 has three state output buffer Controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}$,$\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is in high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output duing the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V258 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM4216C/V258 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operatian occurs automatically. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
The KM4216C/V258 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation ; CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values.
CBRN (CBR refresh without reset) is set if DSF high when $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$ and simply do only refresh operation.
CRRS(CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WB}/\overline{WE}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V258 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Self Refresh *(Only KM4216C/V258F)* : The Self Refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for longer periods of standby, such as a battery back-up. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If $\overline{RAS}$ is low more than 100μs at the condition of CBR, Self Refresh function is accomplished. In this state, the external refresh address do not need to supply additionally on-chip because the refresh counter on-chip gives that addresses needed to refresh. Please note that the ending point of Self Refresh is when $\overline{RAS}$ and $\overline{CAS}$ is high and t_{RPS} of Self Refresh is the time reguiring to complete the last refresh of Self Refresh.

Other Refresh Methods : It is also possible to refresh the KM4216C/V258 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS (Continued)

Table 1. Truth Table for Transfer Operation

*: Don't care

$\overline{RAS}$ Falling Edgd					Function	Transfer Direction	Transfer Data Bit
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	$\overline{SE}$			
H	L	H	L	*	Read Transfer	RAM→SAM	512 × 16
H	L	H	H	*	Split Read Transfer	RAM→SAM	256 × 16

Transfer Operation

Transfer operation is initiated when $\overline{DT/OE}$ is low at the falling edge of $\overline{RAS}$. The state of DSF when $\overline{RAS}$ goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation. (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT/OE}$ is low, $\overline{WB/WE}$ is high, and DSF is low at the falling edge of $\overline{RAS}$. The row address bits in the read transfer cycle indicate which sixteen 512 bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half). Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC, $\overline{DT/OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT/OE}$ must be Synchronized with the rising edge of SC (t_{TSL}/t_{TSD}) to retain the continuity of Serial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT/OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, $\overline{DT/OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT/OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT/OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

DEVICE OPERATIONS (Continued)

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of RAS.

Address: The row address is latched in the falling edge of $\overline{RAS}$. The column address defined by (A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. column addrress pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1= Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g.255th or 511th bit).
Example of SRT applications are shown in Fig.7 through Fig. 10

The normal usage of Split Read Transfer cycle is described in Fig.7. When Read Transfer is executed, data from X_1 row address is fully transferred to the DAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X_2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y_0" Tap address instead of "Y_0" is loaded.
The another example of SRT cycle is described in Fig.8 When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle.

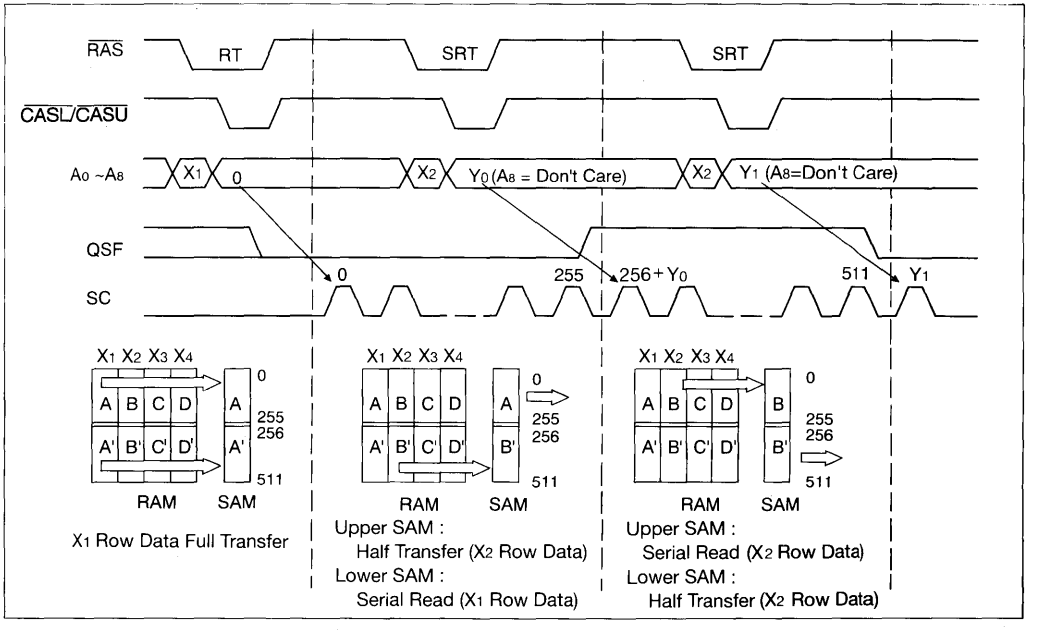


Figure 7. Split Read Transfer Normal Usage (Case1)

DEVICE OPERATIONS (Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig.9, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 10 indicates that SRT cycle is not performed until Serial Read is completed to the boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+ t_{STS}(See Figure 11.)

A split Read Transfer does not change the direction of the SAM I/O port.

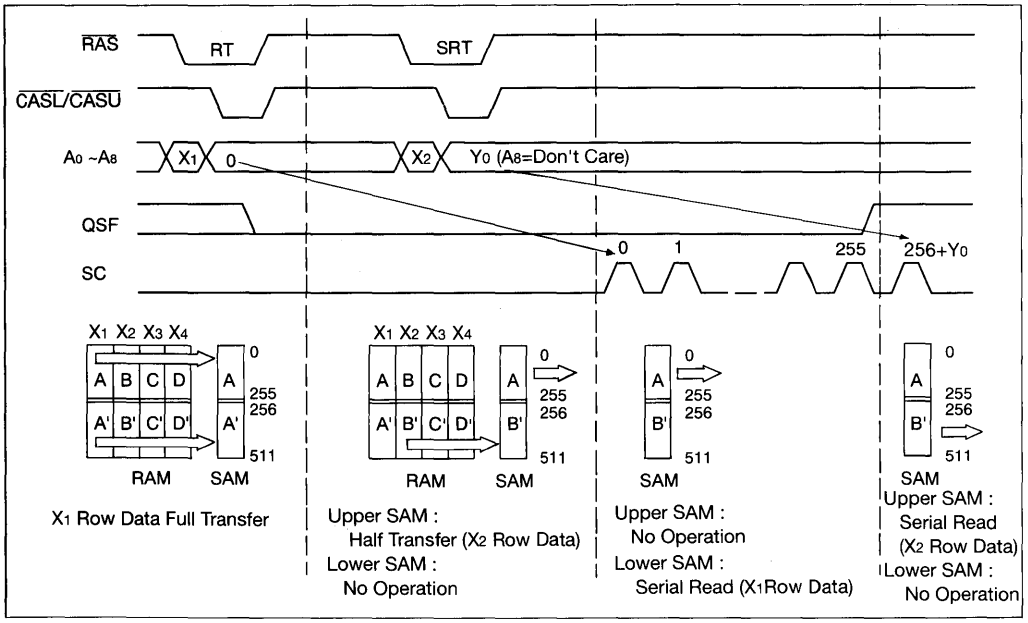


Figure 8. Split Read Transfer Normal Usage (Case 2)

DEVICE OPERATIONS (Continued)

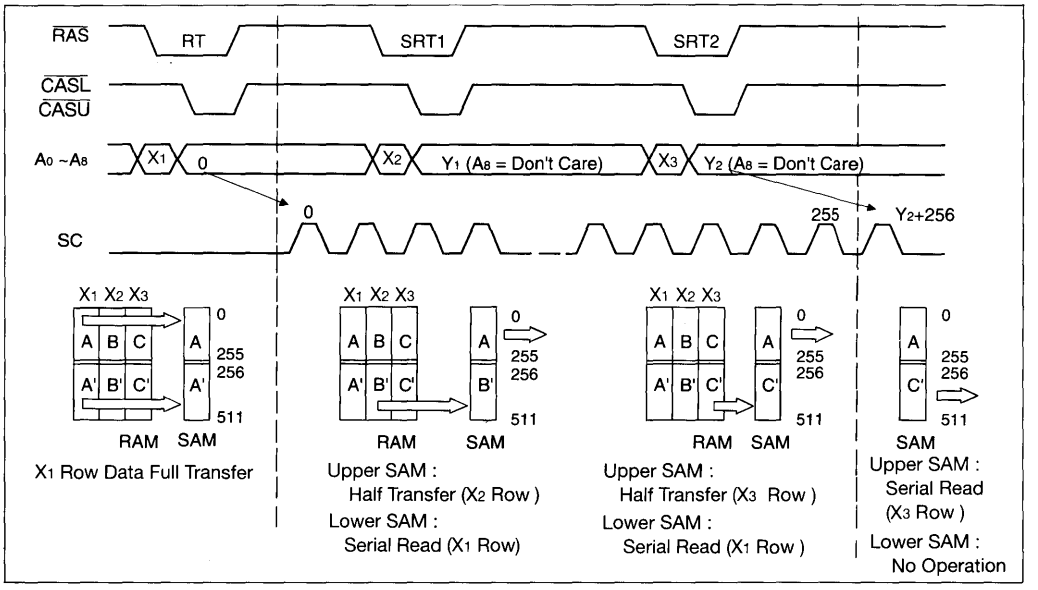


Figure 9. Split Read Transfer Abnormal Usage (Case 1)

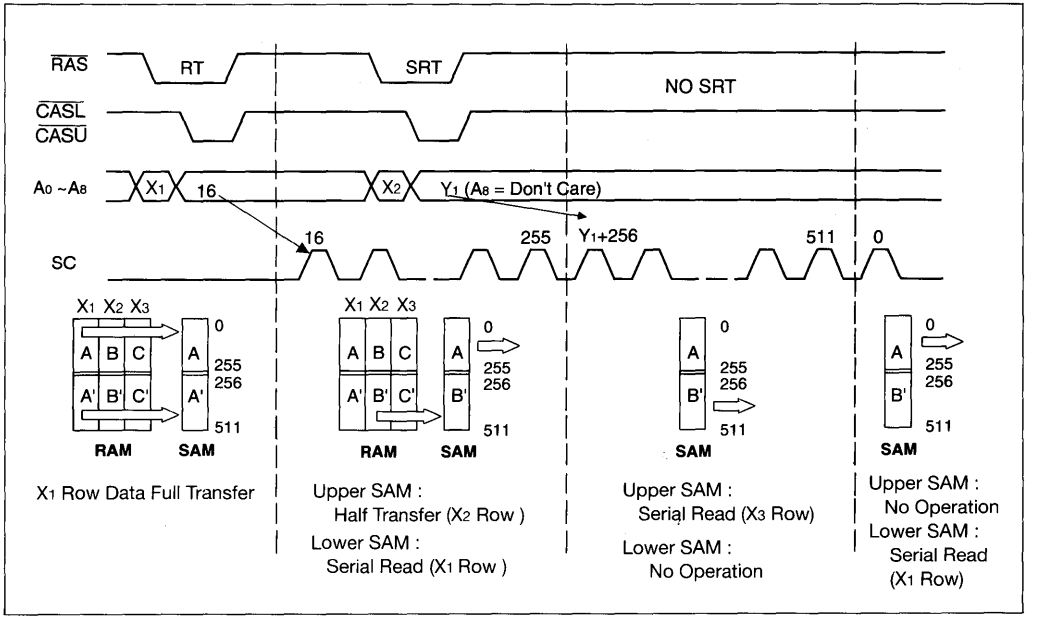


Figure 10. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATIONS (Continued)

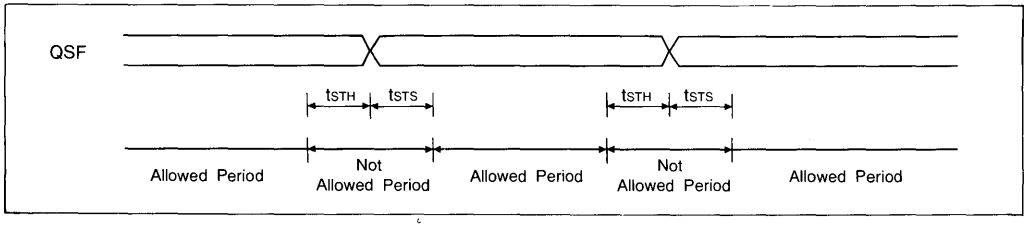


Figure 11. Split Transfer Cycle Limitation Period

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half.
After the last address of each half SAM(255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded TAP address).
This last address is called Stop Point.
The KM4216C/V258 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WB}/\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.
The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.
In Figure 12. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address(70) of the next half. Otherwise, the access will continue in the same half until a SRT occurs or the SAM half boundary (255, 511).
Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. CBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$. The CBRR will take effect immediately; it does not require a SRT to become active valid.

Table 2. Stop Point Setting Address

Stop Register= Store Address of Serial Access Use on the Split Transter Cycle Stop Pointer Set → CBRS Cycle							
Number of Stop Points/Half	**Partition**	**Stop Point Setting Address**					
		A8	**A7**	**A6**	**A5**	**A4**	**A3~A0**
1	(1×256)×2	x	1	1	1	1	x
2	(2×128)×2	x	0	1	1	1	x
4	(4×64)×2	x	0	0	1	1	x
8	(8×32)×2	x	0	0	0	1	x
16	(16×16)×2	x	0	0	0	0	x

*Other Case=Inhibit
X=Don't Care

DEVICE OPERATIONS (Continued)

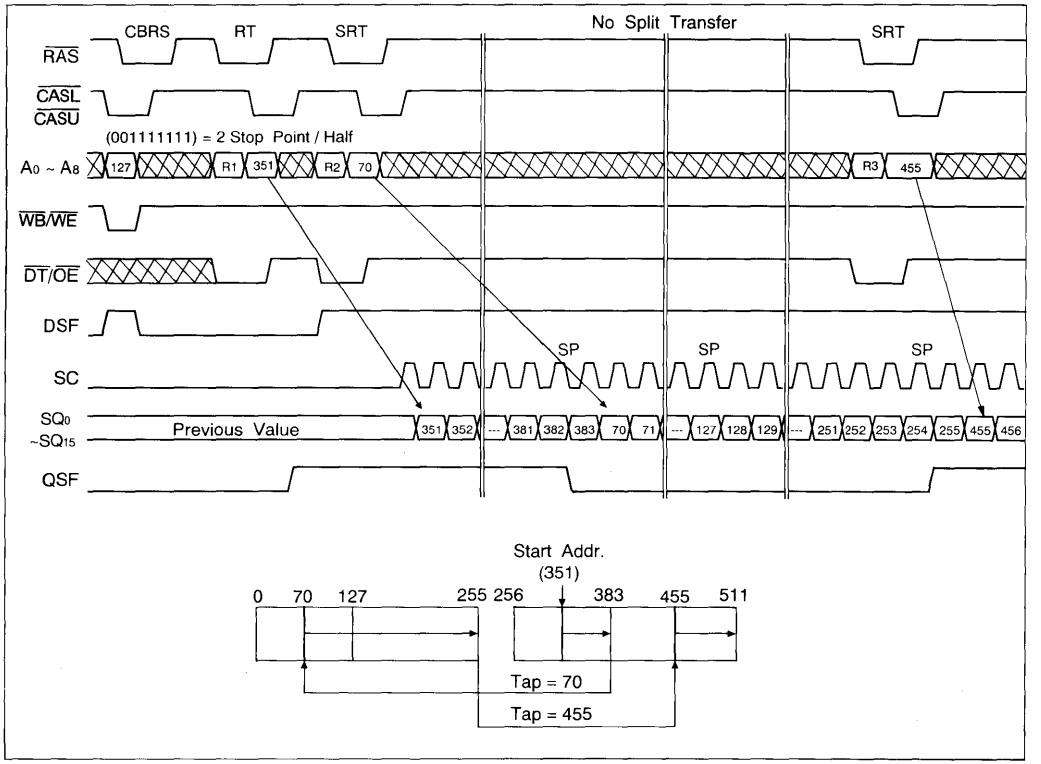
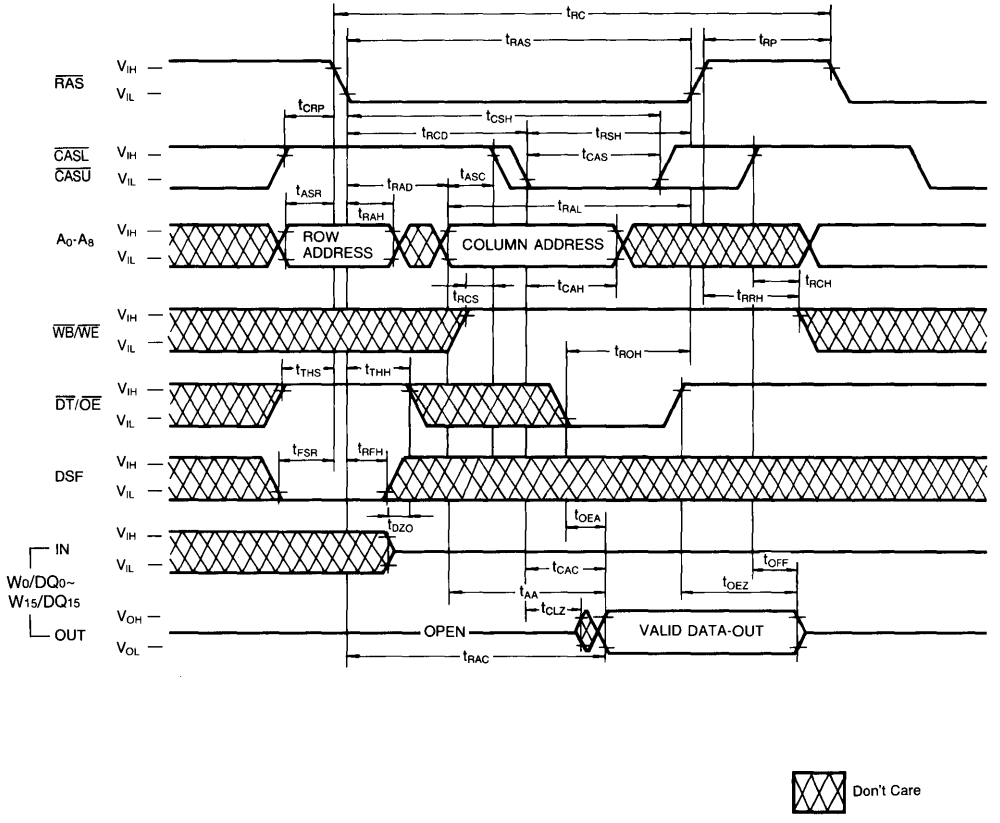


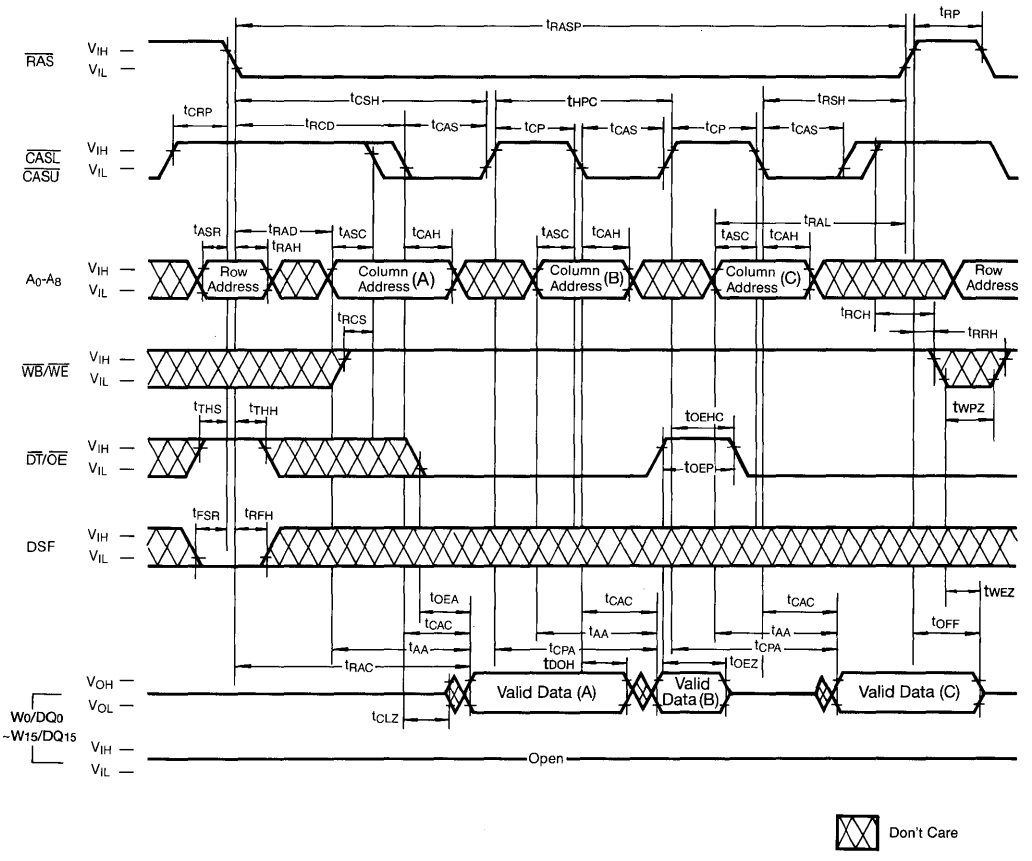
Figure 12. Programmable Split SAM operation

TIMING DIAGRAMS

READ CYCLE



FAST PAGE MODE READ CYCLE (Extended Data Out)



Truth Table for Write Cycle(1)

FUNCTION	$\overline{RAS}$			$\overline{CAS}$	$\overline{CAS}$ or $\overline{WBL(U)}/\overline{WEL(U)}$
	*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 Wi/DQi (3) (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask) (4)	1	0	×	1	Column Mask
Masked Block Write (4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register (2)	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram on the following pages
(2) Old Mask data load
(3) Function table for Old Mask and New Mask

IF		*1 $\overline{WB}/\overline{WE}$	*3 Wi/DQi	Note
LMR Cycle Executed	Yes	0	×	Write using mask register data (Old Mask Data)
		1	×	Non Masked Write
	No	0	Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	×	Non Masked Write

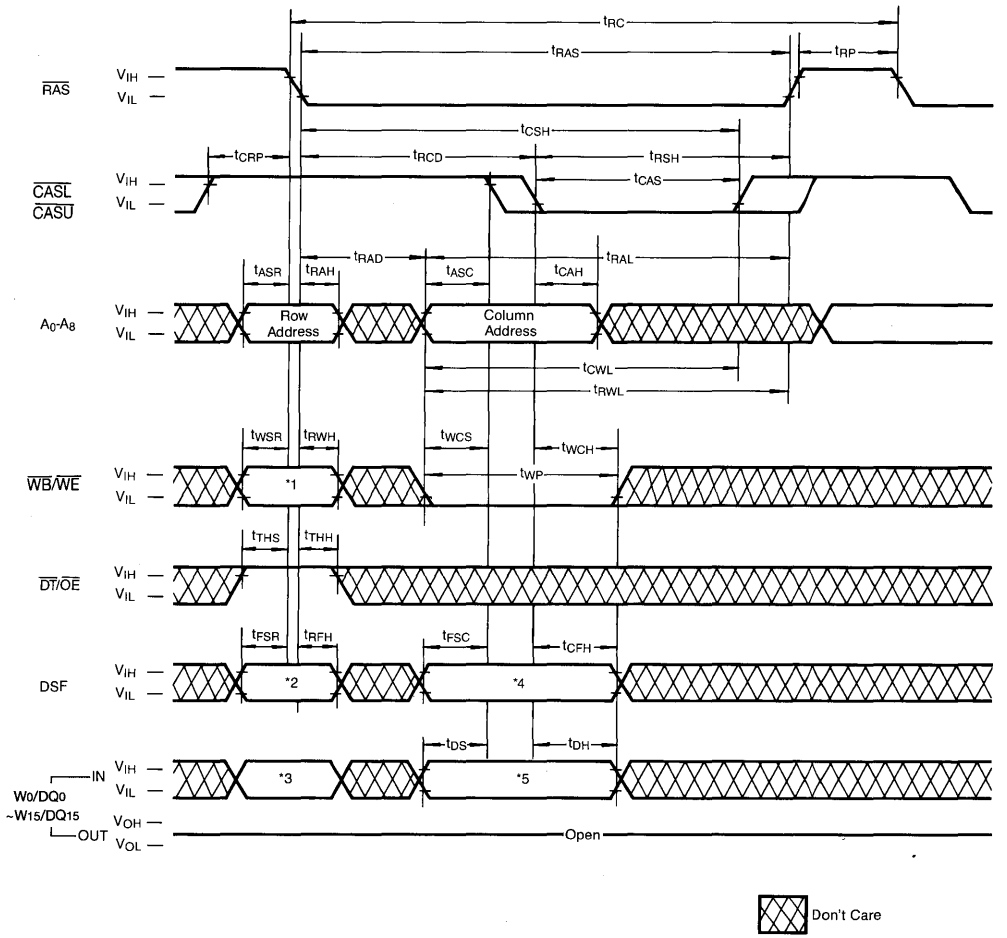
× : Don't Care

(4) Function Table for Block Write Column Mask

Column Address		
A2	A1	A0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

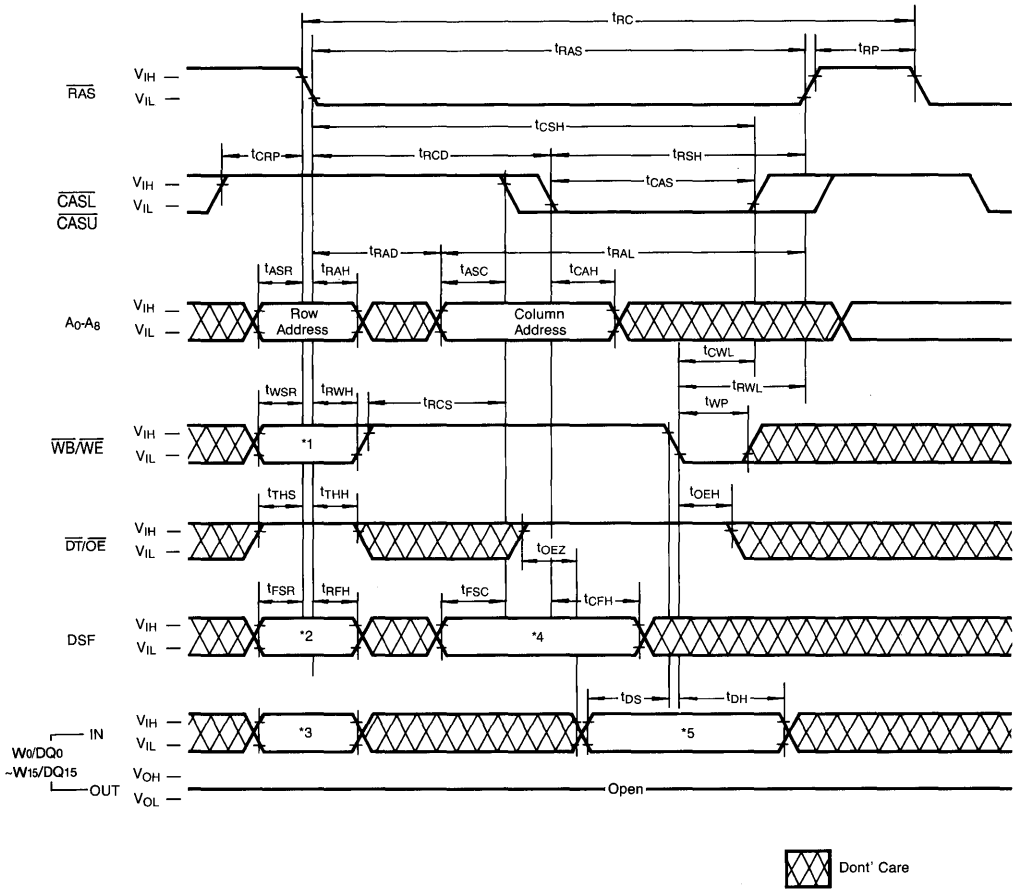
*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W_0/DQ_0	W_8/DQ_8	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
W_1/DQ_1	W_9/DQ_9		
W_2/DQ_2	W_{10}/DQ_{10}		
W_3/DQ_3	W_{11}/DQ_{11}		
W_4/DQ_4	W_{12}/DQ_{12}		
W_5/DQ_5	W_{13}/DQ_{13}		
W_6/DQ_6	W_{14}/DQ_{14}		
W_7/DQ_7	W_{15}/DQ_{15}		

EARLY WRITE CYCLE



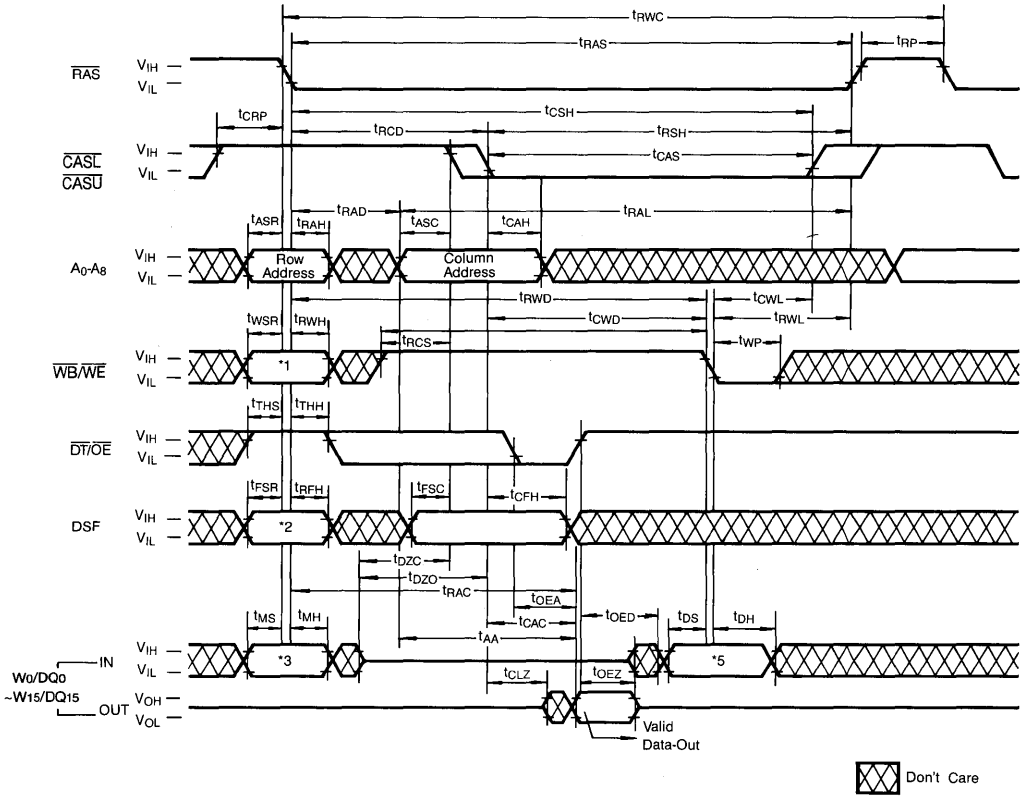
Note : In Block write cycle, only column address A3~A8 are used.

LATE WRITE CYCLE



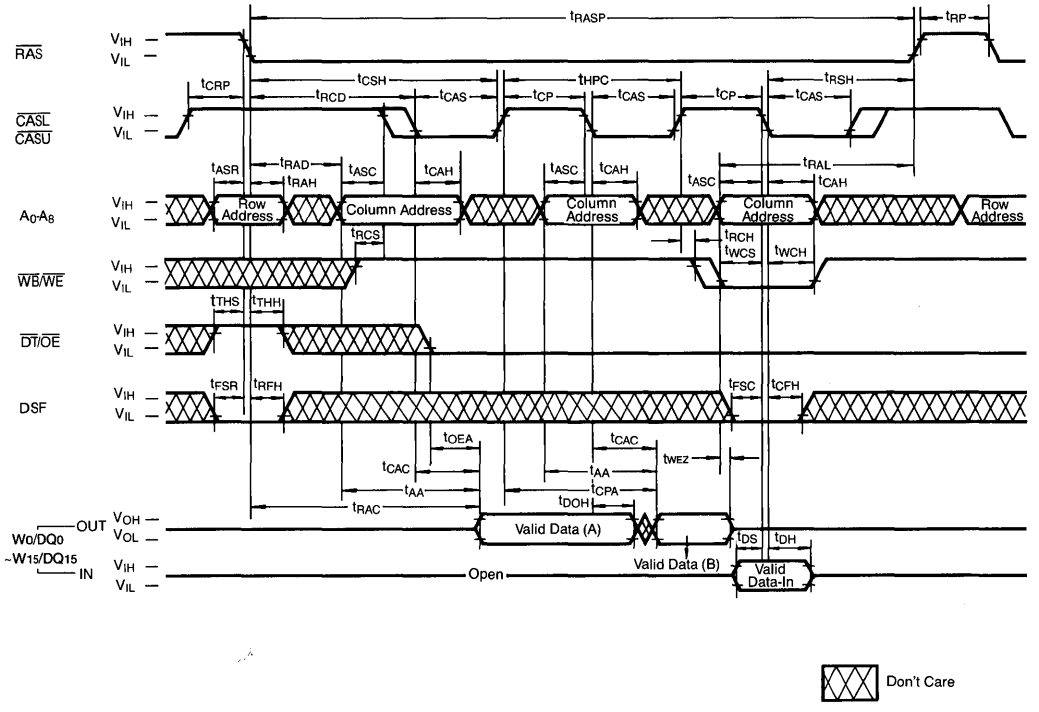
Note : In Block write cycle, only column address A3~A8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE

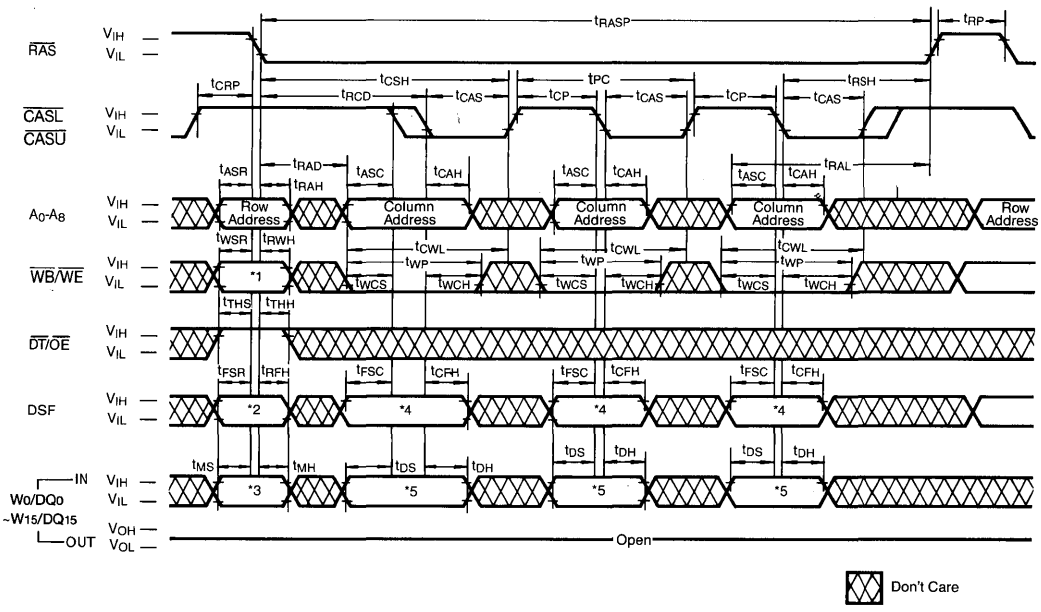


Note : In Block write cycle, only column address A3~A8 are used.

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

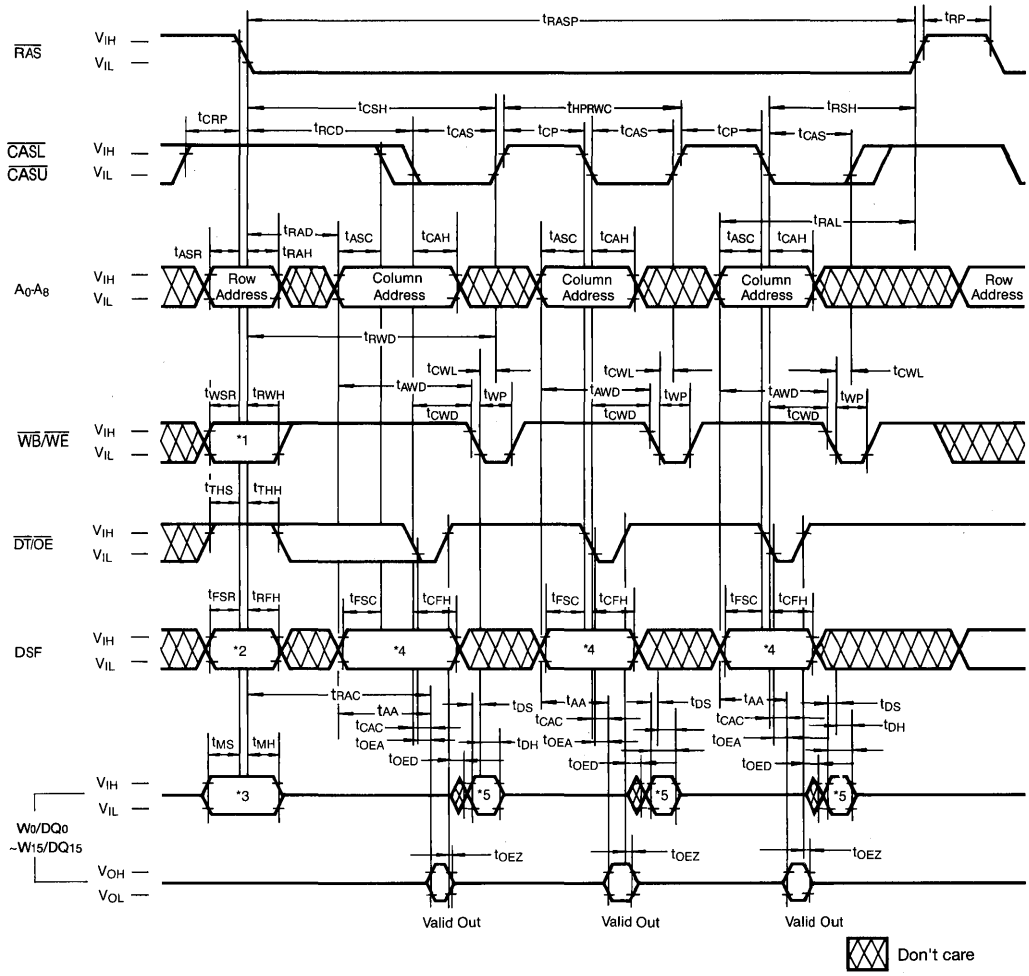


FAST PAGE MODE EARLY WRITE CYCLE



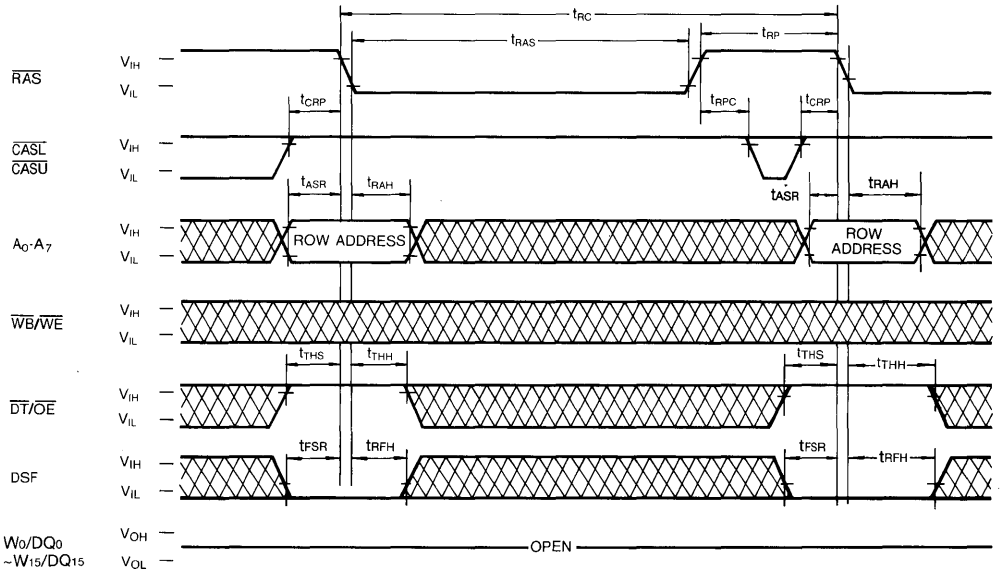
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

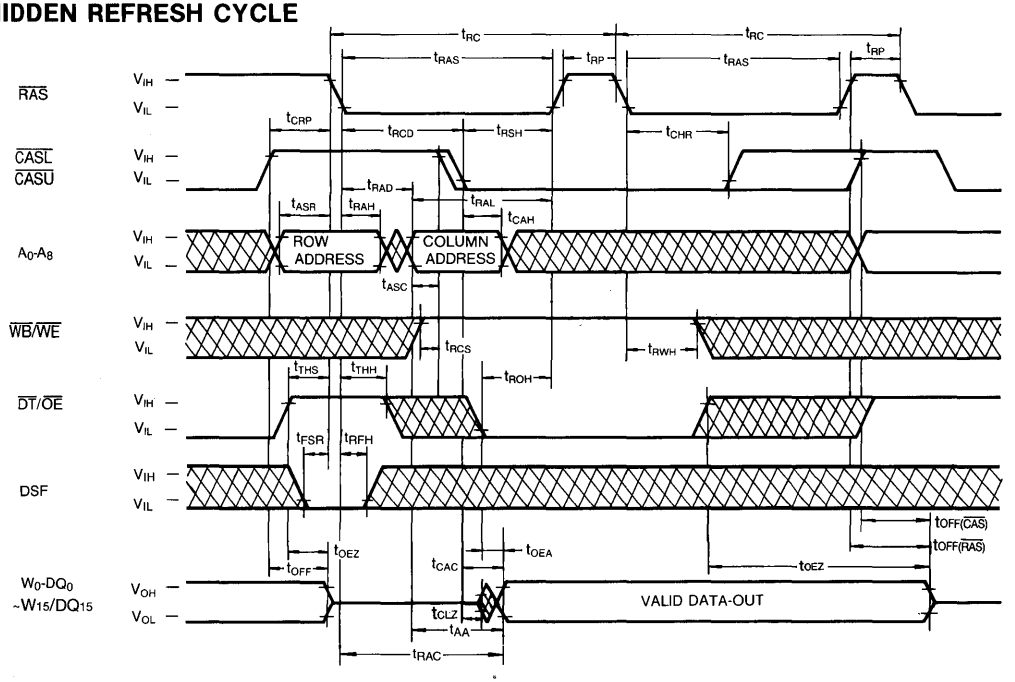


Note : In Block write cycle, only column address A_3~A_8 are used.

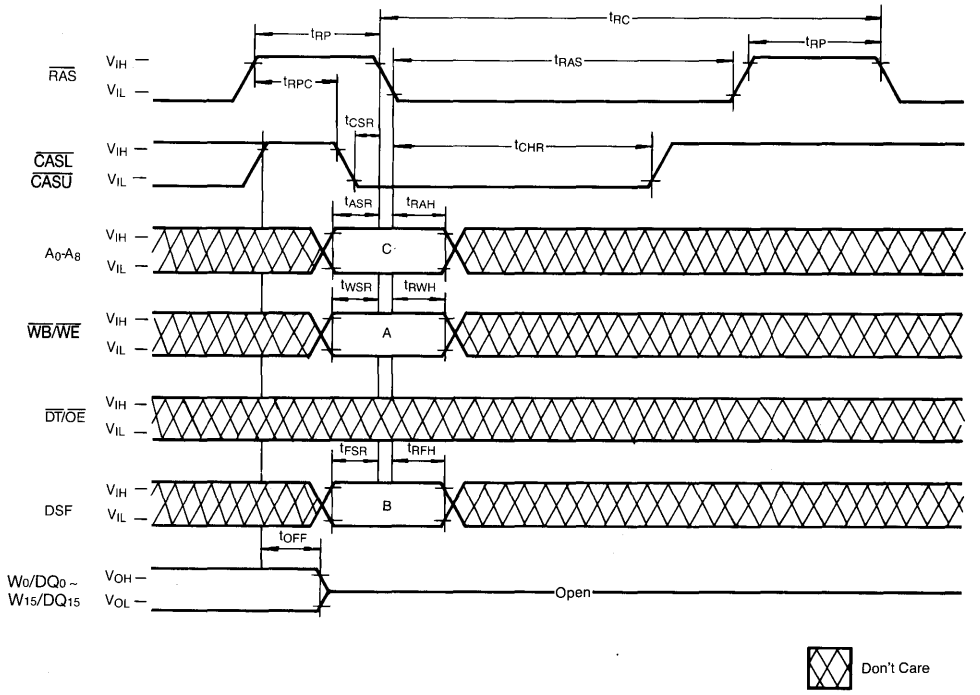
$\overline{RAS}$ ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE



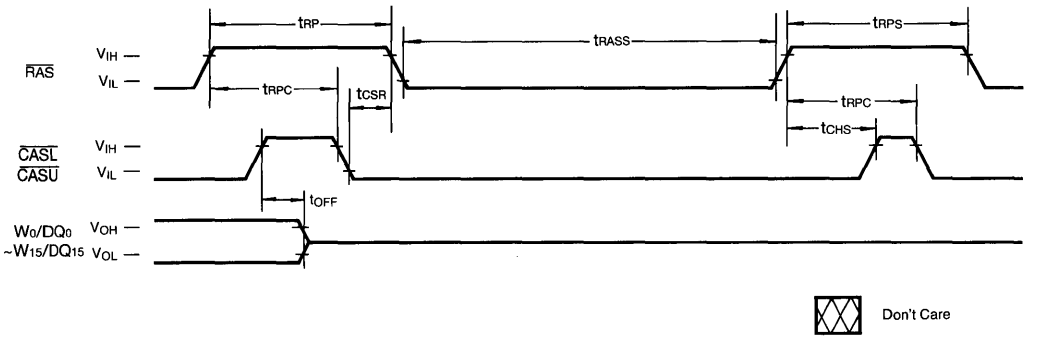
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE FUNCTION TABLE

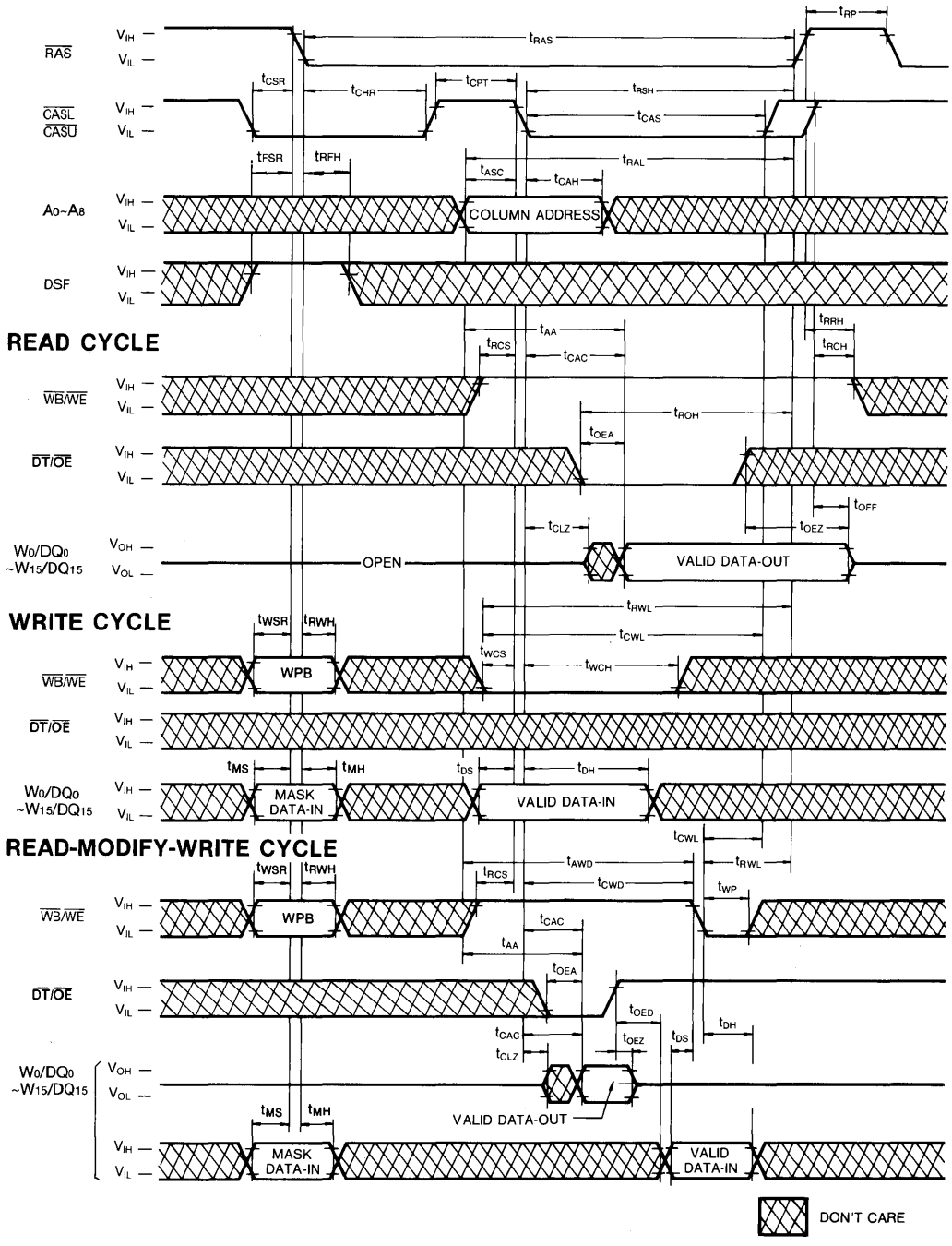
FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	STOP Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

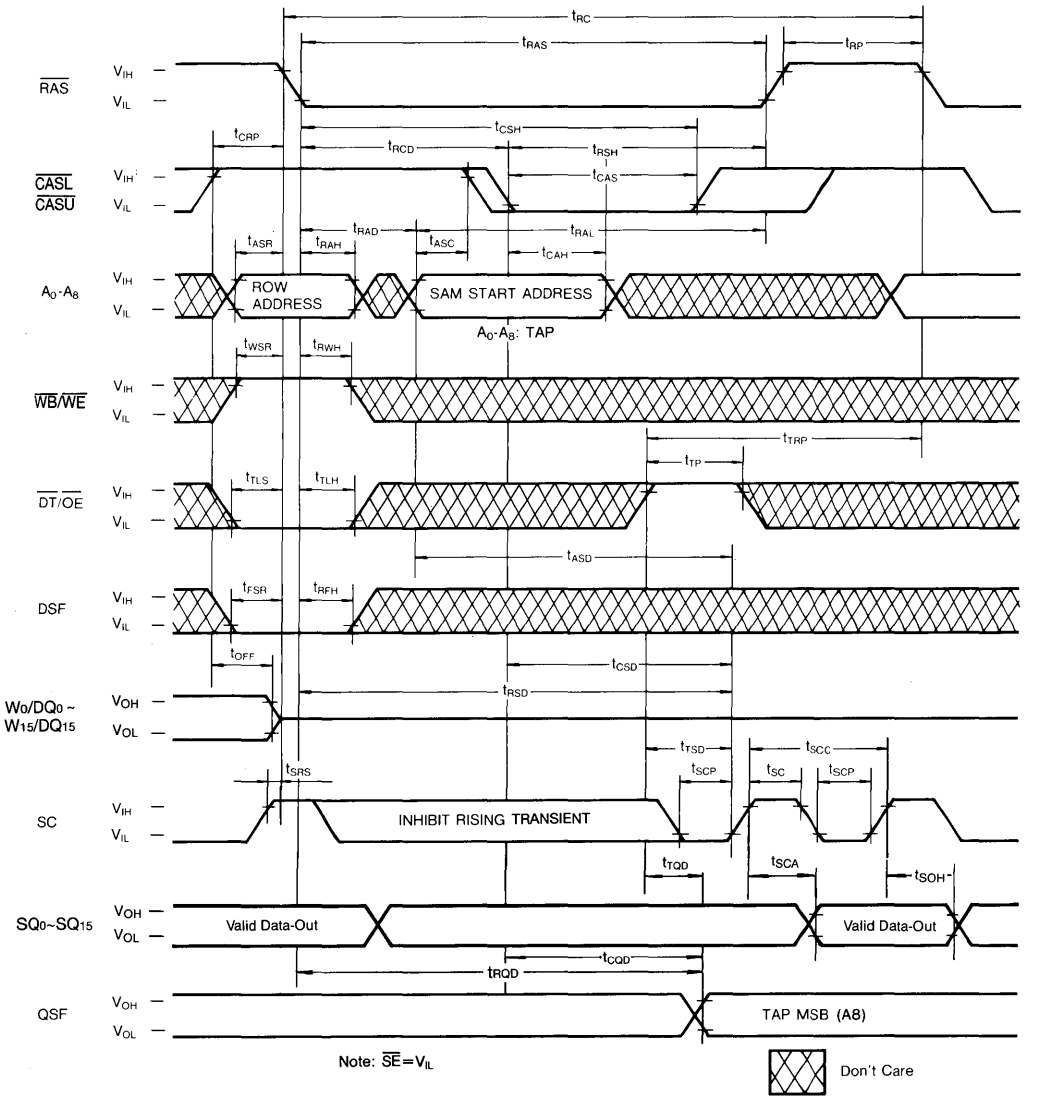


*CBR SELF REFRESH CYCLE IS APPLICABLE WITH CBRR, CBRS, OR CBRN CYCLE

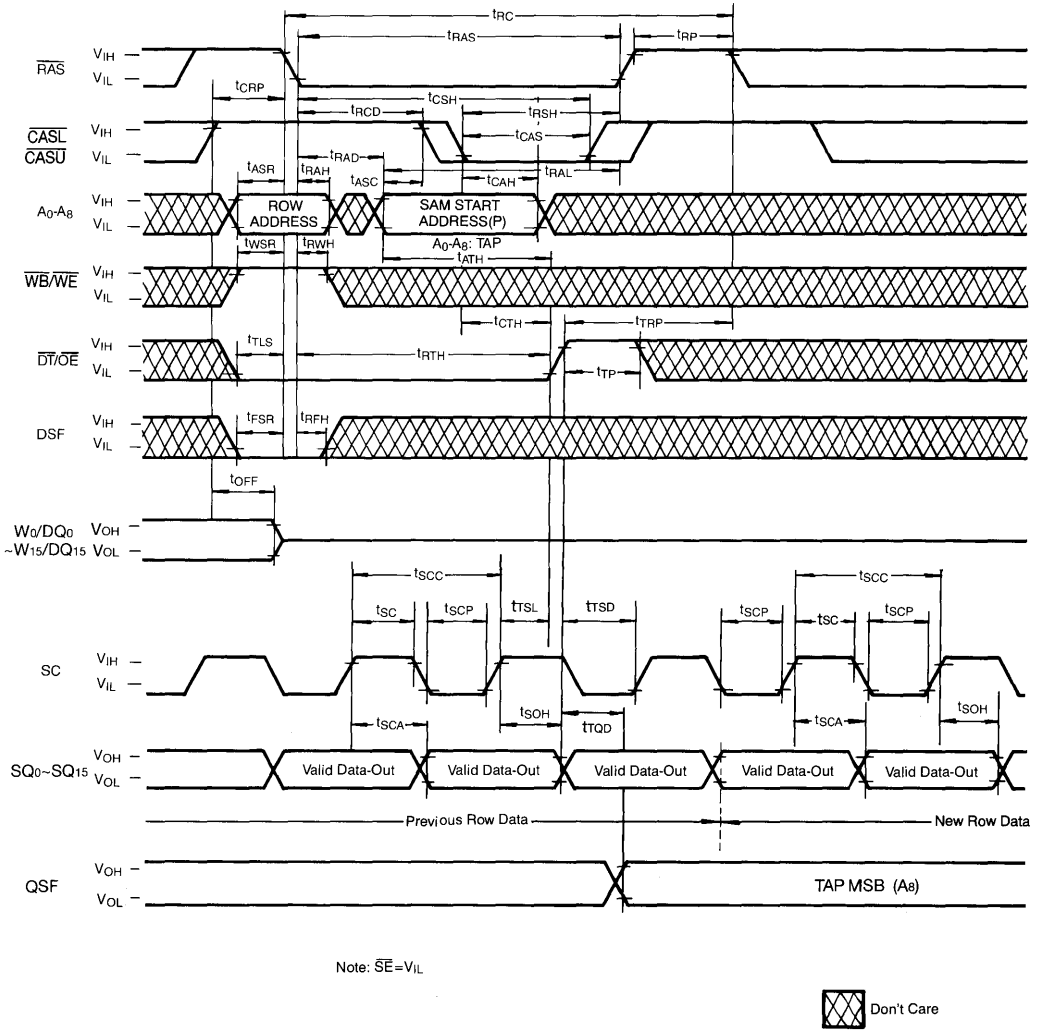
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



READ TRANSFER CYCLE



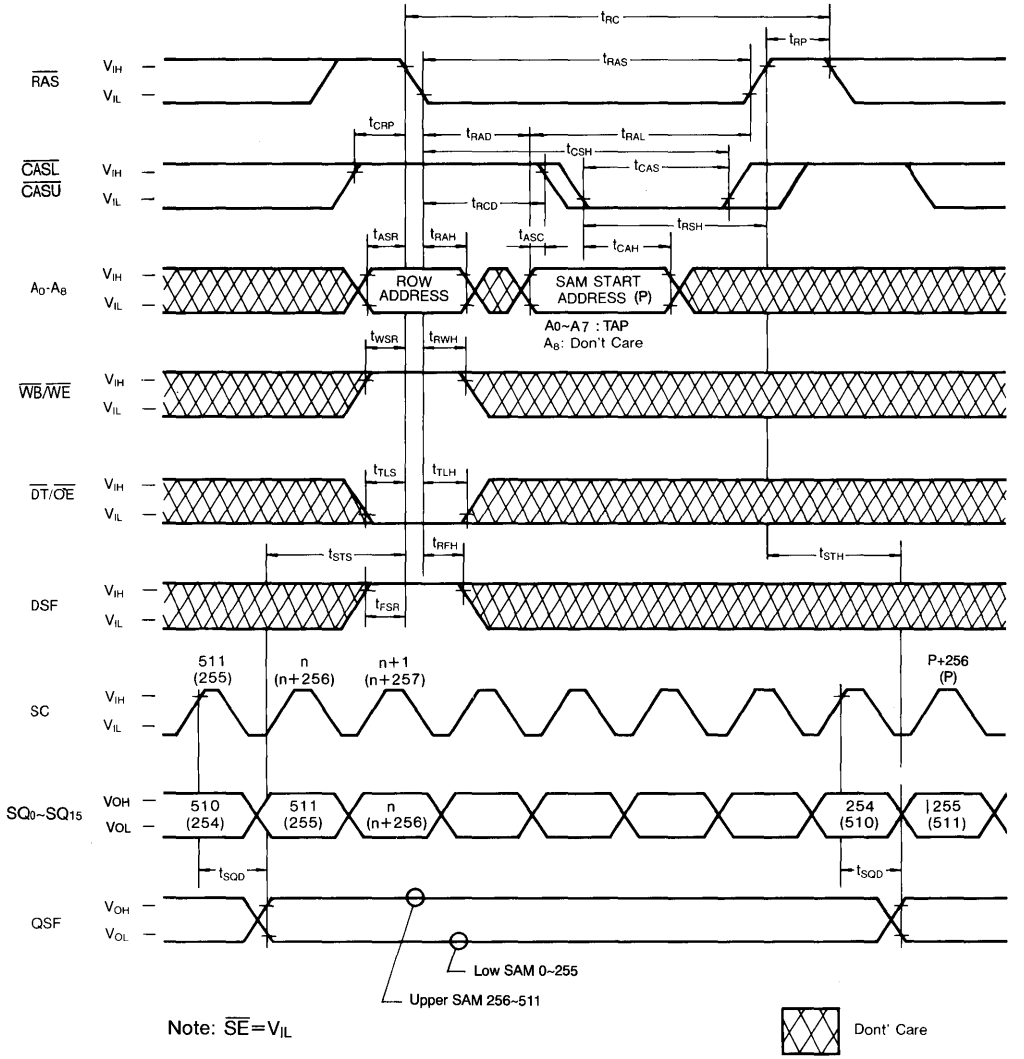
REAL TIME READ TRANSFER CYCLE



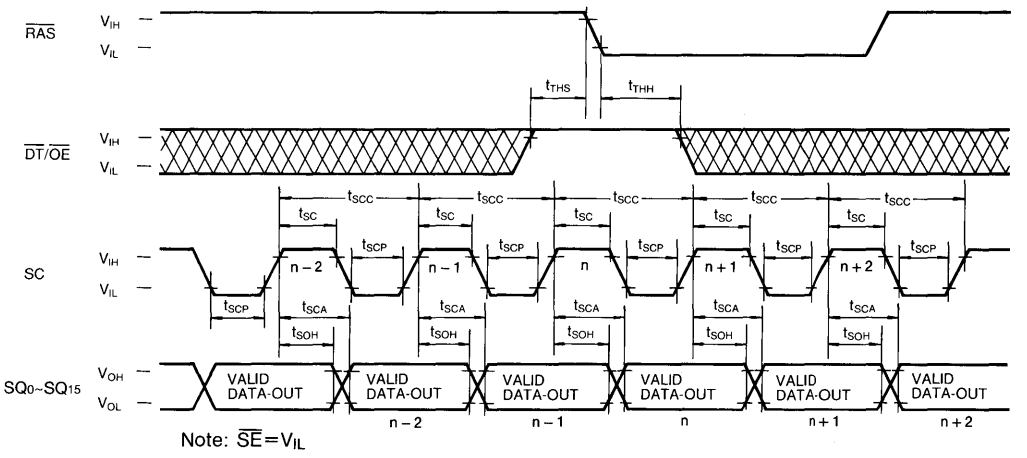
Note: $\overline{SE}$=VIL

Don't Care

SPLIT READ TRANSFER CYCLE

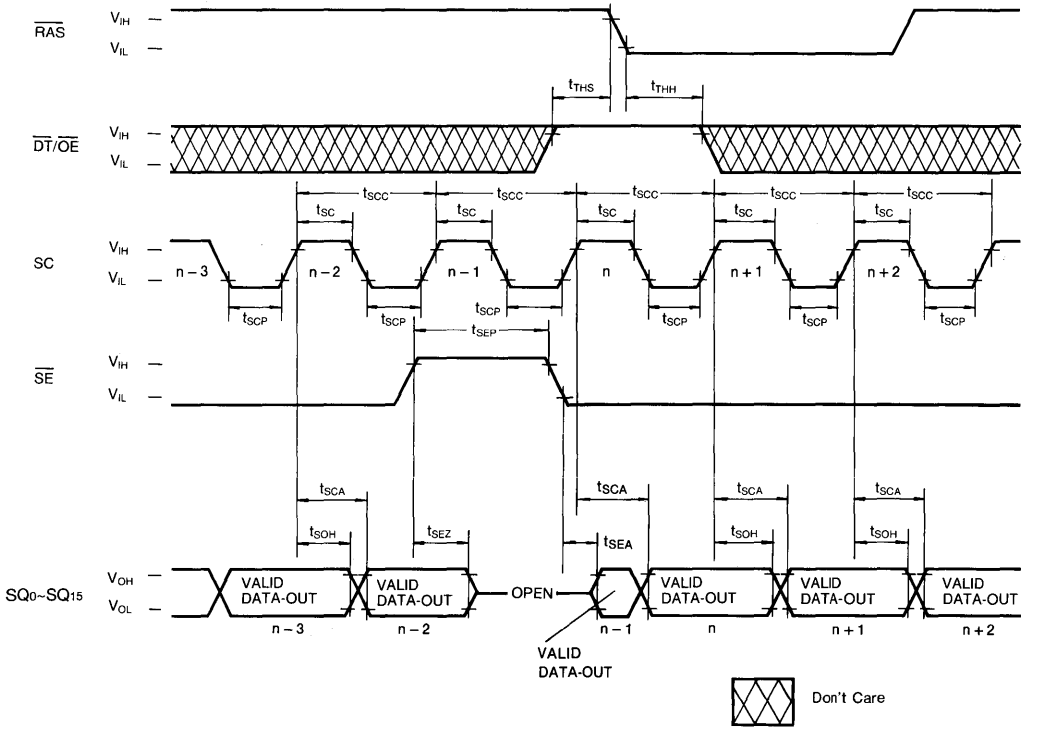


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$=V_{IL}

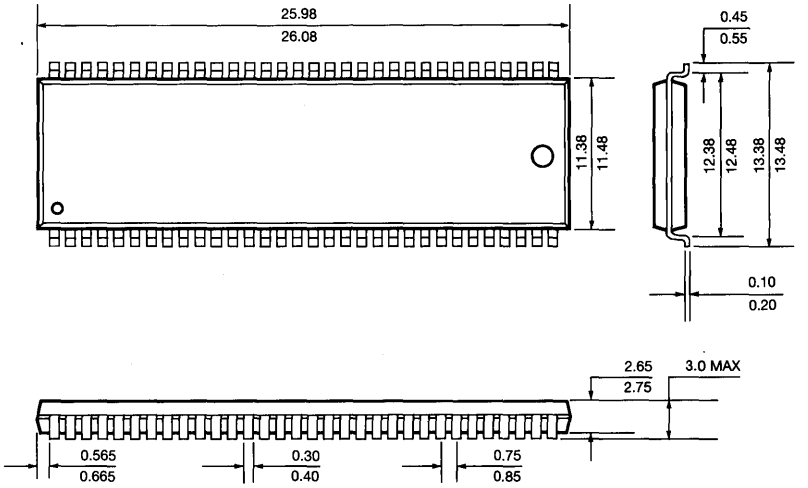
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



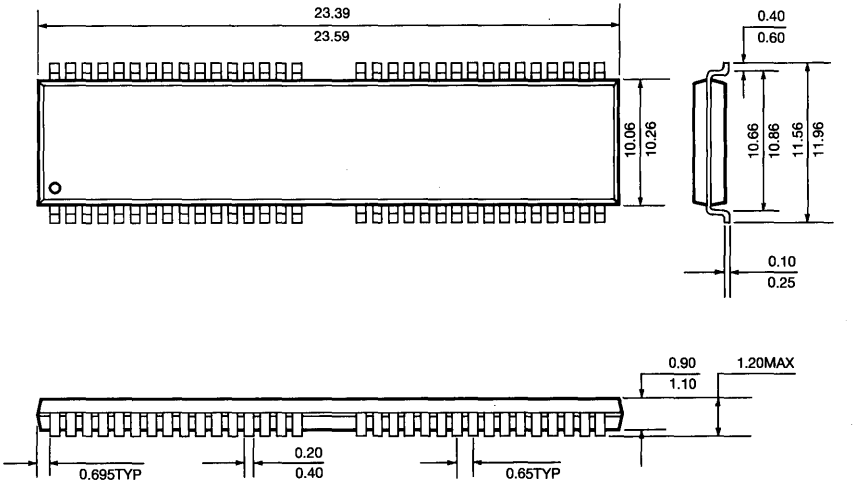
PACKAGE DIMENSIONS

Units: Millimeters

64 Pin Plastic Shrink Small Out Line Package



70(64) Pin Plastic Thin Small Out Line Package (Type II Forward)



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