Overview

SAMSUNG's S3C2412 is a Derivative product of S3C2410A. S3C2412 is designed to provide hand-held devices and general applications with cost-effective, low-power, and high-performance micro-controller solution in small die size. To reduce total system cost and enhance the performance, S3C2410A with 0.18 um CMOS process was migrated to 0.13 um CMOS process.
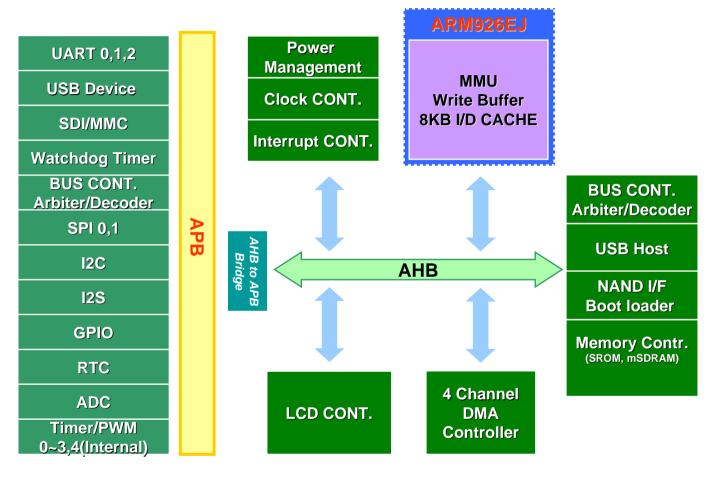
Features Summary

- **ARM926EJ ARM CPU with 8KB I-Cache/8KB D-Cache/MMU**
- **External memory controller (DRAM/ROM Control and Chip Select logic)**
- **LCD controller (max. 16M color TFT at 24 bpp mode and 65K color STN) with 1-ch LCD-dedicated DMA**
- **4-ch DMAs with external request pins**
- **3-ch UART (IrDA1.0, 64-Byte Tx FIFO, and 64-Byte Rx FIFO) / 2-ch SPI**
- **1-ch multi-master IIC-BUS/1-ch IIS-BUS controller**
- **SD Host controller version 1.0 & Multi-Media Card Protocol version 2.11 compatible**
- **2-port USB Host /1- port USB Device (ver 1.1)**
- **4-ch PWM timers & 1-ch internal timer**
- **Watch Dog Timer**
- **117-bit general purpose I/O ports / 24-ch external interrupt source**
- **Power control: Normal, Idle, Stop and Sleep mode**
- **8-ch 10-bit ADC and Touch screen interface**
- **RTC with calendar function**
- **On-chip clock generator with PLL**
- **0.13 μm low-power technology.**

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Functional Block Diagram

APB side		Bridge	AHB core	ARM926EJ	AHB right side

APB peripherals:
- UART 0,1,2
- USB Device
- SDI/MMC
- Watchdog Timer
- BUS CONT. Arbiter/Decoder
- SPI 0,1
- I2C
- I2S
- GPIO
- RTC
- ADC
- Timer/PWM 0~3,4(Internal)

APB

Power Management

Clock CONT.

Interrupt CONT.

ARM926EJ
MMU
Write Buffer
8KB I/D CACHE

AHB to APB Bridge

AHB

LCD CONT.

4 Channel DMA Controller

BUS CONT. Arbiter/Decoder

USB Host

NAND I/F Boot loader

Memory Contr. (SROM, mSDRAM)

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Product Details

■Architecture

- ■Integrated system for hand-held devices and general embedded applications
- ■16/32-Bit RISC architecture and powerful instruction set with ARM926EJ-S CPU core
- ■Enhanced ARM architecture MMU to support WinCE and Linux
- ■Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- ■Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB)

■System Manager

- ■Little/Big Endian support
- ■Address space: 128M bytes for each bank (total 1G bytes)
- ■Supports programmable 8/16/32-bit data bus width for each bank
- ■Eight memory banks:
  - •Six memory banks for ROM, SRAM, and others
  - •Two memory banks for SDRAM
  - •Mobile SDRAM Interface
  - •100/133MHz address and command bus speed
  - •1.8~3.3V interface voltage
- ■Supports external wait signals to expend the bus cycle
- ■Supports self-refresh mode in SDRAM for power down mode

■NAND Flash Boot Loader

- ■Supports booting from NAND flash memory
- ■4KB internal buffer for booting
- ■Supports storage memory for NAND flash memory after booting
- ■8/16bit NAND Flash Interface.

■Cache Memory

- ■64-way set-associative cache with I-Cache (8KB) and D-Cache (8KB)
- ■8words length per line with one valid bit and two dirty bits per line
- ■Pseudo random or round robin replacement algorithm
- ■Write-through or write-back cache operation to update the main memory
- ■The write buffer can hold 16 words of data and four addresses.

■Clock & Power Manager

- ■On-chip MPLL and UPLL:
  - •UPLL generates the clock to operate USB Host/Device.
  - •MPLL generates the clock to operate CPU
- ■Clock can be fed selectively to each function block by software.
- ■Power mode: Normal, Slow, Stop and Sleep mode
  - - Normal mode: Normal operating mode
  - - Stop: All operation clocks are fixed to low.
  - - Idle mode: The clock for only CPU is stopped.
  - - Sleep: The internal power will be off.
- ■ Wake up by EINT[15:0] or RTC alarm interrupt from Power-Off mode

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■ Interrupt Controller

- 59 Interrupt sources
  (One Watch dog timer, 5 timers, 9 UARTs, 24 external interrupts, 4 DMA, 2 RTC, 2 ADC, 1 IIC, 4 SPI, 2 SDI, 2 USB, 1 LCD, 1 Nand and 1 Battery Fault)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

■ Timer with Pulse Width Modulation

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

■ RTC (Real Time Clock)

- Full clock feature: second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

■ General Purpose Input/Output Ports

- 24 external interrupt ports
- multiplexed input/output ports

■ UART

- 3-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive (Tx/Rx)
- Supports external clocks for the UART operation (UEXTCLK)
- Programmable baud rate
- Supports IrDA 1.0
- Each channel has internal 64-byte Tx FIFO and 64-byte Rx FIFO

■ DMA Controller

- 4-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

■ A/D Converter & Touch Screen Interface

- 8-ch multiplexed ADC
- Max. 500KSPS and 10-bit Resolution

■ LCD Controller STN LCD Displays Feature

- Supports 3 types of STN LCD panels: 4-bit dual scan, 4-bit single scan, 8-bit single scan display type
- Supports monochrome mode, 4 gray levels, 16 gray levels, 256 colors and 65K colors for STN LCD
- Supports multiple screen size
  - Typical actual screen size: 320x240, 160x160, and others
  - Maximum virtual screen size is 4 Mbytes.
  - Maximum virtual screen size in 256 color mode: 4096x1024 and others

■ TFT Color Displays Feature

- Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT
- Supports 16 bpp non-palette true-color displays for color TFT
- Supports maximum 16M color TFT at 24 bpp mode
- Supports multiple screen size
  - Typical actual screen size: 320x240, 160x160, and others
  - Maximum virtual screen size is 4Mbytes.
  - Maximum virtual screen size in 64K color mode: 2048x1024, and others

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■ Watchdog Timer

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

■ IIC-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in Fast mode.

■ IIS-Bus Interface

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 64 Bytes FIFO for Tx/Rx
- Supports IIS format and MSB-justified data format
- Support Full Duplex mode

■ USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

■ USB Device

- 1-port USB Device
- 5 Endpoints for USB Device
- Compatible with USB Specification version 1.1
- Support only full speed

■ SD/MMC Host Interface

- Compatible with SD Memory Card Protocol version 1.0
- Compatible with SDIO Card Protocol version 1.0
- 64Bytes FIFO for Tx/Rx
- DMA based or Interrupt based operation
- Compatible with Multimedia Card Protocol version 2.11

■ SPI Interface

- Compatible with 2-ch Serial Peripheral Interface Protocol version 2.11
- 16 bytes FIFO for Tx/Rx
- DMA-based or interrupt-based operation

■ Operating Frequency & Voltage Range

- Core: 1.25V@200MHz, 1.4V@266MHz
- Memory : 1.8V mDRAM@100/133MHz
            3.3V SDRAM @100/133MHz
- I/O : 1.8~3.3V

■ Package

- 272-FBGA