

KMM5322204AW/AWG Fast Page Mode with Extended Data out
2Mx32 DRAM SIMM, 5V, 1K Refresh Using 1Mx16 DRAM

GENERAL DESCRIPTION

The Samsung KMM5322204AW is a 2M bit x 32 Dynamic RAM high density memory module. The Samsung KMM5322204AW consists of four CMOS 1Mx16bit DRAMs in 42-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1uF or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5322204AW is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
 - KMM5322204AW(1024 cycles/16ms Ref. SOJ, Solder)
 - KMM5322204AWG(1024 cycles/16ms Ref. SOJ, Gold)
- Fast Page Mode with Extended data out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height (750 mil), double sided component

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
- 6	60ns	15ns	110ns	30ns
- 7	70ns	20ns	130ns	33ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	RAS1
10	Vcc	46	NC
11	NC	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

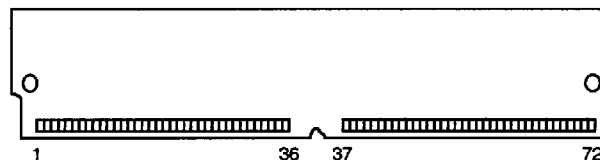
A0 - A9	Address Inputs
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Input
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS
PD1	NC	NC
PD2	NC	NC
PD3	NC	Vss
PD4	NC	NC

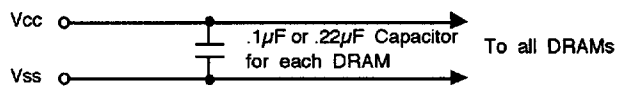
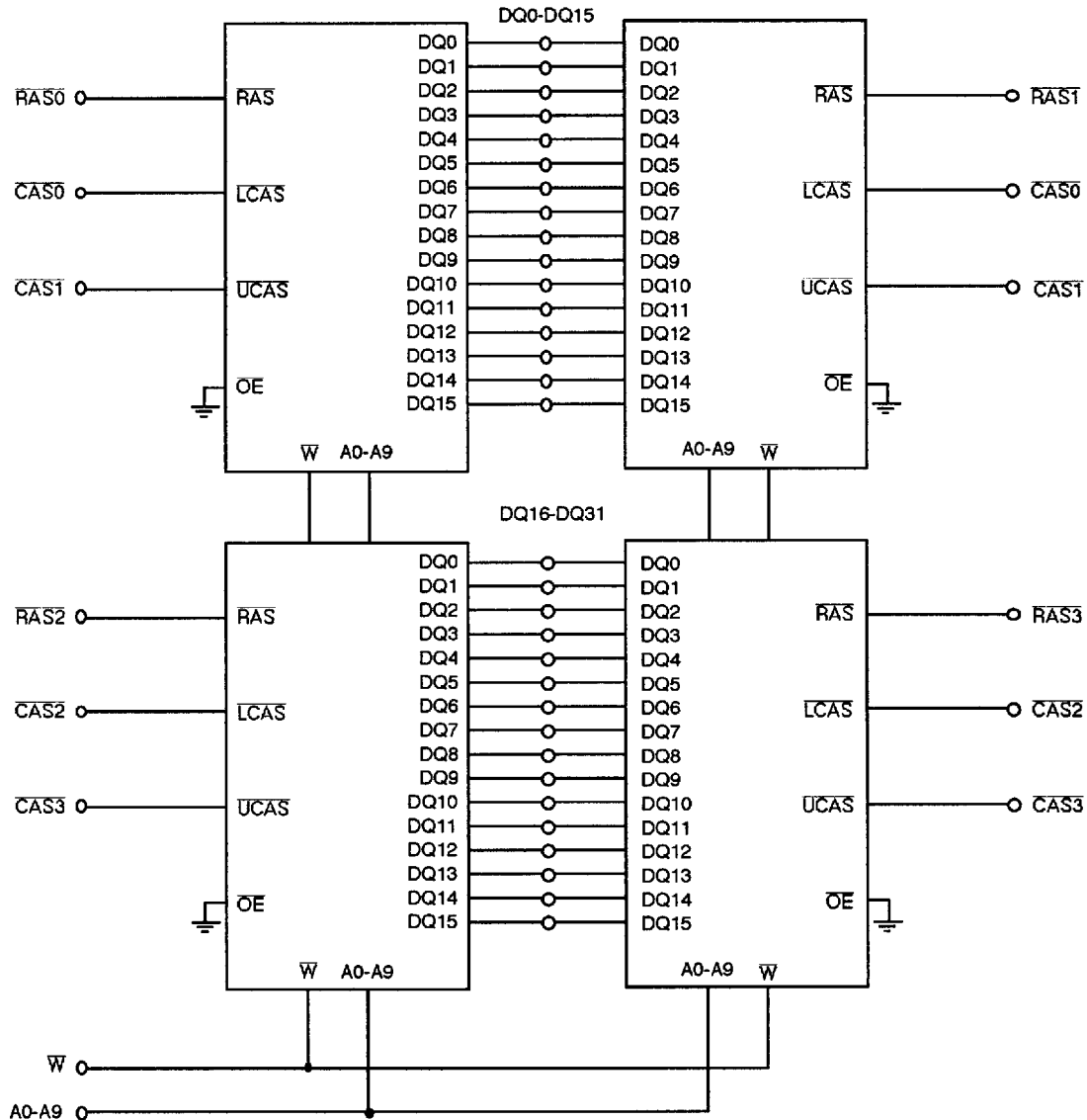
*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	4	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta=0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1*1	V
Input Low Voltage	VIL	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM5322204AW/AWG		Unit
		Min	Max	
ICC1	- 6	-	324	mA
	- 7	-	304	mA
ICC2		-	8	mA
ICC3	- 6	-	324	mA
	- 7	-	304	mA
ICC4	- 6	-	224	mA
	- 7	-	204	mA
ICC5		-	2	mA
ICC6	- 6	-	324	mA
	- 7	-	304	mA
II(L)		-20	20	µA
IO(L)		-10	10	µA
VOH		2.4	-	V
VOL		-	0.4	V

ICC1 : Operating Current * (RAS, CAS, Address cycling @tRC=min.)

ICC2 : Standby Current (RAS=CAS=W=VIH)

ICC3 : RAS Only Refresh Current * (CAS= VIH, RAS cycling @tRC =min.)

ICC4 : EDO Mode Current * (RAS=VIL, CAS, Address cycling : tHPC=min.)

ICC5 : Standby Current (RAS=CAS=W=Vcc-0.2V)

ICC6 : CAS-Before-RAS Refresh Current * (RAS and CAS cycling @tRC=min.)

II(L) : Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test = 0V)

IO(L) : Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)

VOH : Output High Voltage Level (IOH = - 5mA)

VOL : Output Low Voltage Level (IOL = 4.2mA)

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while RAS=VIL. In ICC4, address can be changed maximum once within one EDO mode cycle, tHPC.

CAPACITANCE ($T_a = 25\text{ }^\circ\text{C}$, $V_{cc}=5\text{V}$, $f=1\text{MHz}$)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A9]	CIN1	-	44	pF
Input capacitance [W]	CIN2	-	48	pF
Input capacitance [$\overline{\text{RAS0}}$, $\overline{\text{RAS3}}$]	CIN3	-	20	pF
Input capacitance [$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$]	CIN4	-	29	pF
Input/Output capacitance [DQ0-31]	CDQ1	-	29	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_a \leq 70^\circ\text{C}$, $V_{cc}=5.0\text{V} \pm 10\%$. See notes 1, 2.)

Test condition : $V_{ih}/V_{il}=2.4\text{V}/0.8\text{V}$, $V_{oh}/V_{ol}=2.0\text{V}/0.8\text{V}$, Output loading $C_L=100\text{pF}$

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		ns	
Access time from $\overline{\text{RAS}}$	tRAC		60		70	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		17		20	ns	3,4,5
Access time from column address	tAA		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	15	3	20	ns	6,11,12
Transition time (rise and fall)	tT	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	40		50		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	17		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	10	10K	15	10K	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	30	15	35	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		15		ns	
Write command pulse width	tWCP	10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	10		15		ns	
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	10		15		ns	9
Refresh period	tREF		16		16	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	tRASP	60	200K	70	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		ns	
Output data hold time	tDOH	5		5		ns	

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$, $V_{cc} = 5.0\text{V} \pm 10\%$. See notes 1, 2.)

Test condition : $V_{ih}/V_{il} = 2.4\text{V}/0.8\text{V}$, $V_{oh}/V_{ol} = 2.0\text{V}/0.8\text{V}$, Output loading $C_L = 100\text{pF}$

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	15	3	20	ns	6,11,12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	15	3	20	ns	6,11
$\overline{\text{W}}$ to data delay	tWED	15		20		ns	
$\overline{\text{W}}$ pulse width(Hyper Page Cycle)	tWPE	5		5		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
$\overline{\text{CAS}}$ precharge time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20	35	25	40	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA					ns	3
Hyper Page cycle time	tHPC	30		33		ns	13

NOTES

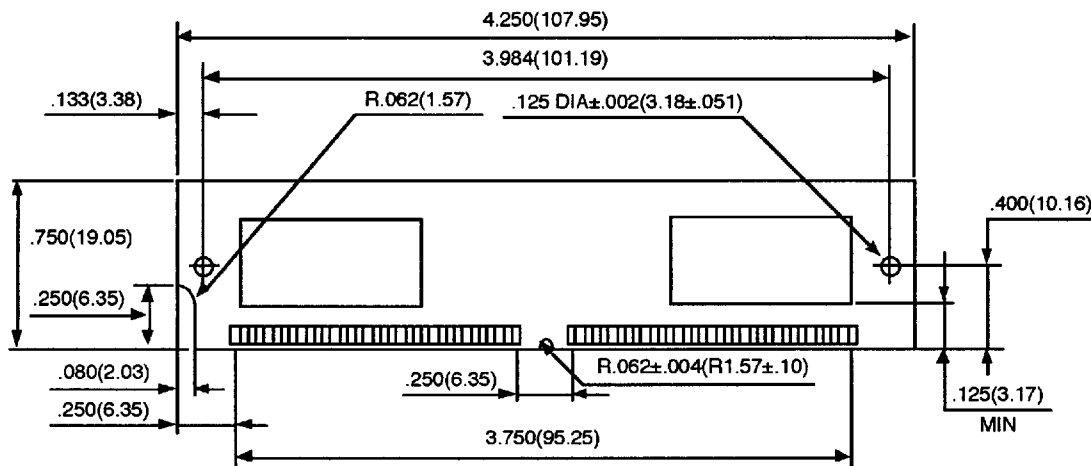
- An initial pause of $200\mu\text{s}$ is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2TTL loads and 100pF.
- Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
- Assumes that tRCD \geq tRCD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- tWCS is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If tWCS \geq tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either tRCH or tRRH must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
- tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
- tASC \geq tCPmin

TIMING DIAGRAM

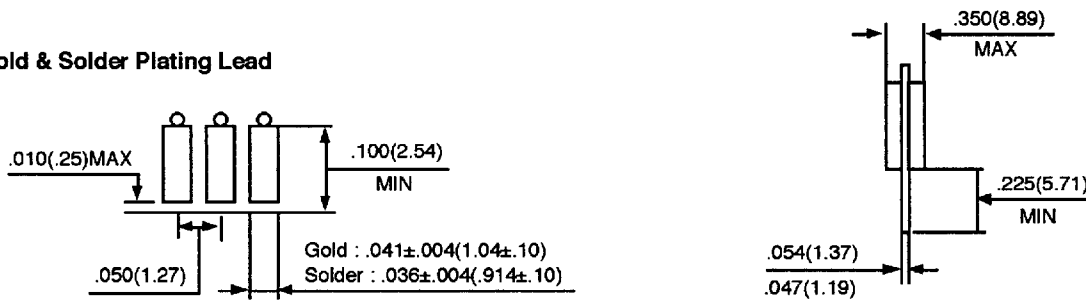
Please refer to attached timing chart (IV) !!!

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Gold & Solder Plating Lead



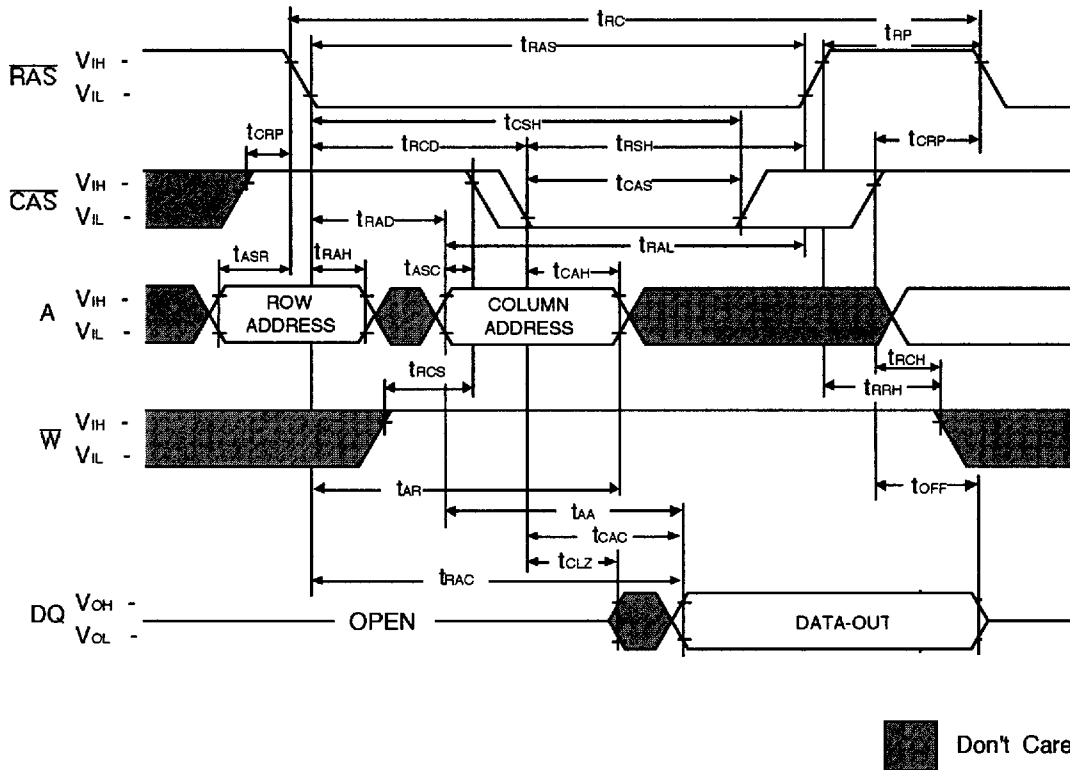
Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 1Mx16 DRAM.
DRAM Part No. : KM416C1204AJ (400 mil)

Revision History
Rev. 0.0. : 23 Dec '94

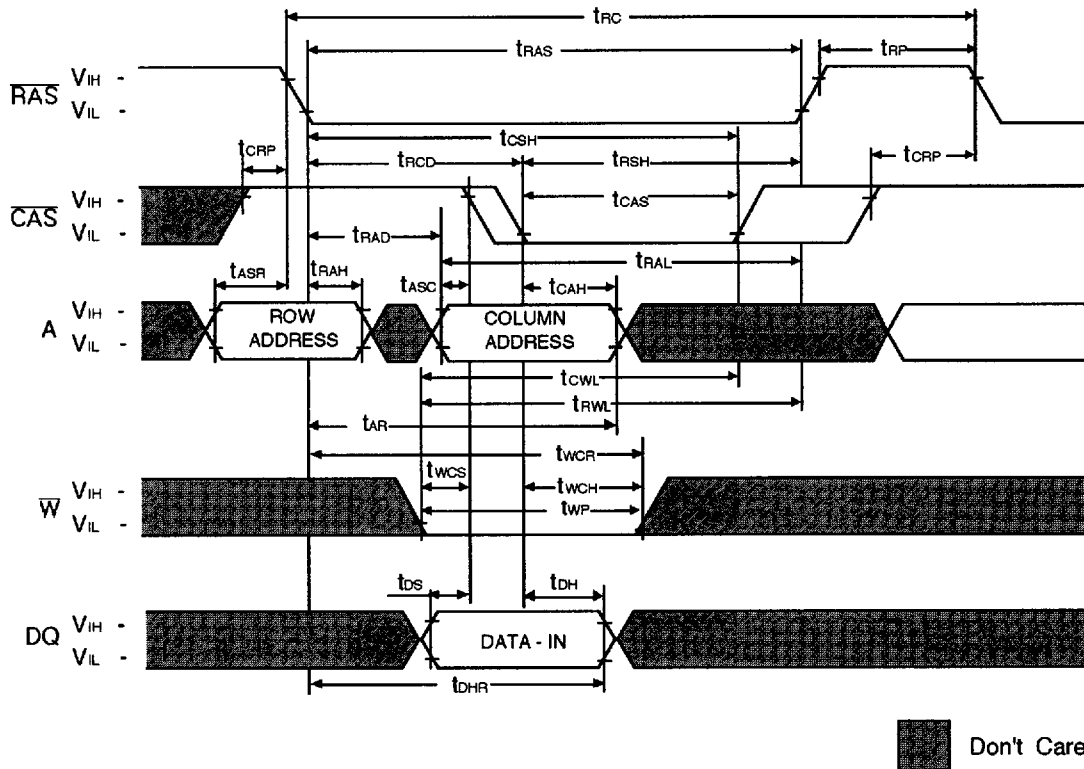
TIMING DIAGRAM

READ CYCLE

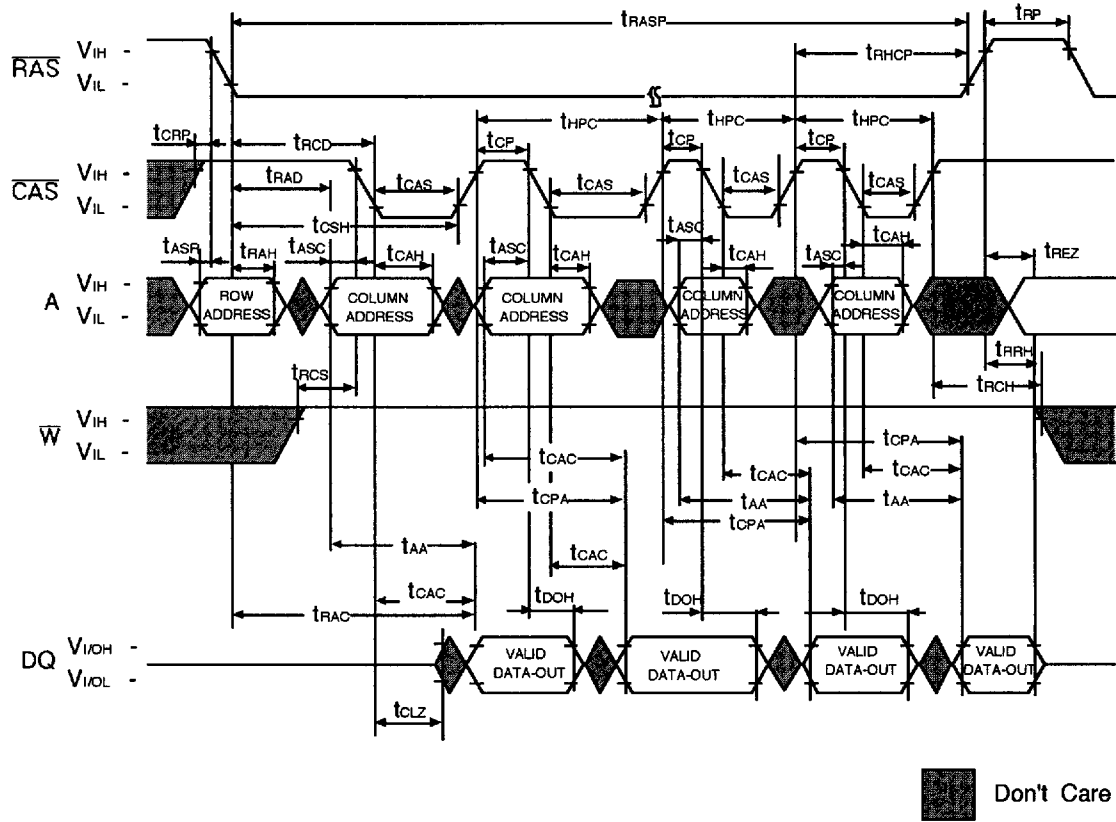


WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN

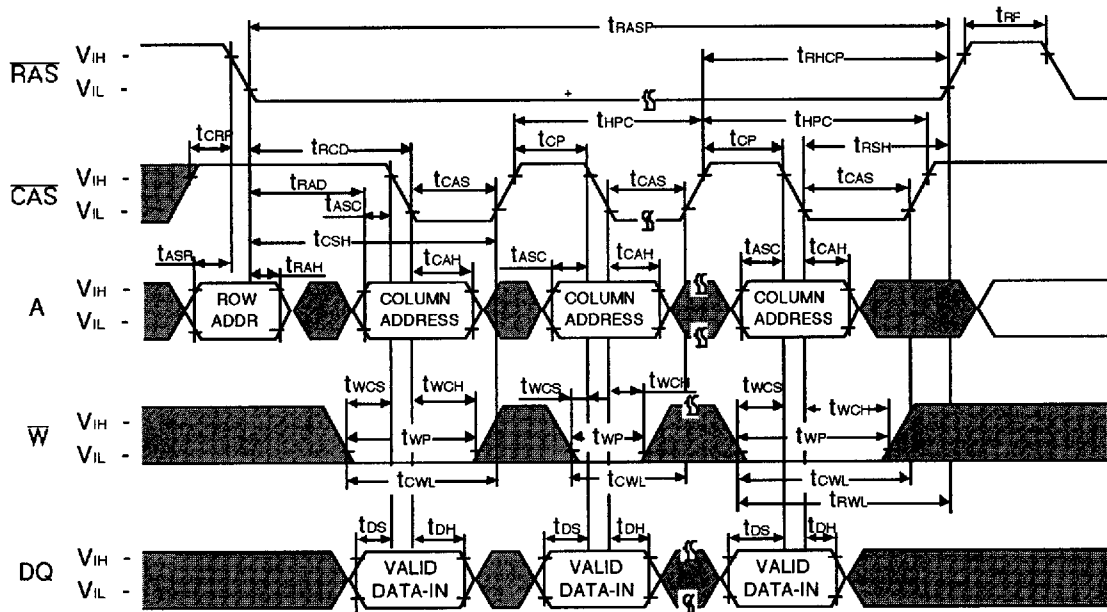


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

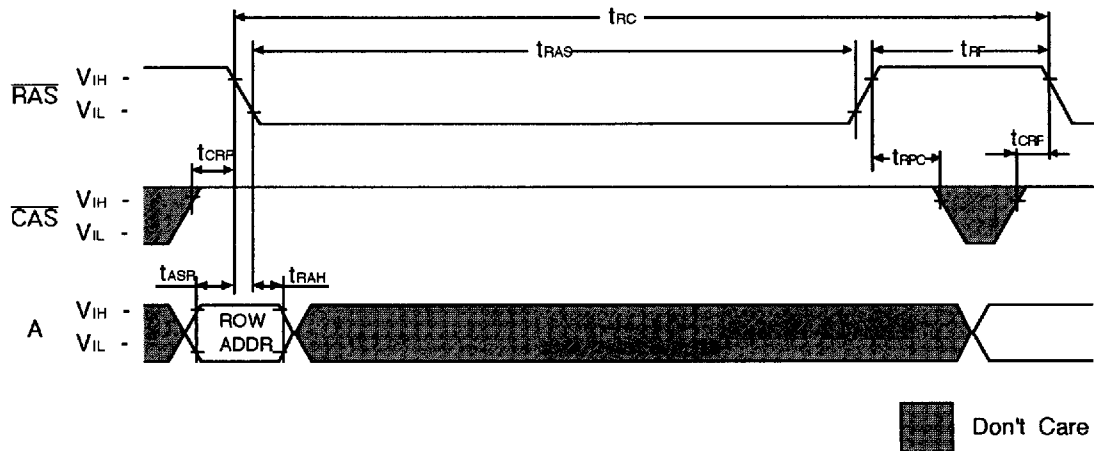
NOTE : D_{OUT} = Open



■ Don't Care

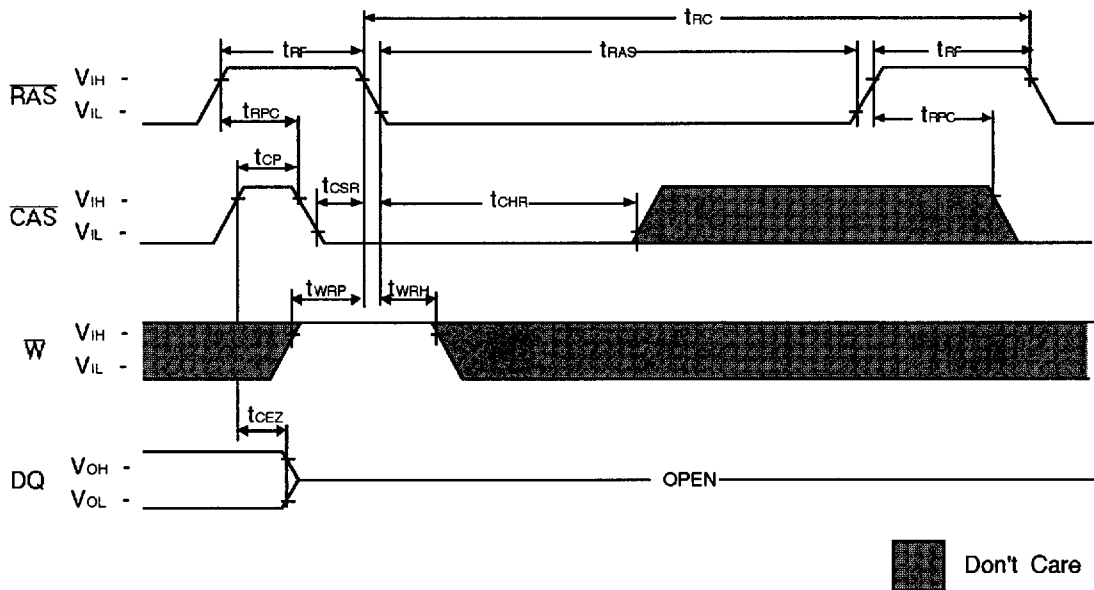
RAS-ONLY REFRESH CYCLE

NOTE : \overline{W} , \overline{OE} , D_{IN} = Don't care
 D_{OUT} = Open

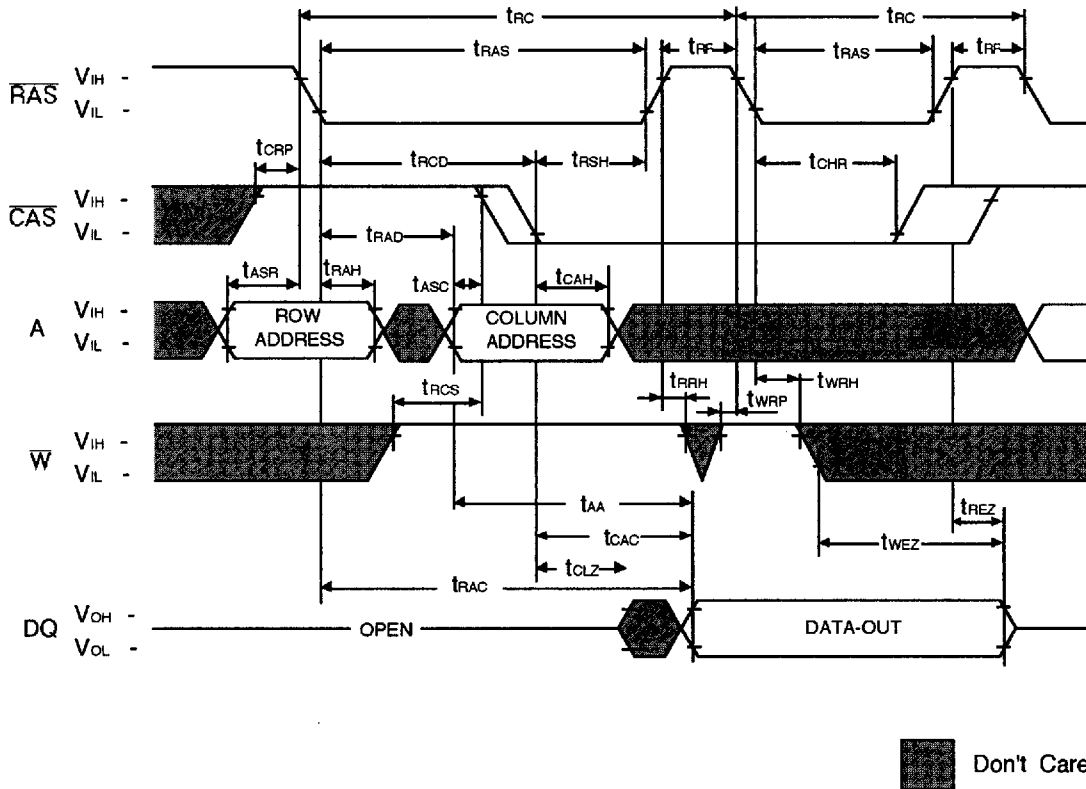


CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \overline{OE} , A = Don't Care

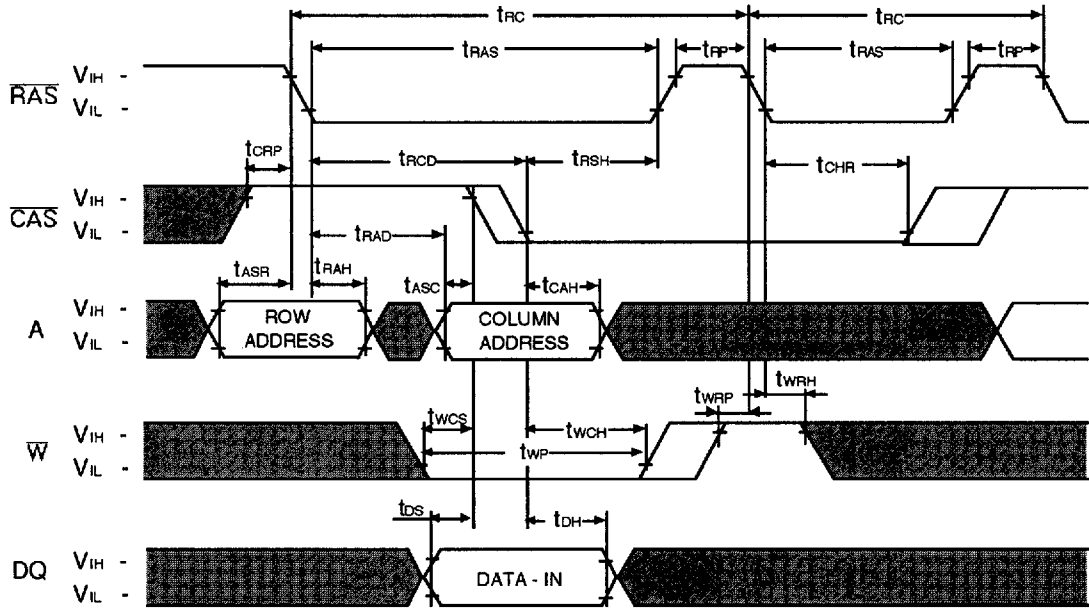


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



■ Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

