Data Book

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Assembly locations: Military products are assembled at SEEQ's offshore (Korea, Philippines, Taiwan) and stateside assembly plants. The assembly plants are identified by a designated alpha code as part of the device backside marking. The alpha codes used are: Korea = K, Philippines = P, Taiwan = T, United States = U.S.A.

Additional copies of this manual or other SEEQ literature may be obtained from:

SEEQ Technology Incorporated
Literature Department
1849 Fortune Drive
San Jose, CA 95131

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SECTION 1

EPROMS

(Erasable Programmable Read Only Memories)

2764 (5133) 64K EPROM
27128 (5143) 128K EPROM

April 1985

Features

- **200 ns Access Times at 0 to 70° C**
- **Programmed Using Intelligent Algorithm**
  - **21 V V_{PP}**
  - **2 Minutes for 27128 (5143)**
  - **1 Minute for 2764 (5133)**
- **JEDEC Approved Bytewide Pin Configuration**
  - **2764 8K x 8 Organization**
  - **27128 16K x 8 Organization**
- **Low Power Dissipation**
  - **100 mA Active Current**
  - **30 mA Standby Current**
- **Extended Temperature Range Available**
- **Silicon Signature™**

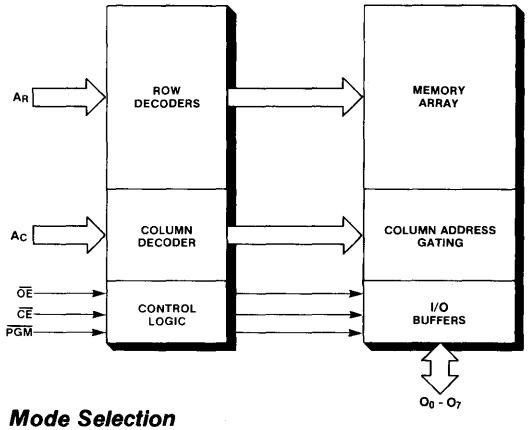
Description

SEEQ's 2764 (5133) and 27128 (5143) are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are pin for pin compatible to JEDEC approved 64K and 128K EPROMs in all operational/programming modes. Both devices have access times as fast as 200 ns over the 0 to 70° C temperature and V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 100 mA and 30 mA respectively. The 200 ns allows higher system efficiency by eliminating the need for wait states in today's 8- or 16-bit microcomputers.

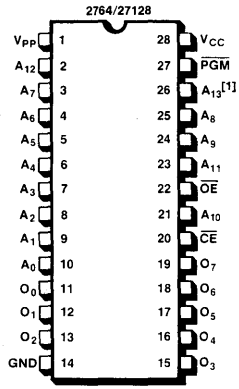
Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{PP} and a TTL "0" to pin 27 (program pin). The 2764 (5133) and 27128 (5143) may be programmed with an intelligent

(continued on page 2)

Block Diagram



Pin Configuration



NOTE 1: PIN 26 IS A NO CONNECT ON THE 2764.

Mode Selection

MODE \ PINS	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

* For Silicon Signature™: A_0 is toggled, A_9 = 12V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

A_C	ADDRESSES — COLUMN (LSB)
A_R	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
PGM	PROGRAM

algorithm that is now available on commercial programmers. The programming time is typically 5 ms/byte or 2 minutes for all 16K bytes of the 27128. The 2764 requires only half of this time, about a minute for 8K bytes. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, both EPROMs may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on SEEQ's EPROMs is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, the product's fab location, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +7V to -0.6V
V_{PP} During Programming with
Respect to Ground ..... +22V to -0.6V
Voltage on A_9 with
Respect to Ground ..... +15.5V to -0.6V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions (27XX = 2764 and 27128)[1]

	27XX-20, 27XX-25 27XX-30, 27XX-45	27XX 27XX-2, 27XX-3, 27XX-4
V_{CC} Supply Voltage[2]	5 V ± 10%	5 V ± 5%
Temperature Range (Read Mode)	0 to 70° C	0 to 70° C
V_{PP} During Programming	21 ± 0.5 V	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[2]	V_{PP} Current	Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	V_{PP} = 21.5V
I_{CC1}[2]	V_{CC} Standby Current			30	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Active Current			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -400 μA

NOTES:
1. The 5133 and 5143 have the same dash numbers and operate with the same operating conditions as the 2764 and 27128 respectively. The specifications are exactly the same.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec) 27XX-2 27XX-20 Min.	27XX-2 27XX-20 Max.	27XX 27XX-25 Min.	27XX 27XX-25 Max.	27XX-3 27XX-30 Min.	27XX-3 27XX-30 Max.	27XX-4 27XX-45 Min.	27XX-4 27XX-45 Max.	Test Conditions
t_{ACC}	Address to Data Valid		200		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		200		250		300		450	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Data Valid		75		100		120		150	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable to Output Float	0	60	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

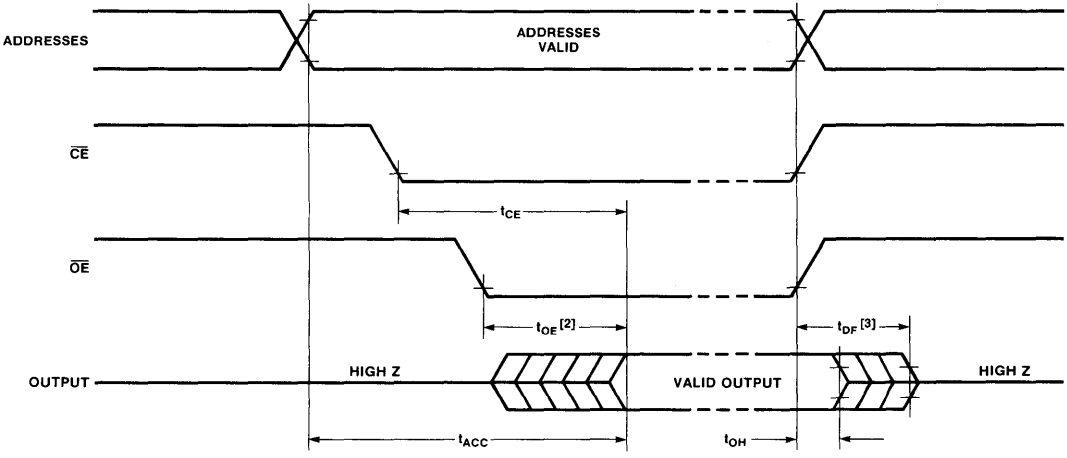
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Erasure Characteristics

The 64K and 128K EPROMs are erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm^2. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer can proceed programming.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column addresses A_0. There are 2 bytes of data available (see Table 2). The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit. This mode is functional at 25 ± 5° C ambient temperature.

Table 2. Silicon Signature Bytes

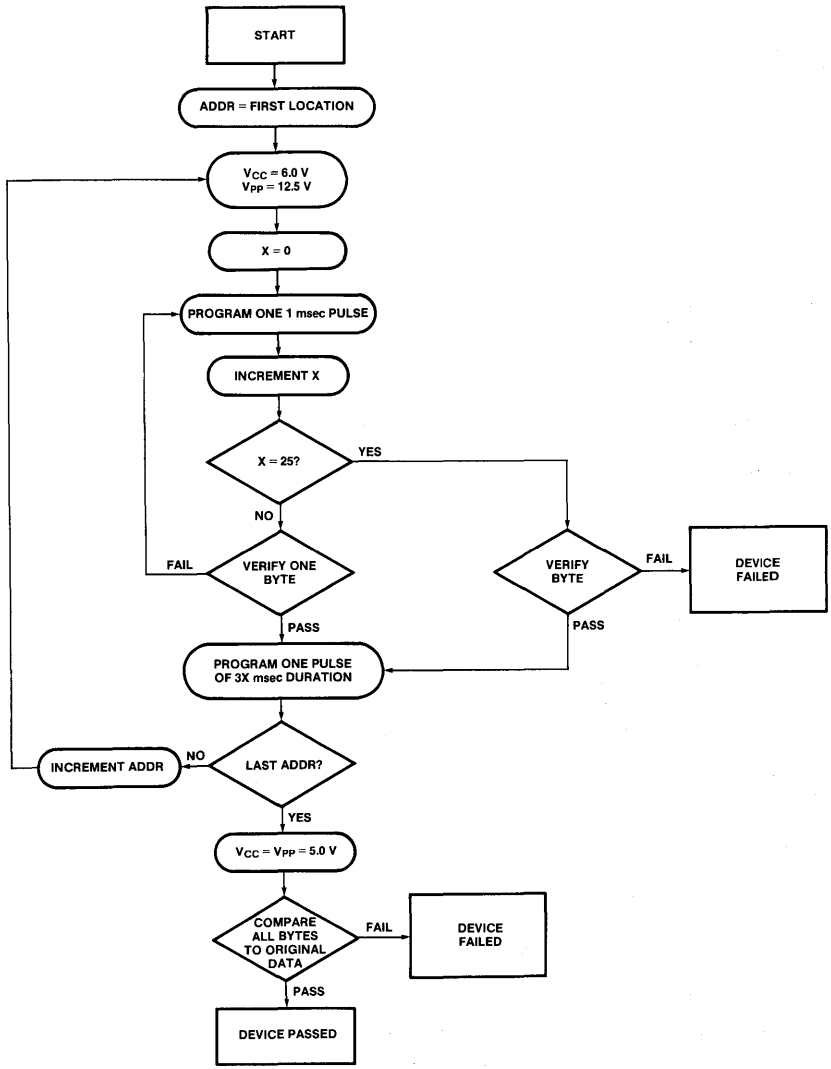
	A_0	Hex Data
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)		
2764	V_{IH}	40
27128	V_{IH}	C1

Programming

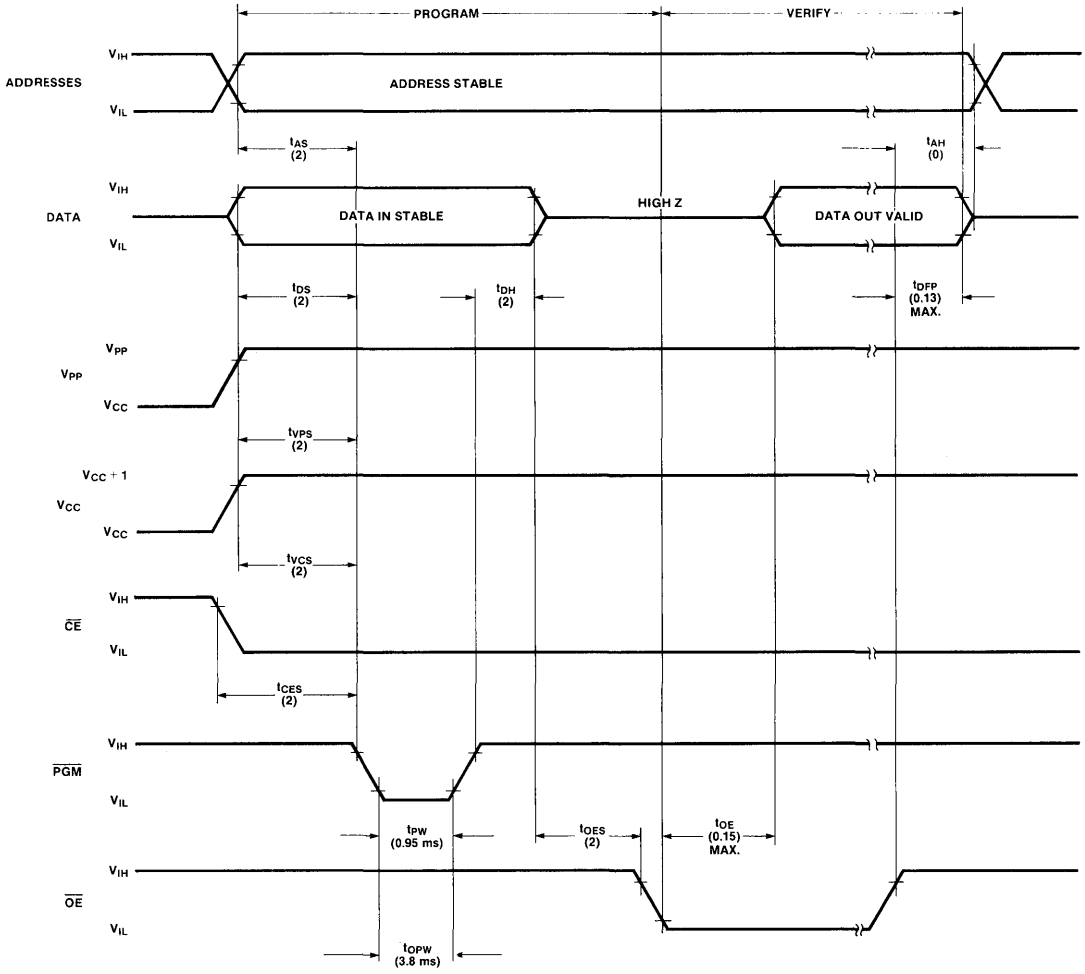
Both EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm. It typically requires only 1 and 2 minute programming time for all 64K and 128K bits respectively.

The intelligent algorithm requires V_{CC} = 6V and V_{PP} = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additional given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5V$.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A V_{IL} AND 2V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

Intelligent Algorithm

AC Programming Characteristics[4] $T_A = 25 \pm 5°C$, V_{CC}[1] = 6.0 V ± 0.25 V, V_{PP} = 21 V ± 0.5 V

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	OE Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}[2]	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3]	$\overline{PGM}$ Overprogram Pulse Width	3.8		63	ms
t_{CES}	$\overline{CE}$ Setup Time	2			μs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Initial Program Pulse width tolerance is 1 msec ± 5%.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, V_{CC} = 5 V ± 5%, T_{PW} = 50 ms ± 10%, and T_{OPW} is not applicable.

*AC Test Conditions

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

Ordering Information

SEEQ's 64K EPROM may be ordered using either the generic product number 2764 or 5133. The package is dual marked with both product numbers. The die, masks, processing, testing, and data sheet specifications are the same. The 5133 is SEEQ's original part number for the 2764 64K EPROM. The same is also true for the 5143 (i.e. 27128) 128K EPROM.

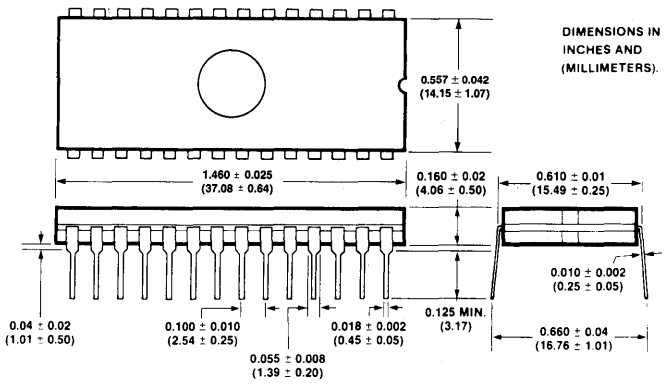
PART NUMBER

D Q 2764 OR D Q 5133 - 25
D Q 27128 - 25 OR D Q 5143 - 25

- ACCESS TIME (BLANK = 250 ns @ 5% V_{CC})
- GENERIC PART NUMBER
- TEMPERATURE: Q = 0 to 70°C
- PACKAGE: D = CERDIP

Package Diagram

28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



27C256
256K CMOS EPROM

August 1985

Features

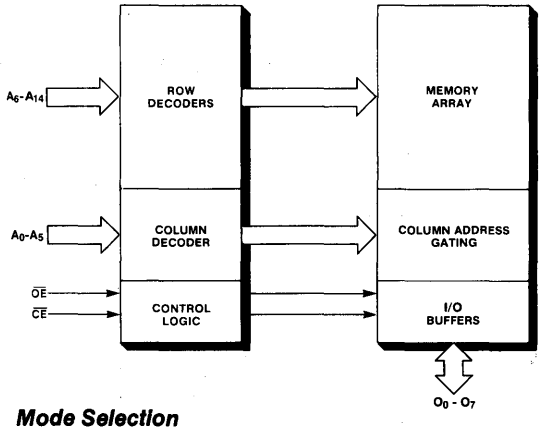
- **256K (32K x 8) CMOS EPROM**
- **Ultra Low Power**
  - **100 μA Max. V_{CC} Standby Current**
  - **40 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **12.5 V_{PP}**
- **250 ns Access Times**
  - **5 V ±10% V_{CC}**
  - **0 to 70° C Temperature Range**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature™**

Description

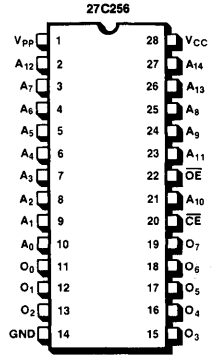
SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its 40 mA active current is less than one half the active power of n-channel EPROMs. In addition the 100 μA V_{CC} standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

The 27C256 is specified over the 0 to 70° C temperature range and at 5 V ± 10% V_{CC}. The access time is specified at 250 ns, making the 27C256 compatible with most of today's microcomputers. Its inputs and outputs are completely TTL compatible.

Block Diagram



Pin Configuration



Mode Selection

MODE \ PINS	CE (20)	OE (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.

*For Silicon Signature™: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5 V V_{PP} and an initial chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +7 V to −0.6 V
V_{PP} with Respect to Ground ..... +14.0 V to −0.6 V
Voltage on A_9 with
Respect to Ground ..... +14.0 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	27C256-25, 27C256-30, 27C256-45	27C256, 27C256-3, 27C256-4
V_{CC} Supply Voltage[1]	5 V ± 10%	5 V ± 5%
Temperature Range (Read Mode)	0 to 70° C	0 to 70° C
V_{PP} During Read[2]	V_{CC}	V_{CC}
V_{PP} During Programming[3]	12.5 ± 0.3 V	12.5 ± 0.3 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}	V_{PP} Current	Read Mode		100	µA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	V_{PP} = 12.5 V
I_{CC1}	V_{CC} Standby Current			100	µA	$\overline{CE} \geq V_{CC}$ -1 V
I_{CC2}	V_{CC} Standby Current			1	mA	$\overline{CE} \geq V_{IH}$
I_{CC3}	V_{CC} Active Current			40	mA	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz, $I_O = 0$
V_{IL}	Input Low Voltage		−0.1	0.8	V	
V_{IH}	Input High Voltage		2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −400 µA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 µF ceramic capacitor on V_{PP} is required during programming only to suppress voltage transients.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec) 27C256 27C256-25 Min.	Max.	27C256-3 27C256-30 Min.	Max.	27C256-4 27C256-45 Min.	Max.	Test Conditions
T_{ACC}	Address to Data Valid		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
T_{CE}	Chip Enable to Data Valid		250		300		450	$\overline{OE} = V_{IL}$
T_{OE}	Output Enable to Data Valid		100		120		150	$\overline{CE} = V_{IL}$
T_{DF}	Output Enable or Chip Enable to Output Float[3]	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
T_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

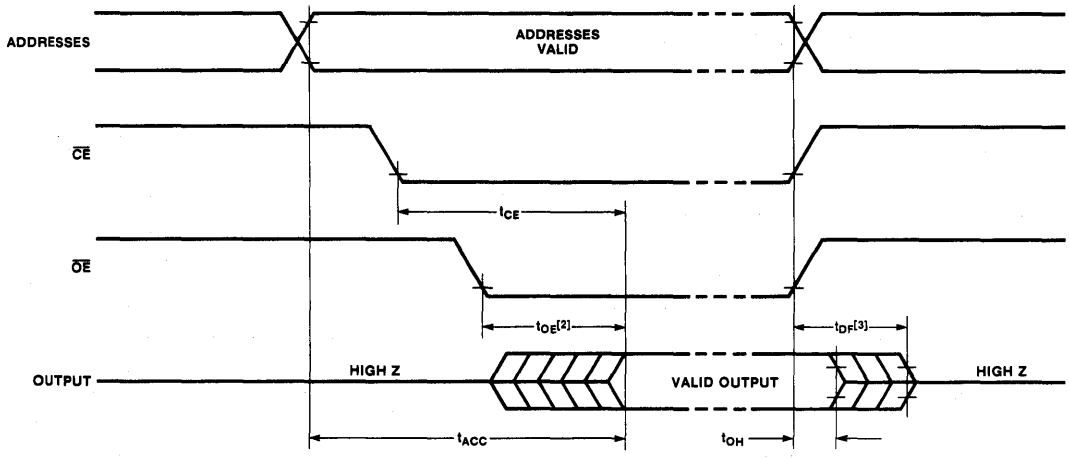
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

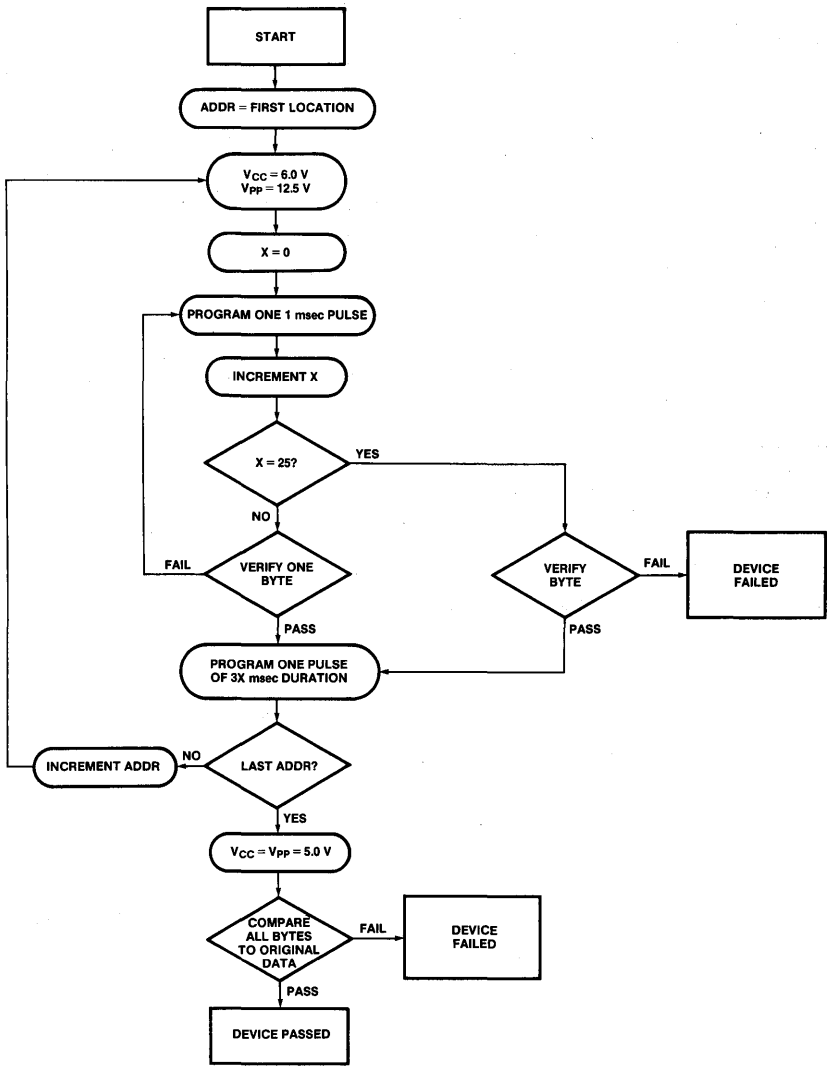
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

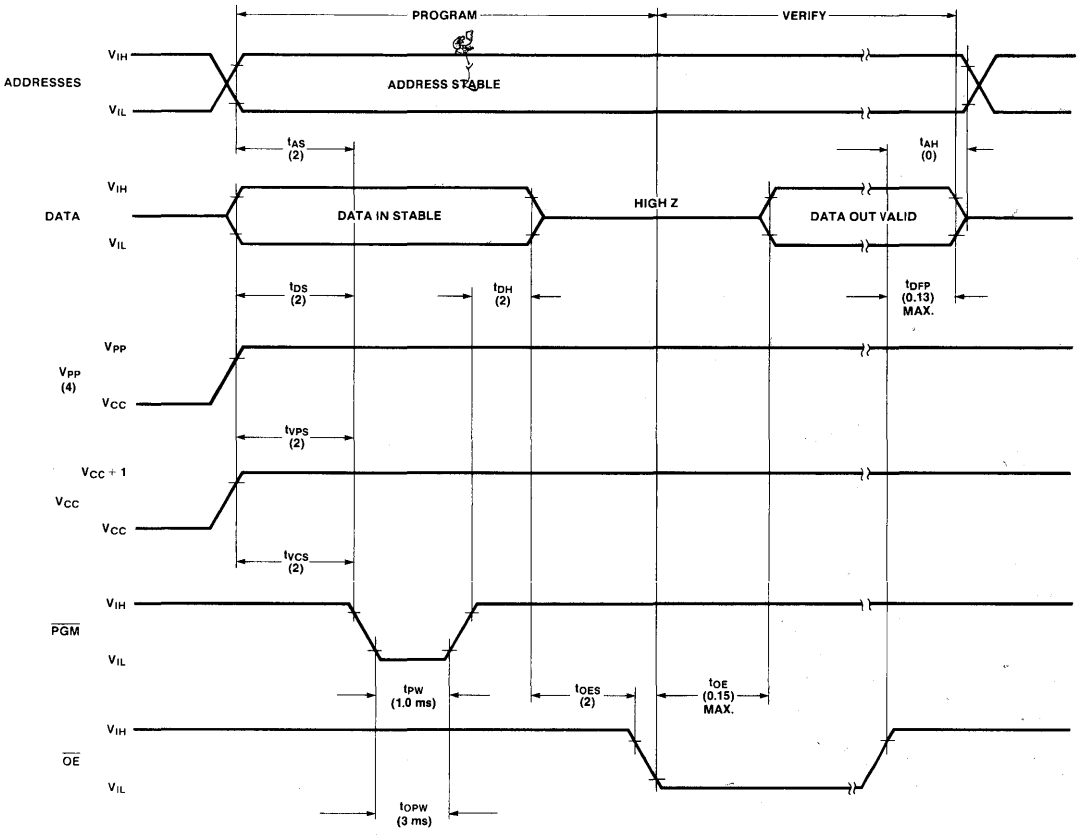
The 27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires $V_{CC} = 6$ V and $V_{PP} = 12.5$ V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5$ V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY TO SUPPRESS VOLTAGE TRANSIENTS.

Intelligent Algorithm

AC Programming Characteristics $T_A = 25 \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$, $V_{PP} = 12.5V$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	$\overline{OE}$ Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*AC Conditions of Test

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

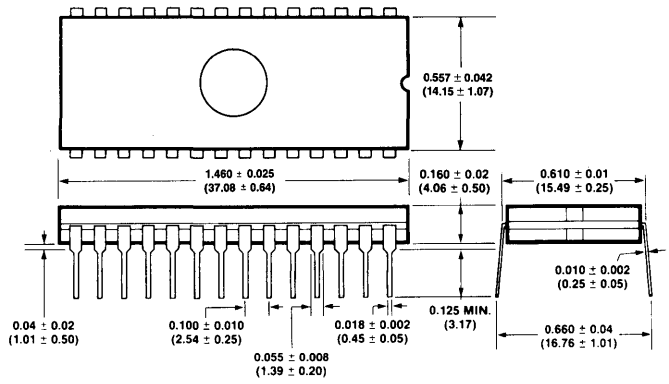
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering and Package Information

D Q 27C256 — XX

- SPEED: BLANK = 250 ns @ 5% V_{CC}; XX = SPEED @ 10% V_{CC}; X = SPEED @ 5% V_{CC}
- GENERIC PART NUMBER
- OPERATING TEMPERATURE RANGE: Q = 0 to 70°C
- PACKAGE TYPE: D = CERDIP

28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

27256
256K EPROM

August 1985

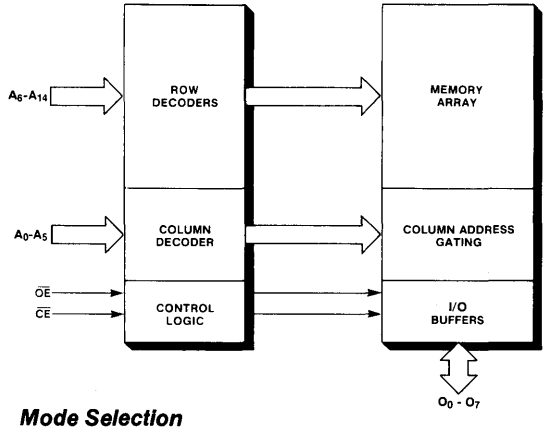
Features

- **256K (32K x 8) EPROM**
- **250 ns Access Times**
  - **5 V ±10% V_{CC}**
  - **0 to 70° C Temperature Range**
- **Low Power**
  - **40 mA Max. V_{CC} Standby Current**
  - **70 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **12.5 V_{PP}**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature™**

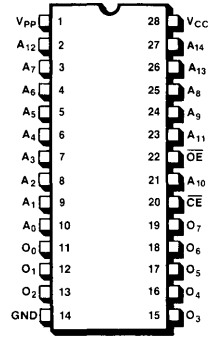
Description

SEEQ's 27256 is a 256K ultraviolet light erasable EPROM. It is organized as 32K x 8, operates from a single 5V supply, and programs using a 12.5V intelligent algorithm. The 27256's operating conditions are specified over the 0 to 70 mA temperature range and at 5V±10% V_{CC}. The active power is only 70 mA, approximately 30% lower than NMOS 256K EPROMs. Consequently, memory system sizes can be increased with a substantial savings in power, resulting in lower power supply cost and inherently greater system reliability. For systems requiring even lower power, a 40 mA active and 100 µA standby power CMOS 27C256 is available from SEEQ. The 27256's low active power is achieved without sacrificing performance. The access time is 200 nsec, making it compatible with most of today's microcomputers. Wait states can be eliminated with the 200 nsec access times.

Block Diagram



Pin Configuration



Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	DOUT
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	DIN
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	DOUT
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.

*For Silicon Signature™: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

An intelligent algorithm is used to program the 27256. Data is programmed using a 12.5V V_{PP} and an initial chip enable pulse of 1 msec. Initially, and after erasure, all bits are in the "1" state. The typically programming time is under five minutes. Programming is available from commercial programmers and is compatible with other 256K EPROM intelligent algorithms.

Incorporated on the 27256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. The product code is used by a programmer to identify the programming algorithm for the 27256.

Absolute Maximum Ratings

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +7 V to −0.6 V
V_{PP} with Respect to Ground ..... +14.0 V to −0.6 V
Voltage on A_9 with
Respect to Ground ..... +14.0 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	27256-20, 27256-25, 27256-30	27256, 27256-2, 27256-3
V_{CC} Supply Voltage[1]	5 V ± 10%	5 V ± 5%
Temperature Range (Read Mode)	0 to 70° C	0 to 70° C
V_{PP} During Read[2]	V_{CC}	V_{CC}
V_{PP} During Programming[3]	12.5 ± 0.3 V	12.5 ± 0.3 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{PP}	V_{PP} Current	Read Mode		100	μA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	V_{PP} = 12.5 V
I_{CO1}	V_{CC} Standby Current			40	mA	$\overline{CE} \geq V_{IH}$
I_{CC2}	V_{CC} Active Current			70	mA	$\overline{CE} = \overline{OE} = V_{IL}$,
V_{IL}	Input Low Voltage		−0.1	0.8	V	
V_{IH}	Input High Voltage		2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −400 μA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 μF ceramic capacitor on V_{PP} is required during programming only to suppress voltage transients.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec) 27C256 27256-20 Min.	27C256 27256-20 Max.	27256 27256-25 Min.	27256 27256-25 Max.	27256-3 27256-30 Min.	27256-3 27256-30 Max.	Test Conditions
T_{ACC}	Address to Data Valid		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
T_{CE}	Chip Enable to Data Valid		250		300		450	$\overline{OE} = V_{IL}$
T_{OE}	Output Enable to Data Valid		100		120		150	$\overline{CE} = V_{IL}$
T_{DF}	Output Enable or Chip Enable to Output Float[3]	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
T_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

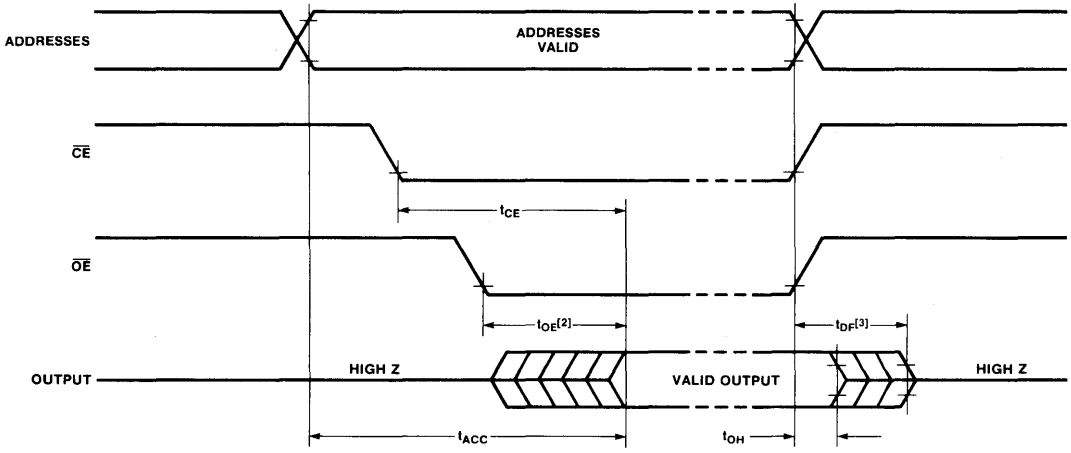
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Erasure Characteristics

The 27256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

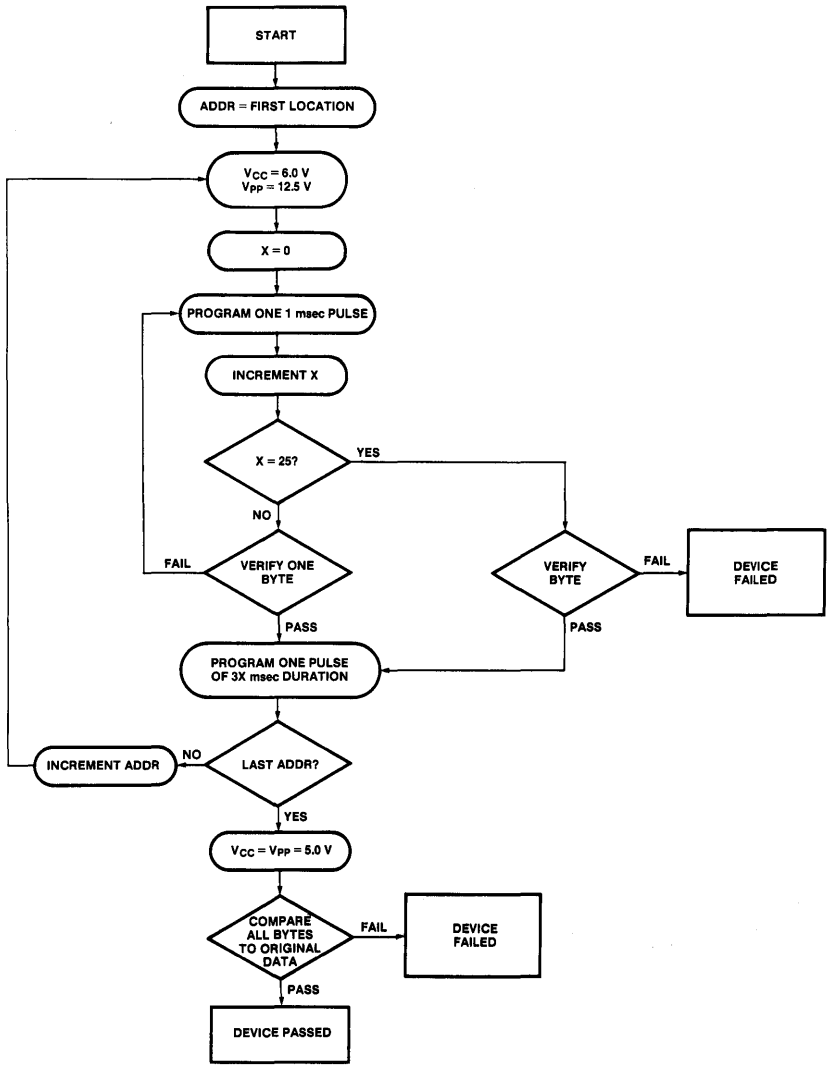
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

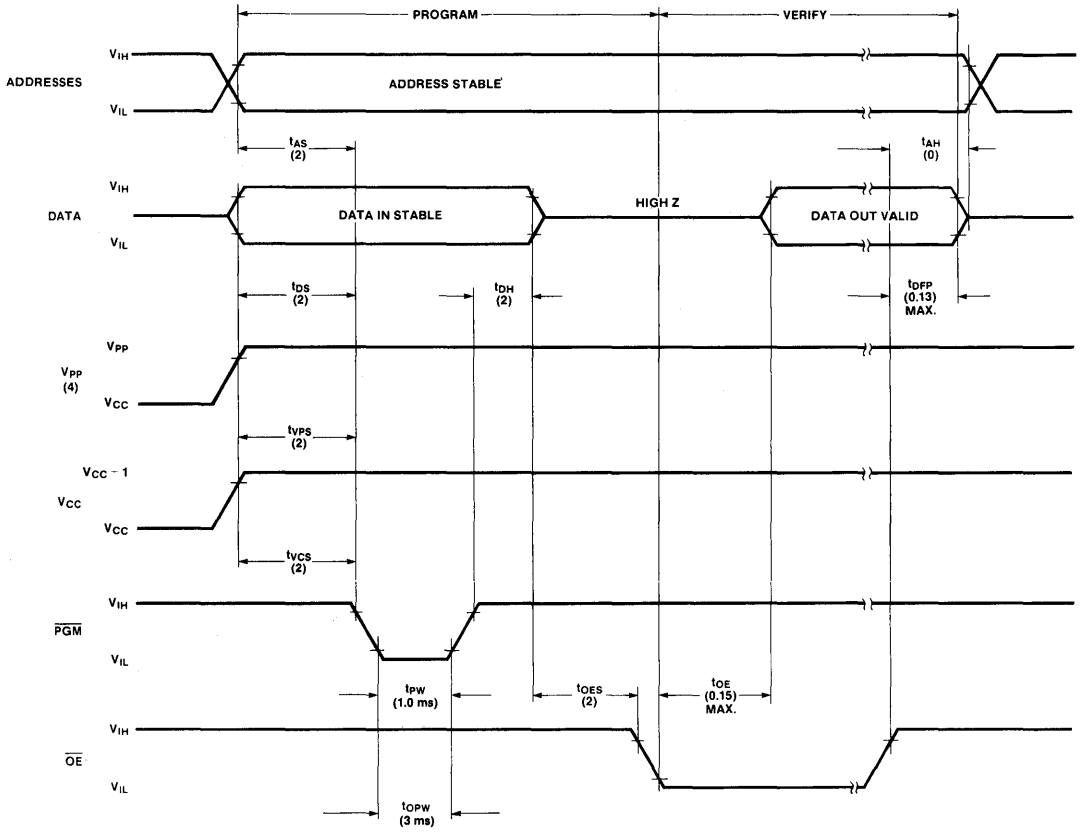
The 27256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires $V_{CC} = 6$ V and $V_{PP} = 12.5$ V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5$ V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY TO SUPPRESS VOLTAGE TRANSIENTS.

Intelligent Algorithm

AC Programming Characteristics $T_A = 25 \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$, $V_{PP} = 12.5V$

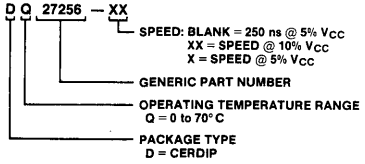
Symbol	Parameter	Limits Min.	Typ.	Max.	Unit
t_{AS}	Address Setup Time	2			μs
t_{OES}	$\overline{OE}$ Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*AC Conditions of Test

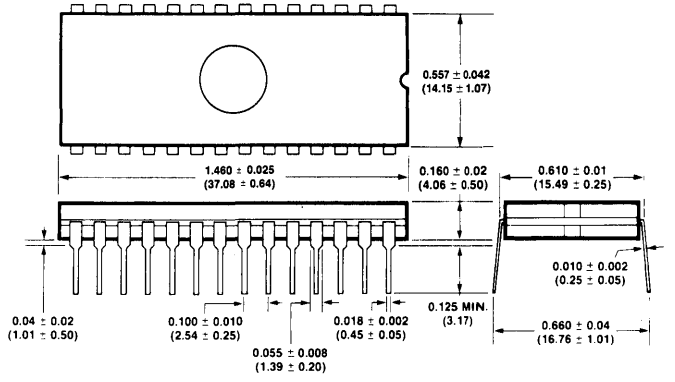
Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering and Package Information



28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

SECTION 2

E²ROMS

(Electrically Erasable Programmable Read Only Memories)

E²ROM CROSS REFERENCE GUIDE

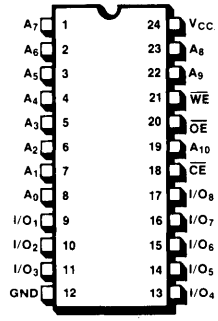
	Features							
Device Type	21 Volt Operation	5 Volt Operation	Latches Only	Latches and Timers	Access Time Faster Than 350 ns	Write Time Faster Than 10 ms	Endurance Higher Than 10,000 Cycles	Nearest SEEQ Equivalent
Intel 2816	X							DQ52B13
Intel 2816A		X						DQ52B13
Intel 2817[1]	X			X				DQ2817A
Intel 2817A[1]		X		X	X			DQ2817A
National 2816	X							DQ2816A
National 2816A		X		X				DQ2816A
Xicor 2816A	X	X		X				DQ2816A
Xicor 2864		X		X				DQ2864
AMD 9864		X		X	X			DQ2864
SEEQ 52B13	X	X	X		X			
SEEQ 2816A	X	X		X	X	X		
SEEQ 2817A		X		X	X	X		
SEEQ 5516A	X	X		X	X	X	X	
SEEQ 5517A		X		X	X	X	X	
SEEQ 52B33		X	X		X	X		
SEEQ 2864		X		X	X	X		

Note:
1. The 2817 and 2817A are supplied in a 28-pin package. All other 16K E²ROMs are in a 24-pin package.

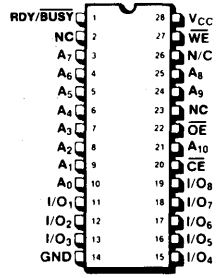
SEEQ's E²ROM Family Configuration

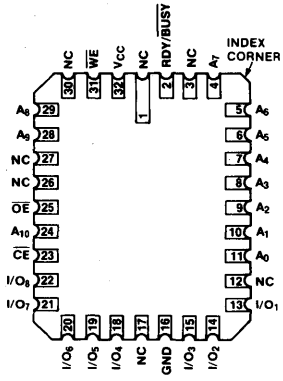
SEEQ's 28XXX family

2816A/5516A

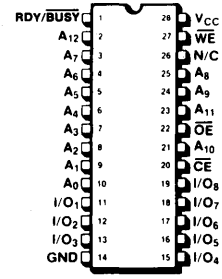


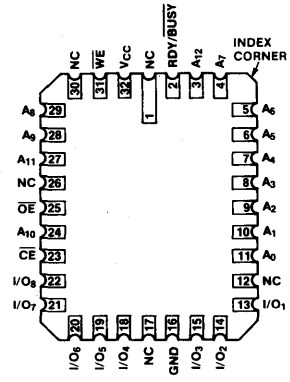
2817A/5517A



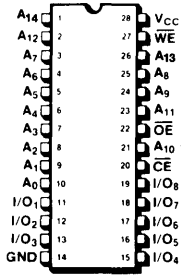


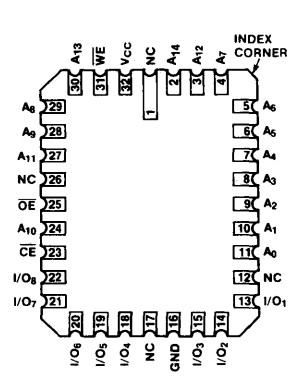
2864/28C64





28C256

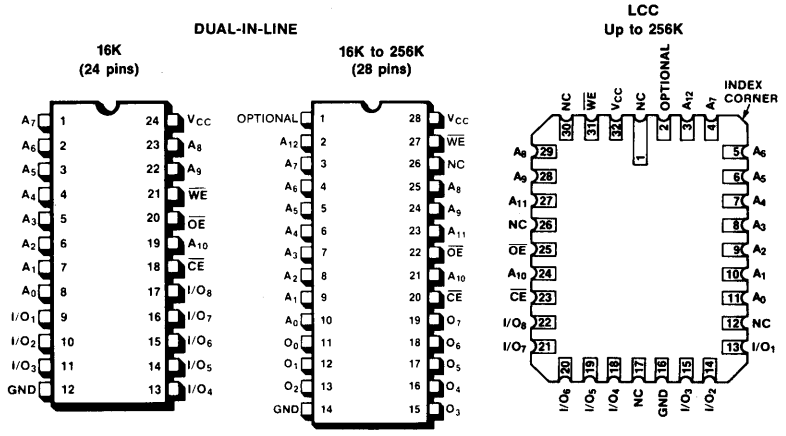




SEEQ's E²ROM Family Configuration

SEEQ's E²ROM family conforms to JEDEC's byte-width pin configuration in both dual-in-line and LCC packages. This allows upgrades from 16K to 256K densities. It should be noted that pin 1 is an optional pin (up to the 256K) used for various E²ROM features such as ready/busy and chip clear.

JEDEC Pin Configuration



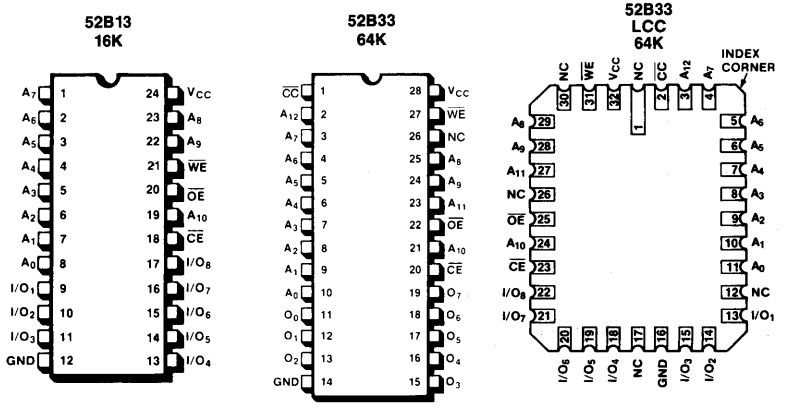
DUAL-IN-LINE

Density \ Pins	1	26
64K	Optional	NC
256K	A14	A13

LCC

Density \ Pins	2	30
64K	Optional	NC
256K	A14	A13

SEEQ's 52BXX family



2816A/5516A
Timer E2
16K Electrical Erasable ROMs

February 1984

Features

- **High Endurance Write Cycles**
  - **5516A: 1,000,000 Cycles/Byte**
  - **2816A: 10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
  - **2 ms Byte Write Time (2816AH)**
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement to 2K x 8 E²ROMs**
  - **21 V 2816**
  - **5 V Timer 2816A**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA max. Active Current**
  - **40 mA max. Standby Current**
- **JEDEC Approved Byte-Wide Pinout**

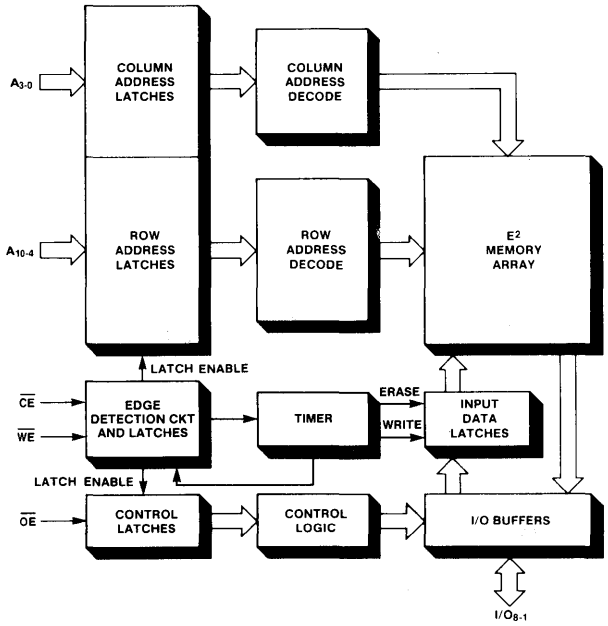
Description

SEEQ's 5516A and 2816A are 5 V only, 2K x 8 electrically erasable read only memories (E²ROMs). E²ROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is ***1 million*** *for the 5516A and 10 thousand for the 2816A. The 5516A's extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride E²ROM process and its innovative "Q cell™" design. The 5516A is ideal for systems that require frequent updates.*

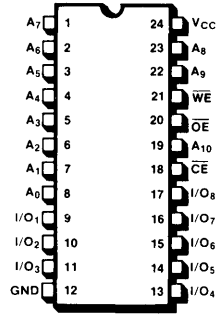
Both E²ROMs have an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The standard 2816A and 5516A's write time is 10 ms. while the

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

2816AH's write time is a fast 2 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

These two timer E²ROMs are ideal for systems with limited board area. For systems where cost is important or higher density is required, SEEQ has a latch only "52B" family at 16K, 32K, and 64K bit densities. The "52B" family has the same JEDEC approved pin configuration but without the on-chip timer. All "52B" family inputs are latched by the falling edge of the write enable signal.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

The chip erase mode clears all data to a TTL high in one 9 ms cycle. This is accomplished by raising both $\overline{WE}$ and $\overline{OE}$ to a high voltage (e.g. 21 V) and having all the data inputs at a TTL high. In addition an optional 21 V byte write (preceded by a byte erase) mode is available.

Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}*	D_{IN}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z
Chip Erase	V_{IL}	V_{ER}	V_{ER}	V_{IH}

*A 21 V input on $\overline{WE}$ is an optional mode.

Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +6V to −0.3V
$\overline{WE}$ During Writing/Erasing with
Respect to Ground ..... +22.5V to −0.3V
Duration of $\overline{WE}$ Supply at 22V
During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Operating Characteristics T_A = 0 to 70° C, V_{CC} = 5 V ±10%, unless otherwise noted.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O's Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode	12	22	V	I_{ER} = 10 μA

AC Characteristics

Read Operation T_A = 0 to 70° C, V_{CC} = 5 V ± 10%, unless otherwise noted

Symbol	Parameter	Limits (ns)						Units
		5516A-250 2816A/2816AH-250		5516A-300 2816A/2816AH-300		2816A-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		ns
t_{CE}	Chip Enable Access Time		250		300		350	ns
t_{AA}	Address Access Time		250		300		350	ns
t_{OE}	Output Enable Access Time		90		100		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		10		ns
t_{HZ}	$\overline{CE}$ to Output in High Z	10	100	10	100	10	100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z	10	100	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	50		50		50		ns
t_{PU}	$\overline{CE}$ to Power-up Time	0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down Time		50		50		50	ns

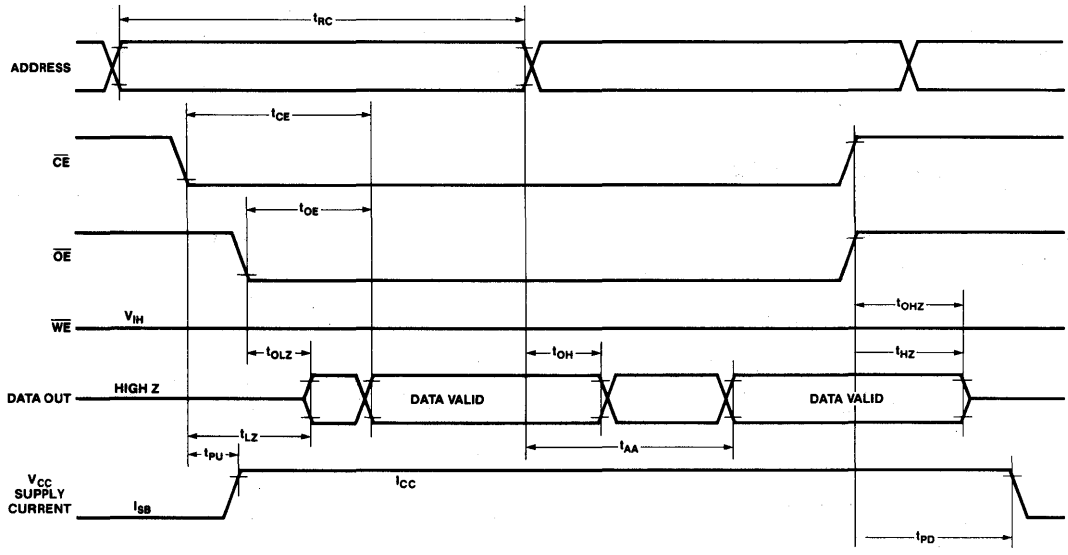
Capacitance T_A = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Cap,	10 pF	$V_{I/O}$ = 0 V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

READ CYCLE TIMING



AC Characteristics

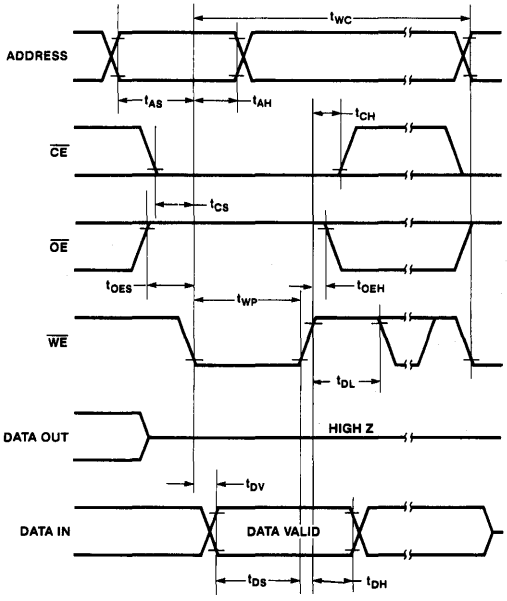
TTL WRITE CYCLE T_A = 0 to 70°C, V_{CC} = 5 V ± 10% unless otherwise noted

Symbol	Parameter		Limits (ns) 5516A-250 2816A/2816AH-250 Min.	Max.	5516A-300 2816A/2816AH-300 Min.	Max.	2816A-350 Min.	Max.	Units
Q	Maximum Number of Write Cycles/Byte	5516A	1,000,000		1,000,000		—		Cycles
		2816A, 2816AH	10,000		10,000		10,000		
t_{WC}	Write Cycle Time	2816AH	2		2		—		ms
		5516A/2816A	10		10		10		
t_{AS}	Address Set Up Time		10		10		10		ns
t_{AH}	Address Hold Time		50		70		70		ns
t_{CS}	Write Set Up Time		0		0		0		ns
t_{CH}	Write Hold Time		0		0		0		ns
t_{CW}	$\overline{CE}$ to End of Write Input		150		150		150		ns
t_{OES}	$\overline{OE}$ Set Up Time		10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time		10		10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width		150		150		150		ns
t_{DL}	Data Latch Time		50		50		50		ns
t_{DV}[2]	Data Valid Time			1		1		1	μs
t_{DS}	Data Set Up Time		20		50		50		ns
t_{DH}	Data Hold Time		20		20		20		ns

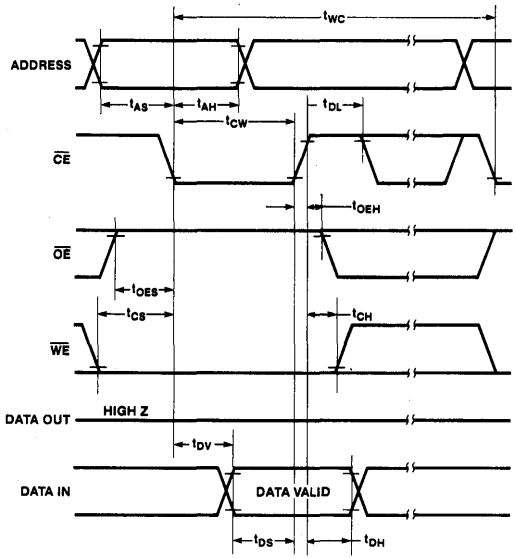
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

TTL Byte Write Cycle

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE

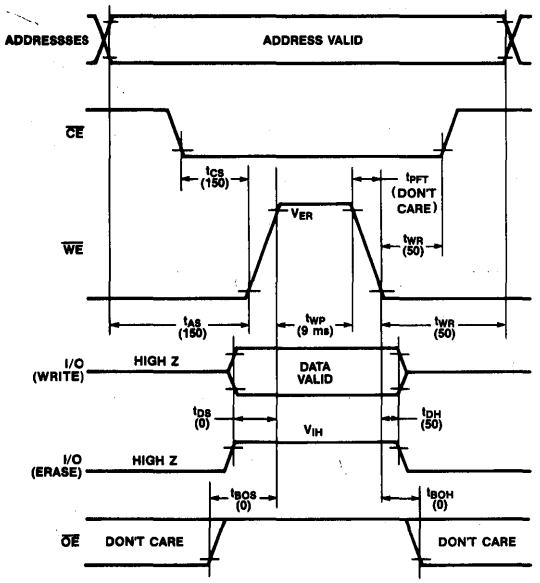


AC Characteristics

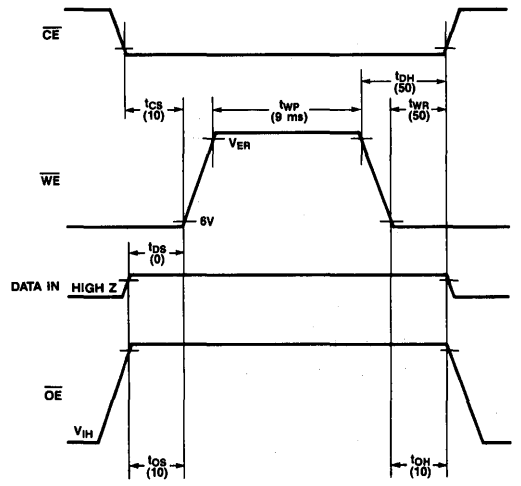
21 V Optional Erase or Write Cycle

(All times shown in parentheses are in ns and are minimum value, unless otherwise noted.)

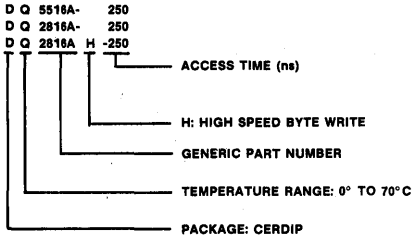
21 V BYTE ERASE OR BYTE WRITE TIMING



21 V CHIP ERASE CYCLE

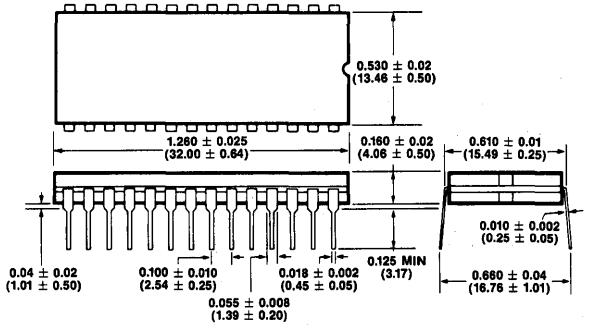


Ordering Information



Package Diagram

24-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

2817A/5517A
Timer E^2
16K Electrical Erasable ROMs

July 1984

Features

- **Ready/Busy Line for End-of-Write**
- **High Endurance Write Cycles**
  - **5517A: 1,000,000 Cycles/Byte**
  - **2817A: 10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
  - **2 ms Byte Write Time (2817AH/5517AH)**
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement for 28 Pin 2K x 8 E^2ROMs**
  - **21 V 2817**
  - **5 V Timer 2817A**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **200 ns max. Access Time**
- **10 Year Data Retention for Each Write**
- **JEDEC Approved Byte-Wide Pinout**

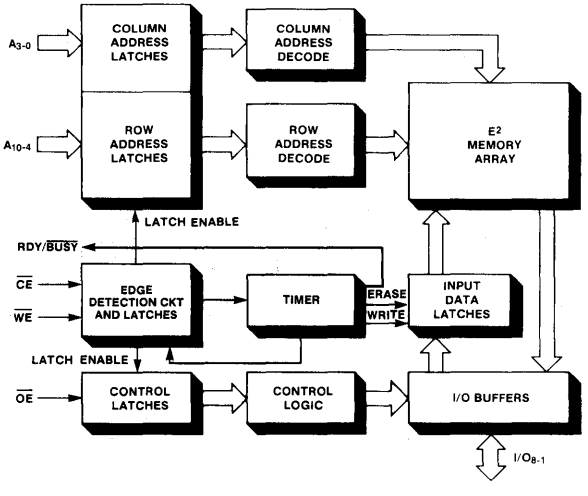
Description

SEEQ's 5517A and 2817A are 5 V only, 2K x 8 electrically erasable read only memories (E^2ROMs). They are packaged in a 28 pin package and have a ready/busy pin. These E^2ROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is 1 million for the 5517A and 10 thousand for the 2817A. The 5517A's extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride E^2ROM process and its innovative "Q cell" design. The 5517A is ideal for systems that require frequent updates and/or high reliability. System reliability is enhanced greatly over lower specified endurance E^2ROMs while still maintaining 10 year data retention.

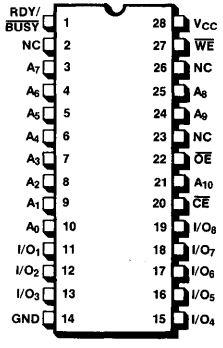
Both E^2ROMs have an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard 5517A/2817A's write time is 10 ms, while the 5517AH/2816AH's write time is a fast 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for either a write or read mode. A byte may be read in 200 ns. The inputs are TTL for both the byte write and read mode.

These two timer E^2ROMs are ideal for systems with limited board area. For systems where cost is important or higher density is required, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
NC	NO CONNECT

automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occured first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Chip Erase	V_{IL}	V_{ER}	V_{ER}	V_{IH}	High Z

Power Up/Down Considerations

The 2817A/5517A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred with V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +6V to -0.3V
$\overline{WE}$ During Writing/Erasing with
Respect to Ground ..... +22.5V to -0.3V
Duration of $\overline{WE}$ Supply at 22V
During W/E Inhibit ..... 24 hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	2817A-200/-250/-300 2817AH-200/-250/-300	5517A-200/-250/-300 5517AH-200/-250/-300	2817A-30
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%	5 V ± 5%
Temperature Range	0° C to +70° C	0° C to +70° C	0° C to +70° C
Q (Maximum Endurance)[2]	10,000 cycles/byte	1,000,000 cycles/byte	10,000 cycles/byte

D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

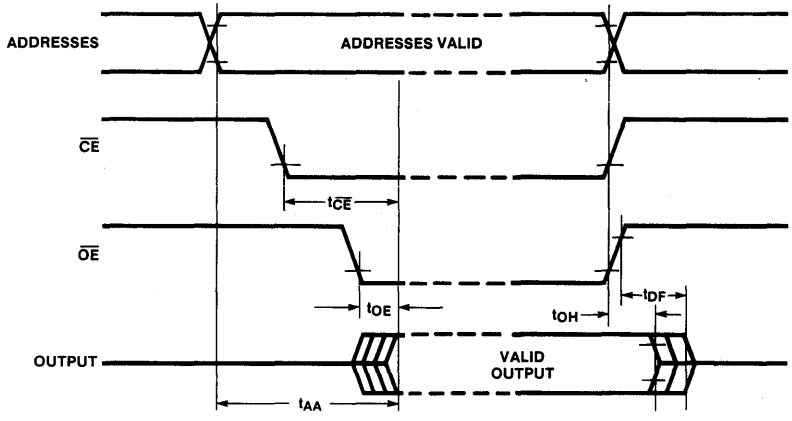
Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 5.5$ V
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = 5.5$ V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{ER}	OE and WE Voltage in Chip Erase Mode	12	22	V	$I_{ER} = 10$ μA

A.C. Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

		Limits (ns)									
		5517AH-200 2817AH-200 5517A-200 2817A-200		5517AH-250 2817AH-250 5517A-250 2817A-250		5517AH-300 2817AH-300 5517A-300 2817A-300		2817A-35			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		75		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



Capacitance $T_A = 25°C$; f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Cap,	10 pF	$V_{I/O} = 0$ V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

A.C. Characteristics

Write Cycle (Over the operating Vcc and temperature range)

		Limits (ns)								
		5517AH-200 2817AH-200 5517A-200 2817A-200		5517AH-250 2817AH-250 5517A-250 2817A-250		5517AH-300 2817AH-300 5517A-300 2817A-300		2817A-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{AS}	Address to Write Set Up Time	10		10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	10		10		10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	100		100		100		100		ns
t_{AH}	Address Hold Time	50		50		50		70		ns
t_{DS}	Data Set Up Time	20		20		50		50		ns
t_{DH}	Data Hold Time	20		20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		50		ns
t_{DV}[2]	Data Valid Time		1		1		1		1	μs
t_{DB}	Time to Device Busy		120		120		120		120	ns

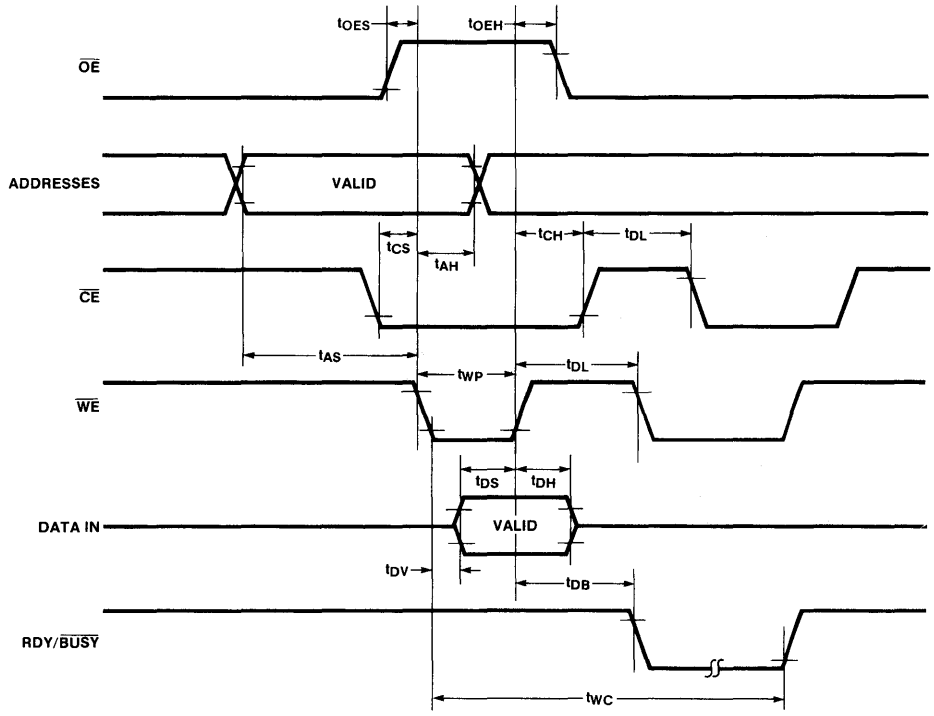
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

A.C. Characteristics

Write Cycle (Over the operating Vcc and temperature range)

		Limits (ns)								
		5517AH		5517A		2816AH		2817A		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WC}	Byte Write Cycle Time		2		10		2		10	ms

Write Cycle Timing



2864/2864H
Timer E^2
64K Electrically Erasable ROMs

PRELIMINARY

August 1985

Features

- **Ready/Busy Pin**
- **High Endurance Write Cycles**
  - **10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
  - **2 ms Byte Write (2864H)**
- **5 V±10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**

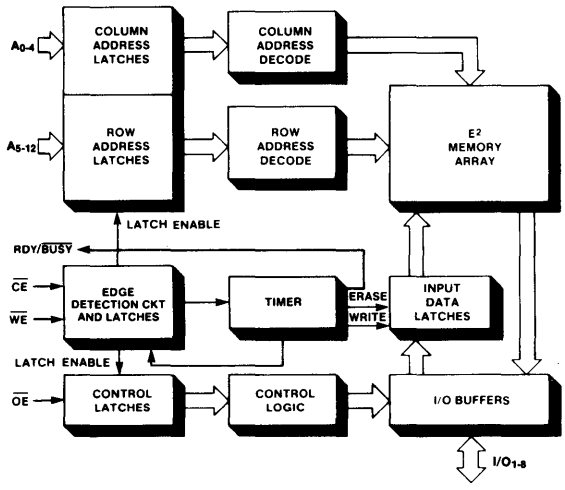
Description

SEEQ's 2864 is a 5 V only, 8K x 8 NMOS electrically erasable read only memory (E^2ROM). It is packaged in a 28 pin package and has a ready/busy pin. This E^2ROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is 10 thousand cycles.

The E^2ROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, a 2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

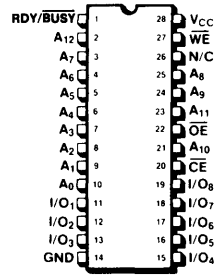
These two timer E^2ROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Block Diagram



Pin Configuration

DUAL-IN-LINE
TOP VIEW



Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-12}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
N/C	NO CONNECT

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	$\overline{I/O}$ (11-13,15-19)	RDY/$\overline{BUSY}$ (1)*
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	High Z

*Pin 1 has an open drain output and requires an external 3K resistor to V_{CC} . The value of the resistor is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

Power Up/Down Considerations

The 2864 has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -10° C to +80° C

All Inputs or Outputs with
Respect to Ground ..... +15 V to -0.3 V
Duration of $\overline{OE}$ Supply at 12 V
During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	2864H-250/H-300 2864-250/-300	2864-35
V_{CC} Supply Voltage	5 V±10%	5 V±5%
Temperature Range	0° C to 70° C	0° C to 70° C
Q (Maximum Endurance)	10,000 cycles/byte	10,000 cycles/byte

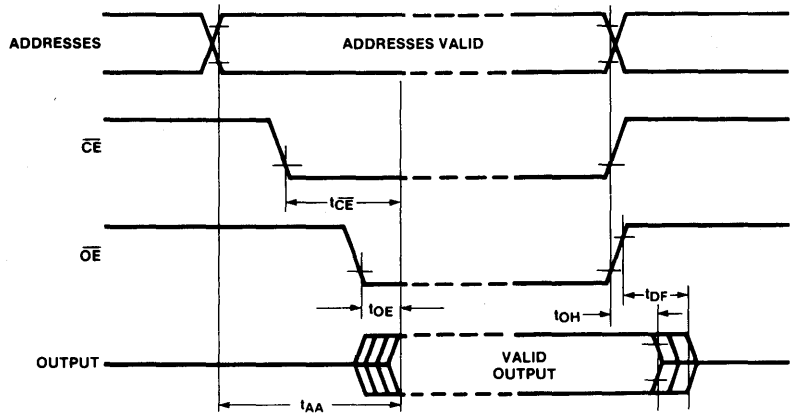
DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA

AC Characteristics Read Operation (Over the operating V_{CC} and temperature range)

		Limits (ns)							
		2864H-250 2864-250		2864H-300 2864-300		2864-35			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



Capacitance T_A[1] = 25°C; f = MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Cap,	10 pF	$V_{I/O}$ = 0 V

AC Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

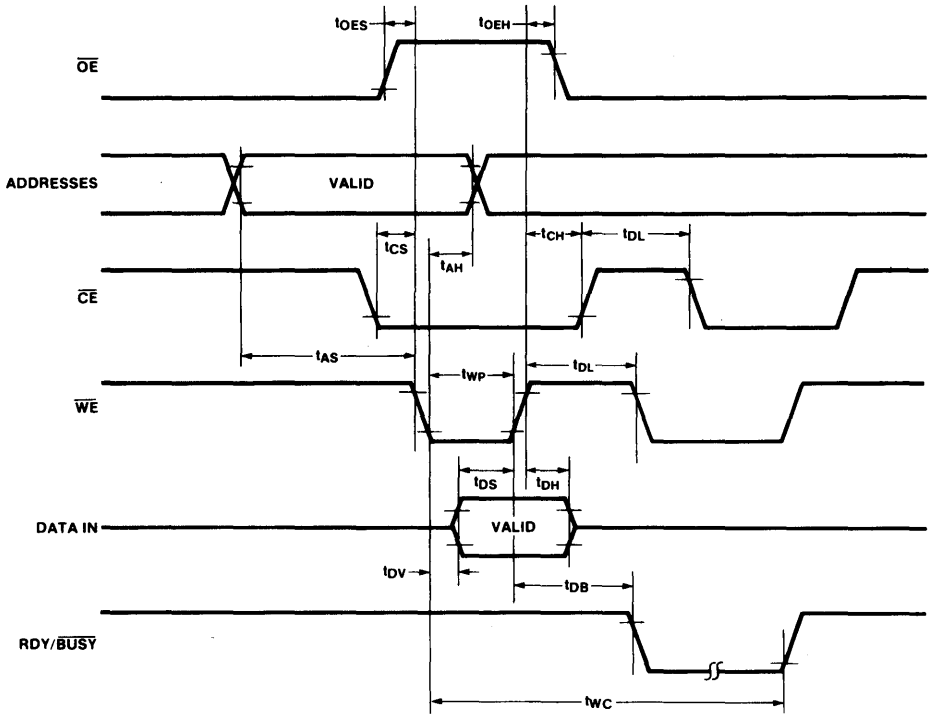
AC Characteristics

Write Cycle (Over the Operating V_{CC} and temperature range)

		Limits						
		2864H-250 2864-250		2864H-300 2864-300		2864-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WC}	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	"H" Family Only		2		2		—	ms
t_{AS}	Address to $\overline{WE}$ Set Up Time	10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	0		0		0		ns
t_{WP}[2]	$\overline{WE}$ Write Pulse Width	150		150		150		ns
t_{AH}	Address Hold Time	50		50		70		ns
t_{DS}	Data Set Up Time	25		25		50		ns
t_{DH}	Data Hold Time	20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		ns
t_{DV}[3]	Data Valid Time		1		1		1	μs
t_{DB}	Time to Device Busy		120		120		120	ns

Notes:
1. This parameter is only sampled and not 100% tested.
2. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 μs maximum after the initiation of a write cycle.

Write Cycle Timing



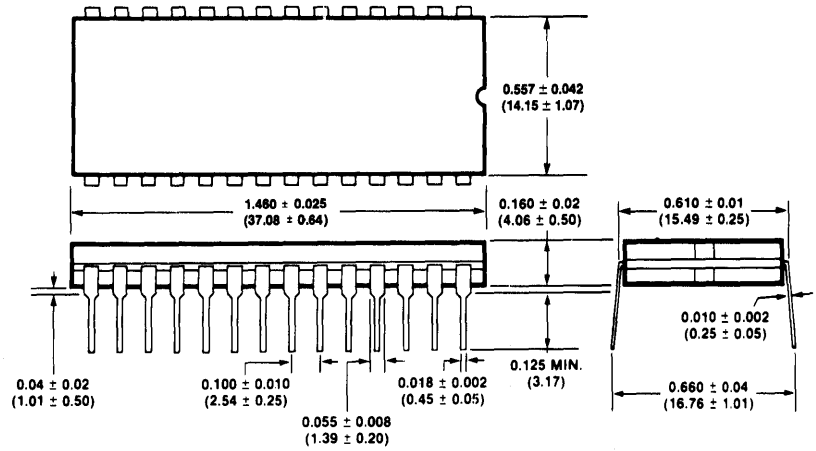
Ordering Information

PART NUMBER **D Q 2 8 6 4 — 250**

PACKAGE TYPE	OPERATING TEMPERATURE RANGE	DEVICE TYPE	WRITE TIME	ACCESS TIME
D= CERDIP	Q = 0° C to + 70° C	2864 = 8K x 8 E²ROM	(BLANK) = 10 ms H = 2 ms	250 = 250 ns 300 = 300 ns

Packaging Information

28-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

52B13/52B13H

E^2

16K Electrically Erasable ROM

August 1984

Features

- *Input Latches*
- *TTL Byte Erase/Byte Write*
- *1 ms (52B13H) or 9 ms Byte Erase/Byte Write*
- *Power Up/Down Protection*
- *10,000 Erase/Write Cycles per Byte*
- *5V ± 10% Operation*
- *Fast Read Access Time — 200 ns*
- *Infinite Number of Read Cycles*
- *Chip Erase and Byte Erase*
- *DiTrace™*
- *JEDEC Approved Byte Wide Memory Pinout*

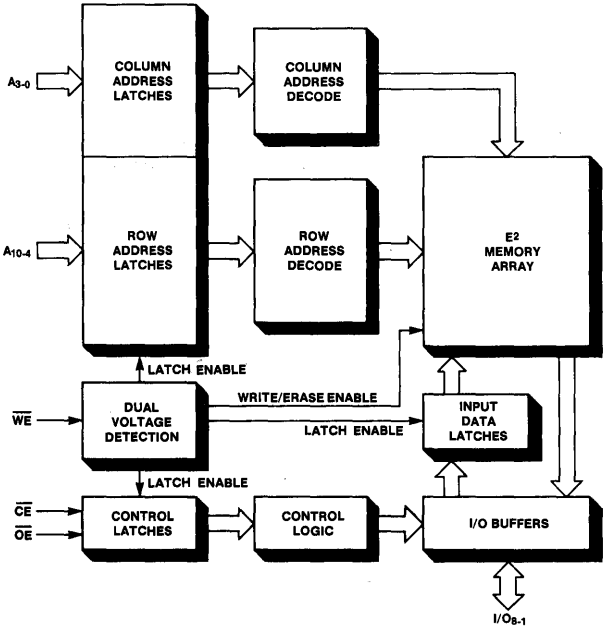
Description

SEEQ's 52B13 and 52B13H are 2048 x 8 bit, 5 volt electrically erasable, read only memories (E^2ROM) with input latches on all address, data and control (chip and output enable) lines. Data is latched and electrically written by either a TTL or a 21V (52B13 only) pulse on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written up to 10,000 times. They are direct pin-for-pin replacement for SEEQ's 5213.

The 52B13 and 52B13H are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications for the 52B13 and 52B13H will be found in military avionics systems, programmable character generators, self-calibrating instruments/

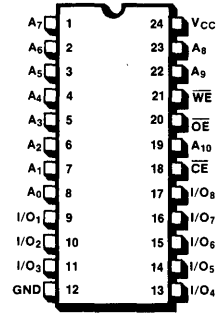
(continued on next page)

Block Diagram



Pin Configuration

52B13/52B13H



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

machines, programmable industrial controllers, and an assortment of other systems. Designing the 52B13 and 52B13H into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance. Extended temperature and military grade versions are available.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1s) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device operates at 5 volts only and the byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation E²ROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal (52B13 only) to be applied to $\overline{WE}$ to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of $\overline{WE}$.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all E²ROMs is that the total number of write and erase cycles is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available t_{CE} time after Chip Enable is applied or t_{ACC} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace™

SEEQ's family of E²ROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection (V_{CC} = 5V ± 10%)

Mode \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

Notes:
1. $\overline{WE}$ may be from V_{IH} to 6V in the read and standby mode.
2. $\overline{WE}$ may be at V_{IL} (TTL W/E Mode) or from 15V to 22V (High Voltage W/E Mode) in the byte erase, byte write, or chip erase mode of the 52B13.

52B13/52B13H Specification Differences

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	52B13		52B13H		Units
		Min.	Max.	Min.	Max.	
t_{WP}	Write Enable Pulse Width					
	Byte Write/Erase	9	70	1	10	ms
	Chip Erase	9	70	9	20	ms
V_{WE}	$\overline{WE}$ Write/Erase Voltage High Voltage Mode	15	22	Not Applicable		V

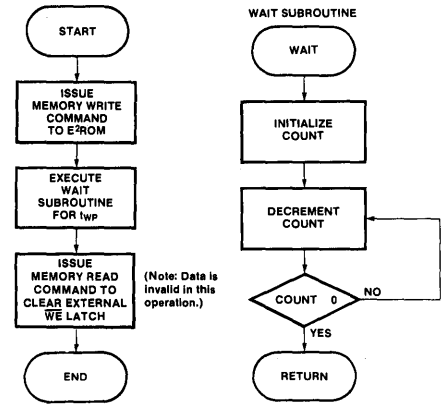
Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

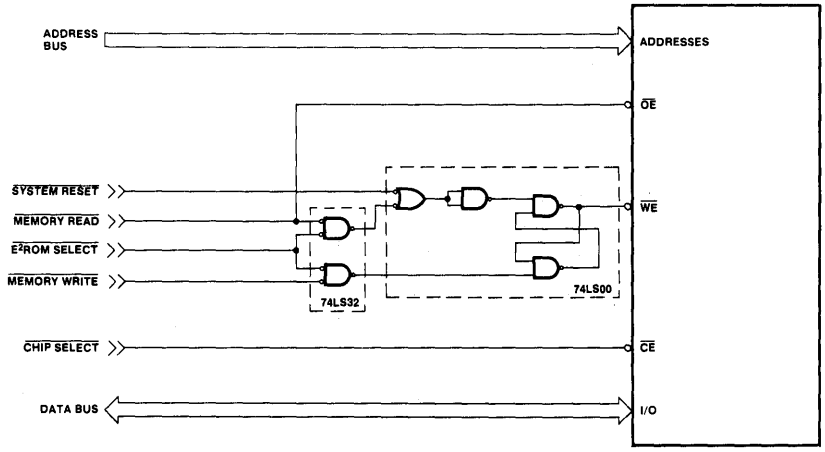
1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Typical E^2ROM Write/Erase Routine



Microprocessor Interface Circuit Example for Byte Write/Erase



Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with Respect to Ground ..... +6V to -0.3V
$\overline{WE}$ During Writing/Erasing with Respect to Ground ..... +22.5V to -0.3V
Duration of $\overline{WE}$ Supply at 22V During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B13-200/-250/-350 52B13H-200/-250/-350
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range	0° C to 70° C
Q (Maximum Endurance)[3]	10,000 cycles/byte

D.C. Operating Characteristics During Read or Write/Erase (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	µA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	µA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	µA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode[2]			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current		15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode[2]	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 µA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0V.
2. Not applicable to 52B13H.
3. Each byte may be written or erased, over the temperature and V_{CC} range, up to the recommended endurance (Q) specification.

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H Min.	52B33 52B33H Max.	Unit	Test Conditions
t_{ACC}	Address to Data Valid	-200		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{CE}	Chip Enable to Data Valid	-200		200	ns	$\overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{OE}[1]	Output Enable to Data Valid	-200	10	80	ns	$\overline{CE} = V_{IL}$
		-250	10	90	ns	
		-350	10	100	ns	
t_{DF}[2]	Output Enable to High Impedance	-200	0	60	ns	$\overline{CE} = V_{IL}$
		-250	0	70	ns	
		-350	0	80	ns	
t_{OH}	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

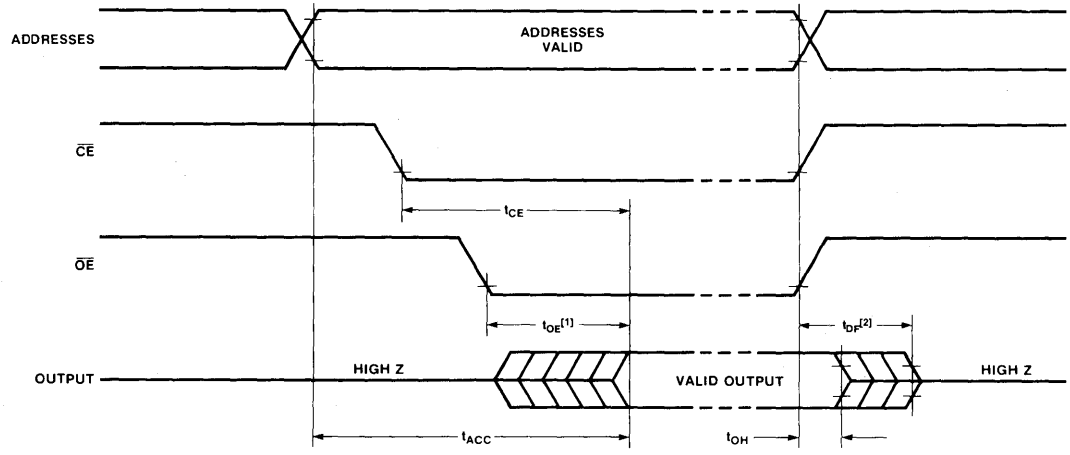
Capacitance[3] $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	10	pF	$V_{OUT} = 0V$
$C_{V_{CC}}$	V_{CC} Capacitance	500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
$C_{V_{WE}}$	V_{WE} Capacitance	10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Read Timing



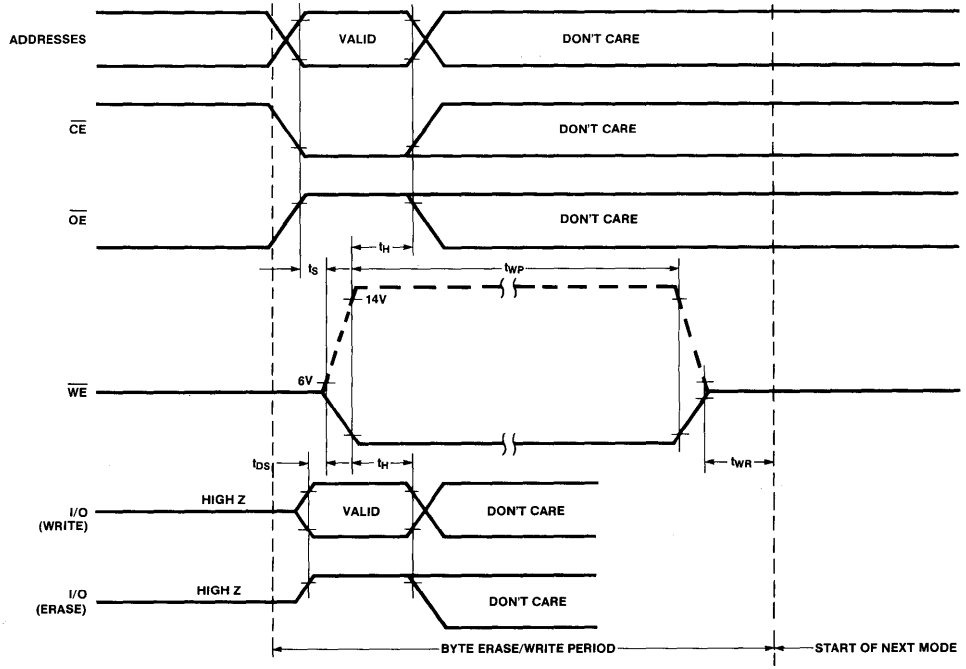
Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.

A.C. Operating Characteristics During Write/Erase (Over the operating V_{CC} and temperature range)

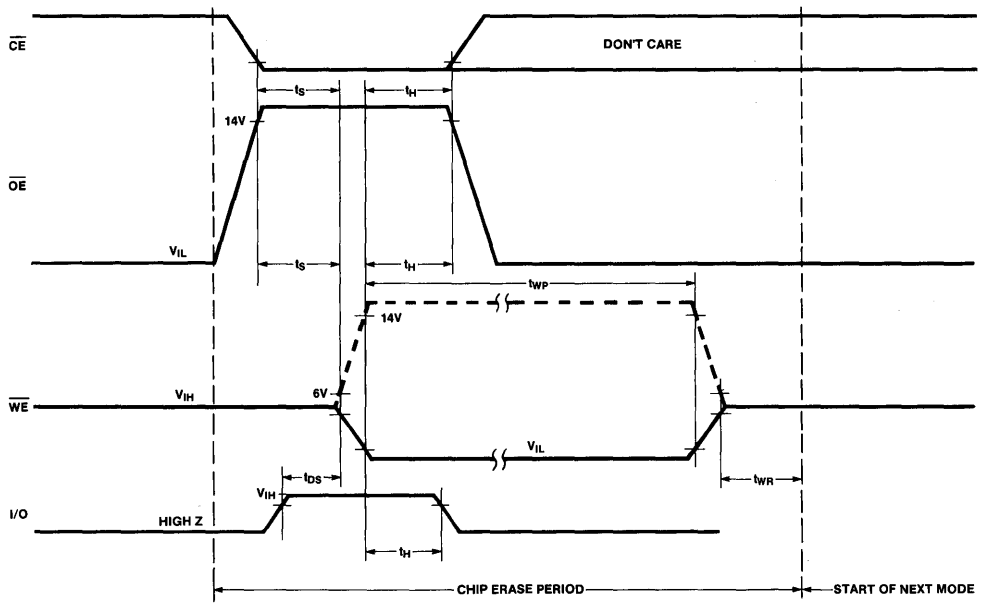
Symbol	Parameter		Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or A_N Setup to WE		50		ns
t_{DS}	Data Setup to $\overline{WE}$		0		ns
t_H[1]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, A_N or Data Change		50		ns
t_{WP}	Write Enable, $\overline{WE}$, Pulse Width	52B13	9		ms
		52B13H	1		ms
t_{WR}[2]	$\overline{WE}$ to Mode Change		50		ns

Notes:
1. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, Address and Data are latched and are "Don't Cares" until t_{WR}, write recovery time, after the trailing edge of $\overline{WE}$.
2. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

Byte Erase or Byte Write Timing



Chip Erase Timing



Ordering and Packaging Information

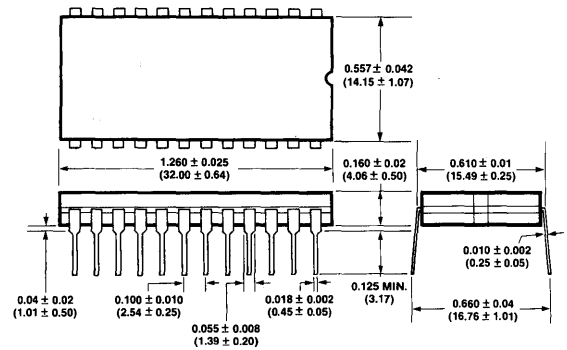
PART NUMBERS

DQ52B13 -350

DQ52B13H -350

- ACCESS TIME (ns)
- 1 ms WRITE TIME AND 5V ONLY
- PRODUCT: 2K x 8 E^2ROM
- TEMPERATURE RANGE: 0° C to 70° C
- PACKAGE: CERDIP

24-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

52B33/52B33H
55B33/55B33H

64K Electrically Erasable E^2ROM

July 1984

Features

- **High Write Endurance Over Temperature Range**
  - **55B33/55B33H; 1,000,000 cycles/byte**
  - **52B33/52B33H; 10,000 cycles/byte**
- **Input Latches**
- **Fast TTL Byte Write Time**
  - **1 ms for 52B33H/55B33H**
  - **9 ms for 52B33/55B33**
- **5 V ± 10% V_{CC}**
- **Power Up/Down Protection**
- **200 ns Read Access Time**
- **DiTrace™**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**

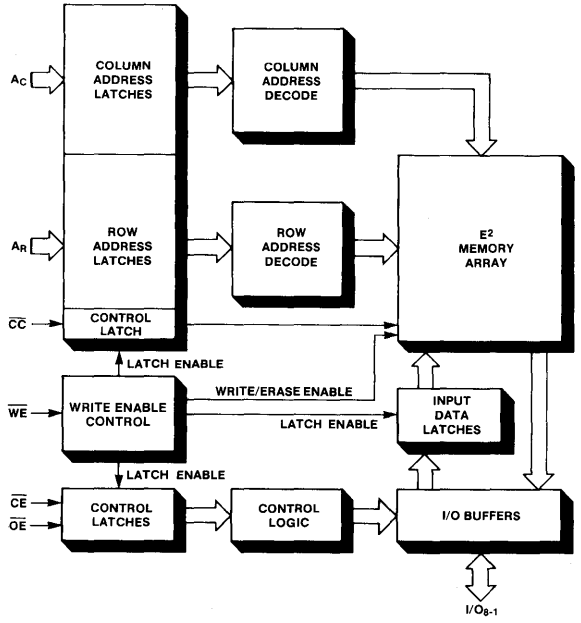
Description

SEEQ's 52B33 and 55B33 are 8196 x 8 bit, 5 volt electrically erasable, read only memories (E^2ROM) which are specified over a 0° C to 70° C temperature range. The 55B33 has a 1,000,000 cycle endurance specification and operates exactly like the 10,000 cycle 52B33. It is ideal for applications requiring frequent writes or where high reliability is needed. The 55B33 gives at least a factor or more improvement in reliability over 10,000 cycle specified E^2ROMs. Data retention for both devices is 10 years.

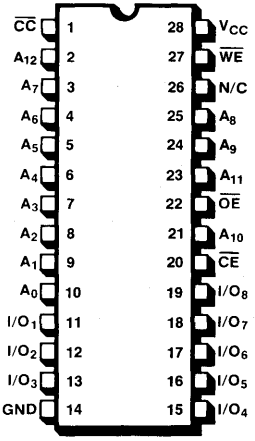
Both products have input latches on all addresses, data, and control (chip and output) lines. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written up to the specified endurance limit of 10,000

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A_C	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

or 1,000,000 times. For applications requiring a faster byte write or erase time, a 52B33H or 55B33H is available at 1 ms, giving a 10 times speed increase.

The pin configuration is to the JEDEC approved byte wide memory pinout. E²ROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by E²ROMs. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other systems. Designing the E²ROMs into these systems is simplified because of the fast access time and input latches. The specified 200 ns access time eliminates or reduces the number of microprocessor wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B33 and 55B33H have six modes of operation (see Table 1) and require only TTL inputs to operate these modes. The "H" members of the family operate in the same manner as the other devices except for a faster write enable pulse width of 1 ms is specified during byte erase or write.

Read

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is bought to a TTL low in order to enable the chip. The write enable ($\overline{WE}$) pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Write

To write in to a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then bought to a TTL low level to latch all the inputs and I/O lines. All inputs can be released after the write enable hold time (t_H) and the next input conditions can be established while the byte is being erased. During this operation, the write enable must be held at a TTL low for 9 ms (t_{WP}). A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H and the 55B33H performs the same as the 52B33/55B33 except that the byte erase/byte write time has been enhanced to 1 ms.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

DiTrace™

SEEQ's family of E²ROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Power Up/Down Considerations

SEEQ's "52B" E² family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

Absolute Maximum Stress Rating*

Temperature
Storage ..... −65° C to +100° C
Under Bias ..... −10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +7V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B33-200/-250/-350 52B33H-250	55B33-250 55B33H-250	52B33-35
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%	5 V ± 5%
Temperature Range	0° C to 70° C	0° C to 70° C	0° C to 70° C
Q (Maximum Endurance)[1,2]	10,000 cycles/byte	1,000,000 cycles/byte	10,000 cycles/byte

D.C. Operating Characteristics During Read or Erase/Write (Over the operating V_{CC} and temperature range)

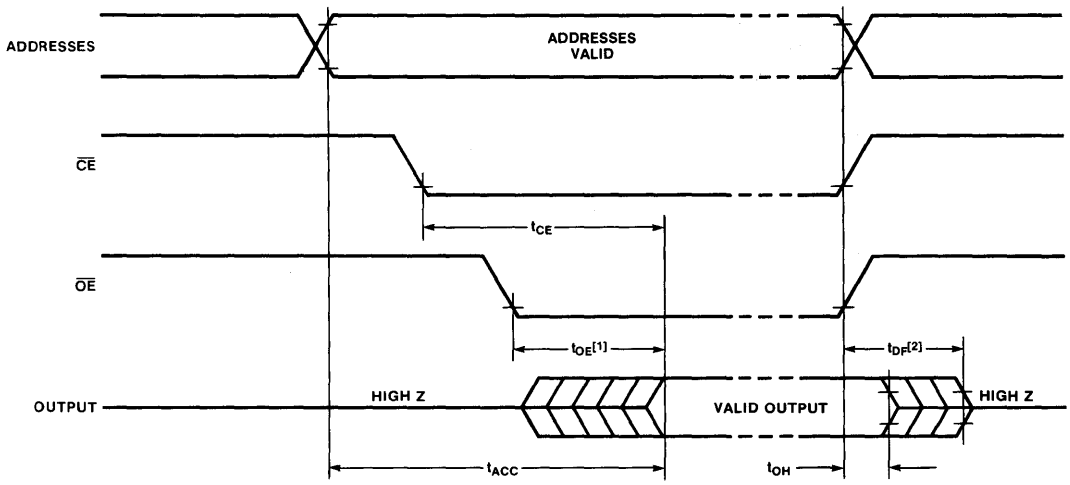
Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage			10	μA	$\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		18	40	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		60	110	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0 V
2. Each byte may be written or erased, over the temperature and V_{CC} range, up to the recommended endurance (Q) specification.

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H Min.	52B33 52B33H Max.	55B33 55B33H Min.	55B33 55B33H Max.	Unit	Test Conditions
t_{ACC}	Address to Data Valid	-200		200		—	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250		250		250	ns	
		-350/-35		350		—	ns	
t_{CE}	Chip Enable to Data Valid	-200		200		—	ns	$\overline{OE} = V_{IL}$
		-250		250		250	ns	
		-350/35		350		—	ns	
t_{OE}[1]	Output Enable to Data Valid	-200	10	80	—	—	ns	$\overline{CE} = V_{IL}$
		-250	10	90	10	90	ns	
		-350/35	10	100	—	—	ns	
t_{DF}[2]	Output Enable to High Impedance	-200	0	60	—	—	ns	$\overline{CE} = V_{IL}$
		-250	0	70	0	70	ns	
		-350/35	0	80			ns	
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[3]	Input and Output Capacitance	All		10		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$

Read Cycle Timing



Notes:

1. $\overline{OE}$ may be delayed to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.
4. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
5. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

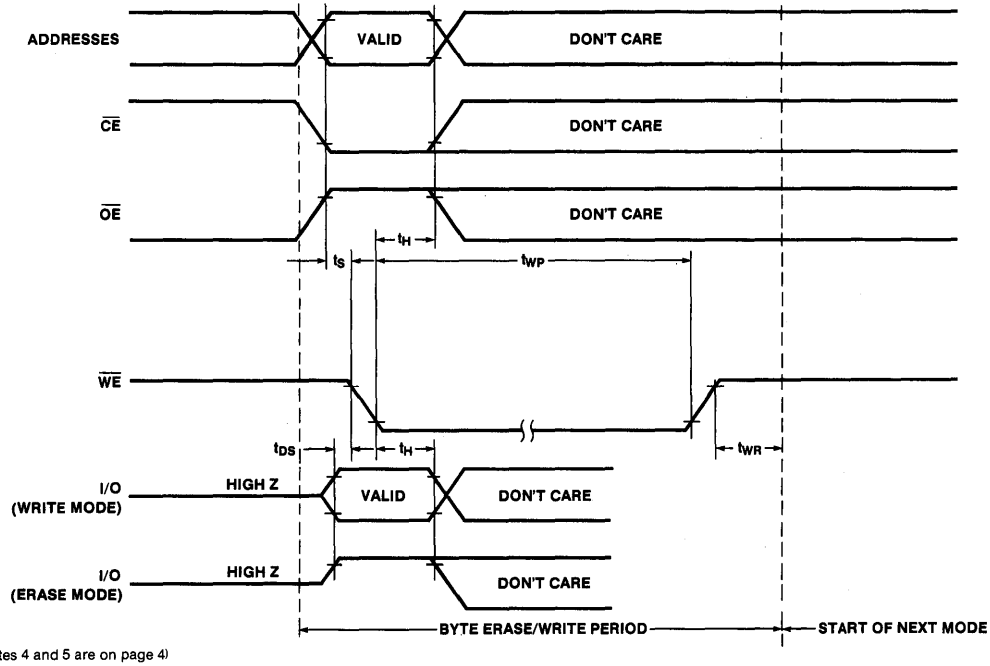
A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

A.C. Operating Characteristics During Write/Erase (Over the operating Vcc and temperature range)

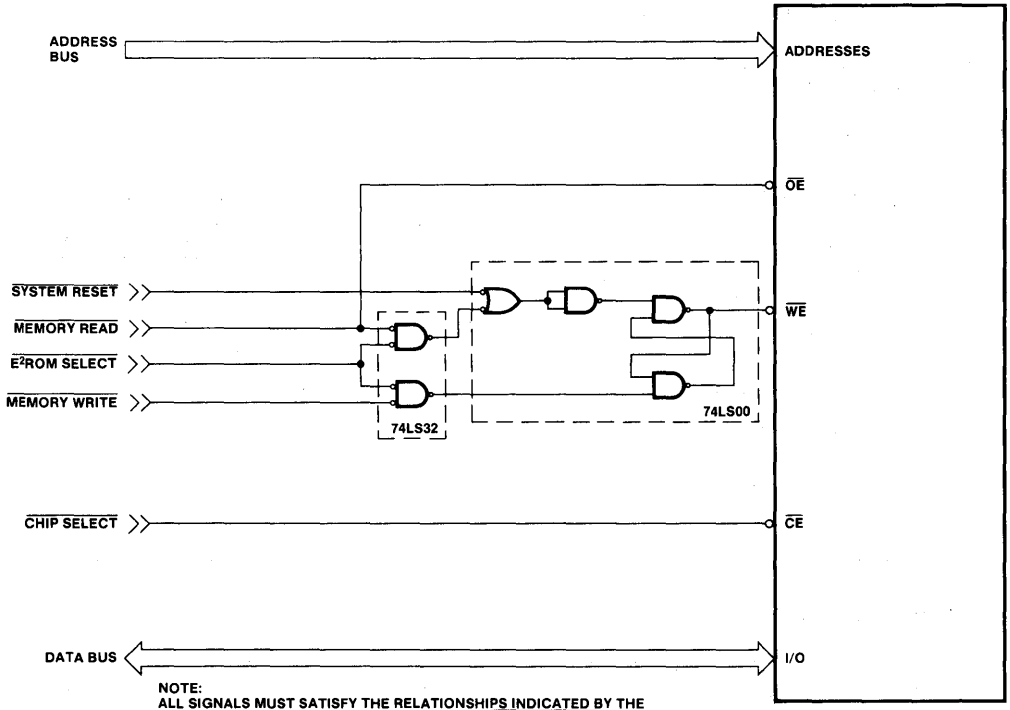
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	0		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width			
	Byte Modes — 52B33/55B33	9		ms
	Byte Modes — 52B33H/55B33H	1		
t_{WR}[5]	$\overline{WE}$ to Mode change			
	$\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle	1		μs

Byte Erase or Byte Write Cycle Timing



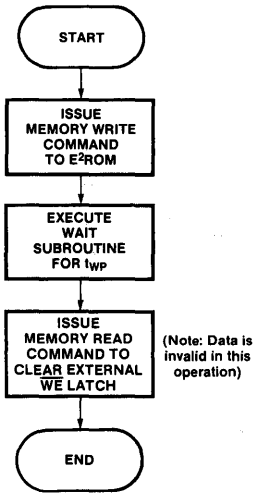
(Notes 4 and 5 are on page 4)

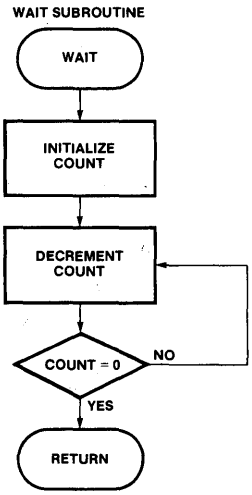
Microprocessor Interface Circuit Example for Byte Write/Erase



NOTE:
ALL SIGNALS MUST SATISFY THE RELATIONSHIPS INDICATED BY THE TIMING DIAGRAMS SHOWN ON PAGES 4 AND 5. $\overline{E^2ROM\ SELECT}$ IS DERIVED FROM THE $\overline{CHIP\ SELECT}$ SIGNALS OF ALL DEVICES FOR WHICH THIS CIRCUIT GATES $\overline{WE}$. THIS MAY ENTAIL A SIMPLE OR FUNCTION. IN CASE OF A SINGLE E^2ROM, THE TWO SIGNALS WOULD BE COMMON.

Typical E²ROM Write/Erase Routine





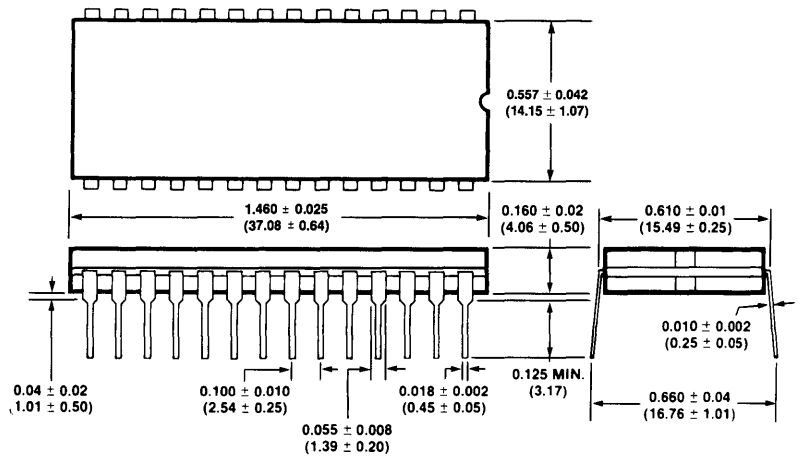
Ordering Information

PART NUMBER: DQ55B33H — 250 / DQ52B33 — 250

PACKAGE TYPE	OPERATING TEMPERATURE RANGE	DEVICE TYPE	WRITE TIME	ACCESS TIME
D= CERDIP	Q = 0°C TO 70°C	52B33 = 10K Endurance	(BLANK) = 10 ms	200 = 200 ns
		55B33 = 1M Endurance	H = 1 ms, 5 Volt	250 = 250 ns
				350 = 350 ns
				35 = 350 ns @ 5% V_{CC}

Packaging Information

28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

SECTION 3

MICRO/LAN

72720
Self-Adaptive E²ROM Single Chip Microcomputer

Features

- **2K x 8 5V E²ROM Program Memory**
- **Write to E²ROM Instruction Allows Processor to Load and Alter its Own Program Memory**
- **E²ROM Programmable Externally as Well as Under Processor Control**
- **E²ROM Programming Instruction can Program External E²ROM**
- **256 x 8 Static RAM**
- **13 Millisecond E²ROM Byte Write/Byte Erase**
- **Program Security Lock to Prevent External Access to User Code**
- **DiTrace™**
- **TMS 7000 Microlanguage Processor Architecture**

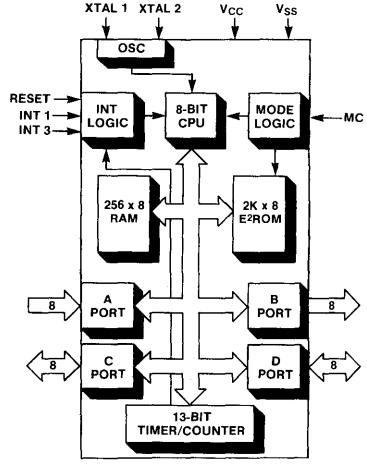
Description

The SEEQ 72720 is a full function single-chip microcomputer, fabricated in N-channel Silicon Gate technology, which contains a 2K x 8 5V non-volatile electrically erasable (E²ROM) program memory. This program memory can be erased and programmed via the processor itself during normal program execution or can be programmed under external control as if it were a standard 5V E²ROM memory component. The E²ROM can easily be expanded off-chip using the processor's Full Expansion Mode. External E²ROM can be programmed with the same instruction used to alter on-chip E²ROM.*

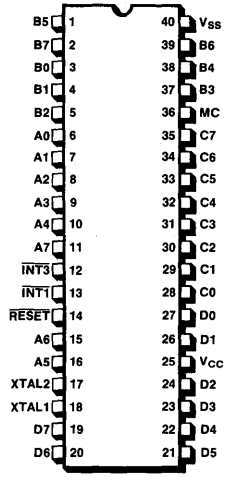
A security lock mechanism is implemented in E²ROM memory which allows the user's program to inhibit external access to its proprietary program code. Once activated this lock can be reset only by an external E²ROM block clear operation which erases the entire program memory contents.

As with other E²ROM devices which SEEQ manufactures, the 72720 has DiTrace™ and Silicon Signature™ features to facilitate production testing and tracking. Each device is encoded with detailed processing and testing information which is stored in a special E²ROM memory as it passes through the manufacturing cycle. Also stored in an unalterable identification code which contains product information such as E²ROM programming parameters.

Block Diagram



Pin Configuration



*TMS7000 under license of Texas Instruments Inc.

Why an E²ROM Microcomputer?

The availability of a single chip microcomputer with non-volatile program memory which can be altered under processor control makes possible the design of low cost products with many new features:

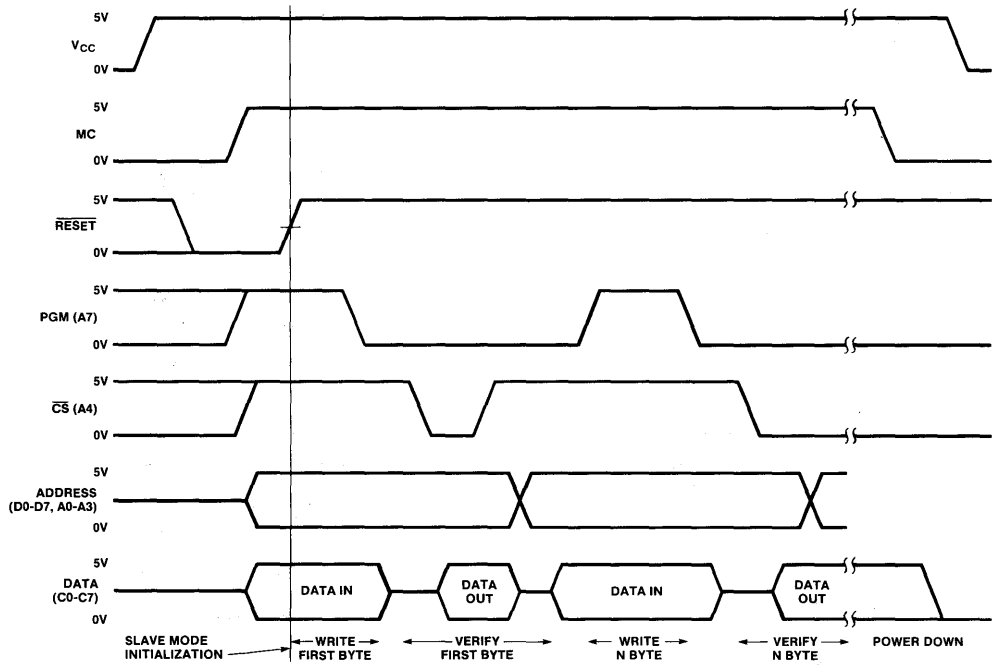
1. *Program and Data Security.*
2. *Self Adaptive Code for machines that learn as they perform their tasks.*
3. *In-Circuit Reprogrammability to eliminate product disassembly for firmware updates.*
4. *Remote Reprogrammability to eliminate service calls for firmware updates.*
5. *Internally Stored Product History including factory test results, product configuration, revision level, and service records.*
6. *Stored Initialization Parameters to eliminate front panel switches and automatically configure product for one or many users.*
7. *Product Usage and Error Logging to simplify maintenance and pinpoint product failure modes.*

Programming The E²ROM

The 72720 provides three modes in which the on-board memory can be programmed:

1. *The Slave Mode which can be activated by resetting the part with 5V applied to a dedicated Mode Control (MC) pin and two I/O port lines, allows the 72720 to be programmed like any E²ROM or EPROM memory component. Address, data and read/write strobes are applied externally. This mode allows the 72720 to be programmed by standard PROM programmers or in-circuit by a master processor.*
2. *In all three normal operating modes, Single Chip, Peripheral Expansion, or Full Expansion, the 72720 can be programmed by executing a new instruction called Program (PRG). The PRG instruction uses any 16-bit register pair in the Register File as a pointer to the E²ROM location to be programmed. The 8 bits of data to be programmed is placed in the A-Register prior to executing PRG. This addressing mode allows E²ROM memory to exist anywhere in the Memory address space of the 72720 (either on- or off-chip). The PRG instruction is a (13 ms) write operation which can write any bit already a "1" to a "0". Any word in E²ROM memory not erased i.e., not all "1s", must be initialized to all "1s", via an extra PRG instruction. The external read/write logic of the 72720 has been designed to allow the programming of external E²ROM memory as well as internal E²ROM using the PRG instruction. Therefore, on-chip E²ROM can be expanded off-chip with no impact on system software or timing.*

Slave Program Timing



3. *A third programming option called the Macro mode (which operates in the Full Expansion mode) provides for E²ROM programming via the internal CPU executing externally stored code. Immediately after RESET, the first instruction fetch occurs from external rather than internal program memory. This mode allows the 72720 to bootstrap itself from external memory in situations where no code exists initially in on-board E²ROM memory.*

Security Lock

Location 01FF in the Peripheral File is a special control register implemented in E²ROM which serves to disable external access to on-board program memory. Security is achieved by writing "1's" to this register after the 72720 has been initialized (at Reset) in either the Single Chip or Peripheral expansion modes. Once the lock is set, the mode of the 72720 cannot be altered via external pins, thereby preventing access to internal memory. The Security Lock can be reset only by an externally generated block clear which erases all internal E²ROM memory.

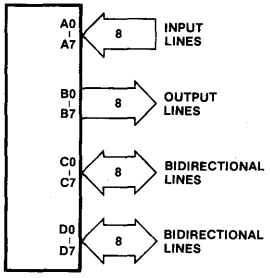
Expansion Modes

In addition to the stand alone Single Chip mode, the 72720 has two expansion modes which provide for the addition of external memory and I/O peripherals to on-chip functions.

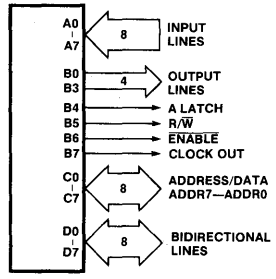
Simplest and most efficient in I/O lines used is the Peripheral Expansion Mode, in which Port "C" becomes a multiplexed 8-bit data/address bus and one-half of Port "B" provides address latching and read/write control for external I/O devices. Devices placed on this expansion bus are accessed the same as if they existed on-chip, sharing the same instruction and timing. This includes the logical instructions, AND, OR, and Exclusive OR which perform read/modify/write cycles on external peripheral file locations to provide bit set, reset, and toggle capabilities.

The second mode is called the Full Expansion Mode. This mode allows the addition of up to 61K bytes of external program and/or data memory to the 72720 using standard 350 to 400 ns memory devices. This mode also provides for external peripheral I/O devices as in the Peripheral Expansion Mode. This mode uses the same I/O lines with the addition of Port "D" to provide the additional address lines required to access the full 64K address space.

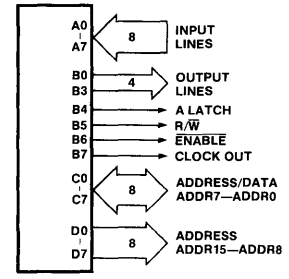
Single Chip Mode



Peripheral Expansion Mode



Full Expansion Mode



Mode Control (Normal Operation)

	Pin Voltages at Reset				
	MC Pin	A4 Pin	A7 Pin	I/O Control Register Bit 7	I/O Control Register Bit 6
Single Chip Mode	0V	X	X	0	0
Peripheral Expansion Mode	0V	X	X	0	1
Full Expansion Mode	0V	X	X	1	0
Read E² Memory Externally	+5V	0V	+5V	X	X
Write E² Memory Externally	+5V	+5V	+5V	X	X

X = Don't Care

Mode Control (Factory Test)

	Pin Voltages at Reset				
	MC Pin	B1 Pin	B2 Pin	A4 Pin	A7 Pin
E²ROM Block Write	+12V	+5V	+5V	+5V	0V
E²ROM Block Clear	+12V	+5V	+5V	+5V	+5V
Read Silicon Signature™	+12V	0V	0V	0V	+5V
Read DiTrace™	+12V	0V	0V	0V	0V

Memory Address Space

The 72720 has a single 64K byte address space divided into three basic areas: a Register File, a Peripheral File and Memory. The Register File resides in the lower 256 bytes of memory and contains the A-Register (accumulator), the B-Register (a secondary accumulator and index register) and 254 general purpose registers. The stack also residing in the Register File is accessed via a separate 8-bit stack pointer register. All accesses to Register File locations require only one machine cycle (400 ns), whereas all other accesses on- or off-chip, require two. The Register File resides entirely on-chip. The Peripheral File occupies the next 256 bytes above the Register File and contains all chip control/status registers and on-chip I/O ports within the first 11 bytes. The remaining 245 locations can be used to access off-chip I/O ports and peripherals in the Peripheral Expansion mode.

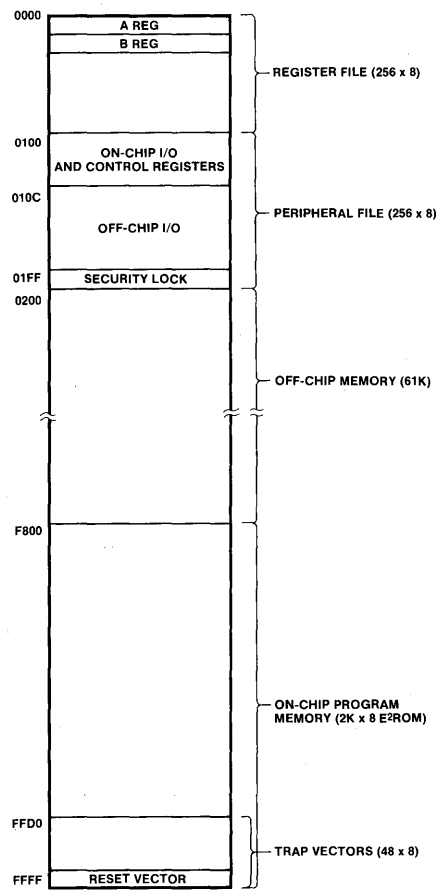
The remainder of the 64K address space is general purpose memory for storage of both programs and data. In the 72720 the upper 2K bytes exist on-chip as E²ROM which serves to store programs, constants, and can also be used to provide non-volatile storage of certain infrequently varying data. The remainder of the address space (≈ 61K) is available in the Full Expansion Mode for any type of memory (including E²ROM) or peripheral devices.

Instruction Set

The 72720 shares the standard instruction set of the TMS7000 Series, which has 61 different instructions, including arithmetic instructions which directly support BCD arithmetic (Decimal Add and Decimal Subtract on packed BCD bytes), single instruction I/O operations on bit fields from 1 to 8 bits that operate without using the accumulator, bit test and jump instructions that function on both I/O and memory, and an 8 x 8 multiply instruction. Also included are a decrement and jump if non-zero instruction for efficient implementation of program loops and several double byte operations including decrement and move.

72720 addressing modes include three byte direct addressing allowing register-to-register operations by-passing the accumulator, 16-bit indirect addressing to the entire 64K address space using any of the 128 register pairs on chip, a special double byte immediate load to the registers indexed with the B-Register, and 16-bit (64K) direct addressing indexed with the B-Register.

72720 Memory Map



Input/Output

In the single chip mode the 72720 provides 32 I/O lines configured as four 8-bit ports A, B, C and D. "A" port is input only, "B" port is output only, and both "C" and "D" ports are fully bi-directional (programmable as input or output on a bit-by-bit basis). Ports "C" and "D" are configured by writing to Data Direction Registers in the Peripheral File address space. The four I/O ports themselves also are accessed as part of the Peripheral File. In addition, like all Peripheral File locations, the I/O ports can be accessed as part of the 64K address space using the Load, Store, and Compare instructions with either Direct, Indirect, or Indexed addressing.

I/O capacity can be easily expanded off-chip using the Peripheral Expansion Mode in which Port "C" becomes a multiplexed 8-bit Data/Address latch and read/write control for external peripheral devices. There are approximately 245 addresses in the Peripheral Files reserved for accessing these external peripheral devices and, since they exist in the same address space as the on-board I/O ports, they can be accessed with the same instructions and timing as on-board I/O.

Timer/Counter

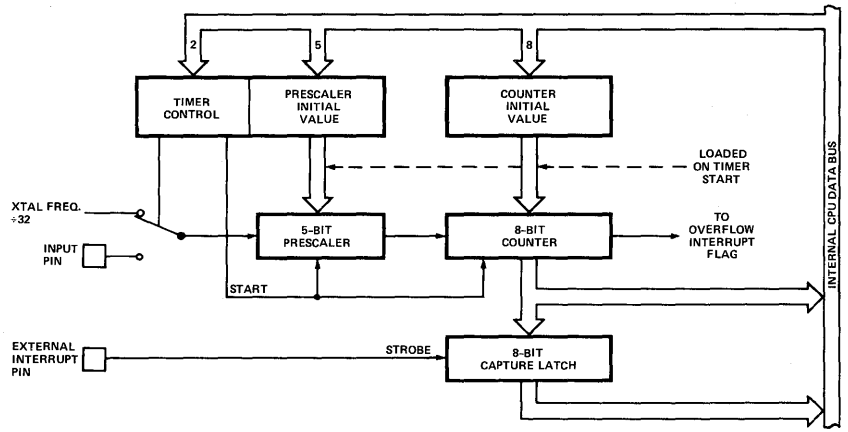
The programmable timer/counter on-board the 72720 consists of an 8-bit binary down counter and a 5-bit clock prescaler counter. The timer/counter can be started and stopped simultaneously via a bit in the timer control register. Each time a "1" is written to this start bit the contents of the prescaler Initial Value and Counter Initial Value registers are loaded into the prescaler and counter, then counting begins. Counter underflow sets a flag that activates an interrupt, or can be polled by the user's program. Counter underflow also initiates automatic reload of the Counter Initial Value to provide unattended generation of periodic pulses. The counter clock source is controlled by a bit in the timer control register and can be either the CPU XTAL divided by 32 (resulting in a 3.2 msec clock period) or can be an external source applied to an input pin. The counter also has associated with it an 8-bit Capture Latch which can be used to instantaneously save the counter value in response to an external interrupt signal. This feature facilitates the measurement of input pulse width and also provides a means of measuring and compensating for variable interrupt response times. Pulse width measurement is accomplished by loading the Capture Latch on each edge of the pulse and comparing the difference. Interrupt response time (latency) is determined by an interrupt service routine, if the interrupt has loaded the Capture, Latch by subtracting the content of the Capture Latch from the current timer value.

The counter Initial Value and Timer Control/Prescaler Initial Value registers are write only and the 8-bit counter and Capture Latch registers are read only. These registers all exist in the 72720's Peripheral File address space.

Interrupts

The 72720 has three hardware interrupt sources and levels in addition to $\overline{RESET}$ (considered a non-maskable interrupt). Level 0 (the highest priority) is RESET followed by Level 1 which is the external interrupt input pin $\overline{INT1}$. Level 2 is the timer underflow interrupt, and Level 3 is the external interrupt pin $\overline{INT3}$. Each of these interrupts has an associated service routine vector location in the upper eight bytes of program memory. Level 1 through 3 are individually enabled/disabled via control bits in the Peripheral File address space. These four interrupt vectors are also activated under program control by executing Trap instructions to vector to the appropriate service routines.

Programmable Timer/Event Counter



8003
EDLC™ Ethernet Data Link Controller

MARCH 1985

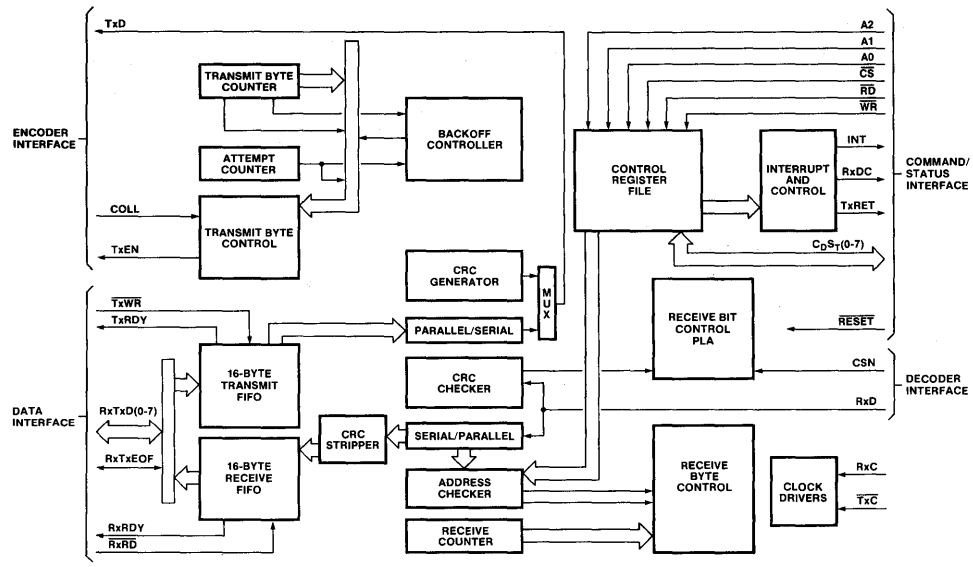
Features

- **Optimized for Burst Mode DMA Applications**
- **100% Ethernet/IEEE 802.3 Compatible**
- **10 MHz Serial/Parallel Conversion**
- **Preamble Generation and Removal**
- **Automatic 32-Bit FCS (CRC) Generation and Checking**
- **Collision Handling, Transmission Deferral and Retransmission with Automatic Jam and Backoff Functions**
- **Error Interrupt and Status Generation**
- **40 Pin Package**
- **Single 5 V ±10% Power Supply**
- **Standard CPU and Peripheral Interface Control Signals**
- **Loopback Capability for Diagnostics**
- **Single Phase Clock**
- **Inputs and Outputs TTL Compatible**

Description

The SEEQ Ethernet Data Link Controller (EDLC) is designed to support the Data Link Layer (layer 2) of the Ethernet specification for Local Area Networks (LAN). The system interface is optimized for ease of connection to commonly available DMA Controllers and specifically for BURST MODE OPERATION. The 8003 interfaces directly to the 8023 Manchester Code Converter to complete the station resident Ethernet functions. The protocol used is Carrier Sense, Multiple Access with Collision Detection (CSMA/CD). The 8003 EDLC chip is a single 40 pin VLSI device which replaces approximately 60 MSI and SSI devices. It is designed to greatly simplify the development of Ethernet communication in computer based systems. The 8003 provides an economic solution for the construction of an Ethernet node, providing high speed data communication at 10 Megabits/second and sees applications in terminals, workstations, personal computers, small business systems, and large computer systems, in both the office and industrial environment. The 8003 EDLC chip has a universal system interface compatible with almost any microprocessor, microcomputer, or system bus, allowing the system designer to make the price/performance tradeoffs for each application. The transmit and receive sections of the EDLC chip are independent and can operate simultaneously to allow reception of a transmitted frame for use in loopback diagnostics modes.

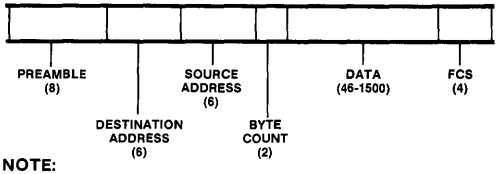
Functional Block Diagram



Functional Description

Frame Format

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a byte-count field, a data field, and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown below.



NOTE:
Field length in bytes in parentheses.

Preamble: *The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.*

Destination Address: *The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.*

Source Address: *The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.*

Byte-Count Field: *The Byte-Count Field consists of two bytes providing the number of valid data bytes in the Data Field, 46 to 1500. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.*

Data Field: *The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.*

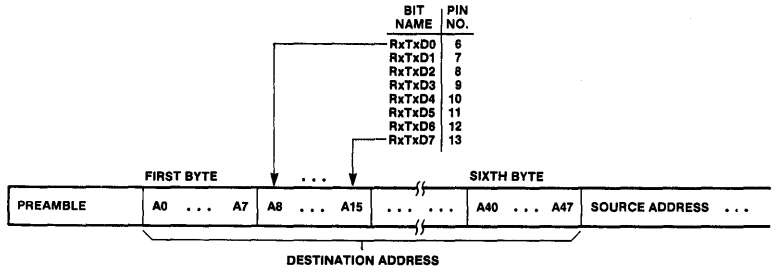
Frame Check Sequence: *The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field, and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.*

Transmitting

The transmit data stream consists of the Preamble, four information fields, and the FCS which is computed in real time by the EDLC chip and automatically appended to the frame at the end of the serial data. The Preamble is also generated by the EDLC chip and transmitted immediately prior to the Destination Address. Destination Address, Source Address, Type Field and Data Field are prepared in the buffer memory prior to initiating transmission. The EDLC chip encapsulates these fields into an Ethernet frame by inserting a preamble prior to these information fields and appending a CRC after the information fields.

Transmission Initiation/Deferral

The Ethernet node initiates a transmission by storing the entire information content of the frame to be transmitted in an external buffer memory, and then transferring initial frame bytes to the EDLC Transmit FIFO. "Transmit-buffer to FIFO" transfers are coordinated via the $\overline{TxWR}$ and TxRDY handshake interface, i.e., bytes are written to the FIFO via $\overline{TxWR}$ only when TxRDY is HIGH. Actual transmission of the data onto the network will only occur if the network has not been busy for the minimum defer time (9.6 μs) and any Backoff time requirements have been satisfied. When transmission begins, the EDLC chip activates the transmit enable (TxEN) line concurrently with the transmission of the first bit of the Preamble and keeps it active for the duration of the transmission.



BITS WITHIN A BYTE ARE TRANSMITTED/RECEIVED BIT NO. "0" FIRST THROUGH BIT NO. "7" LAST.

Figure 1. Bit Serialization/Deserialization

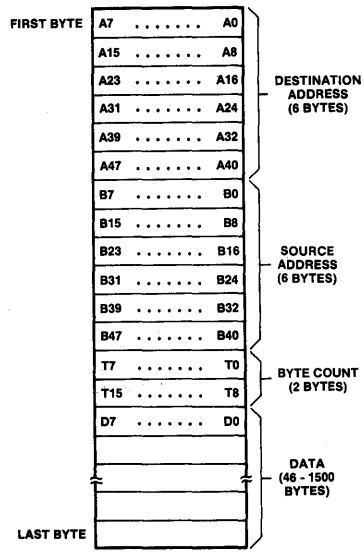


Figure 2. Typical Frame Buffer Format for Byte-Organized Memory

Collision

When concurrent transmissions from two or more Ethernet nodes occur (collision), the EDLC chip halts the transmission of the data bytes in the Transmit FIFO and transmits a Jam pattern consisting of 55555555 hex. At the end of the Jam transmission, the EDLC chip issues a TxRET signal to the CPU, and begins the Backoff wait period.

To reinitiate transmission, the initial bytes of the frame information fields must be reloaded into the EDLC Transmit FIFO. The TxRET is used to indicate to the buffer manager the need for frame reinitialization. The reloading of the Transmit FIFO may be done prior to the Backoff interval elapsing, so that no additional delay need be incurred to retransmission.

Scheduling of retransmission is determined by a controlled randomization process called Truncated Binary Exponential Backoff. The EDLC chip waits a random interval between 0 and 2^K slot times (51.2 μs per slot time) before attempting retransmission, where "K" is the current transmission attempt number (not to exceed 10).

When 16 consecutive attempts have been made at transmission and all have been terminated due to collision, the EDLC Transmit Control sets an error status bit and issues an interrupt to the CPU if enabled.

Terminating Transmission

Transmission terminates under the following conditions:

***Normal:** The frame has been transmitted successfully without contention. Loading of the last data byte into the Transmit FIFO is signaled to the EDLC chip by activation of the RxTxEOF signal concurrently with the last byte of data loaded into the Transmit FIFO. This line acts as a ninth bit in the Transmit FIFO. When this last byte is serialized, the CRC is appended and transmitted concluding frame transmission. The Transmission Successful bit of the Transmit Status Register will be set by a normal termination.*

***Collision:** Transmission attempted by two or more Ethernet nodes. The Jam sequence is transmitted, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun.*

***Underflow:** Transmit data is not ready when needed for transmission. Once transmission has begun, the EDLC chip on average requires one transmit byte every 800 ns in order to avoid Transmit FIFO underflow (starvation). If this condition occurs, the EDLC chip terminates the transmission, issues a TxRET signal, and sets the Transmit-Underflow status bit.*

***16 Transmission Attempts:** If a Collision occurs for the sixteenth consecutive time, the 16-Transmission-Attempts status bit is set, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun. The counter that keeps track of the number of collisions is modulo 16 and therefore rolls over on the 17th collision.*

At the completion of every transmission or retransmission, new status information is loaded into the Transmit Status Register. Dependent upon the bits enabled in the Transmit Command Register, an interrupt will be generated for the just completed transmission. In both collision and underflow the TxRET signal is activated.

Receiving

The EDLC chip is continuously monitoring the network. When activity is recognized via the Carrier Sense (CSN) line going active, the EDLC chip synchronizes itself to the incoming data stream during the Preamble, and then examines the destination address field of the frame. Depending on the Address Match Mode specified, the EDLC chip will either recognize the frame as being addressed to itself in a general or specific fashion or abort the frame reception.

Preamble Processing

The ELDC chip recognizes activity on the Ethernet via the Carrier Sense line. The Preamble is normally 64

bits (8 bytes) long. The Preamble consists of a sequence of 62 alternating "1"s and "0"s followed by "11", with the frame information fields immediately following. In order for the decoder phase-lock to occur, the EDLC chip waits 12 bit times before looking for the "11" end of preamble indicator. If the EDLC chip receives a "00" before receiving the "11" in the Preamble, an error condition has occurred. The frame is not received, and the EDLC chip begins monitoring the network for a carrier again.

Address Matching

Ethernet addresses consist of two 6-byte fields. The first bit of the address signifies whether it is a Station Address or a Multicast/Broadcast Address.

First Bit	Address
0	Station Address (Physical)
1	Multicast/Broadcast Address (logical)

Address matching occurs as follows:

Station Address: All destination address bytes must match the corresponding bytes found in the Station Address Register.

Multicast Address: If the first bit of the incoming address is a 1 and the EDLC chip is programmed to accept Multicast Addresses, the frame is received.

Broadcast Address: The six incoming destination address bytes must all be FF hex. If the EDLC chip is programmed to accept Broadcast or Multicast Addresses the frame will be received.

If the incoming frame is addressed to the EDLC chip specifically (Destination Address matches the contents of the Station Address Register), or is of general or group interest (Broadcast or Multicast Address), the EDLC chip will pass the frame exclusive of Preamble and FCS to the CPU buffer and indicate any error conditions at the end of the frame. If, however, the address does not match, as soon as the mismatch is recognized the EDLC chip will terminate reception and issue an RxDC.

The EDLC chip may be programmed via the Match Mode bits of the Receive Command Register to ignore all frames (Disable Receiver), accept all frames (Promiscuous mode), accept frames with the proper Station Address or the Broadcast Address (Station/Broadcast), or accept all frames with the proper Station Address, the Broadcast Address, or all Multicast Addresses (Station/Broadcast/Multicast).

Terminating Reception

Reception is terminated when either of the following conditions occur:

Carrier Sense Inactive: Indicates that traffic is no longer present on the Ethernet cable.

Overflow: The host node for some reason is not able to empty the Receive FIFO as rapidly as it is filled, and an error occurs as frame data is lost. On average the Receive FIFO must be serviced every 800 ns to avoid this conditions.

Frame Reception Conditions

Upon terminating reception, the EDLC chip will determine the status of the received frame and conditionally load it into the Receive Status Register. An interrupt will be issued if the appropriate conditions as specified in the Receive Command Register are present. The EDLC chip may report the following conditions at the end of frame reception:

Overflow: The EDLC internal Receive FIFO overflows.

Dribble Error: Carrier Sense did not go inactive on a receive data byte boundary.

CRC Error: The 32-bit CRC transmitted with the frame does not match that calculated upon reception.

Short Frame: A frame containing less than 64 bytes of information was received (including FCS).

Good Frame: A frame is received that does not have a CRC error, Shortframe, or Overflow condition.

System Interface

The EDLC chip system interface consists of two independent busses and respective control signals. Data is read and written over the Receive/Transmit Data Bus RxTxD (0-7). These transfers are controlled by the TxRDY and $\overline{TxWR}$ signals for transmitted data, and RxRDY and $\overline{RxRD}$ for received data. All Commands and Station Addresses are written, and all status read over a separate Command/Status Bus CdSt (0-7). These transfers are controlled by the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and A0-A2 signals. The EDLC chip's command and status registers may be accessed at any time. However, it is recommended that writing to the command register be done only during interframe gaps.

With the exception of the two Match Mode bits in the Receive Command Register, all bits in both command registers are interrupt enable bits. Changing the interrupt enable bits during frame transmission does not affect the frame integrity. Asynchronous error events, however, e.g., overflow, underflow, etc., may cause chip operation to vary, if their corresponding enable bits are being altered at the same time.

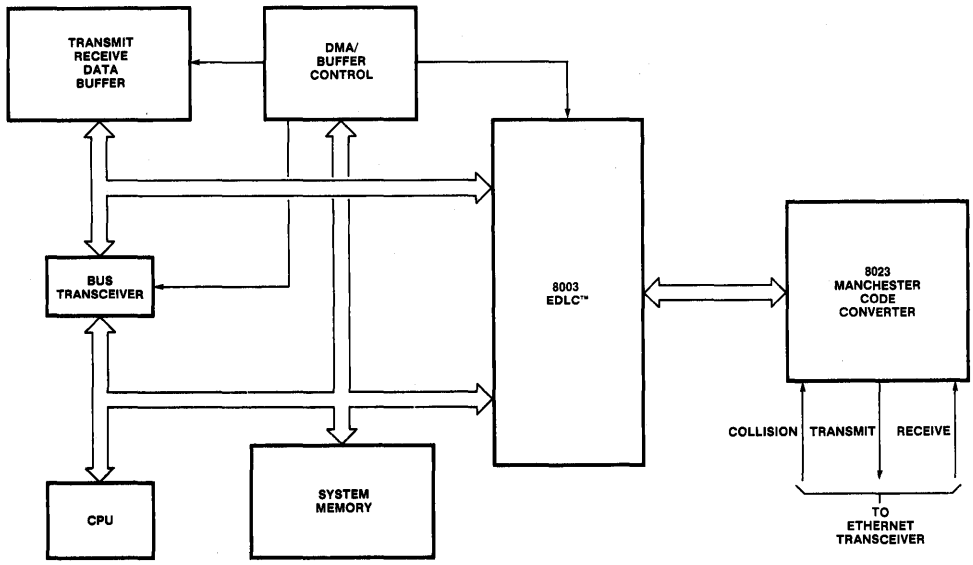


Figure 3. Typical Ethernet Node Configuration

Reading the status registers may also occur at any time during transmission or reception.

Internal Register Addressing

	Register Address			Register Description	
	A2	A1	A0	Read	Write
0	0	0	0	—	Station Addr 0
1	0	0	1	—	Station Addr 1
2	0	1	0	—	Station Addr 2
3	0	1	1	—	Station Addr 3
4	1	0	0	—	Station Addr 4
5	1	0	1	—	Station Addr 5
6	1	1	0	Rx Status	Rx Command
7	1	1	1	Tx Status	Tx Command

Status registers are read only registers. Command and Station Address registers are write only registers. Access to these registers is via the CPU interface: Control signals $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and the Command/Status Data Bus CdSt (0-7).

Station Address Register

The Station Address Register is 6 bytes in length. The contents may be written in any order, with bit "0" of byte "0" corresponding to the first bit received in the data stream, and indicating whether the address is physical or logical. Bit 7 of station address byte 5 is compared to the last bit of the received destination address. The Station Address should be programmed prior to enabling the receiver.

Transmit Command Register

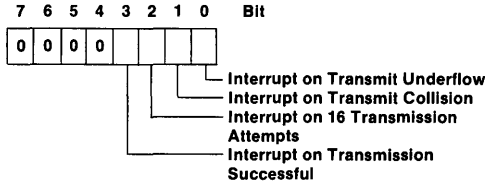
The Transmit Command Register is an interrupt mask register, which provides for control of the conditions allowed to generate transmit interrupts. Each of the four least significant bits of the register may be individually set or cleared. When set, the occurrence of the associated condition will cause an interrupt to be generated. The four specific conditions for which interrupts may be generated are:

- *Underflow*
- *Collision*
- *16 Collisions*
- *Transmission Successful*

The interrupt signal INT will be set when one or more of the specified transmission termination conditions occurs and the associated command bit has been set. The interrupt signal INT will be cleared when the Transmit Status Register is read.

All bits of the Transmit Command Register are cleared upon chip reset.

Transmit Command Register Format



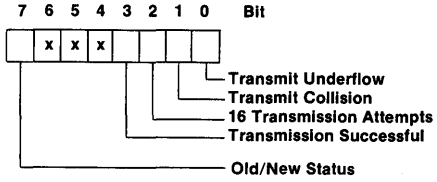
Transmission Successful is set only on the successful transmission or retransmission of a frame.

Transmit Status Register

The Transmit Status Register is loaded at the conclusion of each frame transmission or retransmission attempt. It provides for the reporting of both the normal and error termination conditions of each transmission.

The OLD/NEW status bit is set each time the Transmit Status Register is read, and reset each time new status is loaded into the Transmit Status Register. The OLD/NEW status bit is SET, and all other bits CLEARED upon chip reset.

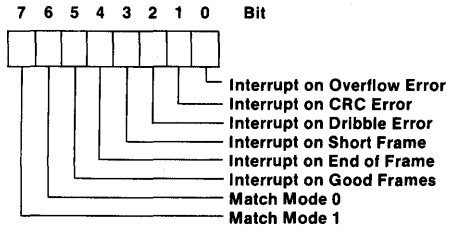
Transmit Status Register Format



Receive Command Register

The Receive Command Register has two primary functions, it specifies the Address Match Mode, and it specifies Frames-of-Interest. i.e. frames whose arrival must be communicated to the CPU via interrupts and status register updates. Frames-of-Interest are frames whose status must be saved for inspection, even at the expense of losing subsequent frames.

Receive Command Register Format



Bits 0-5 specify Interrupt and Frame-of-Interest when set. Bit 4, End of Frame, specifies any type of frame except overflow.

Match Mode Definition

	Match Mode 1	Match Mode 0	Function
0	0	0	Receiver Disable
1	0	1	Receive All Frames
2	1	0	Receive Station or Broadcast Frames
3	1	1	Receive Station, Broadcast/Multicast Frames

Changing the receive Match Mode bits during frame reception may change chip operation and give unpredictable results.

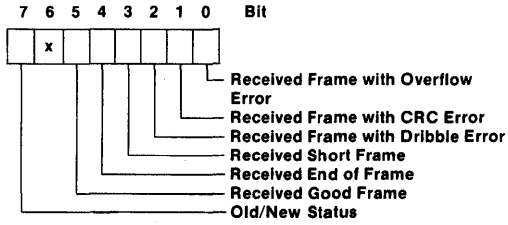
Interrupt Enable and Frames-of-Interest

Bits 0-5 when set specify interrupt generation on occurrence of the corresponding frame reception condition. They also specify the corresponding types of frames to be Frames-of-Interest for use by the Receive Status Register to control status loading.

Receive Status Register

The Receive Status Register is normally loaded with the status of each received frame when the frame has been received or frame reception has been terminated due to an error condition. In addition, this register contains the Old/New Status bit which is set when the Receive Status Register is read or the chip is reset, and cleared only when new status is loaded for a Frame-of-Interest (as defined by bits 0-5 of the Receive Command Register). All other bits are cleared upon chip reset.

Receive Status Register Format



The Old/New Status bit write-protects the Receive Status Register while it contains unread status for a Frame-of-Interest. When this bit is zero, the register is write-protected. The Old/New Status bit is cleared whenever the status of a new Frame-of-Interest is loaded into the Receive Status Register and is set after that status is read. When zero, it indicates "new status for a Frame-of-Interest".

Thus the status of any frame received following the reception of a Frame-of-Interest will not be loaded into the Receive Status Register unless the previous status has been read. If any following frame is received before the status of the previous Frame-of-Interest has been read, the new status will not be loaded, the Receive Discard (RxDC) signal will be issued and the Receive FIFO will be cleared.

With this one exception caused by a write-protect condition, the status of each frame is always loaded into the Receive Status Register on completion of reception.

Any frame received will cause an interrupt to be generated if the corresponding Interrupt Enable bit is set. This interrupt is reset upon reading the Receive Status Register.

These conditions ensure that a maximum number of good frames are received and retained.

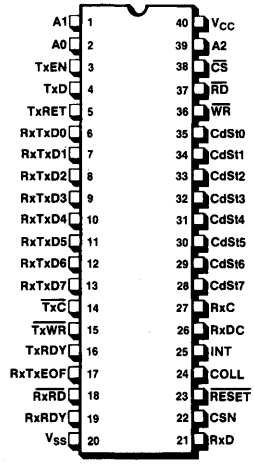


Figure 4. Pin Configuration

Pin Description

The EDLC chip has four groups of interface signals:

- *Power Supply*
- *Encoder/Decoder*
- *Data Buffer*
- *Command/Status*

Power Supply

V_{CC} ..... +5 V
V_{SS} ..... Ground

Encoder/Decoder Interface

$\overline{TxC}$ Transmit Clock (Input): *10 MHz, 50% duty cycle transmit clock used to synchronize the transmit data from the EDLC chip to the encoder. This clock runs continuously, and is asynchronous to RxC.*

TxD Transmit Data (Output): *Serial data output to the encoder. Active HIGH.*

TxEN Transmit Enable (Output): *This signal is used to activate the encoder. It becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. Active HIGH and cleared by Reset.*

RxC Receive Clock (Input): *10 MHz, 50% duty cycle nominal. The receive clock is used to synchronize incoming data to the EDLC chip from the decoder. This clock runs continuously, and is asynchronous to $\overline{TxC}$.*

RxD Receive Data (Input): *Serial input data to the EDLC chip from the decoder. Active HIGH.*

CSN Carrier Sense (Input): *Indicates traffic on the coaxial cable to the EDLC chip. Becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. Active HIGH.*

COLL Collision (Input): *Indicates transmission contention on the Ethernet cable. The Collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.*

Data Buffer Interface

RxTxD (0-7) Receive/Transmit Data Bus (I/O): *Carries Receive/Transmit data byte from/to the EDLC chip Receive/Transmit FIFOs.*

RxTxEOF Receive/Transmit End of Frame (I/O): *Indicates last byte of data on the Receive/Transmit Data Bus. Effectively a ninth bit in the FIFOs with identical timing to RxTxD (0-7). Active HIGH.*

RxRDY Receive Ready (Output): *Indicates that at least one byte of received data is available in the Receive FIFO. This signal will remain active high as long as one byte of data remains in the Receive FIFO. When this condition no longer exists, RxRDY will be deasserted with respect to the leading edge of the $\overline{RxRD}$ strobe that removes the last byte of data from the Receive FIFO. $\overline{RxRD}$ should not be activated if RxRDY is low. Active HIGH and cleared by Reset.*

$\overline{RxRD}$ Receive Read Strobe (Input): *Enables transfer of received data from the EDLC Receive FIFO to the RxTxD Bus. Data is valid from the EDLC Receive FIFO at the RxTxD pins on the rising edge of this signal. This signal should not be activated unless RxRDY is high. Active LOW.*

RxDC Receive Discard (Output): *Asserted when one of the following conditions occurs, and the associated Interrupt Enable bit in the Receive Command Register is reset. (1) Receive FIFO overflow. (2) CRC Error. (3) Short Frame Error. (4) Receive frame address non-match or (5) current frame status lost because previous status was not read. RxDC does not activate on errors when the associated Interrupt Enable bit is set. In this case, EOF will be generated instead when the Receive FIFO is read out. This allows reception of frames with errors. RxDC acts internally to clear the Receive FIFO.*

TxRDY Transmit Ready (Output): *Indicates that the Transmit FIFO has space available for at least one data byte. This signal will remain active high as long as one byte of space exists for transmitted data to be written into. When this condition no longer exists, TxRDY will be deasserted with respect to the leading edge of the $\overline{TxWR}$ strobe that fills the Transmit FIFO. TxRDY is forced inactive during Reset, and when TxRET is active. Active HIGH. Goes high after Reset.*

$\overline{TxWR}$ Transmit Write (Input): *Synchronizes data transfer from the RxTxD Bus to the Transmit FIFO. Data is written to the FIFO on the rising edge of this signal. This signal should not be active unless TxRDY is high. Active LOW.*

TxRET Transmit Retransmit (Output): *Asserted whenever either transmit underflow or transmit collision conditions occur. It is nominally 800 ns in width. Active HIGH. Asserted by Reset.*
TxRET clears the internal Transmit FIFO.

Command/Status Interface

CdSt (0-7) Command/Status Data Bus (I/O): *These lines carry commands and status as well as station address initialization information between the EDLC chip and CPU. These lines are nominally high impedance until activated by $\overline{CS}$ and $\overline{RD}$ being simultaneously active.*

A0-A2 Address (0-2) (Input): *Address lines to select the proper EDLC internal registers for reading or writing.*

$\overline{CS}$ Chip Select (Input): *Chip Select input, must be active in conjunction with $\overline{RD}$ or $\overline{WR}$ to successfully access the EDLC internal registers. Active LOW.*

$\overline{RD}$ Read (Input): *Enables reading of the EDLC internal registers in conjunction with $\overline{CS}$. Data from the internal registers is enabled via the falling edge of $\overline{RD}$ and is valid on the rising edge of the signal. Active LOW.*

$\overline{WR}$ Write (Input): *Enables writing of the EDLC internal registers in conjunction with $\overline{CS}$. Write data on the CdSt (0-7) data lines must be set up relative to the rising edge of the signal. Active LOW.*

INT Interrupt (Output): *Enabled as outlined above by a variety of transmit and receive conditions. Remains active until the status register containing the reason for the interrupt is read. Active HIGH.*

$\overline{RESET}$ (Input): *Initializes control logic, clears command registers, clears the Transmit Status Register, clears bits 0-5 of the Receive Status Register, sets the Old/New Status bit (bit 7 of the Receive Status Register), asserts RxDC and TxRET and clears the Receive and Transmit FIFOs. In addition, TxRDY is forced low during a reset. TxRDY goes high when $\overline{RESET}$ goes high, indicating the EDLC chip is ready to transmit. $\overline{RESET}$ is active LOW.*

Absolute Maximum Ratings

Ambient Temperature
Under Bias ..... -10° C to +80° C
Storage Temperature ..... -65° C to +150° C
All Input or Output Voltages
with Respect to Ground ..... +7 V to -0.5 V
Package Maximum Power Dissipation ... 1.5 Watts

DC Characteristics $T_A = 0°\,C$ to $70°\,C$, $V_{CC} = 4.50$ V to 5.50 V

Symbol	Paramater	Limits[1] Min.	Typ.	Max.	Units	Condition
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0.45 V to 5.25 V
I_O	Output Leakage Current			10	μA	V_{OUT} = 0.45 V to 5.25 V
I_{CC}	V_{CC} Current		150	200	mA	
V_{CH}	Clock Input High Voltage	3.5		V_{CC} + 1	V	
V_{CL}	Clock Input Low Voltage			0.8	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH_1}	Input High Voltage	2.0		V_{CC} + 1	V	Except $\overline{TxWR}$ and $\overline{RxRD}$
V_{IH_2}	Input High Voltage	3.0		V_{CC} + 1	V	$\overline{TxWR}$ and $\overline{RxRD}$
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

NOTE:
1. Typical values are for $T_A = 25°\,C$ and nominal supply voltages.

Operating Conditions

Ambient Temperature Range ..... 0° C to 70° C
V_{CC} Power Supply ..... 4.50 V to 5.50 V

AC Test Conditions

Output Load: 1 Schottky TTL Gate + CL = 100 pF
(All pins except TxEN, TxD)
TxEN, TxD Load: 1 Schottky TTL Gate + CL = 35 pF
Input Pulse Level: 0.4 V to 2.4 V
Timing Reference Level: 1.5 V

Capacitance $T_A = 25°C$, $F_C = 1$ MHz

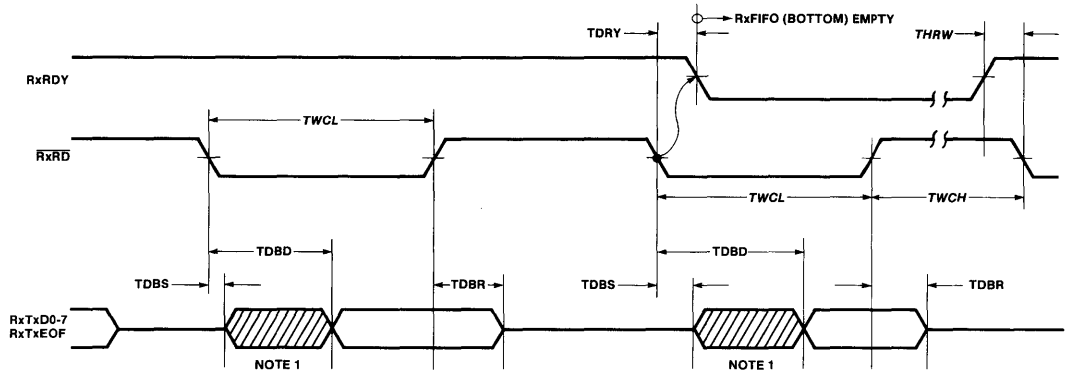
Symbol	Parameter	Maximum	Condition
C_{IN}	Input Capacitance	15 pF	$V_{IN} = 0$ V
$C_{I/O}$	I/O Capacitance	15 pF	$V_{I/O} = 0$ V

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 4.50$ V to 5.50 V

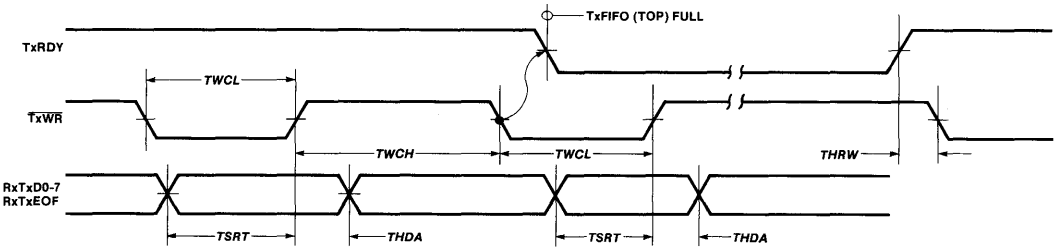
Symbol[5]	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units (ns)	Condition
DATA AND COMMAND/STATUS INTERFACE TIMING						
TDBD	RxTx/CdSt Bus Data Delay			150	ns	
TDBR	RxTx/CdSt Bus Release Delay	10			ns	
TDBS	RxTx/CdSt Bus Seizure Delay	10		150	ns	
TDRY	RxRDY/TxRDY Clear Delay			100	ns	
THAR	$A_{0-2}/\overline{CS}$ Hold	10			ns	
THDA	RxTx/CdSt Bus Hold	0			ns	
THRW	$\overline{RxRD}/\overline{TxWR}$ Hold	0			ns	
TSAR	$A_{0-2}/\overline{CS}$ Setup	0			ns	
TSCS	CdSt Bus Setup	90			ns	
TSRT	RxTx Bus Setup	90			ns	
TWCH	$\overline{RxRD}/\overline{TxWR}/\overline{RD}//\overline{WR}$ High Width	100			ns	
TWCL	$\overline{RxRD}/\overline{TxWR}/\overline{RD}/\overline{WR}$ Low Width	100			ns	
SERIAL TRANSMIT AND RECEIVE INTERFACE TIMING						
TDDC	RxDC Set Delay	800			ns	Note 1
TDIC	INT Clear Delay			150	ns	
TDRE	TxRET Set Delay	2400			ns	Note 3
TDRI	Receive INT Delay	1000			ns	Note 2
TDTD	TxD/TxEN Delay	20		60	ns	CI = 35 pF
TDTI	Transmit INT Delay	1200			ns	Note 4
THRD	RxD Hold	20			ns	
TPCK	RxC/$\overline{TxC}$ Clock Period	95		1000	ns	
TSRD	RxD Setup	30			ns	
TWDC	RxDC High Width	600			ns	
TWRC	RxC High/Low Width	45			ns	
TWRE	TxRET High Width	600			ns	
TWRS	$\overline{RESET}$ Low Width	10,000			ns	
TWTC	$\overline{TxC}$ High/Low Width	45			ns	
TWCO	COLL Width	50			ns	

NOTES:
1. For frame reception with Shortframe or CRC Error. If frame reception is terminated due to Overflow, RxDC will be issued within 1.2 μs of Overflow. If frame reception is terminated due to non-match of address, RxDC will be issued within 2.4 μs of the receipt of the last address bit.
2. Normal frame reception without Overflow. If frame reception is terminated due to Overflow, INT will be issued within 1.2 μs of Overflow.
3. For TxRET caused by Collision or 16 Collision condition. If transmission is terminated due to Underflow TxRET will be issued within 1.2 μs of the Underflow.
4. For INT caused by Collision or 16 Collision condition. If caused by Underflow, INT will be issued within 1.2 μs. If caused by normal termination, INT will be issued within 200 ns of TxEN going LOW.
5. Italics indicate input requirement, non-italics indicate output timing.

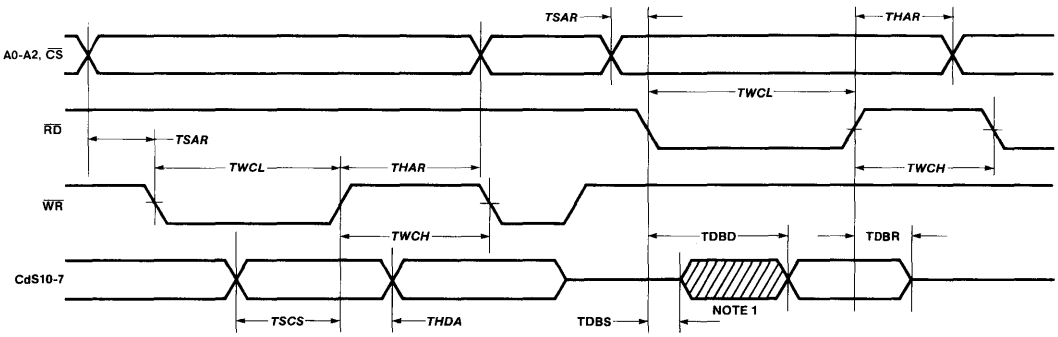
RECEIVE DATA INTERFACE TIMING



TRANSMIT DATA INTERFACE TIMING

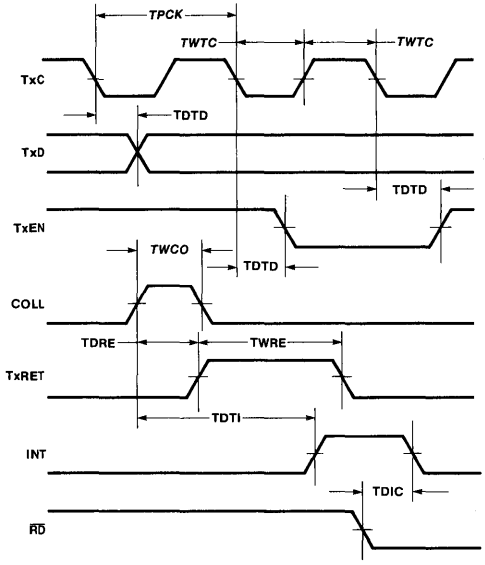


COMMAND/STATUS INTERFACE TIMING

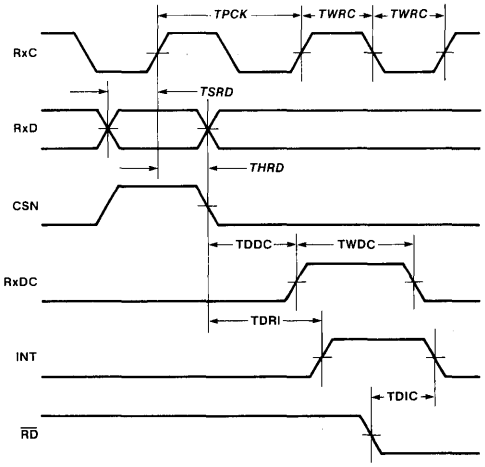


NOTE 1: BUS IS DRIVEN AT THIS TIME. HOWEVER, NO VALID INFORMATION PRESENT.

SERIAL TRANSMIT INTERFACE TIMING



SERIAL RECEIVE INTERFACE TIMING



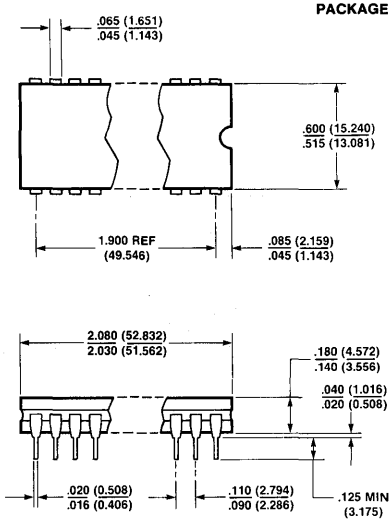
Ordering and Package Information

PART NUMBER

D Q 8003

- PRODUCT: EDLC™ IC
- TEMPERATURE RANGE: 0° C TO 70° C
- PACKAGE: CERDIP

40-LEAD HERMETIC CERDIP
PACKAGE TYPE D



NOTES:
1. FOR SOLDER DIPPED LEADS, THICKNESS WILL BE .020 MAX.

ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

8023A
MCC™ Manchester Code Converter

August 1985

Features

- **Compatible with IEEE 802.3 and Ethernet Rev. 1 Specification**
- **Compatible with the 8003 EDLC™ and Intel 82586 LAN Controller**
- **Directly Replaces SEEQ 8002 and 8023**
- **Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)**
- **Receiver and Collision Squelch Circuit and Noise Rejection Filter**
- **Differential TRANSMIT Cable Driver**
- **Loopback Capability for Diagnostics and Isolation**
- **Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission**
- **20 MHz Crystal Oscillator**
- **Transceiver Interface High Voltage (16 V) and Low Voltage Short Circuit Protection**
- **Low Power CMOS Technology with Single 5V Supply**
- **20 pin DIP Package**

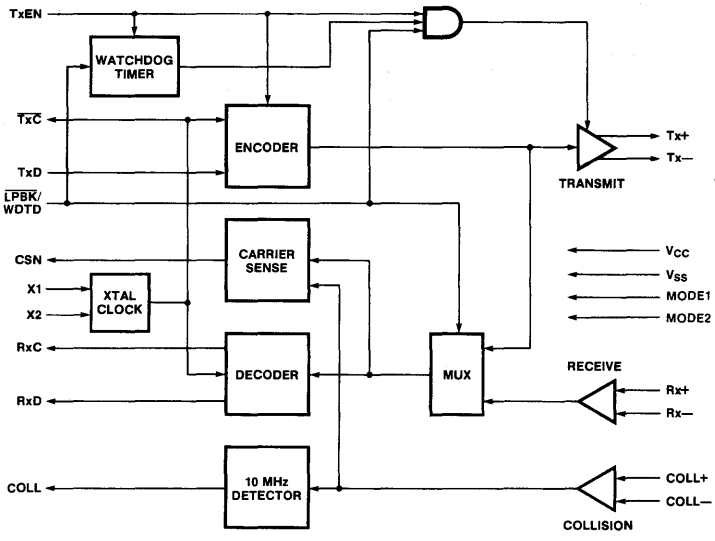
Description

The SEEQ 8023A Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 Ethernet Data Link Controller or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3, and Ethernet Revision 1.

The SEEQ 8023A MCC™ is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the 8003 and a transceiver, the 8023A Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

Functional Block Diagram



Pin Configuration

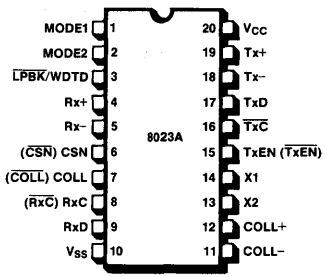


Figure 1. 8023A MCC™ Manchester Code Converter Block Diagram.

Functional Description

The 8023A Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8023A MCC™ recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1", and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exlusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz ±0.01% transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complementary data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

Data encoding and transmission begin with TxEN going active; the first is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero.

To eliminate DC current in the transformer during idle, Tx ± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

Watchdog Timer

A 25 ms watchdog timer is built on chip. It can be enabled or disabled by the $\overline{LPBK}$/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

Differential Input Circuit (Rx+ and Rx–, COLL+ and COLL–)

As shown in Figure 3, the differential input for $\bar{R}x+$ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2 Ω ± 1% resistors in series for proper impedance matching.

The center tap has a 0.01 μF capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

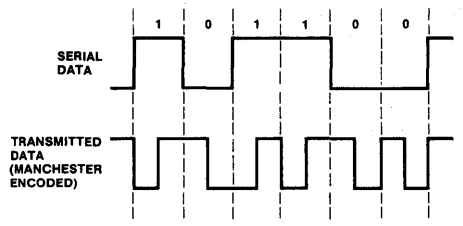


Figure 2. Manchester Coding

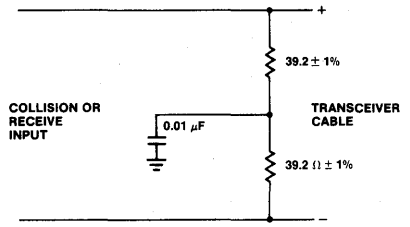


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signal less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) is always rejected, signal greater than -300 mV and wider than 30 ns (18 ns for collision pair) is always accepted.

Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to −8.25 ns within 12 bit cell time worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to −8.25 ns. The RxC high or low time will always be greater than 40 ns. If MODE2 is high or floating, RxC will be held low for 1.2 μs maximum while the PLL is acquiring lock. If MODE2 is low, RxC follows TxC for the first 1.2 μs and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after node just finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5 μs regardless of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhabit period after packet reception. Also, RxD is held low if MODE2 is low or high if MODE 2 is high and RxC reverts to TxC. During clock switching, RxC may stay high for 200 ns maximum. ($\overline{RxC}$ stays low for 200 ns maximum, 40 ns minimum).

Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz ±15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with RxC. However, if a collision arrives during inhabit period 4.5 μs from the time CSN was deasserted, CSN will not be reasserted.

Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except differential output driver and differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the 8023A also generates a 650 ns long COLL signal 550 ns after CSN was deasserted. The watchdog timer remains enabled in this mode.

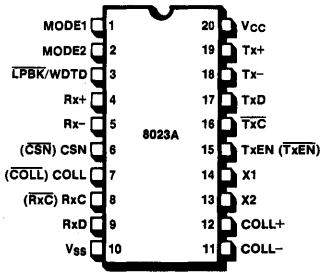


Figure 4. Pin Configuration

Pin Description

The MCC™ chip signals are grouped into four categories:

- *Power Supply and Clock*
- *Controller Interface*
- *Transceiver Interface*
- *Miscellaneous*

Power Supply

V_{CC} ..... +5V
V_{SS} ..... Ground

X1 and X2 Clock (Inputs): *Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.*

Controller Interface

RxC ($\overline{RxC}$) Receive Clock (Output): *This signal is the recovered clock from the phase decoder circuit. It is switched to TxC when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible. If the MODE2 signal is high, RxC is inverted ($\overline{RxC}$) and there is a 1.25 μsec discontinuity at the beginning of frame reception.*

RxD Receive Data (Output) : *The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. However, if the MODE2 signal is HIGH, the RxD output will be HIGH during idle. TTL compatible. Active HIGH.*

CSN ($\overline{CSN}$) Carrier Sense (Output): *The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with RxC. TTL compatible. Normally active HIGH, unless MODE2 is HIGH, in which case $\overline{CSN}$ is active LOW.*

$\overline{TxC}$ Transmit Clock (Output): *A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL compatible.*

TxD Transmit Data (Input): *TxD is the serial input data to be transmitted. The data is clocked into the MCC by $\overline{TxC}$. Active HIGH, TTL compatible.*

TxEN ($\overline{TxEN}$) Transmit Enable (Input): *Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with $\overline{TxC}$. TxEN goes active with the first bit of transmission. TTL compatible. If MODE2 is HIGH, TxEN is inverted.*

COLL ($\overline{COLL}$) Collision (Output): *When asserted, indicates to the controller the simultaneous transmission of two or more stations on network cable. TTL compatible. If MODE2 is HIGH, COLL is inverted.*

Transceiver Interface

Rx+ and Rx- Differential Receiver Input Pair (Input): *Differential receiver input pair which brings the encoded receive data to the 8023A. The last transition is always positive-going to indicate the end of the frame.*

COLL+ and COLL- Differential Collision Input Pair (Input): *This is a 10 MHz ±15% differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% —40%/60%. The last transition is positive-going.*

Tx+ and Tx- Differential Transmit Output Pair (Output): *Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243 Ω resistors to ground as loading. 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8 μs to limit the back swing of the coupling transformer to less than 0.1 V.*

Miscellaneous

MODE1 (Input): *This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, then the output is differentially high when idle (Ethernet Rev. 1 specification).*

MODE2 (Input): *The MODE2 Input signal is normally active LOW. In this configuration, the 8023A operates in a mode compatible with the SEEQ 8003. An alternate mode of operation may be achieved by configuring the MODE signal active HIGH, or by allowing it to float HIGH with its internal pullup. In this configuration, RxC, TxEN, CSN and COLL become active LOW. In addition, RxD is HIGH during idle, and RxC has a 1.2 μs discontinuity during signal acquisition.*

$\overline{LPBK}$/WDTD Loopback/Watchdog Timer Disable (Input):

Normal Operation: *For normal operation this pin should be HIGH or tied to V_{CC}. In normal operation the watchdog timer is enabled.*

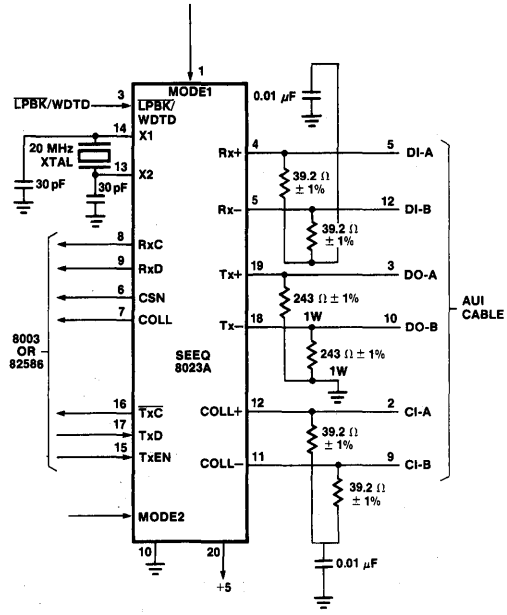


Figure 5. 8023A Interface

Loopback: *When this pin is brought low, the Manchester encoded transmit data from TxD and TxC is routed through the receiver circuit and sent back onto the RxD and RxC Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.*

Watchdog Timer Disable: *When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for longer than 25 ms, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx− lines. The watchdog timer is automatically reset each time TxEN is deasserted.*

Interconnection to a Data Link Controller

Figure 6 shows the interconnections between the 8023A MCC™ and SEEQ's 8003 EDLC™. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

Transmit Data, TxD
Transmit Clock, $\overline{TxC}$
Transmit Enable, TxEN
Collision, COLL

Receiver connections are:

Receive Data, RxD
Receive Clock, RxC
Carrier Sense, CSN

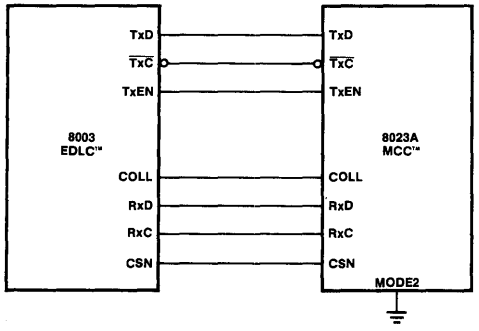


Figure 6. Interconnection of 8023A and 8003

Compatibility with Other LAN Controllers

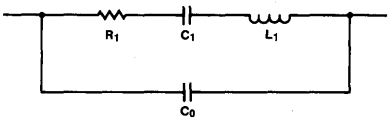
SEEQ's 8023A is compatible with other LAN Controllers, such as the 82586, when Pin 2 (MODE2) of the 8023A is floating or tied to V_{CC}. In this mode of operation, timing and polarity on the controller interface lines are compatible, with the 82586 specification dated March 1984.

Use of Time Domain Reflectometry in the 82586 is not recommended since the TDR transmission does not have a valid preamble.

D.C. and A.C. Characteristics and Timing

Crystal Specification

Resonant Frequency (C_L = 20 pF)	*20 MHz ± 0.005% 0–70° C and ± 0.003% at 25° C*
Type	*Fundamental Mode*
Circuit	*Parallel Resonance*
Load Capacitance (C_L)	*20 pF*
Shunt Capacitance (C_O)	*7 pF Max.*
Equivalent Series Resistance (R1)	*25 Ω Max.*
Motional Capacitance (C1)	*0.02 pF Max.*
Drive Level	*2 mW*



EQUIVALENT CIRCUIT OF CRYSTAL

Absolute Maximum Ratings*

Storage Temperature ..... −65° C to 150° C
All Input and Output Voltage ..... −0.3 to V_{CC} +0.3
V_{CC} ..... −0.3 to 7V
(Rx±, Tx±, COLL±) High Voltage Short Circuit Immunity ..... −0.3 to 16V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics $T_A = 0°C$ –70° C; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{IL}	Input Leakage Current (except MODE1, MODE 2 Receive and Collision Pairs)		10	µA	$0 \le V_{IN} \le V_{CC}$
	MODE1 and MODE2 Input Leakage Current		200	µA	$0 \le V_{IN} \le V_{CC}$
	Receive and Collision Pairs (Rx±, COLL±) Input Leakage Current		2	mA	$V_{IN} = 0$
I_{CC}	V_{CC} Current		100	mA	
V_{IL}	TTL Input Low Voltage	−0.3	0.8	V	
V_{IH}	TTL Input High Voltage (except X1)	2.0	V_{CC}	V	
	X1 Input High Voltage	3.5	V_{CC}	V	
V_{OL}	TTL Output Low Voltage except $\overline{TxC}$		0.4	V	$I_{OL} = 2.1$ mA
	$\overline{TxC}$ Output Low Voltage		0.4	V	$I_{OL} = 4.2$ mA
V_{OH}	TTL Output High Voltage (except RxC, $\overline{TxC}$, RxD	2.4		V	$I_{OH} = -400$ µA
	RxC, $\overline{TxC}$, RxD Output High Voltage	3.9		V	$I_{OH} = -400$ µA
V_{ODF}	Differential Output Swing	± 0.55	± 1.2	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{OCM}	Common Mode Output Voltage	$V_{CC} - 2.5$	$V_{CC} - 1$	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{BKSV}	Tx± Backswing Voltage During Idle		0.1	V	Shunt inductive load ≥ 27 µH
V_{IDF}	Input Differential Voltage (measured differentially)	±0.3	±1.2	V	
V_{ICM}	Input Common Mode Voltage	0	V_{CC}	V	
C_{IN}	Input Capacitance		15	pF	
C_{OUT}	Output Capacitance		15	pF	

A.C. Test Conditions

Output Loading TTL Output: — *1 TTL gate and 20 pF capacitor*

Differential Output: — *243Ω resistor and 10 pF capacitor from each pin to V_{SS} and a termination 78Ω resistor load resistor in parallel with a 27 µH inductor between the two differential output pins*

Differential Signal Delay Time Reference Level: — *50% point of swing*

Differential Output Rise and Fall Time: — *20% to 80% points*

RxC, $\overline{TxC}$, X1 High and Low Time: — *High time measured at 3.0V*
Low time measured at 0.6V

RxD, RxC, $\overline{TxC}$, X1 Rise and Fall Time: — *Measured between 0.6V and 3.0V points*

TTL Input Voltage (except X1): — *0.8V to 2.0V with 20 ns rise and fall time*

X1 Input Voltage: — *0.8V to 3.5V with 5 ns rise and fall time*

Differential Input Voltage: — *At least 300 mV with rise and fall time of 10 ns measured between -0.2V and +0.2V*

Transmit Timing $T_A = 0°C - 70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_6	$\overline{TxC}$ Cycle Time	99.99	100.01	ns
t_7	$\overline{TxC}$ High Time	40		ns
t_8	$\overline{TxC}$ Low Time	40		ns
t_9	$\overline{TxC}$ Rise Time		5	ns
t_{10}	$\overline{TxC}$ Fall Time		5	ns
t_{11}	TxEN Setup Time if Mode2=0 TxEN Setup Time if Mode 2=1	 55		 ns
t_{12}	TxD Setup Time if Mode2=0 TxD Setup Time if Mode2=1	40 55		ns ns
t_{13}	Bit Center to Bit Center Time	99.5	100.5	ns
t_{14}	Bit Center to Bit Boundary Time	49.5	50.5	ns
t_{15}	Tx+ and Tx- Rise Time	49.5	5	ns
t_{16}	Tx+ and Tx- Fall Time		5	ns
t_{17}	Transmit Active Time From The Last Positive Transition	200		ns
t_{17A}	From Last Positive Transition of the Transmit Pair to Differential Output Approaches	400	600	ns
t_{17B}	From Last Positive Transition of the Transmit Pair to Differential Output Approaches Within 40 mV of 0 V		7000	ns
t_{18}	Tx+ and Tx- Output Delay Time		65	ns
t_{19}	TxD Hold Time if Mode2=0 TxD Hold Time if Mode2=1	5 0		ns ns
t_{20}	TxEN Hold Time if Mode2=0 TxEN Hold Time if Mode1=1	5 0		ns ns

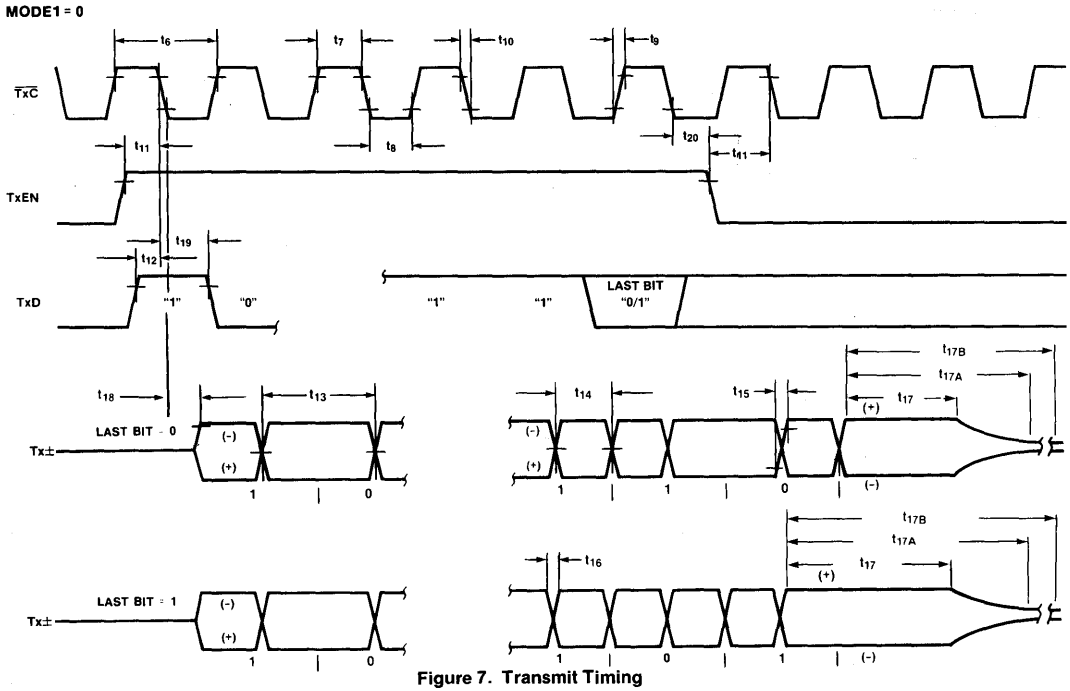


Figure 7. Transmit Timing

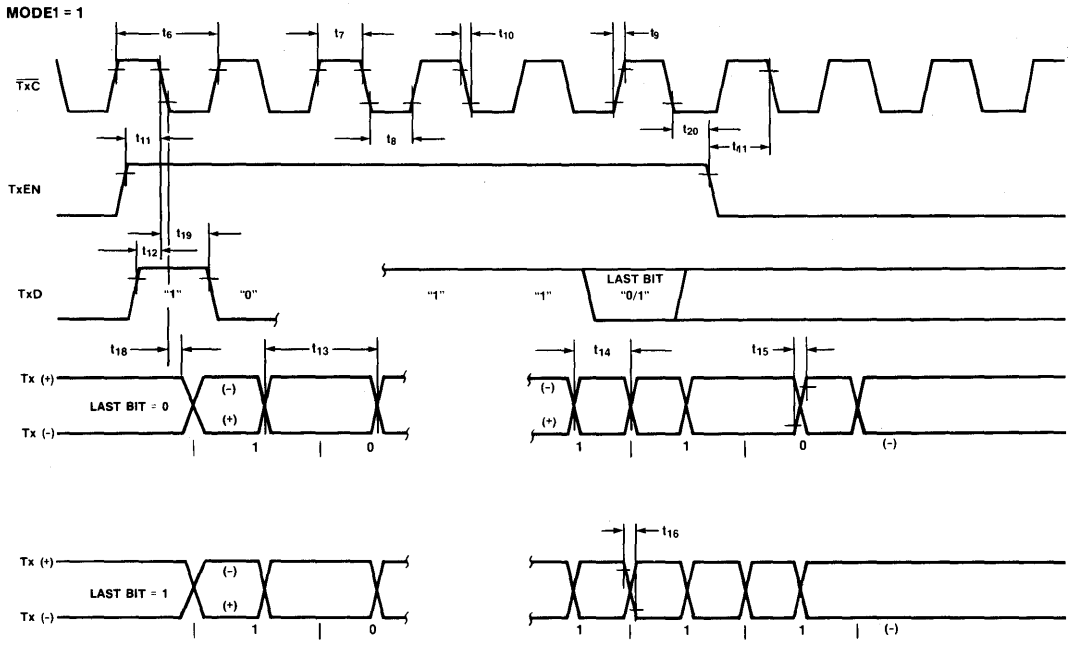


Figure 7. Transmit Timing

Receive Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{21}	CSN Asserts Delay Time		240	ns
t_{22}	CSN Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
t_{23}	CSN Asserts and Deasserts Delay Time	30	70	ns
t_{23A}	$\overline{CSN}$ Deassertion Delay Time	10	35	ns
t_{24}	RxD Delay Time	30	70	ns
t_{26}	RxC, $\overline{RxC}$ Rise and Fall Time		5	ns
t_{27}	During Clock Switch RxC Keeps High, $\overline{RxC}$ Keeps Low Time	40	200	ns
t_{28}	RxC, $\overline{RxC}$ High and Low Time	40		ns
t_{29}	RxC, $\overline{RxC}$ Clock Cycle Time (during data period)	95	105	ns
t_{30}	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	μs
t_{31}	Rx+/Rx– Rise and Fall Time		10	ns
t_{32}	$\overline{RxC}$ Held Low Duration from First Valid Negative-Going Transition	1.15	1.35	μs
t_{33}	$\overline{RxC}$ Stops Delay Time from First Valid Negative-Going Transition		240	ns
t_{34}	Rx+/Rx- Begin Return to Zero from Last Positive-Going Transition	160		ns
t_{35}	RxD Rise Time		10	ns
t_{36}	RxD Fall Time		10	ns

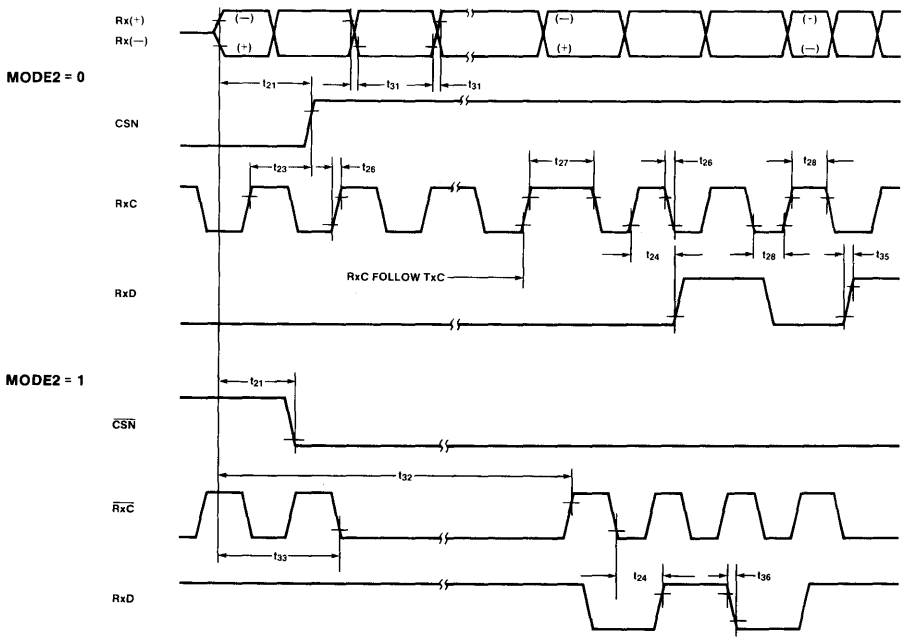


Figure 9. Receive Timing — Start of Packet

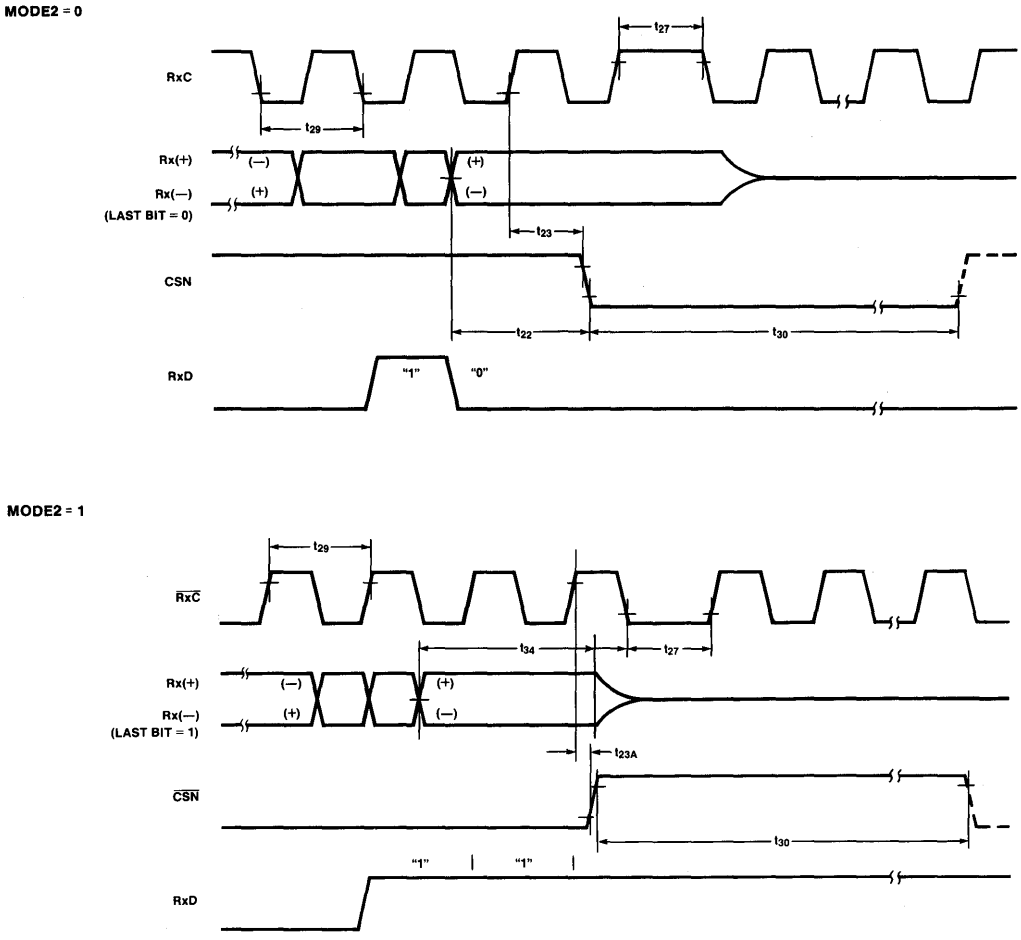


Figure 10. Receive Timing — End of Packet

Collision Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{51}	COLL+/COLL— Cycle Time	86	118	ns
t_{52}	COLL+/COLL— Rise and Fall Time		10	ns
t_{53}	COLL+/COLL— High and Low Time	35	70	ns
t_{54}	COLL+/COLL— Width (measured at –0.3V)	26		ns
t_{55}	COLL Asserts Delay Time		100	ns
t_{56}	COLL Deasserts Delay Time		180	ns
t_{57}	CSN Asserts Delay Time		200	ns
t_{58}	CSN Deasserts Delay Time		280	ns

Notes:

1. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If COLL+ and COLL- arrives within 4.5μs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 μs.
5. If MODE2 = 1, then COLL and CSN are inverted.

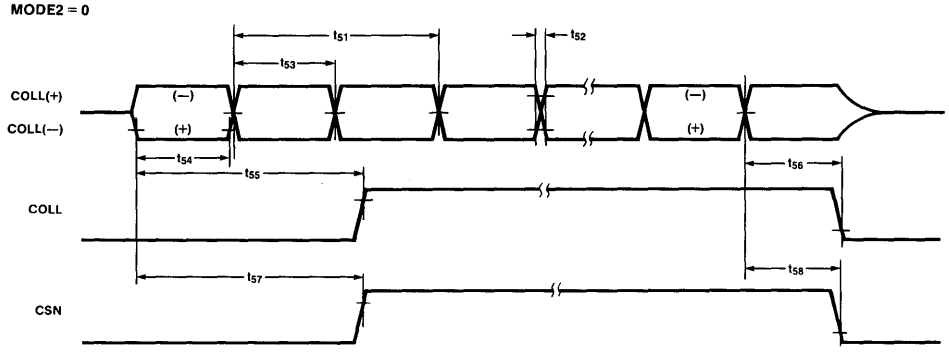


Figure 11. Collision Timing

20 MHz TTL Clock Input Timing $T_A = 0°C - 70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_1	X1 Cycle Time	49.995	50.005	ns
t_2	X1 High Time	15		ns
t_3	X1 Low Time	15		ns
t_4	X1 Rise Time		5	ns
t_5	X1 Fall Time		5	ns
t_6	X1 to $\overline{TxC}$ Delay Time	10	30	ns

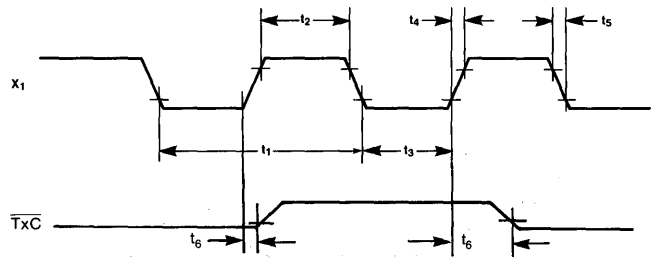


Figure 12. 20 MHz TTL Clock Timing

Loopback Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{61}	LPBK Setup Time	500		ns
t_{62}	LPBK Hold Time	5		μs
t_{63}	In Collision Simulation, COLL Signal Delay Time	475	625	ns
t_{64}	COLL Duration Time	600	750	ns

Note:

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period. RxC is low for 1.2 μs (max). RxD = 0 if MODE2 = 0. RxD = 1 if MODE2 = 1.

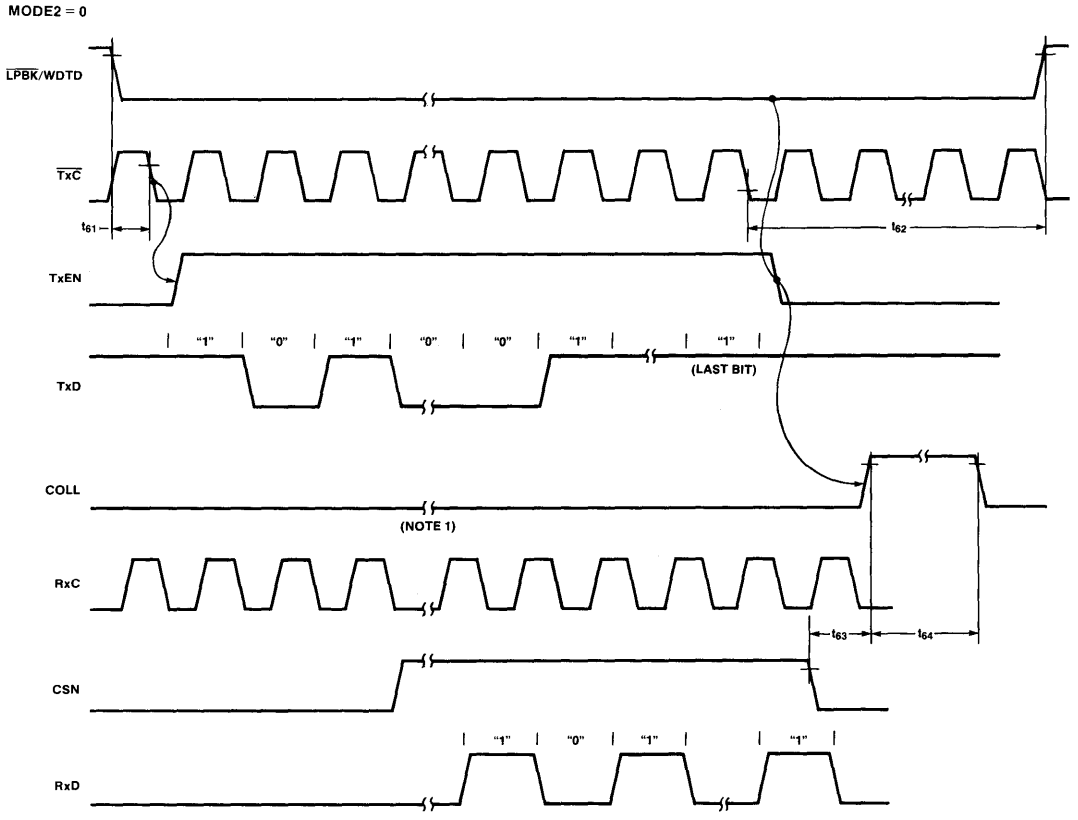


Figure 13. Loopback Timing

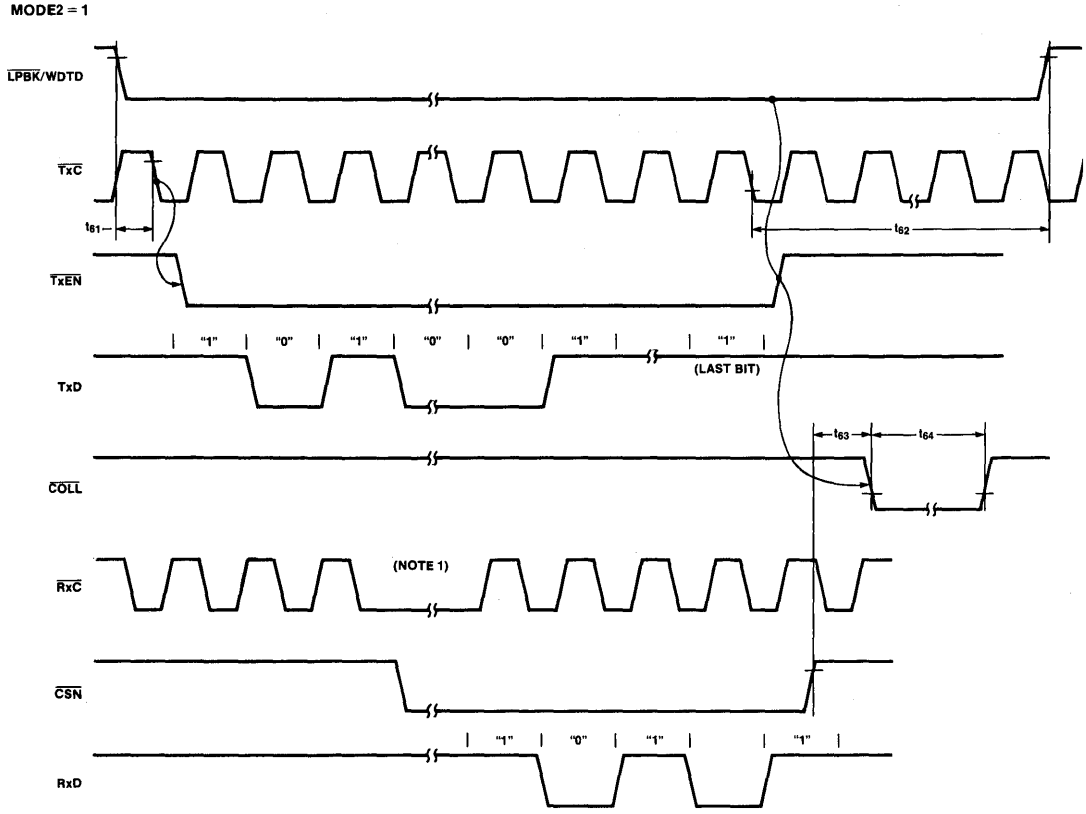


Figure 14. Loopback Timing — (Cont.)

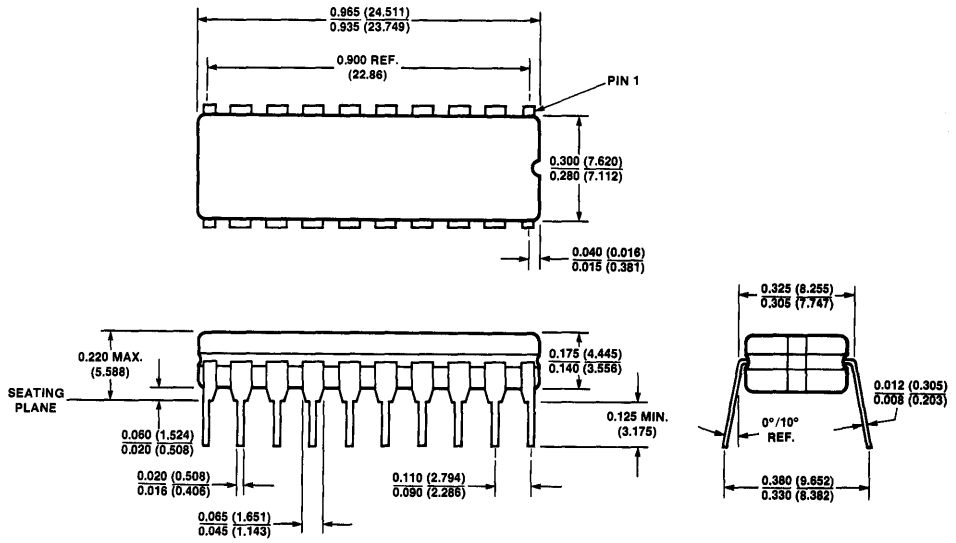
Ordering and Package Information

PART NUMBER

D Q 8023

- 8023 — PRODUCT: MCC™ MANCHESTER CODE CONVERTER
- Q — TEMPERATURE RANGE: 0° C TO 70° C
- D — PACKAGE: CERDIP

20-LEAD HERMETIC CERDIP
PACKAGE TYPE D



NOTES:
1. FOR SOLDER DIPPED LEADS, THICKNESS WILL BE 0.020 MAX.
2. ALL DIMENSIONS ARE IN INCHES AND (MILLIMETERS).

SECTION 4

MILITARY AND INDUSTRIAL TEMPERATURE RANGE

M2764/M27128
(Military Temperature Range)

E2764/E27128
(Extended Temperature Range)

2764/27128 UV EPROM

June 1985

Features

- **Military and Extended Temperature Range**
  - **-55 to +125°C: M2764 (5133)**
  - **-55 to +125°C: M27128 (5143)**
  - **-40 to +85°C: E2764/E27128**
- **250 ns Access Times at -55 to 125°C**
- **Programmed Using Intelligent Algorithm**
- **21 V V_{PP} Programming Voltage**
- **JEDEC Approved Bytewide Pin Configuration**
  - **2764 8K x 8 Organization**
  - **27128 16K x 8 Organization**
- **Low Power Dissipation**
  - **120 mA Active Current**
  - **40 mA Standby Current**
- **Silicon Signature™**

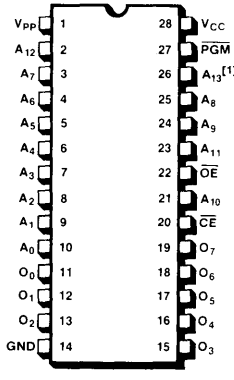
Description

SEEQ's 2764 (5133) and 27128 (5143) are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are specified over the military and extended temperature range and have access times as fast as 250 ns over the V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 120 mA and 40 mA respectively. The 250 ns allows higher system efficiency by eliminating the need for wait states in today's 8- or 16-bit microcomputers.

Pin Configurations

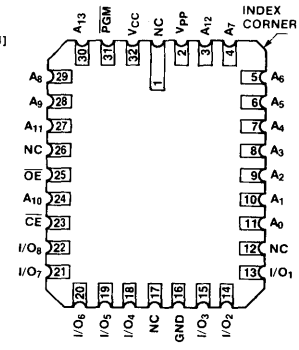
DUAL-IN-LINE
TOP VIEW

2764/27128



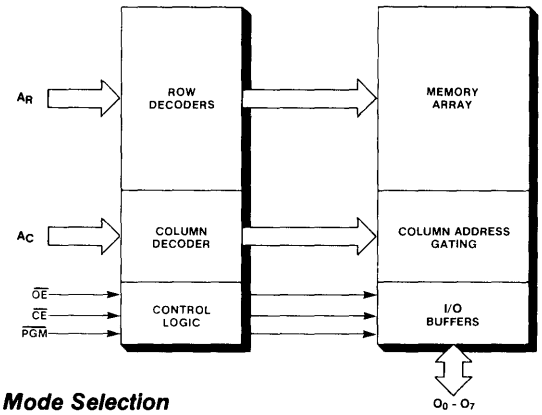
PIN 26 IS A NO CONNECT
ON THE DIP 2764

LEADLESS CHIP CARRIER
BOTTOM VIEW



PIN 30 IS A NO CONNECT
ON THE LCC 2764

Block Diagram



Mode Selection

PINS / MODE	CE (20)	OE (22)	PGM (27)	VPP (1)	VCC (28)	Outputs (11-13, 15-19)
Read	VIL	VIL	VIH	VCC	VCC	DOUT
Output Disable	X	VIH	VCC	VCC	VCC	High Z
Standby	VIH	X	X	VCC	VCC	High Z
Program	VIL	VIH	VIL	VPP	VCC	DIN
Program Verify	VIL	VIL	VIH	VPP	VCC	DOUT
Program Inhibit	VIH	X	X	VPP	VCC	High Z
Silicon Signature™*	VIL	VIL	VIH	VCC	VCC	Encoded Data

X can be either V_{IL} or V_{IH}

*For Silicon Signature™: A_0-A_3 is toggled. A_4 = V_{IL}7, A_9 = 12V, all other addresses are at any TTL level.
Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

AC	ADDRESSES — COLUMN (LSB)
AR	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O0 - O7	OUTPUTS
PGM	PROGRAM

MILITARY

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{PP} and a TTL "0" to pin 27 (program pin). They may be programmed with an intelligent algorithm that is now available on commercial programmers. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, the 27128 and the 2764 may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on the 27128 and 2764 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -65° C to +135° C
All Inputs or Outputs with
Respect to Ground ..... +7V to -0.6V
V_{PP} During Programming with
Respect to Ground ..... +22V to -0.6V
Voltage on A_9 with
Respect to Ground ..... +15.5V to -0.6V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2764-25, M2764-45 M27128-25, M27128-35	E2764-35 E27128-25
V_{CC} Supply Voltage[1]	5 V ± 10%	5 V ± 10%
Temperature Range (Read Mode)	–55 to 125° C	–40 to 85° C
V_{PP} During Programming	21 ± 0.5 V	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current		10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current		10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[2]	V_{PP} Current Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
	Prog. Mode (25° C)		30	mA	V_{PP} = 21.5V
I_{CC1}[2]	V_{CC} Standby Current		40	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Active Current		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current is the sum of I_{CC} and I_{PP}.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)						Test Conditions
		2764-25 27128-25		27128-35		2764-45		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Data Valid		250		350		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		250		350		450	$\overline{OE} = V_{IL}$
t_{OE}[2]	Output Enable to Data Valid		100		125		150	$\overline{CE} = V_{IL}$
t_{DF}[1,3]	Output Enable to Output Float	0	85	0	105	0	130	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable, whichever occurred first	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

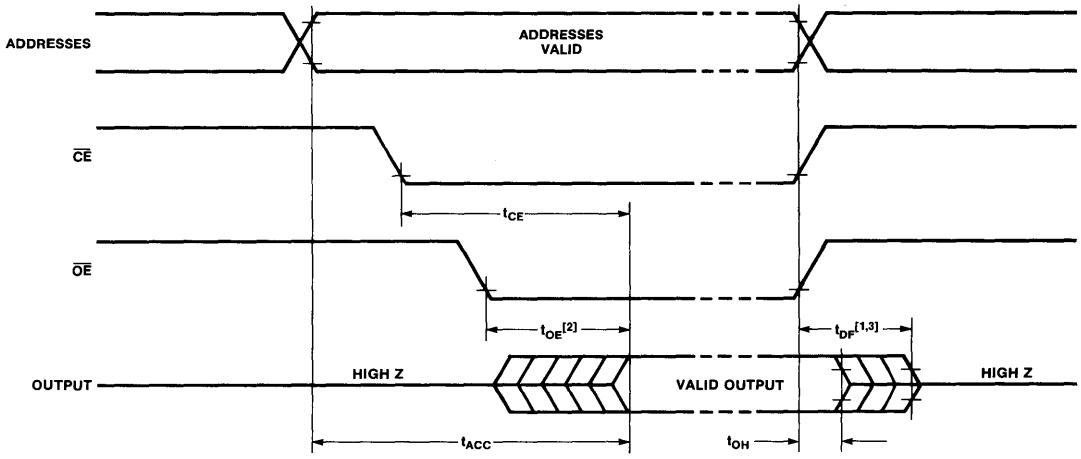
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Equivalent A.C. Test Conditions[4]

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

MILITARY

Erasure Characteristics

The 2764 and 27128 are erased using ultraviolet light which has a wavelenght of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. Silicon Signature allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds programming.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column address A_0. There are 2 bytes of data available. The data (see Table 2) appears on outputs O_0 to O_6, with O_7 used as an odd parity bit. This mode is functional at 25 ± 5° C ambient temperature.

Table 2. Silicon Signature Bytes

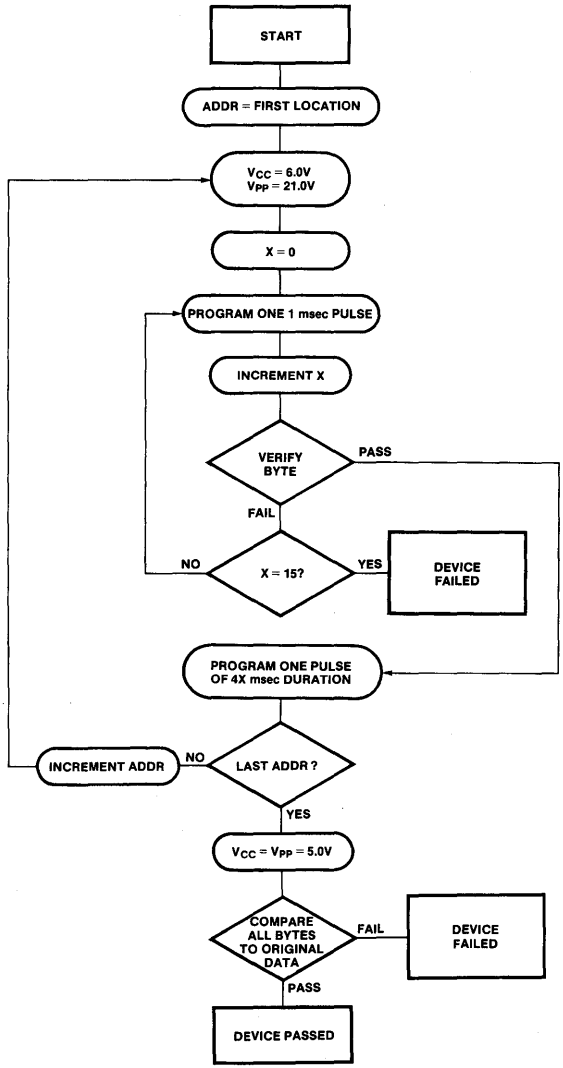
	A_0	Data (Hex)
SEEQ Code (Byte 0)	**V_{IL}**	**94**
Product Code (Byte 1)		
2764	V_{IH}	40
27128	V_{IH}	C1

Programming

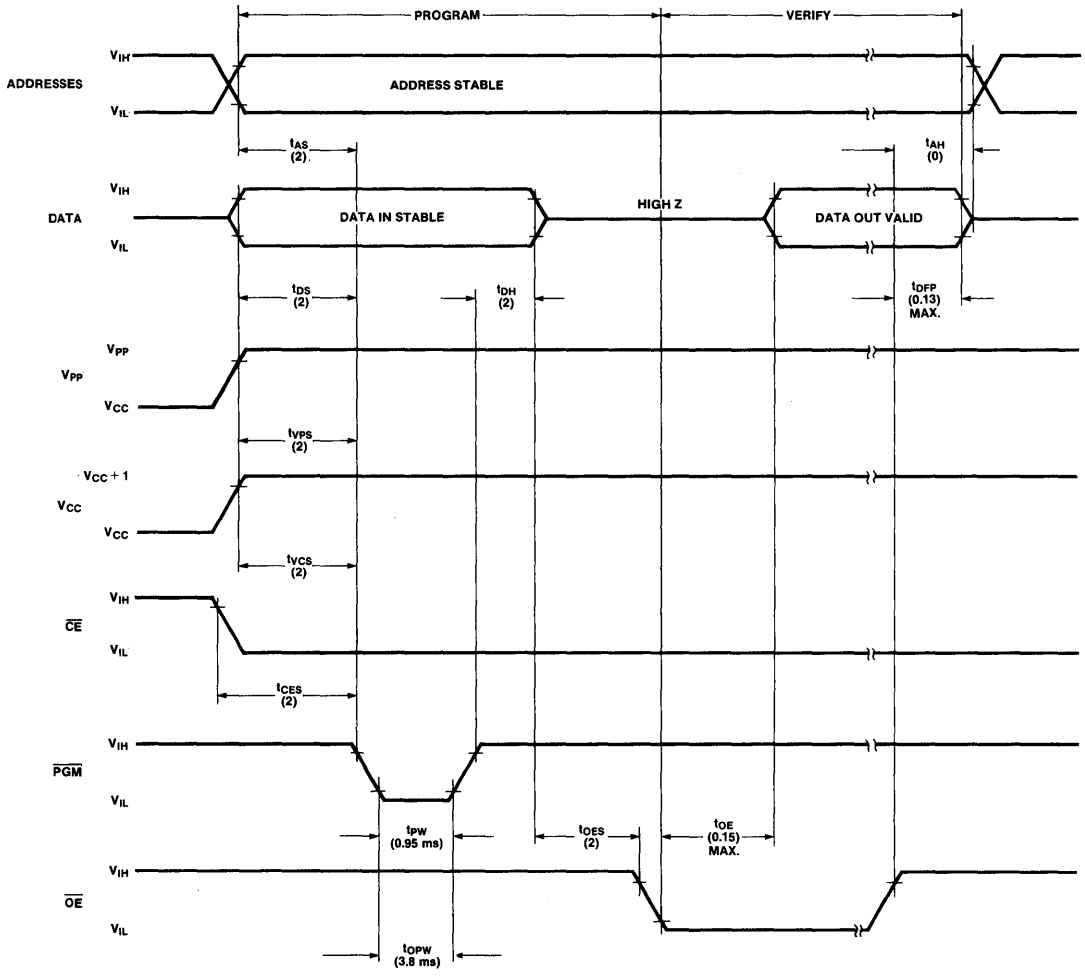
The EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm.

The intelligent algorithm requires V_{CC} = 6V and V_{PP} = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additional given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at V_{CC} = V_{PP} = 5V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A V_{IL} AND 2V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

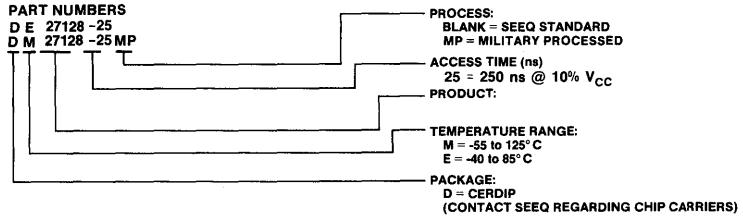
Intelligent Algorithm

AC Programming Characteristics $T_A = 25 \pm 5°C$, V_{CC}[1, 4] $= 6.0V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	OE Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}[2]	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3, 4]	$\overline{PGM}$ Overprogram Pulse Width	3.8		63	ms
t_{CES}	$\overline{CE}$ Setup Time	2			μs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Initial Program Pulse width tolerance is 1 msec ± 5%.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, V_{CC} = 5 V ± 5%, T_{PW} = 50 ms ± 10%, and T_{OPW} is not applicable.

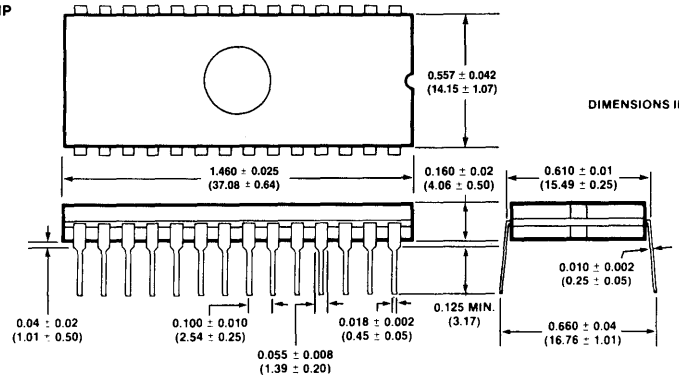
Ordering Information



Packaging Information

28-LEAD HERMETIC CERDIP PACKAGE TYPE D

(For the 32 pin leadless chip carrier, see M27C256 data sheet)

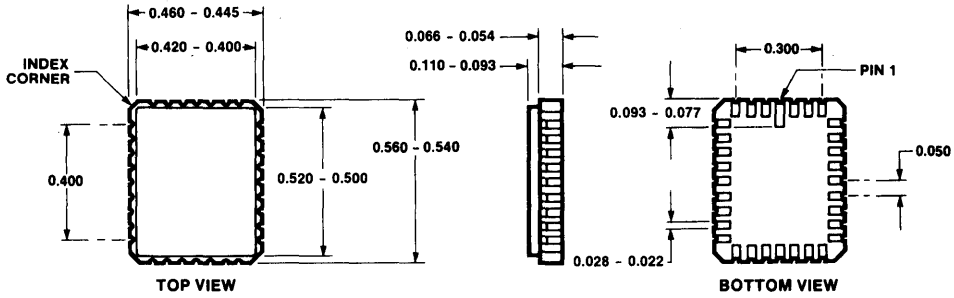


DIMENSIONS IN INCHES AND (MILLIMETERS)

Country Assembly Code (Backside Marking)

K = KOREA, P = PHILIPPINES, T = TAIWAN

LEADLESS CHIP CARRIER 32 PIN PACKAGE



M27256
256K EPROM

August 1985

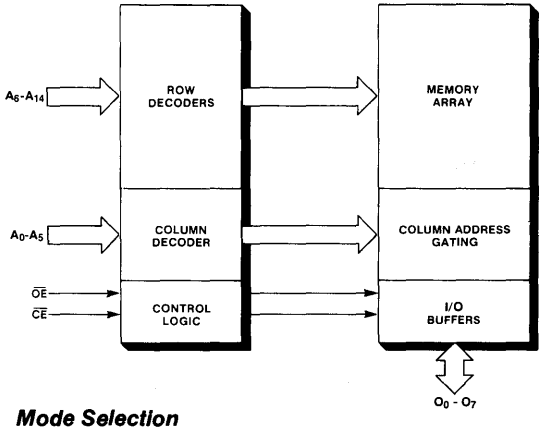
Features

- **256K (32K x 8) EPROM**
- **250 ns Access Times**
  - **— 5 V±10% V_{CC}**
  - **— -55 to 125° C Temperature Range**
- **Low Power**
  - **— 40 mA Max. V_{CC} Standby Current**
  - **— 70 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **—12.5 V_{PP}**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature™**

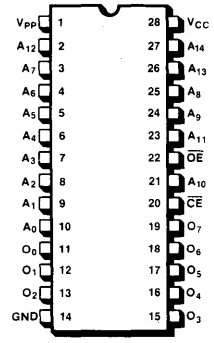
Description

SEEQ's M27256 is a 256K ultraviolet light erasable EPROM. It is organized as 32K x 8, operates from a single 5V supply, and programs using a 12.5V intelligent algorithm. The M27256's operating conditions are specified over the -55 to +125° C temperature range and at 5V ±10% V_{CC}. The active power is only 70 mA, approximately 30% lower than other compatible NMOS 256K EPROMS. Consequently, memory system sizes can be increased with a substantial savings in power, resulting in lower power supply cost and inherently greater system reliability. For systems requiring even lower power, a 40 mA active power CMOS 27C256 is available from SEEQ. The M27256's low active power is achieved without sacrificing performance. The access time is 250 nsec, making it compatible with most of today's microcomputers. Wait states can be eliminated with the 250 nsec access times.

Block Diagram



Pin Configuration



Mode Selection

MODE \ PINS	CE (20)	OE (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.

* For Silicon Signature™: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

MILITARY

An intelligent algorithm is used to program the M27256. Data is programmed using a 12.5V V_{PP} and an initial chip enable pulse of 1 msec. Initially, and after erasure, all bits are in the "1" state. The typical programming time is under five minutes. Programming is available from commercial programmers and is compatible with other 256K EPROM intelligent algorithms.

Incorporated on the M27256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. The product code is used by a programmer to identify the programming algorithm for the M27256.

Absolute Maximum Ratings

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −65° C to +135° C
All Inputs or Outputs with Respect to Ground ..... +7 V to −0.6 V
V_{PP} with Respect to Ground ..... +14.0 V to −0.6 V
Voltage on A_9 with Respect to Ground ..... +14.0 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M272256-25, M272256-30
V_{CC} Supply Voltage[1]	5 V ±10%
Temperature Range (Read Mode)	-55 to 125°C
V_{PP} During Read[2]	V_{CC}
V_{PP} During Programming[3]	12.5 ±0.3 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current		10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current		10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}	V_{PP} Current Read Mode		100	µA	$V_{PP} = V_{CC}$ Max.
	Prog. Mode		30	mA	V_{PP} = 12.5 V
I_{CC1}	V_{CC} Standby Current		40	mA	$\overline{CE} \geq V_{IH}$
I_{CC2}	V_{CC} Active Current		70	mA	$\overline{CE} = \overline{OE} = V_{IL}$,
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 µF ceramic capacitor on V_{PP} is required during programming only to suppress voltage transients.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)				Test Conditions
		M27256-25		M27256-30		
		Min.	Max.	Min.	Max.	
T_{ACC}	Address to Data Valid		250		300	$\overline{CE} = \overline{OE} = V_{IL}$
T_{CE}	Chip Enable to Data Valid		250		300	$\overline{OE} = V_{IL}$
T_{OE}[2]	Output Enable to Data Valid		100		120	$\overline{CE} = V_{IL}$
T_{DF}[3]	Output Enable or Chip Enable to Output Float	0	60	0	105	$\overline{CE} = V_{IL}$
T_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		$\overline{CE} = \overline{OE} = V_{IL}$

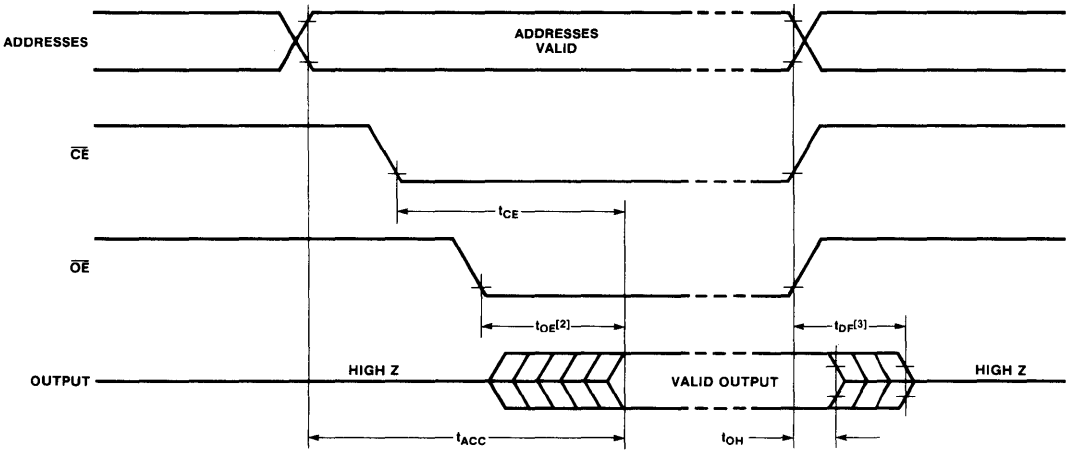
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Equivalent A.C. Test Conditions[4]

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

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Erasure Characteristics

The 27256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

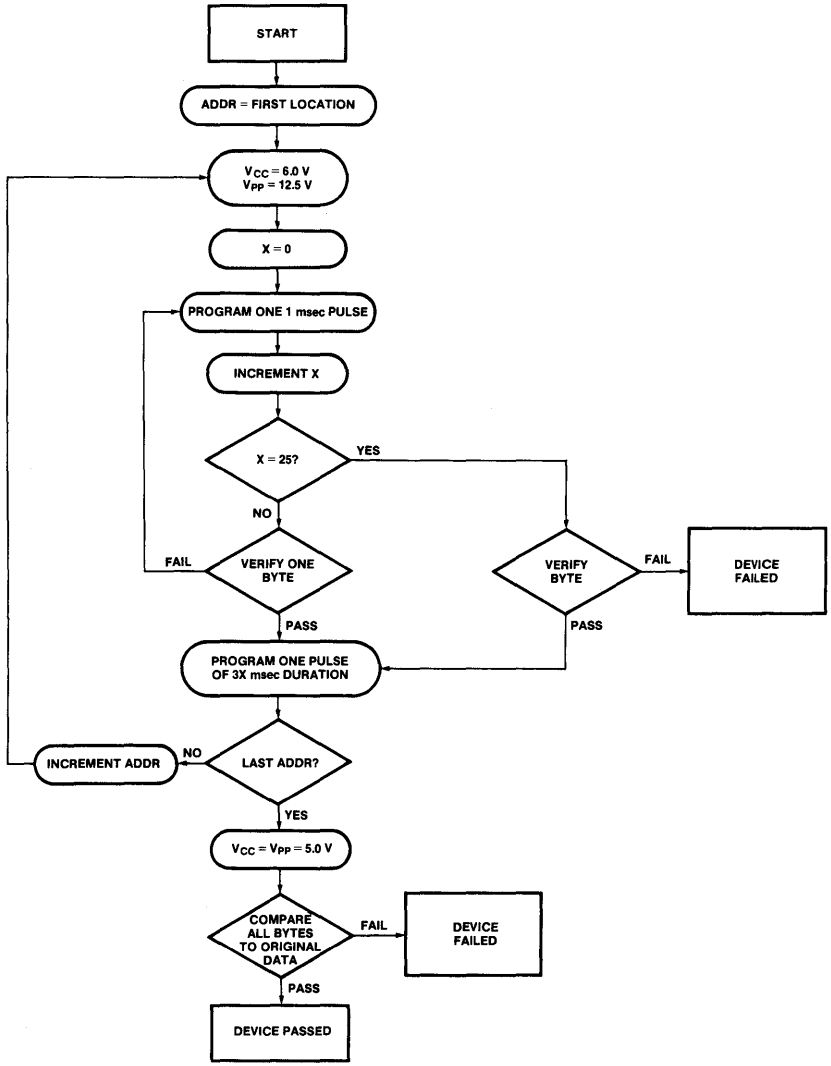
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

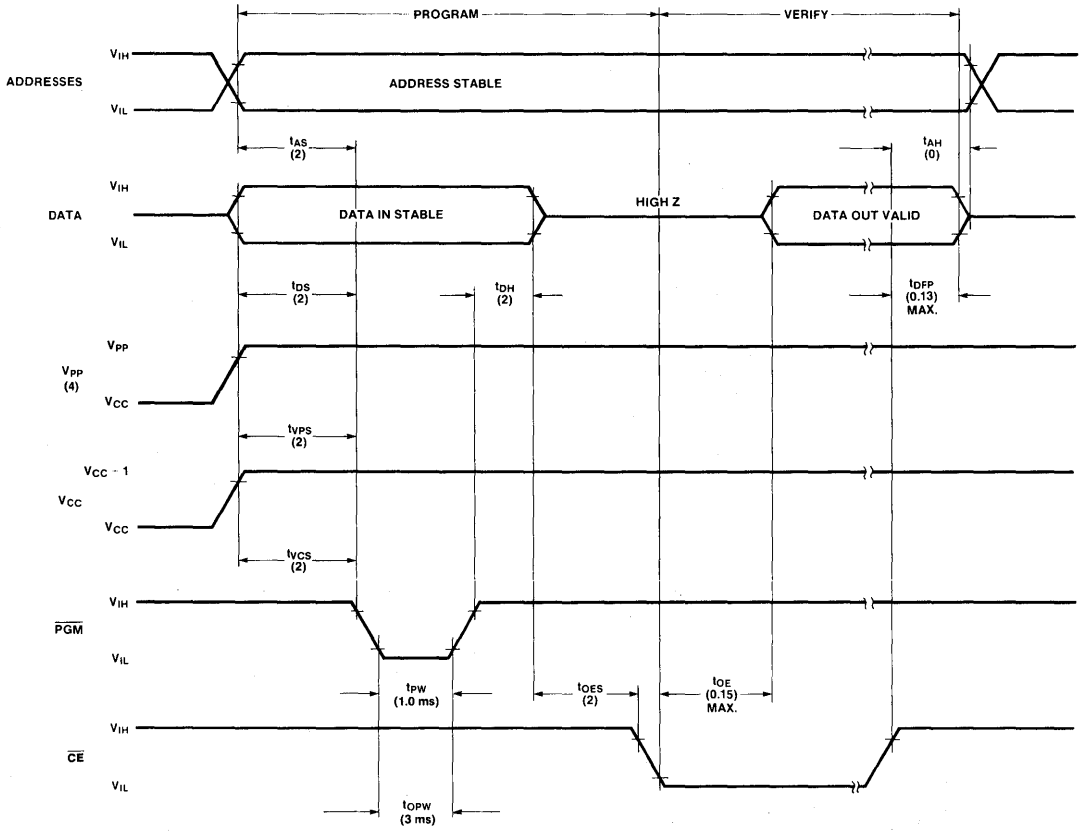
The 27256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires $V_{CC} = 6$ V and $V_{PP} = 12.5$ V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5$ V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY TO SUPPRESS VOLTAGE TRANSIENTS.

Intelligent Algorithm

AC Programming Characteristics $T_A = 25 \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$, $V_{PP} = 12.5V$

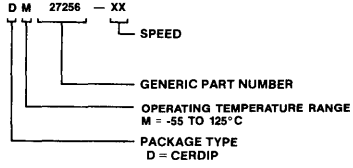
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	$\overline{OE}$ Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*AC Conditions of Test

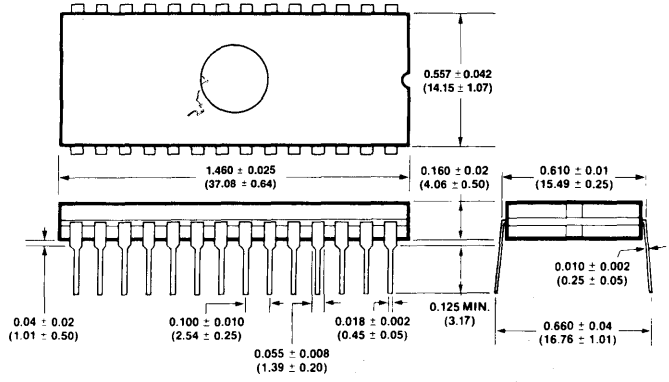
Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering and Package Information



28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

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M27C256
256K CMOS EPROM

August 1985

Features

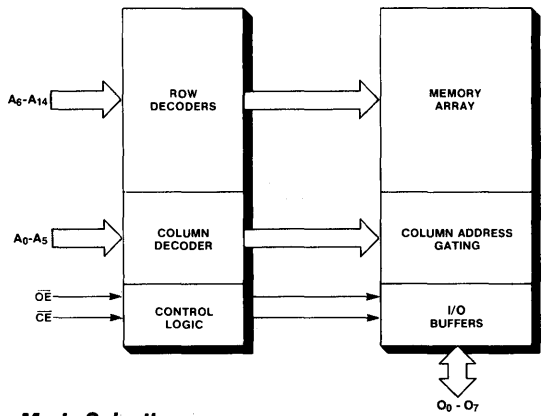
- **256K (32K x 8) CMOS EPROM**
- **Ultra Low Power**
  - **100 μA Max. V_{CC} Standby Current**
  - **40 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **12.5 V_{PP}**
- **250 ns Access Times**
  - **5 V ±10% V_{CC}**
  - **-55 to 125° C Temperature Range**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature™**

Description

SEEQ's M27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its 40 mA active current is less than one half the active power of n-channel EPROMs. In addition the 100μA V_{CC} standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

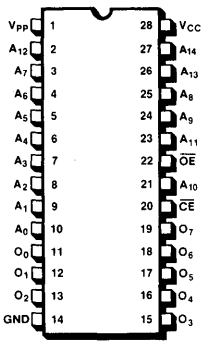
The M27C256 is specified over the -55 to +125° C temperature range and at 5 V±10% V_{CC}. The access time is specified at 250 ns, making the M27C256 compatible with most of today's microcomputers. Its inputs and outputs are completely TTL compatible.

Block Diagram

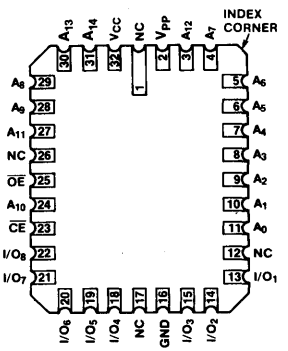


Pin Configuration

DUAL IN-LINE



LEADLESS CHIP CARRIER BOTTOM VIEW



Mode Selection

MODE \ PINS	CE (20)	OE (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	Vcc	Vcc	DOUT
Output Disable	X	V_{IH}	Vcc	Vcc	High Z
Standby	V_{IH}	X	Vcc	Vcc	High Z
Program	V_{IL}	V_{IH}	VPP	Vcc	DIN
Program Verify	V_{IH}	V_{IL}	VPP	Vcc	DOUT
Program Inhibit	V_{IH}	V_{IH}	VPP	Vcc	High Z
Silicon Signature™*	V_{IL}	V_{IL}	Vcc	Vcc	Encoded Data

X can be either V_{IL} or V_{IH}.

*For Silicon Signature™: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
NC	NO CONNECT

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the M27C256 typically in four minutes. Data is programmed using a 12.5 V V_{PP} and an initial chip enable pulse of 1.0 ms.

Incorporated on the M27C256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −65° C to +135° C
All Inputs or Outputs with
Respect to Ground ..... +7 V to −0.6 V
V_{PP} with Respect to Ground ..... +14.0 V to −0.6 V
Voltage on A_9 with
Respect to Ground ..... +14.0 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M27C256-25, M27C256-30
V_{CC} Supply Voltage[1]	5 V ±10%
Temperature Range (Read Mode)	-55 to 125°C
V_{PP} During Read[2]	V_{CC}
V_{PP} During Programming[3]	12.5 ±0.3 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}	V_{PP} Current	Read Mode		100	µA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	V_{PP} = 12.5 V
I_{CC1}	V_{CC} Standby Current			100	µA	$\overline{CE} \geq V_{CC}$ -1 V
I_{CC2}	V_{CC} Standby Current			1	mA	$\overline{CE} \geq V_{IH}$
I_{CC3}	V_{CC} Active Current			40	mA	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz, I_O = 0
V_{IL}	Input Low Voltage		−0.1	0.8	V	
V_{IH}	Input High Voltage		2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −400 µA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 µF ceramic capacitor on V_{PP} is required during programming only to suppress voltage transients.

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AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)				Test Conditions
		M27C56-25		M27C56-30		
		Min.	Max.	Min.	Max.	
T_{ACC}	Address to Data Valid		250		300	$\overline{CE} = \overline{OE} = V_{IL}$
T_{CE}	Chip Enable to Data Valid		250		300	$\overline{OE} = V_{IL}$
T_{OE}[2]	Output Enable to Data Valid		100		120	$\overline{CE} = V_{IL}$
T_{DF}[3]	Output Enable or Chip Enable to Output Float	0	60	0	105	$\overline{CE} = V_{IL}$
T_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		$\overline{CE} = \overline{OE} = V_{IL}$

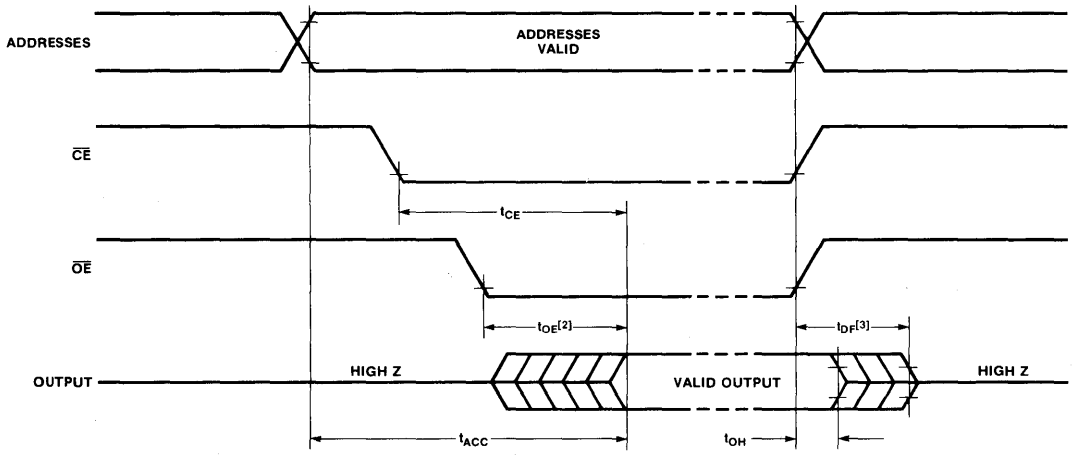
Capacitance[2]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Equivalent A.C. Test Conditions[4]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

Erasure Characteristics

The M27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

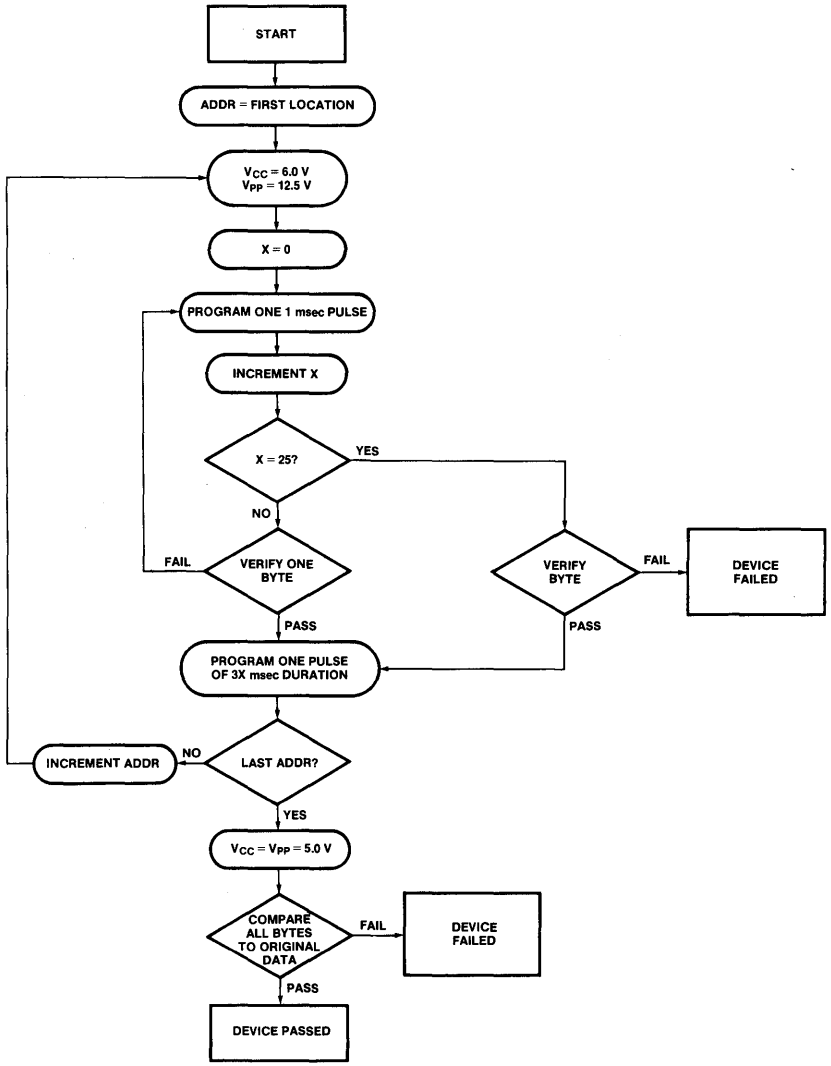
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

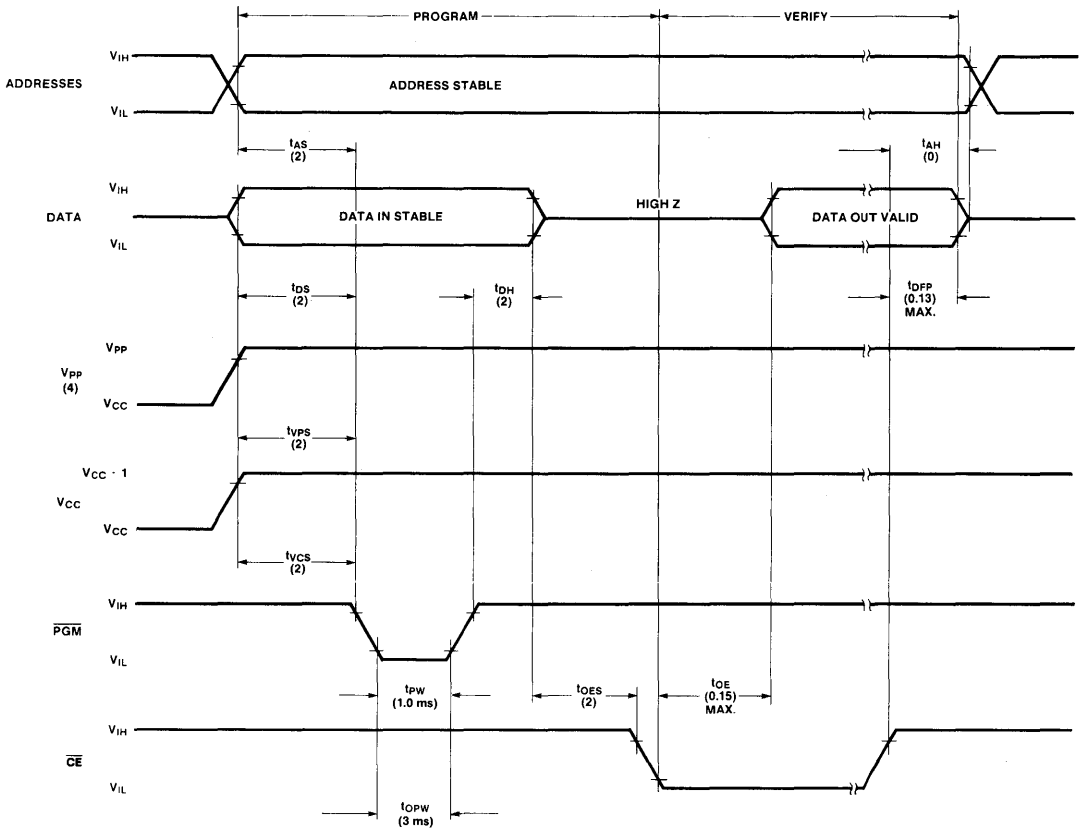
The M27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires $V_{CC} = 6$ V and $V_{PP} = 12.5$ V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5$ V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY TO SUPPRESS VOLTAGE TRANSIENTS.

MILITARY

Intelligent Algorithm

AC Programming Characteristics $T_A = 25 \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$, $V_{PP} = 12.5V$

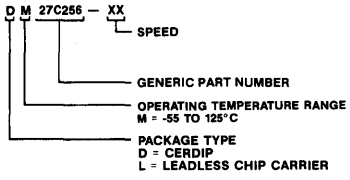
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			µs
t_{OES}	$\overline{OE}$ Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			µs
t_{VCS}	V_{CC} Setup Time	2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*AC Conditions of Test

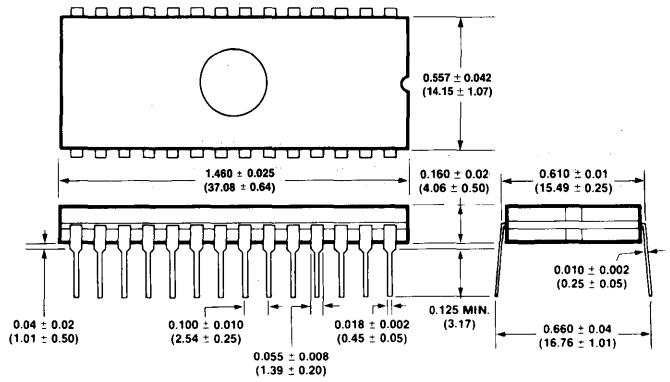
Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering and Package Information

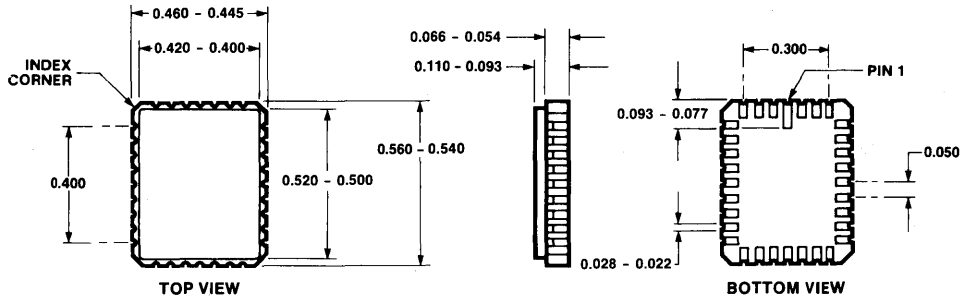


28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

LEADLESS CHIP CARRIER 32 PIN PACKAGE



M2816A
Timer E^2
16K Electrical Erasable ROMs

August 1985

Features

- **High Endurance Write Cycles**
  - **2816A: 10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement to 2K x 8 E^2ROMs**
  - **21 V 2816**
  - **5 V Timer 2816A**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA max. Active Current**
  - **40 mA max. Standby Current**
- **JEDEC Approved Byte-Wide Pinout**

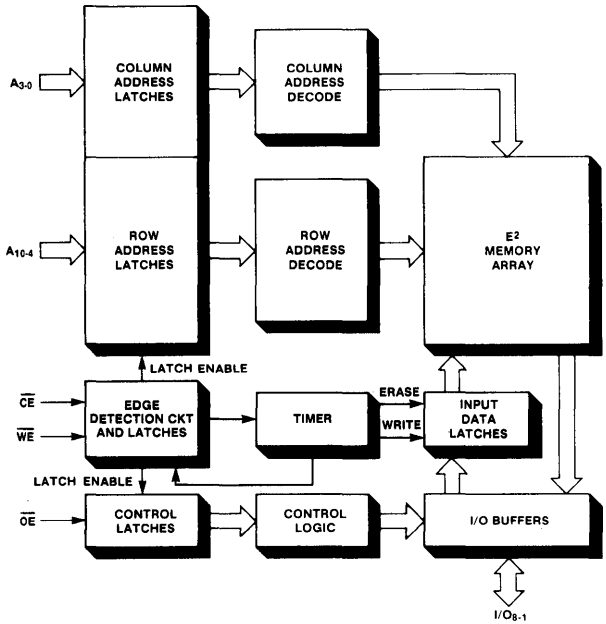
Description

SEEQ's M2816A is a 5 V only, 2K x 8 electrically erasable read only memory (E^2ROM). E^2ROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is 10 thousand for the M2816A. The M2816A's high endurance was accomplished using SEEQ's proprietary oxynitride E^2ROM process and its innovative "Q cell™" design. The M2816A is ideal for systems that require frequent updates.

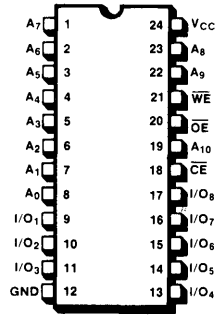
There is an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

for other tasks during the write time. The M2816A's write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

The E²ROM is ideal for systems with limited board area. For systems where cost is important or higher density is required, SEEQ has a latch only "52B" family at 16K and 64K bit densities. The "52B" family has the same JEDEC approved pin configuration but without the on-chip timer. All "52B" family inputs are latched by the falling edge of the write enable signal.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

The chip erase mode clears all data to a TTL high in one 9 ms cycle. This is accomplished by raising both $\overline{WE}$ and $\overline{OE}$ to a high voltage (e.g. 21 V) and having all the data inputs at a TTL high. In addition an optional 21 V byte write (preceded by a byte erase) mode is available.

Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}*	D_{IN}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z
Chip Erase	V_{IL}	V_{ER}	V_{ER}	V_{IH}

*A 21 V input on $\overline{WE}$ is an optional mode.

Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -65° C to +135° C

All Inputs or Outputs with
Respect to Ground ..... +6V to −0.3V

$\overline{WE}$ During Writing/Erasing with
Respect to Ground ..... +22.5V to −0.3V

Duration of $\overline{WE}$ Supply at 22V
During W/E Inhibit ..... 24 Hours

Recommended Operating Conditions

Temperature Range: ..... -55° C to +125° C
V_{CC} Power Supply: ..... 5V ±10%
Q (Maximum Endurance/Byte): ..... 10,000 cycles

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		125	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O's Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode	12	22	V	I_{ER} = 10 µA

MILITARY

AC Characteristics (Over the operating V_{CC} and temperature range)

Read Operation

Symbol	Parameter	Limits (ns)				Units
		M2816A-250		M2816A-350		
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		350		ns
t_{CE}	Chip Enable Access Time		250		350	ns
t_{AA}	Address Access Time		250		350	ns
t_{OE}	Output Enable Access Time		90		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		ns
t_{HZ}	$\overline{CE}$to Output in High Z	10	100	10	100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	50		50		ns
t_{PU}	$\overline{CE}$ to Power-up Time	0		0		ns
t_{PD}	$\overline{CE}$ to Power Down Time		50		50	ns

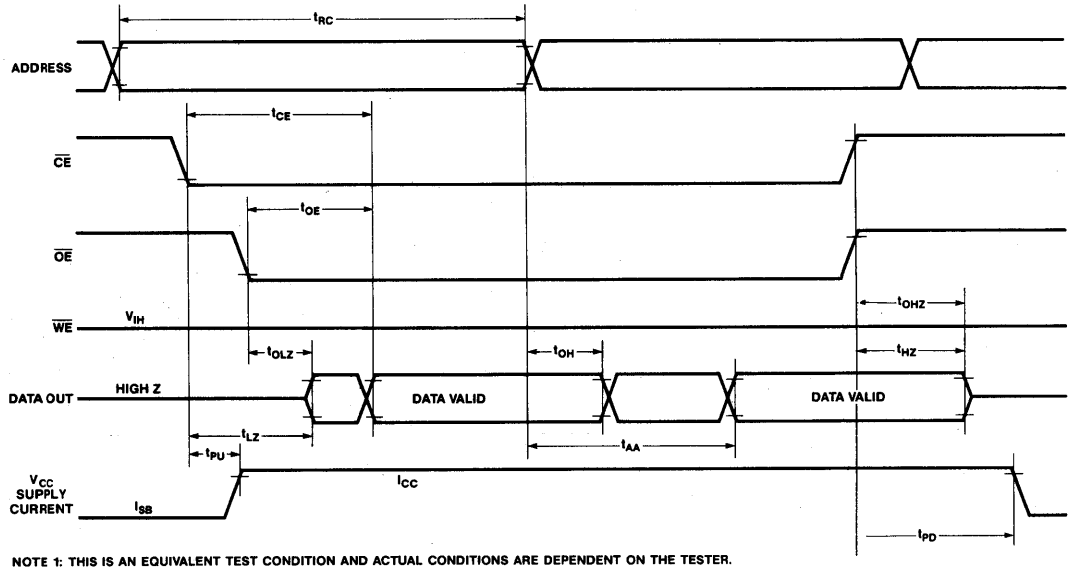
Capacitance $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Cap,	10 pF	$V_{I/O} = 0$ V

Equivalent A.C. Test Conditions[1]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

READ CYCLE TIMING



NOTE 1: THIS IS AN EQUIVALENT TEST CONDITION AND ACTUAL CONDITIONS ARE DEPENDENT ON THE TESTER.

AC Characteristics (Over the operating V_{CC} and temperature range)

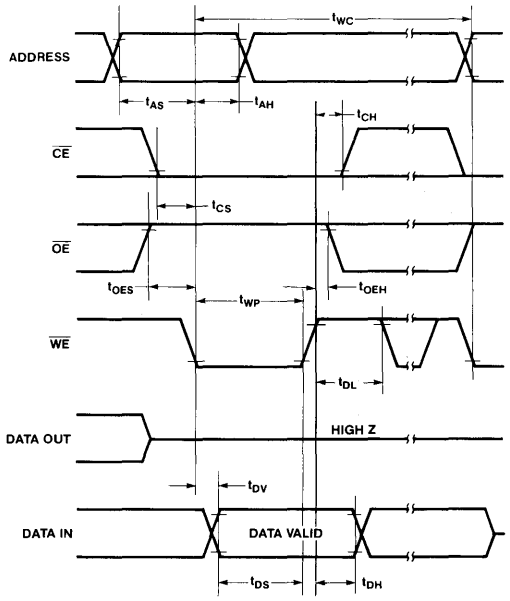
TTL WRITE CYCLE

Symbol	Parameter	Limits (ns)				Units
		M2816A-250		M2816A-350		
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10		10		ms
t_{AS}	Address Set Up Time	10		10		ns
t_{AH}	Address Hold Time	50		70		ns
t_{CS}	Write Set Up Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ to End of Write Input	150		150		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	μs
t_{DS}	Data Set Up Time	20		50		ns
t_{DH}	Data Hold Time	20		20		ns

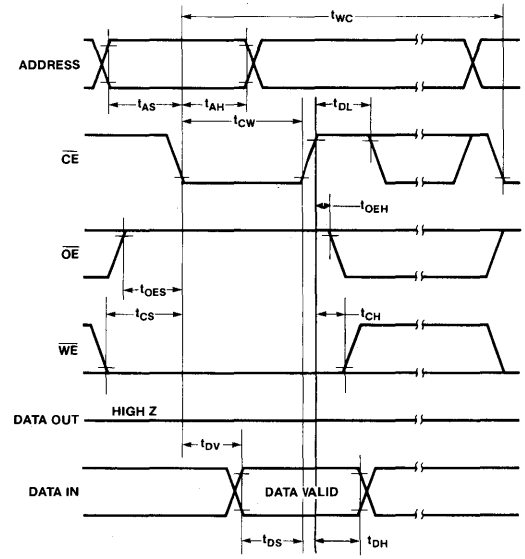
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

TTL Byte Write Cycle

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



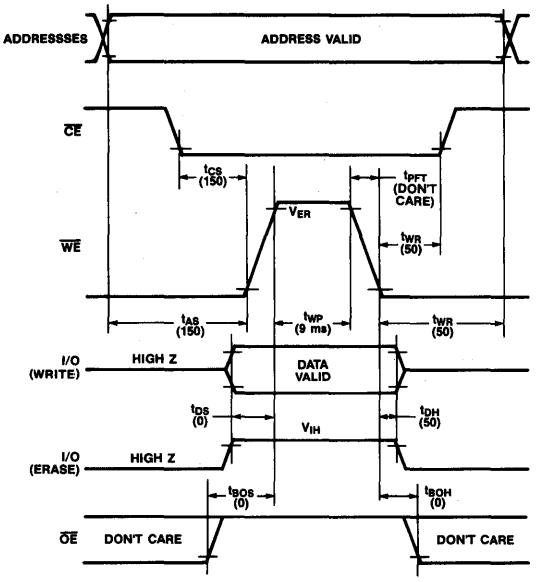
MILITARY

AC Characteristics

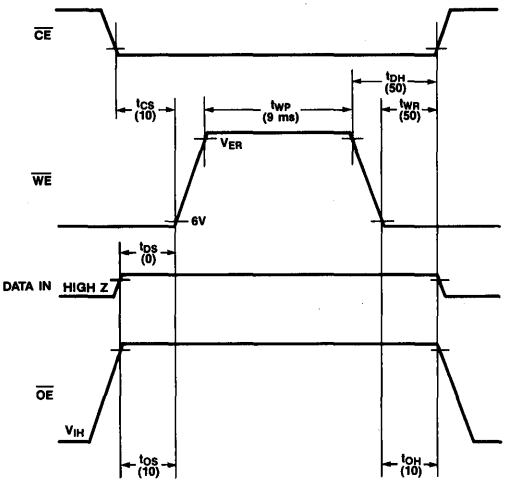
21 V Optional Erase or Write Cycle

(All times shown in parentheses are in ns and are minimum value, unless otherwise noted.)

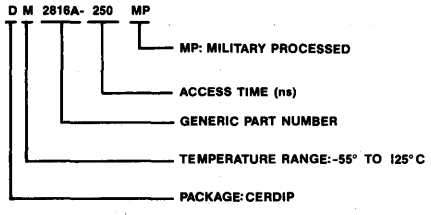
21 V BYTE ERASE OR BYTE WRITE TIMING



21 V CHIP ERASE CYCLE

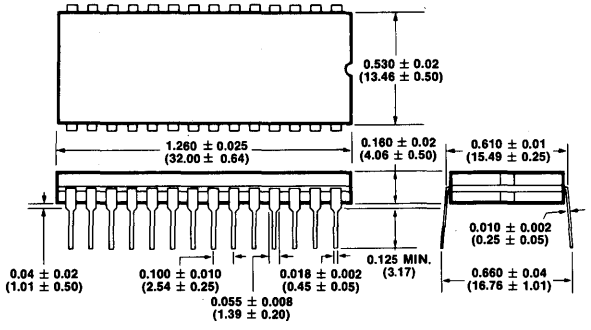


Ordering Information



Package Diagram

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

M2817A

Timer E^2
16K Electrical Erasable ROMs

Aug. 1985

Features

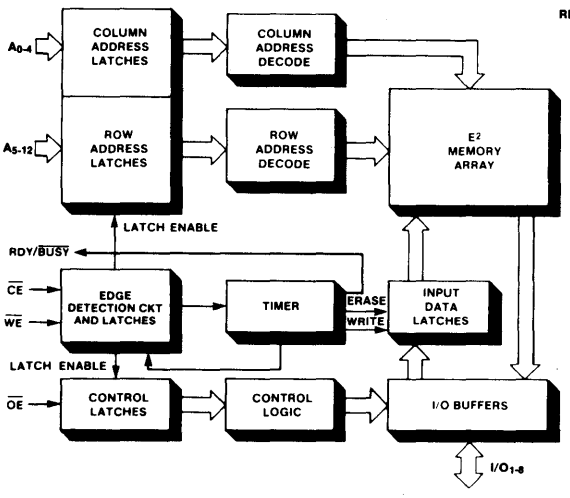
- **Military Temperature Range**
- **Ready/Busy Pin**
- **High Endurance, 10,000 Byte Write Cycles**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA Active Current**
  - **40 mA Standby Current**
- **JEDEC Approved Byte-Wide Pinout**

Description

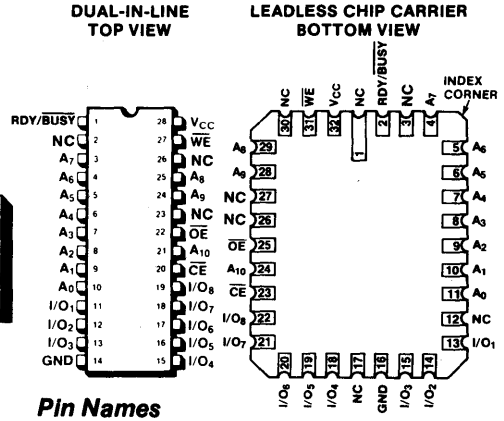
SEEQ's M2817A is a 5 V only, 2K x 8 electrically erasable read only memories (E^2ROMs). It is packaged in a 28 pin package and has a ready/busy pin. This E^2ROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is 10 thousand cycles. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride E^2ROM process and its innovative "Q cell" design. It is ideal for systems which require frequent updates and higher reliabilty over lower specified endurance E^2ROMS.

The M2817A has an internal timer that automatically times out the write time. The on-chip timer, along

Block Diagram



Pin Configuration



Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-12}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
N/C	NO CONNECT

MILITARY

with the input latches, frees the microcomputer system for other tasks during the write time. The 2817A's write cycle time is 10 ms over the military temperature range. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occured first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Chip Erase	V_{IL}	V_{ER}	V_{ER}	V_{IH}	High Z

Power Up/Down Considerations

The M2817A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred with V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
- *Storage ..... -65° C to +150° C*
- *Under Bias ..... -10° C to +135° C*

All Inputs or Outputs with
- *Respect to Ground ..... +6V to -0.3V*

$\overline{WE}$ During Writing/Erasing with
- *Respect to Ground ..... +22.5V to -0.3V*

Duration of $\overline{WE}$ Supply at 22V
- *During W/E Inhibit ..... 24 hours*

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2817A-250	M2817A-30C
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range	-55° C to +125° C	-55° C to +125° C
Q (Maximum Endurance)[2]	10,000 cycles/byte	10,000 cycles/byte

D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

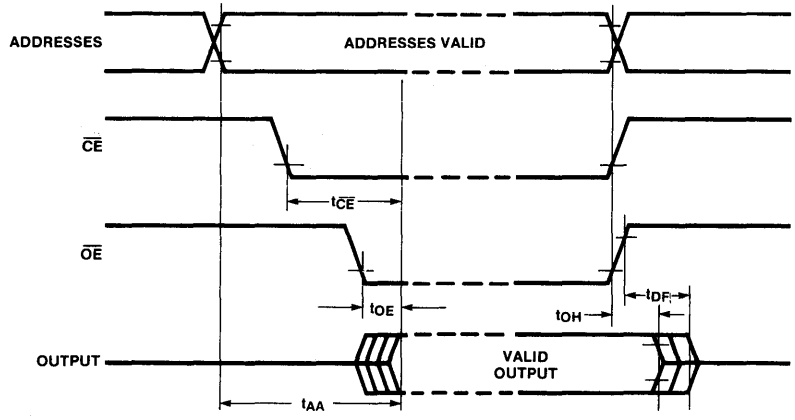
Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
V_{ER}	OE and WE Voltage in Chip Erase Mode	12	22	V	I_{ER} = 10 μA

A.C. Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits (ns) M2817A-250 Min.	M2817A-250 Max.	M2817A-300 Min.	M2817A-300 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read Cycle Timing



MILITARY

Capacitance $T_A = 25°C$; f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Cap.	10 pF	$V_{I/O} = 0$ V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

A.C. Characteristics

Write Cycle (Over the operating V_{CC} and temperature range)

		Limits (ns)				
		M2817A-250		M2817A-300		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{AS}	Address to Write Set Up Time	10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{AH}	Address Hold Time	50		50		ns
t_{DS}	Data Set Up Time	20		50		ns
t_{DH}	Data Hold Time	20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	μs
t_{DB}	Time to Device Busy		200		200	ns

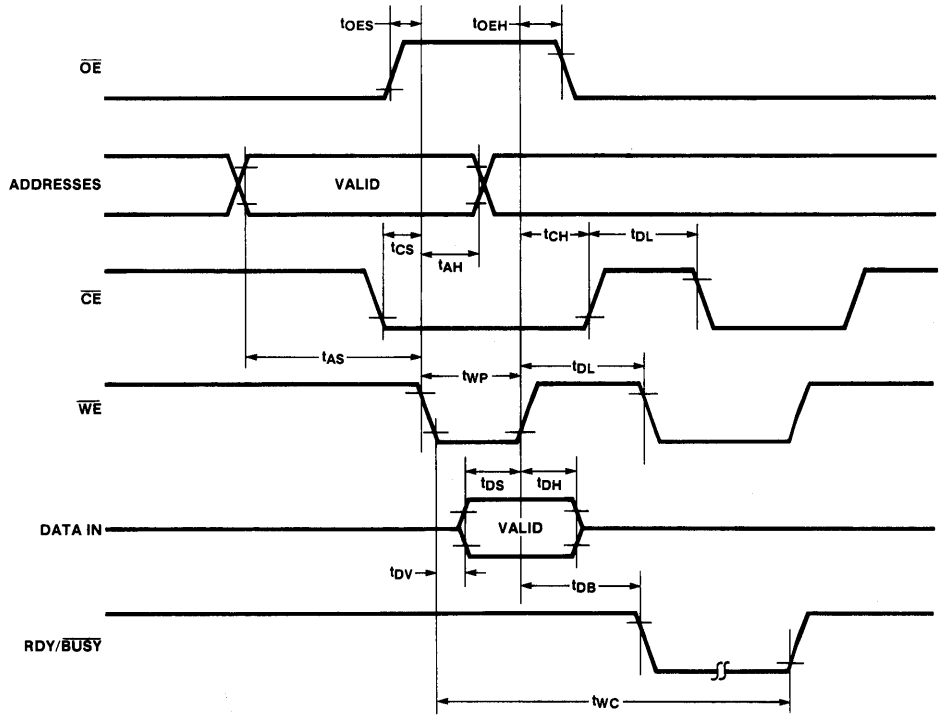
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

A.C. Characteristics

Write Cycle (Over the operating V_{CC} and temperature range)

		Limits (ns)				
		M2817A-250		M2817A-300		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{WC}	Byte Write Cycle Time		10		10	ms

Write Cycle Timing



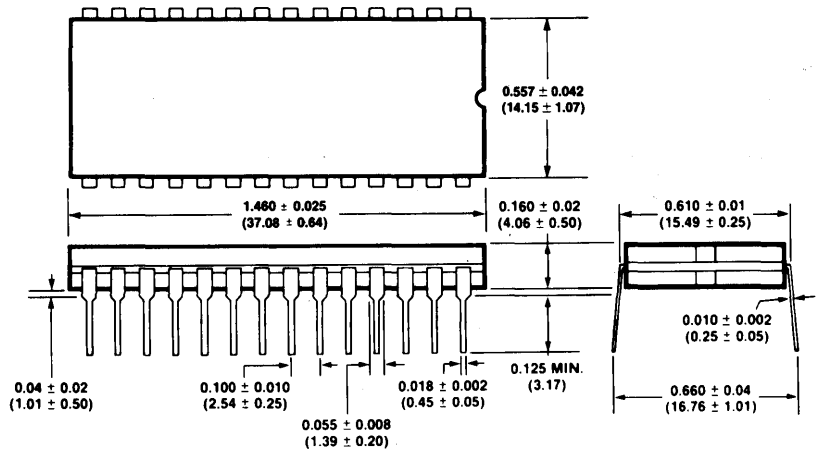
Ordering Information

D M 2817A- 250 MP

- MP — MILITARY PROCESSED
- 250 — READ ACCESS TIME (ns)
- 2817A — GENERIC PART NUMBER
- M — MILITARY TEMPERATURE
- D — PACKAGE: D = CERDIP, L = CHIP CARRIER

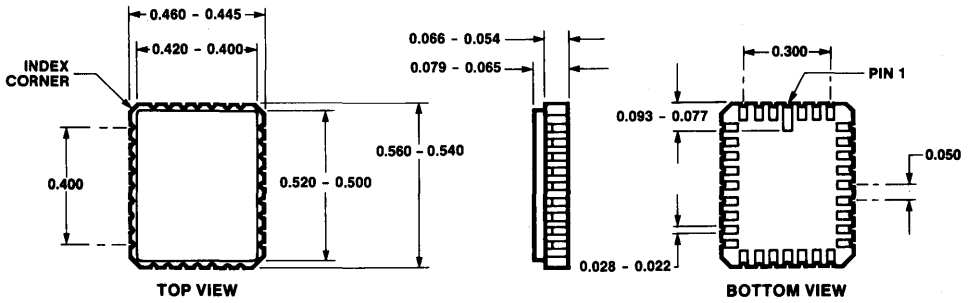
Packaging Information

28-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

LEADLESS CHIP CARRIER 32 PIN PACKAGE



M2864/M2864H
Timer E^2
64K Electrically Erasable ROMs

August 1985

Features

- **64K E^2ROM**
  - **Military Temperature M2864**
- **Ready/Busy Pin**
- **High Endurance Write Cycles**
  - **10,000 Cycles/Byte**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
  - **2 ms Byte Write (M2864H)**
- **5 V±10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**

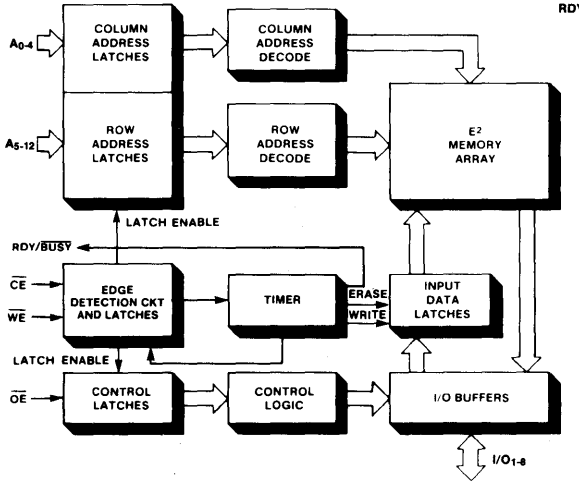
Description

SEEQ's M2864 is a 5 V only, 8K x 8 NMOS electrically erasable read only memory (E^2ROM). It is package in a 28 pin package and has a ready/busy pin. This E^2ROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is 10 thousand cycles.

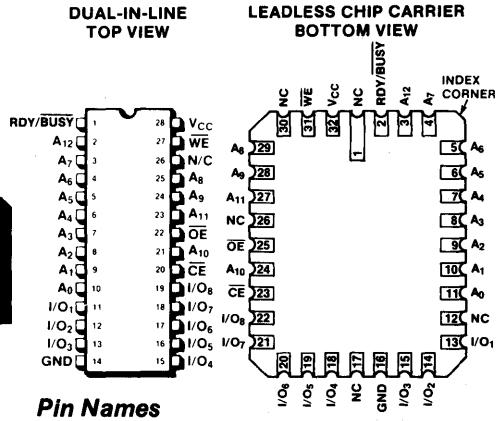
The E^2ROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, an M2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

These two timer E^2ROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Block Diagram



Pin Configuration



Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-12}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
N/C	NO CONNECT

MILITARY

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	RDY/$\overline{BUSY}$ (1)*
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write or Read Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	High Z

*Pin 1 has an open drain output and requires an external 3K resistor to V_{CC}. The resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

Power Up/Down Considerations

The M2864 has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -65° C to +135° C

All Inputs or Outputs with
Respect to Ground ..... +15 V to -0.3 V

Duration of $\overline{OE}$ Supply at 12 V
During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2864-250	M2864H-300 M2864-300	M2864-35
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%	5 V ± 5%
Temperature Range	-55° C to 125° C	-55° C to 125° C	-55° C to 125° C
Q (Maximum Endurance)	10,000 cycles/byte	10,000 cycles/byte	10,000 cycles/byte

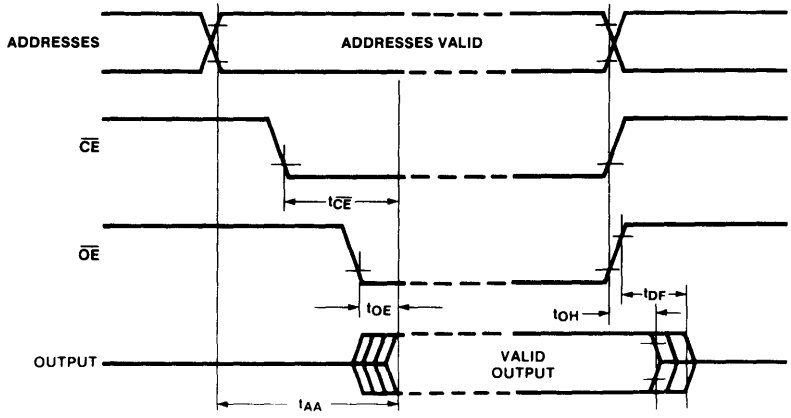
DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{SB}	Standby V_{CC} Current		50	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA

AC Characteristics Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits (ns) M2864-250 Min.	M2864-250 Max.	M2864H-300 M2864-300 Min.	M2864H-300 M2864-300 Max.	M2864-35 Min.	M2864-35 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



MILITARY

Capacitance T_A[1] = 25° C; f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Cap.	10 pF	$V_{I/O}$ = 0 V

AC Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics

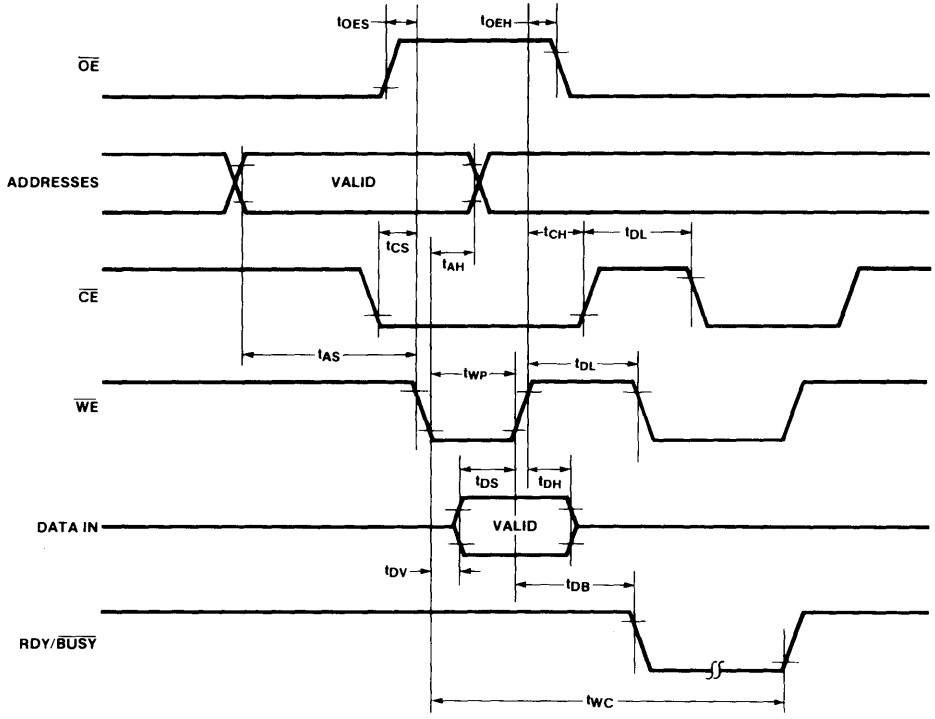
Write Cycle (Over the Operating V_{CC} and temperature range)

		Limits						
		M2864H-250 M2864-250		M2864H-300 M2864-300		M2864-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WC}	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	"H" Family Only		2		2		—	ms
t_{AS}	Address to $\overline{WE}$ Set Up Time	10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	0		0		0		ns
t_{WP}[2]	$\overline{WE}$ Write Pulse Width	150		150		150		ns
t_{AH}	Address Hold Time	50		50		70		ns
t_{DS}	Data Set Up Time	50		50		50		ns
t_{DH}	Data Hold Time	20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		ns
t_{DV}[3]	Data Valid Time		1		1		1	μs
t_{DB}	Time to Device Busy		200		200		200	ns

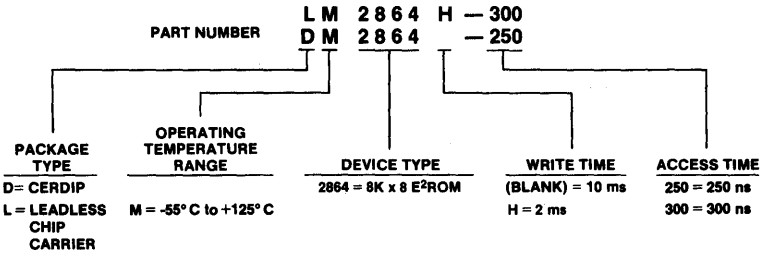
Notes:

1. This parameter is only sampled and not 100% tested.
2. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within a 1 μs maximum after the initiation of a write cycle.

Write Cycle Timing

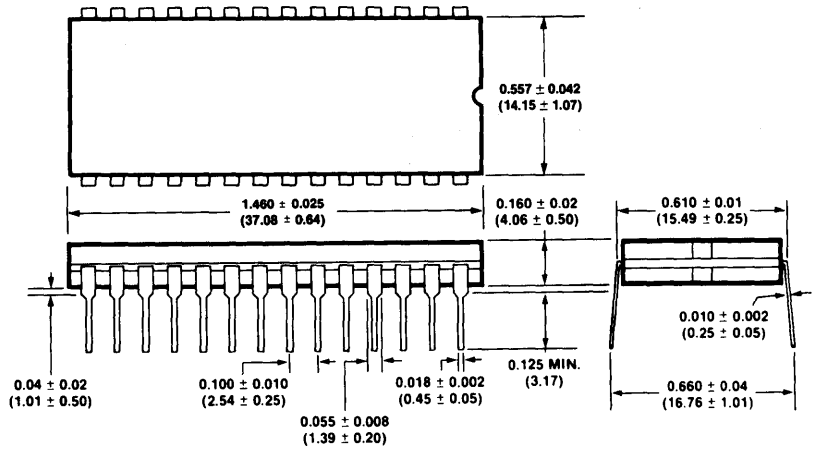


Ordering Information



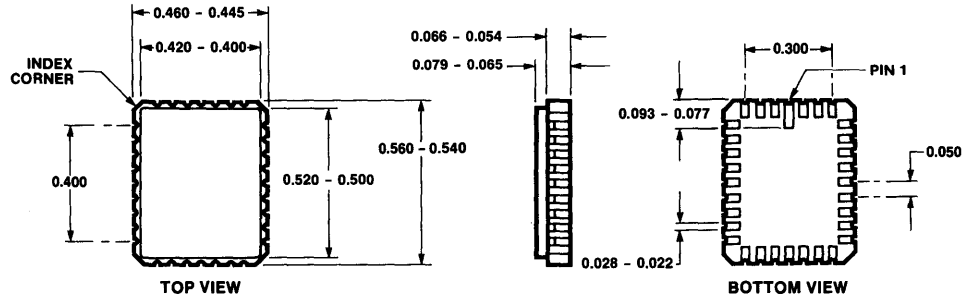
Packaging Information

28-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

LEADLESS CHIP CARRIER 32 PIN PACKAGE



M52B13/M52B13H
(Military Temperature Range)

E52B13/E52B13H
(Extended Temperature Range)

16K Electrically Erasable E^2 ROM

June 1985

Features

- **Full Military and Extended Temperature Range**
  - **M52B13/M52B13H: -55 to 125° C**
  - **E52B13/E52B13H: -40 to 85° C**
- **Input Latches**
- **5V ± 10% 2K X 8 E^2ROM**
- **1 ms (52B13H) or 9 ms Byte TTL Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte**
- **Chip Erase and Byte Erase**
- **Silicon Signature™ and DITrace™**
- **Fast Read Access Time — 250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **M2816 E^2 Compatible**

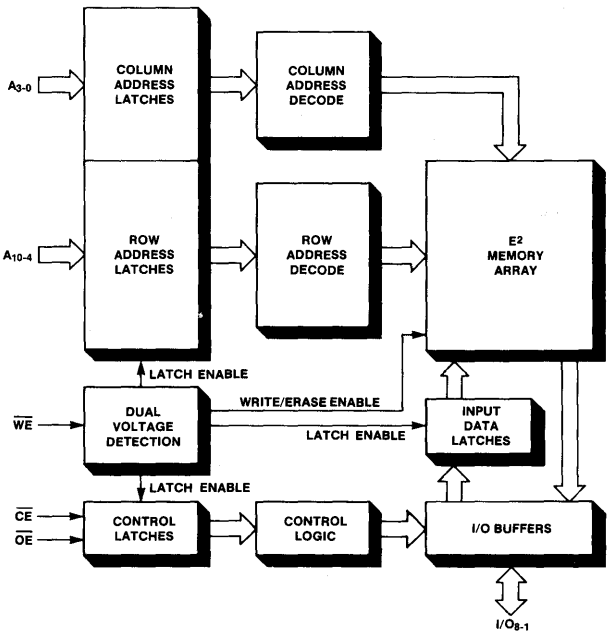
Description

SEEQ's M52B13 and E52B13 are 2048 x 8, 5 volt electrically erasable, read only memories (E^2ROM) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 msec), an M52B13H and E52B13H are also available. Data is latched and electrically written by a TTL (or a 21 V pulse for the M52B13/E52B13) pulse on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written up to 10,000 times.

The M52B13 is compatible to the M2816 and SEEQ's M5213. For system upgrades of these older generation E^2ROMs, the M52B13 is specified over the full –55 to +125° C temperature range and has an access time of 250 ns. The M52B13 is available in a 24 pin cerdip package.

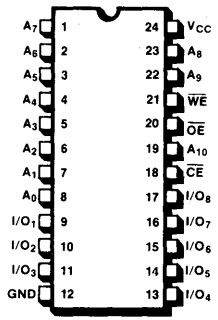
(continued on next page)

Block Diagram



Pin Configuration

M52B13/E52B13



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

MILITARY

These E²ROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems. Designing the E²ROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1's) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device operates at 5 volts only and the byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation E²ROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal (52B13 only) to be applied to $\overline{WE}$ to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of $\overline{WE}$.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all E²ROMs is that the total number of write and erase cycles is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available, t_{CE} time after Chip Enable is applied or t_{ACC} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

SEEQ's family of E²ROMs incorporate Silicon Signature™ and Ditrace™ fields. The Silicon Signature™ feature is a method for storing device and programming information on-chip in an extra row of ROM cells.

Included in the user-accessible Silicon Signature™ field is the manufacturer's name (SEEQ) and the product's wafer fabrication location. The DiTrace™ feature is a method for storing production flow information to the wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection (V_{CC} = 5V ± 10%)

Mode \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase [2]	V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

Notes:
1. $\overline{WE}$ may be from V_{IH} to 6V in the read and standby mode.
2. WE may be at V_{IL} (TTL W/E Mode) or from 14V to 22V (High Voltage W/E Mode) in the byte erase, byte write, or chip erase mode for the 52B13. The 52B13H requires $\overline{WE}$ to be at V_{IL} for these same modes.

52B13/52B13H Specification Differences

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	M52B13 E52B13 Min.	M52B13 E52B13 Max.	M52B13H E52B13H Min.	M52B13H E52B13H Max.	Units
t_{WP}	Write Enable Pulse Width					
	Byte Write/Erase	9		1		ms
	Chip Erase	9		9		ms
V_{WE}	$\overline{WE}$ Write/Erase Voltage High Voltage Mode	14	22	Not Applicable		V

Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. *V_{CC} is less than 3 V.*
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Under the above conditions, the outputs are in a high impedance state.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65°C to +150°C
Under Bias ..... -65°C to +135°C
All Inputs or Outputs with
Respect to Ground ..... +7V to -0.6V
WE During Writing/Erasing
with Respect to Ground ..... +22V to -0.3V
Duration of WE Supply at
22V During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	Read Mode	Byte Write or Erase Mode	Chip Erase Mode
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%	5 V ± 10%
Temperature Range: M52B13/M51B13H	-55 to +125°C	-55 to +125°C	-55 to +100°C
E52B13/E51B13H	-40 to +85°C	-40 to +85°C	-40 to +85°C
Q (Maximum Endurance)[1]	—	10,000 cycles/byte	10,000 cycles/byte

D.C. Operating Characteristics During Read or Write/Erase

Symbol	Parameter	Min.	Nom.[2]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	μA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	μA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[3]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[3]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	μA	$\overline{WE} = V_{IL}$
	Chip Erase—High Voltage Mode[3]			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current		15	35	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	90	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode[3]	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 μA

Notes:
1. Each byte may be written or erased, over the temperature and V_{CC} range, up to the recommended endurance (Q) specification.
2. Nominal values are for T_A = 25°C and V_{CC} = 5.0 V.
3. This mode is not available on the M52B13H/E52B13H.

A.C. Operating Characteristics During Read

Symbol	Parameter	Device Number Extension	M52B13/ M52B13H Min.	M52B13/ M52B13H Max.	E52B13/ E52B13H Min.	E52B13/ E52B13H Max.	Units	Test Conditions
t_{ACC}	Address to Data Valid	-250		250		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-300		300		—	ns	
		-350		—		350	ns	
t_{CE}	Chip Enable to Data Valid	-250		250		250	ns	$\overline{OE} = V_{IL}$
		-300		300		—	ns	
		-350		—		350	ns	
t_{OE}[1]	Output Enable to Data Valid	-250	10	90	10	90	ns	$\overline{CE} = V_{IL}$
		-300	10	90	—	—	ns	
		-350	—	—	10	110	ns	
t_{DF}[2]	Output Enable to High Impedance	-250	0	70	0	70	ns	$\overline{CE} = V_{IL}$
		-300	0	70	—	—	ns	
		-350	—	—	0	80	ns	
t_{OH}	Output Hold	All	0		0		ns	$CE = OE = V_{IL}$
C_{IN}/C_{OUT}[3]	Input Capacitance	All		10		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$
	Output Capacitance	All		10		10	pF	

Equivalent A.C. Test Conditions[6]

Output Load: 1 TTL gate and C_L = 100 pF

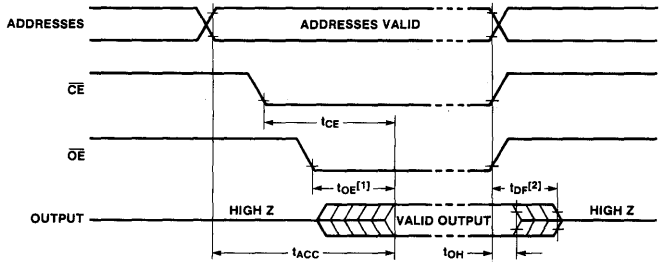
Input Rise and Fall Times: ≤ 20ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

MILITARY

READ TIMING

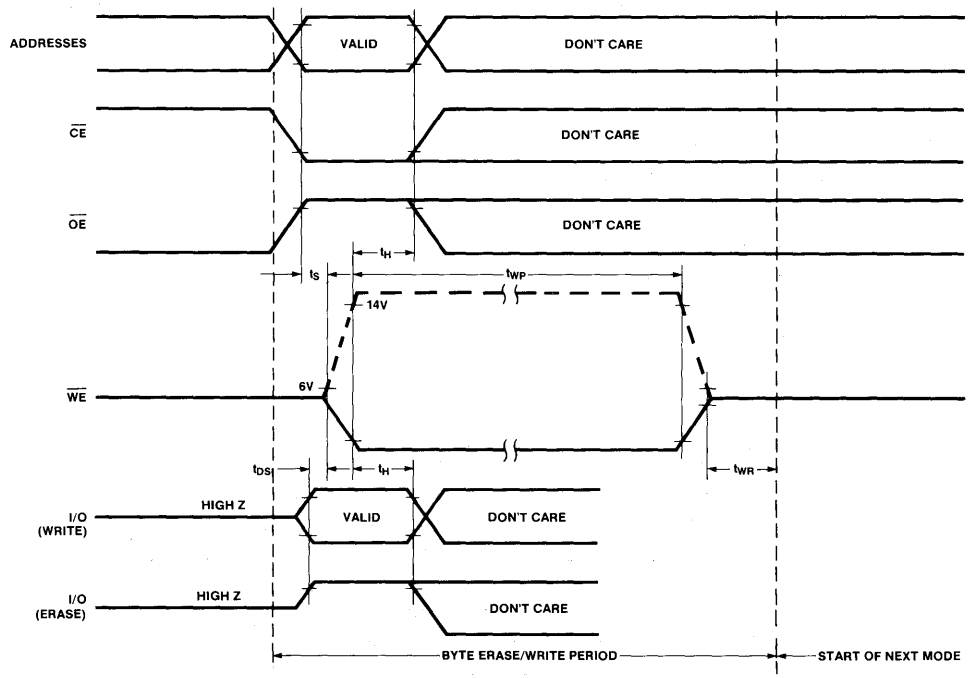


Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.
4. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
5. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
6. These are equivalent test conditions and actual test conditions are dependent on the tester.

A.C. Operating Characteristics During Write/Erase

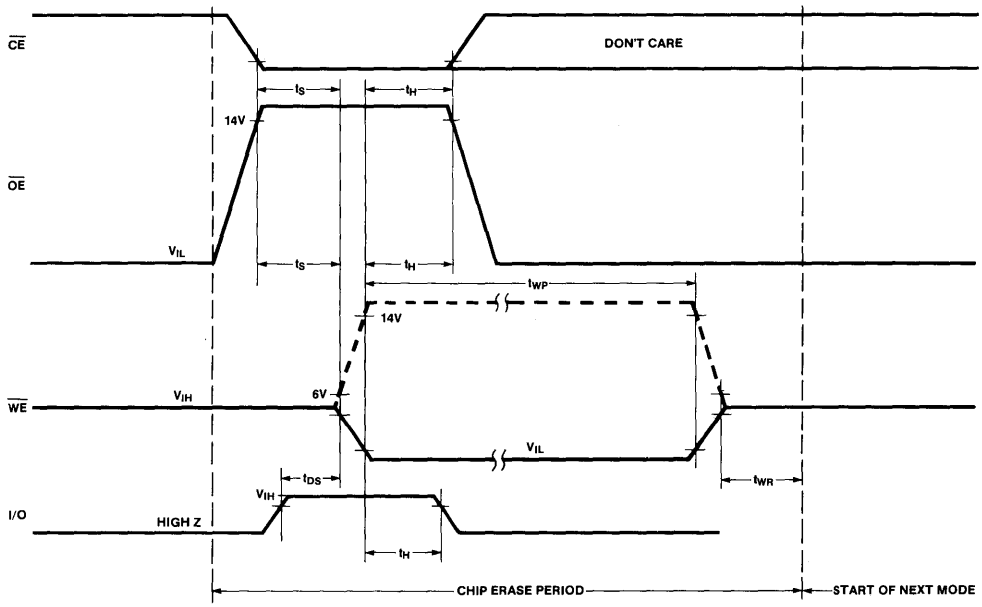
Symbol	Parameter		Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$		50		ns
t_{DS}	Data Setup to $\overline{WE}$		0		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change		50		ns
t_{WP}	Write Enable, $\overline{WE}$, Pulse Width	Chip Clear — All Devices	9		ms
		Byte Modes — M52B13/E52B13	9		ms
		Byte Modes — M52B13H/E52B13H	1		ms
t_{WR}[5]	$\overline{WE}$ to Mode Change		50		ns

BYTE ERASE OR BYTE WRITE TIMING



Notes: See AC notes on page 4-45.

CHIP ERASE TIMING



Ordering and Packaging Information

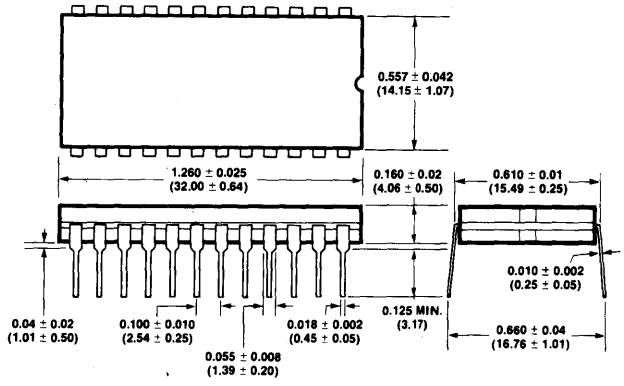
PART NUMBERS

DM52B13 -250

DM52B13H-250MP

- SCREENING:
  MP = MILITARY PROCESSED
  BLANK = SEEQ STANDARD SCREENING
- ACCESS TIME (ns)
- H = 1 ms WRITE TIME
  AND 5 V ONLY OPERATION
  BLANK = 10 ms AND 5 V/21 V OPERATION
- PRODUCT: 2K x 8 E^2ROM
- TEMPERATURE RANGE:
  M = -55 to 125°C
  E = -40 to 85°C
- PACKAGE:
  D = CERDIP
  (CONTACT SEEQ REGARDING
  CHIP CARRIER)

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

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M52B33/M52B33H
E52B33
64K Electrically Erasable E²ROM

March 1985

Features

- **Full Military and Extended Temperature Range**
  - **M52B33/M52B33H: -55 to 125° C**
  - **E52B33: -40 to 85° C**
- **10,000 Write Cycles/Byte Over Temperature**
- **Input Latches**
- **5 V ±10% V_{CC}**
- **1 ms (52B33H) or 9 ms TTL Byte Erase/Byte Write (52B33)**
- **Power Up/Down Protection**
- **DITrace™**
- **Fast Read Access Time—250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte-Wide Memory Pinout**

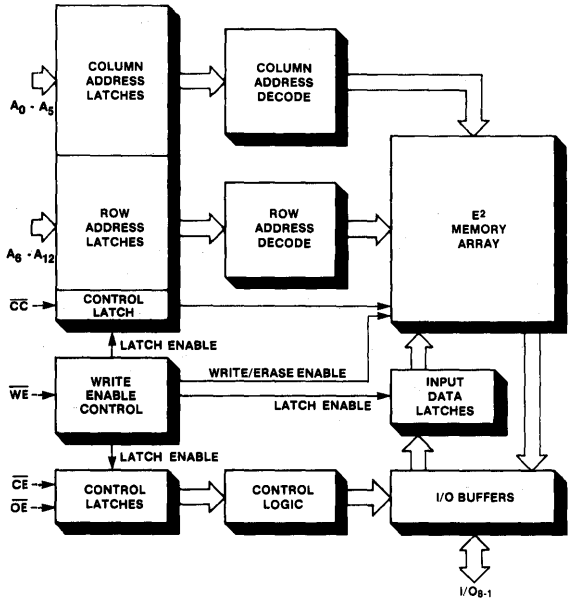
Description

SEEQ's M52B33 and E52B33 are 8196 x 8, 5 V electrically erasable read only memories (E²ROM) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 ms), an M52B33H is also available. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written, there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written up to 10,000 times.

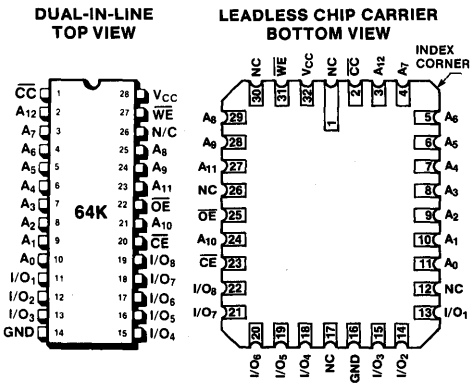
The M52B33 is available in a 28 pin cerdip or 32 pin leadless chip carrier. The pin configuration is to the JEDEC approved byte wide memory pinout for these two types of packages. These E²ROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other

(continued on page 2)

Block Diagram



Pin Configurations



Pin Names

A_C	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

systems. Designing the E²ROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B33 and 52B33H have six modes of operation (see Table 1) and require only TTL inputs to operate these modes.

To write into a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the 52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

For certain applications, the user may wish to erase the entire memory. This feature (chip clear) is optional and the timing specifications are available from SEEQ.

A characteristic of all E²ROMs is that the total number of write and erase cycles is not unlimited. The 52B33 is designed for applications requiring up to 10,000 write and erase cycles per byte over the temperature range. For applications requiring higher endurance or reliability, a 55B33 at 1,000,000 cycles is being characterized. Further information on the 55B33 is available from SEEQ. The write and erase cycling characteristics are completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available, T_{CE} time after Chip Enable is applied or T_{ACC} time from the addresses. System power may be reduced by pacing the device into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

SEEQ's family of E²ROMs incorporates a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to the wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

Power Up/Down Considerations

SEEQ's "52B" E² family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions.

1. V_{CC} is less than 3 V.
2. A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

MILITARY

Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

Absolute Maximum Stress Rating*

Temperature
Storage ..... −65° C to +150° C
Under Bias ..... −65° C to +135° C
All Inputs or Outputs with Respect to Ground ..... +7V to −0.6V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	Read Mode	Byte Write or Erase Mode
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range: M52B33/M52B33H	-55 to +125° C	-55 to +125°C
E52B33	-40 to +85°C	-40 to +85°C
Q (Maximum Endurance)[1]	—	10,000 cycles/byte

DC Operating Characteristics During Read or Erase/Write

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.[2]	Max.	Unit	Test Condition
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max
I_{WE}	Write Enable Leakage Read Mode W/E Mode			 10 10	 μA μA	 $\overline{WE} = V_{IH}$ $\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		15	50	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (DC)	Input Low Voltage (DC)	−0.1		0.8	V	
V_{IL} (AC)	Input Low Voltage (AC)	−0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

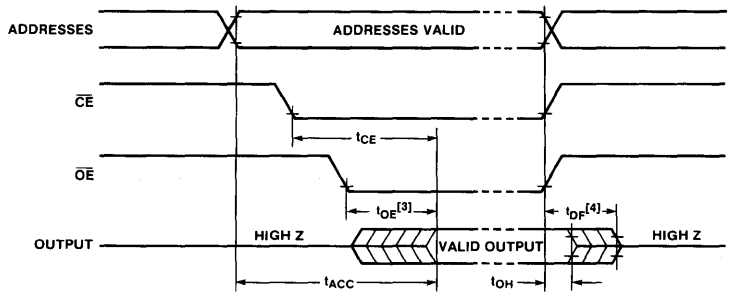
Notes: See page 4-51 for notes.

A.C. Operating Characteristics During Read

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	M52B33 M52B33H Min.	M52B33 M52B33H Max.	E52B33 Min.	E52B33 Max.	Unit	Test Conditions
t_{ACC}	Address to Data Valid	-250 -300		250 300		250 300	ns ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid	-250 -300		250 300		250 300	ns ns	$\overline{OE} = V_{IL}$
t_{OE}[3]	Output Enable to Data Valid	-250 -300	10 10	90 90	10 10	90 90	ns ns	$\overline{CE} = V_{IL}$
t_{DF}[4]	Output Enable to High Impedance	-250 -300	0 0	70 70	0 0	70 70	ns ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[5]	Input/Output Capacitance	All		10		10	pF	V_{IN} = 0 V for C_{IN}, V_{OUT} = 0 V for C_{OUT}, T_A = 25° C

Read Cycle Timing



Notes:
1. Nominal values are for T_A -25°C and V_{CC} = 5.0 V.
2. Each byte may be written or erased, over the temperature and V_{CC} range, up to the recommended endurance (Q) specification.
3. $\overline{OE}$ may be delayed to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
5. This parameter is periodically sampled.
6. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
7. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
8. These are equivalent test conditions and actual test conditions are dependent on the tester.

MILITARY

A.C. Operating Characteristics During Write/Erase

(Over the operating V_{CC} and temperature range)

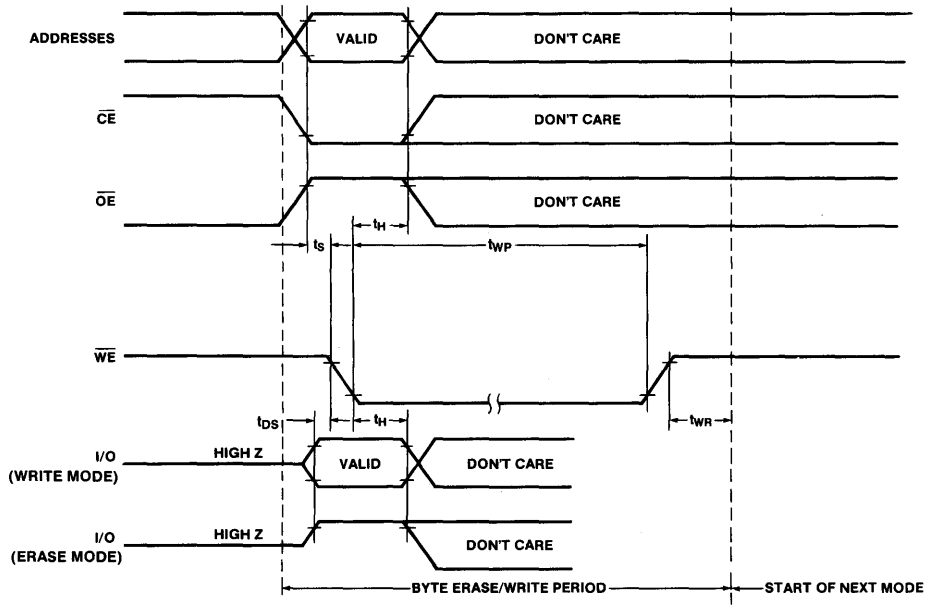
Symbol	Parameter	Limits Min.	Limits Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	0		ns
t_H[6]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable, ($\overline{WE}$) Pulse Width			
	Byte Modes — M52B33/E52B33	9		ms
	Byte Modes — M52B33H	1		ms
	Chip Clear — M52B33/M52B33H	100		ms
	Chip Clear — E52B33	100		ms
t_{WR}[7]	$\overline{WE}$ to Mode Change			
	$\overline{WE}$ to Next Byte Write/Erase Cycle	50		ns
	$\overline{WE}$ to Start of a Read Cycle	1		μs

See page 4 for notes.

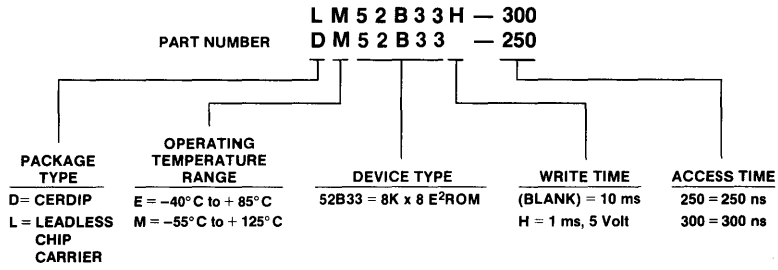
Equivalent A.C. Test Conditions[8]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Byte Erase or Byte Write Cycle Timing

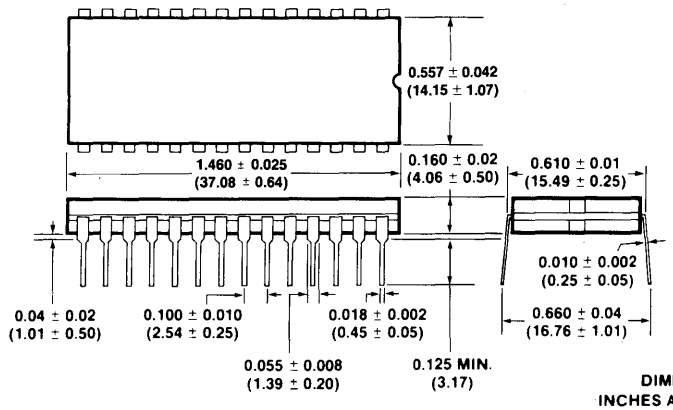


Ordering Information



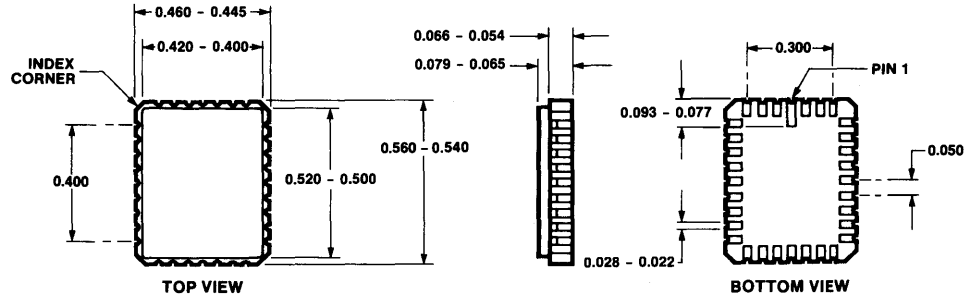
Packaging Information

28-LEAD HERMETIC CERDIP PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

LEADLESS CHIP CARRIER 32 PIN PACKAGE



MILITARY

Military Quality Assurance Program

SEEQ's Management emphasis is on Quality in products and performance, converting the results of the Technology evolution and innovations to the greatest benefit of our customers with an ever increasing degree of system reliability, quality, and functionality.

SEEQ's comprehensive and interactive Quality program is designed to exceed military and customer expectations and requirements.

SEEQ's Quality program uses military standards as a guide; including MIL-Q-9858, MIL-I-45208, MIL-M-38510 Appendix A, MIL-STD-45662, FED-STD-209 and MIL-STD-883. Key segments of the Quality program are described below.

Quality Assurance

SEEQ's Quality Assurance activity audits and monitors the operating system and reports compliance to processing requirements. Included within the activity is inspection of incoming material and outgoing product, audits and process monitors of Fab, Assembly and Test. Product improvement and corrective action is based on statistical data reduction and analysis.

Quality Control

SEEQ's Quality Control activity is an in-line inspection, reporting and statistical control system. Included is product inspection, and disposition of material and processes which do not conform to specification.

Quality Engineering

Quality engineering supports incoming, Fab, assembly, test, customer returns, and failure analysis through the use of statistics and analytical capabilities. Quality Engineering supplies focus, coordination and integration for quality improvement and system optimization, throughout the entire business entity of SEEQ.

Product Monitor Program

SEEQ's Product Monitor Program merges the classical reliability Quality Conformance Inspection (QCI, Groups B, C, and D) and Device Qualification Activities into one comprehensive product data base. Results are published quarterly.

Document Control

Document Control generates, implements and maintains procedures that will ensure control of all documents related to the design, production and testing of manufactured products, including the translation of customer specification requirements into SEEQ internal travelers, specifications and procedures.

SEEQ's Document Control program assures internal specifications and procedures are maintained to the correct revision levels (Engineering Change Notice Control) and provides historical records of all changes.

Reliability Engineering

Reliability (quality over time) is built into each SEEQ device, using proven engineering techniques. Process and product performance is demonstrated using accelerated stresses and tests. Results are jointly analyzed with design and sustaining engineering; then any improvements are incorporated into manufacturing.

Device Physics

The Device Physics groups help characterize the design and process, particularly in regard to quality and reliability. Potential failure mechanisms are analyzed for impact on processing and design. Overall product performance is enhanced by development of test, screens, process or design changes as necessary.

Military Product Processing Program

SEEQ's Military product flow (Chart 1) incorporates manufacturing processing, screening and controls. Controls as specified in Military procedures or customer specifications are an integral part of the processing flows in wafer fabrication, assembly product screening and test. (Table 1)

Quality Conformance Inspection

Group A Tests

Group A — lot acceptance tests (see Table 1) are performed on each of SEEQ's production lots or sub-lots (splits) after completion of all processing. Q.A. electrical and mechanical inspection is performed to an AOQL (Average Outgoing Quality Limit) of 0.65%. For electrical acceptance the 0.65% AOQL is cumulative for all sub-groups. (AC, DC, fct across temperature).

Group B — Tests (see Table 2)

Group B testing is performed by product and package type. The Group B covers the lot's (sub lot) seal date code and the next consecutive five (5*) weeks of seal. The date code marked on the product is the week of seal.

Group C Stresses — (see Table 3)

The product stressed, as part of Group C, is identical to that shipped or from the same process and product family. The seal date code of the product covered will be the same as or within the 51* consecutive weeks following the Group C seal date code. Electrical test is per SEEQ data sheet.

Group D Stresses — (see Table 4)

The package stressed, as part of Group D, is identical to that shipped. The seal date code of product covered will be the same as or within the 51* weeks following the Group D date code.

Product Monitors

On-Going

Process control monitor samples of product are subjected to marking permanency, endurance, pressure pot and hermeticity. These tests are performed and reported by the Quality Assurance activity. Monitor tests and procedures are in accordance with applicable MIL-STD-883 test methods.

*Frequency is stated for Military processed lots. Some group B, C, D stresses and tests for commercial products are performed more frequently.

Extended Product Monitors

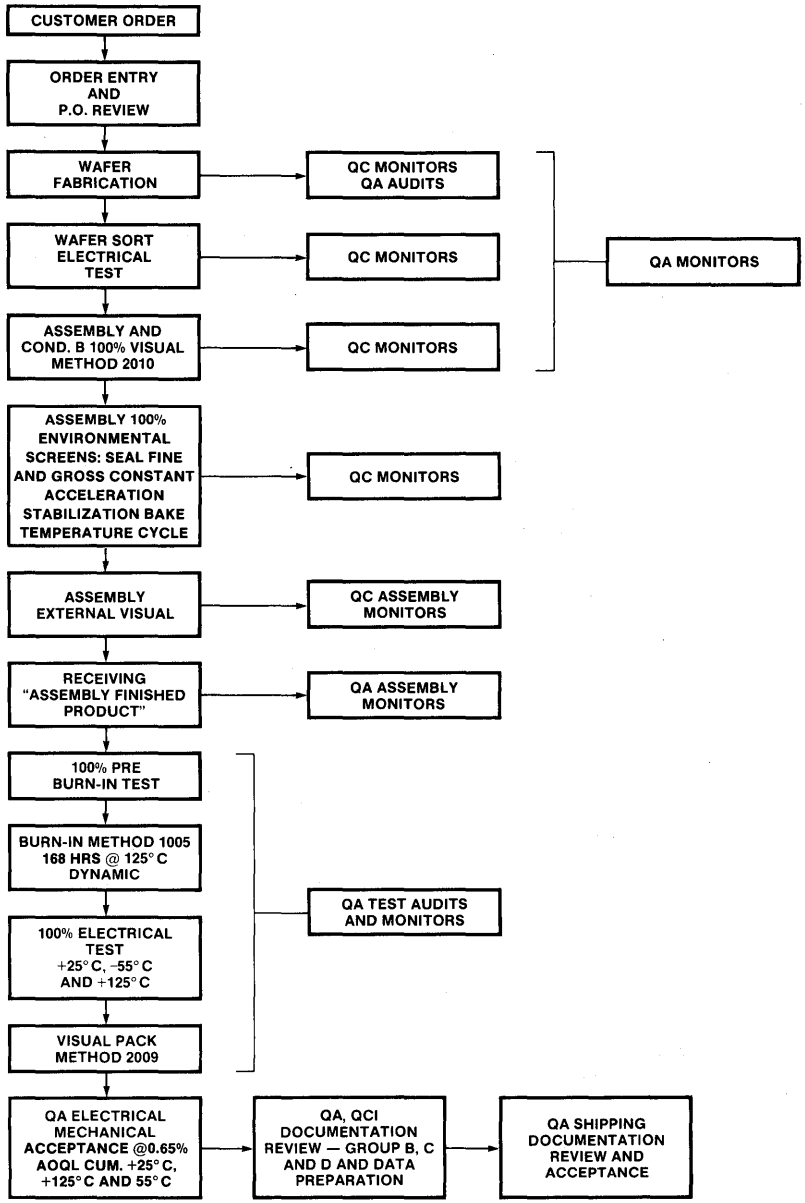
As part of SEEQ's product reliability data program samples of released military product are subjected to extended stresses. The extended stress are summarized as follows:

	Stress	
Stress	Frequency	Duration
Dynamic Life Stress	Annually	10,000 Hours
Endurance (E^2ROM)	Quarterly	1,000,000 Cycles
Endurance (EPROM)	Quarterly	50 Cycles
Temperature Cycle	Quarterly	1,000 Cycles
Data Retention	Quarterly	1,000 Hours
Dynamic Static Life Stress	Quarterly	1,000 Hours

Product Monitor Quality Conformance Inspection Data

SEEQ updates quarterly all product monitor data and can supply summary data upon request. Generic data is defined for Group B, C, and D tests as well as other tests SEEQ deems necessary. Electrical endpoint testing is per SEEQ data sheet using SEEQ standard test programs and equipment. Dynamic life stress (burn-in) is performed in compliance with MIL-STD-883, MIL-STD-883, Method 1015.

Product Processing Flow (Chart 1)



SEEQ Screens, Tests, & Monitors (Table 1)

Military Screen	MIL-STD Method	Reqmt.
Internal Visual	2010, Test Condition B	100%
Stabilization Bake	1008, 24 Hrs @ Condition C	100%
Temperature Cycling	1010, Test Condition C	100%
Constant Acceleration	2001, Test Condition D, Y_1 Orientation Only	100%
Seal (A) Fine (B) Gross	1014 Condition A or B Condition C or D	100%
Visual Inspection		100%
Initial (Pre-Burn-In-Test) Electrical Parameters	Per Applicable SEEQ Specification	100%
Burn-In Stress	1015, Dynamic @ 125° C	100%
(Post-Burn-In—Test) Electrical Parameters Tested within 96 Hrs.	Per Applicable SEEQ Specification	100%
Percent Defective Allowable (PDA) Calculation	5% Cumulative	100%
Quality Assurance Group A Tests (A) Static Tests (B) Dynamic Tests and Switching Tests (C) Functional Tests	Per Applicable SEEQ Specification Cumulative across temperature (–55, 25, 125° C)	.65% AOQL
Qualification or Quality Conformance Inspection Test Sample Selection		
External Visual	2009	100%

SEEQ Quality Monitors

Wafer Fab

Monitors and Audits:
- Phosphorous Content
- Spec. and ECN Control
- Defect Density
- Defect Inspection
- Critical Dimensions
- Oxide Thickness
- On-Going Mask
- SEM (Step Coverage)

Assembly Processing

Monitors:
- 2nd Optical LTPD 10/1, Method 2010 Cond B
- Die Shear (2 Units/4 Hours)
- Bond Strength (2 Units/4 Hours)
- 3rd Optical — LTPD 10/1, Method 2010 Cond B

Assembly Environmentals

Monitors:
- Tin Plating Thickness
- Solderability
- Visual
- Equipment Monitors
- Fine and Gross Leak LTPD 10/1

Assembly Receiving

Monitors:
- Internal Visual
- Bond Strength
- Die Shear
- Lid Torque
- Lead Fatigue

Test and Finish

Monitors:
- PDA Verification
- 96 Hour Test Time Window
- Conformance Audits
- Solderability
- Fine Leak/Gross Leak
- Marking Permanence

Quality Conformance Inspection (QCI)

Monitors:
- Group B (Table 2)
- Group C (Table 3)
- Group D (Table 4)

Group B Tests (Table 2)

Test	Test Method	Test Conditions	Quality Level/ Accept Number
Subgroup 1 Physical Dimensions	2016	Per SEEQ Outline Drawing	2 Devices (no failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (no failures)
Subgroup 3 Solderability	2003	Soldering Temperature of +245°C Plus or Minus 5°C	LTPD 15 Accept = 1
Subgroup 4 Internal Visual and Mechanical	2014	Failure Criteria Based on Design and Construction Requirements of SEEQ Specification	1 Device (no failures)
Subgroup 5 Bond Strength Ultrasonic or Wedge	2011	Test Condition C or D	LTPD 15 Accept = 1
Subgroup 7 (A) Seal (1) Fine (2) Gross	1014	As Applicable	LTPD 5 Accept = 0

Group C Stresses (Table 3)

Test	Test Method	Test Conditions	Quality Level/ Accept Number
Subgroup 1 Steady-State Life Test End-Point Electrical	1005	Condition B, 1000 Hours Per SEEQ Specification	LTPD 5 Accept = 1
Subgroup 2 Temperature Cycling Constant Acceleration Hermeticity Fine Gross Visual Examination End-Point Electrical Parameters	1010 2001 1014	Condition C, 10 Cycles Y_1 Orientation 20,000 (g) As Applicable Per SEEQ Specification	LTPD 15 Accept = 1

Group D Stresses (Table 4)

Test	MIL-STD Test Method	Test Conditions	Minimum Quality Level/ Accept Number
Subgroup 1			
Physical Dimensions	2016	Per SEEQ Outline Drawing	LTPD 15 Accept = 1
Subgroup 2			
Lead Integrity	2004	Test Condition B2	LTPD 15 Accept = 1
Hermeticity, Fine and Gross	1014		
Subgroup 3			
Thermal Shock	1011	T = −55°C to +125°C, 15 Cycles Minimum	LTPD 15 Accept = 1
Temperature Cycling	1010	T = −55°C to +125°C, 100 Cycles Minimum	
Moisture Resistance	1004	90% Minimum Relative Humidity	
Hermeticity, Fine and Gross	1014		
Visual Examination	1004	Per SEEQ or Customer Specification	
End-Point Electrical Parameters	1010	Per SEEQ or Customer Specification	
Subgroup 4			
Mechanical Shock	2002	1500 (g)	LTPD 15 Accept = 1
Vibration, Variable Frequency	2007	20 (g)	
Constant Acceleration	2001	Y_1 Orientation 20,000 (g)	
Hermeticity, Fine and Gross	1014		
Visual Examination	2009	Per SEEQ or Customer Specification	
End-Point Electrical Parameters		Per SEEQ or Customer Specification	
Subgroup 5			
Salt Atmosphere	1009	24 Hours	LTPD 15 Accept = 1
Hermeticity, Fine and Gross	1014		
Visual Examination	1009	Per SEEQ or Customer Specification	
Subgroup 6			
Internal Wafer Vapor	1018	5,000 ppm Maximum Water Content at T = +100°C	3 Devices, 0 Failures or 5 Devices, 1 Failure
Subgroup 7			
Adhesion of Lead Finish	2025	Bend 90°, Inspect at 10x to 20x Magnification	LTPD 15 Accept = 1
Subgroup 8			
Lid Torque	2024	As Applicable to Glass-Frit Packages	LTPD 15 Accept = 1

AOQL Sampling Plan

The sampling plans in use by SEEQ Technology, Inc. are designed to:

1. Reduce the total cost of implementing the system, primarily by concentrating on having simple plans which are easy to administer and document and then reduce the total number of units inspected.

2. Provide a single value, regardless of lot size or history which may be guaranteed to the customer as the average maximum proportion defective shipped.

3. Protect the consumer from receiving any lots with unusually high proportion defective.

4. Significantly improved α and β risk factors compared to AQL plans of the same proportion defective value.

5. Increased flexibility compared to AQL and LTPD plans, particularly at lower allowable proportion defective values.

Lot Acceptance Sampling Plans

Table of Sample Sizes

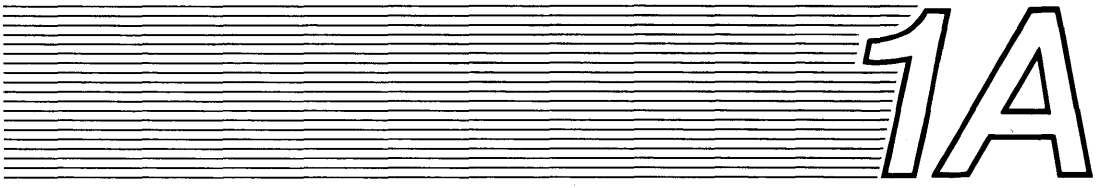
		AOQL								
Lot Size	**A/R Number**	**0.05**	**0.075**	**0.10**	**0.25**	**0.40**	**0.65**	**1.0**	**1.5**	**2.5**
0-100	N/A	100%	100%	100%	100%	100%	100%	100%	100%	100%
101-500	0-1	100%	100%	360	150	90	60	45	30	15
501-1200	1-2	100%	1125	810	330	210	135	90	60	45
1201-∞	2-3	2175	1830	1290	540	345	210	150	105	60

If sample size equals or exceeds lot or batch size do 100% inspection.
A = Accept
R = Reject

SECTION 5

RELIABILITY/APPLICATION NOTES

Memory Products Reliability Note



E^2 RELIABILITY REPORT

August 1985

seeQ
Technology, Incorporated

SEEQ E^2 Reliability Report

Introduction and Product Description

SEEQ offers a family of E^2ROMs (Electrically Erasable Read Only Memories) which range in size from 16K to 64K bits. They conform to the JEDEC configurations for byte wide memories. One family has internal input latches and the second family has internal input latches as well as a timer which performs an automatic erase before write. New developments in process technology, circuit design techniques, and memory cell design combine to provide high performance from these E^2ROMs that require only a single 5-volt power supply. SEEQ uses an innovative Q-cell design on all its E^2ROMs designed since 1983. The Q-cell, combined with oxynitride in the tunnel dielectric, substantially improves the write/erase endurance of E^2ROMs. This gives higher reliability to systems requiring infrequent writes (i.e. once a day for ten years) as well as to systems writing 5-10 times per day.

Programming the state of the memory cells (via the write and erase modes) is accomplished by charging and discharging a floating gate device via Fowler-Nordheim tunneling. This tunneling occurs through a proprietary oxynitride dielectric under the floating gate (see figure 1). Oxynitride is thermal oxide which is annealed with ammonia. The use of oxynitride, provides fast write/erase times (1 msec) at internal voltages that are 25% lower than those required for conventional oxide-only approaches due to its lower barrier height than thermal oxide, . In addition, oxynitride provides lower charge trapping characteristics which gives improved write-erase endurance of each cell. The use of oxynitride in the dielectric area and SEEQ's proprietary Q-cell design allows endurance to be specified up to 1,000,000 cycles/byte.

Memory Cell Operation

Figure 1 shows a basic E^2ROM memory cell. The number of transistors in a E^2ROM memory cell will vary from 1 to 4, depending on the density. As higher densities are designed (e.g. a 256K), the number of transistors in a memory cell will decrease to obtain miminum chip area. For example, SEEQ's 64K E^2ROM is a two transistor cell which is similar to the four transistor cell shown in Figure 1. Transistors $Q_1$and Q_2, and transistors Q_3 and Q_4 are merged in the 64K E^2ROM. In addition, separate read and write lines are not used. However the fundamental write and erase operation of the cell are the same, i.e., electrons are tunneled through the oxynitride from and to the floating gate by applying a high voltage across the sense line (top gate) and the drain.

The cell shown in Figure 1 is used in one of SEEQ's 16K E^2ROM. To read the cell, current through transistor Q1 is sensed to determine whether it is "written" (logical 0) or "erased" (logical 1). During this mode, the sense line is biased to a 2-volt reference level, and a given cell is accessed through the

CELL OPERATING VOLTAGES

Mode	Read	Erase	Write
Row Line	5V	20V*	20V*
Read Line	2V	Floating	Floating
Sense Line	2V	20V*	0V
Write Line	0V	0V	20V*

*Generated Internally

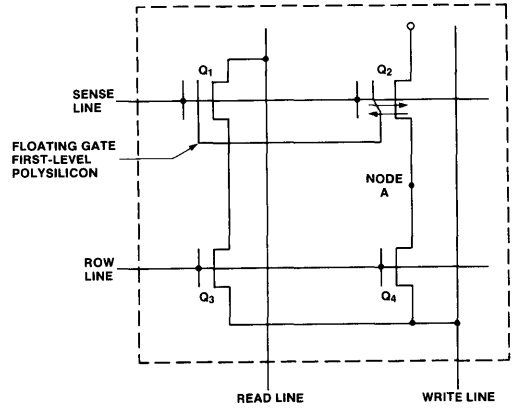


Figure 1. 52B13 Memory Cell

Results

The results are summarized in Table 1. The predictions use an assumed activation energy of Ea = 0.4eV for Ta = 55° C. They show that SEEQ's E²ROMs are more than comparable to other MOS memories. It should be noted that the 52B33 predicated failure rate will not be statistically meaningful until the number of stress device hours is increased.

Read Integrity

Read integrity is defined as the ability of the E²ROM to withstand multiple read cycles without incurring a spurious change in data pattern and/or in performance (e.g. access time). A read integrity failure would be caused by either unintentional charge gain or charge loss at a given cell as a result of the voltages applied to the cell during multiple read operations. This undesirable disturbance of a nonvolatile memory cell is often referred to as "read disturb".

The read integrity characteristics are predicted in Figure 2 through a combination of theory and experiment. First, the threshold behavior of an erased cell is measured experimentally and compared with the theoretical model for accelerated voltage conditions (V_g = 6 V and V_g = 7 V). The theoretical model is based on the Fowler-Nordheim equation and physical parameters derived from the cell structure. A by-product of this comparison is the accuracy demonstrated by the theoretical model. Second, the model is used to predict the threshold behavior of the cell under the normal operating condition of V_g = 2 V.

To interpret the curves of Figure 2, note that the cell threshold must cross the reference sense level of 2 V for a read disturb to take place. Reading from the figure, the predicted operating life is greater than 10 years even under the greatly accelerated voltage of 7 V. Under the normal gate bias of 2 V, the read integrity life is on the order of 10^7 years!

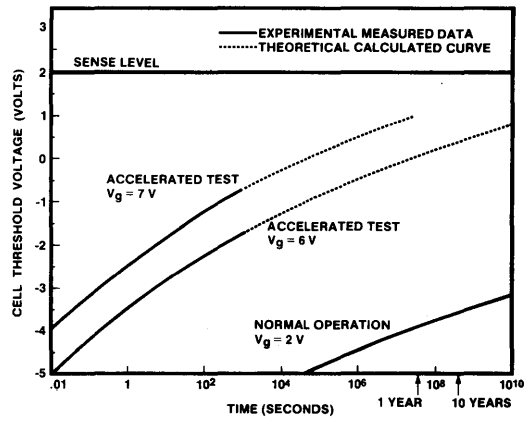


Figure 2. Read Disturb Analysis — Cell Threshold vs. Time

Static Life and Charge Gain Stress Test (CGST)

SEEQ's products have a special built-in stress mode feature which voltage stresses all memory cells simultaneously. The purpose of the stress is to accelerate "charge gain" failures: for example, those bits which would gain charge during multiple read cycles. "Static" refers to the D.C. bias of the cell periphery and "charge gain" refers to the special mode used to bias the memory array at a higher than normal voltage. Failure modes for the static portion include threshold shifts and leakages. The typical failure mechanisms are mobile ion contamination or trapped charges. The failure mode for the "charge gain" portion is a change in the state of the memory cell. The typical failure mechanism is a point defect in oxide layers.

The "static and charge gain" stress mode may be used either for screening or determining the long term "read disturb" reliability of the product.

Test Methods

Units to be stressed were drawn from finished goods inventory and written with an "all 0's" pattern. This eliminates negative charge from all floating gates. These devices were then placed in an oven with all memory cells biased and the ambient temperature held at 125° C.

Table 2. CGST Life Stress Results*

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 125° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	987	221704	2	0.063%/1000 hours

*Note: CGST data is in process for the 52B33 and 2816A/5516A and will be available from SEEQ in 4Q85.

row line (transistor Q_3) and the read line (see cell operating voltage table in Figure 1). For a cell to appear erased, Q_1 should not conduct current (an arbitrary choice of polarity). Therefore, an erased cell will have its threshold voltage raised through programming (floating gate charged with electrons) and a written cell will have its threshold voltage lowered (floating gate discharged of electrons) relative to the 2-volt reference level.

To erase the cell, the effective threshold voltage of the Q_1 is brought positive (as seen by top gate) by intentionally tunneling electrons onto the floating gate through the tunnel region in device Q_2. Refer again to the cell operating voltage table for the conditions used to accomplish this operation. To write the cell, the direction of the tunneling current is reversed, causing the floating gate to discharge its electrons and the effective threshold voltage of Q_1 to drop.

During the write operation, an internally generated voltage of approximately 20 V is applied to both the write and the row lines. Transistor Q_4 transfers this high voltage to node A if the cell has been selected. However, in deselected cells, node A is isolated from the high voltage by virtue of Q_4 being held "off". The voltage difference between node A and the sense line enables electrons to tunnel away from the floating gate.

During the erase operation, an internally generated voltage of approximately 20 V is applied to the row and the sense lines, while the write line is grounded. Transistor Q_4 in this case transfers the ground potential to node A if the cell has been selected. For a deselected cell, node A is isolated from ground by Q_4. The voltage difference between node A and the sense line now enables electrons to tunnel into the floating gate.

Operating Life

The operating life of an $E_2$2ROM is limited by its general reliability which includes integrity of the peripheral circuitry as well as the memory cells. The operating life is characterized using a dynamic high temperature life stress.

Dynamic High Temperature Life Stress

Dynamic high temperature life stress is a standard approach used to evaluate the failure rate distribution of a product under accelerated conditions. The failure rate is statistically derived from the experimental results obtained at elevated temperatures, then extrapolated back to typical operating junction temperature conditions. This extrapolation is accomplished using the Arrhenius relationship and an apparent activation energy consistent with the failure mechanisms observed. This acceleration technique works well for common causes of failure such as oxide defects, interconnect voids, and defective bonding.

For ease of calculation, the instantaneous failure rate is assumed to be constant throughout the lifetime of the product (i.e. the probability density function of the time to failure is assumed to be exponential).

Test Methods

Units to be stressed were drawn from finished goods inventory, and written with a data pattern selected to program both logic states of "1" and "0" into locations in each row and each column of the array. Initial, intermediate, and final electrical testing of the units was conducted at room temperature using a test program that checks all fundamental parametrics and functionality.

Stress Conditions

The dynamic high temperature stress was applied in accordance with the conditions prescribed in MIL-STD-883, Method 1015, Condition D. Oven ambient temperature was maintained at 125° C. The schematics are available upon request.

Table 1. High Temperature Dynamic Life Stress Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 125° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.4 eV)
52B13	560	560,000	0	0.036%/1000 hours
52B33	143	143,000	0	0.142%/1000 hours
5516A/ 2816A	342	346,576	0	0.059%/1000 hours

Results

The results are summarized in Table 2. The predictions use an assumed activation energy of Ea = 0.6eV for Ta = 55° C. The predicted charge gain failure rate is less than ½ the intrinsic failure rate of NMOS, as would be expected. This implies the field usage failure rate would be accurately predicted by dynamic life test.

High Temperature Bake (Unbiased)

(Data Retention)

Intrinsic data retention is defined as the ability to retain valid data over a prolonged period of time under storage conditions (i.e. non-operating). At the cell level, data retention is a measure of the floating gate's ability to retain charge in the absence of applied external gate bias. Data retention failures in a floating gate structure are commonly caused by dielectric defects and can be accelerated by high temperature bake stress. This characteristic provides a technique for both screening potentially defective product from the production flow as well as predicting expected retention lifetimes of outgoing product.

In order to determine the data retention capability of SEEQ's products, unbiased devices are subjected to high temperature bake at +250° C for a specified duration. The failure mode is a change in the state of the memory cell, and the typical failure mechanism is a dielectric defect resulting in "charge loss." Because dielectric defects can be induced by the electric fields generated during write/erase cycles, data retention and endurance are related topics. The effects of cycling on data retention are covered in the endurance section. In this section the intrinsic data retention characteristics are evaluated and compared against the minimum data retention goal of ten years.

Test Method

Units to be stressed are drawn from finished goods inventory and erased to an all 1's pattern (e.g. negative charge on floating gate.)

Stress Conditions

After erasing and initial testing, parts were temperature stressed at 250° C. Voltage stress is not required for this evaluation; therefore all leads are held at ground potential.

Results

The results are summarized in Table 3. Using an activation energy of 0.6 eV, the data retention lifetime predicted by the data exceed 100 years at a 55° C junction temperature. This period exceeds the industry 10 year standard for erasable memories.

Endurance

Endurance is defined as the ability of an E^2ROM to operate to data sheet specifications after repeated write/erase cycles to each byte. SEEQ specifies an endurance of both 10,000 and 1,000,000 cycles/byte. The extraordinary high endurance is accomplished using SEEQ's proprietary oxynitride process and its innovative Q cell design. Products which are specified with 1,000,000 cycle endurance are designated with "55" series part numbers.

Endurance failures are characteristically caused by dielectric breakdown occuring in the tunnel dielectric itself. This breakdown is associated with charge trapping that occurs during repeated write/erase cycles, and the corresponding build-up of electric field within the tunnel dielectric. Because this behavior is central to the device physics of an E^2ROM memory cell, endurance will be discussed in two parts: first at the cell level, then at the product level.

Single Cell Characteristics

During each write/erase operation of a floating-gate E^2ROM cell, a miniscule amount of charge is trapped in the dielectric through which the programming charge tunnels[1]. The cumulative effect of this charge trapping has a strong impact on the effective threshold voltage that the cell exhibits at each write/erase cycle. The envelope of the "written"

Reference:

[1] Ching S. Jeng et al. *IEDM Technology Digest* 1982, p. 811

Table 3. High Temperature Bake Test Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 250° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	150	148192	4	0.003%/1000 hours
2816A/ 2817/ 5516A	37	6216	0	0.0136%/1000 hours

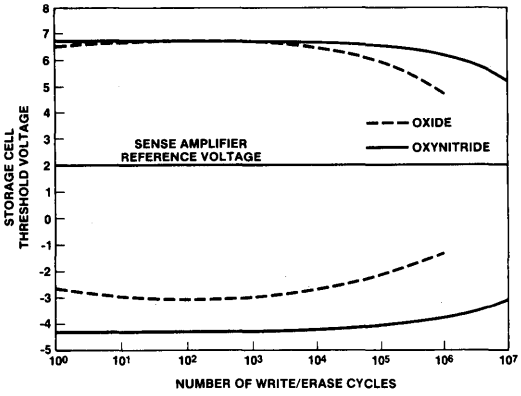


Figure 3. Endurance Characteristics

threshold voltage and the "erased" threshold voltage plotted over a number of cycles is referred to as the cell threshold "window", and is a key figure of merit for any E²ROM cell. Referring to the representative threshold window shown in Figure 3, the net effect of charge trapping results in an initial widening of the window (due to positive trapped charge), and subsequent narrowing of the window (due to net negative trapped charge). Ultimately, negative charge trapping sets the upper limit on endurance when the window becomes too narrow to be useful.

As seen from the endurance plot of Figure 3, the threshold window achieved using the SEEQ oxynitride dielectric represents an improvement over the traditional silicon dioxide case by at least a factor of ten. The oxynitride window demonstrates very little closing at 10^6 cycles, and provides a very useable window at 10^7 cycles.

The improved performance of oxynitride over oxide is directly related to the superior trapping characteristics of the oxynitride film, as shown in Figures 4 and 5. In Figure 4, the positive charge trapping characteristics of oxynitride and oxide are compared as a function of field strength (the principal independent variable). The positive charge trap density is consistently lower for oxynitride by approximately a factor of four. In Figure 5, the negative charge trapping characteristics of oxynitride and oxide are compared as a function of total injected charge (the principal independent variable in this case). Note the benefit of oxynitride in this case continues to increase with increasing charge, thus verifying the endurance improvement first observed in Figure 3.

Product Endurance:

Test Methods

Units were pulled from finished goods inventory and stressed by performing repeated write/erase cycles on every byte in the memory. Data retention, read/write functionality, AC performance, and parametrics were periodically tested against data sheet specs. Failures (typically caused by the selective failure of random bits) were analyzed and compiled for failure rate calculations.

Results

A summary of the results is shown in Table 4. It shows that all of SEEQ's E²ROMs meet or exceed the intrinsic MOS failure rate of 0.05%/1000 hours if you write once per day. It should also be noted that the Q-cell E²ROMs have higher endurance than the non-Q cell 52B13. All of SEEQ's E²ROMs are Q-cell except for the 52B13. For applications where writing occurs more frequent or where a failure rate of less than .05%/1000 hours is required, then a 1,000,000 cycle part such as the 16K autoerase 5516A should be considered.

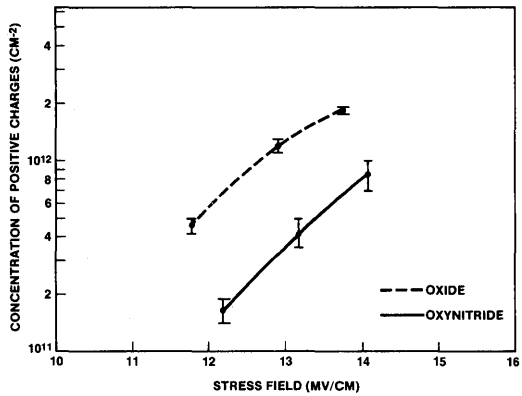


Figure 4. Comparison of Positive Charge Trapping at Tunneling-Dielectric/Si Interface

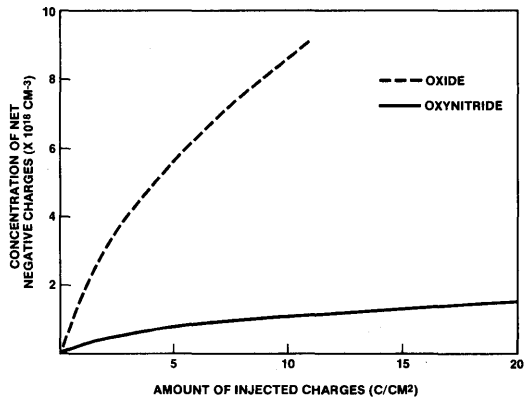


Figure 5. Comparison of Negative Charge Trapping

Table 4. Write/Erase Endurance Test Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 250°C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55°C (Ea = 0.125 eV)	Equivalent Failure Rate Writing Once Per Day
52B13	2797	26,798,000	58	0.4%/1000 cycles	0.017%/1000 HRS
2816A/ 2817/	609	508,030,000	7	0.036%/1000 cycles	0.002%/1000 HRS
5516A	1154	1,781,905,000	16	0.002%/1000 cycles	0.00008%/1000 HRS
52B33	527	52,700,000	6	0.031%/1000 cycles	0.0013%/1000 HRS

Accelerated stress data is updated quarterly and is available from SEEQ Technology. Contact: Literature Dept. M/S 3, 1849 Fortune Dr., San Jose, CA 95131.

Refer questions to:
David Sweetman
Director of QA
(408) 262-5041

Memory Products
Application Note

2A

MICROPROCESSOR INTERFACING WITH SEEQ's LATCHED E²ROM

seeq
Technology, Incorporated

Microprocessor Interfacing with SEEQ's Latched E²ROM

Introduction

This application note describes the interfacing of SEEQ's "latched" Electrically Erasable Read Only Memory (E²ROM or E²) to a microprocessor bus. The latched E²ROM family is comprised of a 16K 52B13 and 64K 52B33. On each of these devices there are internal latches on all inputs except write enable. A byte must first be erased before it can be written. In addition to the latched E²ROM family, SEEQ has a timer E²ROM family. This family is comprised of a 16K 2816A (24 pins), a 16K 2817A (ready/busy) and a 64K 2864 (ready/busy). The timer family has internal latches on all inputs and has an internal timer which automatically performs a byte erase before write. In this application note, the E² used is SEEQ's 52B13, a 2K x 8 memory. Since the timing of the higher-density members of the family is compatible, the circuits given can be extended to interface equally well with the 52B33 (8K x 8). Both bus timing and software timing are used to gate the control signals. The case presented here uses general control signals to permit adaptation to any system's bus structure. In addition, modifications are given for interfacing to specific processors.

Interface Signals

The solution presented here (see Figure 1) uses an $\overline{S}-\overline{R}$ flip-flop (74LS00) with TTL gates (74LS32) to latch $\overline{WE}$ for the 52B13. This flip-flop causes valid data to be latched correctly, satisfies device setup and hold times, and allows easy latch/unlatch of the $\overline{WE}$ signal.

The system-dependent direct bus interface components form the second part of the interface circuit. These components will generate $\overline{\text{CHIP SELECT}}$ and $\overline{\text{E²ROM SELECT}}$ to enable this part of memory. $\overline{\text{CHIP SELECT}}$ is usually generated separately for each word-wide group of devices. In this way, it chooses the actual devices to be written. $\overline{\text{E²ROM SELECT}}$ would be an "OR" function of the $\overline{\text{CHIP SELECT}}$ signals for all the devices for which this latch gates $\overline{WE}$. With $\overline{WE}$ wired in common, only one gated latch is required for the E²ROM array. Of course, fanout must be considered, with a high-current driver used if necessary. In the example bus interfaces shown in this application note, gating for one device is assumed, and $\overline{\text{E²ROM SELECT}}$ is tied directly to $\overline{\text{CHIP SELECT}}$.

The bus interface components perform other tasks common to a memory/bus interface. For a multiplexed data bus, the bus interface components must demultiplex the data and addresses. In addition, this bus interface circuitry may generate $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$, if required. Details of this bus interface are given in the section "Considerations for Special Applications," beginning on page 5.

Details of Operation

Byte Write or Erase

The timing diagram in Figure 2 shows the details of a byte write or erase operation for SEEQ's latched E²ROM family. The two modes are the same, except that hex "FF" is presented to the I/O lines for erasure. Due to this similarity, only the write mode will be discussed.

The first step is initiation of a write cycle. First, the processor issues addresses, and the system's decoding circuitry brings $\overline{\text{CHIP SELECT}}$ valid. Although the chip is enabled at this point, a write to the chip has not yet begun, because $\overline{\text{MEMORY WRITE}}$ has

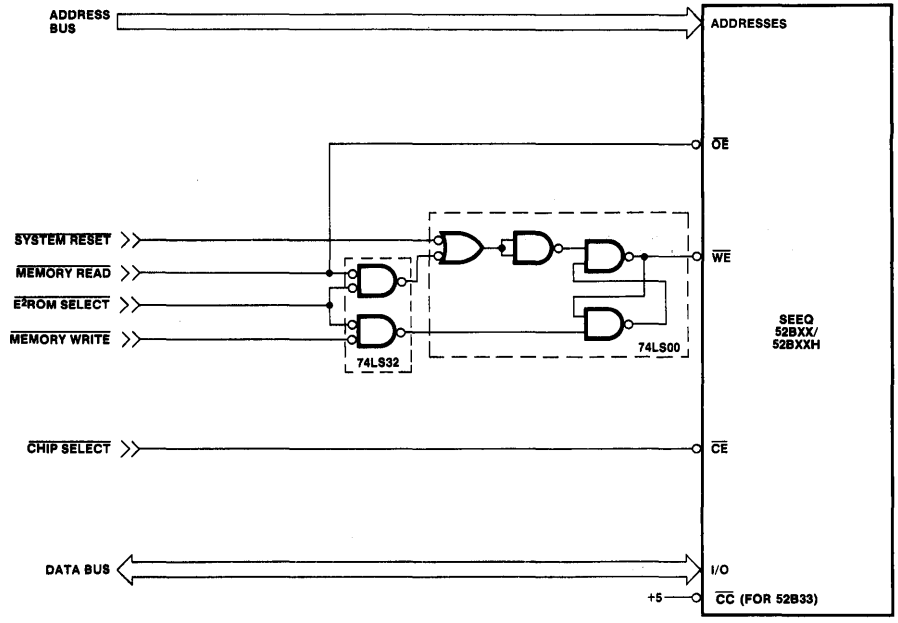


Figure 1. E²ROM Interface Circuit

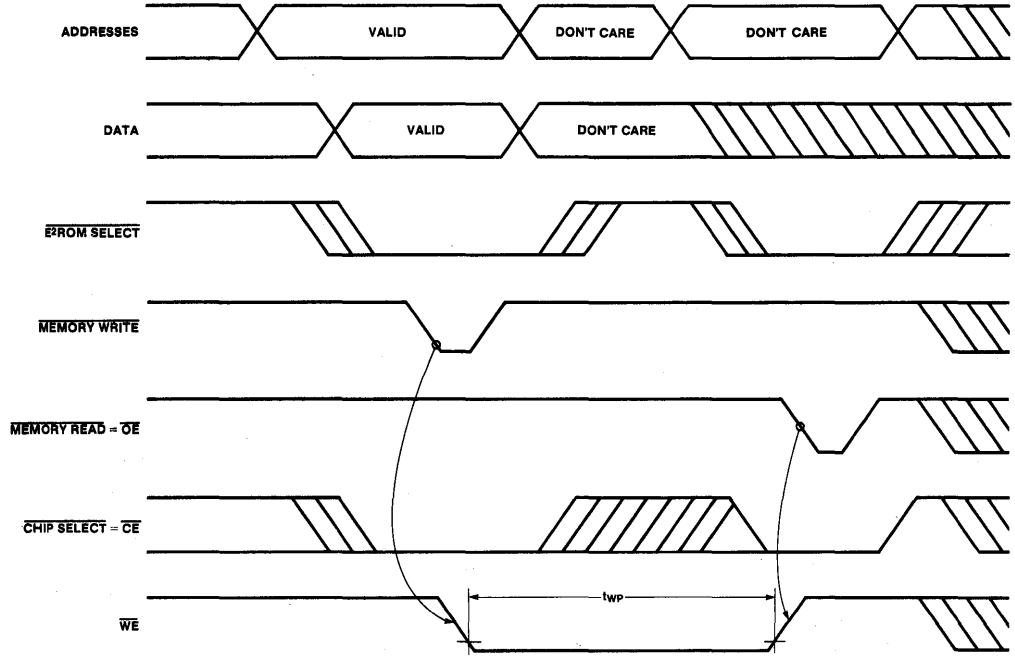


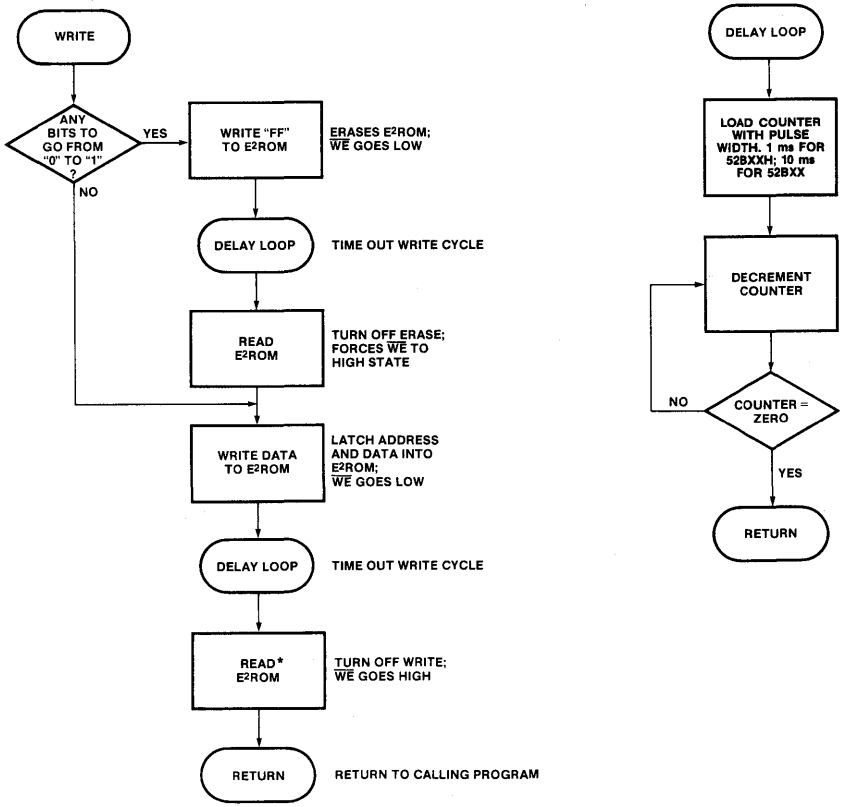
Figure 2. Write-Cycle Timing Diagram Latched E²ROM Interface Application

not yet been issued. This prevents inadvertently writing to an incorrect address as the address lines are allowed to settle out before a write is initiated. Following the timing events above, the active level of MEMORY WRITE sets the flip-flop, bringing $\overline{WE}$ low to the E^2. Data, Addresses, $\overline{CE}$, and $\overline{OE}$ are latched at this point.

In the second part of a write, $\overline{WE}$ continues to be active low for the entire write cycle. This requires a timeout, which can be effected in any of several ways. The designer can use a timing loop in software, or trigger a timer which interrupts the processor after the correct time. The software timeout may require less hardware on-board. The hardware timeout, on the other hand, allows the CPU to perform other tasks. Obviously, a good compromise is a software architecture with regular (perhaps one-millisecond) timing interrupts, for system real-time synchronization. Division of the task between hardware and software is best left to the individual systems engineer.

Regardless of the method used in the timeout, the write pulse is terminated by $\overline{WE}$ being brought high. This is effected by a read to any location in the device, which resets the flip-flop to bring $\overline{WE}$ high. A second read cycle is required for byte verify. System designers should allow extra time between the two reads to meet write recovery time (t_{WR}) requirement. This method of write-cycle termination provides another form of protection against inadvertent writing to the chip. Even if a statistically unlikely succession of glitches were to trigger both flip-flops, enable the gates, and bring $\overline{WE}$ low, a subsequent read to the device could terminate the write before data would be written.

For the case of a fully software-timed write, a flowchart is given for the sequence of operations (see Figure 3). This processor-independent flowchart handles all the erasure and writing for storing data in the E²ROM, using the circuit from Figure 1. In addition, a segment of example code (written for the Z8) is shown (see Figure 4).



*Data is not valid during this cycle.

Figure 3. Flowchart for 52BXX Erase/Write — Software Timing

```
                        186 //-----------------------
                        187 // The following is a general routine for writing
                        188 // data contained in the working register
                        189 // DataReg to an EEROM in
                        190 // the location pointed to by the working register
                        191 // pair AdReg. This EEPROM is assumed to be in the
                        192 // external data memory of Z8.
                        193 // Write FF to erase byte.
P 0060 7C  FF           194 EEWR:   LD      OutReg, #%FF
P 0062 92  70           195         LDE     @AdReg,  OutReg
P 0064 D6  0071         196         CALL    WaitWP          // Wait for Twp
P 0067 82  80           197         LDE     NowReg, @AdReg  // Turn off WE
                        198 // Now, write the data to the part.
P 0069 92  90           199         LDE     @AdReg, DataReg
P 006B D6  0071         200         CALL    WaitWP          // Wait for Twp
P 006E 82  80           201         LDE     NowReg, @AdReg  // turn off WE
                        202
P 0070 AF               203 FinWr:  RET             //return from routine
                        204 // End of EEPROM Write Routine
                        205 //-----------------------------------------------
                        206
                        207 // Timing routines
P 0071 EC  0A           208 WaitWP: LD      RLoop2, #Twp  // # of ms to wait
                        209                         // 10-> wait 10 mS.
                        210                         // 1 -> Wait 1  mS.
                        211
P 0073 D6  007E         212 WPLoop: CALL    Wait1ms
P 0076 00  EE           213         DEC     RLoop2
P 0078 6D  007D         214         JP      Z, DunWP
P 007B 8B  F6           215         JR      WPLoop
P 007D AF               216 DunWP:  RET             // Done with Twp.
                        217
                        218 // Basic 1 msec timing routine-
                        219 // adjust for microprocessor crystal freq.
                        220 // The value of Hex58 (Dec88) works with
                        221 // a Z8 with a 6.144 MHz xtal.
                        222 // Use %6A for 7.3728 MHz xtal. Elimination
                        223 // of NOP, or xtal substitution, will
                        224 // require recalibration.
P 007E FC  6A           225 Wait1ms: LD     RLoop3, #%6A
                        226
P 0080 FF               227 Tim1p:  NOP
P 0081 00  EF           228         DEC     RLoop3
P 0083 6D  0088         229         JP      Z, Dun1ms
P 0086 8B  F8           230         JR      Tim1p
                        231
P 0088 AF               232 Dun1ms: RET             // Done with wait
                        233
                        234 //End of EEPROM Timing Routines
                        235 //---------------------------------
```

Figure 4. Sample Z8 Code for 52BXX Write

Read Operation

The timing for a read (see Figure 5) is simpler than for a write. In the read mode, the on-chip latches are transparent. The leading (falling) edge of $\overline{\text{CHIP SELECT}}$ brings $\overline{\text{CE}}$ low, and the falling edge of $\overline{\text{MEMORY READ}}$ brings $\overline{\text{OE}}$ low. Data is available from the 52BXX E²ROM after a delay of T_{OE} (from $\overline{\text{OE}}$) or T_{CE} (from $\overline{\text{CE}}$). Table 1 shows the T_{ACC} required for operation with sample microprocessors, using no wait states. Memory devices currently available from SEEQ feature T_{CE} as fast as 200 nanoseconds. For certain new microprocessors (for example, the 68000 or 8085A-1) which may require faster access, SEEQ is currently developing memories with access times of 150 nanoseconds or less.

To terminate the read, the rising edge of $\overline{\text{MEMORY READ}}$ brings $\overline{\text{OE}}$ high. $\overline{\text{CE}}$, however, is dependent only on $\overline{\text{CHIP SELECT}}$, and remains active low for the entire microprocessor cycle.

Table 1. Zero-Wait State Required Minimum T_{ACC} (Assuming zero delay for buffers and drivers)

Microprocessor	Clock Freq. (MHz)	Required T_{ACC} (nanoseconds)
72720	10	350
8085A/8085AH	3	460
8085A-2/8085AH-2	5	270
8085A-1/8085AH-1	6	175
8086/8088	5	402
8086-2/8088-2	8	267
8086-1	10	227
Z8	8	310
Z80	2	575
Z80A	2.5	325
Z80B	6	190
6800	1	605

Considerations for Special Applications

Use with Z8, Z8000 Systems

The implementation of the circuit shown in Figure 1 in a Z-Bus application allows simple generation of the control signals. First, the control signals $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$ can be generated by one half of a 74LS139 decoder, as in Figure 6. In addition, for the Z8, the lower byte of addresses must be latched, due to the multiplexing of address and data. This can be easily accom-

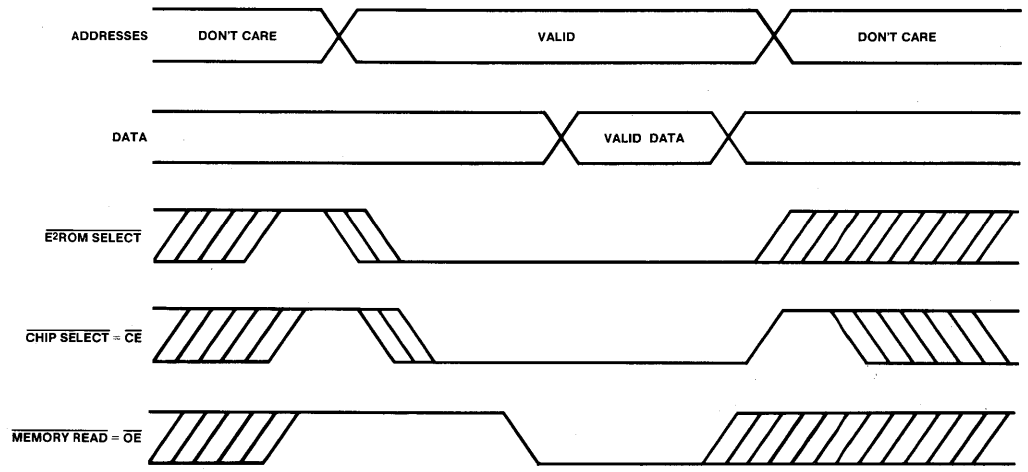


Figure 5. Read-Cycle Timing Diagram

REL/APP NOTES

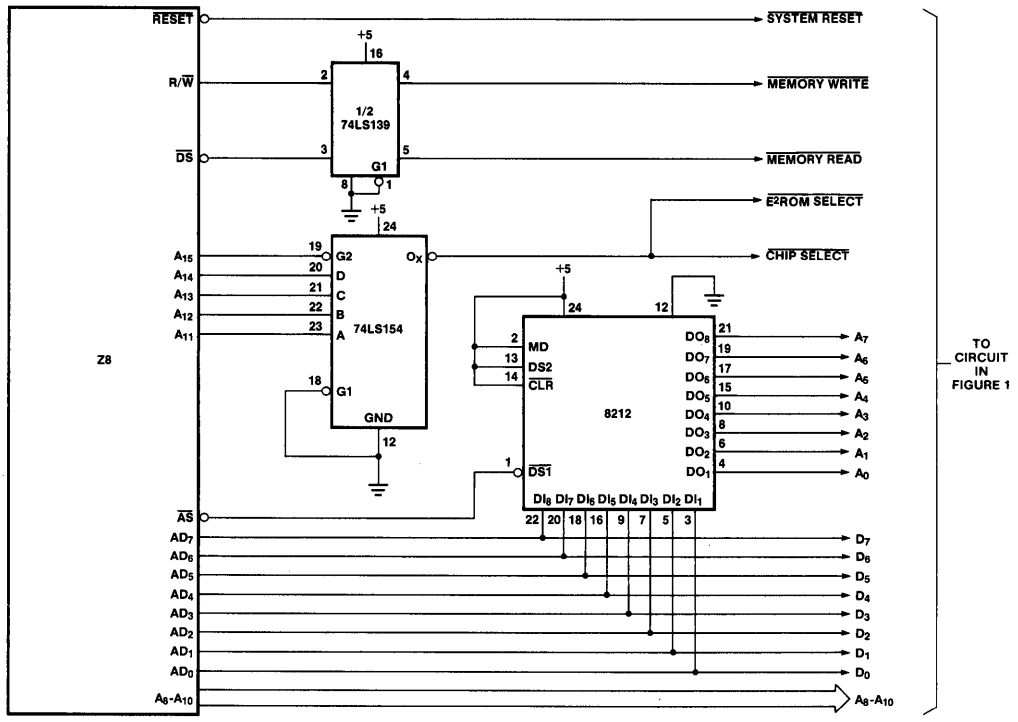


Figure 6. Interfacing to a Z8

plished with an 8212 octal latch, as in Figure 6. Interfacing to a Z8000 (or 16-bit Z-Bus) requires an additional 8212 latch, to demultiplex AD_8-AD_{15}. $\overline{AS}$, the Z-Bus address strobe, is active low, and must be connected to the active low input in order to clock these latches.

Use with Z80 Systems

The circuit shown in Figure 7 provides a bus interface to a Z80, Z80A, or Z80B processor. In Figure 7, $\overline{MEMORY\ READ}$ and $\overline{MEMORY\ WRITE}$ are generated from combining $\overline{MREQ}$ with the Z80 $\overline{RD}$ and $\overline{WR}$, respectively. Since address and data are issued by the Z80 processor on separate lines, the 8212 latch is not needed.

Use with 8085 Systems

The implementation of the E²ROM interface circuit in an 8085 system is extremely simple. Figure 8 shows the bus interfacing necessary. $\overline{MEMORY\ READ}$ and $\overline{MEMORY\ WRITE}$ are issued by the processor directly. However, $\overline{MEMORY\ WRITE}$ must be delayed, as shown in Figure 8, to ensure latching of valid data. $\overline{CHIP\ SELECT}$ is generated from the top 5 address bits and IO/$\overline{M}$, using a 74LS154 decoder. The $\overline{RESET}$ to the 8085 processor also supplies $\overline{RESET}$ for the E²ROM interface. Finally, the demultiplexing of address and data lines is accomplished by a 74LS373 latch triggered by ALE. Alternatively, an 8212 latch can be used but requires more board space.

Interfacing to 8088/8086 (Minimum Mode) Systems

The above considerations for implementation of this solution in an 8085 system also apply to an 8088/8086 system operation in minimum mode, with two additions. As above, the processor issues ALE, $\overline{RD}$, $\overline{WR}$, and multiplexed address/data. However, an inverter is required in order to produce IO/$\overline{M}$ from $\overline{M/IO}$. In addition (for an 8086), another octal latch must be added, in order to demultiplex AD_8-AD_{15}.

The time delay indicated in Figure 8 depends on the type of processor used and its clock frequency. For a 5 MHz 8088/8086, this time delay should be 100 nanoseconds; for an 8088-2/8086-2 at 8 MHz, it should be 60 nanoseconds. For a 10 MHz 8086-1, the time delay should be 50 nanoseconds.

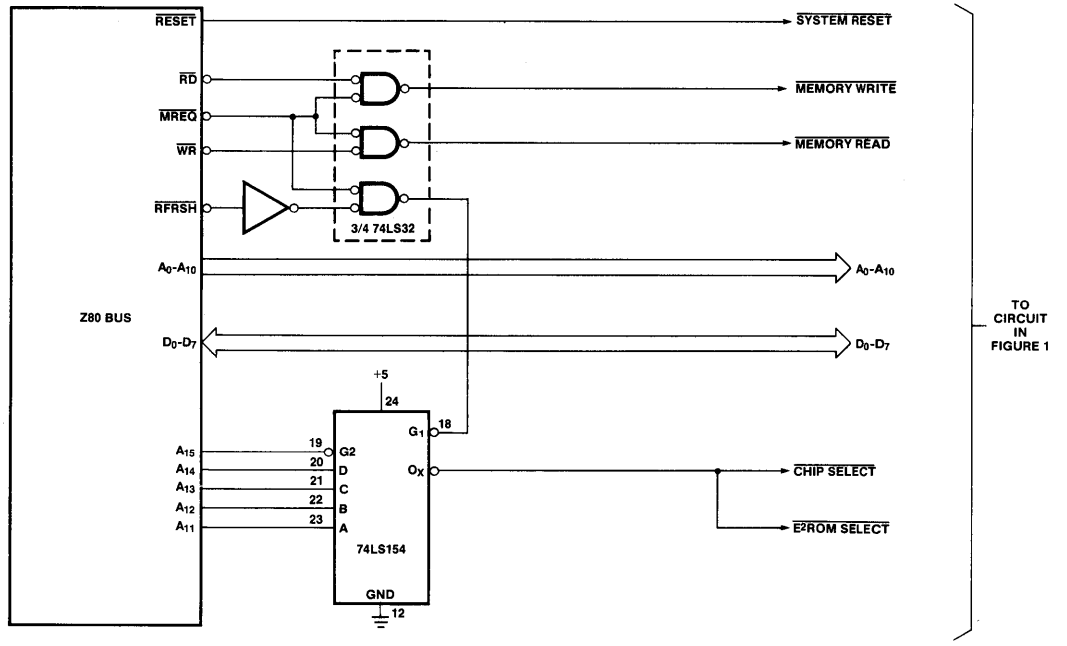


Figure 7. Bus Interface — Z80

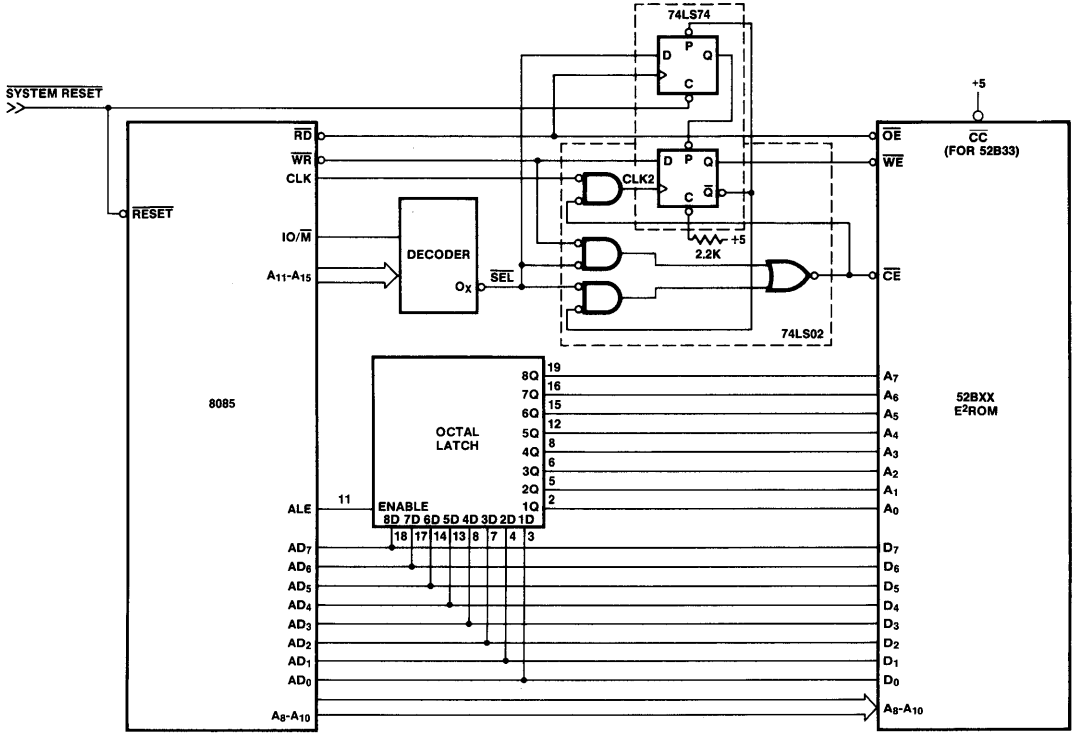


Figure 8. Bus Interface Circuitry — 8085 System

Interfacing with 72720 Systems

The 52BXX E²ROM can be interfaced to SEEQ's new 72720 microcomputer (with 2K x 8 on-board E²ROM) more easily than to any other processor. The 72720 PRG instruction operates off-board, to program an external E²ROM. This instruction initiates latching and timing of $\overline{WE}$, as well as presentation of valid data. These tasks are handled automatically within the 72720. As a result, the write enable latch circuit of Figure 1 is not required. Total 52BXX interface hardware, shown in Figure 9, is very simple, even including a 74LS373 latch to demultiplex the lower eight bits of address. The software required for programming is shown in Figure 10. This example subroutine erases and writes one byte.

Interfacing with the 6800

One example of a complete interface between a 6800 processor and a 52BXX is shown in Figure 11. The DBE signal from the 6800 is delayed for a time between 250 and 350 nanoseconds, in order to provide a strobe for valid data. This data strobe clocks R/$\overline{W}$ into the flip-flop at the correct time, so that the falling edge of $\overline{WE}$ can satisfy timing requirements with respect to valid address, data, and control signals.

Conclusion

This application note has been prepared to assist the designer in implementing the technology of latched E²ROMs in systems requiring adaptability. The designer is encouraged to create new designs based on these ideas. E²ROM technology, while still in its infancy, holds the promise of being the memory breakthrough for the eighties. With a reliably non-volatile approach to alterable program memory, systems for control of avionics, manufacturing, and data acquisition can be enhanced in usefulness. With the timing to use the advanced technology of E²ROMs, the system designer can incorporate more features now, while allowing still more flexibility for the future.

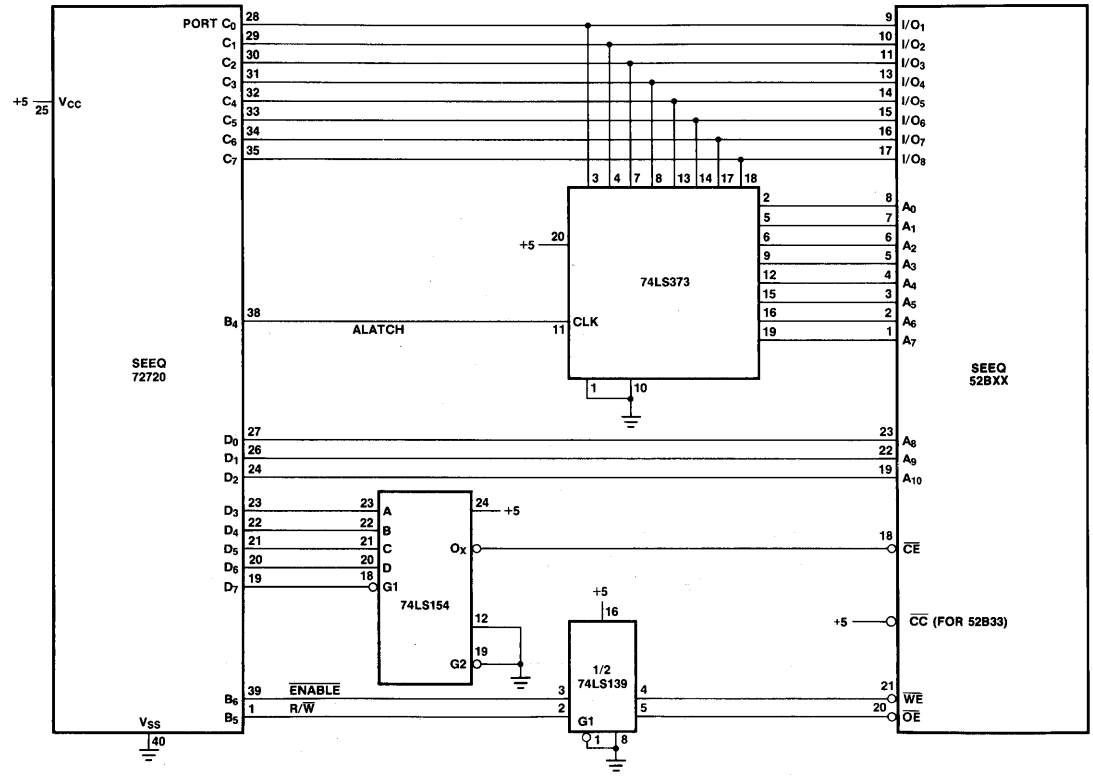


Figure 9. 72720 Interface

```
0 ERRORS
7000 ASSEMBLER  REV 1.3
>
0001  9000        ********************************************************
0002  9000        *                                                      *
0003  9000        *       EEROM  AUTO ERASE BEFORE WRITE ROUTINE         *
0004  9000        *                                                      *
0005  9000        *     DATA TO BE PROGRAMMED IN REGISTER 102            *
0006  9000        *   LOCATION TO BE PROGRAMMED IN REGISTERS 100/101     *
0007  9000        *                                                      *
0008  9000        ********************************************************
0010  9000        *
0020  9000 0066  EEDAT   EQU R102       DATA TO BE PROGRAMMED
0030  9000 0065  EEADR   EQU R101       POINTER TO LOCATION
0040  9000 B8    EEWR    PUSH A         SAVE ACCUMULATOR
0050  9001 22            MOV %>FF,A     IS LOCATION ALREADY ERASED?
      9002 FF
0060  9003 9D            CMPA *EEADR
      9004 65
0070  9005 E2            JEQ PROG
      9006 00
0080  9007 04            PRG *EEADR     IF NOT PROGRAM WITH FF HEX
      9008 65
0090  9009 12    PROG    MOV EEDAT,A    IF ERASED PROGRAM DATA
      900A 66
0100  900B 04            PRG *EEADR
      900C 65
0110  900D B9            POP A          RESTORE ACCUMULATOR
0120  900E 0A            RETS           RETURN
0130  900F              END
<
```

Figure 10. 72720 Code for Programming 52B13/33

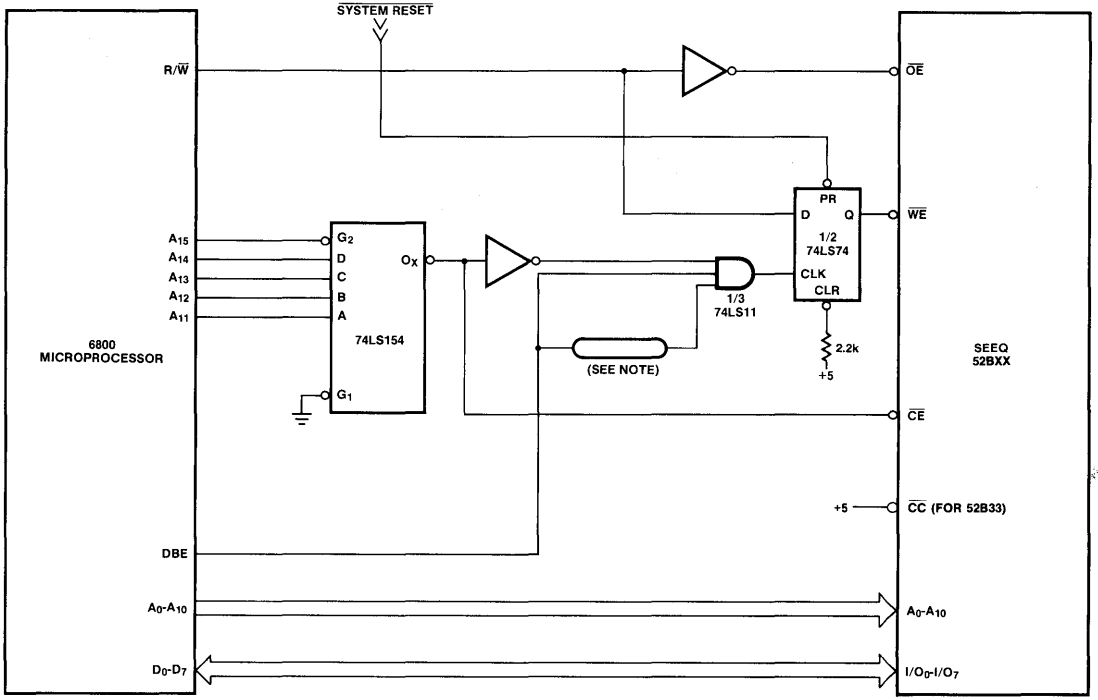
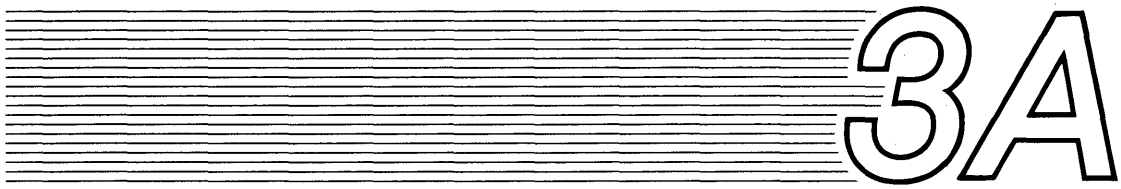


Figure 11. 6800/52BXX Interface

Communications Products Application Note



MANCHESTER ENCODING AND DECODING FOR LOCAL AREA NETWORKS

seeQ
Technology, Incorporated

Manchester Encoding and Decoding for Local Area Networks

Introduction

Ethernet alias IEEE 802.3 CSMA/CD

Ethernet is the first industry-standard protocol for local area networks supported internationally by computer manufacturers in the U.S. and Europe.

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corporation. Since then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be both reliable and efficient in a wide variety of local area network applications.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry-standard. This committee has been populated by representatives from both U.S. and European computer manufacturers. After three years of reviewing and polishing the specification, their work is about to be published by IEEE Press under the name "IEEE 802.3 CSMA/CD Local Area Network Standard Protocol." It is the result of a collaborative effort of the IEEE, the European Computer Manufacturers Association, the American National Standards Institute and dozens of computer industry representatives who have donated their time and expertise to this undertaking.

Ethernet alias IEEE 802.3 CSMA/CD uses broadcast network topology. That is to say, a signal transmitted by any station reaches all other nodes on the network. This is in contrast to other topology types, such as "star" and "ring", which use uni-directional point-to-point interconnects. Transmitted messages in Ethernet are "broadcast" on a 50Ω trunk coaxial cable segment. Communication nodes are attached to this cable via passive taps, so that new nodes can be added at any time without interrupting the network service. Stations on the network can be addressed individually, in "multicast" groups or by the "broadcast mode" to all nodes simultaneously. The broadcast topology is effective for nearly all network applications, yet it is simple and inexpensive to implement.

The medium access method is CSMA/CD, Carrier Sense, Multiple-Access with Collision Detection. Figures 1 and 2 illustrate the transmit and receive state diagrams for this access method. The Carrier Sense function is used to detect activity on the medium. This information is used both for enabling the receiver and for avoiding multiple simultaneous transmissions (collisions) with other transmitters. When a node has a message to be transmitted, it begins to transmit as soon as the medium has been idle for a minimum of 9.6 μs, the minimum for interframe gap. If a collision occurs, the stations transmitting will defer pseudo-random time intervals, then reattempt the transmission. The CSMA/CD network is normally a "peer" network (non-hierarchical) with every node having equal access to the medium.

Figure 3 shows a typical CSMA/CD node configuration. In the station equipment or "Data Terminal Equipment" (DTE), the System Interface connects the host system bus to the network. This interface varies depending on the processor used and the system requirements of the DTE. It could be a direct-memory access (DMA) type, with or without dedicated buffer memory, or a FIFO-based interface.

Data Link functions are performed by SEEQ's 8003 Ethernet Data Link Controller (EDLC™) chip. This device performs medium access control, data encapsulation, data decapsulation and error detection functions.

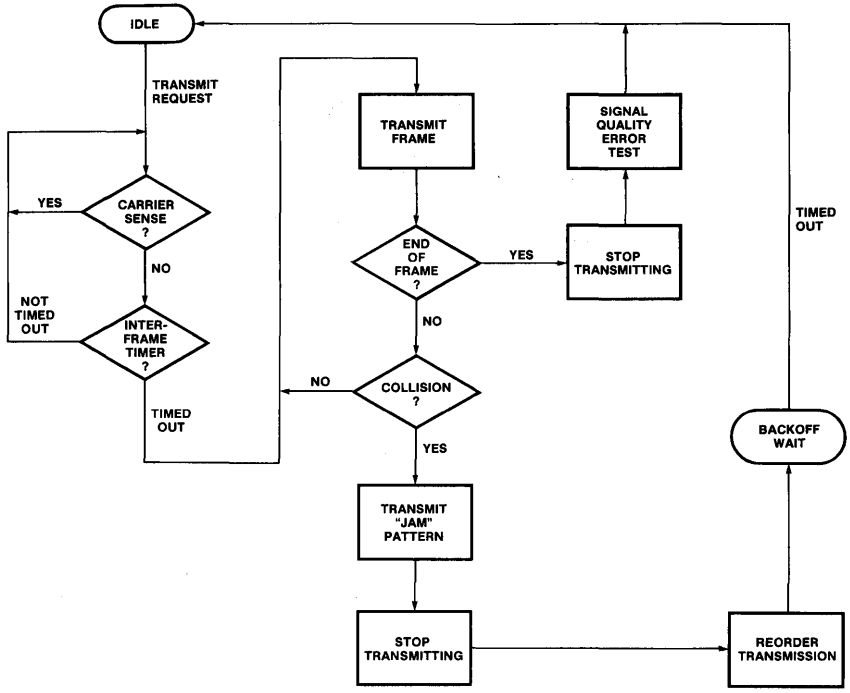


Figure 1. Ethernet/IEEE 802.3 CSMA/CD Transmitter State Diagram

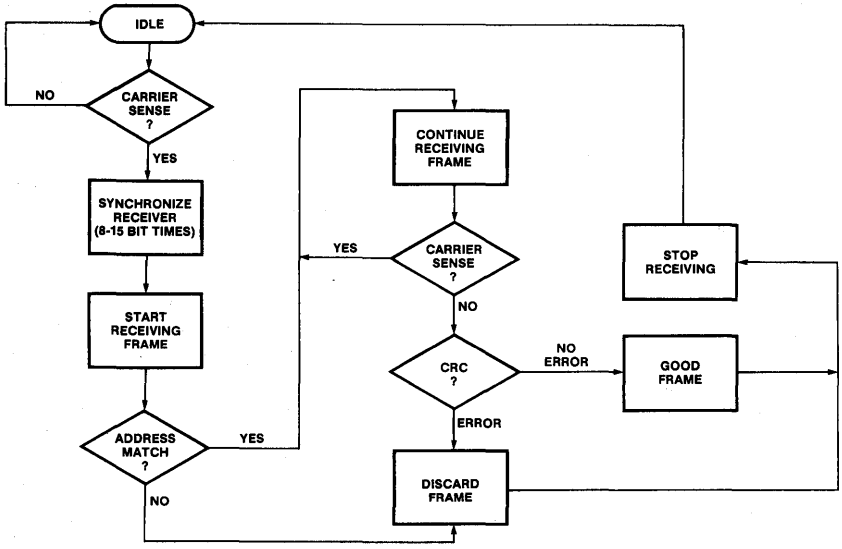


Figure 2. Ethernet/IEEE 802.3 CSMA/CD Receiver State Diagram

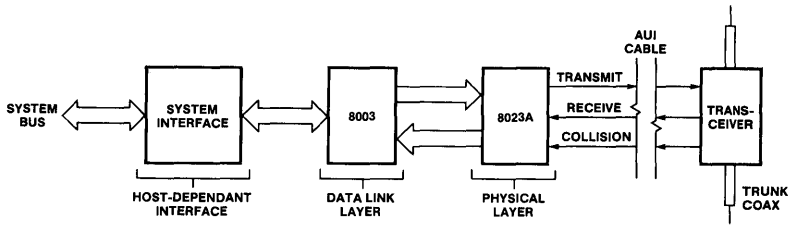
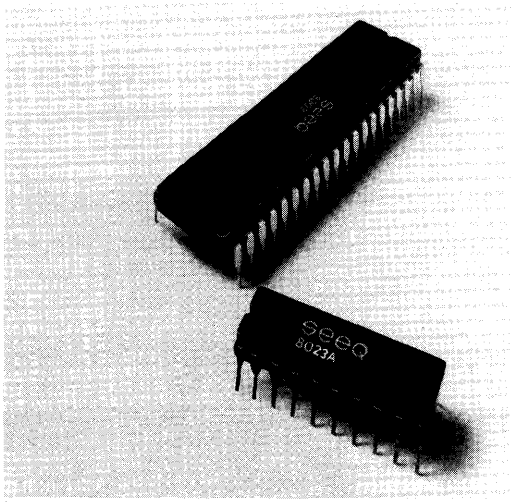


Figure 3. Ethernet Node Configuration

The Physical Layer functions, carrier sense, collision signal detection and data encoding and decoding are performed by SEEQ's 8023A Manchester Code Converter (MCC™) chip. Manchester Code, illustrated in Figure 5, is the bit-encoding format used for the transmitted signal on both the Access Unit Interface (AUI) cable and the Trunk Coax cable.

The AUI cable is optional. The Transceiver or Media Access Unit (MAU) can plug directly into the Data Terminal Equipment (DTE) connector without cabling if desired. The Access Unit Interface consists of 78Ω balanced, shielded twisted-pair connections, biased at the DTE end and transformer-coupled at the Transceiver end.

Besides the passive tap to the Trunk Coax, the Transceiver provides signal amplification, preconditioning on the receive side, impedance matching, DC isolation, collision detection and collision signaling generation.



SEEQ's Ethernet Chip Family: 8003 EDLC™ Ethernet Data Link Controllers, 8023A MCC™ Manchester Code Converter.

PREAMBLE	A_D	A_S	C	INFORMATION	FCS
NO. OF BYTES: 8	6	6	2	46-1500	4

Figure 4. Ethernet/IEEE 802.3 CSMA/CD Frame Format

Figure 4 shows the IEEE 802.3 CSMA/CD Frame Format. The frame is divided into six fields. The first is the Preamble, 8 bytes in length. Alternating 1s and 0s comprising this field serve to synchronize Manchester decoders for receiving. The next two fields are the Destination and Source Address fields, each 6 bytes in length. Next is a byte-count field which contains a value equal to the number of data bytes in the subsequent Information field. The Information field is 46 to 1500 bytes in length. The final field is the Frame Check Sequence. It contains a 32-bit CRC calculation performed on the preceding four (4) fields. (The CRC calculation excludes the Preamble field.) Total frame length is 72 to 1526 bytes.

In summary, the IEEE 802.3 CSMA/CD protocol standard specifies the Data Link and Physical layers of the protocol which include the following:

Data Link Layer

- Link access method (CSMA/CD)
- Collision-handling method
- CRC error detection method
- Node addressing methods
- Frame format

Physical Layer

- Medium characteristics
- Signaling characteristics
- Data Rate 10 MBPS
- Carrier Sense Function
- Collision detection and signaling
- Code for transmitted signal (Manchester Code),

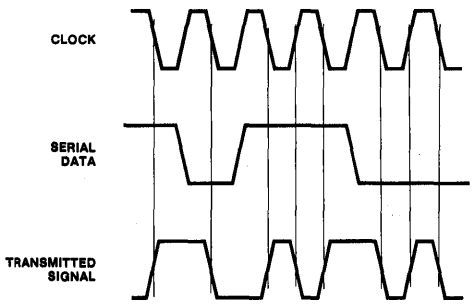


Figure 5. Manchester Code Example

Manchester Code

Manchester Code is the physical signaling code used in the IEEE 802.3 CSMA/CD protocol.

In Manchester Code, clock and data are combined such that each bit is encoded by a transition from low-to-high or high-to-low. This assures that there is adequate timing information present in the serial data stream at all times to keep the receiver in synchronization with the data pattern. The bit-center transitions serve a double purpose. They not only encode the bit being transmitted by the polarity of the transition, but they also serve to mark precisely where the bit center is located in time.

Figure 5 shows an example of Manchester-encoded data. Each serial bit to be transmitted is coded as a high-to-low or low-to-high voltage transition. A HIGH or "mark" bit is coded as a low-to-high transition and a LOW or "space" as a high-to-low. These transitions are shown to occur at the bit-center position in Figure 5. If adjacent data bits alternate between 1 and 0, only the bit-center transitions occur, as is the case during the Preamble. Where two 1s or two 0s occur in sequence, an intervening bit-boundary transition is inserted to correct the polarity of the line for the next bit.

The bit-center transitions provide all the necessary information about both data and clock needed by the receiver to decode the data stream. Bit-boundary transitions are used to restore the correct polarity between two bit cells which are either both 0s or both 1s. These transitions also contain information about both clock and data, but since it is redundant with the information provided by the bit-center transitions, its use in the receiver is optional. In some decoder implementations, it is an integral part of the decoding algorithm, and in others it is not used at all. Table 1 gives a summary of the interpretation of each element of the code.

Table 1. Elements of Manchester Code

	Bit-Center Transition	Bit-Boundary Transition
Data	High-to-Low = 0 Low-to-High = 1	Low-to-High = 0,0 High-to-Low = 1,1 No Transition = 0,1 or 1,0
Clock	Transition occurs at Bit-Center Time	Transition occurs at 50% Time between Two Bit-Centers

Manchester Code Converter Functional Description

Manchester Encoder

Figure 6 shows a typical circuit for implementing the encoder function. A 20 MHz crystal clock provides the precise, stable time base required for the transmitted signal. This clock must be within 0.01% of its nominal value to conform to the IEEE 802.3 CSMA/CD specification. The clock output drives two

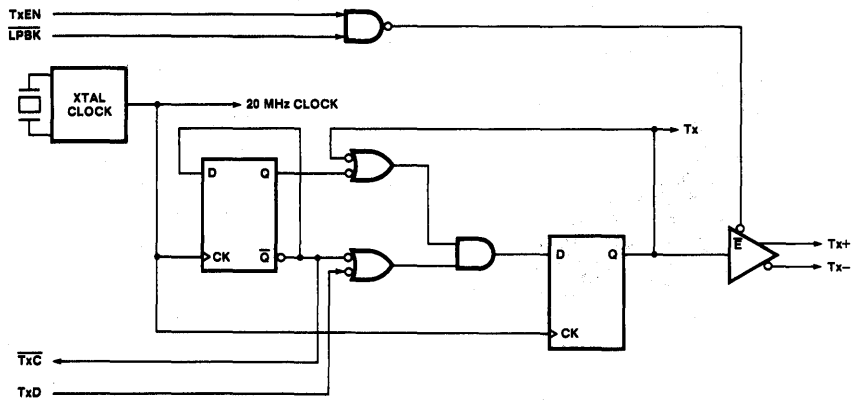


Figure 6. Basic Manchester Encoder

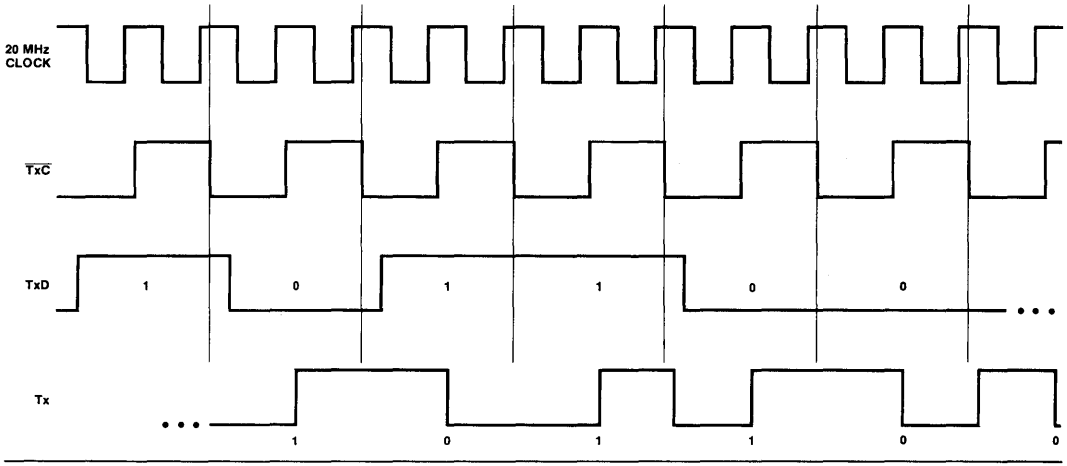


Figure 7. Timing Diagram for Encoder in Figure 6

D-type flip-flops. The flip-flop on the left divides the frequency by 2 and provides true and complement clock outputs at 10 MHz ($\overline{TxC}$ and TxC). $\overline{TxC}$ is used by the 8003 EDLC™ chip to shift out the bits of the frame, one at a time, to the Encoder over the TxD line. The flip-flop on the right samples the TxD data line once every 100 ns when the $\overline{TxC}$ line is high and its clock input goes high. At this time, the complement of the data is loaded into this flip-flop and driven out on the Tx+/— pair. Fifty nanoseconds later, the flip-flop is clocked again. This time $\overline{TxC}$ is low and Q is fed back, inverted to the D input, thus the flip-flop always toggles, encoding the bit-center transition. Fifty nanoseconds later the next bit is inverted and loaded into the encoding flip-flop and the process continues.

The output driver is enabled and disabled by the logical AND of TxEN and $\overline{LPBK}$. Thus, TxEN will enable the output driver except during loopback operation when the driver is unconditionally disabled. This driver can interface directly to the 78Ω twisted pair in the Access Unit Interface (AUI) cable.

An example of encoder operation timing is given in Figure 7.

Collision Signal Detector

The Collision Signal is a 10 MHz carrier transmitted by the Transceiver over the Control In pair of the AUI cable. It is transmitted under two distinct circumstances as follows: 1. A collision or other signal-quality error occurs on the trunk coax medium, or 2. Immediately following a successful transmission from the associated DTE, a brief burst of Collision Signal is given to test the signaling mechanism. The DTE detects this signaling and takes appropriate action.

Carrier Sense Function

The medium is continuously monitored for activity by every node. The medium is considered idle if and only if there are no transitions occuring. Detecting the presence or absence of transitions is done in the DTE Physical Layer circuitry. This information is used to enable the receiver circuits and to prevent collisions with other transmitting nodes.

Manchester Decoder

A basic delay-type Manchester decoder is shown in Figure 8. At the input, a 2-input multiplexer selects the signal source, either the receiver input or, for loopback, the transmitter output. The $\overline{LPBK}$ line controls this selection. Refer also to the timing example in Figure 9 for the operating description to follow.

Synchronization during Preamble

Since the Preamble consists of alternating 1s and 0s, there are no bit-boundary transitions during synchronization. All transitions in the Preamble are bit-center transitions. This fact is key to decoders becoming properly synchronized, which would otherwise be more difficult.

Just prior to the Preamble of a new frame, the decoder's input will be idle. In general, its decoding flip-flop will be in an arbitrary state. The first transition of the

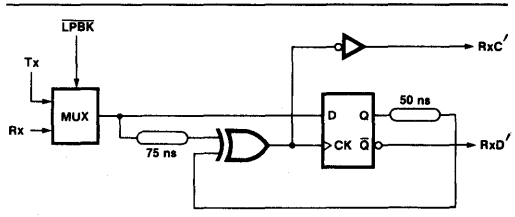


Figure 8. Basic Delay-Type Manchester Encoder

frame is a low-to-high transition encoding the first bit of the Preamble (= 1). Seventy-five nanoseconds after this first bit-center transition occurs, the change propagates through the exclusive-OR gate and complements the clock. Since the flip-flop was in an arbitrary state, the first bit-center transition may or may not clock the flip-flop (only a positive-going transition is active). If Q = 1, the clock will go low and the flop-flop will not change states. If Q = 0, the clock will go high, transferring the level on the D input to the flip-flop. This happens 25 ns before the next bit-center transition, which is the normal Rx sampling time for this decoder (25 ns before bit-center). At that time, Rx will be the complement of the data for the current bit. The second bit of the Preamble is a 0, so in the latter case where initially Q = 0, it will change to 1. Therefore, 75 ns after the first bit-center transition, the flip-flop acquires the right state for the second bit of the frame. $\overline{Q}$ now equals 0 = RxD. This type of decoder acquires RxD synchronization after only one bit time.

Decoding in Operation

Refer to Figures 8 and 9 for this explanation. During frame reception, the decoding flip-flop is clocked 75 ns after each bit-center transition by the bit-center transition itself, propagating through the 75 ns delay line. Seventy-five nanoseconds after the last bit center is 25 nanoseconds before the next. At that time, the Rx line is sampled, transferring the current bit to the $\overline{Q}$ output of the flip-flop. Fifty nanoseconds later, the clock line is complemented, making the exclusive-OR output low, by one of two mutually exclusive events: 1. Either Q changed after the Rx sample because the previous bit and the current bit are opposites, or 2. There was a bit-boundary transition between the previous bit and the current bit because they are like bits. In the first case, the change in Q propagates through the 50 ns delay and then complements the clock. In the second case, the bit-boundary transition propagates through the 75 ns delay and complements the clock. In either case, the exclusive-OR output goes low 25 ns after the bit center time. The clock is then ready for the next Rx sample, 50 ns later.

8023A MCC™ Manchester Code Converter CMOS IC

The 8023A MCC™ provides all the station-resident functions required for the Physical Layer of the Ethernet protocol. It provides coding and decoding of the transmitted signal, carrier sense, collision signaling detection, loopback and crystal clock for transmit timing.

Figure 10 is a block diagram of the 8023A. On the left-hand side of the drawing are the 7 signal lines which connect to the 8003, plus $\overline{\text{LPBK}}$/WDTD, the loop-back/watch dog timer control signal. On the right are the three 78Ω twisted pair connections for the Access Unit Interface, Transmit, Receive and Collision.

The 8023A chip provides all active circuits required for the Physical Layer functions of Ethernet. Only 10 passive components are needed to apply the 8023A as shown in Figure 11.

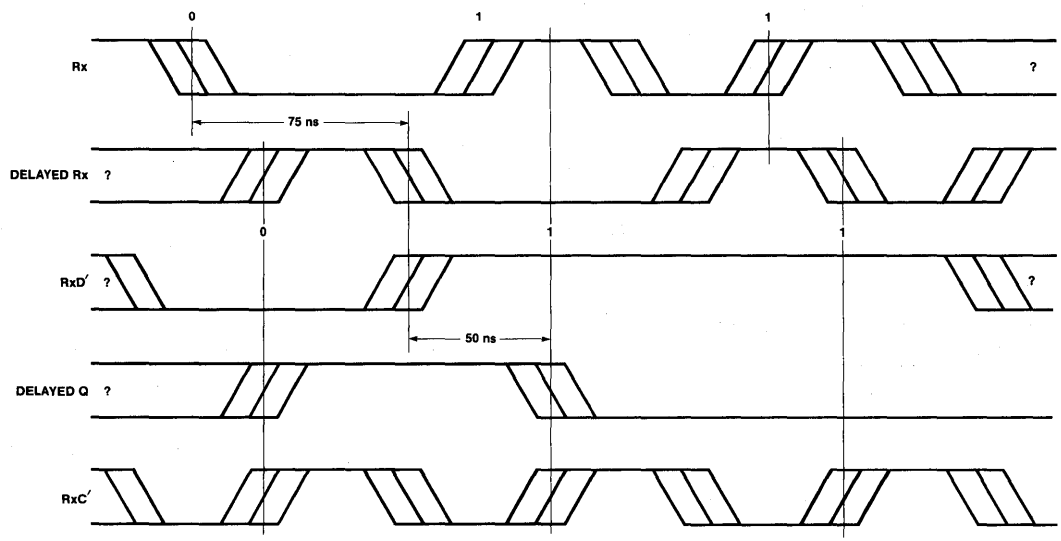


Figure 9. Timing Diagram for Delay-Type Decoder in Figure 8

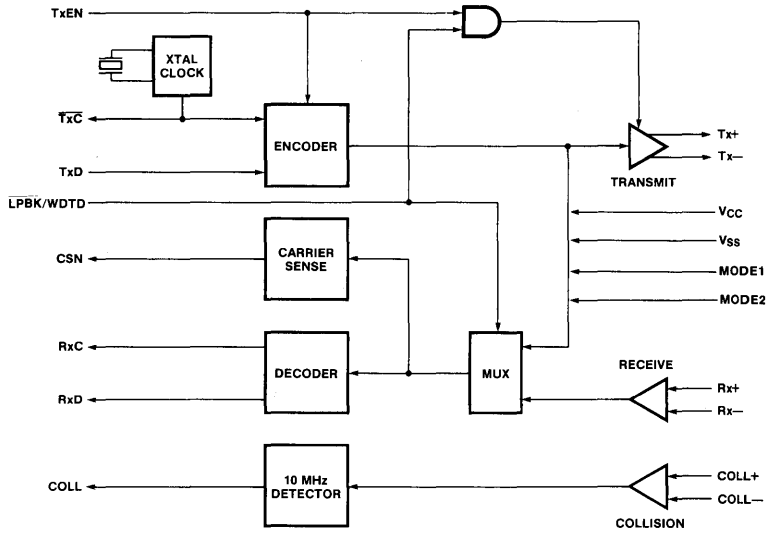


Figure 10. 8023A MCC™ Manchester Code Converter Block Diagram

8023A Manchester Code Converter Features:

- Compatible with IEEE 802.3 CSMA/CD Specification (Ethernet)
- Compatible with SEEQ 8003 EDLC™ and Intel 82586
- Low-power CMOS Technology
- 10 MBPS Data Rate
- 20 MHz crystal oscillator on chip
- Phase-locked Loop decoder for optimum jitter tolerance
- Collision signaling detector on chip
- Loopback capability for diagnostics
- Drives 78Ω transmit twisted pair directly
- No additional active components required
- Performs all DTE-resident Physical Layer protocol functions
- Single +5 V supply
- 0.3 in. 20-pin package

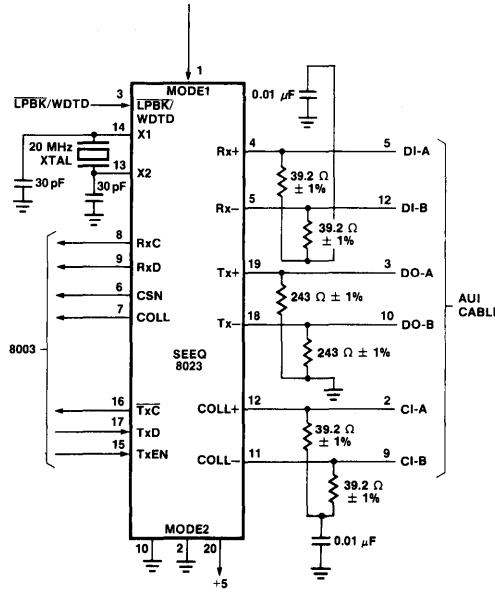


Figure 11. 8023A Application

REL/APP NOTES

Communications Products Application Brief

5A

INTERFACING THE 8003 EDLC™ TO A 16-BIT BUS

by: Gerald Moseley

seeQ
Technology, Incorporated

Interfacing the 8003 EDLC™ to a 16-Bit Bus

Introduction

The SEEQ 8003 Ethernet Data Link Controller (EDLC™) chip together with the SEEQ 8023A Manchester Code Converter (MCC™) chip provide an economical two-chip solution for the Data Link Layer and Physical Layer of the Ethernet protocol. These chips are fully Ethernet compatible and suitable for use in terminals, personal computers, workstations, printers, disk drives and host computers.

The 8003 is a VLSI data link controller chip in a 40-pin package. It replaces approximately 60 MSI and SSI components in a typical Ethernet node configuration. The choice of which one to use is governed by the system interface requirements for the design. The 8003 provides protocol functions like frame formatting, link access control and error control. The part is optimized for Direct Memory Access techniques for frame storage.

The 8023A MCC™ Manchester Code Converter performs the signal encoding and decoding in Manchester Code at 10 million bits per second. It also monitors the channel for "carrier" and "collisions" (two nodes transmit simultaneously). Low-power CMOS technology is used in the 8023A, which is in the 0.3 inch 20-pin package.

Ethernet Node Configuration

A typical Ethernet node is shown in Figure 1. The System Interface on the left connects the host system bus to the network. This interface varies depending on processor and system requirements.

The station-resident hardware, consisting of the System Interface, the 8003 EDLC™ chip and the 8023A MCC™ chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists of 78Ω balanced, shielded twisted-pair connections, DC biased at the station end and transformer-coupled at the Transceiver end.

Besides a passive tap to the Trunk Coax, the transceiver provides signal amplification, preconditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.

Host-Dependent System Interface

There are three basic methods for interfacing the CSMA/CD channel to the system bus. The first one employs First-In, First-Out (FIFO) buffer memory to temporarily hold the transmit and receive frames. On the system-bus side of the FIFOs, data is transferred serially a byte at a time by the processor. The second method uses Direct Memory Access to transfer data directly between the Ethernet Data Link Controller and the system memory. In the third method, Direct Memory Access is also used, this time with a temporary buffer memory intervening between the system memory and the EDLC™ chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. (For more information on DMA-type interfaces, see SEEQ's Application Brief 6).

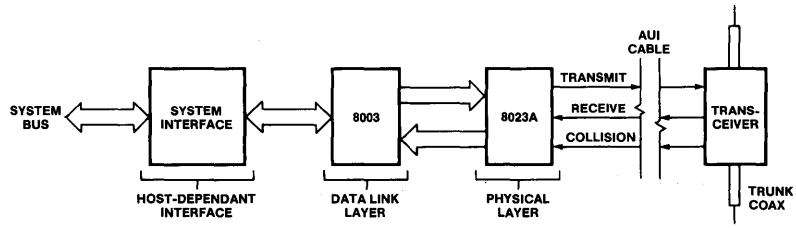


Figure 1. Ethernet Node Configuration

IEEE 802.3 CSMA/CD Standard Protocol for Local Area Networks (Alias Ethernet)

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corporation. Since then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be reliable and efficient in a wide variety of network applications. As a result, it has become the first industry-standard protocol for local area networks, supported internationally by computer manufacturers in the U.S. and Europe.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry standard. After three years of review and refinement, this specification is about to be published by IEEE Press under the title *IEEE 802.3 CSMA/CD Local Area Network Standard Protocol*, ("CSMA/CD" describes the medium access method, **C**arrier **S**ense, **M**ultiple **A**ccess with **C**ollision **D**etection). The IEEE 802.3 document supersedes all previously published Ethernet specifications.

CSMA/CD — Carrier Sense, Multiple Access with Collision Detection

CSMA/CD: This expression describes the medium access method used in Ethernet alias IEEE 802.3 CSMA/CD. **Carrier Sense** means all nodes on the network can detect all signals transmitted on the network from any source. **Multiple Access** means all nodes can have equal access to the network without need for centralized control. A node is permitted to transmit if the network is not already busy. If, however, two or more nodes start to transmit simultaneously, it is called a collision. **Collision Detection** means that all nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes resolve which will retransmit first by differential backoff timing.

Data is transmitted in "packets" or "frames" which begin with a preamble for synchronization and end with a CRC field for error detection. In between, the frame has source and destination addresses, a byte-count field and an information field. Total frame length is 72 to 1526 bytes.

The physical signaling format used in Ethernet is baseband Manchester Code transmitted at a rate of 10 million bits per second. In Manchester Code, each bit is encoded by a transition. A "one" is encoded as a low-to-high transition and a "zero" as a high-to-low. In this way there is a continuous supply of bit-framing information for the receiver, since the transmitted signal is never stationary for more than one bit time.

Interface Techniques for 16-Bit Busses

Ethernet is a byte-oriented protocol. That is to say, the smallest unit of data which can be transmitted is a byte. Hence, the 8003 EDLC™ chip has byte-wide data bus. Whether the System Interface is the FIFO-buffer type or the DMA type, the data transfers to and from the 8003 are byte-wide. This application brief describes some techniques for interfacing this byte-wide communication channel to a 16-bit wide bus.

In designing an Ethernet node, trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance may be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you strike the right balance for your design, several interface techniques will be given in the following sections. They are covered in order of increasing cost/complexity/performance.

In an 8-bit system, the 8003 can be interfaced directly to the data bus as shown in Figure 2. The RxTxD0-7 bus is the bus for transferring frame data. It connects to the internal 16-byte transmit and receive FIFOs. The CdSt0-7 bus is a separate input/output port for control and status. It interfaces to the system bus so that the processor has direct access to all command and status bits. In a 16-bit system, CdSt0-7 would connect either to the upper or lower data byte.

Split-Word 16-Bit Data Interface

Refer to Figure 3 for a circuit diagram of this technique. The split-word method splits the 16-bit word into two halves, using one half for transmit data and the other for receive data. In Figure 3, the upper byte of the system data bus is used for the transmit memory buffer and the lower half for receive. Two 74LS244 tristate buffers isolate the system bus lines from the RxTxD0-7 bus of the 8003. The upper 74LS244 is enabled by $\overline{\text{TxACK}}$ from the DMA Controller. $\overline{\text{TxACK}}$ is the DMA Acknowledge signal for the transmit channel. When enabled, this buffer transfers a byte of data from the upper byte of system memory to the 8003's Transmit FIFO. Similarly, the lower 74LS244 transfers data from the 8003's Receive FIFO to the lower byte of system memory. Configured in this way, the transmit and receive buffers in system memory can occupy the same word-address space.

Full-Word 16-Bit Interface Using Byte-Wide Memory Transfers

Another type of 16-bit interface is one that assembles and disassembles words by transferring the upper byte and the lower byte separately. For example, suppose the convention is chosen that the upper byte is to be the first of the two bytes to be transmitted and the lower byte the second. Then the first byte of a frame and all odd-numbered bytes are always transferred to/from the upper byte of memory, and the second and all even-numbered bytes to/from the lower.

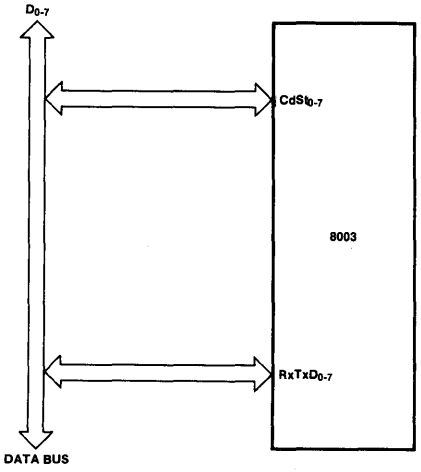


Figure 2. 8-Bit DMA Data Interface

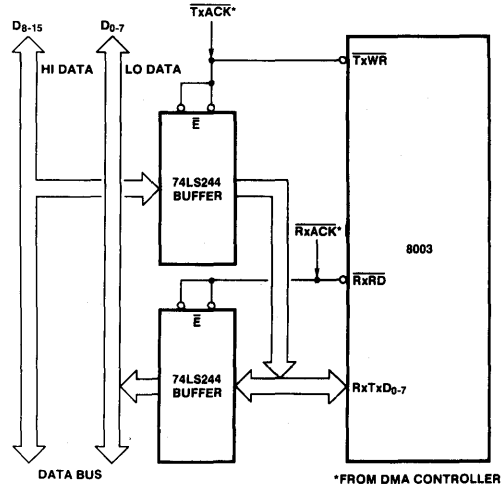


Figure 3. Split-Word 16-Bit DMA Data Interface

REL/APP NOTES

The data interface for this approach is a variation of the one shown in Figure 3. Two tristate buffers are replaced by two bi-directional transceivers. A0, the least-significant bit of the DMA Controller's address is decoded with $\overline{TxACK}$ and $\overline{RxACK}$ to enable the transceivers. The more significant address bits from the DMA Controller, A1 through A_N, are used as the memory address. Upper and lower memory strobes are also controlled by A0. Refer to Table 1 for the truth table.

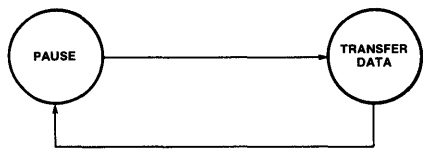
This is the simpler and more economical of two "Full-Word" data interfaces described in this application brief. The other one, shown in Figure 5, assembles and disassembles words in registers, and transfers 16 bits at a time. The advantage of the latter approach is in saving bus bandwidth, since it uses half as many bus cycles to transfer the same amount of data; but there is some additional cost in hardware.

Table 1. A0 Address Decoding for Full-Word 16-Bit Interface Using Byte-wide Memory Transfers

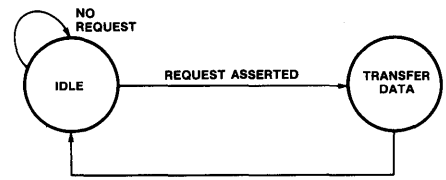
DMA Controller Outputs			Transceiver Enabled Toward (Memory; I/O)		Memory Activity	
A0	$\overline{TxACK}$	$\overline{RxACK}$	Upper	Lower	Upper	Lower
—	1	1	—	—	—	—
0	0	1	I/O	—	Read	—
1	0	1	—	I/O	—	Read
0	1	0	Memory	—	Write	—
1	1	0	—	Memory	—	Write

Note: — indicates not active.

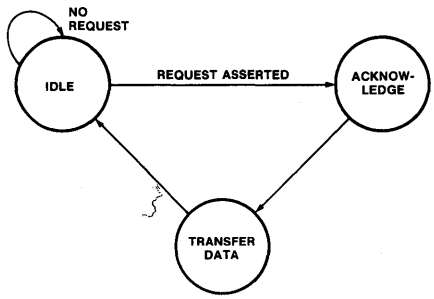
a. No Request, No Wait



b. With Request



c. With Request and Acknowledge



d. With Request, Acknowledge and Bus Arbitration

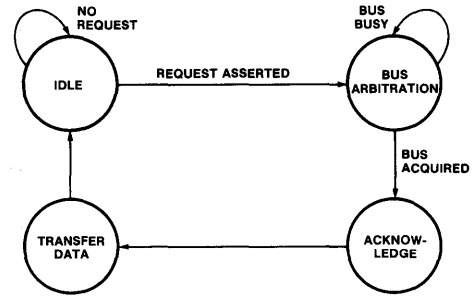


Figure 4. Data Transfer State Diagrams — Four Types

Four types of data transfers are shown in Figure 4. The first, labeled a, is an unconditional transfer sequence such as the type that would be used to refresh a CRT screen. This type has no use in an Ethernet interface since it is not controlled by availability of storage space or stored data.

The diagram in Figure 4 Part b, illustrates a transfer which is initiated "on demand". The transfer takes place only when a "request" is given. An example of this type is data moved by a processor on its own synchronous bus. Physically the request is generated by the processor, manifesting itself as a set of bus-controls, and an address.

Part c illustrates a transfer that is requested by one entity and acknowledged by another. The acknowledge signal is used to notify the requesting entity that the transfer is about to take place. This implementation provides the requesting entity verification that the transfer is taking place. The diagram represents the response of the acknowledging party to the request. The requesting party normally waits for the acknowledgement to occur. This allows the acknowledging party to delay, if necessary, for data access. This mechanism is used on asynchronous busses, like that of the 68000 microprocessor.

The diagram in Part d is that of a transfer with request, acknowledge, and bus arbitration. This implementation is one that is used to transfer information using a DMA controller on the main system bus. There are actually two request/acknowledgement sequences in this transfer, one for bus acquisition and one to transfer information on the acquired bus. Initially a request generated by one of the two "transferees" queues the DMA controller to exit its idle state, and arbitrate for the system bus by generating a "bus request" signal. When the bus master relinquishes the bus, a "bus grant" acknowledgement is received, notifying the DMA controller that it now owns the bus. The DMA controller then performs the transfer, or transfers, by generating a "DMA Acknowledge" to the original requesting device, and generating the appropriate addresses and read/write control signals. Finally the sequence is terminated with control of the bus returning to the main processor through another arbitration.

Diagrams like these can be used to design state machine programs for interfaces like the one in Figure 5, which employs a single-chip state machine.

Helpful Hints for State Machine Designers

As with writing a program, it is desirable to start with a "flow chart" or "state diagram". Examples of state diagrams can be seen in Figure 4. The following are the definitions used in the circle-and-arrow state diagrams used here.

1. Each circle represents a single physical machine state or an unconditional sequence of machine states such that there are no "hidden branches" omitted from the diagram.
2. All conditional branches, and wait states (which may be viewed as conditional branches) are indicated explicitly by arrows. Each arrow is labeled with the condition which determines the branch.

Following these or similar guidelines will help to avoid unforseen anomalies in the operating flow.

Care should be taken in defining the programs for state machines when inputs are asynchronous with respect to the state-register clock. Problems can result when making a conditional branch based on an asynchronous input. Such problems can cause intermittent branching failures with possibilities of perverse consequences. Intermittency makes this type of problem hard to diagnose, so it pays off to avoid them by following these design rules:

1. When a branch is conditional on an asynchronous input bit, assign next-state addresses such that only one state-register flip-flop is affected by the asynchronous bit.
2. For a 3 or more-way conditional branch based on more than one independent asynchronous bit, break it down into independent 2-way branches which conform to rule 1.
3. For inputs which are mutually-dependent combinations of 2 or more bits, it is best to synchronize them with an input register whose clock is synchronized to the state-register clock.

When you have finished the state diagram, you have defined the operating program design. The next step is to choose the hardware that can run your program most efficiently.

After choosing the hardware, you can translate the state diagram, verbatim into program code for the state machine.

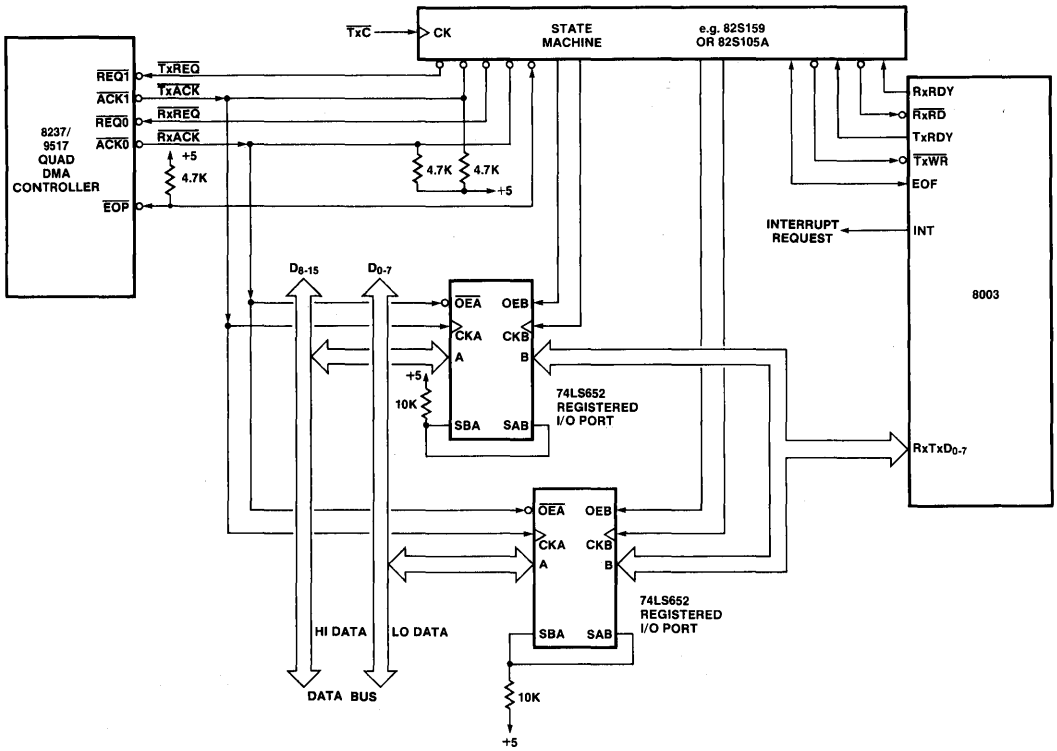


Figure 5. 16-Bit Full-Word DMA Data Interface with 8237/9517 Using Registered I/O Ports

Full-Word 16-Bit Interface Using Registered I/O Ports

This data interface method assembles/disassembles 16-bit words in a pair of 8-bit registered I/O ports. The data transfers between the memory and the I/O ports are 16 bits wide. Transfers between the ports and the 8003 EDLC™ chip are byte-wide.

Registered I/O ports are configured by taking two 8-bit D-type registers with tri-state outputs and connecting them front-to-back. The result is two 8-bit bus connections, each connected to the D inputs of one register and the tri-state outputs of the other. The port has two register clocks and two output-enable controls. An example of such a chip is the 74LS652. The more popular 8-bit registered I/O port chips on the market are in the 0.3 inch 24-pin package.

This interface technique can be used with some variation for any of the three basic types of system interface, i.e. 1. with FIFO frame buffers, 2. with DMA to off-line frame buffers or 3. with DMA to system memory.

A state machine is used to sequence the assembly and disassembly processes. Programmable single-chip state machines and logic blocks, available from multiple sources, are excellent for this type of design. Most are field-programmable one time by burning fuseable links. Normally, the state machine portion of the design can be done in one or two chips.

A circuit example with the 8237/9517 DMA Controller appears in Figure 5. A single-chip state machine, such as the Signetics 82S159 or 82S105A, coordinates the timing for all other components. Two 74LS652s are the two registered I/O ports. The bus lines on the right side of the ports are commoned to make an 8-bit connection to the RxTxD0-7 pins of the 8003. On the left, the 16 port lines connect to the data bus.

Most of the command signals associated with data transfer are sequenced by the state machine. DMA requests ($\overline{REQ0}$ and $\overline{REQ1}$), port output-enable line

OEB, register clock CKB, Transmit FIFO write ($\overline{TxWR}$) and Receive FIFO read ($\overline{RxRD}$) are all under state machine control. Output-enable $\overline{OEA}$ and register clock CKA are controlled by the DMA Acknowledge lines. All the status lines for data transfer connect to the state machine's inputs.

Figures 6 and 7 summarize the state-machine state diagrams for the application in Figure 5. Refer to Figure 6 for the word disassembly diagram. The disassembly process starts with a DMA request issued to the DMA's transmit channel. If the channel is not enabled, no acknowledge will be given and the state machine will remain in the DMA Request State. If the channel is enabled, the DMA Controller will request and acquire the system bus, then issue the DMA Acknowledge. A 16-bit word of data is then read from system memory into the two ports. The next state is Idle 1. Here the state machine waits for a TxRDY ready signal from the 8003 if not already present. When TxRDY is high, the machine goes to the Read First Byte State. This state moves the upper data byte from the upper port into the Transmit FIFO of the 8003. Another idle state occurs where TxRDY is checked for Transmit FIFO readiness. When ready, the lower data byte from the lower port is moved to the Transmit FIFO, ending the cycle.

Refer to Figure 7 for the word assembly state diagram. Word assembly starts in the Idle 1 State. Here, the state machine waits for a signal from the Receive FIFO (RxRDY pin) indicating data is present. When RxRDY is high, the machine advances to load the first byte of the word being assembled to the upper port. As the data is read out of the FIFO, the 8003's EOF line is tested to determine if it is the last byte of the frame. If it is, reading of the second byte is skipped. If not, the Idle 2 State is entered. When ready, the second byte will be loaded into the lower port. Then a DMA Request is given. The DMA Controller will then request the bus, acquire it and give the DMA Acknowledge. Then the state machine passes through the Transfer State, writing the 16-bit word to system memory. That ends the word assembly cycle.

Further References Available from SEEQ

8023A MCC™ Data Sheet

8003 EDLC™ Data Sheet

Application Note 3: Manchester Encoding and Decoding for Local Area Networks

Application Brief 6: DMA Interconnection to the 8003 EDLC™

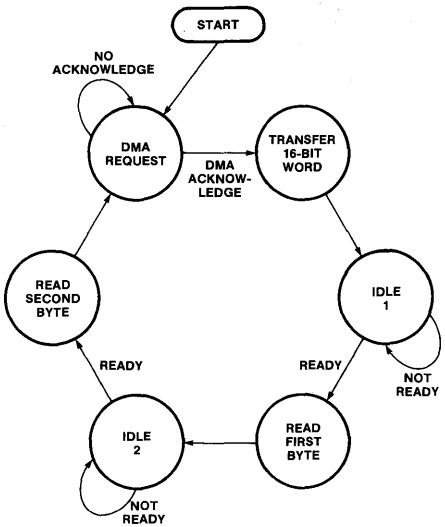


Figure 6. State Diagram for 16-Bit Word Disassembly

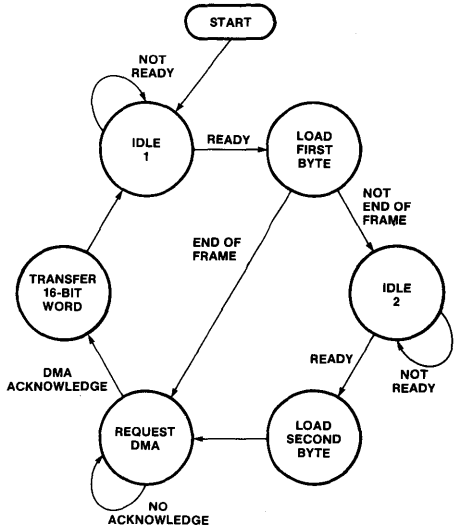
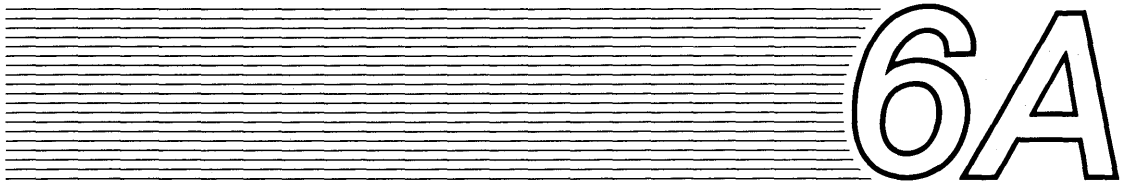


Figure 7. State Diagram for 16-Bit Word Assembly

Communications Products Application Brief



DMA INTERCONNECTION TO THE 8003 EDLC™

seeQ

Technology, Incorporated

DMA Interconnection to the 8003 EDLC™

Introduction

SEEQ's 8003 Ethernet-compatible data link controller provides an economical communication interface for terminals, personal computers, workstations, printers, disk drives and host computers. The 8003 is a 40-pin VLSI device which can replace approximately 60 MSI and SSI components in a typical Ethernet node configuration.

This application brief is about design techniques for an Ethernet node when direct-memory access (DMA) is chosen as the means of transferring data between the system bus and the channel. The methods described herein can be applied to virtually any computer or system bus architecture.

Ethernet local area networks use the **broadcast** network topology. That is to say, a signal transmitted by any station reaches all other nodes on the network. This is in contrast to other types of networks, such as the "star" and the "ring", which use point-to-point interconnections. Transmitted messages in Ethernet are "broadcast" on a segment of 50Ω coaxial cable. Communication nodes are attached to this cable via passive taps, so that new nodes can be added at any time without interrupting the network service. Nodes on the network can be addressed individually, in "multicast" groups, or by the "broadcast mode" to all nodes simultaneously. The broadcast topology is a very efficient mode of communication, yet it is simple and inexpensive to implement.

Ethernet alias IEEE 802.3 CSMA/CD

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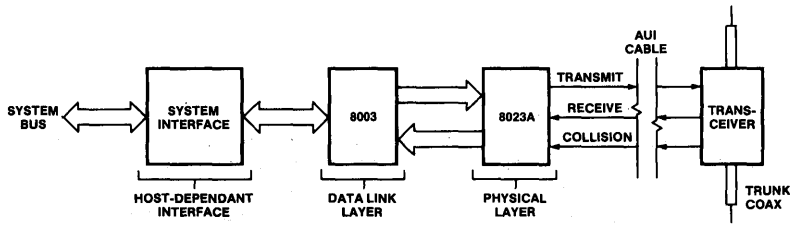


Figure 1. Ethernet Node Configuration

Figure 1 shows a typical CSMA/CD node configuration. The System Interface connects the host system bus to the network. This interface varies depending on processor and system requirements.

Data Link functions are performed by SEEQ's 8003 EDLC™ Ethernet Data Link Controller chip. This device performs medium access control, frame formatting and error detection.

The Physical Layer functions, carrier sense, collision signal detection, data signal encoding and decoding are performed by SEEQ's 8023A MCC™ Manchester Code Converter chip. Manchester Code is the physical signaling format used on the network. Data is transmitted on the network at a rate of 10 million bits per second.

The Data Terminal Equipment hardware, consisting of the System Interface, the 8003 EDLC™ chip and the 8023A MCC™ chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists 78Ω balanced, shielded twisted-pair connections, DC biased at the Data Terminal end and transformer-coupled at the Transceiver end.

Besides the passive tap to the Trunk Coax, the Transceiver provides signal amplification, preconditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.

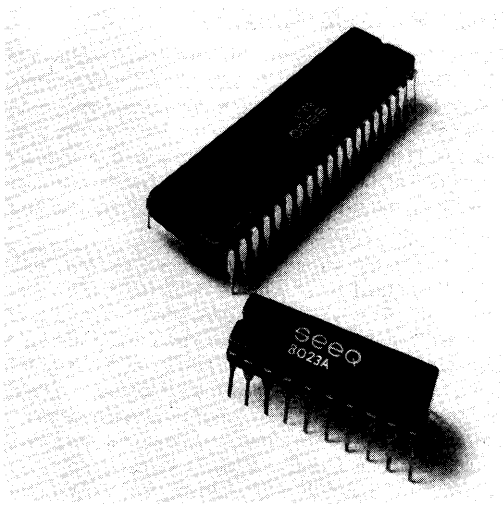


Figure 2. SEEQ's Ethernet Chip Family: 8003 EDLC™ Ethernet Data Link Controller, 8023A MCC™ Manchester Code Converter

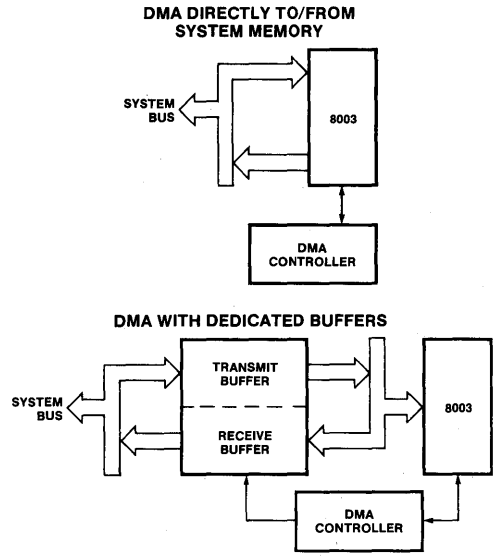


Figure 3. DMA System Interface Techniques

Direct Memory Access System Interface

There are two basic methods for interfacing the CSMA/CD channel to the system bus using DMA, illustrated in Figure 2. The first method uses DMA to transfer data directly between the Ethernet Data Link Controller and the system memory. In the second method, a temporary buffer memory intervenes between the system memory and the EDLC™ chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. These two methods will be the subject of the following sections.

DMA Design Considerations for Ethernet

In designing an Ethernet node, some trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance can be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you evaluate the trade-offs for your design, this section discusses some of the key parameters for you to consider at the outset.

Time is Data

Since the data transmission rate for Ethernet is 10 million bits per second, data transfers during active periods will have to keep up. That means data has to be moved at 1.25 million bytes per second to/from the communication channel. The DMA Controller must meet this speed requirement or frames will be lost. If the system is to support loopback diagnostics, both transmit and receive DMA channels will have to operate simultaneously, together transferring 2.5 million bytes per second. Not just any DMA Controller will do.

Bus Bandwidth

This is only a consideration for systems with heavy communications traffic and/or critical response timing. The transfer of data on the system bus can sometimes use up a considerable percentage of the bus time, at least for short bursts. If this is a problem, the method with dedication buffer memory can be used to offload the system bus (see Figure 2 bottom).

With or Without Dedicated Buffer Memory

If the system architecture does not support 1.25M Bytes/s DMA, the dedicated buffer approach can solve the timing problem. If the system architecture does support high-speed DMA, then bus bandwidth is the key factor which influences this decision. In this case it is clearly a cost-performance issue. The dedicated buffer can relieve system bus traffic, but it takes more hardware to implement.

Cycle-steal or Burst Mode DMA

Refer to Figures 3 and 4. In the Cycle-steal DMA Mode, the DMA Controller "steals" a bus cycle to transfer one and only one byte or word of data. In the Burst DMA Mode, each time the DMA Controller acquires the bus, it can transfer several bytes or all the data to fill or empty a buffer. Either of these two modes can work for Ethernet in principle if the transfer speed is adequate. The Burst Mode is usually preferred by reason of timing efficiency. In Burst Mode, bus arbitration and change-over delays are kept to a minimum. Also, Burst Mode allows the DMA Controller to fill or empty a buffer in one DMA cycle.

On Demand

Transfers between memory and the communication circuitry must be done *on demand*. Some DMA Controller chips will only transfer blocks of data in predetermined lengths. This will not work since the processor and DMA Controller cannot know in advance how many bytes of data can be transferred at a given time.

Maximum Bus Grant Latency

The time it takes to get the bus after a request is made is called bus grant latency. If the DMA method without buffer memory is used, each time a DMA transfer to/from the 8003 EDLC™ chip begins, the DMA Controller must arbitrate for and acquire the system bus. If the latency is too long, the transmitter may underflow or the receiver overflow. The 8003 has transmit and receive FIFOs which are 16 bytes deep, so it must transfer data at least once every 12.8 microseconds when active (16 x 800 nanoseconds). Maximum bus grant latency should be deterministic and always less than that required to prevent underflow and overflow.

8003/DMA Node Hardware

The 8003 has an 8-bit bi-directional data bus ($RxTxD_{0-7}$) for data transfers to and from its internal FIFOs. In Figure 6, the node hardware is configured to transfer data directly to/from system memory over this bus. (This is the technique referred to previously in Figure 3 at the top.) A two-channel DMA Controller is used, providing one channel for transmit data and one for receive data.

A transfer to the transmitter of the 8003 begins with a DMA Request given by the 8003 (its TxRDY pin goes high). The DMA Controller then issues a Bus Request to the processor. After completing the current cycle, the processor halts and gives a bus grant to the DMA Controller, which then transfers the data by issuing a DMA Acknowledge and all necessary address and control signals. Additional transfers would take place if Burst Mode is used until the Transmit FIFO is full, indicated by the TxRDY pin going low. Then the bus is released to the processor and the DMA cycle is over.

Data transfer from the Receive FIFO happens in the same way but with data flowing in the opposite direction. It starts with a DMA Request from the 8003 (its RxRDY pin goes high). If Burst Mode is used, the DMA will continue to transfer until the Receive FIFO is empty, indicated by a low on the RxRDY pin.

The Data Interface for a DMA node with buffer memory appears in Figure 6. In this case, a 4-channel DMA Controller is used. Two channels are needed as before to transfer data between the 8003 and memory. These two channels operate "off-line" and do not require bus arbitration. The other two transfer data between the buffer memory and the system bus. They do require the usual bus arbitration.

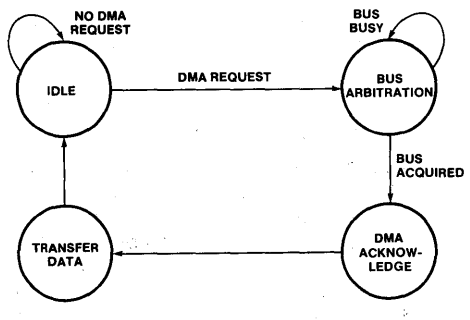


Figure 4. DMA Cycle-steal Mode State Diagram

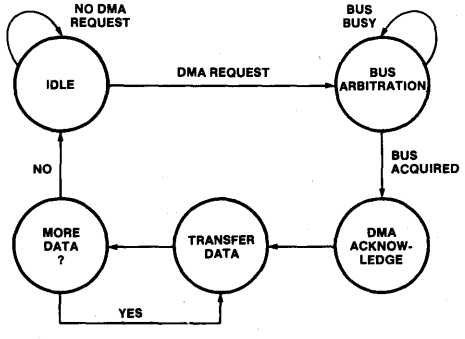


Figure 5. DMA Burst Mode State Diagram

For this design, the $RxTxD_{0-7}$ Receive/Transmit Data Bus of the 8003 connects to a separate bus which is isolated from the system bus by a transceiver. This bus gives the 8003 immediate access to the buffer memory without the need for arbitration.

The two channels for memory-to-memory transfer use the usual bus arbitration method to access the system bus. For these two channels, data being transferred passes through the transceiver shown in the top center of the figure. The tri-state buffer appearing at the bottom center passes the address from the DMA Controller to the System Memory during the transfer. The tri-state buffer and transceiver are enabled by the DMA Controller at the appropriate time in its cycle.

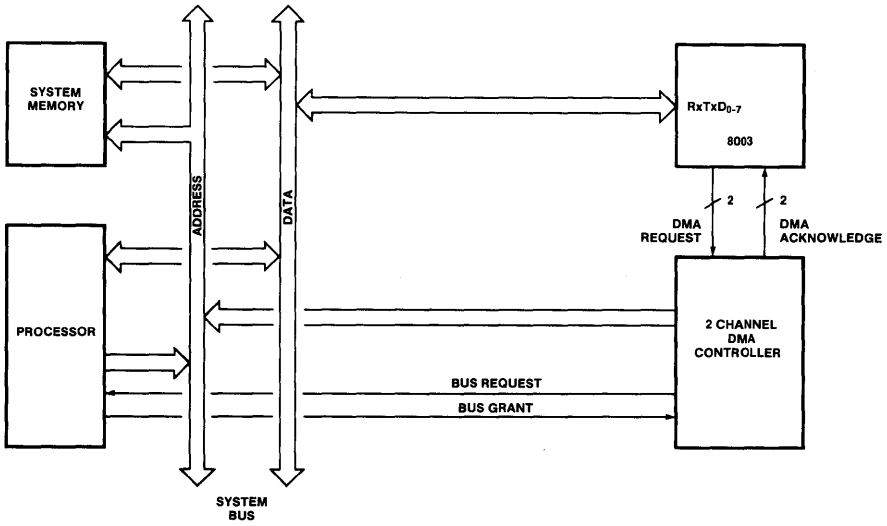


Figure 6. Data Interface for DMA Directly to/from System Memory

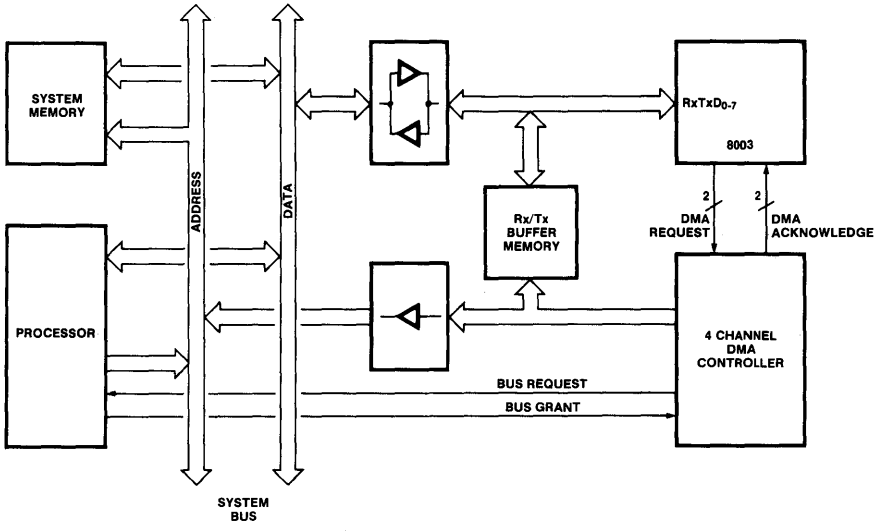


Figure 7. Data Interface for DMA with Buffer Memory

Command Status Interface

The Command/Status Interface for the 8003 is shown in Figure 8. The 8003 has a separate bi-directional 8-bit bus for accessing its internal command and status registers. This bus is labeled "CdSt0-7" in the figure. Three address lines, A_0, A_1 and A_2 select the register to be accessed. Refer to the 8003 data sheet for a full description of these registers and their addresses.

To write to a command register, the system bus decoder must provide a low level to both Chip Select ($\overline{CS}$) and Write ($\overline{WR}$) while data and the three address bits are valid. To read a status register, a low is applied to both Chip Select and Read ($\overline{RD}$) while the address is valid.

The Interrupt Request line (INT) goes high to request an interrupt when specific conditions occur. This line drives the interrupt input of the processor, either directly or through an interrupt-priority logic block. Conditions for generating an interrupt are selected by setting bits in the command registers. For details, see the data sheet. The Interrupt Request line is cleared automatically when the processor reads the status registers.

8237/9517 DMA Controller Interface

The interconnection of popular the 8237/9517 DMA Controller to the 8003 is illustrated in Figure 8. The TxRDY control line from the 8003, which indicates that the Transmit FIFO is not full, is used to generate the DMA request for Channel 1, the transmit channel. Similarly, RxRDY which indicates that the Receive FIFO is not empty generates a request for Channel 0, the receive channel. After a request for Channel 1, the DMA Controller will issue simultaneously a DMA acknowledge (on DACK1) and an input/output write ($\overline{IOW}$), which are used to assert the $\overline{TxWR}$ write line on the 8003. After a request for Channel 0, the DMA Controller will issue simultaneously a DMA acknowledge on DACK0 and an input/output read ($\overline{IOR}$). These are used to assert the $\overline{RxRD}$ read line on the 8003.

The $\overline{EOP}$ control line on the 8237/9517 indicates the "end of process" which has the same meaning as the 8003's "end of frame" line (EOF). These lines are used to terminate the transfer process after the last byte of a frame has been transferred. Both the $\overline{EOP}$ and EOF lines are bi-directional, the direction depending on the direction of data transfer. They are interfaced together by an inverting transceiver, whose direction of operation is controlled by the DACK0 and DACK1 acknowledge lines.

The active polarities of the DREQ and DACK lines on the 8237/9517 are programmable by setting internal control bits. For the interface shown, they should be programmed active high.

68440/68450 DMA Controller Interface

The 8003 interface to the 68440/68450 DMA Controllers from the popular 68000 microcomputer family is shown in Figure 9. The request lines on the 68440/68450 can be programmed to be level or edge sensitive. In this example, level sensitivity is selected by setting internal control bits. As in the previous example of Figure 9, the TxRDY output of the 8003 drives the request line for Channel 1 and the RxRDY requests Channel 0.

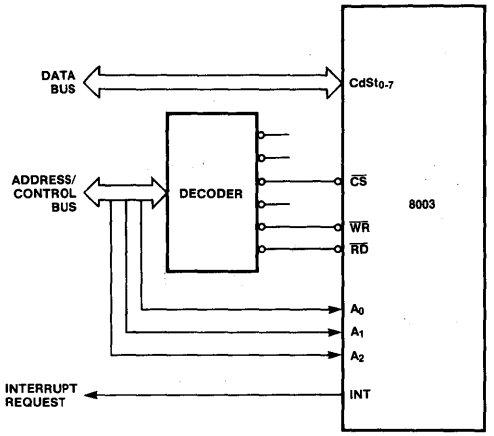


Figure 8. Control/Status Interface

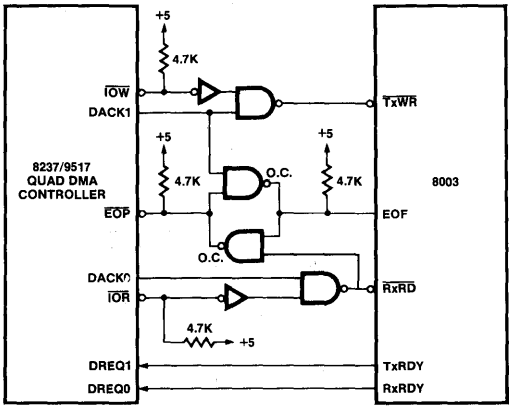


Figure 9. 8003 Interface to 8237/9517 DMA Controller

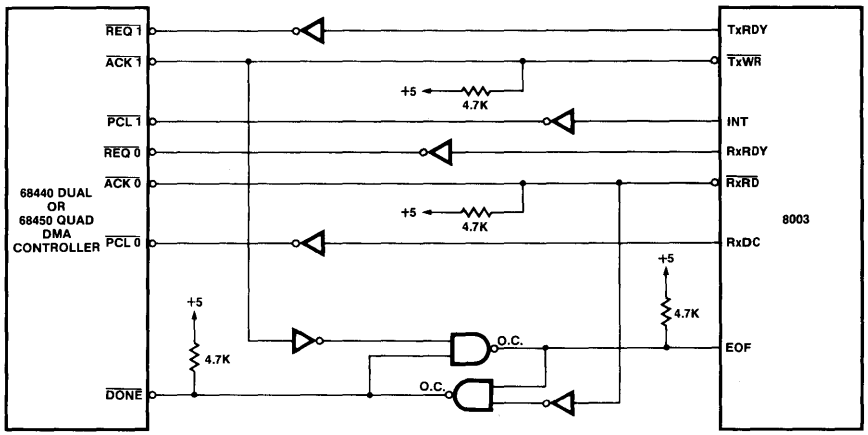


Figure 10. 8003 Interface to 68440/68450 DMA Controller

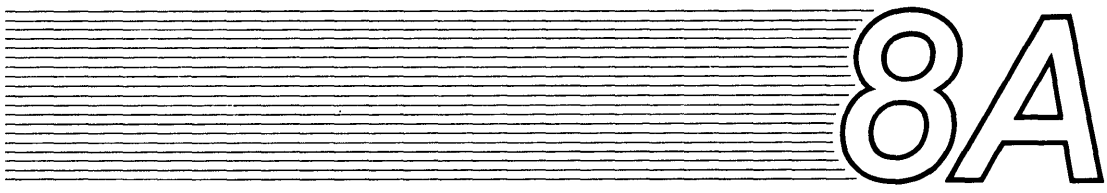
The acknowledge lines on the 68440/68450 can be connected directly to the TxWR and RxRD inputs of the 8003 as shown in Figure 9.

On the 68440/68450, the EOF function pin is called "done". The $\overline{\text{DONE}}$ pin interfaces to the 8003's EOF pin through an inverting bi-directional transceiver shown at bottom center of the drawing. As in the previous example, this signal terminates the channel activity at the end of the frame.

The $\overline{\text{PCL0}}$ and $\overline{\text{PCL1}}$ lines on the DMA Controller are put to good use in this application. They are programmable inputs associated with Channel 0 and Channel 1 respectively. By setting internal control bits, the $\overline{\text{PCL1}}$ line can be programmed to activate the on-chip interrupt request logic. The interrupt request output of the 8003 (INT) is used to drive it. A low on $\overline{\text{PCL1}}$ will interrupt the processor to read the status registers of the 8003. This is used for a variety of conditions which can occur on the network. For example, if 16 consecutive collisions occur, network diagnostics and/or an alarm are ordered by interrupting the processor. The status code which has generated the interrupt is read by the processor from the 8003's internal status registers.

The $\overline{\text{PCL0}}$ input can be programmed to be an input for restarting Channel 0, the receive channel. In this mode, a low on $\overline{\text{PCL0}}$ will re-initialize the channel automatically. It is driven by the 8003's RxDC receive discard line. RxDC goes high following reception of a bad frame or frame fragment. This will in effect discard the bad data and restart the receive channel, without the need for processor intervention in setting up the channel.

Memory Products Application Note



E^2ROM INTERFACING

seeQ

Technology, Incorporated

Contents

E²ROM Interfacing

Introduction

The continuing rapid evolution in semiconductor E²ROM memory device technology offers the system designer an ever-increasing choice of function and capability. With these increasing choices for E²ROM devices, however, comes the problem of standardization (or lack thereof) concerning such specifications as endurance, timing characteristics, interface requirements, ad infinitum. Today, there are two popular types of commercially available E²ROM devices.

Both of these types of devices have the JEDEC-approved pinout shown in Figure 1, including the multi-functional pin 1, but differ in the timing of the control interface. The first E²ROM type, the latched type device, such as SEEQ's 52B33 latches the addresses, control, and data inputs on the falling edge of WRITE ENABLE ($\overline{WE}$). For this type device, the $\overline{WE}$ input must remain active low for the duration of the write cycle. The second type of E²ROM, the timer-type device, latches addresses, data, and control signals on the rising edge of WRITE ENABLE or the rising edge of CHIP ENABLE ($\overline{CE}$). For the timer device, such as SEEQ's 2864 the $\overline{WE}$ input need not be held low for the entire write cycle. The primary difference between the latched and timer devices is the control timing required to interface to the microprocessor. Each of these types of devices has advantages depending on system performance and configuration requirements.

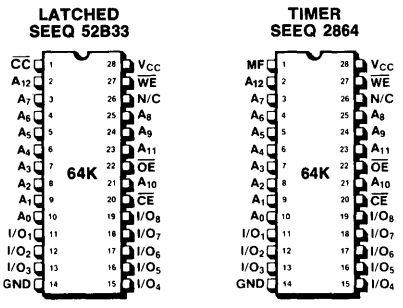


Figure 1. JEDEC Pinout — 64K E²ROMs

When the designer attempts to use the advantages of both in the same system, a problem is encountered.

One of the most frustrating problems facing a system designer is the design of an E²ROM/microprocessor interface that will allow compatible operation of timer and latched type E²ROM devices in the microprocessor-based system. The purpose of this application note is to give examples of cost-effective designs of E²ROM/microprocessor interfaces, which allow the use of both timer and latched E²ROM devices in the system with no changes required to either the controlling software or the hardware. With the interfaces shown in this application note, it is possible to operate with BOTH latched and timer devices simultaneously in the system if the device access times are compatible.

The microprocessor interfaces described in this application note are for the 8085, 8086, 8088, Z80, and 71840. Software examples are provided for the Z80 and 71840 processors. By extension, the Z80 code is easily transportable to 808X processors. In most cases, the hardware required for compatibility consists of only two additional standard (14-pin) TTL packages.

It is hoped that these example interfaces will assist the system designer in implementing E²ROMs in his system. By no means are these special cases presented to limit the system designer, but to provide a starting point for his design. The interface circuits presented are for the family of E²ROM devices (16K, 32K, and 64K). Other extensions of the ideas presented may permit lower power, lower cost, or optimization of other parameters deemed more important.

The body of this application note consists of two sections. First, the Basic Operation section gives the theory of operation of all of the interfaces and should be read to familiarize oneself with those factors common to all of the microprocessor interfaces. Second, the Microprocessor Interface section details the design of the TTL interface required for the given microprocessor.

Basic Operation

Each of the E²ROM microprocessor interfaces described in the next section integrates hardware and software to achieve compatibility between latched and timer E²ROM devices. Naturally, both hardware and software are processor-dependent. However, the write cycle used is basically the same for all the examples shown.

For compatibility between the latched and timer E²ROM devices, the interface provides control waveforms that have timing compatible with both, since the major difference between latched and timer E²ROM devices is the timing of the write control interface to the microprocessor (see Introduction). The basic waveforms for latched and timer E²ROMs are shown in Figures 2a and 2b, respectively. The latched type E²ROM device acquires data on the leading edge of $\overline{\text{WRITE ENABLE}}$

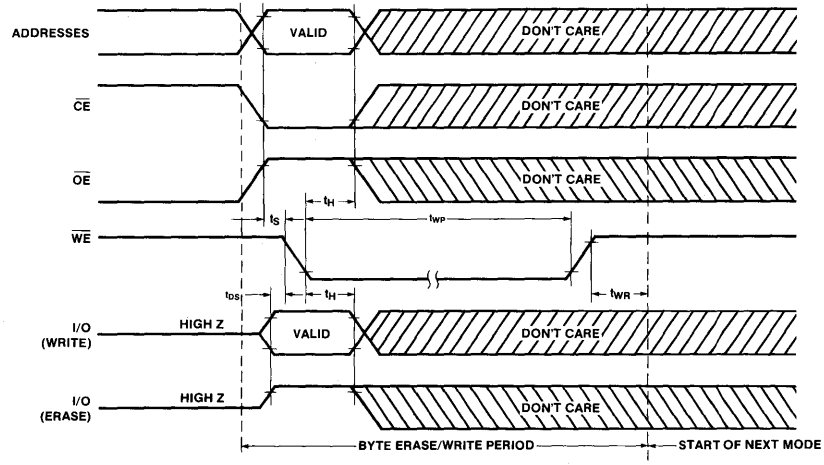


Figure 2a. Latched E²ROM Write Cycle

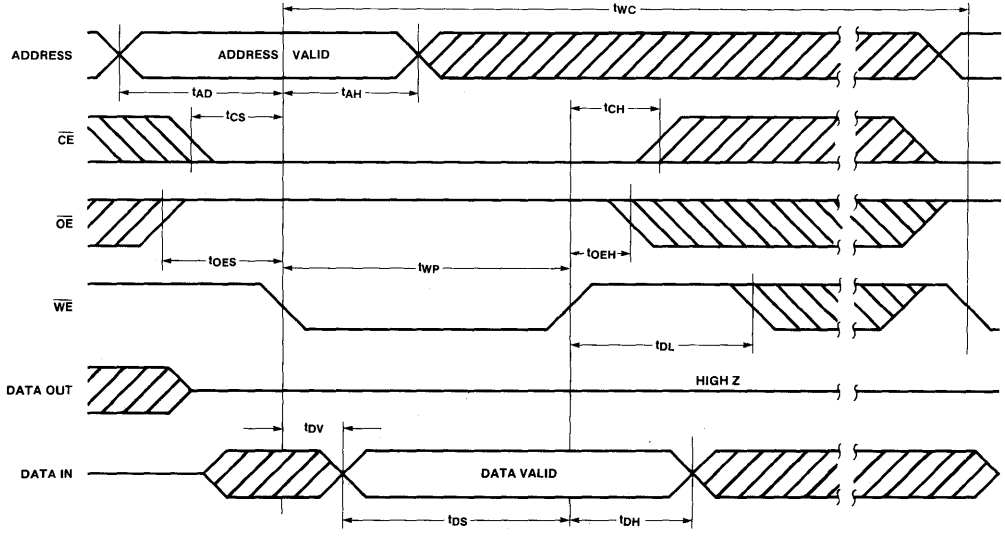


Figure 2b. Timer E²ROM Write Cycle

($\overline{WE}$). The timer type device acquires data on either the trailing edge of $\overline{WE}$ or the trailing edge of $\overline{CHIP\ ENABLE}$ ($\overline{CE}$). Interface compatibility is achieved between the latched and timer devices by strobing the data, control, and addresses on the leading edge of the Write Enable pulse for the latched device and then by strobing the data on the trailing edge of $\overline{CHIP\ ENABLE}$ for the timer device (see Figure 3). By using this technique, the hardware interface is greatly simplified.

The software part of an E^2ROM interface is very simple, but very important. A read operation for both latched and timer E^2ROM devices is accomplished by a straightforward issuance of a microprocessor Read command at a particular address (see Figure 4). A write operation, however, involves a more complex process.

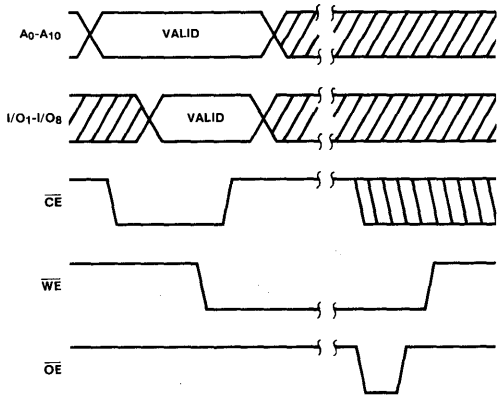
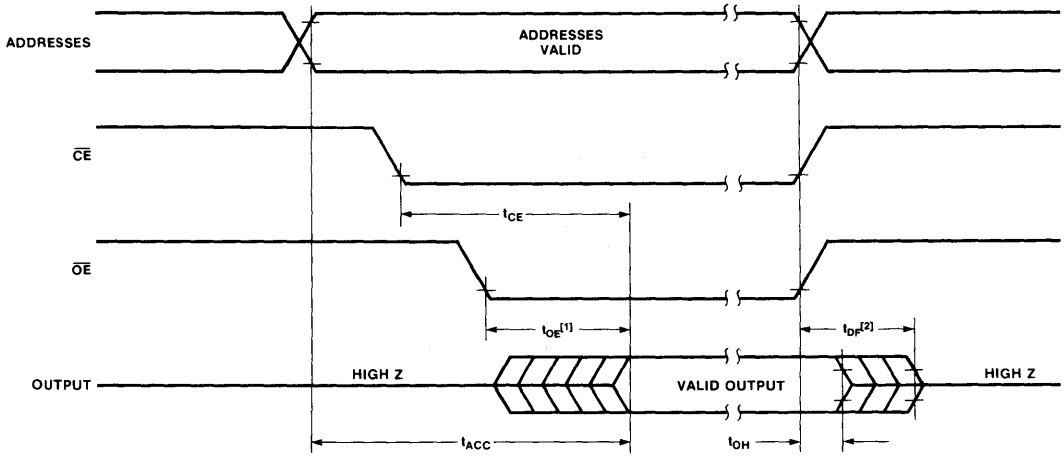


Figure 3. Latched/Timer Compatible E^2ROM Write Cycle

The flow chart for writing to the E^2ROM is the same for all microprocessors and is shown in Figure 5. After a Write command is issued, time is required to allow proper writing to the storage cell of the E^2ROM device. A Read command is then issued to terminate the write operation. Note that this Read command is not to be used to actually read the E^2ROM device, but is inserted to reset the logic circuits used to drive the $\overline{WE}$ input of the E^2ROM device.

Between initiation and termination of a write cycle, the interface uses some timing mechanism to assure proper write conditions to the E^2ROM and to know when the E^2ROM is available for another read/write cycle. The duration of the timeout (t_{WP}) depends upon the type of E^2ROM used. For all types, t_{WP} should fall between the minimum and maximum specifications of all E^2ROMs for which the application is designed. The latched type of device requires less write time than does the timer type device.

The implementation of this timing can be accomplished in either hardware or software. In hardware timing, a timer can interrupt the processor at regular intervals, or at the end of the desired write time (t_{WP}). In software timing, the processor simply counts down, waiting for the desired t_{WP}. For ease of general implementation, the given examples utilize software timing (see Figure 5). The tradeoffs, however, between software and hardware timing comprise an involved topic. The system designer must make this decision, considering such factors as processor throughput, board space, and expense.



Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.

Figure 4. E^2ROM Read Cycle

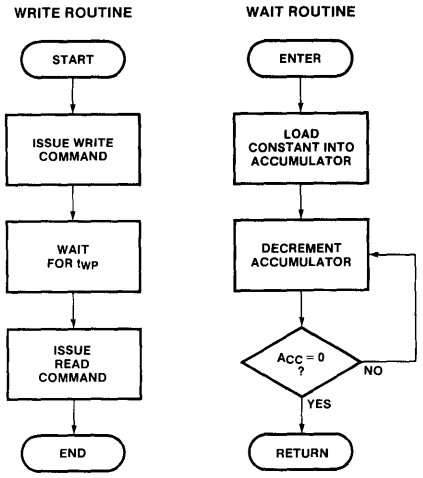


Figure 5. Software Flowchart — E²ROM Write Cycle

After the cycle described by Figure 5 is complete, the E²ROM device is available to be accessed for another Read or Write command. Often, another read will be performed in order to verify the written data. With the solution proposed, this subsequent read cycle will have normal timing, and all required write recovery parameters will be satisfied.

The general description provided above applies to most of the processors shown in the specific examples below. For more detailed information, the reader should refer to the schematic, waveforms, and software that apply to a specific processor.

Microprocessor Interfaces

8085 Interface

The schematic for the 8085 interface to a timer or latched E²ROM device is shown in Figure 6. This interface consists of one each of a 74LS02 and 74LS74 type package and allows the system designer to use the $\overline{WR}$ signal from the 8085 to initiate the write cycle to the E²ROM device. The design permits use of either a timer

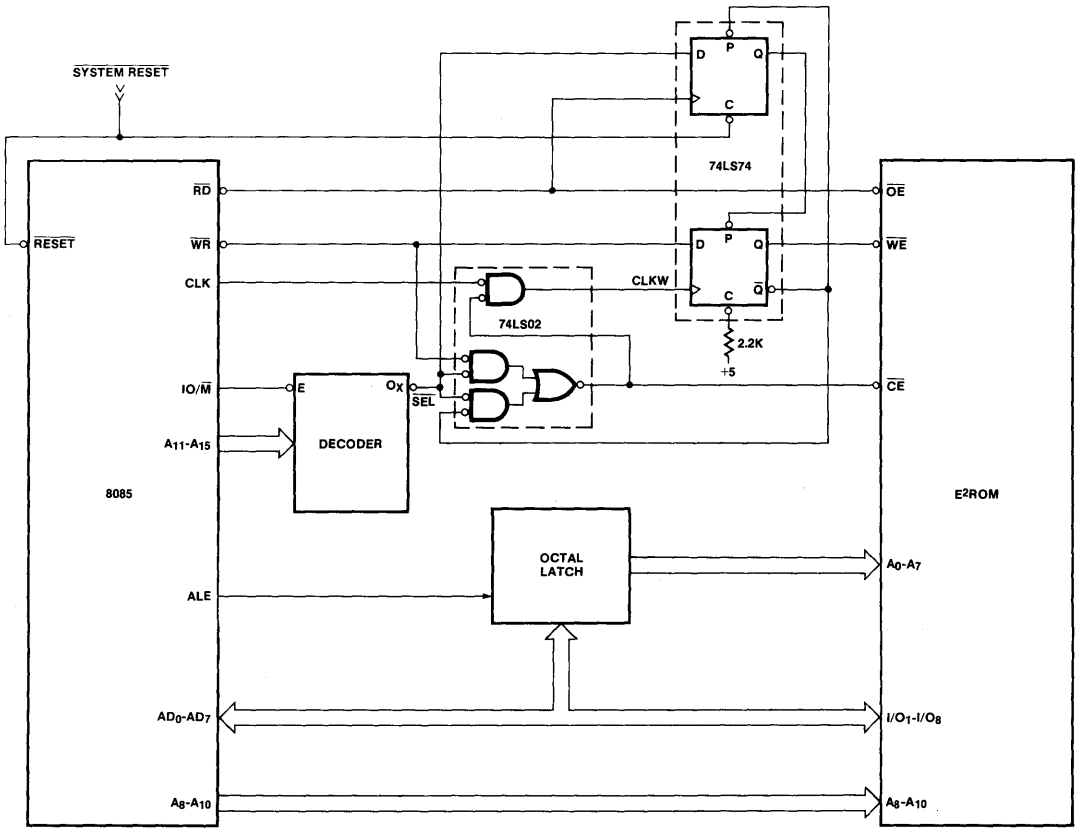


Figure 6. 8085/E²ROM Interface

REL/APP NOTES

OR a latched E^2ROM device with no change required to the controlling software or hardware. The following discussion of the operation of the 8085 interface relies on the 8085 timing diagram summary for read and write cycles shown in Figures 7a and 7b respectively.

Initiating a write cycle requires the software control routine as charted in Figure 5. Should the reader desire a specific example, the Z80 code (see Figure 12) is transportable to the 8085.

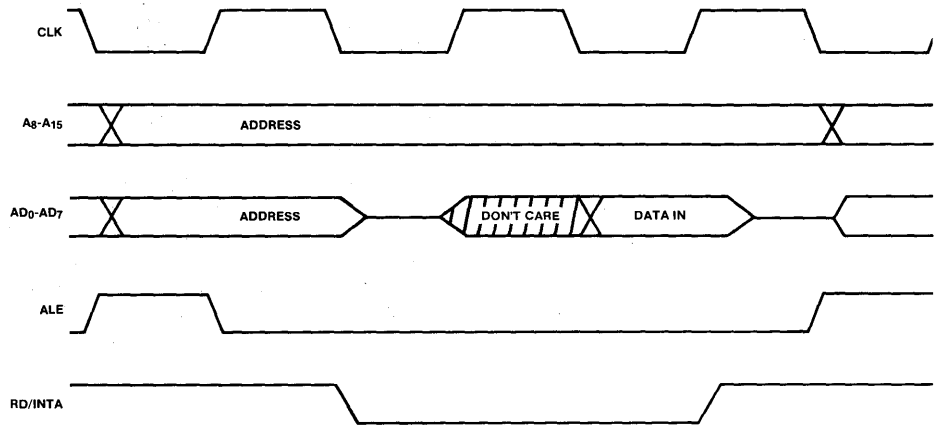


Figure 7a. 8085 Read Timing Summary

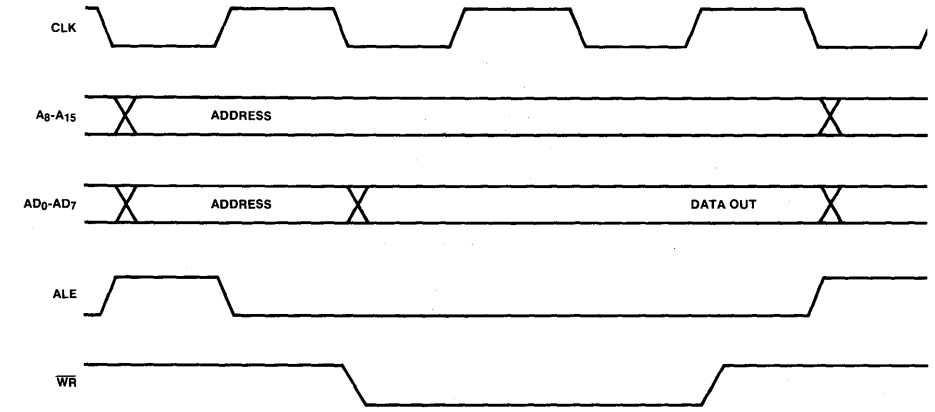
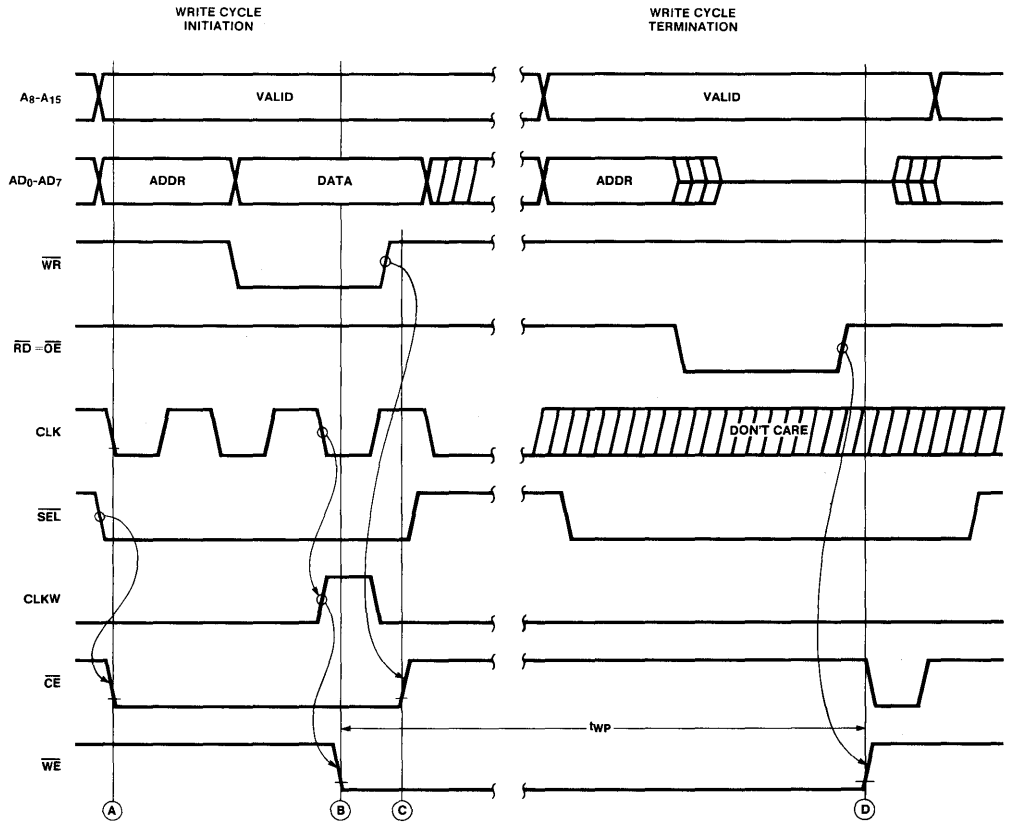


Figure 7b. 8085 Write Timing Summary

The basic write operation waveforms for this interface are shown in Figure 8. The write cycle begins with the addresses becoming valid and being decoded to drive $\overline{\text{SELECT}}$ active low, in order to drive the $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) active low at the E^2ROM device pin (selecting the desired device) (see (A) in Figure 6). An active low level on $\overline{\text{WR}}$ from the 8085 (indicating a write cycle initiation) allows the $\overline{\text{WRITE ENABLE}}$ latch of the interface to be clocked by the next falling edge of the 8085 clock output (CLK) (see (B)). Addresses, data, and control inputs to the latched type E^2ROM are latched in at the falling edge of $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$) — shown as (B) in Figure 8. For the timer type E^2ROM device, however, data is latched on the rising edge of $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) — shown as (C) in Figure 8. Note that $\overline{\text{CE}}$ is held active low for a relatively short period of time, while $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$) is held low for the entire write time of the E^2ROM device. In this manner, the waveforms shown in Figure 3 are produced, providing signals compatible with both the latched and timer type devices.

To end the write cycle, the 8085 issues a Read command to the E^2ROM device. This read cycle enables the Write Reset latch which in turn presets the $\overline{\text{WRITE ENABLE}}$ latch (shown in Figure 6). The preset to the $\overline{\text{WE}}$ latch brings $\overline{\text{WE}}$ to V_{IH} (see (D) in Figure 8). As indicated in Figure 8, this read cycle does not produce valid data from the E^2ROM. This read cycle is used merely to terminate the write cycle.

The latched and timer devices respond identically in a read cycle. The 8085 read cycle, shown in Figure 7a, produces the read cycle waveforms shown in Figure 4.



*A_0-A_7: ADDRESS SIGNALS MULTIPLEXED WITH DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 8. Timing Diagram — 8085/E^2ROM Interface

Z80 Interface

A sample interface is shown for a Z80 processor (see Figure 9). The timing diagram for write cycle waveforms at this interface is also shown (see Figure 10). The basic circuit is very similar to the 8085 interface, with the differences based on the fact that the Z80 has data valid at both edges of $\overline{WR}$ (see Figure 11). This simplified timing allows a more simple interface. The CLK output from the processor is not necessary, and $\overline{WR}$ alone provides timing for the write cycle initiation.

The operation of the circuit is otherwise very similar to the 8085 interface. After addresses are brought valid on the address bus, they are decoded to drive $\overline{SEL}$ active low, which drives $\overline{CE}$ active low at the E^2ROM device pin (see Figure 9, and (A) in Figure 10). At the falling edge of $\overline{WR}$ (when this device is selected), the $\overline{WE}$ latch is clocked, bringing $\overline{WE}$ active low (see (B) in Figure 10). At this time, the latched type device latches address, data, and control signals, while the timer type device latches address and control signals. At the falling edge of $\overline{WR}$, the gating circuitry brings $\overline{CE}$ high, latching data for the timer type part (see (C) in Figure 10). Within a normal processor cycle, a write cycle has been initiated with timing in accordance with the general approach of Figure 3. Even with additional buffers which may be common in a bus oriented system, this interface can be used with a Z80, Z80A, or Z80B operating with no wait states at up to 6 MHz clock frequency. The individual system designer, of course, must check his own application to ensure satisfaction of applicable setup and hold requirements in the specific system for which the application is intended.

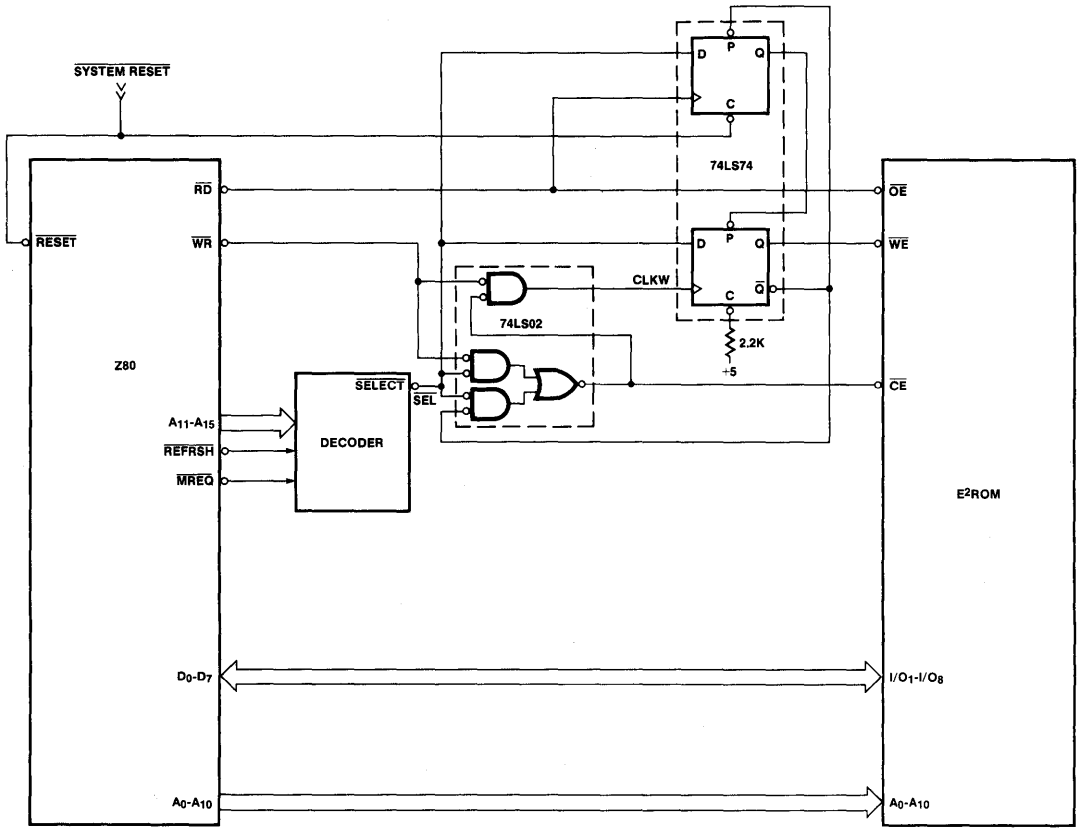


Figure 9. Z80/E^2ROM Interface

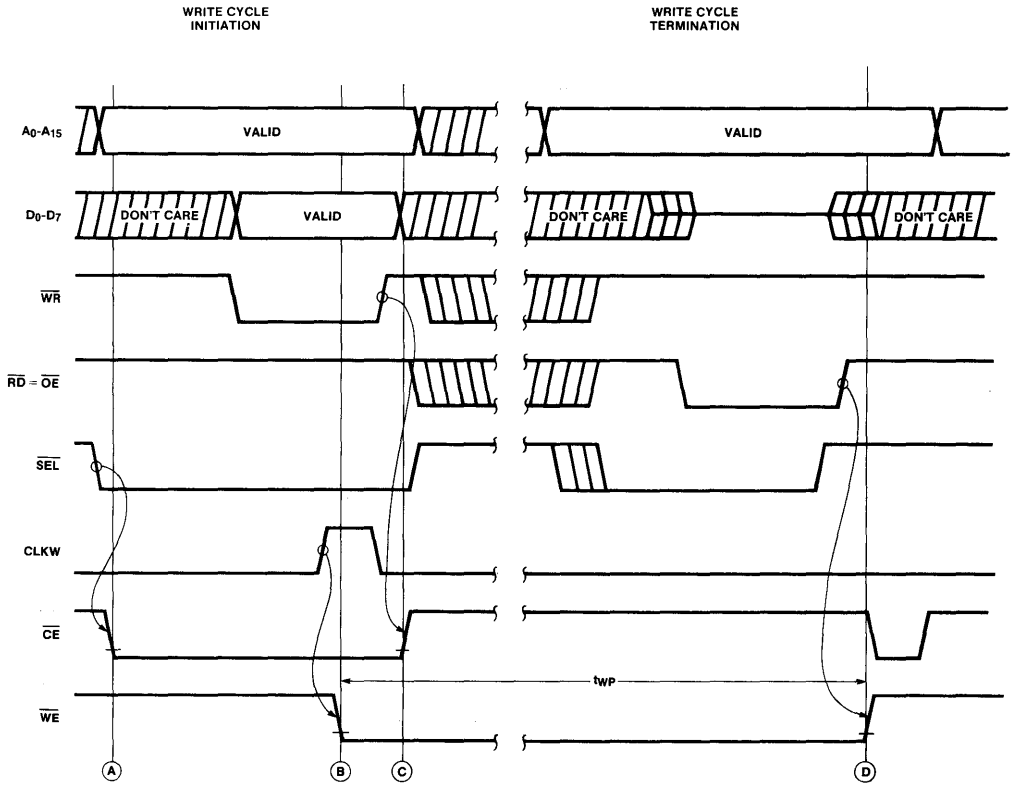


Figure 10. Timing Diagram — E²ROM Interface (Write Cycle)

The termination of a write cycle is very straightforward. As shown in the Basic Operation section (see Figure 5), a read operation to the E²ROM terminates the write cycle, but does not provide valid data. For the interface operation in write cycle termination, the reader should refer to Figure 10. The addresses are brought valid on the address bus, and are decoded to drive $\overline{SEL}$ active low (see (A) in Figure 10). The gating circuitry, however, inhibits $\overline{CE}$, and $\overline{CE}$ remains at V_{IH}. At the rising edge of $\overline{RD}$, the flip-flop receives a positive edge trigger, and clocks in the $\overline{SEL}$ signal to preset the $\overline{WE}$ latch. At this point, $\overline{WE}$ is brought high (see (D) in Figure 10), terminating the write cycle. For the remainder of this processor bus cycle, $\overline{CE}$ becomes valid for a short while. However, $\overline{RD}$ is no longer active low, and no valid data is read in this bus cycle. There is no problem with t_{WR} since the write recovery time occurs during the remaining part of this bus cycle.

Frequently, one may wish to read again from the device, in order to verify data written. This read will be a normal read, following the general waveforms of Figure 4. In a read operation, the interface drives $\overline{CE}$ active low to select the device, and $\overline{RD}$ enables the output from the E²ROM device.

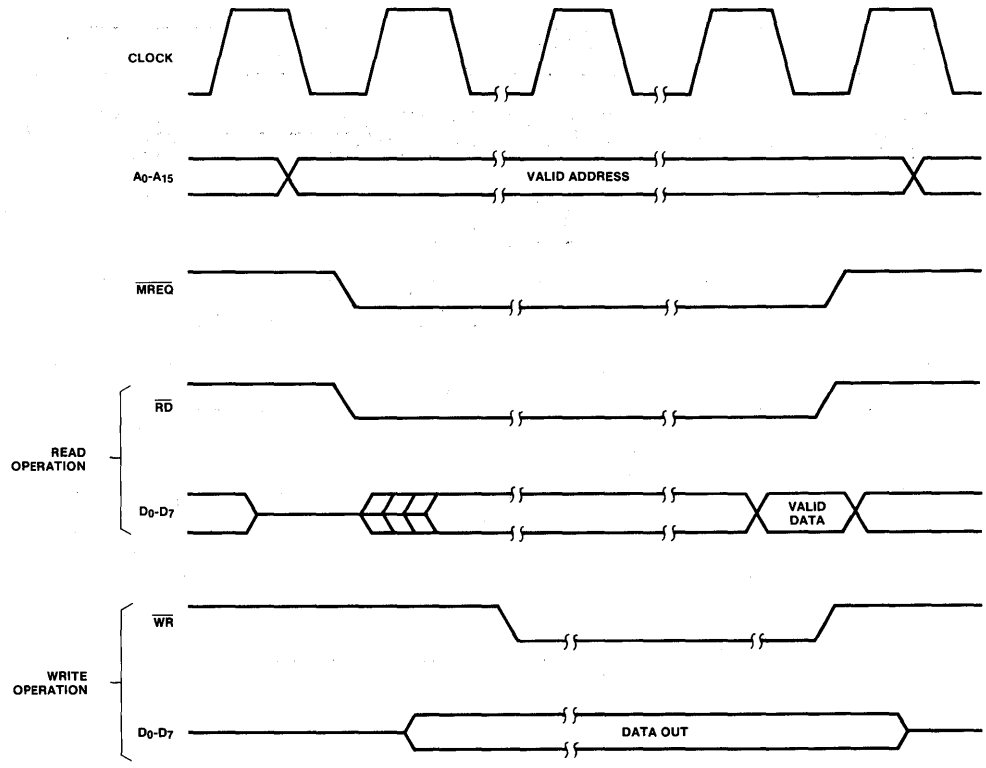


Figure 11. Z80 Read and Write Cycle

```
                                EEWRZ80.1
 LOC   OBJ CODE M STMT SOURCE STATEMENT                              ASM 5.9

                    175
                    176  ;-------------------------------------
                    177  ; Z80 EEROM Write routine.
                    178  ; Incorporates auto-erase and timing
                    179  ; in software.
                    180  ; Accepts: address to be written: Reg DE
                    181  ;          Data    to be written: Reg B
                    182  ; Uses: A, B, D, E Destroys: A
                    183  ;-------------------------------------
                    184
009B   3EFF         185  EEWR:   LD      A,0FFH   ; FF for erasure.
009D   12           186          LD      (DE), A ; BEGIN ERASE
009E   CDAE00       187          CALL    WaitTwp
00A1   1A           188          LD      A, (DE) ; END ERASE
                    189
00A2   78           190          LD      A,B      ; Data to be written
00A3   12           191          LD      (DE), A  ; BEGIN WRITE
00A4   CDAE00       192          CALL    WaitTwp
00A7   1A           193          LD      A, (DE) ; Read to end Write
00A8   1A           194          LD      A, (DE) ; Read to Verify
00A9   B8           195          CP      B        ; Check Verification
00AA   C2C800       196          JP      NZ, ERR1
00AD   C9           197          RET
                    198
                    199
                    200  ;-----------------------------
                    201  ; Wait routine for EEROM Byte/ Erase
                    202  ; Uses: Registers A, B,C
                    203  ; Destroys: A,C
                    204  ;-----------------------------
00AE   78           205  WaitTwp:LD      A,B
                    206  ; Store B reg in TMP1
00AF   3202C0       207          LD      (TMP1),A
                    208
                    209  ; Set timing constant for Twp.
                    210  ; This 16-bit constant is loaded
                    211  ; into Registers BC, and depends
                    212  ; on the speed of the CPU clock.
00B2   3E07         213          LD      A, 07
00B4   47           214          LD      B,A
00B5   3E06         215          LD      A, 06
00B7   4F           216          LD      C,A
                    217
                    218  ; The following loop performs the wait,
                    219  ; by decrementing BC until the 16-bit
                    220  ; number contained in BC equals zero.
                    221
00B8   3E00         222          LD      A, 00H
00BA   0B           223  More:   DEC     BC
00BB   B8           224          CP      B
00BC   C2BA00       225          JP      NZ, More
00BF   B9           226          CP      C
00C0   C2BA00       227          JP      NZ, More
00C3   3A02C0       228  DUN:    LD      A, (TMP1) ; Restore B Reg
00C6   47           229          LD      B,A
00C7   C9           230          RET
```

Figure 12. Z80 E²ROM Erase/Write Routine

8088 Interface

An example interface is shown between an 8088 (operating in minimum mode) and a 16K E^2ROM (see Figure 14). The reader may note that this is almost identical to the 8085 E^2ROM interface (see Figure 6), with only minor differences. First, the NOR gates used cannot be a standard TTL or LSTTL device, but must be a CMOS or other high impedance input, so that the CLK signal is not loaded. The CLK signal, as output by the 8284, is used as the clock input to the 8088. The V_{OH} level on this signal can fall below specification as a result of a TTL load. A CMOS NOR package, such as a 74C02 or similar device, eliminates this problem. Since the 74LS74 operates from bussed control and data lines, its requirements are not so stringent, and a 74LS74 will work fine in most applications.

The operation of this circuit is almost identical to the operation of the 8085 interface, as a comparison of the timing diagrams will show (see Figures 7b and 15) . Because these processors share similar bus timing, the signals differ only in magnitudes of setup and hold times. All required setup and hold times should be confirmed to the satisfaction of the system designer.

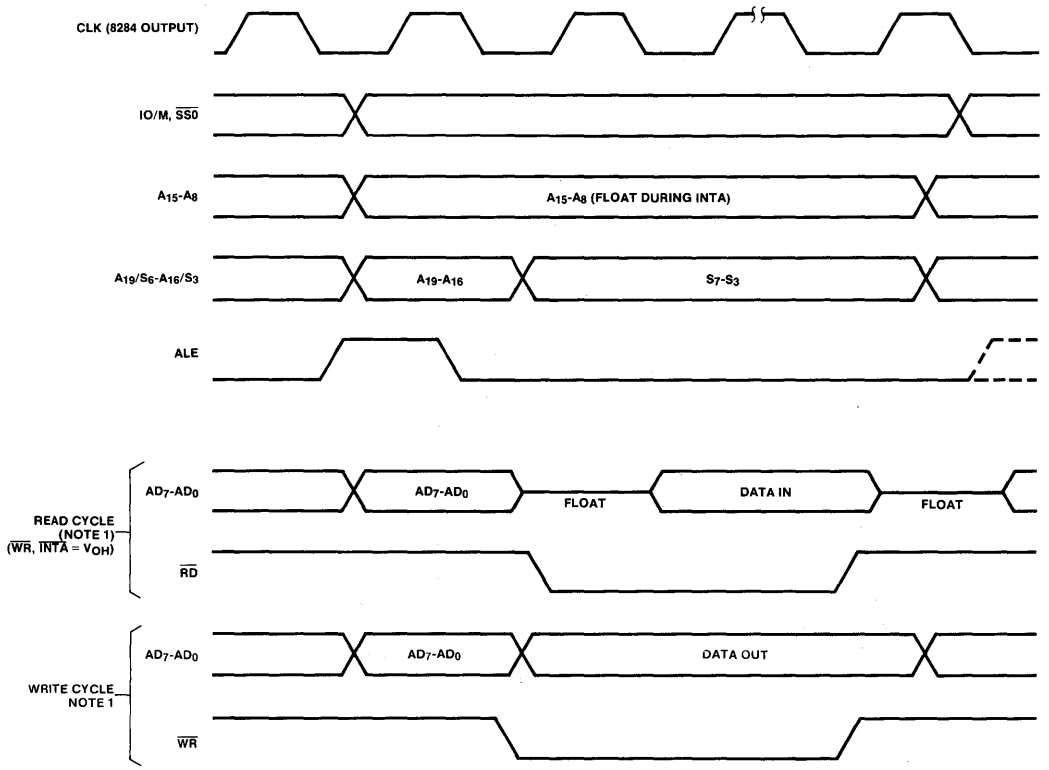


Figure 13. 8088/8086 Bus Timing — Minimum Mode

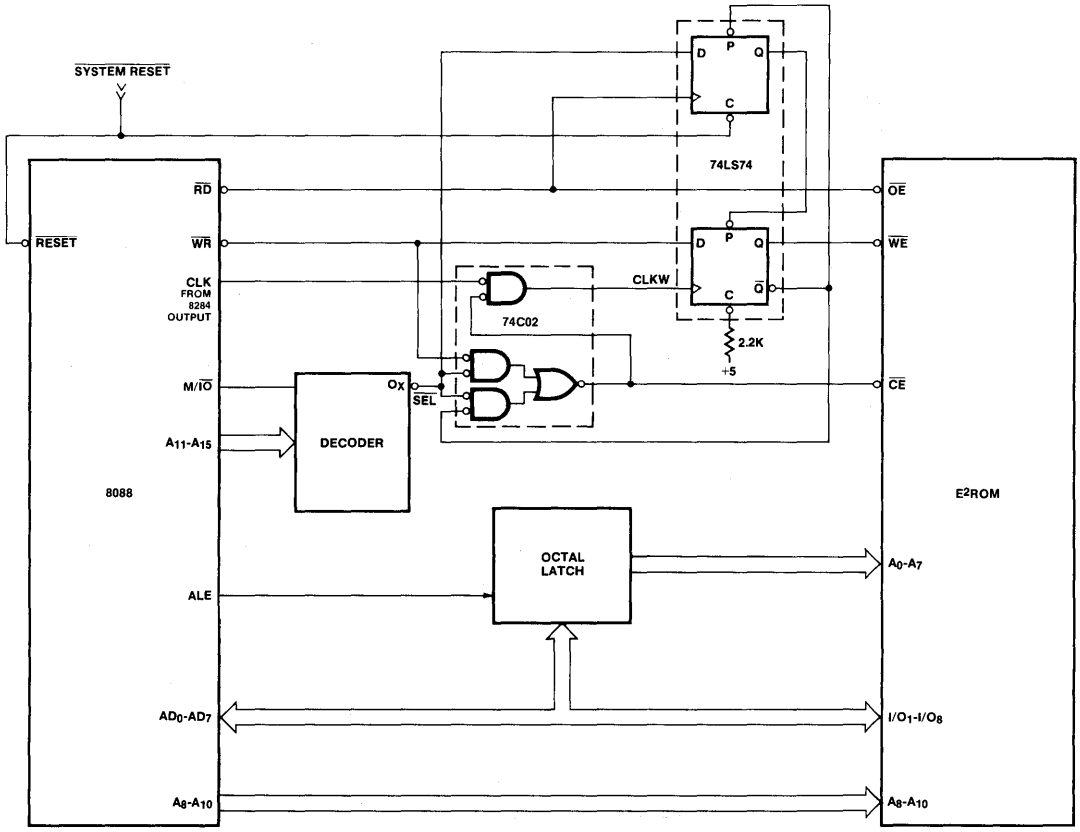
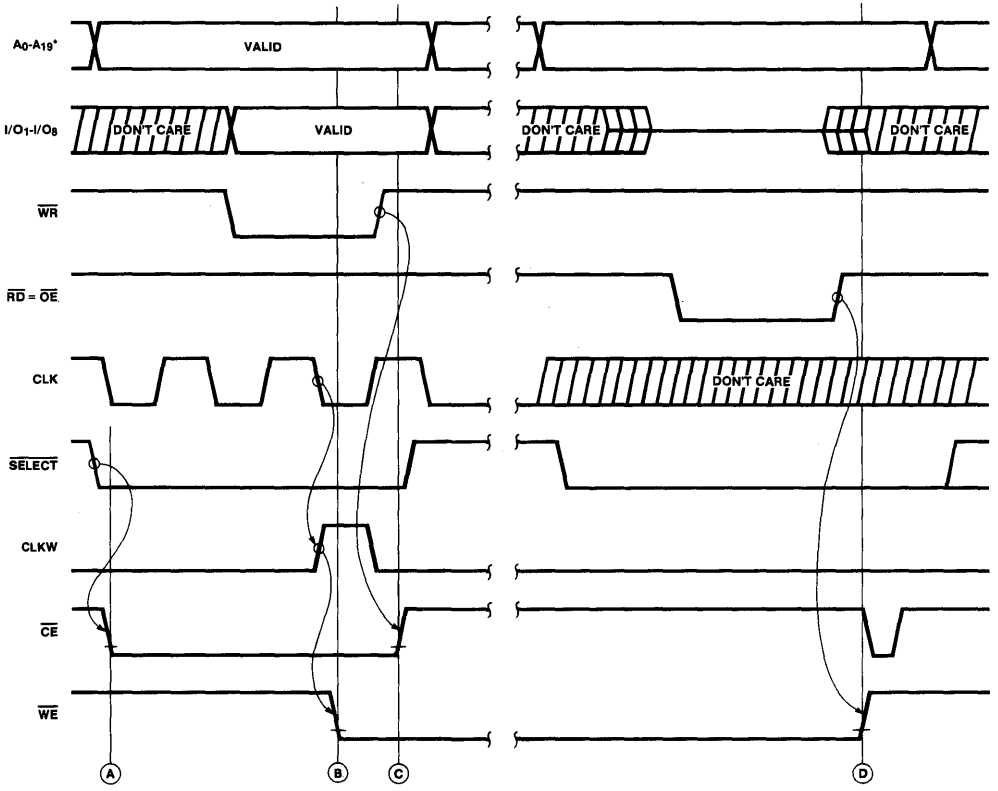


Figure 14. E²ROM Interface — 8088 (Minimum Mode)

REL/APP NOTES



*A_0-A_{19}: ADDRRESS SIGNALS MULTIPLEXED WITH STATUS AND DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 15. Timing Diagram — 8088/8086 E²ROM Interface

8086 Interface

A sample E²ROM interface shown for the 8086 (see Figure 16) compares very closely in layout and operation to that for the 8088 (see Figure 14). The 8086 interface accounts for the 16-bit 8086 data bus by latching both bytes of address and implementing a pair of devices to read and write an entire word at a time. E²ROM interface control signals are identical to those for the 8088 interface (see Figure 15).

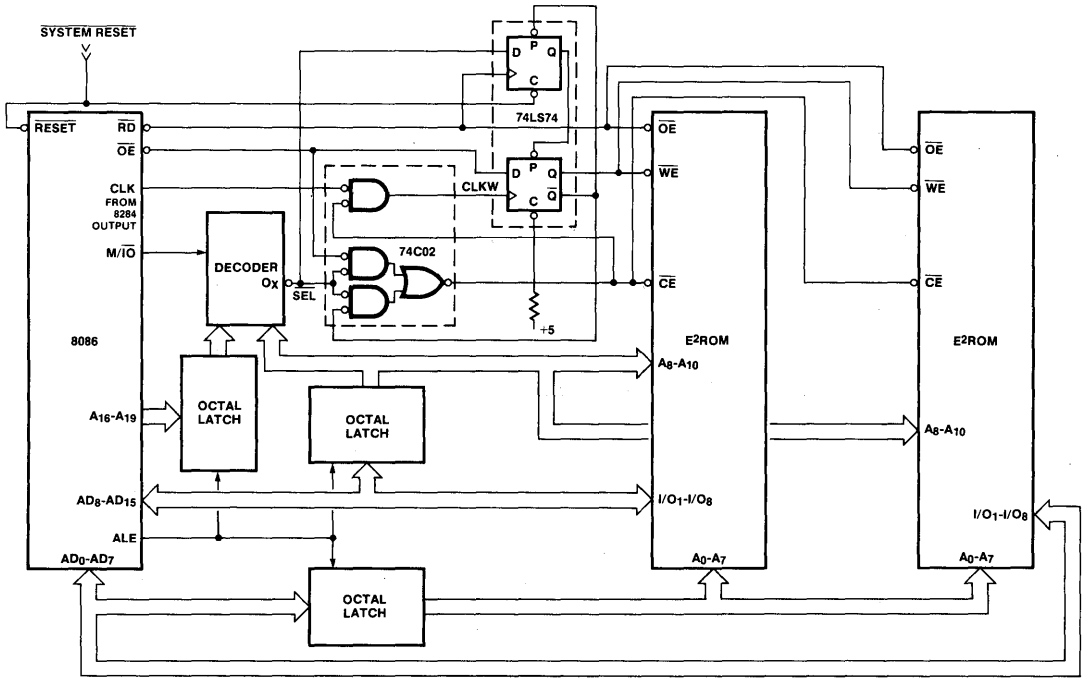


Figure 16. E²ROM Interface — 8086 (Minimum Mode)

71840 (Z8) Interface

An example E²ROM interface is presented for the 71840 (see Figure 17). SEEQ's 71840 is a single-chip microcomputer, with 4K x 8 of **EPROM** and 244 bytes of RAM, which is otherwise compatible with the Z8. Using the architecture and code of the Z8, the 71840 has a logical instruction set, pipelined execution, and a high degree of flexibility, while providing the additional features of Silicon Security™ and EPROM programming. The interface shown includes the octal latch, used to demultiplex the eight address/data bits for the E²ROM. The rest of the circuit acts to produce the control signals shown in Figure 3.

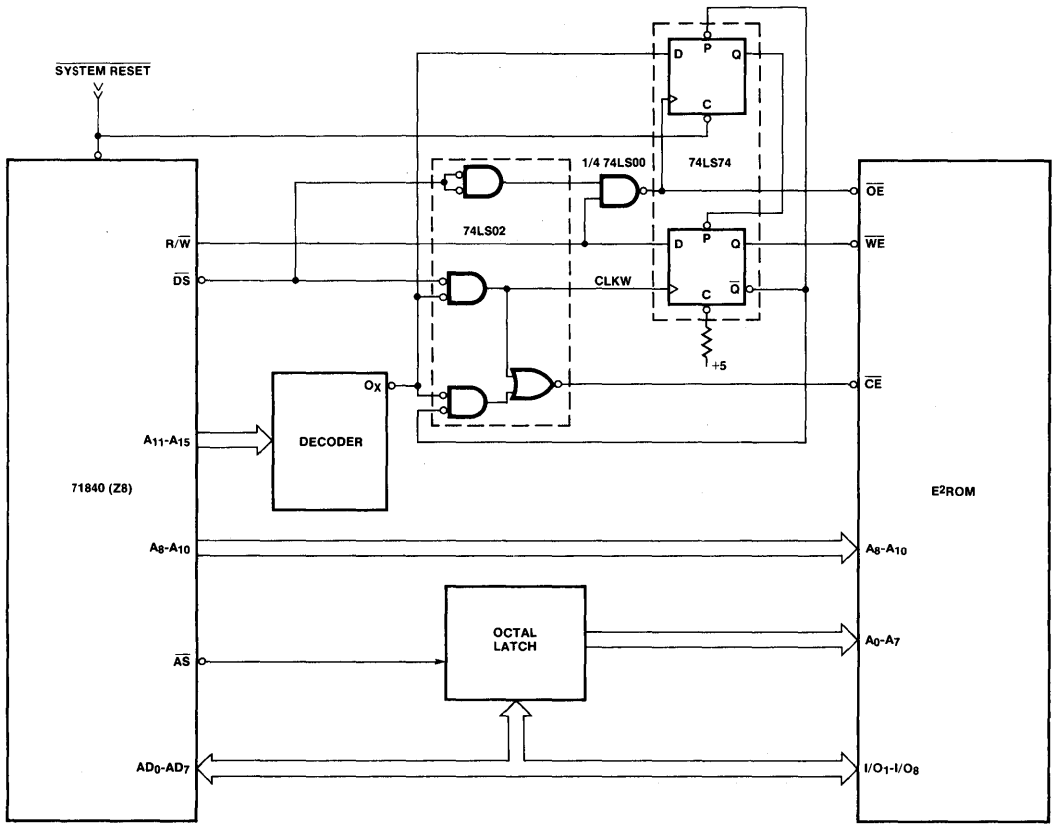


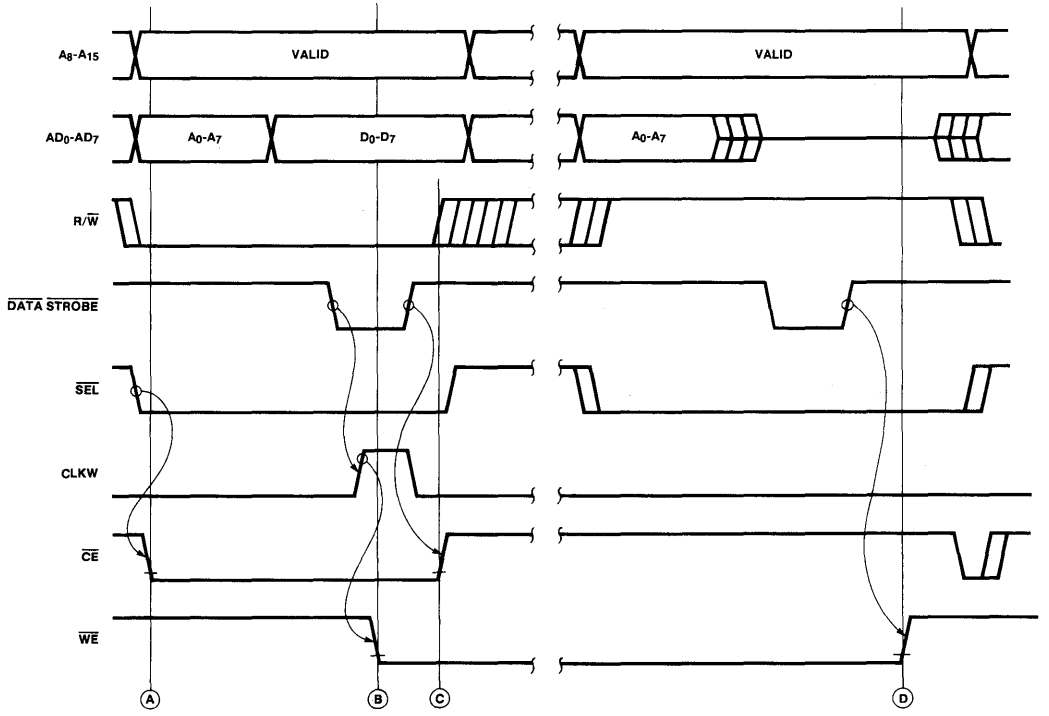
Figure 17. 71840/E²ROM Interface

The operation of the remaining circuitry in write cycle initiation is very simple. The following explanation refers to the timing diagram presented in Figure 18. To initiate the write cycle, the 71840 issues a Write command to the E²ROM device. After addresses become valid, the decoder brings $\overline{SEL}$ active low (see (A) in Figure 18). Subsequently, the falling edge of $\overline{DATA\ STROBE}$ ($\overline{DS}$) clocks R/$\overline{W}$ into the $\overline{WE}$ flip-flop, initiating a write cycle by bringing $\overline{WE}$ active low (see (B) in Figure 18). At this time, the latched E²ROM latches address, data, and control signals.

At the trailing (rising) edge of $\overline{DS}$, the gating circuitry inhibits $\overline{CE}$, and $\overline{CE}$ is brought to V_{IH} (see (C) in Figure 18). At this point, the timer E²ROM latches data and initiates its write cycle. Both devices have begun the write cycle; now the system is able to time out the write cycle, in order to complete storage of charge within the E²ROM cell.

The termination of the write cycle occurs with equal simplicity (see Figure 18). When the processor reads from the E²ROM, the rising edge of $\overline{DS}$ causes the $\overline{WE}$ flip-flop to be preset. This brings $\overline{WE}$ high (see (D) in Figure 18), ending the write cycle.

An example software driver routine is provided for the 71840 (see Figure 19). This routine will handle initiation, timing, and termination of a write cycle, as well as automatic erasure of the byte to be programmed.



*A_0-A_7: ADDRESS SIGNALS MULTIPLEXED WITH DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 18. Timing Diagram — 71840/E²ROM Interface

```
                        186 //-----------------------
                        187 // The following is a general routine for writing
                        188 // data contained in the working register
                        189 // DataReg to an EEROM in
                        190 // the location pointed to by the working register
                        191 // pair AdReg. This EEROM is assumed to be in the
                        192 // external data memory of Z8.
                        193 // Write FF to erase byte.
P 0060 7C  FF           194 EEWR:   LD      OutReg, #%FF
P 0062 92  70           195         LDE     @AdReg,  OutReg
P 0064 D6  0071         196         CALL    WaitWP          // Wait for Twp
P 0067 82  80           197         LDE     NowReg, @AdReg  // Turn off WE
                        198 // Now, write the data to the part.
P 0069 92  90           199         LDE     @AdReg, DataReg
P 006B D6  0071         200         CALL    WaitWP          // Wait for Twp
P 006E 82  80           201         LDE     NowReg, @AdReg  // turn off WE.
                        202
P 0070 AF               203 FinWr:  RET             //return from routine
                        204 // End of EEPROM Write Routine
                        205 //-------------------------------------------
                        206
                        207 // Timing routines
P 0071 EC  0A           208 WaitWP: LD      RLoop2, #Twp  // # of ms to wait
                        209                         // 10-> wait 10 mS.
                        210                         // 1 -> Wait 1  mS.
                        211
P 0073 D6  007E         212 WPLoop: CALL    Wait1ms
P 0076 00  EE           213         DEC     RLoop2
P 0078 6D  007D         214         JP      Z, DunWP
P 007B 8B  F6           215         JR      WPLoop
P 007D AF               216 DunWP:  RET             // Done with Twp.
                        217
                        218 // Basic 1 msec timing routine-
                        219 // adjust for microprocessor crystal freq.
                        220 // The value of Hex58 (Dec88) works with
                        221 // a Z8 with a 6.144 MHz xtal.
                        222 // Use %6A for 7.3728 MHz xtal. Elimination
                        223 // of NOP, or xtal substitution, will
                        224 // require recalibration.
P 007E FC  6A           225 Wait1ms: LD     RLoop3, #%6A
                        226
P 0080 FF               227 Tim1p:  NOP
P 0081 00  EF           228         DEC     RLoop3
P 0083 6D  0088         229         JP      Z, Dun1ms
P 0086 8B  F8           230         JR      Tim1p
                        231
P 0088 AF               232 Dun1ms: RET             // Done with wait
                        233
                        234 //End of EEROM Timing Routines
                        235 //---------------------------------
```

Figure 19. 71840 E²ROM Erase/Write Routine

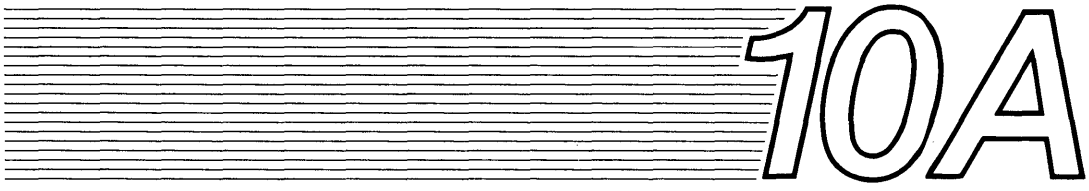
Conclusion

The development in E²ROM memory is continuing at an ever increasing pace. Recent strides in E²ROM cost reduction, access time, and availability have made non-volatile memory suitable for more applications than ever before. It is the purpose of this application note to contribute to this evolution in semiconductor memory by assisting the system designer in the task of E²ROM implementation. Armed with basic hardware and software examples of working E²ROM applications, the designer can more easily complete a feasible E²ROM design, using the flexible, cost-effective devices currently offered.

Acknowledgements

The author wishes to thank J. Oliphant and D. Reynolds for their contributions to this application note.

Power-Up/Down with SEEQ's E^2ROM



POWER-UP/DOWN WITH SEEQ's E^2ROM

seeq
Technology, Incorporated

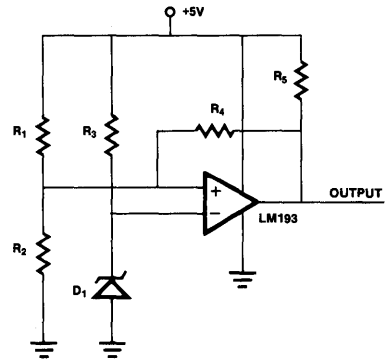
Power-Up/Down with SEEQ's E²ROM

Introduction

Electrically Erasable programmable Read-Only Memories (E²ROMs) are semiconductor devices offering high-density non-volatile random-access data storage. A read operation with E² devices is similar to that for an EPROM or static RAM. The write operation, however, requires a millisecond or longer. Previous generations of E²ROMs required high-voltage wave-shaped pulses during a write operation. With such strict requirements for the write control signal, the typical E² system designer was careful to ensure the correct level of this signal under all conditions, including power-related situations when the system is turned off or on. Only recently has the convenience of E²ROM been available in devices which can be written with simple TTL-compatible signals. SEEQ offers such devices in several densities.

With the advent of five-volt E²ROMs, non-volatile memory has shown far greater flexibility and ease of implementation. The ease of use allowed by TTL interfaces cannot release the designer from the normal constraint of ensuring reliable operation during power on/off situations. What signals should the interface devices provide when the system is turned off or on (or otherwise loses power)? Under conditions of extreme or repeated brownouts? During times such as these, when V_{CC} may be outside of specified limits for correct operation of support logic, this support logic can supply signals to the E²ROM which initiate an undesired write cycle. This causes an inadvertent write to a location in the E²ROM. In order to ensure system reliability in such situations, it is very important to ensure that inputs (during power up/down conditions) from support devices do not cause inadvertent writes to an E²ROM device. A certain amount of the required protection is included on-board the E²ROMs, and is described below. At the system designer's option, system reliability may be enhanced by absolute prevention of false writes.

The purpose of this application note is to provide the system designer with a simple method by which to prevent false writes during power-up and power-down situations. A simple circuit is shown (see Figure 1), its operation is explained, and some useful design considerations are outlined.



R_1 = 63.4 KΩ (1% Metal Film)
R_2 = 71.5 KΩ (1% Metal Film)
R_3 = 51 KΩ
R_4 = 1.5 MΩ (1% Metal Film)
R_5 = 10 KΩ
D_1 = LT1004 - 2.5

Figure 1. E²ROM Write-Protection Circuit

The ideas and designs presented in this note are meant to serve as a starting point for the designer, to assist him in accomplishing his goal. The solution given, however, is not the only approach. There are many ways to ensure desired signals to the E²ROM during power up/down conditions. The designer is encouraged to tailor his solution to the specific requirements of his application.

Using E²ROM's Built-in Protection

In SEEQ's E²ROMs, protection against false writes has been simplified by 3 built-in protection mechanisms on the chip. This protection logic (transparent to the user) does not make writing any less convenient. Table 1 shows the conditions which are required in order to guarantee initiation of a write cycle V_{CC} must be within specified limits, $\overline{CE}$ must be active low, and $\overline{OE}$ must be V_{IH}, T_{CS} (50 ns) before the falling edge of $\overline{WE}$. Due to E²ROM's protection logic, under certain other conditions, there are modes in which writing is inhibited (see Table 2). First, if V_{CC} is less than 3.0 V, writing is prevented, regardless of the other input signals. Second, OUTPUT ENABLE ($\overline{OE}$) at V_{IL} (satisfying T_{CS}) inhibits writing. Third, in order to inhibit a write cycle, $\overline{WE}$ or $\overline{CE}$ can be held at V_{IH}.

Several failure modes are prevented by the protection logic described above. For example, if V_{CC} comes up with $\overline{WE}$ already low, this will be interpreted as a continuous low on $\overline{WE}$ and will not initiate a write cycle, because a falling edge on $\overline{WE}$ is required AFTER V_{CC} rises. Inadvertent writes are prevented when V_{CC} is less than 3.0 V (see Table 2); all that is left to external circuitry is write-protection for V_{CC} between the levels of 3.0 V (the lowest V_{CC} level at which the device can write) and the V_{CC} level at which the support logic issues valid signals.

Table 1. Conditions Required to Guarantee Write-Cycle Initiation in E²ROMs

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{CC}	All Other Pins
	V_{IL}	V_{IH}	4.5 -5.5 V	X

Notes:
1. Active levels shown in above table require T_S set-up time of 50 ns (see E²ROM's data sheet)
2. X = TTL Don't Care.

External Write-Protection Circuitry

With the protection logic on board the E²ROMs, the part can be protected against inadvertent writes in any of several ways. The system designer can ensure that $\overline{CE}$ is high during power-up and power-down. Alternatively, one can ensure that $\overline{WE}$ never has a falling edge during power-up or power-down. For example, one could ensure that $\overline{WE}$ stays at V_{IL} on power-up until a latch is reset, releasing a pull-down. This would ensure write prevention.

Another manner of write protection has been to bring $\overline{OE}$ low during power-up and power-down. This inhibits writing (see Table 2), often allows the simplest realization, and is the general path chosen in this application note. Yet the timing and levels of signals provided must be scrutinized here, as well.

Merely inserting a pull-up on $\overline{OE}$ will tend to pull $\overline{OE}$ down when V_{CC} is low, but may not force a valid V_{IL} level. Inserting a low forward voltage drop diode between the system-wide $\overline{RESET}$ signal and the E²ROM's $\overline{OE}$ signal may work, but depends on the timing of V_{CC} and $\overline{RESET}$.

The specific form of protection against inadvertent write cycles chosen for this application note, one with more certainty of protecting against inadvertent writes, is to force either $\overline{OE}$ low (V_{IL}) or $\overline{CE}$ High (V_{IH}) during power-up and power-down. Figure 1 shows a circuit that can be used to fulfill this requirement.

Table 2. Conditions Required to Inhibit Write-Cycle Initiation in E²ROMs

	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{CC}	All Other Pins
Inhibition Mode 1	V_{IH}	X	X	X	X
Inhibition Mode 2	X	V_{IH}	X	X	X
Inhibition Mode 3	X	X	V_{IL}	X	X
Inhibition Mode 4	X	X	X	Under 3.0 V	X

Notes:
1. Active levels shown in above table require T_S set-up time of 50 ns (see E²ROM's data sheet)
2. X = TTL Don't Care.

The circuit shown in Figure 1 provides a proper output signal (comparator's output) to prevent false write. During power-up, as is shown in Figure 2A, the output of the comparator is kept low from the time that V_{CC} is 2.5 V until it reaches 4.8 volts. The output switches to V_{IH} when V_{CC} goes above 4.8 volts. During power-down, however, as is shown in Figure 2B, the comparator's output is forced low as soon as V_{CC} falls below 4.6 V and is kept low until V_{CC} goes below 2.5 volts. Circuit functionality is not guaranteed below this point.

To prevent inadvertent writes, either $\overline{OE}$ or $\overline{CE}$ pin can be used. The first method is by forcing and keeping $\overline{OE}$ low (V_{IL}) when V_{CC} is below 4.5 volts. This can be done, as is shown in Figure 3A, by connecting comparator's output directly to E²ROM's $\overline{OE}$ pin. As soon as V_{CC} falls below 4.6 V, the $\overline{OE}$ is forced low preventing any internal write initiation. This pin is kept low (valid) until V_{CC} goes below 2.5 volts. Internal protection circuitry protects the part beyond this point (activated when V_{CC} falls below 3.0 V).

The second method of protecting the part against inadvertent write is by forcing and keeping $\overline{CE}$ high when V_{CC} is below 4.5 and above 2.5 volts. This can be done, as is shown in Figure 3B, by NAND gating (74HCT00) the comparator's output with a CS signal. The output of the NAND gate, which is connected to E²ROM's $\overline{CE}$ pin, is controlled by the CS input when V_{CC} is above 4.6 volts. The other input controls NAND gate's output when V_{CC} is below 4.6 V (above 2.5 V). Keep in mind that the CS line must be a high true signal and the NAND gate should be a high speed CMOS device.

Either method described above can be used for protection against inadvertent writes. System designers have to determine their need first and based upon that, select one of the above circuits or one of their own.

Circuit Operation

The circuit shown in Figure 1 is designed to provide a high (V_{IH}) output (comparator's output) when V_{CC} is above 4.8 volts and a low (V_{IL}) output when V_{CC} falls below 4.6 V (above 2.5 V). This is done by using a comparator (LM193 available from National Semiconductor), a temperature compensated voltage reference device (LT1004MH-2.5 available from Linear Technology) and a few resistors. The circuit has been designed to operate over military temperature range.

As it can be seen in Figure 1, the negative input of the comparator is connected to ground through a temperature compensated voltage reference device (D_1) and to V_{CC} through a resistor (R_3). As long as

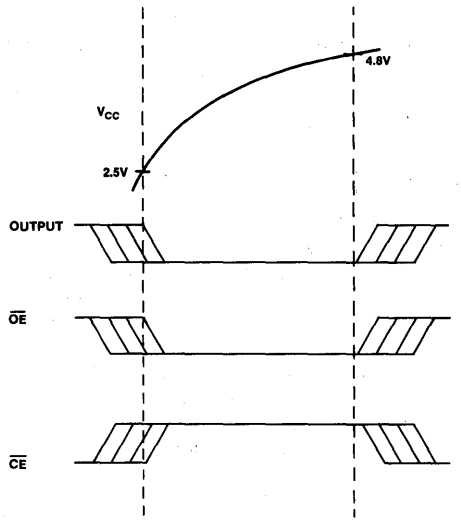


Figure 2A. Timing Diagram—Power-Up Using Either $\overline{CE}$ or $\overline{OE}$ Protection

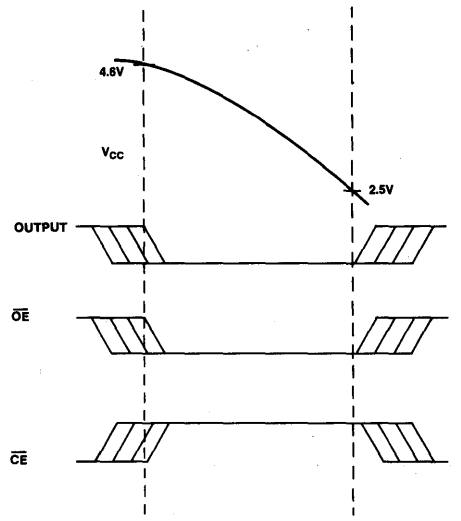


Figure 2B. Timing Diagram—Power-Down Using Either $\overline{CE}$ or $\overline{OE}$ Protection

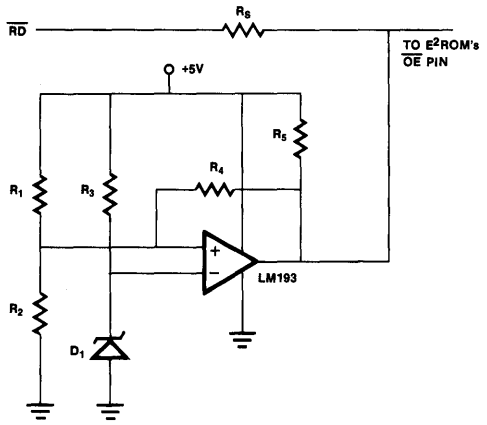


Figure 3A. $\overline{OE}$ Protection Circuit

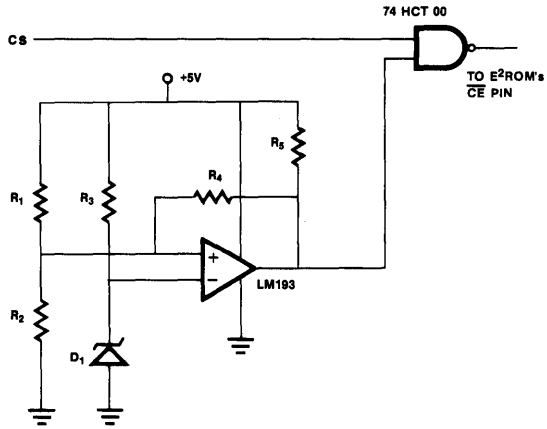


Figure 3B. $\overline{CE}$ Protection Circuit

V_{CC} is below 2.5 V, D_1 is not conducting (no current flow through it). However, as soon as V_{CC} goes above 2.5 V and stays there, D_1 conducts providing a 2.5 V reference voltage at the negative input (no current flow into negative input). The resistor (R_3) is used to limit the amount of current through D_1.

The positive input on the other hand, is connected to a voltage divider (R_1 & R_2) as well as the output (through R_4). The voltage at this input forces the output to go either high (V_{IH}) or low (V_{IL}). When V_{CC} is below 4.6 V, the voltage divider causes this input to be below reference voltage with respect to ground forcing the output low. On the other hand, when V_{CC} goes above 4.8 V, the positive input voltage goes above reference voltage forcing the output high. The output stays high as long as V_{CC} is above 4.8 volts. The feedback resistor (R_4) is used to enforce output voltage on the positive input while R_5 is used as a pull-up resistor. Proper device selection, as is recommended in this Application Note, can insure correct operation of the circuit over military temperature range.

System Consideration

As was mentioned above, correct circuit operation requires proper device selection. The comparator and temperature compensated voltage reference device (D_1) selections are critical. You have to be sure that D_1 provides 2.5 V drop across allowing half a volt safety margin between external protection circuit and the internal one (3.0 V internal power protection). It is suggested to use devices recommended in this Application Note. Other circuit elements that can influence circuit operation are the resistors. For correct operation over temperature, it is recommended to use 1% metal film resistor for R_1, R_2 and R_4. The other two can be carbon film resistors.

If $\overline{CE}$ pin is used for protection, the comparator's output must be NAND gated with a CS signal. Proper gate output is guaranteed if a high speed CMOS gate is used. Also, designers have to make sure that the CS input is a high true signal. However, no NAND gate is needed if $\overline{OE}$ pin is used to protect the part against false write. Comparator's output can be connected to $\overline{OE}$ (through R_S). A choice of values for R_S Resistor depends on $\overline{OE}$ driver (RD line). The R_S resistor is used to insure a low $\overline{OE}$ input when V_{CC} is below 4.6 V (comparator's output is low). If open collector driver is used, the pull-up resistor can replace R_S.

Conclusion

It has always been important for a system designer to ensure reliability as his system is turned off and on. Currently, the importance of this area of design is increasing. As the usage of five-volt E²ROMs increases, applications are expanding into environments where V_{CC} may be undependable, power glitches may exist, and in general a system must be more fault-tolerant. With the circuit contained in this application note, the designer can more easily ensure that his system meets applicable specifications and is able to utilize the convenience of E²ROMs.

SECTION 6

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Dyne-A-Mark Corp.
Fort Lauderdale, FL
(305) 771-6501

Dyne-A-Mark Corp.
Maitland, FL
(305) 831-2097

Dyne-A-Mark Corp.
Palm Bay, FL
(305) 727-0192

Georgia
Electronic Sales, Inc.
Norcross, GA
(404) 448-6554

Illinois
KMA Sales
Rolling Meadows, IL
(312) 398-5300

Indiana
Valentine & Assoc.
Greenwood, IN
(317) 888-2260

Indiana (Cont.)
Valentine & Assoc.
South Bend, IN
(219) 288-7070

Iowa
Advanced Technical Sales
Overland Park, KS
(913) 642-6675

Kansas
Advanced Technical Sales
Overland Park, KS
(913) 642-6675

Maryland
L.D. Lowery
Columbia, MD
(301) 964-0225

Massachusetts
New England Tech. Sales.
Burlington, MA 01803
(617) 272-0434

Michigan
Rathsburg Assoc., Inc.
Detroit, MI
(313) 882-1717

Minnesota
Cahill, Schmitz & Cahill
St. Paul, MN
(612) 646-7217

Missouri
Advanced Tech. Sales
St. Louis, MO
(314) 878-2921

New Mexico
Compass Marketing
Albuquerque, NM
(505) 888-0800

New York
ERA Inc.
Commack, NY
(516) 543-0510

GenTech
Binghamton, NY
(607) 648-8833

New York (Cont.)
GenTech
Liverpool, NY
(315) 451-3480

GenTech
Pittsford, NY
(716) 381-2820

GenTech
Pleasant Valley, NY
(914) 635-3233

North Carolina
ESI
Cary, NC
(919) 467-8486

Ohio
The Lyons Corp.
Dayton, OH
(513) 278-0714

The Lyons Corp.
Richfiled, OH
(216) 659-9224

Oklahoma
Bonser-Philhower Sales
Tulsa, OK
(918) 744-99964

Oregon
Northwest Marketing
Assoc., Inc.
Portland, OR
(503) 620-0441

Pennsylvania
L.D. Lowery
Broomall, PA
(513) 278-0714

The Lyons Corp.
Bridgeville, PA
(513) 278-0714

Texas
Bonser-Philhower Sales
Austin, TX
(512) 346-9186

Bonser-Philhower Sales
Houston, TX
(713) 531-4144

Texas (Cont.)
Bonser-Philhower Sales
Richardson, TX
(214) 234-8438

Utah
Waugaman Assoc., Inc.
Salt Lake City, UT
(801) 261-0802

Washington
Northwest Marketing
Assoc. Inc.
Bellevue, WA
(206) 455-5846

Wisconsin
KMA Sales
Milwaukee, WI
(414) 259-1771

Canada
Electro Sources, Inc.
Rexdale, Ontario
Canada
(416) 675-4490

Authorized North American Distributors

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RM Electronics
Huntsville, AL
(205) 852-1550

Schweber Elect., Inc.
Huntsville, AL
(205) 882-2200

Arizona
Anthem Elect., Inc.
Tempe, AZ
(602) 244-0900

Schweber Elect., Inc.
Phoenix, AZ
(602) 997-4874

Time Electronics
Tempe, AZ
(602) 967-2000

California
Anthem Elect. Inc.
Chatsworth, CA
(213) 700-1000

Anthem Elect., Inc.
E. Irvine, CA
(714) 768-4444

Anthem Elect., Inc.
San Diego, CA
(619) 279-5200

Anthem Elect., Inc.
San Jose, CA
(408) 946-8000

Bell Industries
Roseville, CA 95678
(916) 969-3100

Bell Industries
Sunnyvale, CA 94089
(408) 734-8570

Schweber Elect., Inc.
Canoga, CA
(213) 999-4702

Schweber Elect., Inc.
Irvine, CA
(714) 556-3880

Schweber Elect., Inc.
Sacramento, CA
(916) 929-9732

California (Cont.)
Schweber Elect. Inc.
San Diego, CA
(619) 450-0454

Schweber Elect. Inc.
San Jose, CA
(408) 946-7171

Time Electronics
Anaheim, CA
(714) 937-0911

Time Electronics
Chatsworth, CA
(818) 998-7200

Time Electronics
San Diego, CA
(619) 586-1331

Time Electronics
Sunnyvale, CA
(408) 734-9888

Time Electronics
Torrance, CA
(213) 320-0880

Colorado
Anthem Elect., Inc.
Englewood, CO
(303) 790-4500

Bell Industries
Wheatridge, CO
(303) 424-1985

Time Electronics
Englewood, CO
(303)850-7701

Connecticut
Lionex
Meriden, CT
(203) 265-1244

Schweber Elect., Inc.
Danbury, CT
(203) 792-3500

Time Electronics
Cheshire, CT
(203) 271-3200

Florida
Schweber Elect., Inc.
Altamonte Springs, FL
(305) 331-7555

Schweber Elect., Inc.
Hollywood, FL
(305) 927-0511

Time Electronics
Ft. Lauderdale, FL
(305) 974-4800

Time Electronics
Orlando, FL
(305) 841-6565

Georgia
Electro-Air Corp.
Atlanta, GA
(404) 351-3545

Q.C./Southeast, Inc.
Norcross, GA
(404) 449-9508

Schweber Elect., Inc.
Norcross, GA
(404) 449-9170

Time Electronics
Norcross, GA
(404) 448-4448

Illinois
RM Electronics
Elk Grove Village, IL
(312) 364-6622

Schweber Elect., Inc.
Elk Grove Village, IL
(312) 364-3750

Time Electronics
Wood Dale, IL
(312) 350-0610

Indiana
Graham Electronics
Fort Wayne, IN
(219) 423-3422

Graham Electronics
Indianapolis, IN
(317) 634-8202

Indiana (Cont.)
Graham Electronics
Lafayette, IN
(317) 423-5564

RM Electronics
Indianapolis, IN
(317) 291-7110

Iowa
Schweber Elect., Inc.
Cedar Rapids, IA
(319) 373-1417

Kansas
Schweber Elect., Inc.
Overland Park, KS
(913) 492-2921

Maryland
Lionex
Columbia, MD
(303) 964-0040

Schweber Elect., Inc.
Gaithersburg, MD
(301) 840-5900

Time Electronics
Columbia, MD
(301) 964-3090

Massachusetts
Lionex
Wilmington, MA
(617) 657-5170

Schweber Elect., Inc.
Bedford, MA
(617) 275-5100

Time Electronics
Woburn, MA
(617) 935-8080

Michigan
RM Electronics
Grand Rapids, MI
(616) 531-9300

Schweber Elect., Inc.
Livonia, MI
(313) 525-8100

Minnesota
Schweber Elect., Inc.
Edina, MN
(612) 941-5280

Time Electronics
Bloomington, MN
(612) 944-9192

Missouri
Schweber Elect., Inc.
Earth City, MO
(314) 739-0526

Time Electronics
St. Louis, MO
(314) 391-6444

New Hampshire
Schweber Elect., Inc.
Manchester, NH
(603) 625-2250

New Jersey
Lionex
Fairfield, NJ
(201) 227-7960

Schweber Elect., Inc.
Fairfield, NJ
(201) 227-7800

New Mexico
Bell Industries
Albuquerque, NM
(505) 292-2700

New York
Lionex
Hauppauge, NY
(516) 273-1660

Schweber Elect., Inc.
Rochester, NY
(716) 424-2222

Schweber Elect., Inc.
Westbury, NY
(516) 334-7474

New York (Cont.)
Time Electronics
Hauppauge, NY
(516) 273-0100

Time Electronics
E. Syracuse, NY
(315) 432-0355

North Carolina
Schweber Elect., Inc.
Raleigh, NC
(919) 867-0000

Ohio
Bell Industries
Dayton, OH
(513) 434-8231

Graham Electronics
Cincinnati, OH
(513) 772-1661

Graham Electronics
Columbus, OH
(614) 895-1590

Schweber Elect., Inc.
Beachwood, OH
(216) 464-2970

Schweber Elect., Inc.
Dayton, OH
(513) 439-1800

Time Electonics
Dublin, OH
(614) 761-1100

Oklahoma
Quality Components
Tulsa, OK
(918) 664-8812

Schweber Elect., Inc.
Tulsa, OK
(918) 622-8000

Oregon
Anthem Electronics
Lake Oswego, OR
(503) 684-2661

Bell Industries
Lake Oswego, OR
(503) 241-4115

Time Electronics
Portland, OR
(503) 685-3780

Pennsylvania
Lionex
Horsham, PA
(215) 443-5150

Pennsylvania
Schweber Elect., Inc.
Horsham, PA
(215) 441-0600

Schweber Elect., Inc.
Pittsburgh, PA
(412) 782-1600

Time Electronics
King of Prussia, PA
(215) 337-0900

Texas
Quality Components
Addison, TX
(214) 733-4300

Quality Components
Austin, TX
(512) 835-0220

Quality Components
Sugarland, TX
(713) 491-2255

RM Electronics
Dallas, TX
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Schweber Elect., Inc.
Austin, TX
(512) 458-8253

Schweber Elect. Inc.
Dallas, TX
(214) 661-5010

Schweber Elect., Inc.
Houston, TX
(713) 784-3600

Time Electronics
Austin, TX
(214) 241-7441

Time Electronics
Dallas, TX
(214) 241-7441

Utah
Anthem Elect., Inc.
Salt Lake City, UT
(801) 973-8555

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Bell Industries
Salt Lake City, UT
(801) 972-6969

Washington
Anthem Elect., Inc.
Redmond, WA
(206) 881-0850

Bell Industries
Bellevue, WA 98005
(206) 747-1515

Time Electronics
Bellevue, WA
(206) 641-3640

Time Electronics
Redmond WA
(206) 882-1600

Wisconsin
Bell Industries
Waukesha, WI
(414) 547-8879

RM Electronics
New Berlin, WI
(414) 784-4420

Schweber Elect., Inc.
Brookfield, WI
(414) 784-9020

Canada
Future Electronics
Calgary, Alberta
(403) 259-6408

Future Electronics
Edmunton, Alberta
(403) 486-0974

Future Electronics
Vancouver, British
Columbia
(604) 438-5545

Future Electronics
Downsview, Ontario
(416) 638-4771

Future Electronics
Ottawa, Ontario
(613) 829-8313

Future Electronics
Pointe Claire, Quebec
(514) 694-7710

INTERNATIONAL SALES OFFICES

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1849 Fortune Drive
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Telex: 296609

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Dammas House
Dammas Lane
Old Town
Swindon SN1 3EF U.K.
Tel: 0793-694999
Telex: 851444588

Southern European Sales Office

SEEQ Technology, Inc.
53 Rue de Chambourcy
78 300 Poissy, France
Tel: 3-0741146
Telex: 842695477

Authorized International Manufacturer's Representatives/Distributors

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RAE Industrial Electronics Pty. Ltd.
Victoria
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Sydney
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Crows Nest
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Austinmer
Tel: (02) 232 6933

Austria
Othmar Lackner Elektron Bauelemente & Gerate
Vienna
Tel: (0/222) 7526180

Belgium
MCA Tronix
Liege
Tel: (0/41) 362780 or 95

Denmark
Exatec
Copenhagen
Tel: (010) 45 156 5001

Finland
Komdel Oy
Espoo
Tel: (010) 358 0 885 011

Federal Rep. of Germany
Adicom
Industrie-Vertretungen
Munich
Tel: (0/89) 22 72 86

Astek Electronik
Vertriebs GmbH
Hamburg
Tel: (0/4106) 71084 or 86

Federal Rep. of Germany
Dacom Elecktronic
Vertriebs GmbH
Stuttgart
Tel: 0711/741021-22

Metronik GmbH
Munchen
Tel: (0/89) 611 4063

France
Radio Television Francaise (RTF)
Gentilly
Tel: (16/1) 664 11 01

RepTronic
Paris
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Hong Kong
Electrocon Products Ltd.
Kowloon
Tel: 3-687214-6

India
SRI RAM Assoc.
Bangalore
Tel: 602 140

Israel
Vectronics Ltd.
Herzlia
Tel: (0/52) 556070 or 71

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Eledra
Milano
Tel: (0/2) 34 97 51

Italy (Cont.)
Cefra Spa
Milano
Tel: (0/2) 235264
Rome
Tel:(0/6) 8456253

Japan
Japan Macnics Corporation (JMC)
Kawasaki-City
Tel: (0/44) 711 0022
Osaka City
Tel: (0/6) 325-0880

Rikei
Tokyo
Tel: 345 1411

Korea
Hanaro
Seoul
Tel: (02) 783 7141

The Netherlands
Techmation, Electronics B.V.
Haaften
Tel: (31) 04189 2222

New Zealand
VSI Electronics (N.Z.) Ltd.
Epsom, Auckland
Tel: 600 760

Norway
Heko-Tech
Fjellhamar
Tel: 010 47 270 5244

South Africa
Advanced Semiconductor Devices (PTY) Ltd.
Sandton
Tel: (011) 802-5820

Singapore/Malaysia
Desner Electronics (Far East) PTE Ltd.
Singapore
Tel: 3373188

Spain
Semiconductores
Barcelona
Tel: (9/3) 217 23 40

Sweden
Svensk Teleindustri AB
Vallingby
Tel: 010 46 438 0320

Switzerland
Anatec AG Electronische Bauteile
Zug
Tel: (0/42) 315 477

Taiwan
Bright Up Industries Co. Ltd.
Taipei
Tel: (0/2) 773 2194

Turkey
Turkelek Electronic Co., Ltd.
Ankara
Tel: (41) 18 94 83
Istanbul
Tel: (1) 143 40 46

United Kingdom
iMicrobusiness Ltd.
Newbury/Berkshire
Tel: 0635/42808

Kudos Electronics
Wokingham/Berkshire
Tel: 0734-794515

Pronto Electronic Systems Ltd.
Gants Hills/Essex
Tel: (0/1) 554 6222