CMOS LINEAR

2nd EDITION

-THOMSON
OELECTRONICS

CMOS LINEAR - 2nd EDITION

CMOS LINEAR

APRIL 1990

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON Microelectronics can now offer you a complete range of CMOS LINEAR devices including :

— OPERATIONAL AMPLIFIERS

— COMPARATORS

— TIMERS

This family of monolithics CMOS circuits provides the designers with high performance operation at low supply current and very good speed to power ratio.

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PRODUCT GUIDE

THE CMOS PRODUCTS RANGE

1 - CMOS OPERATIONAL AMPLIFIERS

3 CONFIGURATIONS

TS271	SINGLE
TS27X2	DUAL
TS27X4	QUAD

3 OFFSET VOLTAGE SELECTIONS

TS27X	10mV max.
TS27XA	5mV max.
TS27XB	2mV max.

SUPPLY CURRENT OPTIONS

TS271	PROGRAMMABLE	
TS27X	HIGH	1mA
TS27MX	MEDIUM	150 µA
TS27LX	LOW	10 µA

3 PACKAGE TYPES

N	DIP8 / DIP14
D	SO8 / SO14
J	CERDIP8 / CERDIP 14

3 TEMPERATURE RANGES

TS27XC	0 to + 70 °C
TS27XI	- 40 to + 105 °C
TS27XM	- 55 to + 125 °C

S90CMOS-01

2 - CMOS COMPARATORS

LOW POWER COMPs

TS372	DUAL
TS374	QUAD

MICROPOWER COMPs

TS3702	DUAL	Push Pull Output
TS3704	QUAD	
TS393	DUAL	Open Drain Output
TS339	QUAD	

3 TEMPERATURE RANGES

TS37XC / TS370XC / TS339C / TS393C	0 to + 70 °C
TS37XI / TS370XI / TS339I / TS393I	- 40 to + 105 °C
TS37XM / TS370XM / TS339M / TS393M	- 55 to + 125 °C

3 PACKAGE TYPES

N	DIP8 / DIP14
D	SO8 / SO14
J	CERDIP8 / CERDIP 14

S90CMOS-02

3 - CMOS TIMERS

2 CONFIGURATIONS

TS555	SINGLE
TS556	DUAL

3 TEMPERATURE RANGES

TS55XC	0 to + 70 °C
TS55XI	- 40 to + 105 °C
TS55XM	- 55 to + 125 °C

3 PACKAGE TYPES

N	DIP8 / DIP14
D	SO8 / SO14
J	CERDIP8 / CERDIP 14

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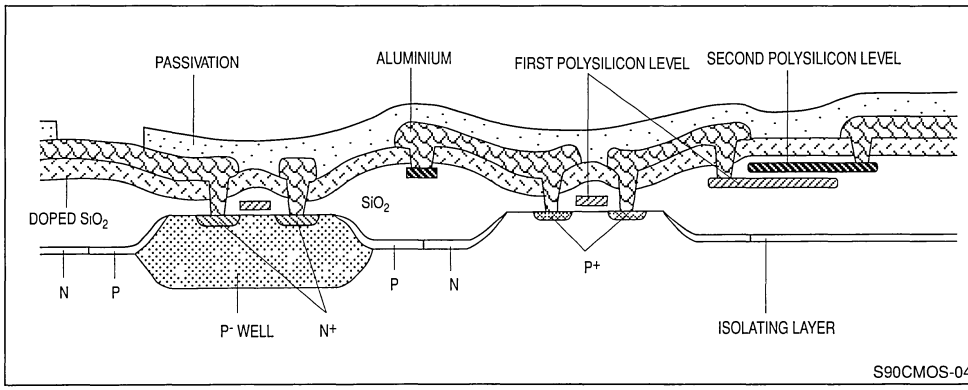
TECHNOLOGY

1 - PROCESS

Figure 1.



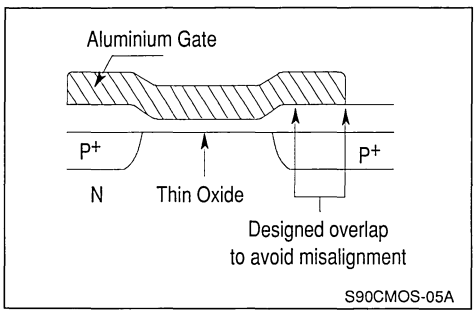
The SGS-THOMSON Microelectronics CMOS process uses for Standard Linear Products a 4µm P Well technology with dual layer polysilicon gate.

This process offers major advantages compared to traditional ones:

- The phosphorus doped polysilicon gate traps free sodium ions providing **ultra stable drift-free input MOS transistors.**
- Self aligned gate reduces **the gate-drain capacitance** and meanwhile **increases the speed** of the MOS transistors.

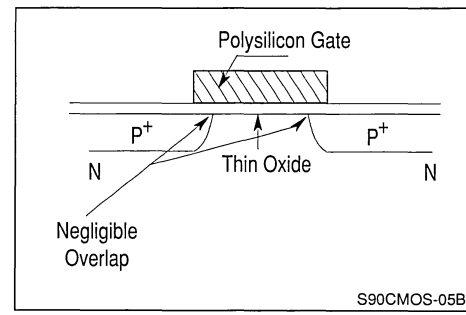
2. SELF ALIGNED GATE

Figure 2A : Drain/source diffusion is made **before** the gate's etching.



These figures illustrate the differences between metal gate and polysilicon gate MOS transistors. The overlap which causes capacitance is considerably reduced and becomes negligible.

Figure 2B : Drain/source diffusion is made **after** the gate's etching.
The gate is used as a mask during the diffusion.



The self aligned polysilicon gate reduces the parasitic capacitance of the structure and also reduces the number of critical mask alignments which leads to cost reduction.

CMOS OPERATIONAL AMPLIFLIERS

TS271 - TS27X2 series - TS27X4 series

FEATURES	BENEFITS
• VOLTAGE RANGE FROM 3 to 16V (MAX=18V)	• ALLOWS DESIGN IN WIDE APPLICATION RANGE (FROM BATTERY OPERATION TYPE UP TO USUAL 12V SUPPLY VOLTAGE TYPE)
• SINGLE SUPPLY VOLTAGE	• AVOIDS NEGATIVE TYPE POWER SUPPLY
• ADAPTABLE BIAS CURRENT	• ALLOWS BEST CONSUMPTION/SPEED RATIO (COST EFFECTIVENESS)
• EXTREMELY LOW INPUT CURRENT (1pA)	• MINIMIZES STATIC ERROR IN LOW IMPEDANCE APPLICATIONS
• OFFSET VOLTAGE STABILITY (0.7µV/°C)	• ANSWERS TO INSTRUMENTATION MARKET NEEDS WITH GENERAL PURPOSE TYPE PRICING
• ADAPTABLE BANDWITH AND SLEW RATE **TS27LX** / **TS27MX** / **TS27X** / **UNIT** **Svo**: 0.04 / 0.6 / 5.5 / V/µs **GBP**: 0.1 / 1 / 3.5 / MHz	• MORE PERFORMANCE REGARDING TO CONSUMPTION (0.35 MHz/mW) ALLOWS SMALL SIZE POWER SUPPLY, LESS HEAT DISSIPATION, HIGHER RELIABILITY
• DYNAMIC BEHAVIOUR - TS271 / TS272 / TS274 - TS271 / TS27M2 / TS27M4	• EASY REPLACEMENT OF – JFET OPERATIONAL AMPLIFIERS FAMILY – BIPOLAR OPERATIONAL AMPLIFIERS FAMILY WITH BETTER BEHAVIOUR
• SYMETRICAL OUTPUT CURRENTS	• ALLOWS USE OF SAME LOADS ON BOTH SIDES OF THE OUTPUT
• LOW OUTPUT DYNAMIC IMPEDANCE	• REDUCES SETTLING TIME
• LINEARITY OF THE TRANSFERT FUNCTION (IN SINGLE OR DUAL POWER SUPPLY UTILISATION)	• LOWERS GAIN DISPERSION IN OPEN-LOOP OPERATION MODE
• EXCELLENT PHASE MARGIN (DUE TO INTERNAL COMPENSATION)	• IMPROVES THE STABILITY FOR HIGH CAPACITANCE LOAD (MORE THAN 100pF)
• OFFSET NULL CAPABILITY (TS271)	• MINIMIZES STATIC ERROR (WHEN USED IN COMPARATOR MODE)
• LARGE AND CONTINUOUS PROGRAMMATION RANGE (FROM 1µA UP TO 200µA) (TS271)	• ALLOWS HIGH OPTIMISATION FOR ALL TYPES OF APPLICATIONS

LOW POWER CMOS COMPARATORS

TS372 - TS374

FEATURES	BENEFITS
• SINGLE or DUAL SUPPLY OVER A WIDE RANGE **(3 to 16 V or ± 1.5 to ± 8V)**	• WIDE APPLICATION RANGE BATTERY OPERATION ABILITY
• VERY LOW SUPPLY CURRENT : **150 µA** / comparator	• POWER SAVING HALF OF LM339
• FAST RESPONSE TIME : **200 ns** WITH TTL INPUT	• 1.5× LM339 SPEED
• VERY LOW INPUT BIAS CURRENT Typ : **1pA**	• MINIMIZED STATIC ERROR
• LM393 - LM339 PIN to PIN COMPATIBLE	• EASY OF UPGRADE IN REDESIGN
• OPEN DRAIN CMOS OUTPUT	• LOGIC "AND" / "OR" FUNCTION POSSIBILITY

MICROPOWER CMOS COMPARATORS

TS393 - TS339

FEATURES	BENEFITS
• SINGLE or DUAL SUPPLY OVER A WIDE RANGE **(3 to 16 V or ± 1.5 to ± 8V)**	• WIDE APPLICATION RANGE BATTERY OPERATION ABILITY
• EXTREMELY LOW SUPPLY CURRENT : **10 µA** / Comparator	• 20 TIMES LESS THAN BIPOLAR LM339/393
• FAST RESPONSE TIME : **1.1 µS** WITH TTL INPUT	• CONSUMPTION / SPEED RATIO OPTIMISATION
• VERY LOW INPUT BIAS CURRENT Typ : **1pA**	• MINIMIZED STATIC ERROR
• LM393 / 399 PIN TO PIN COMPATIBLE	• EASY OF UPGRADE IN REDESIGN
• OPEN DRAIN CMOS OUTPUT	• LOGIC "AND" / "OR" FUNCTION POSSIBILITY

TS3702 - TS3704

FEATURES	BENEFITS
• SINGLE or DUAL SUPPLY OVER A WIDE RANGE **(3 to 16 V or ± 1.5 to ± 8V)**	• WIDE APPLICATION RANGE BATTERY OPERATION ABILITY
• EXTREMELY LOW SUPPLY CURRENT : **10 µA** / Comparator	• 20 TIMES LESS THAN BIPOLAR LM339/393
• FAST RESPONSE TIME : **1.1 µs** WITH TTL INPUT	• CONSUMPTION / SPEED RATIO OPTIMISATION
• VERY LOW INPUT BIAS CURRENT Typ : **1pA**	• MINIMIZED STATIC ERROR
• LM393 / 399 PIN TO PIN COMPATIBLE	• EASY OF UPGRADE IN REDESIGN
• PUSH PULL CMOS OUTPUT	• NO EXTERNAL PULL UP RESISTOR REQUIRED

CMOS TIMERS

TS555 - TS556

FEATURES	BENEFITS
• SINGLE SUPPLY OVER A WIDE RANGE **2 to 16V**	• WIDE APPLICATION RANGE
• VERY LOW SUPPLY CURRENT : **100 µA** typ. / Timer	• 30 TIMES LESS THAN BIPOLAR NE555/6
• VERY HIGH SPEED **2.7 MHz max. ASTABLE FREQUENCY**	• 30 TIMES FASTER THAN BIPOLAR NE555/6
• NE555 / NE556 PIN-TO-PIN COMPATIBLE	• EASE OF UPGRADE IN REDESIGN
• SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS	• LOWER DECOUPLING CAPACITORS REQUIRED

CMOS CROSS REFERENCE

1 - CMOS OPERATIONAL AMPLIFLIERS

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC271ACD	TS271ACD
TLC271ACP	TS271ACN
TLC271AID	TS271AID
TLC271AIP	TS271AIN
TLC271BCD	TS271BCD
TLC271BCP	TS271BCN
TLC271BID	TS271BID
TLC271BIP	TS271BIN
TLC271CD	TS271CD
TLC271CP	TS271CN
TLC271ID	TS271ID
TLC271IP	TS271IN
TLC272ACD	TS272ACD
TLC272ACP	TS272ACN
TLC272AID	TS272AID
TLC272AIP	TS272AIN
TLC272BCD	TS272BCD
TLC272BCP	TS272BCN
TLC272BID	TS272BID
TLC272BIP	TS272BIN
TLC272CD	TS272CD
TLC272CP	TS272CN
TLC272ID	TS272ID
TLC272IP	TS272IN
TLC274ACD	TS274ACD
TLC274ACN	TS274ACN
TLC274AID	TS274AID

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC274AIN	TS274AIN
TLC274BCD	TS274BCD
TLC274BCN	TS274BCN
TLC274BID	TS274BID
TLC274BIN	TS274BIN
TLC274CD	TS274CD
TLC274CN	TS274CN
TLC274ID	TS274ID
TLC274IN	TS274IN
TLC27L2ACD	TS27L2ACD
TLC27L2ACP	TS27L2ACN
TLC27L2AID	TS27L2AID
TLC27L2AIP	TS27L2AIN
TLC27L2BCD	TS27L2BCD
TLC27L2BCP	TS27L2BCN
TLC27L2BID	TS27L2BID
TLC27L2BIP	TS27L2BIN
TLC27L2CD	TS27L2CD
TLC27L2CP	TS27L2CN
TLC27L2ID	TS27L2ID
TLC27L2IP	TS27L2IN
TLC27L4ACD	TS27L4ACD
TLC27L4ACN	TS27L4ACN
TLC27L4AID	TS27L4AID
TLC27L4AIN	TS27L4AIN
TLC27L4BCD	TS27L4BCD
TLC27L4BCN	TS27L4BCN

1 - CMOS OPERATIONAL AMPLIFLIERS (continued)

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC27L4BID	TS27L4BID
TLC27L4BIN	TS27L4BIN
TLC27L4CD	TS27L4CD
TLC27L4CN	TS27L4CN
TLC27L4ID	TS27L4ID
TLC27L4IN	TS27L4IN
TLC27M2ACD	TS27M2ACD
TLC27M2ACP	TS27M2ACN
TLC27M2AID	TS27M2AID
TLC27M2AIP	TS27M2AIN
TLC27M2BCD	TS27M2BCD
TLC27M2BCP	TS27M2BCN
TLC27M2BID	TS27M2BID
TLC27M2BIP	TS27M2BIN
TLC27M2CD	TS27M2CD

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC27M2CP	TS27M2CN
TLC27M2ID	TS27M2ID
TLC27M2IP	TS27M2IN
TLC27M4ACD	TS27M4ACD
TLC27M4ACN	TS27M4ACN
TLC27M4AID	TS27M4AID
TLC27M4AIN	TS27M4AIN
TLC27M4BCD	TS27M4BCD
TLC27M4BCN	TS27M4BCN
TLC27M4BID	TS27M4BID
TLC27M4BIN	TS27M4BIN
TLC27M4CD	TS27M4CD
TLC27M4CN	TS27M4CN
TLC27M4ID	TS27M4ID
TLC27M4IN	TS27M4IN

NATIONAL SEMICONDUCTOR	SGS-THOMSON REPLACEMENT
LMC660CN	TS27M4ACN
LMC660AIN	TS27M4BIN
LMC660CM	TS27M4ACD
LMC660AIM	TS27M4BID

NATIONAL SEMICONDUCTOR	SGS-THOMSON REPLACEMENT
LMC662CN	TS27M2ACN
LMC662AIN	TS27M2BIN
LMC662CM	TS27M2ACD
LMC662AIM	TS27M2BID

2 - CMOS COMPARATORS

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC372CD	TS372CD
TLC372CP	TS372CN
TLC372ID	TS372ID
TLC372IP	TS372IN

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC374CD	TS374CD
TLC374CN	TS374CN
TLC374ID	TS374ID
TLC374IN	TS374IN

2 - CMOS COMPARATORS (continued)

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC3702CD	TS3702CD
TLC3702CP	TS3702CN
TLC3702ID	TS3702ID
TLC3702IP	TS3702IN
TLC3704CD	TS3704CD
TLC3704CN	TS3704CN
TLC3704ID	TS3704ID
TLC3704IN	TS3704IN

TEXAS INSTRUMENTS	SGS-THOMSON REPLACEMENT
TLC339CD	TS339CD
TLC339CN	TS339CN
TLC339ID	TS339ID
TLC339IN	TS339IN
TLC393CD	TS393CD
TLC393CP	TS393CN
TLC393ID	TS393ID
TLC393IP	TS393IN

3 - CMOS TIMERS

NATIONAL SEMICONDUCTOR	SGS-THOMSON REPLACEMENT
LMC555CM	TS555CD
LMC555CN	TS555CN

SIGNETICS	SGS-THOMSON REPLACEMENT
ICM7555CD	TS555CD
ICM7555CN	TS555CN
ICM7555ID	TS555ID
ICM7555IN	TS555IN

TEXAS INSTRUMENT	SGS-THOMSON REPLACEMENT
TLC555CD	TS555CD
TLC555CP	TS555CN
TLC555ID	TS555ID
TLC555IP	TS555IN
TLC556CD	TS556CD
TLC556CN	TS556CN
TLC556ID	TS556ID
TLC556IN	TS556IN

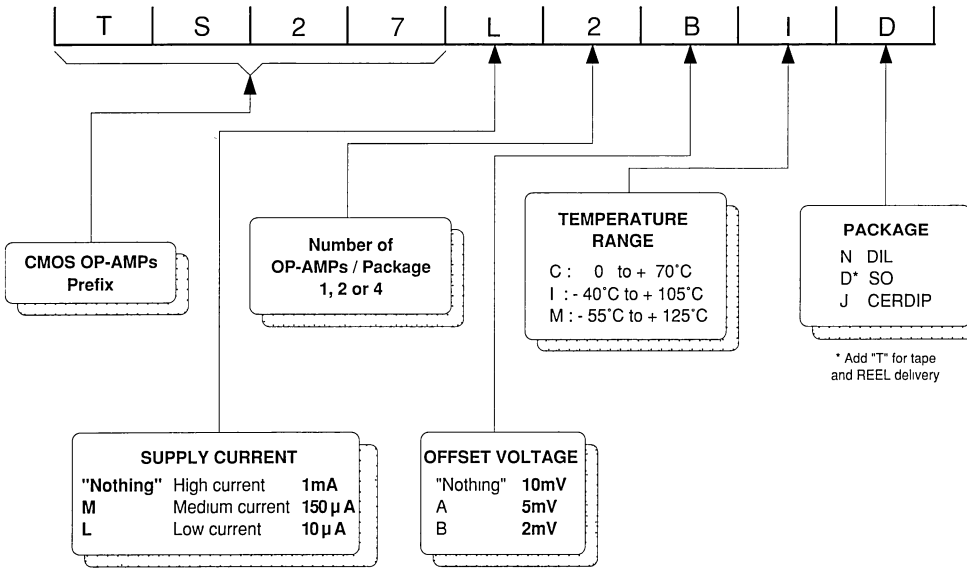
INTERSIL	SGS-THOMSON REPLACEMENT
ICM7555CBA	TS555CD
ICM7555IPA	TS555IN
ICM7556IPD	TS556IN

NEC	SGS-THOMSON REPLACEMENT
µPD5555C	TS555CN
µPD555G2	TS555CD
µPD5556C	TS556CN
µPD5556G2	TS556CD

SAMSUNG	SGS-THOMSON REPLACEMENT
KS555D	TS555ID
KS555N	TS555IN
KS555HD	TS555CD
KS555HN	TS555CN
KS556D	TS556CD
KS556N	TS556CN

CMOS ORDERING INFORMATION

1 - CMOS OPERATIONAL AMPLIFLIERS



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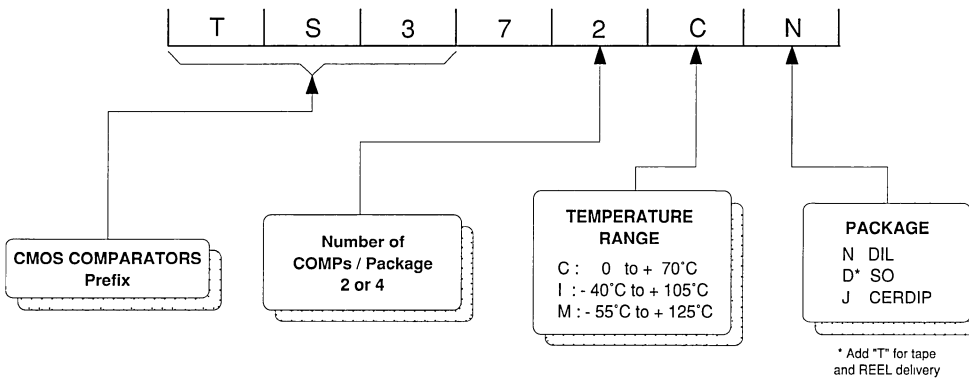
2 - CMOS COMPARATORS



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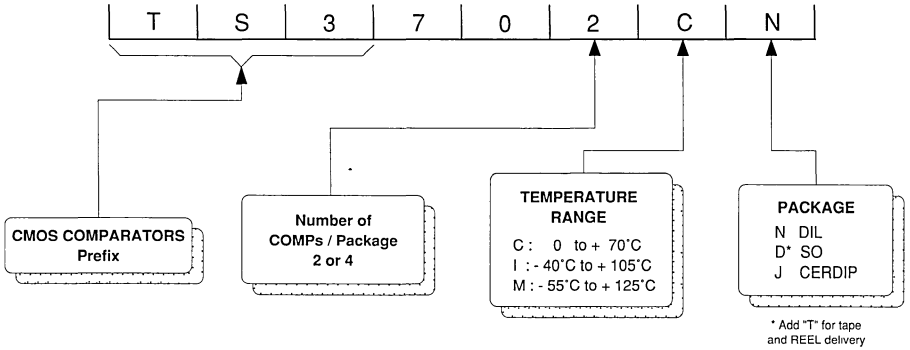
2 - CMOS COMPARATORS (continued)



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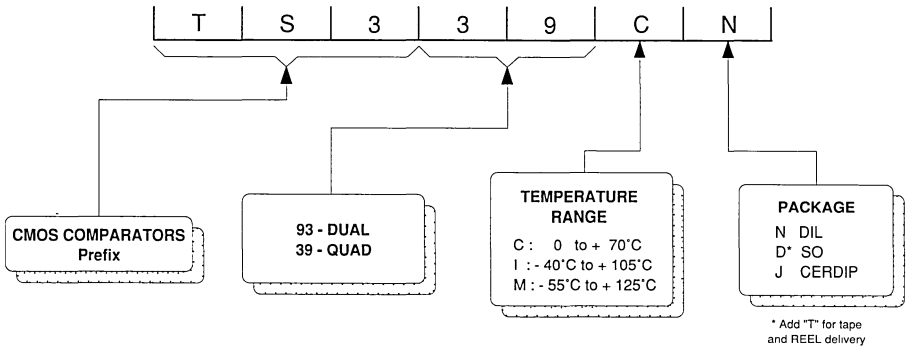

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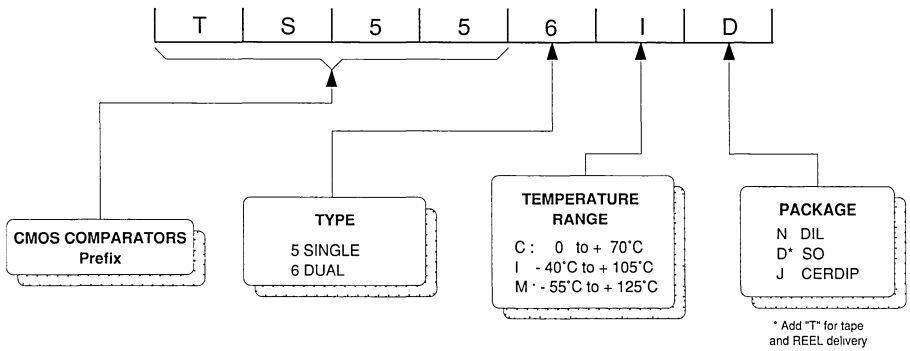
3 - CMOS TIMERS



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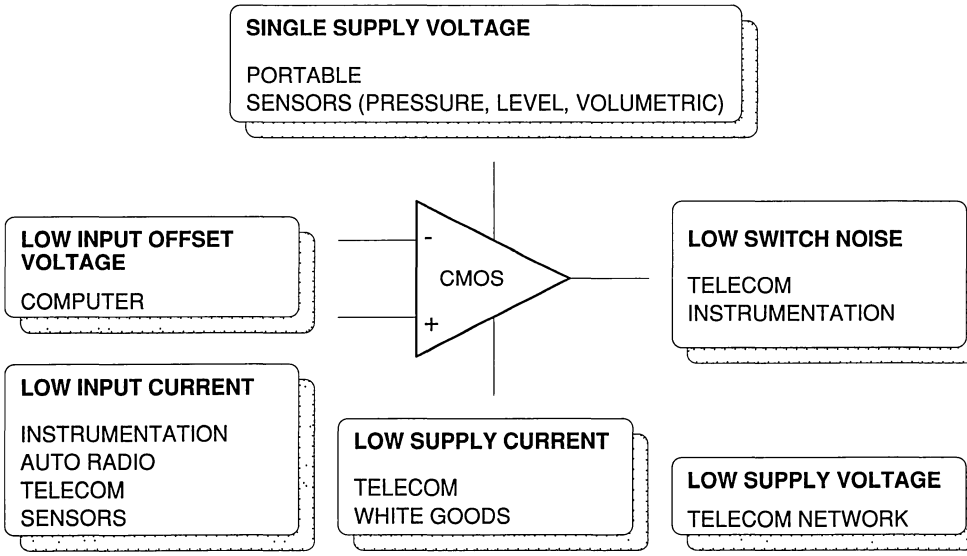
APPLICATIONS



S90CMOS-11

MULTI SEGMENT POSITION

TELECOM	SUBSCRIBER CARD (FILTER), EXCHANGE BOARD, MOBILE PHONE...
CONSUMER	VCR, TV SET, CD PLAYER WHITE MARKET AND TOYS...
AUTOMOTIVE	INJECTION CONTROL, ABS, CAR RADIO...
COMPUTER	PERIPHERALS, DISK DRIVE...
INDUSTRIAL	ELECTRICITY, GAZ AND WATER METERING, TEMPERATURE SENSORS...

SELECTION GUIDE

CMOS OPERATIONAL AMPLIFIERS

Characteristics specified at V_{CC} = +10V, T_{AMB} = +25°C

Type	Configuration	Main Feature	Single Supply	Operating Voltage Range (V)	Supply Current Typ/amp (mA)	Input Offset Voltage Max (mV)	Gain Bandwidth Product Typ (MHz)	Slew Rate Typ (V/µs)
TS271	Single	Programmable	Yes	3* to 16	0.01 to 0.8	10	0.1 to 2.5	0.04 to 4.5
TS271A	Single	Programmable	Yes	3* to 16	0.01 to 0.8	5	0.1 to 2.5	0.04 to 4.5
TS271B	Single	Programmable	Yes	3* to 16	0.01 to 0.8	2	0.1 to 2.5	0.04 to 4.5
TS27L2	Dual	Very Low Power	Yes	3* to 16	0.01	10	0.1	0.04
TS27L2A	Dual	Very Low Power	Yes	3* to 16	0.01	5	0.1	0.04
TS27L2B	Dual	Very Low Power	Yes	3* to 16	0.01	2	0.1	0.04
TS27M2	Dual	Low Power	Yes	3* to 16	0.15	10	1	0.6
TS27M2A	Dual	Low Power	Yes	3* to 16	0.15	5	1	0.6
TS27M2B	Dual	Low Power	Yes	3* to 16	0.15	2	1	0.6
TS272	Dual	High Speed	Yes	3* to 16	1.0	10	3.5	5.5
TS272A	Dual	High Speed	Yes	3* to 16	1.0	5	3.5	5.5
TS272B	Dual	High Speed	Yes	3* to 16	1.0	2	3.5	5.5
TS27L4	Quad	Very Low Power	Yes	3* to 16	0.01	10	0.1	0.04
TS27L4A	Quad	Very Low Power	Yes	3* to 16	0.01	5	0.1	0.04
TS27L4B	Quad	Very Low Power	Yes	3* to 16	0.01	2	0.1	0.04
TS27M4	Quad	Low Power	Yes	3* to 16	0.15	10	1	0.6
TS27M4A	Quad	Low Power	Yes	3* to 16	0.15	5	1	0.6
TS27M4B	Quad	Low Power	Yes	3* to 16	0.15	2	1	0.6
TS274	Quad	High Speed	Yes	3* to 16	1.0	10	3.5	5.5
TS274A	Quad	High Speed	Yes	3* to 16	1.0	5	3.5	5.5
TS274B	Quad	High Speed	Yes	3* to 16	1.0	2	3.5	5.5

* For selected devices only.

CMOS COMPARATORS

Characteristics specified at V_{CC} = +5V, T_{AMB} = +25°C

Type	Configuration	Main Feature	Single Supply	Operating Voltage Range (V)	Supply Current Typ/comp (mA)	Input Offset Voltage Max (mV)	Response Time (Typ) (with overdrive = 5mV) (ns)	Output Type
TS372	Dual	Low Power	Yes	3* to 16	150	10	600	Open Drain
TS374	Quad	Low Power	Yes	3* to 16	150	10	600	Open Drain
TS393	Dual	Micro Power	Yes	3* to 16	9	5	2100	Open Drain
TS339	Quad	Micro Power	Yes	3* to 16	9	5	2100	Open Drain
TS3702	Dual	Micro Power	Yes	3* to 16	9	5	2300	Push-Pull
TS3704	Quad	Micro Power	Yes	3* to 16	9	5	2300	Push-Pull

* For selected devices only.

CMOS TIMERS

Characteristics specified at V_{CC} = +5V, T_{AMB} = +25°C

Type	Configuration	Main Feature	Single Supply	Operating Voltage Range (V)	Supply Current Typ/Timer (mA)	Max Frequency Astable Mode (MHz)
TS555	Single	Low Power	Yes	2 to 16	100	2.7
TS556	Dual	Low Power	Yes	2 to 16	100	2.7

OPERATIONAL AMPLIFIERS CMOS versus BIPOLAR & JFET

Characteristics specified at T_{AMB} = +25°C

TS271 versus COMPETITIVE SINGLE OPERATIONAL AMPLIFIERS

Type	Technology	Main Feature	Single Supply	Operating Voltage Max (V)	Supply Current Typ (mA)	Adjustable	Input Offset Voltage Max (mV)	Bandwidth (MHz)	Slew Rate (V/µs)
LF355	JFET	General Purpose	No	± 18	2	Offset	10	2.5	5
TL061	JFET	Low Power	No	± 18	0.2	Offset	15	1	3.5
TL071	JFET	Low Noise	No	± 18	1.4	Offset	8	4	16
TL081	JFET	General Purpose	No	± 18	1.4	Offset	8	4	16
TS27	C MOS	Program mable	Yes	± 18	0.01 0.3	Offset	2 5 10	0 1 to 2 5	0.07 to 4
LM301A	Bipolar	General Purpose	No	± 18	1.8	Offset Frequency	5	1	0.5
LM308A	Bipolar	Precision	No	± 18	0.3	Offset Frequency	0.5	0.8	0.15
LM318	Bipolar	Ultra-fast	No	± 20	5	Offset	10	15	70
TDB7910	Bipolar	Power	Yes	± 18	10	Offset Frequency	6	1	0.5
UA741	Bipolar	General Purpose	No	± 18	1.7	Offset	5	1	0.5
UA748	Bipolar	General Purpose	No	± 18	1.8	Offset Frequency	5	1	0.5
UA776	Bipolar	Program mable	No	± 18	0.02-0.16	Offset	5	0.01 to 1	0 03 to 0 8

TS27x2 versus COMPETITIVE DUAL OPERATIONAL AMPLIFIERS

Type	Technology	Main Feature	Single Supply	Operating Voltage Max (V)	Supply Current (per amplifier) Typ (mA)	Input Offset Voltage Max (mV)	Bandwidth (MHz)	Slew Rate (V/µs)
TL062	JFET	Low Power	No	± 18	0.2	15	1	3.5
TL072	JFET	Low Noise	No	± 18	1.4	8	4	16
TL082	JFET	General Purpose	No	± 18	1.4	8	4	16
TS272	C-MOS	Low Power	Yes	+ 16	0.01 to 1	2, 5, 10	0.1 to 3.5	0.1 to 5
LM2904	Bipolar	Low Power	Yes	± 16 or 32	0.3	5	1.1	0.6
LM358	Bipolar	Low Power	Yes	± 16 or 32	0.3	5	1.1	0.6
LS204	Bipolar	High Performance	No	± 18	0.4	3.5	2.5	1
MC1458	Bipolar	General Purpose	No	± 18	1.6	5	1	0.8
MC4558	Bipolar	Wide Band	No	± 18	1.6	5	5.5	2.2
TEB1033	Bipolar	High Stability	No	± 18	0.5	1	2.5	1

TS27x4 versus COMPETITIVE QUAD OPERATIONAL AMPLIFIERS

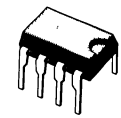
Type	Technology	Main Feature	Single Supply	Operating Voltage Max (V)	Supply Current (per amplifier) Typ (mA)	Input Offset Voltage Max (mV)	Bandwidth (MHz)	Slew Rate (V/µs)
TL064	JFET	Low Power	No	± 18	0.2	15	1	3.5
TL074	JFET	Low Noise	No	± 18	1.4	8	4	16
TL084	JFET	General Purpose	No	± 18	1.4	8	4	16
TS274	C-MOS	Low Power	Yes	+ 16	0.01 to 1	2, 5, 10	0.1 to 3.5	0.1 to 5
LM2902	Bipolar	Low Power	Yes	± 16 or 32	0.3	5	1.3	0.4
LM324	Bipolar	Low Power	Yes	± 16 or 32	0.3	5	1.3	0.4
LM346	Bipolar	Programmable	No	± 18	0.25	3	1	0.5
LM348	Bipolar	Differential Output	No	± 18	0.5	5	1.3	0.5
LS404	Bipolar	High Performance	No	± 18	0.4	3.5	2.5	1
MC3403	Bipolar	Differential Output	Yes	± 18 or 36	0.7	5	1	0.6
TEB4033	Bipolar	High Stability	No	± 18	0.5	1	2.5	1

DATASHEETS

OPERATIONAL AMPLIFLIERS

PROGRAMMABLE SINGLE CMOS OP-AMPs

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{SET}
- VERY LARGE I_{SET} RANGE
- PIN TO PIN COMPATIBLE WITH SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS271C/AC/BC	0°C to + 70°C	•	•	•
TS271I/AI/BI	- 40°C to + 105°C	•	•	•
TS271M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS271ACN				

DESCRIPTION

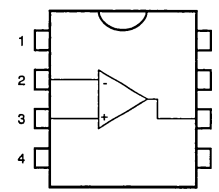
The TS271 is low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifiers uses the SGS-THOMSON silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the required speed. These devices are specified for the following I_{SET} current values : 1.5µA, 25µA, 130µA.

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

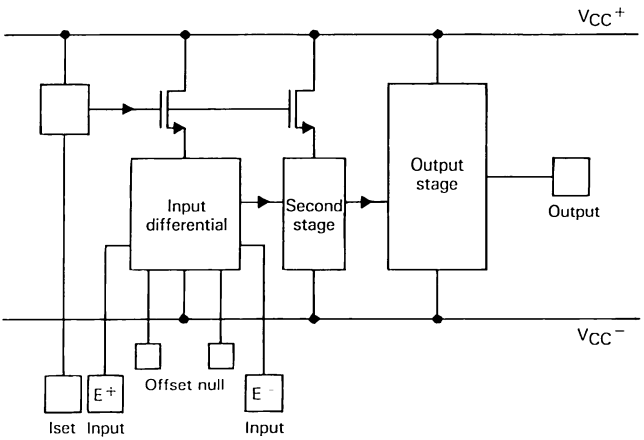
DIP8 - CERDIP 8 - SO8



1 - Offset Null
2 - Inverting Input
3 - Non-inverting Input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - I_{SET}

S90TS271-01

BLOCK DIAGRAM



S90TS271-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS271C/AC/BC TS271I/AI/BI TS271M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

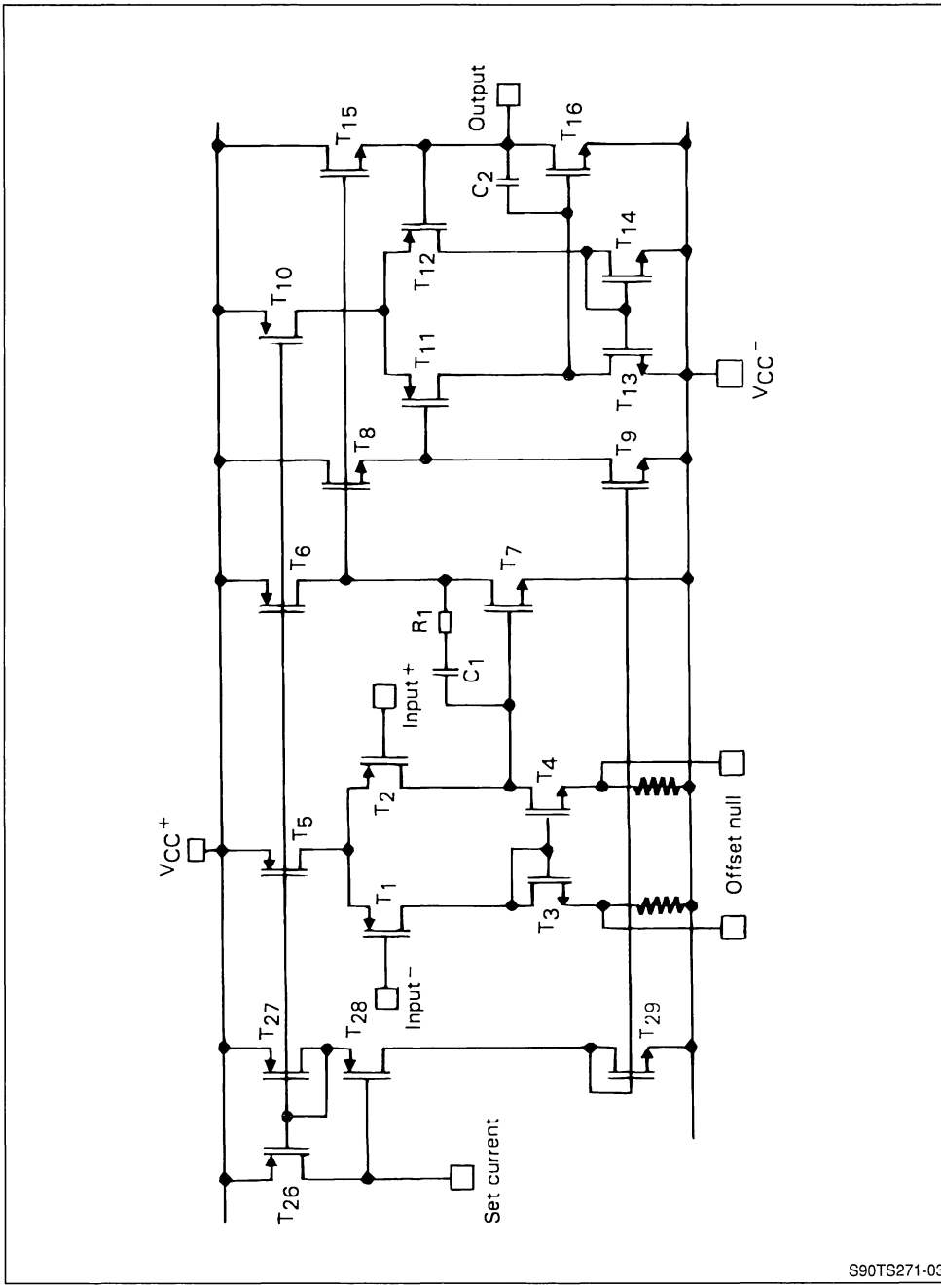
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage

OPERATING CONDITIONS

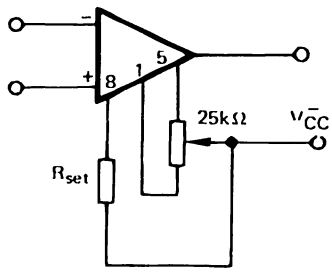
Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only

SCHEMATIC DIAGRAM



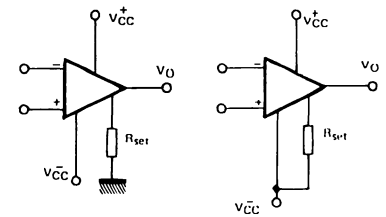
OFFSET VOLTAGE NULL CIRCUIT



S90TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{SET} > 25µA), TS271ACX (I_{SET}> 90µA)

RESISTOR BIASING

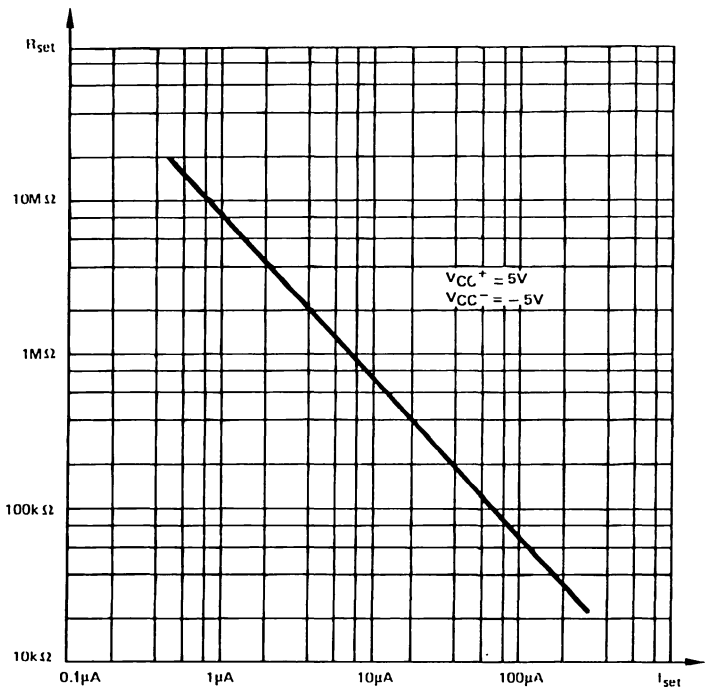


S90TS271-05

R_{SET} CONNECTED TO GROUND

R_{SET} CONNECTED TO V_{CC}^- (R_{SET} VALUE :SEE FIG.1)

Figure 1 : R_{SET} Connected to V_{CC}^-.



S90TS271-06

ELECTRICAL CHARACTERISTICS FOR I_{SET} = 1.5µA

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter		TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage								mV
	V_O = 1.4V, V_i = 0V	TS271C/I/M		1.1	10		1.1	10	
		TS271AC/AI/AM		0.9	5		0.9	5	
		TS271BC/BI/BM		0.25	2		0.25	2	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	TS271C/I/M			12			12	
		TS271AC/AI/AM			6.5			6.5	
		TS271BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift			0.7			0.7		µV/°C
I_{io}	Input Offset Current								pA
	V_i = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				100			200	
I_{ib}	Input Bias Current								pA
	V_i = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				150			300	
V_{OH}	High Level Output Voltage								V
	V_i = 10mV, R_L = 1MΩ		8.8	9		8.8	9		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		8.7			8.6			
V_{OL}	Low Level Output Voltage (Vi = - 10mV)				50			50	mV
A_{vd}	Large Signal Voltage Gain								V/mV
	V_o = 1V to 6V, R_L = 1MΩ, V_i = 5V		30	100		30	100		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		20			20			
GBP	Gain Bandwidth Product (A_v = 40dB,								MHz
	R_L = 1MΩ, C_L = 100pF, f_{in} = 10 kHz)			0.1			0.1		
CMR	Common Mode Rejection Ratio								dB
	V_o = 1.4V, V_i = 1V to 7.4V		60	80		60	80		
SVR	Supply Voltage Rejection Ratio								dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V		60	80		60	80		
I_{CC}	Supply Current (per amplifier)								µA
	A_v = 1, no load, V_o = 5V			10	15		10	15	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				17			18	
I_o	Output Short Circuit Current								mA
	V_i = 10mV, V_o = 0V		45	60	85	45	60	85	
I_{sink}	Output Sink Current								mA
	Vi = - 10mV, V_o = V_{CC}		35	45	65	35	45	65	
S_{vo}	Slew-Rate at Unity Gain								V/µs
	R_L = 1MΩ, C_L= 100pF			0.04			0.04		
Ø m	Phase Margin at Unity Gain								degrees
	A_v = 40 dB, R_L = 1MΩ								
		C_L= 10pF		35			35		
		C_L= 100pF		10			10		
K_{ov}	Overshoot Factor								%
		C_L = 10pF		40			40		
		C_L = 100pF		70			70		
V_n	Equivalent Input Noise Voltage								nV/√Hz
	f = 1kHz, R_S = 10Ω			68			68		

TYPICAL CHARACTERISTICS FOR I_{SET} = 1.5µA

Figure 2 : Supply Current (each amplifier) versus Supply Voltage.

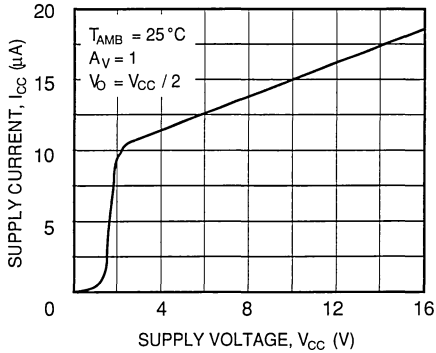


Figure 3 : Input Bias Current versus Free Air Temperature.

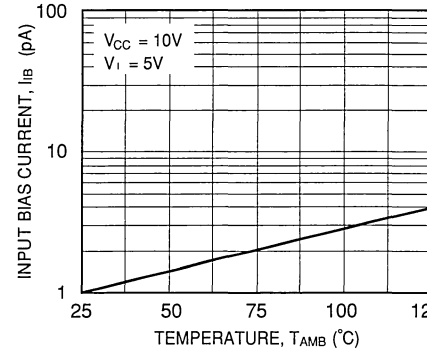


Figure 4a : High Level Output Voltage versus High Level Output Current.

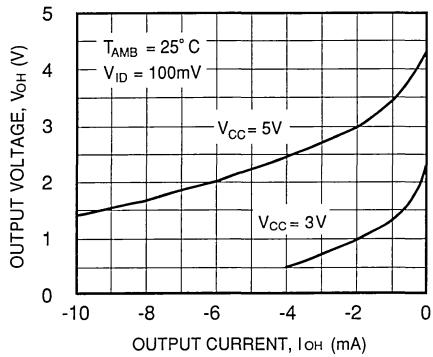


Figure 4b : High Level Output Voltage versus High Level Output Current.

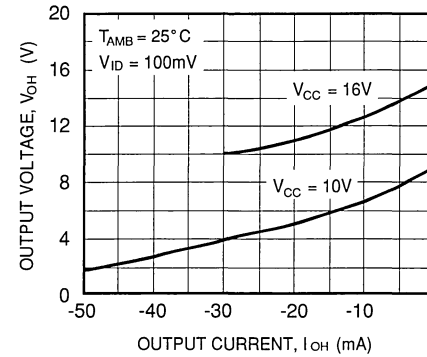


Figure 5a : Low Level Output Voltage versus Low Level Output Current.

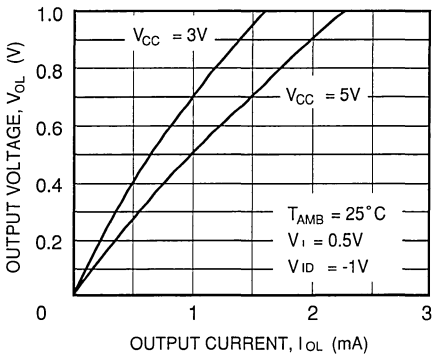
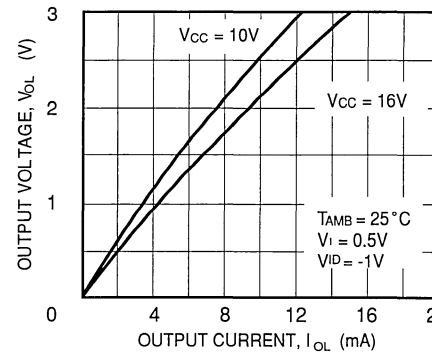


Figure 5b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 1.5µA (continued)

Figure 6 : Open Loop Frequency Response and Phase Shift.

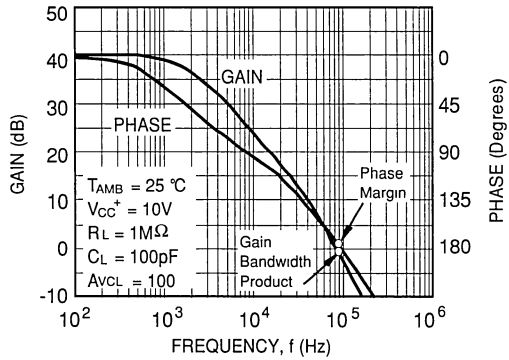


Figure 7 : Gain Bandwidth Product versus Supply Voltage.

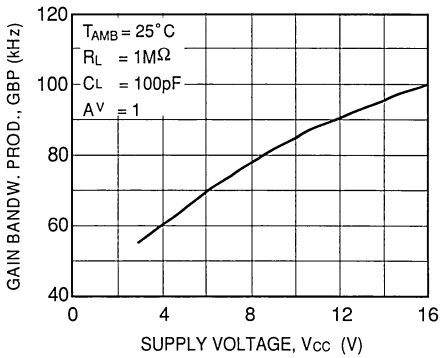


Figure 8 : Phase Margin versus Supply Voltage.

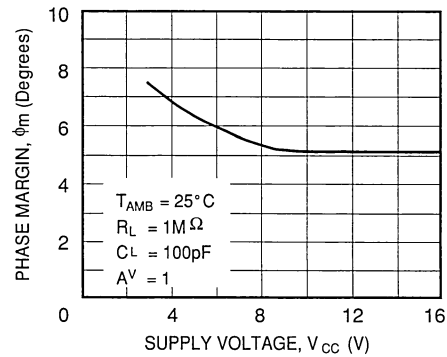


Figure 9 : Phase Margin versus Capacitive Load.

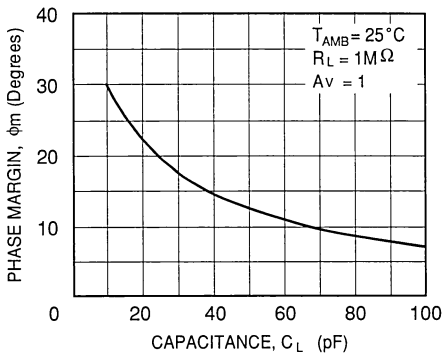
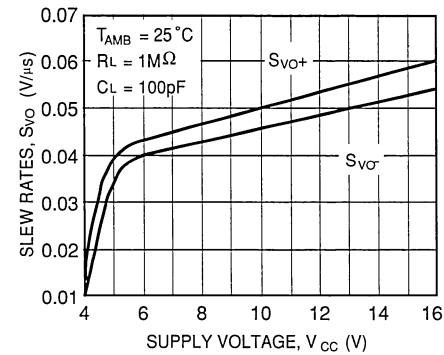


Figure 10 : Slew Rates versus Supply Voltage.



ELECTRICAL CHARACTERISTICS FOR I_{SET} = 25µA

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage							mV
	V_O = 1.4V, V_i = 0V TS271C/I/M		1.1	10		1.1	10	
	TS271AC/AI/AM		0.9	5		0.9	5	
	TS271BC/BI/BM		0.25	2		0.25	2	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$ TS271C/I/M			12			12	
	TS271AC/AI/AM			6.5			6.5	
	TS271BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current							pA
	V_i = 5V, V_o = 5V		1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$			100			200	
I_{ib}	Input Bias Current							pA
	V_i = 5V, V_o = 5V		1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$			150			300	
V_{OH}	High Level Output Voltage							V
	V_i = 10mV, R_L = 100kΩ	8.7	8.9		8.7	8.9		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	8.6			8.5			
V_{OL}	Low Level Output Voltage (Vi = - 10mV)			50			50	mV
A_{vd}	Large Signal Voltage Gain							V/mV
	V_o = 1V to 6V, R_L = 100kΩ, V_i = 5V	30	50		30	50		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	20			10			
GBP	Gain Bandwidth Product (A_v = 40dB,							MHz
	R_L = 100kΩ, C_L = 100pF, f_{in} = 100 kHz)		0.7			0.7		
CMR	Common Mode Rejection Ratio							dB
	V_o = 1.4V, V_i = 1V to 7.4V	60	80		60	80		
SVR	Supply Voltage Rejection Ratio							dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	80		60	80		
I_{CC}	Supply Current (per amplifier)							µA
	A_v = 1, no load, V_o = 5V		150	200		150	200	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$			250			300	
I_o	Output Short Circuit Current							mA
	V_i = 10mV, V_o = 0V	45	60	85	45	60	85	
I_{sink}	Output Sink Current							mA
	Vi = - 10mV, V_o = V_{CC}	35	45	65	35	45	65	
S_{vo}	Slew-Rate at Unity Gain							V/µs
	R_L = 100kΩ, C_L= 100pF		0.6			0.6		
Ø m	Phase Margin at Unity Gain							degrees
	A_v = 40 dB, R_L = 100kΩ							
	C_L= 10pF		50			50		
	C_L= 100pF		30			30		
K_{ov}	Overshoot Factor							%
	C_L = 10pF		30			30		
	C_L = 100pF		50			50		
V_n	Equivalent Input Noise Voltage							nV/√Hz
	f = 1kHz, R_S = 10Ω		38			38		

TYPICAL CHARACTERISTICS FOR I_{SET} = 25µA

Figure 11 : Supply Current (each amplifier) versus Supply Voltage.

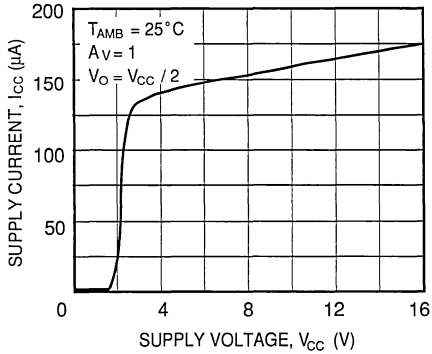


Figure 12 : Input Bias Current versus Free Air Temperature.

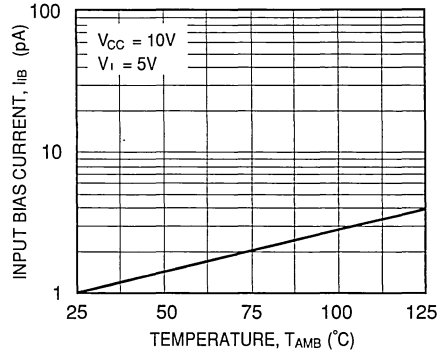


Figure 13a : High Level Output Voltage versus High Level Output Current.

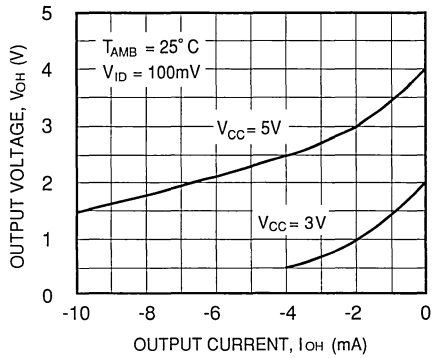


Figure 13b : High Level Output Voltage versus High Level Output Current.

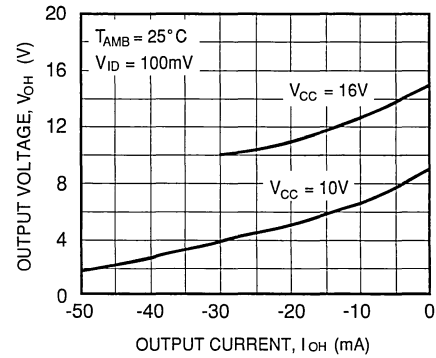


Figure 14a : Low Level Output Voltage versus Low Level Output Current.

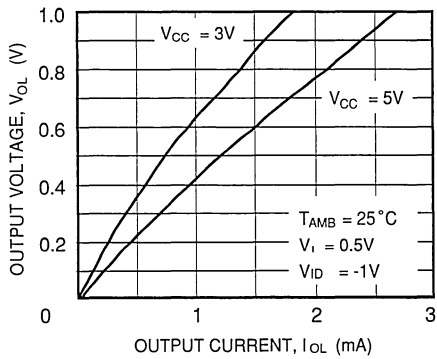
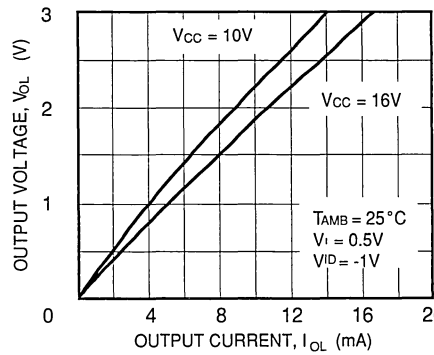


Figure 14b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 25µA (continued)

Figure 15 : Open Loop Frequency Response and Phase Shift.

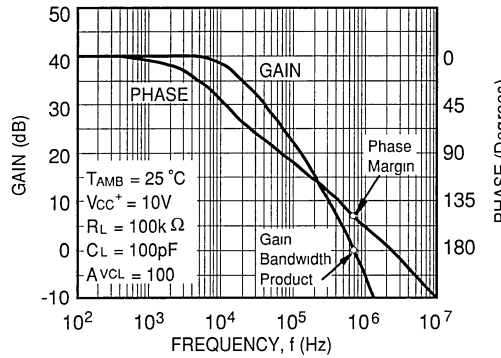


Figure 16 : Gain Bandwidth Product versus Supply Voltage.

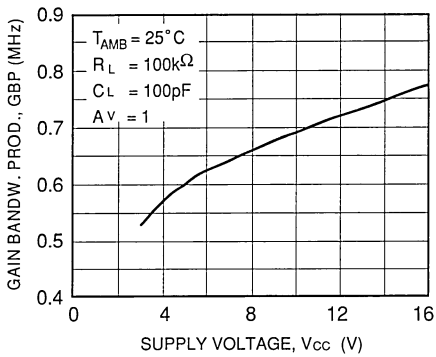


Figure 17 : Phase Margin versus Supply Voltage.

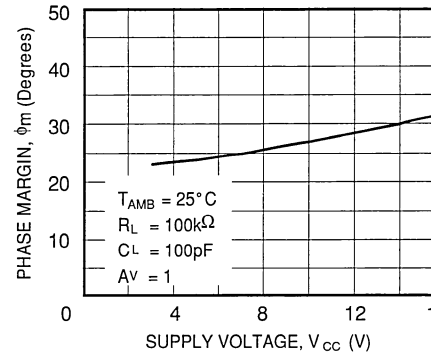


Figure 18 : Phase Margin versus Capacitive Load.

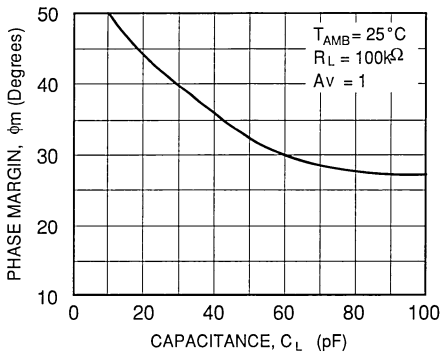
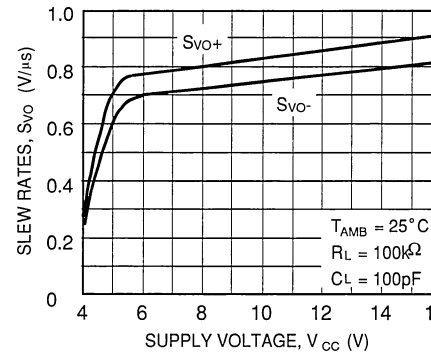


Figure 19 : Slew Rates versus Supply Voltage.



ELECTRICAL CHARACTERISTICS FOR I_{SET} = 130µA

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter		TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage								mV
	V_O = 1.4V, V_I = 0V	TS271C/I/M		1.1	10		1.1	10	
		TS271AC/AI/AM		0.9	5		0.9	5	
		TS271BC/BI/BM		0.25	2		0.25	2	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	TS271C/I/M			12			12	
		TS271AC/AI/AM			6.5			6.5	
		TS271BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift			5			5		µV/°C
I_{io}	Input Offset Current								pA
	V_I = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				100			200	
I_{ib}	Input Bias Current								pA
	V_I = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				150			300	
V_{OH}	High Level Output Voltage								V
	V_I = 10mV, R_L = 10kΩ		8.2	8.4		8.2	8.4		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		8.1			8			
V_{OL}	Low Level Output Voltage (V_I = - 10mV)				50			50	mV
A_{vd}	Large Signal Voltage Gain								V/mV
	V_o = 1V to 6V, R_L = 10kΩ, V_I = 5V		10	15		10	15		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		7			6			
GBP	Gain Bandwidth Product (A_v = 40dB,								MHz
	R_L = 10kΩ, C_L = 100pF, f_{in} = 200 kHz)			2.3			2.3		
CMR	Common Mode Rejection Ratio								dB
	V_o = 1.4V, V_I = 1V to 7.4V		60	80		60	80		
SVR	Supply Voltage Rejection Ratio								dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V		60	70		60	70		
I_{CC}	Supply Current (per amplifier)								µA
	A_v = 1, no load, V_o = 5V			800	1300		800	1300	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				1400			1500	
I_o	Output Short Circuit Current								mA
	V_I = 10mV, V_o = 0V		45	60	85	45	60	85	
I_{sink}	Output Sink Current								mA
	Vi = - 10mV, V_o = V_{CC}		35	45	65	35	45	65	
S_{vo}	Slew-Rate at Unity Gain								V/µs
	R_L = 10kΩ, C_L= 100pF			4.5			4.5		
Ø m	Phase Margin at Unity Gain								degrees
	A_v = 40 dB, R_L = 10kΩ								
		C_L= 10pF		65			65		
		C_L= 100pF		50			50		
K_{ov}	Overshoot Factor								%
		C_L = 10pF		30			30		
		C_L = 100pF		30			30		
V_n	Equivalent Input Noise Voltage								nV/√Hz
	f = 1kHz, R_S = 10Ω			30			30		

TYPICAL CHARACTERISTICS FOR I_{SET} = 130µA

Figure 20 : Supply Current (each amplifier) versus Supply Voltage.

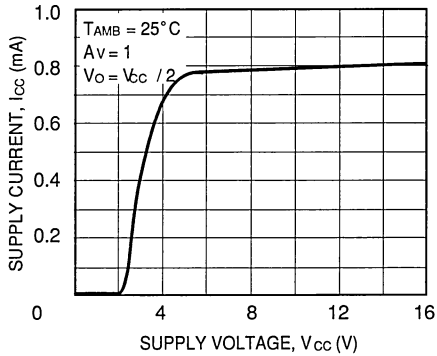


Figure 21 : Input Bias Current versus Free Air Temperature.

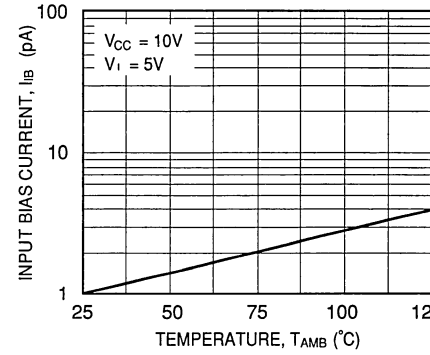


Figure 22a : High Level Output Voltage versus High Level Output Current.

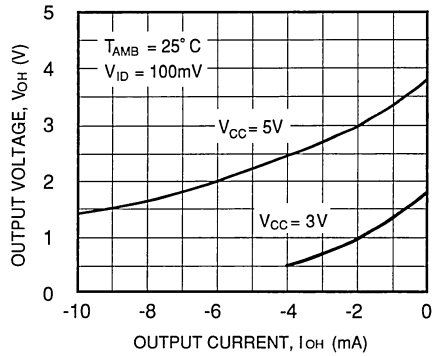


Figure 22b : High Level Output Voltage versus High Level Output Current.

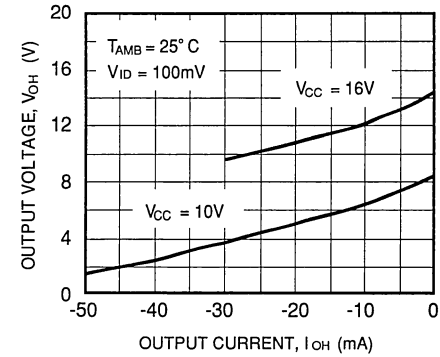


Figure 23a : Low Level Output Voltage versus Low Level Output Current.

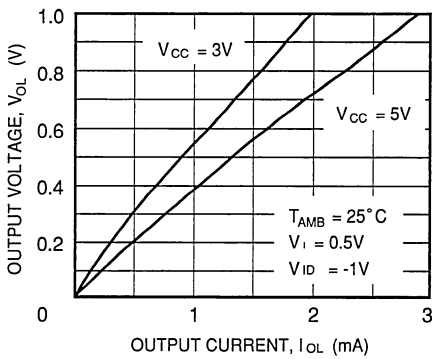
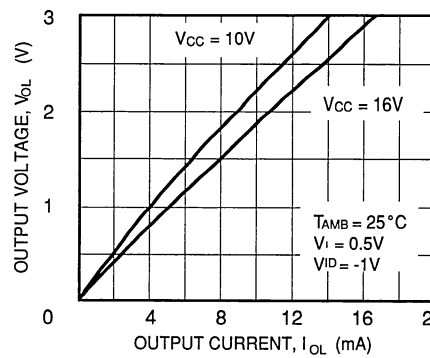


Figure 23b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS FOR I_{SET} = 130µA (continued)

Figure 24 : Open Loop Frequency Response and Phase Shift.

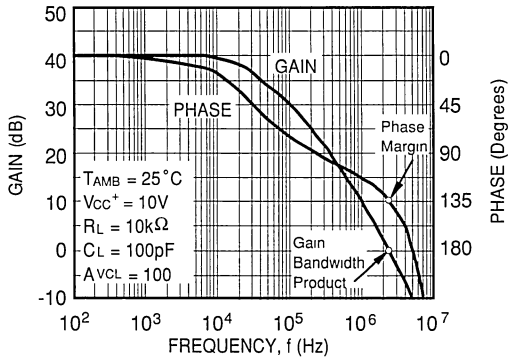


Figure 25 : Gain Bandwidth Product versus Supply Voltage.

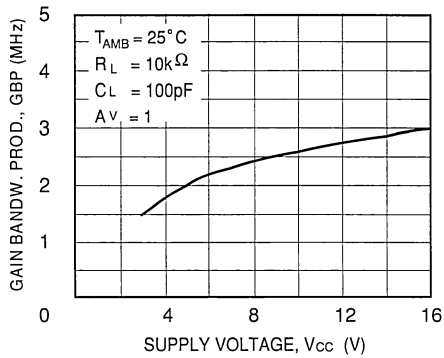


Figure 26 : Phase Margin versus Supply Voltage.

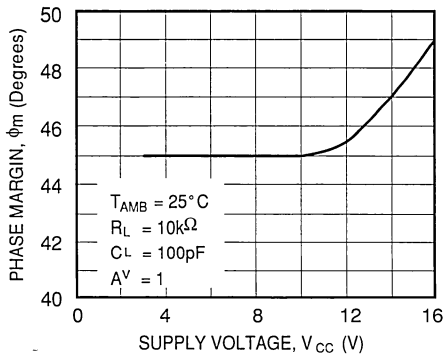


Figure 27 : Phase Margin versus Capacitive Load.

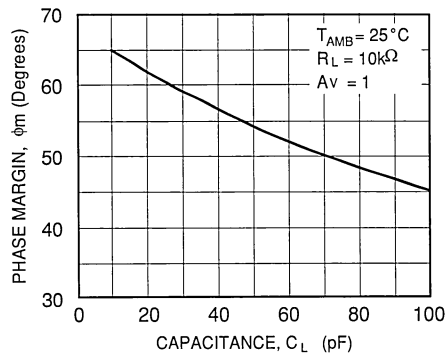
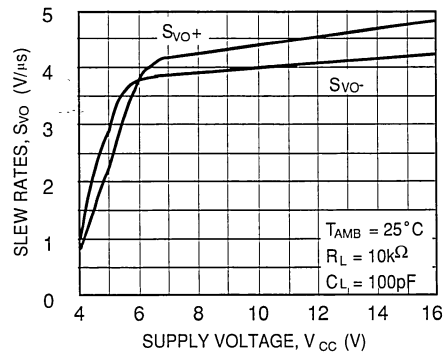
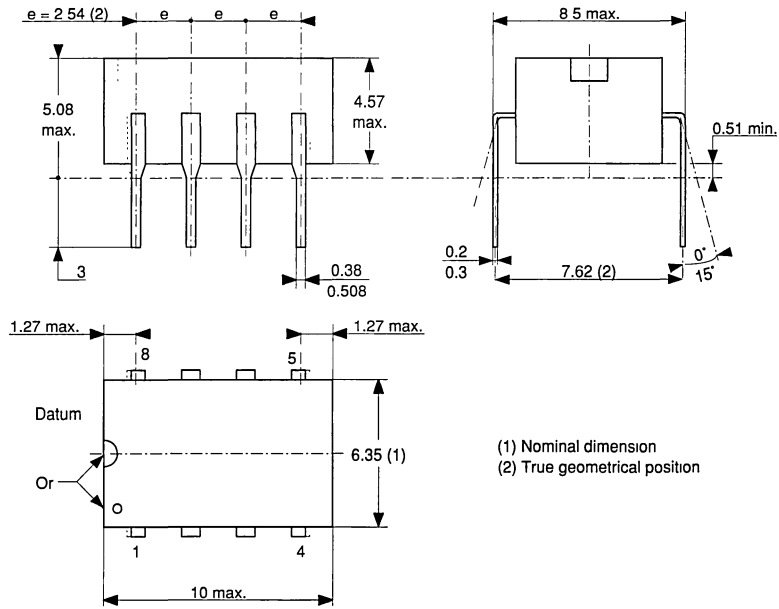


Figure 28 : Slew Rates versus Supply Voltage.

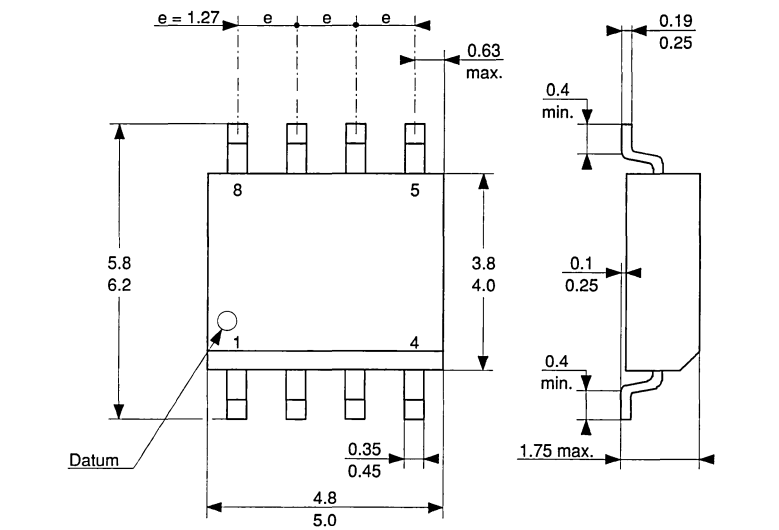


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

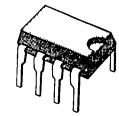


8 PINS - PLASTIC MICROPACKAGE (SO)



HIGH SPEED DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS272C/AC/BC	0°C to + 70°C	●	●	●
TS272I/AI/BI	- 40°C to + 105°C	●	●	●
TS272M/AM/BM	- 55°C to + 125°C	●	●	●
Example : TS272ACN				

DESCRIPTION

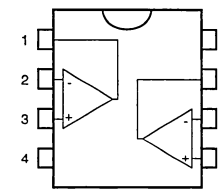
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

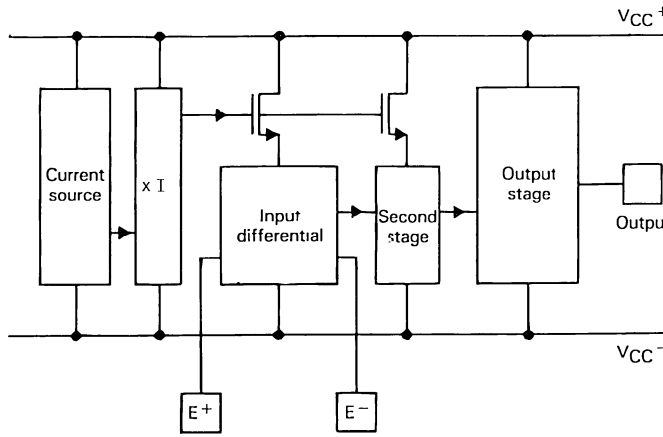
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{cc}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{cc}^+

S90TS272-01

BLOCK DIAGRAM



S90TS272-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS272C/AC/BC TS272I/AI/BI TS272M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

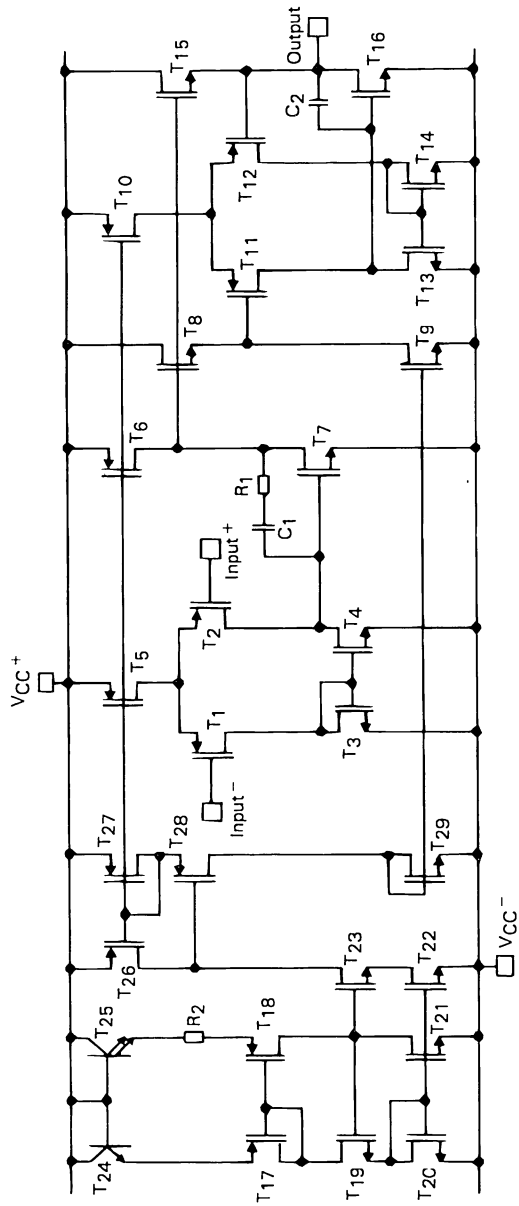
Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 * to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS272)



S90TS272-03

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS272C/AC/BC			TS272I/AI/BI TS272M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_i = 0V TS272C/I/M TS272AC/AI/AM TS272BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS272C/I/M TS272AC/AI/AM TS272BC/BI/BM		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage V_i = 10mV, R_L = 10kΩ $T_{MIN} \le T_{AMB} \le T_{MAX}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 10kΩ, V_i = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product A_v = 40dB, R_L = 10kΩ, C_L = 100pF f_{in} = 200 kHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_i = 1V to 7.4V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_v = 1, no load, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1000	1500 1600		1000	1500 1700	µA
I_o	Output Short Circuit Current V_i = 10mV, V_o = 0V	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain R_L = 10kΩ, C_L= 100pF		5.5			5.5		V/µs
Ø m	Phase Margin at Unity Gain A_v = 40 dB, R_L = 10kΩ, C_L= 100pF		40			40		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 10Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

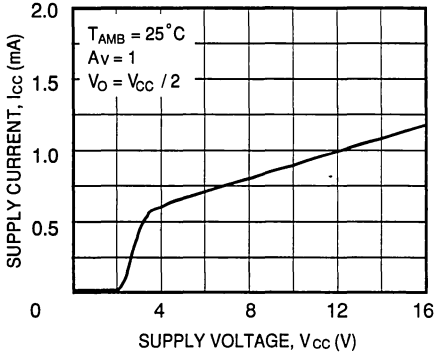


Figure 2 : Input Bias Current versus Free Air Temperature.

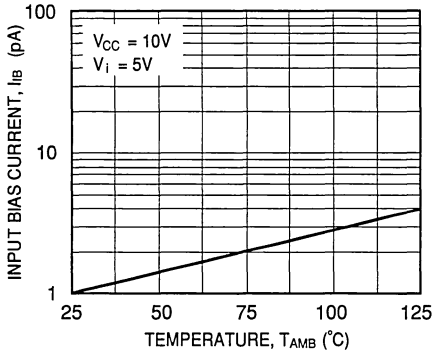


Figure 3a : High Level Output Voltage versus High Level Output Current.

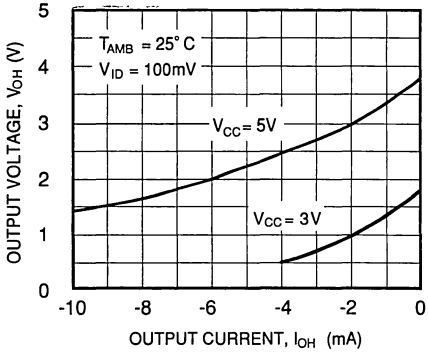


Figure 3b : High Level Output Voltage versus High Level Output Current.

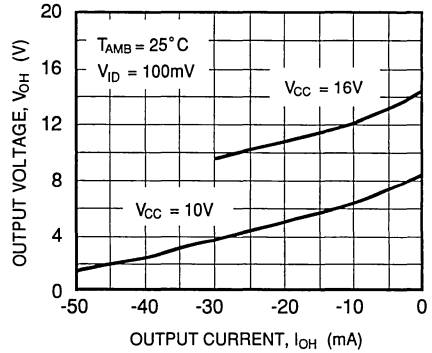


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

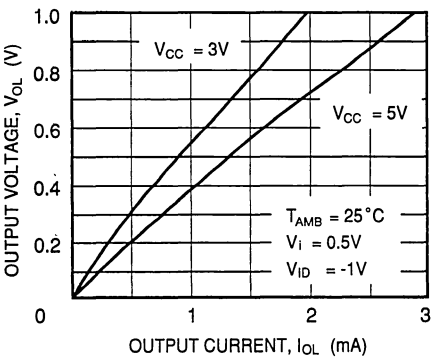
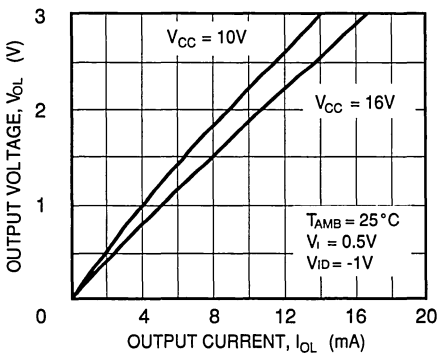


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

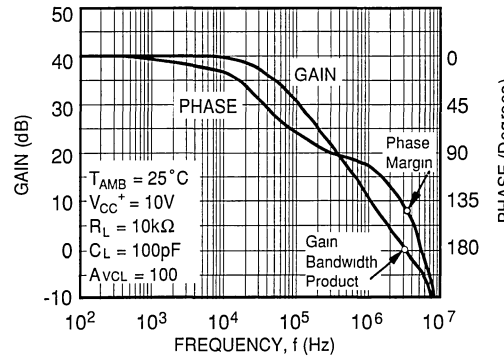


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

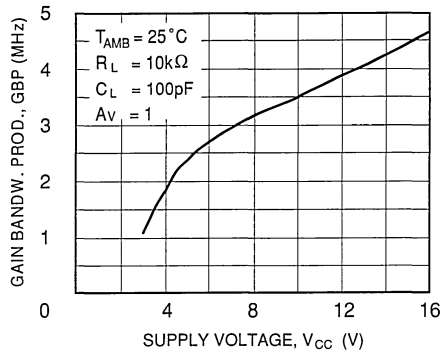


Figure 7 : Phase Margin versus Supply Voltage.

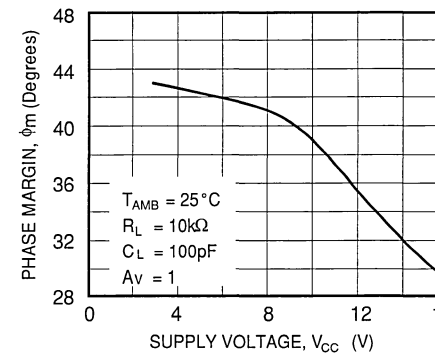


Figure 8 : Phase Margin versus Capacitive Load.

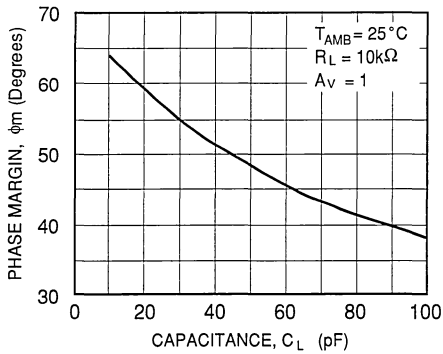
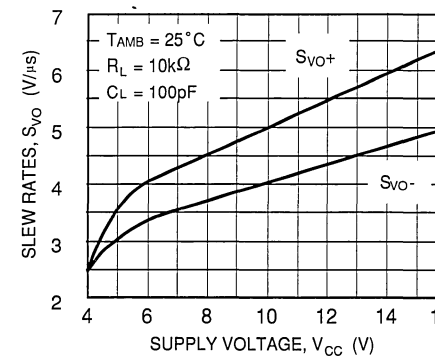
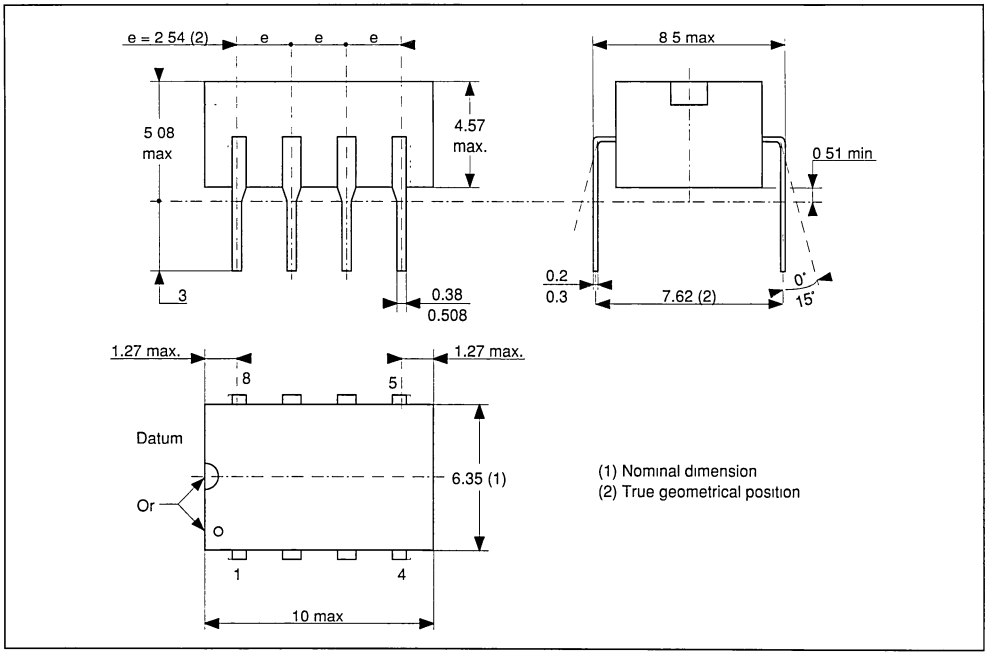


Figure 9 : Slew Rates versus Supply Voltage.

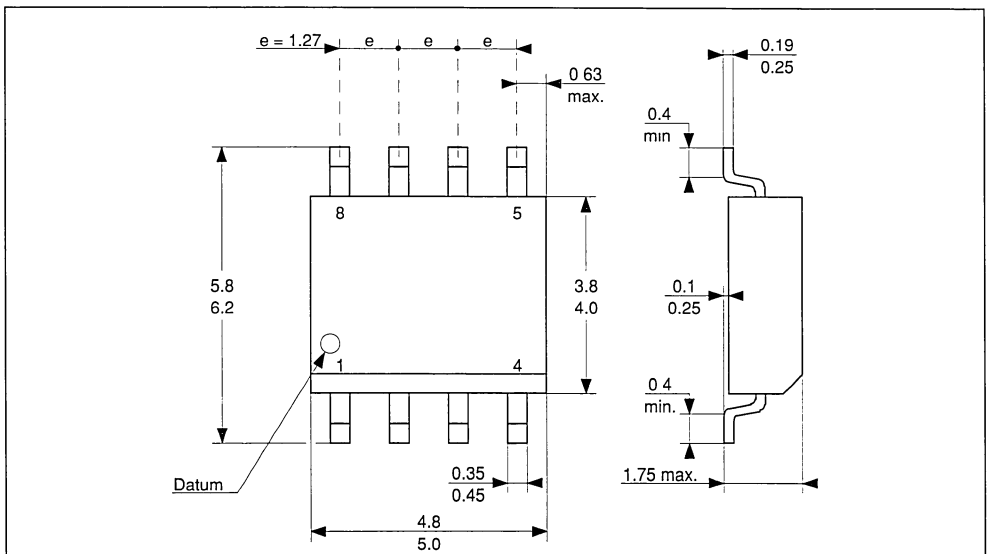


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

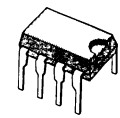


8 PINS - PLASTIC MICROPACKAGE (SO)



VERY LOW POWER DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27L2C/AC/BC	0°C to + 70°C	•	•	•
TS27L2I/AI/BI	- 40°C to + 105°C	•	•	•
TS27L2M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27L2ACN				

DESCRIPTION

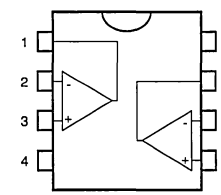
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

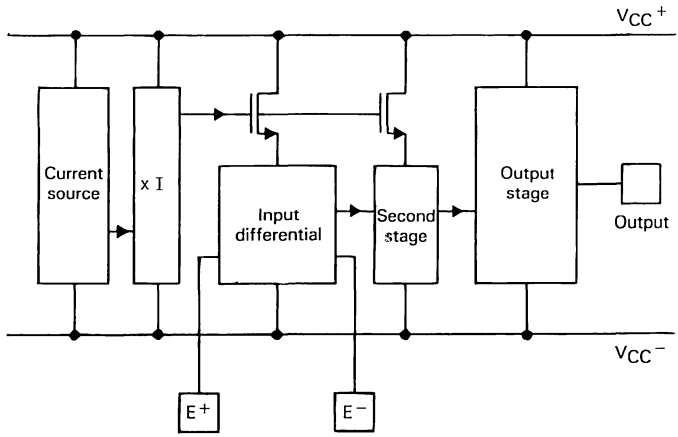
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

S90TS27L2-01

BLOCK DIAGRAM



S90TS27L2-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27L2C/AC/BC TS27L2I/AI/BI TS27L2M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

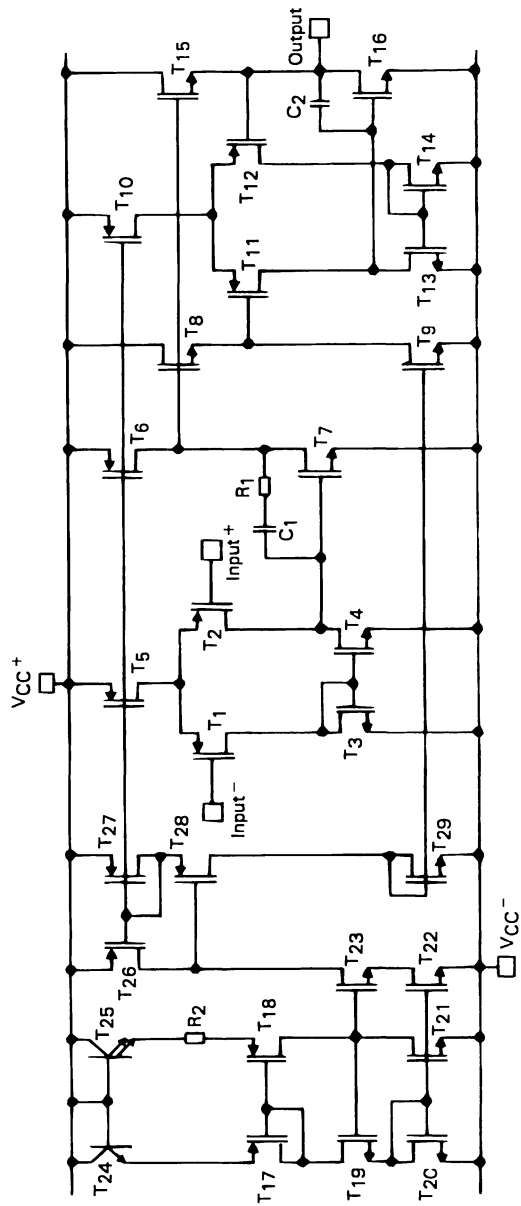
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only

SCHEMATIC DIAGRAM (for 1/2 TS27L2)



S90TS27L2-03

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25^oC$ (unless otherwise specified)

Symbol	Parameter		TS27L2C/AC/BC			TS27L2I/AI/BI TS27L2M/AM/BM			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage								mV
	$V_O = 1.4V$, $V_I = 0V$	TS27L2C/I/M		1.1	10		1.1	10	
		TS27L2AC/AI/AM		0.9	5		0.9	5	
		TS27L2BC/BI/BM		0.25	2		0.25	2	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	TS27L2C/I/M			12			12	
		TS27L2AC/AI/AM			6.5			6.5	
		TS27L2BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift			0.7			0.7		$\mu V/^oC$
I_{io}	Input Offset Current								pA
	$V_I = 5V$, $V_o = 5V$			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				100			200	
I_{ib}	Input Bias Current								pA
	$V_I = 5V$, $V_o = 5V$			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				150			300	
V_{OH}	High Level Output Voltage								V
	$V_I = 10mV$, $R_L = 1M\Omega$		8.8	9		8.8	9		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		8.7			8.6			
V_{OL}	Low Level Output Voltage								mV
	$V_i = -10mV$				50			50	
A_{vd}	Large Signal Voltage Gain								V/mV
	$V_o = 1V$ to $6V$, $R_L = 1M\Omega$, $V_I = 5V$		60	100		60	100		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		45			40			
GBP	Gain Bandwidth Product								MHz
	$A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$			0.1			0.1		
	$f_{in} = 10$ kHz								
CMR	Common Mode Rejection Ratio								dB
	$V_o = 1.4V$, $V_I = 1V$ to $7.4V$		65	80		65	80		
SVR	Supply Voltage Rejection Ratio								dB
	$V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$		60	80		60	80		
I_{CC}	Supply Current (per amplifier)								µA
	$A_v = 1$, no load, $V_o = 5V$			10	15		10	15	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				17			18	
I_o	Output Short Circuit Current								mA
	$V_I = 10mV$, $V_o = 0V$		45	60	85	45	60	85	
I_{sink}	Output Sink Current								mA
	$V_i = -10mV$, $V_o = V_{CC}$		35	45	65	35	45	65	
S_{vo}	Slew-Rate at Unity Gain								V/µs
	$R_L = 1M\Omega$, $C_L = 100pF$			0.04			0.04		
$\varnothing m$	Phase Margin at Unity Gain								degrees
	$A_v = 40$ dB, $R_L = 1M\Omega$, $C_L = 100pF$			45			45		
K_{ov}	Overshoot Factor			30			30		%
V_n	Equivalent Input Noise Voltage								$nV/\sqrt{Hz}$
	$f = 1kHz$, $R_S = 10\Omega$			68			68		
V_{O1}/V_{O2}	Cross Talk Attenuation			120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

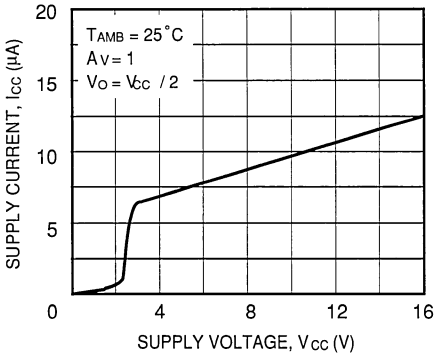


Figure 2 : Input Bias Current versus Free Air Temperature.

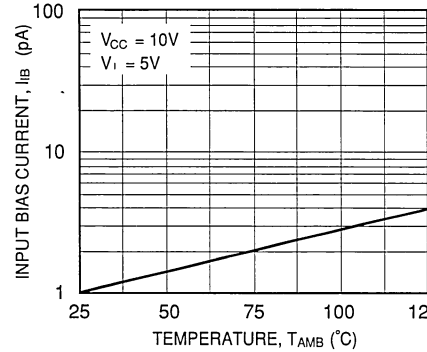


Figure 3a : High Level Output Voltage versus High Level Output Current.

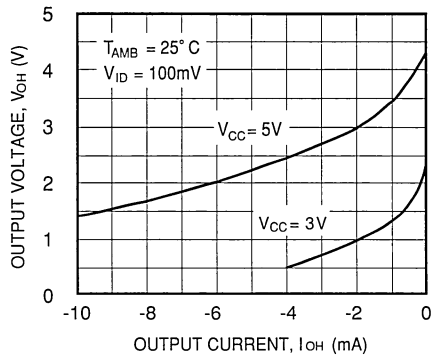


Figure 3b : High Level Output Voltage versus High Level Output Current.

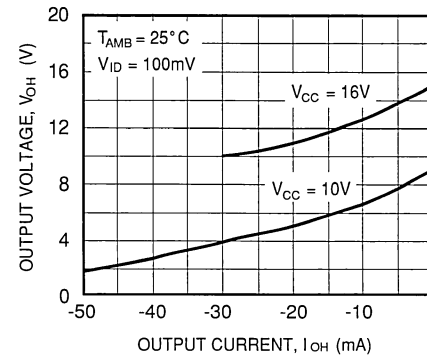


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

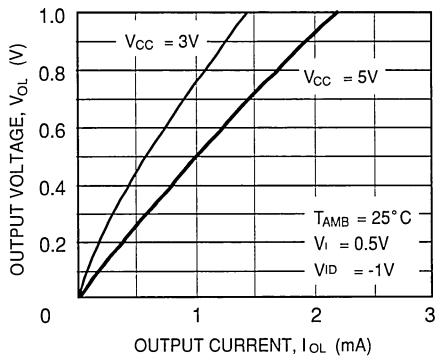
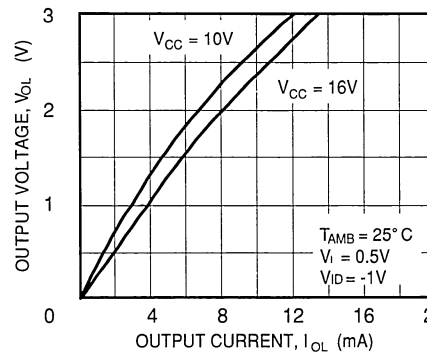


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

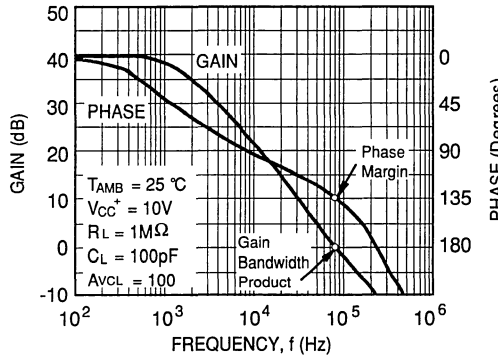


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

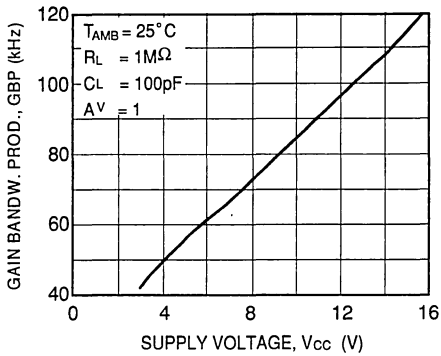


Figure 7 : Phase Margin versus Supply Voltage.

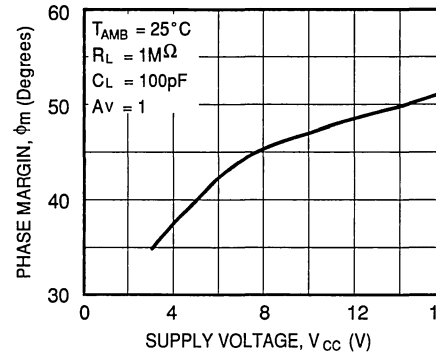


Figure 8 : Phase Margin versus Capacitive Load.

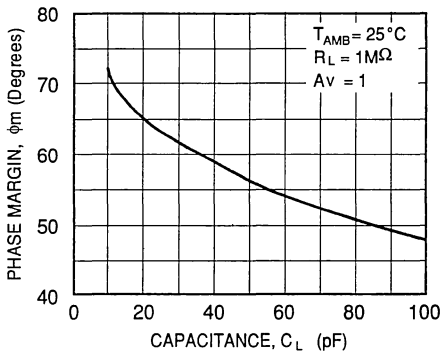
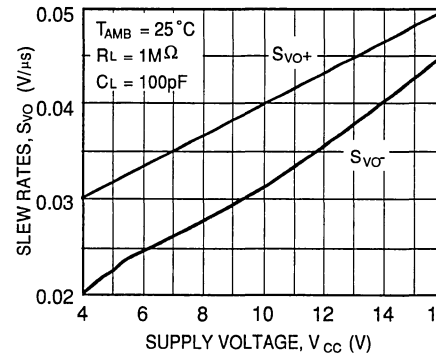
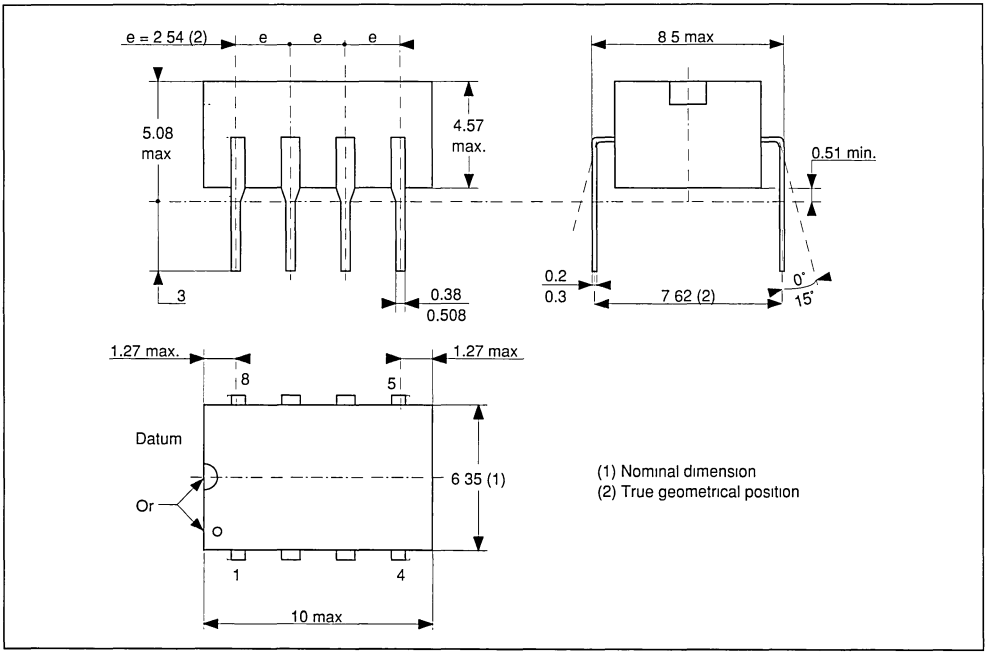


Figure 9 : Slew Rates versus Supply Voltage.

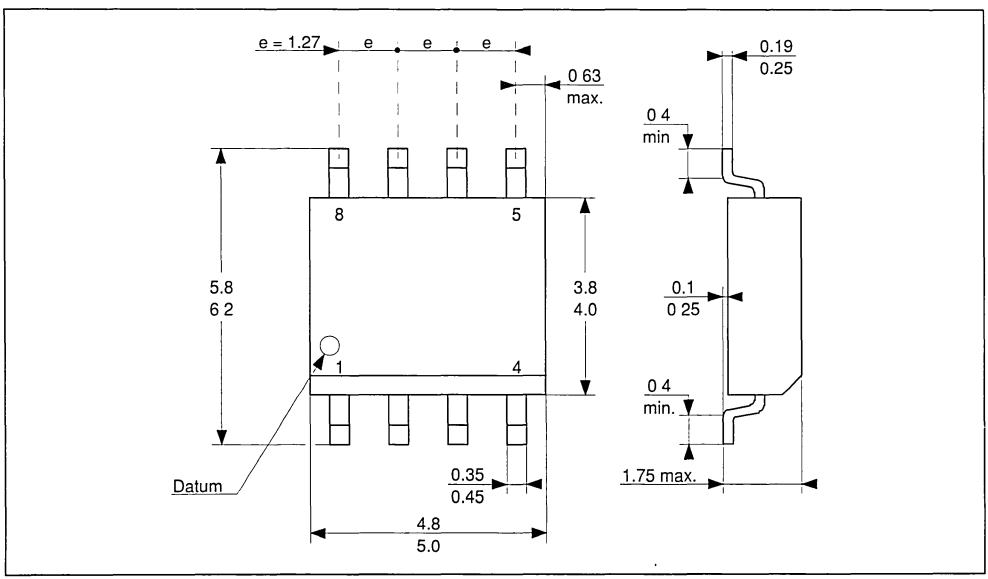


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



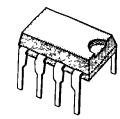
8 PINS - PLASTIC MICROPACKAGE (SO)



TS27M2C,I,M

LOW POWER DUAL CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27M2C/AC/BC	0°C to + 70°C	•	•	•
TS27M2I/AI/BI	- 40°C to + 105°C	•	•	•
TS27M2M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27M2ACN				

DESCRIPTION

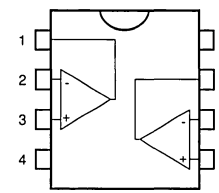
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

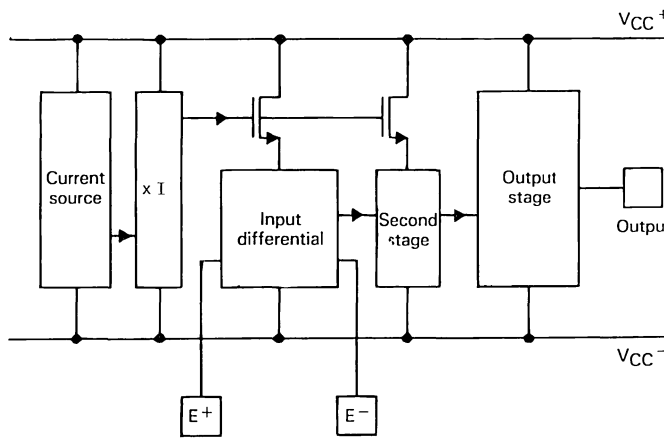
DIP8 - CERDIP 8 - SO8



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

S90TS27M2-01

BLOCK DIAGRAM



S90TS27M2-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27M2C/AC/BC TS27M2I/AI/BI TS27M2M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

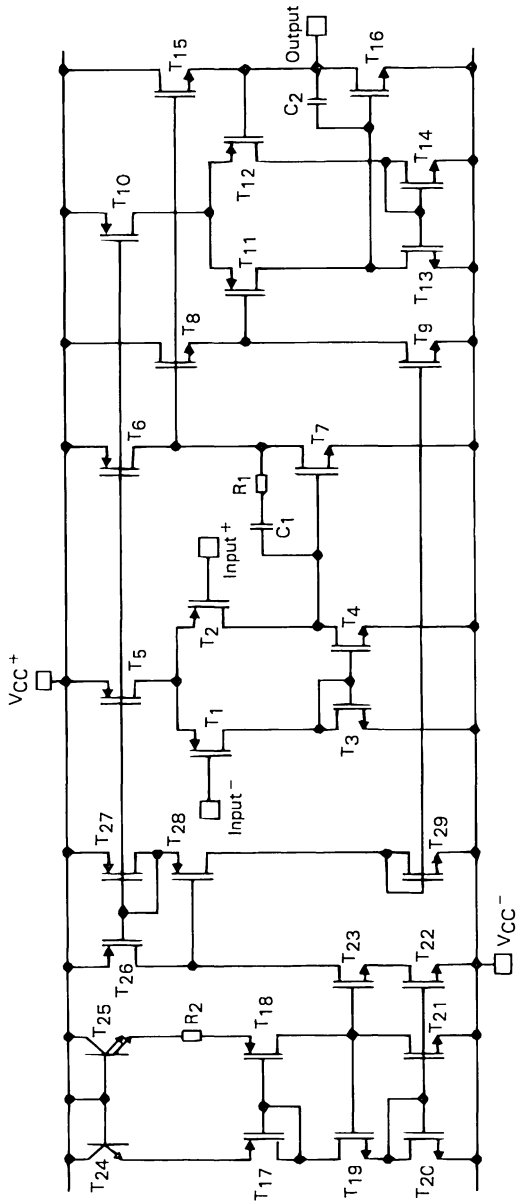
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/2 TS27M2)



S90TS27M2-03

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS27M2C/AC/BC			TS27M2I/AI/BI TS27M2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_I = 0V TS27M2C/I/M TS27M2AC/AI/AM TS27M2BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS27M2C/I/M TS27M2AC/AI/AM TS27M2BC/BI/BM		1 1 0.9 0 25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current V_I = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current V_I = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage V_I = 10mV, R_L = 100kΩ $T_{MIN} \le T_{AMB} \le T_{MAX}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 100kΩ, V_I = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product A_v = 40dB, R_L = 100kΩ, C_L = 100pF f_{in} = 100 kHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_I = 1V to 7.4V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_v = 1, no load, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		150	200 250		150	200 300	µA
I_o	Output Short Circuit Current V_I = 10mV, V_o = 0V	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain R_L = 100kΩ, C_L= 100pF		0.6			0.6		V/µs
Ø m	Phase Margin at Unity Gain A_v = 40 dB, R_L = 100kΩ, C_L= 100pF		45			45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 10Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

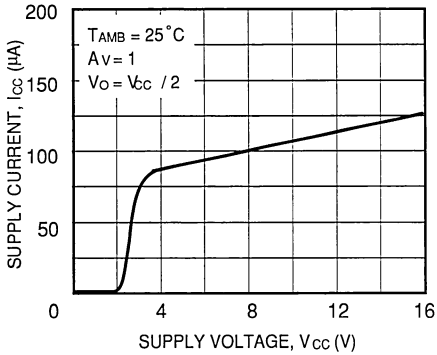


Figure 2 : Input Bias Current versus Free Air Temperature.

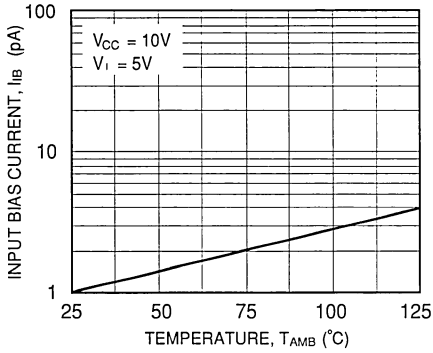


Figure 3a : High Level Output Voltage versus High Level Output Current.

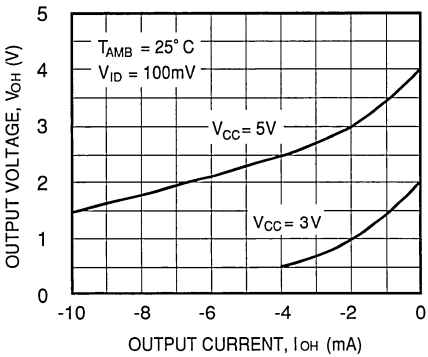


Figure 3b : High Level Output Voltage versus High Level Output Current.

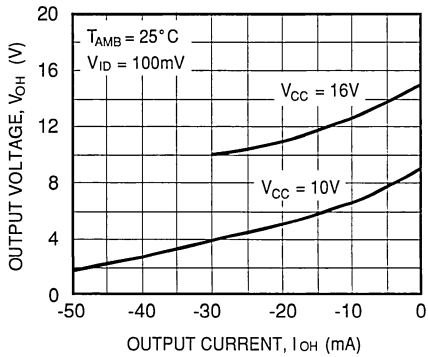


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

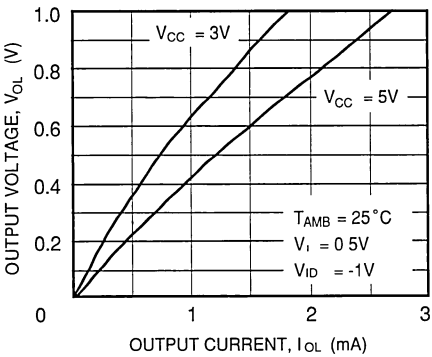
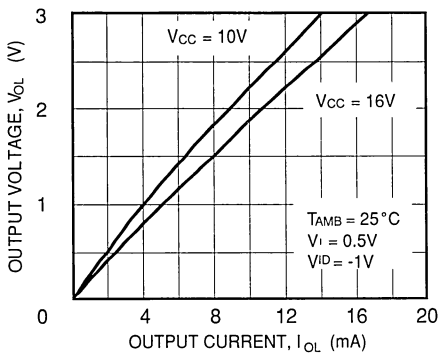


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

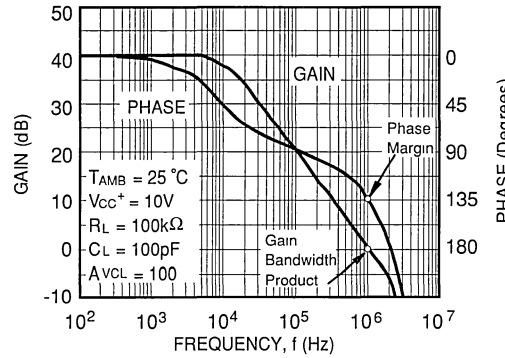


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

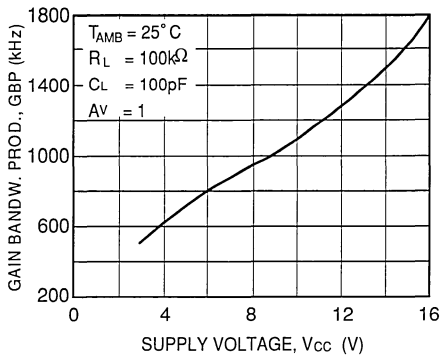


Figure 7 : Phase Margin versus Supply Voltage.

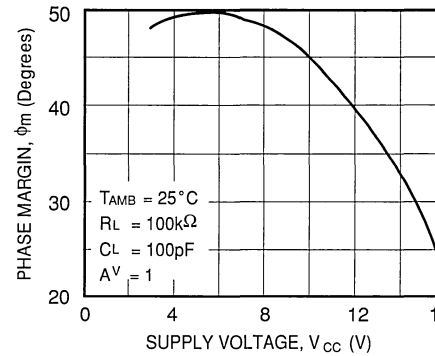


Figure 8 : Phase Margin versus Capacitive Load.

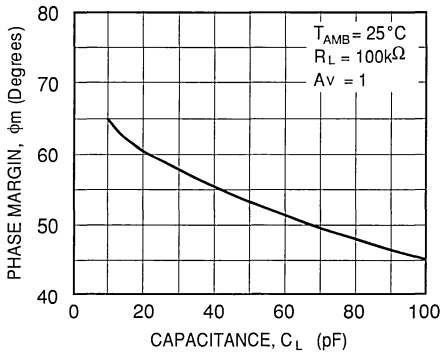
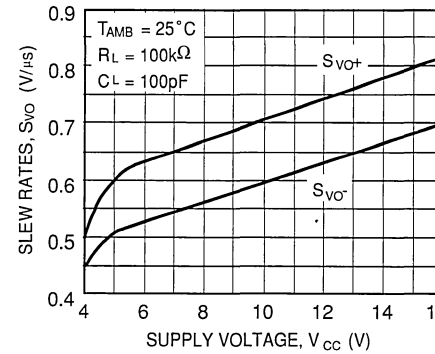
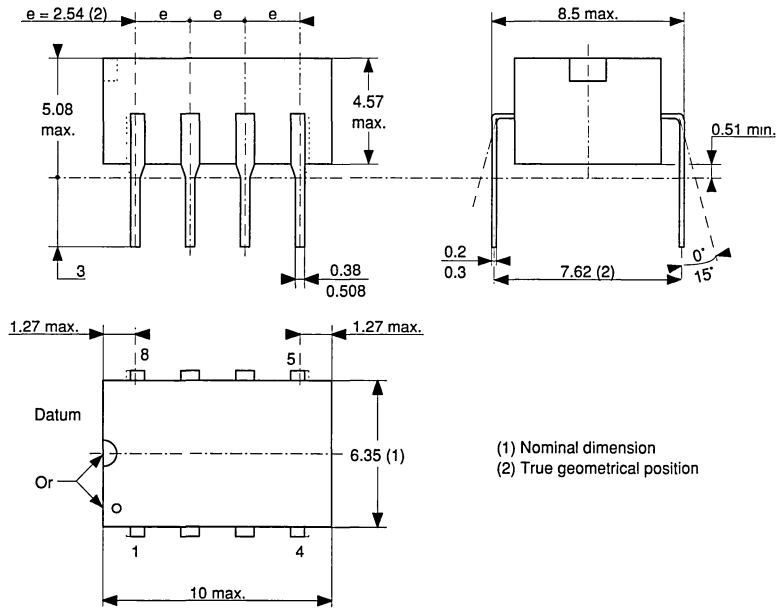


Figure 9 : Slew Rates versus Supply Voltage.

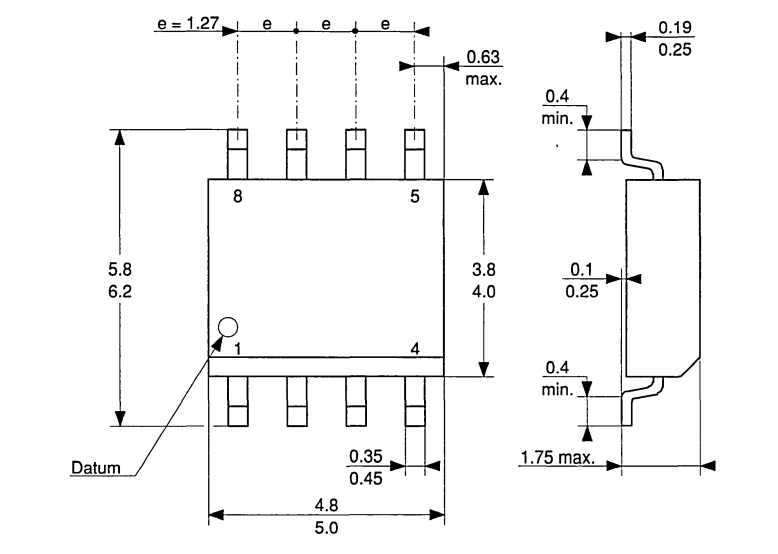


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



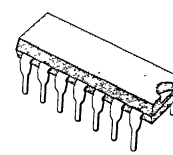
8 PINS - PLASTIC MICROPACKAGE (SO)



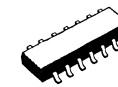
TS274C,I,M

HIGH SPEED QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS274C/AC/BC	0°C to + 70°C	•	•	•
TS274I/AI/BI	- 40°C to + 105°C	•	•	•
TS274M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS274ACN				

DESCRIPTION

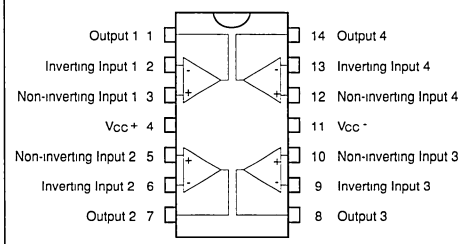
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

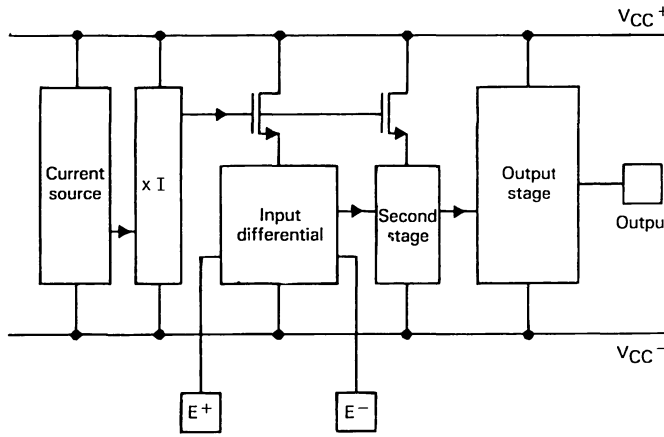
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS274-01

BLOCK DIAGRAM



S90TS274-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS274C/AC/BC TS274I/AI/BI TS274M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

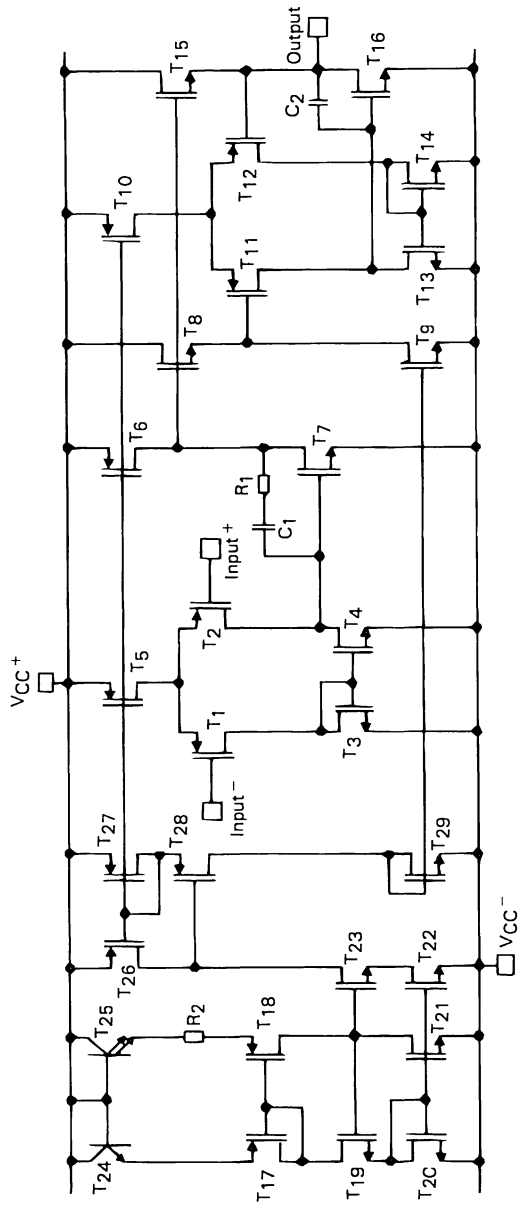
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS274)



S90TS274-03

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter		TS274C/AC/BC			TS274I/AI/BI TS274M/AM/BM			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage								mV
	V_O = 1.4V, V_i = 0V	TS274C/I/M		1.1	10		1.1	10	
		TS274AC/AI/AM		0.9	5		0.9	5	
		TS274BC/BI/BM		0.25	2		0.25	2	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$	TS274C/I/M			12			12	
		TS274AC/AI/AM			6.5			6.5	
		TS274BC/BI/BM			3			3.5	
DV_{io}	Input Offset Voltage Drift			2			2		µV/°C
I_{io}	Input Offset Current								pA
	V_i = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				100			200	
I_{ib}	Input Bias Current								pA
	V_i = 5V, V_o = 5V			1			1		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				150			300	
V_{OH}	High Level Output Voltage								V
	V_i = 10mV, R_L = 10kΩ		8.2	8.4		8.2	8.4		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		8.1			8			
V_{OL}	Low Level Output Voltage								mV
	Vi = - 10mV				50			50	
A_{vd}	Large Signal Voltage Gain								V/mV
	V_o = 1V to 6V, R_L = 10kΩ, V_i = 5V		10	15		10	15		
	$T_{MIN} \le T_{AMB} \le T_{MAX}$		7			6			
GBP	Gain Bandwidth Product								MHz
	A_v = 40dB, R_L = 10kΩ, C_L = 100pF			3.5			3.5		
	f_{in} = 200 kHz								
CMR	Common Mode Rejection Ratio								dB
	V_o = 1.4V, V_i = 1V to 7.4V		65	80		65	80		
SVR	Supply Voltage Rejection Ratio								dB
	V_{CC}^+ = 5V to 10V ,V_o = 1.4V		60	70		60	70		
I_{CC}	Supply Current (per amplifier)								µA
	A_v = 1, no load, V_o = 5V			1000	1500		1000	1500	
	$T_{MIN} \le T_{AMB} \le T_{MAX}$				1600			1700	
I_o	Output Short Circuit Current								mA
	V_i = 10mV, V_o = 0V		45	60	85	45	60	85	
I_{sink}	Output Sink Current								mA
	Vi = - 10mV, V_o = V_{CC}		35	45	65	35	45	65	
S_{vo}	Slew-Rate at Unity Gain								V/µs
	R_L = 10kΩ, C_L= 100pF			5.5			5.5		
Ø m	Phase Margin at Unity Gain								degrees
	A_v = 40 dB, R_L = 10kΩ, C_L= 100pF			40			40		
K_{ov}	Overshoot Factor			30			30		%
V_n	Equivalent Input Noise Voltage								nV/√Hz
	f = 1kHz, R_S = 10Ω			30			30		
V_{O1}/V_{O2}	Cross Talk Attenuation			120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

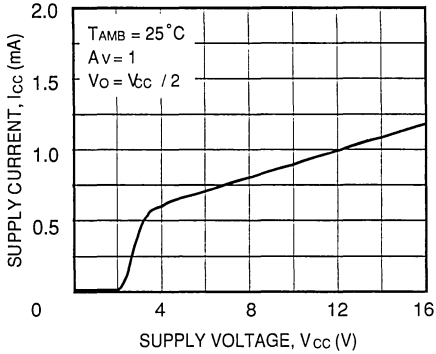


Figure 2 : Input Bias Current versus Free Air Temperature.

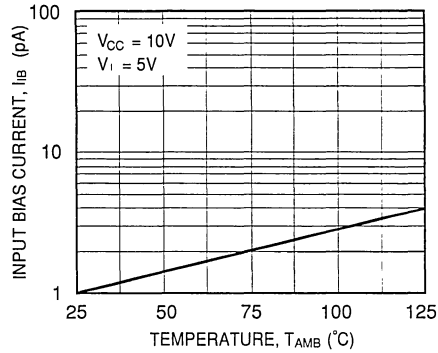


Figure 3a : High Level Output Voltage versus High Level Output Current.

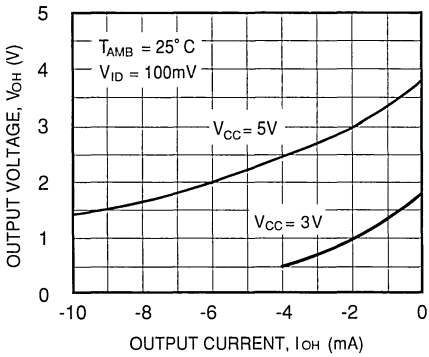


Figure 3b : High Level Output Voltage versus High Level Output Current.

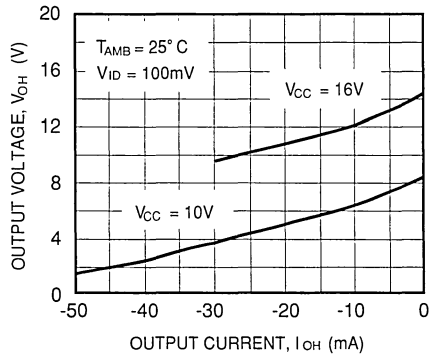


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

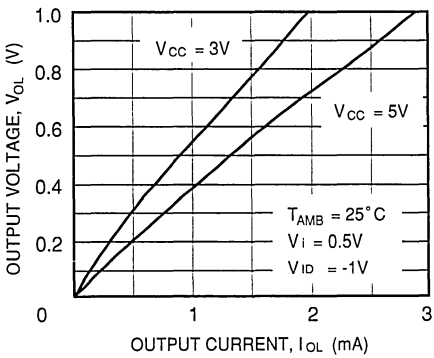
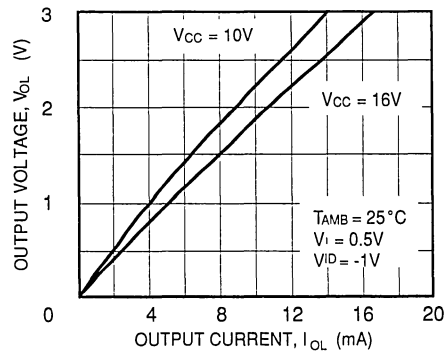


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

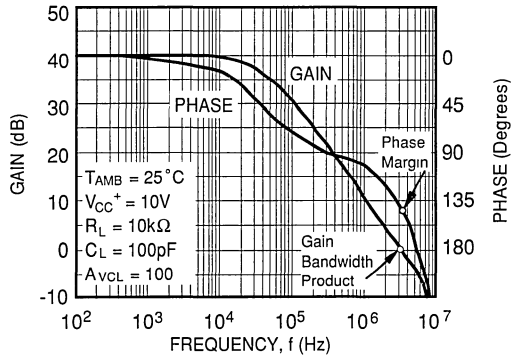


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

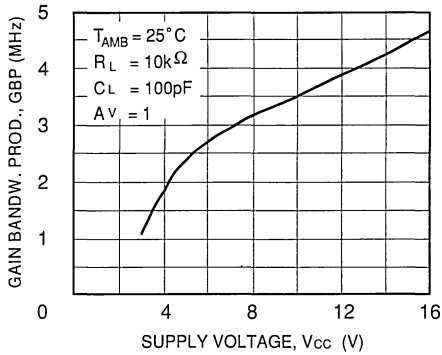


Figure 7 : Phase Margin versus Supply Voltage.

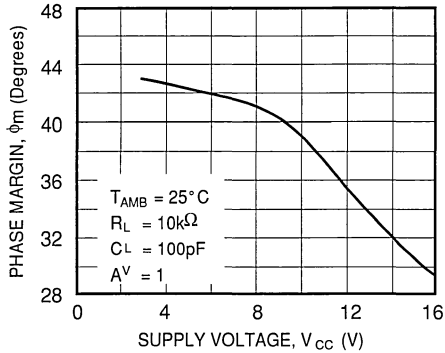


Figure 8 : Phase Margin versus Capacitive Load.

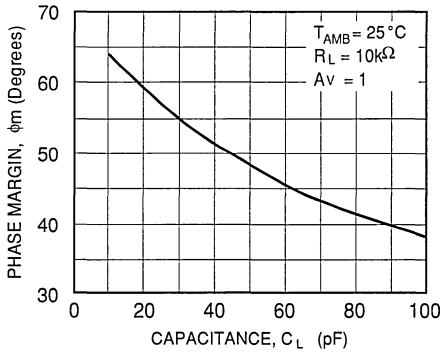
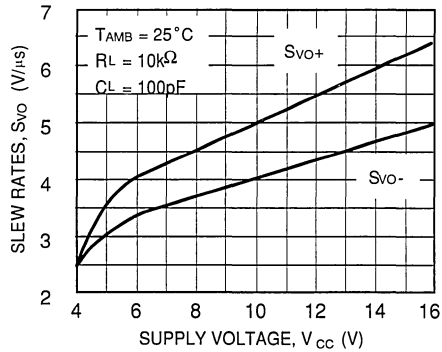
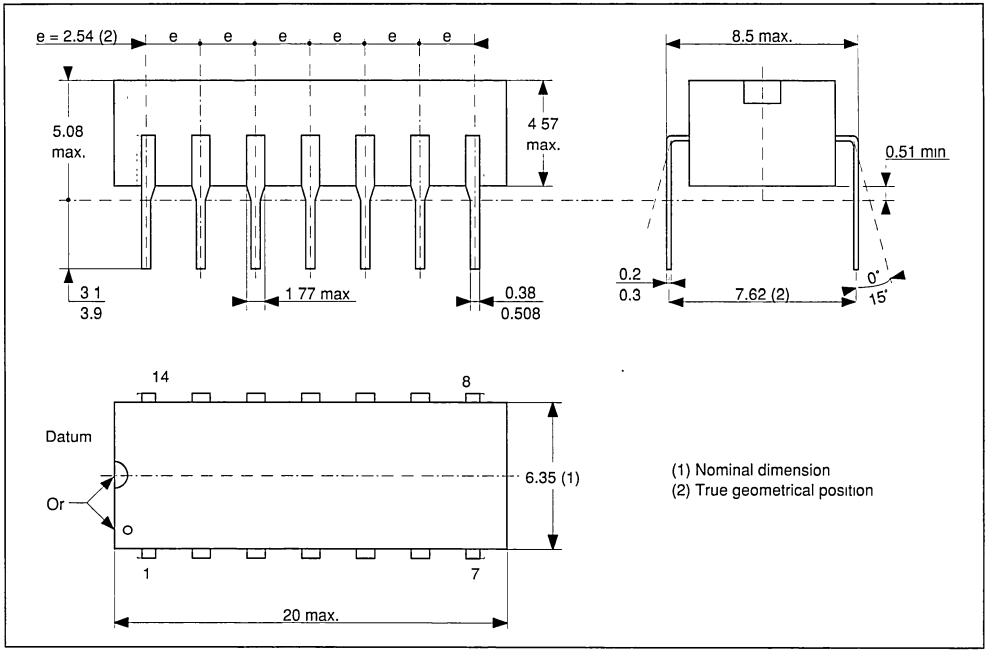


Figure 9 : Slew Rates versus Supply Voltage.

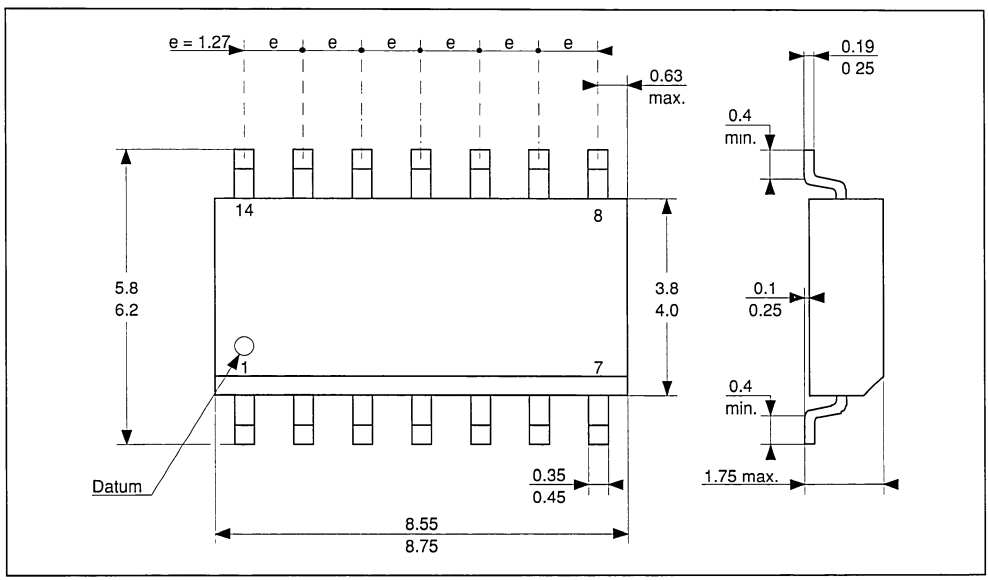


PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP

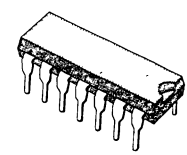


14 PINS - PLASTIC MICROPACKAGE (SO)

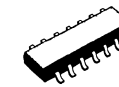


VERY LOW POWER QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27L4C/AC/BC	0°C to + 70°C	•	•	•
TS27L4I/AI/BI	- 40°C to + 105°C	•	•	•
TS27L4M/AM/BM	- 55°C to + 125°C	•	•	•
Example : TS27L4ACN				

DESCRIPTION

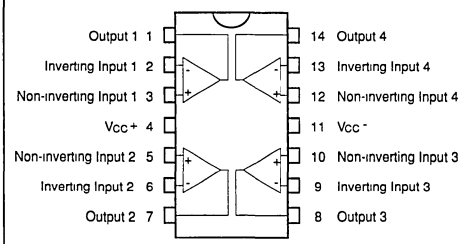
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

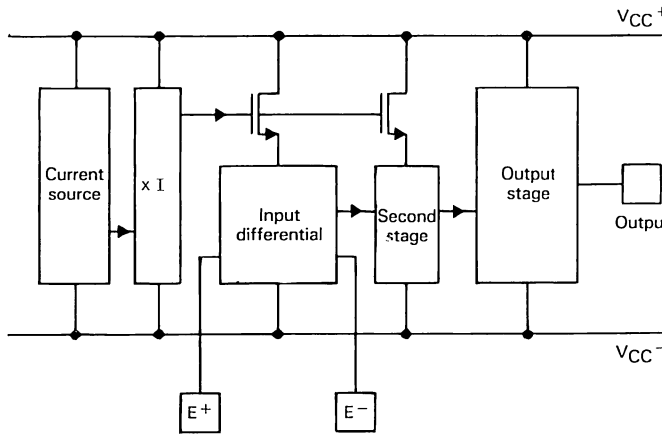
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS27L4-01

BLOCK DIAGRAM



S90TS27L4-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27L4C/AC/BC TS27L4I/AI/BI TS27L4M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

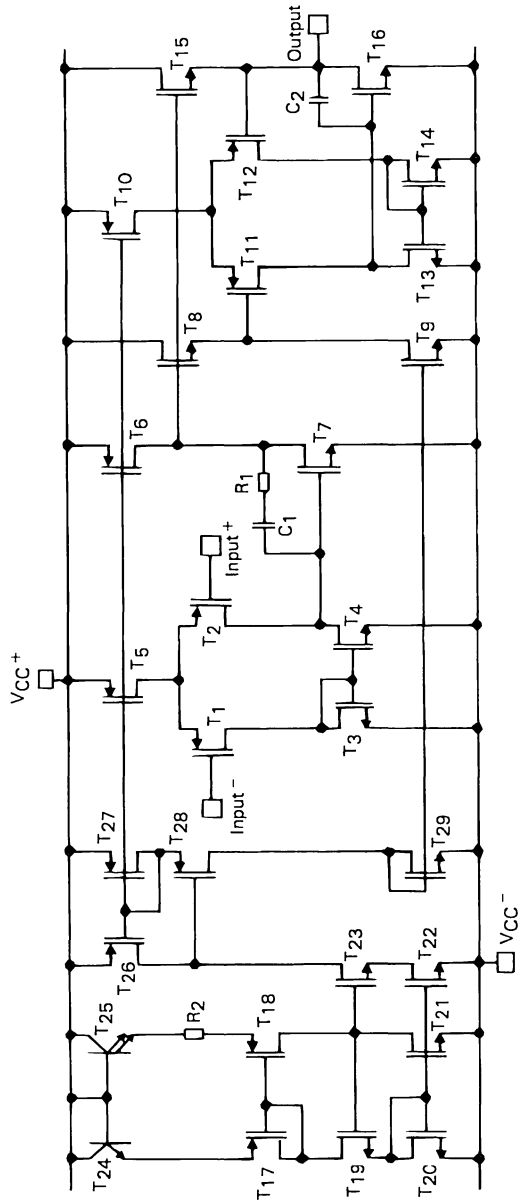
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27L4)



S90TS27L4-03

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{AMB} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TS27L4C/AC/BC			TS27L4I/AI/BI TS27L4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_i = 0V$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS27L4C/I/M TS27L4AC/AI/AM TS27L4BC/BI/BM		 1.1 0.9 0.25 	 10 5 2 12 6.5 3		 1.1 0.9 0.25 	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		0.7			0.7		µV/°C
I_{io}	Input Offset Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current $V_i = 5V$, $V_o = 5V$ $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage $V_i = 10mV$, $R_L = 1M\Omega$ $T_{MIN} \le T_{AMB} \le T_{MAX}$	8.8 8.7	9		8.8 8.6	9		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_o = 1V$ to 6V, $R_L = 1M\Omega$, $V_i = 5V$ $T_{MIN} \le T_{AMB} \le T_{MAX}$	60 45	100		60 40	100		V/mV
GBP	Gain Bandwidth Product $A_V = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$ $f_{in} = 10$ kHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_o = 1.4V$, $V_i = 1V$ to 7.4V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to 10V ,$V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_V = 1$, no load, $V_o = 5V$ $T_{MIN} \le T_{AMB} \le T_{MAX}$		10	15 17		10	15 18	µA
I_o	Output Short Circuit Current $V_i = 10mV$, $V_o = 0V$	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, $V_o = V_{CC}$	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$		0.04			0.04		V/µs
Ø m	Phase Margin at Unity Gain $A_V = 40$ dB, $R_L = 1M\Omega$, $C_L = 100pF$		45			45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, $R_S = 10\Omega$		68			68		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

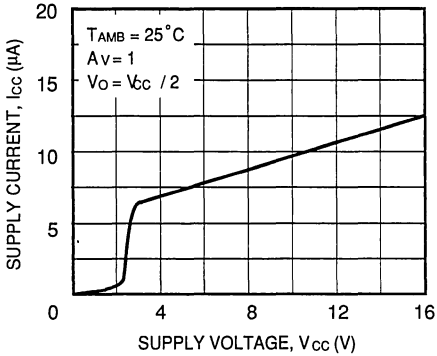


Figure 2 : Input Bias Current versus Free Air Temperature.

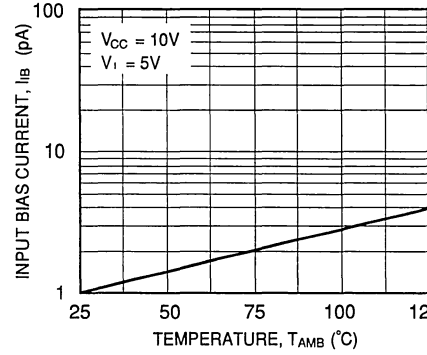


Figure 3a : High Level Output Voltage versus High Level Output Current.

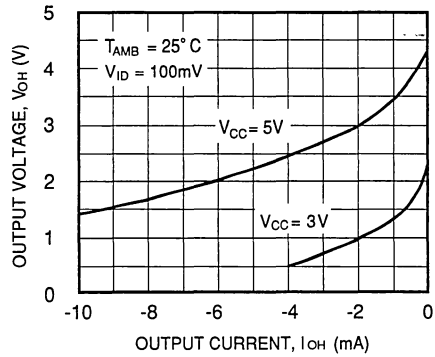


Figure 3b : High Level Output Voltage versus High Level Output Current.

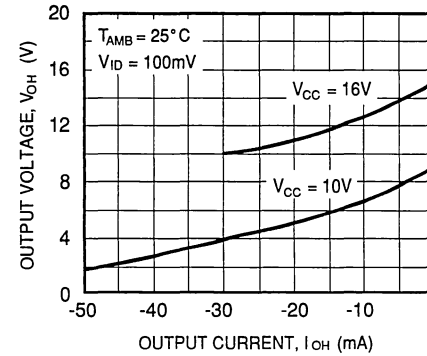


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

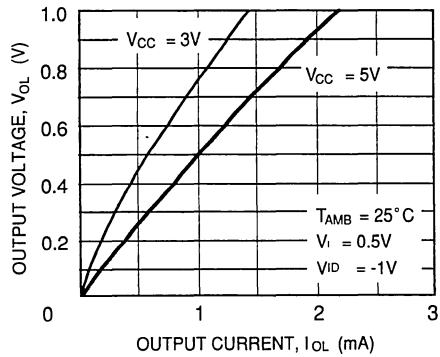
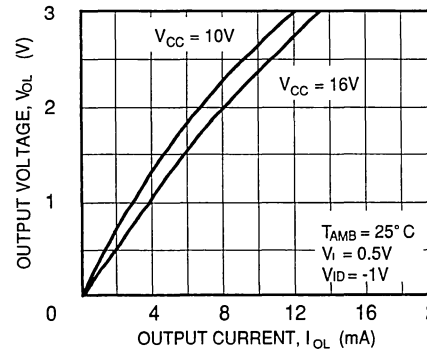


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

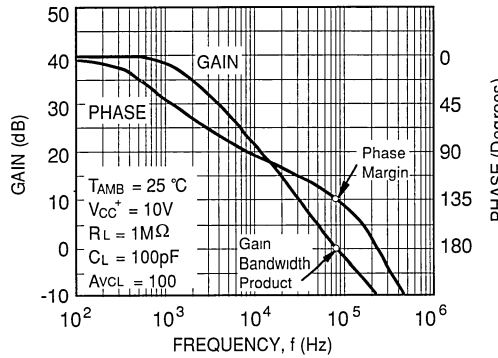


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

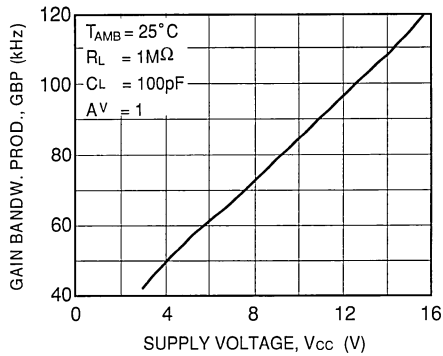


Figure 7 : Phase Margin versus Supply Voltage.

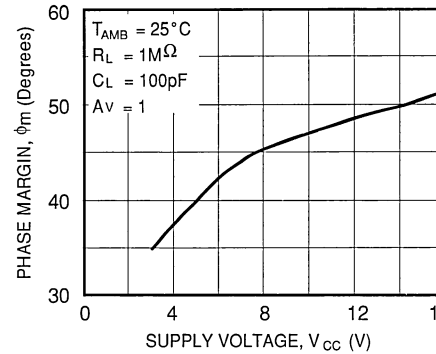


Figure 8 : Phase Margin versus Capacitive Load.

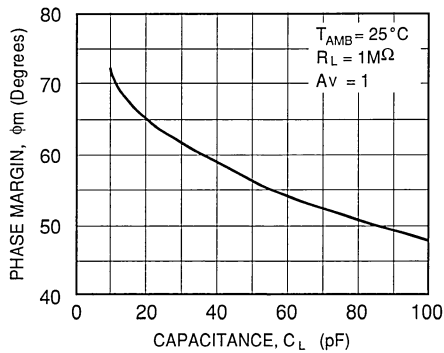
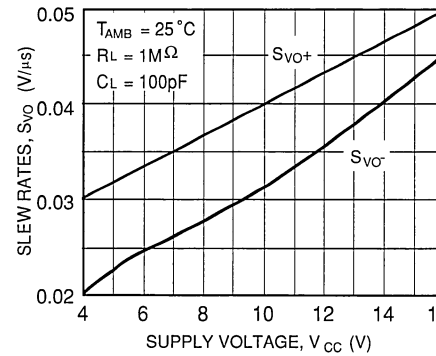
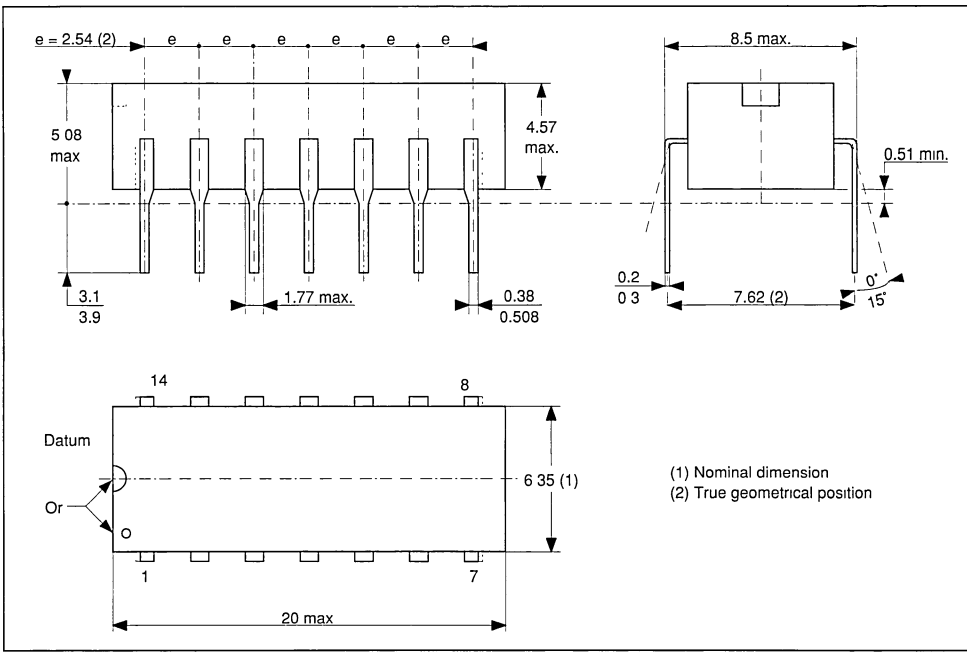


Figure 9 : Slew Rates versus Supply Voltage.

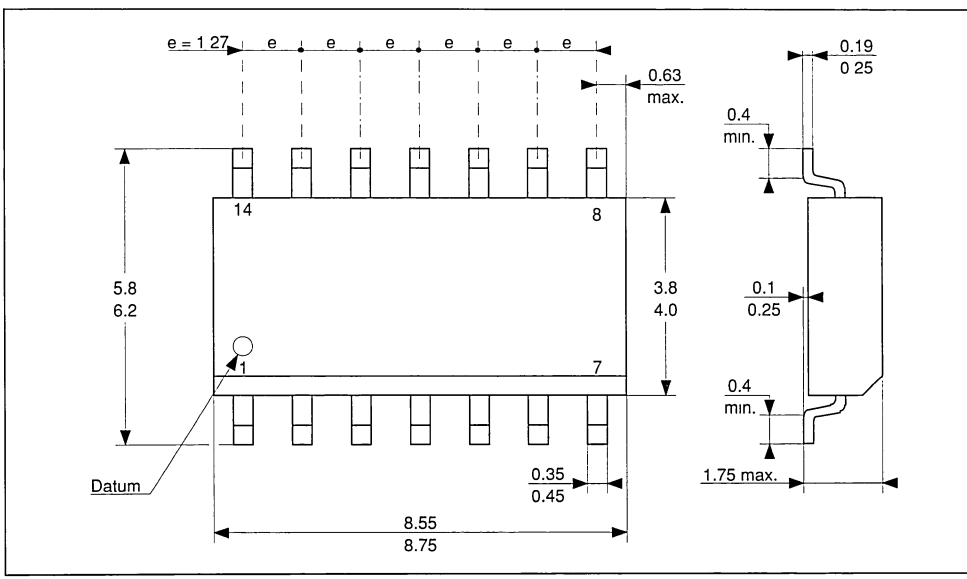


PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



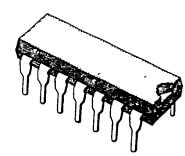
14 PINS - PLASTIC MICROPACKAGE (SO)



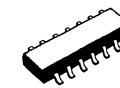
TS27M4C,I,M

LOW POWER QUAD CMOS OP-AMPs

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS27M4C/AC/BC	0°C to + 70°C	●	●	●
TS27M4I/AI/BI	- 40°C to + 105°C	●	●	●
TS27M4M/AM/BM	- 55°C to + 125°C	●	●	●
Example : TS27M4ACN				

DESCRIPTION

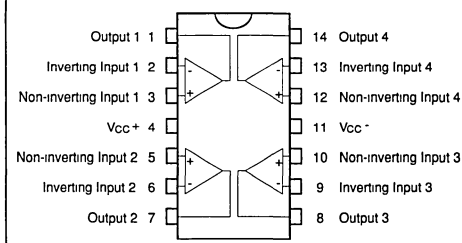
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :
- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

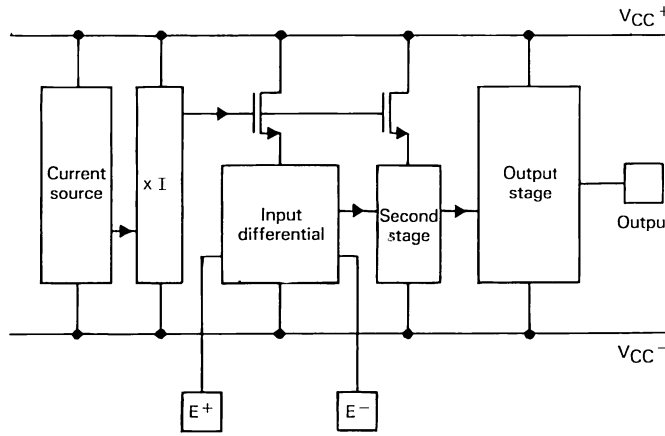
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS27M4-01

BLOCK DIAGRAM



S90TS27M4-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	- 0.3 to 18	V
I_O	Output Current for $V_{CC}^+ \geq 15V$	± 30	mA
T_{oper}	Operating Free-Air Temperature Range TS27M4C/AC/BC TS27M4I/AI/BI TS27M4M/AM/BM	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

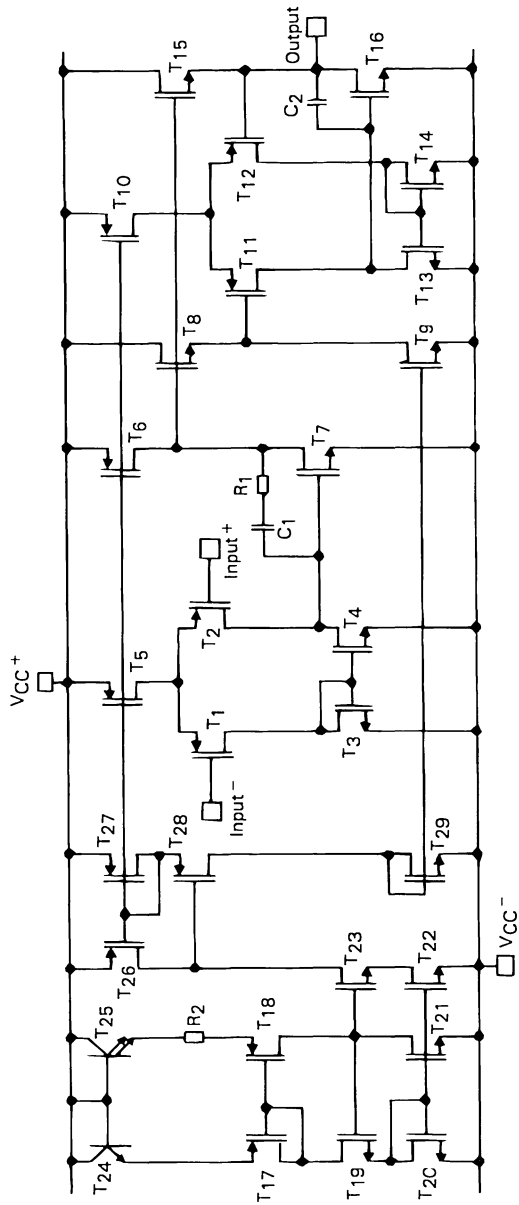
Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3* to 16	V
V_{ic}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

* Selected devices only.

SCHEMATIC DIAGRAM (for 1/4 TS27M4)



S90TS27M4-03

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = + 10V, V_{CC}^- = 0V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	TS27M4C/AC/BC			TS27M4I/AI/BI TS27M4M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_O = 1.4V, V_i = 0V TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM		 1.1 0.9 0.25	 10 5 2 12 6.5 3		 1.1 0.9 0.25	 10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current V_i = 5V, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage V_i = 10mV, R_L = 100kΩ $T_{MIN} \le T_{AMB} \le T_{MAX}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage Vi = - 10mV			50			50	mV
A_{vd}	Large Signal Voltage Gain V_o = 1V to 6V, R_L = 100kΩ, V_i = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product A_v = 40dB, R_L = 100kΩ, C_L = 100pF f_{in} = 100 kHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4V, V_i = 1V to 7.4V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = 5V to 10V ,V_o = 1.4V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_v = 1, no load, V_o = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$		150	200 250		150	200 300	µA
I_o	Output Short Circuit Current V_i = 10mV, V_o = 0V	45	60	85	45	60	85	mA
I_{sink}	Output Sink Current Vi = - 10mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew-Rate at Unity Gain R_L = 100kΩ, C_L= 100pF		0.6			0.6		V/µs
Ø m	Phase Margin at Unity Gain A_v = 40 dB, R_L = 100kΩ, C_L= 100pF		45			45		degrees
K_{ov}	Overshoot Factor		30			30		%
V_n	Equivalent Input Noise Voltage f = 1kHz, R_S = 10Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

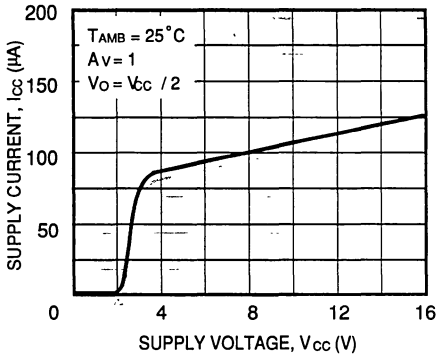


Figure 2 : Input Bias Current versus Free Air Temperature.

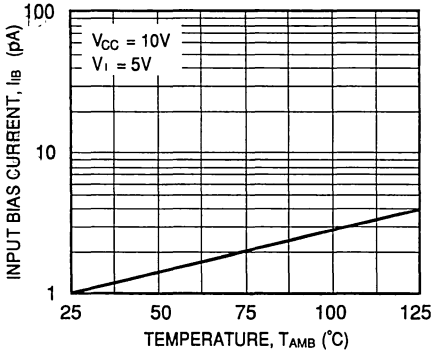


Figure 3a : High Level Output Voltage versus High Level Output Current.

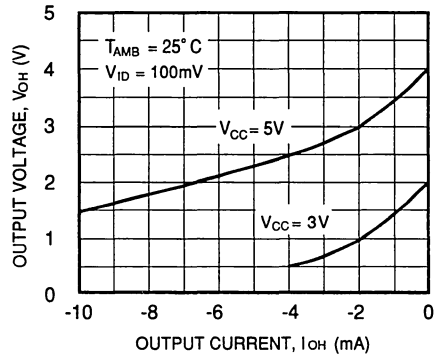


Figure 3b : High Level Output Voltage versus High Level Output Current.

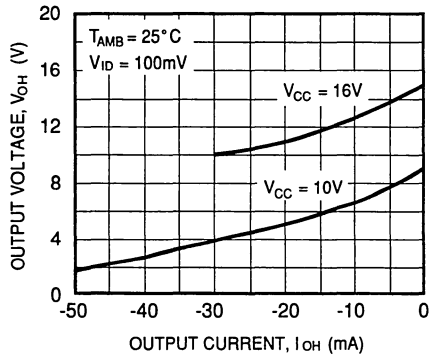


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

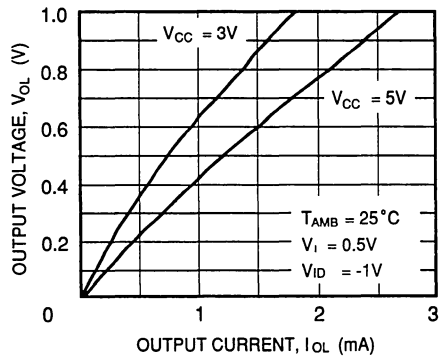
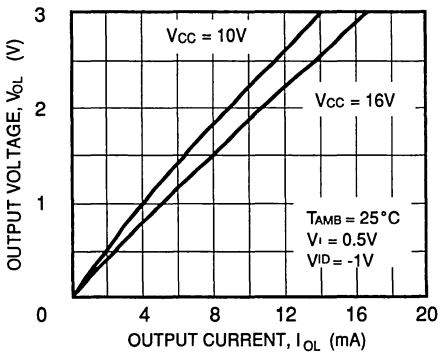


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



TYPICAL CHARACTERISTICS (continued)

Figure 5 : Open Loop Frequency Response and Phase Shift.

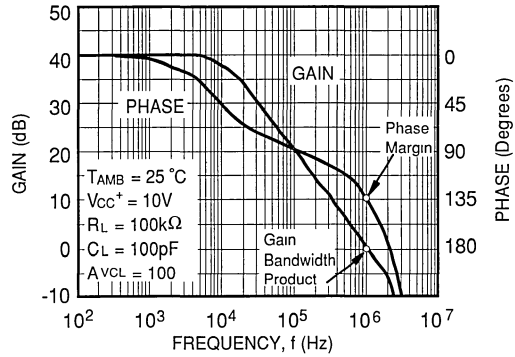


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

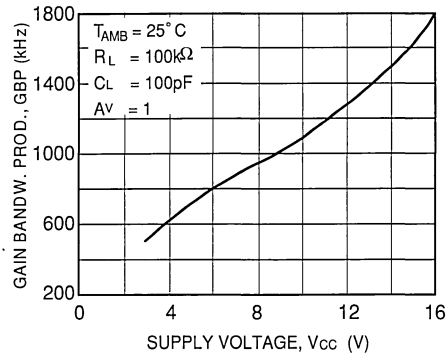


Figure 7 : Phase Margin versus Supply Voltage.

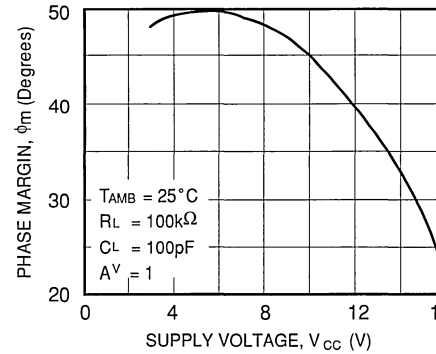


Figure 8 : Phase Margin versus Capacitive Load.

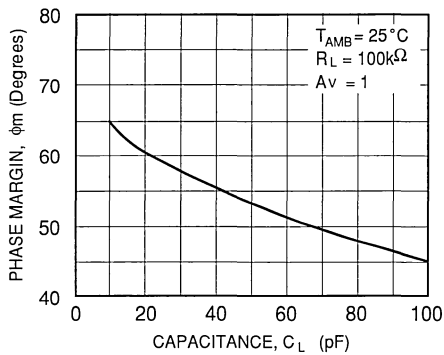
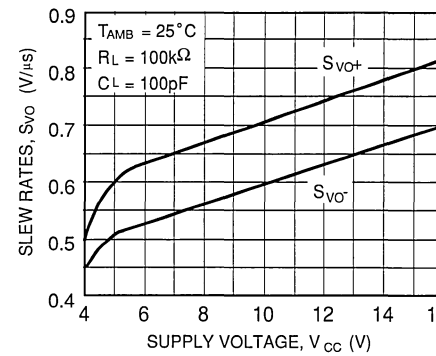
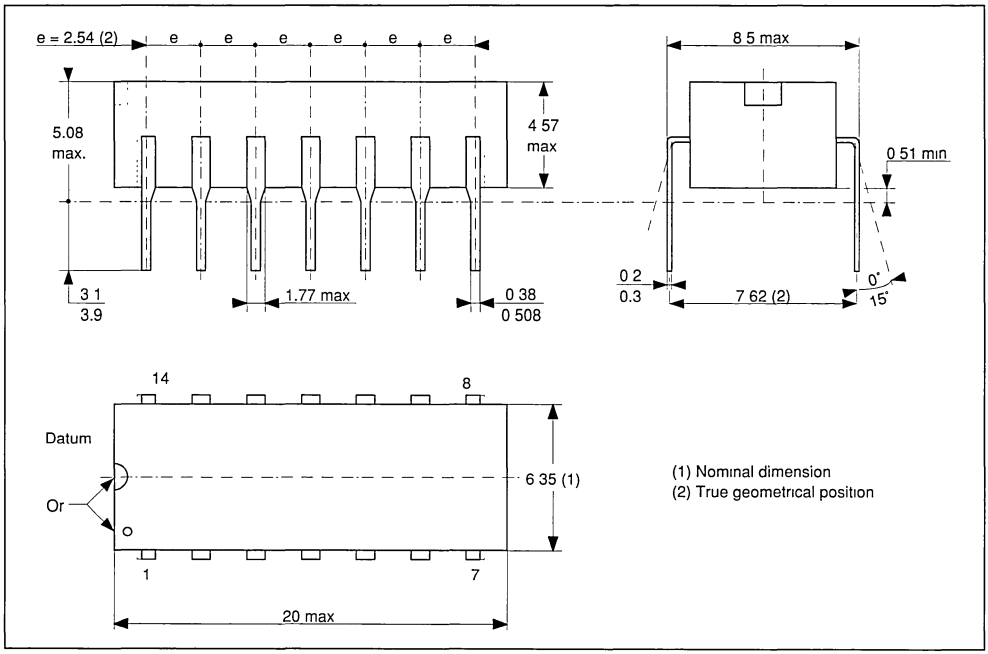


Figure 9 : Slew Rates versus Supply Voltage.

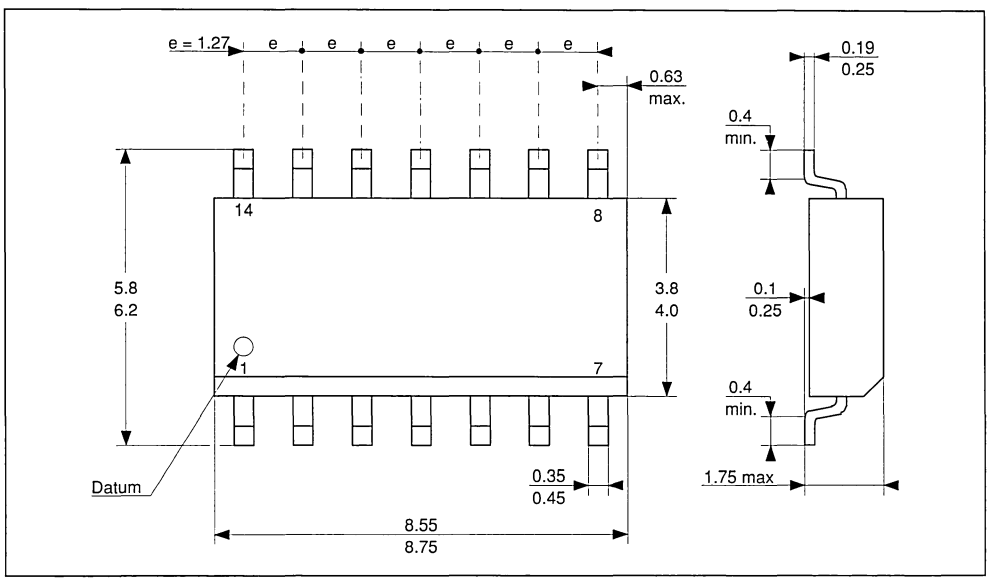


PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



14 PINS - PLASTIC MICROPACKAGE (SO)



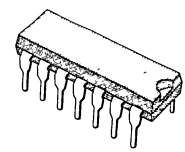
DATASHEETS

COMPARATORS

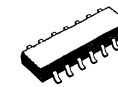
MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

PRELIMINARY DATA

- EXTREMELY LOW SUPPLY CURRENT : 11µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

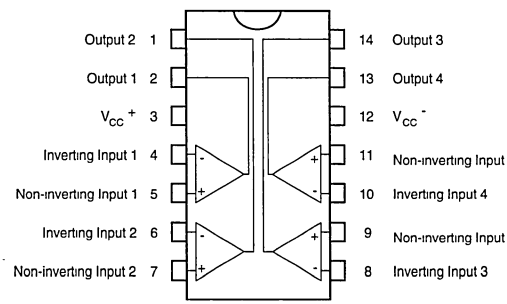
The TS339 is a micropower CMOS quad voltage comparator with extremely low consumption of 11µA typ / comparator (20 times less than bipolar LM339). Similar performances are offered by the quad micropower comparator TS3704 with a push-pull CMOS output.
Thus response times remain similar to the LM339.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS339C	0°C to + 70°C	•	•	•
TS339I	- 40°C to + 105°C	•	•	•
TS339M	- 55°C to + 125°C	•	•	•
Example : TS339CN				

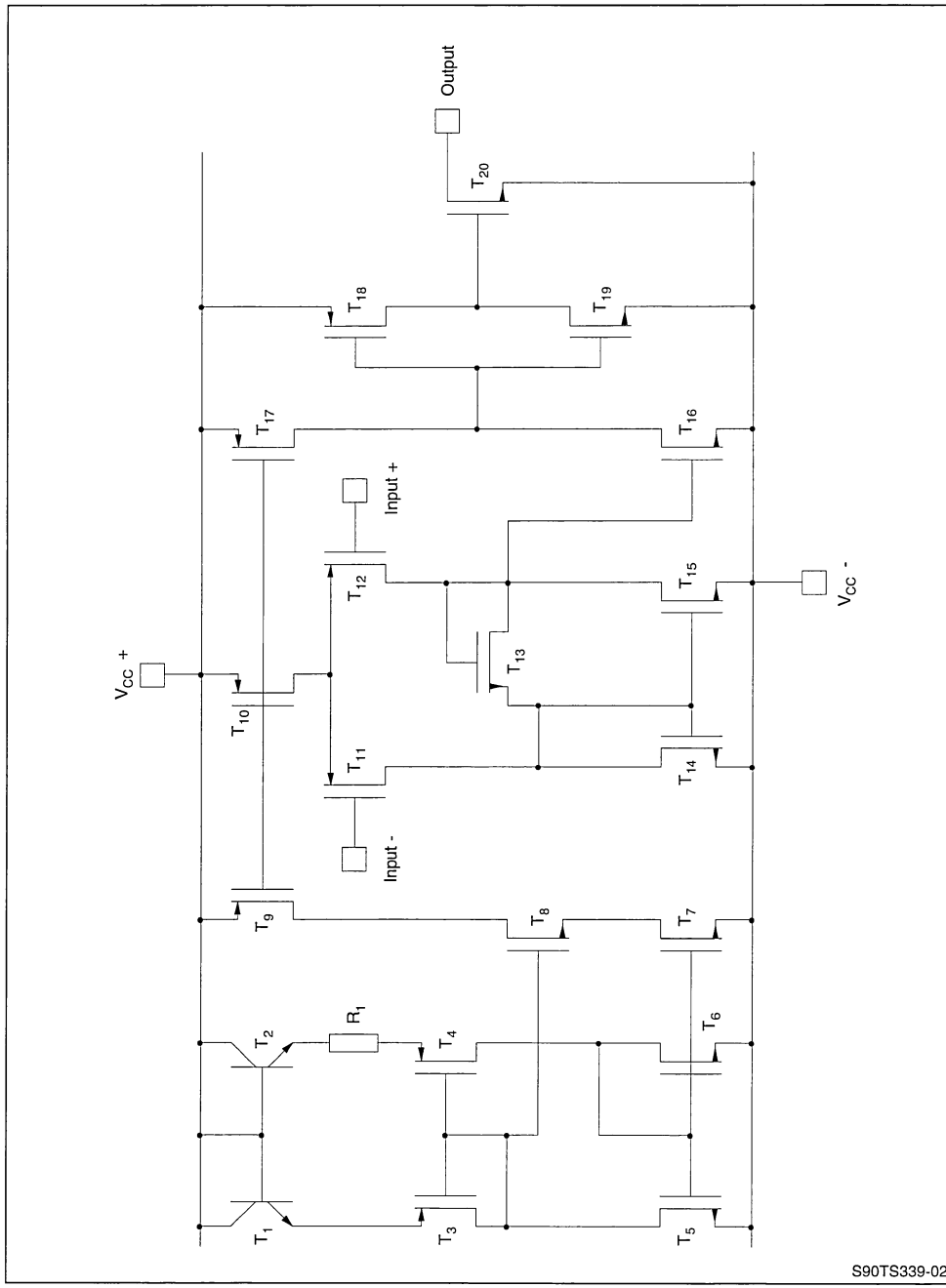
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS339-01

SCHEMATIC DIAGRAM (for 1/4 TS339)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage (Note 1)		18	V
V_{id}	Differential Input Voltage (Note 2)		± 18	V
V_i	Input Voltage (Note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS339C TS339I TS339M	0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range		- 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2 Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.
4 Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage Range	TS339C,I TS339M	3* to 16 4 to 16	V
V_{ic}	Common Mode Input Voltage		0 to V_{CC}^+ -1.5	V

* For selected devices only

ELECTRICAL CHARACTERISTICS

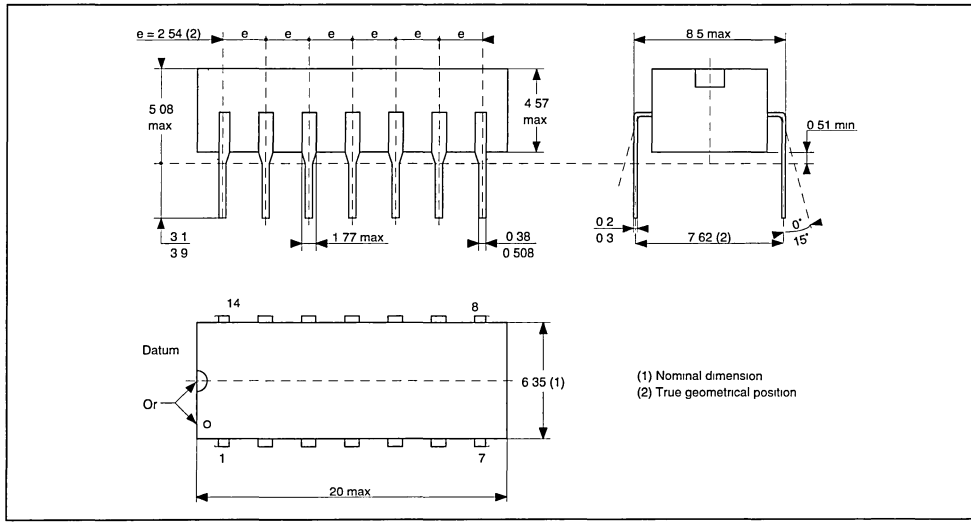
V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{AMB} = 25°C
(unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (V_{IC} = $V_{ICR\ Min}$, V_{CC}^+ = 5V to 10V), (note 1)		1.4	5	mV
I_{io}	Input Offset Current		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Voltage Range	0 to V_{CC} - 1.2 V			V
CMR	Common-mode Rejection Ratio (V_{IC} = V_{ICRMIN})		75		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = +5V to +10V)		85		dB
I_{OH}	High Level Output Current (V_{id} = 1V, V_{oh} = +5V)		2	40	nA
V_{OL}	Low Level Output Voltage (V_{id} = 1V, I_{ol} = 6mA)		350	400	mV
I_{CC}	Supply Current (4 comparators) - no load - Outputs low		44	80	µA
t_{PHL}	Response Time High to Low V_{ic} = 0V, f = 10kHz, C_L = 15pF, Overdrive 5mV TTL Input		 2.9 0.16		µs
t_{PLH}	Response Time Low to High V_{ic} = 0V, f = 10kHz, C_L = 15pF, Overdrive 5mV TTL Input		 1.5 0.8		µs
t_{THL}	Transition Time High to Low f = 10kHz, C_L = 15pF, Overdrive 50mV		 20		ns

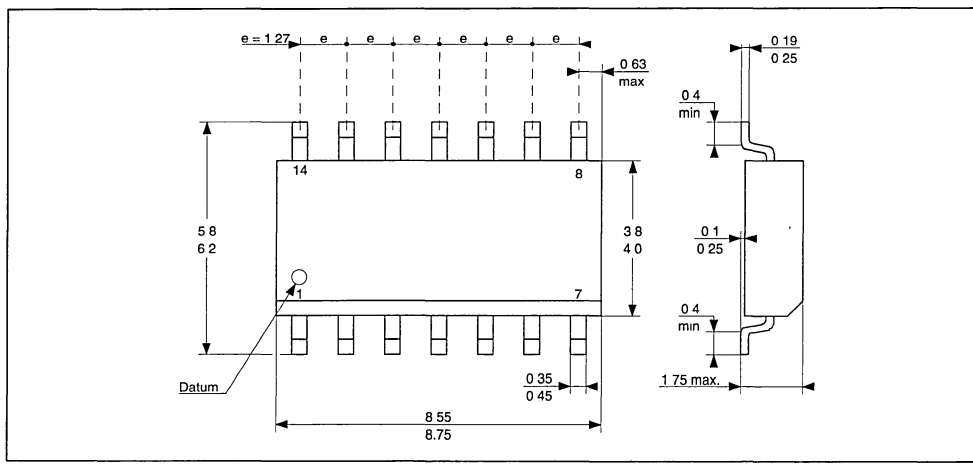
Note : 1.The specified offset voltage is the maximun value required to drive the output up to 4 5V or down to 0 3V.

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP

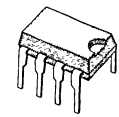


14 PINS - PLASTIC MICROPACKAGE (SO)



LOW POWER DUAL CMOS VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 3V TO 16V OR ± 1.5V TO ± 8V
- VERY LOW SUPPLY CURRENT :0.1mA/COMP INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150mV TYP
- OUTPUT COMPATIBLE WITH TTL, MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 200ns TYP FOR TTL LEVEL INPUT STEP



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

DESCRIPTION

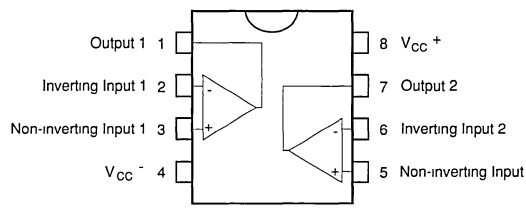
These devices consist of two independent precision voltage comparators, designed to operate with single or dual supplies.
These differential comparators use the SGS-THOMSON silicon lin MOS process giving them an excellent consumption-speed ratio.
These devices are ideally suited for low consumption applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS372C	0°C to + 70°C	•	•	•
TS372I	- 40°C to + 105°C	•	•	•
TS372M	- 55°C to + 125°C	•	•	•
Example : TS372CN				

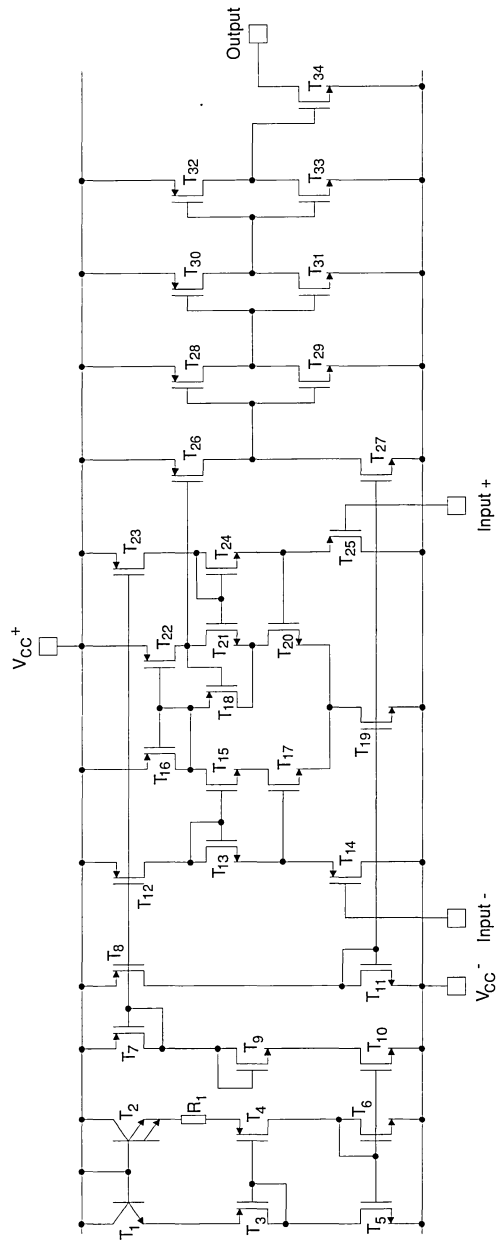
PIN CONNECTIONS (Top view)

DIP8 - CERDIP 8 - SO8



S90TS372-01

SCHEMATIC DIAGRAM (for 1/2 TS372)



S90TS372-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
	Duration of Output Short-Circuit to GND (Note 4)	Unlimited	
T_{oper}	Operating Free-Air Temperature Range TS372C TS372I TS372M	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage Range	3 to 16	V

Notes : 1 All voltage values, except differential voltage, are with respect to network ground terminal.
2 Differential voltages are the non-inverting input terminal with respect to the inverting input terminal
3 The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

ELECTRICAL CHARACTERISTICS AT SPECIFIED FREE-AIR TEMPERATURE, V_{CC}^+ = 5V

(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (V_{IC} = $V_{ICR\ Min}$ - Note 1) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$		 2	 10 12	mV
I_{io}	Input Offset Current (Note 1) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M		 1	 100 200	pA
I_{ib}	Input Bias Current T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M		 1	 150 300	pA
V_{ICR}	Common-mode Input Voltage Range T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M	 0 to V_{CC} - 2 0 to V_{CC} - 2.25 0 to V_{CC} - 2.5			V
I_{OH}	High Level Output Current (V_{ID} = 1V) T_{AMB} = 25°C V_{OH} = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$ V_{OH} = 15V		 0.1	 1	nA µA
V_{OL}	Low Level Output Voltage (V_{ID} = - 1V, I_{OL} = 4mA) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$		 100	 400 700	mV
I_{OL}	Low Level Output Current T_{AMB} = 25°C, V_{ID} = - 1V, V_{OL} = 1.5V	 6	 45		mA
I_{CC}	Supply Current (two comparators) T_{AMB} = 25°C, V_{ID} = - 1 V, no load		 0.3	 0.75	mA

SWITCHING CHARACTERISTICS (V_{CC}^+ = 5V, T_{AMB} = 25°C)

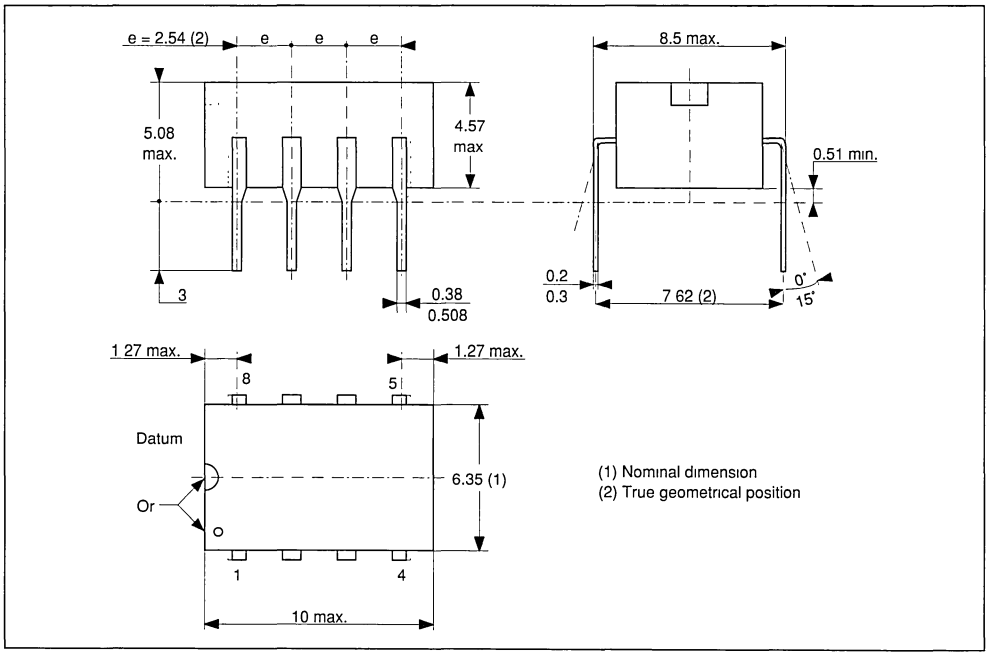
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RE}	Response Time (R_L = 5.1kΩ connected to 5V, C_L = 15pF - Note2) • 100mV input step with 5mV overdrive • TTL level input step		 600 200		ns

Notes : 1 The offset voltage and offset current which are given, are the maximum values required to drive the output down to 400mV or up to 4V with R_L = 10kΩ to V_{CC}.

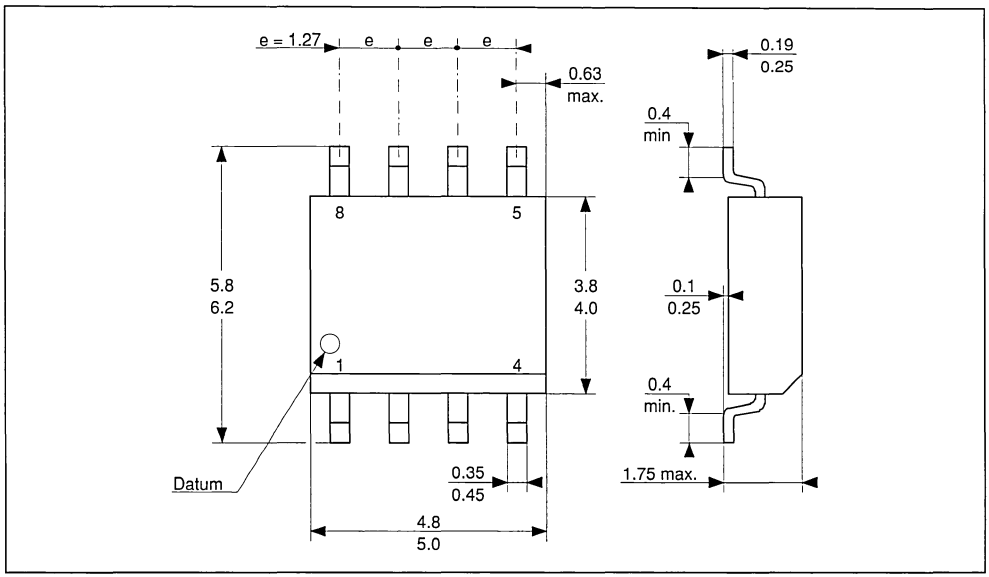
2 The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4V

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

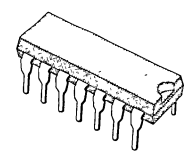


8 PINS - PLASTIC MICROPACKAGE (SO)

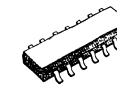


LOW POWER QUAD CMOS VOLTAGE COMPARATORS

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 3V TO 16V OR ± 1.5V TO ± 8V
- VERY LOW SUPPLY CURRENT :0.1mA/COMP INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150mV TYP
- OUTPUT COMPATIBLE WITH TTL, MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 200ns TYP FOR TTL LEVEL INPUT STEP



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

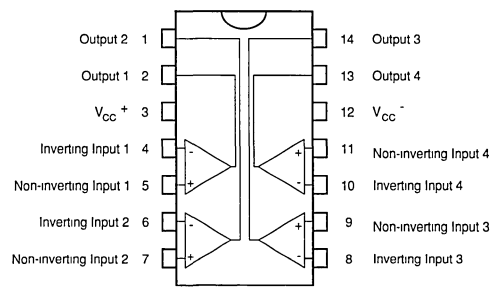
These devices consist of four independent precision voltage comparators, designed to operate with single or dual supplies.
These differential comparators use the SGS-THOMSON silicon lin MOS process giving them an excellent consumption-speed ratio.
These devices are ideally suited for low consumption applications.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS374C	0°C to + 70°C	•	•	•
TS374I	- 40°C to + 105°C	•	•	•
TS374M	- 55°C to + 125°C	•	•	•
Example : TS374CN				

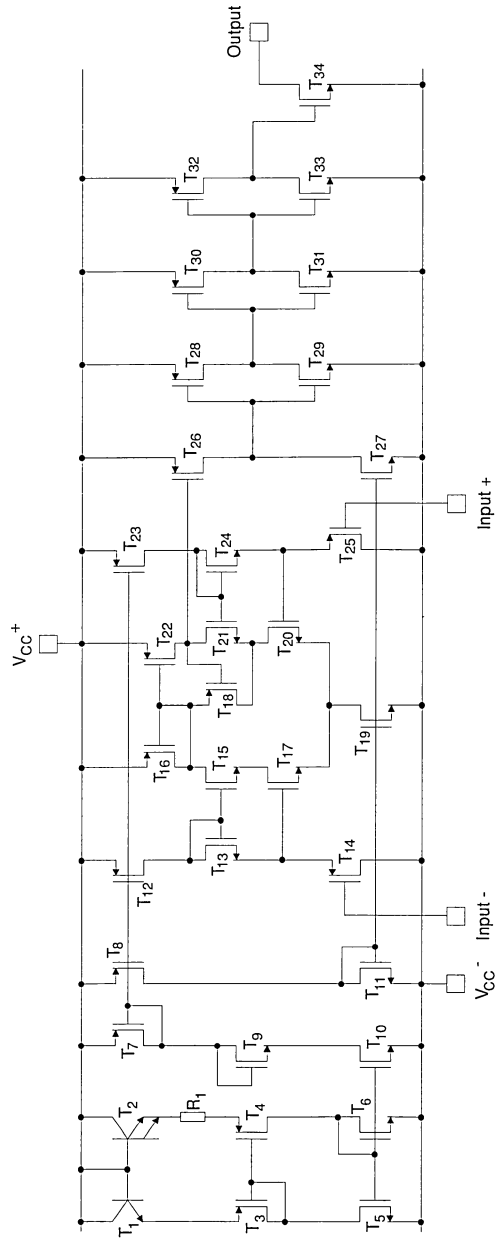
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS374-01

SCHEMATIC DIAGRAM (for 1/4 TS374)



S90TS374-02

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage (Note 1)	18	V
V_{id}	Differential Input Voltage (Note 2)	± 18	V
V_i	Input Voltage (Note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
	Duration of Output Short-Circuit to GND (Note 4)	Unlimited	
T_{oper}	Operating Free-Air Temperature Range TS374C TS374I TS374M	 0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage Range	3 to 16	V

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

ELECTRICAL CHARACTERISTICS AT SPECIFIED FREE-AIR TEMPERATURE, V_{CC}^+ = 5V

(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (V_{IC} = $V_{ICR\ Min}$ - Note 1) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$		 2	 10 12	mV
I_{io}	Input Offset Current (Note 1) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M		 1	 100 200	pA
I_{ib}	Input Bias Current T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M		 1	 150 300	pA
V_{ICR}	Common-mode Input Voltage Range T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$ TS372C TS372I / TS372M	 0 to V_{CC} - 2 0 to V_{CC} - 2.25 0 to V_{CC} - 2.5			V
I_{OH}	High Level Output Current (V_{ID} = 1V) T_{AMB} = 25°C V_{OH} = 5V $T_{MIN} \le T_{AMB} \le T_{MAX}$ V_{OH} = 15V		 0.1	 1	 nA µA
V_{OL}	Low Level Output Voltage (V_{ID} = - 1V, I_{OL} = 4mA) T_{AMB} = 25°C $T_{MIN} \le T_{AMB} \le T_{MAX}$		 100	 400 700	mV
I_{OL}	Low Level Output Current T_{AMB} = 25°C, V_{ID} = - 1V, V_{OL} = 1.5V	 6	 45		mA
I_{CC}	Supply Current (four comparators) T_{AMB} = 25°C, V_{ID} = - 1 V, no load		 0.6	 1	mA

SWITCHING CHARACTERISTICS (V_{CC}^+ = 5V, T_{AMB} = 25°C)

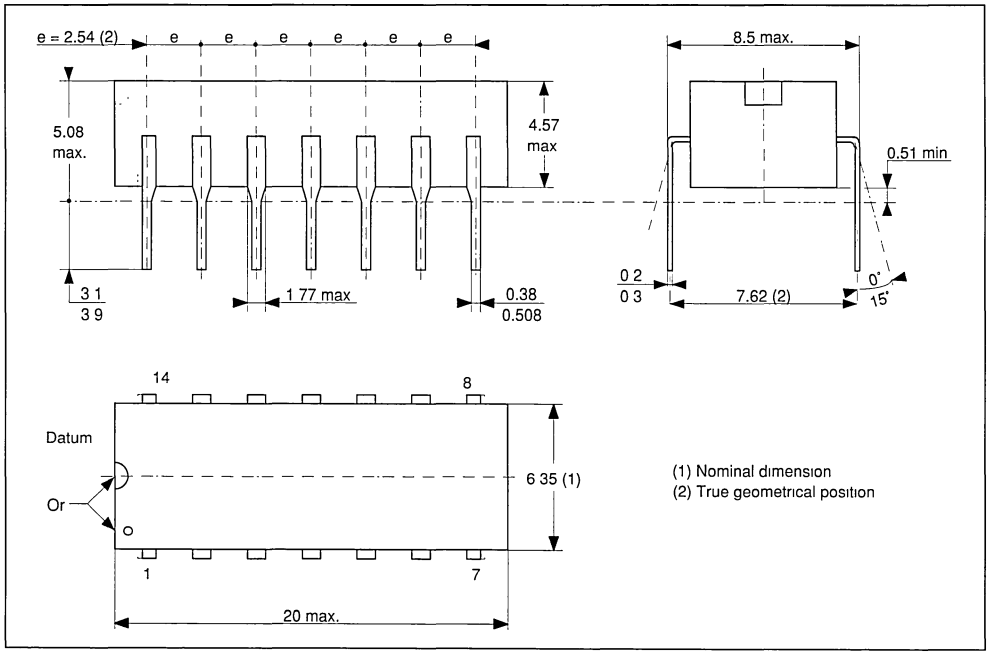
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RE}	Response Time (R_L = 5.1kΩ connected to 5V, C_L = 15pF - Note2) • 100mV input step with 5mV overdrive • TTL level input step		 600 200		ns

Notes : 1 The offset voltage and offset current which are given, are the maximum values required to drive the output down to 400mV or up to 4V with R_L = 10kΩ to V_{CC}.

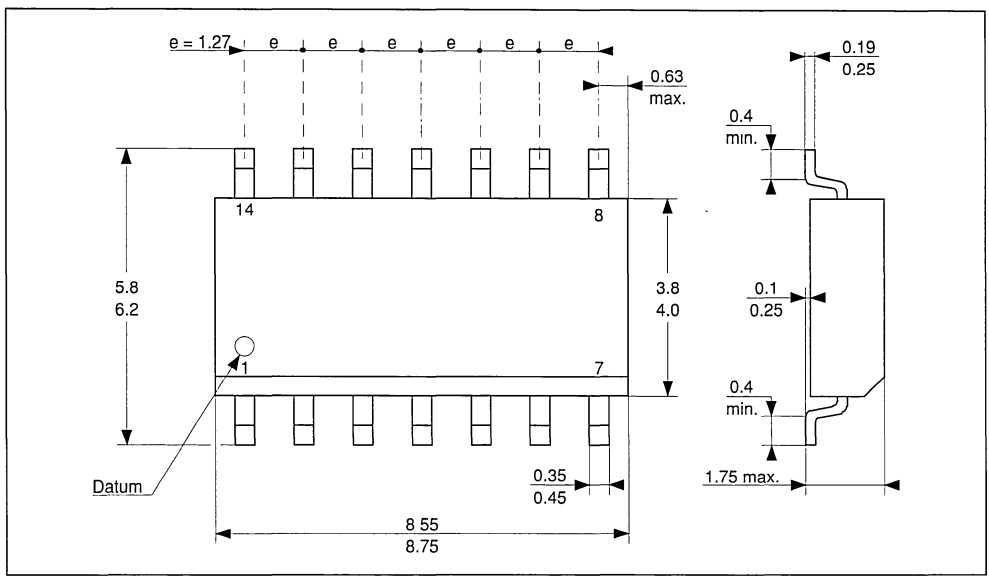
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4V.

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



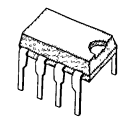
14 PINS - PLASTIC MICROPACKAGE (SO)



MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

PRELIMINARY DATA

- EXTREMELY LOW SUPPLY CURRENT : 11µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

DESCRIPTION

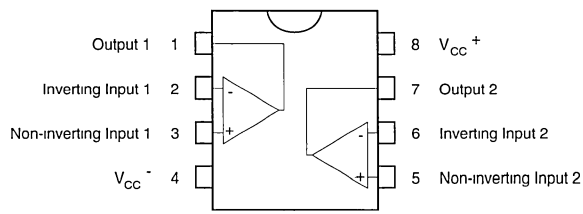
The TS393 is a micropower CMOS dual voltage comparator with extremely low consumption of 11 µA typ / comparator (20 times less than bipolar LM393). Similar performances are offered by the dual micropower comparators TS3702 with a push-pull CMOS output.
Thus response times remain similar to the LM393.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS393C	0°C to + 70°C	•	•	•
TS393I	- 40°C to + 105°C	•	•	•
TS393M	- 55°C to + 125°C	•	•	•
Example : TS393CN				

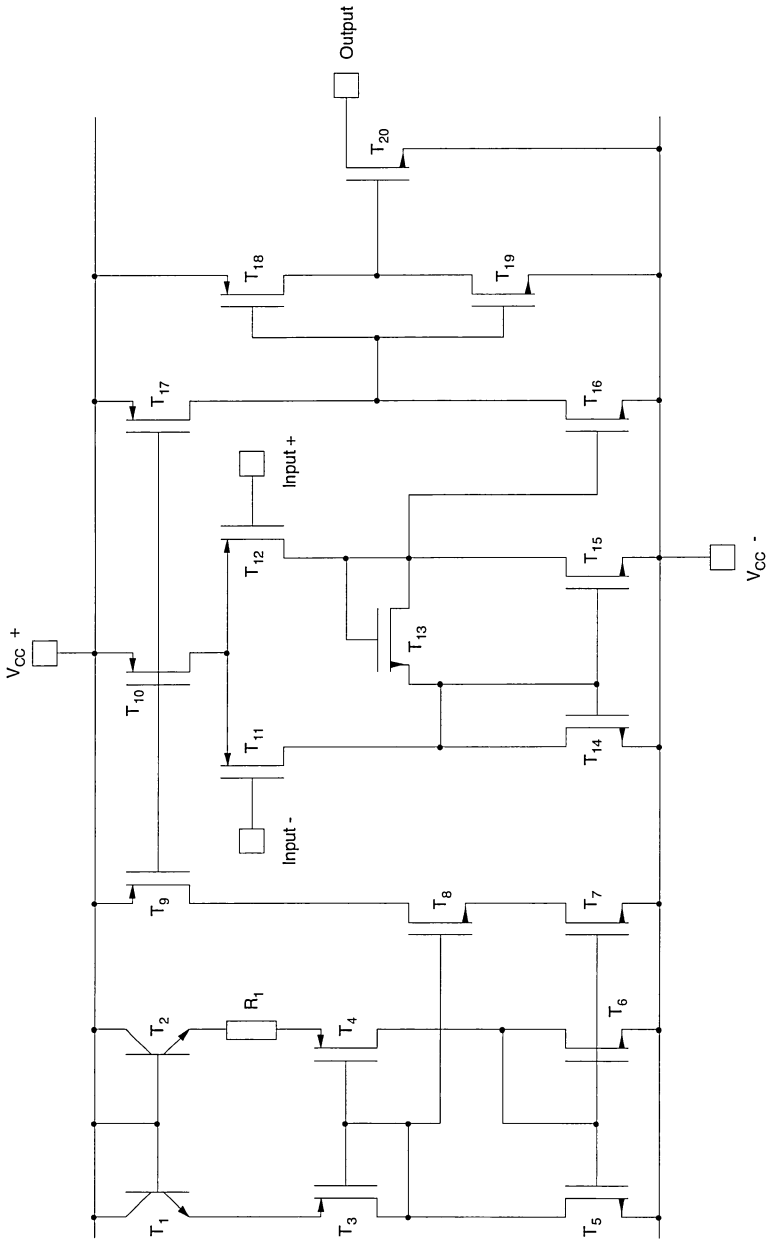
PIN CONNECTIONS (Top view)

DIP8 - CERDIP 8 - SO8



S90TS393-01

SCHEMATIC DIAGRAM (for 1/2 TS393)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage (Note 1)		18	V
V_{id}	Differential Input Voltage (Note 2)		± 18	V
V_i	Input Voltage (Note 3)		18	V
V_O	Output Voltage		18	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS393C TS393I TS393M	0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range		- 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage Range	TS393C,I TS393M	3* to 16 4 to 16	V
V_{ic}	Common Mode Input Voltage		0 to V_{CC}^+ -1.5	V

* For selected devices only

ELECTRICAL CHARACTERISTICS

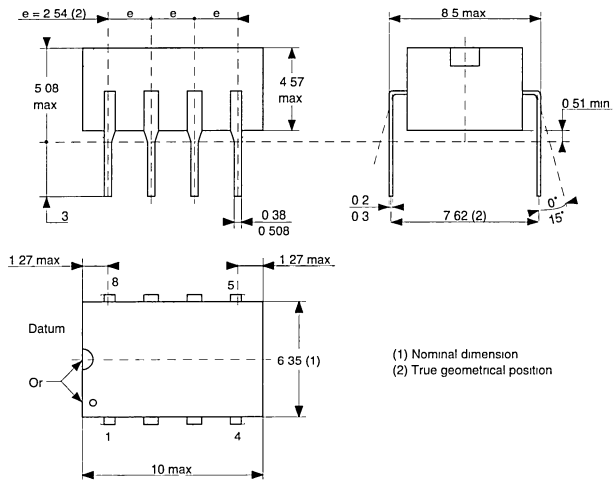
V_{CC}^+ = 5V, V_{CC}^- =0V, T_{AMB}=25°C
(unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (V_{IC} = $V_{ICR\ Min}$, V_{CC}^+ = 5V to 10V), (note 1)		1.4	5	mV
I_{io}	Input Offset Current		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Voltage Range	0 to V_{CC} - 1.2 V			V
CMR	Common-mode Rejection Ratio (V_{IC}= V_{ICRMIN})		71		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = +5V to +10V)		80		dB
I_{OH}	High Level Output Current (V_{id} = 1V, V_{oh} = +5V)		2	40	nA
V_{OL}	Low Level Output Voltage (V_{id} = 1V , I_{ol} = 6mA)		350	400	mV
I_{CC}	Supply Current (2 comparators) - no load - Outputs low		22	40	µA
t_{PHL}	Response time high to low V_{ic} = 0V, f = 10kHz, C_L = 15 pF, Overdrive 5mV TTL Input		 2.7 0.16		µs
t_{PLH}	Response time low to high V_{ic} = 0V, f = 10kHz, C_L = 15 pF, Overdrive 5mV TTL Input		 1.5 0.7		µs
t_{THL}	Transition Time High to Low f = 10kHz, C_L = 15 pF, Overdrive 50mV		 20		ns

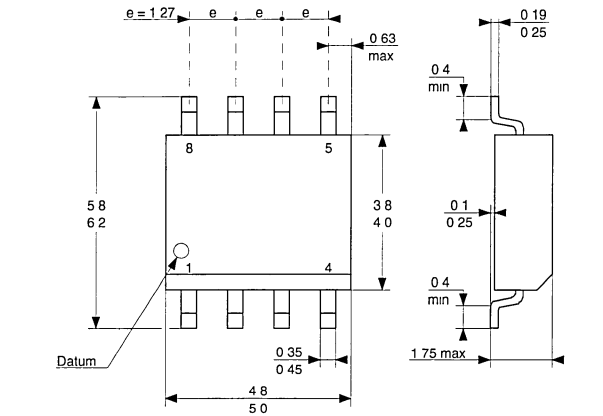
Note : 1.The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



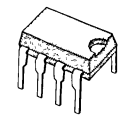
8 PINS - PLASTIC MICROPACKAGE SO



MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

PRELIMINARY DATA

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)

DESCRIPTION

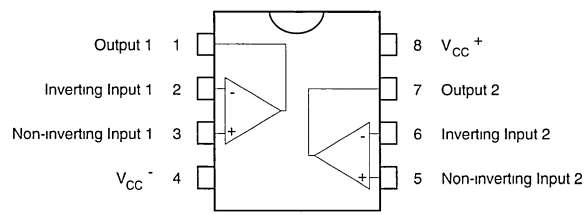
The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9 µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.
Thus response times remain similar to the LM393.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS3702C	0°C to + 70°C	•	•	•
TS3702I	- 40°C to + 105°C	•	•	•
TS3702M	- 55°C to + 125°C	•	•	•
Example : TS3702CN				

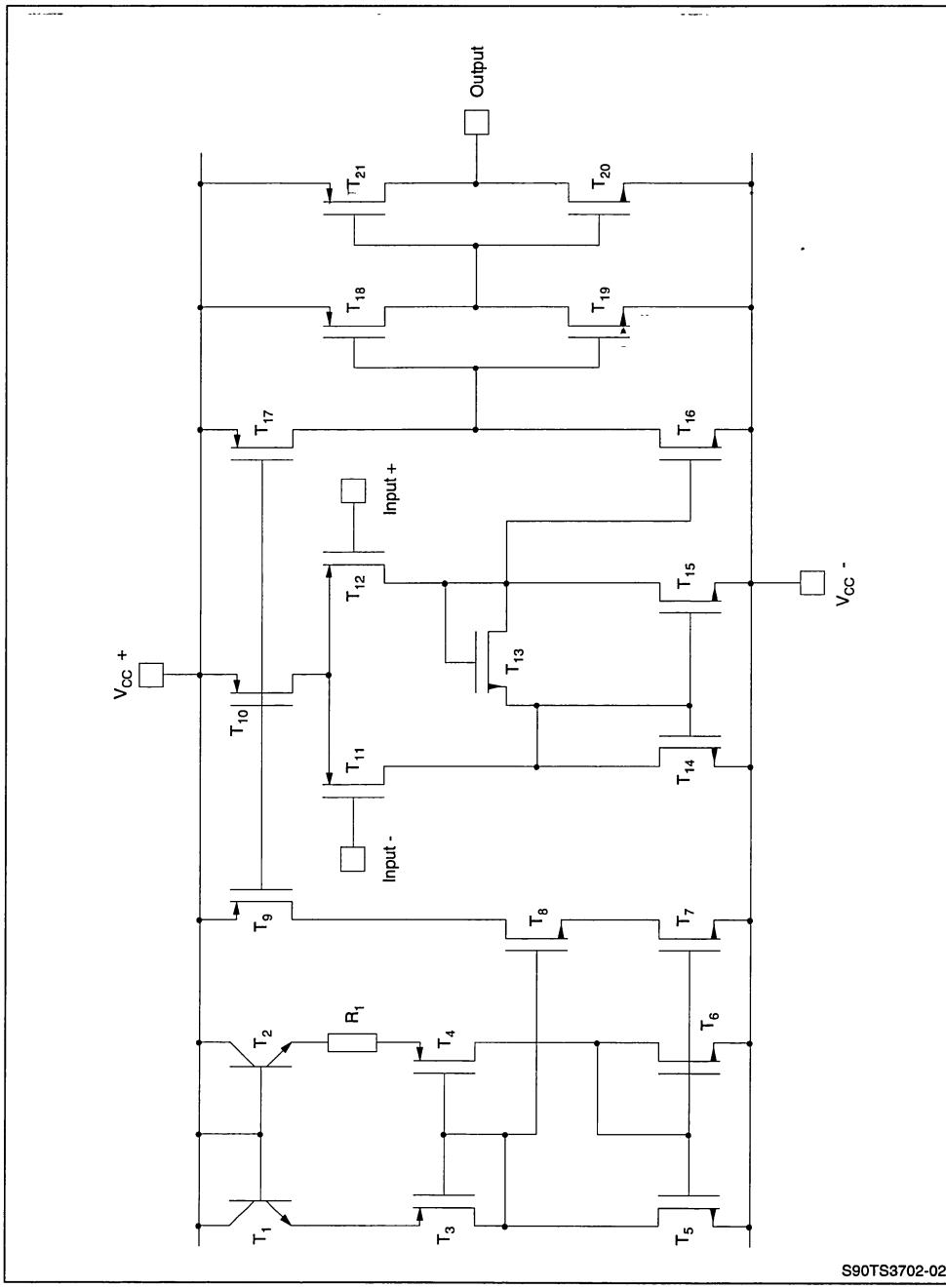
PIN CONNECTIONS (Top view)

DIP8 - CERDIP 8 - SO8



S90TS3702-01

SCHEMATIC DIAGRAM (for 1/2 TS3702)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage (Note 1)		16	V
V_{id}	Differential Input Voltage (Note 2)		± 16	V
V_i	Input Voltage (Note 3)		16	V
V_O	Output Voltage		16	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS3702C TS3702I TS3702M	0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range		- 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage Range	TS3702C,I TS3702M	3* to 14 4 to 14	V
V_{ic}	Common Mode Input Voltage		0 to V_{CC}^+ -1.5	V

* For selected devices only

ELECTRICAL CHARACTERISTICS

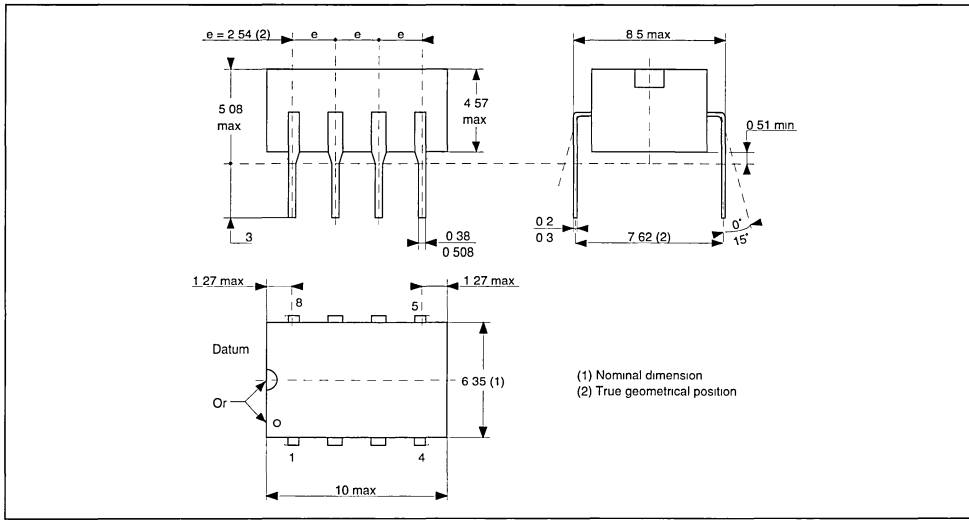
V_{CC}^+ = 5V, V_{CC}^- =0V, T_{AMB}=25°C
(unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (V_{IC} = $V_{ICR\ Min}$, V_{CC}^+ = 5V to 10V), (note 1)		1.2	5	mV
I_{io}	Input Offset Current		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Voltage Range	0 to V_{CC} - 1.2 V			V
CMR	Common-mode Rejection Ratio (V_{IC} = V_{ICRMIN})		82		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = +5V to +10V)		90		dB
V_{oh}	High Level Output Voltage (V_{id} = 1V , I_{oh} = -4mA)	4.5	4.7		V
V_{OL}	Low Level Output Voltage (V_{id} = -1V , I_{ol} = 4mA)		220	300	mV
I_{CC}	Supply Current (2 comparators) - no load - Outputs low		18	40	µA
t_{PHL}	Response time high to low V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive 5mV TTL Input		 3.0 0.17		µs
t_{PLH}	Response time low to high V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive 5mV TTL Input		 1.9 0.8		µs
t_f	Fall time f = 10kHz, C_L = 50pF, Overdrive 50mV		30		ns
t_r	Rise time f = 10kHz, C_L = 50pF, Overdrive 50mV		70		ns

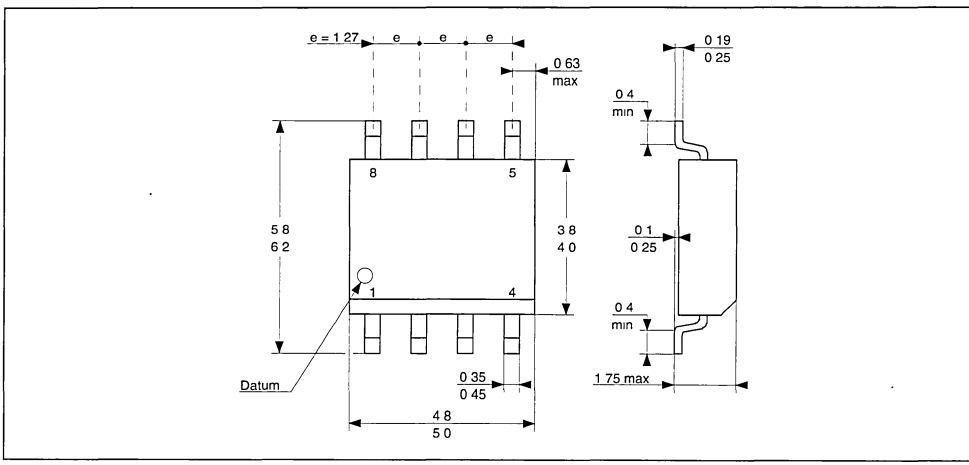
Note : 1.The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



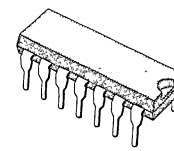
8 PINS - PLASTIC MICROPACKAGE SO



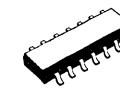
MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

PRELIMINARY DATA

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT: 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

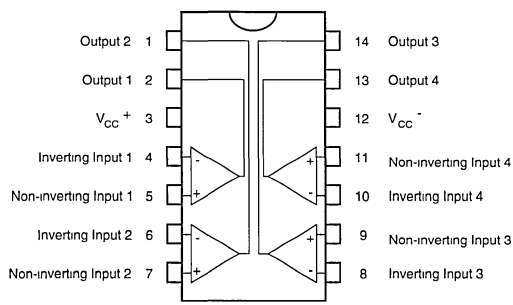
The TS3704 is a micropower CMOS quad voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.
Thus response times remain similar to the LM339.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TS3704C	0°C to + 70°C	•	•	•
TS3704I	- 40°C to + 105°C	•	•	•
TS3704M	- 55°C to + 125°C	•	•	•
Example : TS3704CN				

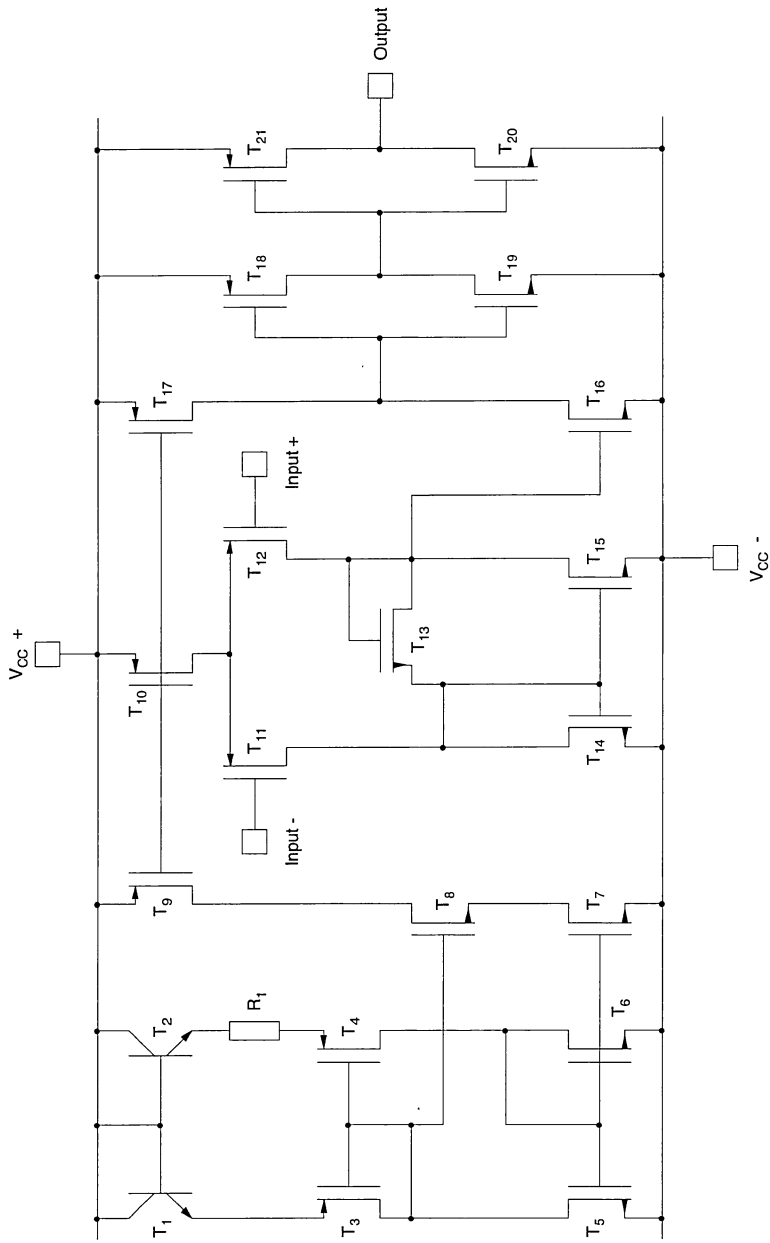
PIN CONNECTIONS (Top view)

DIP14 - CERDIP 14 - SO14



S90TS3704-01

SCHEMATIC DIAGRAM (for 1/4 TS3704)



S90TS3704-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage (Note 1)		16	V
V_{id}	Differential Input Voltage (Note 2)		± 16	V
V_i	Input Voltage (Note 3)		16	V
V_O	Output Voltage		16	V
I_O	Output Current		20	mA
T_{oper}	Operating Free-Air Temperature Range	TS3704C TS3704I TS3704M	0 to + 70 - 40 to + 105 - 55 to + 125	°C
T_{stg}	Storage Temperature Range		- 65 to + 150	°C

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the postive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}^+	Supply Voltage Range	TS3704C,I TS3704M	3* to 14 4 to 14	V
V_{ic}	Common Mode Input Voltage		0 to V_{CC}^+ -1.5	V

* For selected devices only

ELECTRICAL CHARACTERISTICS

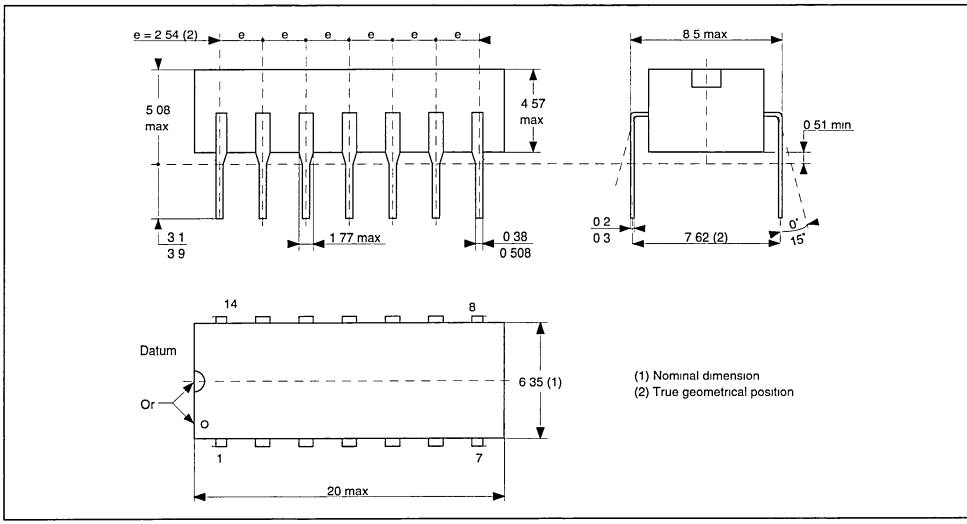
$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{AMB} = 25°C$
(unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{IC} = V_{ICR\ Min.}$, $V_{CC}^+ = 5V$ to 10V), (note 1)		1.2	5	mV
I_{io}	Input Offset Current		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Voltage Range	0 to V_{CC} - 1.2 V			V
CMR	Common-mode Rejection Ratio ($V_{IC} = V_{ICRMIN}$)		78		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = +5V$ to +10V)		92		dB
V_{oh}	High Level Output Current ($V_{id} = 1V$, $I_{oh} = -4mA$)	4.5	4.7		V
V_{OL}	Low Level Output Current ($V_{id} = -1V$, $I_{ol} = 4mA$)		234	300	mV
I_{CC}	Supply Current (4 comparators) - no load - Outputs low		36	80	µA
t_{PHL}	Response time high to low $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive 5mV TTL Input		 2.3 0.17		µs
t_{PLH}	Response time low to high $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive 5mV TTL Input		 1.3 0.8		µs
t_f	Fall time f = 10kHz, $C_L = 50pF$, Overdrive 50mV		30		ns
t_r	Rise time f = 10kHz, $C_L = 50pF$, Overdrive 50mV		70		ns

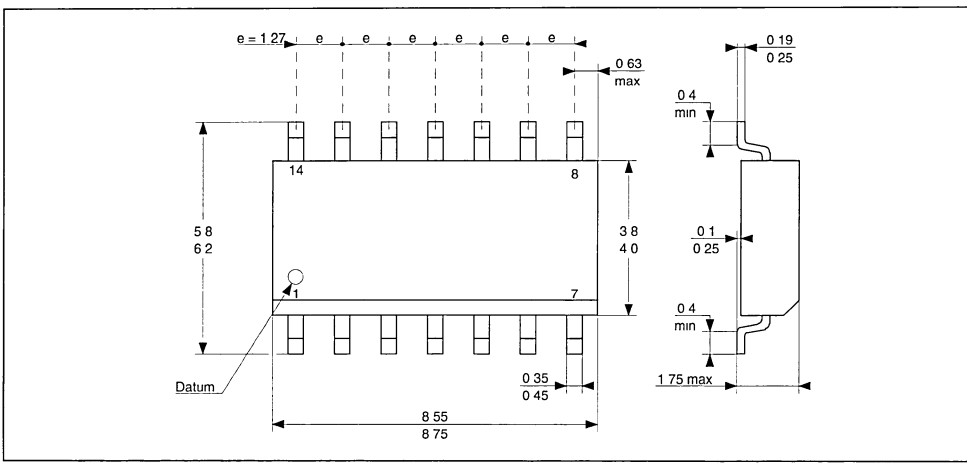
Note : 1.The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



14 PINS - PLASTIC MICROPACKAGE (SO)



DATASHEETS

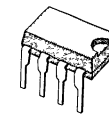
TIMERS

SGS-THOMSON MICROELECTRONICS

TS555C,I,M

LOW POWER SINGLE CMOS TIMERS

- VERY LOW POWER CONSUMPTION : 100µA typ at V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555
- VOLTAGE RANGE : +2V to +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : 10^{12} Ω
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

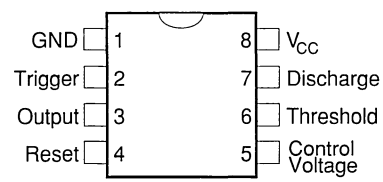
DESCRIPTION

The TS555 is a single CMOS timer which offers very low consumption ($I_{CC(TYP)}$ TS555 = 100µA $I_{CC(TYP)}$ NE555 = 3mA) and high frequency ($f_{(MAX)}$ TS555 = 2.7 MHz - $f_{(MAX)}$ NE555 = 0.1 MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.
The TS555 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE555.
Timing capacitors can also be minimized due to high input impedance (10^{12} Ω).

ORDER CODES

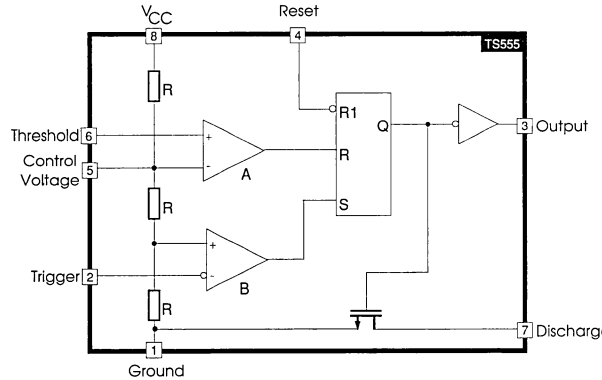
Part Number	Temperature Range	Package		
		N	D	J
TS555C	0 to +70°C	●	●	●
TS555I	-40 to +105°C	●	●	●
TS555M	-55 to +125°C	●	●	●
Examples : TS555CD , TS555IN				

PIN CONNECTION (top view)



S90TS555-01

BLOCK DIAGRAM



S90TS555-02

FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified
HIGH ↔ Level Voltage ≥ Max voltage specified
X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range		°C
	TS555C	0 to +70	
	TS555I	-40 to +105	
	TS555M	-55 to +125	
T_{STG}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 65 -	 200 200	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.2 1.1	 1.3 -	 1.4 1.5	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.05 -	 0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.1 -	 0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.5 1.5	 1.9 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 0.67 -	 0.95 1.05	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 110 -	 250 250	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 2.9 2.8	 3.3 -	 3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.2 -	 0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 - -	 0.3 -	 0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 4.4 4.4	 4.6 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 1.36 1.26	 1.67 -	 1.96 2.06	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 170 -	 400 400	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 7.4 7.3	 8 -	 8.6 8.7	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 80mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.9 -	 1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 50mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 1.2 -	 2 2.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -10mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 10.5 10.5	 11 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 3.2 3.1	 4 -	 4.8 4.9	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

DYNAMIC ELECTRICAL CHARACTERISTICS

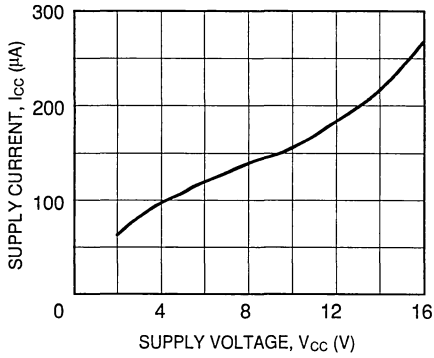
T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS555C - TS555I - TS555M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - R = 10 kΩ , C = 0.1 µF - (Note 1) V_{CC} = +2V V_{CC} = +5V V_{CC} = +12V	 - - -	 1 2 4	 - - -	%
	Timing Shift with supply voltage variations (Monostable) R = 10 kΩ , C = 0.1 µF , V_{CC} = +5V ± 1V	-	0.38	-	%/V
	Timing Shift with temperature $T_{MIN} \leq T_{AMB} \leq T_{MAX}$, V_{CC} = +5V	-	75	-	ppm/°C
f_{MAX}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω , C = 200 pF , V_{CC} = +5V	-	2.7	-	MHz
	Astable frequency accuracy - (Note 2) R_A= R_B = 1kΩ to 100kΩ , C = 0.1µF V_{CC} = +5V V_{CC} = +12V	 - -	 3 3	 - -	%
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 1kΩ to 100kΩ , C = 0.1µF , V_{CC} = +5 to +12V	-	0.1	-	%/V
t_r	Output Rise Time (V_{CC} = +5V , C_{LOAD}= 10pF)	-	25	-	ns
t_f	Output Fall Time (V_{CC} = +5V , C_{LOAD} = 10pF)	-	20	-	ns
t_{PD}	Trigger Propagation Delay (V_{CC} = +5V)	-	100	-	ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)	-	350	-	ns

Notes : 1. See Figure 1
2. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage.



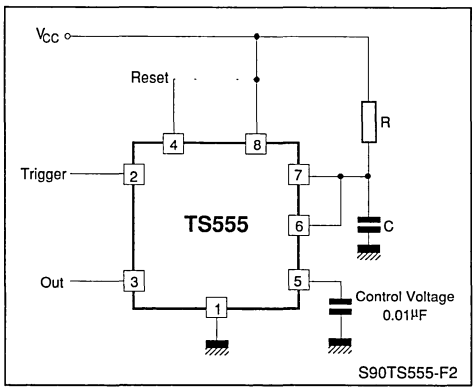
S90TS555-F1

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2.



S90TS555-F2

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH.

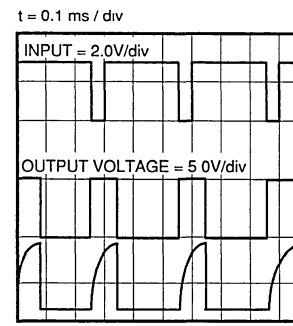
The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3.



S90TS555-F3

ASTABLE OPERATION

When the circuit is connected as shown in figure 4 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 4.

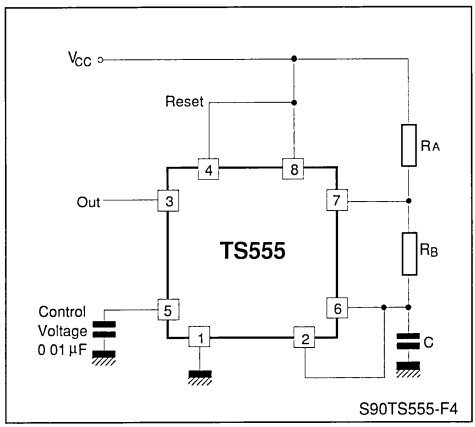
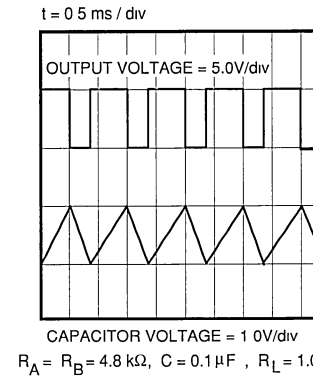
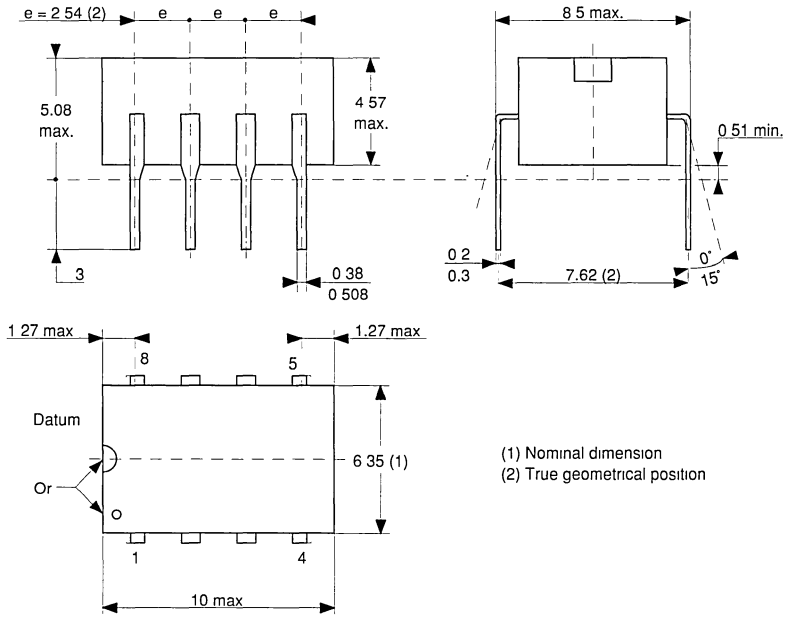


Figure 5.

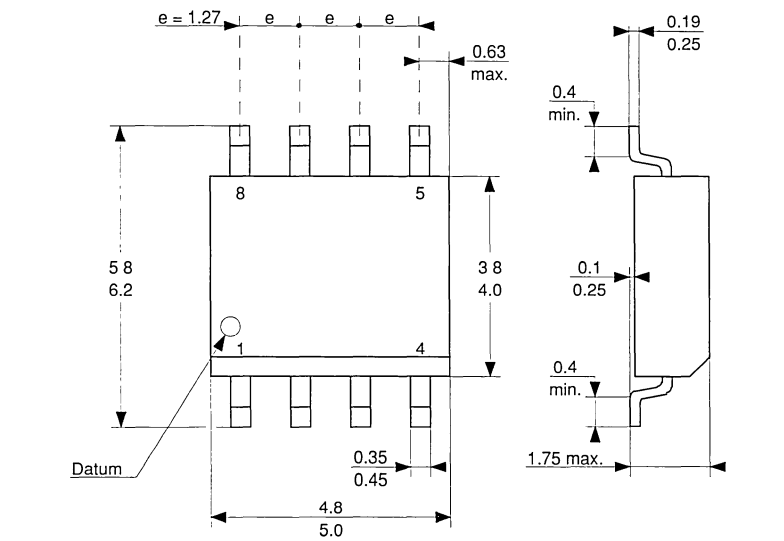


PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



8 PINS PLASTIC MICROPACKAGE (SO)

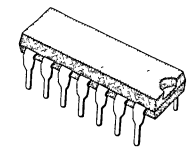


SGS-THOMSON MICROELECTRONICS

TS556C,I,M

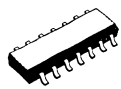
LOW POWER DUAL CMOS TIMERS

- VERY LOW POWER CONSUMPTION : 100µA typ / TIMER AT V_{CC} = 5V
- HIGH MAXIMUM ASTABLE FREQUENCY 2.7MHz
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE556
- VOLTAGE RANGE : +2V TO +18V
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

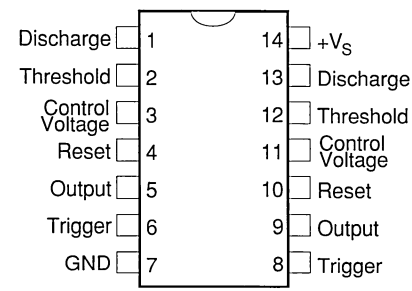
DESCRIPTION

The TS556 is a dual CMOS timer which offers very low consumption ($I_{CC(TYP)}$ TS556 = 200µA $I_{CC(TYP)}$ NE556 = 6mA) and high frequency ($f_{(MAX)}$ TS556 = 2.7MHz - $f_{(MAX)}$ NE556 = 0.1MHz) Thus, either in Monostable or Astable mode, timing remains very accurate.
The TS556 provides reduced supply current spikes during output transitions, which enables the use of lower decoupling capacitors compared to those required by bipolar NE556.
Timing capacitors can also be minimized due to high input impedance ($10^{12}\Omega$).

ORDER CODES

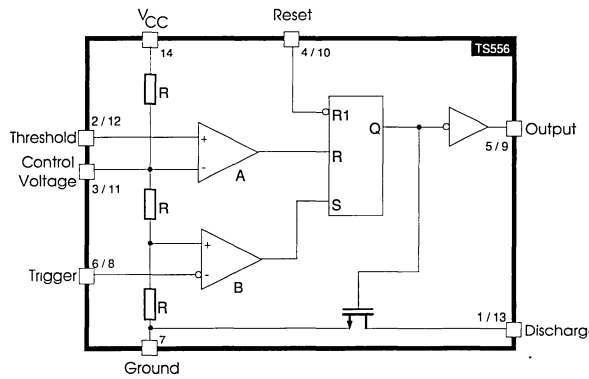
Part Number	Temperature Range	Package		
		N	D	J
TS556C	0 to +70°C	●	●	●
TS556I	-40 to +105°C	●	●	●
TS556M	-55 to +125°C	●	●	●
Examples : TS556CD , TS556IN				

PIN CONNECTION (top view)



S90TS556-01

BLOCK DIAGRAM (1/2 TS556)



S90TS556-02

FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

LOW ↔ Level Voltage ≤ Min voltage specified
HIGH ↔ Level Voltage ≥ Max voltage specified
X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{OPER}	Operating Temperature Range		°C
	TS556C	0 to +70	
	TS556I	-40 to +105	
	TS556M	-55 to +125	
T_{STG}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+2 to +16	V

STATIC ELECTRICAL CHARACTERISTICS

V_{CC} = +2V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 130 -	 400 400	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.2 1.1	 1.3 -	 1.4 1.5	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.05 -	 0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.1 -	 0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.5 1.5	 1.9 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 0.67 -	 0.95 1.05	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 220 -	 500 500	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 2.9 2.8	 3.3 -	 3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.2 -	 0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.3 -	 0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 4.4 4.4	 4.6 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 1.36 1.26	 1.67 -	 1.96 2.06	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

STATIC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +12V , T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
I_{CC}	Supply Current (no load, High and Low States) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 340 -	 800 800	µA
V_{CL}	Control Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 7.4 7.3	 8 -	 8.6 8.7	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 80mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 0.9 -	 1.6 2.0	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 50mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 - -	 1.2 -	 2 2.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -10mA) T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 10.5 10.5	 11 -	 - -	V
V_{TRIG}	Trigger Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 3.2 3.1	 4 -	 4.8 4.9	V
I_{TRIG}	Trigger Current	-	10	-	pA
I_{TH}	Threshold Current	-	10	-	pA
V_{RESET}	Reset Voltage T_{AMB} = + 25 °C $T_{MIN} \le T_{AMB} \le T_{MAX}$	 0.4 0.3	 1.1 -	 1.5 2.0	V
I_{RESET}	Reset Current	-	10	-	pA
I_{DIS}	Discharge Pin Leakage Current	-	1	100	nA

DYNAMIC ELECTRICAL CHARACTERISTICS

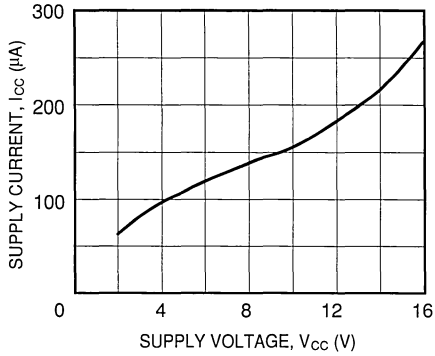
T_{AMB} = +25°C , Reset to V_{CC}
(Unless otherwise specified)

Symbol	Parameter	TS556C - TS556I - TS556M			Unit
		Min	Typ	Max	
	Timing Accuracy (Monostable) - R = 10 kΩ , C = 0.1 µF - (Note 1) V_{CC} = +2V V_{CC} = +5V V_{CC} = +12V	 - - -	 1 2 4	 - - -	%
	Timing Shift with supply voltage variations (Monostable) R = 10 kΩ , C = 0.1 µF , V_{CC} = +5V ± 1V	-	0.38	-	%/V
	Timing Shift with temperature $T_{MIN} \leq T_{AMB} \leq T_{MAX}$, V_{CC} = +5V	-	75	-	ppm/ °C
f_{MAX}	Maximum astable frequency R_A = 470Ω , R_B = 200Ω , C = 200 pF , V_{CC} = +5V	-	2.7	-	MHz
	Astable frequency accuracy - (Note 2) R_A= R_B = 1kΩ to 100kΩ , C = 0.1µF V_{CC} = +5V V_{CC} = +12V	 - -	 3 3	 - -	%
	Timing Shift with supply voltage variations (Astable mode) R_A = R_B = 1kΩ to 100kΩ , C = 0.1µF , V_{CC} = +5 to +12V	-	0.1	-	%/V
t_r	Output Rise Time (V_{CC} = +5V , C_{LOAD}= 10pF)	-	25	-	ns
t_f	Output Fall Time (V_{CC} = +5V , C_{LOAD} = 10pF)	-	20	-	ns
t_{PD}	Trigger Propagation Delay (V_{CC} = +5V)	-	100	-	ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)	-	350	-	ns

Notes : 1 See Figure 1
2 See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus Supply Voltage.



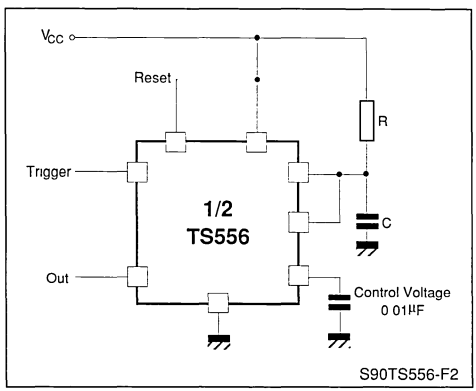
S90TS556-F1

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2.



S90TS556-F2

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4 or 10) and the Trigger terminal (pin 6 or 8) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

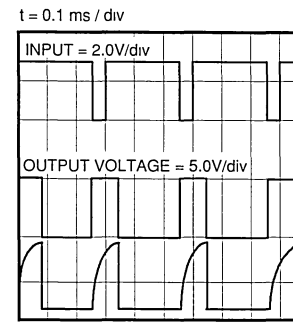
When a negative trigger pulse is applied to the trigger terminal, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R \times C$.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3.



S90TS556-F3

ASTABLE OPERATION

When the circuit is connected as shown in figure 4, it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 4.

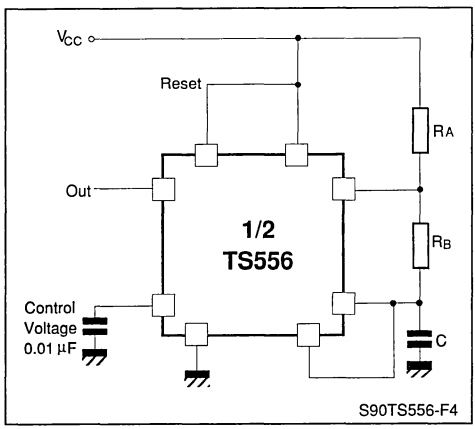
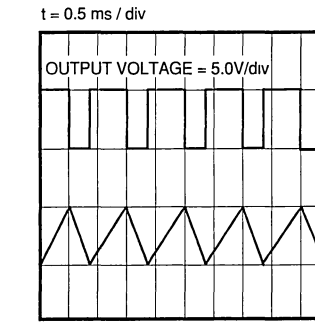
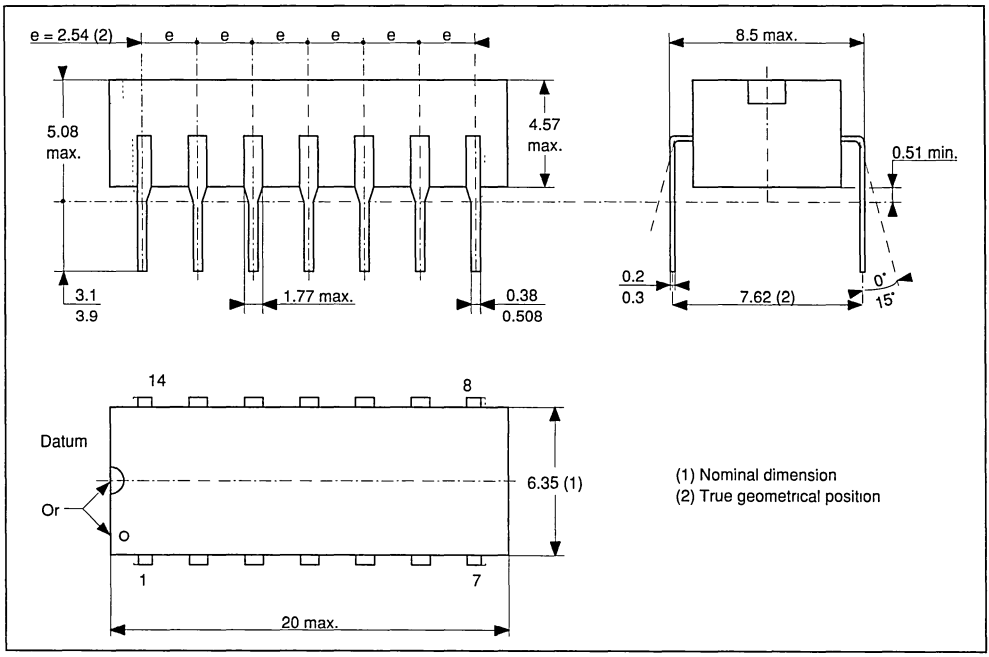


Figure 5.

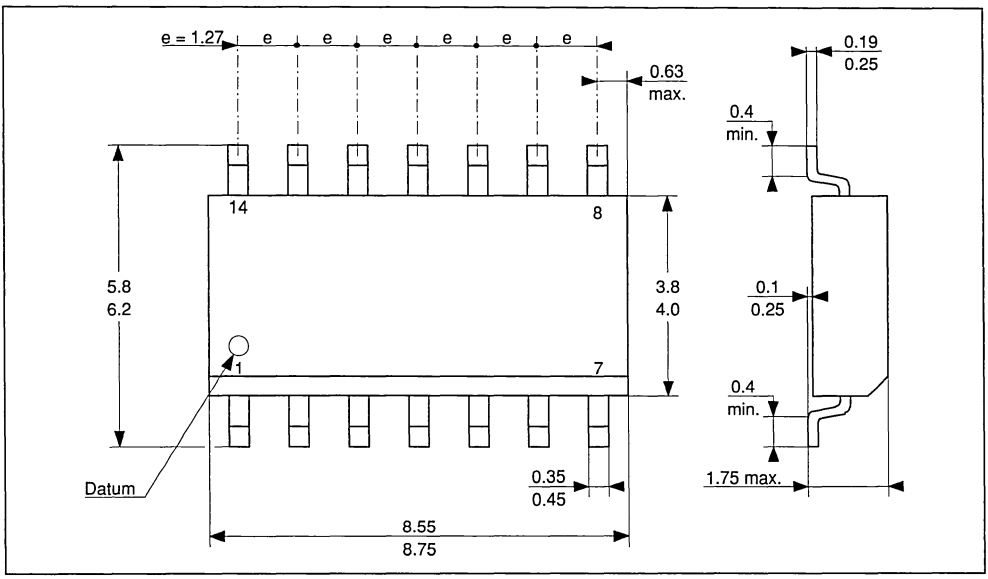


PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



14 PINS PLASTIC MICROPACKAGE (SO)



RELIABILITY REPORT

RELIABILITY REPORT

1. RELIABILITY TEST DESCRIPTION

1.A - ELECTRICAL TESTS (Die oriented tests)

Static life test :

This test was performed to point out die problems connected to the superficial contamination and to the layout structure.

Test conditions :

- V_{CC} = +10 V
- T_{AMB} = 125°C
- T_J = 135°C
- Package = plastic DIL or SO (see Fig1 page 145)

1.B - ENVIRONMENTAL TESTS (Package oriented tests)

To evaluate the moisture resistance and thermomechanical behaviour, we have performed a reliability characterization including the following tests:

- Thermal Humidity with Bias (T.H.B.)
- Pressure Cooker Test (PRESSURE POT)
- Temperature Cycling -55 +150 °C

PERIOD: Year 89

Results are given for all standard linear products

2. ELECTRICAL RELIABILITY TEST RESULTS

TEST CONDITIONS	TIME	SAMPLE SIZE	REJECTS
LIFE TEST : V_{CC} = + 10 V T_{AMB} = 125°C	1000H 2000H	620 280	0 0

3. ENVIRONMENTAL RELIABILITY TEST RESULTS

BIASED MOISTURE LIFE TEST

TEST CONDITIONS	TIME	SAMPLE SIZE	REJECTS
PLASTIC DIL 85°C 85% R.H.	1000H	780	0
SO PACKAGE 85°C 85% R.H.	1000H	580	0

TEST	TEST CONDITIONS	SAMPLE SIZE	FAILURE	NOTE
PRESSURE POT	T_{AMB} = 121°C P = 2.08 ATM T = 168 H	1333 2521	0 0	1 2
TEMPERATURE CYCLING	1000 cycles (T_{AMB}= -55°C to +150°C) 10 min. at extreme temperatures, 5 min. max. transfer time.	950 1000	0 0	1 2

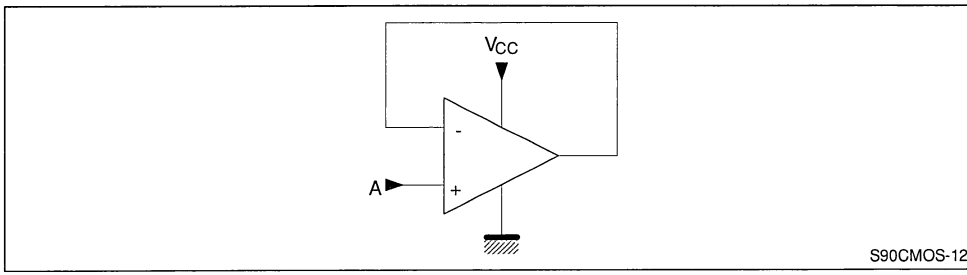
Notes : 1. Plastic DIL Package
2. SO Package

4. FAILURE RATE CALCULATION AT :

- T_J max = 125°C (observed value and at 60% CL)
  $\lambda = 1.01 \times 10^{-6}$F/H
- T_J = 55°C (at 60 % CL) and EA = 1 eV
  λ = 2.5FITS

5. CIRCUIT CONFIGURATION FOR RELIABILITY TESTS

Figure 1 : HTB and THB Life Test
For 50% "A" Connected to V_{CC}
For 50% "A" Connected to 0V
V_{CC} = +10V



When a low number of samples has been employed (as during homologation tests) and when a proper confidence level is required in order to estimate a correct λ value we suggest accepting a value C' obtained by table 2 instead of C = number of failures employed in previous formula (1).

The new value for λ will be :

$$\lambda = \frac{C' \text{ (extracted by table 2)}}{N \times T}$$

Table 2.

NUMBER OF FAILURES	CONFIDENCE LEVEL					
	50%	60%	70%	80%	90%	95%
0	0.693	0.916	1.20	1.66	2.305	2.99
1	1.678	2.022	2.439	2.99	3.89	4.74
2	2.674	3.12	3.615	4 28	5 30	6.30
3	3.672	4 16	4.762	5.50	6.70	7.75
4	4.671	5.25	5.891	6.70	8.00	9.15
5	5.67	6.30	7.005	7.90	9.25	10.50
6	6.669	7.35	8.111	9.10	10.55	11.85
7	7.669	8.40	9.209	10.25	11.75	13.15
8	8.669	9.45	10.30	11.40	13.00	14.45
9	9.668	10.50	11.38	12.50	14.20	15.70
10	10.66	11.55	12.47	13.65	15.40	16.95

APPENDIX : FAILURE RATE CALCULATION

Reliability evaluation of a device means also failure rate (λ) evaluation, both during infant mortality and useful life.

The reliability test used for failure rate evaluation is H.T.R.B.

In its simple form the failure rate is:

$$\lambda = \frac{C}{N \times T}$$

Where :

λ = Failure rate (at a given temperature)

C = Number of failures

N = Number of tested devices

T = Number of test hours

To determine failure rate at other temperature an acceleration factor F must be used.

F is determined, for a given thermal activation energy EA, by the Arrhenius relationship as :

$$F(T_1, T_2) = EXP\left[-\frac{EA}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

Where :

EA = Thermal activation energy (eV)

K = Boltzmann's constant (8.63×10^{-5} eV/°K)

T = Absolute temperature in °K

Then

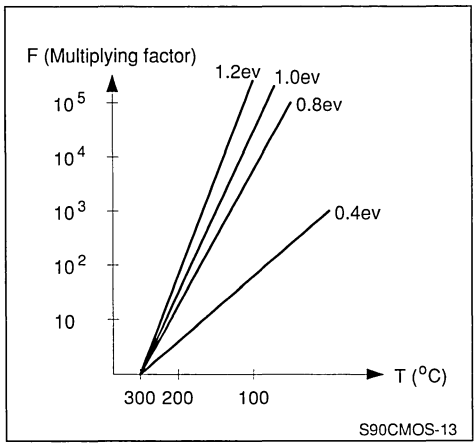
$$\lambda(T_1) = F(T_1, T_2) \times \lambda(T_2)$$

Where :

T1 <T2

Fig. 2 shows temperature derating curves and multiplying factors for temperature reduction.
The various lines correspond to the activation energies associated with the different failure mechanisms involved.

Figure 2 : Arrhenius plot.



TAPE AND REEL SPECIFICATION

TAPE AND REEL PACKING SPECIFICATION FOR SOIC

1 - PURPOSE :

This specification is formulated to provide dimensions, tolerances and characteristics about tape and reel necessary to surface mount components such that they may be automatically placed. This specification covers taping for active surface mount components in SOIC package type.

2 - REFERENCE DOCUMENTS

2 - 1 . "EIA 481-A"

2 - 2 . "IEC 286-3"

2 - 3 . "Special customer request"

3 - GENERAL

3 - 1 . Reel material = Plastic antistatic or conductive

3 - 2 . Cavity tape material = Black conductive (less than $10^5\Omega$ per square)

3 - 3 . Cover tape material = Transparent antistatic (less than $10^{10}\Omega$ per square) or conductive (less than $10^5\Omega$ per square)

4 - QUANTITY AND DIMENSIONS

All drawings dimensions are in millimeters.

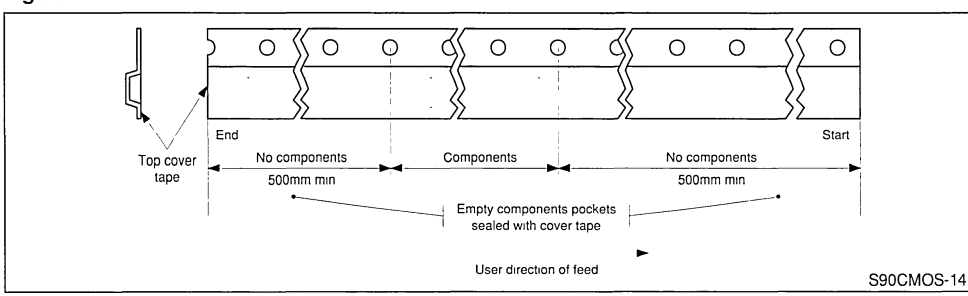
4 - 1 . QUANTITY AND DIMENSIONS - See table 1

Table 1.

PACKAGE	TAPE WIDTH (mm)	QTY / REEL
SO8	12	2500
SO14	16	2500
SO16 (narrow)	16	2500

4 - 2 . LEADER AND TRAINER

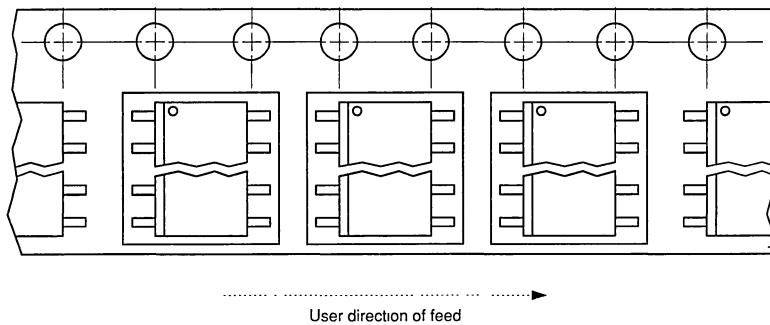
Figure 1.



The trailer end of the tape carrier is secured to the reel.
The devices are oriented with the terminals facing to the bottom of the carrier pocket.

4 - 3 . DEVICES ORIENTATION

Figure 2.



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The devices are oriented in the carrier pocket with pin number 1 adjacent to the sprocket holes.

4 - 4 .OVERALL REEL DIMENSIONS

Figure 3.

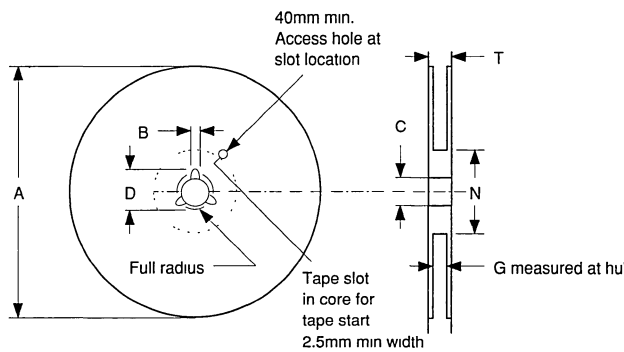

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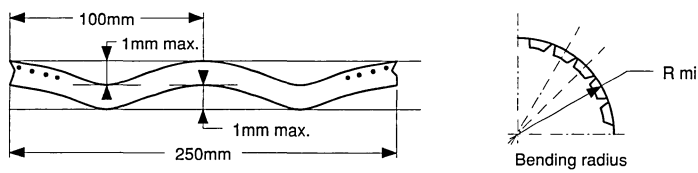
Figure 4.



Camber (top view)
Allowable camber to be 1mm / 100mm nonaccumulative over 250mm

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4 - 4 .OVERALL REEL DIMENSIONS (continued)

Table 2.

Tape Size	A max	B min	C	D min	N min	G	T max	R min
12 mm	330	1.5	13 ± 0.2	20.2	50	12.4 +2/-0	18.4	30
16 mm	330	1.5	13 ± 0.2	20.2	50	12.4 +2/-0	22.4	40

4 - 5 . CARRIER POCKET DIMENSIONS

Figure 5.

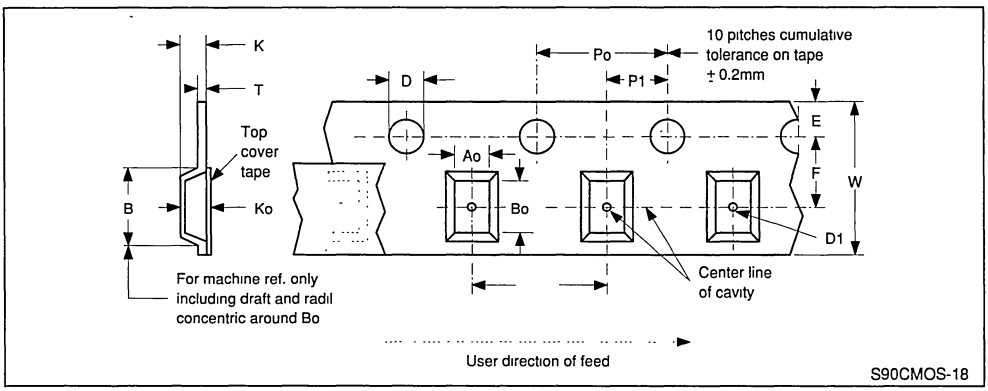

Table 3.

Tape Size	D	E	P_O	T	A_O	B_O	K_O
12 / 16mm	1.5 +0.1/0	1.75 ± 0.1	4 ± 0.1	0.4	See note		

Table 4.

Tape Size	B_1 max	D_1 min	F	K max	P_1	W
12mm	8.2	1.5	5.5 ± 0.05	4.5	2 ± 0.05	12 ± 0.3
16mm	12.1	1.5	7.5 ± 0.1	6.5	2 ± 0.1	16 ± 0.3

Note : Ao, Bo and Ko are determined by components size. The clearance between the component and the carrier pocket is :

a - 0.05 mm minimum to 0.65 mm maximum for 12 mm tape

b - 0.05 mm minimum to 0.90 mm maximum for 16 mm tape

NOTES

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