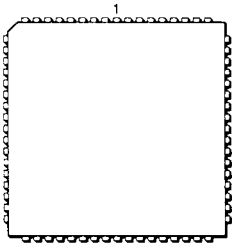
## FEATURES

- 100 ns Instruction Cycle Time
- 32-Bit ALU/Accumulator
- Wait States for Communication to Slow Off-Chip Memories/Peripherals
- 16 bit Internal and External Architecture
- Single 5V Supply
- Packaging: 68-Pin PLCC
- CMOS Technology

## 68 PIN PLCC PACKAGE



SC18025CV

## GENERAL DESCRIPTION

This data sheet provides the user with the necessary information to integrate this dedicated DSP (Digital Signal Processor) into the Sierra ARIA™ sound chip set.

The SC18025 is part of a chip set, used with the Multimedia System Controller (SC18000 or SC18005) and in conjunction with a ROM (SC18050, SC18051 or SC18052). By selecting a Multimedia System Controller and ROM a three chip set will be matched to form one of the three combinations called ST8000, ST8001 or ST8002.

The SC18025 contains a real time multi-tasking operating system kernel, as well as the algorithms for creating ARIA synthesis and performing audio recording and playback. The operating system kernel consists of a Task Manager and a Task Sequencer. The Task Manager handles the installation and removal of DSP tasks including verification that newly installed tasks are correctly initialized. The Task Sequencer is responsible for sequencing all active DSP tasks using a cooperative multi-tasking scheme. The following features are integrated into the operating system kernel:

- An interrupt handler for DAC/ADC control and synchronization as well as management of the DAC/ADC double buffering system
- PC IRQ generation for DSP Tasks requiring such interrupts
- Functions to handle command parameter buffering and retrieval

The algorithms contained within the SC18025 allow for generation of ARIA synthesis and controlling recording and playback. ARIA synthesis is based on a sampled waveform technique utilizing waveforms stored in the Sound ROM (SC18051 or SC18052). The following functions are performed when generating ARIA synthesis:

- Execution of up to 32 synthesis operators to generate the individual instrument sounds
- Mixing of the 32 individual operator outputs

## BLOCK DIAGRAM

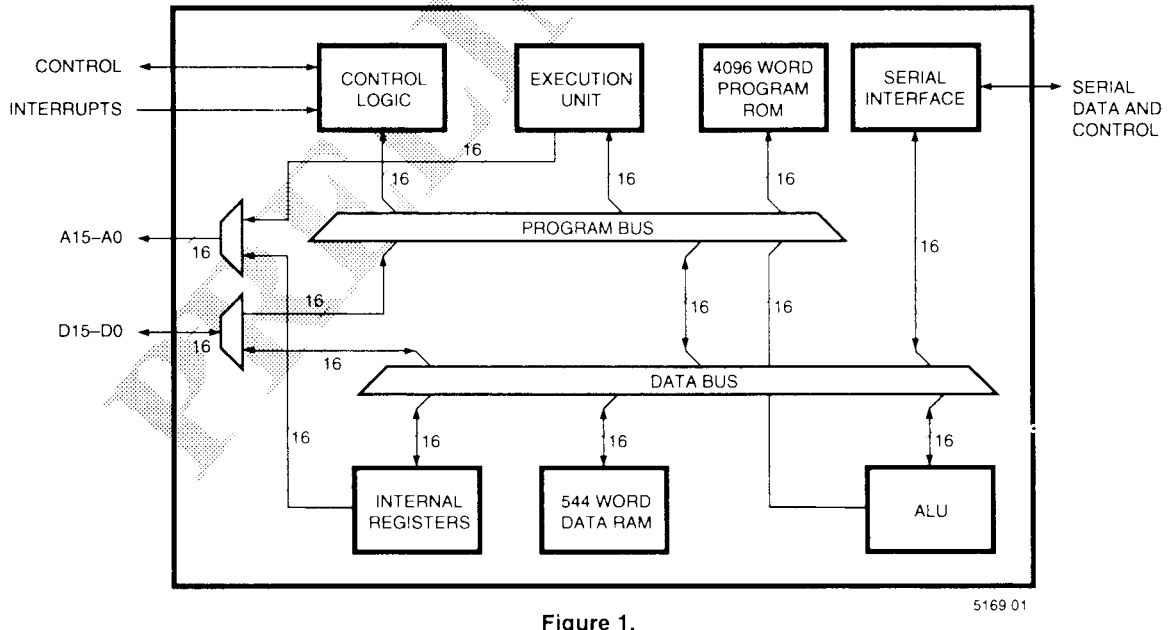



Figure 1.

Sound Blaster is a trademark of Creative Labs, Inc.
ARIA is a trademark of Sierra Semiconductor

## GENERAL DESCRIPTION (continued)

- Amplitude Envelope Generation for each operator
- Low Frequency Oscillator (LFO) effects generation
- Individual operator volume and stereo pan settings as well as master volume scaling

The audio recording and playback functions support various formats of PCM linear samples as well as 4:1 ADPCM compression/decompression. The SC18025 supports the following modes of operation while in PCM Audio Only mode:

- Up to 4 mono or 2 stereo channels of audio playback at rates up to 44.1 kHz
- Up to 3 mono channels or 1 stereo channel of audio playback and 1 mono or stereo channel of audio recording at rates up to 44.1 kHz

In addition, various DSP commands are used to control the ARIA synthesizer and Audio playback/recording functions.

## PIN DESCRIPTIONS

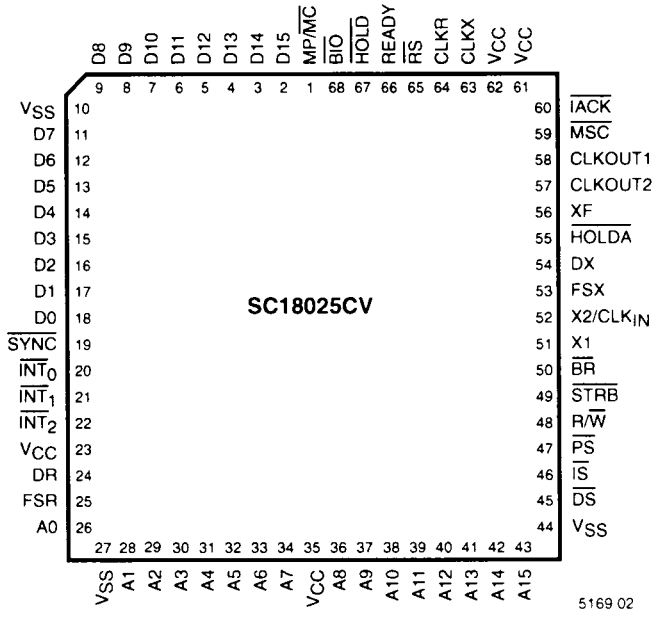
| PIN NAME | PIN NUMBER | I/O/Z† | DESCRIPTION |
|---|---|---|---|
| A15–A0 | 43–36, 34–28, 26 | O/Z | 16-Bit address bus A15 (MSB) through A0 (LSB). |
| $\overline{BIO}$ | 68 | I | Branch control input. Polled by BIOZ instruction. |
| $\overline{BR}$ | 50 | O | Bus request signal. Asserted when the SC18025 requires access to an external global data memory space. |
| CLKOUT1 | 58 | O | Master clock output (crystal or $CLK_{IN}$ frequency/4). |
| CLKOUT2 | 57 | O | A second clock output signal. (-90° phase) |
| CLKR | 64 | I | Clock for receive input for serial port. |
| CLKX | 63 | I | CLock for transmit output for serial port. |
| D15–D0 | 2–9, 11–18 | I/O/Z | 16-Bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data and I/O spaces. |
| DR | 24 | I | Serial data receive input. |
| $\overline{DS}$ | 45 | O/Z | Data memory space select signal. |
| DX | 54 | O/Z | Serial data transmit output. |
| FSR | 25 | I | Frame synchronization pulse for receive input. |
| FSX | 53 | I/O/Z | Frame synchronization pulse for transmit. Configurable as either an input or an output. |
| $\overline{HOLD}$ | 67 | I | Hold input. When asserted, SC18025 goes into an idle mode and places the data, address, and control lines in the high impedance state. |
| $\overline{HOLDA}$ | 55 | O | Hold acknowledge signal. |
| $\overline{IACK}$ | 60 | O | Interrupt acknowledge signal. |
| $\overline{INT_2}$–$\overline{INT_0}$ | 22–20 | I | External user interrupt inputs. |
| $\overline{IS}$ | 46 | O/Z | I/O space select signal. |
| MP/$\overline{MC}$ | 1 | I | Microprocessor/microcomputer mode select pin. |
| $\overline{MSC}$ | 59 | O | Microstate complete signal. |
| $\overline{PS}$ | 47 | O/Z | Program memory space select signal. |
| READY | 66 | I | Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete. |
| $\overline{RS}$ | 65 | I | Reset input. |
| R/$\overline{W}$ | 48 | O/Z | Read/write signal. |
| $\overline{STRB}$ | 49 | O/Z | Strobe signal. |
| $\overline{SYNC}$ | 19 | I | Synchronous input. |
| $V_{CC}$ | 23, 35, 61, 62 | I | 5V supply pins. |

## PIN DESCRIPTIONS

| PIN NAME | PIN NUMBER | I/O/Z† | DESCRIPTION |
|---|---|---|---|
| $V_{SS}$ | 10, 27, 44 | I | Ground pins. |
| X1 | 51 | O | Output from internal oscillator from crystal. |
| X2/CLKIN | 52 | I | Input to internal oscillator from crystal or external clock. |
| XF | 56 | O | External flag output (latched software-programmable signal). |

† I/O/Z denotes input/output/high-impedance rate.

## CONNECTION DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (unless otherwise noted)

| | |
|---|---|
| Supply voltage range, $V_{CC}$ (see Note 1) | -0.3V to 7V |
| Input voltage range: Pins 24 and 25 | -0.3V to 15V |
| All other inputs | -0.3V to 7V |
| Output voltage range | -0.3V to 7V |
| Continuous power dissipation | 2W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | -55°C to 150°C |

**NOTE 1:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those listed in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**NOTE 2:** All voltage values ar with respect to $V_{SS}$.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $V_{IH}$ | High-level input voltage | All inputs except | | | | |
| | | $CLK_{IN}$/CLKX/CLKR | 2.35 | | $V_{CC}$+0.3 | V |
| | | $INT_{0-2}$ | 2.5 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Low-level input voltage | All inputs except MP/$\overline{MC}$ | -0.3 | | 0.8 | V |
| | | MP/$\overline{MC}$ | -0.3 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | 300 | µA |
| $I_{OL}$ | Low-level output current | | | | 2 | mA |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## ELECTRICAL CHARACTERISTICS OVER SPECIFIED FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = Min., $I_{OH}$ = Max. | 2.4 | 3 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = Min., $I_{OH}$ = Max. | | 0.3 | 0.6 | V |
| $I_Z$ | Three-state current | $V_{CC}$ = Max. | -20 | | 20 | µA |
| $I_I$ | Input current | $V_I$ = $V_{SS}$ to $V_{CC}$ | -10 | | 10 | µA |
| $I_{CC}$ | Supply current Normal | $T_A$ = 0°C, $V_{CC}$ = Max., fx = Max. | | 110 | 185 | mA |
| | Idle/$\overline{HOLD}$ | | | 50 | 100 | |
| $C_I$ | Input capacitance | | | 15 | | pF |
| $C_O$ | Output capacitance | | | 15 | | pF |

**NOTE:** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

## CLOCK CHARACTERISTICS AND TIMING

The SC18025 can use either its internal oscillator or an external frequency source for a clock.

### Internal Clock Option

The internal oscillator is enabled by connecting a crystal across X1 and X2/$CLK_{IN}$ (see Figure 2). The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be either fundamental or overtone mode, and parallel resonant, with an effective series resistence of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned LC circuit.

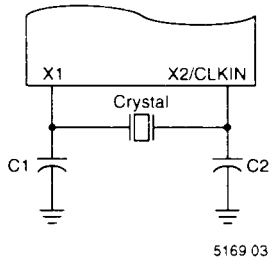



**Figure 2. Internal Clock Option**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_x$ | Input clock frequency | $T_A$ = 0°C to 70°C | 6.7 | | 40.96 | MHz |
| $f_{sx}$ | Serial port frequency | | 0[1] | | 5,120 | kHz |
| C1, C2 | | | | 10 | | pF |

**NOTE 1:** The serial port is tested at a minimum frequency of 1.25 MHz. However, the serial port is fully static and will properly function down to $f_{sx}$ = 0 Hz.

**Table 1.**

### External Clock Option

An external frequency source can be used by injecting the frequency directly into X2/$CLK_{IN}$ with X1 left unconnected. The external frequency injected must conform to the specifications in Table 2.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(C)}$ | CLKOUT1/CLKOUT2 cycle time | 97.7 | | 597 | ns |
| $t_{d(CIH-C)}$ | $CLK_{IN}$ high to CLKOUT1/CLKOUT2/$\overline{STRB}$ high/low | 5 | | 30 | ns |
| $t_{f(C)}$ | CLKOUT1/CLKOUT2/$\overline{STRB}$ fall time | | | 5 | ns |
| $t_{r(C)}$ | CLKOUT1/CLKOUT2/$\overline{STRB}$ rise time | | | 5 | ns |
| $t_{w(CL)}$ | CLKOUT1/CLKOUT2 low pulse duration | 2Q–8 | 2Q | 2Q+8 | ns |
| $t_{W(CH)}$ | CLKOUT1/CLKOUT2 high pulse duration | 2Q–8 | 2Q | 2Q+8 | ns |
| $t_{d(C1-C2)}$ | CLKOUT1 high to CLKOUT2 low, CLKOUT2 high to CLKOUT1 high | Q–5 | Q | Q+5 | ns |

**Table 2. Switching Characteristics Over Recommended Operating Conditions (Q = 1/4$t_{c(C)}$)**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(CI)}$ | $CLK_{IN}$ cycle time | 24.4 | | 150 | ns |
| $t_{f(CI)}$ | $CLK_{IN}$ fall time (see Note 1) | | | 5 | ns |
| $t_{r(CI)}$ | $CLK_{IN}$ rise time (see Note 1) | | | 5 | ns |
| $t_{w(CIL)}$ | $CLK_{IN}$ low pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2) | 20 | | | ns |
| $t_{w(CIH)}$ | $CLK_{IN}$ high pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2) | 20 | | | ns |
| $t_{su(S)}$ | $\overline{SYNC}$ setup time before $CLK_{IN}$ low | 5 | | Q–5 | ns |
| $t_{h(S)}$ | $\overline{SYNC}$ hold time from $CLK_{IN}$ low | 8 | | | ns |

**NOTE 1:** Value derived from characterization data and not tested.

**NOTE 2:** CLKIN duty cycle[$t_{r(CI)}$ + $t_{w(CIH)}$]/$t_{c(CI)}$ must be within 40–60%.

**Table 3. Timing Requirements Over Recommended Operating Conditions (Q = 1/4$t_{c(C)}$)**

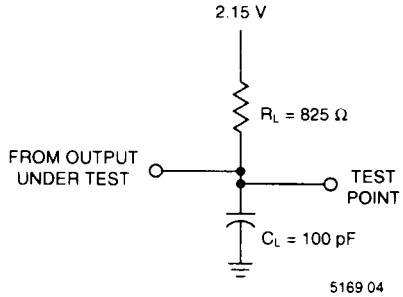



**Figure 3. Test Load Circuit**

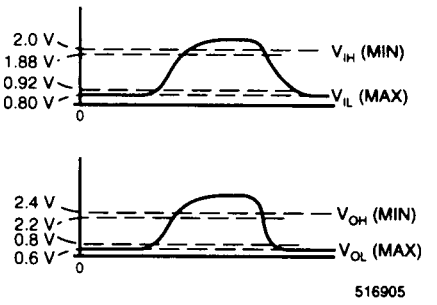



**Figure 4. Voltage Reference Levels**

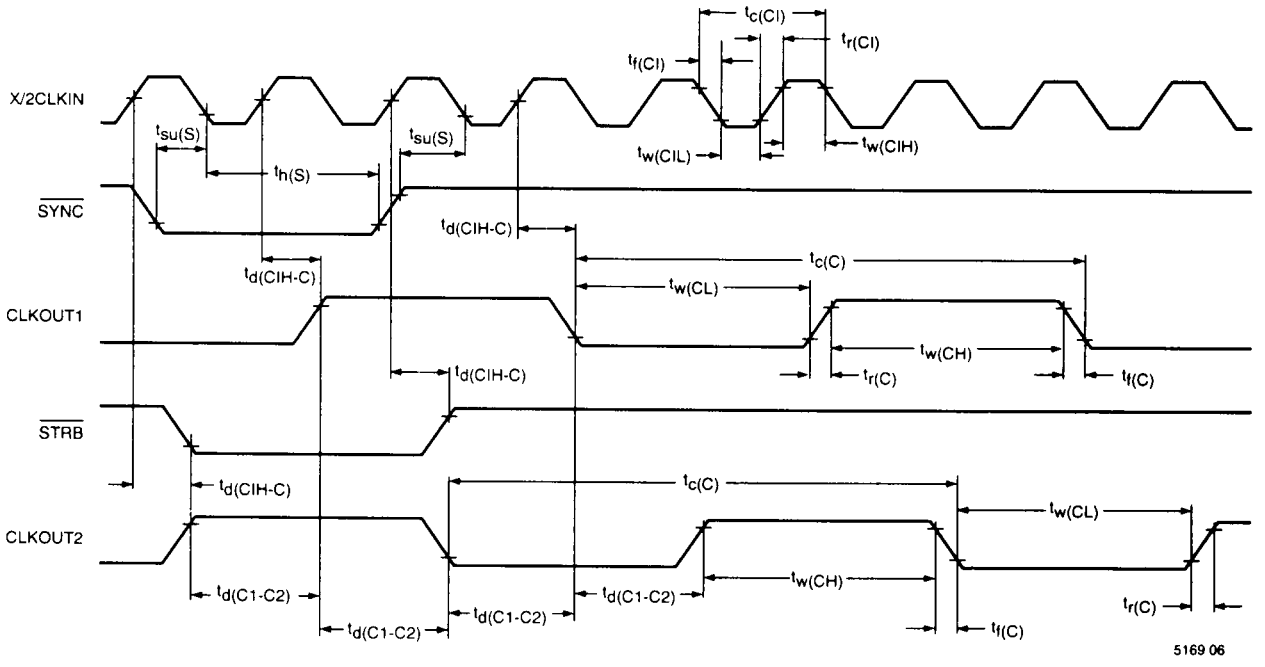



**Figure 7. Clock Timing**

## MEMORY AND PERIPHERAL INTERFACE TIMING

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(C1-S)}$ | $\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present) | Q–6 | Q | Q+6 | ns |
| $t_{d(C2-S)}$ | CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present) | -6 | 0 | 6 | ns |
| $t_{su(A)}$ | Address setup time before $\overline{STRB}$ low (see Note 3) | Q–12 | | | ns |
| $t_{h(A)}$ | Address hold time after $\overline{STRB}$ high (see Note 3) | Q–8 | | | ns |
| $t_{w(SL)}$ | $\overline{STRB}$ low pulse duration (no wait states, see Note 4) | 2Q–5 | | 2Q+5 | ns |
| $t_{w(SH)}$ | $\overline{STRB}$ high pulse duration (betwen consecutive cycles, see Note 4) | 2Q–5 | | 2Q+5 | ns |
| $t_{su(D)W}$ | Data write setup time before $\overline{STRB}$ high (no wait states) | 2Q–20 | | | ns |
| $t_{h(D)W}$ | Data write hold time from $\overline{STRB}$ high | Q–10 | Q | | ns |
| $t_{en(D)}$ | Data bus starts being driven after $\overline{STRB}$ low (write cycle) (see Note 2) | 0 | | | ns |
| $t_{dis(D)}$ | Data bus three-state after $\overline{STRB}$ high (write cycle) (see Note 2) | | Q | Q+15 | ns |
| $t_{d(MSC)}$ | $\overline{MSC}$ valid from CLKOUT1 | -12 | 0 | 12 | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** Value derived from characterization data and not tested.

**NOTE 3:** A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address."

**NOTE 4:** Delays between CLKOUT1/CLKOUT2 edges and $\overline{STRB}$ edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait states.

**Table 4. Switching Characteristics Over Recommended Operating Conditions**

| SYMBOL | PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{a(A)}$ | Read data access time from address time (read cycle, see Notes 2 & 3) | | | 3Q–35 | ns |
| $t_{su(D)R}$ | Data read setup time before $\overline{STRB}$ high | 23 | | | ns |
| $t_{h(D)R}$ | Data read hold time from $\overline{STRB}$ high | 0 | | | ns |
| $t_{d(SL-R)}$ | READY valid after $\overline{STRB}$ low (no wait states) | | | Q–20 | ns |
| $t_{d(C2H-R)}$ | READY valid after CLKOUT2 high | | | Q–20 | ns |
| $t_{h(SL-R)}$ | READY hold time after $\overline{STRB}$ low (no wait states) | Q+3 | | | ns |
| $t_{h(C2H-R)}$ | READY hold after CLKOUT2 high | Q+3 | | | ns |
| $t_{d(M-R)}$ | READY valid after $\overline{MSC}$ valid | | | 2Q–25 | ns |
| $t_{h(M-R)}$ | REDAY hold time after $\overline{MSC}$ valid | 0 | | | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address."

**NOTE 3:** Read data access time is defined as $t_{s(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R}$.

**Table 5. Timing Requirements Over Recommended Operating Conditions**

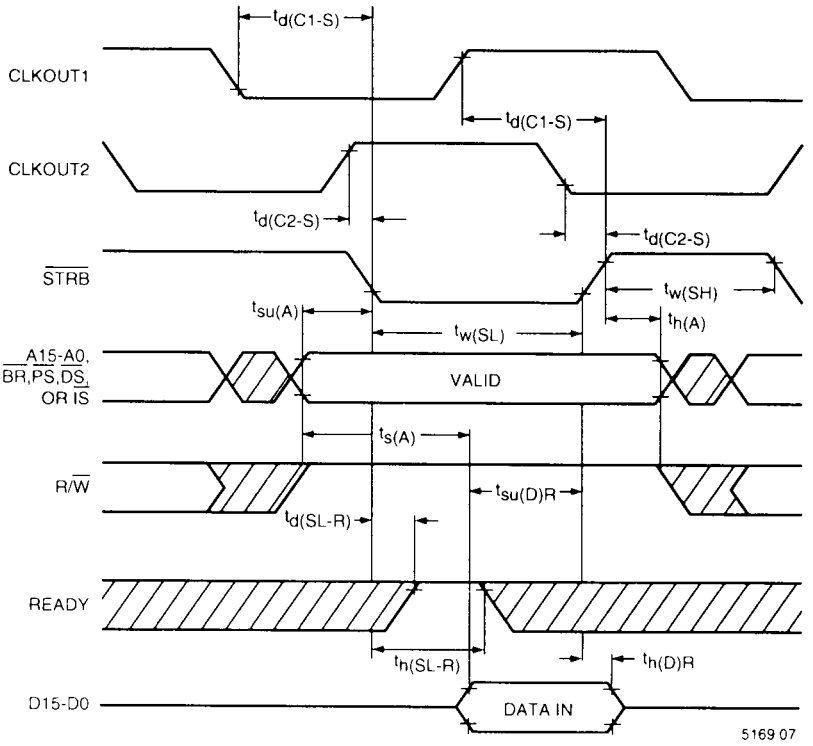



**Figure 6. Memory Read Timing**

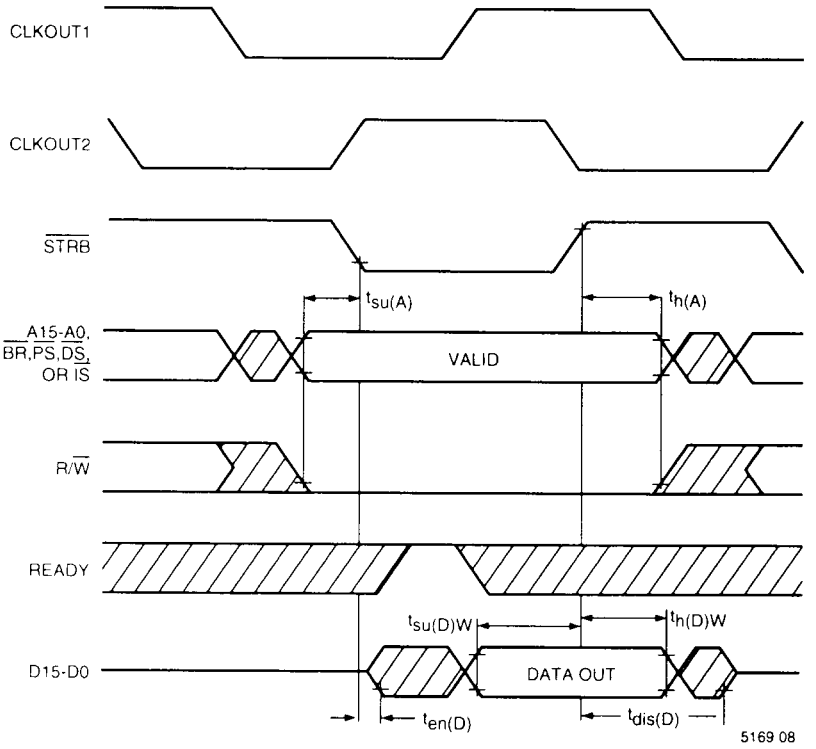



**Figure 7. Memory Write Timing**

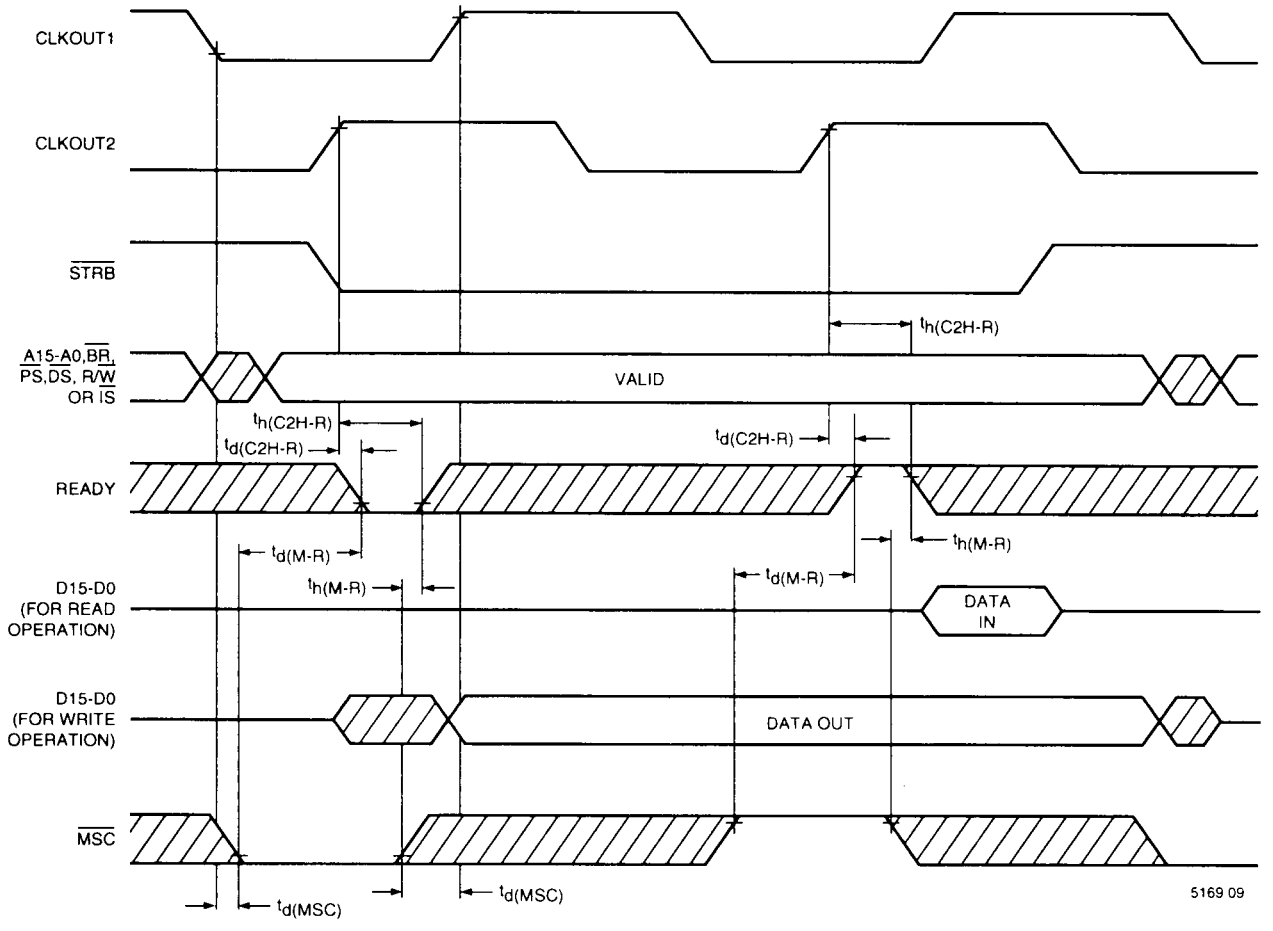



**Figure 8. One Wait-State Memory Access Timing**

## RS, INT, BIO, AND XF TIMING

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(RS)}$ | CLKOUT1 low to reset state entered (see note 2) | | | 22 | ns |
| $t_{d(IACK)}$ | CLKOUT1 to IACK valid | -6 | 0 | 12 | ns |
| $t_{d(XF)}$ | XF valid before falling edge of STRB | Q–15 | | | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** Value derived from characterization data and not tested.

**NOTE 3:** RS, INT, and BIO are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

**Table 6. Switching Characteristics Over Recommended Operating Conditions**

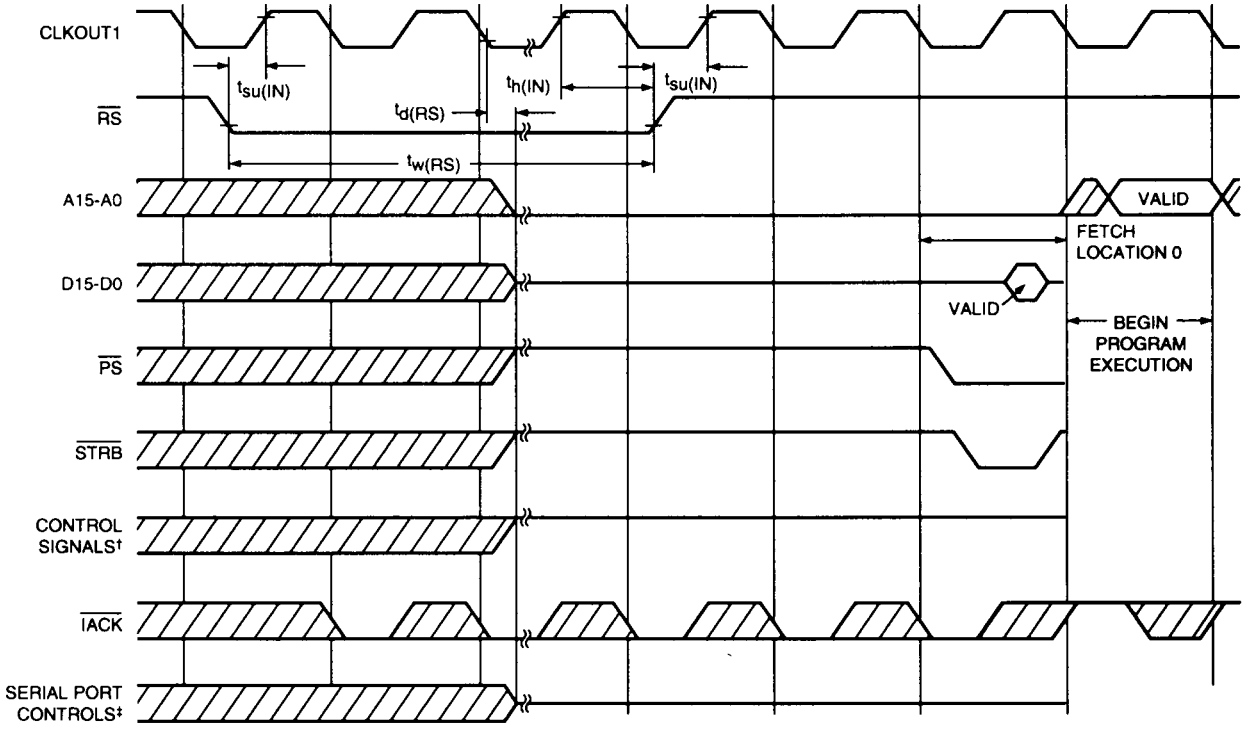
| SYMBOL | PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(IN)}$ | $\overline{INT}/\overline{BIO}/\overline{RS}$ setup before CLKOUT1 high | 32 | | | ns |
| $t_{h(IN)}$ | $\overline{INT}/\overline{BIO}/\overline{RS}$ hold after CLKOUT1 high | 0 | | | ns |
| $t_{f(IN)}$ | $\overline{INT}/\overline{BIO}$ fall time (see Note 2) | | | 8 | ns |
| $t_{w(IN)}$ | $\overline{INT}/\overline{BIO}$ low pulse duration | $t_{c(C)}$ | | | ns |
| $t_{w(RS)}$ | $\overline{RS}$ low pulse duration | $3t_{c(C)}$ | | | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** Value derived from characterization data and not tested.

**NOTE 3:** $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

**Table 7. Timing Requirements Over Recommended Operating Conditions**




†Control signals are $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and XF.
‡Serial port controls are DX and FSX.

**Figure 9. Reset Timing**

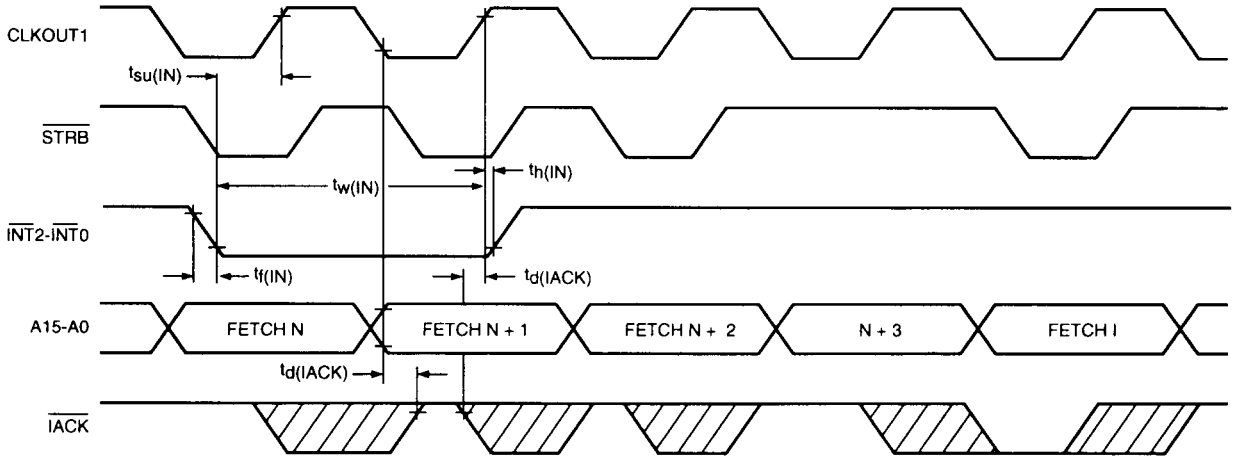



**Figure 10. Interrupt Timing**

5169 11

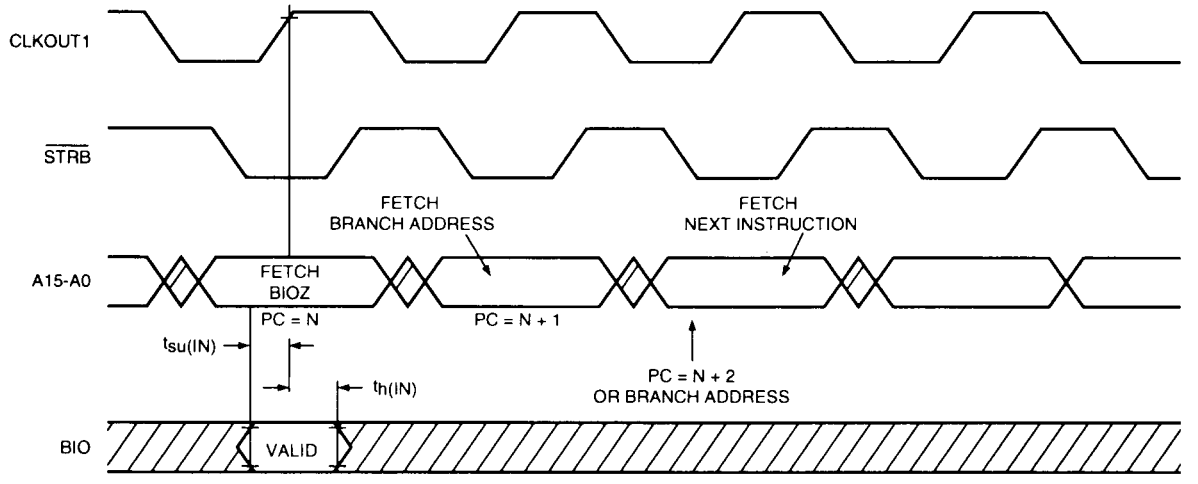



**Figure 11. $\overline{BIO}$ Timing**

5169 12

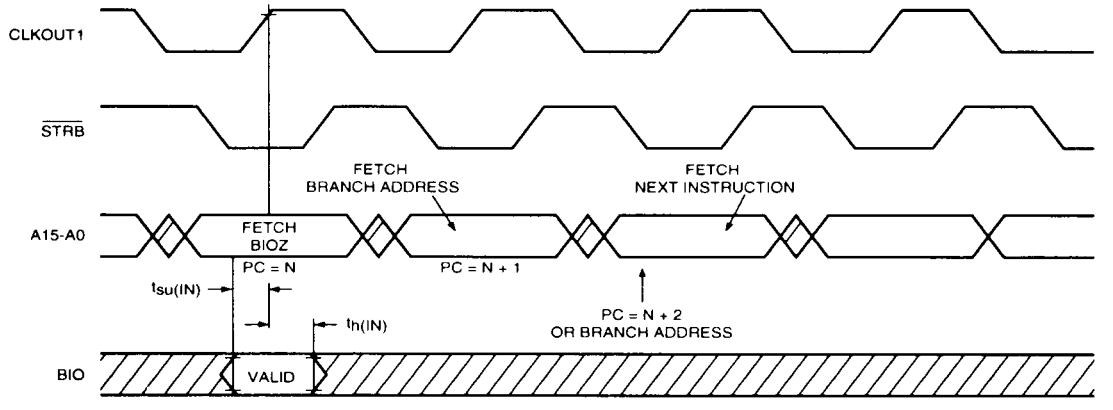



**Figure 12. External Flag Timing**

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## $\overline{HOLD}$ TIMING

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(C2H-H)}$ | $\overline{HOLD}$ valid after CLKOUT2 high | | | Q–24 | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**Table 8. Timing Requirements Over Recommended Operating Conditions**

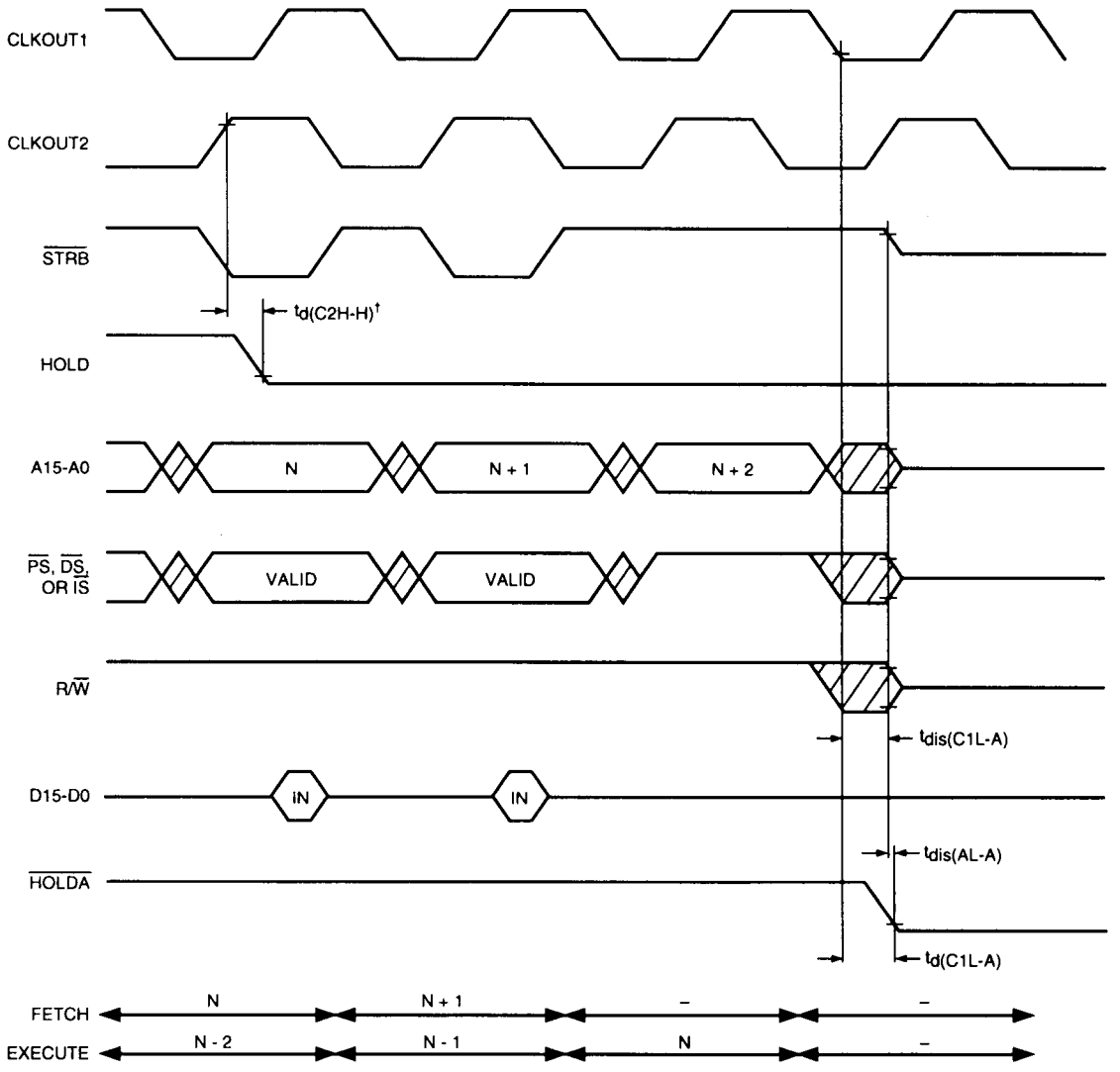
| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(C1L-AL)}$ | $\overline{HOLDA}$ low after CLKOUT1 low | 0 | | 10 | ns |
| $t_{dis(AL-A)}$ | $\overline{HOLDA}$ low to address three-state (see Note 2) | | 0 | | ns |
| $t_{dis(C1L-A)}$ | Address three-state after CLKOUT1 low ($\overline{HOLD}$ mode, see Notes 2, 3) | | | 20 | ns |
| $t_{d(HH-AH)}$ | $\overline{HOLD}$ high to $\overline{HOLDA}$ high | | | 25 | ns |
| $t_{en(A-C1L)}$ | Address driven before CLKOUT1 low ($\overline{HOLD}$ mode, see Notes 2, 3) | | | 8 | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** Value derived from characterization data and not tested.

**NOTE 3:** A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{STRB}$, and R/$\overline{W}$ timings are all included in timings referenced as "address."

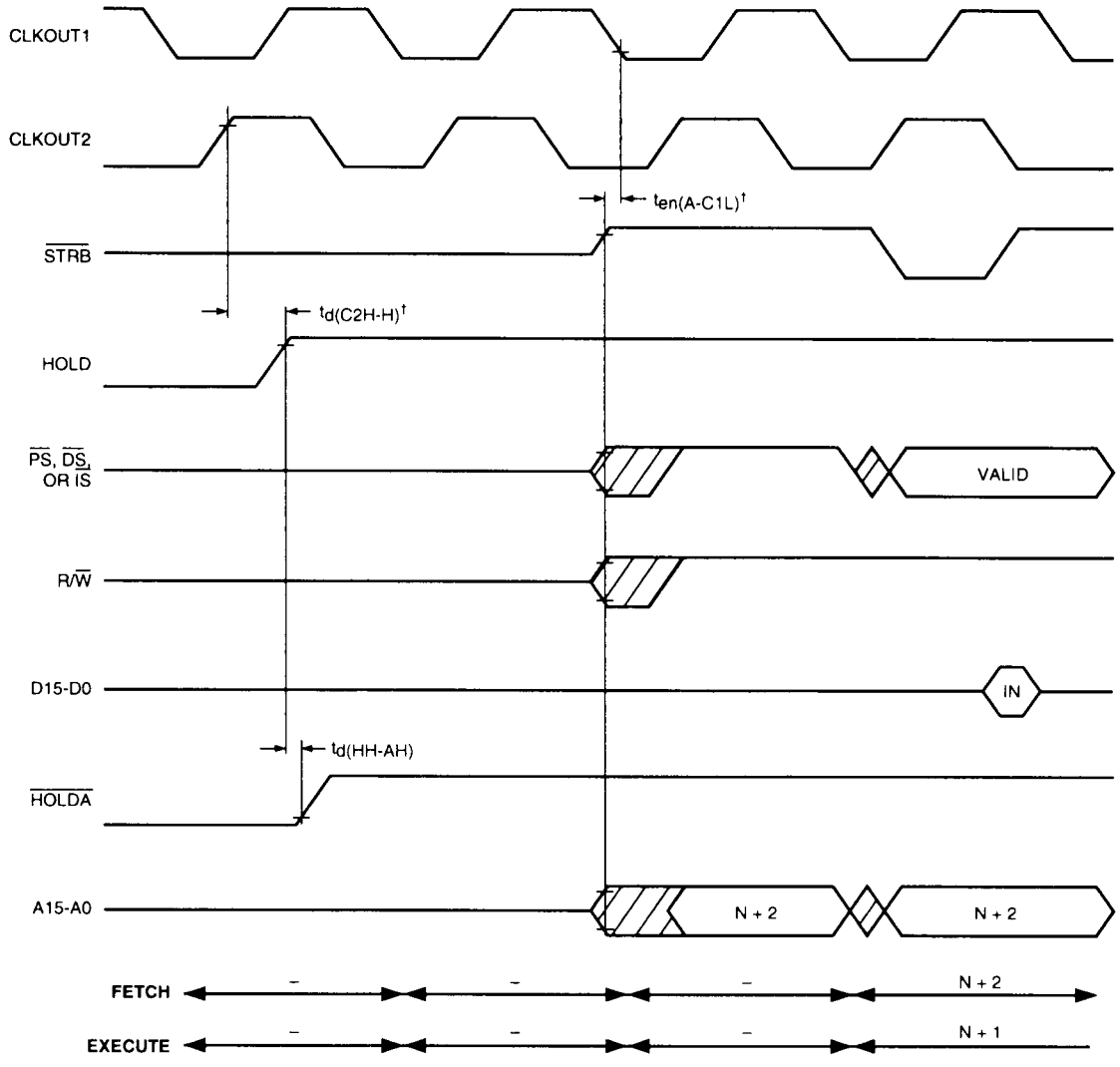
**Table 9. Switching Characteristics Over Recommended Operating Conditions**




†$\overline{HOLD}$ is an asynchronous input and can occur at any time during a clock cycle if the specified timing is met the exact sequence shown will occur, otherwise, a delay of one CLKOUT2 cycle will occur.

5169 14

**Figure 13. $\overline{HOLD}$ Timing (Part A)**




†HOLD is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur, otherwise, a delay of one CLKOUT2 cycle will occur.

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**Figure 14. HOLD Timing (Part B)**

## SERIAL PORT TIMING

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(CH-DX)}$ | DX valid after CLKX rising edge (see Note 2) | | | 75 | ns |
| $t_{d(FL-DX)}$ | DX valid after FSX falling edge (TXM = 0, see Note 2) | | | 40 | ns |
| $t_{d(CH-FS)}$ | FSX valid after CLKX rising edge (TXM = 1) | | | 40 | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** The last occurence of FSX falling and CLKX rising.

**Table 10. Switching Characteristics Over Recommended Operating Conditions**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(SCK)}$ | Serial port clock (CLKX/CLKR) cycle time[3] | 200 | | | ns |
| $t_{f(SCK)}$ | Serial port clock (CLKX/CLKR) fall time (see Note 2) | | | 25 | ns |
| $t_{r(SCK)}$ | Serial port clock (CLKX/CLKR) rise time (see Note 2) | | | 25 | ns |
| $t_{w(SCK)}$ | Serial port clock (CLKX/CLKR) low pulse duration (see Note 4) | 80 | | | ns |
| $t_{w(SCK)}$ | Serial port clock (CLKX/CLKR) high pulse duration (see Note 4) | 80 | | | ns |
| $t_{su(FS)}$ | FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0) | 18 | | | ns |
| $t_{h(FS)}$ | FSX/FSR setup time after (CLKX/CLKR falling edge (TXM = 0) | 20 | | | ns |
| $t_{su(DR)}$ | DR setup time before CLKR falling edge | 10 | | | ns |
| $t_{h(DR)}$ | DR hold time after CLKR falling edge | 20 | | | ns |

**NOTE 1:** $Q = 1/4t_{c(C)}$.

**NOTE 2:** Value derived from characterization data and not tested.

**NOTE 3:** The serial port is tested at a minimum frequency of 1.25 MHz. However, the serial port is fully static and will properly function down to $f_{sx}$ = 0 Hz.

**NOTE 4:** The duty cycle of the serial port clock must be within 40–60%.

**Table 11. Timing Requirements Over Recommended Operating Conditions**

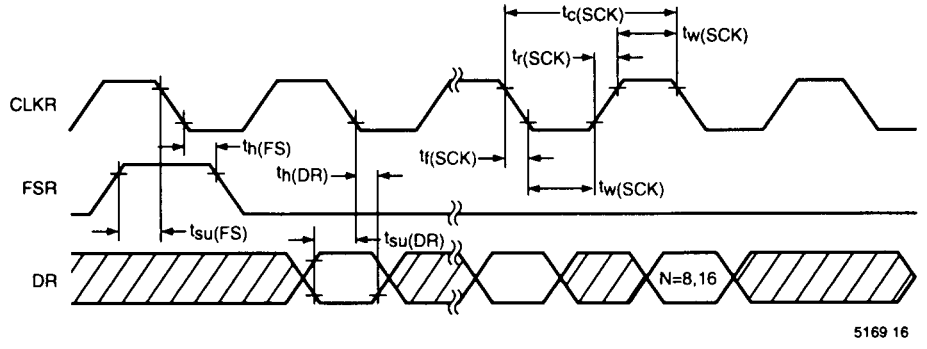



**Figure 15. Serial Port Receive Timing**

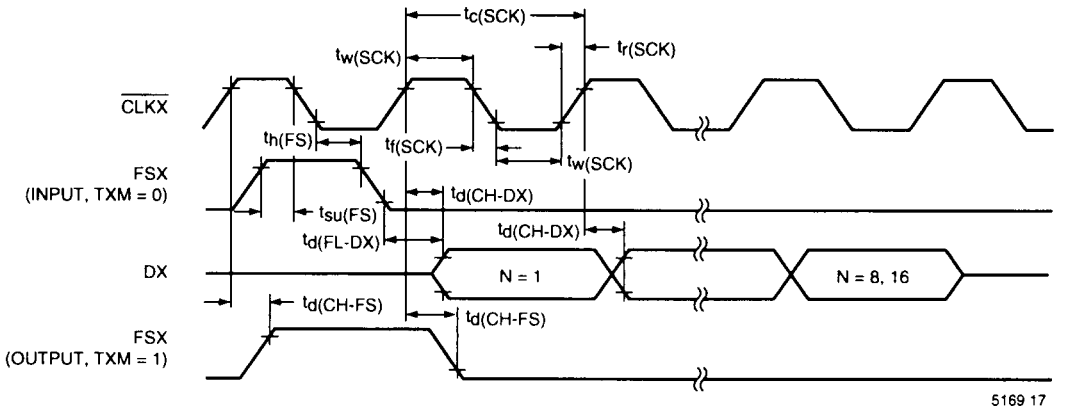
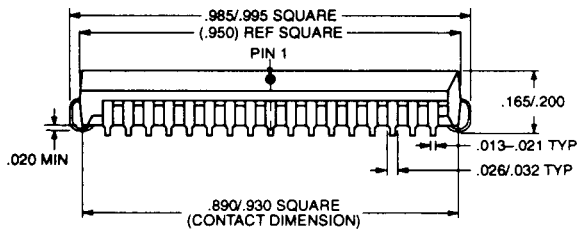
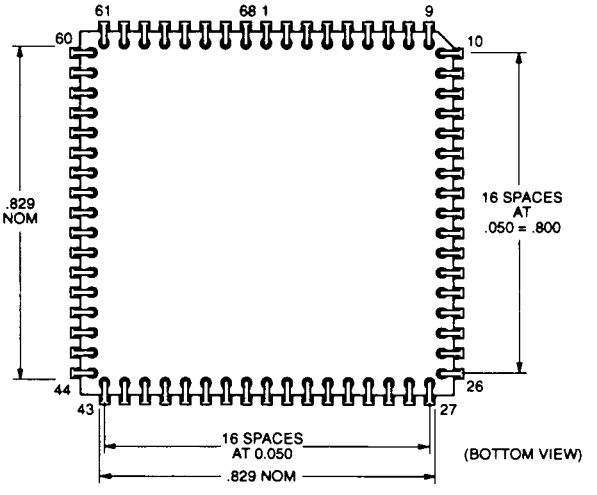



**Figure 16. Serial Port Receive Timing**

## PHYSICAL DIMENSIONS—INCHES (MILLIMETERS)

### Package 68-Lead PLCC




THERMAL RESISTANCE CHARACTERISTICS

| PARAMETER | | MAX | UNIT |
|---|---|---|---|
| RθJA | Junction to free air thermal resistance | 46 | °C W |
| RθJC | Junction to case thermal resistance | 11 | °C W |





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