

FEATURES 32 PIN DIP PACKAGE ☐ Record and Playback ☐ Aria Synthesis ☐ General MIDI Sound Samples Single 5 Volt Power Supply ☐ Ad Lib Emulation 32 pin Plastic Dip ☐ Sound Blaster Emulation ☐ Low Power Dissipation ☐ 4:1 ADPCM Compression and ☐ Fully Static Operation Decompression **GENERAL DESCRIPTION** The SC18051 contains samples of The SC18051 is organized as 524,288 sounds that form the General MIDI words by 8 bits. The device is fully sound library and can be run on TTL compatible on all inputs and the Aria synthesizer. This chip is outputs and uses a single 5 Volt SC18051CN used in conjunction with Sierra's power supply. The device is fully

static, requiring no clock operation.

When the chip is not enabled, the

power supply current is reduced

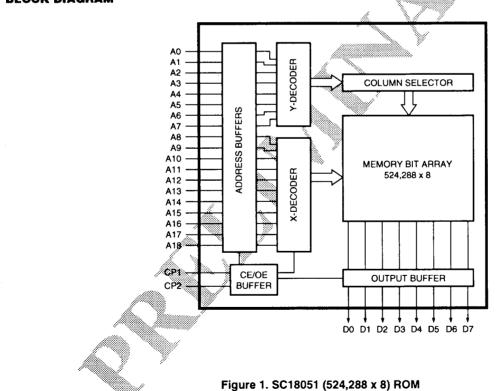
to a 30 uA maximum.

BLOCK DIAGRAM

SC18005 Audio System Controller

and the SC18025 Audio Processor

to make up the ST8001 Chip set.

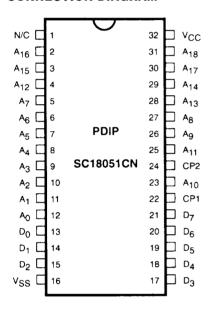


Sound Blaster is a registered trademark of Creative Labs Inc. AdLib is a registered trademark of AdLib Inc. ARIA is a trademark of Sierra Semiconductor.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
A ₀ -A ₁₈	12-5, 27-26, 23, 25, 4, 28-29, 3-2, 30-31	Address inputs.
D ₀ -D ₇	13–15, 17–21	Data outputs.
CP1, CP2	22, 24	Control pins.
N/C	1	Not connected.
V _{CC}	32	+5V supply.
V _{SS}	16	Ground.

CONNECTION DIAGRAM



CAPACITANCE $T_A = 25^{\circ}C$, f = 1.0MHz

SYMBOL	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
C _{IN}	Input capacitance	$V_{IN} = 0V$	5	5	pF
C _{OUT}	Output capacitance	$V_{IN} = 0V$	7	8	pF

TRUTH TABLE

(For simplicity, all control functions in the truth table are defined as active high.)

CP1 = CE/OE	CP2 = CE/OE	OUTPUTS	POWER
CE/OE active	CE/OE active	Data out	I _{CC}
CE inactive	X	High Z	I_{SB}
OE inactive	CE active	High Z	I _{CC}
Х	CE inactive	High Z	I_{SB}
CE active	OE inactive	High Z	I _{CC}

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias – T _A	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Operating Temperature	+125°C
Input or Output Voltages	-0.3 to V _{CC} +0.3V
Maximum V _{DD}	-0.3V to 7V
Maximum Power	500mW

NOTE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those listed in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 10\%$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{OL}	Output LOW voltage	3.2mA I _{OL}		0.4	V
V_{OH}	Output HIGH voltage	-1.0mA I _{OH}	2.4		V
V_{IL}	Input LOW voltage		-0.3	0.8	V
V _{IH}	Input HIGH voltage		2.2	V _{CC} +0.3	v
I _{LI}	Input leakage current	$V_{IN} = 0V V_{CC}$	-10	10	μА
I_{LO}	Output leakage current	$V_0 = 0V$ to V_{CC} , outputs deselected	-10	10	μА
I _{CC1}	Power supply current – active	$I_0 = 0$, TR = t_{CYC} , duty = 100% $V_I = 0.8V$ or 2.2V		40	mA
I _{CC2}	Power supply current – active	$I_0 = 0$, TR = t_{CYC} , duty = 100% $V_I = GND$ or V_{CC}		35	mA
I _{SB}	Power supply current – standby	Chip in standby mode, $V_I = GND$ to V_{CC}		150	μА

NOTE: It is recommended that a high frequency bypass capacitor between the power supply pin and the ground pin be utilized.

AC TIMING DIAGRAMS

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{AA}	Address access time		200	ns
t _{OH}	Output hold time	0		ns

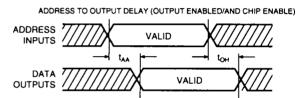


Figure 3.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{OE}	Output enable access		80	ns
t _{OEO}	Disable time from Output Enable	0	70	ns

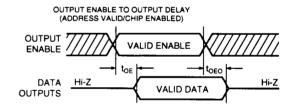


Figure 4.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t _{CEO}	Disable time fromChip Enable	0	70	ns
t _{ACE}	Chip enable access time		200	ns

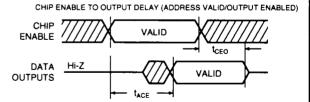


Figure 5.

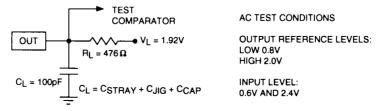
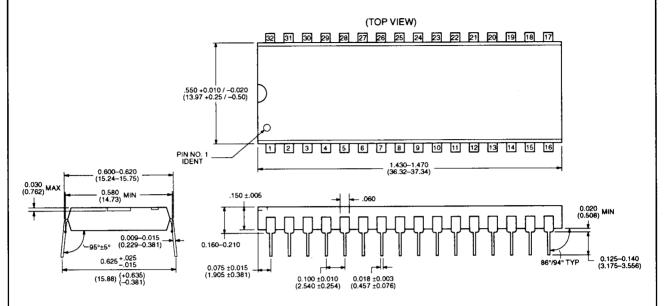


Figure 6. Test Load

PHYSICAL DIMENSIONS—INCHES (MILLIMETERS)

Package 32-Lead Plastic DIP



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