BIPOLAR MEMORIES

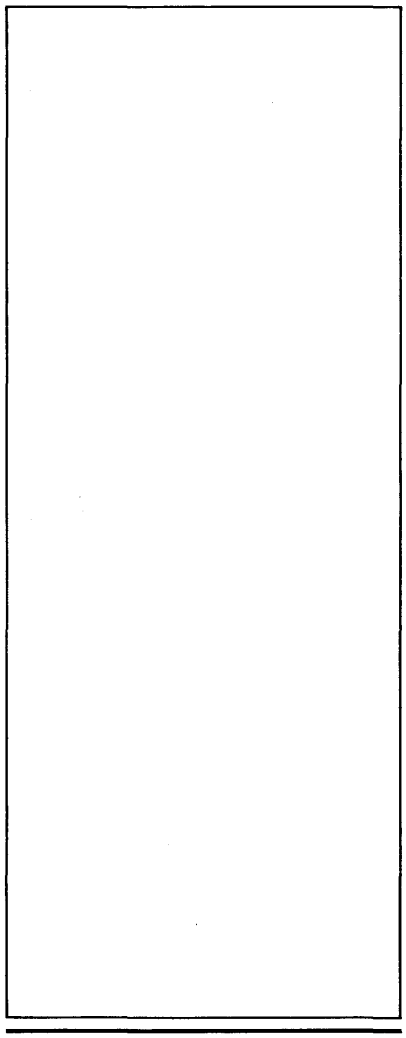

TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS*

CHARACTERISTICS	SYMBOL	RATING	UNIT
TTL MEMORIES			
Storage Temperature	T_{STG}	−60 to +150	°C
Output and Supply Voltages	V_{OUT}, V_{CC}	−0.5 to +6.0	V
Input Voltages	V_{IN}	−0.5 to +6.0	V
Output Currents	I_{OUT}	100	mA
Input Currents	I_{IN}	−30 to +30	mA
ECL MEMORIES			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8	Vdc
Input Voltage (V_{CC} = 0)	V_{IN}	0 to V_{EE}	Vdc
Output Source Current	I_o		
Continuous		50	mAdc
Surge		100	mAdc
Storage Temperature Range	T_{stg}	−54 to +175	°C
Operating Junction Temperature	T_J	125	°C
Operating Temperature Range	T_A	−30 to +85	°C
Power Supply Regulation Required	—	±10%	—

*These ratings do not imply that the device will function or meet the specified parameters at the levels indicated. They do, however, indicate those levels at which permanent damage and/or parameter degradation could occur. Exposure to these levels over extended periods of time could affect reliability and should, therefore, be avoided.

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2048 BIT BIPOLAR ROM (256x8 ROM)
4096 BIT BIPOLAR ROM (512x8 ROM)

8204
8205

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8205 and 8204 are high performance bipolar ROM's incorporating the storage output or memory data register into the chip. Data is addressed by applying address information to the address lines. After valid data appears at the output of the memory array, (typically 35ns after the address is applied) and if the circuit is enabled, the strobe pulse will enter data into the 8 bit output latch register. A D-type latch (L) is used to enable the tri-state output drivers. If the circuit enable signals are valid, the strobe will set the latch. This turns on the output stage. The latch will remain set and keep the output enabled until the chip is disabled and the next strobe pulse occurs. If the strobe line is held high, the ROM will function in a conventional mode. The output will be controlled solely by the chip enable and the output latches will be bypassed.

Refer to back of Bipolar Memory section for ASCII (ADDRESS) to EBCDIC (DATA) and EBCDIC (ADDRESS) to ASCII (DATA) and ORDERING BLANKS.

FEATURES

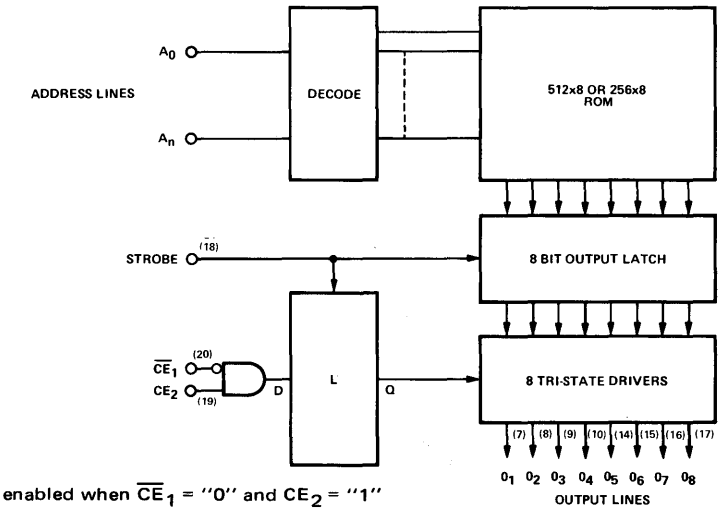
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- ON THE CHIP STORAGE LATCHES
- TRI-STATE OUTPUT
- PROTECTED INPUTS

APPLICATIONS

MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE

BLOCK DIAGRAM

8204 (256x8) AND 8205 (512x8) MEMORY ORGANIZATION



Chip is enabled when $\overline{CE}_1$ = "0" and CE_2 = "1"

Address Pins	8204	8205
A_0	(21)	(21)
A_1	(22)	(22)
A_2	(23)	(23)
A_3	(1)	(1)
A_4	(2)	(2)
A_5	(4)	(3)
A_6	(5)	(4)
A_7	(6)	(5)
A_8	—	(6)

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS: $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Input "0" Current			-400	μA	V_{in} = 0.45V	
Input "1" Current			25	μA	V_{in} = 5.5V	
Input (0) Threshold Voltage			.85	V		
Input (1) Threshold Voltage	2			V		
Input Clamp Voltage	-1.2V			V	I_{in} = -18mA	
Output (0) Current		0.25	0.5	V	I_{out} = 9.6 mA	
Output (1) Current	2.7	3.3		V	I_{out} = -2.0mA	
Output (1) Short Circuit Current	-20	-35	-70	mA	V_{out} = 0V, V_{CC} = 5.0V	
Input Capacitance		5		pF	V_{IH} = 2.0V, V_{CC} = 5.0V	
Output Capacitance		8		pF	V_{out} = 2.0V, V_{CC} = 5.0V	
Power Supply Current		135	170	mA	V_{CC} = 5.0V	
Output (1) off Leakage Current (Chip Disabled)			40	μA	V_{out} = 5.5V	
Output (0) off Leakage Current (Chip Disabled)			-40	μA	V_{out} = 0.45V	

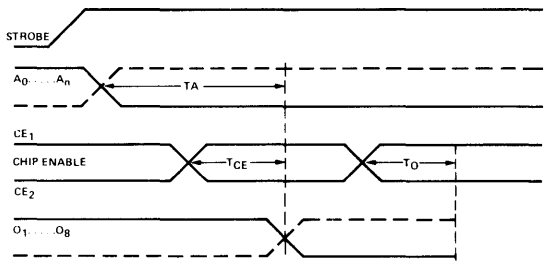
SWITCHING CHARACTERISTICS $0 \leqslant T_A \leqslant 75^\circ C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

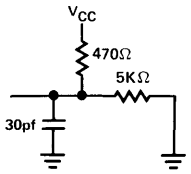
CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	NOTES
Address Access Time T_A		35	75	ns	Read Mode I or Read Mode II	6
Address Hold Time T_{ADS}	0	-10		ns	Read Mode 2 Only	6
Chip Enable Access Time T_{CE}		20	50	ns	Read Mode I or Read Mode II	6
Chip Enable Hold Time T_{CDS}	15	5		ns	Read Mode II Only	6
Output Disable Time T_O		20	50	ns	Read Mode I or Read Mode II	6
Strobe Pulse Width T_{SW}	35	20		ns	Read Mode II Only	6
Strobe Set-Up Time T_S		30	75	ns	Read Mode II Only	6
Output Disable Time T_R		18	35	ns	Read Mode II Only	6

NOTES
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30 mA. Output currents must not exceed ±100 mA. Storage temperature must be between $-60^\circ C$ to $+150^\circ C$.
5. Chip disabled.
6. Rise and fall times for tests must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

MEMORY TIMING

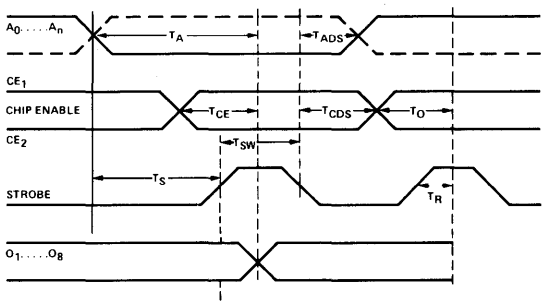
READ MODE I (OUTPUT LATCHES NOT USED)



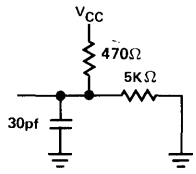


If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an 'off' or high impedance state after it has been enabled.

READ MODE II (OUTPUT LATCHES USED)



NOTE: T Cycle Time = TA + TADS + TSW + TCDS



In Read Mode II, data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

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8-BIT CONTENT ADDRESSABLE MEMORY (4x2 CAM) 8220

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{nj}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

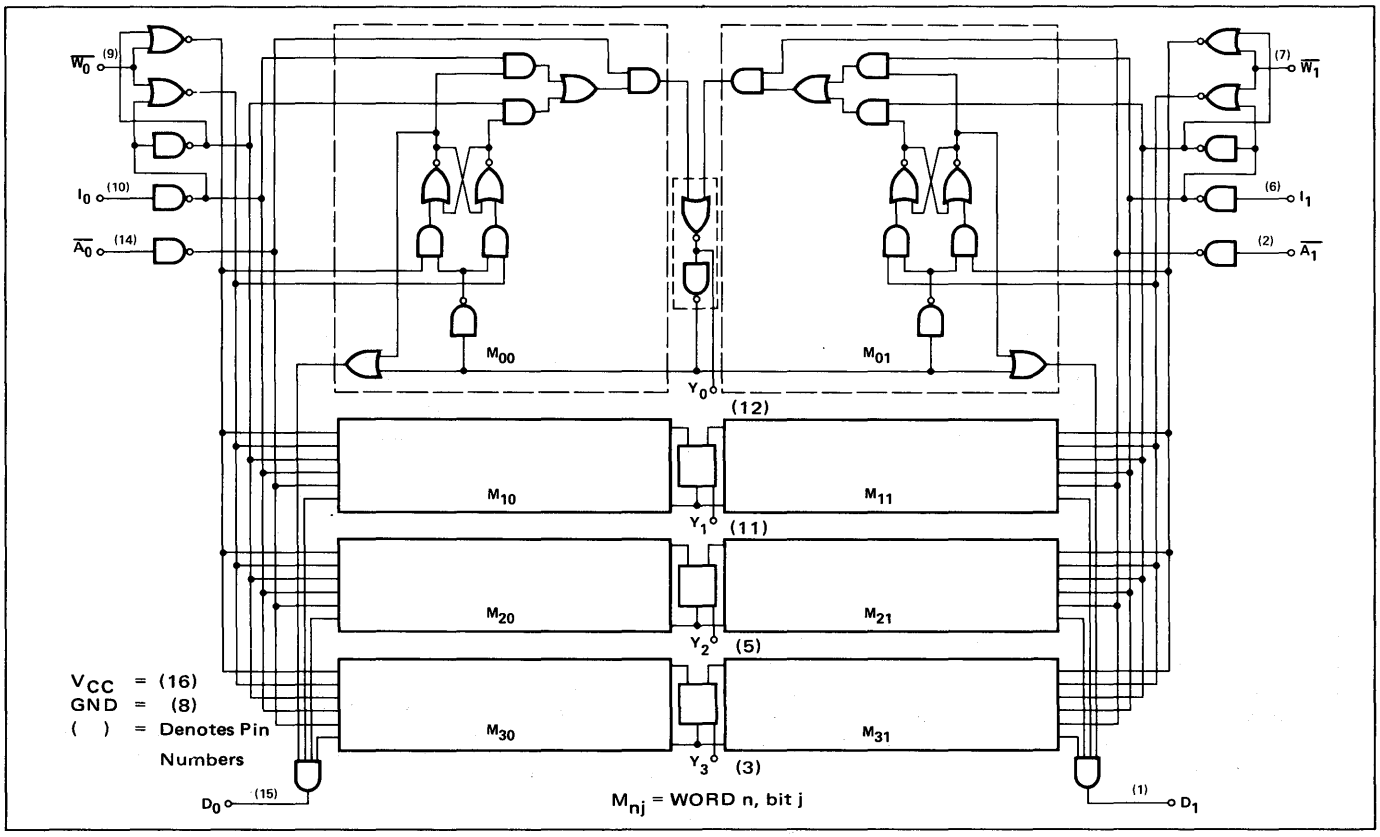
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

DATA-TO-MEMORY COMPARISON
PATTERN RECOGNITION
HIGH SPEED INFORMATION RETRIEVAL
CACHE MEMORY
AUTO CORRELATION
VIRTUAL MEMORY
LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				$\overline{Wj}$	$\overline{Aj}$	I_j	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	μA		2.0V					10
Dj			100	μA				0V	0V		10
"1" Input Current											
Ij and $\overline{A_j}$			40	μA		4.5V	4.5V				
$\overline{Wj}$			80	μA	4.5V						
"0" Input Current											
Ij, Yn and $\overline{Aj}$	-0.1		-1.2	mA		0.4V	0.4V	0.4V			
$\overline{W_j}$			-2.4	mA.							
Power Consumption		85/ 425	118/ 590	mA/mW	V_{CC} = 5.0 Volts						

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				NOTES
	MIN.	TYP.	MAX.	UNITS	
Delay Time					
Associate (Aj to Yn)		20	35	ns	See Notes 8 & 11
Associate (Ij to Yn)		45	65	ns	See Notes 8 & 11
Read-Out (Yn to Dj)		30	45	ns	See Notes 8 & 11
Write-In to Read-Out (Wj to Dj)		45	65	ns	See Notes 8 & 11
Write Pulse Width	35	20		ns	See Notes 8 & 11
Ij Set-Up Time (I_{SO})	10			ns	See Notes 8 & 11
Ij Hold Time ($_{HO}$)	10			ns	See Notes 8 & 11

NOTES

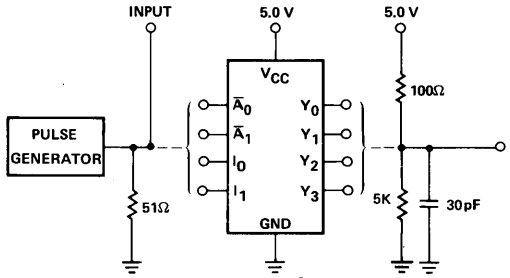
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Prior to this test write in a "0" in all or desired Memory cells as follows: Wj = Ij = 0V, Aj = V_{CC}.
9. Output sink current is supplied through a resistor to V_{CC}.
10. Connect an external 1K ohm + 1% resistor from V_{CC} to the output terminal for this test.
11. See AC test Figures on the following pages.

MODE OF OPERATION

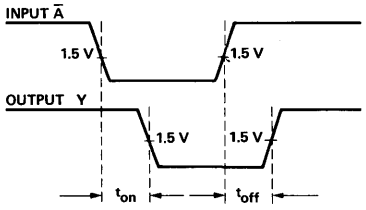
FUNCTION	$\overline{W_0}$ $\overline{W_1}$ $\overline{A_0}$ $\overline{A_1}$ I_0 I_1	REMARKS (Ref. Definitions & Glossary)	FUNCTION	$\overline{W_0}$ $\overline{W_1}$ $\overline{A_0}$ $\overline{A_1}$ I_0 I_1	REMARKS (Ref. Definitions & Glossary)		
HOLD	1 1 1 1 x x	NO OPERATION	HOLD	1 1 1 1 x x	NO OPERATION		
ASSOCIATE	1 1 1 0 x x	Question: ? $I_1=M_{i1}$ — YES — $Y_i=1$, $Y_k=0$; NO — $Y_i=Y_k=0$	WRITE-IN	1 0 1 1 x x	Forced Y_i=1, Y_k=0		WRITE I_1 into M_{i1}
	1 1 0 1 x x	Question: ? $I_0=M_{i0}$ — YES — $Y_i=1$, $Y_k=0$; NO — $Y_i=Y_k=0$		0 1 1 1 x x	Y_i=1, Y_k=0		WRITE I_0 into M_{i0}
	1 1 0 0 x x	Question: $I_1=M_{i1}$ and ? $I_0=M_{i0}$ — YES — $Y_i=1$, $Y_k=0$; NO — $Y_i=Y_k=0$		0 0 1 1 x x	Y_i=1, Y_k=0		WRITE I_1 and I_0 into M_{i1} and M_{i0}
			READ-OUT	1 1 1 1 x x	Y_i=1, Y_k=0		D_0= 1 - IF M_{i0}=1; 0 - IF M_{i0}=0
				1 1 1 1 x x	Y_i=1, Y_k=0		D_1= 1 - IF M_{i1}=1; 0 - IF M_{i1}=0
				1 1 1 1 x x	Y_i=0, Y_k=0		$D_0=D_1$ = 1

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY

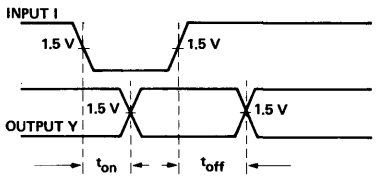


ASSOCIATE DELAY



NOTES:
1. When checking $\overline{A_0}$ let $\overline{A_1}$ = "1" and when checking $\overline{A_1}$ let $\overline{A_0}$ = "1".
2. $\overline{W_0}$ = $\overline{W_1}$. = "1".

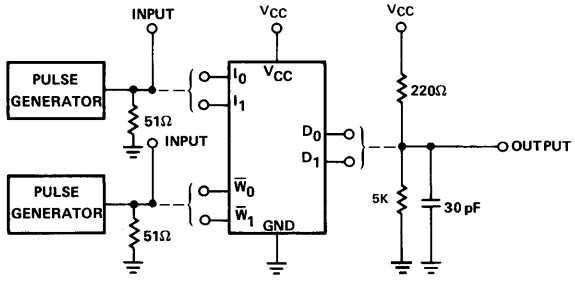
INPUT DELAY

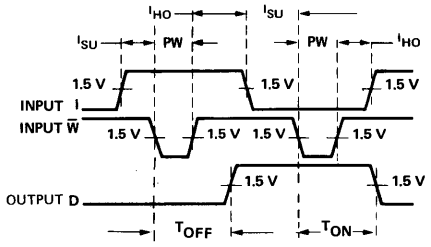


NOTES:
1. When checking I_1, $\overline{A_1}$ = "0" and $\overline{A_0}$ = "1" and when checking I_0, $\overline{A_0}$ = "0" and $\overline{A_1}$ = "1"
2. $\overline{W_0}$ = $\overline{W_1}$ = "1".

AC TEST FIGURES AND WAVEFORMS (Cont'd)

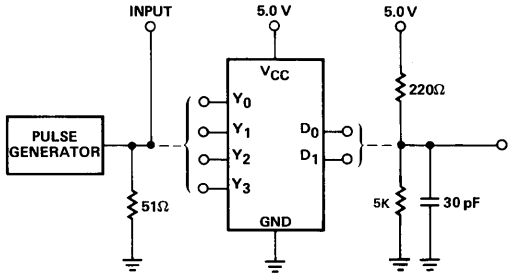
WRITE DELAY

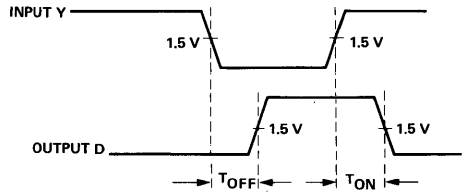




NOTES:
1. $A_0 = \overline{A}_1 = "1"$.
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY





NOTES:
1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1 = "1"$.
3. $\overline{A}_0 = \overline{A}_1 = "1"$.
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:
1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
   Frequency: 10 MHz ±5 MHz
   Amplitude: 0V to 3V
   Rise & Fall Times: 5 ns ±2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

I_j — Data Inputs
Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

$\overline{A}_j$ — Associate Controls
A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. Y_n = "1" = Match, Y_n = "0" Mismatch). A logical "1" at this pin forces all Y_n to a "1".

$\overline{W}_j$ — Write Enable
A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

Y_n — "Associate" Output and Address Selection Control
During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that A = 1 forces all Y_n = 1).

D_j — Data Output
These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under "Y_n" above.

GLOSSARY OF TERMS — SUBSCRIPTS

A.
- n = Word number = 0, 1, 2 and 3
- j = Bit number = 0 or 1
- i = Input/Output number(s) associated with cell(s) upon which a "Write-in", "Read-out" or other function is being performed.
- k = Input/Output number(s) other than "i" above.
- M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples
1. I_j for bit "1" equals I_1.
2. $M_{nj} = M_{10}$ = word "1" bit "0".
3. $Y_i = 0$, $Y_k = 1$: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3} = 0$ and $Y_{0,2} = 1$.

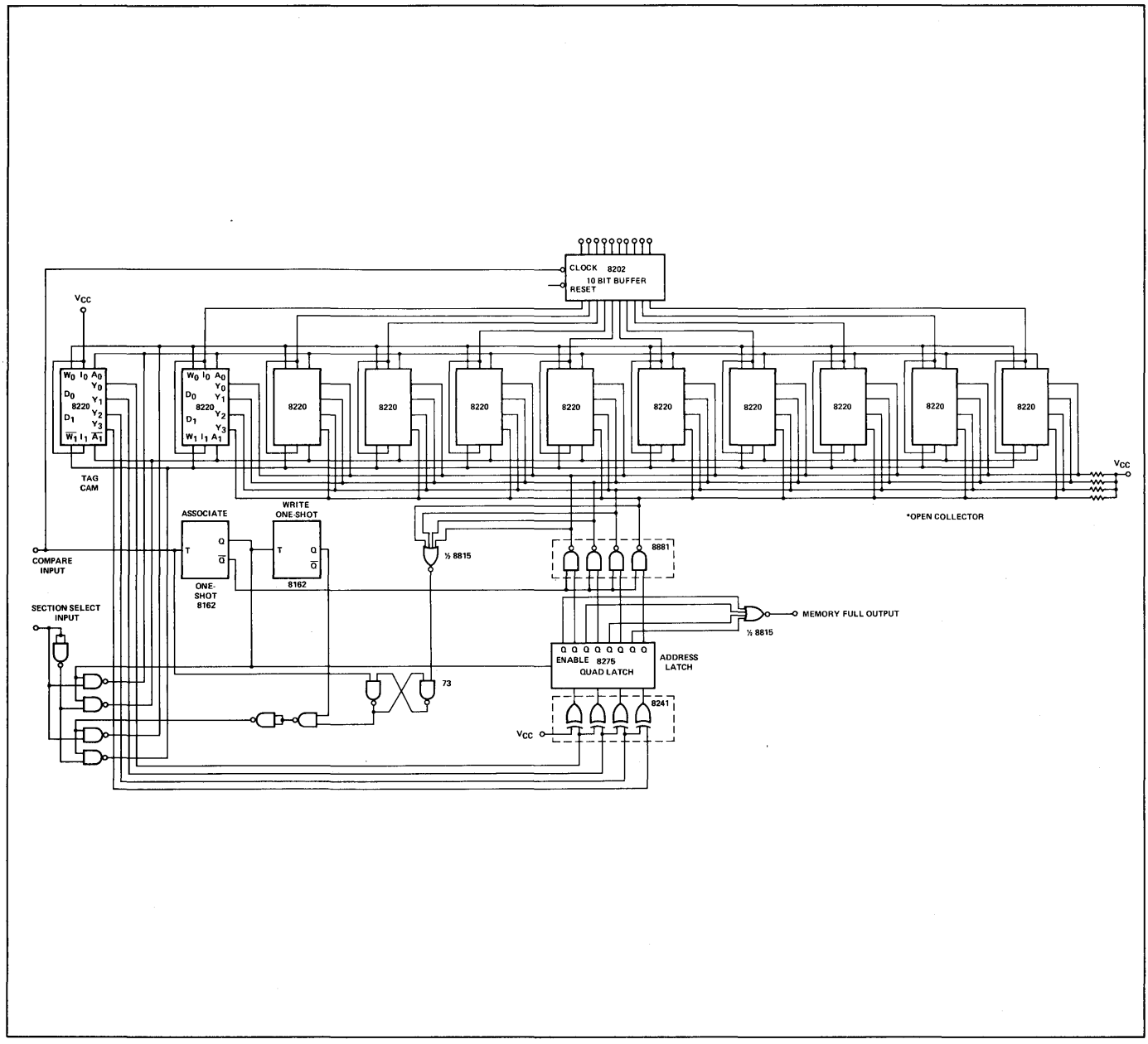
APPLICATION: LEARNING MEMORY

This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning" i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

By monitoring the Y_n lines of the tag CAM, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).



DESCRIPTION

The 8223 is a TTL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which permits wired AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum. The 8223 may be programmed to any desired pattern by the user. (See fusing procedure.) This feature is ideal for prototype hardware and systems requiring propriety codes.

A Truth Table/Order Blank is included on page 4-43 for ordering custom patterns.

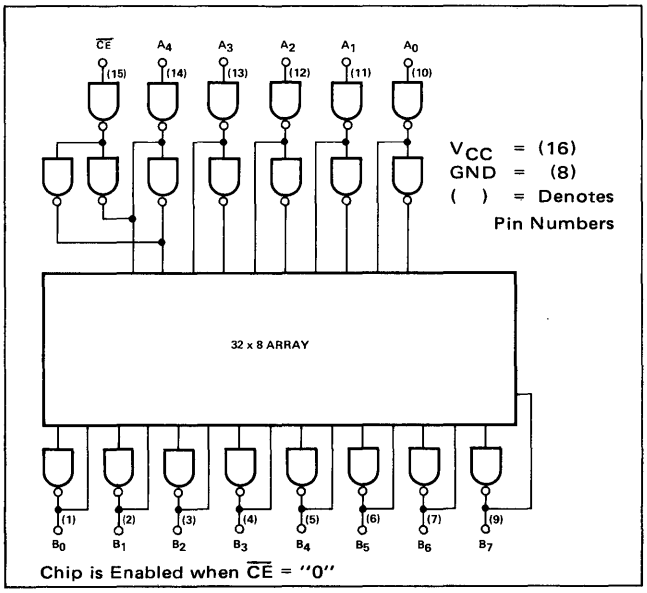
FEATURES

- **BUFFERED ADDRESS LINES**
- **ON THE CHIP DECODING**
- **CHIP ENABLE CONTROL LINE**
- **OPEN COLLECTOR OUTPUTS**
- **DIODE PROTECTED INPUTS**
- **NO SEPARATE FUSING PINS**
- **BOARD LEVEL PROGRAMMABLE**

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

S8223 $-55°C \leq T_A \leq +125°C$ N8223 $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

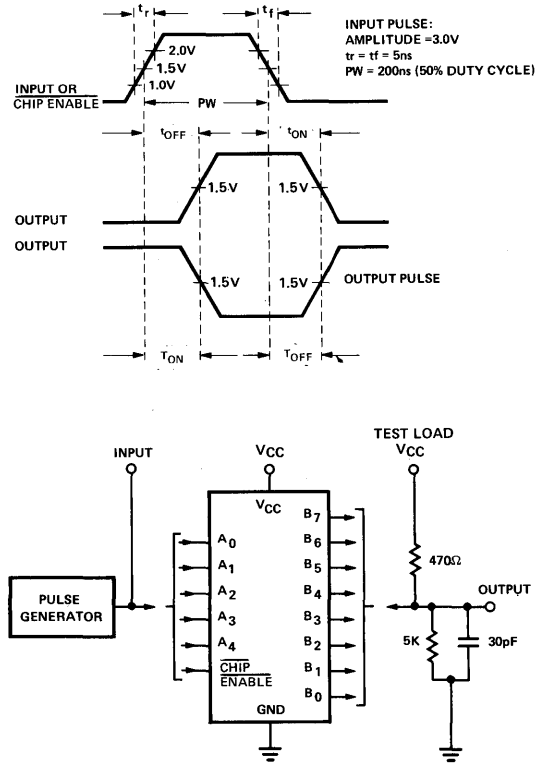
CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
"1" Output Leakage Current (N8223-)			100	μA			2.0V	5.5V	13
(S8223-)			250	μA				2.7V	
"0" Output Voltage (N8223-) (S8223-)			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
(N8223-)			0.5	V	0.8V	2.0V	0.8V	16mA	6,10
"1" Input Current									
An, Address			40	μA		4.5V			
$\overline{\text{Chip Enable}}$ Input			80	μA			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1		-1.6	mA	0.4V		0.4V		
Power Consumption		62/310	77/400	mW/mA		4.5V	4.5V		14

SWITCHING CHARACTERISTICS S8223 $-55°C \leq T_A \leq 125°C$, N8223 $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Access Time (t_{ON}, t_{OFF})					
Address		35	50	ns	$T_A = 25°C$ Only
S8223			65	ns	Full Temp
N8223			60	ns	Full Temp
Chip Select		35	50	ns	$T_A = 25°C$ Only
S8223			60	ns	Full Temp
N8223			55	ns	Full Temp

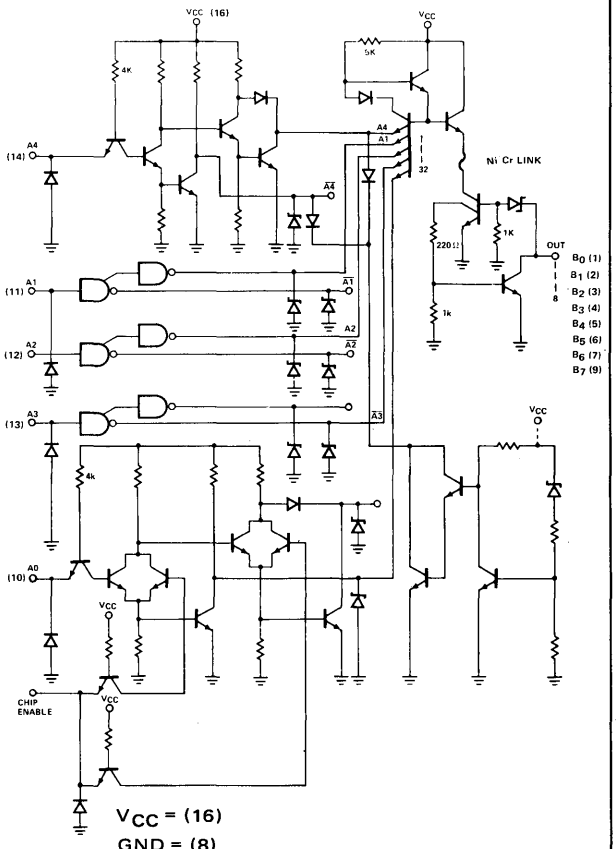
NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
14. $V_{CC} = 5.25V$.

AC TEST FIGURE AND WAVEFORMS



Ground Pin 15 When Testing Address-Output Delays

SCHEMATIC DIAGRAM



V_{CC} = (16)
GND = (8)
(8) denotes pin number ( )

8223 PROGRAMMING PROCEDURE

The 8223 Standard part is shipped with all outputs at logical "0". To write a logical "1" proceed as follows:

Simple Programming Procedure using "bench" Equipment (See below)

1. Start with pin 8 grounded and V_{CC} removed from pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground (i.e., 0.4V maximum) for a "0", and +5.0V (i.e., +2.8V minimum) for a "1" at the address input lines.
5. Apply +12.5V ±0.5V to the output to be programmed through a 390 ohm ±10% resistor. (Program one output at a time.)
6. After a short delay apply +12.5V to V_{CC} (pin 16) and remove as quickly as possible (rise time of 50μsec or less). The V_{CC} overshoot should be limited to 1.0V maximum. If necessary, a clamping circuit should be used.
   NOTE: Normal practice in test fixture layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A capacitor of 10 microfarads minimum, connected from the +12.5V to ground, should be located close to the unit being programmed.
7. Verify that the bit has programmed by applying 5 volts to V_{CC} and 5 volts through a 1k resistor to the output.
8. Proceed to the next output and repeat, or change address and repeat.
9. Continue until the entire bit pattern is programmed into your custom 8223.
10. If during verification a bit had been found not to have programmed, return to that bit and repeat the programming procedure once.

Fast Programming Procedure

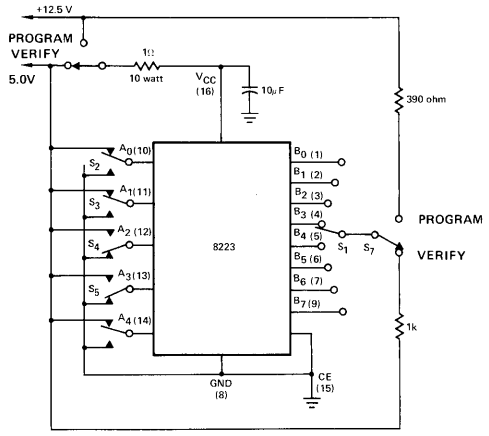
1. Remove V_{CC} (open or ground pin 16).
2. Remove any load from the output.
3. Ground $\overline{CE}$ (pin 15)
4. Address the word to be programmed by applying 5 volts for a "1" and ground for a "0" to the address lines.
5. Apply +12.5V ±0.5V to the output to be programmed through a 390 ohm ±10% resistor. (Program one output at a time.)
6. After a minimum delay of 100μsec, apply +12.5V to V_{CC} (pin 16) for 1.0mS. The V_{CC} rise time must be 50μsec or less. Limit the V_{CC} overshoot to 1.0 volts max.
7. Reduce V_{CC} to ground (<0.5V) and remove the load from the output.
8. Repeat steps 5 and 6 for other outputs of the same word, or repeat 4 through 6 for a different word until the entire bit pattern is programmed.

After programming the 8223, the unit should be checked to insure the code is correct.

BOARD LEVEL PROGRAMMING PROCEDURE FOR THE 8223

The chip select controls which 8223 is being programmed when several PROMS are collector OR'd. To program in this manner, the only change required is to reduce the 390 ohm resistor to $\frac{200 \text{ ohm}}{N}$ where N is the number of outputs tied together ($2 \leqslant N \leqslant 12$).

MANUAL PROGRAMMER DIAGRAM



NOTES
1. The 10μF capacitor across pin 16 to ground is required to eliminate noise from V_{CC}.
2. During programming switch S_8 must be in the verify position long enough for the 10μF capacitor to discharge to 5.0 volts.

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64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM)

8225

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8225 is a TTL 64-bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 8225 is ideally suited for application in scratch pads and high-speed buffer memories.

Words are selected through a 4-input binary decoder when the chip enable input ($\overline{CE}$) is at logic "0". Data is written into the memory when Read Enable (RE) is at logic "0" and read from the memory when RE is at logic "1".

The outputs of the 8225 are logical "1" during write operation, therefore, inputs and outputs can be commoned in busses to reduce the number of I/O leads. Output collectors are uncommitted.

FEATURES

- CHIP ENABLE LINE FOR EXPANSION
- OPEN COLLECTOR OUTPUTS FOR EXPANSION
- ON THE CHIP DECODING
- ALL OUTPUTS "1" DURING WRITING
- DIODE PROTECTED INPUTS

APPLICATIONS

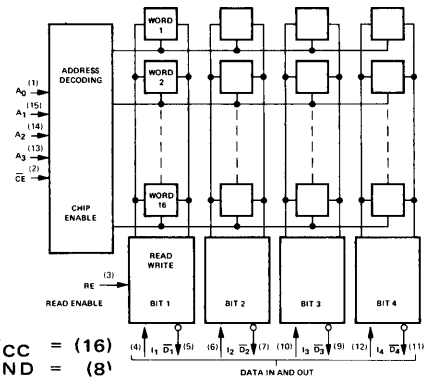
SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS (First in–first out)
CONTROL STORE

TRUTH TABLE

RE	$\overline{CE}$ (Chip Enable)	MODE	OUTPUTS
0	0	Write	"1"
1	0	Read	Information
X	1	Chip Disable	"1"

X = Either State

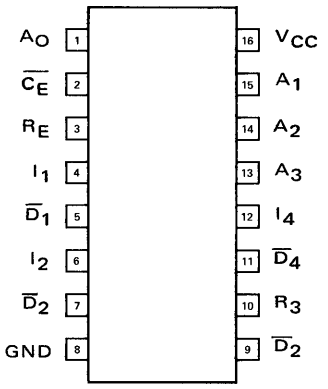
BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.
Chip is enabled when $\overline{CE}$ = "0"

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS $0°C \leq T_A\ 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

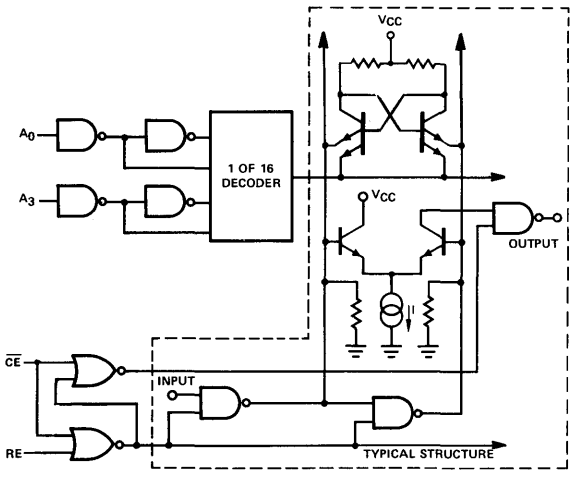
CHARACTERISTICS	LIMITS				CHIP ENABLE	INPUTS		DATA INPUTS	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS		WRITE	ADDRESS			
"0" Output Voltage			.4	V	.8V	Pulse			16mA	6,8,0,
"1" Output Leakage Current			100	μA	.8V	Pulse		.8V	5.25V	8,9
"0" Input Current	-.1		-1.6	mA	.4V	.4V	.4V	.4V		11
"1" Input Current										
Chip Enable			80	μA	4.5V					
Write, Address, Data			40	μA	4.5V	4.5V	4.5V	4.5V		11
Input Clamp Voltage	-1.5			V	-18mA	-18mA	-18mA	-18mA		11
Power Consumption		80 400	110/ 550	mA/ mW	0V	5V	0V	0V		10,5

SWITCHING CHARACTERISTICS $0 \leqslant T_A \leqslant 75^\circ C$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Minimum Write Pulse Width (W_{PW})	30	18		ns	
Input Setup Time (I_{SU})	20	18		ns	
Input Hold Time (I_{HO})	10	0		ns	
Address Setup Time (A_{SU})	10			ns	
Address Hold Time (A_{HO})	10			ns	
Access Time (T_A)			60	ns	See Note 12
Access Time (T_A)		35	50	ns	$T_A = 25^\circ C$, See Note 12
Data Pulse Width (D_{PW})	20			ns	
Write Recovery Time (T_{WR})		25	40	ns	
Write Access Time (T_{WA})		25	50	ns	
Chip Enable Recovery Time (T_{CR})		20	35	ns	
Chip Enable Access Time (T_{CA})		20	35	ns	

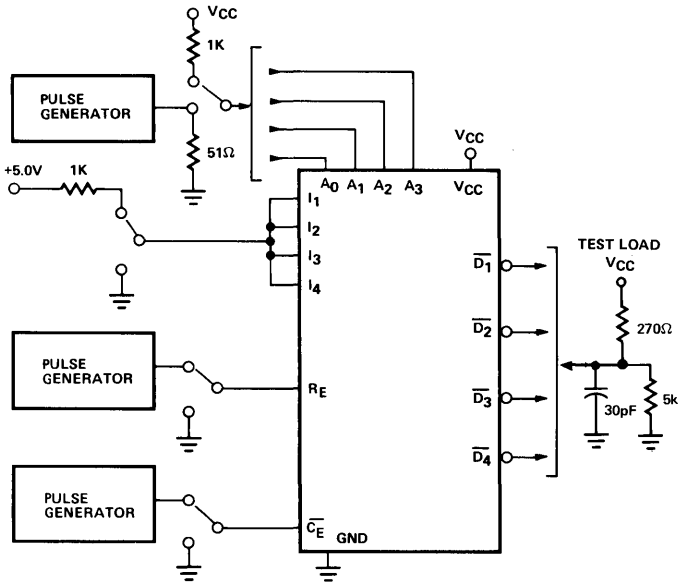
NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. $V_{CC} = 5.0V$.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
9. For any given binary code on the Address inputs the Write input must be momentarily brought to a logical "0" level.
10. All sense outputs in "0" state.
11. Test each input one at a time.
12. Address Pulse Width (A_{PW}) is 40ns for this test.
13. Rise and fall times of inputs for AC tests are ≤5ns. Pulse amplitudes are 2.5 volts and measurements are made at 1.5 volts.

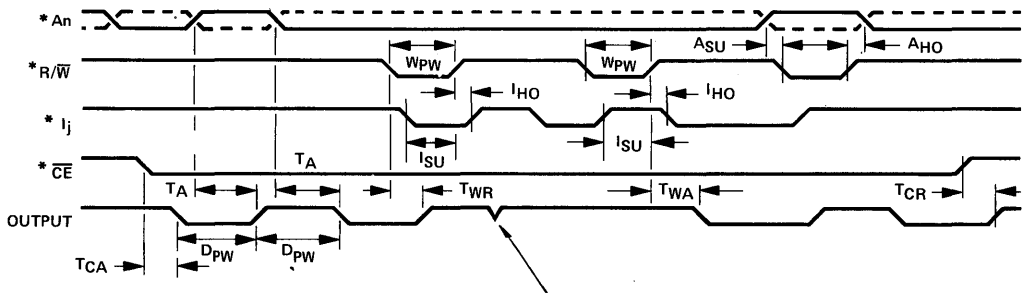
FUNCTIONAL DIAGRAM



ONE LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

AC TEST FIGURES AND WAVEFORMS





NOTE: NEGATIVE TRANSITION DOES NOT GO BELOW 2.6 VOLTS AND GENERALLY IS NOT MEASURABLE.

* See Note 13.

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4096 BIT BIPOLAR ROM (1024x4 ROM) 8228

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8228 is a 4096 Bit Bipolar Read Only Memory organized as 1024 words by 4 bits per word. Available in a 16 pin dual in-line package, the 8228 can provide very high bit packing density by replacing four standard 256X4 ROMS.

The 8228 is fully TTL compatible and includes on-the-chip decoding. Typical access time is 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I - CD162, while custom circuits are identified as N8228I - CXXX. A truth table/order blank is included on page 4-46 for ordering custom patterns.

See page 4-35 for CD162 Pattern and USASCII Row Character Generator.

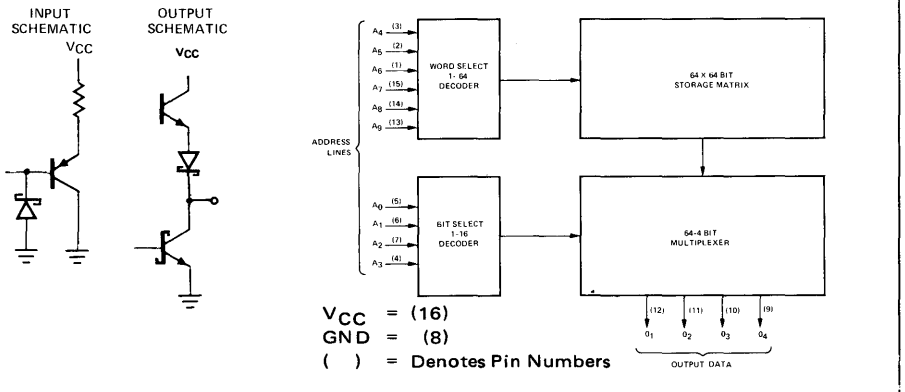
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TOTEM POLE OUTPUTS
- DIODE PROTECTED INPUTS
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)

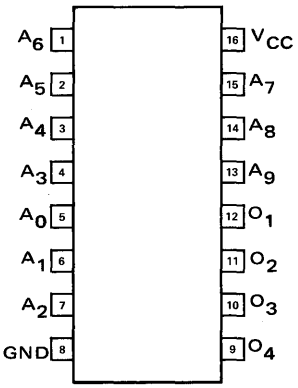
APPLICATIONS

MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATION
CONTROL STORE

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 11.2 mA	
"1" Output Voltage	2.7			V	I_{out} = -1.0 mA	
"0" Input Current		-10	-400	μA	V_{in} = 0.45V	
"1" Input Current		1	25	μA	V_{in} = 5.5V	
Input Threshold Voltage						
"0" Level			.85	V		
"1" Level	2.0			V		

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Input Clamp Voltage	-1.2			V	I_{in} = -18mA	
Power Consumption		140	170	mA	O_1 to O_3 = "0"	
Output Short Circuit Current	-20		-70	mA	V_{OUT} = 0 Volts	

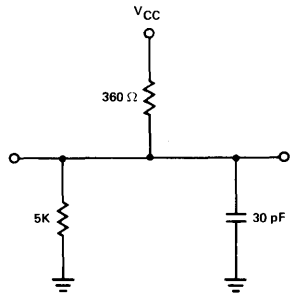
SWITCHING CHARACTERISTICS $0 \leqslant T_A \leqslant 75^oC$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output		50	70	ns		5

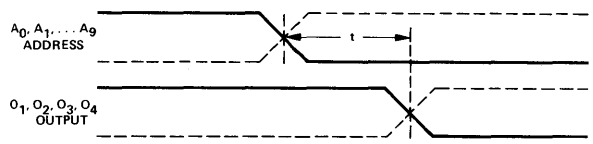
NOTES
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30mA. Output currents must not exceed ±100mA. Storage temperature must be between -60°C to +150°C.
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

AC TEST FIGURE AND WAVEFORM

TEST LOAD



READ CYCLE



DESCRIPTION

The 82S06 and 82S07 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 45ns. The typical write time (the time between applying one address and storing data) is 30ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S06 and 82S07 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

The memories are TTL compatible and operate from single 5 volt supply.

APPLICATIONS

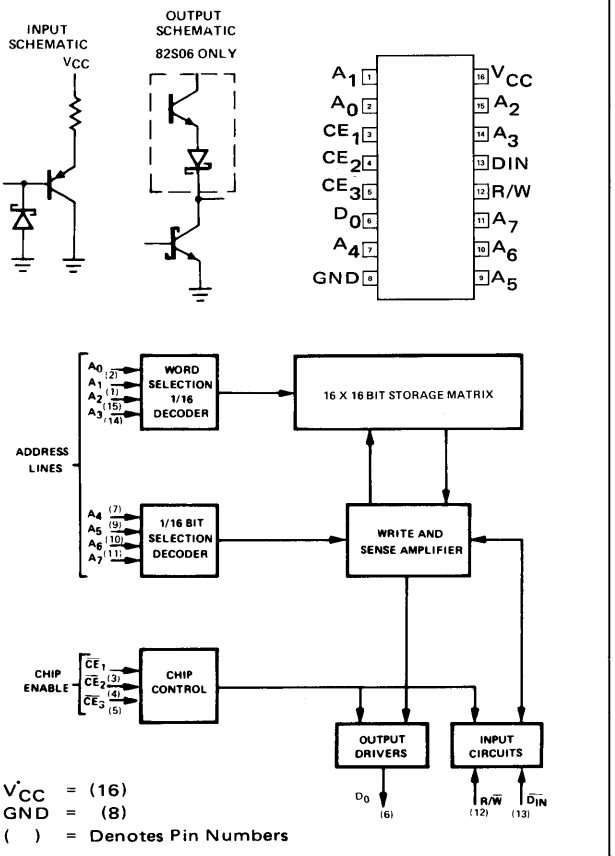
BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 μA INPUT LOADING**
- **TRI-STATE (82S06) OR OPEN COLLECTOR (82S07) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM

256 BIT BIPOLAR RANDOM ACCESS MEMORY



VCC = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT.

ELECTRICAL CHARACTERISTICS (T_A = 0 to 75°C, V_{CC} = 5.0V ±5) Note 1, 2, 3

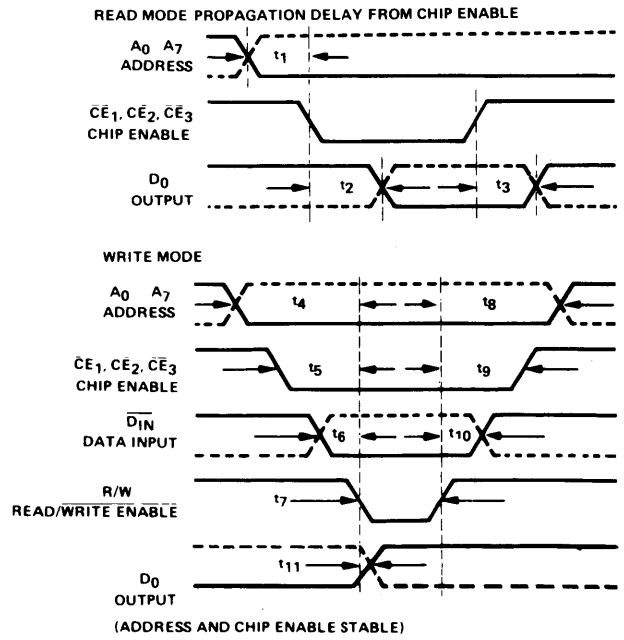
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		-10	-100	μA	V_{in} = 0.45V	
"1" Input Current		<1.0	25	μA	V_{in} = 5.5V	
"0" Output Voltage		0.35	0.45	V	I_{out} = 16mA	
Output Leakage Current (82S07)		<1.0	40	μA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", V_{out} = 5.5V	
Output "off" Current (82S06)		<1.0	±100	μA	$\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ = "1", 0.45 ≤ V_{out} ≤ 5.5V	
"1" Output Voltage (82S06)	2.6			V	$\overline{CE}_1$ = $\overline{CE}_2$ = $\overline{CE}_3$ = "0" I_{out} = -3.2mA	
"0" Input Threshold			0.85	V		
"1" Input Threshold	2.0		2.0	V		
Power Consumption		80/400	115/604	mA/mW		
Input Clamp Voltage	-1.2	-0.8		V	I_{in} = -18mA	
Input Capacitance		5.0		pF		
Output Capacitance		8.0		pF		
Output Short Circuit Current (82S06)	-20		-70	mA	V_{out} = 0V	

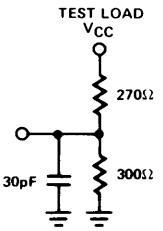
SWITCHING CHARACTERISTICS $0 \leqslant T_A \leqslant 75^oC$, $4.75 \leqslant V_{CC} \leqslant 5.25V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output			45	65	ns	T_A=25° C Only	4,5
Access Time—Address to Output				80	ns		
Address Set-Up Time (read)	t_1	25	10	80	ns		
Propagation Delay							4,5
Chip Enable to Output Enable	t_2		25	40	ns		
Propagation Delay							4,5
Chip Enable to Output Disable	t_3		25	40	ns		
Address to Write Enable							4,5
Set-Up Time	t_4	25	5		ns		
Chip Enable to Write Enable							4,5
Set-Up Time	t_5	10	0		ns		
Data Input to Write Enable							4,5
Set-Up Time	t_6	10	0		ns		
Write Enable Pulse Width	t_7	30	15		ns		4,5
Address Hold Time	t_8	10	0		ns		4,5
Chip Enable Hold Time	t_9	10	0		ns		4,5
Data Input Hold Time	t_{10}	10	0		ns		4,5
Write Enable Propagation Delay	t_{11}		30	40	ns		4,5

NOTES
1. Positive current is defined as into the terminal referenced
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30mA. Output currents must not exceed ±100mA. Storage temperature must be between −60°C to +150°C.
4. Refer to Timing Diagram for definition of terms and test load.
5. Rise and fall times for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5 volts.

TIMING DIAGRAM





t_1 = set up time for an address input to chip enable for valid data at outputs,
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

DESCRIPTION

The 82S12/112 is a Schottky TTL 32 bit multiport memory organized in 8 words of 4 bits each. The device is ideally suited for high speed accumulators and buffer memories.

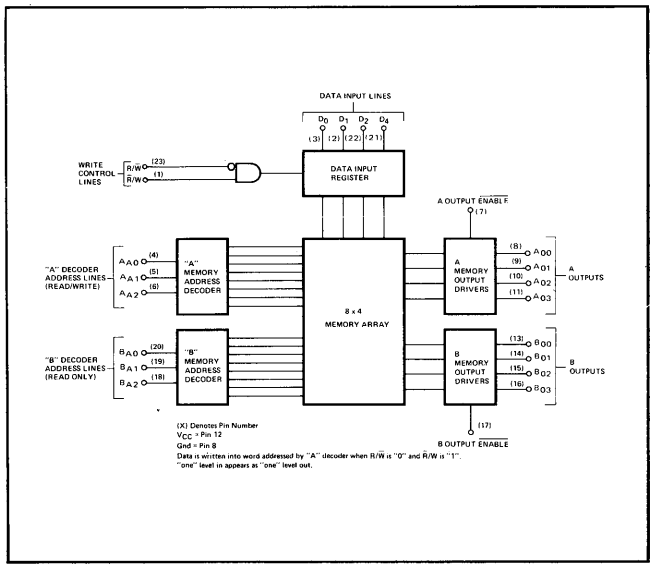
Stored data is addressed through 2 independent sets of 3-input decoders, and read out when the corresponding output enable line is low. Two separate word locations can, therefore, be read at the same time by enabling both the A and B output drivers. In addition, data can be read and written at the same time by utilizing the "A" address to specify the location of the word to be written, and the "B" address to specify the word to be read.

The 82S12/112 can be used in larger memory arrays since it includes all the control logic required to disable the chip and the outputs are open-collector devices suitable for "Wire-ORing."

FEATURES

- LOW CURRENT INPUT BUFFERS (−25μA TYPICAL)
- SEPARATE INPUT DECODERS FOR EACH WORD
- SEPARATE OUTPUT ENABLE LINES FOR EACH WORD
- OPEN COLLECTOR (82S12) OR TRI-STATE (82S112) OUTPUTS
- 2 WRITE ENABLE LINES
- FAST ACCESS (20 ns TYPICAL)
- USEFUL 8 X 4 ORGANIZATION
- TTL COMPATIBLE
- NON INVERTING DATA LINES

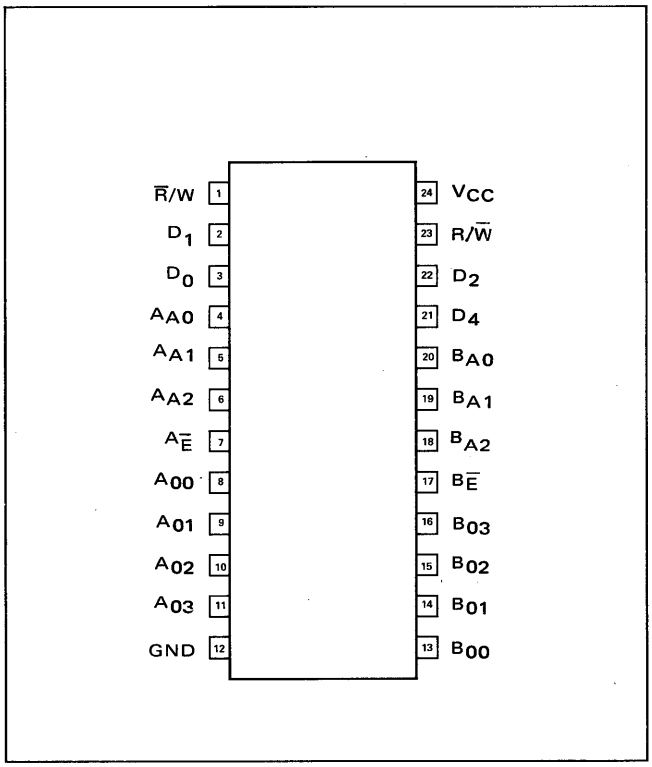
BLOCK DIAGRAM



APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
GENERAL REGISTER

PIN CONFIGURATION



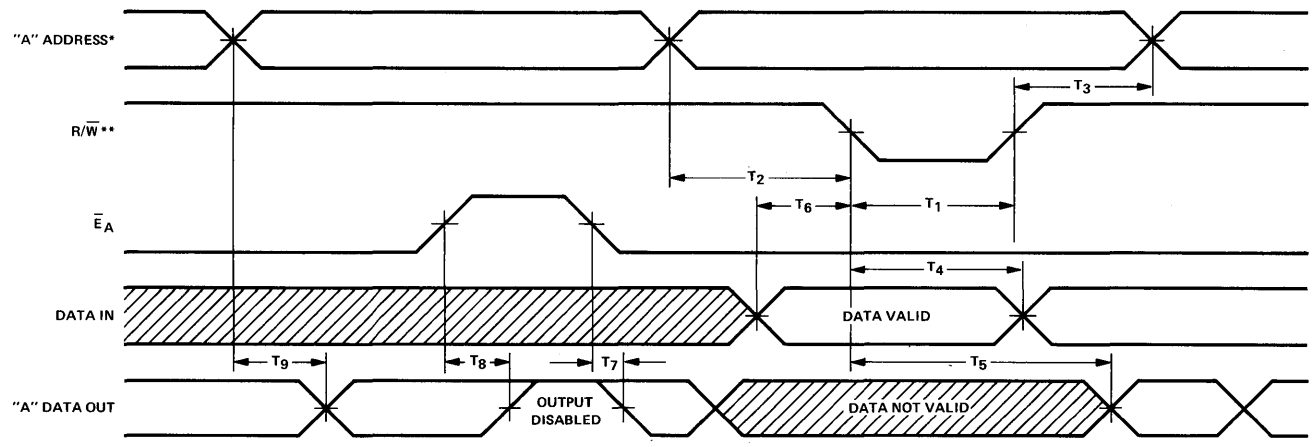
TRUTH TABLE

R/W	R/W	A OUTPUT ENABLE	B OUTPUT ENABLE	MODE	OUTPUTS A	OUTPUTS B
0	X	1	1	Outputs Disabled	"1"	"1"
0	X	1	0	Read	"1"	Data
0	X	0	1	Read	Data	"1"
0	X	0	0	Read	Data	Data
1	1	1	1	Read	"1"	"1"
1	1	1	0	Read	"1"	Data
1	1	0	1	Read	Data	"1"
1	1	0	0	Read	Data	Data
1	0	1	1	Write	"1"	"1"
1	0	1	0	Write	"1"	Data "B" Address
1	0	0	1	Write	Data Being Written	"1"
1	0	0	0	Write	Data Being Written	Data "B" Address

OBJECTIVE ELECTRICAL SPECIFICATIONS $0°C \leq T_A \leq 75°C$; $-4.75\ V \leq V_{CC} \leq 5.25\ V$.

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
Input "0" Current				−250	μA	V_{in} = 0.45 V
Input "1" Current				25	μA	V_{in} = 5.5 V
Input "0" Threshold Voltage				0.85	V	
Input "1" Threshold Voltage		2.0			V	
Input Clamp Voltage		−1.2			V	I_{in} = −18 mA
Output "0" Current		16			mA	V_{out} = 0.5 V
Output "0" Current		9.6				V_{out} = 0.45 V
Output "1" Voltage (825112)		2.6			Volts	I_{out} = −3.2 mA
Output Off Current (82S12)				40	μA	$V_{out} \leq 5.5$ V
Output Off Current (82S112)		−40		+40	μA	$0.45 \leq V_{out} \leq 5.5$ V
Power Consumption			110/550	160/840	mA/mW	Outputs Enabled
Write Pulse Width	T_1	30	15		ns	T_A = 25°C Only
	T_1	45				
Address Set Up Time	T_2		10		ns	
Address Hold Time	T_3		0		ns	
Data Input Hold Time	T_4		0		ns	
Write Access Time	T_5		30		ns	
Data Input Set Up Time	T_6		5		ns	
Output Enable Time	T_7		10	20	ns	
Output Disable Time	T_8		10	20	ns	
Address Access Time	T_9		20	30	ns	

TIMING DIAGRAM



T_1 WRITE PULSE WIDTH – Width of write pulse (when R/W="1" and R/W="0")

T_2 ADDRESS SETUP TIME – Required delay between beginning of valid Address and beginning of Write pulse.

T_3 ADDRESS HOLD TIME – Required delay between end of Write pulse and end of valid Address.

T_4 DATA INPUT HOLD TIME – Required delay between start of Write pulse and end of Valid Data input.

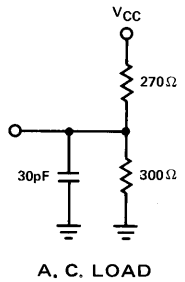
T_5 WRITE ACCESS TIME – Delay between beginning of Write pulse and Data Out at new value.

T_6 DATA INPUT SET-UP TIME – Required delay between beginning ov Valid Data Input and start of Write pulse.

T_7 OUTPUT ENABLE TIME – Delay between beginning of Output Enable high and when Data Output becomes valid.

T_8 OUTPUT DISABLE TIME – Delay between when Output Enable becomes low and Data Output is in off state.

T_9 ADDRESS ACCESS TIME – Delay between beginning of Valid Address (with Output Enable high, R/W high and R/W low) and when Data Output becomes valid.



A. C. LOAD

NOTES

*"B" Address functions identically in read mode. No write mode through B address decoder.

**R/W input is either the reverse of R/W or held high.

Outputs can be disabled during write cycle to penetrate a known output state during write.

DESCRIPTION

The 82S16 and 82S17 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 30ns. The typical write time (the time between applying one address and storing data) is 30ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S16 and 82S17 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

The memories are TTL compatible and operate from single 5 volt supply.

APPLICATIONS

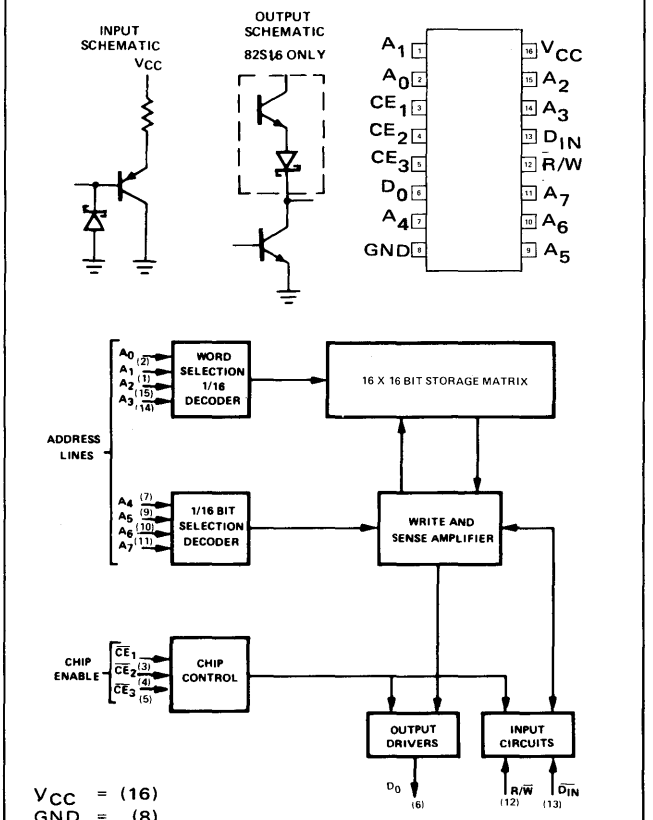
BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 μA INPUT LOADING**
- **TRI-STATE (82S16) OR OPEN COLLECTOR (82S17) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM

256 BIT BIPOLAR RANDOM ACCESS MEMORY



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

"ONE" LEVEL IN ON DATA INPUT APPEARS AS "ZERO" LEVEL OUT. Chip is enabled when $\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3$ = "0"

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$) Note 1, 2, 3

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		-10	-100	μA	V_{in} = 0.45V	
"1" Input Current		<1.0	25	μA	V_{in} = 5.5V	
"0" Output Voltage		.35	0.45	V	I_{out} = 16mA	
Output Leakage Current (82S17)		<1.0	40	μA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", V_{out} = 5.5V	
Output "off" Current (82S16)		<1.0	40	μA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", $0.45 \leq V_{out} \leq 5.5V$	
"1" Output Voltage (82S16)				V	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3$ = "0" I_{out} = -3.2mA	
"0" Input Threshold	2.6			V		
"1" Input Threshold	2.0			V		
Power Consumption		80/400	115/604	mA/mW		
Input Clamp Voltage	-1.2	-.8		V	I_{in} = -18mA	
Input Capacitance		5		pF		
Output Capacitance		8		pF		
Output Short Circuit (82S16)	-20		-70	mA	V_{out} = 0V	

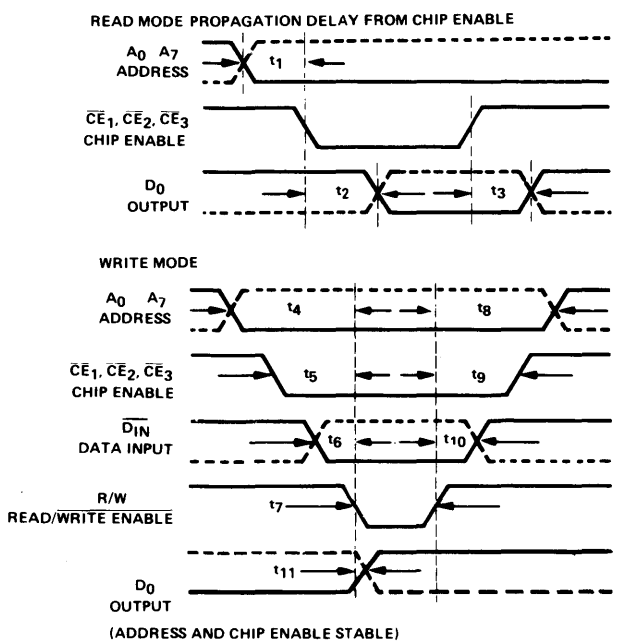
SWITCHING CHARACTERISTICS $0 \leqslant 75°C, 4.75 \leqslant V_{CC} \leqslant 5.25V$

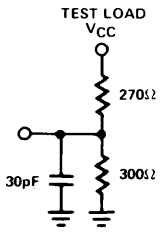
CHARACTERISTICS		LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTES
Access Time—Address to Output			30	50	ns	$T_A = 25°C$ Only	4,5
Access Time—Address to Output				60			
Address Set-Up Time (read)	t_1	25	10	65	ns		
Propagation Delay							4,5
Chip Enable to Output Enable	t_2		20	40	ns		
Propagation Delay							4,5
Chip Enable to Output Disable	t_3		20	40	ns		
Address to Write Enable							4,5
Set-Up Time	t_4	20	5		ns		
Chip Enable to Write Enable							4,5
Set-Up Time	t_5	10	0		ns		
Data Input to Write Enable							4,5
Set-Up Time	t_6	10	0		ns		
Write Enable Pulse Width	t_7	30	15		ns		4,5
Address Hold Time	t_8	0	0		ns		4,5
Chip Enable Hold Time	t_9	0	0		ns		4,5
Data Input Hold Time	t_{10}	0	0		ns		4,5
Write Enable Propagation Delay	t_{11}		30	40	ns		4,5
Output Short Circuit Current (82S16)		−20		-70	mA	$V_{out} = 0V$	4,5

NOTES:

1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V, Input currents must not exceed 30mA, Output currents must not exceed 100mA, Storage temperature must be between -60 C to +150 C.
4. Refer to Timing Diagram for definition of terms and test load.
5. Rise and fall times for this test must be 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5 volts.

TIMING DIAGRAM





t_1 = set up time for an address input to chip enable for valid data at outputs,
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

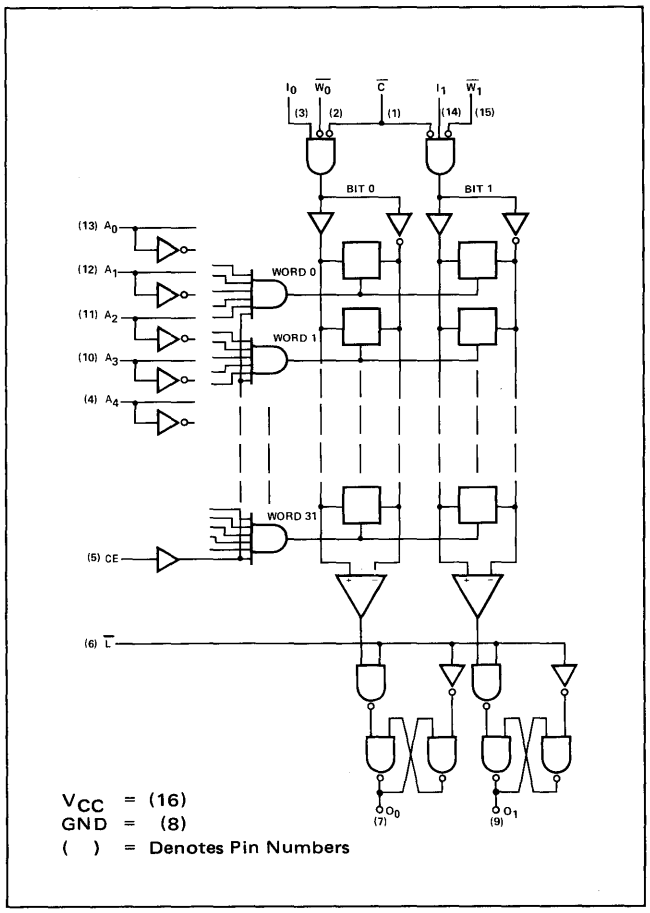
FEATURES

- BUFFERED ADDRESS LINES
- ON CHIP LATCHES
- ON CHIP DECODING
- BIT MASKING CONTROL LINES
- ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS WITH 40mA CAPABILITY
- PROTECTED INPUTS
- VERY HIGH SPEEDS (25ns TYP)

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C; 4.75V \leq V_{CC} \leq 5.25$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.45	V	V_{out} = 40mA	
"1" Output Leakage Current			40	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			−1.6	mA	V_{in} = 0.45V	
"1" Input Current (All Inputs)			25	μA	V_{in} = 5.5V	
Input "0" Threshold Voltage			0.85	V		
Input "1" Threshold Voltage	2.0			V		
Power Consumption			130/683	mA/mW		
Input Clamp Voltage	−1.2				I_{in} = −18mA	

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C, 4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Read Access Time Address to Output	t_1		25	50	ns		
Address Set-Up Time	t_2	15	8		ns		
Data Set-Up Time	t_3	20	15		ns		
Address Hold Time	t_4	0			ns		
Control or Write Pulse Width	t_5	20	15		ns		
Write Access Time	t_6		20	25	ns		
Address to Latch Set-Up Time	t_7		25	50	ns		
Latch Address to Address Hold Time	t_8	10	7		ns		
Delatch Access Time	t_9		15	25	ns		
Data Hold Time Earliest	t_{10}	5	0		ns		

AC WAVEFORM

Read Access Time

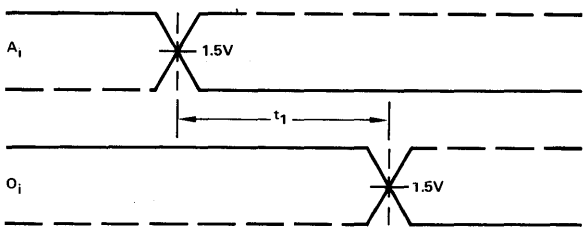
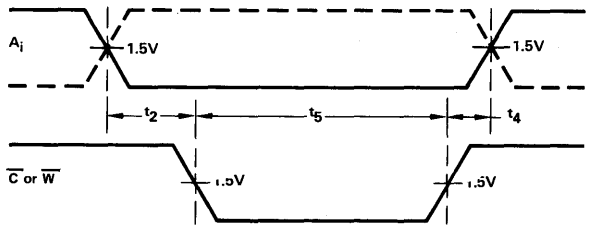


FIGURE 1

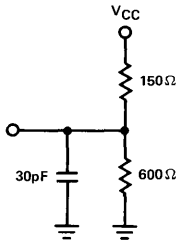
Address Setup and Hold Time



$t_r = t_f \leq 5$ ns, INPUT VOLTAGE = 2.8 Volts

FIGURE 2

TEST LOAD



AC WAVEFORMS

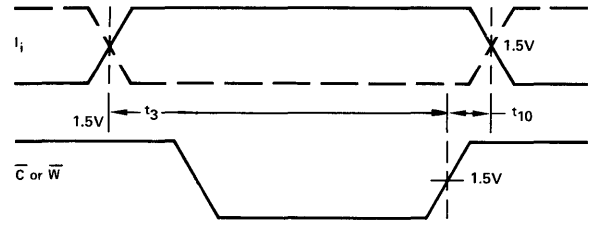


Fig. 3 Data Setup and Hold Time

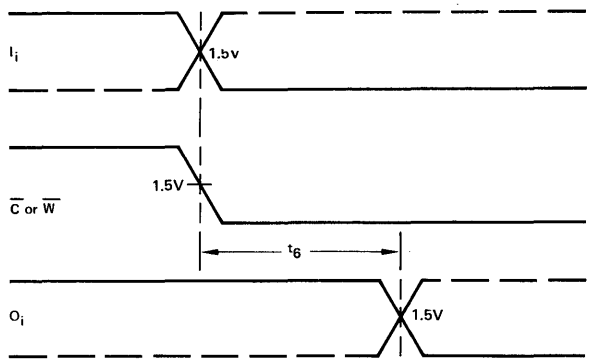


Fig. 4 Write Access Time

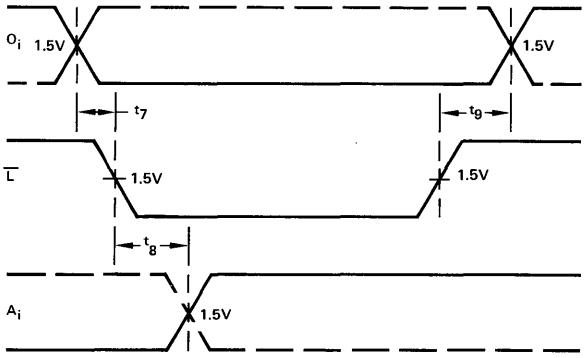
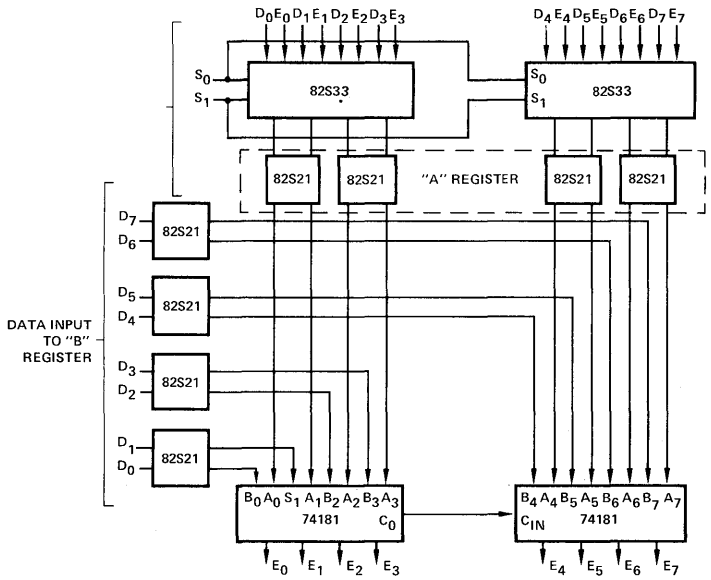


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

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256-BIT BIPOLAR PROGRAMMABLE ROM (32×8 PROM)
(82S23 OPEN COLLECTOR)(82S123 TRI-STATE)

82S23
82S123

OBJECTIVE SPECIFICATION

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S23 (open Collector Outputs) and the 82S123 (Tristate Outputs) are Bipolar 256 Bit Read Only Memories organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. A chip enable line is provided and the outputs are bare collector or Tristate to allow for memory expansion capability.

The 82S23 and 82S123 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35 nS.

The standard 82S23 and 82S123 are supplied with all outputs at a logical "0." If a programmed unit is required the Truth Table/Order Blank on page 4-43 of the TTL MSI/Memory Handbook may be used.

FEATURES

- PNP INPUTS
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- A CHIP ENABLE LINE
- OPEN COLLECTOR OR TRISTATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- BOARD PROGRAMMABLE

APPLICATIONS

PROTOTYPING

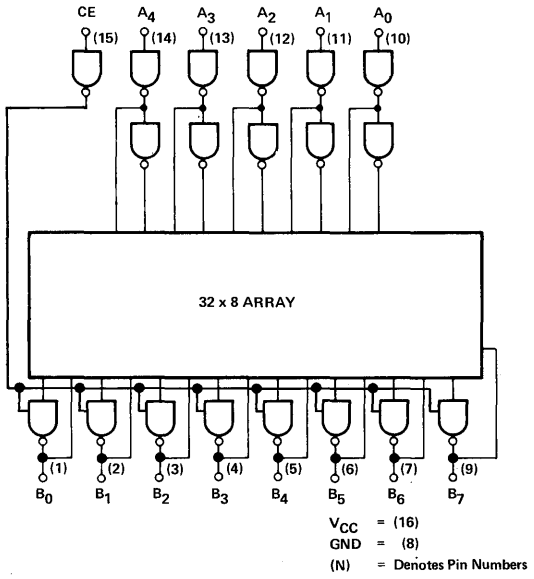
VOLUME PRODUCTION

MICROPROGRAMMING

HARDWIRED ALGORITHMS

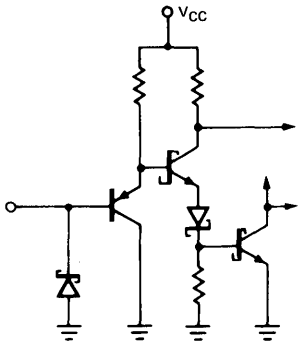
CONTROL STORE

LOGIC DIAGRAM

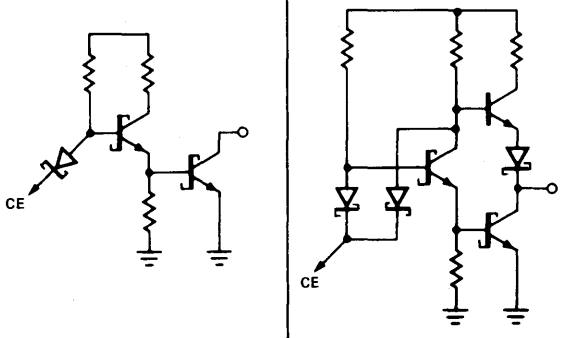


INPUT/OUTPUT SCHEMATIC DIAGRAMS

INPUT SCHEMATIC



OUTPUT SCHEMATICS



82S23 82S123

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} = 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 20mA	
"0" Output Voltage			0.45	V	I_{out} = 9.6mA	
"1" Output Leakage			40	μA	CE = "1" V_{out} = 5.5V	12
82S23			100	μA	CE = "0" V_{out} = 5.5V	12
82S123	-40		+40	μA	V_{out} = 0.5V/V_{out} = 5.5V CE = "1"	12
"1" Output Current 82S123	-2.0			mA	V_{out} = 2.4V, CE = "0"	After Fusing
"0" Input Current			-250	μA	V_{in} = 0.45V	
"1" Input Current			50	μA	V_{in} = 5.5V	
Input Threshold Voltage						
"0" Level	.85			V		
"1" Level			2.0	V		
Propagation Delay						
Address to Output		35	50	ns	T_A = 25°C only	
			60	ns		
Enable to Output		15	30	ns	T_A = 25°C only	
			35	ns		
Input Calmp Voltage	-1.2			V	I_{in} = -18mA	
Power Consumption						
82S23		80/400	115/605	mA/mW		
82S123		80/400	115/605	mA/mW		
Output Short Circuit Current	20		90	mA	V_{out}=OV	

NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is definec as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. For detailed conditions, see AC testing.
12. Connect an external 1k resistor from V_{CC} to the output terminal for this test.

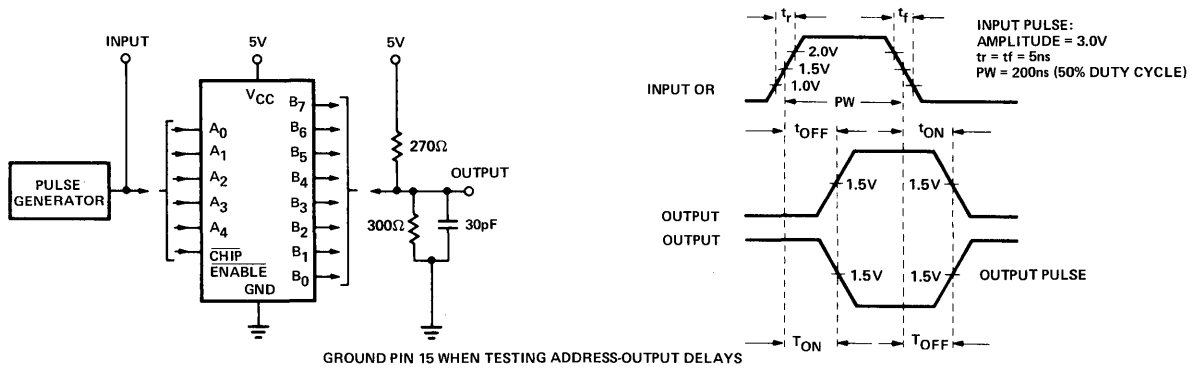
OBJECTIVE FUSING PROCEDURE

The 82S23/82S123 standard part is shipped with all outputs at Logical "0". To write a Logical "1" proceed as follows:
1. GND Pin 8 and apply 5V to V_{CC}, Pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground for a "0" and 5.0 ±0.25V for a "1" at the address input lines.
5. Raise V_{CC} to 10.0V ±0.5V.
6. Apply 65 ±3 mA to the output to be programmed to logic "1". (The voltage will be between 12 to 18V until fused, and must be clamped at 20.0V max.)
7. Release fusing current.
8. Reduce V_{CC} to 5.0V.
9. Proceed to the next output and repeat,or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 82S23/82S123.

NOTE:

After 1.0 SEC of programming, a 25% duty cycle on power must be imposed to avoid over heating.

AC TEST FIGURE AND WAVEFORMS



GROUND PIN 15 WHEN TESTING ADDRESS-OUTPUT DELAYS

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1024 BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S26
82S29

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S26 (open Collector Outputs) and the 82S29 (tri State Outputs) are Bipolar 1024 Bit Read Only Memories organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

The 82S26 and 82S29 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35ns.

The standard 82S26 and 82S29 are supplied with all outputs at a logical "0". If a programmed unit is required the Truth Table/Order Blank on page 4-44/45 can be used.

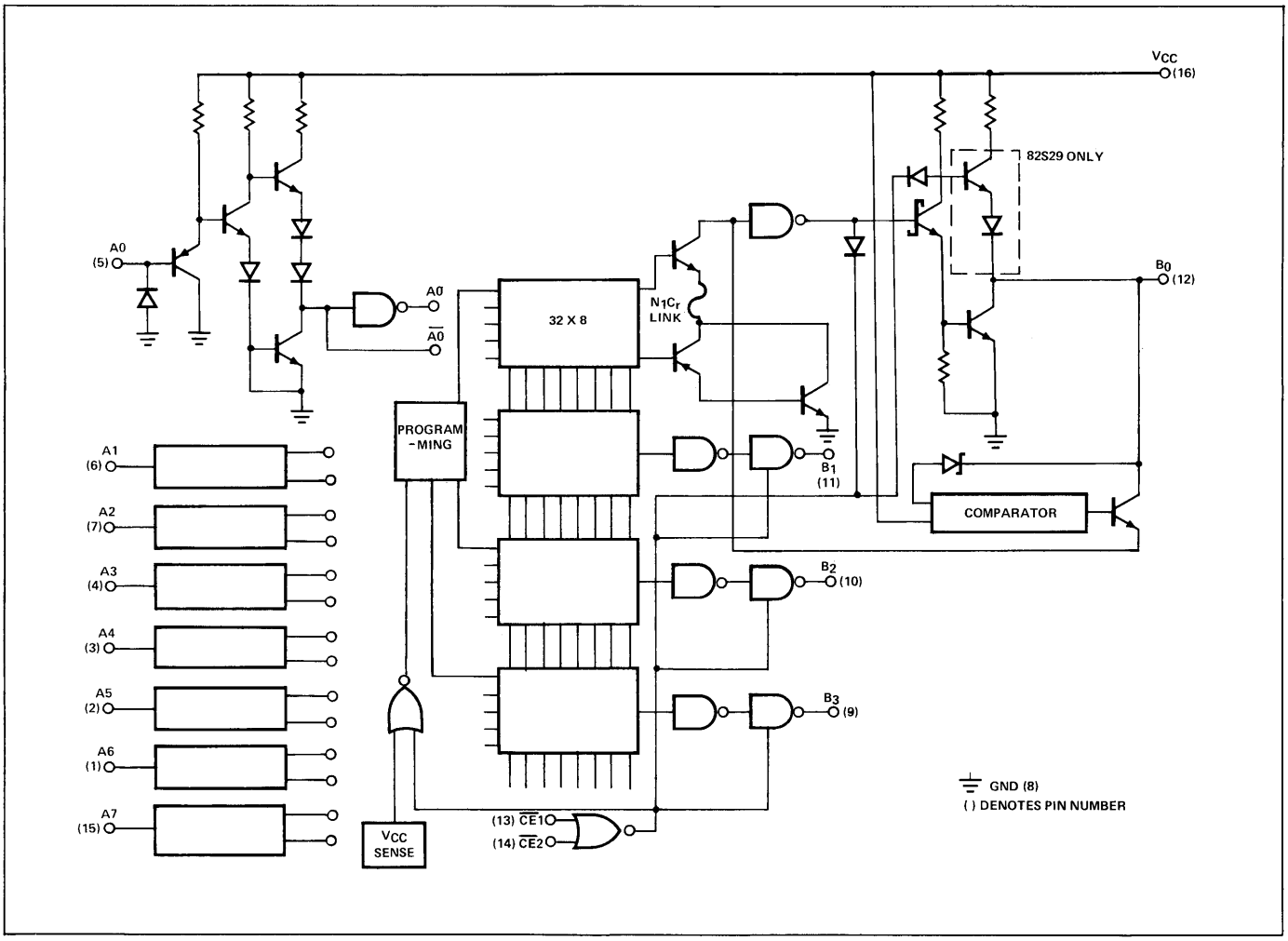
APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CONTROL STORE

FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TWO CHIP ENABLE LINES
- OPEN COLLECTOR OR TRI STATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- BOARD LEVEL PROGRAMMABLE

LOGIC DIAGRAM



PROGRAMMING

82S26 AND 82S29 PROGRAMMING PROCEDURE

1. Connect pin 8 (Grnd) to ground.

2. Disable the device by bringing $\overline{CE}_1$ and/or $\overline{CE}_2$ to a logical "1" (greater than 2.6 volts). If only one CE pin is used for the control of programming the other CE pin should be at logical "0" (0.4 volts or less).

3. Raise V_{CC} (pin 16) to 12.5 ±0.5 volts. (A 10μF in parallel with a 200pF high frequency capacitor should be connected between pins 16 and 8, as near the device as possible, to minimize noise on the V_{CC} line.)

4. Address the word to be programmed, using standard TTL logic levels. Apply 85 ±5mA into the output to be programmed to a logical "1". The output must be limited to 22 volts ±5% and only one output at a time should be programmed.

5. Wait until the current generator has reached the 22 volt clamp. (The current generator will be supplying about 50mA min.) Then drop both $\overline{CE}_1$ and $\overline{CE}_2$ to a logical "0" for 2.0msec. (fall time ≤50μsec).

6. Return $\overline{CE}_1$ and/or $\overline{CE}_2$ to a logical "1" for 10 microseconds.

7. Repeat steps 5, 6, and 7 until the entire word has been programmed. Change address and repeat steps 5, 6, and 7 until the entire device is programmed. At this point V_{CC} can be dropped to 5.0 volts and the chip enabled so that the outputs can be tested to verify that all bits programmed; if one or more bits have not programmed, return to the proper address and repeat steps 3 to 6 once for each unprogrammed bit.

NOTE: Do not apply the high V_{CC} (12.5 volts) for greater than 1.0 seconds continuously. At that point use a 20% duty cycle.

OPERATION OF THE 82S26/82S29 PROGRAMMER

INTRODUCTION

Figure 1 shows the complete programmer schematic. The memory to be programmed is inserted, and by means of seven single-pole, double-throw (SPDT) switches, the binary address is selected. Notice that these switches may easily be replaced by thumbwheel switches. The memory outputs are programmed, one at a time, by means of four double-pole, double-throw (DPDT) switches. This arrangement has the advantage that the switches are normally in the verify mode, indicating the state of the output (logic "0" when not programmed). By switching to the programming position, the outputs may be altered to a logic "1" which will turn on the light emmiting diode (LED) indicator. Upon return to the verify position the LED indicator will stay lit for a programmed bit position.

Once the switch is in the programming position, it may remain there as long as the operator wishes. The total programming cycle is set up to last only for 5ms and is controlled by one-shots as shown in the timing diagram, Fig. 2. The programmer timing follows the recommendation of the Signetics revised programming procedure and is easily adaptible to automatic programming and duplicating equipment.

CIRCUIT DESCRIPTION

Activating one of the four programming switches triggers one-shot No. 1 for 5 milliseconds. This activates gate No. 1 of the peripheral driver (75451) and, by releasing zener diode No. 1, V_{CC} is raised to 12.5V for 5 milliseconds while the 82S26 or 82S29 chip is disabled. (It should be mentioned that use of the 74121 eliminates contact bounce problems since it is non-retriggerable.)

After a time delay of 1 millisecond generated by one-shot No. 2, one-shot No. 3 is turned on. This turns off the output transistor of gate No. 2 of the 75451, enabling the programming current source. The constant current generator consists of LM309 No. 3 that is clamped to 22V by zener diode No. 2. The programming current is determined by the 59 ohm resistor and maintained at a constant 85mA.

An additional time delay of 1 millisecond, established by one-shot No. 4, guarantees that even slow current sources have reached the required current before the chip is enabled for 2ms to open the NiCr link. One-shot No. 5 establishes the chip enable ($\overline{CE}$) signal and thus the programming time.

Figure 2 shows that V_{CC} for the memory is held at 12.5V for an additional 1 millisecond before the output of one-shot No. 1 allows the supply to return to 5V.

The two time delays of 1 millisecond generated by one-shots No. 2 and No. 4 can be shortened to the microsecond range for automatic programming equipment if fast switching and a fast current source, as the one discussed above, are chosen. Should it be desired to make the programmer self-contained, a power supply suggestion is also shown in Figure 2.

PROGRAMMER

82S26-82S29

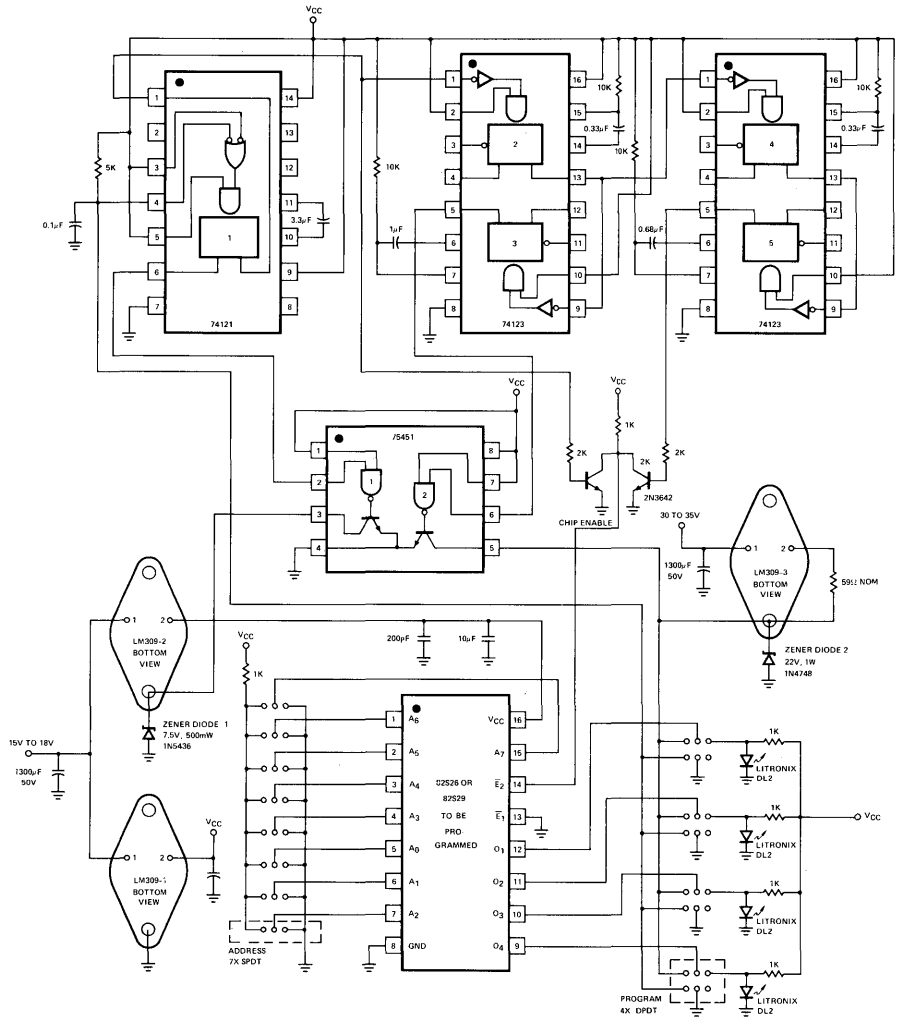


FIGURE 1

POWER SUPPLY AND WAVEFORMS

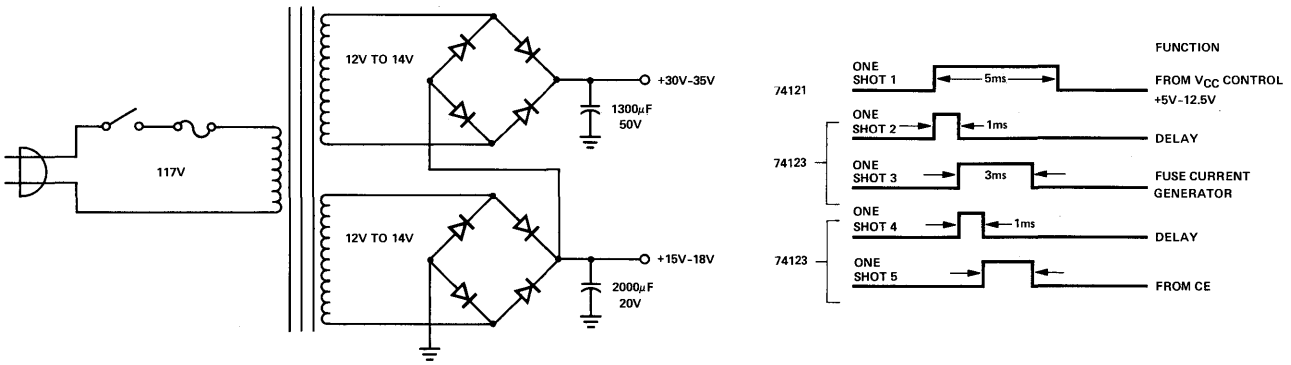


FIGURE 2

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25$

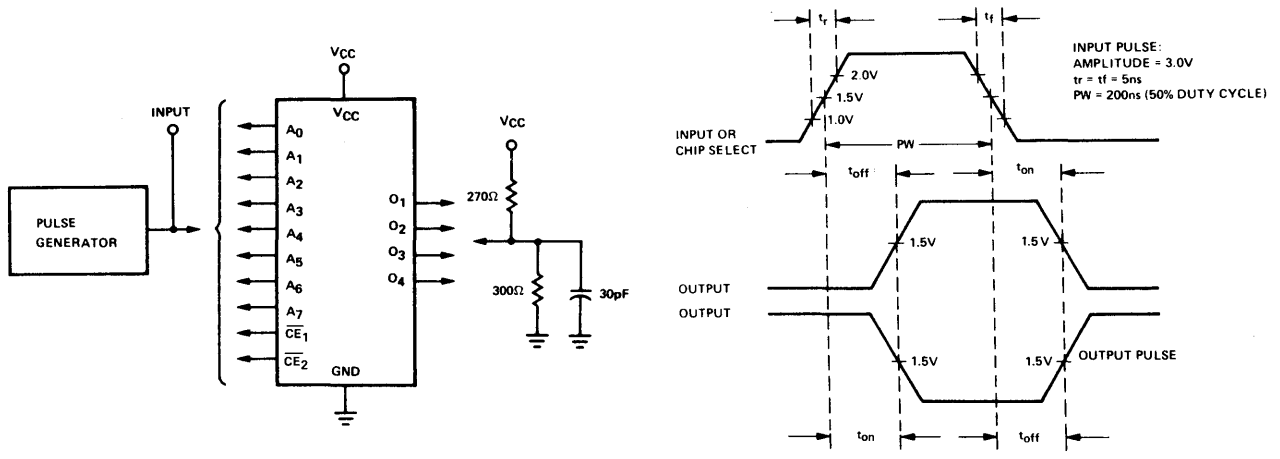
CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
"0" Output Voltage			0.5	V	I_{out} = 16mA
"1" Output Leakage (82S26)			40	μA	CE_1 or CE_2 = "1", V_{out} = 5.5V
(82S29)			100	μA	CE_1 = CE_2 = "0", V_{out} = 5.5V
(82S29)	-40		+40	μA	CE_1 or CE_2 = "1", V_{out} = .45 to 2.4V
"1" Output Current (82S29)	-2.0			mA	CE_1 = CE_2 = "0", V_{out} = 2.4V
"0" Input Current			-250	μA	V_{in} = 0.45V
"1" Input Current			50	μA	V_{in} = 5.5V
Input Threshold Voltage					
"0" Level	.85			V	
"1" Level			2.0	V	
Power Consumption (82S26)		105/525	130/685	mA/mW	
(82S29)		115/575	145/760	mA/mW	
Input Clamp Voltage	1.2			V	I_{in} = -18mA
Output Short Circuit Current	-20		-70	mA	V_{out} = 0 Volts

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Propagation Delay					
Address to Output			60	ns	T_A = 25°C only
			70	ns	
Chip Enable to Output			25	ns	T_A = 25°C only
			30	ns	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.

AC TEST FIGURE AND WAVEFORM



Ground Pins 13 and 14 when testing address-Output delays

signetics

ECL HIGH PERFORMANCE 256-PROM 10139

PRELIMINARY INFORMATION

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 10139 is an ECL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to low state when the chip enable input is high. This device is fully compatible with all of Signetics series 10,000 products. Address to output access time is 15 ns typical. Power dissipation is 580 milliwatts typical with separate internal bond wires and metal systems for V_{CC1} and V_{CC2}. The 10139 may be programmed to any desired pattern by the user. The 10139 is suitable for use in high performance ECL systems. A Truth Table/Order Blank is attached.

TEMPERATURE RANGE

–30 to +85°C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

V_{CC} = GND, V_{EE} = –5.2V ±5%

FEATURES

- 15 ns TYPICAL ACCESS TIME
- 16 PIN PACKAGE
- EASY PROGRAMMING
- FULLY DECODED
- FULLY COMPATIBLE WITH ECL 10,000 SERIES
- HIGH IMPEDANCE INPUTS 50K OHM PULLDOWN
- OPEN EMITTER OUTPUTS

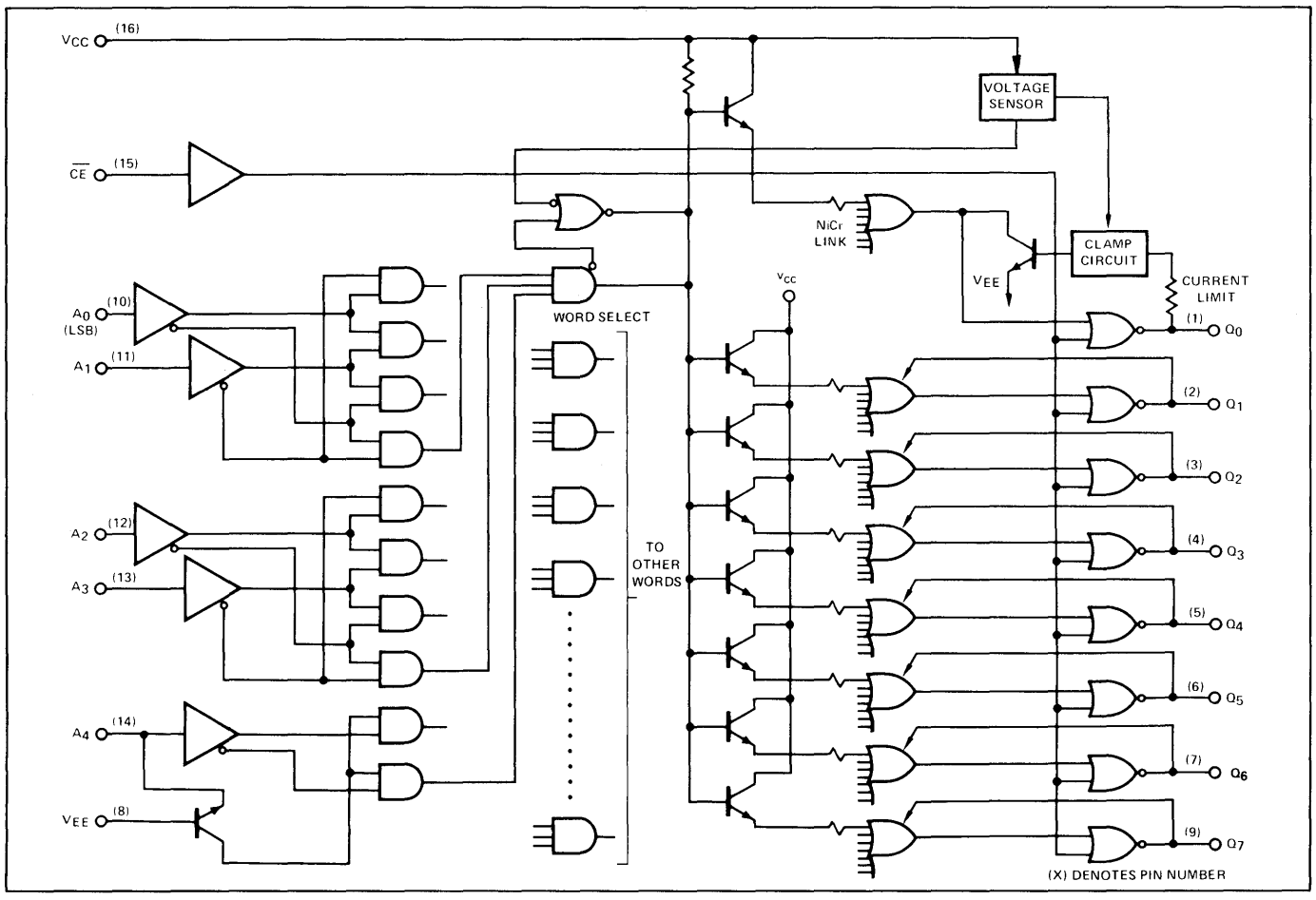
APPLICATIONS

PROGRAMMABLE LOGIC
CONTROL STORES
MICROPROGRAMMING
VOLUME PRODUCTION
HARDWIRED ALGORITHMS

PACKAGE TYPE

F: 16 Pin CERDIP

BLOCK DIAGRAM



PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, R_L = 50Ω, V_{EE} = −5.2V)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Drain Current	I_{EO}		110	145	mAdc
Input Current V_{IH} = −0.810V, V_{IL} = −1.850V	 I_{inH} I_{inL}	 30		265	 μAdc μAdc
Output Voltage Logic "1" (V_{IH} = −0.810V, V_{IL} = −1.850V)	V_{OH}	−0.960		−0.810	Vdc
Logic "0" (V_{IH} = −0.810V, V_{ILA} = 1.850V)	V_{OL}	−1.990		−1.650	Vdc
Threshold Voltage Logic "1" (V_{IHA} = −1.105V, V_{ILA} = −1.475V)	V_{OHA}	−0.980			Vdc
Logic "0" (V_{IHA} = −1.105V, V_{ILA} = 1.475V)	V_{OLA}			−1.630	Vdc

PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, V_{EE} = −5.2V, R_L = 50Ω)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable Prop Delay			10	15	ns
Output Rise Time (20 to 80%) Output Fall Time (20 to 80%)			4.2 4.2		ns ns
Access Time Address to Output	T_{AD}		15	20	ns

RECOMMENDED PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write logical "1's", proceed as follows:

MANUAL (see Fig. 1)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Address the word to be programmed by applying 4.0 to 4.6 volts for a logic "1" and 0.0 to 1.0 volts for a logic "0" to the appropriate address inputs.

STEP 2

Raise V_{CC} (Pin 16) to 12 volts.

STEP 3

After V_{CC} has stabilized at 12 volts (including any ringing which may be present on the V_{CC} line) apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

STEP 4

Return V_{CC} to 5.2 volts.

CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 volts for more than 1 second.

STEP 5

Verify that the selected bit has programmed by connecting a 460Ω resistor to ground and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once.

STEP 6

If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (see Fig. 2)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Apply the proper address data and raise V_{CC} (Pin 16) to 12 volts.

STEP 2

After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.5 \leqslant PW \leqslant 1$ ms).

STEP 3

Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time; The delay between output programming pulses should be equal to or less than 1.0 ms.)

STEP 4

After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at 12 volts during the entire programming time.

STEP 5

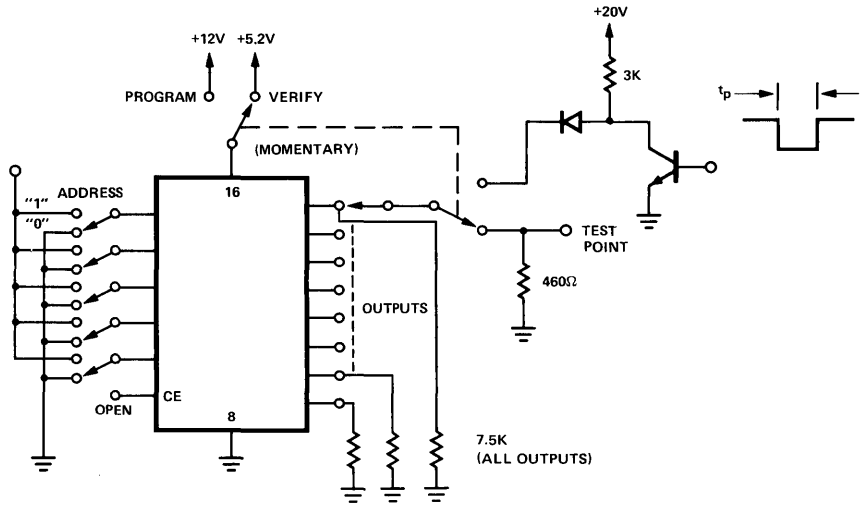
After stepping through all address words, return V_{CC} to +5.2 and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once.

PROGRAMMING SPECIFICATIONS

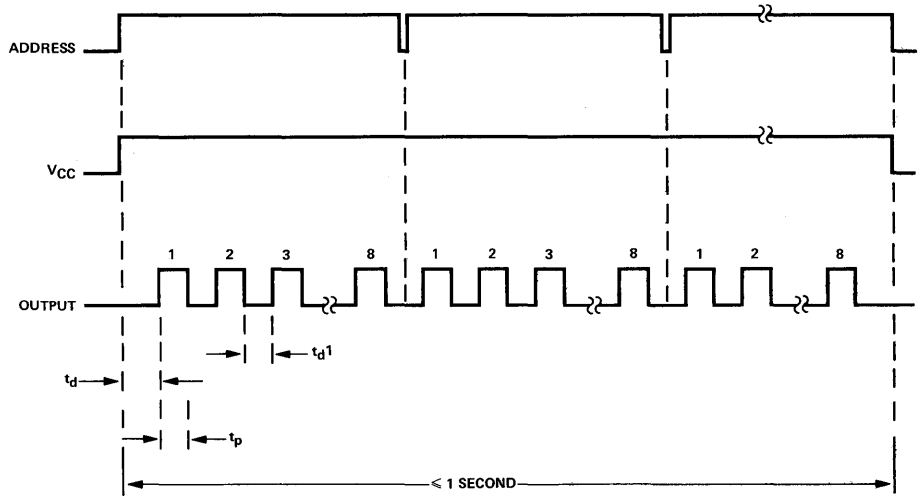
CHARACTERISTIC	SYMBOL	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
Power Supply Voltage To Program To Verify	 V_{CCP} V_{CCV}	 11.5 5.0	 12.0 5.2	 12.5 5.4	 Volts Volts	
Programming Supply Current	I_{CCP}			250	mA	V_{CC} = 12.0 Volts
Address Voltage logical "1" logical "0"	 V_{IH} V_{IL}	 4.0 0.0	 	 4.6 1.0	 Volts Volts	
Max. Time at $V_{CC} = V_{CCP}$				1.0	Sec.	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mA	
Output Program Pulse Width	t_p	0.5		1.0	ms	
Output Pulse Rise Time				10	μs	
Programming Pulse Delay (1) following V_{CC} change between output pulses	 t_d t_d1	 0.1 0.01	 	 1.0 1.0	 ms ms	

NOTE:
(1) Maximum is specified to minimize the amount of time V_{CC} is at 12 volts.

MANUAL PROGRAMMING CIRCUIT



AUTOMATIC PROGRAMMING CIRCUIT



signetics

ECL 64x1 RAMS | 10140 | 10148 | 10151

-30 to +85°C CERDIP

ADVANCED INFORMATION

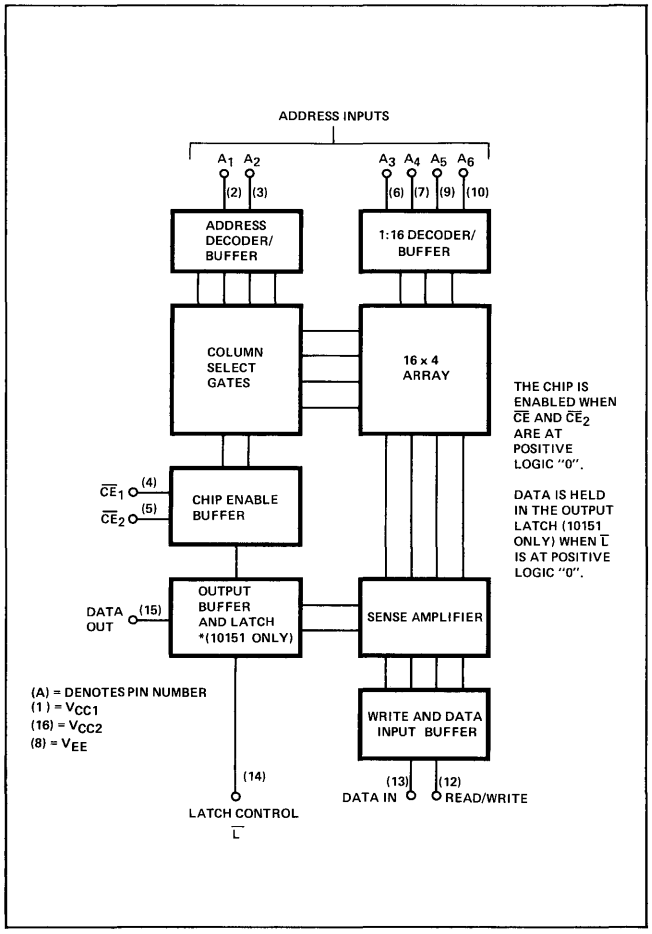
DIGITAL 10,000 ECL SERIES

DESCRIPTION

The 10140, 10148 and 10151 are 64 Bit ECL Random Access Memories (RAM's) organized as 64 words with 1 bit per word. The words are selected by six binary address lines; full word decoding is incorporated on the chip. Two chip enable input lines are provided for additional decoding flexibility. The chip is disabled when either chip enables are high, which causes the output of the 10140 and 10148 to go low.

The 10151 has an internal latch on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$ is a "1" and data is being read from the 10151 the latch is effectively bypassed. The data at the output will be that of the addressed word. When I goes from a logic "1" to logic "O" the outputs are latched and will remain latched regardless of the state of any other address or control line. When L goes from "O" to "1" the outputs unlatch and will take the state of the addressed word. The 10151 and 10148 logic levels are fully compatible with the 10,000 series and are specified for driving a 50Ω load. The 10140 is compatible with series 10,000 ECL except the output is specified for driving a 90Ω load.

LOGIC DIAGRAM



FEATURES

- 10 ns TYPICAL ACCESS TIME
- 16 PIN PACKAGE
- ON THE CHIP LATCH (AVAILABLE ON 10151)
- ON THE CHIP DECODING
- TWO CHIP ENABLE CONTROL LINES
- HIGH IMPEDANCE INPUTS 50k OHM PULL-DOWN
- OPEN EMITTER OUTPUTS

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

TRUTH TABLE (10151)

$\overline{CE}$	$\overline{RW}$	$\overline{L}$	MODE	OUTPUTS
0	0	0	Write Data	
0	0	1	Write Data	
0	1	0	Read	Data stored in addressed word
0	1	1	Read	Data stored in addressed word
1	0	0	Chip Disabled	Data from last address when CE = "0"
1	0	1	Chip Disabled	Logical "1"
1	1	0	Chip Disabled	Data from last address when CE = "0"
1	1	1	Chip Disabled	Logical "1"

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	40	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Operating Junction Temperature	T_J	110	°C
Operating Temperature Range	T_A	-30 to +85	°C
Power Supply Regulation Required	—	±10% ±5%	—

$V_{CC1} = V_{CC2} = Gnd$

SWITCHING CHARACTERISTICS T_A = 25°C, R_L = 50Ω for 10148 and 10151, R_L = 90Ω for 10140

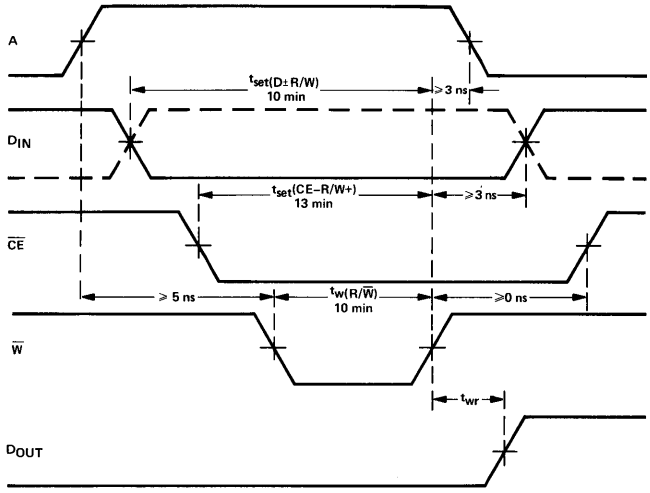
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable					
Turn-On	t_{CE-D+}	—	8	12	ns
Turn-Off	t_{CE+D-}	—	8	12	
Access Time for Address to Output					
	t_{A+D+}	—	10	15	ns
	t_{A+D-}	—	10	15	
	t_{A-D+}	—	10	15	
	t_{A-D-}	—	10	15	
Write Pulse Width	$t_{w(R/W)}$	10			ns
Chip Enable Pulse Width	$t_{w(CE)}$	13			ns
Set-Up Time for Data to Write	$t_{set(D±R/W+)}$	10			ns
Set-Up Time for Data to Chip Enable	$t_{set(D±CE+)}$	10			ns
Set-Up Time for Write to Chip Enable	$t_{set(W-CE+)}$	10			ns
Set-Up Time for Chip Enable to Write	$t_{set(CE-R/W+)}$	13			ns
Set-Up Time for Data to Latch (10151 only)	$t_{set(D±I-)}$				ns
Set-Up Time for Latch Release to Data (10151 only)	$t_{set(I+D±)}$				ns
Set-Up Time for Latch to Address (10151 only)	$t_{set(I-A±)}$				ns

ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 50Ω for 10148 and 10151, RL = 90Ω for 10140

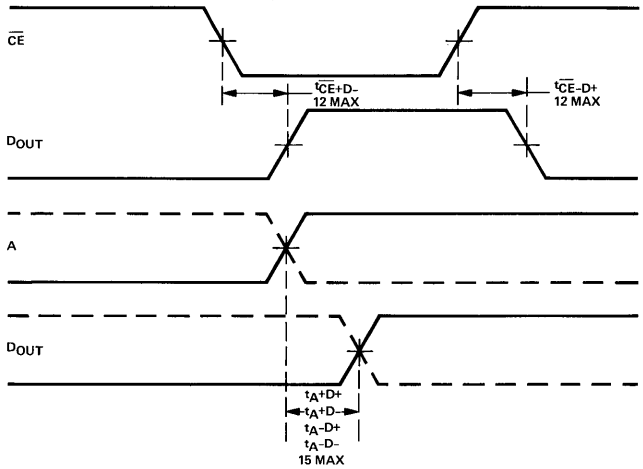
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Drain Current (V_{EE} = -5.2 V)	I_{EO}	—	80	—	mAdc
Input Current					μAdc
(V_{IH} = -0.810 V, V_{EE} = -5.2 V)	I_{inH}	—	—	265	
(V_{IL} = -1.850 V, V_{EE} = -5.2 V)	I_{inL}	0.5	—	—	
Output Voltage					
Logic "1" (V_{IH} = -0.810 V, V_{IL} = -1.850 V, V_{EE} = -5.2 V)	V_{OH}	-0.960	—	-0.810	Vdc
Logic "0" (V_{IH} = -0.810 V, V_{IL} = -1.850 V, V_{EE} = -5.2 V)	V_{OL}	-1.990	—	-1.650	Vdc
Threshold Voltage					
Logic "1" (V_{IHA} = -1.105 V, V_{ILA} = -1.475 V, V_{EE} = -5.2 V)	V_{QHA}	-0.980	—	—	Vdc
Logic "0" (V_{IHA} = -1.105 V, V_{ILA} = -1.475 V, V_{EE} = -5.2 V)	V_{OLA}	—	—	-1.630	Vdc

TIMING DIAGRAMS

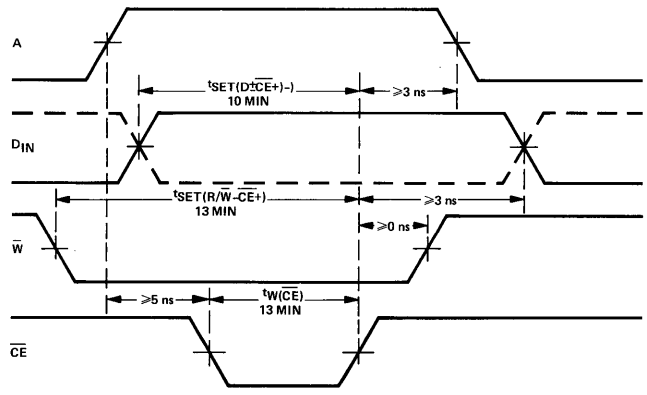
WRITE TIMING DIAGRAMS—WRITE STROBE MODE



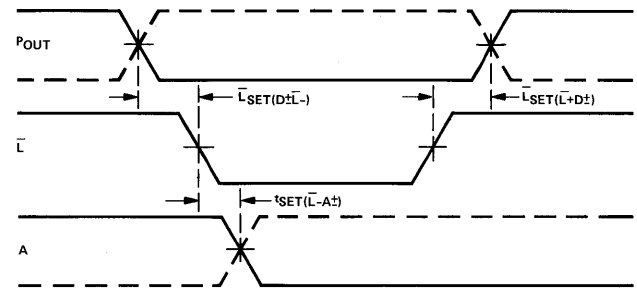
READ TIMING DIAGRAM



CHIP ENABLE STROBE MODE



10151 LATCH TIMING DIAGRAM



DESCRIPTION

The 10145 is an ECL 64-bit read-write random access memory organized as 16 words of 4 bits each. Words are selected through fully decoded and buffered inputs when the chip enable ($\overline{CE}$) is low. Data is written into the selected word by bringing the READ/$\overline{WRITE}$ input low. Outputs are low during write.

On-chip input pulldown resistors allow any unused inputs to be left open. Open emitter outputs allow corresponding bits of different devices to be tied together to form a "Wire OR" logic connection.

The 10145 utilizes separate internal metal systems and wire bonds for V_{CC1} and V_{CC2}. The exceptionally high speed of the 10145 makes it particularly suited for register file and and scratch pad applications.

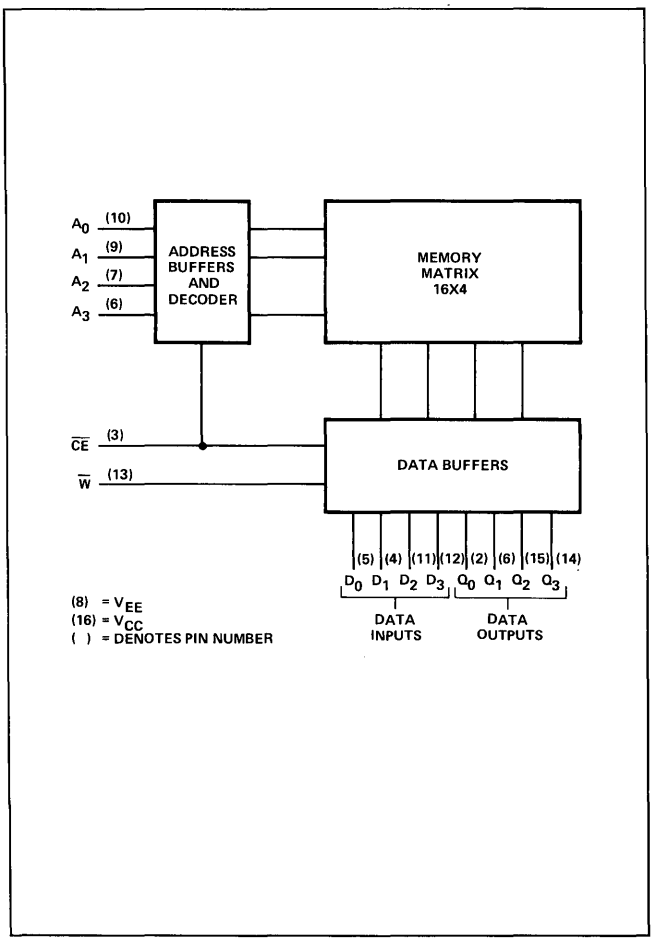
FEATURES

- 8.5ns ADDRESS ACCESS TIME (TYP)
- INPUT PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS AND CHIP ENABLE INPUT FOR MEMORY EXPANSION
- 50 Ohm OUTPUT SPECIFICATION
- SINGLE -5.2V POWER SUPPLY
- FULLY DECODED INPUTS
- FULLY COMPATIBLE WITH SIGNETICS 10,000 SERIES FAMILY OF INTEGRATED CIRCUITS

APPLICATIONS

SCRATCH PAD MEMORIES
BUFFER MEMORIES
REGISTER FILES
CONTROL STORES

BLOCK DIAGRAM



PACKAGE TYPES

F: 16 Pin Cerdip
I: 16 Pin Laminated Ceramic

ELECTRICAL CHARACTERISTICS V_{EE} = -5.2V, V_{CC} = 0V, R_L = 50Ω TO -2.0V

CHARACTERISTIC	SYMBOL	CONDITIONS	TEMP.	MIN.	TYP.	MAX.	UNITS
Supply Current	I_E		25°C		116	145	mA
Input Current (Pins 3, 6, 7, 9, 10)	I_{INH}	$V_{IN} = V_{IH}$ MAX.	25°C			200	μA
Input Current (Pins 4, 5, 11, 12)	I_{INH}	$V_{IN} = V_{IH}$ MAX.	25°C			220	μA
Input Current (Pin 13)	I_{INH}	$V_{IN} = V_{IH}$ MAX.	25°C			455	μA
Input Current (All Inputs)	I_{INL}	$V_{IN} = V_{IL}$ MIN.	25°C	0.5			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	SYMBOL	CONDITIONS	TEMP.	MIN.	TYP.	MAX.	UNITS
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.06 -.96 -.89		-.89 -.81 -.70	Vdc
Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.89 -1.85 -1.825		-1.675 -1.65 -1.615	Vdc
Output Voltage (Threshold)	V_{OHA}	$V_{IN} = V_{IHA}$, V_{ILA}	-30°C 25°C 85°C	-1.08 -.98 -.91			Vdc
Output Voltage (Threshold)	V_{OLA}	$V_{IN} = V_{IHA}$, V_{ILA}	-30°C 25°C 85°C			-1.655 -1.63 -1.595	Vdc

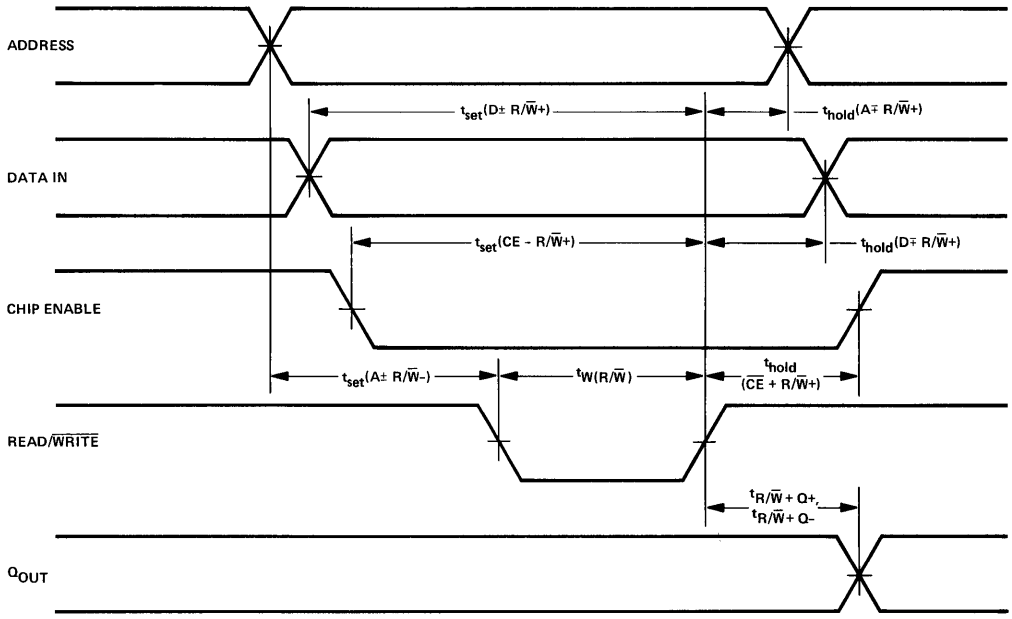
SWITCHING CHARACTERISTICS V_{EE} = -3.2V, V_{CC} = 2V, R_L = 50Ω TO GND

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Access Time — Chip Enable to Output Address to Output	$^tC\overline{E}$ - Q+, $^tC\overline{E}$ + Q- ^tA + Q+, ^tA - Q+ ^tA+ Q-, ^tA - Q -		5.0 8.5		ns ns
Write Strobe Mode					
Data Set-up	$^tSET(D\pm R/\overline{W}+)$		7.5		ns
Chip Enable Set-up	$^tSET(CE- R/\overline{W}+)$		11.0		ns
Address	$^tSET(A\pm R/\overline{W}-)$		3.5		ns
Data Hold	$^tHOLD(D\mp R/\overline{W}+)$		3.0		ns
Chip Enable Hold	$^tHOLD(\overline{CE}+ R/\overline{W}+)$		3.0		ns
Address Hold	$^tHOLD(A\mp R/\overline{W}+)$		3.5		ns
Recovery Time	$^tR/\overline{W}+$ Q+, $^tR/\overline{W}+$ Q-		7.5		ns
Write Pulse Width	$^tW(R/\overline{W})$		7.5		ns
Chip Enable Strobe Mode					
Data Set-up	$^tSET(D\pm \overline{CE}+)$		7.5		ns
Read/$\overline{\text{Write}}$ Set-up	$^tSET(R/\overline{W}- \overline{CE}+)$		11.0		ns
Address Set-up	$^tSET(A\pm\overline{CE}-)$		3.0		ns
Data Hold	$^tHOLD(D\mp\overline{CE}+)$		3.0		ns
Read/$\overline{\text{Write}}$ Hold	$^tHOLD(R/\overline{W} + \overline{CE}+)$		3.0		ns
Address Hold	$^tHOLD(A\mp CE+)$		3.0		ns
Chip Enable Pulse Width	$^tW(\overline{CE})$		7.5		ns
Rise Time (20%-80%)	t_+		2.5		ns
Fall Time (20%-80%)	t_-		2.5		ns

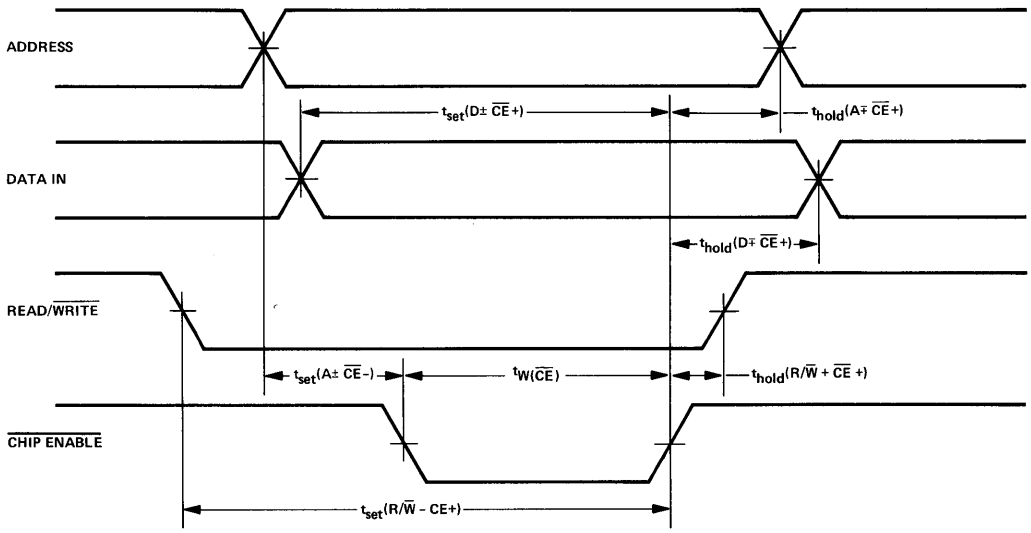
TEST VOLTAGE VALUES Vdc ± 1%					
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

TIMING DIAGRAMS

WRITE CYCLE
READ/WRITE STROBE MODE

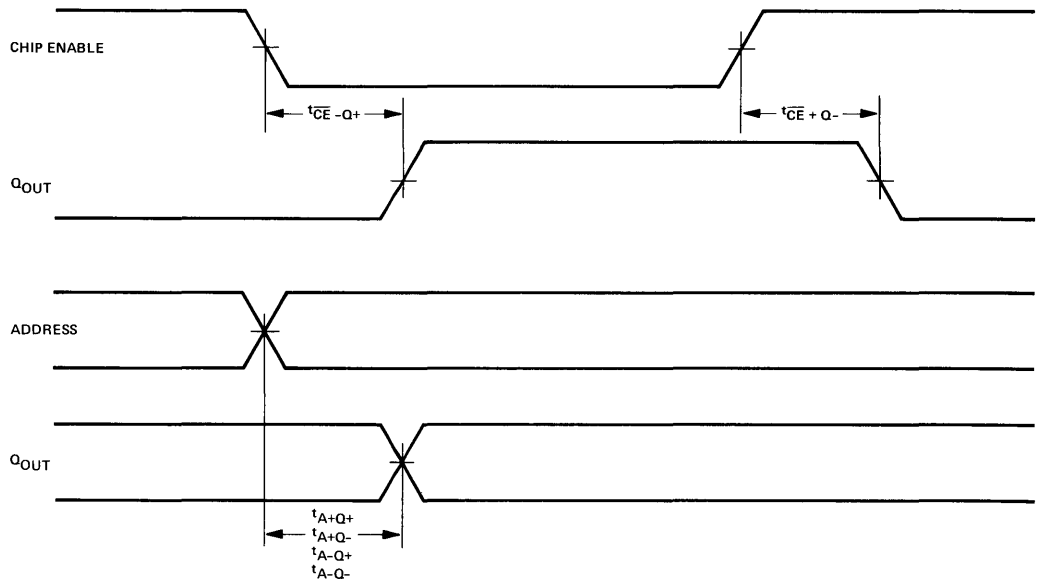


WRITE CYCLE
CHIP ENABLE STROBE MODE

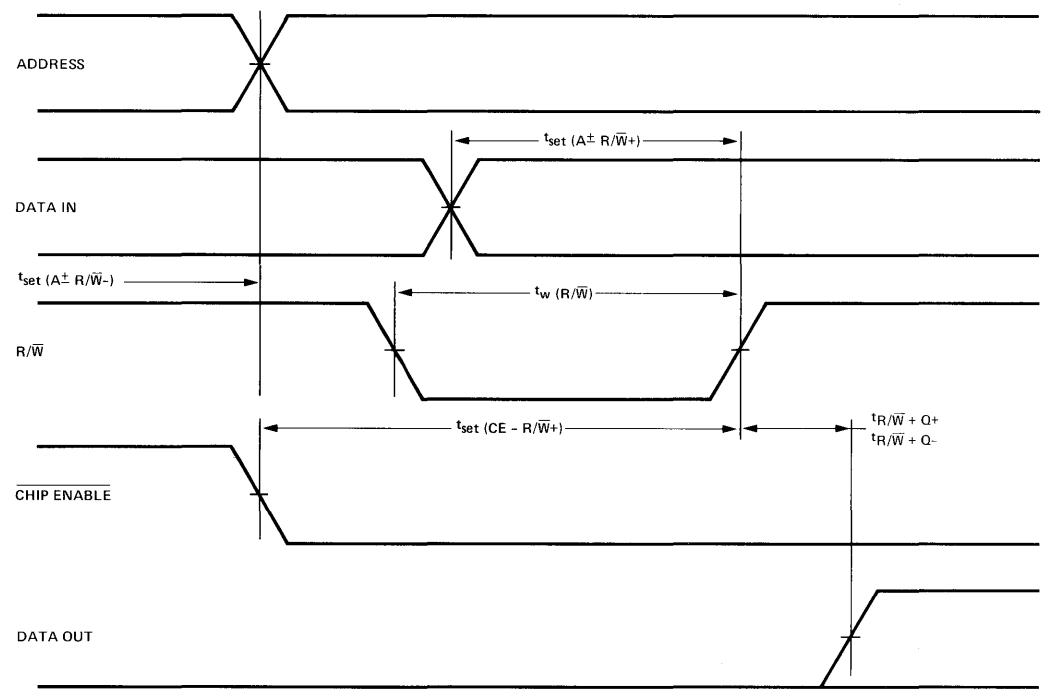


TIMING DIAGRAMS (Cont'd)

READ CYCLE



WRITE/READ CYCLE



CUSTOMER ORDERING INFORMATION

N8205 - CB175 ASCII-TO-EBCDIC, EBCDIC-TO-ASCII
N8204 - CB504 ASCII-TO-EBCDIC CODE CONVERTER
N8204 - CB505 EBCDIC-TO-ASCII CODE CONVERTER

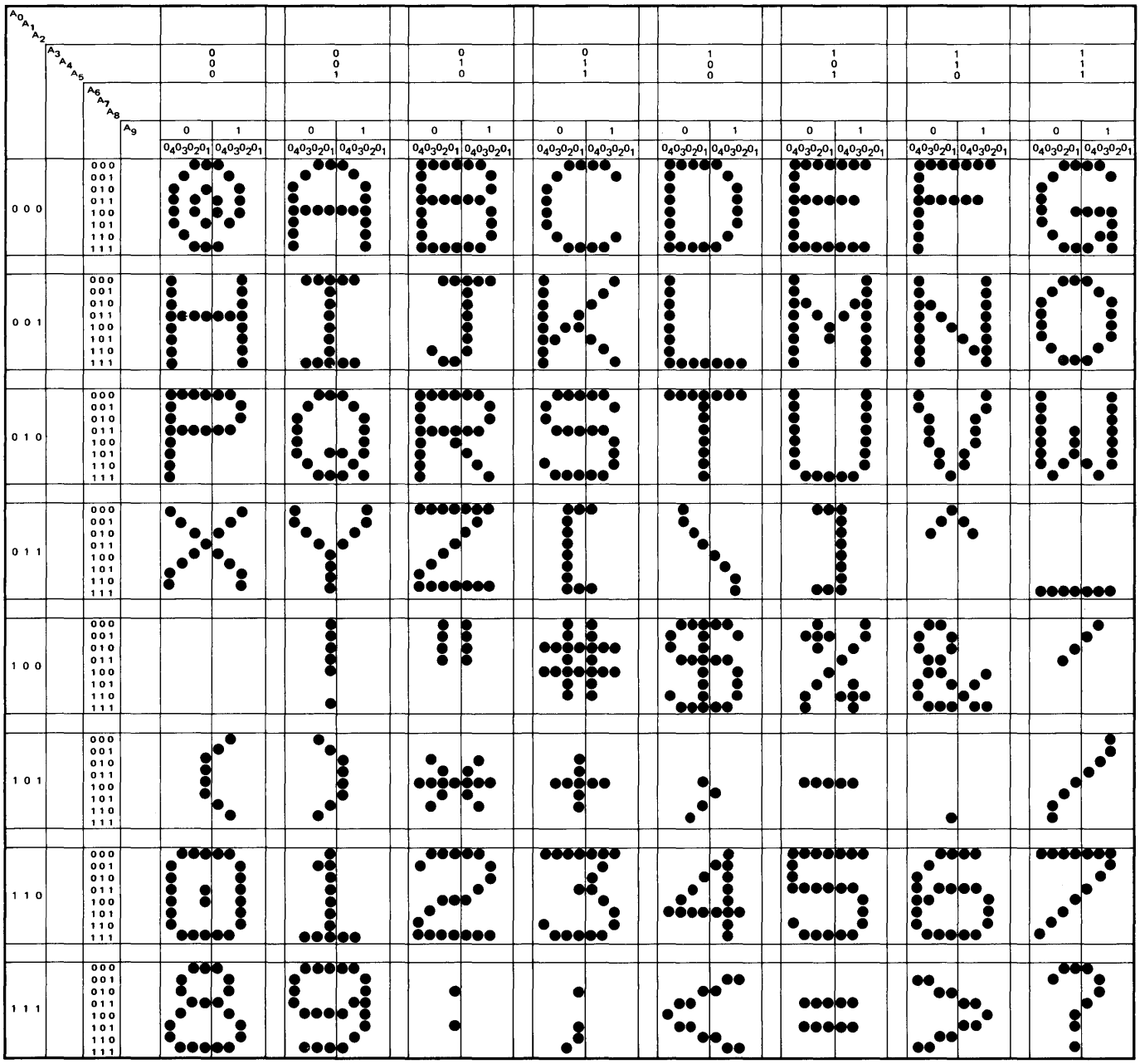
ASCII (ADDRESS) TO EBCDIC (DATA) 8205 — CB175 FIRST HALF 8204 — CB504

0 00000000	1 00000001	2 00000010	3 00000011	128 00100000	129 00100001	130 00100010	131 00100011
4 00110111	5 00101101	6 00101110	7 00101111	132 00100100	133 00010101	134 00000110	135 00010111
8 00010110	9 00000101	10 00100101	11 00001011	136 00101000	137 00101001	138 00101010	139 00101011
12 00001100	13 00001101	14 00001110	15 00001111	140 00101100	141 00001001	142 00001010	143 00011011
16 00010000	17 00010001	18 00010010	19 00010011	144 00110000	145 00110001	146 00011010	147 00110011
20 00111100	21 00111101	22 00110010	23 00100110	148 00110100	149 00110101	150 00110110	151 00001000
24 00011000	25 00011001	26 00111111	27 00100111	152 00111000	153 00111001	154 00111010	155 00111011
28 00011100	29 00011101	30 00011110	31 00011111	156 00000100	157 00010100	158 00111110	159 11100001
32 01000000	33 01001111	34 01111111	35 01111011	160 01000001	161 01000010	162 01000011	163 01000100
36 01011011	37 01101100	38 01010000	39 01111101	164 01000101	165 01000110	166 01000111	167 01001000
40 01001101	41 01011101	42 01011100	43 01001110	168 01001001	169 01010001	170 01010010	171 01010011
44 01101011	45 01100000	46 01001011	47 01100001	172 01010100	173 01010101	174 01010110	175 01010111
48 11110000	49 11110001	50 11110010	51 11110011	176 01011000	177 01011001	178 01100010	179 01100011
52 11110100	53 11110101	54 11110110	55 11110111	180 01100100	181 01100101	182 01100110	183 01100111
56 11111000	57 11111001	58 01111010	59 01011110	184 01101000	185 01101001	186 01110000	187 01110001
60 01001100	61 01111110	62 01101110	63 01101111	188 01110010	189 01110011	190 01110100	191 01110101
64 01111100	65 11000001	66 11000010	67 11000011	192 01110110	193 01110111	194 01111000	195 10000000
68 11000100	69 11000101	70 11000110	71 11000111	196 10001010	197 10001011	198 10001100	199 10001101
72 11001000	73 11001001	74 11010001	75 11010010	200 10001110	201 10001111	202 10010000	203 10011010
76 11010011	77 11010100	78 11010101	79 11010110	204 10011011	205 10011100	206 10011101	207 10011110
80 11010111	81 11011000	82 11011001	83 11100010	208 10011111	209 10100000	210 10101010	211 10101011
84 11100011	85 11100100	86 11100101	87 11100110	212 10101100	213 10101101	214 10101110	215 10101111
88 11100111	89 11101000	90 11101001	91 01001010	216 10110000	217 10110001	218 10110010	219 10110011
92 11100000	93 01011010	94 01011111	95 01101101	220 10110100	221 10110101	222 10110110	223 10110111
96 01111001	97 10000001	98 10000010	99 10000011	224 10111000	225 10111001	226 10111010	227 10111011
100 10000100	101 10000101	102 10000110	103 10000111	228 10111100	229 10111101	230 10111110	231 10111111
104 10001000	105 10001001	106 10010001	107 10010010	232 11001010	233 11001011	234 11001100	235 11001101
108 10010011	109 10010100	110 10010101	111 10010110	236 11001110	237 11001111	238 11011010	239 11011011
112 10010111	113 10011000	114 10011001	115 10100010	240 11011100	241 11011101	242 11011110	243 11011111
116 10100011	117 10100100	118 10100101	119 10100110	244 11101010	245 11101011	246 11101100	247 11101101
120 10100111	121 10101000	122 10101001	123 11000000	248 11101110	249 11101111	250 11111010	251 11111011
124 01101010	125 11010000	126 10100001	127 00000111	252 11111100	253 11111101	254 11111110	255 11111111

EBCDIC (ADDRESS) TO ASCII (DATA) 8205 — CB175 SECOND HALF 8204 — CB505

256 00000000	257 00000001	258 00000010	259 00000011	384 11000011	385 01100001	386 01100010	387 01100011
260 10011100	261 00001001	262 10000110	263 01111111	388 01100100	389 01100101	390 01100110	391 01100111
264 10010111	265 10001101	266 10001110	267 00001011	392 01101000	393 01101001	394 11000100	395 11000101
268 00001100	269 00001101	270 00001110	271 00001111	396 11000110	397 11000111	398 11001000	399 11001001
272 00010000	273 00010001	274 00010010	275 00010011	400 11001010	401 11001010	402 01101011	403 01101100
276 10011101	277 10000101	278 00001000	279 10000111	404 01101101	405 01101110	406 01101111	407 01110000
280 00011000	281 00011001	282 10010010	283 10001111	408 01110001	409 01110010	410 11001011	411 11001100
284 00011100	285 00011101	286 00011110	287 00011111	412 11001101	413 11001110	414 11001111	415 11010000
288 10000000	289 10000001	290 10000010	291 10000011	416 11010001	417 01111110	418 01110011	419 01110100
292 10000100	293 00001010	294 00010111	295 00011011	420 01110101	421 01110110	422 01110111	423 01111000
296 10001000	297 10001001	298 10001010	299 10001011	424 01111001	425 01111010	426 11010010	427 11010011
300 10001100	301 00000101	302 00000110	303 00000111	428 11010100	429 11010101	430 11010110	431 11010111
304 10010000	305 10010001	306 00010110	307 10010011	432 11011000	433 11011001	434 11011010	435 11011011
308 10010100	309 10010101	310 10010110	311 00000100	436 11011100	437 11011101	438 11011110	439 11011111
312 10011000	313 10011001	314 10011010	315 10011011	440 11100000	441 11100001	442 11100010	443 11100011
316 00010100	317 00010101	318 10011110	319 00011010	444 11100100	445 11100101	446 11100110	447 11100111
320 00100000	321 10100000	322 10100001	323 10100010	448 01111011	449 01000001	450 01000010	451 01000011
324 10100011	325 10100100	326 10100101	327 10100110	452 01000100	453 01000101	454 01000110	455 01000111
328 10100111	329 10101000	330 01011011	331 00101110	456 01001000	457 01001001	458 11101000	459 11101001
332 00111100	333 00101000	334 00101011	335 00100001	460 11101010	461 11101011	462 11101100	463 11101101
336 00100110	337 10101001	338 10101010	339 10101011	464 01111101	465 01001010	466 01001011	467 01001100
340 10101100	341 10101101	342 10101110	343 10101111	468 01001101	469 01001110	470 01001111	471 01010000
344 10110000	345 10110001	346 01011101	347 00100100	472 01010001	473 01010010	474 11101110	475 11101111
348 00101010	349 00101001	350 00111011	351 01011110	476 11110000	477 11110001	478 11110010	479 11110011
352 00101101	353 00101111	354 10110010	355 10110011	480 01011100	481 10011111	482 01010011	483 01010100
356 10110100	357 10110101	358 10110110	359 10110111	484 01010101	485 01010110	486 01010111	487 01011000
360 10111000	361 10111001	362 01111100	363 00101100	488 01011001	489 01011010	490 11110100	491 11110101
364 00100101	365 01011111	366 00111110	367 00111111	492 11110110	493 11110111	494 11111000	495 11111001
368 10111010	369 10111011	370 10111100	371 10111101	496 00110000	497 00110001	498 00110010	499 00110011
372 10111110	373 10111111	374 11000000	375 11000001	500 00110100	501 00110101	502 00110110	503 00110111
376 11000010	377 01100000	378 00111010	379 00100011	504 00111000	505 00111001	506 11111010	507 11111011
380 01000000	381 00100111	382 00111101	383 00100010	508 11111100	509 11111101	510 11111110	511 11111111

N82281 – CB 162 PATTERN
USASC II ROW CHARACTER GENERATOR



PUNCHED CARD PROGRAM INPUT FOR 8204 & 8205

The customer may specify the content of the ROM either by filling out the accompanying form or by using punched cards. He should note that:

1. "Zero" levels on data out lines are defined as low.
2. Address bit A_0 is the least significant address bit. (See 8204 and 8205 data sheet)

Punched Card Data Input - Data to program the 8205 and the 8204 can be supplied in punched card-format. The format for the data is shown in Figure 1. Each data word is preceded by an address word which identifies its position in memory. Figure 2 shows the deck format for the 8204 256 x 8 bit ROM. For the 8204 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. The 64 customer data cards follow immediately. Figure 3 shows the deck format for the 8205 512 x 8 ROM. For the 8205 the first card in the deck contains the part number and it is immediately followed by up to 40 alphanumeric characters of customer supplied information used to identify the part. 128 data cards follow immediately. The left-most digit in the data word corresponds to output O_8 and the right-most digit to output O_1.

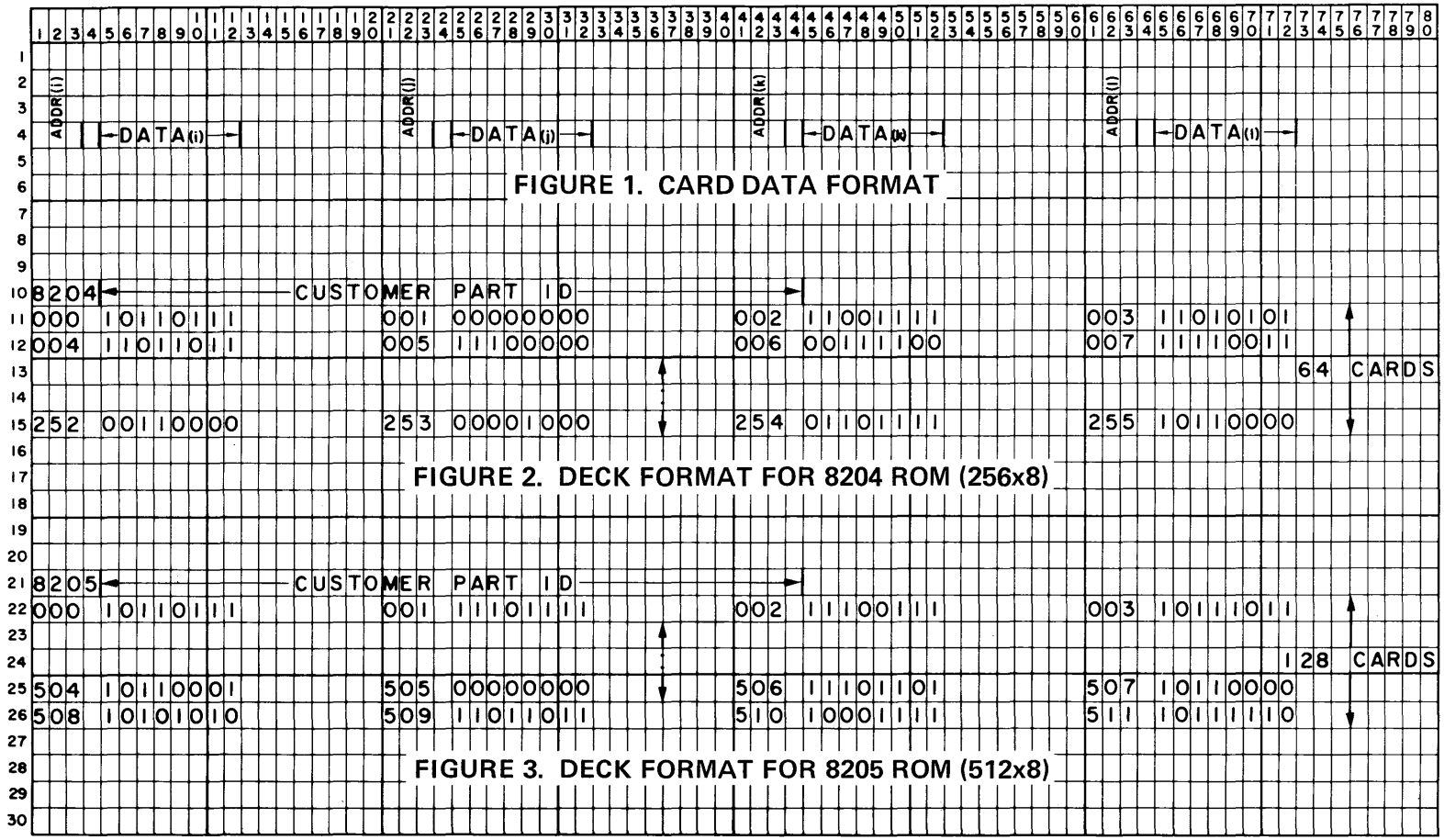


FIGURE 1. CARD DATA FORMAT

FIGURE 2. DECK FORMAT FOR 8204 ROM (256x8)

FIGURE 3. DECK FORMAT FOR 8205 ROM (512x8)

Punched card data to program can be transmitted directly to Signetics. Data information to program the ROM requires 128 80-column IBM punched cards per 4096 bit device and 64 punched cards per 256 bit device.

Input Deck Format

For each 4096 bit ROM, the customer should prepare an input card deck as shown in Figure 1. The first two cards should be punched as shown and placed at the start of the deck. The third card should contain "8228" in the first four columns. In the next 40 positions, the customer should fill in his own part identification. These first three cards are then followed by 128 data cards. Immediately following are two cards to terminate the computer run. These should be punched by the customer.

Data Cards

Figure 2 shows the layout used in the data cards. Each data card specifies eight addresses and the four bits of data associated with these addresses. Address (i) tells the computer what position to assign Data (i) to etc. Immediately under this, a typical layout for the first two and the last data cards is shown.

INPUT CARD

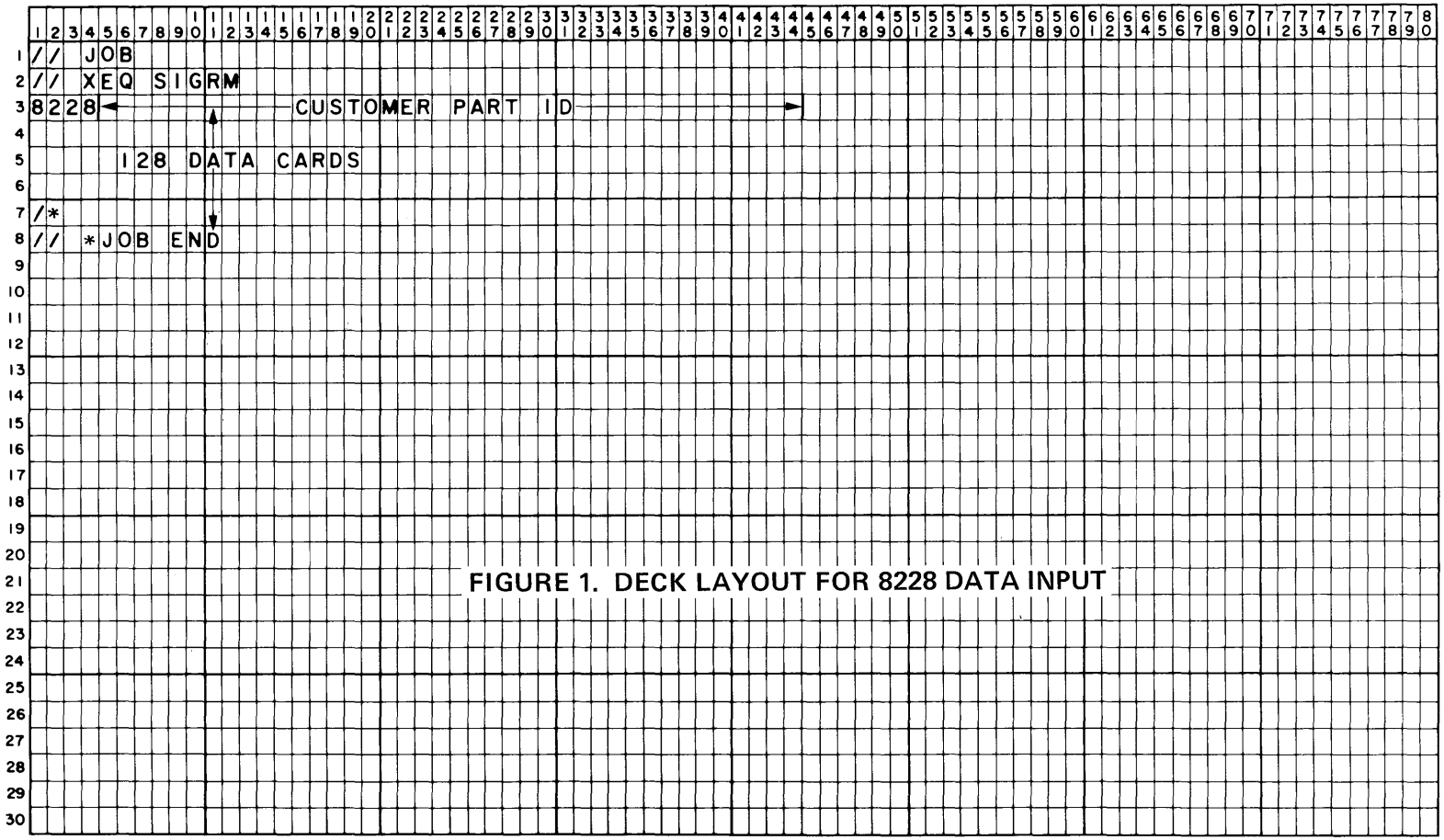


FIGURE 1. DECK LAYOUT FOR 8228 DATA INPUT

DATA CARDS

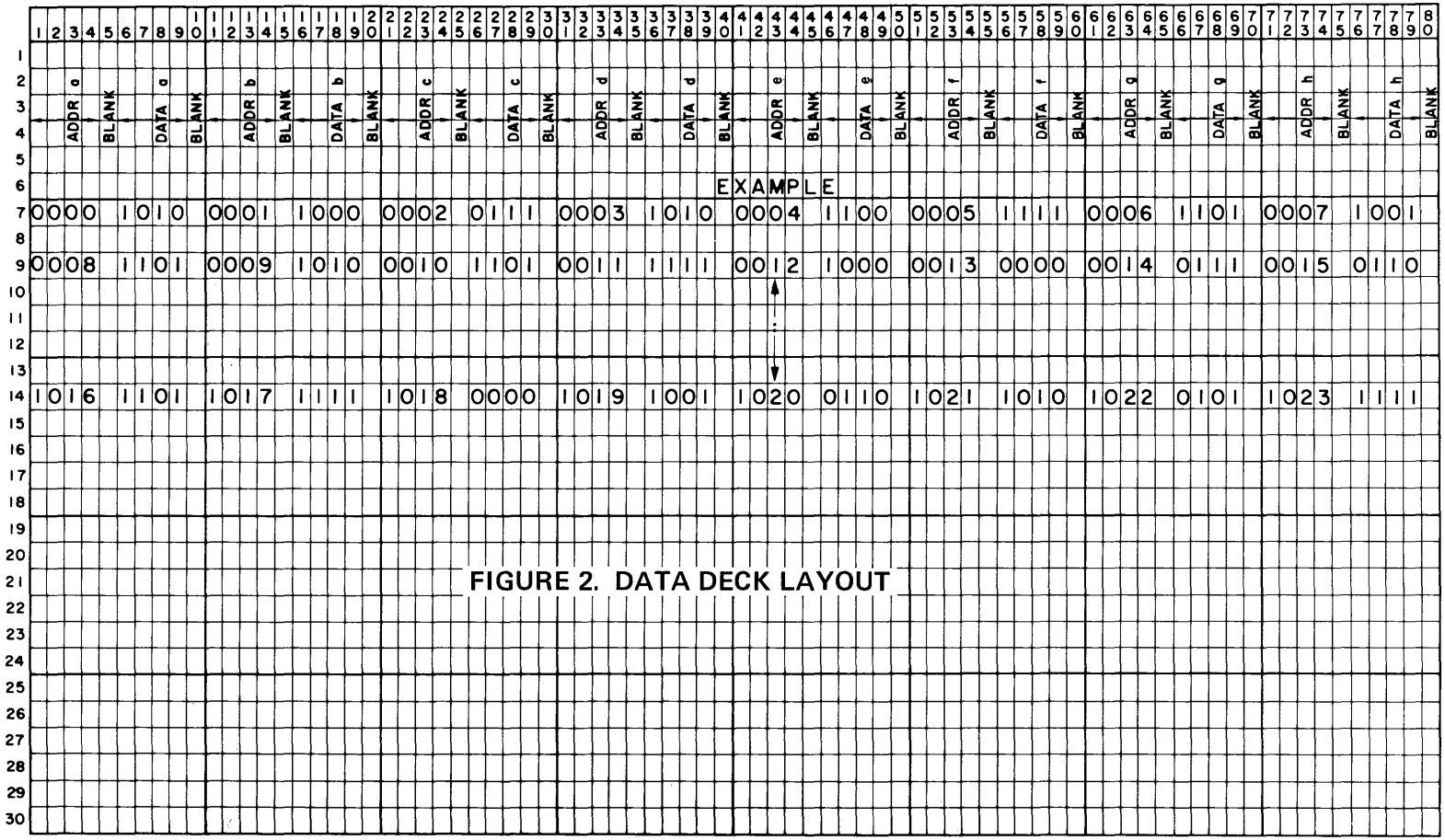


FIGURE 2. DATA DECK LAYOUT

(8204,8205)

2048/4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Note: For 256 x 8 Use This Page Only

Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	Word	OUTPUT O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0									64									128									192								
1									65									129									193								
2									66									130									194								
3									67									131									195								
4									68									132									196								
5									69									133									197								
6									70									134									198								
7									71									135									199								
8									72									136									200								
9									73									137									201								
10									74									138									202								
11									75									139									203								
12									76									140									204								
13									77									141									205								
14									78									142									206								
15									79									143									207								
16									80									144									208								
17									81									145									209								
18									82									146									210								
19									83									147									211								
20									84									148									212								
21									85									149									213								
22									86									150									214								
23									87									151									215								
24									88									152									216								

25	89	153	217
26	90	154	218
27	91	155	219
28	92	156	220
29	93	157	221
30	94	158	222
31	95	159	223
32	96	160	224
33	97	161	225
34	98	162	226
35	99	163	227
36	100	164	228
37	101	165	229
38	102	166	230
39	103	167	231
40	104	168	232
41	105	169	233
42	106	170	234
43	107	171	235
44	108	172	236
45	109	173	237
46	110	174	238
47	111	175	239
48	112	176	240
49	113	177	241
50	114	178	242
51	115	179	243
52	116	180	244
53	117	181	245
54	118	182	246
55	119	183	247
56	120	184	248
57	121	185	249
58	122	186	250
59	123	187	251
60	124	188	252
61	125	189	253
62	126	190	254
63	127	191	255

2048/4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDERING BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Note: For 256 x 8 Use Previous Page Only

Word	OUTPUT								Word	OUTPUT								Word	OUTPUT								Word	OUTPUT							
	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
256									320									384									448								
257									321									385									449								
258									322									386									450								
259									323									387									451								
260									324									388									452								
261									325									389									453								
262									326									390									454								
263									327									391									455								
264									328									392									456								
265									329									393									457								
266									330									394									458								
267									331									395									459								
268									332									396									460								
269									333									397									461								
270									334									398									462								
271									335									399									463								
272									336									400									464								
273									337									401									465								
274									338									402									466								
275									339									403									467								
276									340									404									468								
277									341									405									469								
278									342									406									470								
279									343									407									471								
280									344									408									472								

281	345	409	473
282	346	410	474
283	347	411	475
284	348	412	476
285	349	413	477
286	350	414	478
287	351	415	479
288	352	416	480
289	353	417	481
290	354	418	482
291	355	419	483
292	356	420	484
293	357	421	485
294	358	422	486
295	359	423	487
296	360	424	488
297	361	425	489
298	362	426	490
299	363	427	491
300	364	428	492
301	365	429	493
302	366	430	494
303	367	431	495
304	368	432	496
305	369	433	497
306	370	434	498
307	371	435	499
308	372	436	500
309	373	437	501
310	374	438	502
311	375	439	503
312	376	440	504
313	377	441	505
314	378	442	506
315	379	443	507
316	380	444	508
317	381	445	509
318	382	446	510
319	383	447	511

(8223,8224) (82S23, 82S123) (10139)

CB (XXX) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

WORD	INPUTS						OUTPUTS							
	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

(82S26) (82S29)

CB (XXXX) 1024 BIT READ ONLY MEMORY TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
0					64					128					192				
1					65					129					193				
2					66					130					194				
3					67					131					195				
4					68					132					196				
5					69					133					197				
6					70					134					198				
7					71					135					199				
8					72					136					200				
9					73					137					201				
10					74					138					202				
11					75					139					203				
12					76					140					204				
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60					124					188					252				
61					125					189					253				
62					126					190					254				
63					127					191					255				

(8228)
4096 BIT READ ONLY MEMORY TRUTH TABLE/ORDER BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1	Word	OUTPUT O_4	O_3	O_2	O_1
0					70					140					210				
1					71					141					211				
2					72					142					212				
3					73					143					213				
4					74					144					214				
5					75					145					215				
6					76					146					216				
7					77					147					217				
8					78					148					218				
9					79					149					219				
10					80					150					220				
11					81					151					221				
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13					83					153					223				
14					84					154					224				
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16					86					156					226				
17					87					157					227				
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32					102					172					242				
33					103					173					243				
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62					132					202					272				
63					133					203					273				
64					134					204					274				
65					135					205					275				
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68					138					208					278				
69					139					209					279				

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4096 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

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P.O. NO.: _____

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DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
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283					353					423					493				
284					354					424					494				
285					355					425					495				
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309					379					449					519				
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315					385					455					525				
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328					398					468					538				
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332					402					472					542				
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348					418					488					558				
349					419					489					559				

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4096 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
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561					631					701					771				
562					632					702					772				
563					633					703					773				
564					634					704					774				
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569					639					709					779				
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571					641					711					781				
572					642					712					782				
573					643					713					783				
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575					645					715					785				
576					646					716					786				
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586					656					726					796				
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588					658					728					798				

589					659					729					799				
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591					661					731					801				
592					662					732					802				
593					663					733					803				
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622					692					762					832				
623					693					763					833				
624					694					764					834				
625					695					765					835				
626					696					766					836				
627					697					767					837				
628					698					768					838				
629					699					769					839				

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Word	OUTPUT				Word	OUTPUT				Word	OUTPUT				Word	OUTPUT			
	O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1		O_4	O_3	O_2	O_1
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841					911					981									
842					912					982									
843					913					983									
844					914					984									
845					915					985									
846					916					986									
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848					918					988									
849					919					989									
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851					921					991									
852					922					992									
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863					933					1003									
864					934					1004									
865					935					1005									
866					936					1006									
867					937					1007									
868					938					1008									

869					939					1009									
870					940					1010									
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875					945					1015									
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880					950					1020									
881					951					1021									
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908					978														
909					979														

SALES OFFICES

New England Regional Sales Office
Lexington, Massachusetts 02173
Miller Building, Suite 11
594 Marrett Road
Phone (617) 861-0840
TWX: (710) 326-6711

Wappingers Falls, New York
Imperial Plaza
Phone: (914) 297-4074

Newmarket, Ont., Canada
303 Towercrest Dr.
Phone: (416) 895-4256

Atlantic States Regional Sales Offices
Fort Lee, New Jersey 07024
2460 LeMoine Avenue
Phone (201) 947-9870
TWX: (710) 991-9794

Woodbury, Long Island, New York 11797
20 Crossway Park, North
Phone (516) 364-9100
TWX: (510) 221-2158

Clearwater, Florida 33515
3267 San Mateo Blvd.
Phone (813) 726-3747

Medford, New Jersey 08055
Cedar Brook Building
Taunton Blvd.
Phone (609) 665-5071
TWX: (510) 683-6291

Rockville, Maryland 20852
11400 Rockville Pike, Suite 304
Phone (301) 881-5710
TWX: (710) 828-0532

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5105 Tollview Drive, Suite #209
Phone (312) 259-8300
TWX: (910) 687-0765

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725 S. Adams Road
Phone (313) 642-3789
TWX: (810) 232-1673

Dallas, Texas 75230
12830 Hillcrest, Suite 111
Phone (214) 661-1296
TWX: (910) 860-5451

Indianapolis, Indiana 46205
4002 Meadows Drive, Suite J
Phone (317) 545-3232
TWX: (810) 341-3248

Minneapolis, Minnesota 55431
8200 Humboldt Ave., S.
Phone (612) 884-7451
TWX: (910) 576-2845

Northwest Regional Sales Office
Sunnyvale, California 94086
465 Mathilda, Suite 301
Phone (408) 736-7565

Southwest Regional Sales Offices
Irvine, California 92664
2061 Business Center Drive, Suite 214
Phone (714) 833-8980
TWX: (910) 595-1506

Del Mar, California 92014
P. O. Box 788
Phone (714) 453-7570

Phoenix, Arizona 85022
12601 N. Cave Creek Rd., Suite 105
Phone (602) 971-2517 TWX: (910) 950-1299

Encino, California 91316
15910 Ventura Blvd., Suite 813
Phone: (213) 990-2610 TWX: (910) 495-1772

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Scottsdale 85254: Adrig Sales, Box 1607
Phone: (602) 947-4336 TWX: (910) 950-1293

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Toronto 17, Ontario: Corning Glass Works of Canada, Ltd.,
135 Vanderhoff Ave.
Phone: (416) 421-1500 TWX: (610) 491-2155

Montreal 265, Quebec: Corning Glass Works of Canada,
7065 Chester Ave.

COLORADO
Denver 80237: Parker Webster Company, 8213 E. Kenyon Dr.
Phone: (303) 770-1972 TWX: (910) 935-0881

CONNECTICUT
Hamden 06518: Kanan Associates, P. O. Box 5204
Phone: (203) 288-9276 TWX: (710) 465-1540

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Altamonte Springs 32701: WMM Associates, Inc., 505 Tivoli Ct.
Phone: (305) 831-4645

Clearwater 33516: WMM Associates, Inc.,
Hulmac Building, Suite 115,
3118 Gulf to Bay Boulevard
Phone: (813) 726-8871, (813) 726-8872

Pompano Beach 33060: WMM Associates, Inc.,
1628 E. Atlantic Blvd.
Phone: (305) 943-3091

INDIANA
Indianapolis 46250: R. H. Newsom Associates, 6320 Woburn Dr.
Phone: (317) 849-4442

KANSAS
Overland Park 66201: B. C. Electronics, 7520 West 63rd
Phone: (913) 831-2922 TWX: (910) 743-6862

MASSACHUSETTS
Newton Highlands 02161: Kanan Associates, 88 Needham Street
Phone: (617) 969-7140 TWX: (710) 335-1686

MICHIGAN
Detroit 48224: Rathsburg Associates, 16621 East Warren Avenue
Phone: (313) 882-1717

MISSOURI
St. Louis 63132: B. C. Electronics, 1573 North Warson Road
Phone: (314) 426-3231 TWX: (910) 765-0940

NEW MEXICO
Albuquerque 87110: Staley Company Inc., 2925 Charleston N.E.
Phone: (505) 294-2660

UPSTATE NEW YORK
Dewitt 13214: TriTech Electronics, Inc.,
P. O. Box C Phone: (315) 446-2881

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Winston-Salem 27101: Murphy-Cota, 1106 Burke Street
Phone: (919) 723-1002 TWX: (510) 931-3101

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Phone: (513) 435-1301

Fairview Park 44126: Norm Case Associates, P.O. Box 4791
Phone: (216) 333-4120 TWX: (810) 421-8396

TEXAS

Dallas 75229: McCoy Associates, 4339 Southcrest Road
Phone: (214) 352-9517

Richardson 75080: Semiconductor Sales Associates,
312 North Central Expressway, Suite 213
Phone: (214) 231-6181

Houston 77023: Semiconductor Sales Associates,
975 Corbindale, Suite 109
Phone: (713) 969-7700

WASHINGTON

Bellevue 98009: Western Technical Sales, P. O. Box 902
Phone: (206) 454-3906 (503) 224-5107 TWX: (910) 443-2309

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Phone: (602) 273-7331 TWX: (910) 951-1550

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Culver City 90230: Hamilton Electro Sales,
10912 W. Washington
Phone: (213) 870-7171 TELEX: 677-100, 674-381, 674-354

El Monte 91731: G. S. Marshall, 9674 Telstar Avenue
Phone: (213) 686-1500 TWX: (910) 587-1565

Los Angeles 90022: KT/Wesco Electronics, 5650 Jillson Street
Phone: (213) 685-9525 TWX: (910) 580-1980

Mountain View 94041: Hamilton/Avnet Electronics,
340 East Middlefield Road
Phone: (415) 961-7000 TELEX: 348-201

Palo Alto 94303: Wesco Electronics, 3973 East Bayshore Road
Phone: (415) 968-3475 TWX: (910) 379-6488

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8917 Complex Dr.
Phone: (714) 279-2421

San Diego 92123: Kierulff Electronics,
8797 Balboa Avenue
Phone: (714) 278-2112 TWX: (910) 335-1182

Sunnyvale 94063: Cramer Electronics,
720 Palomar
Phone: (408) 739-3011

CANADA

Downsview 463, Ontario: Cesco Electronics, Ltd.,
24 Martin Ross Avenue
Phone: (416) 661-0220 TELEX: 02-29697

Downsview, Ontario: Cramer Electronics, 920 Alness Ave.,
Unit 9
Phone: (416) 661-9222

Montreal, Quebec: Cesco Electronics, Ltd., 4050 Jean Talon West
Phone: (514) 735-5511 TWX: (610) 421-3445

Montreal, Quebec: Hamilton/Avnet, 935 Montee De Liesse
Phone: (514) 735-6393 TWX: (610) 421-3731

Ottawa, Ontario: Hamilton/Avnet Electronics, 880 Lady Ellen Place
Phone: (613) 725-3071

Ottawa, Ontario: Cesco Electronics, Ltd., 1300 Carling Avenue
Phone: (613) 729-5118

Quebec: Cesco Electronics, Ltd., 128 St. Vallier Street
Phone: (418) 524-3518

COLORADO

Denver 80216: Hamilton/Avnet Electronics, 5921 N. Broadway
Phone: (303) 534-1212 TELEX: 45872

Denver 80222: Cramer Electronics, 5465 E. Evans Place at Hudson
Phone: (303) 758-2100

CONNECTICUT

Hamden 06514: Arrow Electronics,
295 Treadwell Street
Phone: (203) 248-3801

Georgetown 06829: Hamilton/Avnet Electronics,
643 Danbury Road
Phone: (203) 762-0361

North Haven 06473: Cramer Electronics, 35 Dodge Avenue
Phone (203) 239-5641

FLORIDA

Hollywood 33021: Hamilton/Avnet Electronics, 4020 No. 29th Ave.
Phone: (305) 925-5401 TELEX: 51-4328

Hollywood 33020: Schweber Electronics, 2830 North 28th Terrace
Phone: (305) 927-0511

Orlando 32805: Hammond Electronics, 911 West Central Blvd.
Phone: (305) 241-6601 TWX: (810) 850-4121

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Atlanta 30340: Schweber Electronics,
4126 Pleasantdale Road, Suite 14
Phone: (404) 449-9170

Norcross 30071: Hamilton/Avnet Electronics
6700 Interstate 85 Access Road, Suite 2B
Phone: (404) 448-0800 TELEX: 542-127

ILLINOIS

Elk Grove 60007: Schweber Electronics, 1380 Jarvis Avenue
Phone: (312) 593-2740

Elmhurst 60126: Semiconductor Specialists, Inc.,
195 Spangler Avenue, Elmhurst Industrial Park
Phone: (312) 279-1000 TWX: 254-0169

Schiller Park 60176: Hamilton/Avnet Electronics,
3901 No. 25th Avenue
Phone: (312) 678-6310 TELEX: 728-330

INDIANA

Indianapolis 46241: Semiconductor Specialists,
P.O. Box 41630, Weir Cook Airport
Phone: (317) 243-8271 TWX: (810) 341-3126

KANSAS

Lenexa 66215: Hamilton/Avnet Electronics,
37 Lenexa Industrial Center
Phone: (913) 888-8900

MARYLAND

Hanover 21076: Hamilton/Avnet Electronics, 7255 Standard Drive,
Phone: (301) 796-5000 TELEX: 879-68

Rockville 20850: Pioneer Washington Electronics, Inc.,
1037 Taft Street Phone: (301) 424-3300

Rockville 20852: Schweber Electronics, 5640 Fisher Lane
Phone: (301) 881-2970

MASSACHUSETTS

Burlington 01803: Hamilton/Avnet Electronics
185 Cambridge Street
Phone: (617) 273-2120 TELEX: 9496-61

Needham Heights 02194: Kierulff/Schley, 14 Charles Street
Phone: (617) 449-3600 TWX: (710) 326-1179

Newton 02150: Cramer Electronics, 85 Wells Avenue
Phone: (617) 969-7700

Waltham 02154: Schweber Electronics, 213 Third Ave.,
Phone: (617) 890-8484

MICHIGAN

Livonia 48150: Hamilton/Avnet Electronics,
12870 Farmington Road
Phone: (313) 522-4700

Detroit 48240: Semiconductor Specialists, Inc.,
25127 W. Six Mile Road
Phone: (313) 255-0300 TWX: (910) 254-0169

MINNESOTA

Minneapolis 55423: Semiconductor Specialists, Inc.,
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