Sil3726 SATA Port Multiplier
Data Sheet

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Revision History

Revision	Date	Comment
A	4/2005	Derived from preliminary specification rev. 0.51
B	6/2006	Updated green package, Converted to standard format
C	7/2006	Datasheet is no longer under NDA, removed confidential markings.

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Overview

Description

Silicon Images SiI 3726 SATA Port Multiplier is 1-to-5 SATA Port Multiplier designed to provide a high performance link between a single SATA host port and five SATA device ports. With its unique data aggregation capability and 3 Gbps serial link capability, the SiI 3726 SATA Port Multiplier is able to take full advantage of 3 Gbps host link bandwidth and FIS-based switching host controllers by bundling together data from device ports and sending it over the 3 Gbps host link. Additionally, the feature-rich SiI 3726 supports all the port multiplier related SATA II extensions allowing system designers to exploit the full potential of SATA in their storage solutions.

The SiI 3726 SATA Port Multiplier supports host and device link rates of 1.5 Gbps and 3 Gbps with auto-negotiation allowing system designers to utilize 3 Gbps host links with today's 1.5 Gbps hard drives, and to future-proof designs for the emergence of 3 Gbps SATA hard drives. Additionally, the SiI 3726 contains a SATA Enclosure Management Bridge (SEMB) to pass in-band enclosure management information between the host and an enclosure management device. Other important features include, programmable high drive capability for backplane and external applications, asynchronous notification to eliminate the need for host polling to determine if a device has been added or removed, and hot plug support.

The SiI 3726 is designed for optimum power, performance and price. It is based on Silicon Images industry leading SATALink technology. It leverages much of the circuit innovation at the physical layer of Silicon Image's proprietary reduced-overhead Multi-layer Serial Link (MSLTM) architecture, which was pioneered and proven with our market-leading PanelLink® products. Silicon Image has shipped over 35 million units of PanelLink® products for host systems and displays in the PC and the CE markets, notable for their noisy operating conditions.

Features

Overall Features

- One-to-five native SATA Port Multiplier
- Full support for FIS-based switching and command-based switching SATA host controllers
- Advanced data aggregation architecture for ultra-fast read and write operations with FIS-based switching controllers
- 21mm x 21mm, 364 pin BGA package with a 20 x 20 array of balls
- High-speed, native SATA connections to host and device
- Host and device status and activity LEDs

Robust, High Performance PHY Technology

- 1.5 Gbps and 3.0 Gbps PHY support with auto-negotiation
- Compliant with SATA II external PHY specifications
- Independently programmable PHY settings to support extended PCB trace lengths and external SATA applications
- Industry proven SATALink technology

Storage System Features

- Hot-plug and ATAPI support
- SATA Enclosure Management Bridge (SEMB) support with I^2C interface to the external Storage Enclosure Processor (SEP)
- Far-end Re-timed loop-back BIST for host initiated system testing
- Supports host control of hard disk drive staggered spin-up
- Asynchronous notification support

Architecture Features

- Features independent 8 kByte FIFO per device serial ATA channel for reads and writes
- High performance data movement between all SATA ports

Applications

- Expansion Storage Bricks
- Disk Shelves
- Storage Enclosures

Functional Block Diagram

Figure 1 shows the Block Diagram for the Sil 3726 SATA Port Multiplier.

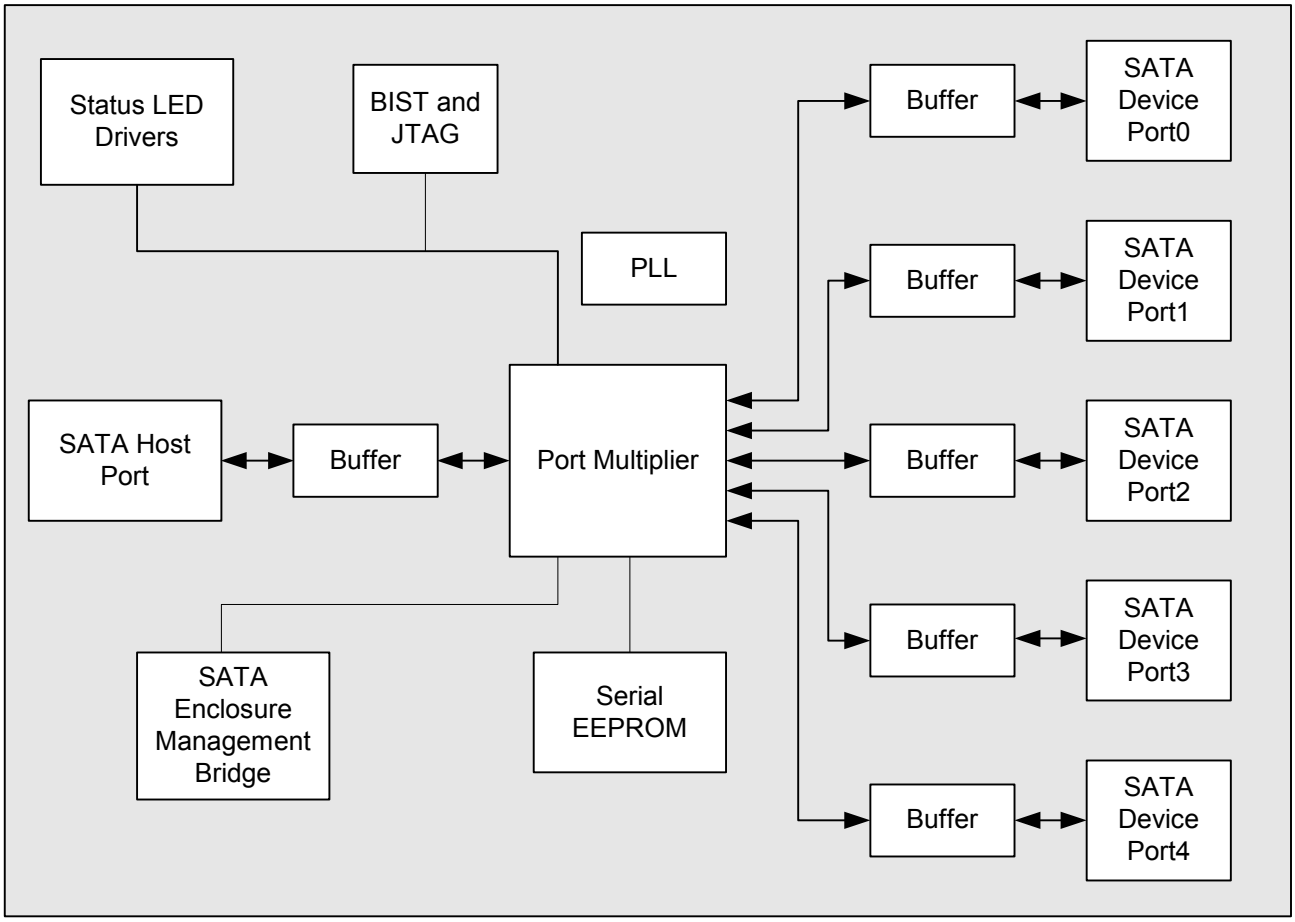

Figure 1: Sil 3726 SATA Port Multiplier Block Diagram

The following sections will describe the features of the port multiplier.

SATA Ports

The host port supports the SATA-II speed of 3 Gbps and auto-negotiates to 1.5 Gbps to interface with SATA-I host controllers. The device ports operate at SATA-II speeds of 3 Gbps or auto-negotiate to 1.5 Gbps. All ports support hot plug and extended (48 bit LBA) drive capability.

LED Modes

Device/Host LED Modes

Table 1 shows the device or host LED modes and descriptions. The mode is determined by the LED_MODE pin (pin A3). LED pins are open-drain and sink current up to 12mA in their low voltage active state (LED On), or are high impedance in their high voltage non-active state (LED Off). These signals will operate with an external pull-up resistor and LED.

Each activity will turn on or off LED0 for approximately 70ms. The blinking rate is approximately 400ms on and 400ms off.

Table 1: Device or Host LED Modes and Descriptions

LED_MODE	LED1	LED0	Description
0 (PC mode)	Off	Off	Power on, no device attached
0 (PC mode)	On	Off	PHY communication established, (activity = LED0 On)
0 (PC mode)	Blink	Blink	Error
1 (Enterprise mode)	Off	Off	Power on, no device
1 (Enterprise mode)	On	Off	Error

System LED Modes

Table 2 shows the System LED modes and their descriptions.

Table 2: System LED Modes and Descriptions

Signal	Description
LED_S0	EEPROM load error On: Loading error Off: No loading errors
LED_S1	System ready On: System is ready Off: System is not ready
LED_S2	System error On: System error Off: No system errors

In normal operation, if system reset is released, LED_S3 will turn-on while the firmware loads into the SiI 3726 SATA Port Multiplier (~ 1 second). When the firmware load is complete, LED_S1 will turn-on indicating the system is ready to be used.

High Speed Serial Interface Optimization

In order to accommodate different system environments, the port multiplier allows the designer to configure the device PHYs to support various cable/PCB lengths on each serial I/O independently.

PHY Configuration Settings

Table 3 shows the configuration settings and description for each high-speed serial port.

Pre-emphasis and equalization are used to compensate the signal degradation due to increased cable lengths. Without pre-emphasis or equalization, jitter at the receiver end will increase along with the increase of the cable length, causing signal degradation and Bit Error Rate problems. The effect may depend on the system environment. Factors such as cable quality, PCB implementation, receiver load, etc. all affect the signal quality. Please consult with Silicon Image's technical support department for more information.

Table 3: PHY Configuration Settings

Serial Port	Signal	Settings and Description
Host Port	HIO[2:0]	HIO[2:0] = 0b000 (Default). PC motherboard to device applications up to 1m internal cable, external desktop up to 2m external cable ((2 Meter eSATA cable) or short backplane up to 18 inch of FR4 (0.012 mil trace width with 1 oz copper) HIO[2:0] = 0b001: Tx amplitude will be 100mV lager than 000 setting HIO[2:0] = 0b010 – 0b100 (Reserved. please consult with Silicon Image technical support for this detail): external desktop up to 4m external cable or short backplane up to 30 inch of FR4 (0.012 mil trace width with 1 oz copper) 0b 010: Only pre-emphasis enabled 0b 011: Only equalization enabled 0b111: Both pre-emphasis and equalization enabled HIO[2:0] = 0b101 – 0b111 (Reserved. Contact Silicon Image Technical Support for details): external desktop longer than 4m external cable or short backplane longer than 30 inch of FR4 (0.012 mil trace width with 1 oz copper) 0b010: Only pre-emphasis enabled 0b011: Only equalization enabled 0b111: Both pre-emphasis and equalization enabled
Device #0	DAIO[1:0]	DxIO[1:0] = 0b00 (Default): PC motherboard to device applications up to 1m internal cable, external desktop up to 2m external cable (2 Meter eSATA cable) or short backplane up to 18 inch of FR4 (0.012 mil trace width with 1 oz copper) DxIO[1:0] = 0b01: Tx amplitude will be 100mV lager than 00 setting DxIO[1:0] = 0b10 (Reserved. Contact Silicon Image Technical Support): external desktop up to 4m external cable or short backplane up to 30 inch of FR4 (0.012 mil trace width with 1 oz copper). Both pre-emphasis and equalization are enabled DxIO[1:0] = 0b11 (Reserved. Contact Silicon Image Technical Support): external desktop longer than 4m external cable or short backplane longer than 30 inch of FR4 (0.012 mil trace width with 1 oz copper). Both pre-emphasis and equalization are enabled
Device #1	DBIO[1:0]	
Device #2	DCIO[1:0]	
Device #3	DDIO[1:0]	
Device #4	DEIO[1:0]	

Tx Eye Measurement

The SiI 3726 SATA Port Multiplier has the capability to output random (scrambled) and deterministic data patterns (primitives) to downstream devices bypassing the OOB sequence for eye measurement testing.

Upon completing the device enumeration process, the port multiplier outputs COM_RESET/COMINIT periodically. This implementation maintains compatibility with the SATA compliant host/device and enables hot plug support. But this implementation also prevents evaluating the Tx eye quality by connecting it directly to the oscilloscope.

By bypassing the OOB sequence after the host completes the device enumeration sequence, the Tx will output a random data pattern. The port multiplier can bypass the OOB sequence by setting pin Y12 (OOB_BP) to high. In addition to this, if CONT primitive is disabled by setting pin Y11 (CONT_DIS) to high, the Tx will output a deterministic data pattern. The output generation (1.5 G or 3.0 G) can be selected by pin W12 (TX_GEN).

The random data pattern is a scrambled data pattern and useful for eye mask testing. The deterministic pattern is a repetitive pattern of primitives and is useful for jitter analysis. The primitive is normally synchronous and includes Align primitives every 256DWORDs.

GPIO Support

The 32 bits in General Status and Control Register [130] each correspond to its associated General Purpose Output pin on a write (GPO[31:0]). If the bit is set to 0, the GPO will output a high logic level. Bits [2:9] and [22:29] are not assigned to the pins and the value in the bit field does not effect the operation.

The 32 bits in General Status and Control Register [130] each correspond to its associated General Purpose Input pin on a read (GPI[31:0]). If the GPI1 is high, bit 1 will be set. Some of these GPI pins are reserved for various other functions as follows.

- Bit fields [12:10 / EMID [2:0]
- Bit fields [9:2] / 1000_0000b
- Bit fields [24:14] / DEIO[1], DDIO[0], DCIO[1:0], DBIO[1:0], DAIO[1:0]
- Bits 27 and 25 / DEIO[0], DDIO[1]

GPI pins have internal pull-downs, and GPO pins are initialized to drive low by the firmware.

The Read/Write Port Multiplier command can be used to read or write the GSCR. Address 0x0F must be specified in PortNum field of the command FIS in order to read or write the GSCR. The details of the Read/Write Port Multiplier commands are defined in the SATA II Port Multiplier Specification.

BIST Support

The SiI 3726 SATA Port Multiplier supports far-end retimed loopback BIST only as a target as described by the SATA II Port Multiplier Specification. If the port multiplier receives a BIST activated FIS, it enters BIST mode and loops back the SATA interface. The port multiplier does not propagate the BIST activated FIS to the other ports.

Serial ATA Power Mode Request

Either the host or the devices may initiate power mode requests. If the request is initiated by the device, upon receipt of the appropriate PMREQ (PMREQ_P or PMREQ_S) request, the port multiplier sends back the PMACK primitives and disables the TxP/TxN pair for the port.

If the request is initiated by the host, the port multiplier sends back the PMACK primitives and disables the TxP/TxN pair for the host port. The port multiplier issues the PMREQ to the all attached devices. Upon receipt of PMACK primitives from the physical devices, the TxP/TxN pair will be disabled.

Device Enumeration Sequence

The device enumeration process is defined in the SATA II Port Multiplier Specification.

Upon receipt of the software reset with 0x0F as the PM port number, the SiI 3726 SATA Port Multiplier issues a Register Frame Information Structure (FIS) with the Port Multiplier Signature. Before receiving the software reset with 0x0F as the PM port number, the port multiplier delivers all Frame Information Structures to port 0 regardless of the PM port number value in the receiving FIS.

After sending the software reset with 0x0F as the PM port number, the PM aware host resets each device port by programming bit 1 in the SControl register and writing 0xFFFF_FFFF in the SError register to clear the bits in the register.

The host should examine the SStatus and SError registers to determine whether or not a device is connected to the device ports. If a device is attached to the port, the host should initialize the device before it using it for a read or a write operation.

Storage Enclosure Support

The SiI 3726 SATA Port Multiplier is compliant with the SATA II port multiplier specification. It has a SATA Enclosure Management Bridge (SEMB) that passes in-band enclosure management data between the host controller and a companion enclosure management device through an I^2C bus.

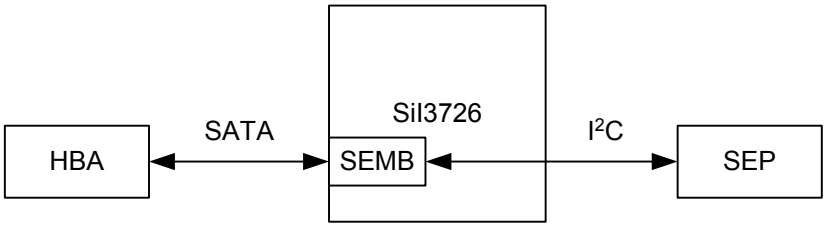

Figure 2: Enclosure Management Support Overview

The port multiplier supports the SAF-TE and SES protocols. The host issues Enclosure Management commands through the SATA interface. Enclosure Management commands use the SEP_ATTN commands in the Command register and the SEP command code in the Features register. The SEP command protocol is defined in the SAF-TE or SES specification.

The I^2C interface is multi-master capable and can transfer data at 0 - 400 kbits/s. The SEMB I^2C address is 0001xxx0, where xxx are selected using pins EM_ID[2:0]. This allows up to eight SiI 3726 SATA Port Multipliers on the same SEMB I^2C bus. The SEP I^2C address should be 0xC0, as defined in the SATA II specification.

Internal Register Space

The SiI 3726 SATA Port Multiplier has 32-bit wide registers that control its internal operations.

General Status and Control (GSCR) Registers

These registers are defined in the SATA II Port Multiplier specification.

The Read/Write Port Multiplier command is used to read or write the GSCR registers. Address 0x0F must be specified in the PortNum field of the command FIS in order to read or write the GSCR. The Read/Write Port Multiplier commands are defined in the SATA II Port Multiplier Specification.

Addr	Name	31	30	29	28	27	26	25	24
0x00 GSCR[00]	Product Identifier	Device ID							
		23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
		Device ID							
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
		Vendor ID							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		Vendor ID							

Bit	Label	R/W	Description	Default
This register defines the Device ID and Vendor ID associated with the SiI 3726.				
31:16	Device ID	R	The default value of 0x3726 identifies the device as Silicon Image SiI3726.	0x3726
15:0	Vendor ID	R	This field defaults to 0x1095 to identify the vendor as Silicon Image.	0x1095

Addr	Name	31	30	29	28	27	26	25	24
0x01 GSCR[01]	Revision Information	RSVD0							
		23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
		RSVD0							
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
		Revision ID/Chip Revision ID							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		RSVD0					PM spec		RSVD0

Bit	Label	R/W	Description	Default
This register defines the revision ID associated with the SiI3726.				
31:16	RSVD0	R	This bit field is reserved and returns a zero value.	0x0000
15:8	Revision ID/Chip Revision ID	R	This bit field is set to indicate the revision level of the chip design, revision 0x17 is defined by this specification.	0x17
7:3	RSVD0	R	This bit field is reserved and returns a zero value.	0b00000
2:1	PM spec	R	This register defines the Port Multiplier Specification Supports. This bit field is set to 0x11 to indicate that SiI 3726 supports the Port Multiplier Specification and 1.1.	0b00
0	RSVD0	R	This bit field is reserved and returns a zero value.	0b0

Addr	Name	31	30	29	28	27	26	25	24
0x02 GSCR[02]	Port Information	RSVD0							
		23	22	21	20	19	18	17	16
		RSVD0							
		15	14	13	12	11	10	9	8
		RSVD0							
		7	6	5	4	3	2	1	0
		RSVD0				Number of Fan-out ports			

Bit	Label	R/W	Description	Default
This register defines port information associated with the SiI3726.				
31:4	RSVD0	R	This bit field is reserved and returns a zero value.	0x0000 000
3:0	Number of Fan-out ports	R	This bit field is set to 0x06 to indicate that SiI3726 supports one host and five device ports.	0x6

Addr	Name	31	30	29	28	27	26	25	24
0x20 GSCR[32]	Error Information	RSVDRW							
		23	22	21	20	19	18	17	16
		RSVDRW							
		15	14	13	12	11	10	9	8
		RSVDRW							
		7	6	5	4	3	2	1	0
		RSVDRW		Error Information	Error Information	Error Information	Error Information	Error Information	Error Information

Bit	Label	R/W	Description	Default
31:06	RSVDRW	R/W	This bit field is reserved and returns the value written to it.	0x0000
5	Error Information	R/W	This bit is set to 1 when the bits in port5 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33]..	0b0
4	Error Information	R/W	This bit is set to 1 when the bits in port4 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33].	0b0
3	Error Information	R/W	This bit is set to 1 when the bits in port3 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33].	0b0
2	Error Information	R/W	This bit is set to 1 when the bits in port2 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33].	0b0
1	Error Information	R/W	This bit is set to 1 when the bits in port1 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33].	0b0
0	Error Information	R/W	This bit is set to 1 when the bits in port0 PSCR[1] SError register are set. The bits used for this bit are selected by the GSCR[33].	0b0

Addr		Name	31	30	29	28	27	26	25	24
0x21 GSCR[33]		Error Information	Error Information							
			23	22	21	20	19	18	17	16
			Error Information							
			15	14	13	12	11	10	9	8
			Error Information							
			7	6	5	4	3	2	1	0
			Error Information							
Bit	**Label**	**R/W**	**Description**							**Default**
31:0	Error Information	R/W	This bit field provides the bits used for error information in the GSCR[32] Error Information register. If the bit set to 1, that bit will be used by the GSCR[32].							0x0400 FFFF

Addr		Name	31	30	29	28	27	26	25	24
0x40 GSCR[64]		Optional Features Support	RSVD0							
			23	22	21	20	19	18	17	16
			RSVD0							
			15	14	13	12	11	10	9	8
			RSVD0							
			7	6	5	4	3	2	1	0
			RSVD0				Async notification support	Dynamic SSC Transmit Enable support	Issuing PMREQ_P to host support	BIST support
Bit	**Label**	**R/W**	**Description**							**Default**
31:4	RSVD0	R	This bit field is reserved and returns a zero value.							0x0000 000
3	Async notification support	R	This bit field is set to 1 to indicate that the Sil3726 supports Asynchronous notification.							0b1
2	Dynamic SSC Transmit Enable support	R	This bit field is set to 0 to indicate that the Sil3726 does not support Dynamic SSC Transmit Enable.							0b0
1	Issuing PMREQ_P to host support	R	This bit field is set to 0 to indicate that the Sil3726 does not support issuing PMREQ_P to host.							0b0
0	BIST support	R	This bit field is set to 1 to indicate that the Sil3726 supports BIST.							0b1

Addr	Name	31	30	29	28	27	26	25	24
0x60 GSCR[96]	Optional Features Enable	RSVD0							
		23	22	21	20	19	18	17	16
		RSVD0							
		15	14	13	12	11	10	9	8
		RSVD0							
		7	6	5	4	3	2	1	0
		RSVD0				Enable Asynchronous notification	Enable Dynamic SSC Transmit	Enable issuing PMREQ_P to host	Enable BIST

Bit	Label	R/W	Description	Default
31:4	RSVD0	R	This bit field is reserved and returns a zero value.	0x0000000
3	Enable Asynchronous notification	R	Setting this bit enables Asynchronous notification.	0b0
2	Enable Dynamic SSC Transmit	R	The SiI3726 does not support Dynamic SSC Transmit and setting this bit does not affect the operation.	0b0
1	Enable issuing PMREQ_P to host	R	The SiI3726 does not support issuing PMREQ_P to the host and setting this bit does not affect the operation.	0b0
0	Enable BIST	R	Setting this bit enables BIST.	0b1

Addr	Name	31	30	29	28	27	26	25	24
0x03 - 0x1F GSCR[03-31], 0x22 - 0x3F GSCR[34-63], 0x41 - 0x5F GSCR[65-95], 0x61 - 0x7F GSCR[97-127]	Reserved	RSVD0							
		23	22	21	20	19	18	17	16
		RSVD0							
		15	14	13	12	11	10	9	8
		RSVD0							
		7	6	5	4	3	2	1	0
		RSVD0							

Bit	Label	R/W	Description	Default
31:0	RSVD0	R	This bit field is reserved and returns a zero value.	0x00000000

Addr		Name	31	30	29	28	27	26	25	24
0x80 - 0x81 GSCR[128-129, 0x83 - 0xFF GSCR[131-255]		Vendor Unique	Vendor Unique							
			23	22	21	20	19	18	17	16
			Vendor Unique							
			15	14	13	12	11	10	9	8
			Vendor Unique							
			7	6	5	4	3	2	1	0
			Vendor Unique							
Bit	**Label**	**R/W**	**Description**							**Default**
31:0	Vendor Unique	R/W	These registers define vendor unique and may be used by the firmware. The user shall not access these registers.							0x0000 0000

Addr		Name	31	30	29	28	27	26	25	24
0x82 GSCR[130]		GPIO	GPIO							
			23	22	21	20	19	18	17	16
			GPIO							
			15	14	13	12	11	10	9	8
			GPIO							
			7	6	5	4	3	2	1	0
			GPIO							
Bit	**Label**	**R/W**	**Description**							**Default**
31:0	GPIO	R/W	The bit field is corresponding to the GPO pins on a write. If the bit 0 is set, the GPO 0 will output high. The bit field is corresponding to the GPI pins on a read. If the GPI 1 is high, the bit 1 will be set. GPI pins have internal pull-downs, and GPO pins will be initialized to drive low by the firmware. For details, see GPIO Support on page 10.							N/A

Port Status and Control Registers (PSCR)

The registers are defined in the SATA II Extensions to Serial ATA 1.0a Specification.

The Read/Write Port Multiplier command may be used to read or write the PSCR. The port number must be specified in the PortNum field of the command FIS in order to read or write the PSCR. The Read/Write Port Multiplier commands are defined in the SATA II Port Multiplier specification.

Addr	Name	31	30	29	28	27	26	25	24
0x00 PSCR[00]	SStatus	RSVD0							
		23	22	21	20	19	18	17	16
		RSVD0							
		15	14	13	12	11	10	9	8
		RSVD0				IPM			
		7	6	5	4	3	2	1	0
		SPD				DET			

Bit	Label	R/W	Description	Default
31:12	RSVD0	R	This bit field is reserved and returns a zero value.	0x00000
11:08	IPM	R	This field identifies the current interface power management state. 0000: Device not present or communicating not established 0001: Interface in active state 0010: Interface in partial power management state 0110: Interface in slumber power management state Others: Reserved	0x0
7:4	SPD	R	This field identifies the negotiated interface communication speed. 0000: No negotiated speed 0001: Generation 1 communication rate (1.5 Gb/s) 0010: Generation 2 communication rate (3 Gb/s) Others: Reserved	0x0
3:0	DET	R	This field indicates the interface device detection and PHY state. 0000: No device detected and PHY communication not established 0001: Device presence detected, but PHY communication not established 0010: Device presence detected and PHY communication established 0110: PHY in off-line mode as a result of the interface being disabled or running in a BIST loopback mode Others: Reserved, no action	0x0

Addr		Name	31	30	29	28	27	26	25	24
0x01 PSCR[01]		SError	DIAG							
			23	22	21	20	19	18	17	16
			DIAG							
			15	14	13	12	11	10	9	8
			ERR							
			7	6	5	4	3	2	1	0
			ERR							
Bit	**Label**	**R/W**	**Description**							**Default**
31:16	DIAG	R/W	This field contains bits as defined in Table 4. Writing a 1 to the register bit clears the B, C, F, N, H, W, and X bits. Writing a 1 to the corresponding bits in the Port Interrupt Status register also clears the F, N, W, and X bits. The B, C, and H bits operate independently of the corresponding Error Counter registers. If the error counters are used, these bits should be ignored.							0x0000
15:0	ERR	R/W	This field is not implemented; all bits are always zero.							0x0000

Table 4: SError Bit Definitions

Bit	Definition	Description
B	10b to 8b decode error	Latched decode error or disparity error from the Serial ATA PHY
C	CRC error	Latched CRC error from the Serial ATA PHY
D	Disparity error	N/A; always 0. This error condition is combined with the decode error and reported as B errors.
F	Unrecognized FIS type	Latched unrecognized FIS error from the Serial ATA link
I	PHY internal error	N/A; always 0
N	PHYRDY change	Indicates a change in the status of the Serial ATA PHY
H	Handshake error	Latched handshake error from the Serial ATA PHY
R	Reserved	Always 0
S	Link sequence error	N/A; always 0
T	Transport state transition error	N/A; always 0
W	ComWake	Latched ComWake status from the Serial ATA PHY

Addr	Name	31	30	29	28	27	26	25	24
0x02 PSCR[02]	SControl	RSVDRW							
		23	22	21	20	19	18	17	16
		RSVDRW				PMP			
		15	14	13	12	11	10	9	8
		SPM				IPM			
		7	6	5	4	3	2	1	0
		SPD				DET			

Bit	Label	R/W	Description	Default
31:20	RSVDRW	R/W	This bit field is reserved and returns the value written to it.	0x000
19:16	PMP	R/W	This field identifies the currently selected Port Multiplier port for accessing the SActive register and some bit fields of the Diagnostic registers.	0x0
15:12	SPM	R/W	This field selects a power management state. A non-zero value written to this field causes initiation of the select power management state. This field self-resets to 0 as soon as action begins to initiate the power management state transition. 0000: No power management transition requested 0001: Transition to the partial power management state initiated 0010: Transition to the slumber power management state initiated 0100: Transition from a power management state initiated (ComWake asserted) Others: Reserved	0x0
11:8	IPM	R/W	This field identifies the interface power management states that may be invoked via Serial ATA interface power management capabilities. 0000: No interface power management restrictions (partial and slumber modes enabled) 0001: Transitions to the partial power management state are disabled 0010: Transitions to the slumber power management state are disabled 0011: Transitions to both the partial and slumber power management states are disabled Others: Reserved	0x0
7:4	SPD	R/W	This field identifies the highest allowed communication speed the interface is allowed to negotiate. 0000: No restrictions (default value) 0001: Limit to Generation 1 (1.5 Gb/s) 0010: Limit to Generation 2 (3.0 Gb/s) Others: Reserved	0x0
3:0	DET	R/W	This field controls host adapter device detection and interface initialization. 0000: No action 0001: COMRESET is periodically generated until another value is written to the field 0100: No action Others: Reserved; no action	0x0

Addr	Name	31	30	29	28	27	26	25	24
0x03 - 0x0F PSCR[03–15]	Reserved	RSVD0							
		23	22	21	20	19	18	17	16
		RSVD0							
		15	14	13	12	11	10	9	8
		RSVD0							
		7	6	5	4	3	2	1	0
		RSVD0							

Bit	Label	R/W	Description	Default
31:00	RSVD0	R	This bit fields are reserved and return a zero value.	0x0000 0000

Device Initialization

Firmware must be downloaded into the SiI 3726 SATA Port Multiplier from a Serial EEPROM for normal operation. The serial EEPROM is connected to pin numbers A9 (Serial Clock) and B9 (Serial Data).

Auto-Initialization from the EEPROM

EEPROM Specifications

The port multiplier requires an external 64 kByte (or two 64 kByte EEPROMs for double buffering) serial EEPROM (400 KHz) memory device. When double buffering is used (for fail over purposes) the primary EEPROM address must be set to “000” and the secondary EEPROM address must be set to “001”.

When powered-up, the port multiplier verifies the checksum in the primary EEPROM before loading the firmware. If the checksum does not match, the port multiplier loads the firmware from the secondary EEPROM.

The firmware contained in the EEPROM is shown below:

Address	Contents
0x0000 – 0xFFED	Code to configure the SiI 3726
0xFFEC – 0xFFF3	System Information, may contain the Serial Number, must be an ASCII string (null terminated)
0xFFF4 – 0xFFF7	Vendor ID and Chip ID 0x10953726
0xFFF8 – 0xFFFB	Firmware Revision
0xFFFC – 0xFFFF	Signature / CheckSum

The sequence of events is as follows:

1. System power-up
2. Code transfer from the EEPROM (I^2C) to the SiI 3726 SATA Port Multiplier (boot)
3. The port multiplier starts operating under software control (normal operation)

EEPROM Read/Write Operations

The timing diagram for read or write operations is shown in Figure 3. The high-level timing for a random read or write is shown in Figure 4. The high-level timing for a block transfer is shown in Figure 5.

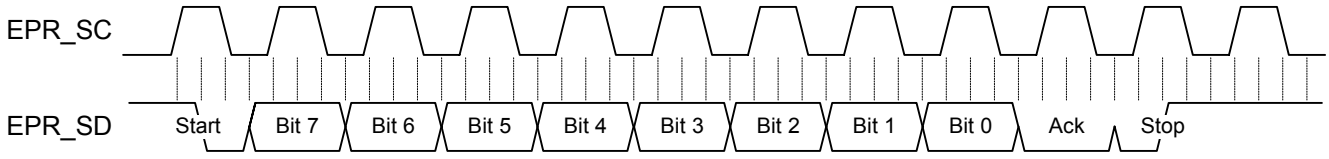

Figure 3: I^2C Transfer Timing

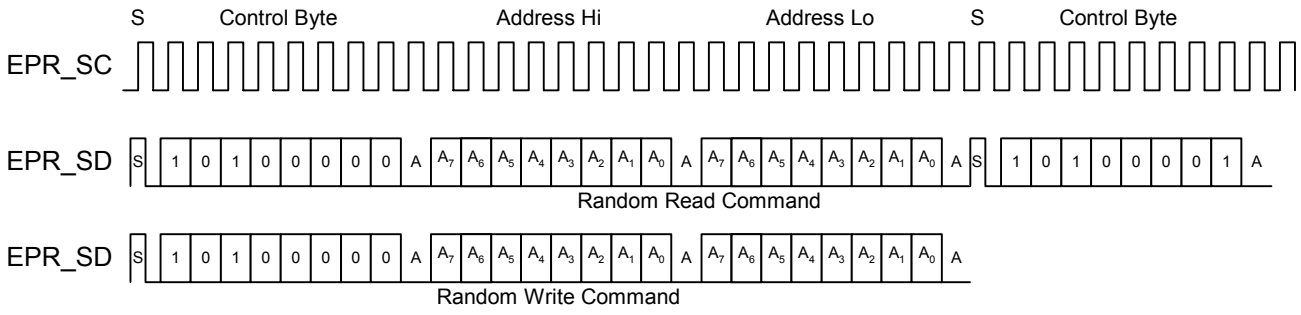

Figure 4: I^2C Random Read and Write Timing

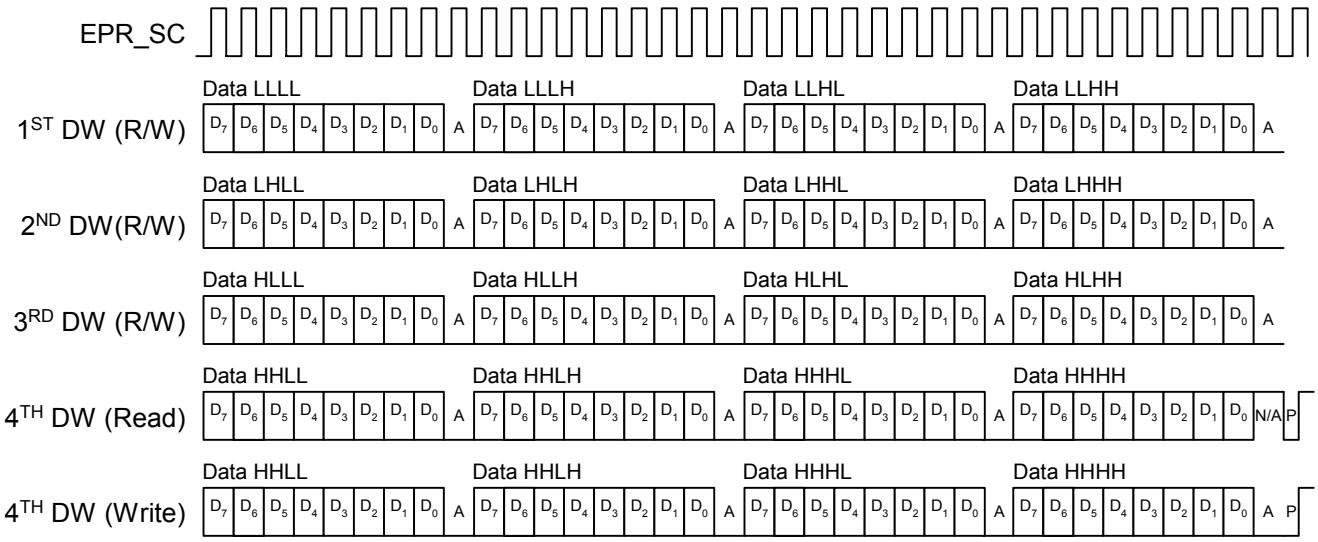

Figure 5: I²C Block Transfer

System Reset

System reset (pin A10) must be low whenever the voltage is in or out of operation range and remain for 100 ms after both 1.8V and 3.3V are stable. An example circuit is shown in Figure 6.

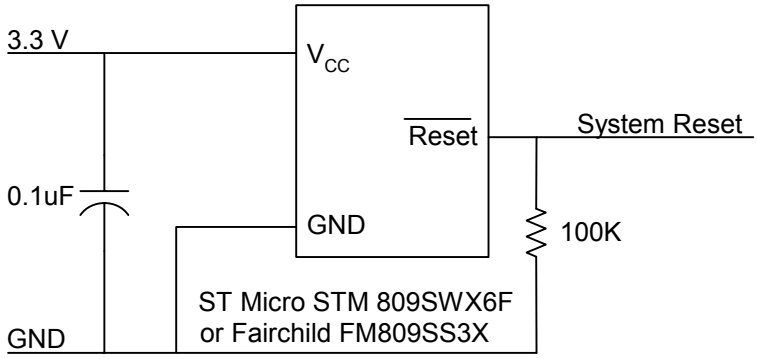

Figure 6: Power-Up Reset Circuit

Electrical Characteristics

Specifications are for commercial temperature ranges, 0°C to +70°C, unless otherwise specified.

Absolute Maximum Ratings

Table 5 specifies the absolute maximum ratings for the device.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDDO	I/O supply voltage	4.0	V
VDDA, VDDI	Core supply voltage	2.15	V
VIN	Input voltage for 3.3V I/O	-0.3 ~ VDDO+0.3	V
V_{CLKI_IN}	Input voltage for CLKI	-0.3 ~ VDDA+0.3	V
IOUT	DC output current	16	mA
θ_{JA}	Thermal resistance	17.6	°C/W

DC Specifications

Table 6 specifies the DC specifications of the device.

Table 6: DC Specifications

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
VDDA	Analog supply voltage		1.71	1.8	1.89	V
VDDI	Digital supply voltage		1.71	1.8	1.89	V
VDDO	I/O supply voltage		3.0	3.3	3.6	V
$IDD_{1.8V}$	1.8V supply voltage			800[1]	1300[2]	mA
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{IH}	Input high current	$V_{IN} = V_{DD}$	-10		10	µA
I_{IL}	Input low current	$V_{IN} = V_{SS}$	-10		10	µA
I_{ILOD}	Open drain sink current				12	mA
V_{OH}	Output high voltage		2.4			V
V_{OL}	Output low voltage				0.4	V
I_{OZ}	3-State Leakage Current			-10		µA

Notes:
Note 1: Attached to the 3 G host and all device ports attached to 1.5 G devices.
Note 2: Attached to 3 G host and devices.
Notes 1 and 2: 3.3V power consumption depends upon the LED, JTAG, I_2C and enclosure management status. If all are disabled, 3.3V power consumption will be uA.

SATA Interface DC Specifications

Table 7 shows the SATA interface DC specifications.

Table 7: SATA Interface DC Specifications

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
VDOUT_00	TX+/- Differential peak-to-peak voltage swing	50 Ω Termination PHY Configuration Setting = 000b for host port and 00b for device ports	500	550	650	mV
V_{DIN}	Rx+/Rx- Differential peak-to-peak input sensitivity		240			mV
VSQ	Rx+/Rx- OOB signal detection threshold		50	125	240	mV
VDOH	Tx+/Tx- Differential output common-mode voltage	Must be AC coupled	VDD-375	VDD-250	VDD-125	mV
VACCM	Tx AC common-mode voltage				50	mV
VDIH	Rx+/Rx- Differential input common-mode voltage	Must be AC coupled	-50	0	50	mV
ZDIN	Tx Pair differential impedance	RREF1 = 1 kOhms 1% RREF2 = 4.99 kOhms 1%	85	100	115	Ω
ZDOUT	Rx Pair differential impedance	RREF1 = 1 kOhms 1% RREF2 = 4.99 kOhms 1%	85	100	115	Ω
ZSIN	Tx Single-ended impedance	RREF1 = 1 kOhms 1% RREF2 = 4.99 kOhms 1%	40			Ω
ZSOUT	Rx Single-ended impedance	RREF1 = 1 kOhms 1% RREF2 = 4.99 kOhms 1%	40			Ω

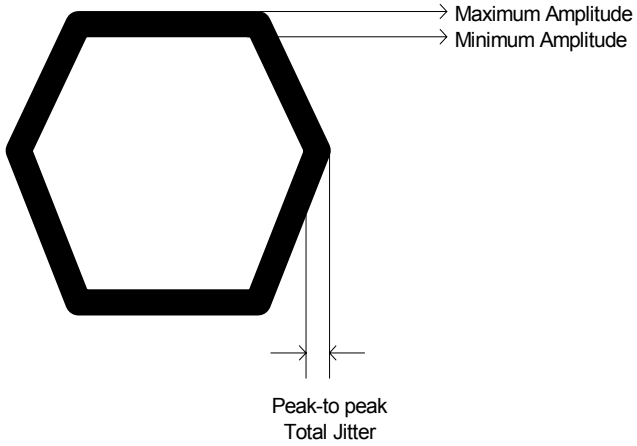

Figure 7: Eye Diagram

CLKI SerDes Input Reference Clock Requirements

Table 8 shows the input reference clock requirements.

Table 8: CLK1 SerDes Reference Clock Input Requirements

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
TCLKI_FREQ	Nominal frequency	RREF1: 1Kohms 1% RREF2: 4.99Kohms 1%		25		MHz
VCLKI_IH	Input high voltage	-	0.7 x VDDA			V
VCLKI_IL	Input Low Voltage	-			0.3 x VDDA	V
TCLKI_J	CLKI frequency tolerance	-	-50		+50	ppm
TCLKI_ RISE_FALL	Rise and fall times at CLKI	25 MHz reference, 20% - 80%			4	ns
TCLKI_ RC_DUTY	CLKI duty cycle	20% - 80%	40		60	%

SATA Interface Timing Specifications

Table 9 shows the SATA interface timing specifications.

Table 9: SATA Interface Timing Specifications

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
TTX_RISE_FALL	Transmitter rise and fall time	20%-80% at Gen1 20%-80% at Gen2	85 67		273 136	ps
TTX_DC_FREQ	Tx DC Clock frequency skew		-350		+350	ppm
TTX_AC_RREQ	Tx AC Clock frequency skew	SerDes Ref_Clk = SSC AC Modulation	-5000		+0	ppm
TTX_SKEW	Tx Differential skew				15	ps

SATA Interface Transmitter Output Jitter Characteristics

Table 10 and
Table 11 show the SATA output jitter characteristics.

Table 10: SATA Interface Transmitter Output Jitter Characteristics (1.5 G)

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
TJ5UI_1.5 G	Total Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		58		ps
DJ5UI_1.5 G	Deterministic Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		15		ps
TJ250UI_1.5 G	Total Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		55		ps
DJ250UI_1.5 G	Deterministic Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		15		ps

Table 11: SATA Interface Transmitter Output Jitter Characteristics (3.0 G)

Symbol	Parameter	Condition	Type Limits			Units
			Minimum	Typical	Maximum	
TJfBAUD/ 10_3.0G	Total Jitter, fC3dB=fBAUD/10	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		63		ps
DJfBAUD/ 10_3.0G	Deterministic Jitter, fC3dB=fBAUD/10	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		16		ps
TJfBAUD/ 500_3.0G	Total Jitter, fC3dB=fBAUD/500	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		63		ps
DJfBAUD/ 500_3.0G	Deterministic Jitter, fC3dB=fBAUD/500	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		21		ps
TJfBAUD/ 1667_3.0G	Total Jitter, fC3dB=fBAUD/1667	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		86		ps
DJfBAUD/ 1667_3.0G	Deterministic Jitter, fC3dB=fBAUD/1667	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		20		ps

Pin Descriptions

Sil 3726 SATA Port Multiplier Pin-out

Table 12 and Table 13 list the Sil 3726 SATA Port Multiplier pin numbers, names, types, and descriptions. Table 12 is sorted by pin name, and Table 13 is sorted by pin number. Note that NC (No Connect pins) must not be connected to any circuitry on the PCB.

Table 12: Sil3726 Pin List (Sorted by Pin Name)

Pin Number	Pin Name	Type	Internal Resistor	Description
Y11	CONT_DIS	Input	Pull-Down (60 kΩ)	CONT disable in OOB bypass mode. Leave NC for normal operation. For details, see Tx Eye Measurement on page 9.
D16	DAIO0	Input	Pull-Down (60 kΩ)	Device0 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C15	DAIO1	Input	Pull-Down (60 kΩ)	Device0 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C11	DBIO0	Input	Pull-Down (60 kΩ)	Device1 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C10	DBIO1	Input	Pull-Down (60 kΩ)	Device1 interface optimization input bit. For details, see High Speed Serial Interface Optimization on page 9.
C9	DCIO0	Input	Pull-Down (60 kΩ)	Device2 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C8	DCIO1	Input	Pull-Down (60 kΩ)	Device2 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C7	DDIO0	Input	Pull-Down (60 kΩ)	Device3 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization. on page 9.
C6	DDIO1	Input	Pull-Down (60 kΩ)	Device3 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
B5	DEIO0	Input	Pull-Down (60 kΩ)	Device4 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
B6	DEIO1	Input	Pull-Down (60 kΩ)	Device4 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
A11	EM_ID0	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 0. This pin is used to set the Identification Number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
B11	EM_ID1	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 1.This pin is used to set the Identification Number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
B10	EM_ID2	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 2 This pin is used to set the Identification Number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
A12	EM_SC	I/O	Pull-Up (70 kΩ) 4 mA	Enclosure management serial clock. This pin is used to send/receive serial clock to/from Enclosure processor, and complies with I^2C Bus Specification. For details, see Storage Enclosure Support on page 11.
B12	EM_SD	I/O	Pull-Up (70 kΩ) 4 mA	Enclosure management serial data. This pin is used to send/receive serial data to/from Enclosure processor, and complies with I^2C Bus Specification. For details, see Storage Enclosure Support on page 11.

A9	EPR_SC	I/O	Pull-Up (70 kΩ) 4 mA	EEPROM serial clock. This pin is used to send serial clock to EEPROM having I^2C interface to download firmware from EEPROM. For details, see Firmware must be downloaded into the Sil 3726 SATA Port Multiplier from a Serial EEPROM for normal operation. The serial EEPROM is connected to pin numbers A9 (Serial Clock) and B9 (Serial Data). Auto-Initialization from the EEPROM on page 20.
B9	EPR_SD	I/O	Pull-Up (70 kΩ) 4 mA	EEPROM serial data. This pin is used to send/receive serial data to/from EEPROM having I2C interface to download firmware from EEPROM. For details, see Firmware must be downloaded into the Sil 3726 SATA Port Multiplier from a Serial EEPROM for normal operation. The serial EEPROM is connected to pin numbers A9 (Serial Clock) and B9 (Serial Data). Auto-Initialization from the EEPROM on page 20.
B3	GPI 31	Input	Pull-Down (60 kΩ)	GPI signal bit 31
W4	GPO 31	Output	8 mA	GPO signal bit 31
Y4	GPO 30	Output	8 mA	GPO signal bit 30
V5	GPO 21	Output	8 mA	GPO signal bit 21
V6	GPO 20	Output	8 mA	GPO signal bit 20
V7	GPO 19	Output	8 mA	GPO signal bit 19
V8	GPO 18	Output	8 mA	GPO signal bit 18
V9	GPO 17	Output	8 mA	GPO signal bit 17
V10	GPO 16	Output	8 mA	GPO signal bit 16
V11	GPO 15	Output	8 mA	GPO signal bit 15
V12	GPO 14	Output	8 mA	GPO signal bit 14
V13	GPO 13	Output	8 mA	GPO signal bit 13
V14	GPO 12	Output	8 mA	GPO signal bit 12
V15	GPO 11	Output	8 mA	GPO signal bit 11
V16	GPO 10	Output	8 mA	GPO signal bit 10
W17	GPO 1	Output	8 mA	GPO signal bit 1
Y17	GPO 0	Output	8 mA	GPO signal bit 0
C14	HIO0	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C13	HIO1	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C12	HIO2	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 2. For details, see High Speed Serial Interface Optimization on page 9.
Y16	LED_A0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port0 [0]. This pin indicates the status of device port0 together with LED_A1 pin. For details, see LED Modes on page 8.
W16	LED_A1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port0 [1]. This pin indicates the status of device port0 together with LED_A0 pin. For details, see LED Modes on page 8.
Y14	LED_B0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port1 [0]. This pin indicates the status of device port1 together with the LED_B1 pin. For details, see LED Modes on page 8.
W14	LED_B1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port1 [1]. This pin indicates the status of device port1 together with the LED_B0 pin. For details, see LED Modes on page 8.
Y7	LED_C0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port2 [0]. This pin indicates the status of device port2 together with the LED_C1 pin. For details, see LED Modes on page 8.
W7	LED_C1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port2 [1]. This pin indicates the status of device port2 together with the LED_C0 pin. For details, see LED Modes on page 8.

Y6	LED_D0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port3 [0]. This pin indicates the status of device port3 together with the LED_D1 pin. For details, see LED Modes on page 8.
W6	LED_D1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port3 [1]. This pin indicates the status of device port3 together with the LED_D0 pin. For details, see LED Modes on page 8.
Y5	LED_E0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port4 [0]. This pin indicates the status of device port4 together with the LED_E1 pin. For details, see LED Modes on page 8.
W5	LED_E1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port4 [1]. This pin indicates the status of device port4 together with the LED_E0 pin. For details, see LED Modes on page 8.
Y15	LED_H0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED host port [0] This pin, together with the LED_H1 pin, indicates the status of the host port. For details, see LED Modes on page 8.
W15	LED_H1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED host port [1]. This pin indicates the status of host port together with the LED_H0 pin. For details, see LED Modes on page 8.
A3	LED_MODE	Input	Pull-Down (60 kΩ)	Select LED mode. For details, see LED Modes on page 8.
Y13	LED_S0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [0]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
W13	LED_S1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [1]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
Y8	LED_S2	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [2]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
W8	LED_S3	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [3]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
A13	NC	-	-	Do not connect to any circuitry
A14	NC	-	-	Do not connect to any circuitry
A15	NC	-	-	Do not connect to any circuitry
A16	NC	-	-	Do not connect to any circuitry
A17	NC	-	-	Do not connect to any circuitry
A4	NC	-	-	Do not connect to any circuitry
B13	NC	-	-	Do not connect to any circuitry
B14	NC	-	-	Do not connect to any circuitry
B15	NC	-	-	Do not connect to any circuitry
B16	NC	-	-	Do not connect to any circuitry
B17	NC	-	-	Do not connect to any circuitry
B4	NC	-	-	Do not connect to any circuitry
H18	NC	-	-	Do not connect to any circuitry
H19	NC	-	-	Do not connect to any circuitry
J18	NC	-	-	Do not connect to any circuitry
K16	NC	-	-	Do not connect to any circuitry
M1	NC	-	-	Do not connect to any circuitry
M3	NC	-	-	Do not connect to any circuitry
M5	NC	-	-	Do not connect to any circuitry
N1	NC	-	-	Do not connect to any circuitry
N2	NC	-	-	Do not connect to any circuitry

N3	NC	-	-	Do not connect to any circuitry
W10	NC	-	-	Do not connect to any circuitry
W11	NC	-	-	Do not connect to any circuitry
W9	NC	-	-	Do not connect to any circuitry
Y10	NC	-	-	Do not connect to any circuitry
Y9	NC	-	-	Do not connect to any circuitry
Y12	OOB_BP	Input	Pull-Down (60 kΩ)	OOB Bypass mode. Leave NC for normal operation. For details, see Tx Eye Measurement on page 9.
J20	PCLKI1	Input	-	Crystal oscillator Input or external clock input (25 MHz crystal)
H20	PCLKO1	Output	-	Crystal oscillator output (25 MHz crystal)
J19	RREF1	Input	-	External reference resistor input, 1 kΩ 1% resistor needs to be connected.
M2	RREF2	Input	-	External Reference Resistor Input, 4.99 kΩ,, 1% resistor needs to be connected
A10	RST_N	Input-Schmitt Trigger	-	System Reset. This pin is used to reset the Sil 3726.
U19	RXNDA	Input	-	Serial device port0 differential receiver – input. Must be AC coupled.
F19	RXNDB	Input	-	Serial device port1 differential receiver – input. Must be AC coupled..
D2	RXNDC	Input	-	Serial device port2 differential receiver – input. Must be AC coupled..
H2	RXNDD	Input	-	Serial device port3 differential receiver – input. Must be AC coupled..
R2	RXNDE	Input	-	Serial device port4 differential receiver – input. Must be AC coupled.
L20	RXNH	Input	-	Serial host port differential receiver – input. Must be AC coupled.
U20	RXPDA	Input	-	Serial device port0 differential receiver + input. Must be AC coupled.
F20	RXPDB	Input	-	Serial device port1 differential receiver + input. Must be AC coupled.
D1	RXPDC	Input	-	Serial device port2 differential receiver + input. Must be AC coupled.
H1	RXPDD	Input	-	Serial device port3 differential receiver + input. Must be AC coupled.
R1	RXPDE	Input	-	Serial device port4 differential receiver + input. Must be AC coupled.
L19	RXPH	Input	-	Serial HOST port differential receiver + input. Must be AC coupled.
A8	TCK	Input	Pull-Up (70 kΩ)	JTAG clock
B8	TDI	Input	Pull-Up (70 kΩ)	JTAG data Input
A7	TDO	Output	-	JTAG data output
B7	TMS	Input	Pull-Up (70 kΩ)	JTAG mode select
A6	TRSTN	Input	Pull-Up (70 kΩ)	JTAG reset. This pin must be tied to ground if the JTAG function is not used.
W12	TX_GEN	-	Pull-Down (60 kΩ)	Tx generation rate in OOB Bypass mode. Leave NC for normal operation mode. For details, see Tx Eye Measurement on page 9.
R20	TXNDA	Output	-	Serial device port0 differential transmitter – output. Must be AC coupled.
D20	TXNDB	Output	-	Serial device port1 differential transmitter – output. Must be AC coupled.
F1	TXNDC	Output	-	Serial device port2 differential transmitter – output. Must be AC coupled.

K1	TXNDD	Output	-	Serial device port3 differential transmitter – output. Must be AC coupled.
U1	TXNDE	Output	-	Serial device port4 differential transmitter – output. Must be AC coupled.
N19	TXNH	Output	-	Serial HOST port differential transmitter – output. Must be AC coupled.
R19	TXPDA	Output	-	Serial device port0 differential transmitter + output. Must be AC coupled.
D19	TXPDB	Output	-	Serial device port1 differential transmitter + output. Must be AC coupled.
F2	TXPDC	Output	-	Serial device port2 differential transmitter + output. Must be AC coupled.
K2	TXPDD	Output	-	Serial device port3 differential transmitter + output. Must be AC coupled.
U2	TXPDE	Output	-	Serial device port4 differential transmitter + output. Must be AC coupled.
N20	TXPH	Output	-	Serial host port differential transmitter + output. Must be AC coupled.

Table 13: SiI3726 Pin List (Sorted by Pin Number)

Pin Number	Pin Name	Type	Internal Resistor	Description
A3	LED_MODE	Input	Pull-Down (60 kΩ)	Select LED mode. For details, see LED Modes on page 8.
A4	NC	-	-	Do not connect to any circuitry
A5	GPI 26	Input	Pull-Down (60 kΩ)	GPI signal bit 26
A6	TRSTN	Input	Pull-Up (70 kΩ)	JTAG reset. This pin must be tied to ground if the JTAG function is not used.
A7	TDO	Output	-	JTAG data output
A8	TCK	Input	Pull-Up (70 kΩ)	JTAG clock
A9	EPR_SC	I/O	Pull-Up (70 kΩ) 4 mA	EEPROM serial clock. This pin is used to send serial clock to EEPROM having I^2C interface to download firmware from EEPROM. For details, see Firmware must be downloaded into the SiI 3726 SATA Port Multiplier from a Serial EEPROM for normal operation. The serial EEPROM is connected to pin numbers A9 (Serial Clock) and B9 (Serial Data). Auto-Initialization from the EEPROM on page 20.
A10	RST_N	Input-Schmitt Trigger	-	System Reset. This pin is used to reset SiI 3726
A11	EM_ID0	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 0. This pin is used to set the identification number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
A12	EM_SC	I/O	Pull-Up (70 kΩ) 4 mA	Enclosure management serial clock. This pin is used to send/receive serial clock to/from Enclosure processor, and complies with I^2C Bus Specification. For details, see Storage Enclosure Support on page 11.
A13	NC	-	-	Do not connect to any circuitry
A14	NC	-	-	Do not connect to any circuitry
A15	NC	-	-	Do not connect to any circuitry
A16	NC	-	-	Do not connect to any circuitry
A17	NC	-	-	Do not connect to any circuitry

A18	GPI 0	Input	Pull-Down (60 kΩ)	GPI signal bit 0
B3	GPI 31	Input	Pull-Down (60 kΩ)	GPI signal bit 31
B4	NC	-	-	Do not connect to any circuitry
B5	DEIO0	Input	Pull-Down (60 kΩ)	Device4 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
B6	DEIO1	Input	Pull-Down (60 kΩ)	Device4 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
B7	TMS	Input	Pull-Up (70 kΩ)	JTAG mode select
B8	TDI	Input	Pull-Up (70 kΩ)	JTAG data input
B9	EPR_SD	I/O	Pull-Up (70 kΩ) 4 mA	EEPROM serial data. This pin is used to send/receive serial data to/from EEPROM having I^2C interface to download firmware from EEPROM. For details, see Firmware must be downloaded into the SiI 3726 SATA Port Multiplier from a Serial EEPROM for normal operation. The serial EEPROM is connected to pin numbers A9 (Serial Clock) and B9 (Serial Data). Auto-Initialization from the EEPROM on page 20.
B10	EM_ID2	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 2. This pin is used to set the Identification Number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
B11	EM_ID1	Input	Pull-Down (60 kΩ)	Enclosure management ID input bit 1. This pin is used to This pin is used to set the Identification Number together with other EM_ID pins for SEMB. For details, see Storage Enclosure Support on page 11.
B12	EM_SD	I/O	Pull-Up (70 kΩ) 4 mA	Enclosure management serial data. This pin is used to send/receive serial data to/from Enclosure processor, and complies with I^2C Bus Specification. For details, see Storage Enclosure Support on page 11.
B13	NC	-	-	Do not connect to any circuitry
B14	NC	-	-	Do not connect to any circuitry
B15	NC	-	-	Do not connect to any circuitry
B16	NC	-	-	Do not connect to any circuitry
B17	NC	-	-	Do not connect to any circuitry
B18	GPI 1	Input	Pull-Down (60 kΩ)	GPI signal Bit 1
C5	GPI 28	Input	Pull-Down (60 kΩ)	GPI signal Bit 28
C6	DDIO1	Input	Pull-Down (60 kΩ)	Device3 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C7	DDIO0	Input	Pull-Down (60 kΩ)	Device3 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C8	DCIO1	Input	Pull-Down (60 kΩ)	Device2 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C9	DCIO0	Input	Pull-Down (60 kΩ)	Device2 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
C10	DBIO1	Input	Pull-Down (60 kΩ)	Device2 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C11	DBIO0	Input	Pull-Down (60 kΩ)	Device1 interface optimization input bit. For details, see High Speed Serial Interface Optimization on page 9.
C12	HIO2	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 2. For details, see High Speed Serial Interface Optimization on page 9.
C13	HIO1	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9..

C14	HIO0	Input	Pull-Down (60 kΩ)	Host interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9..
C15	DAIO1	Input	Pull-Down (60 kΩ)	Device0 interface optimization input bit 1. For details, see High Speed Serial Interface Optimization on page 9.
C16	GPI 13	Input	Pull-Down (60 kΩ)	GPI signal Bit 13
D1	RXPDC	Input	-	Serial device port2 differential receiver + input. Must be AC coupled.
D2	RXNDC	Input	-	Serial device port2 differential receiver + input. Must be AC coupled.
D5	GPI 29	Input	Pull-Down (60 kΩ)	GPI signal Bit 29
D16	DAIO0	Input	Pull-Down (60 kΩ)	Device0 interface optimization input bit 0. For details, see High Speed Serial Interface Optimization on page 9.
D19	TXPDB	Output	-	Serial device port1differential transmitter + output. Must be AC coupled.
D20	TXNDB	Output	-	Serial device port1 differential transmitter – output. Must be AC coupled.
F1	TXNDC	Output	-	Serial device port2 differential transmitter – output. Must be AC coupled.
F2	TXPDC	Output	-	Serial device port2 differential transmitter + output. Must be AC coupled.
F19	RXNDB	Input	-	Serial device port1 differential receiver – input. Must be AC coupled.
F20	RXPDB	Input	-	Serial device port1 differential receiver + input. Must be AC coupled.
H1	RXPDD	Input	-	Serial device port3 differential receiver + input. Must be AC coupled.
H2	RXNDD	Input	-	Serial device port3 differential receiver + input. Must be AC coupled.
H18	NC	-	-	Do not connect to any circuitry
H19	NC	-	-	Do not connect to any circuitry
H20	PCLKO1	Output	-	Crystal oscillator output (25 MHz crystal)
J18	NC	-	-	Do not connect to any circuitry
J19	RREF1	Input	-	External reference resistor input. 1 kΩ 1% resistor needs to be connected.
J20	PCLKI1	Input	-	Crystal oscillator Input or external clock input (25 MHz crystal)
K1	TXNDD	Output	-	Serial device port3 differential transmitter – output. Must be AC coupled.
K2	TXPDD	Output	-	Serial device port3 differential transmitter – output. Must be AC coupled.
K16	NC	-	-	Do not connect to any circuitry
L19	RXPH	Input	-	Serial host port differential receiver + input. Must be AC coupled.
L20	RXNH	Input	-	Serial host port differential receiver + input. Must be AC coupled.
M1	NC	-	-	Do not connect to any circuitry
M2	RREF2	Input	-	External reference resistor input. 4.99 kΩ 1% resistor needs to be connected
M3	NC	-	-	Do not connect to any circuitry
M5	NC	-	-	Do not connect to any circuitry
N1	NC	-	-	Do not connect to any circuitry

N2	NC	-	-	Do not connect to any circuitry
N3	NC	-	-	Do not connect to any circuitry
N19	TXNH	Output	-	Serial host port differential transmitter – output. Must be AC coupled.
N20	TXPH	Output	-	Serial host port differential transmitter + output. Must be AC coupled.
R1	RXPDE	Input	-	Serial device port4 differential receiver + input. Must be AC coupled.
R2	RXNDE	Input	-	Serial device port4 differential receiver – input. Must be AC coupled.
R19	TXPDA	Output	-	Serial device port0 differential transmitter + output. Must be AC coupled.
R20	TXNDA	Output	-	Serial device port0 differential transmitter – output. Must be AC coupled.
U1	TXNDE	Output	-	Serial device port4 differential transmitter – output. Must be AC coupled.
U2	TXPDE	Output	-	Serial device port4 differential transmitter + output. Must be AC coupled.
U19	RXNDA	Input	-	Serial device port0 differential receiver – input. Must be AC coupled.
U20	RXPDA	Input	-	Serial device port0 differential receiver + input. Must be AC coupled.
V5	GPO 21	Output	8 mA	GPO signal bit 21
V6	GPO 20	Output	8 mA	GPO signal bit 20
V7	GPO 19	Output	8 mA	GPO signal bit 19
V8	GPO 18	Output	8 mA	GPO signal bit 18
V9	GPO 17	Output	8 mA	GPO signal bit 17
V10	GPO 16	Output	8 mA	GPO signal bit 16
V11	GPO 15	Output	8 mA	GPO signal bit 15
V12	GPO 14	Output	8 mA	GPO signal bit 14
V13	GPO 13	Output	8 mA	GPO signal bit 13
V14	GPO 12	Output	8 mA	GPO signal bit 12
V15	GPO 11	Output	8 mA	GPO signal bit 11
V16	GPO 10	Output	8 mA	GPO signal bit 10
W4	GPO 31	Output	8 mA	GPO signal bit 31
W5	LED_E1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port4 [1]. This pin indicates the status of device port4 together with LED_E0 pin. For details, see LED Modes on page 8.
W6	LED_D1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port3 [1]. This pin indicates the status of device port3 together with LED_D0 pin. For details, see LED Modes on page 8.
W7	LED_C1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port2 [1]. This pin indicates the status of device port2 together with LED_C0 pin. For details, see LED Modes on page 8.
W8	LED_S3	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [3]. This pin indicates the status of firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
W9	NC	-	-	Do not connect to any circuitry
W10	NC	-	-	Do not connect to any circuitry

W11	NC	-	-	Do not connect to any circuitry
W12	TX_GEN	-	Pull-Down (60 kΩ)	Tx generation rate in OOB Bypass mode. Leave NC for normal operation mode. For details, see Tx Eye Measurement on page 9.
W13	LED_S1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [1]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
W14	LED_B1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port1 [1]. This pin indicates the status of device port1 together with LED_B0 pin. For details, see LED Modes on page 8.
W15	LED_H1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED host port [1]. This pin indicates the status of host port together with LED_H0 pin. For details, see LED Modes on page 8.
W16	LED_A1	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port0 [1]. This pin indicates the status of device port0 together with LED_A0 pin. For details, see LED Modes on page 8.
W17	GPO 1	Output	8 mA	GPO signal bit 1
Y4	GPO 30	Output	8 mA	GPO signal bit 30
Y5	LED_E0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port4 [0]. This pin indicates the status of device port4 together with LED_E1 pin. For details, see LED Modes on page 8.
Y6	LED_D0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port3 [0]. This pin indicates the status of device port3 together with LED_D1 pin. For details, see LED Modes on page 8.
Y7	LED_C0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port2 [0]. This pin indicates the status of device port #2 together with LED_C1 pin. For details, see LED Modes on page 8.
Y8	LED_S2	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [2]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
Y9	NC	-	-	Do not connect to any circuitry
Y10	NC	-	-	Do not connect to any circuitry
Y11	CONT_DIS	Input	Pull-Down (60 kΩ)	CONT disable in OOB bypass mode. Leave NC for normal operation. For details, see Tx Eye Measurement on page 9.
Y12	OOB_BP	Input	Pull-Down (60 kΩ)	OOB bypass mode. Leave NC for normal operation. For details, see Tx Eye Measurement on page 9.
Y13	LED_S0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	System LED [0]. This pin indicates the status of the firmware loading during boot-up, and the system after then together with other LED_S pins. For details, see LED Modes on page 8.
Y14	LED_B0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port1 [0]. This pin indicates the status of device port1 together with LED_B1 pin. For details, see LED Modes on page 8.
Y15	LED_H0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED host port [0]. This pin indicates the status of HOST port together with LED_H1 pin. For details, see LED Modes on page 8.
Y16	LED_A0	Output-Open Drain	Pull-Up (70 kΩ) 12 mA	LED device port0 [0]. This pin indicates the status of device port0 together with LED_A1 pin. For details, see LED Modes on page 8.
Y17	GPO 0	Output	8 mA	GPO signal bit 0

Table 14: Power Supply Pin List

Pin Number	Pin Name	Type	Description
A1, B2, C1, C3, D4, E1, E3, F4, G1, G3, H5	VDD RX3	Power	VDD (1.8V) for SATA PHY Receiver3
H4, J1, J3, K4, K5, L1, L3	VDD TX3	Power	VDD (1.8V) for SATA PHY Transmitter3
N4, N5, P1, P3	VDD P2	Power	VDD (1.8V) for SATA PHY PLL2
P5, R4, T1, T3, U4, V1	VDD RX4	Power	VDD (1.8V) for SATA PHY Receiver4
V3, W2, Y1, Y3	VDD TX4	Power	VDD (1.8V) for SATA PHY Transmitter4
D6, D10, D11, D15, E5, E6, E10, E11, E15, E16, F5, T5, T6, T7, T14, T15, T16, U5, U6, U7, U14, U15, U16	3V3DDO	Power	VDD I/O (3.3V)
D7, D8, D9, D12, D13, D14, E7, E8, E9, E12, E13, E14, T8, T9, T10, T11, T12, T13, U8, U9, U10, U11, U12, U13	VDDD	Power	VDD (1.8V)
P16, P18, P20, R17, T18, T20, U17, V18, V20, W19, Y18, Y20	VDD RX1	Power	VDD (1.8V) for SATA PHY Receiver1
K18, K20, L17, M16, M18, M20, N17	VDD TX1	Power	VDD (1.8V) for SATA PHY Transmitter1
G18, G20, H17, J16	VDD P1	Power	VDD (1.8V) for SATA PHY PLL1
D17, E18, E20, F17, G16	VDD RX2	Power	VDD (1.8V) for SATA PHY Receiver2
A20, B19, C18, C20	VDD TX2	Power	VDD (1.8V) for SATA PHY Transmitter2

Package Pin Descriptions

Pin Descriptions

Figure 8 shows the Pin-Diagram for the 21 mm x 21 mm BGA with a 20 x 20 array of Balls.

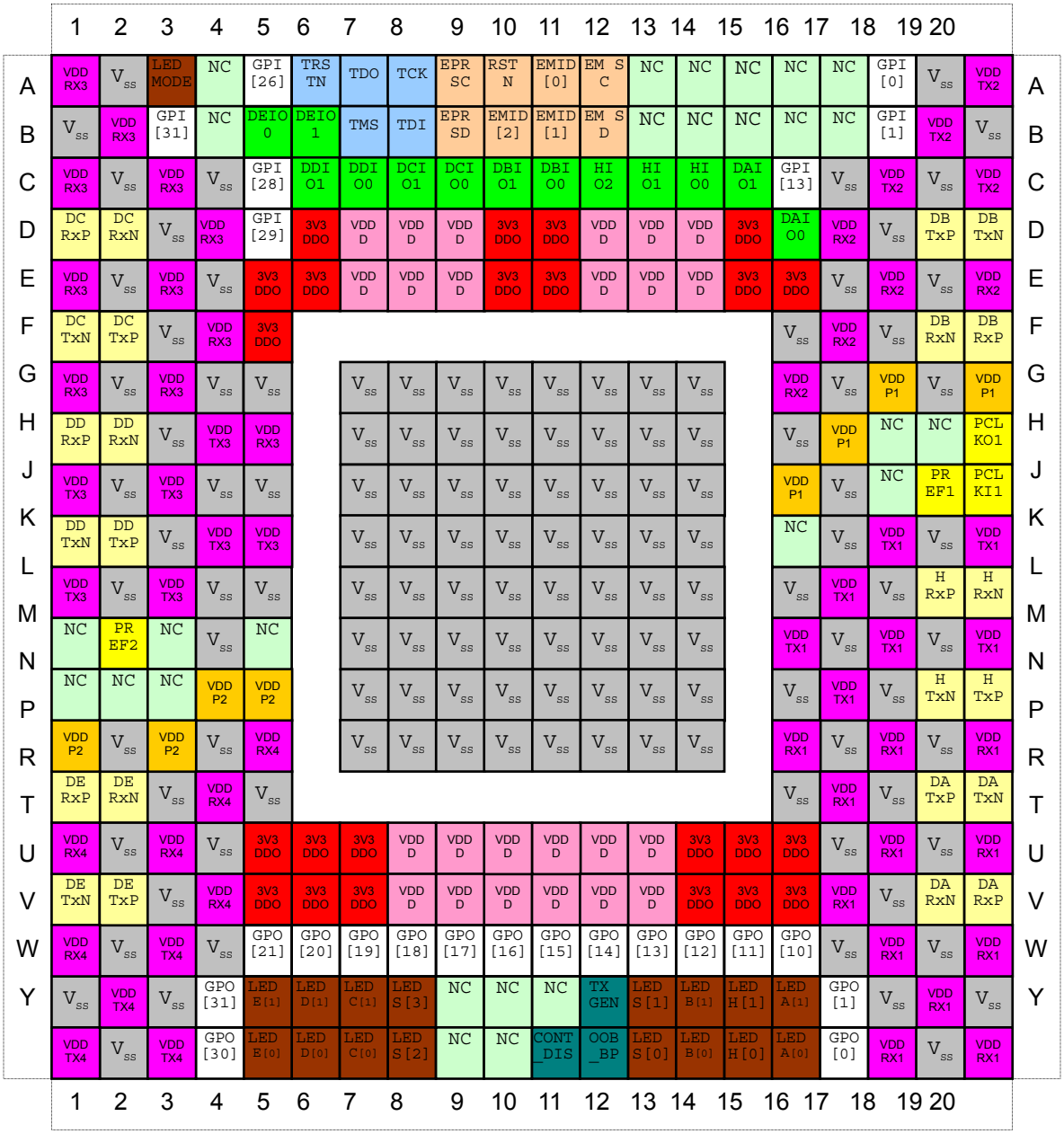

Figure 8: Sil3726 Pinout Diagram

Package Information

Dimensions

Figure 9 shows the dimensions of the 364-Ball HSBGA package.

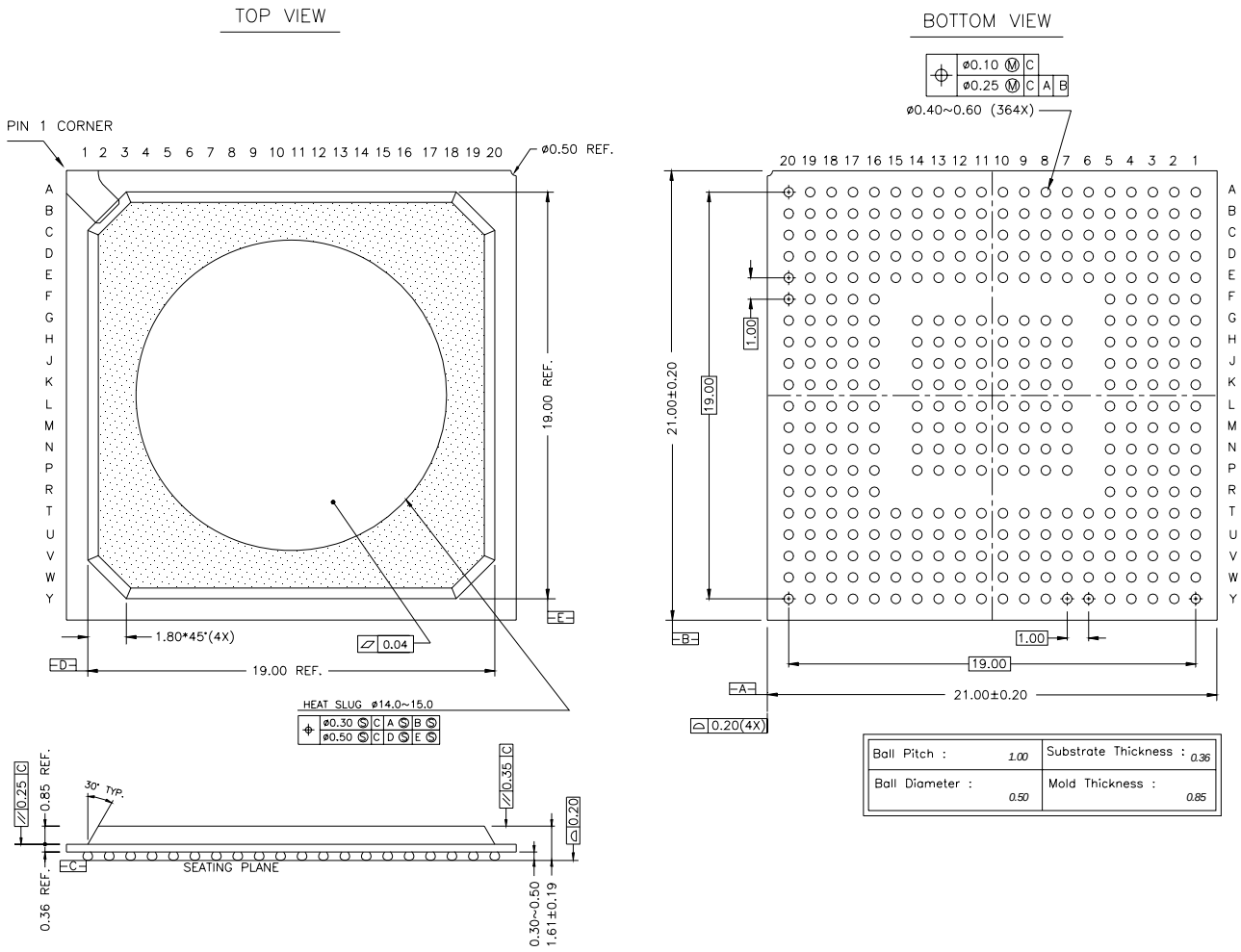

Figure 9: 364 Ball HSBGA Package Dimensions (in Millimeters)

Part Ordering Numbers:

- SiI3726CB (364-pin BGA, standard package) shown in Figure 10.
- SiI3726CBHU (364-pin BGA, green package) shown in Figure 11.

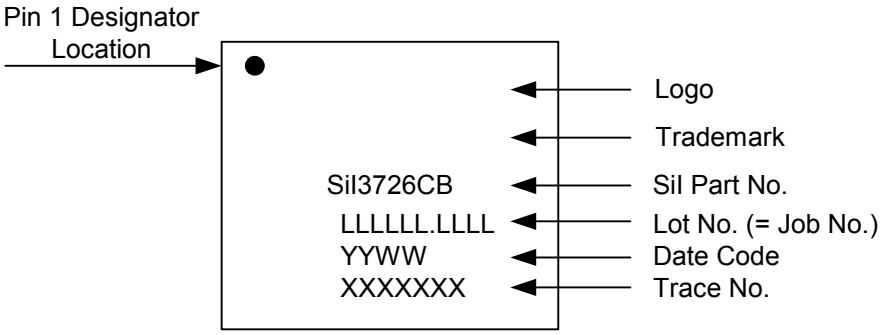

Figure 10: Marking Specification - SiI3726CB

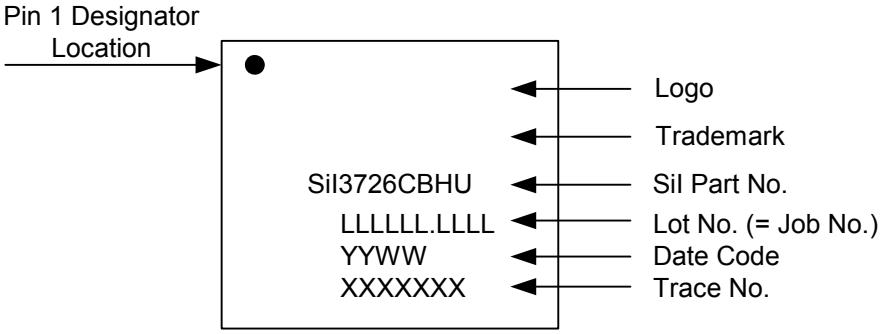

Figure 11: Marking Specification - SiI3726CBHU

References

For more details about Serial ATA technology, refer to the following industry specifications:

- Serial ATA /High Speed AT Attachment Specification, Revision 1.0a
- Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.2
- Serial ATA II: Port Multiplier, Revision 1.1 and Revision 1.2 Release Candidate
- Serial ATA II: Electrical Specification, Revision 1.0
- Serial ATA II: Cables and Connectors, Volumes 1 and 2

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