SONY

Semiconductor IC

Data Book 1991

Radio Communication System ICs

SONY Radio Communication System ICs 1991

SONY®

Semiconductor Integrated Circuit Data Book 1991

List of Model Names/ Index by Usage 1

Description 2

FM IF Amplifier 3

MODEM ICs 4

PLL ICs 5

GaAs MES FET 6

Semiconductor Integrated Circuit Data Book 1991

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PREFACE

This is the 1991 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

Sony Semiconductor Data Books

The following data books are available for the respective products applications.

1. TVs
2. Videos
3. CCD Cameras & Peripherals
4. Compact Discplayers
5. Analog Audio
6. Floppy Disk/Hard Disk Drive ICs
7. Radio Communication System ICs
8. A/D, D/A Converters
9. SPECL Standard Logic
10. Microcomputers
11. Microprocessors
12. Memories
13. Discrete Semiconductors

In addition, a List of Semiconductor Products covering all manufacutured device on the market, is issued twice a year.

Data books offer information pertaining to the listed products.

Contents

Page

1. List of Model Names 6

2. Index by Usage 7

3. IC Nomenclature 10

4. Precautions for IC Application 12
   1) Absolute maximum ratings 12
   2) Protection against electrostatic breakdown 13
   3) Mounting method 17

5. Quality Assurance and Reliability 19

6. Data Sheets 25
   1) FM IF Amplifier 25
   2) MODEM ICs 111
   3) PLL ICs 175
   4) GaAs MES FET 221

1. List of Model Names

Type	Page	Type	Page	Type	Page
CX-7925B/B-1 CXD1225M/M-1	177	CXA1356M/N	211	CXD1231Q-Z	147
CX-7961A/A-1	188	CXA1402M/N	35	CXD1233M	166
CXA1002M/N	27	CXA1474M/N	103	CXD1237Q/R	129
CXA1003BM/BN	38	CXA1484M/N	107	CXD1270Q/R	155
CXA1183M	71	CXA1493M/N	84	3SK165	223
CXA1184M/N	88	CXA1541M	219	3SK166	227
CXA1293M/N	51	CXD1118M/M-1	199	SGM2004M	231
CXA1343M/N	58	CXD1230M	113	SGM2006M/P	235

2. Index by Usage

1) FM IF Amplifier

Type	Function	Page
CXA1002M/N	FM IF amplifier for cellular radio for 2nd IF I_{CC}=2.5mA CXA1002N : VSOP package	27
CXA1402M/N	FM IF amplifier for cellular radio for 2nd IF I_{CC}=1.5mA CXA1002M/N pin compatible (NEW)	35
CXA1003BM/BN	FM IF amplifier for cellular radio for 2nd MIX I_{CC}=5.7mA CXA1003BN : VSOP package	38
CXA1293M/N	FM IF amplifier for cellular pin replaceable with CXA1003BM/BN I_{CC}=3.0mA CXA1293N : VSOP package (NEW)	51
CXA1343M/N	FM IF amplifier for cellular built in gain control amplifier and RSSI output buffer	58
CXA1183M	FM IF amplifier for cordless phone built in JAM detect circuit	71
CXA1493M/N	FM IF amplifier for cordless phone built in detect output LPF and highly efficient RSSI function ☆	84
CXA1184M/N	FM IF amplifier for double conversion pocket pager	88
CXA1474M/N	FM IF amplifier for single conversion pocket pager I_{CC}=500μA 16P VSOP package (NEW)	103
CXA1484M/N	FM IF amplifier for double conversion pocket pager 20P VSOP package I_{CC}=1.4mA (NEW)	107

☆: Under development
(New): New device

2) MODEM ICs

Type	Function	Page
CXD1230M	DATA SCF IC for AMPS/TACS cellular radio	113
CXD1237Q/R	1 chip SCF for AMPS/TACS/DOC cellular radio (NEW)	129
CXD1231Q-Z	MODEM LSI for AMPS/TACS cellular radio	147
CXD1270Q/R	MODEM LSI for AMPS/TACS cellular radio built in DTMF (NEW)	155
CXD1233M	MODEM LSI for cordless phone	166

(New): New device

3) PLL ICs

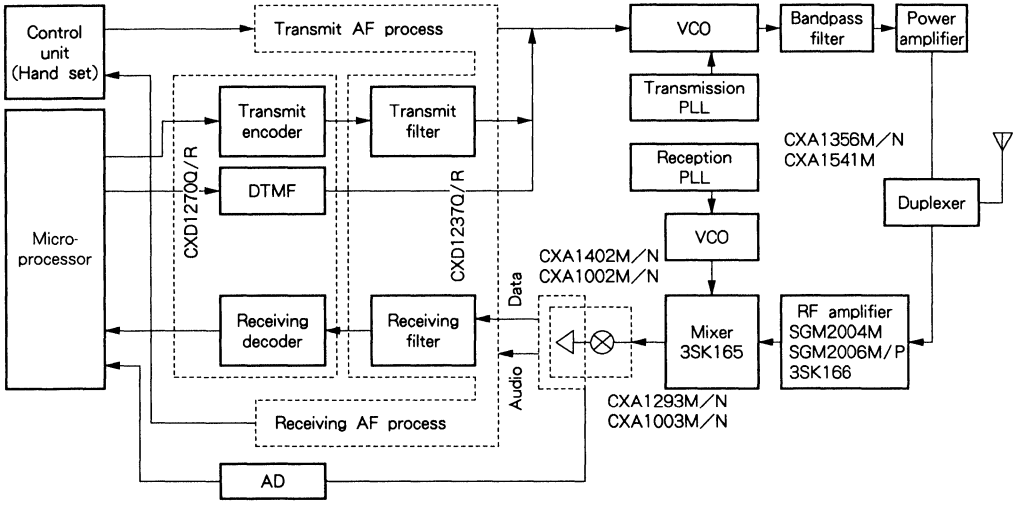
Type	Function	Page
CX-7925B/B-1 CXD1225M/M-1	1 chip PLL IC for low power cordless phone in Japan f_{MAX}=382MHz CXD1225M/M-1 is CX-7925B's SOP package version	177
CX-7961A/A-1	1 chip PLL IC for low power cordless phone in Japan f_{MAX}=255MHz	188
CXD1118M/M-1	CX-7961A's SOP package version	199
CXA1356M/N	1.5GHz synthesizer PLL for cellular equipment 16P VSOP package (NEW)	211
CXA1541M	1.2GHz dual mudulus prescaler for cellular equipment I_{CC}=3.5mA MB501 pin compatible ☆	219

☆: Under development
(New): New device

4) GaAs MES FET

Type	Function	Page
3SK165	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	223
3SK166	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	227
SGM2004M	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	231
SGM2006M/P	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	235

■ Cellular System Block Diagram



Note) DTMF (Dual Tone Multi Frequency)

3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] CX20011A

- Improvement mark
  "A" is affixed when specifications are partially improved.
- Product number
  Identifies individual product.
- Category number
  Indicates the product category in one or two digits.
  Bipolar IC: 0, 1, 8, 10, 20, 22
  MOS IC: 5, 7, 23, 79
- Sony IC mark

b) New nomenclature

[Example] CXA1001AP

- Package mark
  P: Plastic Dual In-line Package
  D: Ceramic Dual In-line Package
  M: Small Outline L-Leaded Package
  L: Single In-line Package
  Q: Quad Flat L-Leaded Package
  S: Shrink Dual In-line Package
  N: Very Small Outline Package (SSOP)
  R: Very Small Quad Flat Package
- Improvement mark
  "A" is affixed when specifications are improved.
- Product number
  Identifies the individual product.
- Product category mark
  A: Bipolar IC
  B: Bipolar digital IC
  D: MOS logic IC
  K: Memory, Mask ROM
  P, Q: Microcomputer, Microprocessor
  L: CCD signal processor
- Sony IC mark

c) Nomenclature of field effect transistors

No.1	No.2	No.3	No.4	No.5
(Figure)	(Letter)	(Letter)	(Figure)	(Letter)

The No.1 figure denotes the type of semiconductor device.

The device's number of effective electrical connections minus one is used for this number (n-1).

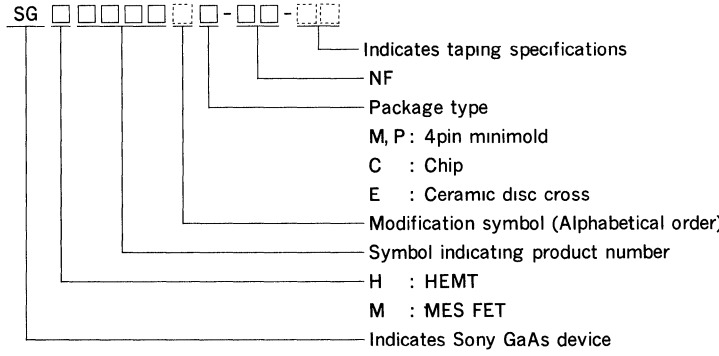
The No.2 letter shows the symbol "S" representing semiconductor device's registered with the Electronic Industries Association of Japan (EIAJ).

The No.3 letter shows the polarity and application of the semiconductor device. For example, "K" indicates an N-Channel FET.

The No.4 figure represents a sequential number registered with the Electronic Industries Association of Japan for each of the preceding types (No.1 figure, No.2 and No.3 letters).

The No.5 letter changes in A, B, C, ... alphabet order every are modified for improvement.

d) Nomenclature of GaAs discrete devices



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (VDD)

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation PD

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

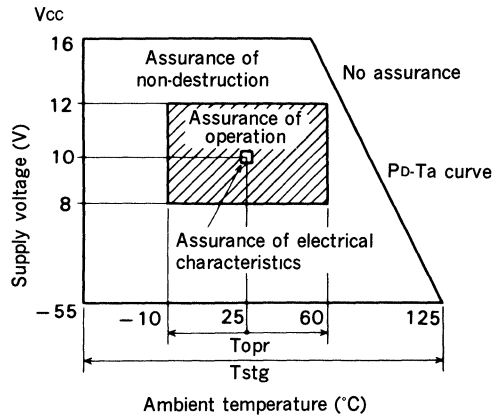
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

A general example on the relation with Absolute Maxium Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

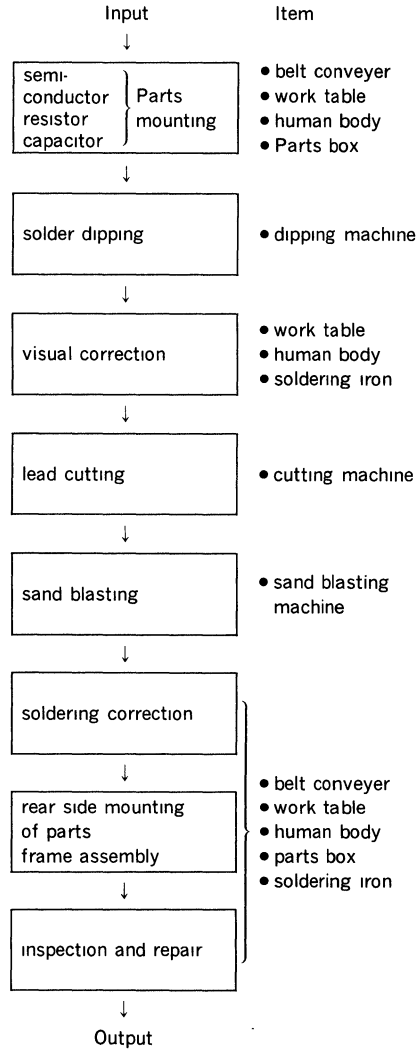
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.

One method is keeping relative humidity in the work room to about 50%.

Operator

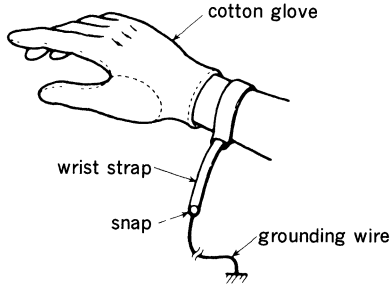
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

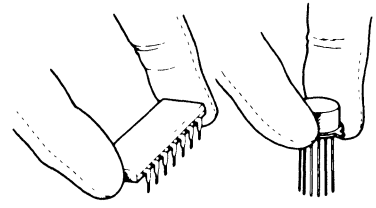


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

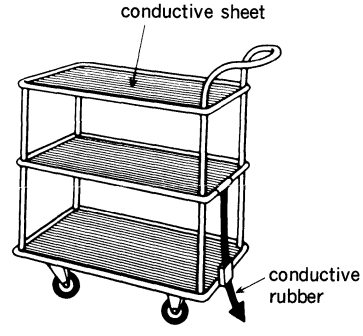
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

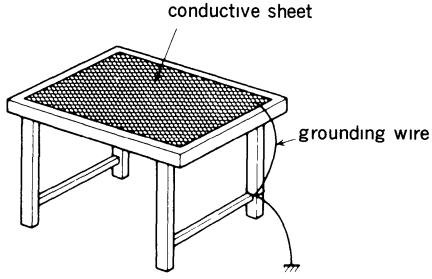
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

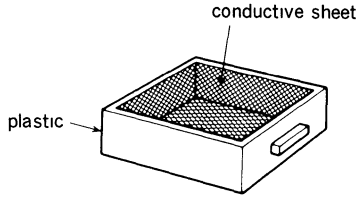
grounding of work table



(3) Semiconductor device case

Use a conductive case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

(5) Other points of caution

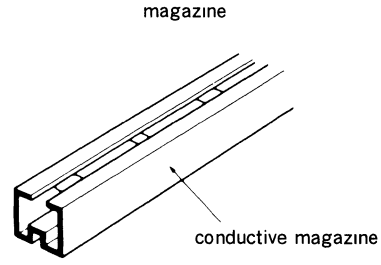
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

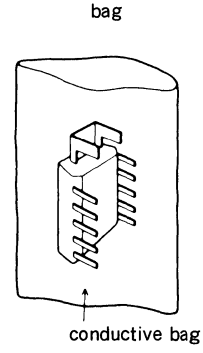
Use conductive, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

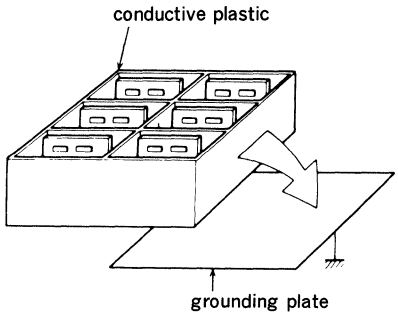
Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



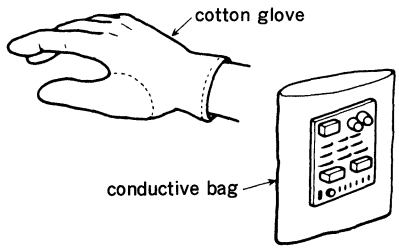
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

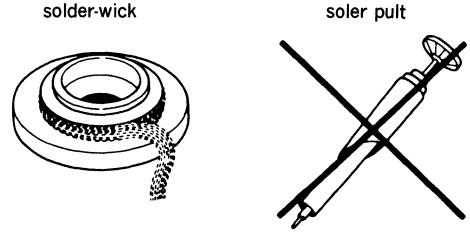
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table for soldering. Do not solder on foam styrol, vinyl, or melamine resin.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

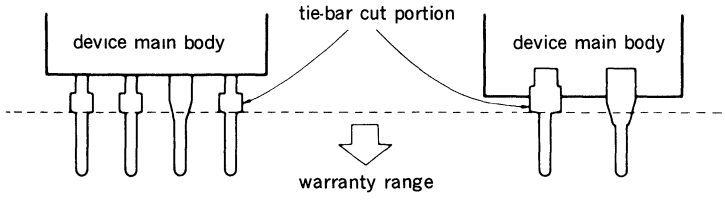
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

  For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.
- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

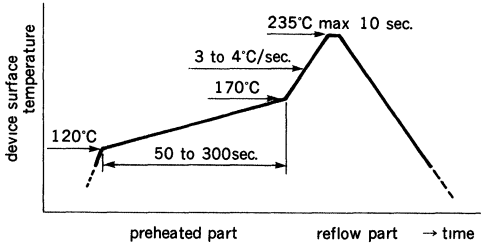
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

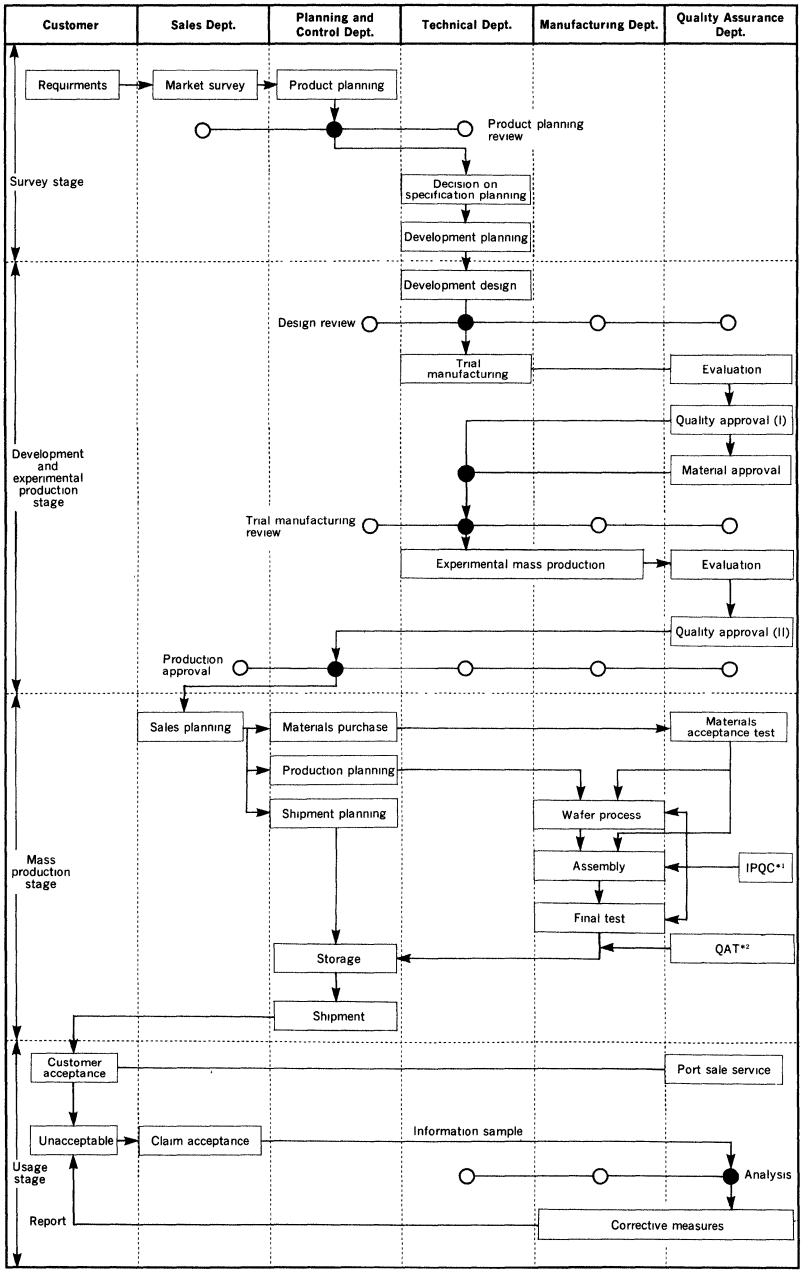
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1 IPQC In Process Quality Control
*2 QAT Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

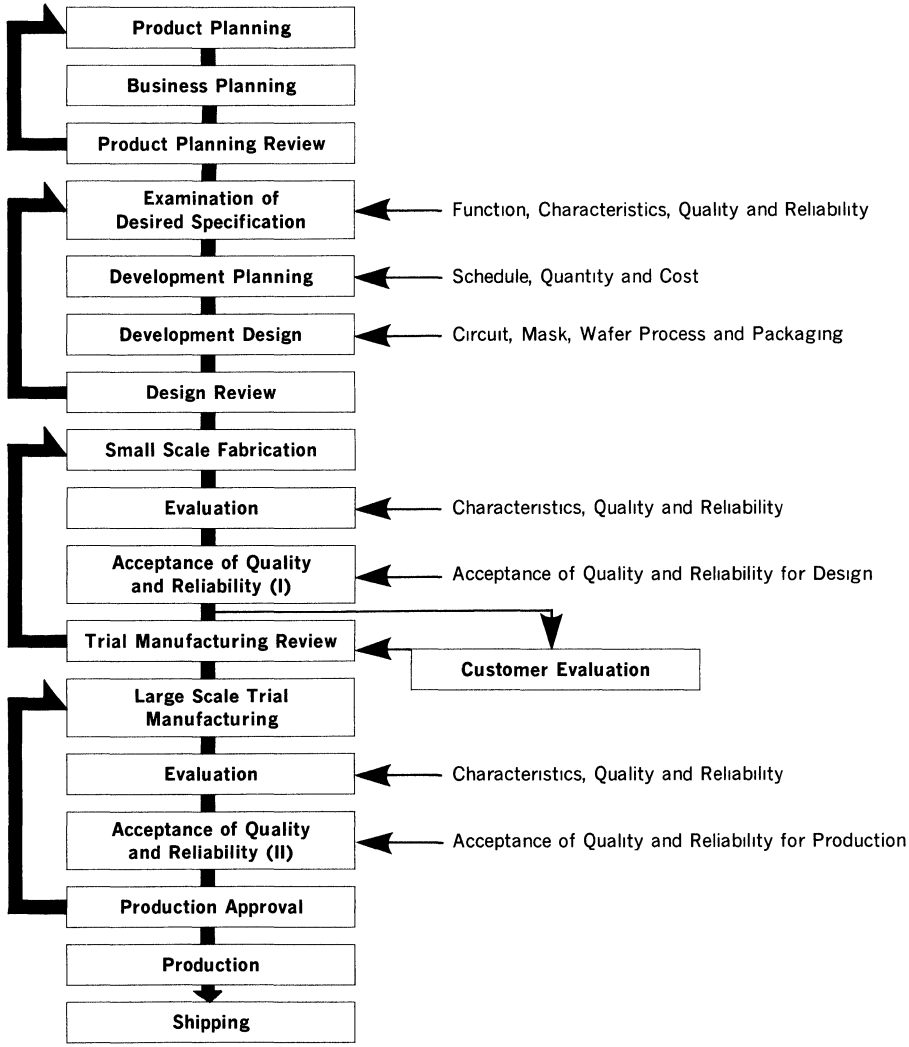
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

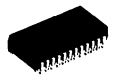
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

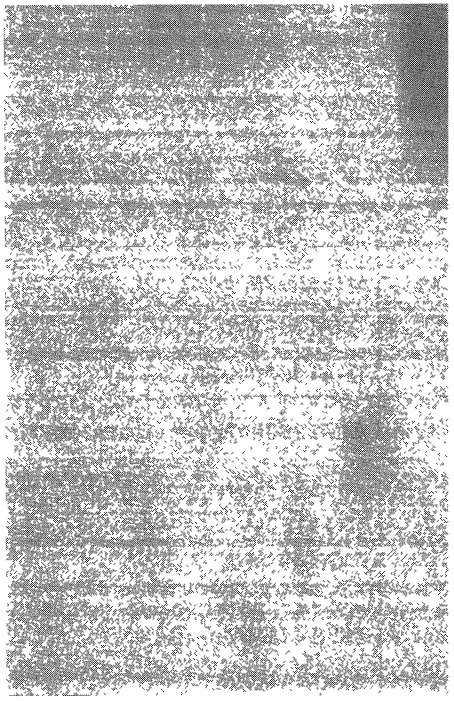
Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



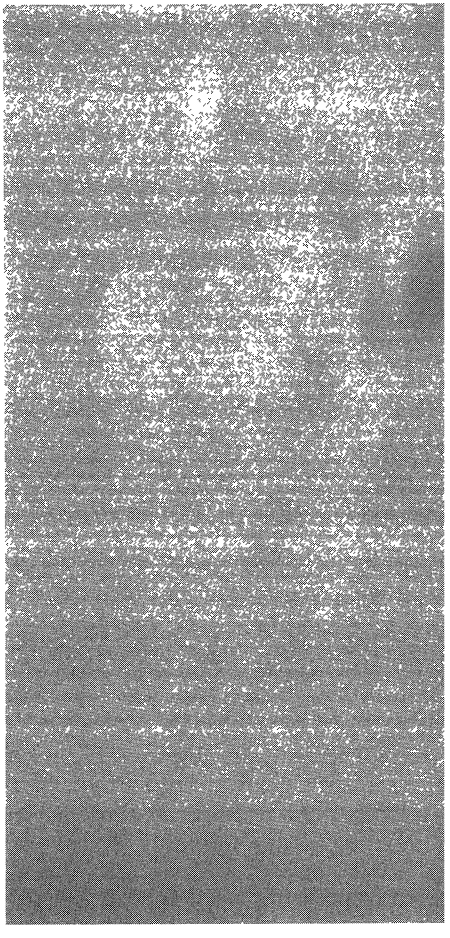
Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2 54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1 778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1 27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	Q F J	QUAD FLAT J-LEADED PACKAGE		P	1 27mm (50MIL)	J-Lead	4-direction
		Q F N	QUAD FLAT NON-LEADED PACKAGE		C	1 27mm (50MIL)	Leadless	Package under side

*P……Plastic, C……Ceramic



FM IF Amplifier



1) FM IF Amplifier

Type	Function	Page
CXA1002M/N	FM IF amplifier for cellular radio for 2nd IF I_{CC}=2.5mA CXA1002N : VSOP package	27
CXA1402M/N	FM IF amplifier for cellular radio for 2nd IF I_{CC}=1.5mA CXA1002M/N pin compatible (NEW)	35
CXA1003BM/BN	FM IF amplifier for cellular radio for 2nd MIX I_{CC}=5.7mA CXA1003BN : VSOP package	38
CXA1293M/N	FM IF amplifier for cellular pin replaceable with CXA1003BM/BN I_{CC}=3.0mA CXA1293N : VSOP package (NEW)	51
CXA1343M/N	FM IF amplifier for cellular built in gain control amplifier and RSSI output buffer	58
CXA1183M	FM IF amplifier for cordless phone built in JAM detect circuit	71
CXA1493M/N	FM IF amplifier for cordless phone built in detect output LPF and highly efficient RSSI function ☆	84
CXA1184M/N	FM IF amplifier for double conversion pocket pager	88
CXA1474M/N	FM IF amplifier for single conversion pocket pager I_{CC}=500μA 16P VSOP package (NEW)	103
CXA1484M/N	FM IF amplifier for double conversion pocket pager 20P VSOP package I_{CC}=1.4mA (NEW)	107

☆: Under development
(New): New device

Low Power FM IF Amplifier

Description

CXA1002M/N is an FM IF amplifier most suitable for cellular and FM radios.

Features

- Includes all the functions needed for cellular radios such as FM detecting circuit, RSSI, IF amplifier and others.
- Wide operating voltage range 4.5 to 9.5 V and low current consumption.
  (During Vcc=5 V, Icc=2.5 mA Typ.)
- Built-in audio output buffer circuit reduces external parts to a minimum.
- Wide range RSSI and excellent temperature characteristics.
- Compact 16 pin SOP and 16 pin VSOP package.

Functions

- IF amplifier and limiter
- RSSI (Received Signal Strength Indicator)
- FM detecting circuit

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	17		V
• Operating temperature	Tstg	−35 to	+85	°C
• Storage temperature	Topr	−55 to	+150	°C
• Allowable power dissipation	PD	500		mW

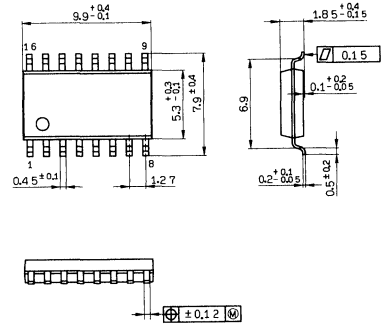
Recommended Operating Condition

• Supply voltage	Vcc	4.5 to	9.5	V

Package Outline

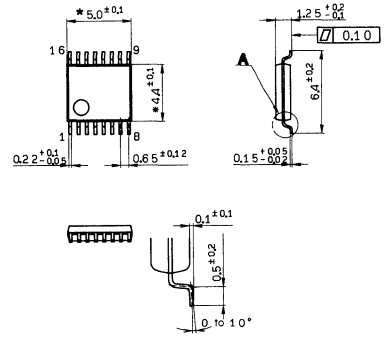
Unit: mm

CXA1002M 16 pin SOP (Plastic)



SOP-16P-LO1

CXA1002N 16 pin VSOP (Plastic)

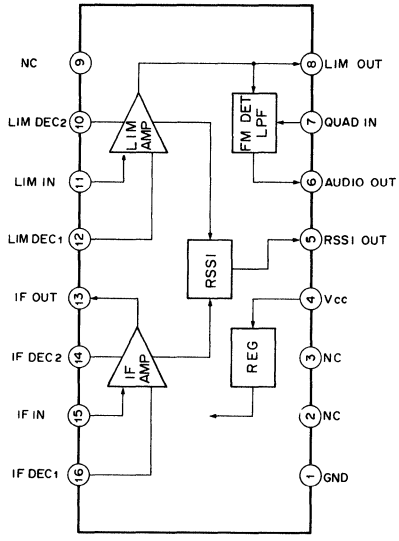


Note) The size marked * does not include the remaining resin.

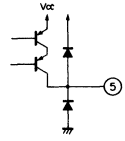
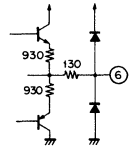
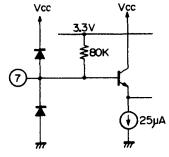
VSOP-16P-LO1

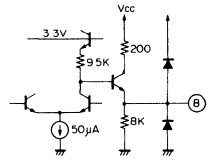
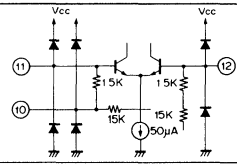
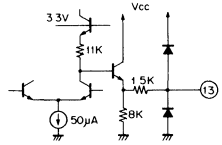
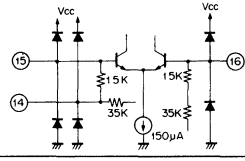
80518-YA

Block Diagram and Pin Configuration (Top View)



Pin Description and Equivalent circuit

No.	Symbol	Voltage (Typ)	Equivalent Circuit	Description
1	GND	0 V		Ground pin
4	Vcc	5.0 V		Supply pin
5	RSSI OUT			The current output corresponds to the input signal level to IF and LIM amplifiers.
6	AUDIO OUT	2.5 V		FM detected signal is output.
7	QUAD IN	3.3 V		Input pin of quadrature detecting circuit.

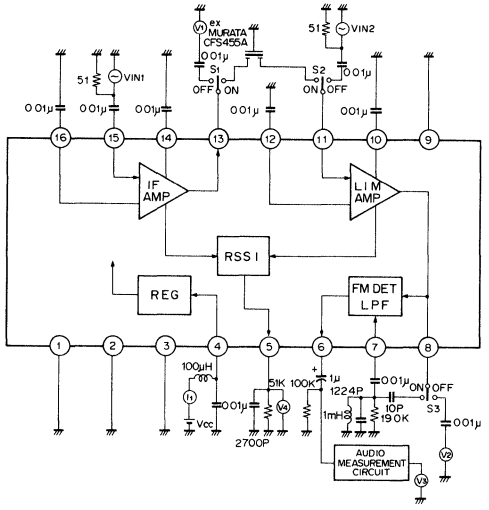
No.	Symbol	Voltage (Typ)	Equivalent Circuit	Description
8	LIM OUT	1.7 V		Output pin of limiter.
10 11 12	LIM DEC2 LIM IN LIM DEC1	1.7 V 1.7 V 1.7 V		Input and decoupling pin of limiter. Connect pins 10 and 12 to GND by means of a capacitor (0.01 to 0.047 μF).
13	IF OUT	1.6 V		Output pin of IF amplifier.
14 15 16	IF DEC2 IF IN IF DEC1	1.6 V 1.6 V 1.6 V		Input and decoupling pin of IF amplifier. Connect pins 14 and 16 to GND by means of a capacitor (0.01 to 0.047 μF).

Electrical Characteristics

See the Electrical Characteristics Test Circuit
Ta=25°C, Vcc=5 V, 0 dBm=223.6 mVrms

No.	Item	Symbol	SW turned ON	Input signal No.	Remarks	Test Point	Min.	Typ.	Max.	Unit
1	Consumption current	Icc				I_1	2.0	2.5	3.0	mA
2	IF amp voltage gain	VG1		V_{IN_1}: 455kHz −50 dBm		V_1	34	36	38	dB
3	Limiter voltage gain	VG2		V_{IN_2}: 455kHz −90 dBm		V_2	70	72	74	dB
4	Limiter output voltage	VO2		V_{IN_2}: 455kHz −20 dBm		V_2	500	570	640	mVp-p
5	Audio output voltage	VO3	S3	V_{IN_2}: 455kHz −20 dBm	f_{AUDIO} = 1 kHz DEV = ±8 kHz FM	V_3	115	195	245	mVrms
6	Audio output distortion	VD3		V_{IN_2}: 455kHz −20 dBm	f_{AUDIO} = 1 kHz DEV = ±8 kHz FM	V_3			1	%
7	Audio output S/N	SN3		V_{IN_2}: 455kHz −20 dBm		V_3	40			dB
8	Audio output AMRR	AR3		V_{IN_2}: 455kHz −20 dBm	f_{AUDIO} = 1 kHz MOD = ±80% AM	V_3	30			dB
9	RSSI output voltage L	VO4L	S1, S2	V_{IN_1}: 455kHz −100 dBm		V_4	0.25	0.40	0.55	V
10	RSSI output voltage H	VO4H	S1, S2	V_{IN_1}: 455kHz −20 dBm		V_4	1.50	1.85	2.20	V

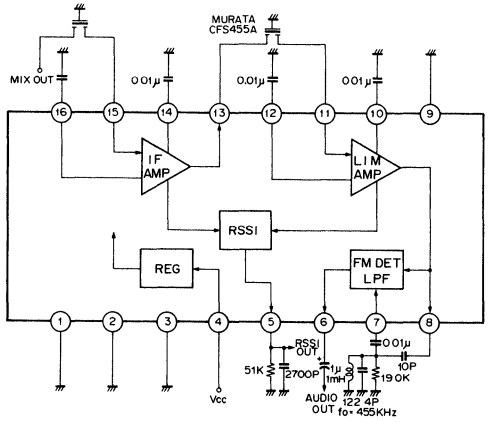
Electrical Characteristics Test Circuit



Operation

Signals passing through the filter and input through pin 15, amplified at IF amplifier and output through pin 13. IF amplifier output is subjected again to band limitation, to amplitude limitation at the limiter amplifier and output through pin 8. The limiter amplifier output is phase shifted at the LC resonance circuit and after undergoing quadrature detection, audio signals are output from pin 6.
For RSSI, at IF and limiter amplifiers stages, a current corresponding to the input levels is obtained, added up and output from pin 5.
RSSI voltage output is obtained by connecting a suitable I to V conversion circuit (resister and capacitor parallel circuit) to pin 5.

Application Circuit



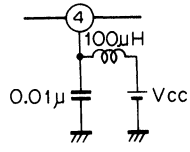
Notes on Usage

Voltage gain of IF amplifier in CXA1002M/N is about 36 dB. Voltage gain of the limiter amplifier is rather high at 72 dB. Please take the following precautions:

1. Decouple pin 4 (Vcc) with L and C as near to the pins as possible.
2. Be sure to ground pins 2, 3 and 9 (NC).
3. Separate input line from the output line as far as possible, and make the wiring short.
4. Decoupling capacitors of IF amplifier (pins 14, 16) and limiter amplifier (pins 10, 12) should be grounded as close to the respective pins as possible.
5. Work out the GND pattern to obtain an impedance as low as possible.
6. Electrostatic separation of the limiter amplifier input and output parts by setting up and shield plate gives better efficiency. (Mark use of pin 1 GND and pin 9 NC)

Application Note

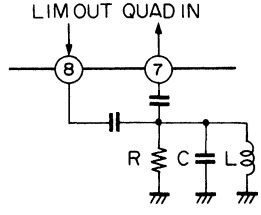
1) Supply
With the built-in voltage regulator, CXA1002M/N has wide operating power supply voltage range from +4.5 to 9.5 V (Typ. 5.0 V). Within the above supply voltage range, there are almost no changes in the characteristics.
Decouple pin 4 (Vcc) with L and C. (See Fig. below)



Decoupling

2) Filter
The most suitable band pass filter to be connected between pins 13 and 11 of CXA1002M/N should have the following specifications.
- I/O impedance : 1.5 kΩ ±10%
- Insertion loss (center frequency): <6 dB

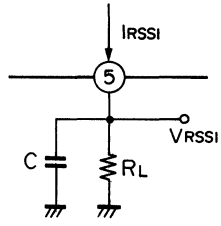
3) Phase shifter
To execute quadrature FM detection, the limiter output (pin 8) phase is shifted 90° by means of the RLC parallel resonance circuit or the discriminator and input through pin 7.
The Fig. below show the phase shifter made up by the RLC parallel resonance circuit. In this case set L, C value so that the 2nd IF signal frequency and the parallel resonance frequency become similar. As R value sets the audio output level, select this value so as to obtain the required output.



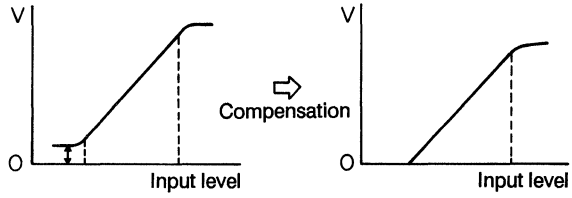
RLC Phase Shifter

4) Audio output
FM modulated audio and data signals are demodulated at the previous stage and output from pin 6 (Audio out).

5) RSSI
RSSI is function that detects the magnitude of the input signal level. In CXA1002M/N, it is output with current, and increases almost uniformly within the range of IF input level −100 to 0 dBm (2.24 μ to 224 mVrms). It is almost free from the supply voltage and temperature influence. However the output current is distributed within a range of ±20% by means of the resistance inside the IC.
When voltage output is required, it performs I to V conversion by means of a resistance. The value of that resistance is determined by RSSI's maximum output current and the maximum allowable voltage of pin 5. With RSSI's maximum output current at about 60 μA (Typ. 45 μA) and the allowable maximum voltage (performance guaranteed maximum voltage) at V_{CC} −1.8 V, select the resistance according to the supply voltage and the required output voltage.
When an output voltage of V_{CC} −1.8 V and above is required use the function after amplifying by means of an operational amplifier.
When the RSSI output voltage is required at AMPS which is the cellular radio standard. A uniform increase from 0 V is defined. However, for CXA1002M/N as there is an offset of about 0.3 to 0.5 V (V_{CC}=5 V, R_L=51 kΩ), arrange to start from 0 V by using an offset compensation circuit.

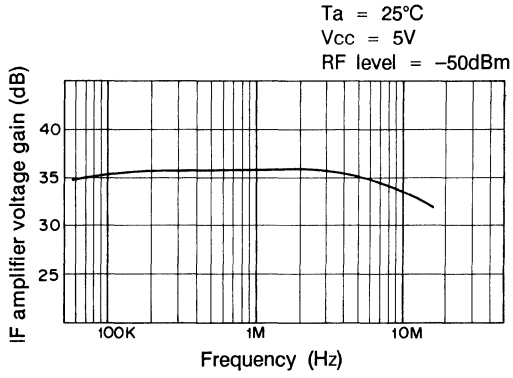


RSSI I to V circuit

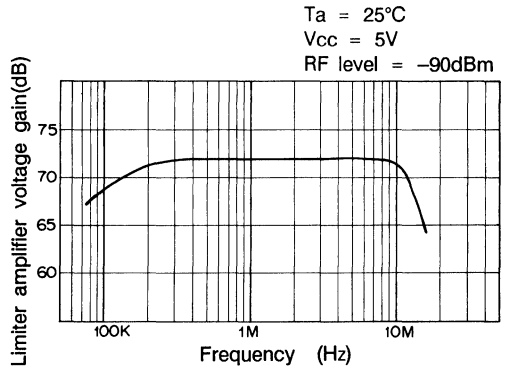


RSSI output voltage offset compensation

IF amplifier voltage gain frequency characteristics

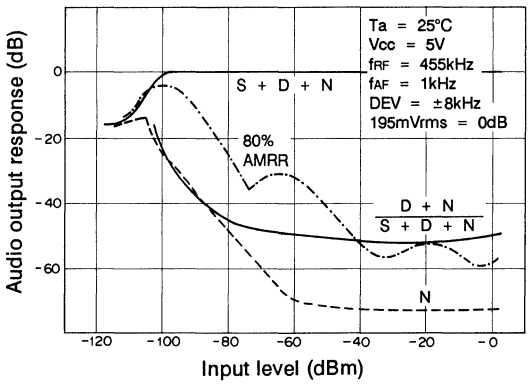


Limiter amplifier voltage gain frequency characteristics

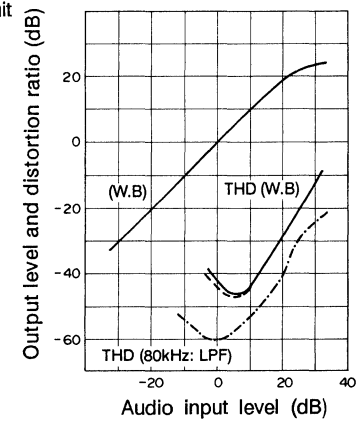


Audio demodulation characteristics (IF IN/AUDIO OUT)

*Used Audio Test Circuit



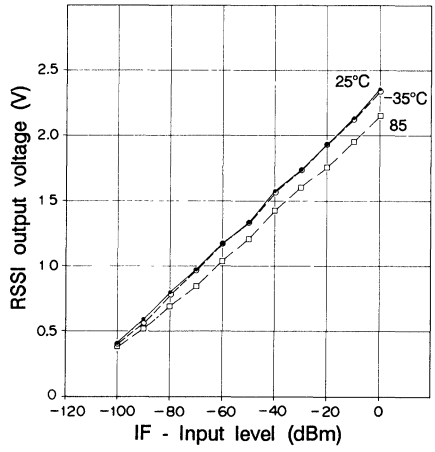
Audio I/O characteristics



Ta = 25°C
Vcc = 5V
RF level = −20dBm
fRF = 455kHz
fAF = 1kHz
DEV = ±2.9kHz

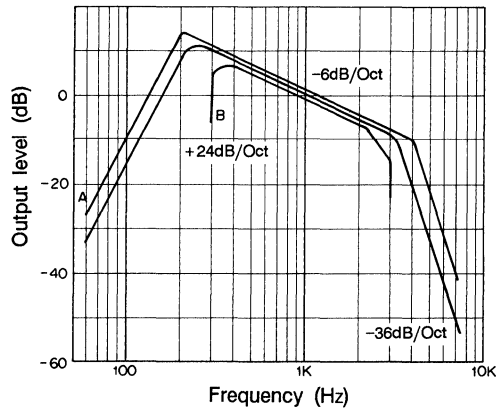
THD
(Audio measurement circuit)

RSSI characteristics

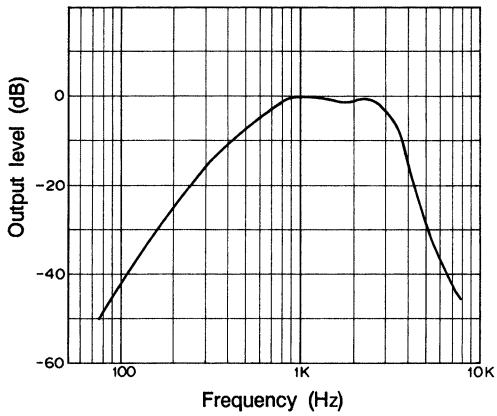


RX-audio filter frequency characteristics (A-B AMPS Standard)

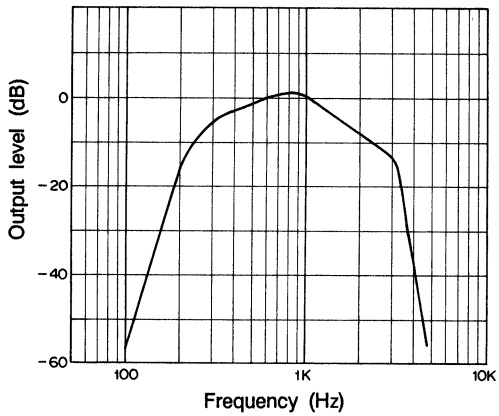
(BPF+DEEMP)



C-message filter frequency characteristics



Audio test circuit frequency characteristics



SONY CXA1402M/N

Low Power FM IF Amplifier — Advance Information

Description

The CXA1402M/N is an FM IF amplifier most suitable for cellular radios.

Features

- Includes all the functions needed for cellular radios such as IF limiter, FM detecting circuit, RSSI and others.
- Wide operating voltage, 3.0V to 6.0V and low current consumption.
  (I_{CC}=1.2mA Typ. at 3.6V)
- Built-in audio output buffer circuit reduces external parts to a minimum
- Wide range RSSI and excellent temperature characteristics.

Applications

Cellular radio set

Functions

- IF amplifier, limiter
- RSSI (Receiving Signal Strength Indicator)
- FM detecting circuit

Structure

Bipolar silicon monolithic IC

CXA1402M	CXA1402N
16pin SOP (Plastic)	16pin VSOP (Plastic)

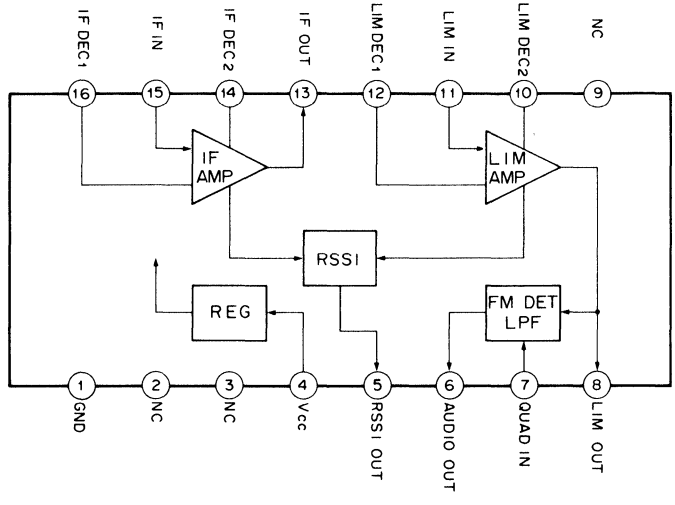
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	14	V
• Operating temperature	T_{opr}	−35 to +85	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable powr dissipation	P_D	500	mW

Operating Condition

• Supply voltage	V_{CC}	3.0 to 6.0	V

Block Diagram and Pin Configuration (Top View)



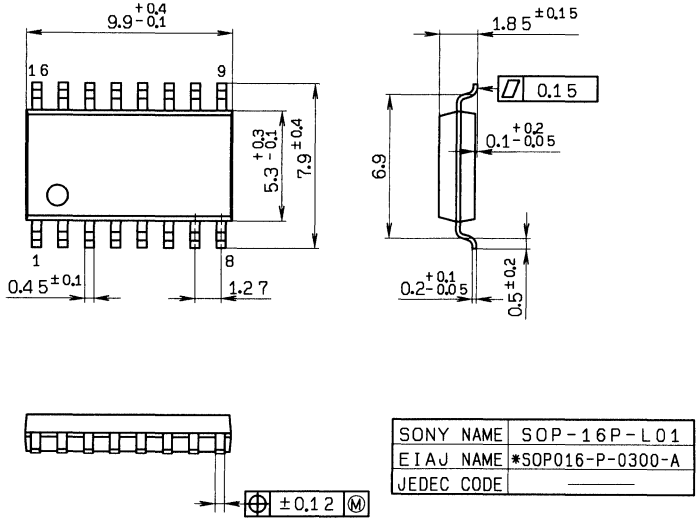
AE90740-HP

Electrical Characteristics (V_{CC}=3.6V, Ta=25°C, 0 dBm=0.223V)

No.	Item	Symbol	Input signal	Remarks	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC} 1			0.9	1.2	1.8	mA
2	IF amp voltage gain	VG1	V_{IN1} 455kHz −50dBm		48	49	53	dB
3	Limiter voltage gain	VG2	V_{IN2} 455kHz −90dBm		71	73	78	dB
4	Limiter output voltage	VO2	V_{IN2} 455kHz −20dBm		570	600	630	mVp-p
5	Audio output voltage	VO3	V_{IN2} 455kHz −20dBm	f_{AUDIO}=1kHz DEV=8kHz	155	195	225	mV_{RMS}
6	Audio output distortion	VD3	V_{IN2} 455kHz −20dBm	f_{AUDIO}=1kHz DEV=8kHz			1	%
7	Audio output S/N	SN3	V_{IN2} 455kHz −20dBm	f_{AUDIO}=1kHz DEV=8kHz	40			dB
8	Audio output AMRR	AR3	V_{IN2} 455kHz −20dBm	f_{AUDIO}=1kHz MOD=30%	30			dB
9	RSSI output voltage L	VO4L	V_{IN1} 455kHz −100dBm			0.3		V
10	RSSI output voltage H	VO4H	V_{IN1} 455kHz −20dBm			1.3		V

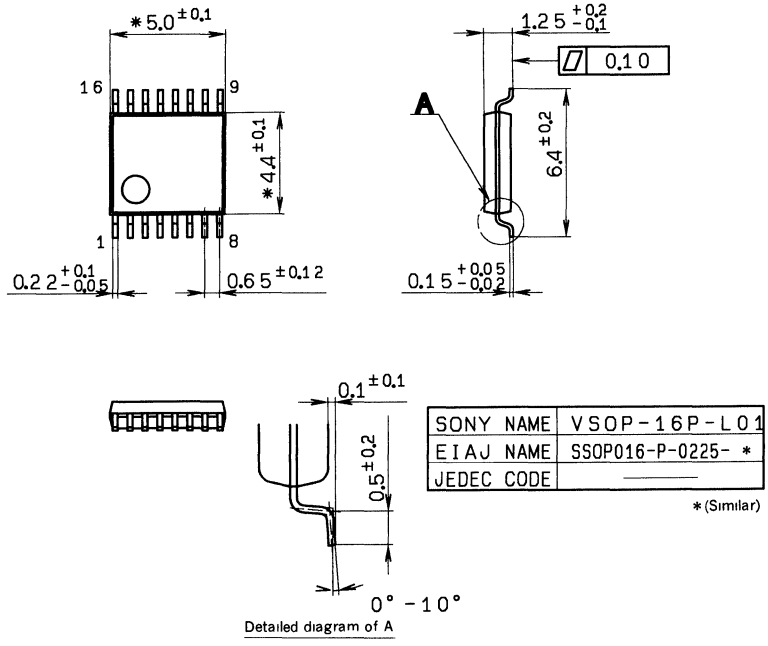
Package Outline Unit: mm

CXA1402M 16pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

CXA1402N 16pin VSOP (Plastic) 225mil



Detailed diagram of A

SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225- *
JEDEC CODE	———

*(Similar)

Dimensions marked with * does not include resin residue

SONY

CXA1003BM/BN

Low Power FM IF Amplifier

Description

CXA1003BM/BN are single-chip ICs for FM Radio such as cellular mobile, etc..

Features

- It includes all the functions needed to the cellular mobile such as second mixer, FM detecting circuit, muting circuit, RSSI, etc..
- It has wide operating voltage (4.5 to 9.5V) and low current consumption. (During V_{CC}=5V, I_{CC}=5.7 mA Typ.)
- It includes the audio output buffer, so it needs small number of peripheral parts.
- It has wide RSSI range and excellent temperature characteristics.

Functions

- Second mixer and oscillation circuit
- IF amplifier and limiter
- RSSI (Received Signal Strength Indicator)
- FM detecting circuit
- Muting circuit

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	17	V
• Operating temperature	Topr	−35 to +85	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	780 (CXA1003BM)	mW
		500 (CXA1003BN)	mW

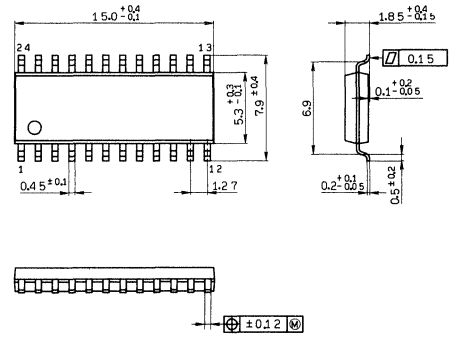
Recommended Operating Condition

• Supply voltage	Vcc	4.5 to 9.5	V

Package Outline

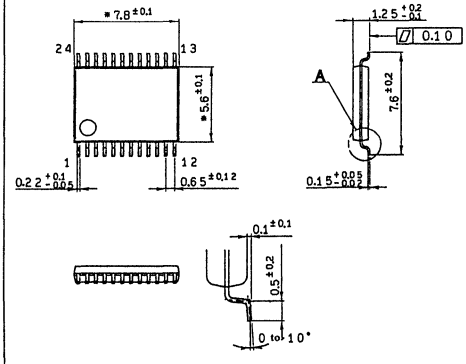
Unit: mm

CXA1003BM 24 pin SOP (Plastic)



SOP-24P-L01

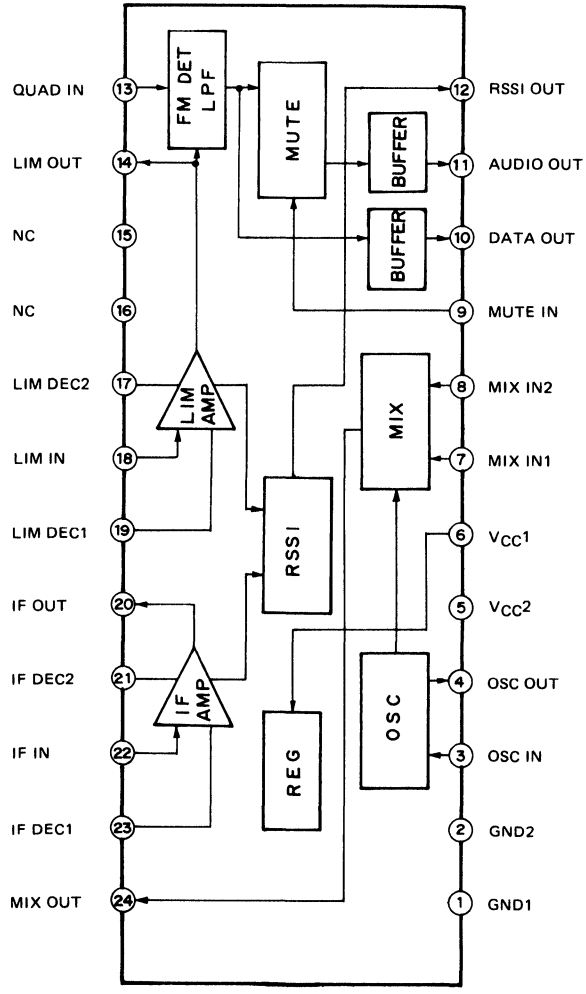
CXA1003BN 24 pin VSOP (Plastic)



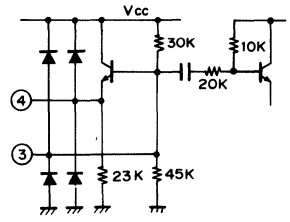
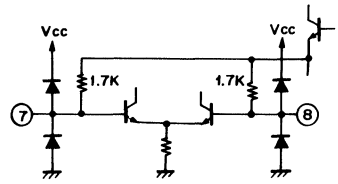
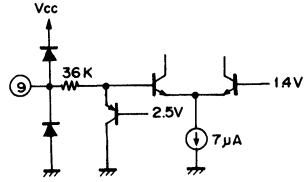
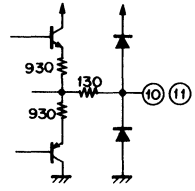
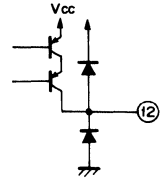
VSOP-24P-L01

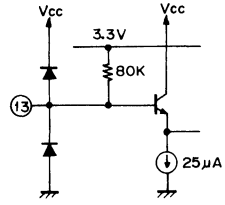
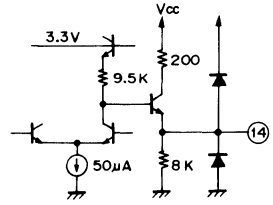
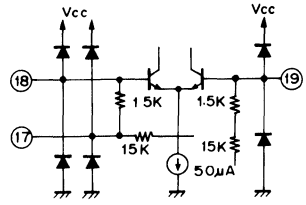
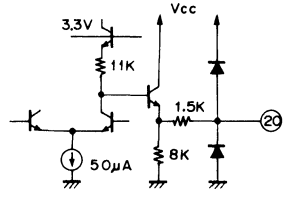
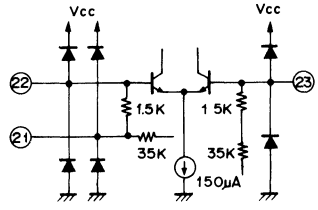
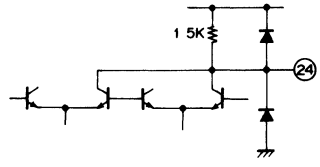
70567A-ST

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
1 2	GND1 GND2	0V		Grounding pin
3 4	OSC IN OSC OUT	3.0V 2.3V		Connect a crystal oscillator to compose a Colpitts type oscillation circuit. In case of using an external oscillator, input a signal to pin ③ and connect pin ④ to Vcc.
5 6	Vcc2 Vcc1	5.0V		Power supply pin
7 8	MIX IN1 MIX IN2	1.2V 1.2V		Input pin of mixer. In case of using a single input, connect pin ⑧ to GND with capacitor.
9	MUTE IN			Control pin of pin ⑪ ; audio output. A signal is output at L (≦0.8V), and is muted at H (≧2.0V).
10 11	DATA OUT AUDIO OUT	2.5V 2.5V		FM detected signal is output. The output of pin ⑪ can be muted by the input of pin ⑨.
12	RSSI OUT			Output current is corresponding to a input signal level.

No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
13	QUAD IN	3.3V		Input pin of quadrature detecting circuit. Connect a resonance circuit between pin ⑬ and ⑭ .
14	LIM OUT	1.7V		Output pin of limiter.
17 18 19	LIM DEC2 LIM IN LIM DEC1	1.7V 1.7V 1.7V		Input and decoupling pin of limiter. Connect pin ⑰ and ⑲ to GND with capacitor (0.01 to 0.047μF).
20	IF OUT	1.6V		Output pin of IF amp.
21 22 23	IF DEC2 IF IN IF DEC1	1.6V 1.6V 1.6V		Input pin and decoupling pin of IF amp. Connect pin ㉑ and ㉓ to GND with capacitor (0.01 to 0.047μF).
24	MIX OUT	3.8V		Output pin of mixer.

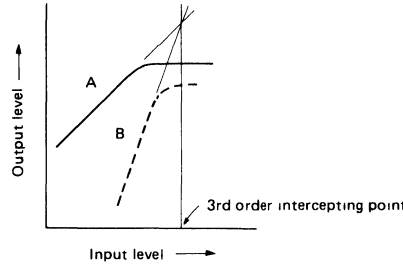
Electrical characteristics

(Ta=25°C, V_{CC}=5V See the Electrical Characteristics Test Circuit)
0 dBm=223.6 mVrms

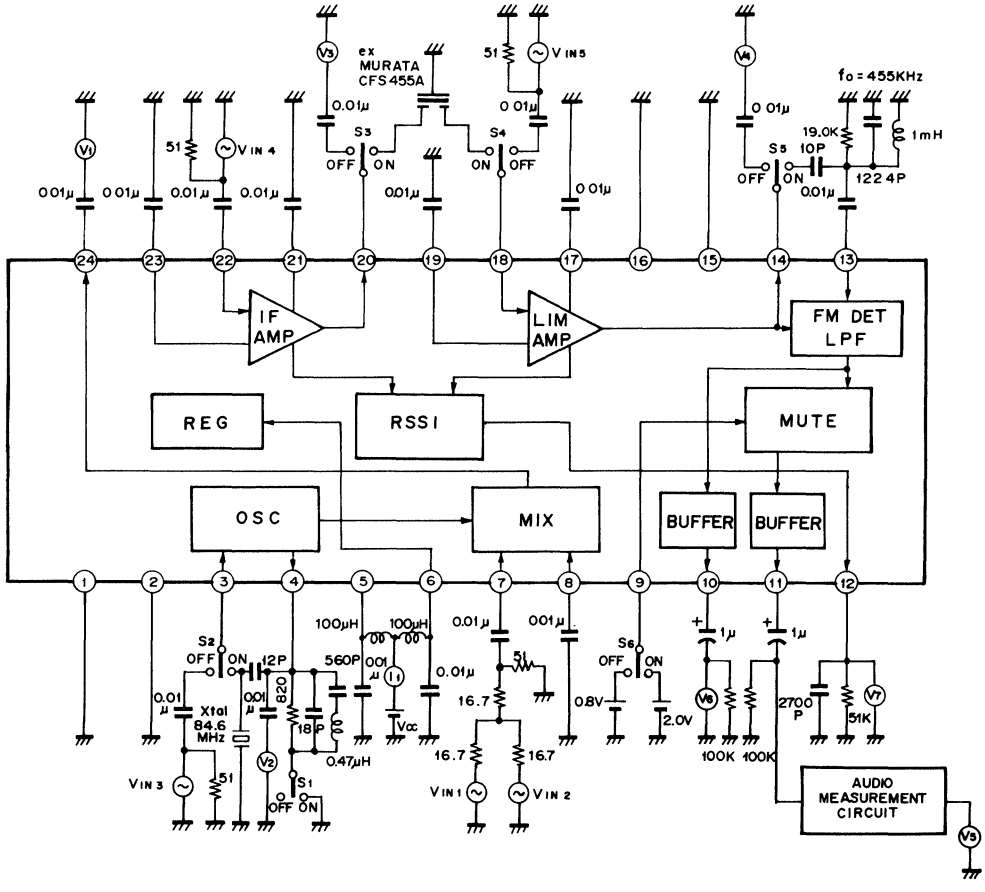
No.	Item	Symbol	SW which turns ON	Input signal, No.	Remark	Test point	Min.	Typ.	Max.	Unit
1	Consumption current	I_{CC}				I_1	4.7	5.7	7.3	mA
2	Mixer conversion gain	VG1		V_{IN1}: 80MHz −40dBm V_{IN3}: 80.455MHz 10dBm	f_{OUT}=455kHz Output level of 455kHz component Input level of pin ⑦.	V_1	18	20	22	dB
3	3rd order intercepting point	IM1		V_{IN1}: 80.06MHz V_{IN2}: 80.12MHz V_{IN3}: 80.455MHz 10dBm	f_{OUT}=455kHz See Note	V_1	−6.0	−4.5		dBm
4	Oscillator output voltage	VO1	S1, S2		0dB=223.6mVrms	V_2	−5	0	+5	dB
5	IF amp voltage gain	VG2		V_{IN4}: 455kHz −50dBm		V_3	34	36	38	dB
6	Limiter voltage gain	VG3		V_{IN5}: 455kHz −90dBm		V_4	70	72	74	dB
7	Limiter output voltage	VO3		V_{IN5}: 455kHz −20dBm		V_4	500	570	640	mVp-p
8	Audio output voltage	VO4	S5	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5	155	195	245	mVrms
9	Audio output distortion	VD4		V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5			1	%
10	Audio output S/N	SN4		V_{IN5}: 455kHz −20dBm		V_5	40			dB
11	Audio output AMRR	AR4		V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz MOD=±80% AM	V_5	30			dB
12	Crosstalk in muting	MX4	S6	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5			−65	dB
13	Data output voltage	VO5	S5	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_6	155	195	245	mVrms
14	RSSI output voltage L	VO6	S3, S4	V_{IN4}: 455kHz −100dBm		V_7	0.25	0.40	0.55	V
15	RSSI output voltage H	VO7	S3, S4	V_{IN4}: 455kHz −20dBm		V_7	1.50	1.85	2.20	V

Note) See next page

Note) Definition of the 3rd order intercepting point. The 3rd order intercepting point is determined by the input level of pin ⑦ at the tangent intersection of A and B. A and B is 455 kHz component in case of 1 and 2. In case 1, V_{IN1} is 80 MHz, V_{IN2} is terminated by 50Ω and V_{IN3} is 10 dBm 80.455 MHz. In case 2, V_{IN1} is 80.06 MHz, V_{IN2} is 80.12 MHz (level of V_{IN1} and V_{IN2} is eaqual) and V_{IN3} is 10 dBm 80.455 MHz.

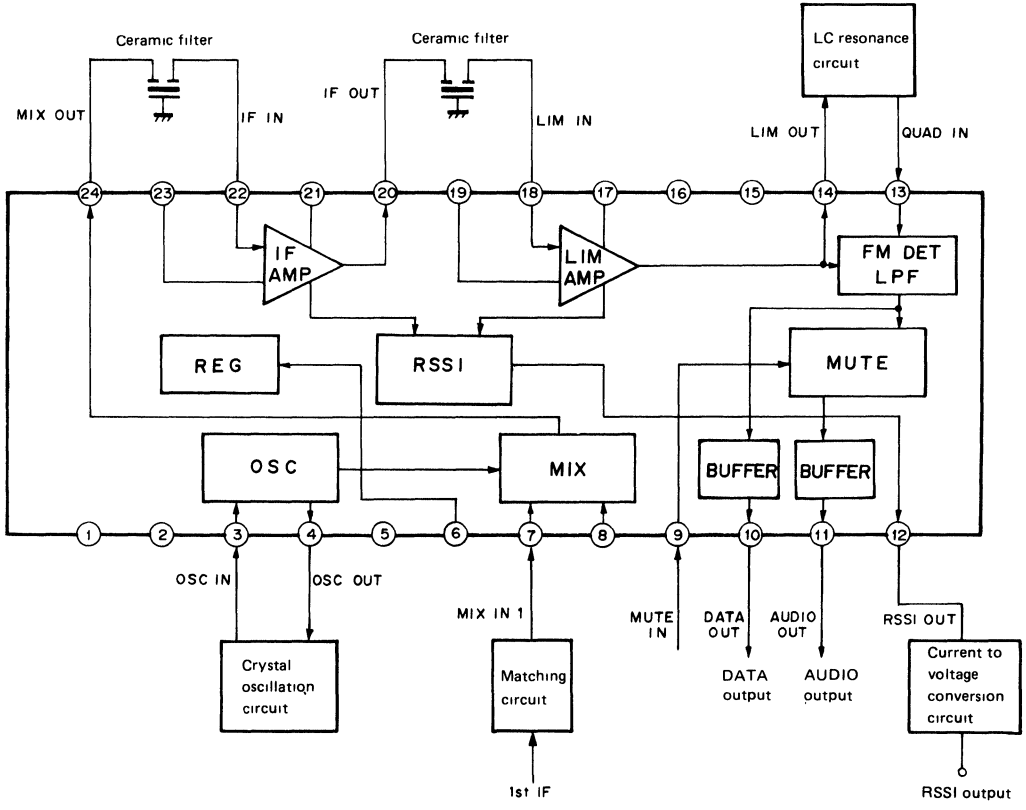


Electrical Characteristics Test Circuit



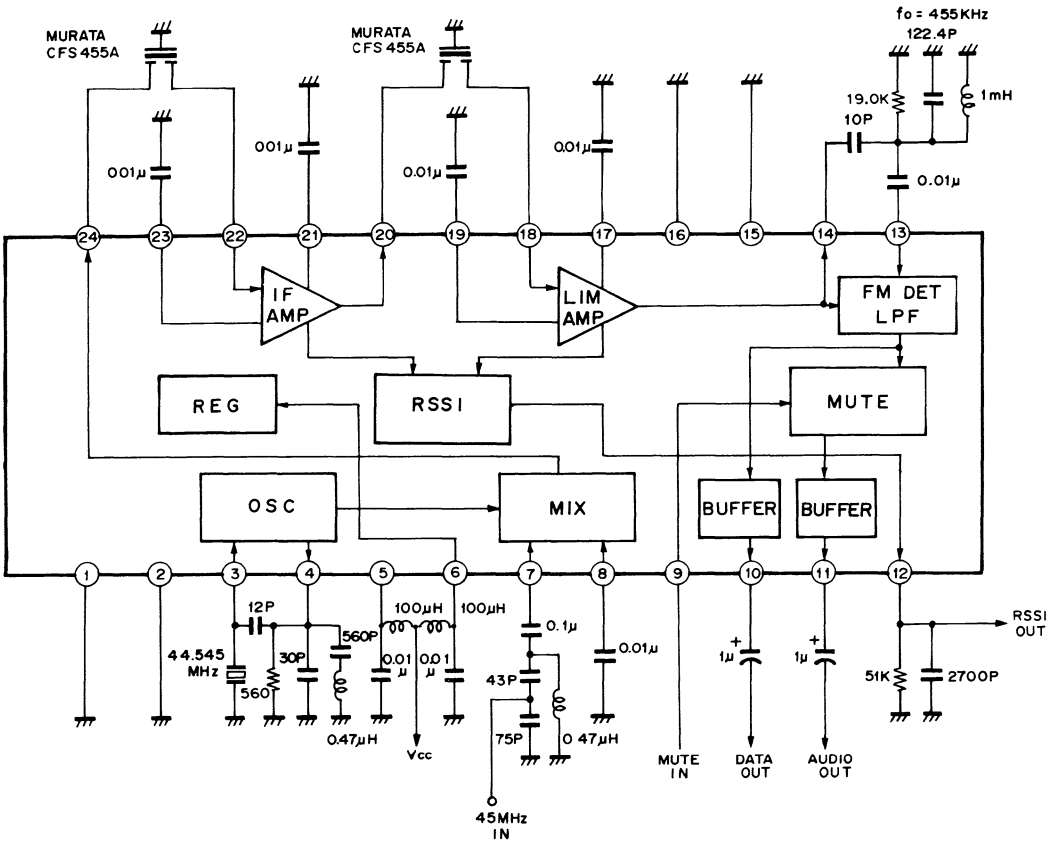
Description of Operation

The signals which have been input from pins ⑦ and ⑧ are mixed with the local oscillation signals from the oscillator in the mixer, and the frequency converted signal is output from pin ㉔ . The oscillator is self-oscillated by composing Colpitts type crystal oscillation circuit between pin ③ and ④ . In addition, it is possible to apply a local oscillation signal to pin ③ from the external circuit. After the bandwidth is limited by BPF, the mixer output is amplified by IF amplifier and output from pin ⑳ . The IF amplifier output is limited its bandwidth again, and amplitude limited by the limiter and output from pin ⑭ . The limiter amplifier output is phase-shifted by LC resonance circuit, etc., and audio signal is output from pin ⑩ and ⑪ after being quadrature detected. The output from pin ⑪ can be muted by control signal from pin ⑨ . The control signal is muting at "H" in TTL level and through at "L".



The RSSI output is the currents corresponding to the input levels at the IF amplifier and the limiter. It is possible to convert a current into a voltage by connecting a proper I. V conversion circuit.

Application Circuit



Note on Use

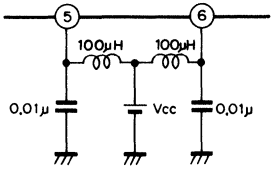
CXA1003BM/BN have very high at voltage gain, so take care of the following.

1. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C as near to the pins as possible.
2. Connect pin ⑮ and ⑯ (NC) to GND.
3. Separate input line from the output line as far as possible, and make the wiring short.
4. Connect pin ⑧, ㉑, ㉓, ⑰ and ⑲ to GND with capacitor as near to pins as possible.
5. The GND impedance should be as low as possible.
6. It is better to separate statically the input from the output of the limiter with shielding plate.

Notes on Application

1) Power supply

The CXA1003BM/BN have a voltage regulater within the IC, so these have wide operating power supply range (+4.5 to +9.5V; Typ: 5.0V). There is little change in characteristics in the operating range. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C. (See Fig. right)



Power supply decoupling

2) Oscillator

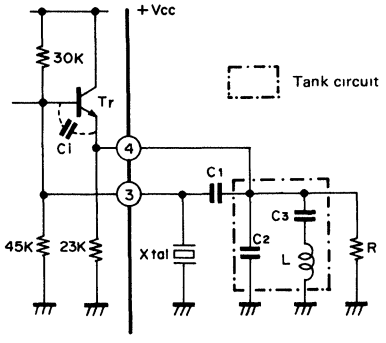
The method to use oscillator of CXA1003BM/BN is the following:

(a) Method to input from pin ③ with the self-excitating oscillation signal by composing a crystal oscillation circuit of the Colpitts type to pin ③ and ④.

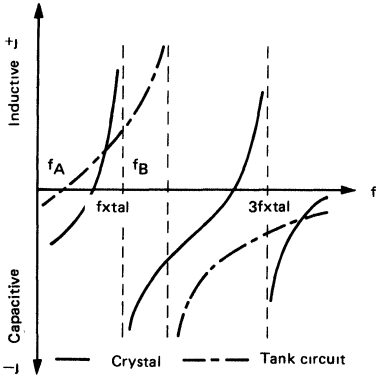
(b) Method to input directly the external local oscillation signal to pin ③.

<Crystal oscillation circuit>

The 3rd overtone crystal oscillation circuit of the Colpitts type is Fig. bellow.



Colpitts type crystal oscillation circuit



Reactance characteristics

The conditions of the 3rd overtone oscillation of this oscillation circuit are the following.

- The parallel resonance frequency (f_B) of the tank circuit should be smaller than the 3rd oscillation frequency ($3f_{xtal}$) and the serial resonance frequency (f_A) should be smaller than the basic oscillation frequency (f_{xtal}) ($3f_{xtal} > f_B$, $f_{xtal} > f_A$).
- The load capacitance (:C_L) of the crystal should be adequate.
- The f_t of the amplifier (Tr) should be sufficiently larger than $3f_{xtal}$.

The constant is determined so as to satisfy these conditions.
The oscillation level is set at 280 to 890 mVrms (Typ: 500 mVrms) and adjust the level by changing the resistance value (R). The slight adjustments of the oscillation frequency and oscillation level are performed with C_2 and L.

<In case of direct input>
In case of direct input, connect pin ④ to V_{CC} and input external local oscillation signal to pin ③. Input level at this point is also 280 to 890 mVrms (Typ: 500 mVrms).

3) Mixer

Mixer of the CXA1003BM/BN is a double balance type Input ports are pin ⑦ and ⑧, and in case of single input, input signal to pin ⑦, and connect pin ⑧ to GND with capacitor. It is possible to use differential input. The standard input level is −110 to −30 dBm (0.7μ to 7.0 mVrms), and input through a suitable matching circuit.

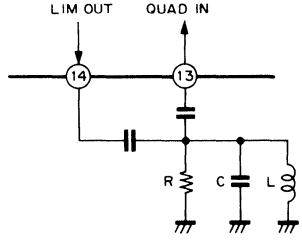
4) Filter

The band-pass filters which are connected between pin ㉔ and ㉒ and between pin ⑳ and ⑱ of the CXA1003BM/BN are desired to have the specifications as follows.

- Input/output impedance: 1.5 kΩ ± 10%
- Insertion loss (center frequency): <6 dB

5) Phase shifter

Input to pin ⑬ to shift the phase of the limiter output (pin ⑭) 90° by the RLC parallel resonance circuit or the discriminator, etc. in order to quadrature FM detection. The Fig. below shows the RLC phase shifter. In this case, determine the L and C values so that the 2nd IF signal frequency and the parallel resonance frequency are the same, and the audio output level is determined by R value. RLC Phase shifter or Oscillator is connected between pin ⑬ and ⑭, the phase shifted signal is input to pin ⑬ and demodulated in quadrature detector.



RLC phase shifter

6) Audio output, data output and muting

The FM modulated audio or data signal is demodulated in the prior stage and is output from pin ⑪ (AUDIO OUT) and ⑩ (DATA OUT). Output from pin ⑪ can be muted by control signal of TTL level from pin ⑨ (MUTE IN). (See table below.)

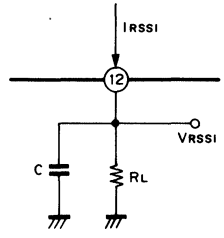
Control signal	Audio signal
H ($\geq$2.0V)	Mute
L ($\leq$0.8V)	Slew

Table of muting control

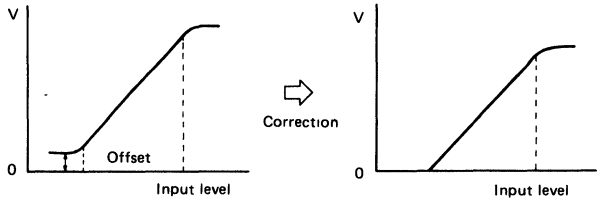
7) RSSI

The function of RSSI is to detect the input level, and output current increases monotonously within the range of IF input level −100 to 0 dBm (2.24μ to 224 mVrms). The power supply and temperature effect little on output current. However, the output current is distributed within the range of ±20% due to the resistance within the IC. In case voltage output is required, it needs current to voltage conversion circuit composing with resistance, etc. The resistance value is determined by the RSSI maximum output current and the allowable maximum voltage of pin ⑫. The RSSI maximum output current is approximately 60 μA (Typ: 45 μA) and the allowable maximum voltage (recommended maximum voltage) is V_{CC}−1.8V, select the resistance according to the power supply and the required output voltage. In case the output voltage is required above V_{CC}−1.8V, amplify a voltage using an operational amplifier, etc.

The AMPS defines that the RSSI output voltage increases monotonously from 0 to 0.5V. The CXA1003BM/BN have an offset of approximately 0.3 to 0.5V (V_{CC} = 5V R_L = 51 kΩ), if it needs, utilize the offset correction circuit.

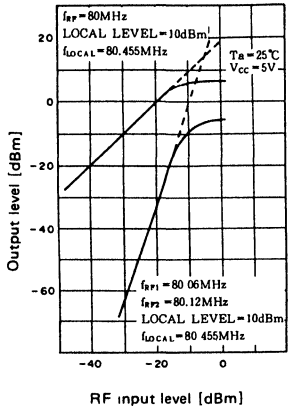


Current to voltage conversion with resistance of RSSI output

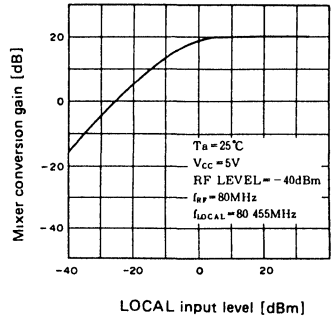


Offset correction of RSSI output voltage

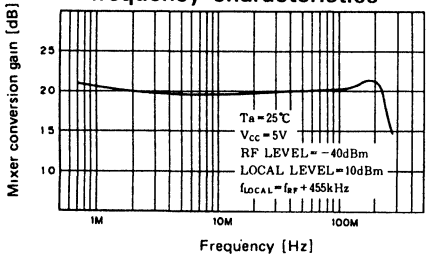
Mixer I/O characteristics and the 3rd order intercepting point



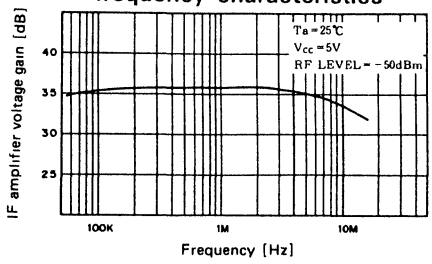
Mixer conversion gain vs. Local input level



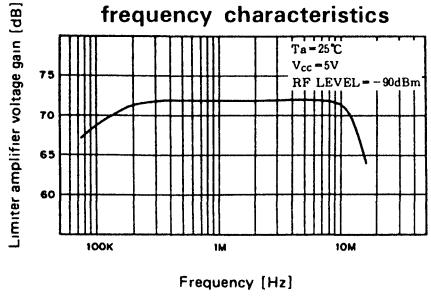
Mixer conversion gain frequency characteristics



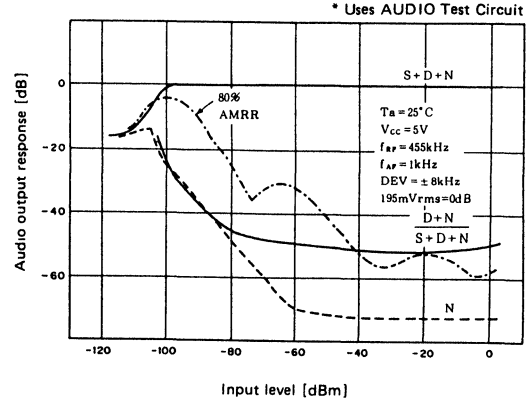
IF amplifier voltage gain frequency characteristics



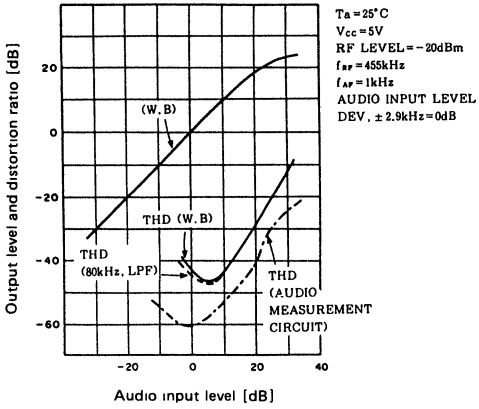
Limiter voltage gain frequency characteristics



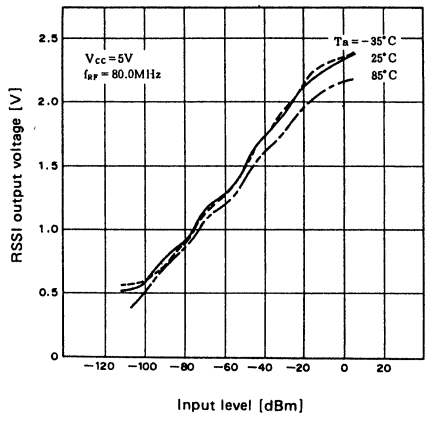
Audio demodulation characteristics (IF IN/AUDIO OUT)



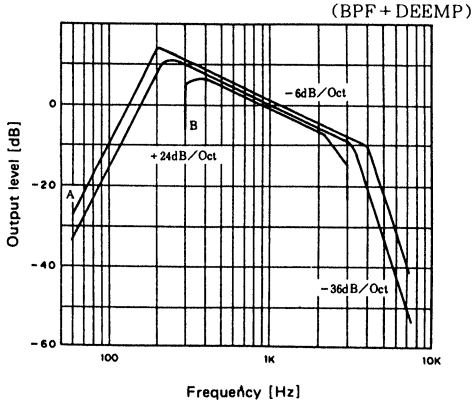
Audio I/O characteristics



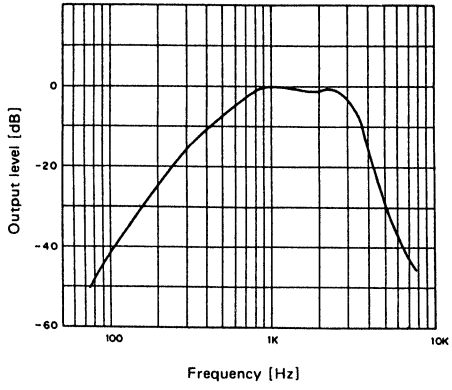
RSSI characteristics (MIX IN/RSSI OUT)



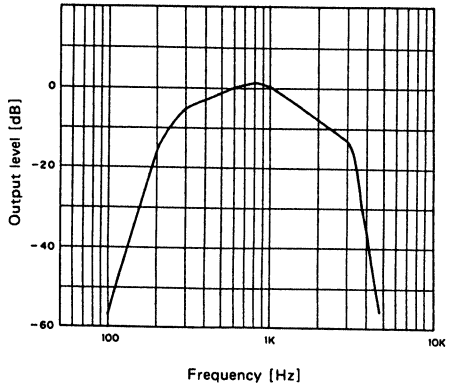
RX-audio filter frequency characteristics (A-B; AMPS Typ.)



C-message filter frequency characteristics



Audio measurement circuit frequency characteristics



SONY

CXA1293M/N

Low Power FM IF Amplifier

Preliminary

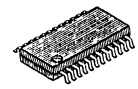
Description

The CXA1293M/N are single-chip ICs FM Radio such as CELLULAR mobile, etc.

Features

- Low current consumption (I_{CC}=3mA, at V_{CC} 3.6V)
- It includes all the functions needed to the cellular mobile such as second mixer, FM detecting circuit, muting circuit, RSSI, etc...
- It has low and wide operating voltage (3.0 to 6.0V).
- It includes the output buffer, so it needs small number of peripheral parts.
- It has wide RSSI range and excellent temperature characteristics.
- It is pin replaceable with CXA1003BM/N.
- Very small package 24 Pin SOP/VSOP

CXA1293M	CXA1293N
24pin SOP (Plastic)	24pin VSOP (Plastic)



- IF amplifier and limiter
- RSSI
- FM detecting circuit
- Muting circuit

Structure

Bipolar silicon monolithic IC

Functions

- Second mixer and oscillator

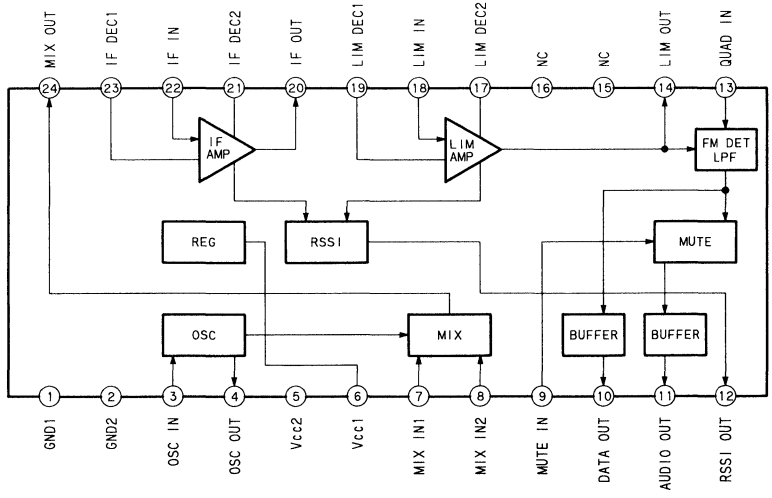
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	13	V
• Operating temperature	T_{opr}	−35 to +85	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	600	mW (CXA1293M)
		400	mW (CXA1293N)

Operating Condition

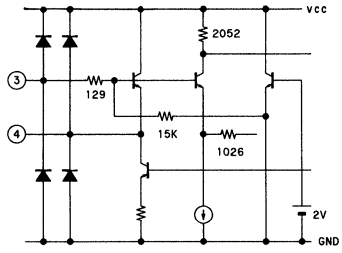
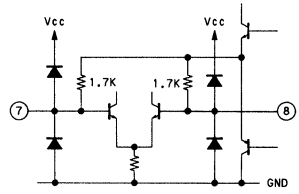
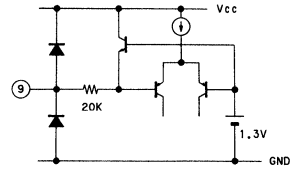
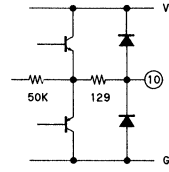
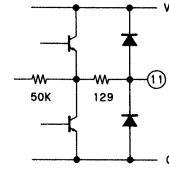
• Supply voltage	V_{CC}	3.0 to 6.0V	V

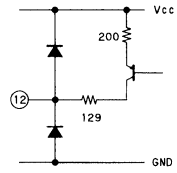
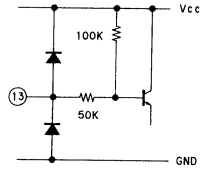
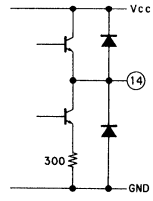
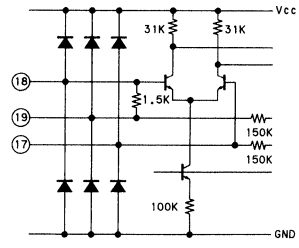
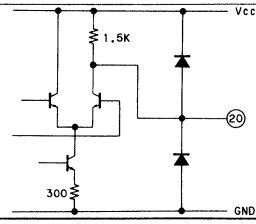
Block Diagram and Pin Configuration (Top View)

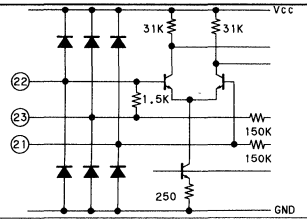
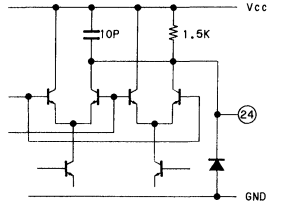


PE90X34-HP

Pin Description

Pin No.	Synbol	Voltage (Typ)	Equivalent ciruit	Description
1 2	GND1 GND2	0V		Grounding pin
3 4	OSC IN OSC OUT	1.3V 0.6V		Connect a crystal oscillator to compose a Colpitts type oscillation circuit. In case of using an external oscillator, input a signal to pin ③ and connect pin ④ to V_{CC}
5 6	V_{CC} 1 V_{CC} 2	3.6V		Power supply pin
7 8	MIX IN1 MIX IN2	1.3V 1.3V		Input pin of mixer. In case of using a single input, connect pin ⑧ to GND with capacitor.
9	MUTE IN			Control pin of pin ⑪; andio output. A signal is output at L (≦0.8V), and is muted at H (≧2.0V).
10	DATA OUT	1.3V		FM detected signal is output.
11	AUDIO OUT	1.3V		FM detected signal is output. The output of pin ⑪ can be muted by the input of pin ⑨.

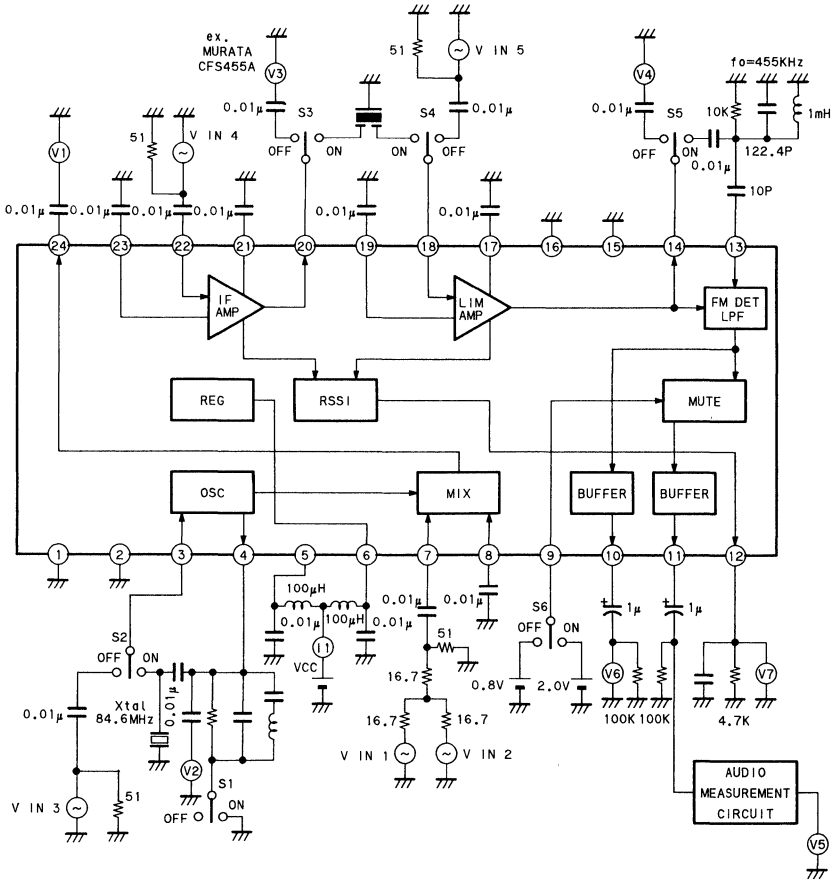
Pin No.	Synbol	Voltage (Typ)	Equivalent ciruit	Description
12	RSSI OUT	0.4V		Output current is corresponding to the input signal level.
13	QUAD IN	3.6V		Input pin of quadrature detecting circuit. Connect a resonance circuit between pin ⑬ and ⑭.
14	LIM OUT	2.6V		Output pin of limiter.
17 18 19	LIM DEC2 LIM IN LIM DEC1	2.6V 2.6V 2.6V		Input and decoupling pin of limiter. Connect pin ⑰ and ⑲to GND with capacitor (0.01 to 0.047μF).
20	IF OUT	1.3V		Output pin of IF amp.

Pin No.	Symbol	Voltage (Typ)	Equivalent ciruit	Description
21 22 23	IF DEC2 IF IN IF DEC1	2.6V 2.6V 2.6V		Input pin and decoupling pin of IF amp. Connect pin ㉑ and ㉓ to GND with capacitor (0.01 to 0.047μF).
24	MIX OUT	3.0V		Output pin of mixer.

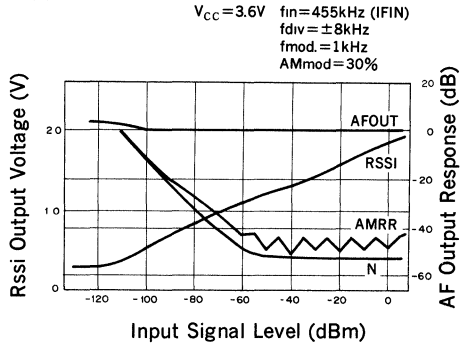
Electrical Characteristics (Ta=25°C, V_{CC}=3.6V See the Electrical Characteristics Test circuit)
0dBm=223.6mVrms.

No.	Item	Symbol	Input signal No.	Remark	Test point	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}			I1		3.8		mA
2	Mixer conversion gain	VG1	Vin 80MHz, −40dBm Vin 80.455MHz, 0dBm	fout=455kHz, output level of 455kHz component input level	V1		15.4		dB
3	IF amp voltage gain	VG2	Vin 455kHz, −50dBm		V3		49		dB
4	Limiter output gain	VG3	Vin5 455kHz, −90dBm		V4		73		dB
5	Audio output voltage	VO4	Vin5 455kHz, −20dBm	faudio=1kHz, Dev.= ±8kHz FM	V5		195		mV
6	Audio output distortion	VD4	Vin5 455kHz, −20dBm	faudio=1kHz, Dev.= ±8kHz FM	V5			1.0	%
7	Audio output S/N	SN4	Vin5 455kHz, −20dBm		V5	40			dB
8	Audio output AMRR	AR4	Vin5 455kHz, −20dBm	faudio=1kHz, Dev.= ±80% FM	V5	30			dB
9	Crosstalk in muting	MX4	Vin5 455kHz, −20dBm	faudio=1kHz, Dev.= ±8kHz FM	V5			−65	dB
10	Data output voltage	VO5	Vin5 455kHz, −20dBm	faudio=1kHz, Dev.= ±8kHz FM	V6		203		mV
11	RSSI output VOL. L	VO6	Vin4 455kHz, −100dBm		V7		0.50		V
12	RSSI output VOL. H	VO7	Vin4 455kHz, −20dBm		V7		1.55		V

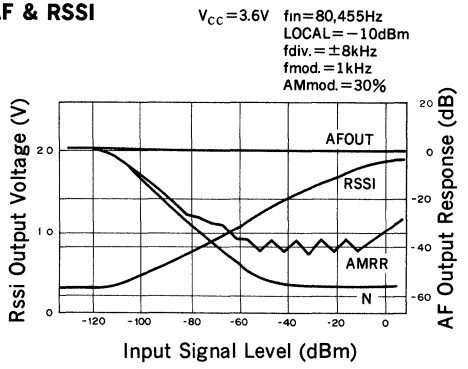
Electrical Characteristics Test Circuit



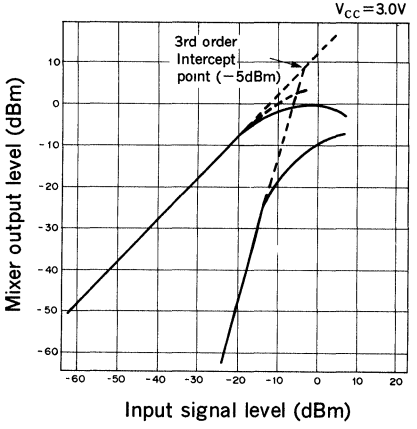
AF & RSSI



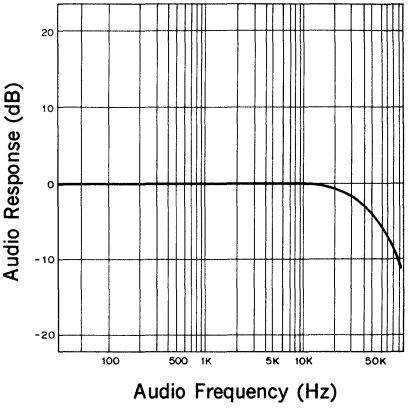
AF & RSSI



Input signal level vs. Mixer output level

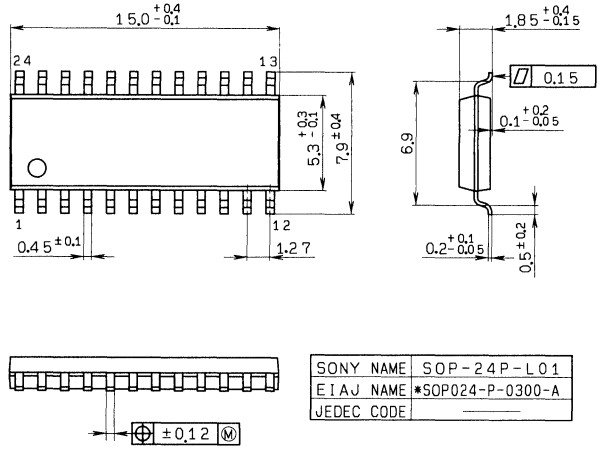


Detected Audio Frequency Response



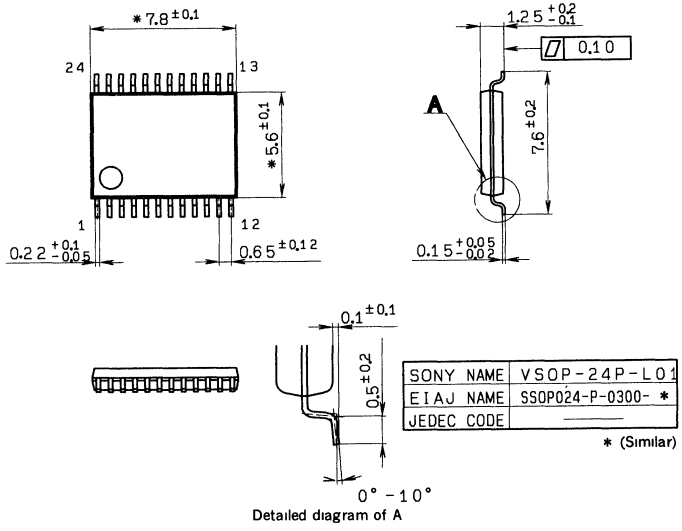
Package Outline **Unit : mm**

CXA1293M 24pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-24P-L01
EIAJ NAME	*SOP024-P-0300-A
JEDEC CODE	———

CXA1293N 24pin VSOP (Plastic) 275mil



Detailed diagram of A

SONY NAME	VSOP-24P-L01
EIAJ NAME	SSOP024-P-0300- *
JEDEC CODE	———

* (Similar)

Dimensions marked with * does not include resin residue

SONY®

CXA1343M/N

Low Power FM IF Amplifier

Description

CXA1343M/N are single-chip ICs for FM Radio such as CELLULAR mobile, etc...

Features

- It includes the all the functions needed to the cellular mobile such as second mixer, FM detecting circuit, RSSI (Received Signal Strength Indicator) etc...
- Built in gain adjustable AF amplifier and built in RSSI output buffer for low impedance output. (AF out 3.0V MAX, RSSI output imp. ≒ 100 Ω)
- It has wide operating voltage (4.5 to 9.5V) and low current comsumption. (I_{CC} = 5.7mA typ., at V_{CC} = 5V)
- It has wide RSSI range and excellent temperature characteristics.
- Very small package 24 pin SOP/VSOP

Functions

- Second mixer and oscillator
- IF amplifier and limitter
- RSSI output buffer
- FM detecting circuit
- Gain adjustable AF amplifier

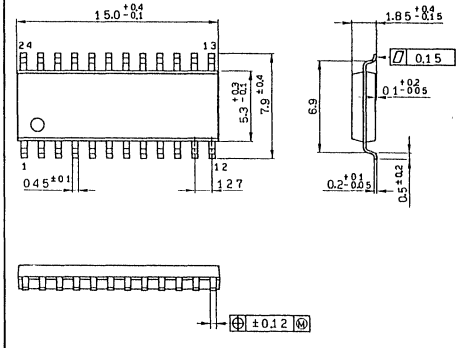
Structure

Bipolar silicon monolithic IC

Package Outline

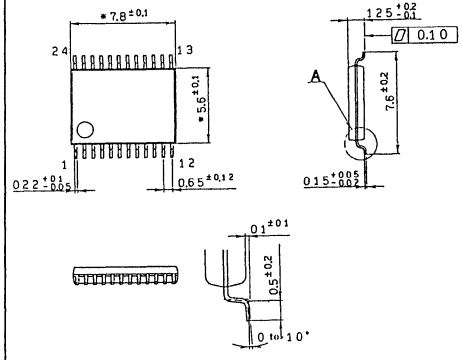
Unit : mm

CXA1343M 24 pin SOP (Plastic)



SOP-24P-L01

CXA1343N 24 pin VSOP (Plastic)



VSOP-24P-L01

Absolute Maximum Ratings (Ta = 25 °C)

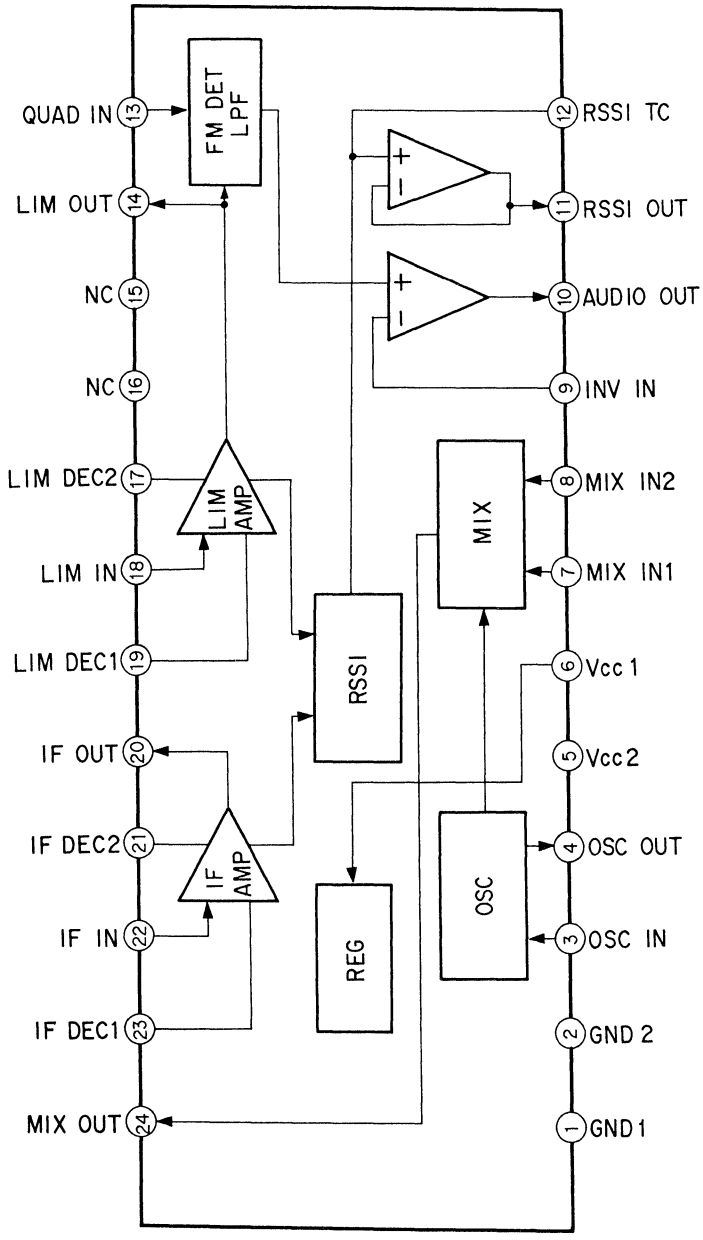
• Supply voltage	V_{CC}	17	V	
• Operating temperature	Topr	− 35 to + 85	°C	
• Storage temperature	Tstg	− 65 to + 150	°C	
• Allowable power dissipation	P_D	780	mW	(CXA1343M)
		500	mW	(CXA1343N)

Recommended Operating Condition

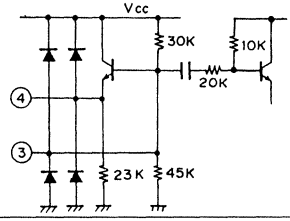
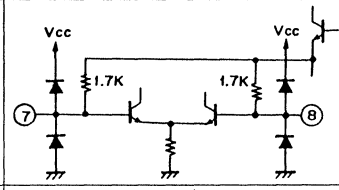
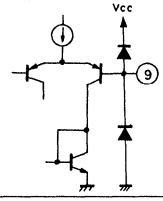
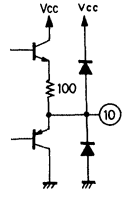
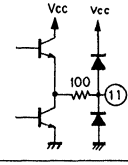
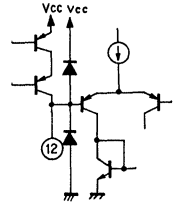
• Supply voltage	V_{CC}	4.5 to 9.5	V

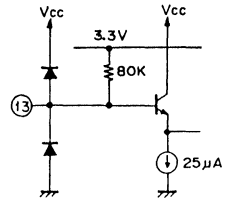
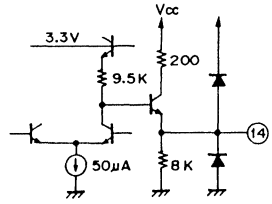
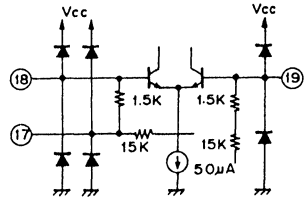
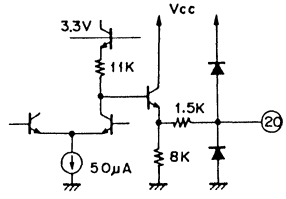
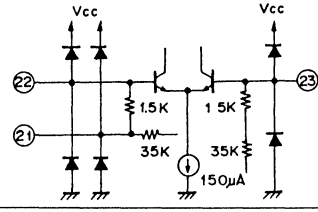
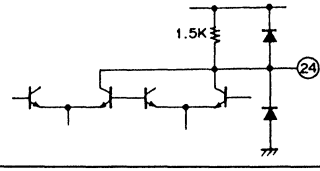
E89202 – ST

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
1 2	GND1 GND2	0V		Grounding pin
3 4	OSC IN OSC OUT	3.0V 2.3V		Connect a crystal oscillator to compose a Colpitts type oscillation circuit. In case of using an external oscillator, input a signal to pin ③ and connect pin ④ to Vcc.
5 6	Vcc2 Vcc1	5.0V		Power supply pin
7 8	MIX IN1 MIX IN2	1.2V 1.2V		Input pin of mixer. In case of using a single input, connect pin ⑧ to GND with capacitor.
9	INV IN	2.5V		Inverse input pin of the audio output amplifier
10	AUDIO OUT	2.5V		Output pin of the FM-detected signal. Amplifier gain can be adjusted by connecting an appropriate feedback circuit between this pin and pin ⑨.
11	RSSI OUT			RSSI output pin. Output voltage is corresponding to the level of signals input to the IF and LIM amplifiers.
12	RSSI TC			Time constant pin for RSSI. Current output is converted into voltage by connecting an appropriate R, C parallel circuit.

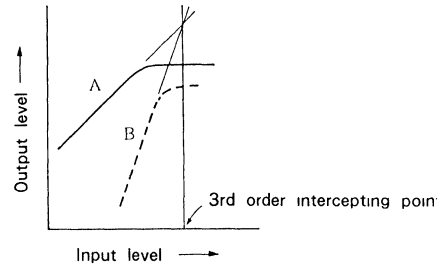
No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
13	QUAD IN	3.3V		Input pin of quadrature detecting circuit. Connect a resonance circuit between pin ⑬ and ⑭.
14	LIM OUT	1.7V		Output pin of limiter.
17 18 19	LIM DEC2 LIM IN LIM DEC1	1.7V 1.7V 1.7V		Input and decoupling pin of limiter. Connect pin ⑰ and ⑲ to GND with capacitor (0.01 to 0.047 μF).
20	IF OUT	1.6V		Output pin of IF amp.
21 22 23	IF DEC2 IF IN IF DEC1	1.6V 1.6V 1.6V		Input pin and decoupling pin of IF amp. Connect pin ㉑ and ㉓ to GND with capacitor (0.01 to 0.047 μF).
24	MIX OUT	3.8V		Output pin of mixer.

Electrical Characteristics

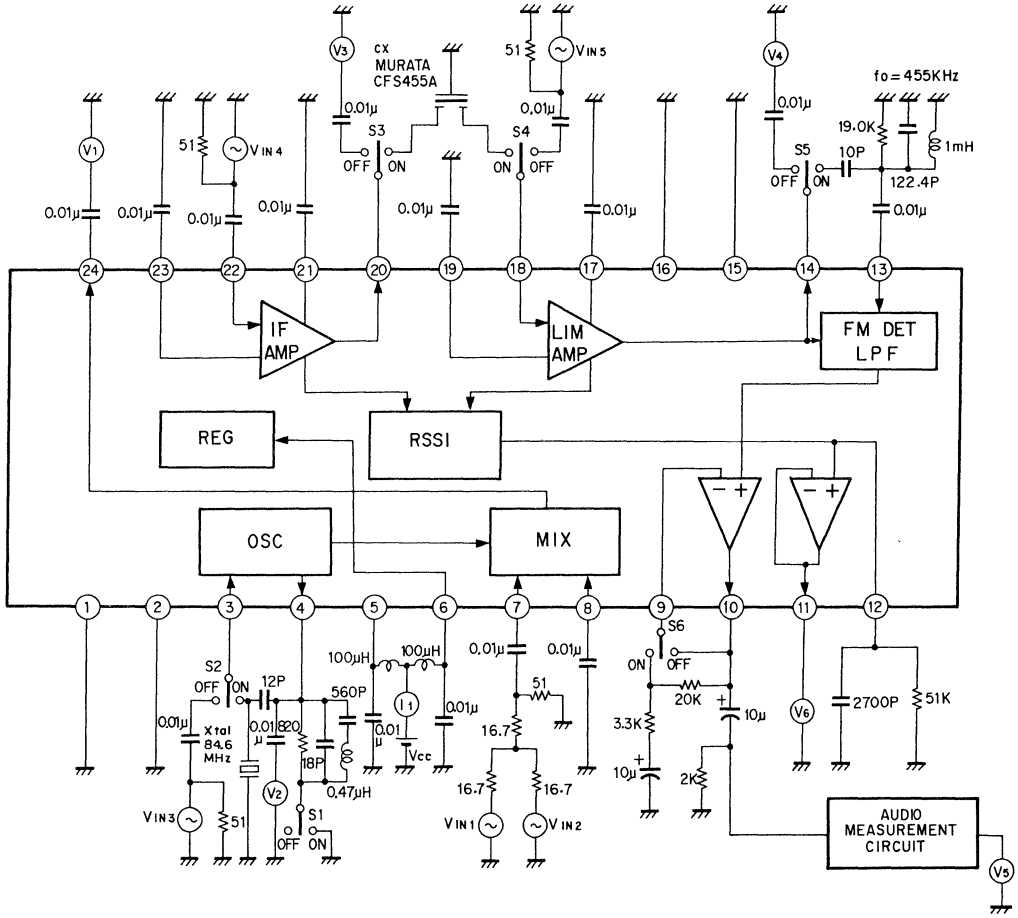
(Ta = 25°C, V_{CC} = 5V See the Electrical Characteristics Test Circuit)
0dBm = 223.6mVrms

No.	Item	Symbol	SW which turns ON	Input signal, No.	Remark	Test point	Min.	Typ.	Max.	Unit
1	Consumption current	Icc				I_1	4.7	5.7	7.3	mA
2	Mixer conversion gain	VG1		V_{IN1} : 80.0MHz, − 40dBm V_{IN2} : 80.455MHz, 10dBm	f_{OUT} = 455kHz Output level of 455kHz component input level of pin ⑦.	V_1	18	20	22	dB
3	3rd order intercepting point	IM1		V_{IN1} : 80.06MHz V_{IN2} : 80.12MHz V_{IN3} : 80.455MHz, 10dBm	f_{OUT} = 455kHz See Note	V_1	− 6.0	− 4.5		dBm
4	Oscillator output voltage	VO1	S1, S2		0dB = 223.6mVrms	V_2	− 5	0	5	dB
5	IF amp voltage gain	VG2		V_{IN4} : 455kHz, − 50dBm		V_3	34	36	38	dB
6	Limiter voltage gain	VG3		V_{IN5} : 455kHz, − 90dBm		V_4	70	72	74	dB
7	Limiter output voltage	VO3		V_{IN5} : 455kHz, − 20dBm		V_4	500	570	640	mVp-p
8	Audio output voltage	VO4	S5	V_{IN5} : 455kHz, − 20dBm f_A = 1kHz, DEV = ± 8kHz FM	G_V = 1, R_L = 2kΩ	V_5	155	195	245	mVrms
9	Audio output S/N	SN4	S5		G_V = 1, R_L = 2kΩ	V_5	40			dB
10	Audio output AMRR	AR4	S5	V_{IN5} : 455kHz, − 20dBm f_A = 1kHz, MOD = 80% AM	G_V = 1, R_L = 2kΩ	V_5	30			dB
11	Audio maximum output voltage	VM4	S5, S6	V_{IN5} : 455kHz, − 20dBm f_A = 1kHz, FM	G_V = 7, R_L = 2kΩ	V_5	3.0			Vp-p
12	Audio output distortion	VD4	S5, S6	V_{IN5} : 455kHz, − 20dBm f_A = 1kHz, FM	G_V = 7, R_L = 2kΩ, Adjust DEV. AFout = 2.5V	V_5			1	%
13	Audio output impedance	ZO4			G_V = 1				10	Ω
14	RSSI output voltage L	VL5		V_{IN4} : 455kHz, − 100dBm		V_6	0.25	0.40	0.55	V
15	RSSI output voltage H	VH5		V_{IN5} : 455kHz, − 20dBm		V_6	1.50	1.85	2.20	V
16	RSSI output impedance	ZO5					80	100	130	Ω

Note) Definition of the 3rd order intercepting point. The 3rd order intercepting point is determined by the input level of pin ⑦ at the tangent intersection of A and B. A and B is 455kHz component in case of 1 and 2. In case 1, V_{IN1} is 80MHz, V_{IN2} is terminated by 50 Ω and V_{IN3} is 10dBm 80.455MHz. In case 2, V_{IN1} is 80.06MHz, V_{IN2} is 80.12MHz (level of V_{IN1} and V_{IN2} is equal) and V_{IN3} is 10dBm 80.455MHz.

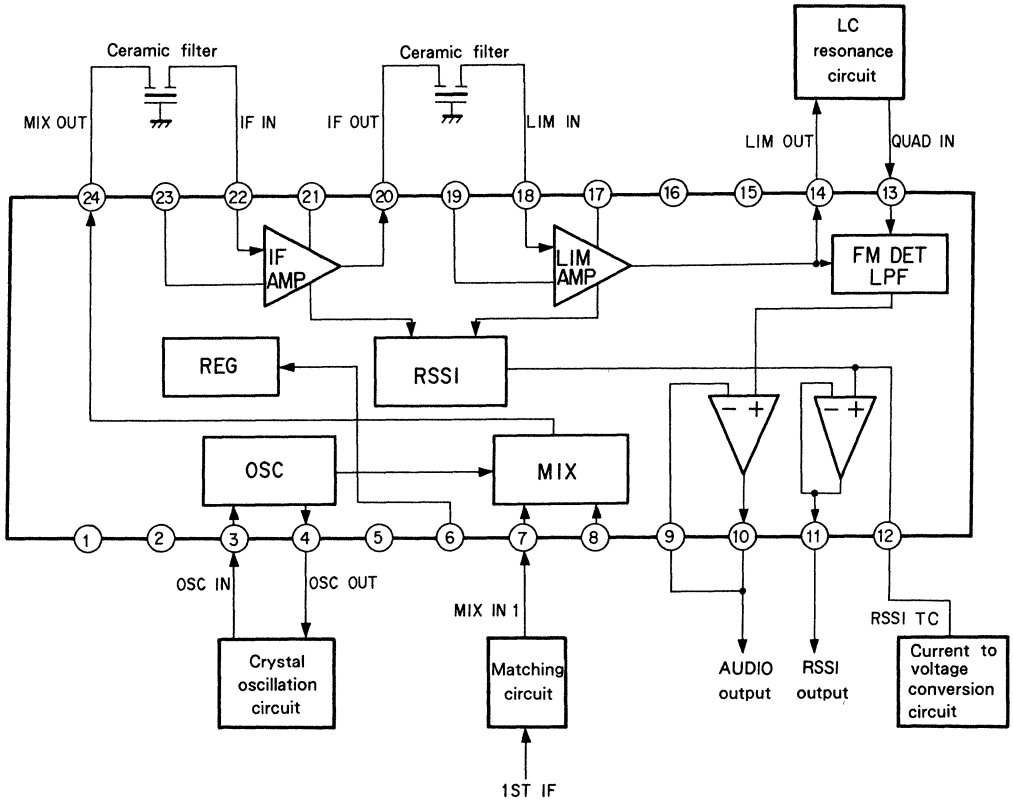


Electrical Characteristics Test Circuit



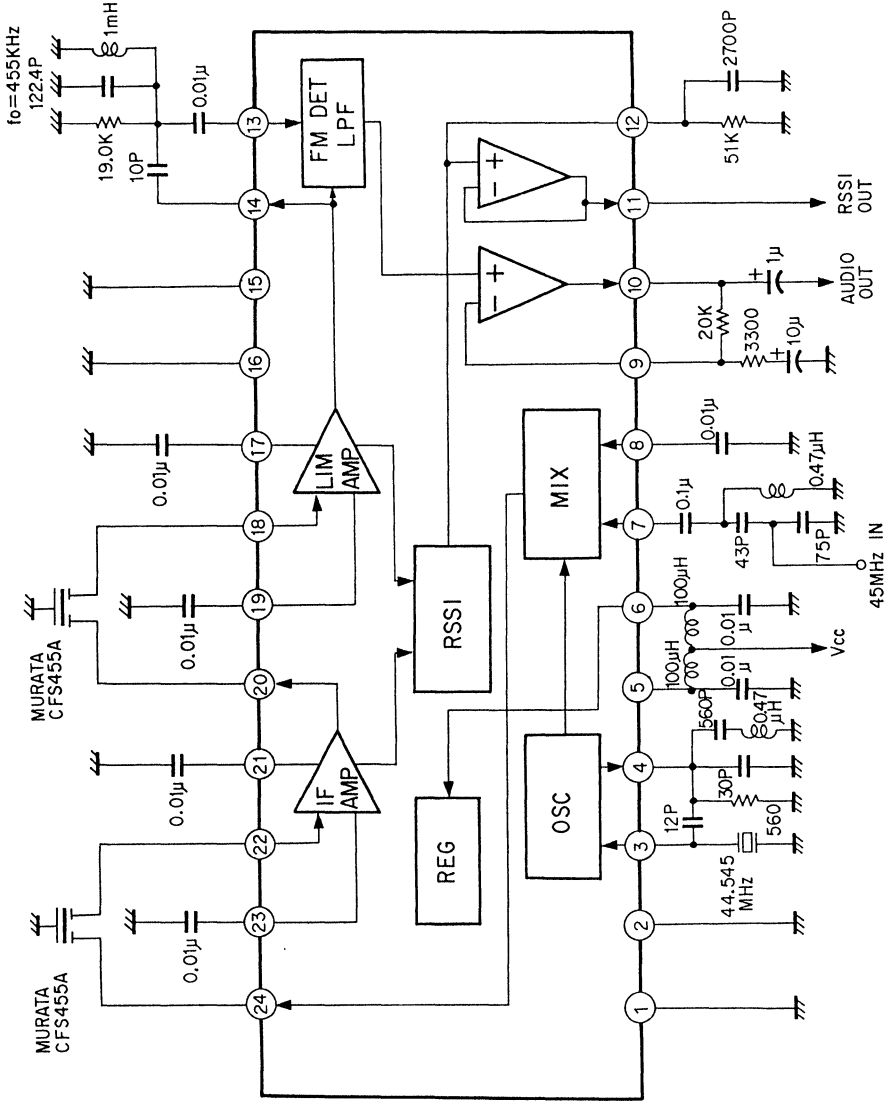
Description of Operation

The signals which have been input from pins ⑦ and ⑧ are mixed with the local oscillation signals from the oscillator in the mixer, and the frequency converted signal is output from pin ㉔. The oscillator is self-oscillated by composing Colpitts type crystal oscillation circuit between pin ③ and ④. In addition, it is possible to apply a local oscillation signal to pin ③ from the external circuit. After the bandwidth is limited by BPF, the mixer output is amplified by IF amplifier and output from pin ⑳. The IF amplifier output is limited its bandwidth again, and amplitude limited by the limiter and output from pin ⑭. The limiter amplifier output is phase-shifted by LC resonance circuit, etc., and audio signal is output from pin ⑩ after being quadrature detected.



The RSSI output is the currents corresponding to the input levels at the IF amplifier and the limiter. It is possible to convert a current into a voltage by connecting a proper I. V conversion circuit.

Application Circuit



Note on Use

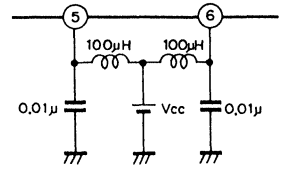
CXA1343M/N have very high at voltage gain, so take care of the following.

1. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C as near to the pins as possible.
2. Connect pin ⑮ and ⑯ (NC) to GND.
3. Separate input line from the output line as far as possible, and make the wiring short.
4. Connect pin ⑧, ㉑, ㉓, ⑰ and ⑲ to GND with capacitor as near to pins as possible.
5. The GND impedance should be as low as possible.
6. It is better to separate statically the input from the output of the limiter with shielding plate.

Notes on Application

1) Power supply

The CXA1343M/N have a voltage regulator within the IC, so these have wide operating power supply range (+4.5 to +9.5V ; Typ : 5.0V). There is little change in characteristics in the operating range. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C. (See Fig. right)



Power supply decoupling

2) Oscillator

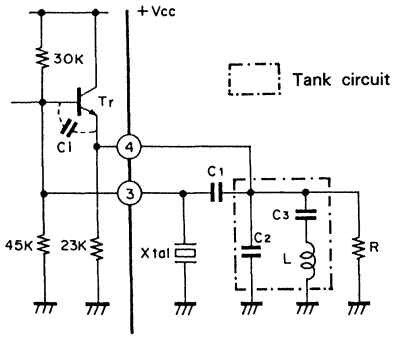
The method to use oscillator of CXA1343M/N is the following :

(a) Method to input from pin ③ with the self-excitation oscillation signal by composing a crystal oscillation circuit of the Colpitts type to pin ③ and ④.

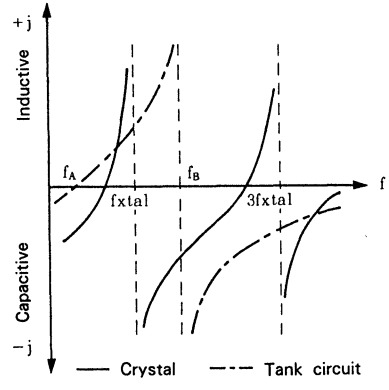
(b) Method to input directly the external local oscillation signal to pin ③.

< Crystal oscillation circuit >

The 3rd overtone crystal oscillation circuit of the Colpitts type is Fig. bellow.



Colpitts type crystal oscillation circuit



Reactance characteristics

The conditions of the 3rd overtone oscillation of this oscillation circuit are the following.

- The parallel resonance frequency (f_B) of the tank circuit should be smaller than the 3rd oscillation frequency ($3f_{xtal}$) and the serial resonance frequency (f_A) should be smaller than the basic oscillation frequency (f_{xtal}) ($3f_{xtal} > f_B$, $f_{xtal} > f_A$).
- The load capacitance (: C_L) of the crystal should be adequate.
- The f_t of the amplifier (Tr) should be sufficiently larger than $3f_{xtal}$.

The constant is determined so as to satisfy these conditions.
The oscillation level is set at 280 to 890mVrms (Typ : 500mVrms) and adjust the level by changing the resistance value (R). The slight adjustments of the oscillation frequency and oscillation level are performed with C_2 and L.

< In case of direct input >
In case of direct input, connect pin ④ to V_{CC} and input external local oscillation signal to pin ③.
Input level at this point is also 280 to 890mVrms (Typ : 500mVrms).

3) Mixer

Mixer of the CXA1343M/N is a double balance type. Input ports are pin ⑦ and ⑧, and in case of single input, input signal to pin ⑦, and connect pin ⑧ to GND with capacitor. It is possible to use differential input. The standard input level is −110 to −30dBm (0.7 μ to 7.0mVrms), and input through a suitable matching circuit.

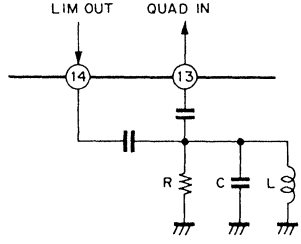
4) Filter

The band-pass filters which are connected between pin ㉔ and ㉒ and between pin ⑳ and ⑱ of the CXA1343M/N are desired to have the specifications as follows.

- Input/output impedance : 1.5k Ω ± 10 %
- Insertion loss (center frequency) : < 6dB

5) Phase shifter

Input to pin ⑬ to shift the phase of the limiter output (pin ⑭) 90° by the RLC parallel resonance circuit or the discriminator, etc. in order to quadrature FM detection. The Fig. below shows the RLC phase shifter. In this case, determine the L and C values so that the 2nd IF signal frequency and the parallel resonance frequency are the same, and the audio output level is determined by R value. RLC Phase shifter or Oscillator is connected between pin ⑬ and ⑭, the phase shifted signal is input to pin ⑬ and demodulated in quadrature detector.



RLC phase shifter

6) Audio output

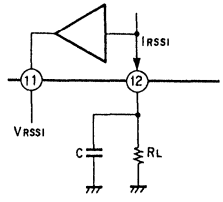
The FM modulated audio signal is demodulated in the prior stage and is output from pin ⑩ (AUDIO OUT). Amplifier gain can be adjusted by connecting an appropriate feedback circuit between this pin and pin ⑪.

7) RSSI

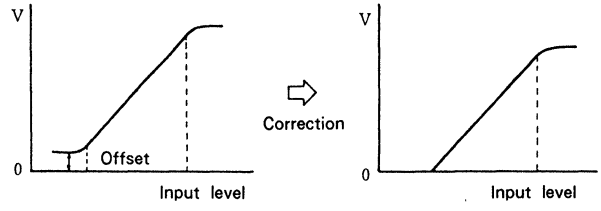
RSSI is a function that detects input signal level. In this CXA1343/N, the current output is converted into voltage by the current/voltage conversion circuit connected to pin 12, then it is output from pin 11. The signal is amplified almost uniformly within the IF input level range from −100 to 0dBm (2.24 μ to 224mVrms). The power supply and temperature effect little on output current. However, the output current is distributed within the range of ±20 % due to the resistance within the IC.

The value of resistances connected to pin ⑫ is determined by the RSSI maximum output current and the allowable maximum voltage of pin ⑫. The RSSI maximum output current is approximately 60 μA (Typ : 45 μA) and the allowable maximum voltage (recommended maximum voltage) is $V_{CC}-1.8V$, select the resistance according to the power supply and the required output voltage. In case the output voltage is required above $V_{CC}-1.8V$, amplify a voltage using an operational amplifier, etc.

The AMPS defines that the RSSI output voltage increases monotonously from 0. The CXA1343M/N have an offset of approximately 0.3 to 0.5V ($V_{CC}=5V$ $R_L=51k\Omega$), so perform from 0V with the offset correction circuit.

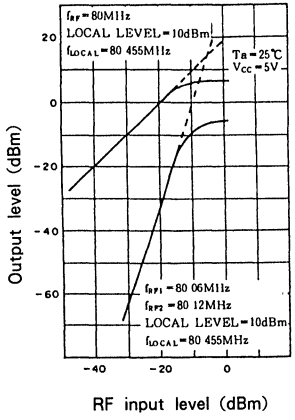


Current to voltage conversion with resistance of RSSI output

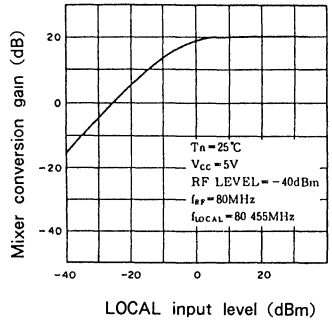


Offset correction of RSSI output voltage

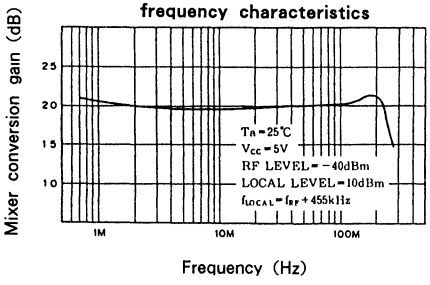
Mixer I/O characteristics and the 3rd order intercepting point



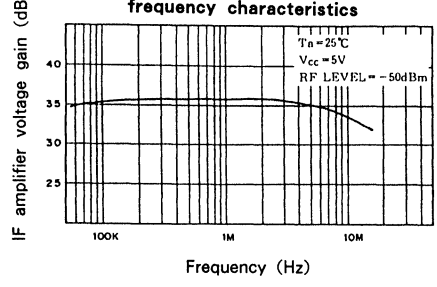
Mixer conversion gain vs. Local input level



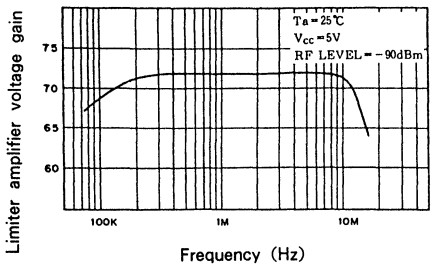
Mixer conversion gain frequency characteristics



IF amplifier voltage gain frequency characteristics

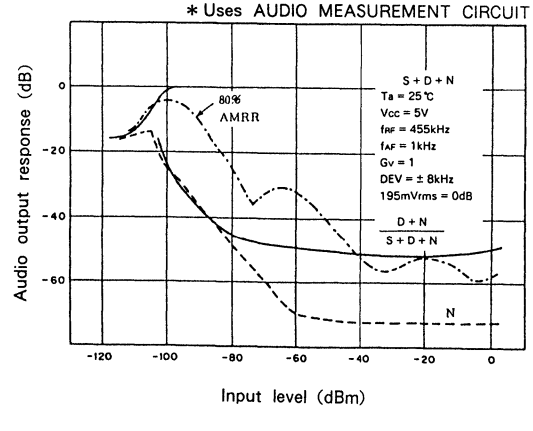


Limiter voltage gain frequency characteristics

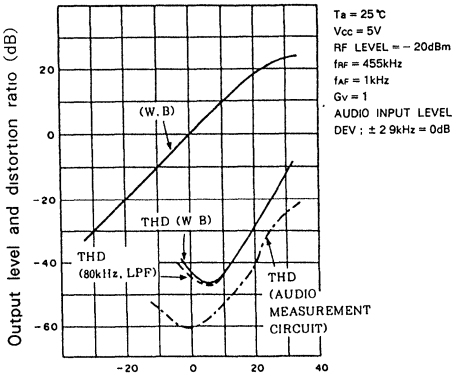


Audio demodulation characteristics (IF IN/Audio OUT)

* Uses AUDIO MEASUREMENT CIRCUIT

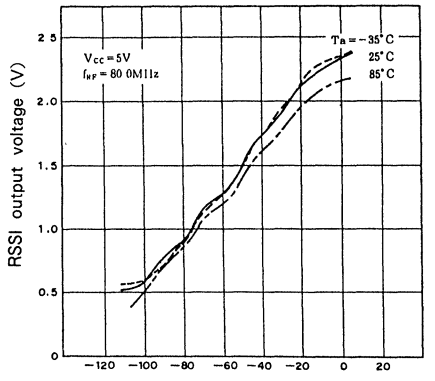


Audio I/O characteristics



Audio input level (dB)

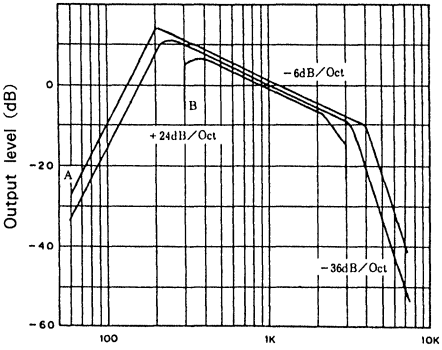
RSSI characteristics (MIX IN/RSSI OUT)



Input level (dBm)

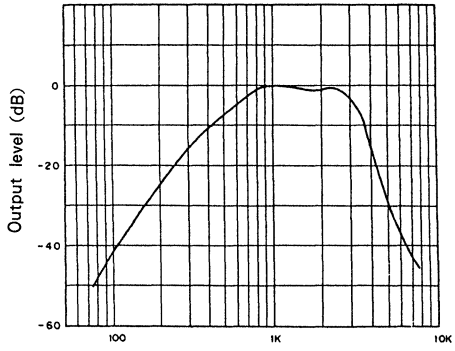
RX-audio filter frequency characteristics

(A − B ; AMPS Typ.) (BPF + DEEMP)



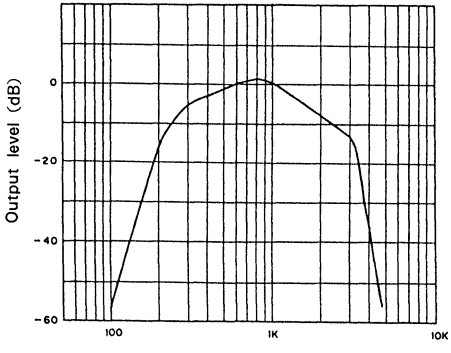
Frequency (Hz)

C-message filter frequency characteristics



Frequency (Hz)

Audio measurement circuit frequency characteristics



Frequency (Hz)

SONY

CXA1183M

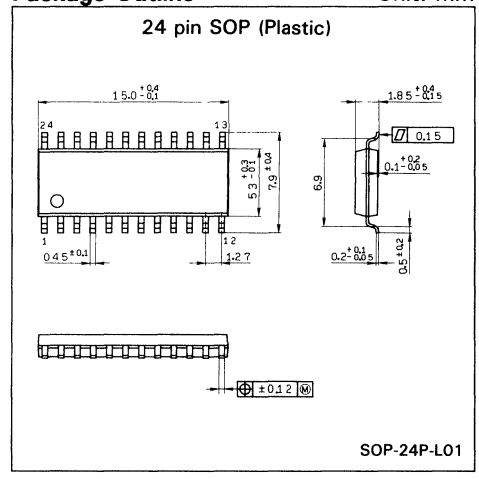
Low-voltage FM IF Amplifier

Description

CXA1183M is a monolithic IC designed for FM communication devices such as cordless telephones. It contains among others, a jamming detection function, mixer, IF limiter, FM detector and squelch circuit.

Package Outline

Unit: mm



Features

- Low operating voltage: (1.8 to 6.0 V)
- Low power consumption: (3.5 mA at 3.6 V)
- Built-in JAM detection function (JAM DET)
- Fewer external parts

Functions

- Mixer
- Local oscillator
- IF limiter
- FM detector
- Squelch circuit
- Receiving Signal Strength Indicator (RSSI)
- Jamming detection (JAM DET)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

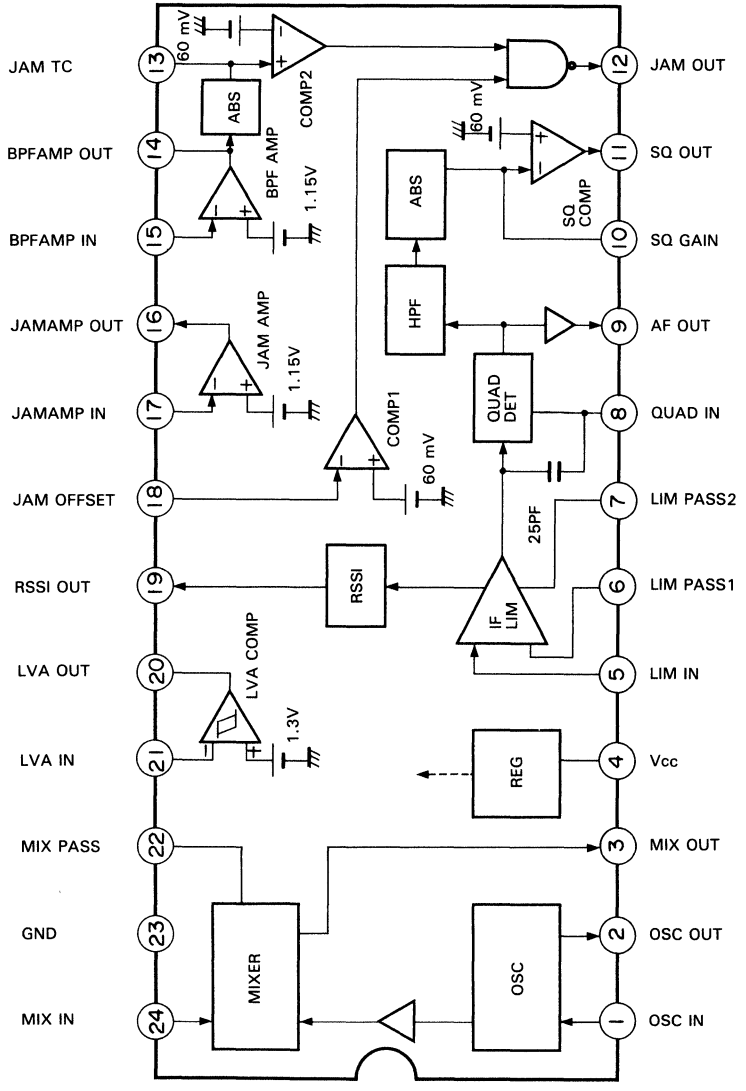
• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

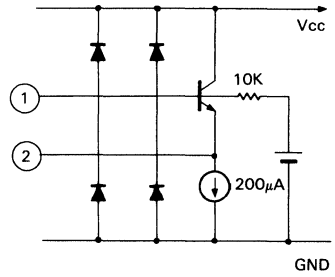
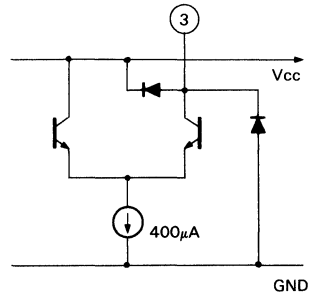
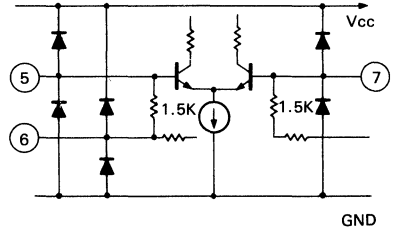
• Supply voltage	Vcc	1.8 to 6.0	V

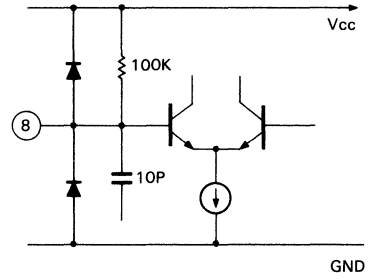
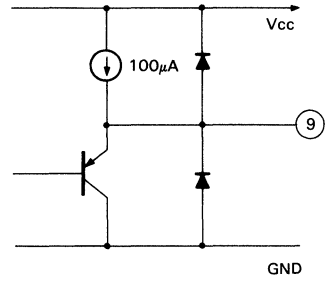
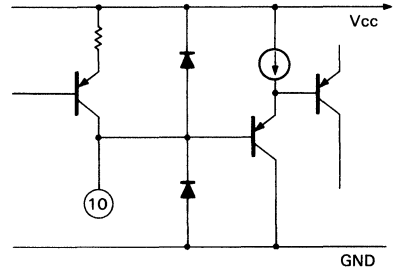
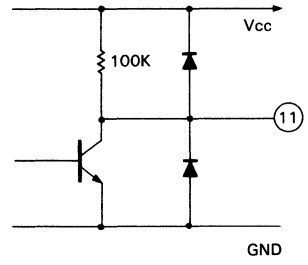
E89233-TO

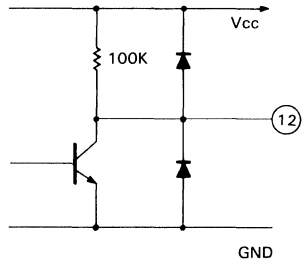
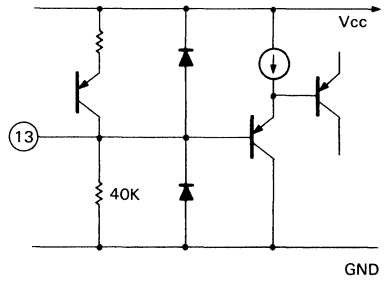
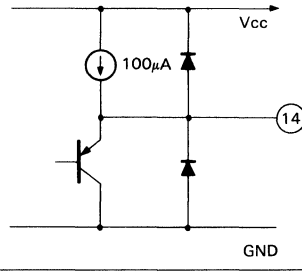
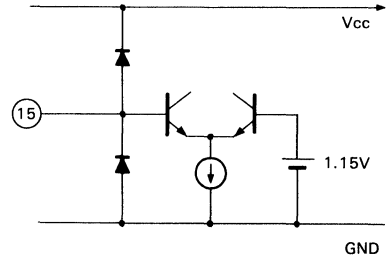
Block Diagram and Pin Configuration (Top View)

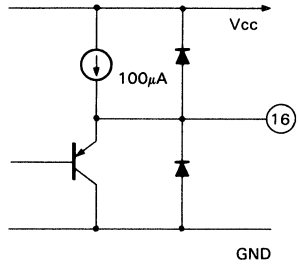
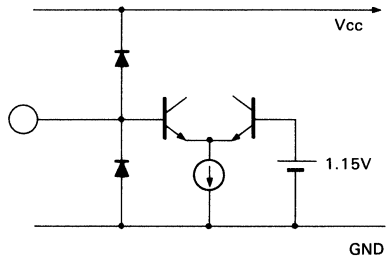
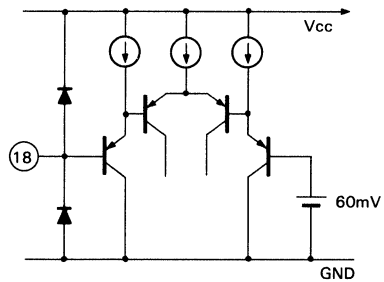
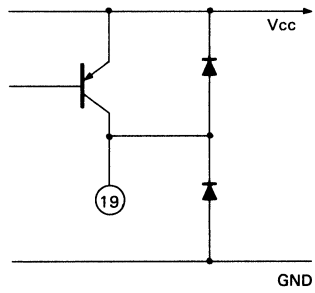


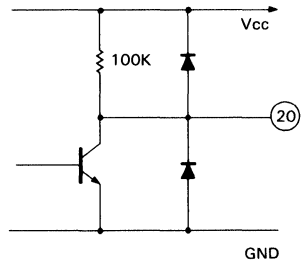
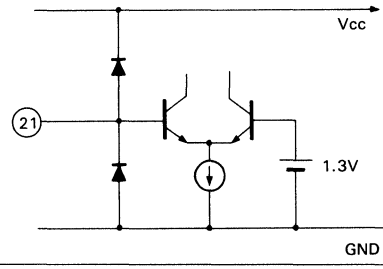
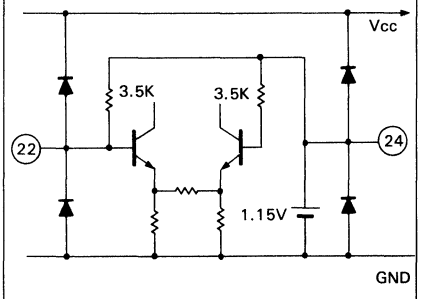
Pin Description and Equivalent Circuit

No.	Symbol	Voltage (Typ.) V	Equivalent circuit	Description
1 2	OSC IN OSC OUT	1.13V 0.42V		Connected to a crystal oscillator to form a Colpitts type oscillating circuit. When an external oscillator is used, connect to pin No. 1.
3	MIX OUT	3.3V		Mixer output pin. As open-collector output, it is connected to a load resistor of 1.5 kΩ.
4	Vcc	3.6V		Supply pin.
5 6 7	LIM IN LIM PASS1 LIM PASS2	2.95V 2.95V 2.95V		Pin 5: Limiter input pin. Pins 6, 7: Bypass capacitor connecting pins.

No.	Symbol	Voltage (Typ.) V	Equivalent circuit	Description
8	QUAD IN	3.6V		Connected to a quadrature detector resonance circuit.
9	AF OUT	1.15V		FM detected signals are output.
10	SQ GAIN	0V		Sets the gain and time constant of the squelch circuit.
11	SQ OUT	3.6V		Squelch circuit output pin. Turns to L when AF OUT S/N ratio deteriorates.

No	Symbol	Voltage (Typ.) V	Equivalent circuit	Description
12	JAM OUT	3 6V		JAM DET output pin. The output turns to "L" when a jamming signal is input.
13	JAM TC	0V		Sets the time constant of JAM DET.
14	BPFAMP OUT	1.15V		Output pin of BPF operational amplifier used in JAM DET
15	BPFAMP IN	1.15V		Input pin of the BPF operational amplifier used in JAM DET.

No.	Symbol	Voltage (Typ.) V	Equivalent circuit	Description
16	JAMAMP OUT	1.15V		Output pin of the operational amplifier, which determines the sensitivity of JAM DET.
17	JAMAMP IN	1.15V		Input pin of the operational amplifier, which determines the sensitivity of JAM DET.
18	JAM OFFSET	0V		Input pin of the comparator, which stops JAM DET when the signal is weak.
19	RSSI OUT	0V		RSSI output pin.

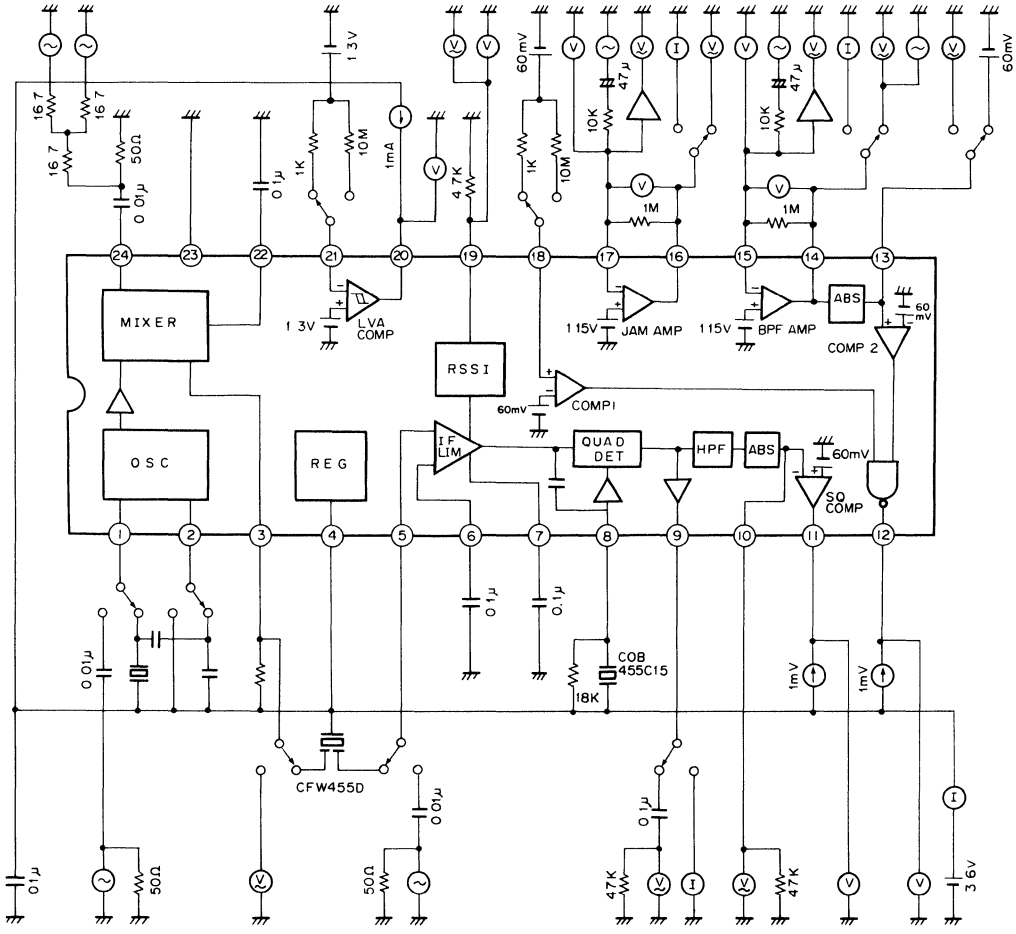
No.	Symbol	Voltage (Typ.) V	Equivalent circuit	Description
20	LVA OUT	0V		Output pin of the low voltage alarm (LVA). Output turns to "H" when Pin 21 voltage goes below 1.3 V.
21	LVA IN			Sets the threshold voltage of LVA comparator.
22 24	MIX PASS MIX IN	1.14V 1.15V		Pin 22 connects mixer bypass capacitor. Pin 24 mixer input pin.
23	GND	0V		Ground pin.

Electrical Characteristics

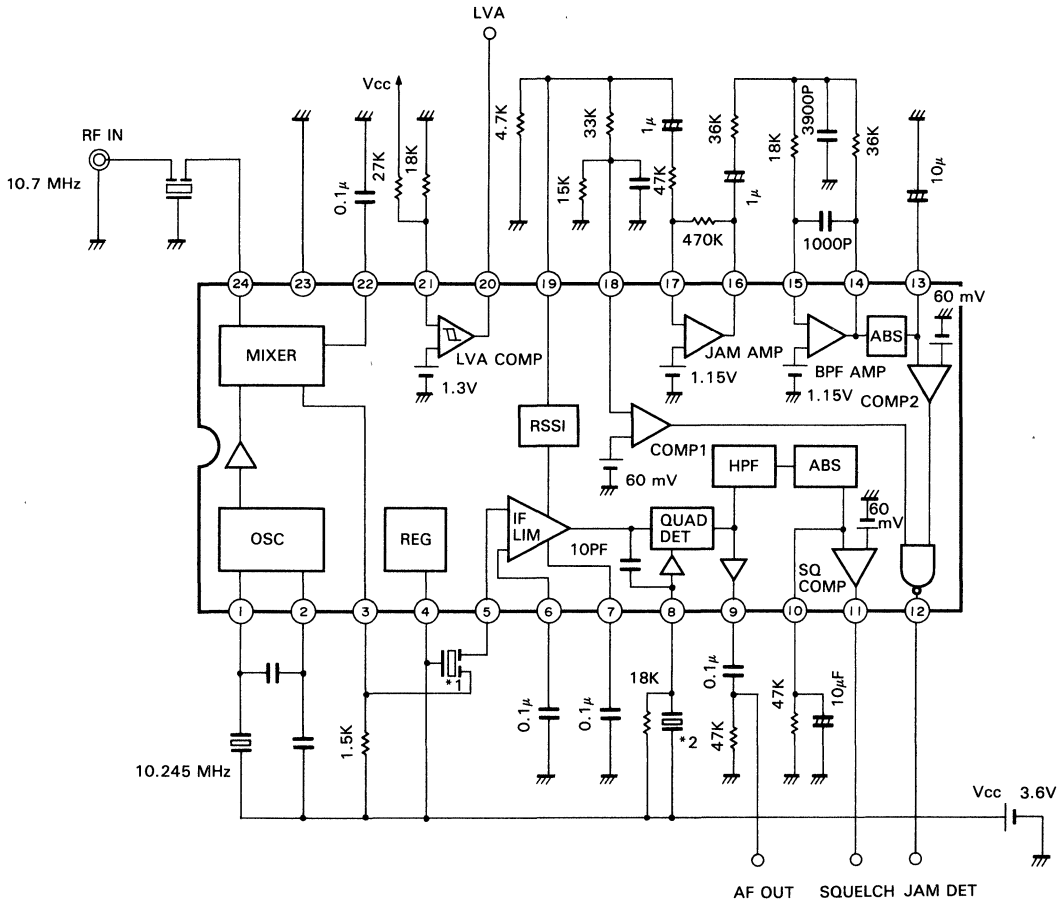
V_{CC} = 3.6V, Vin = 60 dBμ, f_{in} = 10.7 MHz
f_{OSC} = 10.245 MHz, F_{MOD} = 1 kHz, f_{DIV} ± 3 kHz
AM_{MOD} = 30% Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	I_{CC}	V_{in} = 0	2.5	3.5	5.5	mA
Mixer gain	$G_{V\ (MIX)}$	R_L = 1.5 kΩ	16	20	24	dB
Mixer input resistance	$R_{IN\ (MIX)}$		2.8	3.5	4.2	kΩ
Input for −3 dB limiting sensitivity	$V_{IL\ (MIX)}$		—	—	36	dBμ
IF amplifier input resistance	$R_{IN\ (IF)}$		1.2	1.5	1.8	kΩ
Detected output voltage	$V_{O\ (AF)}$		70	90	110	mVrms
Detected output current	$I_{O\ (AF)}$		120	140	200	μA
S/N	S/N		26	—	—	dB
Total harmonic distortion ratio	THD		—	1.0	1.5	%
AM rejection ratio	AMRR		35	—	—	dB
RSSI output voltage	VRSSI 1	$V_{IN(IF)}$ = 30dBμ	—	521	—	mV
	VRSSI 2	$V_{IN(IF)}$ = 60dBμ	460	740	1010	mV
	VRSSI 3	$V_{IN(IF)}$ = 90dBμ	0.71	1.03	1.35	V
HPF cut-off frequency	$f_{C\ (SQ)}$		7	10	13	kHz
Squelch reference voltage	$V_{ref\ (SQ)}$		54	60	78	mV
Squelch low-level output	$V_{OL\ (SQ)}$	I_O = 1 mA	—	—	0.2	V
COMP1 reference voltage	$V_{ref\ (JAML)}$		54	60	78	mV
COMP2 reference voltage	$V_{ref\ (JAMB)}$		54	60	78	mV
COMP1 input bias current	$I_{B\ (JAML)}$		—	—	100	nA
COMP2 input bias current	$I_{B\ (JAMB)}$		—	—	100	nA
JAM amplifier gain	$G_{V\ (JAM)}$		65	85	—	dB
BPF amplifier gain	$G_{V\ (BPF)}$		65	85	—	dB
JAM amplifier output current	$I_{O\ (JAM)}$		70	100	125	μA
BPF amplifier output current	$I_{O\ (BPF)}$		70	100	125	μA
JAM amplifier input bias current	$I_{B(JAM)}$		—	—	100	nA
BPF amplifier input bias current	$I_{B(BPF)}$		—	—	100	nA
JAM output low-level	$V_{OL(JAM)}$	I_O = 1 mA	—	—	0.2	V
LVA reference voltage	$V_{ref\ (LVA)}$		1.18	1.3	1.42	V
LVA hysteresis width	$V_{H\ (LVA)}$		50	65	75	mV
LVA output low-level	$V_{OL\ (LVA)}$	I_O = 1 mA	—	—	0.2	V

Electrical Characteristics Test Circuit



Application Circuit



*1 MURATA CO. CFW455D
*2 MURATA CO. CDB455C15

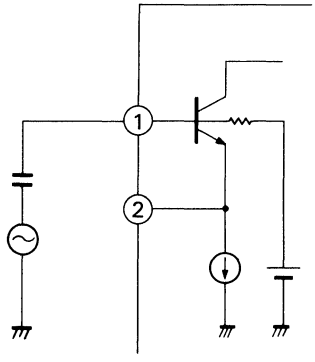
Handling

Handle carefully. IF amplifier features a rather high 100 dB voltage gain with high frequencies.

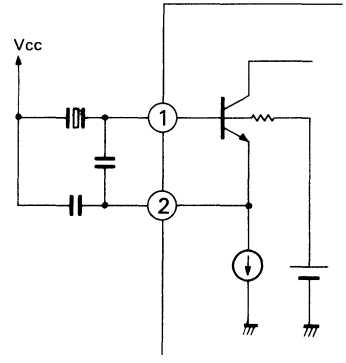
1. Use as thick a pattern as possible and insert a bypass capacitor between the power source and ground.
2. Install the input and output lines as far from each other as possible, and keep wiring as short as possible.
3. Ground the bypass capacitors of the mixer (pin 22) and IF amplifier (pins 6 and 7) as close as possible to their respective pins.
4. The ground pattern impedance should be as low as possible.

Application Notes

1. Oscillator
   The following diagrams show the applications for the CXA1183M oscillator.



(a) How to input local oscillation signals from an external source.



(b) How to form colpitts type oscillation circuits.

2. Mixer
   The CXA1183M mixer is of the double balanced type. Pin 24 is the input pin and pin 22 is grounded through a capacitor.

3. 455 kHz filter
   A 1.5 kΩ I/O impedance band-pass filter is recommended for CXA1183M.

4. IF amplifier
   IF amplifier features a 100 dB high level voltage gain. 455 kHz frequency is mainly used for the IF amplifier AC operation. DC components are cut off by means of Pins 6 and 7 capacitors.

5. QUAD DET
   To compose a quadrature FM detector, an RLC parallel resonance circuit or ceramic discriminator is connected to pin 8.

CXA1183M exclusive ceramic discriminator
CDB455C15 (MURATA CO.)

6. AF OUT
The audio output pin is connected to an emitter-follower circuit. To employ, cut off DC using a capacitor, and keep a 3 kΩ or larger load resistor.

7. Squelch circuit
The squelch circuit can directly drive a CMOS or a small input current device, as it is connected to Vcc, through a 100 kΩ resistance.
The squelch circuit HPF is set to approximately 10 kHz, and the threshold voltage of the comparator is set to approximately 60 mV.
The capacitor and resistor of pin 10 adjust the squelch circuit sensitivity and time constant.

$$R = \frac{Vref \cdot K \cdot Rin}{AF\ (noise)}$$

Time constant $T = C \cdot R$

Vref	60 mV
K	Constant $4\sqrt{2}$
AF (noise)	The noise level at which the squelch operates (peak-to-peak)

The squelch output reverses from high to low as noise increases.

8. LVA (Low Voltage Alarm)
LVA indicates the battery is running out.
Vref is set to approximately 1.3 V (hysteresis is approximately 5%). When the pin 21 voltage drops lower than reference VREF voltage, the output turns from low to high.
LVA can directly drive such a CMOS or a small input current device as it is connected to Vcc through a 100 kΩ resistance.

9. RSSI (Receiving Signal Strength Indicator)
RSSI indicates the input signal level. In CXA1183M, a current is output and this output increases in correspondence with the IF input level increase. Current-voltage conversion through a resistance is required for JAMDET use.

10. JAM DET (Jamming detection)
JAM DET is used to detect jamming using the beat component between the jamming and the desired signals. The JAM DET is used when undesired signals interfere in a conversation on a cordless phone or in other FM communications.

11. COMP1
COMP1 is used to stop JAM DET from operating when the electrical signal is weak. As the reference voltage is set to approximately 60 mV, adjust the operation point using an external resistor.

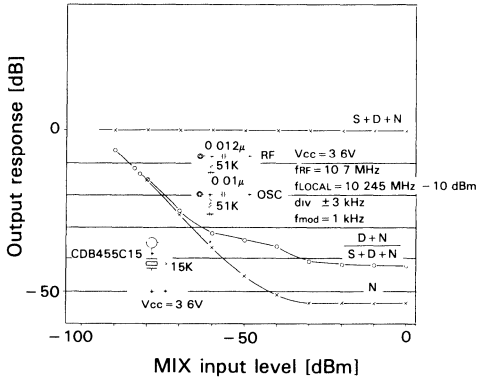
12. COMP2
COMP2 comparator detects the beat component of JAM DET. The reference voltage is set to approximately 60 mV.

13. JAM amplifier
Amplifies the beat components that are between jamming and desired signals. In CXA1183M, as the reference voltage of the comparator used for JAM DET is constant JAM DET sensitivity is set through this JAM amplifier.

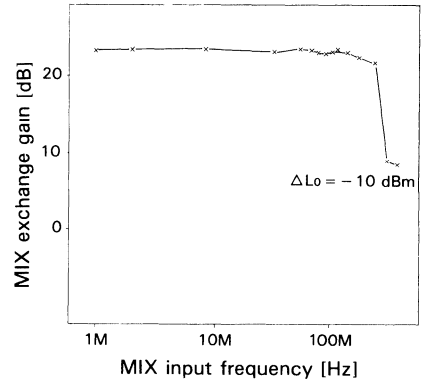
14. BPF amplifier
This is the OP amplifier that forms the active filter. It cuts off noise to maintain steady operation of the JAM DET.

15. ABS (Absolute Value Circuit)
ABS is an Absolute Value Circuit that converts the AC output of JAM DET and squelch circuits into DC output.

CXA1183M Output response



CXA1183M Exchange gain frequency characteristics



SONY CXA1493M/N

FM/IF Amplifier for Cordless Telephone — Advance Information

Description

The CXA1493M/N is an FM IF amplifier designed for cordless telephones. In addition to on-chip AF 3-pole LPF, squelch filter amplifier and meter circuit, the adoption of a 20P VSOP package allows for weight reduction and set shrinkage.

Features

- Built-in AF LPF with variable cutoff possible
- Built-in squelch filter amplifier
- Built-in meter circuit (RSSI)
- Low current consumption (3.8mA at 3.0V)
- Compact package (20pin SOP/VSOP)

Applications

Cordless telephones and other FM communication devices

Structure

Bipolar silicon monolithic IC

CXA1493M	CXA1493N
20pin SOP (Plastic)	20pin VSOP (Plastic)

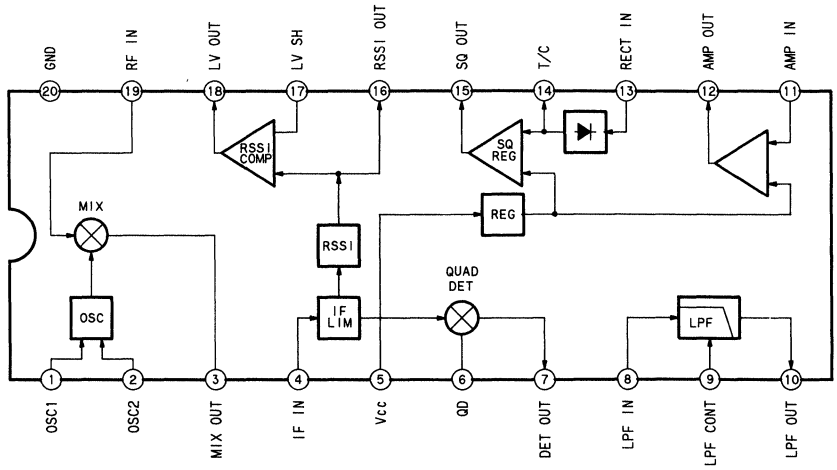
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	14.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	500	mW

Operating Condition

• Supply voltage	V_{CC}	2.7 to 7.0	V

Block Diagram and Pin Configuration (Top View)

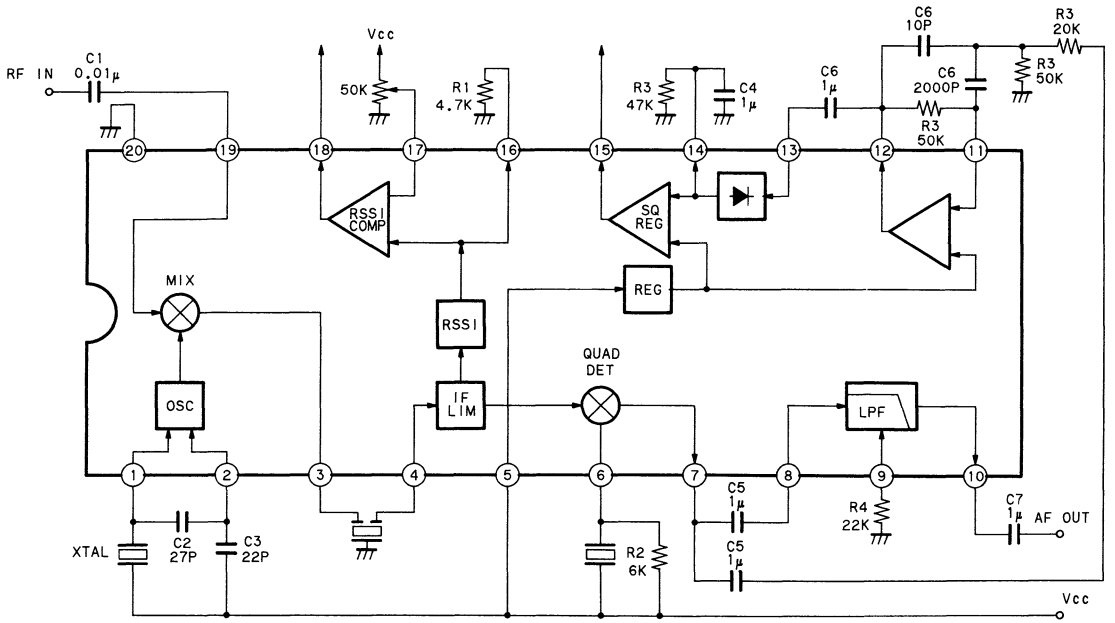


AE90721-HP

Electrical Characteristics (V_{CC}=3.0V, f_C=21.4MHz, f_{MOD}=1kHz, f_{DIV}=3kHz, AM_{MOD}=30%, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	V_{in}=0		3.8		mA
Mixer gain	$G_{V\ (MIX)}$	R_I=2.0kΩ		12		dB
Mixer input resistance	$R_{IN\ (MIX)}$			3.5		kΩ
Limiting sensitivity	$V_{IL\ (MIX)}$			10		dBμ
IF AMP input resistance	$R_{IN\ (IF)}$			2.0		kΩ
Detected output voltage	$V_{O\ (AF)}$			200		mVrms
Detected output current	$I_{O\ (AF)}$			150		μA
S/N ratio	S/N	V_{in}=60dBμ	40			dB
Total harmonic distortion factor	THD			1.0	3.0	%
AM rejection ratio	AMRR	V_{in}=60dBμ	40			dB
RSSI output voltage	V_{RSSI1}	V_{in} (IF)=0dBμ			0.2	V
	V_{RSSI2}	V_{in} (IF)=30dBμ		1.1		V
	V_{RSSI3}	V_{in} (IF)=45dBμ		1.6		V
RSSI dynamic range	D_{RSSI}		45			dB
LPF cutoff frequency variable range			2.0		4.5	kHz
LPF cutoff frequency accuracy	$F_{C\ (LPF)}$		−10		10	%
Squelch low level output	$V_{OL\ (SQ)}$	I_O=0.2mA			0.3	V
RSSI COMP input bias current	$I\ B_{(RSSI)}$				100	nA
SQ COMP input bias current	$I\ B_{(SQ)}$				100	nA

Application Circuit

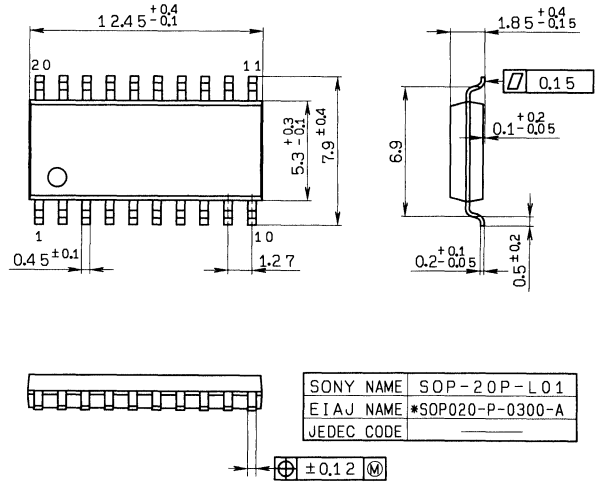


FM IF AMP FOR CORDLESS TELEPHONE

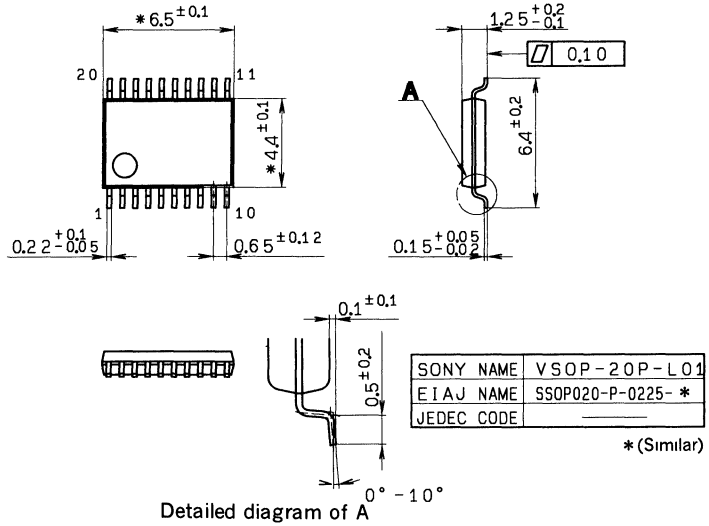
Application circuits shown are typical examples illustrating the operation of the devices Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Package Outline **Unit : mm**

CXA1493M 20pin SOP (Plastic) 300mil 0.3g



CXA1493N 20pin VSOP (Plastic) 225mil



Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY

CXA1184M/N

Low-voltage FM IF Amplifier

Description

CXA1184M and CXA1184N are designed for FM communication devices. They incorporate a paging system, mixer, IF limiter, FM detector, operational amplifier, comparator, and others.

Features

- Low operating voltage 1.0 to 4.0 V
- Low power consumption 2 mA at 1.5 V
- Built-in power source voltage monitor.

Applications

IF Amplifier for Paging System Receiver

Structure

Bipolar silicon monolithic IC

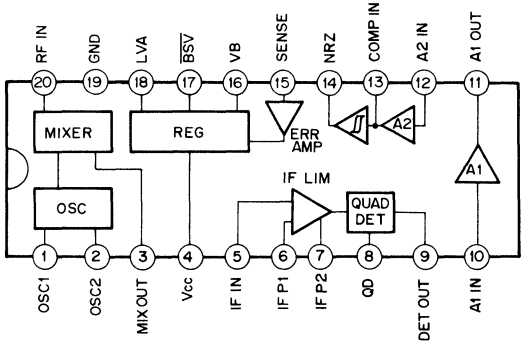
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C

Recommended Operating Conditions

• Supply voltage	Vcc	1.0 to 4.0	V

Block Diagram and Pin Configuration



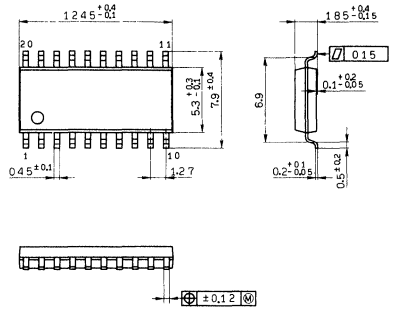
Note) DET · DETECTOR
LIM LIMITTER
REG · REGURATOR
ERR : ERROR CORRECTION

Package Outline

Unit: mm

CXA1184M

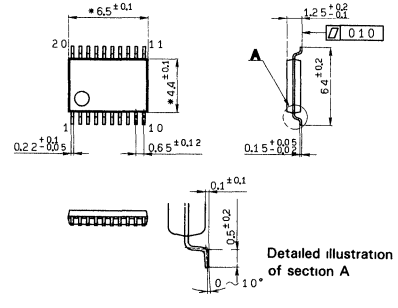
20 pin SOP (Plastic)



SOP-20P-L01

CXA1184N

20 pin VSOP (Plastic)

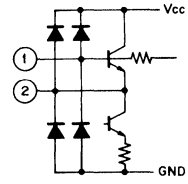
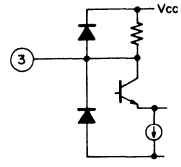
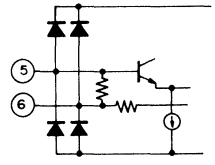
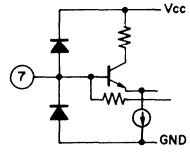
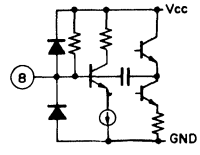


VSOP-20P-L01

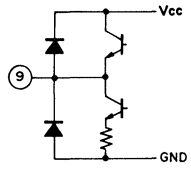
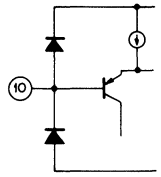
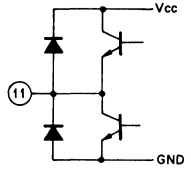
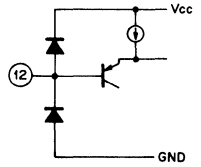
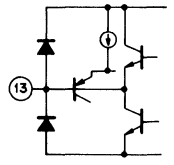
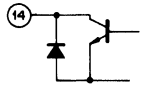
Note: *The dimension with an asterisk does not include residual resin

E88Z43-TO

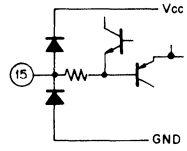
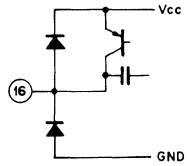
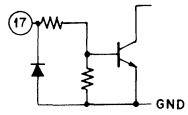
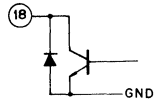
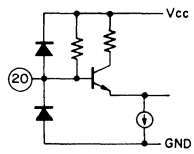
Pin Description

No	Symbol	Equivalent circuit	Description
1	OSC1		Those pins are connected to the external parts of an oscillating circuit. The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Vcc, pins 1 and 2 respectively.
2	OSC2		
3	MIX OUT		Mixer output pin. Connect a 455 kHz ceramic filter between this pin and the IF IN pin.
4	Vcc		Vcc pin.
5	IF IN		Input pin for the IF limiter amplifier.
6	IF P1		Connection pin of the bypass capacitor for the IF limiter amplifier. Connect a capacitor of about 0.047 μF between this pin and ground (or Vcc).
7	IF P2		Connection pin of the bypass capacitor for the IF limiter amplifier. Connect a capacitor of about 0.047μF between this pin and ground (or Vcc).
8	QD		Connected to a quadrature detector phase shifter.

Pin Description

No.	Symbol	Equivalent circuit	Description
9	DET OUT		Recovered signal output.
10	A1 IN		Input pin of inverting OP amplifier A1.
11	A1 OUT		Output pin of OP amplifier A1.
12	A2 IN		Input pin of OP amplifier A2.
13	COMP IN		Input pin of the comparator. This pin is internally connected to the output of OP amplifier A2.
14	NRZ		NRZ (Non Return Zero) output pin.

Pin Description

No	Symbol	Equivalent circuit	Description
15	SENSE		Voltage control pin for external bias supply.
16	VB OUT		Supplies bias voltage to external circuit transistors and others
17	BSV		Reduces IC power consumption Lowering pin voltage below 0.35 V stops IC operation.
18	LVA		Output pin for Low Voltage Alarm (LVA) The pin turns to high impedance when power voltage drops below 1.05 V.
19	GND		Ground pin.
20	RF IN		Mixer input pin.

Electrical Characteristics

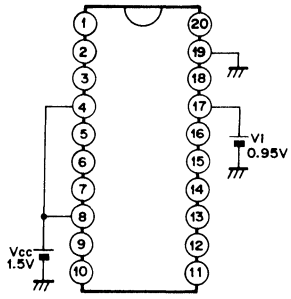
V_{CC} = 1.5 V, Ta = 25°C, f_S = 21.7 MHz,
f_{MOD} = 256 Hz, f_{DIV} = 2.3 kHz, AM$_{MOD}$30%

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption (during operation)	I_{CC}	Test circuit 1	1.2	2.0	2.5	mA
Power consumption (during battery saving)	I_{CCS}	Test circuit 1 VI = 0.3 V	—	—	20	μA
Input for −3 dB Limiting	V_{IN} (LIM)	Test circuit 3	—	7	—	dBμ
AM rejection ratio	AMRR	Vin = 60dBμ Test circuit 3	25	—	—	dB
OP amplifier input bias current	I_{BIAS}	Test circuit 2	—	30	100	nA
OP amplifier open loop gain	A_V	Test circuit 4	45	60	—	dB
OP amplifier output voltage amplitude	V_O	Test circuit 5	0.25	—	—	Vp-p
Comparator hysteresis width	V_{TW}	Test circuit 6	30	40	5.0	mV
NRZ* output leak current	I_{LNRZ}	Test circuit 7	—	—	5.0	μA
NRZ* saturation voltage	V_{SATNRZ}	I_{SINK} = 200μA Test circuit 8	—	—	0.4	V
VB output current	I_{OUT}	V_B = 0.9V	0.1	—	—	mA
VB output voltage	V_{BOUT}	Test circuit 9	0.95	—	—	V
Sense voltage	V_{SEN}	Test circuit 9	85	100	115	mV
LVA threshold voltage	V_{PML}	Test circuit 10	1.05	1.10	1.15	V
LVA hysteresis width	V_{PMTH}	$V_{PMH} - V_{PML}$	40	50	70	mV
LVA output leak current	I_{LLVA}	Test circuit 7	—	—	5.0	μA
LVA saturation voltage	V_{SATLVA}	Test circuit 8	—	—	0.4	V
Recovered signal voltage	V_{DET}	Test circuit 3	10	—	—	mVrms
BSV high level	V_{THBSV}		0.95	—	—	V
BSV low level	V_{TLBSV}		—	—	0.35	V

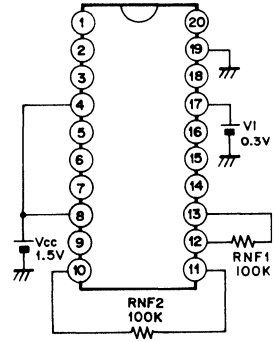
*NRZ: Non Return Zero

Electrical Characteristics Test Circuit

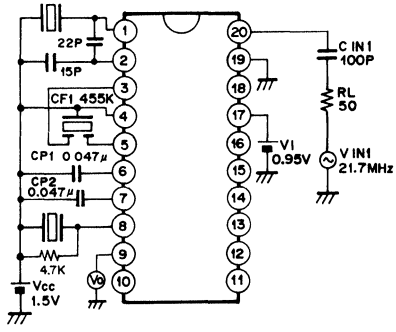
1)



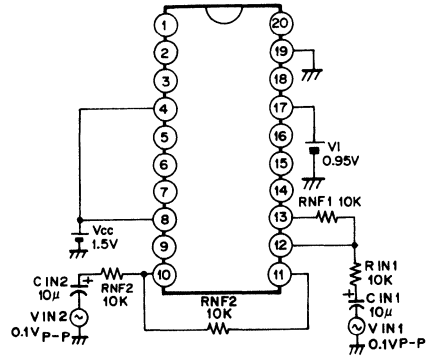
2)



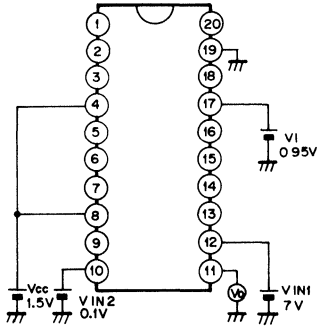
3)



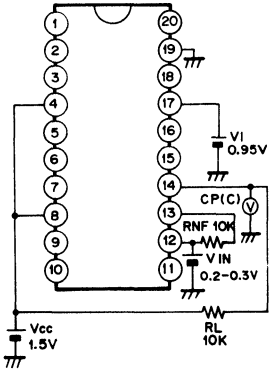
4)



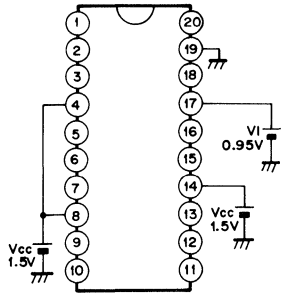
5)



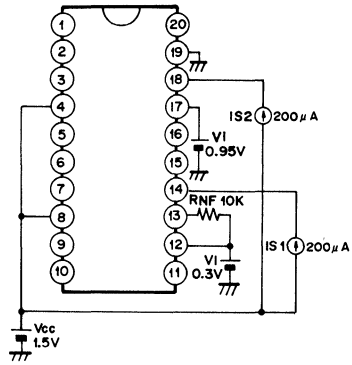
6)



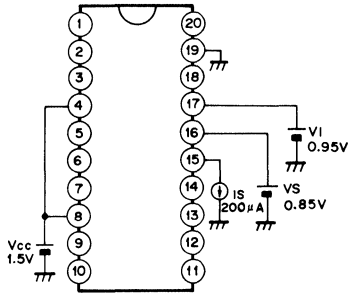
7)


VI
0.95V
Vcc
1.5V
Vcc
1.5V

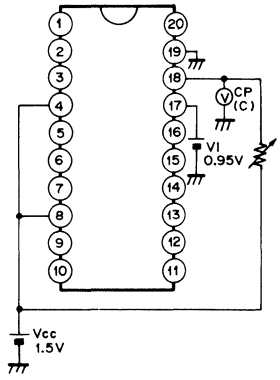
8)


IS2 200μA
VI
0.95V
RNF 10K
IS1 200μA
VI
0.3V
Vcc
1.5V

9)


VI
0.95V
IS
200μA
VS
0.85V
Vcc
1.5V

10)


CP
(C)
VI
0.95V
Vcc
1.5V

Test Method

Input for −3 dB Limiting V_{IN} (LIM)

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 40 dBμ

Here, the value of V_{AC} is specified as V_{AC1}. Next, the signal level V_L is changed to 19dBμ and V_{AC} value is hence specified as V_{AC2}.

$$20 \log \frac{V_{AC1}}{V_{AC2}} < 3 \text{ dB}$$

AM rejection ratio (AMRR)

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 40 dBμ

Here, the value of V_{AC} is specified as V_{AC1}. Next, AM is modified to:

Modulation ratio:	AM_{MOD} = 30%
Modulation frequency:	f_{MOD} = 256 Hz

and the V_{AC} value is hence specified as V_{AC2}.

$$AMRR = 20 \log \frac{V_{AC1}}{V_{AC2}} > 25 \text{ dB}$$

Recovered signal voltage V_{DET}

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 50 dBμ

Here, the value of the pin-9 output voltage is expressed as V_{DET}.

OP amplifier output voltage amplitude V_O (OP)

Use test circuit 5. If output voltage V is expressed as V_1 when V_{IN} is 0.1 V, and as V_2 when V_{IN} is 0.3 V, it follows that:

$$V_O = V_1 - V_2$$

Comparator hysteresis width V_{TW}
Use test circuit 6.
Vary V_{IN} between 0.1 to 0.3 V.
Specify V_{IN} voltage, as V_1 when (C) voltage changes from low to high.
Similarly, specify V_{IN} voltage as V_2, when (C) voltage changes from high to low.

Therefore: VHY $V_{TW} = V_1 - V_2$

LVA threshold voltage V_{PML} and recovery voltage V_{PMH}
Use test circuit 10.
Vary power voltage V_{CC} from 1.3 to 0.95 V.
Specify V_{CC} as V_{PML}, when (C) voltage changes from low to high.
Similarly, specify V_{CC} as V_{PMH}, when (C) voltage changes from high to low.

Design Reference Values

Ta = 25°C, Vcc = 1.4V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Mixer input resistance	$R_{IN\ (MIX)}$		1.3	1.6	1.9	kΩ
Mixer input capacity	$C_{IN\ (MIX)}$		–	4.0	–	pF
Mixer output resistance	$R_{OUT\ (MIX)}$		1.44	1.8	2.16	kΩ
IF input resistance	$R_{IN\ (IF)}$		1.44	1.8	2.16	kΩ
IF gain stability	$G_{S\ (IF)}$	Ta = −20 to +60°C	–	±6	–	dB
Detector output resistance	$R_{OUT\ (QD)}$		1.28	1.6	2.0	kΩ
OP amplifier max. input voltage	V_{INMAX}		–	–	0.39	V
OP amplifier min. input voltage	V_{INMIN}		0.05	–	–	V
Comparator max. input voltage	$V_{INMAXCOMP}$		–	–	0.39	V
Comparator min. input voltage	$V_{INMINCOMP}$		0.05	–	–	V
OP amplifier off-set voltage	V_{OFS}		–	–	3	mV

1) Supply

This IC incorporates a regulation and is designed to operate steadily on a wide range of supply voltage from 1.0 to 4.0 V.

Decoupling on the wiring to the supply pin (pin 4) should be done as close to the pin as possible.

2) Oscillation input

Oscillation input method

a) Using pins 1 and 2, input self-excited oscillation signals through the composition of a Colpitts type crystal oscillating circuit.

b) Input local oscillation signals to pin 1 directly.

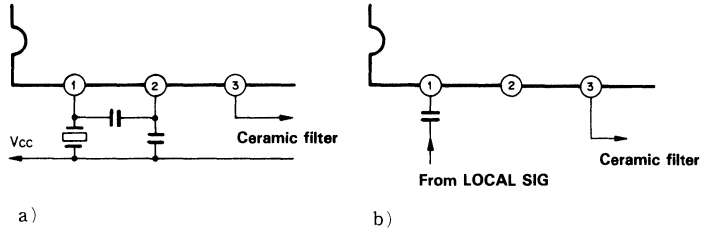


Fig. 1

3) Mixer

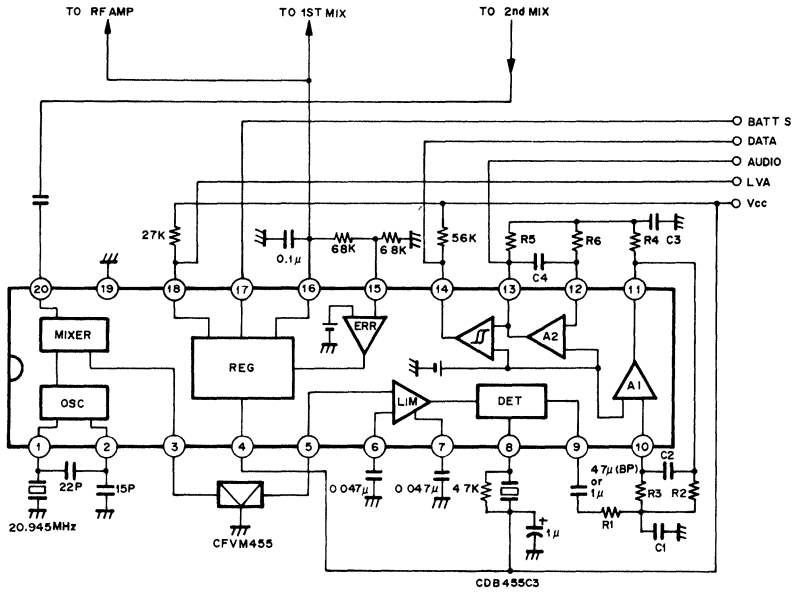
This IC's mixer is of the double balance type. Pin 24 is the input pin. Input through a suitable alignment circuit. Input impedance is at 1.6kΩ. The mixer output features a built-in 1.6kΩ load resistance at pin 3.

4) IF filter

The filter to be connected between this IC's mixer and the IF limiter should have the following specifications.

I/O impedance : 1.6kΩ ±10%
Band width : Use according to application

Application Circuit



5) IF limiter

The IF limiter of this IC features a gain of about 100 dB. To this effect, the following points should be considered for the wiring connecting IF limiter input pin (pin 5) and decoupling capacitor pins (pins 6 and 7).

a) Wiring to mixer output (pin 3) and IF limiter input (pin 5) should be as short and as far apart as possible to avoid neutral interference.

b) Connect a decoupling capacitor to IF limiter IF P1 (pin 6) and IF P2 (pin 7).
Here the decoupling capacitor should be positioned as close as possible to each pin and the wiring be as short as can be.

c) As IF limiter output shows at QD (pin 8), keep the wiring connected to QD pin,R, L, C and the ceramic discriminator as short as possible. Interference to the mixer output, IF limiter input and others must be kept to a minimum.

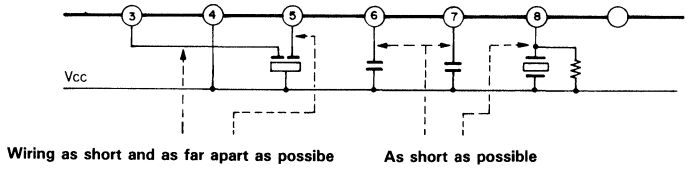


Fig. 2

6) Detector

The detector is of the quadrature type. To phase shift, either R, L, C resonance circuit or the ceramic discriminator is connected to pin 8.

The phase capacitor of the quadrature detector is built-in. FM (FSK) signals demodulated by this detector have their high frequency components dropped by the LPF formed inside from CRs, to be output at DET OUT (pin 9). DET OUT output impedance is about 3kΩ.

For the CXA1184M ceramic discriminator, CDB455C3 (Murata Production) is recommended.

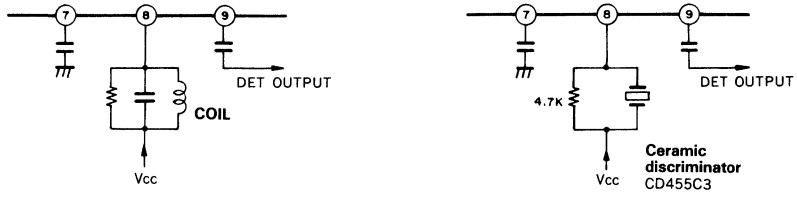


Fig. 3

7) OP AMP, NRZ OUT

This IC has 2 built-in operation amplifiers.

One of these operation amplifiers is connected inside the IC to NRZ comparator.

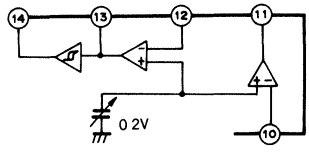


Fig. 4

Making use of these operation amplifiers an LPF or the sort is made up to eliminate noise during signal demodulation and input to the following NRZ comparator.

NRZ comparator molds the waveform of input signals to output them as square waves. NRZ comparator output is an open collector.

Accordingly as CPU is a CMOS, in case the supply voltage differs, by following the method indicated in Fig. 5 direct interfacing becomes possible.

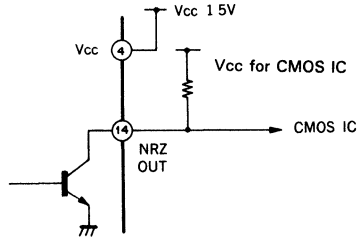


Fig. 5

8) VB SENSE, VB OUT

This controls the base bias of the external transistor. Pin 16 VB OUT can be used as the previous amplifier 1st mixer bias.

9) LVA OUT

When supply voltage turns low this pin turns to High (Open). Output is an open collector and, similarly as NRX OUT, can directly drive CMOS.

This LVA setting voltage is at 1.1V ±50 mV with hysterisis versus supply voltage.

Hysterisis width is at 50mV ±10 mV.

10) $\overline{\text{BSV}}$

By turning this pin to low, this IC's operation can be stopped.

This pin can also be directly connected to CMOS.

Consumption current with $\overline{\text{BSV}}$ is 20 μA (at 1.5 V) and below.

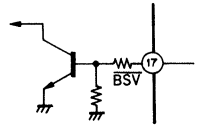
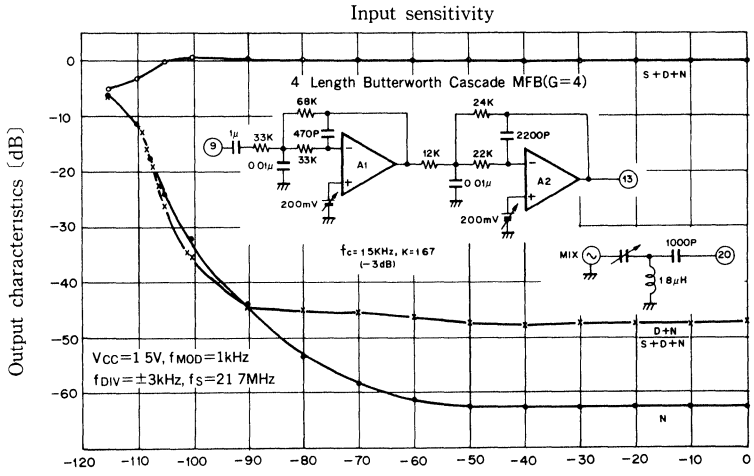
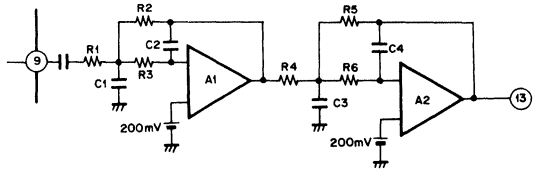


Fig. 6

Mixer input signal vs Output characteristics

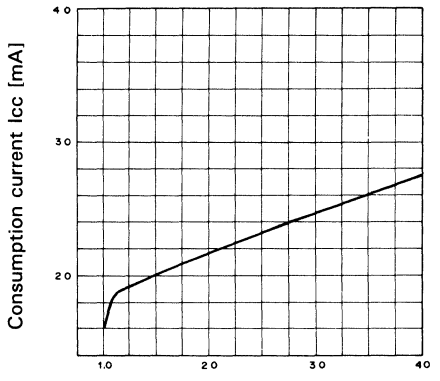


4th LP Butterworth cascade MFB constant using OP1 and OP2 inside CXA1184M.

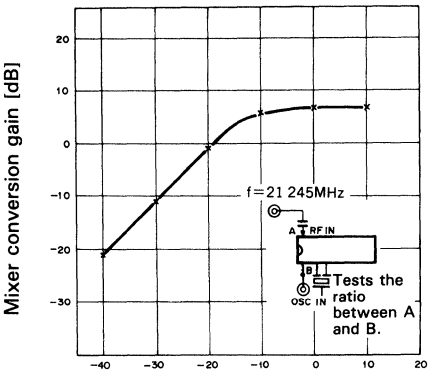


f_{MOD}	256Hz
f_c (−3dB)	400Hz
A1Gain	1
A2Gain	4
R1	47KΩ
R2	47KΩ
R3	22KΩ
R4	47KΩ
R5	180KΩ
R6	33KΩ
C1	0.0012μF
C2	680pF
C3	0.015μF
C4	1200pF

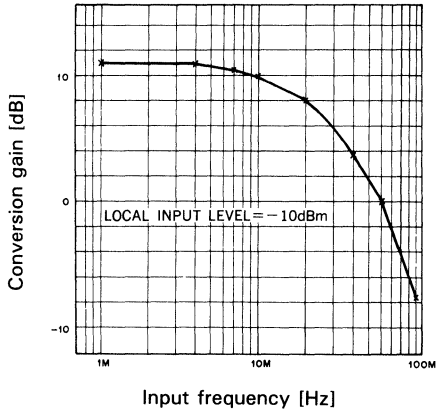
Supply voltage vs. Consumption Current



Logical input level vs. Mixer conversion



Input frequency vs. Conversion gain



SONY®

CXA1474M/N

Ultra Low Current Consumption FM IF Amplifier for Pager

Advance Information

Description

The CXA1474M/N is an ultra low current consumption FM IF amplifier, employed the latest bipolar process. It is suitable for radio communication system requested low current consumption and compact sets.

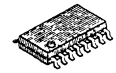
Features

- Ultra low current consumption 500μA (V_{CC}=1.5V Typ.)
- Low voltage operation V_{CC}=1.0 to 4.0V
- Fewer external parts
- Built-in reference power supply for operational amplifier and comparator
- Ultra small package 16pin VSOP

Functions

- 2nd IF, LIM
- FM detector
- 2 operational amplifiers for 4 length LPF
- FSK comparator (invertible)
- Regular OUT for RF, 1st MIX
- Power saving function
- Low voltage alarm

CXA1474M	CXA1474N
16pin SOP (Plastic)	16pin VSOP (Plastic)



Applications

Single super pager (Japan)
Low power double super pager (Overseas)

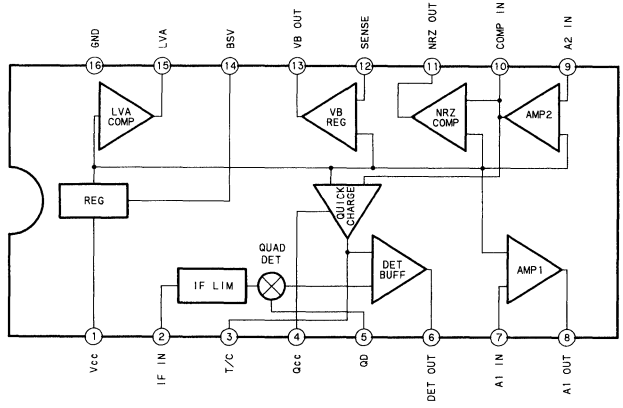
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C

Operating Condition

• Supply voltage	V_{CC}	1.0 to 4.0	V

Block Diagram



AE89850A0X-HP

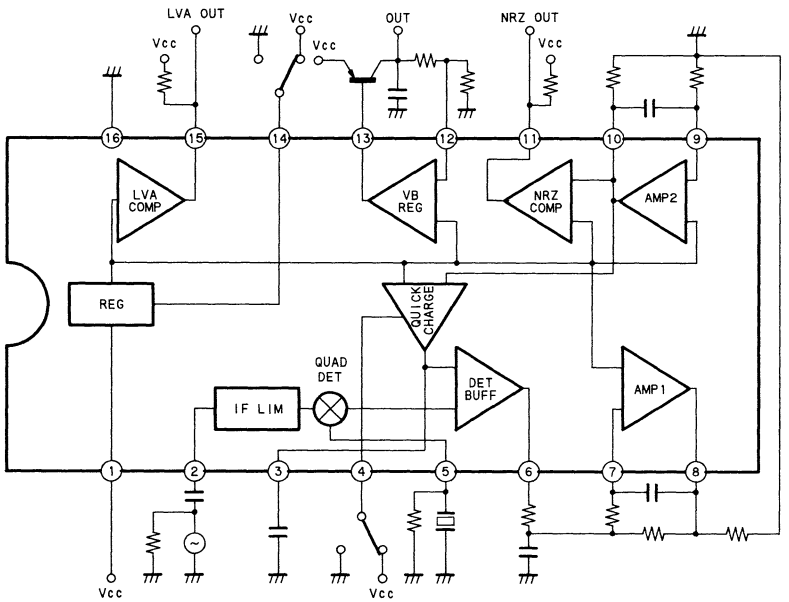
Electrical Characteristics (V_{CC}=1.5V, Ta=25°C, fs=455kHz, f_{MOD}=256Hz, f_{DIV}=2.3kHz, AM_{MOD}=30%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	I_{CC}	OPERATION	350	500	650	μA
Power consumption	I_{CCS}	POWER SAVE			20	μA
Input limiting	V_{IN}			7		dBμ
AM rejection ratio	AMRR	V_{IN}=60dBμ	25			dB
Input bias current	I_{BIAS}			30	100	μA
OP amp open loop gain	A_V		45	60		dB
OP amp output voltage amplitude	V_O		0.25			Vp-p
Comparator hysteresis width	V_{TW}			20		mV
NRZ output leak current	I_{LNRZ}				5.0	μA
NRZ saturation voltage	V_{SATNRZ}				0.4	V
VB output current	I_{OUT}		10			mA
VB output voltage	V_{BOUT}		0.9			V
Sense voltage	V_{SEN}		180	200	220	mV
LVA threshold voltage	V_{PML}		1.05	1.10	1.15	V
LVA hysteresis width	V_{PMTH}		40	50	70	mV
LVA output leak current	I_{LLVA}				5.0	μA
LVA saturation voltage	V_{SATLVA}				0.4	V
Recovered signal voltage	V_{DET}		15	20	25	mVrms
BSV high level	V_{THBSV}		0.95			V
BSV low level	V_{TLBSV}				0.35	V

Design Reference Values

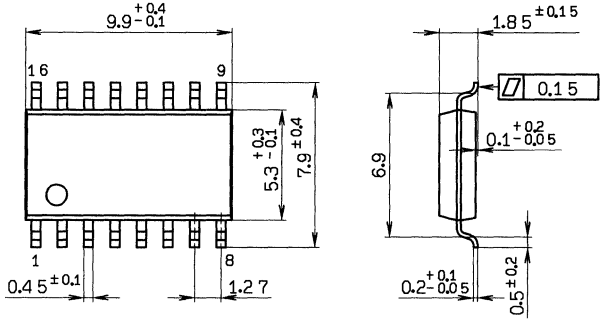
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IF input resistance	R_{IN}(IF)		1.6	2.0	2.4	kΩ
IF gain stability	GS (IF)	Ta=−20 to 60°C	−6		+6	dB
Detector output resistance	R_{OUT}(QD)			−	200	Ω
OP amp MAX input voltage	$V_{IN\ MAX}$		0.39			V
OP amp MIN input voltage	$V_{IN\ MIN}$				0.05	V
Comparator MAX input voltage	$V_{IN\ MAXCOMP}$		0.39			V
Comparator MIN input voltage	$V_{IN\ MINCOMP}$				0.05	V
OP amp offset voltage	V_{OFS}				3	mV

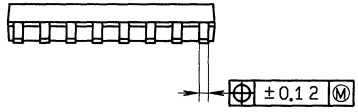
Test Circuit



Package Outline Unit : mm

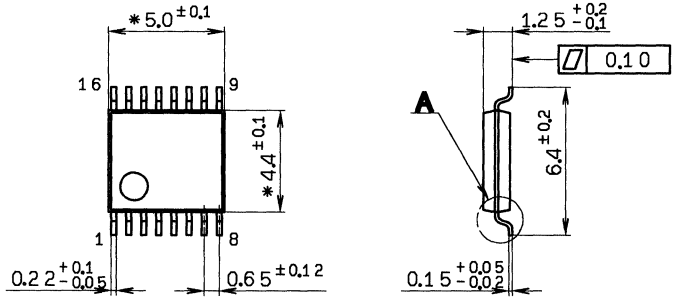
CXA1474M 16pin SOP (Plastic) 300mil 0.2g

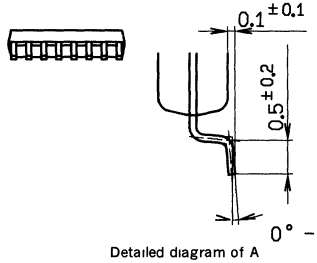




SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

CXA1474N 16pin VSOP (Plastic) 225mil





Detailed diagram of A

SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225- *
JEDEC CODE	———

*(Similar)

Dimensions marked with * do not include resin residue

SONY®

CXA1484M/N

Low Current Consumption FM IF Amplifier for Double Super Pager

Advance Information

Description

The CXA1484M/N is a low current consumption FM IF amplifier employed the latest bipolar process. It is suitable for double super pager because of internal 2nd MIX and OSC.

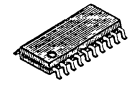
Features

- Ultra low current consumption 1.4mA (V_{CC}=1.5V Typ.)
- Built-in 2nd MIX and OSC
- Low voltage operation V_{CC}=1.0 to 4.0V
- Fewer external parts
- Built-in reference power supply for operational amplifier and comparator
- Ultra small package 20pin VSOP
- CXA1184M/N pin replaceable

Functions

- 2nd MIX and OSC
- 2nd IF and LIM
- FM detector
- 2 operation amplifiers for 4 length LPF
- FSK comparator (invertable)
- Power saving function
- Low voltage alarm

CXA1484M	CXA1484N
20pin SOP (Plastic)	20pin VSOP (Plastic)



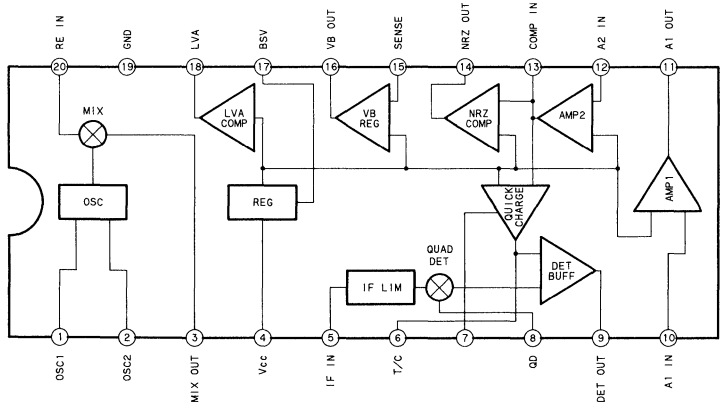
Applications

Double super pager (Overseas)

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C

Block Diagram



AE89851A0X-HP

Electrical Characteristics

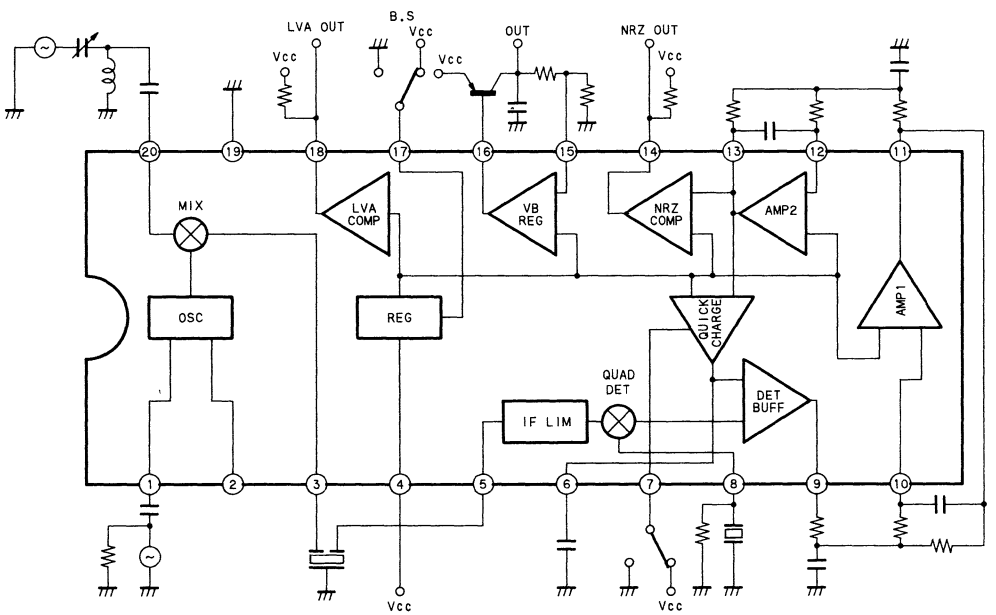
(V_{CC}=1.5V, Ta=25°C, fs=21.4MHz, f_{MOD}=256Hz, f_{DIV}=2.3kHz, AM_{MOD}=30%)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	I_{CC}		1.0	1.4	1.8	mA
Power consumption	I_{CCS}				20	μA
Input limiting	V_{IN}			7		dBμ
AM rejection ratio	AMRR	V_{IN}=60dBμ	25			dB
Input bias current	I_{BIAS}			30	100	μA
OP amp open loop gain	A_V		45	60		dB
OP amp output voltage amplitude	V_O		0.25			Vp-p
Comparator hysteresis width	V_{TW}			20		mV
NRZ output leak current	I_{LNRZ}				5.0	μA
NRZ saturation voltage	V_{SATNRZ}				0.4	V
VB output current	I_{OUT}		10			mA
VB output voltage	V_{BOUT}		0.9			V
Sense voltage	V_{SEN}		180	200	220	mV
LVA threshold voltage	V_{PML}		1.05	1.10	1.15	V
LVA hysteresis width	V_{PMTH}		40	50	70	mV
LVA output leak current	I_{LLVA}				5.0	μA
LVA saturation voltage	V_{SATLVA}				0.4	V
Recovered signal voltage	V_{DET}		15	20	25	mVrms
BSV high level	V_{THBSV}		0.95			V
BSV low level	V_{TLBSV}				0.35	V

Design Reference Values

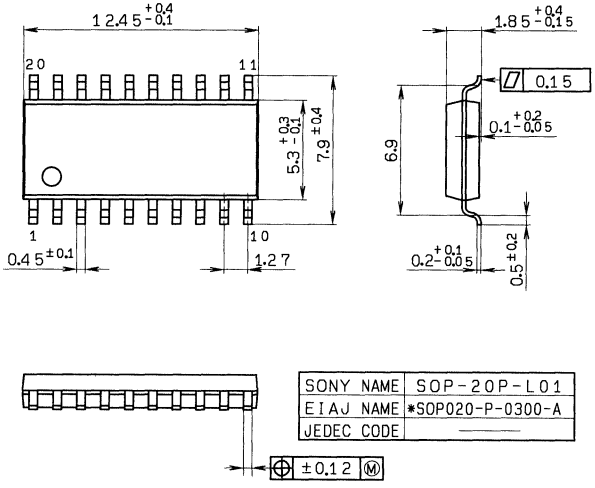
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
MIXER input resistance	R_{IN}(MIX)		1.6	2.0	2.4	kΩ
MIXER input capacity	C_{IN}(MIX)			3.0		pF
MIXER output resistance	R_{OUT}(MIX)		1.6	2.0	2.4	kΩ
IF input resistance	R_{IN}(IF)		1.6	2.0	2.4	kΩ
IF gain stability	G_S (IF)	Ta=−20 to +60°C	−6		+6	dB
Detector output resistance	R_{OUT}(QD)			−	200	Ω
OP amp MAX input voltage	$V_{IN\ MAX}$		0.39			V
OP amp MIN input voltage	$V_{IN\ MIN}$				0.05	V
Comparator MAX input voltage	$V_{IN\ MAXCOMP}$		0.39			V
Comparator MIN input voltage	$V_{IN\ MINCOMP}$				0.05	V
OP amp offset voltage	V_{OFS}				3	mV

Test Circuit



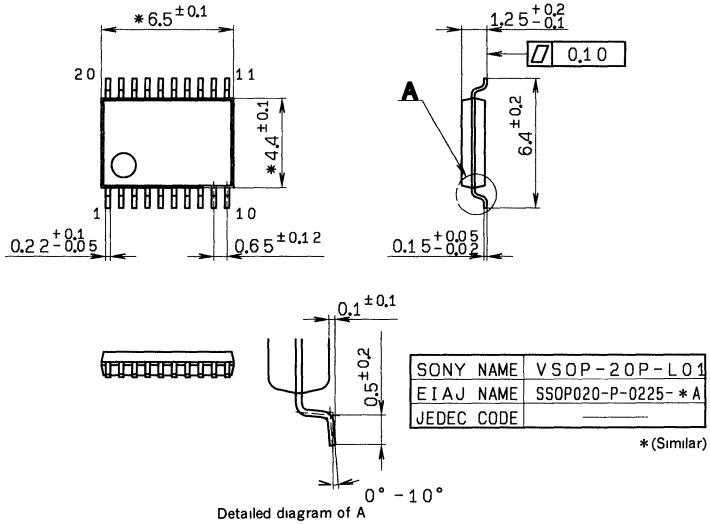
Package Outline Unit : mm

CXA1484M 20pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-20P-L01
EIAJ NAME	*SOP020-P-0300-A
JEDEC CODE	———

CXA1484N 20pin VSOP (Plastic) 225mil

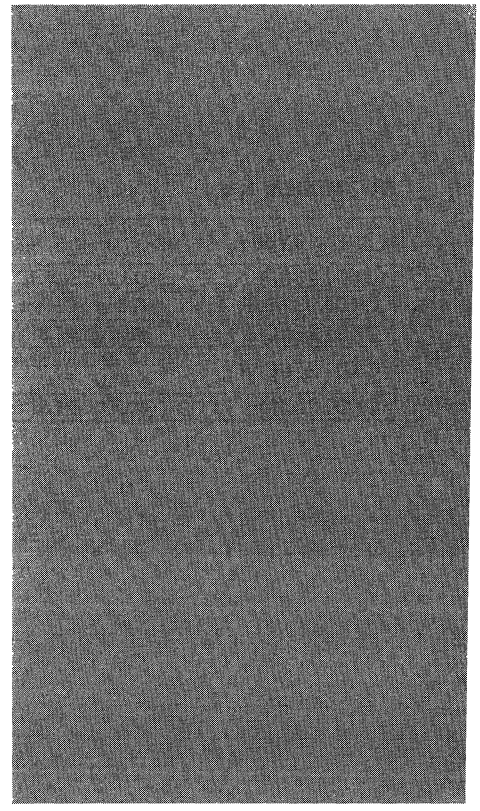


SONY NAME	VSOP-20P-L01
EIAJ NAME	SSOP020-P-0225-*A
JEDEC CODE	———

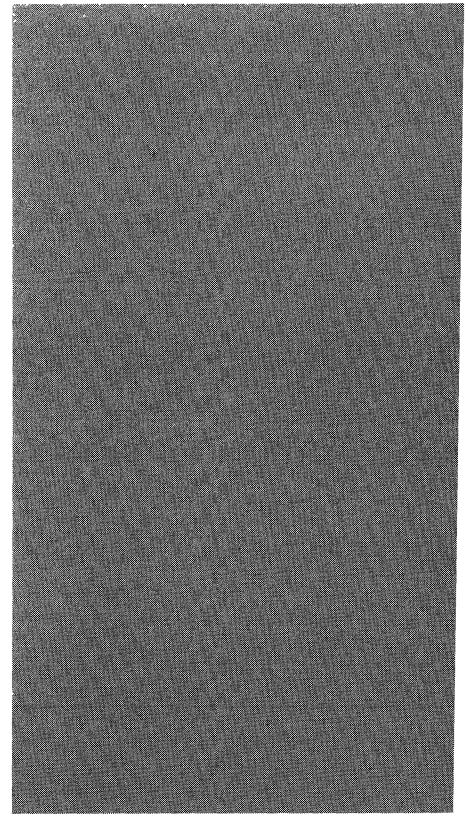
*(Similar)

Detailed diagram of A

Dimensions marked with * do not include resin residue



MODEM ICs



2) MODEM ICs

Type	Function		Page
CXD1230M	DATA SCF IC for AMPS/TACS cellular radio		113
CXD1237Q/R	1 chip SCF for AMPS/TACS/DOC cellular radio	(NEW)	129
CXD1231Q-Z	MODEM LSI for AMPS/TACS cellular radio		147
CXD1270Q/R	MODEM LSI for AMPS/TACS cellular radio built in DTMF	(NEW)	155
CXD1233M	MODEM LSI for cordless phone		166

(New): New device

SONY

CXD1230M

Cellular Radio Telephone Filter IC

Description

CXD1230M is a filter IC developed for cellular radio telephone. Usage in conjunction with DATA • SAT LSI CXD1231Q-Z provides a modem.

Features

- Adoption of switched capacitor technology realizes substantial filter shrinkage.
- Conforms with North American AMPS standards and British TACS standards.
- 5V single supply operation.
- Low consumption [37.5mW (Typ.) 5V during operation]

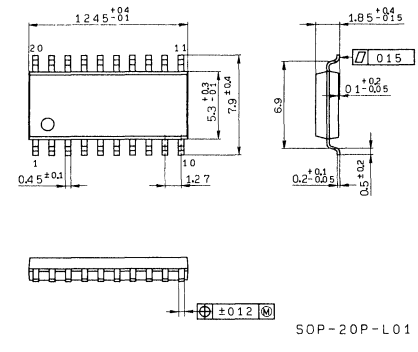
Functions

- Received WIDE BAND DATA filtering.
- Received SAT filtering.
- Received SAT PLL lock detection.
- Transmitted WIDE BAND DATA, ST, SAT, addition.
- Transmitted WIDE BAND DATA, ST, SAT, filtering.

Package Outline

Unit : mm

20 pin SOP (Plastic)



Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

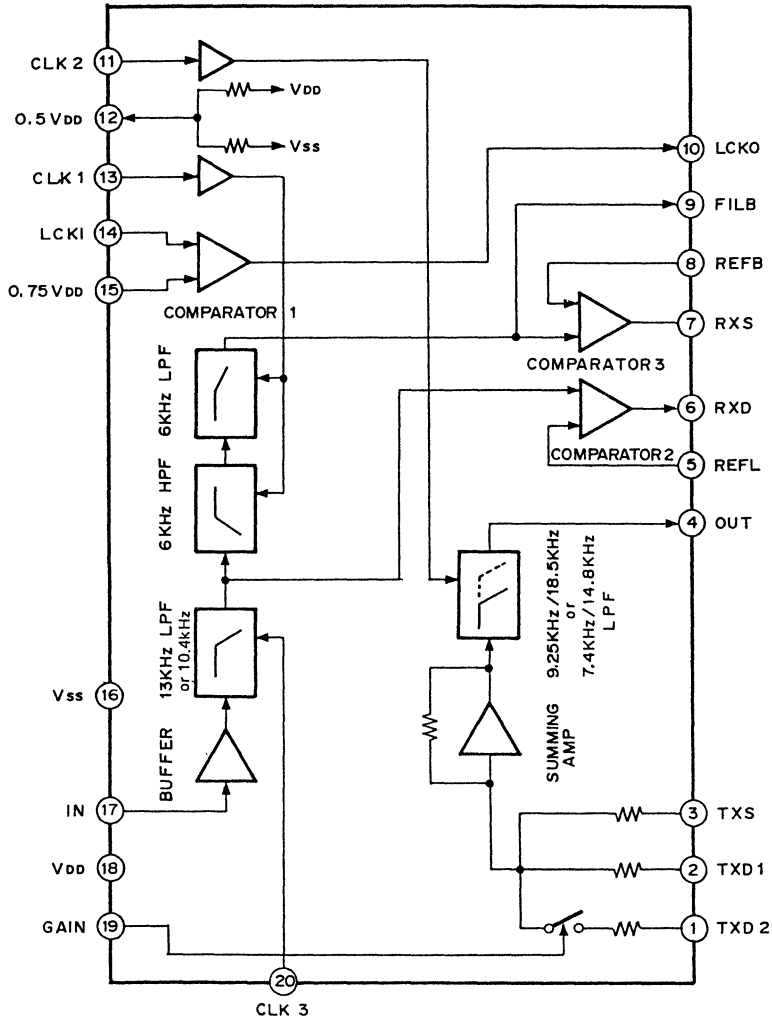
• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

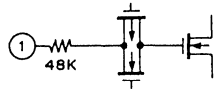
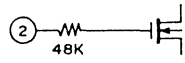
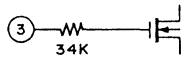
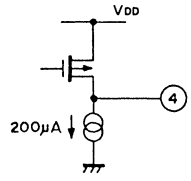
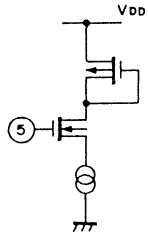
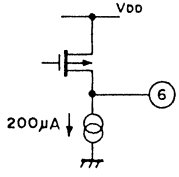
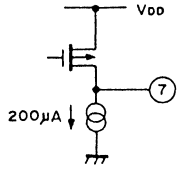
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	−34 to +75	°C

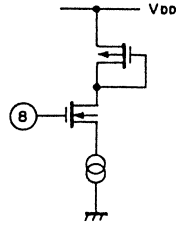
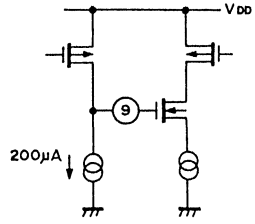
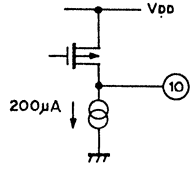
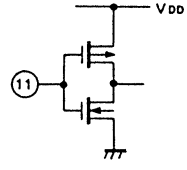
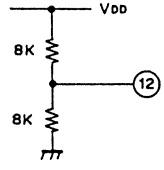
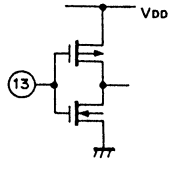
71229-ST

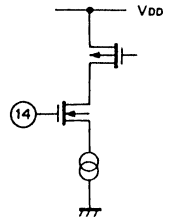
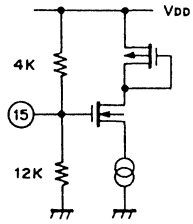
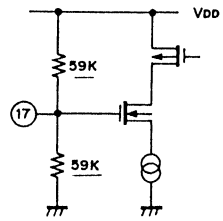
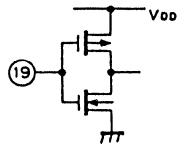
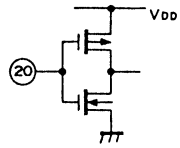
Block Diagram



Pin Description and Equivalent Circuit

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
1	TXD2		I		Input pin 1 for transmission of WIDE BAND DATA and ST from mobile station to land station.
2	TXD1		I		Input pin 2 for transmission of WIDE BAND DATA and ST from mobile station to land station.
3	TXS		I		Input pin for transmission of SAT from mobile station to land station.
4	OUT		O		Output pin for Transfer LPF (low pass filter) with variable cutoff frequency.
5	REFL		I		Comparator reference voltage input pin for WIDE BAND DATA received by mobile station from land station. Eliminates LPF output offset for received WIDE BAND DATA by means of 1 external capacitance.
6	RXD		O		Comparator output pin for WIDE BAND DATA received by mobile station fromland station. When LPF for received WIDE BAND DATA output voltage exceeds reference voltage (pin5), output level of this pin goes from "low" to "high."
7	RXS		O		Comparator output pin for SAT received by mobile station from land station. When 6kHz LPF for received SAT output voltage exceeds reference voltage (pin 8), output level of this pin goes from "low" to "high."

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
8	REFB		I		Comparator reference voltage input pin for SAT received by mobile station from land station. Eliminates 6kHz LPF output offset for received SAT, by means of 1 external capacitance.
9	FILB		O		6kHz LPF output pin for SAT received by mobile station from land station. Connected to the comparator input used to receive SAT.
10	LCKO		O		Comparator output pin for PLL lock detection of received SAT. When input voltage (pin 14) exceeds reference voltage (pin 15), output level of this pin goes from "low" to "high."
11	CLK2		I		Clock input pin of transfer LPF with variable cutoff frequency. Cut off frequency in AMPS mode with 400kHz input is 18.5kHz ; with 200kHz input it is 9.25kHz. In TACS mode with 320kHz input cutoff frequency is 14.8kHz ; with 160kHz input it is 7.4kHz.
12	0.5VDD	2.5V	O		Internal operational amplifiers virtual ground level output pin. Output voltage of this pin will be half that of the supplied voltage. An external capacitance of 3.3 is required as a ripple filter.
13	CLK1		I		Clock input pin for 6kHz HPF (high pass filter) of received SAT and 6kHz LPF. Input clock frequency is 400kHz in both AMPS mode and TACS modes.

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
14	LCKI		I		Input pin for comparator used to detect PLL lock of received SAT.
15	0.75V_{DD}	3.75V	I		Reference voltage input pin for comparator used to detect PLL lock of received SAT. This pin is biased at 3/4 of the supplied voltage. An external capacitance of 3.3 is required as ripple filter.
16	V_{SS}				Ground pin
17	IN	2.5V	I		Input pin for WIDE BAND DATA and SAT received by mobile station from land station. Connected to voltage follower with input biased at half that of supplied voltage.
18	V_{DD}				Supply voltage pin
19	GAIN		I		Gain switching input pin for WIDE BAND DATA and ST to be transmitted. Input level must be "low" for ST transmission, and "high" for data transmission.
20	CLK3		I		Clock input pin for received WIDE BAND DATA LPF. In AMPS mode 400kHz, while in TACS mode 320kHz is input.

Note) 1. Pin voltage value is at V_{DD}=5V.
2. Resistance and current values are at Typ.

Electrical Characteristics

See electrical characteristics test circuits 1 to 3
Ta=25℃, V_{DD}=5V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption		I_{DD}			7.5	10.0	mA
Input voltage	Received signal input	IN				1.0	Vp-p
	Transmitted signal input 1	TXD1				0.7	Vp-p
	Transmitted signal input 2	TXD2				0.7	Vp-p
	Transmitted signal input 3	TXS				1.0	Vp-p
Input impedance	Received signal input	Z_{IN}		24	29		kΩ
	Transmitted signal input 1	Z_{TXD1}		40	48		kΩ
	Transmitted signal input 2	Z_{TXD2}		40	48		kΩ
	Transmitted signal input 3	Z_{TXS}		30	34		kΩ
Output voltage	7kHz band pass filter	FILB				1.0	Vp-p
	9kHz/18kHz low pass filter	OUT				2.0	Vp-p
	Comparator reference voltage	REF		3.55	3.75	3.90	V
	Analog reference voltage	AREF		2.35	2.50	2.65	V
Gain	Transmitted signal input 1	G_{TXD1}		−3.4	−2.9	−2.4	dB
	Transmitted signal input 2	G_{TXD2}		−3.4	−2.9	−2.4	dB
	Transmitted signal input 3	G_{TXS}		−0.5	0	+0.5	dB
Blocking range attenuation	Received data filter 1		AMPS mode, 13kHz, 1Vp-p input	−3.85	−3.35	−2.85	dB
	Received data filter 2		TACS mode 10.6kHz, 1Vp-p input	−3.56	−3.06	−2.56	dB
	Received SAT filter 1		AMPS mode 3kHz, 1Vp-p input	−23.0	−22.57	−21.07	dB
			AMPS mode 7kHz, 1Vp-p input	−0.05	0	+0.05	dB
			AMPS mode 12kHz, 1Vp-p input	−9.40	−8.90	−8.40	dB
	Received SAT filter 2		TACS mode 3kHz, 1Vp-p input	−27.88	−26.38	−24.00	dB
			TACS mode 7kHz, 1Vp-p input	−0.05	0	+0.05	dB
			TACS mode 12kHz, 1Vp-p input	−13.00	−12.28	−11.78	dB
	Transmitted filter 1		AMPS mode CLK2=400kHz 18.5kHz, 0.5Vp-p input	−3.08	−2.58	−2.08	dB
			AMPS mode CLK2=200kHz 9.25kHz, 0.5Vp-p input	−2.93	−2.43	−1.93	dB

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Blocking range attenuation	Transmitted filter 2		TACS mode CLK2=320kHz 15.4kHz, 0.5Vp-p input	−3.51	−3.01	−2.51	dB
			TACS mode CLK2=160kHz 7.7kHz, 0.5Vp-p input	−3.61	−3.11	−2.61	dB

Electrical Characteristics Test Circuit 1 (Frequency Characteristics, Output Voltage)

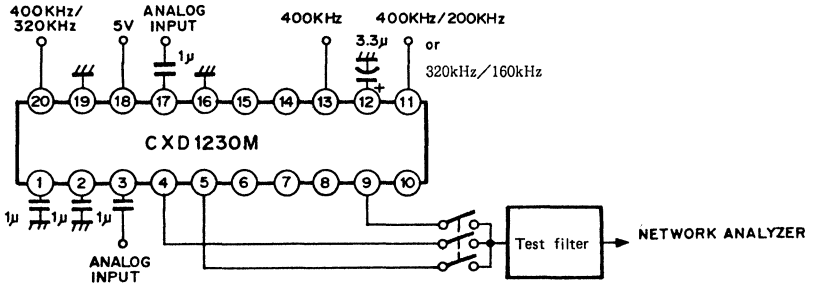


Fig.1

Electrical Characteristics Test Circuit 2 (Summing Amplifier Gain)

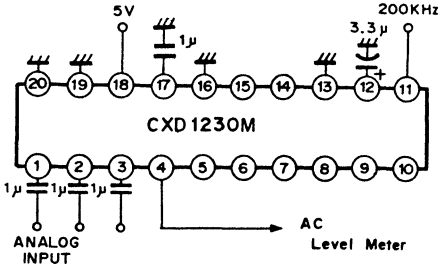


Fig.2

Electrical Characteristics Test Circuit 3 (Current Consumption)

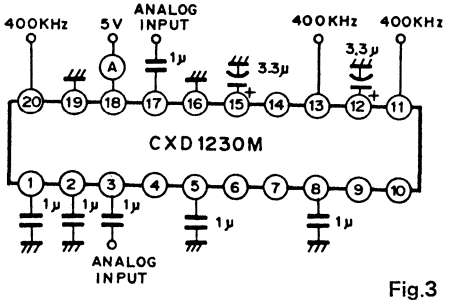


Fig.3

Operations

CXD1230M is a filter IC developed for cellular mobile telephone based on North American AMPS Standards (Advanced Mobile Phone Service) and British TACS Standards (Total Access Communication System).
By using this IC in conjunction with DATA•SAT LSI CXD1231Q-Z, a modem with the following funcions can be set up :

(1) Filtering of received WIDE BAND DATA
(2) Filtering of received SAT
(3) Detection of PLL lock of received SAT
(4) Summing of WIDE BAND DATA, ST, and SAT to be transmitted
(5) Filtering of WIDE BAND DATA, ST, and SAT to be transmitted

This section provides brief descriptions of these function.

1. Filtering of received WIDE BAND DATA

With the cellular mobile telephone system, data is transmitted between band and mobile stations, during speech or hand-off, in order to set channels. This data, called WIDE BAND DATA, is manchester coded. Transfer speed is 20kbaud for AMPS standards and 16kbaud for TACS standards. The received WIDE BAND DATA is fed through a buffer amplifier via a voltage follower to the quartic Butterworth low pass filter that operates as a data demodulating roll-off filter. In CXD1230M, as a switched capacitor filter is used, a cutoff frequency proportionate to the sampling clock frequency is obtained. Accordingly, with AMPS standards, when the sampling clock frequency is 400kHz, the low pass filter cutoff frequency is 13kHz (Typ.). Similarly, with TACS standards, when the sampling clock frequency is 320kHz, the low pass filter cutoff frequency is 10.4kHz (Typ.). The filter output is shaped to the CMOS logic level by means of a comparator and then sent out to CXD1231Q-Z.

2. Filtering of received SAT

In the cellular mobile telephone system, even during speech, a sine wave signal called SAT (Supervisory Audio Tone) is transmitted between the land station and mobile station to have them recognize each other. SATs of three frequencies, 5.97kHz, 6.00kHz, and 6.03kHz, are available for, both AMPS and TACS. The SAT frequency to be used is determined at the hand-off time by 2 bits data called SCC (SAT Color Code) which is transmitted from the land station to the mobile station. During speech, the mobile station recognizes the land station by receiving SAT from the land station, and the land station recognizes the mobile station by receiving SAT from the mobile station.

Similarly to the WIDE BAND DATA, SAT received from the land station is fed through the buffer amplifier to the 13kHz quartic Butterworth low pass filter. Then SAT is fed to the 6kHz quartic Butterworth high pass filter to prevent interference from the voice component (300Hz to 3kHz), and then to the 6kHz quadratic Tchebycheff low pass filter (pass range ripple 1dB) to reduce the high band noise (6kHz to 13kHz) in the event of a weak electric field strength. These 6kHz highpass and low pass filters are of switched capacitor type, providing a cutoff frequency of 6kHz (Typ.) when the sampling clock frequency is 400kHz. The above three filters constitute a band pass filter with a center frequency of approx. 7kHz so that SAT can be efficiently detected. The output of the 6kHz low pass filter is shaped to the CMOS logic level with a comparator, and is then sent out to CXD1231Q-Z.

3. Detection of PLL lock of received SAT

In CXD1231Q, DPLL locks when the SAT having the frequency specified with SCC is received. CXD1230M has a comparator to detect this lock/unlock state. The comparator output changes from "low" level to "high" level when the level of the SAT lock detect signal (SDET) from CXD1231Q-Z exceeds the reference voltage ($0.75V_{DD}$).

4. Summing of WIDE BAND DATA, ST, and SAT to be transmitted

In the cellular mobile telephone system, WIDE BAND DATA or ST, and SAT are transmitted from the mobile station to the land station. ST is a signal transmitted at the end of the call or ringing. The frequency is 10kHz for AMPS standards and 8kHz for TACS standards. From CXD1231Q-Z to CXD1230M, the WIDE BAND DATA, ST and the SAT are fed through a −18dB attenuation pad.

CXD1230M has an inverting amplifier which operates as a summing amplifier to sum these signals before transmission. In the transmission filter of the next stage summing amplifier during WIDE BAND DATA transmission, a quatric Butterworth low pass filter with a cutoff frequency of 18.5kHz for AMPS standards and 14.8kHz for TACS standards, is selected. During ST transmission a qaqtric Butterworth low pass filter with a cutoff frequency of 9.25kHz for AMPS standards and 7.4kHz for TACS standards, is selected.

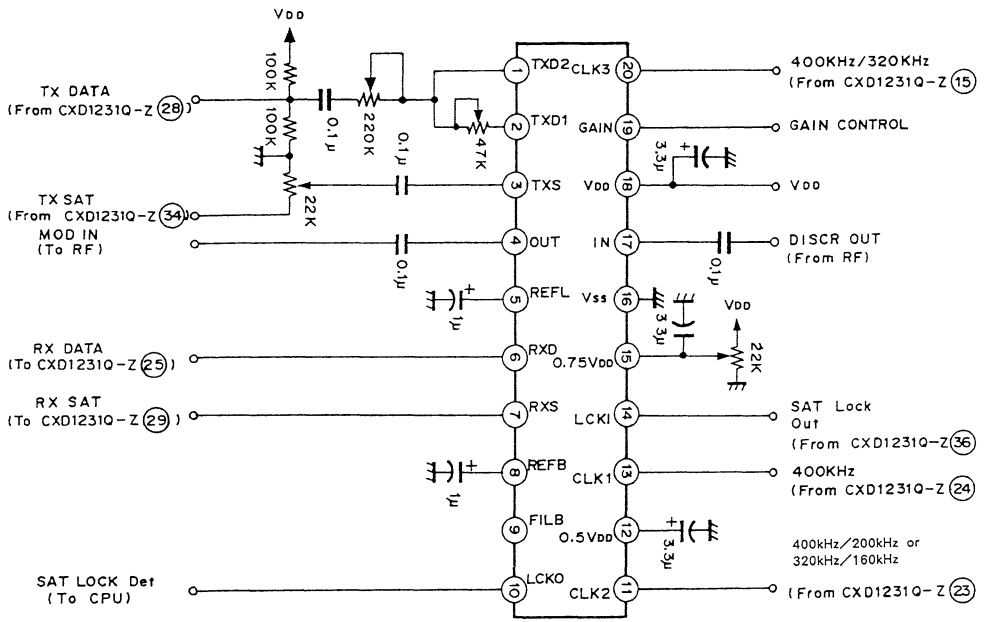
To compensate for the amplitude characteristics difference (−2.98dB to −4.62dB) between the 18.5kHz, 14.8kHz and 9.25kHz, 7.4kHz low pass filters at the ST frequency (10kHz), +3dB or −2.9dB can be selected as the summing amplifier gain. When ST is transmitted, +3dB gain can be obtained by setting the gain control input (GAIN) to "low" level, and −2.9dB gain by setting GAIN to "high" level. CXD1230M is provided with two input pins (TXD1 and TXD2) before the WIDE BAND DATA and ST so that the gain can be further adjusted by inserting appropriate resistors into the respective input lines. This allows the output level difference between ST transmission and data transmission to be completely compensated.

5. Filtering of WIDE BAND DATA, ST, and SAT to be transmitted

In the next stage of the summing amplifier, a low pass filter is provided to remove high-order harmonics from the summing amplifier output. The AMPS standards require a "20kHz ±10% quartic Butterworth low pass filter" as the transmission WIDE BAND DATA roll-off filter. In CXD1230M, the filter used in the next stage of the summing amplifier is an 18.5kHz quartic Butterworth low pass filter, and this filter also satisfies the condition of 38dB or more attenuation at 60kHz specified by AMPS. When ST and SAT are transmitted, the cutoff frequency of this transmitting filter must be lowered from 18.5kHz because the frequencies of ST and SAT are 10kHz and 6kHz, respectively. CXD1230M making the best of the switched capacitor filter merits, provides a cutoff frequency of 18.5kHz (Typ.) when the sampling frequency is 400kHz, and 9.25kHz (Typ.) when the sampling frequency is 200kHz.

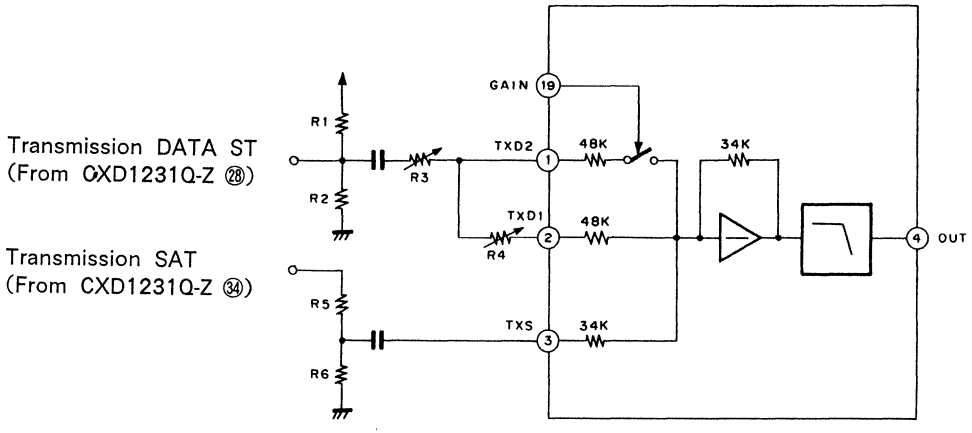
Similarly, for the TACS standards, a cutoff frequency of 14.8kHz (Typ.) when the sampling frequency is 320kHz, and 7.4kHz (Typ.) when the sampling frequency is 160kHz, are provided to cope with the transmission speed difference.

Application Circuit



Application Notes

1. Summing amplifier gain adjustment and Transmission DATA, ST, SAT input level adjustment.



Note) Resistances are typical values.

The following explanation applies to AMPS standards.

The summing amplifier configuration shown in the above figure is that of an inverting amplifier.

Accordingly, during TXS input (Transmission SAT) a gain of 0 dB (Typ.) is obtained. During TXD1 and TXD2 input (Transmission DATA, ST), when R4=0Ω, that is when pins 1 and 2 are short-circuited, a gain of +3.0dB (Typ.) is obtained when SW is ON and −2.9dB (Typ.) when SW is Off. Gain switching during Transmission DATA and ST is provided because of the difference in cutoff frequency between the filter used for data transmission (18.5kHz) and that used for ST transmission (9.25kHz). This would cause a transmission output level difference of −3.0 to −4.6dB between DATA and ST. The summing amplifier gain is set to −2.9dB and the transmission output level difference compensated by turning SW on and the summing amplifier gain to +3.0dB through setting the gain control input to "Low" during ST transmission. Also, for the same purpose the gain control input is set to "High" and SW turned Off during data transmission ST. Still as at this stage level compensation is not complete, through the insertion of R4 gain adjustment becomes possible. For all practical purposes proceed as follows.

① Set the CLK2 frequency to 400kHz and the gain control level to "High". Apply a 10kHz, 0.7Vp-p sine wave to pin 2 through R4 and measure the transmission filter output at pin 4. The measurement obtained corresponds to the output level during Data transmission.

② Set CLK frequency to 200kHz and the gain control level to "Low". Apply a 10kHz 0.7Vp-p sine wave to pins 1 and 2 through R4 and measure at pin 4 level the transmission filter output. The measurement obtained corresponds to the output level during ST transmission.

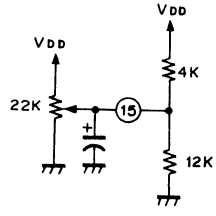
③ Adjust R4 to equalize the readings of the transmission output levels obtained at the above measurements.

For TACS standards as the transmission speed is 0.8 times (16k baud) that of AMPS standards, the respective frequencies above are all multiplied by 0.8 times to make a similar gain adjustment possible.

The MODEM (CXD1231Q-Z) transmission DATA, ST output and transmission SAT output are attenuated through R3, R5 and R6 and then input to CXD1230M.
The attenuation ratio of R3, R5 and R6 is set to −18dB.

The MODEM (CXD1231Q-Z) cannot be convected as it is by capacitor coupling to CXD1230M because the MODEM transmission DATA, ST output pin turns to high impedance by turning ENBL pin 30 to "Low" level, except during transmission. In this case, external resistors R1 and R2 (EX : 100kΩ) are used to bias the center voltage and then the capacitor coupling is executed.

2. 0.75 V_{DD} adjustment

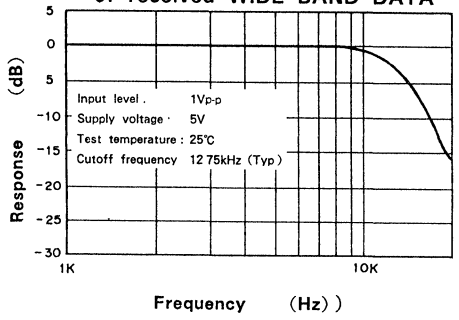


Note) Resistances are typical values.

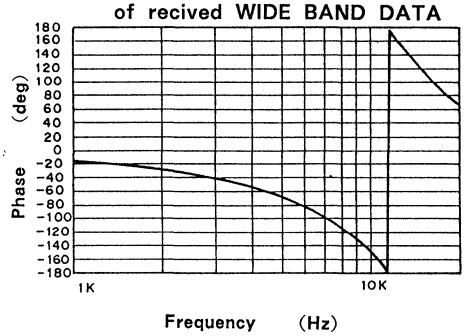
Supply voltage divided to 0.75V_{DD} inside CXD1230M is output at pin 15 (0.75V_{DD}). This value can be adjusted as shown in the above figure.

AMPS mode

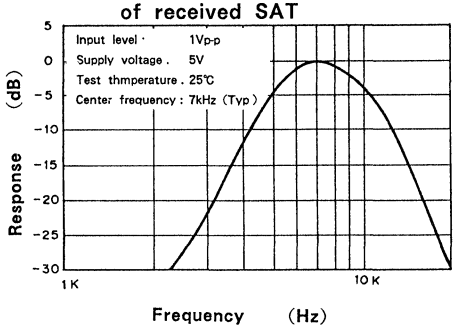
LPF amplitude characteristics of received WIDE BAND DATA



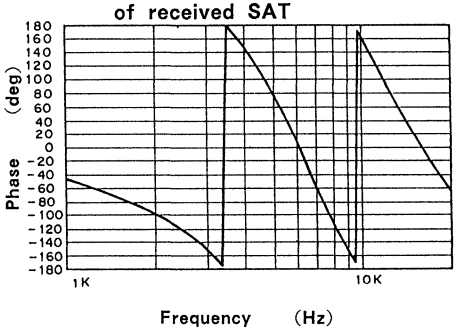
LPF amplitude characteristics of recived WIDE BAND DATA



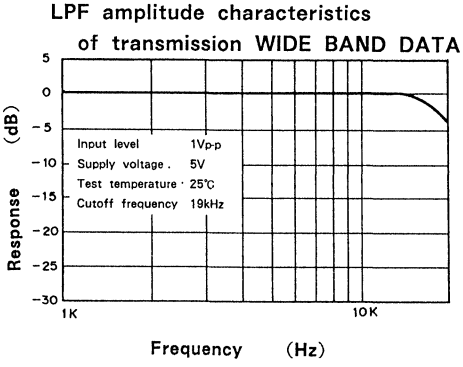
BPF amplitude characteristics of received SAT



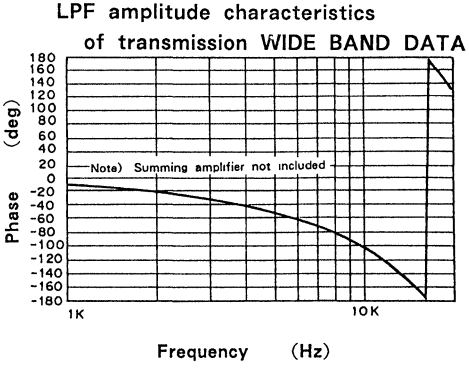
BPF amplitude characteristics of received SAT



LPF amplitude characteristics of transmission WIDE BAND DATA

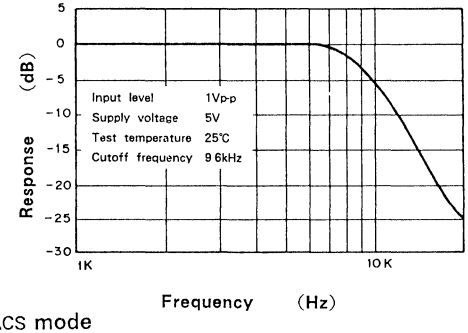


LPF amplitude characteristics of transmission WIDE BAND DATA

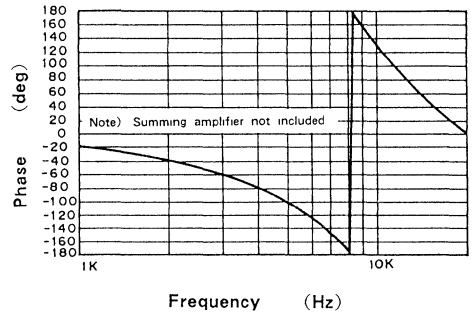


TACS mode

LPF amplitude characteristics of transmission SAT, ST

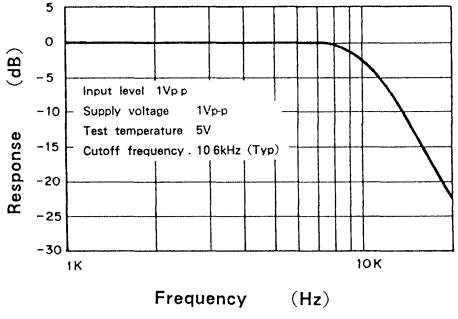


LPF phase characteristics for ST, SAT transmission

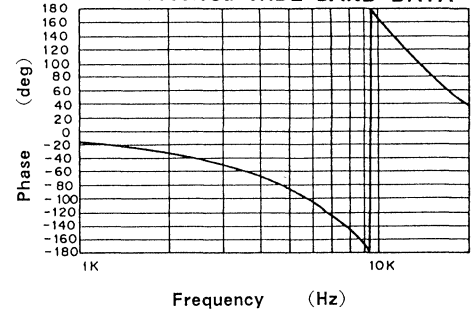


TACS mode

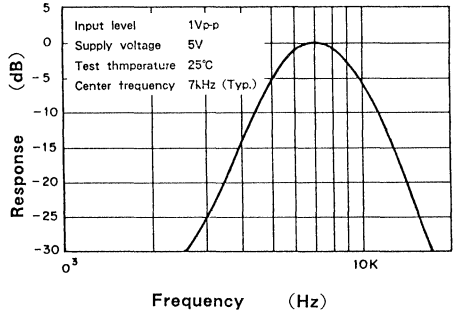
LPF phase characteristics of received WIDE BAND DATA



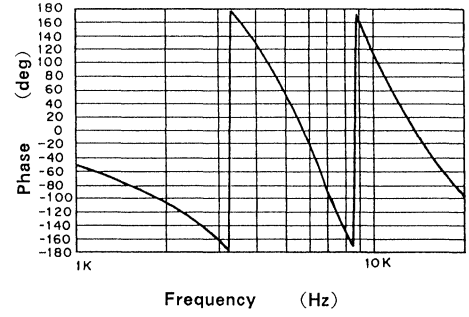
LPF phase characteristics of received WIDE BAND DATA



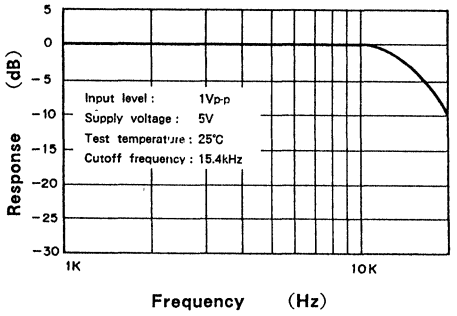
BPF phase characteristics of received SAT



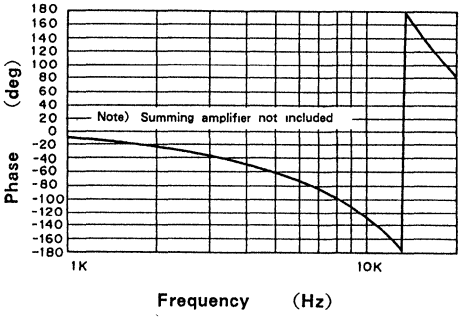
BPF phase characteristics of received SAT



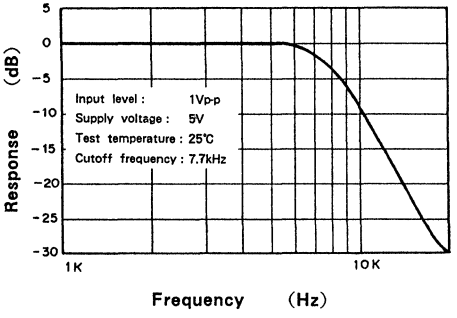
LPF phase characteristics
of transmission WIDE BAND DATA



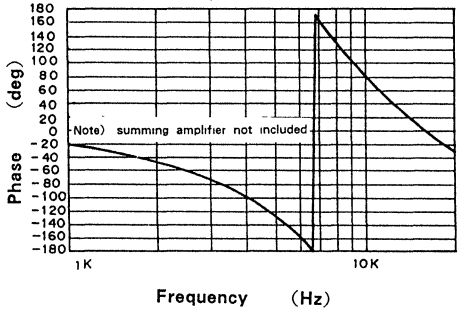
LPF phase characteristics
of transmission WIDE BAND DATA



LPF amplitude characteristics
of transmission SAT, ST



LPF phase characteristics
for ST, SAT transmission



SONY

CXD1237Q/R

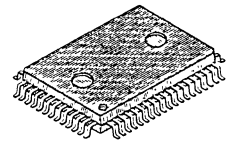
Cellular Radio Telephone Filter LSI

Description

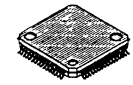
The CXD1237Q/R is a filter LSI developed for cellular radio telephone. Ultra low current consumption LSI built in voice signal processing and electrical volume, in addition to DATA, SAT processing.

Usage in conjunction with control signal processing LSI CXD1270Q/R provides a modem.

CXD1237Q
64 pin QFP (Plastic)



CXD1237R
64 pin VQFP (Plastic)



Structure

Silicon gate CMOS IC

Features

- Ultra low current consumption
  I_{DD}=1.8mA (in operation)
  I_{DD}=0.6mA (at power save)(at 5V, Typ.)
- Power save is possible by standby control
- AMPS, TACS, DOC standards
- Adoption of SCF technology obtains stable characteristics.
- Built in electrical volume (3dB step 8 stages)

Functions

- Filtering of received WBD
- Filtering of received SAT
- PLL lock detection of received SAT
- Summing of WBD, ST, SAT to be transmitted
- Filtering of received VOICE
- Filtering of transmitted VOICE
- Volume control (2-channel)

Absolute Maximum Ratings

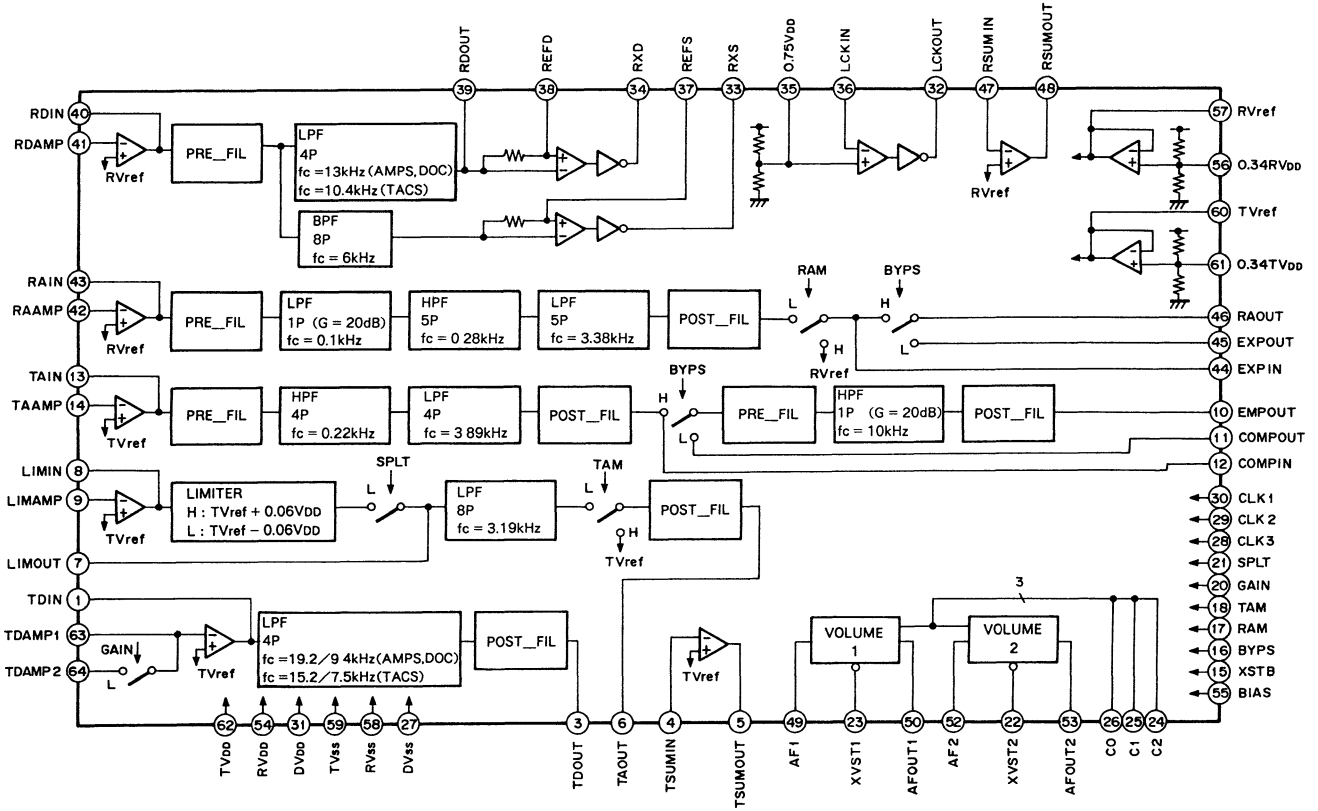
• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	–34 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–34 to +85	°C

E90450 – ST

Block Diagram



Note) Pin No. for QFP package.

Pin Description

Pin No.		Symbol	I/O	Description
QFP	VQFP			
1	63	TDIN	O	Summing amplifier output for TX WBD, ST, SAT inputs
2	64	NC	—	—
3	1	TDOUT	O	Filter outputs of TX WBD, ST, SAT
4	2	TSUMIN	I	TX summing amplifier input. Use this pin to add data (TDOUT output) and voice (TAOUT output).
5	3	TSUMOUT	O	TX summing amplifier output
6	4	TAOUT	O	TX voice filter output
7	5	LIMOUT	I/O	TX voice limiter output. Use this pin as input when testing rear portion TX splutter filter characteristics independently.
8	6	LIMIN	O	Limiter input gain control amplifier output for TX voice
9	7	LIMAMP	I	Limiter input gain control amplifier input for TX voice
10	8	EMPOUT	O	Emphasis output. Normally, input to limiter.
11	9	COMPOUT	I	Input external output compandor.
12	10	COMPIN	O	Output pin to input to external compandor. Bypass control of compandor is executed at BYPS pin.
13	11	TAIN	O	TX voice gain control amplifier output.
14	12	TAAMP	I	TX voice gain control amplifier input.
15	13	XSTB	I	Standby control pin other than volume block. Only RX WBD filter block is active during standby. Standby at "L".
16	14	BYPS	I	Compandor, expander bypass control. Compandor, expander is bypassed at "H".
17	15	RAM	I	RX voice mute control. Mute at "H".
18	16	TAM	I	TX voice mute control. Mute at "H".
19	17	NC	—	—
20	18	GAIN	I	TX data summing input gain control. (Switching input for TDAMP2 pin) Open at "H".

Pin No.		Symbol	I/O	Description
QFP	VQFP			
21	19	SPLT	I	Switching input for TX splutter filter. At "H", input from LIMOUT, splutter filter own characteristics can be observed. Normally, at "L". With pull down resistor.
22	20	XVST2	I	Electrical volume 2 standby control. Standby at "L". With pull down resistor.
23	21	XVST1	I	Electrical volume 1 standby control. Standby at "L". With pull down resistor.
24	22	C2	I	Electrical volume 1, 2 control pin (MSB). Control at 3 bits; C2, C1 and C0. With pull down resistor.
25	23	C1	I	Electrical volume 1, 2 control pin. With pull down resistor.
26	24	C0	I	Electrical volume 1, 2 control pin (LSB). With pull down resistor.
27	25	DVss	——	Digital GND
28	26	CLK3	I	CLK input for TX DATA. At AMPS, DOC: 400/200kHz. At TACS: 320/160kHz
29	27	CLK2	I	CLK input for voice filter 400kHz.
30	28	CLK1	I	CLK input for RX DATA. At AMPS, DOC: 400kHz. At TACS: 320kHz
31	29	DV_{DD}	——	Digital power supply
32	30	LCKOUT	O	Comparator output for RX SAT PLL lock detection
33	31	RXS	O	Comparator output for RX SAT
34	32	RXD	O	Comparator output for RX WBD
35	33	$0.75V_{DD}$	I	Comparator reference voltage input for RX SAT PLL lock detection. Bias 0.75 times of power supply voltage. Normally, an external capacitance of 1 μF is required between this pin and RVss.
36	34	LCKIN	I	Comparator input for RX SAT PLL lock detection.
37	35	REFS	I	Comparator reference voltage input for RX SAT. Eliminates front portion band pass filter output offset by means of 0.1 μF capacitance between this pin and RVss.
38	36	REFD	I	Comparator reference voltage input for RX WBD. Eliminates front portion low pass filter output offset by means of 0.1 μF capacitance between this pin and RVss.
39	37	RDOUT	O	RX WBD filter output. Usable as RX voice introduction filter.
40	38	RDIN	O	Gain control amplifier output for RX WBD and SAT input.

Pin No.		Symbol	I/O	Description
QFP	VQFP			
41	39	RDAMP	I	Gain control amplifier input for RX WBD and SAT
42	40	RAAMP	I	Gain control amplifier input for RX voice input
43	41	RAIN	O	Gain control amplifier output for RX voice input
44	42	EXPIN	O	External expander input
45	43	EXPOUT	I	External expander output. Bypass control at BYPS, the same as TX compandor.
46	44	RAOUT	O	RX voice filter output
47	45	RSUMIN	I	RX summing amplifier input. Used to sum up DTMF HT and LT.
48	46	RSUMOUT	O	RX summing amplifier output
49	47	AF1	I	Electrical volume input 1.
50	48	AFOUT1	O	Electrical volume output 1. Volume is controlled at C2, C1 and C0.
51	49	NC	—	—
52	50	AF2	I	Electrical volume input 2.
53	51	AFOUT2	O	Electrical volume output 2. Volume is controlled at C2, C1 and C0.
54	52	RV_{DD}	—	RX power supply
55	53	BIAS	I	Bias current setting pin of internal OP amplifier. Normally, connect 500kΩ between this pin and RV_{DD}. (See Notes on Operation)
56	54	$0.34RV_{DD}$	I	OP amplifier reference voltage input for RX block. Bias 0.34 times of power supply voltage. Normally, an external capacitance of 1 µF is required between this pin and RVss.
57	55	RVref	O	OP amplifier reference voltage output for RX block. Bias 0.34 times of power supply voltage. Normally, an external capacitance of 1 µF is required between this pin and RVss.
58	56	RVss	—	RX ground pin
59	57	TVss	—	TX ground pin
60	58	TVref	O	OP amplifier reference voltage output for TX block. Bias 0.34 times of power supply voltage. Normally, an external capacitance of 1 µF is required between this pin and TVss.
61	59	$0.34TV_{DD}$	I	OP amplifier reference voltage output for TX block. Bias 0.34 times of power supply voltage. Normally, an external capacitance of 1 µF is required between this pin and TVss.
62	60	TV_{DD}	—	TX power supply
63	61	TDAMP1	I	TX SAT input
64	62	TDAMP2	I	TX WBD, ST input. Gain control at GAIN pin (Switching)

Electrical Characteristics

(V_{DD}=5V ±10%, Ta=–34 to +85°C)

Item	Symbol	Pin name	Condition	Standards			Unit
				Min.	Typ.	Max.	
Power supply current 1	I_{DD}	RV_{DD}, TV_{DD}, DV_{DD} Total	XSTB="H" XVST1="H" XVST2="H" BIAS resistor=500kΩ	—	1.8	2.8	mA
Power supply current 2	I_{STB1}	The same as above	XSTB="L" XVST1="L" XVST2="L" BIAS resistor=500kΩ	—	0.6	1	mA
Power supply current 3	I_{STB2}	The same as above	XSTB="L" XVST1="H" XVST2="H" BIAS resistor=500kΩ	—	0.8	1.2	mA
Digital input voltage at "L"	V_{IL}	SPLT, GAIN, TAM, RAM, BYPS, XSTB, XVST1, XVST2, C0, C1, C2, CLK1, CLK2, CLK3	—	—	—	0.3V_{DD}	V
Digital input voltage at "H"	V_{IH}	The same as above	—	0.7V_{DD}	—	—	V
Digital input current at "L"	I_{IL}	The same as above	V_{IN}=GND	–10	—	10	µA
Digital input current at "H"	I_{IH1}	GAIN, TAM, RAM, BYPS, XSTB, CLK1, CLK2, CLK3	V_{IN}=V_{DD}	–10	—	10	µA
Digital input current at "H" (With pull down resistor)	I_{IH2}	SPLT, XVST1, XVST2, C0, C1, C2	The same as above	—	—	100	µA
Digital output voltage at "L"	V_{OL}	RXD, RXS, LCKOUT	I_{OL}=0.4mA	0.8	—	—	V
Digital output voltage at "H"	V_{OH}	The same as above	I_{OH}=–0.4mA	—	—	4	V
Analog input voltage range	V_{IA}	RDAMP, RAAMP, TAAMP, LIMAMP, TDAMP1, TDAMP2, RSUMIN, TSUMIN, AF1, AF2	—	—	—	1	Vp-p
Analog input resistor 1	R_{I1}	AF1, AF2	Input pin –0.34V_{DD}	70	130	190	kΩ
Analog input resistor 2	R_{I2}	COMPOUT	The same as above	500	640	800	kΩ
Analog input resistor 3	R_{I3}	TDAMP2, EXPOUT	The same as above	—	0.6	1	kΩ

Item	Symbol	Pin name	Condition	Standards			Unit
				Min.	Typ.	Max.	
Analog output load resistor 1	R_{L1}	EXPIN, RAOUT, EMPOUT, COMPIN, TAOUT, TDOUT, RSUMOUT, AFOUT1, TSUMOUT, AFOUT2	Output pin –0.34V_{DD} BIAS resistor=500kΩ	10	—	—	kΩ
Analog output load resistor 2	R_{L2}	RDIN, RAIN, TAIN, LIMIN, TDIN	The same as above	100	—	—	kΩ
Analog output voltage range	V_{OA}	EXPIN, RAOUT, EMPOUT, COMPIN, RSUMOUT, TSUMOUT, TAOUT, TDOUT, RDOUT, AFOUT1, AFOUT2	BIAS resistor=500kΩ Load resistor=10kΩ	—	—	0.4	Vp-p
Limiter voltage at "L"	V_{LL}	LIMAMP – LIMOUT	SPLT="L"	0.34V_{DD} –0.066V_{DD}	0.34V_{DD} –0.06V_{DD}	0.34V_{DD} –0.054V_{DD}	V
Limiter voltage at "H"	V_{LH}	The same as above	The same as above	0.34V_{DD} +0.054V_{DD}	0.34V_{DD} +0.06V_{DD}	0.34V_{DD} +0.066V_{DD}	V
Electrical volume step voltage	V_{STEP}	AF1 – AFOUT1 AF2 – AFOUT2	—	2.5	3	3.5	dB
RX DATA filter gain 1 (AMPS)	G_{RD1}	RDAMP – RDOUT	Input: –18dBV 13kHz CLK1=400kHz	–5	–3	–1	dB
RX DATA filter gain 2 (TACS)	G_{RD2}	The same as above	Input: –18dBV 10.4kHz CLK1=320kHz	–4	–3	–2	dB
RX SAT filter gain	G_{SAT}	RDAMP – REFS	Input: –18dBV 6kHz CLK2=400kHz	–1	0	1	dB
TX DATA filter gain 1 (AMPS)	G_{TD1}	TDAMP1 – TDOUT	Input: –18dBV 19.2kHz CLK3=400kHz	–5	–3	–1	dB
TX DATA filter gain 2 (AMPS)	G_{TD2}	The same as above	Input: –18dBV 9.4kHz CLK3=200kHz	–4	–3	–2	dB
TX DATA filter gain 3 (TACS)	G_{TD3}	The same as above	Input: –18dBV 15.2kHz CLK3=320kHz	–5	–3	–1	dB
TX DATA filter gain 4 (TACS)	G_{TD4}	The same as above	Input: –18dBV 7.5kHz CLK3=160kHz	–4	–3	–2	dB

Item	Symbol	Pin name	Condition	Standards			Unit
				Min.	Typ.	Max.	
RX voice filter gain	G_{RA}	RAAMP – RAOUT	Input: –18dBV 1kHz RAM="L" BYPS="H"	–1	–0.3	1	dB
RX voice mute	G_{RAM}	The same as above	Input: –18dBV 1kHz RAM="H" BYPS="H"	50	—	—	dB
RX voice S/N	SN_R	The same as above	Input: –18dBV 1kHz RAM="L" BYPS="H" Band: 50Hz to 30kHz	50	—	—	dB
RX voice distortion factor	THD_R	The same as above	The same as above	—	—	–50	dB
TX voice gain	G_{TA}	TAAMP – TAOUT	Input: –18dBV 1kHz TAM="L" BYPS="H" SPLT="L" EMPOUT → LIMAMP	–1	–0.3	1	dB
TX voice mute	G_{TAM}	The same as above	Input: –18dBV 1kHz TAM="H" BYPS="H" SPLT="L" EMPOUT → LIMAMP	50	—	—	dB
TX voice S/N	SN_T	The same as above	Input: –18dBV 1kHz TAM="L" BYPS="H" SPLT="L" EMPOUT → LIMAMP Band: 50Hz to 30kHz	45	—	—	dB
TX voice distortion factor	THD_T	The same as above	The same as above	—	—	–45	dB

Description of Operation

CXD1237Q/R is a filter IC developed for cellular mobile telephone based on North American AMPS Standards (Advanced Mobile Phone Service), British TACS Standards (Total Access Communication System) and Canadian DOC Standards (Document of Canada).

By using this LSI in conjunction with control signal processing LSI CXD1270Q/R, a modem with the following functions can be set up:

(1) Filtering of received WIDE BAND DATA
(2) Filtering of received SAT
(3) PLL lock detection of received SAT
(4) Summing of WIDE BAND DATA, ST and SAT to be transmitted
(5) Filtering of WIDE BAND DATA, ST and SAT to be transmitted
(6) Filtering of received voice
(7) Filtering of transmitted voice
(8) Volume control

This section provides brief descriptions of these functions.

1. Filtering of received WIDE BAND DATA

With the cellular mobile telephone system, data is transmitted between land and mobile stations, during speech or hand-off, in order to set channels. This data, called WIDE BAND DATA, is manchester code. Transfer speed is 20kbaud for AMPS and DOC standards and 16kbaud for TACS standards. The received WIDE BAND DATA is fed through gain control amplifier and prefilter to the 4 pole Butterworth low pass filter that operates as a data demodulating roll-off filter. In CXD1237Q/R , as a switched capacitor filter is used, a cutoff frequency proportionate to the sampling clock frequency is obtained. Accordingly, with AMPS and DOC standards, when the sampling clock frequency is 400kHz, the low pass filter cutoff frequency is 13kHz (Typ.). Similarly, with TACS standards, when the sampling clock frequency is 320kHz, the low pass filter cutoff frequency is 10.4kHz (Typ.). The filter output is shaped to the CMOS logic level by means of a comparator and then sent out to CXD1270Q/R.

2. Filtering of received SAT

In the cellular mobile telephone system, even during speech, a sine wave signal called SAT (Supervisory Audio Tone) is transmitted between land and mobile stations to have them recognize each other. SATs of three frequencies, 5.97kHz, 6.00kHz and 6.03kHz, are available for, both AMPS, TACS and DOC. The SAT frequency to be used is determined at the hand-off time by 2 bits data called SCC (SAT Collar Code) which is transmitted from the land station to the mobile station. During speech, the mobile station recognizes the land station by receiving SAT from the land station, and the land station recognizes the mobile station by receiving SAT from the mobile station.

Similarly to the WIDE BAND DATA, SAT received from the land station is fed through the gain control amplifier and prefilter. Then SAT is fed to the 6kHz 8 pole Butterworth band pass filter to prevent interference from the voice component (300Hz to 3kHz), and then to the 6kHz 8 pole Butterworth band pass filter to reduce the high band noise (6kHz to 13kHz) in the event of a weak electric field strength. SAT can be efficiently detected by adopting switched capacitor filter. The output of the 6kHz band pass filter is shaped to the CMOS logic level with a comparator, and is then sent out to CXD1270Q/R.

3. PLL lock detection of received SAT

In CXD1270Q/R, DPLL locks when the SAT having the frequency specified with SCC is received. CXD1237Q/R has a comparator to detect this lock/unlock state. The comparator output changes from "low" level to "high" level when the level of the SAT lock detect signal (SDET) from CXD1270Q/R exceeds the reference voltage ($0.75V_{DD}$).

4. Summing of WIDE BAND DATA, ST and SAT to be transmitted

In the cellular mobile telephone system, WIDE BAND DATA or ST and SAT are transmitted from the mobile station to the land station. ST is a signal transmitted at the end of the call or ringing. The frequency is 10kHz for AMPS and DOC standards and 8kHz for TACS standards. From CXD1270Q/R to CXD1237Q/R, the WIDE BAND DATA, ST and the SAT are fed through an attenuation pad.

CXD1237Q/R has an inverting amplifier which operates as a summing amplifier to sum these signals before transmission. In the transmission filter of the next stage summing amplifier during WIDE BAND DATA transmission, a 4 pole Butterworth low pass filter with a cutoff frequency of 19.2kHz for AMPS and DOC standards and 15.2kHz for TACS standards, is selected. During ST transmission a 4 pole Butterworth low pass filter with a cutoff frequency of 9.4kHz for AMPS and DOC standards and 7.5kHz for TACS standards, is selected.

To compensate for the amplitude characteristics difference between the 19.2kHz, 15.2kHz and 9.4kHz, 7.5kHz low pass filters at the ST frequency (10kHz), the summing amplifier gain can be selected in two ways. When ST is transmitted, + several dB gain can be obtained by setting the gain control input (GAIN) to "low" level, and – several dB gain by setting GAIN to "high" level. Adjust external resistor to obtain suitable gain.

5. Filtering of WIDE BAND DATA, ST and SAT to be transmitted

In the next stage of the summing amplifier, a low pass filter is provided to remove high-order harmonics from the summing amplifier output. The AMPS and DOC standards require a "20kHz ±10% 4 pole Butterworth low pass filter" as the transmission WIDE BAND DATA roll-off filter. In CXD1237Q/R, the filter used in the next stage of the summing amplifier is an 19.2kHz 4 pole Butterworth low pass filter, and this filter also satisfies the condition of 38dB or more attenuation at 60kHz specified by AMPS. When ST and SAT are transmitted, the cutoff frequency of this transmitting filter must be lowered from 19.2kHz because the frequencies of ST and SAT are 10kHz and 6kHz, respectively. CXD1237Q/R making the best of the switched capacitor filter merits, provides a cutoff frequency of 19.2kHz (Typ.) when the sampling frequency is 400kHz, and 9.4kHz (Typ.) when the sampling frequency is 200kHz.

Similarly, for the TACS standards, a cutoff frequency of 15.2kHz (Typ.) when the sampling frequency is 320kHz, and 7.5kHz (Typ.) when the sampling frequency is 160kHz, are provided to cope with the transmission speed difference.

6. Filtering of received voice

To satisfy various standards 3 types of Butterworth filters are included.

At the input stage a gain control amplifier is available with a prefilter to eliminate folded distortion. At the output stage a post filter is equipped to eliminate carriers.

RDOUT output is input to the gain control amplifier. After passing through the prefilter, deemphasis is performed at 1 pole Butterworth low pass filter. Then band limitation is executed at 5 pole Butterworth high pass filter and 5 pole Butterworth low pass filter to pass through the post filter for output.

At RAM muting control and at BYPS expander bypass control are executed.

7. Filtering of transmitted voice

In the transmission system, after passing through the gain control amplifier and the prefilter, band limitation occurs at the 4 pole Butterworth high pass filter and the 4 pole Butterworth low pass filter. After going through the post filter prefilter, emphasis is executed at 1 pole Butterworth high pass filter, to pass through the post filter for output.

After what this output is passed through the gain control amplifier and input to the limiter to be clipped at 1.7V ± 0.3V (Typ. when V_{DD}=5V). It is then passed through a steep 8 pole Butterworth low pass filter as splutter filter to be output after going through the post filter.

Muting control is executed at TAM and the compander bypass control, at BYPS.

Normally SPLT is at "L". However, by turning is to "H" the splutter filter own characteristics can be observed without passing through the limiter.

8. Volume control

As the volume control for voice, ringing and others, 2 systems of electrical volumes are featured (3dB step, 8 stages). Control for both volumes is commonly executed through 3 bits C0, C1 and C2.

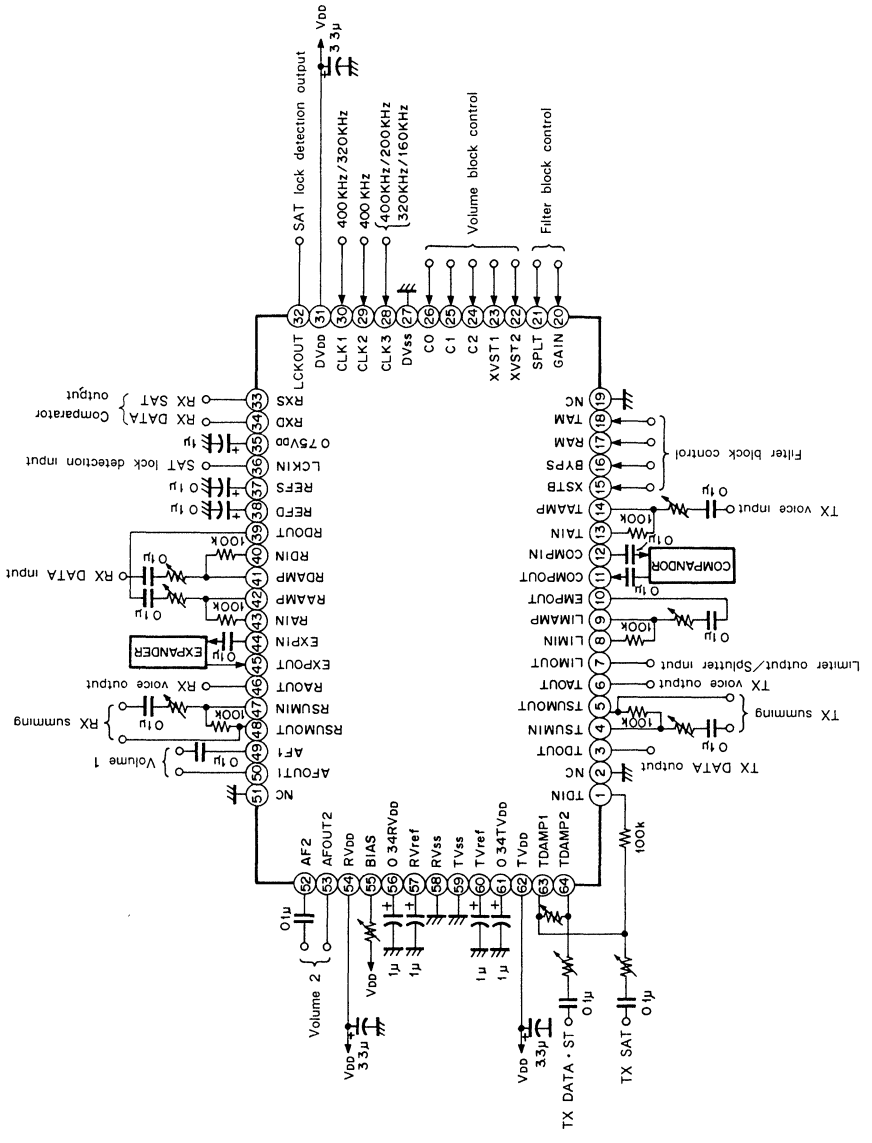
C2	C1	C0	Gain (dB)
L	L	L	0
L	L	H	–3
L	H	L	–6
L	H	H	–9
H	L	L	–12
H	L	H	–15
H	H	L	–18
H	H	H	–21

9. Others

One summing amplifier is available for each of the receiving and transmission systems respectively.

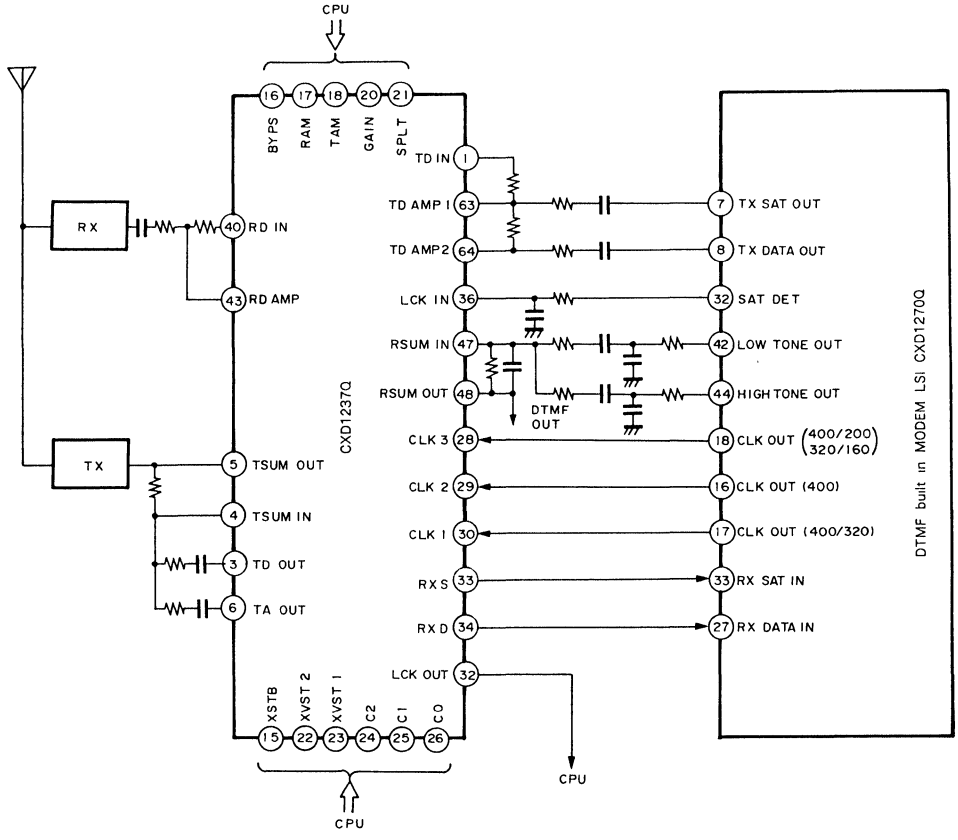
The summing amplifier for the receiving system can be used to sum up LT and HT of DTMF while that of the transmission system can be used to add data and voice.

Application Circuit



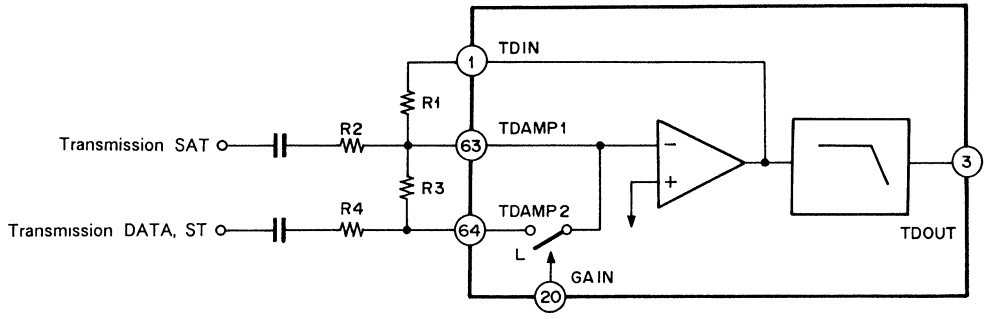
Note) Pin No. for QFP package.

Connecting Example of CXD1237Q/R and CXD1270Q/R (CXD1237: Pin No. of QFP)



Notes on Operation

1. Gain adjustment of the summing amplifier for transmission data



Note) Pin No. for QFP package

Attenuation adjustment of transmission SAT is executed at R2 and R1 in the above circuit and that for transmission DATA, ST at R4, R3 and R1. Attenuation at –20dB is recommended.

Moreover, to correct the transmission output level difference between DATA and ST, adjustment is effected at R3.

During ST transmission GAIN is set to "L" and gain raised. During DATA transmission GAIN is set to "H" and gain lowered for use.

2. Selection of AMPS, TACS and DOC

Selection of the various standards is effected by varying the input frequency to CLK1 and CLK3 as indicated below.

Standard	CLK1	CLK3
AMPS, DOC	400kHz	400kHz (DATA) 200kHz (ST, SAT)
TACS	320kHz	320kHz (DATA) 160kHz (ST, SAT)

CLK2 is fixed to 400kHz.

3. Standby control

CXD1237Q/R features 3 independent standby control pins XSTB, XVST1 and XVST2 that control the 3 blocks as indicated below.

Pin	Control block	H	L
XSTB	All blocks except Volume 1 and 2	Active	Only the block up to RDAMP-RXD and RVref generating circuit active
XVST1	Volume 1	Active	Standby
XVST2	Volume 2	Active	Standby

4. Output voltage range and supply current adjustment

In CXD1237Q/R, output level range and supply current vary according to the bias resistor connected between BIAS and RV_{DD}.

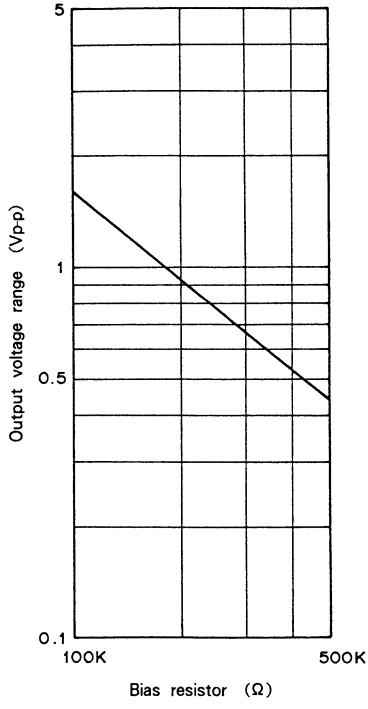
Details indicated in the Electrical Characteristics are values when the bias resistor=500kΩ and the output load is at 10kΩ .

The bias current of the internal operational amplifier is determined through the bias resistor. Reducing this bias resistor will enlarge the output level range and supply current while inversely, enlarging it will reduce the output range and supply current.

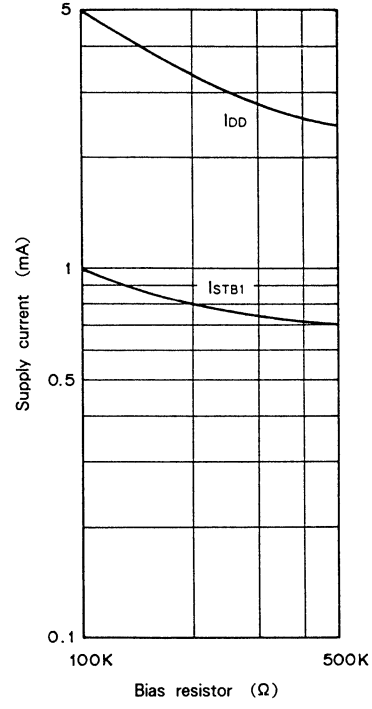
That is through the adjustment of the bias resistor the desired output voltage range and supply current can be obtained.

For reference, the relation between the bias resistor and output level range, supply current is shown below.

Bias resistor vs. Output voltage range



Bias resistor vs. Supply current

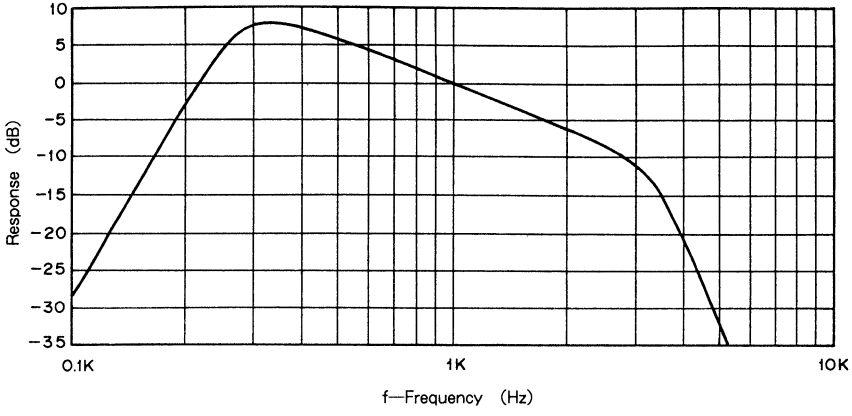


5. Others

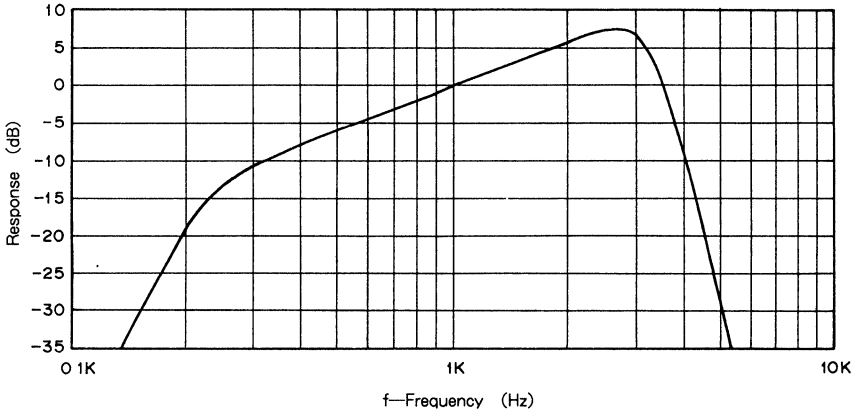
1) Note that there is a 2-pin difference between QFP and VQFP packages.
2) Pins with pull down resistances (6 pins)
   SPLT, XVST1, XVST2, C0, C1, C2

Filter Characteristics

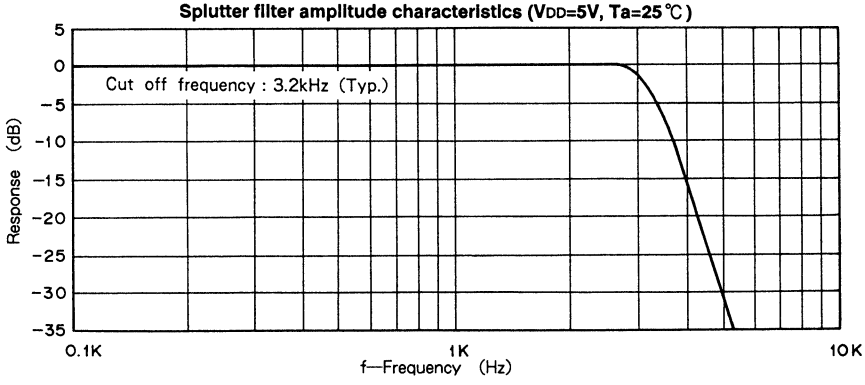
RX voice filter amplitude characteristics (V_{DD}=5V, Ta=25℃)



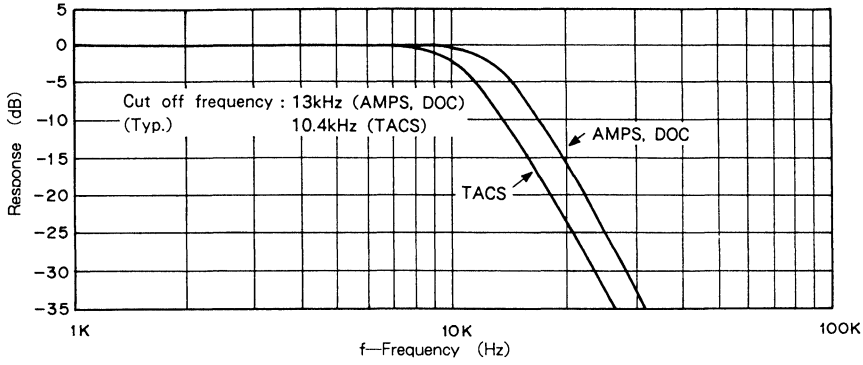
TX voice filter (Splutter is included) amplitude characteristics (V_{DD}=5V, Ta=25℃)



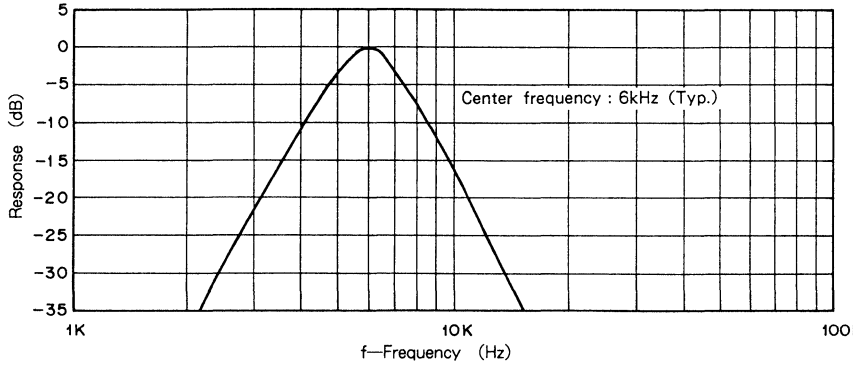
Splutter filter amplitude characteristics (V_{DD}=5V, Ta=25℃)



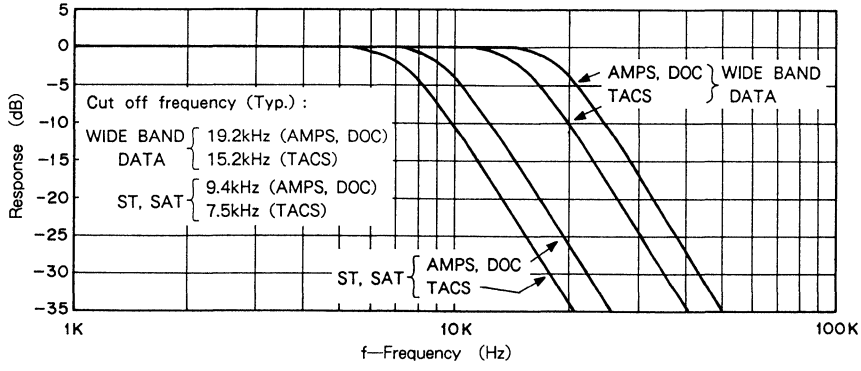
LPF amplitude characteristics for RX WIDE BAND DATA (V_{DD}=5V, Ta=25℃)



BPF amplitude characteristics for RX SAT (V_{DD}=5V, Ta=25℃)



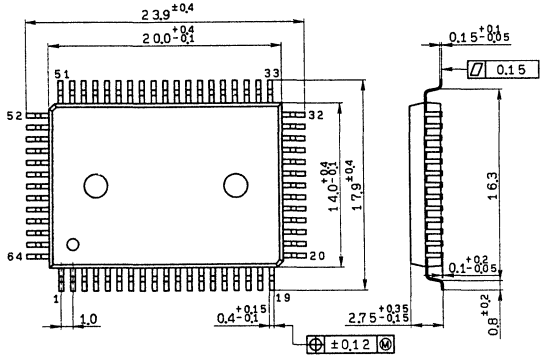
LPF amplitude characteristics for TX WIDE BAND DATA, ST, SAT (V_{DD}=5V, Ta=25℃)



Package Outline Unit: mm

CXD1237Q

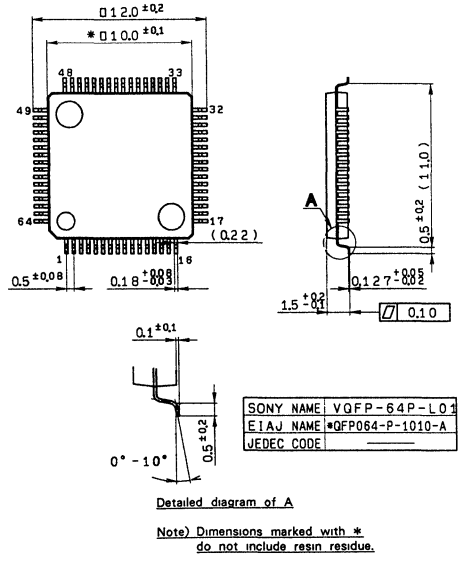
64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———

CXD1237R

64pin VQFP (Plastic) 0.3g



SONY NAME	VQFP-64P-L01
EIAJ NAME	*QFP064-P-1010-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY

CXD1231Q-Z

Cellular Radio Telephone DATA SAT LSI

Description

CXD1231Q-Z is a DATA SAT modulation/demodulation IC developed for cellular radio telephone.

Usage in conjunction with filter IC CXD1230M provides a modem.

Features

- Conforms with North American AMPS standards and British TACS standards.
- Uses the manchester code decoder with low error rate.
- SAT detection circuit produces few errors even with weak electric field.
- Low power consumption.

Functions

- Decoding of received data.
- Detection of received SAT.
- SAT output with same frequency and phase as received SAT.
- Transmitted DATA, ST encode.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

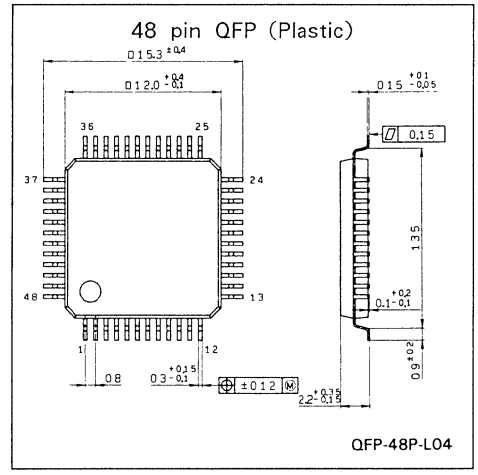
• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	−34 to +75	°C

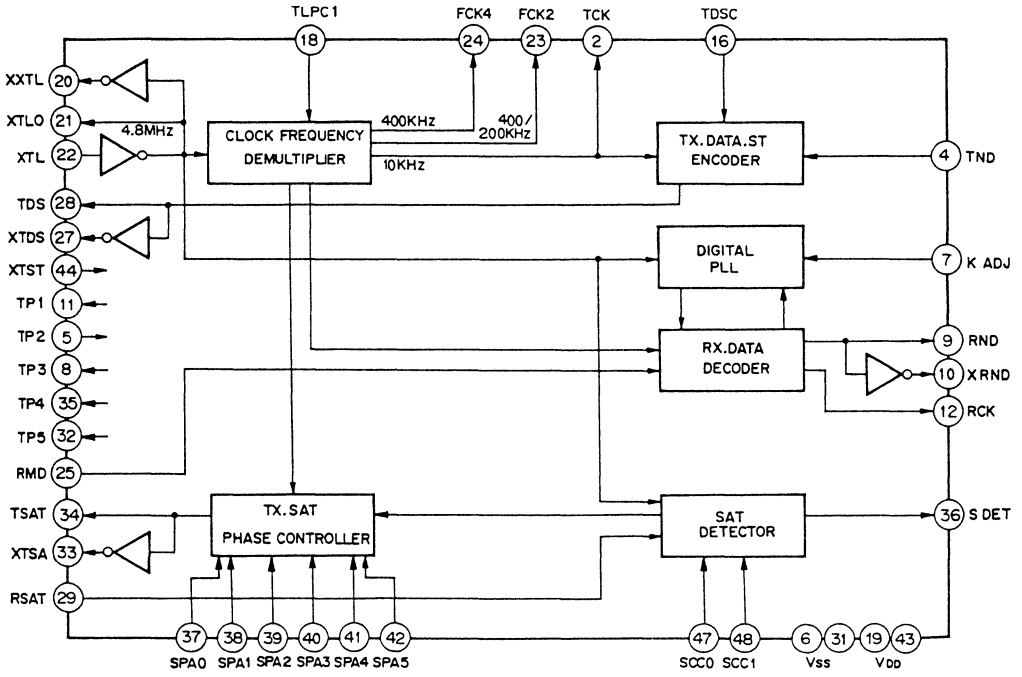
Package Outline

Unit : mm

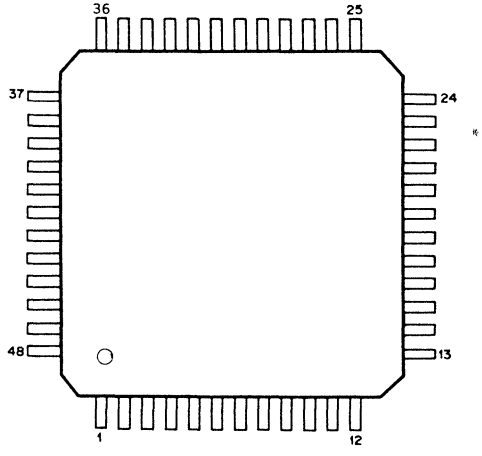


71228A-ST

Block Diagram



Pin Configuration (Top View)

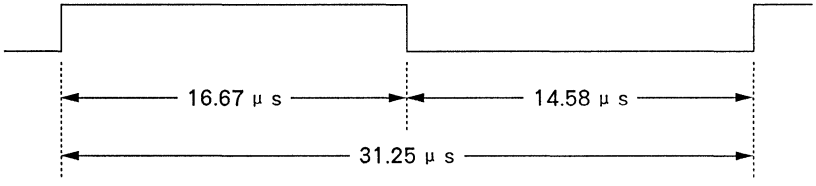


Pin Description

No.	Symbol	I/O	Description
1	NC	——	
2	TCK	O	Clock output of transmitted DATA, ST, 10kHz at AMPS mode and 8kHz at TACS mode.
3	AMPS	I	AMPS/TACS mode select input, AMPS mode at Open and TACS mode at L.
4	TND	I	Transmitted NRZ • DATA input.
5	TP2	I	Test input. Normally fixed at low level.
6	V_{SS}	——	GND
7	KADJ	I	PLL lock range select input for received manchester Data decoder, ±78Hz at high level and ±19.5Hz at low level.
8	TP3	O	Test output.
9	RND	O	Received NRZ DATA output.
10	XRND	O	RND (pin 9) inverting output.
11	TP1	O	Test output.
12	RCK	O	Clock output (10kHz) extracted from received DATA, 10kHz at AMPS mode and 8kHz at TACS mode.
13		——	
14		——	
15	FCK3 *1	O	Clock output of switched capacitor filter, 400kHz at AMPS mode and 320kHz at TACS mode.
16	TDSC	I	ON/OFF control input of received manchester DATA, ST.
17	TLPC2 *2	I	Frequency select input 2 of FCK2 (pin 23).
18	TLPC1 *2	I	Frequency select input 1 of FCK2 (pin 23).
19	V_{DD}	——	+5V
20	XXTL	O	4.8MHz inverting output of XTLO (pin 21).
21	XTLO	I	4.8MHz output of crystal oscillator.
22	XTL	I	Crystal oscillator input or 4.8MHz clock input from the external circuit.
23	FCK2 *2	O	Clock output of switched capacitor filter.
24	FCK4	O	400kHz clock output of switched capacitor filter.
25	RMD	I	Received manchester DATA input.
26	TP6	O	Test output.
27	XTDS	O	TDS (pin 28) inverting output.
28	TDS	O	Transmitted manchester Data, ST output.
29	RSAT	I	Received SAT input.
30	ENBL	I	High impedance control input of TDS (pin 28) and XTDS (pin 27). Output at Open, High impedance at low level.
31	V_{SS}	——	GND
32	TP5	O	Test output.

No.	Symbol	I/O	Description
33	XTSA	O	TSAT (pin 34) inverting output.
34	TSAT	O	Transmitted SAT output.
35	TP4	O	Test output
36	SDET	O	SAT detection output.
37	SPA0	I	Transmitted SAT phase compensation input 0.(LSB).
38	SPA1	I	Transmitted SAT phase compensation input 1.
39	SPA2	I	Transmitted SAT phase compensation input 2.
40	SPA3	I	Transmitted SAT phase compensation input 3.
41	SPA4	I	Transmitted SAT phase compensation input 4.
42	SPA5	I	Transmitted SAT phase compensation input 5.(MSB).
43	V_{DD}	——	+5V
44	XTST	I	Test input, normally fixed at high level.
45	NC	——	
46	NC	——	
47	SCC0	I	SAT color code lower bit input.
48	SCC1	I	SAT color code upper bit input.

*1 320kHz Clock Duty



*2 FCK2 Chart

AMPS	Open ("H")		"L"			
TLPC2	Don't care		Open		"L"	
TLPC1	"H"	"L"	"H"	"L"	"H"	"L"
FCK2	400kHz	200kHz	400kHz	200kHz	320kHz	160kHz

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V
Topr=−34 to +75℃

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Output no load		5		mA
		I_{DDS}	Static state $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$	0		0.1	mA
Output voltage	H level	V_{OH}	$I_{OH}=-0.4$mA	4.0		V_{DD}	V
	L level	V_{OL}	$I_{OL}=2$mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leak current		I_{LI}		−10		10	μA

I/O capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Test conditions : $V_{DD}=V_I=0V$, $f_M=1MHz$

Functions

CXD1231Q-Z is a DATA and SAT LSI designed for the US cellular radio telephone system. Combined with the switched capacitor filter CXD1230M it conforms with North American AMPS (Advanced Mobile Phone Service) and British TACS (Total Access Communication System) standards.

It features the following functions.

1) Decoding of the received DATA.
2) Detection of the received SAT.
3) SAT transmission in the same frequency and phase as for received.
4) Encoding of the transmitting DATA and ST.

The following is description of each function.

Decoding of the received DATA

With the cellular radio telephone system, DATA for selecting a channel is exchanged between land and mobile stations during cell movement after circuit connection. This DATA is called WIDE BAND DATA coded in the Manchester code. Transfer speed is 20kbaud for AMPS standards and 16kbaud for TACS standards. The following diagram shows the logical values "1" and "0" of the Manchester code.

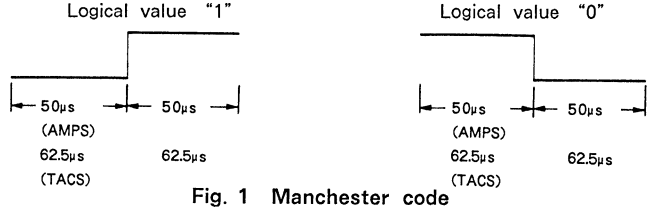


Fig. 1 Manchester code

To decode DATA input in this Manchester code, clock components are extracted by DPLL and the second half values of each bit are picked up using the clock. The decoded DATA is output as NRZ data from the output RND (Pin 9) and XRND (Pin 10) and its bit-clock is output from the output RCK (Pin 12).
Timing of RCK with RND or XRND is shown in Fig. 2.

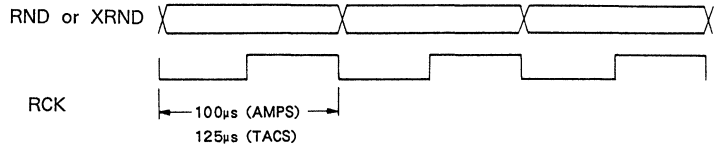


Fig. 2 Timing of RCK with RND or XRND

Detection of the received SAT

With the cellular radio telephone system, sinusoidal wave signals called SAT (Supervisory Audio Tone) are exchanged between land and mobile stations after radio link with either AMPS or TACS standards. SAT has three waves, 5.97kHz, 6.00kHz and 6.03kHz ; frequency is selected from those during cell movement. The selected one is notified in SAT color code to the mobile station by land station. During circuit connection, land and mobile stations confirm each other through reception of the designated SAT frequency.

When SAT signal with the frequency designated in SAT color code is detected, SDET (Pin 36) becomes "H".

SAT transmission with the same frequency and phase as for received

The land station confirms a mobile station through receiving SAT signal in the same frequency and phase as it has transmitted. The mobile station is required to transmit SAT signal in the same frequency and phase as received. For this purpose, the mobile station transmits the signal by phase-correcting DPLL output locked in the received SAT. Connecting the amount of phase depends on the transmitting circuit delay ; this is correctly executed by varying 64 stages in 3.6° steps (0° to 226.8°) and then further shifting the phase by 180° and selecting the output TSAT pin (Pin 34) and XTSA (inversion output of TSAT, Pin 33). Thus the phase can be compensated from 0° to 360° in 3.6° steps.

Table 1 shows the compensated value of the phase assuming that the TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Table 1

SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	Phase delay	
						TSAT	XTSA
0	0	0	0	0	0	0°	180°
0	0	0	0	0	1	3.6°	183.6°
0	0	0	0	1	0	7.2°	187.2°
⋮						⋮	⋮
1	1	0	0	0	0	172.8°	352.8°
1	1	0	0	0	1	176.4°	356.4°

Phase delay at pins TSAT and XTSA assuming that TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Encoding of the transmitting DATA and ST

ST is a signal transmitted when conversation ends or when the bell is rang. The frequency is 10kHz for AMPS and 8kHz for TACS standards. It is output from TDS (Pin 28) and XTDS (Pin 27) with the DATA and ST (NRZ) input to TND (Pin 4), In synchronization with the clock output from TCK (Pin 2), and encoded in the Manchester code. However, it does not transmit the encoded data when the control input TDSC (Pin 16) is at "L" but fixes TDS to "H" and XTDS to "L".

Timing of TCK and TND is shown in Fig. 3.

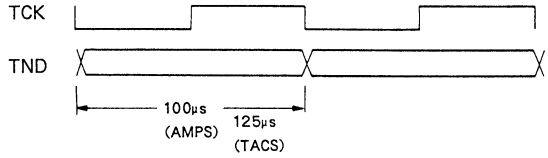
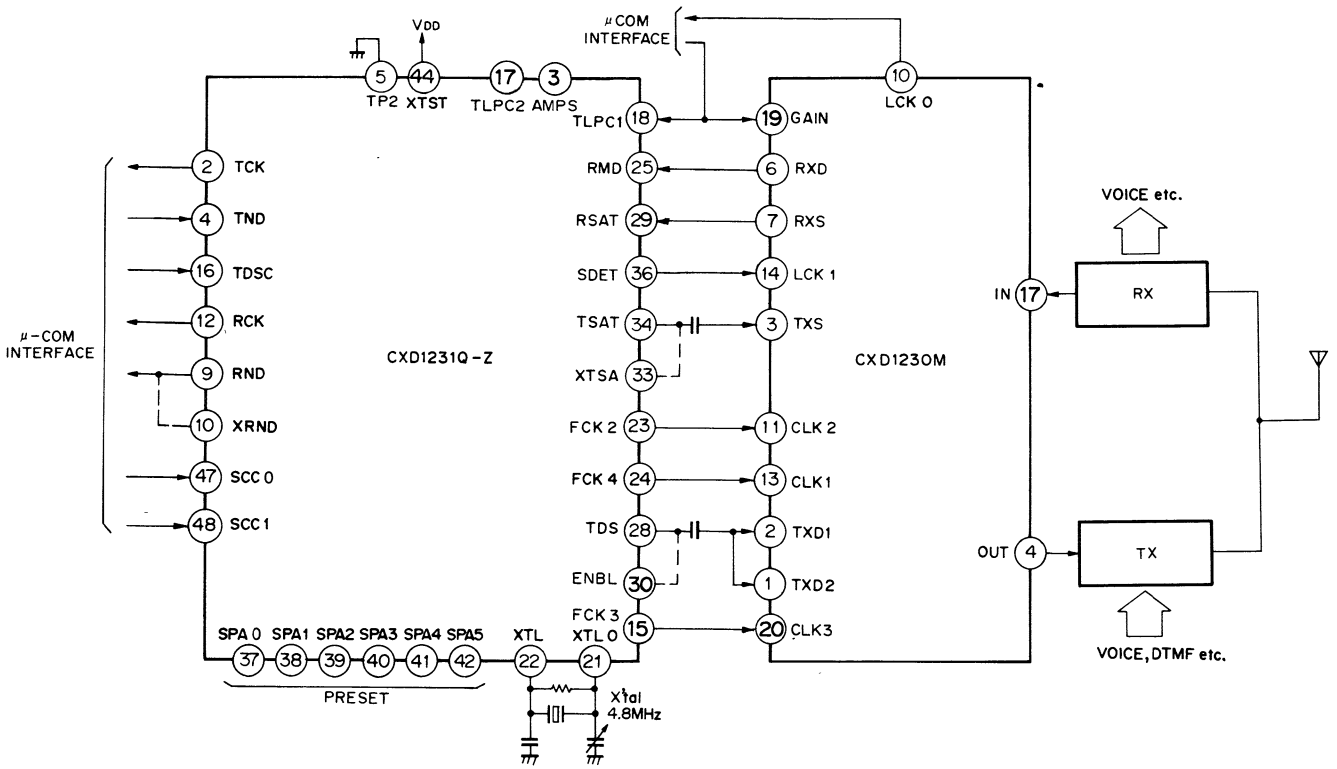


Fig. 3 Timing of TCK and TND

Application Circuit



SONY®

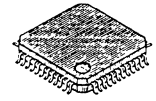
CXD1270Q/R

Modem LSI with built-in DTMF for Cellular Use

Description

The CXD1270Q/R, is a cellular radio telephone IC, combines cellular radio telephone DATA SAT LSI CXD1231Q with DTMF signal generating circuit.

CXD1270Q
48 pin QFP (Plastic)



CXD1270R
48 pin VQFP (Plastic)

Features

- Conforms with North American AMPS standards and British TACS standards
- SAT detection circuit produces few errors even with weak electric field
- DTMF signal output by pulse density modulation

Applications

AMPS/TACS cellular

Structure

Silicon gate CMOS IC

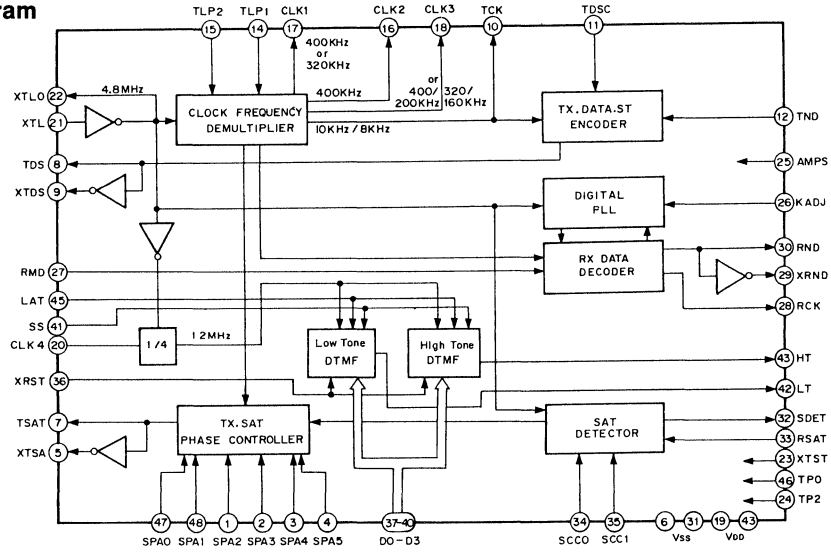
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_I	−0.3 to V_{DD}+0.3	V
• Output voltage	V_O	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

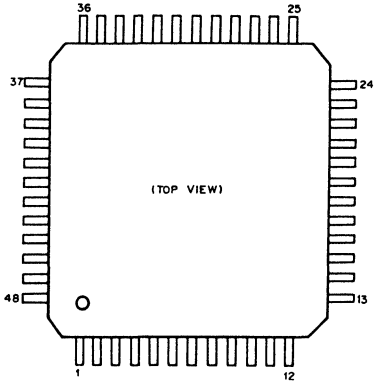
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−34 to +75	°C

Block Diagram



E90783 – ST

Pin Configuration

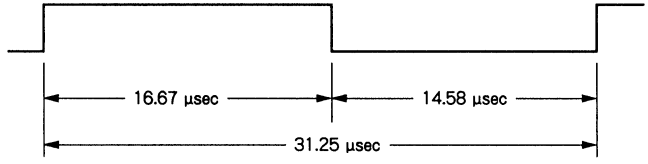


Pin Description

Pin No.	Symbol	I/O	Description
1	SPA2	I	TX SAT phase compensation input 2
2	SPA3	I	TX SAT phase compensation input 3
3	SPA4	I	TX SAT phase compensation input 4
4	SPA5	I	TX SAT phase compensation input 5 (MSB)
5	XTSA	O	TSAT (Pin 7) inverting output
6	Vss	——	GND
7	TSAT	O	TX SAT output
8	TDS	O	TX manchester DATA and ST output
9	XTDS	O	TDS (Pin 8) inverting output
10	TCK	O	TX DATA and ST CLK output
11	TDSC	I	ON/OFF control input of RX manchester DATA and ST
12	TND	I	TX NRZ and DATA input
13	ENBL	I	High impedance control input of TDS (Pin 8) and XTDS (Pin 9)
14	TLP1	I	Frequency select 1 of CLK3 (Pin 18)
15	TLP2	I	Frequency select 2 of CLK3 (Pin 18)
16	CLK2	O	CLK output for SCF (400kHz)
17	CLK1	O	CLK output for SCF (AMPS; 400kHz, TACS; 320kHz)
18	CLK3	O	CLK output for SCF
19	VDD	——	+5V
20	CLK4	O	1/4 frequency division output of crystal oscillator (1.2MHz)
21	XTL	I	Crystal oscillator input (4.8MHz)
22	XTLO	O	Crystal oscillator output
23	XTST	I	Test input (Normally fixed at low level)
24	TP2	I	

Pin No.	Symbol	I/O	Description
25	AMPS	I	AMPS/TACS mode select input (AMPS mode at open and TACS mode at low level)
26	KADJ	I	PLL lock range select input for RX manchester DATA decoder
27	RMD	I	RX manchester DATA input
28	RCK	O	CLK output extracted from RX DATA
29	XRND	O	RND (Pin 30) inverting output
30	RND	O	RX NRZ DATA output
31	Vss	——	GND
32	SDET	O	SAT detection output
33	RSAT	I	RX SAT input
34	SCC0	I	SAT collar code lower bit input
35	SCC1	I	SAT collar code upper bit input
36	XRST	I	Reset input (Active at low level)
37	D0	I/O	DTMF frequency set up bit input 0 (LSB) (Normally input mode)
38	D1	I/O	DTMF frequency set up bit input 1 (Normally input mode)
39	D2	I/O	DTMF frequency set up bit input 2 (Normally input mode)
40	D3	I/O	DTMF frequency set up bit input 3 (MSB) (Normally input mode)
41	SS	I/O	DTMF Start/Stop select input (Start at high level) (Normally input mode)
42	LT	O	DTMF low tone output
43	VDD	——	+5V
44	HT	O	DTMF high tone output
45	LAT	I	DTMF set up LATCH input
46	TP0	I	Test input (Normally fixed at high level)
47	SPA0	I	TX SAT phase compensation input 0 (LSB)
48	SPA1	I	TX SAT phase compensation input 1

320kHz Clock Duty



CLK3 Chart

AMPS	Open ("H")		"L"	
TLP2	Don't care		"L"	
TLP1	"H"	"L"	"H"	"L"
CLK3	400kHz	200kHz	320kHz	160kHz

Electrical Characteristics

1) DC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	At operation		5		mA
	I_{DDS}	At stand still V_{IH}=V_{DD}, V_{IL}=Vss			0.1	mA
Output voltage	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5			V
	V_{OL}	I_{OL}=4mA			0.4	V
Input leak current 1	I_{LI1}	Normal pin	–10		10	μA
Input leak current 2	I_{LI2}	Bidirectional pin (During input)	–40		40	μA
Input voltage	V_{IHC}	CMOS input	0.7V_{DD}			V
	V_{ILC}				0.3V_{DD}	V
	V_{IHT}	TTL input	2.2			V
	V_{ILT}				0.8	V
	V_{T^+}	Schmitt trigger input	0.8V_{DD}			V
	V_{T^-}				0.2V_{DD}	V
	V_{T^+}–V_{T^-}		0.7	0.9		V

2) I/O level of each pin

I/O level		Pin name
Input level	CMOS level	SPA0 to SPA5, TDSC, TND, TLP1, TLP2, XTST, TP2, AMPS, KADJ, RMD, RSAT, SCC0, SCC1, D0 to D3, SS, LAT, TP0
	TTL level	ENBL
	Schmitt trigger	XRST
Output level	CMOS level	XTSA, TSAT, TDS, XTDS, TCK, CLK1 to CLK4, RCK, XRND, RND, SDET
	Tri-state	LT, HT

3) Oscillation cell electrical characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logical threshold	LVth			V_{DD}/2		V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Incorporated feedback resistance	R_{FB}	V_{IH}=Vss or V_{DD}	500K	2M	5M	Ω
Output voltage	V_{OH}	I_{OH}=–1mA	V_{DD}/2			V
	V_{OL}	I_{OL}=1mA			V_{DD}/2	V

4) I/O capacitance

(V_{DD}=V_I=0V, f_M=1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
I/O pin	$C_{I/O}$			11	pF

5) Pull up/down processing pin

Processing	Pin name
Pull up	SPA0 to SPA5, ENBL, TLP2, AMPS
Pull down	TND

6) AC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Set up time for D0 to D3 LAT			30			ns

Functions

CXD1270Q/R is a DATA and SAT LSI designed for the cellular radio telephone system. Combined with the switched capacitor filter CXD1230M or CXD1237Q/R it conforms with North American AMPS (Advanced Mobile Phone Service) and British TACS (Total Access Communication System) standards.
It features the following functions.

1) Decoding of the received DATA.
2) Detection of the received SAT.
3) SAT transmission in the same frequency and phase as for received SAT.
4) Encoding of the transmitting DATA and ST.

The following is description of each function.

Decoding of the received DATA

With the cellular radio telephone system, DATA for selecting a channel is exchanged between land and mobile stations during cell movement after circuit connection. This DATA is called WIDE BAND DATA coded in the Manchester code. Transfer speed is 20kbaud for AMPS standards and 16kbaud for TACS standards. The following diagram shows the logical values "1" and "0" of the Manchester code.

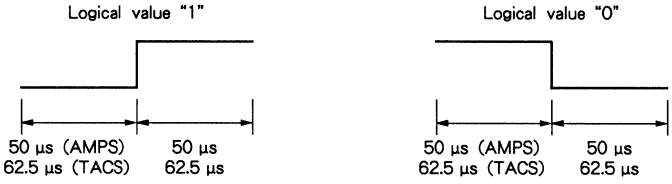


Fig. 1. Manchester code

To decode DATA input in this Manchester code, clock components are extracted by DPLL and the second half values of each bit are picked up using the clock. The decoded DATA is output as NRZ data from the output RND (Pin 30) and XRND (Pin 29) and its bit-clock is output from the output RCK (Pin 28).
Timing of RCK with RND or XRND is shown in Fig. 2.

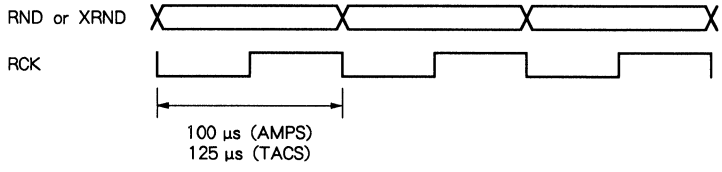


Fig. 2. Timing of RCK with RND or XRND

Detection of the received SAT

With the cellular radio telephone system, sine wave signals called SAT (Supervisory Audio Tone) are exchanged between land and mobile stations after radio link with either AMPS or TACS standards. SAT has three waves, 5.97kHz, 6.00kHz and 6.03kHz; frequency is selected from those during cell movement. The selected one is notified in SAT collar code to the mobile station by land station. During circuit connection, land and mobile stations confirm each other through reception of the designated SAT frequency.

When SAT signal with the frequency designated in SAT collar code is detected, SDET (Pin 32) becomes "H".

SAT transmission in the same frequency and phase as for received SAT

The land station confirms a mobile station through receiving SAT signal in the same frequency and phase as it has transmitted. The mobile station is required to transmit SAT signal in the same frequency and phase as received. For this purpose, the mobile station transmits the signal by phase-correcting DPLL output locked in the received SAT. Connecting the amount of phase depends on the transmitting circuit delay; this is correctly executed by varying 64 stages in 3.6° steps (0° to 226.8°) and then further shifting the phase by 180° by means of selecting the output TSAT pin (Pin 7) and XTSA (inverting output of TSAT, Pin 5). Thus the phase can be compensated from 0° to 360° in 3.6° steps.

Table below shows the compensated value of the phase assuming that the TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	Phase delay	
						TSAT	XTSA
0	0	0	0	0	0	0°	180°
0	0	0	0	0	1	3.6°	183.6°
0	0	0	0	1	0	7.2°	187.2°
			⋮			⋮	⋮
1	1	0	0	0	0	172.8°	352.8°
1	1	0	0	0	1	176.4°	356.4°

Table 1. Phase delay at pins TSAT and XTSA assuming that TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Encoding of the transmitting DATA and ST

ST (Signaling Tone) is a signal transmitted when conversation ends or when the bell is rang. The frequency is 10kHz for AMPS and 8kHz for TACS standards. It is output from TDS (Pin 8) and XTDS (Pin 9) with the DATA and ST (NRZ) input to TND (Pin 12), in synchronization with the clock output from TCK (Pin 10), and encoded in the Manchester code. However, it does not transmit the encoded data when the control input TDSC (Pin 11) is at "L" but fixes TDS to "H" and XTDS to "L".

Timing of TCK and TND is shown in Fig. 3.

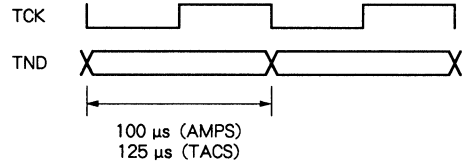


Fig. 3. Timing of TCK and TND

DTMF Block

(1) Setting of frequency (frequency division ratio)

Low Tone (Hz)	Frequency division ratio N	Realized frequency f (Hz)	D3	D2	D1	D0
697	143	699.3	0	0	0	0
770	130	769.2	0	0	0	1
852	117	854.7	0	0	1	0
941	106	943.3	0	0	1	1
2K	50	2000	0	1	0	0

High Tone (Hz)	Frequency division ratio N	Realized frequency f (Hz)	D3	D2	D1	D0
1209	83	1204.8	1	0	0	0
1336	75	1333.3	1	0	0	1
1477	68	1470.6	1	0	1	0
1633	61	1639.3	1	0	1	1
2K	50	2000	1	1	0	0

Note) Besides the frequency for LT and HT, employed for the usual push button, a 2kHz frequency can be output at both LT and HT.

(2) Setting of LT, HT Start/Stop

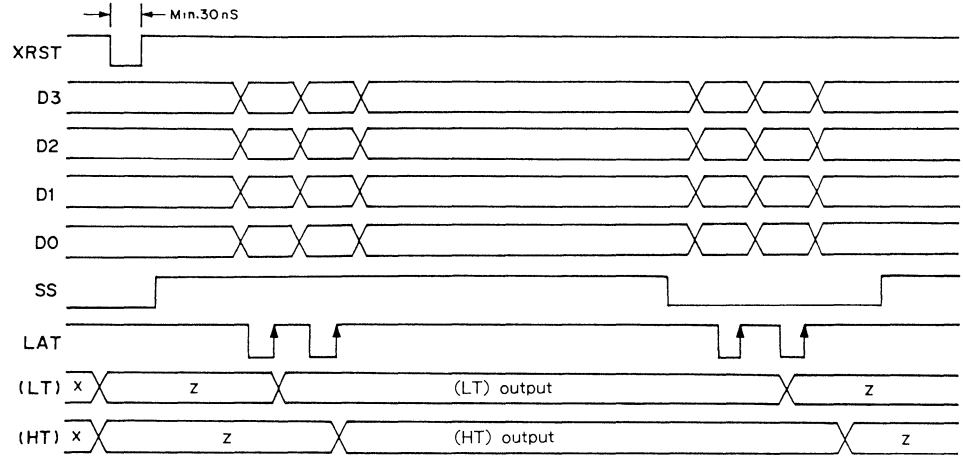
Start/Stop for both LT and HT is controlled through SS input signal.

	SS	LAT
LT, HT Start	1	⌐
LT, HT Stop	0	⌐

(3) LT, HT output

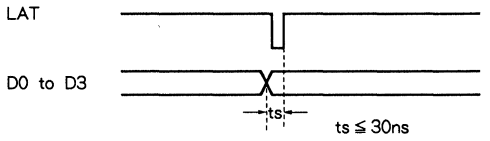
LT and HT outputs are output by pulse density modulation system. This system means frequency, obtained at frequency division ratio **N** determined by **D0** to **D3**, divided 1/12 frequency division sine wave counter, and outputs pulse waveform varied with density suitable for each count value. These outputs, tri-state output system, is controlled through start/stop signal.

(4) Timing chart

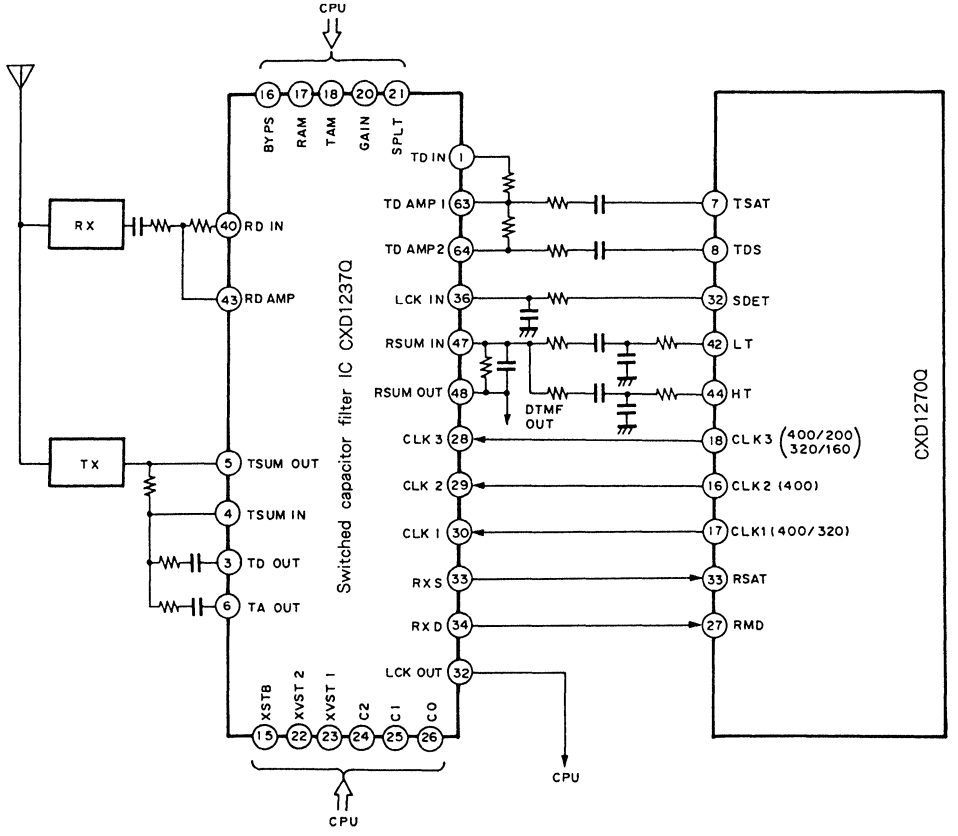


Note) LT, HT distinction is controlled through D3.
D3= "High" ...HT, D3= "Low" ...LT
After resetting, at the point where the first SS= "High" is read at LAT rising edge, LT (HT) output starts. At the same time data of D0 to D3 is loaded in and the frequency division ratio is set.
Also, SS= "Low" is read and LT (HT) is stopped. In such case, for D3 only it is necessary to set "Low" and "High" for the respective distinction of LT and HT. However D0 to D2 is ignored.

AC Characteristics Timing Diagram

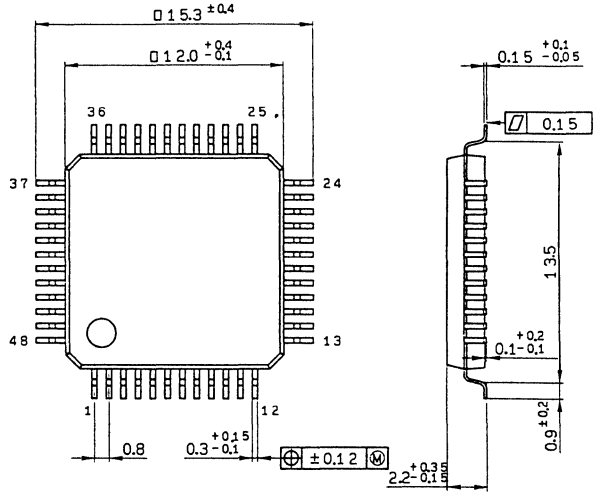


CXD1270Q/R and CXD1237Q/R Connecting Example (CXD1237: QFP Pin No.)



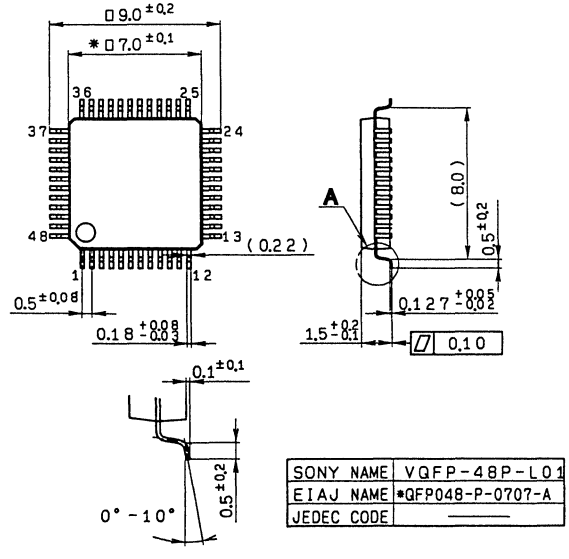
Package Outline Unit : mm

CXD1270Q 48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXD1270R 48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue

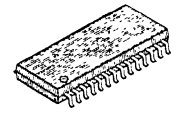
SONY CXD1233M

Cordless Telephone Modem IC

Description

CXD1233M developed for cordless telephones, provides a modem when used in conjunction with microcomputor and filter.

28pin SOP(Plastic)



Features

- Uses the low error rate manchester code, decoder and encoder.
- Built-in comparator for received manchester data.
- Compatible with 4 types of data transfer speeds.
- Wide supply voltage range
- Low power consumption

Application

Cordless telephone
(Low power, Digital direct modulation type)

Structure

Silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

• Supply voltage	V_{DD}	V_{SS}-0.5 to +7.0	V
• Input voltage	V_I	V_{SS}-0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}-0.5 to V_{DD}+0.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C

Recommended Operating Condition

• Supply voltage	V_{DD}	3.0 to 5.0 (Typ. 3.6)	V

Electrical Characteristics

V_{DD} = 3.0 to 5.0V, V_{SS} = 0V, T_{opr} = −20 to +75°C

Item		Symbol	Min.	Typ.	Max.	Unit
Supply current (Output pin at no load)		I_{DD}		1		mA
Input voltage		V_{IHC}	0.7V_{DD}			V
		V_{ILC}			0.3V_{DD}	
Output voltage	I_{OH} = −1mA	V_{OHI}	V_{DD}-0.5			V
	I_{OL} = 2mA	V_{OLI}			0.4	V
Input leak current		I_{LII}	−10		10	μA
Output leak current	Tristate pin (During high impedance)	I_{LZ}	−40		40	μA

E89Y08-HP

Oscillation Cell Electrical Characteristics

V_{DD} = 3.0 to 5.0V, V_{SS} = 0V, T_{opr} = −20 to +75°C

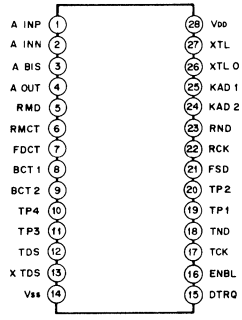
Item		Symbol	Min.	Typ.	Max.	Unit
Logic threshold value		LV_{th}		$V_{DD}/2$		V
Input voltage		V_{IH}	0.7V_{DD}			V
		V_{IL}			0.3V_{DD}	V
Feedback resistance	V_{IN} = V_{SS}, or V_{DD}	R_{FB}	500K	2.6M	8M	Ω
Output voltage	I_{OH} −0 5mA	V_{OH}	$V_{DD}/2$			V
	I_{OL} 0.5mA	V_{OL}			$V_{DD}/2$	V

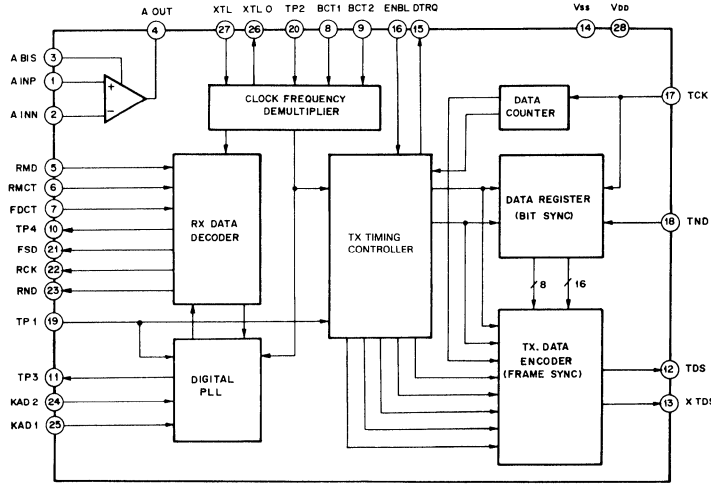
I/O Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF

Test conditions: V_{DD} = V_I = 0V, f = 1 MHz

Block Diagram and Pin Configuration





Pin Description

No.	Symbol	I/O	Description
1	AINP	I	Comparator non-inverted input for received manchester data.
2	AINN	I	Comparator inverted input for received manchester data.
3	ABIS	I	Comparator bias setting input for received manchester data.
4	AOUT	O	Comparator output for received manchester data.
5	RMD	I	Received manchester data input.
6	RMCT	I	Pin for the selection of inverted RMD (Normally fixed at 'L' at 'H' Data inverted)
7	FDCT	I	Pin for the selection of frame sync pattern ('L' for Hand set, 'H' for Base set)
8	BCT1	I	Data bit rate selection (BCT 1, BCT 2) Normally (H,H): Compatible with 1200bps (L,L): Compatible with 600bps (L,H): Compatible with 4800bps (H,L): Compatible with 2400bps
9	BCT2	I	
10	TP4	O	Output for test
11	TP3	O	Output for test
12	TDS	O	Transmitted manchester data output
13	XTDS	O	Inverted TDS (Pin 12)
14	Vss	–	GND pin
15	DTRQ	O	Data request output for transmission.
16	ENBL	I	Enable input (ENABLE at 'L')
17	TCK	I	Clock input synchronous with TND (pin 18)
18	TND	I	NRZ data input for transmission.
19	TP1	I	Test input (normally fixed at 'L')
20	TP2	I	Test input (normally fixed at 'L')
21	FSD	O	Frame sync detection output.
22	RCK	O	Clock output extracted from transmitted data.
23	RND	O	Transmitted NRZ data output.
24	KAD2	I	PLL logic range select input for transmitted manchester data.
25	KAD1	I	
26	XTLO	O	Crystal oscillator output (4.608MHz)
27	XTL	I	Crystal oscillator input or external clock input (4.608MH)
28	VDD	–	Supply pin

Operation

Transmitted data decode

With the cordless telephone system data exchanges are done between HS (Hand Set) and BS (Base Set).

Data format is as follows:

Bit Sync	Frame Sync	ID + Error Correction Data	Control Data
12 bit or more	16 bit	37 bit (1 bit is twice sync signal 1 bit)	

Bit sync: Signal that indicates the beginning of data '01010101 . . . . .' that is the repetition of '0' and '1' data for 12 bit or more.

Frame sync: 16 bit signal that indicates whether the data is from BS to HS or from HS to BS.

For HS data (BS→HS) FDCT = "L"
1100010011010110

For BS data (HS→BS) FDCT = "H"
1001001100110110

ID + correction compensation data: a 37-bit manchester code.

Control code: The number of bits varies according to the type of equipments. However it should be a figure divisible by 8 when added to 37-bit. Manchester code.

Bit sync and Frame sync are NRZ data. Then the manchester code data where each bit is inverted at its middle and the latter half indicates the logic value. This bit's length is twice that of the bit sync or frame sync. The manchester code logic value "1", "0" is indicated in the Fig. below.

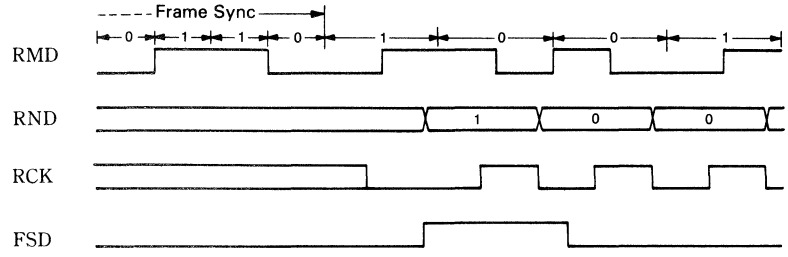
t the time for one bit of the manchester code changes according to the value of BCT 1 and BCT 2. t is compatible with the 4 types of transmission speed of data.

Bit rate

Table 1

BCT1	BCT2	Bit rate	t
0	1	4800BPS	208.3μs
1	0	2400BPS	416.7μs
1	1	1200BPS	833.3μs
0	0	600BPS	1666.7μs

To decode data input through RMD pin, clock components are extracted at D–PLL and using this clock the frame sync signal is detected. Moreover the manchester code logic value is extracted. The frame sync detection signal is output from FSD pin, decoded data is output from RND pin as NRZ. That bit clock is output from RCK pin.



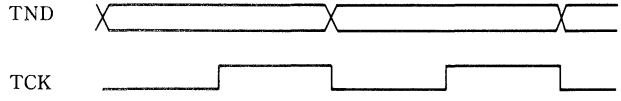
Transmission data encode

Data format in Fig. is assembled through ENBL, TCK and TND that have been sent from μ-COM, and output from TDS and XTDS. The speed of output data matches the bit rate shown in table 1. As ENBL signal is output, the bit sync signal begins to be output from TDS and XTDS. Consequently the frame sync signal depending on FDCT value, is output.

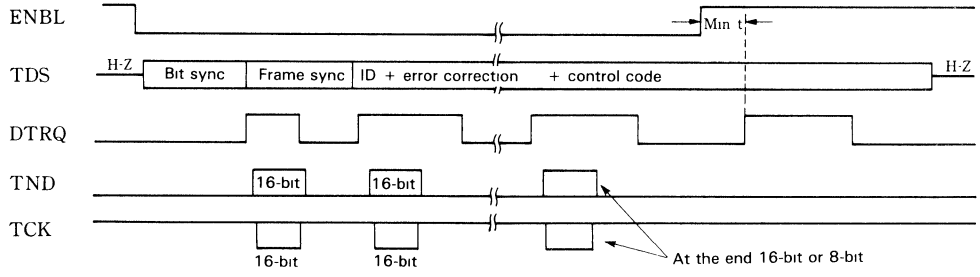
When FDCT = 'L' '1001001100110110'
When FDCT = 'H' '1100010011010110' } Frame sync signal

Simultaneously as the frame sync begins to be output, 'H' is output from DTRQ pin and requests data to μ-COM.

DTRQ becomes a clock pulse and is output. Then every time DTRQ = H is on, from μ-COM, NRZ data is sent to TND and the clock is sent the required number of times, 16-bit at a time. As data comes in a number of bits multiplied by 8, data transmitted at the end comes in either 16-bit or 8-bit. The timing of TND and TCK is shown in the Fig. below.

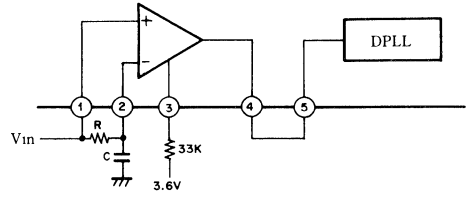


Data input at NRZ is encoded to manchester code and output from TDS and XTDS. As data and clock transmission from μ-COM to TND and TCK ends, ENBL should go back to 'H' before the next DTRQ-'H' turns on, in terms of time t (Table 1). ENBL = 'H' state is on, and as manchester code output ends, TDS and XTDS turn to H–Z (High impedance).



Transmission data timing

Operation of Built-in AMP



The built-in amplifier in CXD1233M serves to interface between the band limitation LPF (fc:about 3kHz) and the DPLL. It can be used as a comparator to amplify the filter output level (100mVrms) up to logic amplitude. Here as DC to low pass contained in the filter output, is output by means of a primary RC filter to become the comparator comparison voltage, as a result. There is not need to rely on the DC offset of the filter output and drift, since the comparator output duty can be maintained at around a stable 50%.

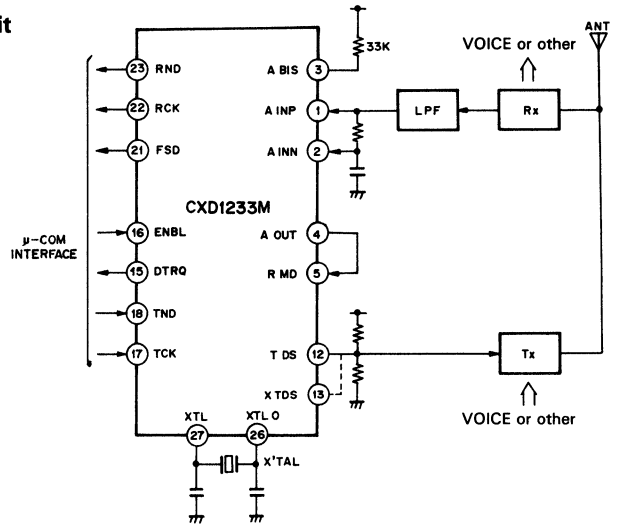
When R = 22kΩ, and C = 1μF, the primary RC filter cut off frequency becomes 7Hz (–3dB).

Electrical Characteristics

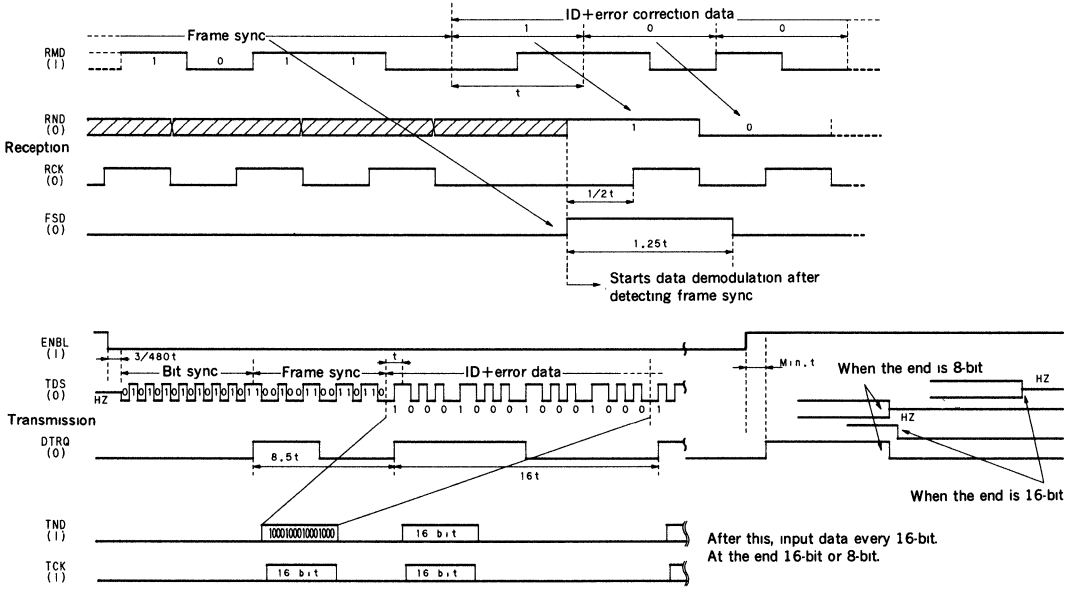
$T_a = 25°C$, $V_{DD} = 3.6V$

Item	Test conditions	Min.	Typ.	Max.	Unit
Offset voltage	Input conversion			50	mV
Open loop gain	DC gain	20			dB
Input level	f = 1.2kHz		100		mV_{rms}

Application Circuit

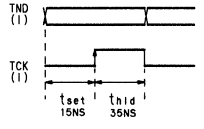


CXD1233M Reception/Transmission Timing chart



Divide ID+error data into 16-bit and input them from TND as NRZ signal. TCK is input clock. Inputs the first 16-bit within 8.5t. From the next 16-bit, input within 16t.

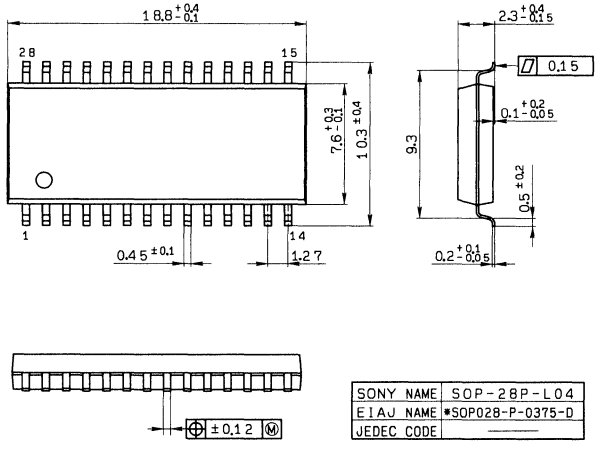
Input starts when DTRQ (data request) is high.



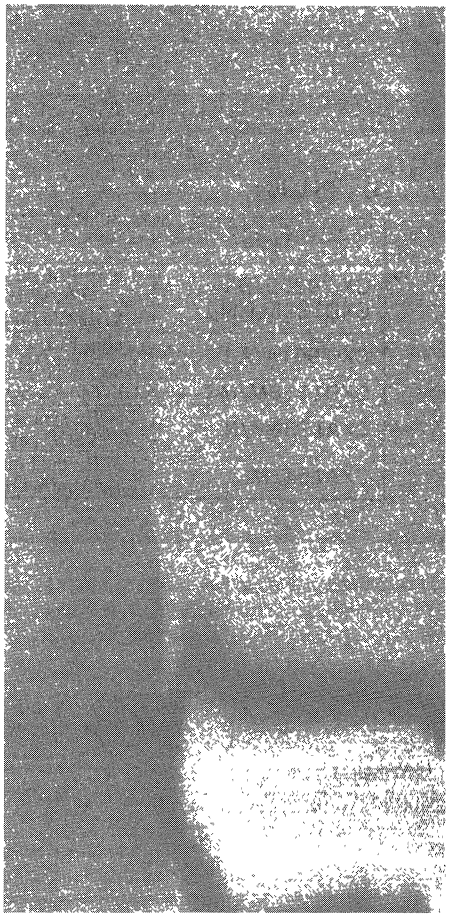
Bit rate	t (us)
4800	208.3
2400	416.7
1200	833.3
600	1666.7

Package Outline Unit: mm

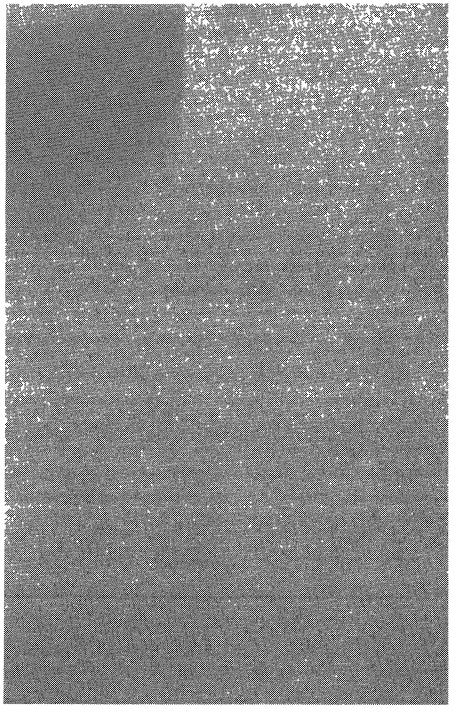
28pin SOP (Plastic) 375mil 0.7g



SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	———



PLL ICs



3) PLL ICs

Type	Function	Page
CX-7925B/B-1 CXD1225M/M-1	1 chip PLL IC for low power cordless phone in Japan f_{MAX}=382MHz CXD1225M/M-1 is CX-7925B's SOP package version	177
CX-7961A/A-1	1 chip PLL IC for low power cordless phone in Japan f_{MAX}=255MHz	188
CXD1118M/M-1	CX-7961A's SOP package version	199
CXA1356M/N	1.5GHz synthesizer PLL for cellular equipment (NEW) 16P VSOP package	211
CXA1541M	1.2GHz dual mudulus prescaler for cellular equipment ☆ I_{CC}=3.5mA MB501 pin compatible	219

☆: Under development
(New): New device

Frequency Synthesizer PLL

Description

CX-7925B/CXD1225M are used for the digital selection of TV broadcasting as well as AM, FM and various radio waves. These PLL IC's were developed through high speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is guaranteed as follows.
  CX-7925B/CXD1225M } 300MHz
  CX-7925B-1/CXD1225M-1 } 350MHz
  Usage up to 1GHz is possible when combined with an ECL (general-purpose) prescaler.
- Programmable divider permits the division of a program frequency up to 1/262, 151
- Programmable reference divider permits the selection of comparison frequency at will.
  (E.G. Using a 4MHz crystal oscillator selection from 244Hz to 2MHz is possible)
- High-speed phase comparator provides high C/N ratio.
- Operation control through 3pins.
- 3 independent pins (AM1, FM1, TV1) are provided for the signal input at respective frequencies.
- Multipurpose output terminals are provided (A0, B0)
- Low consumption (Standard: 120W)

Structure

N-channel silicon gate MOS

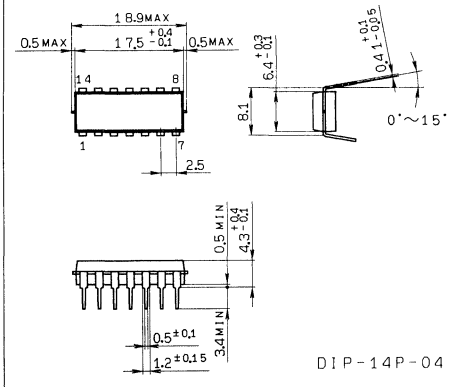
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Input pin voltage	V_{IN}	−1 to +7	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Starage temperature	T_{stg}	−55 to +150	°C

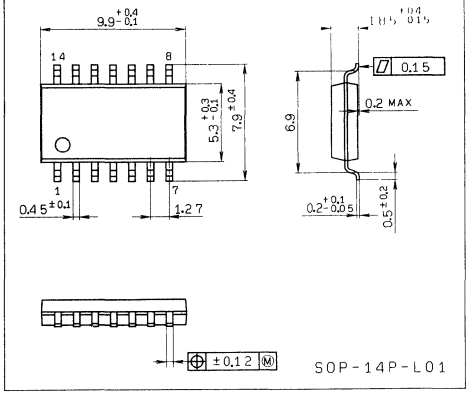
Package Outline

Unit: mm

CX-7925B/7925B-1 14pin DIP (Plastic)



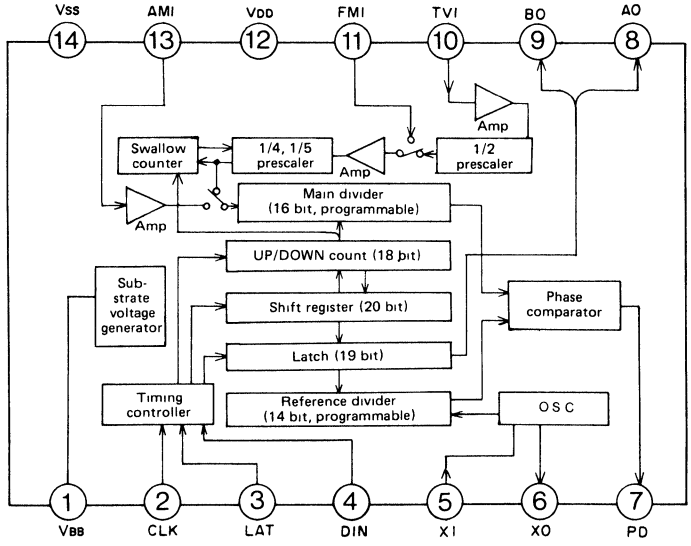
CXD1225M/1225M-1 14pin SOP (Plastic)



Recommended Operating Conditions

Item	Pin Remarks	Symbol	Operating range	Unit
Supply voltage		V_{DD}	+4.5 to +5.5	V
High level input voltage	CLK, DIN LAT	V_{IH}	+2.6 to V_{DD} +0.5	V
Low level input voltage		V_{IL}	−1.0 to 0.8	V
High frequency signal input amplitude	TVI	e_{IN}	0.3 to 4.0	Vp-p
High frequency signal input amplitude	FMI	e_{IN}	0.2 to 4.0	Vp-p
High frequency signal input amplitude	AMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	XI	e_{IN}	0.6 to 4.0	Vp-p
Operating temperature		T_{opr}	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

No.	Symbol	Description
1	V_{BB}	Substrate pin. (Connect 0.01μF capacitor between this pin and GND)
2	CLK	Clock input pin for 20bit serial data input.
3	LAT	Latch signal input pin for shift register input data (latched with signal rise) Also, Up/Down clock input pin (state changes with signal rise)
4	DIN	Data input pin. Also, Up/Down mode select pin (Up at 'H' level, Down at 'L' level)
5	XI	Crystal oscillator connection pin for reference signal generation. (Max. 13MHz Standard 4.0MHz)
6	XO	
7	PD	Phase comparator output pin (3States)
8	AO	External control signal output pin/unlock output pin (E/E MOS push-pull)
9	BO	External control signal output pin/data check pin (E/E MOS push-pull)
10	TVI	High frequency signal input pin (Max. 300MHz or 350MHz) 1/2 prescaler built-in.
11	FMI	High frequency signal input pin (Max. 150MHz or 180MHz)
12	V_{DD}	Supply (+5V)
13	AMI	High frequency signal input pin (Max. 40MHz or 50MHz)
14	V_{SS}	Ground pin

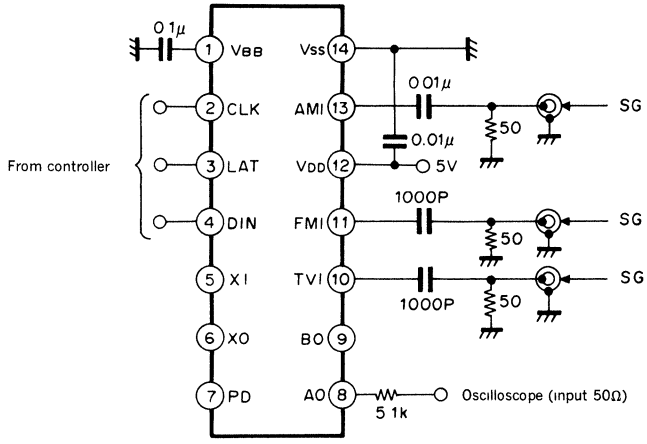
Electrical Characteristics

(Within Recommended Operation Conditions range, unless otherwise specified) V_{SS}=0V

Item	Pin, Remarks	Symbol	Conditions	CX-7925B/ CXD1225M			CX-7925B-1/ CXD1225M-1			Unit
				min.	Typ.	Max.	min.	Typ.	Max.	
Operating supply current	V_{DD}	I_{DD}	Note2		24	40		28	40	mA
Operating input frequency	TVI	f_{OP}	e_{IN}=0.3 to 4.0Vp-p	20		300	20		350	MHz
	FMI	f_{OP}	e_{IN}=0.2 to 4.0Vp-p	20		150	20		180	MHz
	AMI	f_{OP}	e_{IN}=0.2 to 2.5Vp-p	0.05		40	0.05		50	MHz
Input leak current	Logic input	I_{IL}	V_{IH}=0 to V_{DD} Note1	−10		+10	−10		+10	μA
High level output current	Phase comparator (3 value output) PD	I_{OH}	V_{OUT}=3V Note2			−0.2			−0.2	mA
Low level output current		I_{OL}	V_{OUT}=1V Note2	+0.2			+0.2			mA
High impedance leak current		I_{HZ}	V_{OUT}=2V Note1	−50		+50	−50		+50	nA
High level output voltage	Push-pull by E/E MOS: Composition AO, BO	V_{OH}	I_{OH}=−20μA	2.8			2.8			V
Low level output voltage		V_{OL}	I_{OL}=1mA			0.6			0.6	V

Note 1) Ta=25°C
Note 2) V_{DD}=5V Ta=25°C

Operating Input Frequency Test Circuit



Control input data to CX-7925B/CXD1225M: T1-H, T2-H, A-L, B-H
SG: HP's 8640B
(Input level read directly at built-in level meter)

Operation

〔1〕 Signal input from the local oscillator

CX-7925B/CXD1225M use 3 independent input pins according to frequency and application.

- AMI pin

  Reception pin for AM and TV broadcast. Signal input up to 40MHz is warranted for CX7925B/CXD1225M and 50MHz for CX-7925B-1/CXD1225M-1.

  Frequency division ratio when using this pin is 1/2 to 1/65537.

- FMI pin

  Reception pin for FM and TV broadcast. Signal input up to 150MHz is warranted for CX-7925B/CXD1225M and 180MHz for CX-7925B-1/CXD1225M-1, Accordingly the external prescaler is not required for FM reception. For TV reception, the entire TV bandwidth can be overed through combination with an external prescaler up to 1/8. Frequency division ratio ranges from 1/12 to 1/262151. When not in use this pin stays open.

- TVI pin

  This pin is solely used for TV broadcast reception. With the built-in 1/2 prescaler signal input up to 300MHz is warranted for CX-7925B/CXD1225M and 350MHz for CX-7925B-1/CXD1225M-1. The entire bandwidth can be covered through combination with an external prescaler up to 1/4. Frequency division ratio ranges from 1/24 to 1/524302. When not in use this pin is grounded internally via a resistor of more than 100kΩ.

〔2〕 Phase comparator output

The phase comparator output (PD pin) has a 3-level value. The pin is at High level when the input signal is more aduanced in phase than the reference signal. At Low level when the phase lags behind and at high impedance when they are in phase.

〔3〕 Control signal and control system

CX-7925B/CXD1225M are designed as controllers compatible with general 4 or 8-bit microcomputers. There are 3 control input pins CLK, LAT, DIN and 2 control output pins AB and BO. Through the proper combination of these pins, the simplification and multi-functionalization of the system can be realized.

CX-7925B/CXD1225M feature 3 data input modes, (normal mode), Up/Down mode and Data check mode with different signal input patterns for each.

[3-1] Control signal input modes

(a) Data input mode (normal mode)

To set all initial values of CX-7925B/CXD1225M a total of 40bit of data has to be input 20bits at a time. With LAT pin at Low, as data is input to DIN pin, data is input to the shift register 1bit at a time with the rising edge of the clock input to CLK pin.

After 20bit of data has been transmitted to the shift register, with CLK at High as LAT pin is set to High, data is latched, (after data is latched, turn LAT pin back to Low, Varying DIN and CLK pins while LAT pin is at High may affect data internally).

As will be described in detail later on, input data is input either in the programmable divider or the reference divider according to the state of the last bitC. In practice input from the controller the 20bit of the data including first the reference divider frequency, input pin selection and AO, BO output pins data using the above methed. Here the data last bit is set to Low.

Next input 20bit including data used to set the programmable divider, in the same way. Here set the last bitC to High. This sets all internal states. After that, to vary only the programmable divider value, varying only the latter 20bit of data will suffice (In this case too, C is to be set to High).

To vary the programmable divider value (channel selection, AFT) the usage of Up/Down mode mentioned hereafter will improve efficiency.

(b) UP/DOWN mode

After setting CLK pin to Low, the contents of UP/DOWN counter can be increased or decreased by one according to DIN pin High, Low level. This by turning LAT pin (normally at Low level) from High to Low. By repeating this process the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

This mode is used to check if data has been correctly input from the controller to the data register. Data left in the shift register immediately after input data has been latched is output bit by bit from BO pin. This at the rising edge of a clock input pin and at to CLK pin while it is held to High and after LAT pin is set to Low. The shift register data can only be output from BO pin when bits T1 and T2 of the data are at High and Low, respectively.

[3-2] Control data assignment

CX7925B/CXD1225M is assigned in 20bits. The last 2bits are the data identification code. Identifying the code will tell the data contents. Though unrelated to users, switching to Test mode is also performed using this code. Each of the programmable divider and reference divider frequency number is given in binary value with LSB at the leading digit.

(a) Control input data of the Reference divider (C=Low)

This can be described as the initialization setting data. It is always input when power is fed or when a channel band is switched. The input data composition is as follows.

	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	PI1	PI2	A	B	T1	C
	LSB													MSB						

- R0 to R13 ; Reference divider frequency division numbers. (binary value with R0 as LSB)
  There is an offset element between the input data and the actual frequency division numbers. The relationship being (actual frequency division numbers)=(Input data+2)
- PI1, PI2 ; Specification of the signal input pin.

Input / PI1, PI2	AMI	FMI	TVI
PI1	—	L	H
PI2	L	H	H

• A, B, T1 ; Each of AO and BO pins features 2 functions selected according to T1 value. When T1 is at Low, A and B values are output as they are to AO and BO pins. These signals can be used to select the prescaler frequency division, the filter constant, the channel band signal and various other purposes. When the prescaler M54465P (mitsubishi) for TV reception is used the following selection codes for frequency division ratio apply.

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at High, AO output pin outputs the phase comparator LOCK/UNLOCK state.
AO pin H; UNLOCK
L; LOCK
BO pin becomes, as described in Paragraph〔3-1〕C for Data check mode, the shift register data output pin.Through the clock input to CLK pin the shift register content is continuously output. Note that when T1 is at High, AO and BO pins can not be used for external control.

• C ; This code determines the latch direction of the input data. In this case, set to Low.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C=High)
This data determines the Programmable divider frequency division ratio.

N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C
LSB																	MSB		

• N0 to N17; Programmable divider frequen division numbers. (Binary value with N0 as LSB) The actual frequency division number differs according to the pin selected for the signal input as follows.

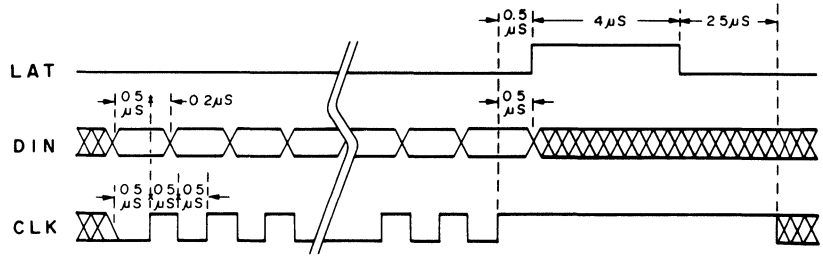
Control data		Input pin	N frequency division input data range	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
—	L	AMI	0 to 65535	N+2	2 to 65537
L	H	FMI	4 to 262143	N+8	12 to 262151
H	H	TVI	4 to 262143	2 • (N+8)	24 to 524302

- T2 ; T2 is used for Test mode selection.Users usually set this data to Low. To test the frequency division output and reference output this T2 bit and afore mentioned T1 bit are set to High while A and B bits are set to Low. Then, a reference output and a frequency division output can be observed at AO and Bo pins respectively.
- C ; As described before, set to High in this case.

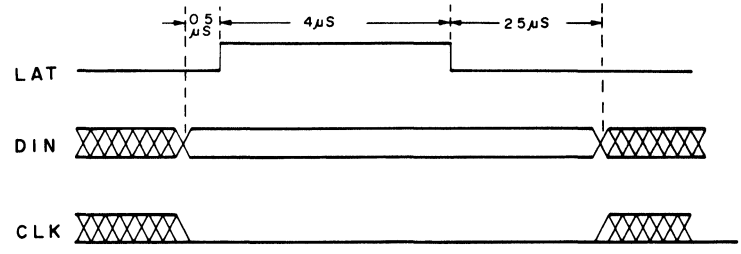
[3-3] Data input and control signal timing

(a) Data input mode (normal mode)

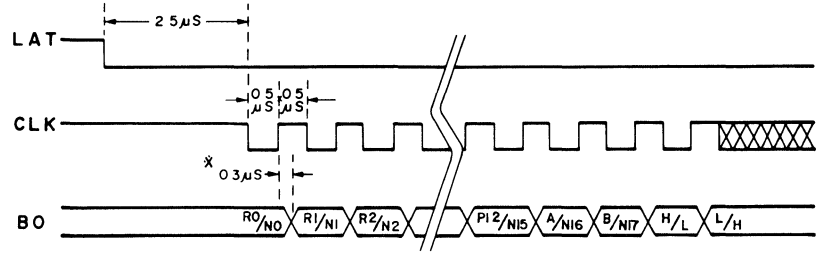
Various timings show the minimum value unless otherwise indicated.



(b) UP/DOWN mode



(c) DATA CHECK mode (Shift register data check)



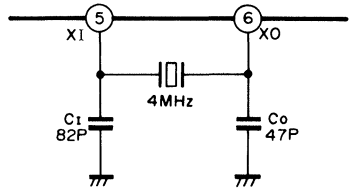
(※ Mark indicates data is output within this timing)

〔4〕 Reference signal (Reference divider input signal)

The connection of a chrystal oscillator to X1 and XO allow these IC's to generate reference signals. The input of an external clock signal to X1 pin permits the usage of an external clock as reference signal.

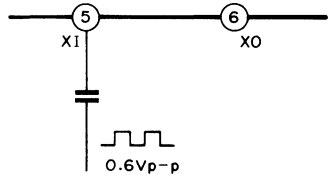
〔4-1〕 Reference signal generation by means of built-in oscillator

Connect a chrystal oscillator with a frequency of 1MHz to 13MHz to X1 and XO pins, as shown below. The diagram below shows an example where a standard 4MHz osillator is used. The capacitance ratio of C_1, C_O should be 1 to 2 : 1 while their serial capacitance values should be the specific load capacitance of the chrystal oscillator.

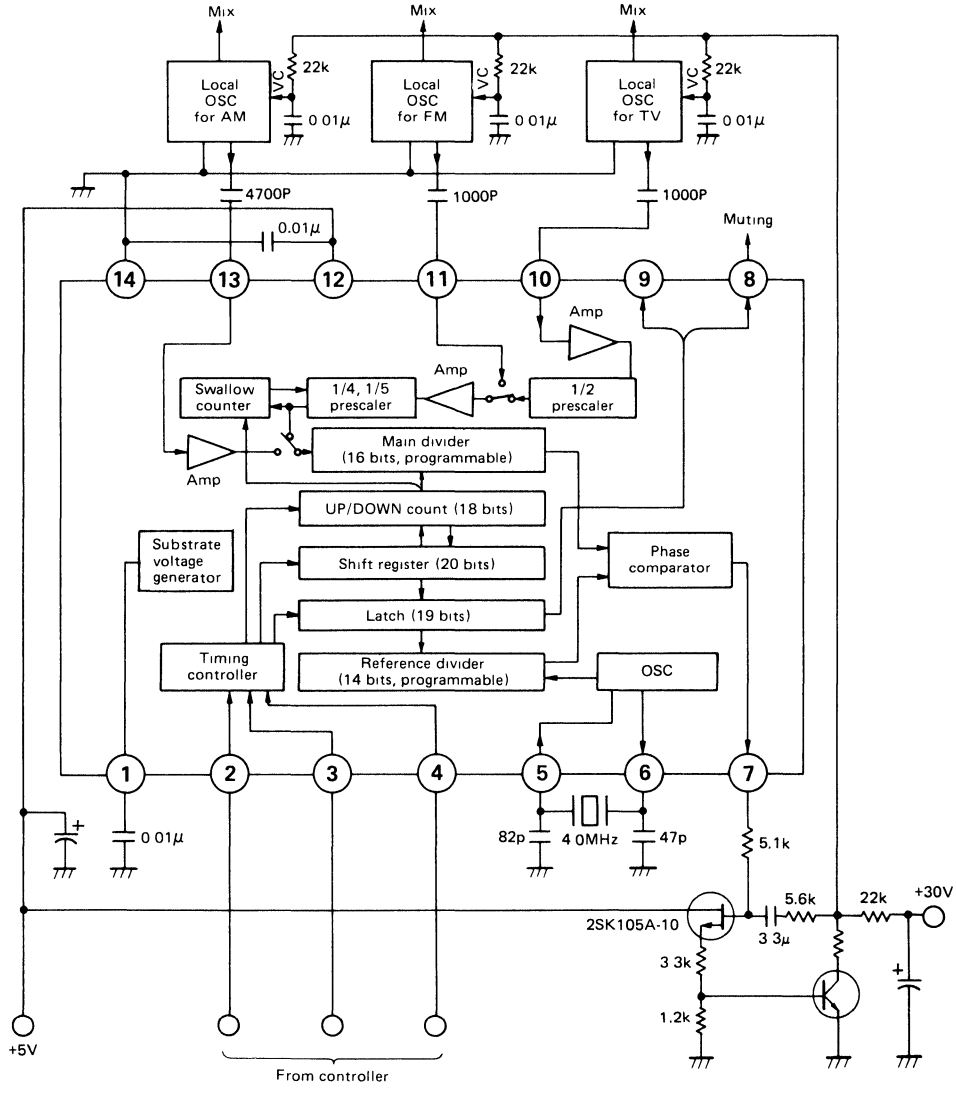


〔4-2〕 Reference signal generation by means of external clock

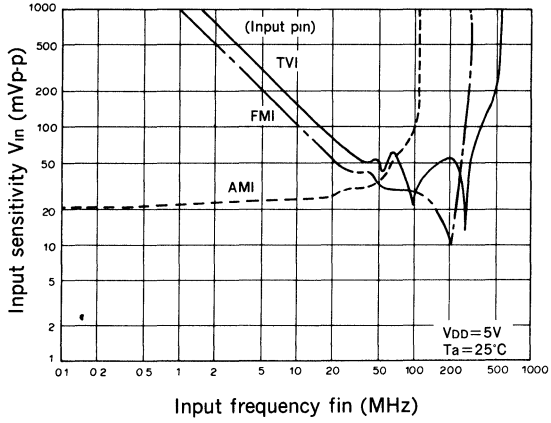
When an external clock signal, such as a clock signal obtained from the controller is to be used as reference clock, input it to X1 pin via a capacitor as shown below. The clock frequency range is guaranteed up to 13MHz. However, the usage of a signal with proper rise and fall (over 5V/μs) is recommended especially when the frequency is low. This is to prevent malfunction.



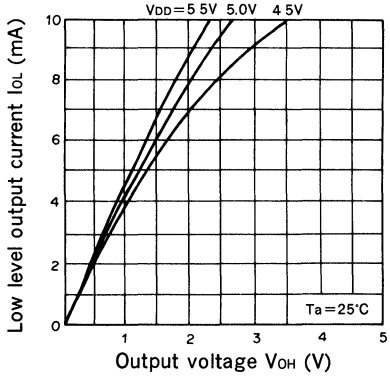
Application Circuit

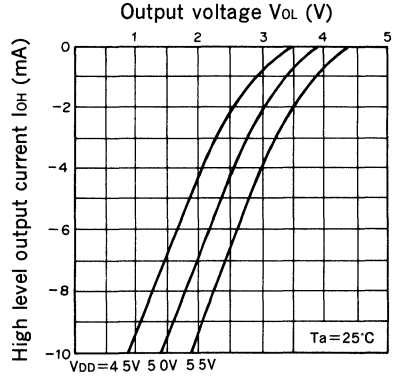


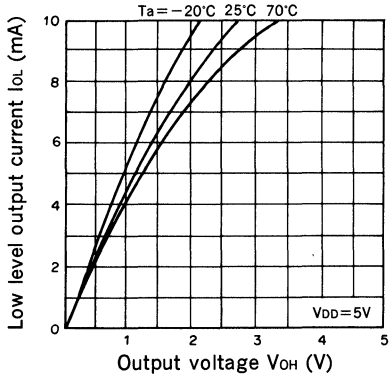
High Frequency Input Sensitivity Characteristics

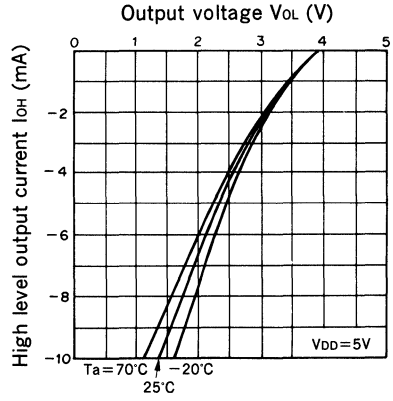


AO, BO pins Output Current Characteristics

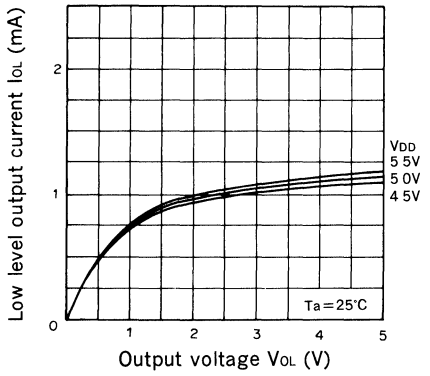


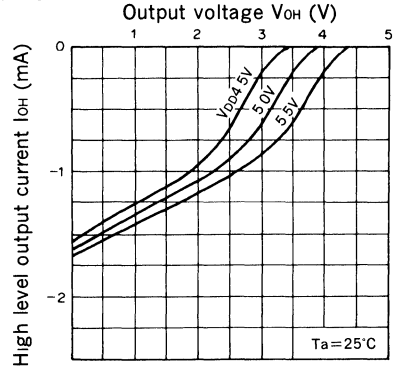


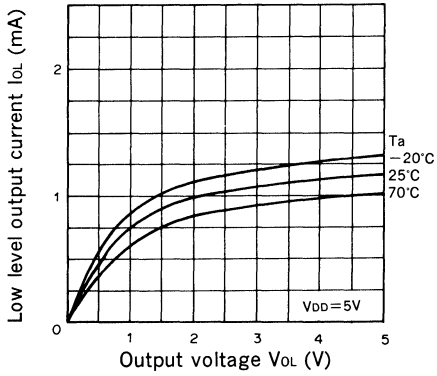


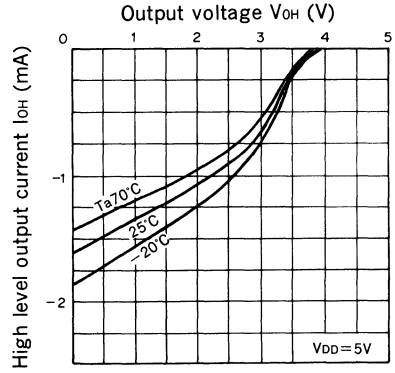


PD (Phase Comparator) pin Output Current Characteristics

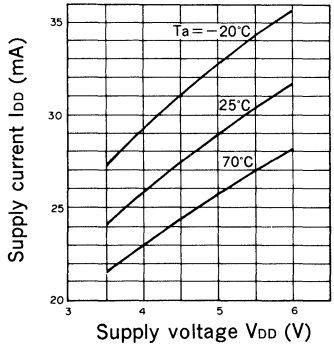








Supply Current IDD and Voltage Characteristics



SONY® CX-7961A/7961A-1

Frequency Synthesizer PLL

Description

CX-7961A is a PLL IC for the digital selection of AM, FM and TV Broadcasting as well as other radio waves, developed using the high-speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is warranted as follows:
  CX-7961A Up to 180MHz
  CX-7961A-1 Up to 240MHz
  They can be used up to 1GHz when used combined with an ECL prescaler (general-purpose).
- Programmable divider makes it possible to divide a program frequency up to 1/262,151.
- Programmable reference divider realizes selection of a given reference frequency (e.g. 244Hz – 2MHz can be selected when a 4MHz crystal oscillator is used).
- High C/N ratio with the high-speed phase comparator.
- Operation control using three terminals in serial mode.
- Independent 3 terminals (AM1, FM1 and TV1) are provided for a high frequency signal input depending on its frequency band.
- Multi-purpose output terminals are provided (AO, BO).
- Low power consumption (standard: 35m W).

Structure

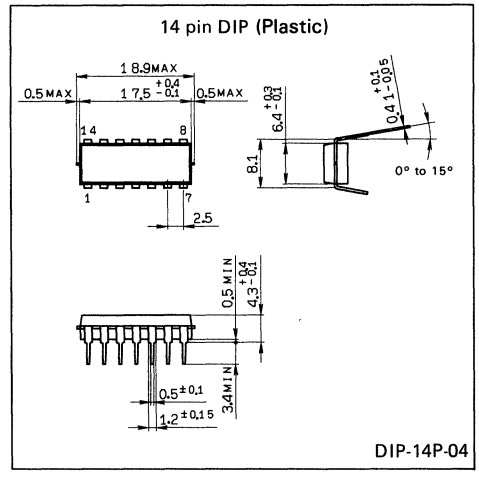
N-channel silicon gate MOS IC

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Terminal input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Package Outline

Unit: mm

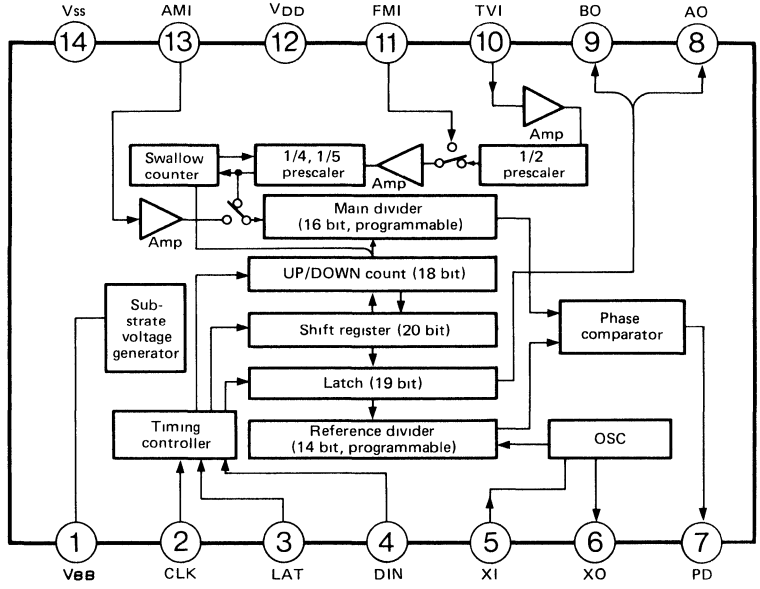


Recommended Operating Conditions

Item	Pin, remark	Symbol	Operating range	Unit
Power supply voltage		V_{DD}	+2.7 to +3.3	V
High level input voltage	CLK, DIN	V_{IH}	+1.5 to V_{DD} +0.5	V
Low level input voltage	LAT	V_{IL}	−0.5 to +0.5	V
High frequency signal input amplitude	TVI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	VMI	e_{IN}	0.2 to 2 5	Vp-p
High frequency input amplitude	AMI	e_{IN}	0.2 to 1.5	Vp-p
High frequency input amplitude	XI	e_{IN}	0.6 to 2.5	Vp-p
Operating temperature		Topr	−20 to +70	°C

50291A-HP

Block Diagram and Pin Configuration



Pin Description

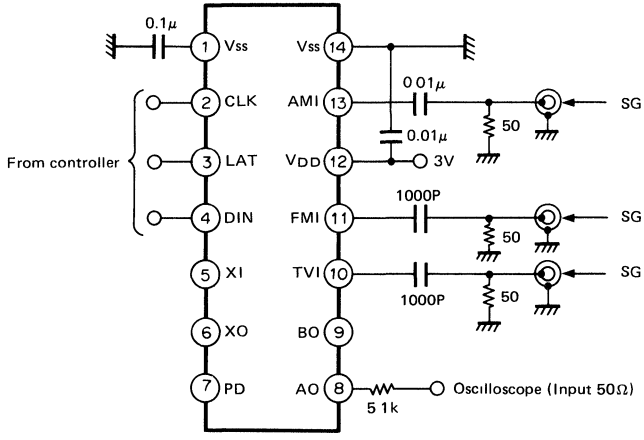
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0 01μF capacitor to the ground)
2	CLK	Clock input terminal for 20-bit serial data input (to be shifted with signal rise)
3	LAT	Latch signal input terminal for shift register input data (to be latched with signal rise) as well as the UP/DOWN clock input terminal (its state to be changed with signal rise)
4	DIN	Data input terminal as well as the UP/DOWN mode switching terminal (UP at "H" level, DOWN at "L" level)
5	XI	Crystal oscillator connection terminal for the reference signal generation (7 2MHz max , 4 0MHz standard)
6	XO	
7	PD	Phase comparator output terminal (three states)
8	AO	External control signal output terminal/unlock output terminal (E/E MOS push-pull)
9	BO	External control signal output terminal/data check terminal (E/E MOS push-pull)
10	TVI	High frequency signal input terminal (180MHz or 240MHz max) 1/2 prescaler is built-in
11	FMI	High frequency signal input terminal (90MHz or 125MHz max)
12	V_{DD}	Power supply (+3V)
13	AMI	High frequency signal input terminal (20MHz or 25MHz max)
14	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Pin, remark	Symbol	Condition	CX-7961A			CX-7961A-1			Unit
				Min.	Typ	Max.	Min.	Typ	Max.	
Operating power supply current	V_{DD}	I_{DD}	f_{IN} = 110MHz Note 2		10	18		13	18	mA
Operating input frequency	TVI	fop	e_{IN} = 0.2~2.5Vp-p	10		180	10		240	MHz
	FMI	fop	e_{IN} = 0.2~2.5Vp-p	10		90	10		125	MHz
	AMI	fop	e_{IN} = 0.2~1.5Vp-p	0.05		20	0.05		25	MHz
Input leak current	Logic input	I_{IL}	V_{IH} = 0~V_{DD} Note 1	-10		+10	-10		+10	μA
High level output current	Phase comparator (3-value output) PD	I_{OH}	V_{OUT} = 1.5V Note 2			-0.1			-0.1	mA
Low level output current		I_{OL}	V_{OUT} = 0.5V Note 2	+0.1			+0.1			mA
High impedance leak current		I_{HZ}	V_{OUT} = 1.0V Note 1	-50		+50	-50		+50	nA
High level output voltage	Push-pull by E/E MOS Structure AO, BO	V_{OH}	I_{OH} = -20μA	1.5			1.5			V
Low level output voltage		V_{OL}	I_{OL} = 0.6mA			0.4			0.4	V

Note 1 Ta = 25°C Note 2 V_{DD} = 5V Ta = 25°C

Operating Input Frequency Measuring Circuit



Control input data to CX-7961A/7961A-1 T1-H, T2-H, A-L, B-H

SG HP's 8640B (Input level is directly read with the built-in level meter)

Operating Description

(1) Signal input from the local oscillator

CX-7961A is provided with 3 independent input terminals corresponding to the signal frequency and applications.

- AMI terminal

  Reception terminal of AM broadcast with the warranted signal input up to 20MHz or 25MHz. The frequency division ratio using this terminal is 1/2 to 1/65537.

- FMI terminal

  Reception terminal of FM and TV broadcasts with the warranted signal input up to 90MHz or 125MHz. An external prescaler is not required in reception of FM channels. When TV is received, entire TV band width can be covered with combination of an external prescaler up to 1/8. The frequency division ratio ranges from 1/12 to 1/262.151. This terminal is open when it is not in use.

- TVI terminal

  This terminal is dedicated to reception of TV broadcasts. Signal input up to 180MHz or 240MHz are warranted with the built-in 1/2 prescaler. When combined with an external prescaler up to 1/4, entire TV bandwidth can be covered. The frequency division ranges from 1/24 to 1/524 302. When this terminal is not in use, it is grounded internally via a resistor of more than 100 kilo-ohms.

(2) Phase comparator

The phase comparator output (PD terminal) has a 3-value level. When the input signal is advanced in phase than the reference signal, the terminal becomes HIGH level, LOW level when the phase is lagging behind and high impedance when they are in phase

(3) Control signal and control system

CX-7961A is designed as a controller compatible with general 4-bit or 8-bit microcomputers. Three control input terminals, CLK, LAT and DIN, are available. Two control output terminals, AO and BO are also available. By combining these terminals properly, simplification of the system or multi-functional system can be realized.

(3-1) Control signal input modes

CX-7961A has three control signal input modes. DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its signal input system

(a) DATA INPUT mode (normal mode)

To set all initial values of CX-7961A it is required to input total 40-bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rise of clock input to the CLK terminal After transmitting 20-bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW Varying of the DIN and CLK terminals with the LAT terminal HIGH may affect the data internally)

As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20-bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.

Then, input the 20-bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20-bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)

When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the UP/DOWN content can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

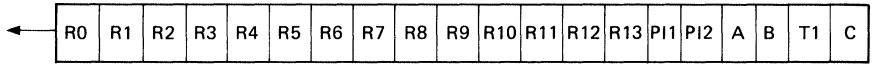
This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bit of the data is respectively at HIGH or LOW only. T1 and T2 bits will be described in the following item.

(3-2) Control data assignment

The CX-7961A control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.



- R0 – R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input terminal.

Input / PI1, PI2	AMI	FMI	TVI
PI1	–	L	H
PI2	L	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching an external prescaler's frequency division ratio, the filter constant and channel band, etc. When the prescaler M54465P (Mitsubishi) is used, the selection code of frequency division ratio will be as follows:

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

AO terminal H: UNLOCK
L LOCK

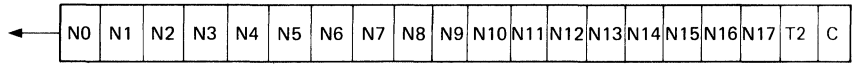
This can be used as a muting signal.
The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH

• C This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.



• N0 – N17: Programmable divider frequency division number.
(Binary value with N0 as the LSB.) Actual frequency division number will be as follows depending on a terminal selected for the signal input.

Control data		Input terminal	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 – 65,535	N + 2	2 – 65,537
L	H	AMI	4 – 262,143	N + 8	12 – 262,151
H	H	TVI	4 – 262,143	2 · (N + 8)	24 – 524,302

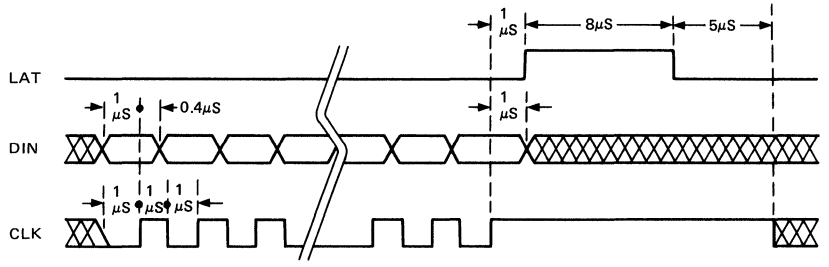
• T2: T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

• C: As described before. Set to HIGH in this case.

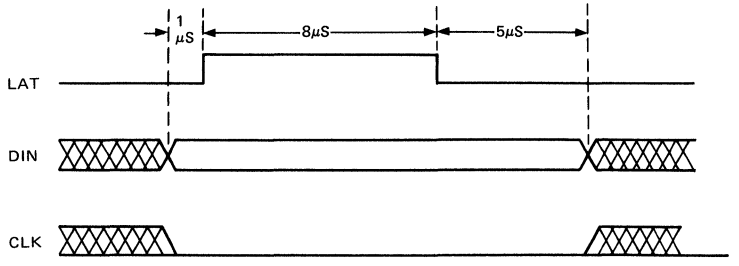
(3-3) Data input and control signal times

(a) Data input mode (normal mode)

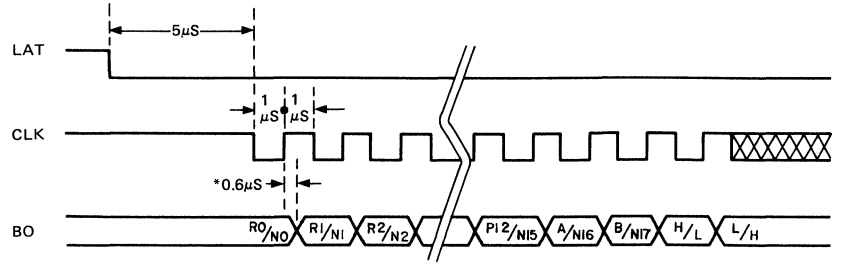
Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



(* denotes data is output within this timing.)

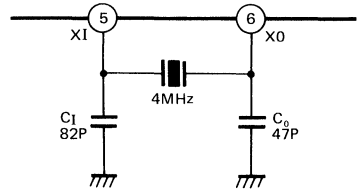
(4) Reference signal (Input signal of the reference divider)

CX-7961A can generate a reference signal by connecting a crystal oscillator to XI and XO. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

(4-1) Reference signal generator with the built-in oscillator

As shown below, connect a crystal oscillator to the XI and XO. A crystal oscillator with the frequency of 1MHz – 7.2MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used.
Be sure to make the capacitance ratio of C_I and C_O at 1 – 1 : 1 and their serial capacitance values be the specified load capacitance of the crystal oscillator.

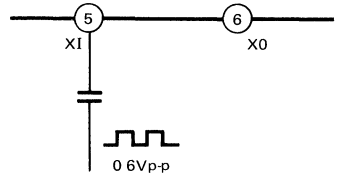
CX-7961A



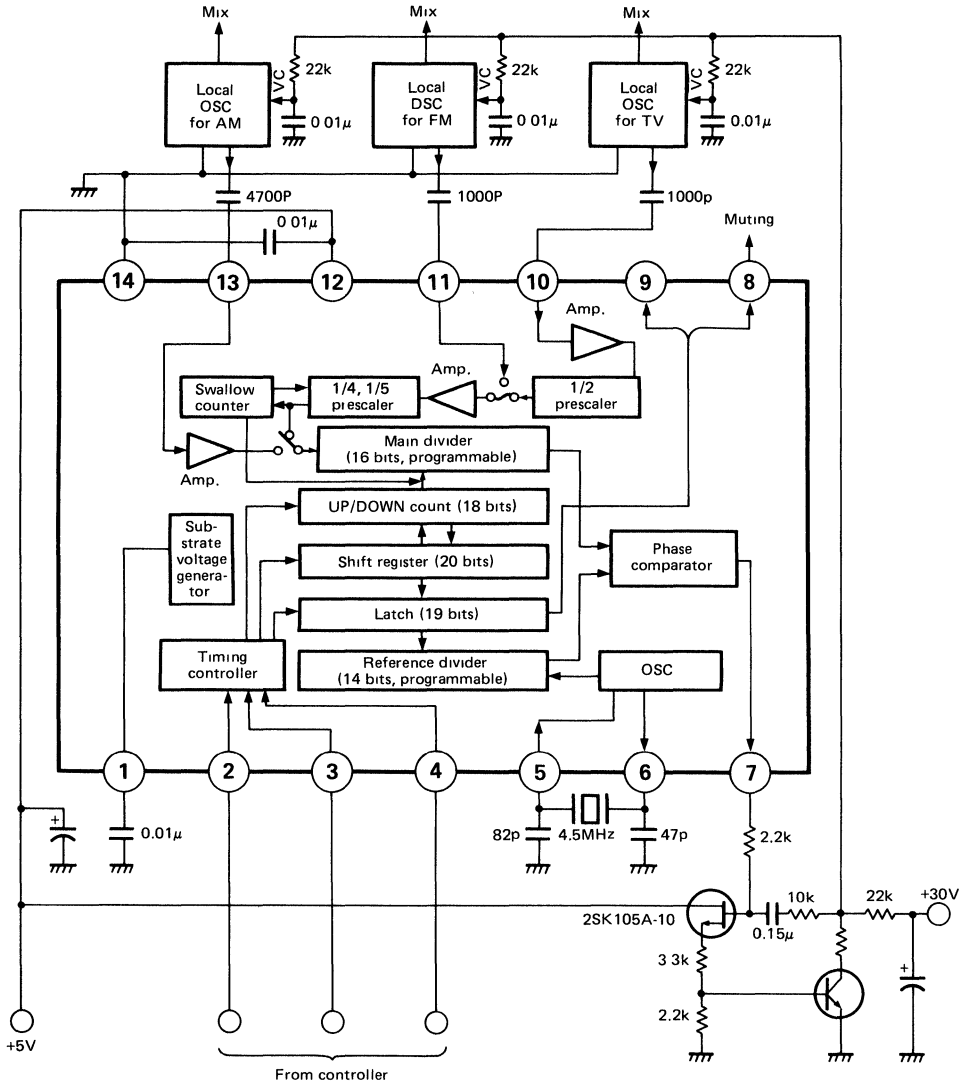
(4-2) Reference signal generator with an external clock

When an external clock signal, e g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 7.2MHz but use signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from mulfunction.

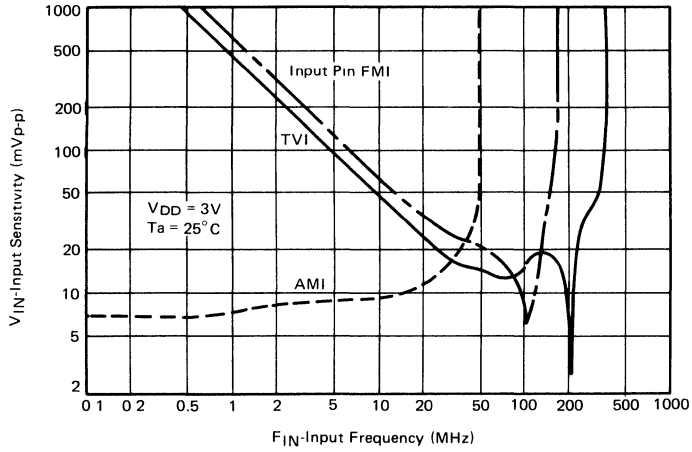
CX-7961A

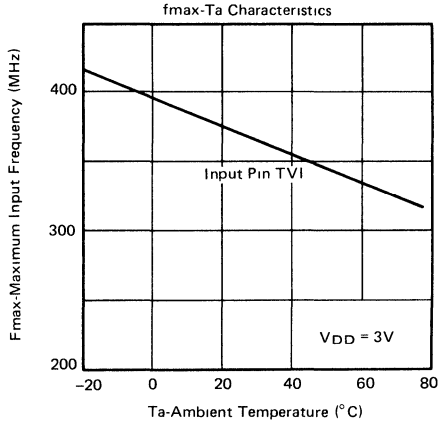


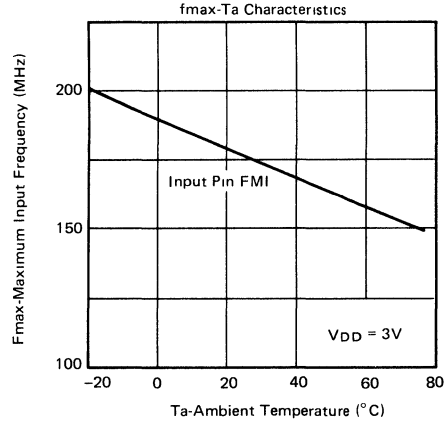
Application Circuit



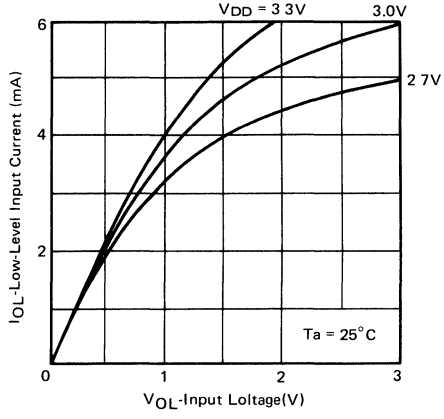
Characteristics of high-frequency input sensitivity

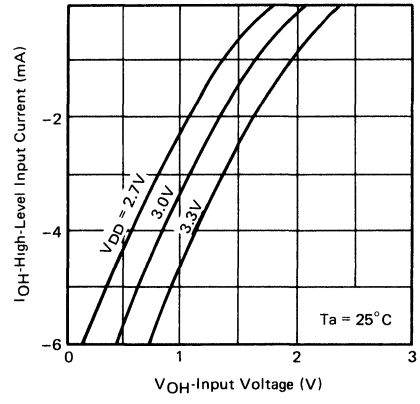




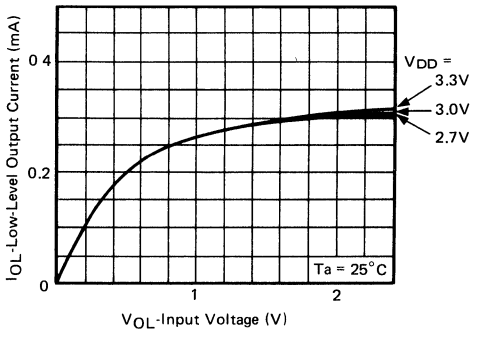


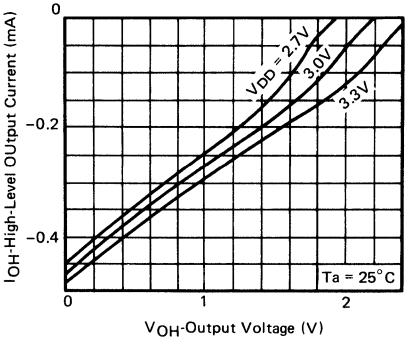
Output current characteristics of AO and BO terminals

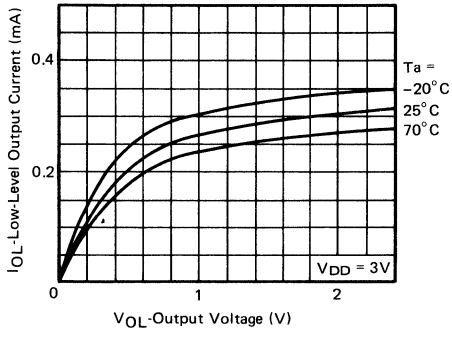


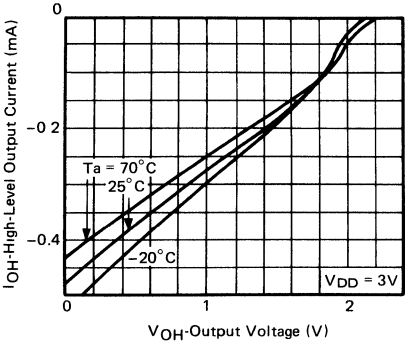


Output current characteristics of PD (Phase discriminator) terminal

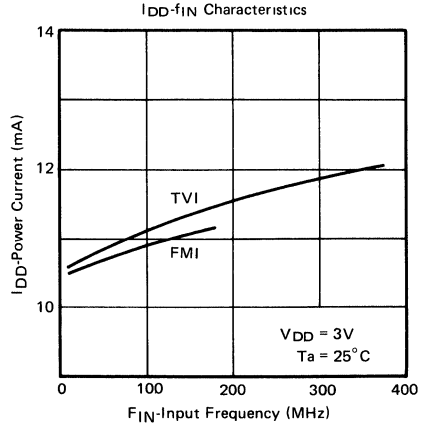


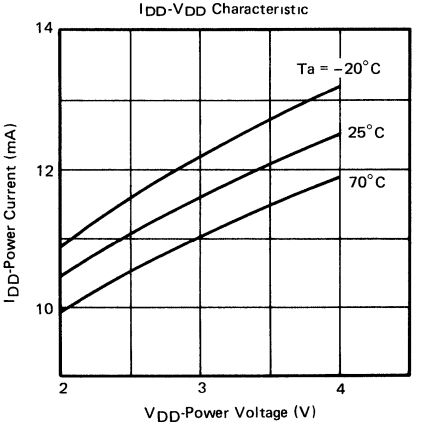






Power current characteristics





Frequency Synthesizer

Description

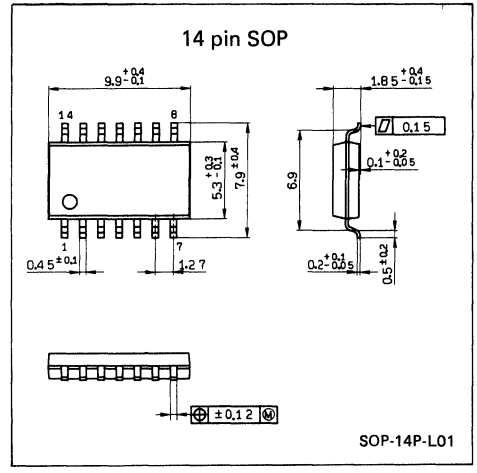
This PLL IC was developed through High-speed N-Channel silicon gate MOS technology.
CXD1118M is not only used for AM, FM and TV Broadcasting but also for the digital tuning of various radio waves.

Features

- The guranteed maximum operation frequency:
  CXD1118M 180 MHz
  CXD1118M-1 240 MHz
  1 GHz when used combined with an ECL prescaler (general purpose).
- Programmable main divider: 1/262,151 frequency. (Max.)
- Programmable reference divider: Enables at will selection of a given reference frequency. (e.g. 244 Hz to 2 MHz with the use of a 4 MHz crystal oscillator)
- High C/N ratio is realized through the high-speed phase comparator.
- Operation is controlled by three pins in serial mode.
- High frequency signal inputs are handled by 3 independent pins AMI, FMI and TVI, depending on the frequency band.
- Multipurpose output pins (AO and BO).
- Low power consumption 35W (Typ.)

Package Outline

Unit: mm



Structure

N-Channel silicon gate MOS

Absolute Maximum Ratings (Ta = 25°C, VSS = 0V)

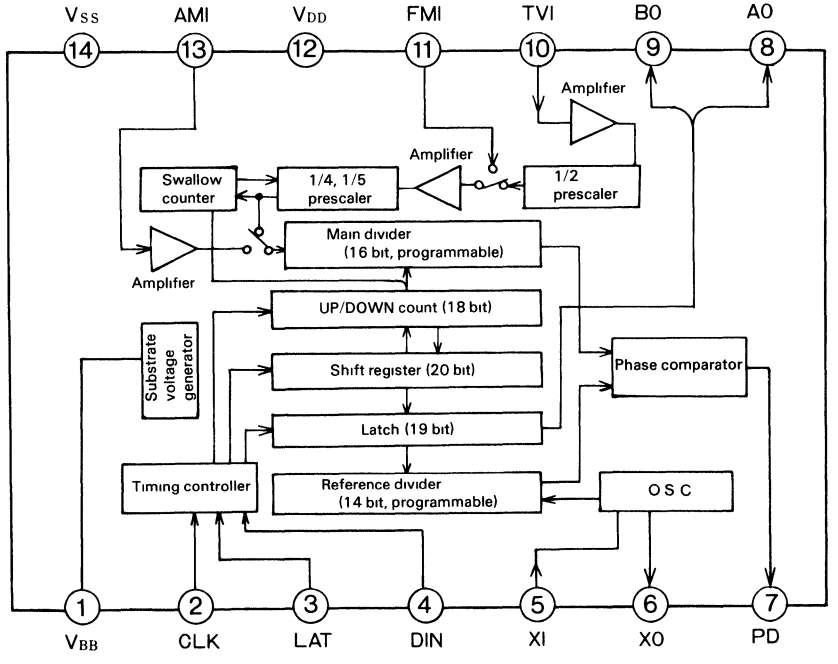
• Supply voltage	VDD	−0.5 to +7	V
• Input pin voltage	VIN	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

61134-TO

Recommended Operating Conditions

Item	Pin	Symbol	Operating range	Unit
Supply voltage		V_{DD}	2.7 to 3.3	V
High level input voltage	CLK, DIN	V_{IH}	1.5 to V_{DD} +0.5	V
Low level input voltage	LAT	V_{IL}	−0.5 to +0.5	V
High frequency signal input amplitude	TVI	e_{IN}	0 2 to 2.5	Vp-p
High frequency signal input amplitude	FMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	AMI	e_{IN}	0.2 to 1.5	Vp-p
High frequency signal input amplitude	XI	e_{IN}	0.6 to 2 5	Vp-p
Operating temperature		Topr	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

No	Symbol	Description
1	V_{BB}	Substrate pin (connect 0.01 μF capacitor to the ground).
2	CLK	Clock input pin for 20-bit serial data input (to be shifted with signal rise.)
3	LAT	Latch signal input pin for shift register input data (to be latched with signal rise) Also, UP/DOWN clock input pin (condition changes with signal rise)
4	DIN	Data input pin. Also, UP/DOWN mode switching pin (Up at "H" level and DOWN at "L" level)
5	XI	Crystal oscillator connection pin for reference signal.
6	XO	Generation (7.2 MHz Max, 4.0 MHz Typ.)
7	PD	Phase comparator output pin (three-state).
8	AO	External control signal output pin/unlock output pin (E/E MOS push-pull)
9	BO	External control signal output pin/data check pin (E/E MOS push-pull)
10	TVI	High frequency signal input pin (180 MHz or 240 MHz Max.) Built-in 1/2 prescaler
11	FMI	High frequency signal input pin (90 MHz or 125 MHz Max.)
12	V_{DD}	Power supply (+3V).
13	AMI	High frequency signal input pin (20 MHz or 25 MHz Max.)
14	V_{SS}	Ground pin

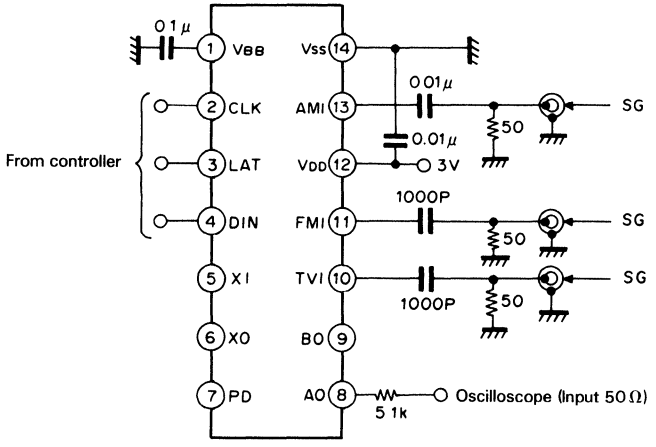
Electrical Characteristics

(Within the range of Recommended operating conditions, unless otherwise specified) VSS = 0V

Item	Pin·Remarks	Symbol	Condition	CXD1118M			CXD1118M-1			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating supply current	VDD	IDD	fIN=110 MHz *2		10	18		13	18	mA
Operating input frequency	TVI	fOP	eIN=0 2 to 2 5 Vp-p	10		180	10		240	MHz
	FMI	fOP	eIN=0 2 to 2 5 Vp-p	10		90	10		125	MHz
	AMI	fOP	eIN=0 2 to 1 5 Vp-p	0 05		20	0 05		25	MHz
Input leak current	Logic input	IIL	VIH=0 to VDD *1	−10		10	−10		10	μA
High level output current	Phase comparator (3-value output) PD	IOH	VOUT=1 5V *2			−0 1			−0 1	mA
Low level output current		IOL	VOUT=0 5V *2	0 1			0 1			mA
High impedance leak current		IHZ	VOUT=1 0V *1	−50		50	−50		50	nA
High level output voltage	Push-pull by E/E MOS Structure AO, AB	VOH	IOH=−20μA	1 5			1 5			V
Low level output voltage		VOL	IOL=0 6mA			0 4			0 4	V

Note)*1 Ta = 25°C
*2 VDD = 3V Ta = 25°C

Operating Input Frequency Test Circuit



Control input data to CXD1118M. T1-H, T2-H, A-L, B-H
SG: HP's 8640B (Input level read directly at 8640B's level meter)

Description of Operation

1. Signal input from the local oscillator

1) CXD1118M is provided with 3 independent input pins to handle corresponding signal frequencies and applications.

- **AMI pin**

  It is mainly used for the reception of AM broadcasts to guarantee signal inputs of 20 MHz or 25 MHz.

  The frequency division ratio when using this pin is 1/2 to 1/65537.

- **FMI pin**

  This is mainly used for the reception of FM broadcasts to guarantee signal inputs of 90 MHz or 125 MHz.

  For FM reception while no external prescaler is required, all bands can be covered. The frequency division ratio ranges from 1/12 to 1/262,151. Also, when not in use, this pin remains open.

- **TVI pin**

  Mainly used for TV and FM broadcast reception, this pin features a built-in 1/2 prescaler. This is to ensure signal inputs up to 180 MHz or 240 MHz Also, in combination with a 1/4 external prescaler, the entire TV bandwidth can be covered. The frequency division ratio ranges from 1/24 to 1/524,302. When this pin is not in use, it is grounded internally via a resistor of over 100 kΩ.

2. Phase comparator output

The phase comparator output (PD pin) has a 3-value level. When the input signal is more advanced in phase than the reference signal the pin turns to HIGH level when it is lagging behind in phase it turns to LOW, and when they are in phase it is set to High Impedance.

3. Control signal and control system

The CXD1118M design makes it compatible with general 4 or 8-bit microcomputers. It has three control input pins: CLK, LAT and DIN. Proper usage of these and the other two available control output pins, AO and BO can accomplish system simplification or multi-functionalization.

1) Control signal input modes

CXD1118M features three control signal input modes with respectively different signal input systems: DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode.

(1) DATA INPUT mode (normal mode)

To set all the initial values of CXD1118M, it is necessary to input a total of 40-bit data in this mode, 20 bits at a time. When data is input to Din pin, with LAT pin set to LOW, the data is input one bit at a time to the shift register with the rise of the clock input to the CLK pin.

After transmitting 20-bit data to the shift register, the data is latched by setting LAT pin to HIGH, while CLK is in HIGH state. (After the data latching, set LAT pin back to LOW. Note that while LAT pin is at HIGH, any changes occurring to DIN and CLK pins may internally affect the data.

As will be referred to in details later on, input data is taken in either the programmable or the reference divider, whichever, depending on the state of the last bit C.

For all practical purposes, first of all input through the controller the 20-bit data that includes: the reference divider frequency division number, the input pin selection and the AO/BO output pin data, accoring to the above mentioned input method. For this, set the last bit C of the Data to LOW. Next, input the 20-bit data, including the programmable divide; setting data, the same way. For this, the last bit C of the data is set to HIGH. Then, all internal states are set. After this setting, to effect a change on only the value of the programmable divider, a change executed on only the latter 20-bit data, will suffice. (For that purpose also, C is set to HIGH). To change the value of the programmable divider (program selection channel, AFT) by using the following UP/DOWN mode higher effectiveness can be attained.

(2) UP/DOWN mode

After setting CLK pin to LOW, LAT pin (usually at LOW level) is changed to HIGH. Changing LAT pin level from HIGH to LOW enduces DIN pin HIGH/LOW level changes. According, UP/DOWN counter content increases or decreases by one. By repeating the process the setting value of the programmable divider can be altered as required.

(3) DATA CHECK mode

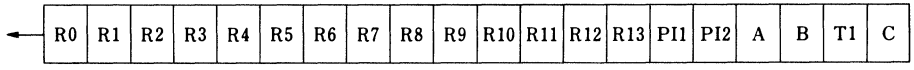
This mode is used to check if the data is correctly input from the controller to the shift register. The data left in the shift register, immediately after the input data has been latched, is output, one bit at a time, from BO pin. This happens with the rising edge of CLK pin, to which a clock is input after LAT pin is set to LOW while CLK pin is held at HIGH level. However the shift register data can only be output from BO pin when the T1 and T2 bits of the data are respectively at HIGH and LOW. T1 and T2 are described in the following paragraph.

2) Consist of control data

The CXD1118M control data is assigned in 20 bits, of which the last two are the data recognition code. Recognizing this code gives access to the data content. Moreover, although unrelated to the user, this code is used for the switch to TEST mode. As mentioned hereafter, the frequency division number of each of the programmable divider and the reference divider, is given in the binary value with the leading digit of LSB.

(1) Control input data of the reference divider and others. (C =LOW)

This can be considered as the initial setting data. It has to be input when feeding power supply or switching channel bands. The input data is assigned as follows:



- R0 — R13: Reference divider frequency division number (binary value with the LSB of R0).
  There is an affect component between the input data and the actual frequency division number. The relationship is as follows:
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input pin.

Input / PI1, PI2	AMI	FMI	TVI
PI1	—	L	H
PI2	L	H	H

- A, B, T1: A0 and B0 pins have 2 types of functions. The switching occurs according to T1 value. When T1 is at LOW A and B values are output, as they are, to A0 and B0 pin. These signals can be used for a variety of purposes, such as switching the external prescaler's frequency division ratio, the filter constant, the channel bands and others. When the M54465P prescaler (MITSUBISHI), essentially for TV reception is used, the selection code of the frequency division ratio becomes as follows.

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T is at High, the AO output pin outputs the LOCK/UNLOCK state of the phase comparator.

AO pin H: UNLOCK
L. LOCK

Accordingly, it can be used as a muting signal. As described in article (3-1) 3) for the Data Check Mode, BO pin becomes the data output pin of the shift register. By inputting the lock to CLK pin, the shift register content is continuously output. Note that when T1 is at High, AO and BO pins cannot be used for external control.

• C This is a code to determine the latch direction of the input data. In this case, set to LOW

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(2) Programmable divider input data (C = HIGH)
This data determines the programmable divider's frequency ratio.

← N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C

• N0 – N17. Programmable divider frequency division number (Binary value with N0 as the LSB)
The actual frequency division number taken as the input signal differs accroding to the selected pin as follows:

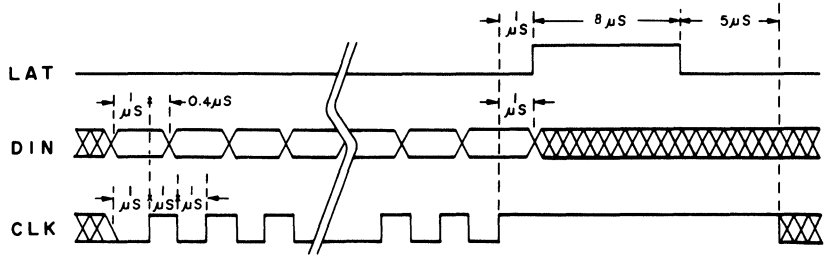
Control data		Input pin	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 to 65,535	N+2	2 to 65,537
L	H	AMI	4 to 262,143	N+8	12 to 262,151
H	H	TVI	4 to 262,143	2·(N+8)	24 to 524,302

• T2: T2 is used for the selection of test mode. Users should usually keep this data to LOW. To check the frequency division and reference outputs, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. Then the reference output and the frequency division output will be displayed at the AO and BO pins, respectively.

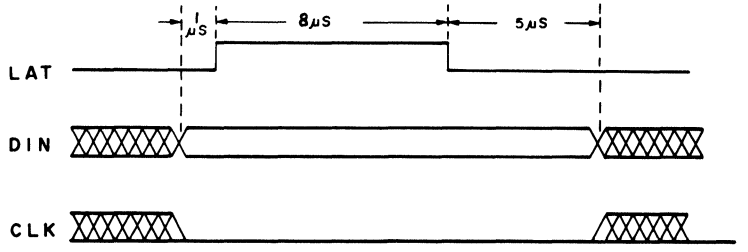
• C: As previously mentioned. Set to HIGH in this case.

3) Data input and control signal timing
(1) Data input mode (normal mode)

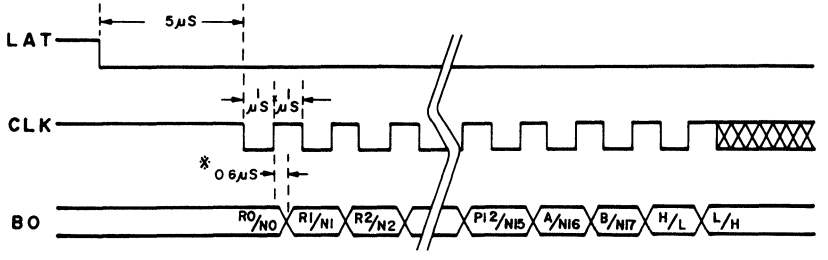
Each timing indicates the minimum value, unless otherwise specified.



(2) UP/DOWN mode



(3) DATA CHECK MODE (DATA check of the shift register)



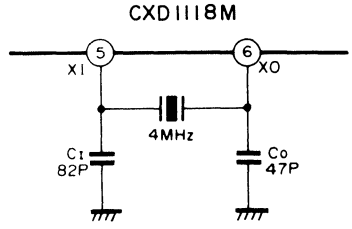
(* Indicates data is output within this timing)

4. Reference signal (Input signal of the reference divider)

CXD1118M can generate a reference signal by connecting a crystal oscillator to XI and XO. By inputting an external clock signal to XI pin, the external clock can be used as a reference signal.

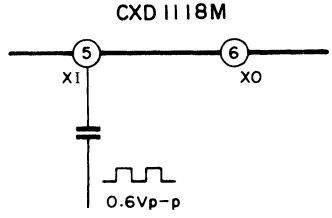
1) Reference signal generation through built in oscillator

As shown in figure below, connect a crystal oscillator to XI and XO pins. A crystal oscillator with a frequency of 1 MHz to 7.2 MHz can be used. The figure below shows an example where a standard 4 MHz oscillator is used. Set the capacitance ratio of CI and CO at 1 to 2.1 CI and CO serial capacitance values should be the specified load capacitance of the crystal oscillator.

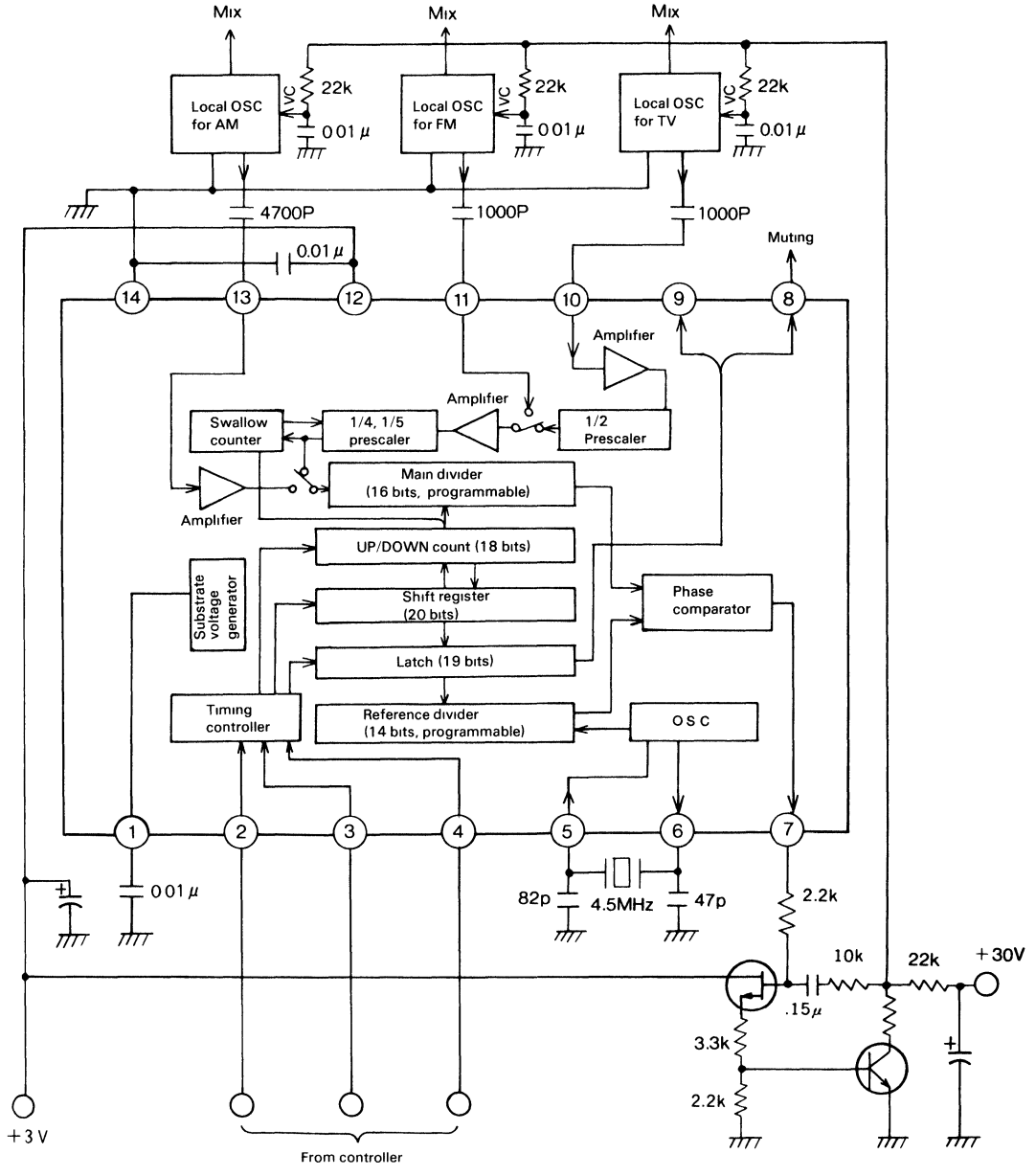


2) Reference signal generation through an external clock

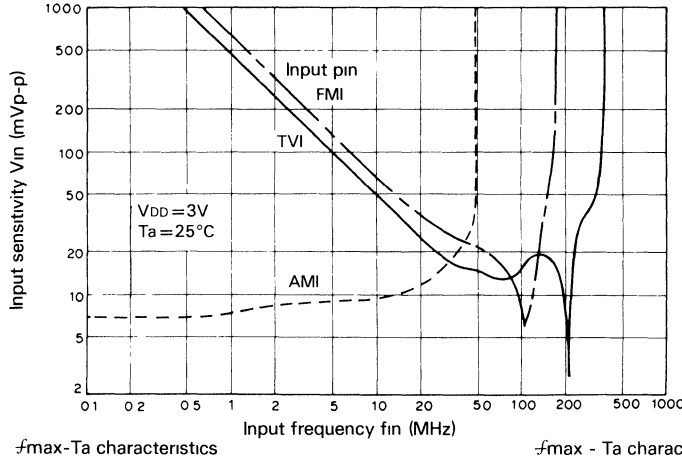
When an external clock signal, such as for instance, a clock signal obtained from the controller is used as the reference clock, connect to XI pin via a capacitor, as shown in figure below. The clock frequency range is guranteed up to 7.2 MHz. However, when the frequency is especially low, use a signal of proper rise and decay. (more than 5V/μs). This is to deter malfunction.

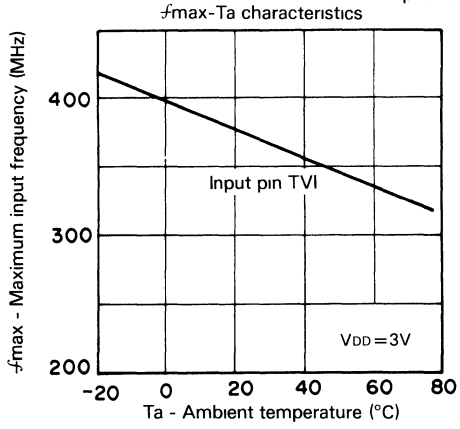


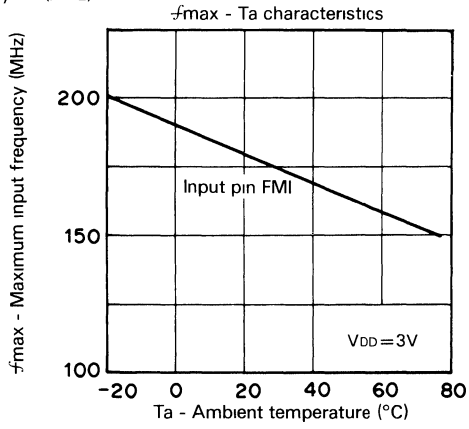
Application Circuit



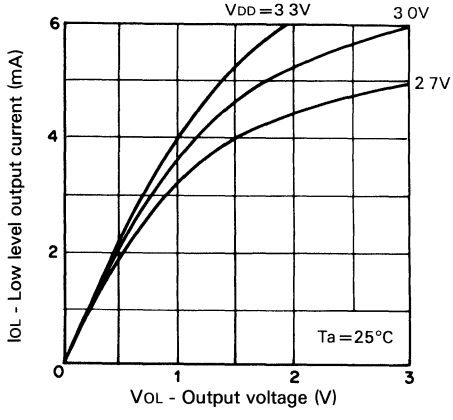
High frequency input sensitivity characteristics

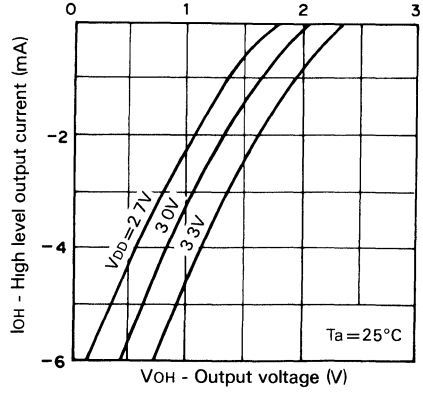




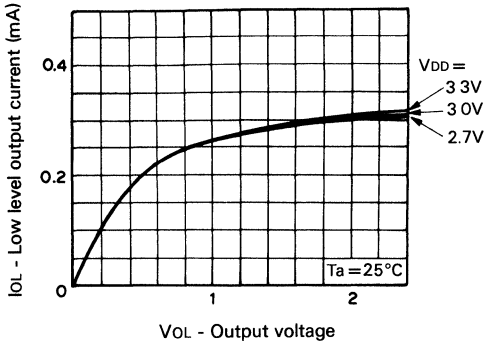


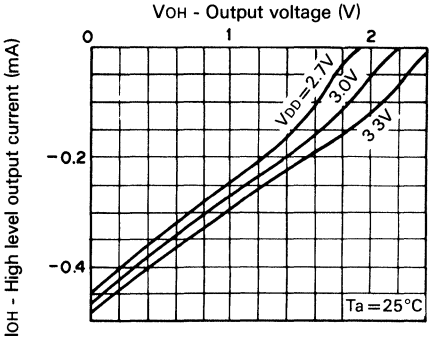
Output current characteristics of AO and BO pins

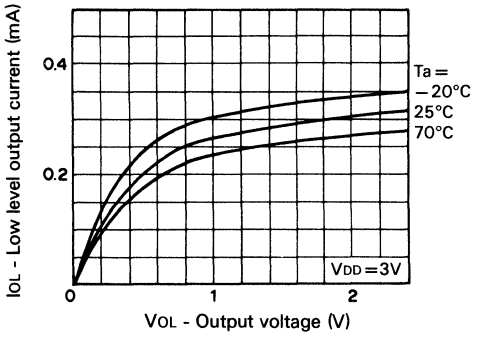


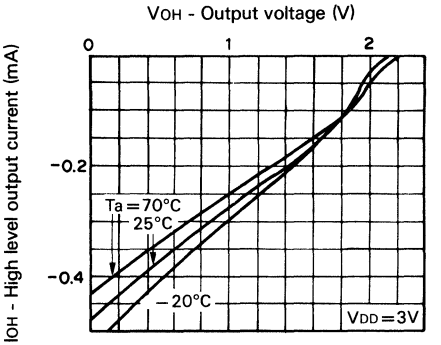


PD (Phase discriminator) pin output current characteristics

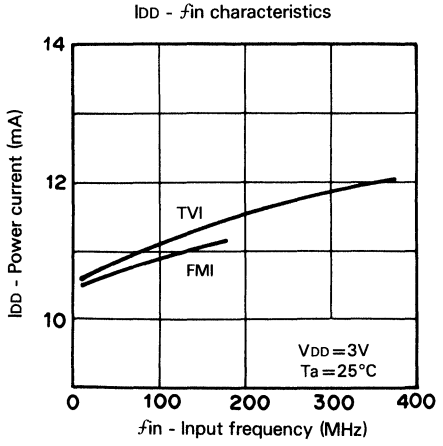


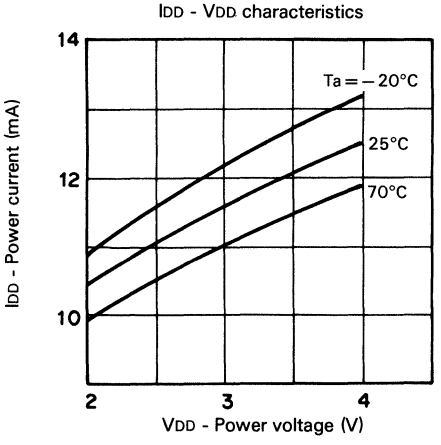






Power current characteristics





SONY

CXA1356M/N

1GHz Band PLL IC for Mobile Communications

Preliminary

Description

The CXA1356M/N are frequency synthesizer PLL ICs which have developed for 1GHz mobile communication systems. These ICs have low current consumption, small package and are appropriate for portable sets of cellular units, etc.

CXA1356M	CXA1356N
16 pin SOP (Plastic)	16 pin VSOP (Plastic)

Features

- Low current consumption Icc=13.5mA (Vcc=5.0V)
- Maximum operating frequency 1.8GHz (typ.)
- High input sensitivity
- Ultra small 16-pin VSOP package

Applications

1GHz mobile communication equipment for cellular, etc.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	300	mW

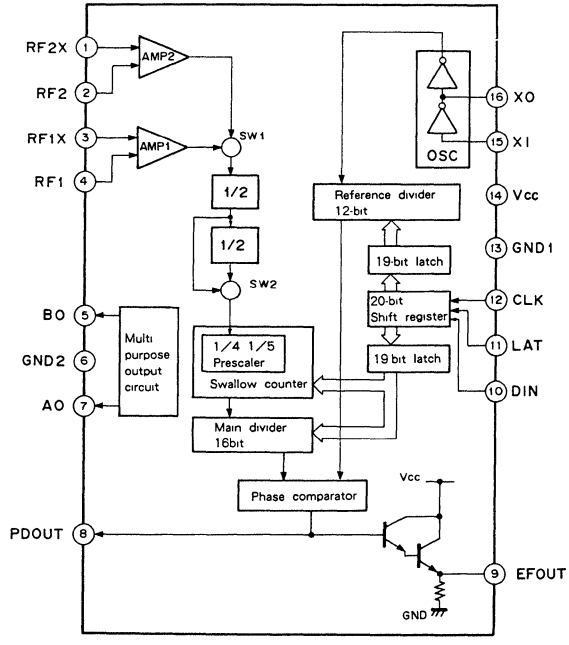
Structure

Bipolar silicon monolithic IC

Operating Conditions

• Supply voltage	Vcc	4.5 to 5.5	V
• Operating temperature	Topr	−35 to +85	°C

Block Diagram and Pin Configuration



PE90628 – ST

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption		Icc			13.5		mA
Maximum operating frequency		fMAX			1800		MHz
DIN CLK LAT	"H" input voltage	VIH			3		V
	"L" input voltage	VIL			2		V
	"H" input current	IIH			0.1		μA
	"L" input current	IIL			–0.1		μA
PD OUT	"H" output current	IOH	VPDOUT=2.5V		–240		μA
	"L" output current	IOL	VPDOUT=2.5V		240		μA

Description of Operation

Control Signal and Control System

The CXA1356M/N is designed to work with a controller which consists of general 4-bit/8-bit microprocessor. It has 3 pins of CLK, LAT and DIN as the control data input pins. As the output pins for control, two pins of AO and BO are also available. A simple, multi-function system can be implemented by taking advantage of these pins.

[1] Control Signal Input Process

The signal input process is comprised of two different data modes, DATA READ mode (normal mode) and DATA CHECK mode.

(a) DATA READ mode (normal mode)

To completely initialize this IC two 20 bit data streams, for a total of 40 bits of data, must be input in this mode. First, make the LAT pin in the LOW state and input data at the DIN pin in synchronization with the clock. The data is read into the shift register one bit at a time with each clock pulse.

After 20 bits of data have been stored in the shift register, the data is latched by making the LAT pin HIGH while holding the CLK pin HIGH. (After the data is latched return the LAT pin to LOW. If the CLK or DIN pins change while the LAT pin is HIGH the stored data may change. So take care.)

As explained in detail below, the data is input into the main divider or reference divider according to the value of C bit. In order to actually use this IC, at first input the 20 bits of input data which represent the reference divider division number, input pin selection, and AO and BO output pin data from the controller by the above sequence. At this time, the last C bit data should be LOW.

Next, set up the main divider data using the same method with 20 bits of input data. At this time, make C bit high. After this the IC is completely initialized. If only the main divider division number need to be changed, by repeating the latter sequence (C bit; HIGH), a new set of data can be stored.

(b) DATA CHECK mode

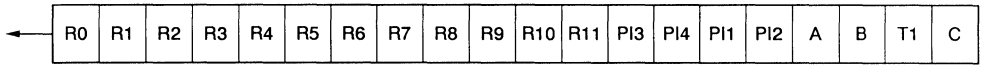
This mode is provided to verify the correctness of data which is input into the shift register by the controller. Immediately after input data is latched and the LAT pin is returned LOW (remembering to keep CLK HIGH), the data can be output to pin BO one bit at a time with each clock pulse. At that time, the T1 and T2 bits must be held HIGH and LOW respectively in order to output the shift register data to pin BO. T1 and T2 bits are explained in the "Control Data Structure" section.

[2] Control Data Structure

Control data for the CXA1356M/N is constructed a 20-bit data stream. The last two bits represent the function code which recognizes the purpose of the data stream. Selecting the TEST mode is also provided for using this code. As explained later, the first bit of two data stream is the LSB of a binary value of the main divider or reference divider division number.

(a) Control input data for reference divider (C=LOW)

As this data is called initialization data, whenever the power is turned on this input sequence is mandatory. The data format is assigned below.



←	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	PI3	PI4	PI1	PI2	A	B	T1	C

- R0 to R11 : Reference divider divisor. (Binary value with R0 as LSB).
  In practice, there is an offset component between the actual division number and the input data. Their relationship is as follows.
  (Actual divider division number) = (Input data) +2

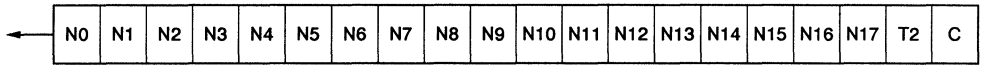
- PI1 to PI4 : Input signal pin selection.

PI1	PI2	PI3	PI4	
L	H	L	L	RF1 input
H	H	L	L	RF2 input

- A, B, T1 : Each of the AO and BO pins has two functions which are switched depending on the T1 value. When T1 is LOW, A and B are output to the AO and BO pins respectively.
  When T1 is HIGH, the AO pin outputs the LOCK/UNLOCK state signal of the phase comparator.
  AO pin: H : LOCK
  L : UNLOCK
  The BO pin outputs the shift register contents in the DATA CHECK mode in synchronization with the clock pulse. See [1] (b)

- C : This is a code to determine the latch direction of the input data. Input LOW for this mode.

(b) Control input data for main divider (C=HIGH)
Sets up main divider division number data.



• N0 to N17 : Main divider division number (Binary value with N0 as LSB). Main divider has a 1/4 fixed divider circuit at the input, and the actual divisor is shown in the following relationship (PI3=PI4=LOW) :

Range of Division Input Data N	Relation Between N and True Division Number	Range of True Division Number
4 to 262,143	ND=4 • (N+8)	48 to 1,048,604

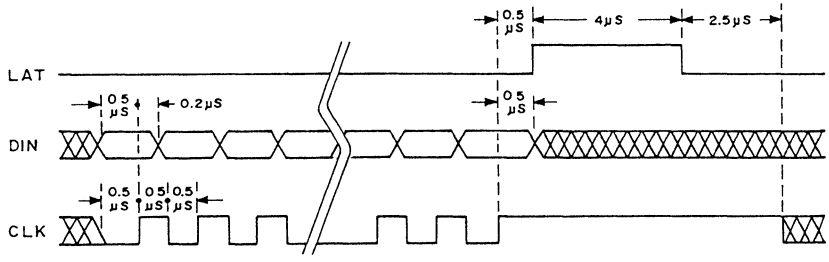
• T2 : Used to select test mode. Normal user should input a LOW value.
When the main divider output and reference divider output must be checked, make this T2 bit and the T1 bit HIGH and input a LOW for A and B. The AO and BO output pins will output the reference divider output and main divider output respectively.

• C : As described before. Input HIGH for this mode.

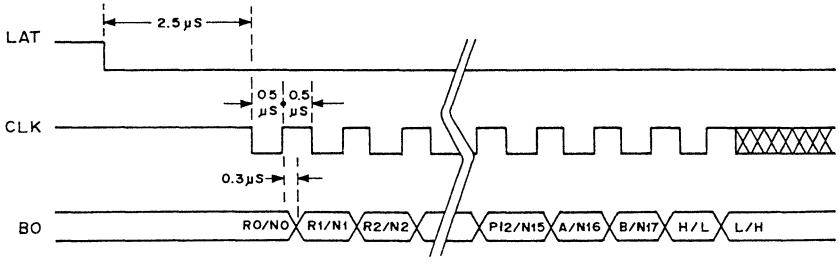
Input data				AO output	BO output
T1	T2	A	B		
L	L			A	B
H	L			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output

[3] Data Input and Control Signal Timing

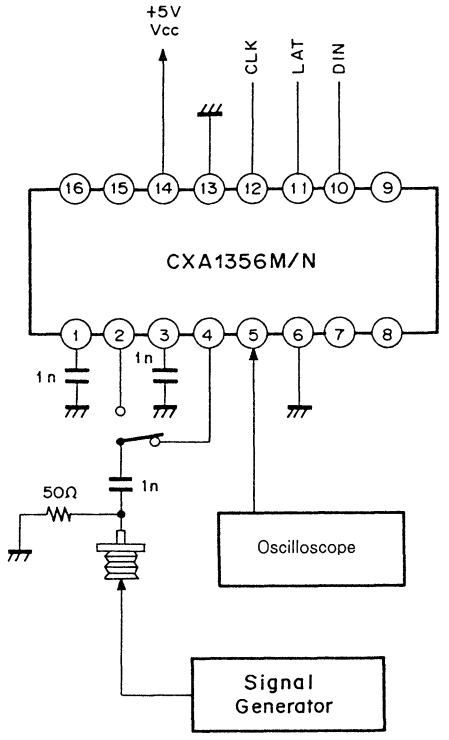
(a) DATA READ mode (normal mode)



(b) DATA CHECK mode (shift register data check)

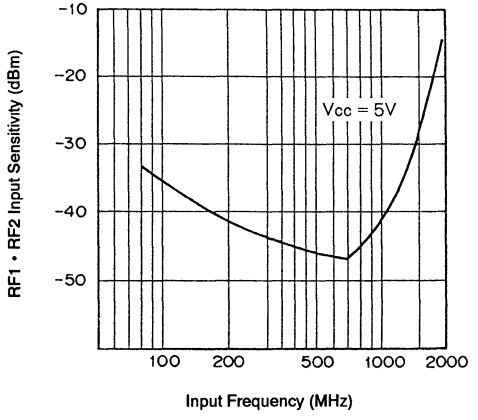


Electrical Characteristic Test Circuit
High Frequency Input Sensitivity Test Circuit

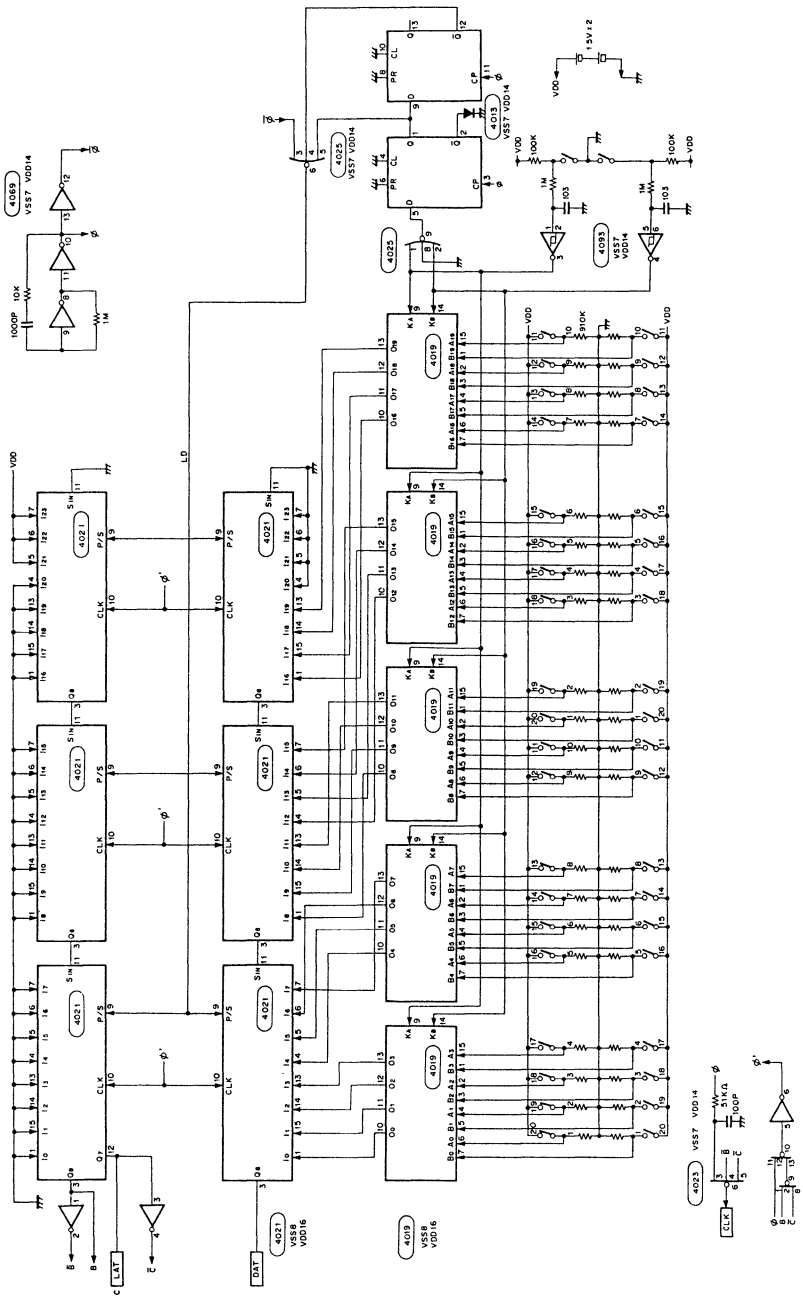


Example of Representative Characteristics

RF1 and RF2 Input Sensitivity vs. Input Frequency Characteristics



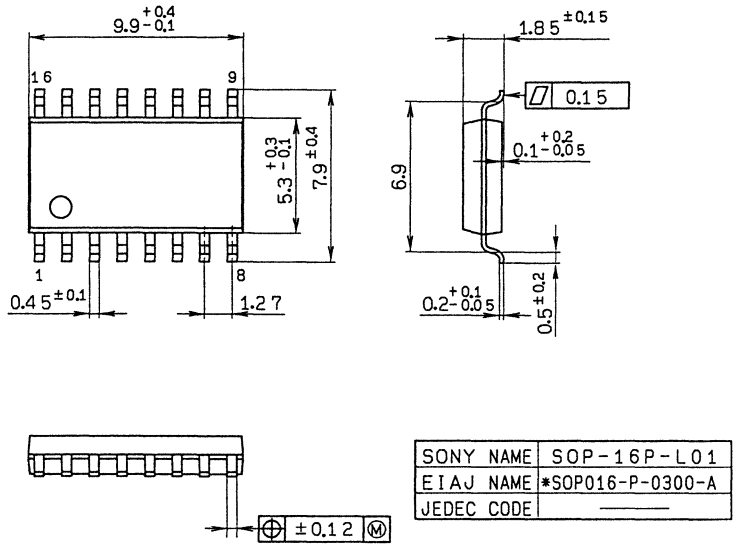
DATA, CLK, LATCH INPUT CIRCUIT



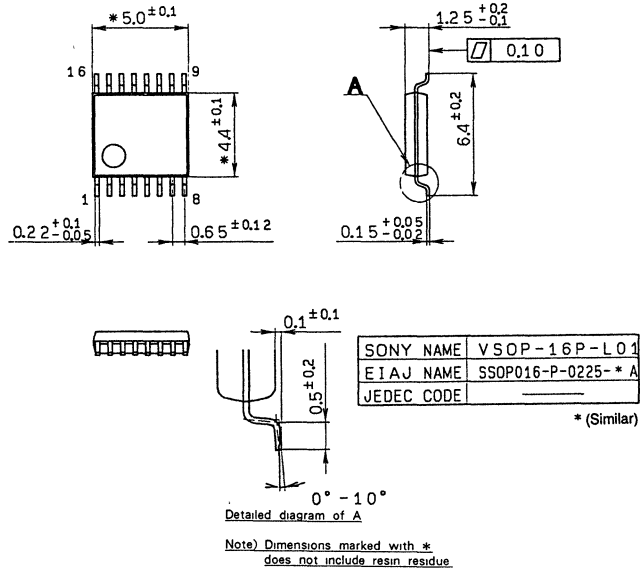
Package Outline

Unit : mm

CXA1356M 16pin SOP (Plastic) 300mil 0.2g



CXA1356N 16pin VSOP (Plastic) 225mil



Note) Dimensions marked with * does not include resin residue

SONY® CXA1541M

1.2 GHz 2 Modulus Prescaler for Cellular Equipment — Advance Information

Description

The CXA1541M is a 1.2GHz 2 modulus prescaler developed for cellular equipment use. At 3.0mA, current compensation is minimal while pin compatibility with MB501L/SL permits easy replacement.

Features

- Ultra low current consumption (3.0mA at V_{CC}=5.0V)
- Pin compatible with MB501
- Achieves high input sensitivity
- Maximum operating frequency of 1.2GHz is guaranteed.
- 64/65 and 128/129 frequency divisions can be selected.

Applications

1GHz band radio communications and cellular equipment

Operating Conditions

- Supply voltage V_{CC} 4.5 to 5.5 V
- Operating temperature T_{opr} −34 to +85 °C

8pin SOP (Plastic)

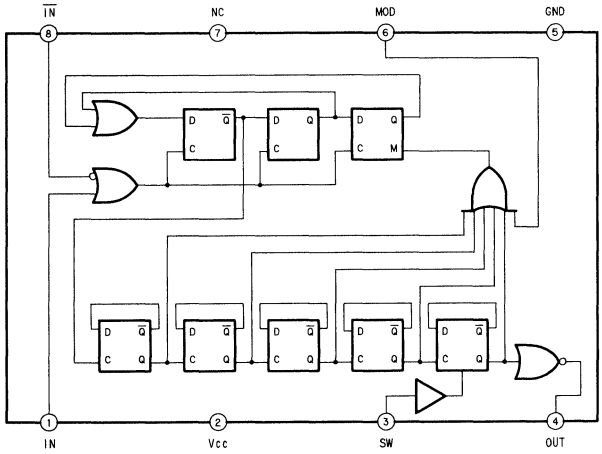
Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

- Supply voltage V_{CC} 7.0 V
- Storage temperature T_{stg} −65 to +150 °C
- Allowable power dissipation P_D 400 mV

Block Diagram and Pin Configuration

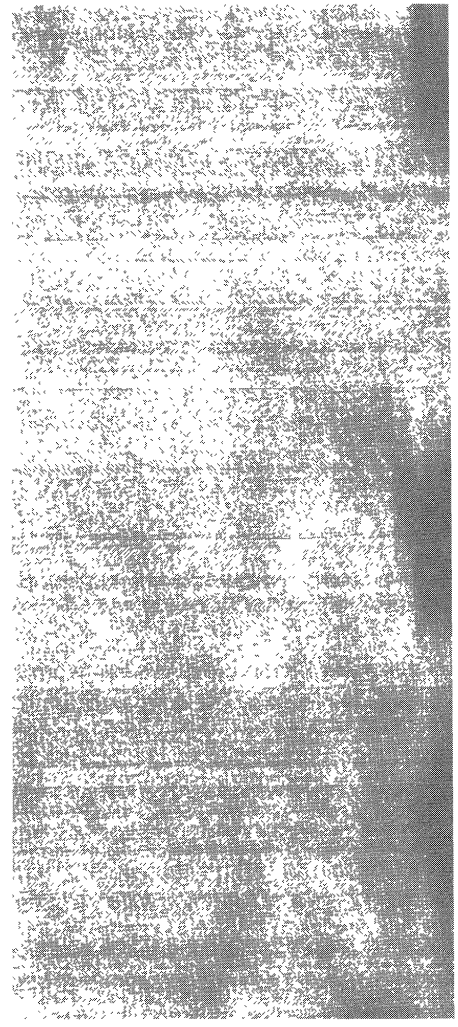


No.	Pin Function
1	Input
2	V_{CC}
3	64/128 frequency division ration select input
4	Output
5	GND
6	Swallow select input
7	NC
8	Reference input

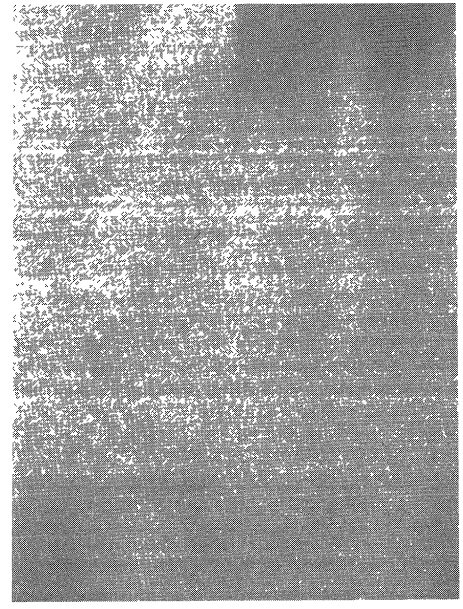
Function Table

64/128	MOD	Frequency division ratio
H	H	64
H	L	65
L	H	128
L	L	129

AE90185-HP



GaAs MES FET



4) GaAs MES FET

Type	Function	Page
3SK165	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	223
3SK166	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	227
SGM2004M	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	231
SGM2006M/P	RF amplifier, mixer, oscillator, GaAs dual gate MES FET	235

SONY

3SK165

GaAs N-Channel Dual-Gate MES FET

Description

The 3SK165 is a GaAs N-channel Dual-Gate MES FET for low noise UHF amplifiers and mixers. Low noise and high gain characteristics are accomplished by optimum mask pattern design. Easier high frequency circuits adjustments are made possible by the miniaturized plastic molded package which contributes to reduce parasitic elements of the device.

Features

- Low NF — NF = 1.2 dB (Typ.) at 800MHz
- High PG — PG = 20 dB (Typ.) at 800MHz
- High stability

Applications

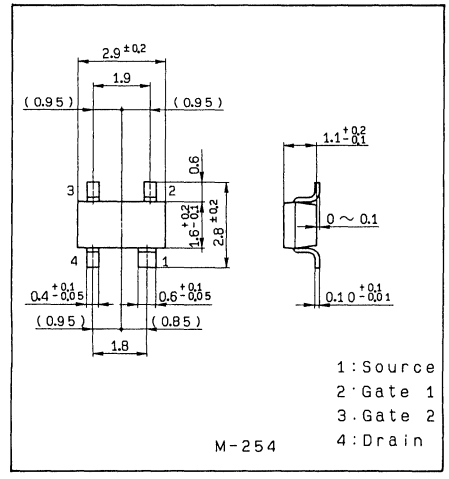
- UHF Amplifier, mixer, oscillator

Absolute Maximum Ratings (Ta = 25°C)

• Drain to source voltage	V_{DSX}	8	V
• Gate 1 to source voltage	V_{G1S}	−6	V
• Gate 2 to source voltage	V_{G2S}	−6	V
• Drain current	I_D	80	mA
• Channel temperature	Tch	150	°C
• Storage temperature	Tstg	− 55 to + 150	°C
• Allowable power dissipation	P_D	150	mW

Package Outline

Unit: mm



Electrical Characteristics

Ta = 25°C

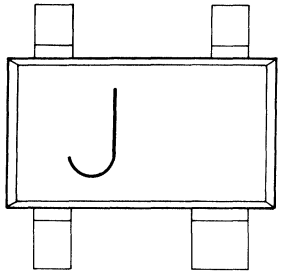
Item	Symbol	Condition	Min	Typ	Max	Unit
Drain to source voltage	V_{DSX}	I_D = 200μA, V_{G1S} = 0V, V_{G2S} = −5V	8			V
Gate 1 cutoff current	I_{G1SS}	V_{G1S} = −4V, V_{G2S} = 0V, V_{DS} = 0V			−20	μA
Gate 2 cutoff current	I_{G2SS}	V_{G2S} = −4V, V_{G1S} = 0V, V_{DS} = 0V			−20	μA
Drain saturation current*	I_{DSS}*	V_{DS} = 5V, V_{G1S} = 0V, V_{G2S} = 0V	20		55	mA
Gate 1 cutoff voltage	V_{G1S} (OFF)	V_{DS} = 5V, I_D = 100μA, V_{G2S} = 0V	−1		−4	V
Gate 2 cutoff voltage	V_{G2S} (OFF)	V_{DS} = 5V, I_D = 100μA, V_{G1S} = 0V	−1		−4	V
Forward transfer admittance	g m	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1 5V, f = 1KHz	15	22		mS
Input capacitance	Ciss	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1 5V, f = 1MHz		0 5	1 0	pF
Reverse transfer capacitance	Crss			7 5	25	fF
Power gain	PG	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1 5V, f = 800MHz	16	20		dB
Noise figure	NF			1 2	2 5	dB

* Classification

Rank	I_{DSS}	Unit
3SK165-0	20—55	mA
3SK165-1	20—35	mA
3SK165-2	30—55	mA

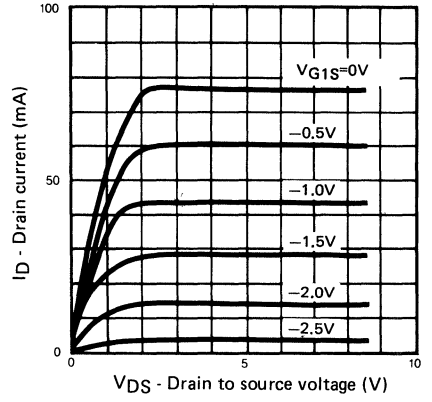
E89332-ST

Mark



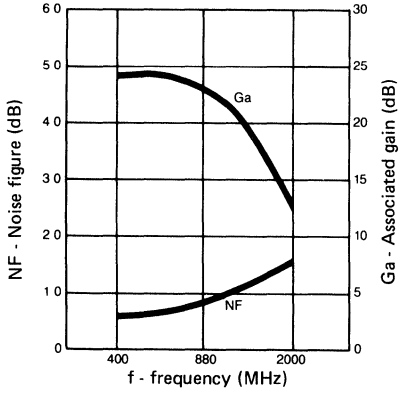
Output characteristics

(Ta=25°C, V_{G2S}=1.5V, V_{G1S}=−0.5V/step)



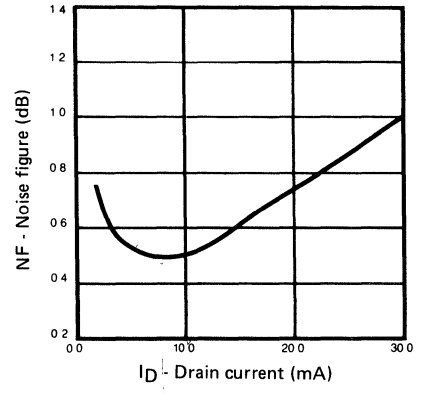
NF, Ga frequency dependence

(V_{DS}=5.0V, V_{G2S}=1.5V, I_D=10mA)

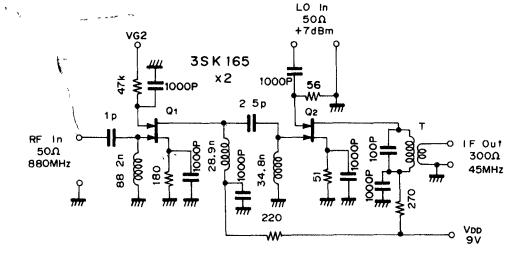


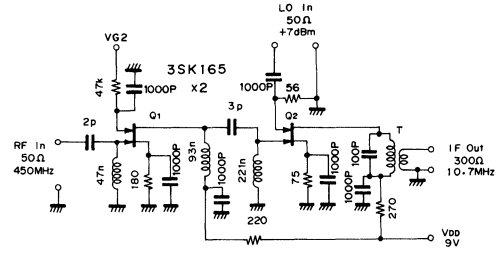
NF-I_D characteristics

(V_{DS}=5.0V, V_{G2S}=1.5V, Frequency at 450MHz)



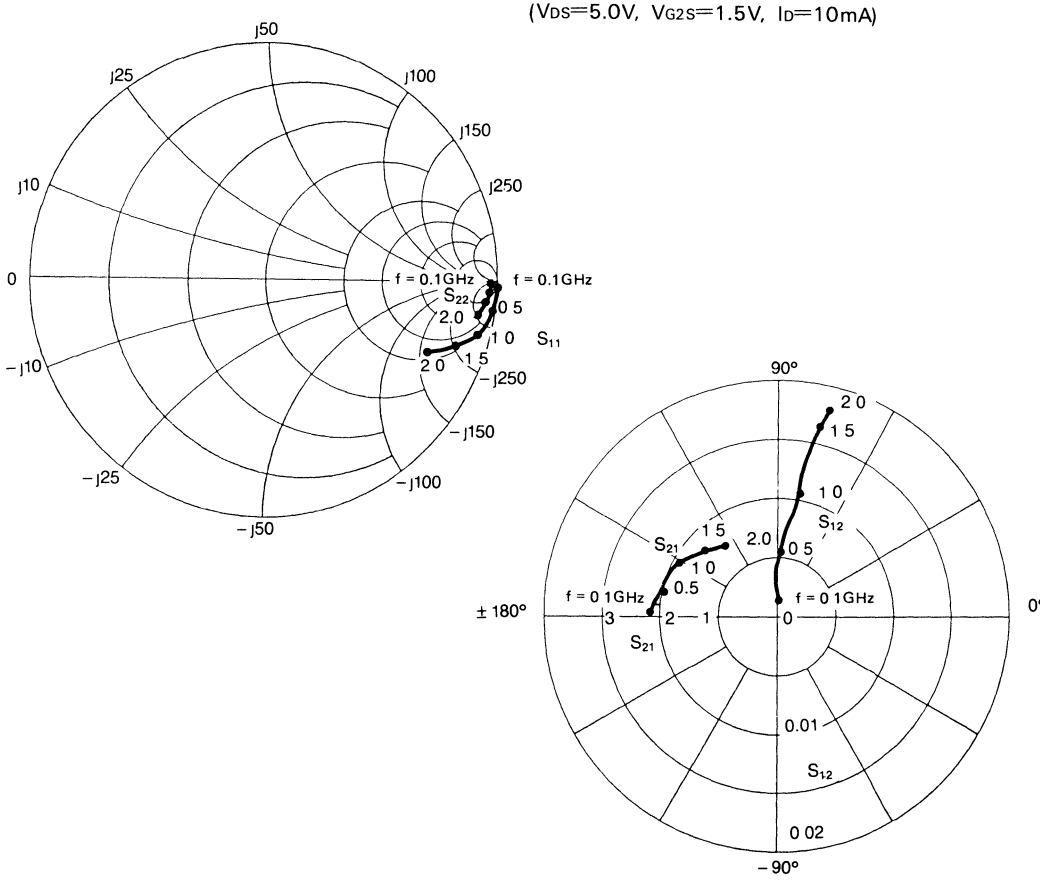
Application Circuit (Front-end amplifier)





S-Parameters vs. Frequency characteristics

(V_{DS}=5.0V, V_{G2S}=1.5V, I_D=10mA)



S-Parameter Data of FET 3SK165

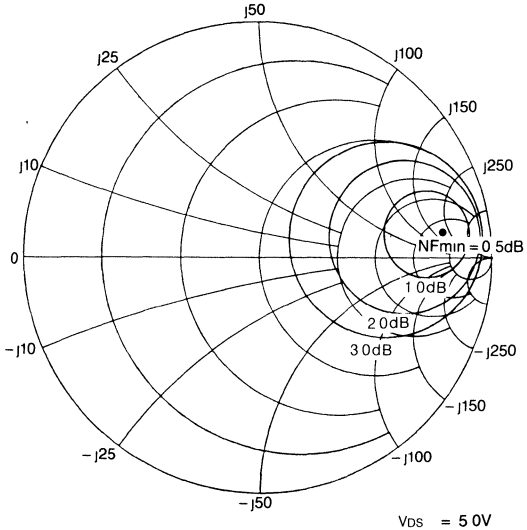
Z_O=50Ω

Frequency MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	.999	-1.60	2.065	177.40	0.0011	88.48	.961	-.77
200	.998	-2.97	2.044	172.69	0.0021	93.67	.961	-1.85
300	.999	-4.28	2.180	169.86	0.0023	105.04	.971	-2 98
400	.993	-5.70	2.077	170.12	0.0049	89.67	.958	-3.51
500	989	-6.98	1.981	167.14	0.0054	83.41	.958	-4.17
600	.979	-8.16	1.999	161.04	0.0068	83.94	.960	-5.09
700	.969	-9.57	2.004	160.63	0.0082	83.47	.955	-5.68
800	.958	-10.84	1.957	159.23	0.0084	82.97	.955	-6.83
900	.948	-12.16	1.856	153.88	0.0091	79.56	.948	-7.22
1000	.938	-13.23	1.938	150.58	0.0106	78.17	.949	-8.58
1200	.912	-15.27	1.789	147.43	0.0131	79.92	.941	-10.37
1400	.877	-17.11	1.823	139.04	0.0151	74.26	.936	-12.06
1600	.841	-19.12	1.700	137.04	0.0156	78.12	.935	-13.26
1800	.805	-21.04	1.704	132.09	0.0171	77.47	.928	-13.91
2000	.756	-22.32	1.448	126.14	0.0176	76.07	.922	-14.46

Noise figure characteristics

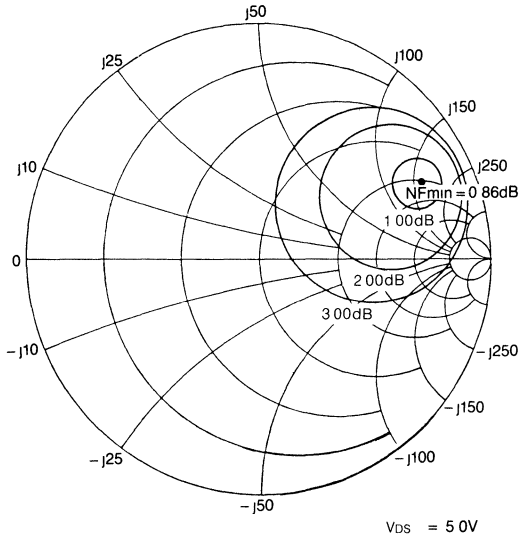
(V_{DS}=5.0V, V_{G2S}=1.5V, I_D=10mA)

at 450MHz



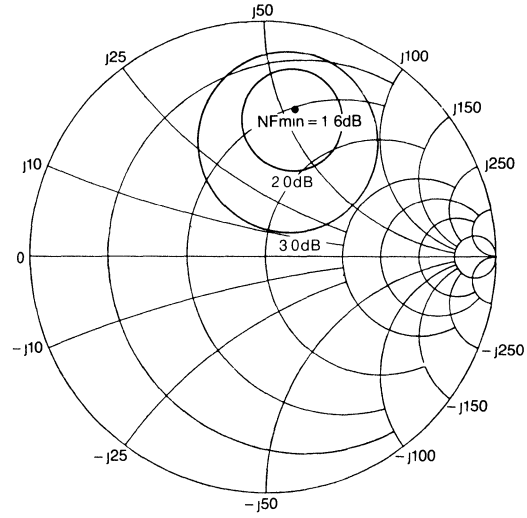
V_{DS} = 5 0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 450 MHz
NF min 0.50 dB
Ga 23.83 dB
Gamma (S); MAG 0.799 ANG 7.78°
Gamma (L); MAG 0.887 ANG 7.31°

at 880MHz



V_{DS} = 5 0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 880 MHz
NF min 0 86 dB
Ga 23 70 dB
Gamma (S); MAG 0.771, ANG 25 07°
Gamma (L); MAG 0.830, ANG 21.84°

at 2000MHz



Frequency (MHz)	Ga (dB)	NF (dB)	Gamma- S		Gamma- L	
			MAG	ANG	MAG	ANG
400	23 54	0 59	0 824	3 16°	0 910	8.75°
450	23.83	0 50	0 799	7 78°	0 887	7 31°
500	22 79	0 47	0 792	12 03°	0 848	14 56°
880	23.70	0 86	0 771	25 07°	0 830	21 84°
2000	12 92	1 60	0.643	78,48°	0.559	46 00°

V_{DS} = 5.0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 2000 MHz
NF min 1.60 dB
Ga 12.91 dB
Gamma (S); MAG 0.643, ANG 78.48°
Gamma (L); MAG 0.559, ANG 46.00°

SONY

3SK166

GaAs N-channel Dual-Gate MES FET

Description

3SK166 is a GaAs N-channel Dual-Gate MES FET for low noise UHF amplifiers. Low noise and high gain characteristics are accomplished by optimum mask pattern design. Easier high frequency circuits adjustments are made possible by the miniaturized plastic molded package which contributes to reduce parasitic elements of the device.

Features

- Low NF — NF = 1.2 dB (Typ.) at 800 MHz
- High PG — PG = 20 dB (Typ.) at 800 MHz
- High Stability

Structure

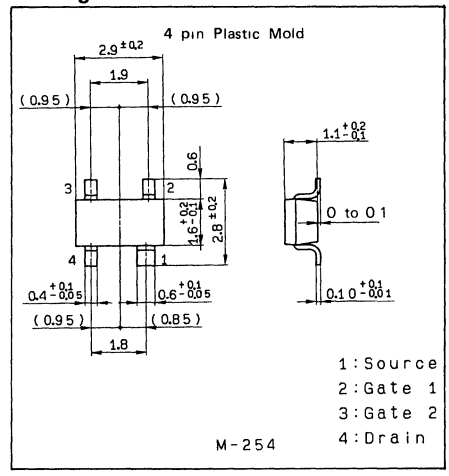
GaAs N-channel Dual-Gate MES (Metal Semiconductor) type FET.

Applications

- UHF Amplifier, oscillator.

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Drain to source voltage	V_{DSX}	8	V
• Gate 1 to source voltage	V_{G1S}	−6	V
• Gate 2 to source voltage	V_{G2S}	−6	V
• Drain current	I_D	80	mA
• Channel temperature	Tch	150	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	150	mW

Electrical Characteristics

Ta=25°C

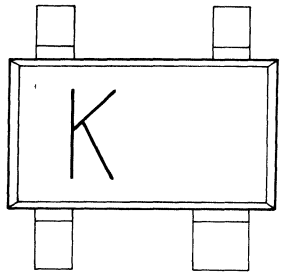
Item	Symbol	Condition	Min	Typ	Max	Unit
Drain to source voltage	V_{DSX}	I_D = 200μA, V_{G1S} = 0V, V_{G2S} = −5V	8			V
Gate 1 cutoff current	I_{G1SS}	V_{G1S} = −5V, V_{G2S} = 0V, V_{DS} = 0V			−20	μA
Gate 2 cutoff current	I_{G2SS}	V_{G2S} = −5V, V_{G1S} = 0V, V_{DS} = 0V			−20	μA
Drain saturation current	I_{DSS}*	V_{DS} = 5V, V_{G1S} = 0V, V_{G2S} = 0V	20		80	mA
Gate 1 cutoff voltage	V_{G1S} (OFF)	V_{DS} = 5V, I_D = 100μA, V_{G2S} = 0V	−1		−4	V
Gate 2 cutoff voltage	V_{G2S} (OFF)	V_{DS} = 5V, I_D = 100μA, V_{G1S} = 0V	−1		−4	V
Forward transfer admittance	g_m	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1.5V, f = 1KHz	25	40		mS
Input capacitance	C_{iss}	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1.5V, f = 1MHz		13	20	pF
Reverse transfer capacitance	C_{rss}			25	40	fF
Power gain	PG	V_{DS} = 5V, I_D = 10mA, V_{G2S} = 1.5V, f = 800MHz	18	20		dB
Noise figure	NF			12	25	dB

* Classification

Rank	I_{DSS}	Unit
3SK166-0	20—80	mA
3SK166-1	30—55	mA
3SK166-2	45—80	mA

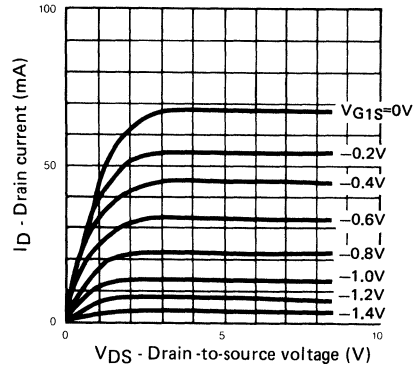
E89333-ST

Mark



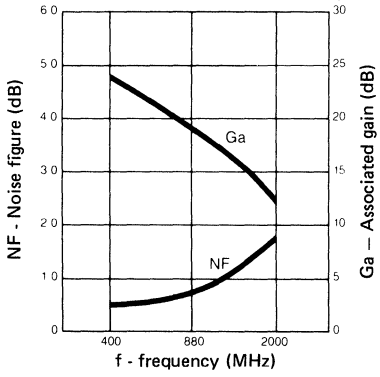
Output characteristics

(Ta=25°C, V_{G2S}=1.5V, V_{G1S}=−0.2V/step)



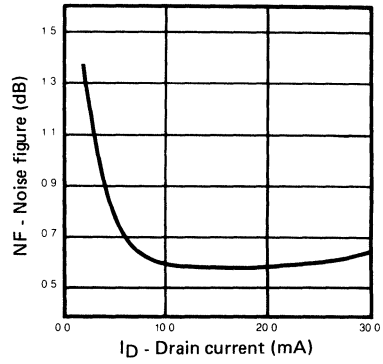
NF, Ga frequency dependence

(V_{DS}=10V, V_{G2S}=1.5V, I_D=10mA)

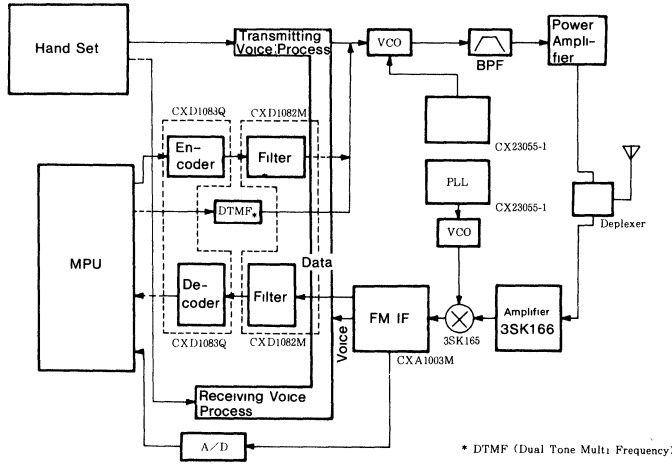


NF-I_D characteristics

(V_{DS}=5.0V, V_{G2S}=1.5V, Frequency at 450MHz)

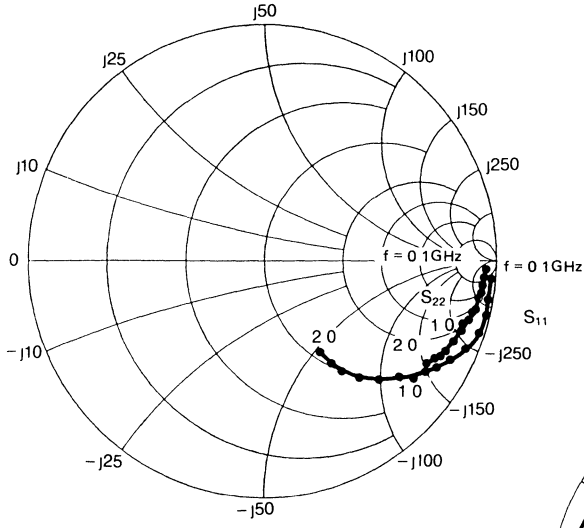


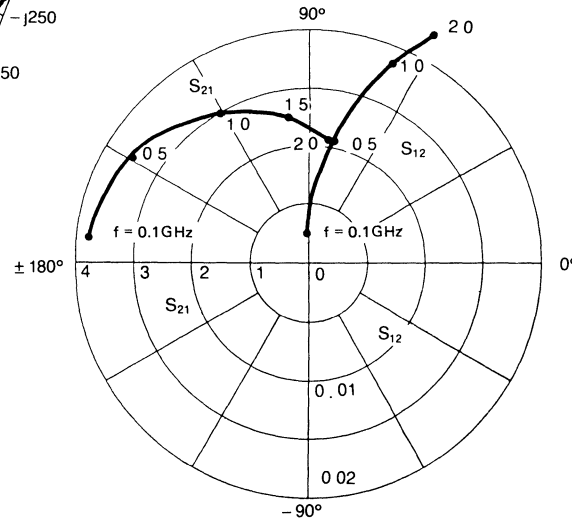
Application Example for Cellular System



S-Parameter vs. Frequency characteristics

(V_{DS}=5.0V, V_{G2S}=1.5V, I_D=10mA)





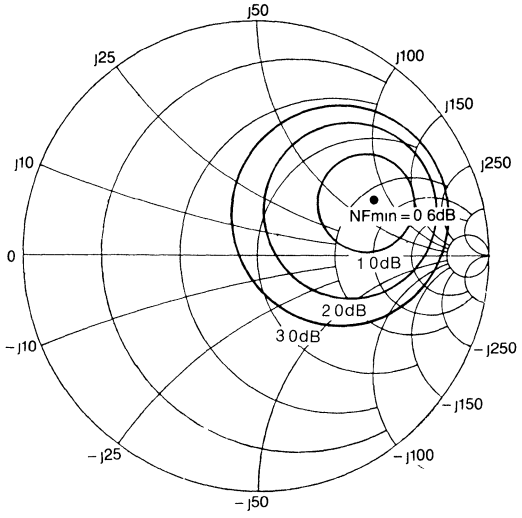
S-Parameter Data of FET 3SK166

Zo=50Ω

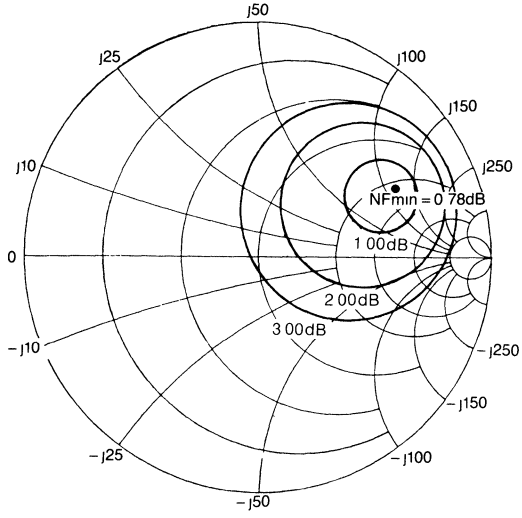
Frequency MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	.997	-4.90	3.815	173.47	0.0025	90.83	.941	-1.80
200	.991	-9.59	3.745	165.74	0.0041	86.98	.939	-4.18
300	.998	-13.04	3.672	161.43	0.0095	84.23	979	-9.40
400	.959	-18.65	3.647	155.81	0.0105	82.44	.928	-8.23
500	.933	-22.47	3.471	149.90	0.0110	76.78	.925	-9 44
600	.904	-26.50	3.400	141.51	0.0134	76.78	926	-11.85
700	.873	-30.25	3.311	137.92	0.0153	72.93	.913	-12.87
800	844	-33.71	3.173	132.54	0.0160	73.56	.912	-15.33
900	.814	-36.72	3.002	125.45	0.0172	69.08	.896	-16 30
1000	.780	-39.35	3.058	120.39	0.0189	66.18	.897	-18.80
1200	.707	-44.48	2.741	112.87	0.0217	65.07	.882	-22.55
1400	.641	-49.20	2.636	103.06	0.0246	60.53	868	-25 75
1600	.587	-52.59	2.412	95.81	0.0236	61.71	.863	-28.06
1800	.520	-54.29	2.357	88.93	0.0245	62.06	.855	-29.88
2000	.452	-57.35	2 145	80.33	0.0239	60.92	834	-31.69

Noise figure characteristics

at 450MHz (V_{DS}=5.0V, V_{G2S}=1.5V, I_D=10mA) at 880MHz

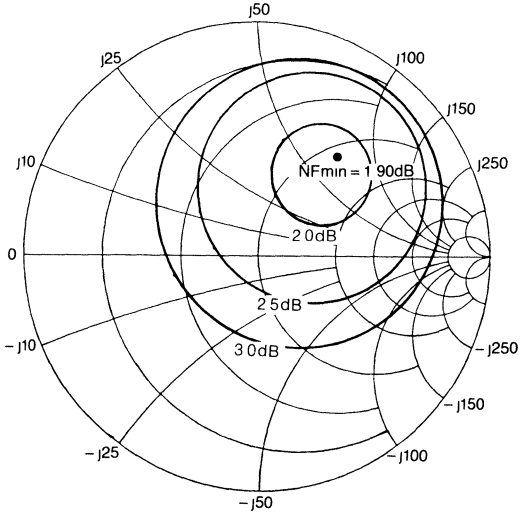


V_{DS} = 5 0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 450 MHz
NF min 0 60 dB
Ga 23 02 dB
Gamma (S), MAG 0.559 ANG 26 73°



V_{DS} = 5 0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 880 MHz
NF min 0 78 dB
Ga 19 25 dB
Gamma (S); MAG 0.616, ANG 26.89°

at 2000MHz



Frequency (MHz)	Ga (dB)	NF (dB)	Gamma- S		Gamma- L	
			MAG	ANG	MAG	ANG
400	24 31	0.51	0 689	21 39°	0 902	14 07°
450	23.02	0 60	0 559	26 73°	0 894	16 93°
500	22 43	0.66	0 690	19 49°	0 894	17 93°
880	19 25	0 78	0 616	26 87°		
2000	12.90	1 90	0 542	51 14°		

V_{DS} = 5 0V
V_{G2S} = 1 5V
I_D = 10mA
Frequency 2000 MHz
NF min 1 90 dB
Ga 12 90 dB
Gamma (S); MAG 0.542, ANG 51.14°

SONY®

SGM2004M

GaAs N-channel Dual Gate MES FET

Description

SGM2004M is an N-channel dual gate GaAs MES FET for UHF band low-noise amplification. This FET is suitable for a wide range of applications including TV tuners, cellular radios and DBS IF amplifiers.

Features

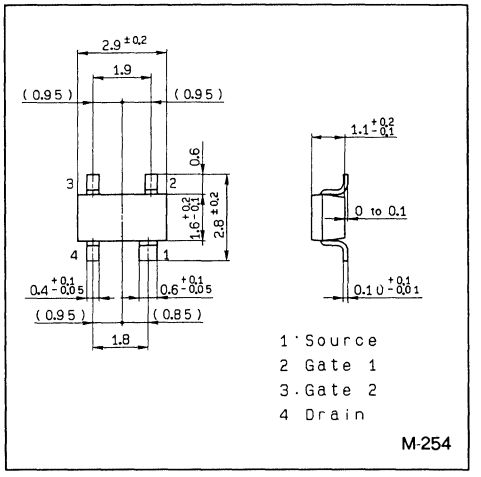
- Low voltage operation
- Low noise : NF = 1.6 dB (Typ.) at 800 MHz
- High gain : Ga = 18 dB (Typ.) at 800 MHz
- Low cross-modulation
- High stability
- Built-in gate-protection diode
- Standard SOT-143 package

Application

UHF band amplifier, mixer and oscillator

Package Outline

Unit : mm



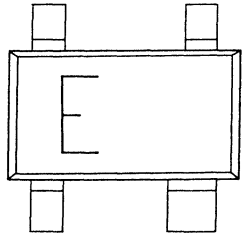
Structure

GaAs N-channel dual gate metal semiconductor field effect transistor

Absolute Maximum Ratings (Ta = 25 °C)

• Drain to source voltage	V_{DSX}	12	V
• Gate 1 to source voltage	V_{G1S}	−5	V
• Gate 2 to source voltage	V_{G2S}	−5	V
• Drain current	I_D	55	mA
• Allowable power dissipation	P_D	150	mW
• Channel temperature	Tch	150	°C
• Storage temperature	Tstg	−55 to +150	°C

Mark

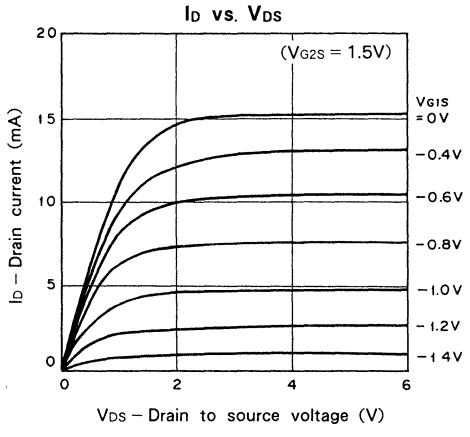


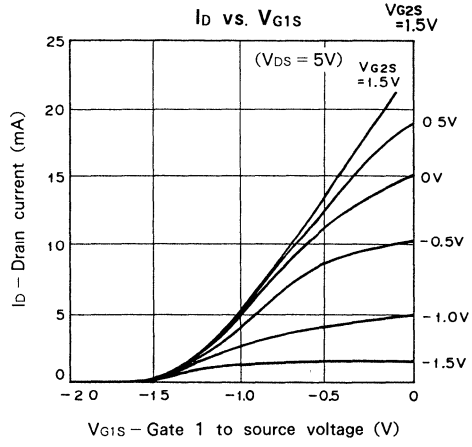
E88Z09-ST

Electrical Characteristics (Ta = 25℃)

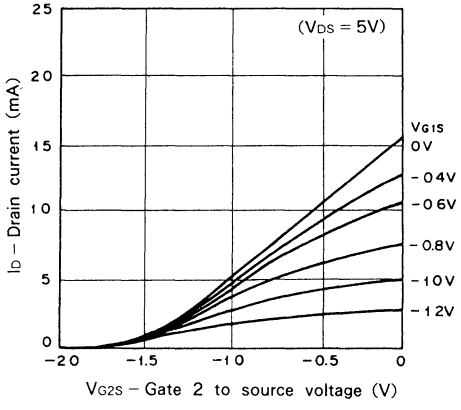
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain to source voltage	V_{DSX}	I_D = 20 μA V_{G1S} = 0V V_{G2S} = − 4.0V	11			V
Gate 1 cutoff current	I_{G1SS}	V_{G1S} = − 4.5V V_{G2S} = 0V V_{DS} = 0V			− 8	μA
Gate 2 cutoff current	I_{G2SS}	V_{G2S} = − 4.5V V_{G1S} = 0V V_{DS} = 0V			− 8	μA
Gate 2 to drain cutoff current	I_{G2DO}	V_{G2D} = − 12V			− 10	μA
Drain saturation current	I_{DSS}	V_{DS} = 5V V_{G1S} = 0V V_{G2S} = 0V	8		28	mA
Gate 1 cutoff voltage	V_{G1S} (OFF)	V_{DS} = 5V I_D = 100 μA V_{G2S} = 0V			− 2.5	V
Gate 2 cutoff voltage	V_{G2S} (OFF)	V_{DS} = 5V I_D = 100 μA V_{G1S} = 0V			− 2.5	V
Forward transfer admittance	gm	V_{DS} = 5V I_D = 8mA V_{G2S} = 1.5V f = 1KHz	11	15		mS
Input capacitance	Ciss	V_{DS} = 5V I_D = 8mA V_{G2S} = 1.5V f = 1MHz		0.9	2	pF
Reverse transfer capacitance	Crss			25	40	fF
Noise figure	NF	V_{DS} = 5V I_D = 8mA V_{G2S} = 1.5V f = 800MHz		1.6	2.5	dB
Associated gain	Ga		15	18		dB

Typical Characteristics (Ta = 25℃)

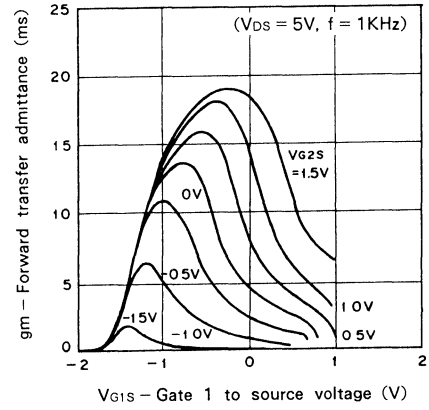




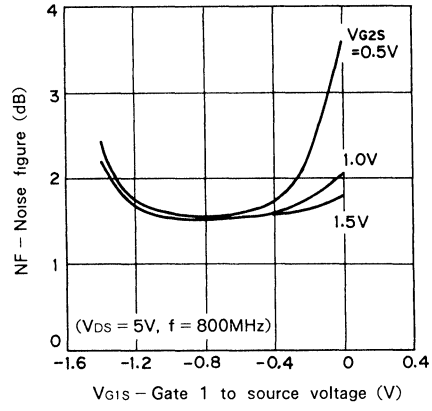
I_D vs V_{G2S}



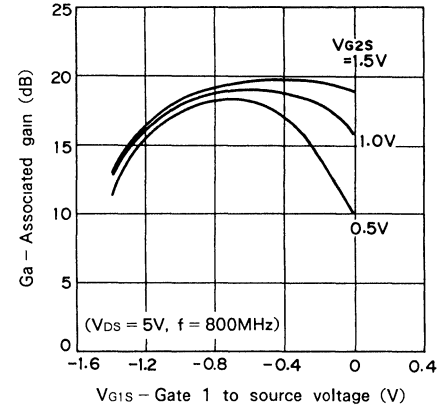
gm vs. V_{G1S}



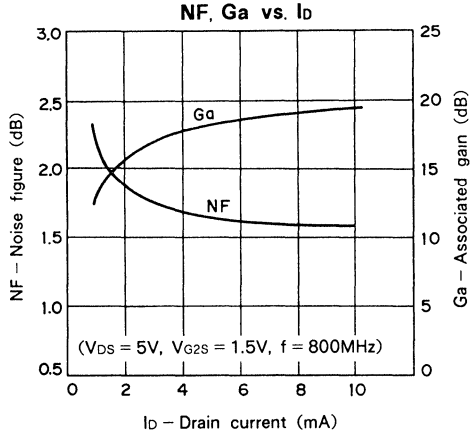
NF vs. V_{G1S}



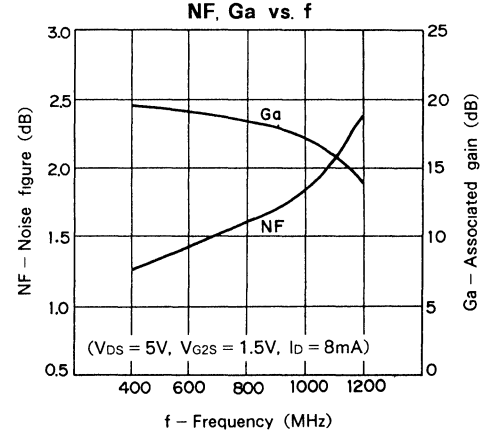
Ga vs. V_{G1S}



NF, Ga vs. I_D

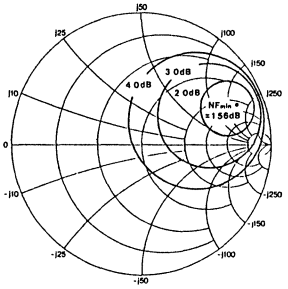


NF, Ga vs. f



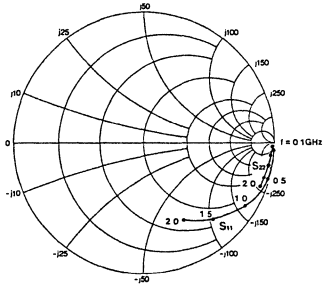
Noise Figure Characteristics (V_{DS} = 5V, V_{G2S} = 1.5V, I_D = 8 mA)

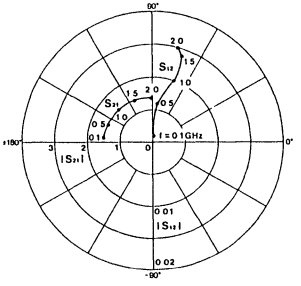
at 800 MHz



f (MHz)	Ga (dB)	NFmin (dB)	NF50 (dB)	Rn (Ω)	Γ (S)		Γ (L)	
					MAG	ANG	MAG	ANG
600	19.3	1.45	3.61	53.4	.830	17.3°	.862	1.3°
800	18.5	1.56	3.69	55.8	.793	22.2°	.895	5.8°
1000	16.4	1.77	3.73	60.3	.714	26.0°	.832	5.2°

S-parameters vs. Frequency Characteristics (V_{DS} = 5V, V_{G2S} = 1.5V, I_D = 8 mA)





f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	1.00	− 3.2°	1.50	175°	.001	78.2°	.978	− 1.4°
200	.999	− 6.3°	1.49	171°	.003	89.2°	.979	− 2.3°
300	.992	− 9.7°	1.49	166°	.004	92.7°	.975	− 3.3°
400	.981	− 12.7°	1.48	162°	.004	80.4°	.970	− 4.4°
500	.974	− 15.8°	1.47	157°	.006	82.4°	.968	− 5.3°
600	.967	− 18.8°	1.47	153°	.006	60.0°	.966	− 6.0°
700	.950	− 22.1°	1.47	149°	.008	78.7°	.968	− 7.2°
800	.939	− 25.3°	1.46	144°	.009	76.4°	.965	− 8.2°
900	.926	− 28.5°	1.46	140°	.010	78.1°	.966	− 9.4°
1000	.911	− 31.5°	1.46	135°	.010	70.9°	.965	− 10.2°
1100	.894	− 34.3°	1.46	131°	.011	74.7°	.976	− 11.1°
1200	.863	− 37.3°	1.45	126°	.011	60.9°	.953	− 12.7°
1300	.843	− 40.6°	1.44	122°	.012	74.5°	.956	− 13.7°
1400	.818	− 43.7°	1.43	117°	.013	77.1°	.952	− 14.6°
1500	.792	− 47.1°	1.41	113°	.014	70.7°	.950	− 15.7°
1600	.769	− 50.3°	1.40	108°	.014	70.1°	.944	− 16.4°
1700	.746	− 53.4°	1.39	104°	.014	76.3°	.946	− 17.2°
1800	.725	− 56.5°	1.39	100°	.014	79.2°	.947	− 18.2°
1900	.696	− 59.2°	1.38	95.8°	.015	76.2°	.949	− 19.4°
2000	.665	− 61.8°	1.37	91.2°	.015	74.6°	.948	− 20.4°

SONY

SGM2006M/P

GaAs N-channel Dual Gate MES FET

Description

SGM2006M/P is an N-channel dual gate GaAs MES FET for UHF band low-noise amplification. This FET is suitable for a wide range of applications including TV tuners, cellular radios and DBS IF amplifiers.

Features

- Low voltage operation
- Low noise : NF = 1.2 dB (Typ.) at 800 MHz
- High gain : Ga = 22 dB (Typ.) at 800 MHz
- High stability
- Built-in gate-protection diode
- Standard SOT-143 package

Application

UHF band amplifier, mixer and oscillator

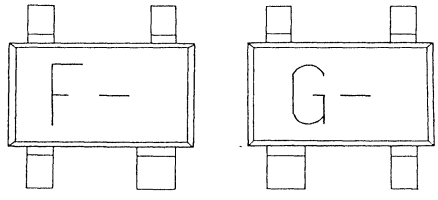
Structure

GaAs N-channel dual gate metal semiconductor field effect transistor

Absolute Maximum Ratings (Ta = 25 °C)

• Drain to source voltage	V_{DSX}	12	V
• Gate 1 to source voltage	V_{G1S}	−5	V
• Gate 2 to source voltage	V_{G2S}	−5	V
• Drain current	I_D	55	mA
• Allowable power dissipation	P_D	150	mW
• Channel temperature	Tch	150	°C
• Storage temperature	Tstg	−55 to +150	°C

Mark

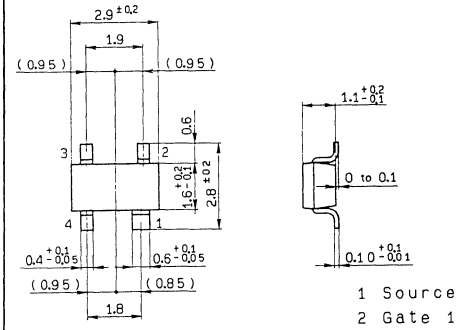


SGM2006M SGM2006P

Package Outline

Unit : mm

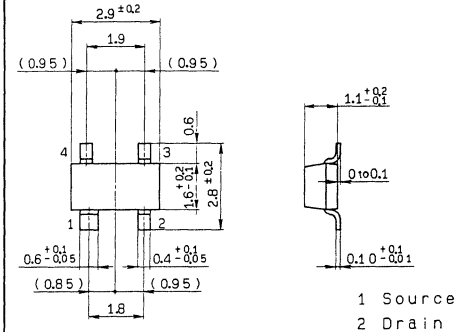
SGM2006M



1 Source
2 Gate 1
3 Gate 2
4 Drain

M-254

SGM2006P



1 Source
2 Drain
3 Gate 2
4 Gate 1

M-255

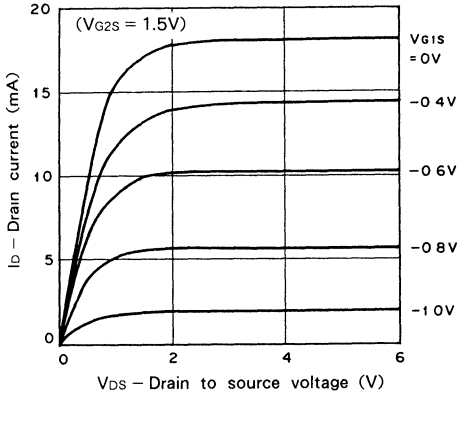
E88Z10-ST

Electrical Characteristics (Ta = 25℃)

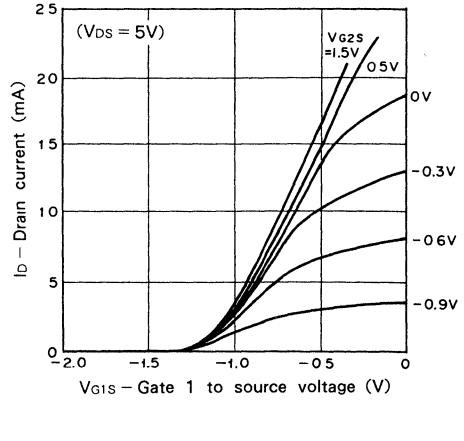
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain to source voltage	V_{DSX}	I_D = 20 μA V_{G1S} = 0V V_{G2S} = − 4.0V	11			V
Gate 1 cutoff current	I_{G1SS}	V_{G1S} = − 4.5V V_{G2S} = 0V V_{DS} = 0V			− 8	μA
Gate 2 cutoff current	I_{G2SS}	V_{G2S} = − 4.5V V_{G1S} = 0V V_{DS} = 0V			− 8	μA
Gate 2 to drain cutoff current	I_{G2DO}	V_{G2D} = − 12V			− 10	μA
Drain saturation current	I_{DSS}	V_{DS} = 5V V_{G1S} = 0V V_{G2S} = 0V	10		35	mA
Gate 1 cutoff voltage	V_{G1S} (OFF)	V_{DS} = 5V I_D = 100 μA V_{G2S} = 0V			− 2.5	V
Gate 2 cutoff voltage	V_{G2S} (OFF)	V_{DS} = 5V I_D = 100 μA V_{G1S} = 0V			− 2.5	V
Forward transfer admittance	gm	V_{DS} = 5V I_D = 10mA V_{G2S} = 1.5V f = 1KHz	20	26		mS
Input capacitance	Ciss	V_{DS} = 5V I_D = 10mA V_{G2S} = 1.5V f = 1MHz		1.1	3	pF
Reverse transfer capacitance	Crss			28	40	fF
Noise figure	NF	V_{DS} = 5V I_D = 10mA V_{G2S} = 1.5V f = 800MHz		1.2	2.0	dB
Associated gain	Ga		18	22		dB

Typical Characteristics (Ta = 25℃)

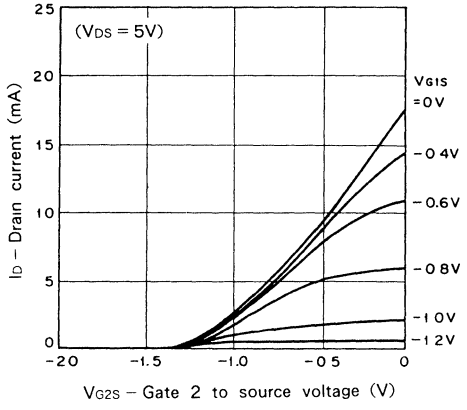
I_D vs. V_{DS}



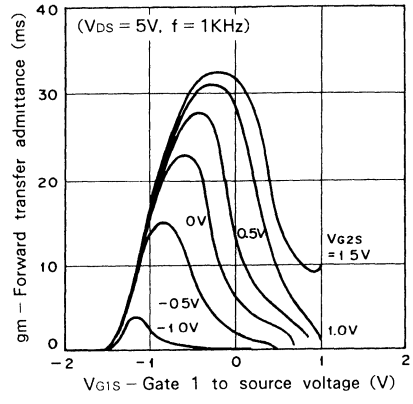
I_D vs. V_{G1S}



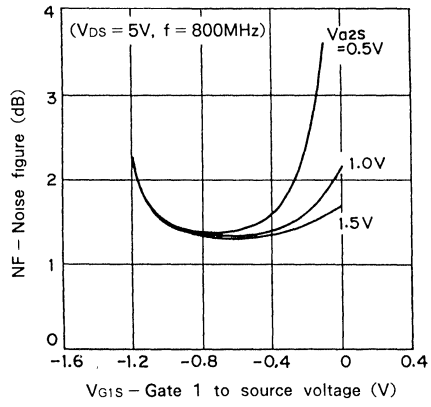
I_D vs. V_{G2S}



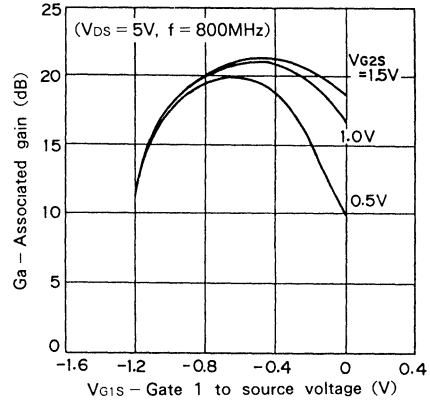
gm vs. V_{G1S}



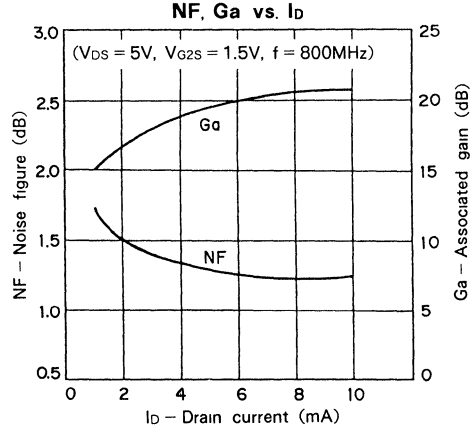
NF vs. V_{G1S}



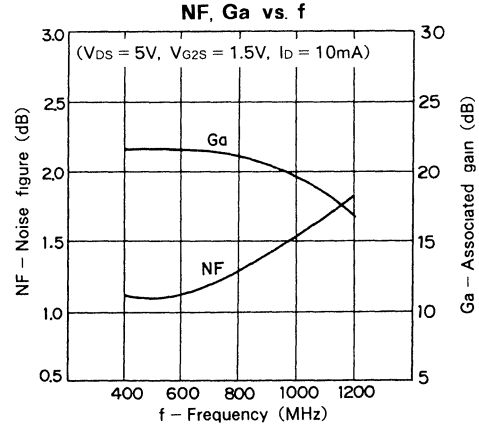
Ga vs. V_{G1S}



NF, Ga vs. I_D

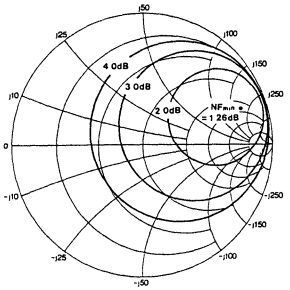


NF, Ga vs. f



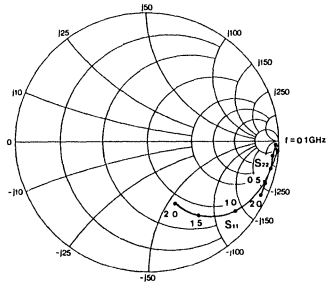
Noise Figure Characteristics (V_{DS} = 5V, V_{G2S} = 1.5V, I_D = 10 mA)

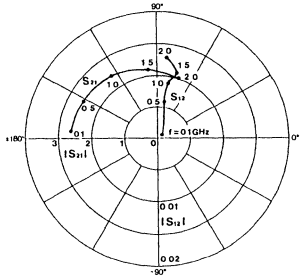
at 800 MHz



f (MHz)	Ga (dB)	NFmin (dB)	NF50 (dB)	Rn (Ω)	Γ (S)		Γ (L)	
					MAG	ANG	MAG	ANG
600	21.2	1.23	2.59	29.1	.823	18.9°	.824	3.1°
800	20.8	1.26	2.59	29.2	.804	20.4°	.896	5.8°
1000	19.5	1.57	2.78	37.7	.750	24.2°	.865	3.9°

S-parameters vs. Frequency Characteristics (V_{DS} = 5V, V_{G2S} = 1.5V, I_D = 10 mA)





f (MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	1.00	− 4.0°	2.63	174°	.001	50.9°	.976	− 1.6°
200	.996	− 8.0°	2.62	168°	.002	84.7°	.975	− 2.8°
300	.985	− 12.3°	2.61	163°	.004	85.8°	.971	− 4.0°
400	.968	− 16.0°	2.57	157°	.004	77.0°	.968	− 5.2°
500	.953	− 19.9°	2.55	152°	.006	80.2°	.965	− 6.4°
600	.933	− 24.1°	2.53	146°	.006	84.4°	.966	− 7.8°
700	.916	− 27.6°	2.51	141°	.007	75.3°	.964	− 8.7°
800	.895	− 31.5°	2.49	135°	.008	77.9°	.963	− 9.9°
900	.872	− 35.1°	2.47	130°	.009	77.1°	.962	− 11.3°
1000	.844	− 38.8°	2.45	125°	.009	79.8°	.961	− 12.3°
1100	.819	− 42.1°	2.42	119°	.010	72.3°	.959	− 13.6°
1200	.778	− 44.8°	2.36	114°	.010	75.4°	.955	− 15.0°
1300	.747	− 48.9°	2.33	108°	.010	76.0°	.953	− 16.5°
1400	.713	− 52.4°	2.29	103°	.011	80.0°	.950	− 17.7°
1500	.679	− 55.7°	2.24	97.1°	.011	74.2°	.945	− 19.1°
1600	.646	− 58.6°	2.18	92.1°	.011	70.0°	.939	− 19.7°
1700	.616	− 61.5°	2.14	87.4°	.012	76.5°	.946	− 20.9°
1800	.589	− 63.8°	2.12	82.0°	.012	83.6°	.949	− 22.1°
1900	.552	− 65.7°	2.09	76.8°	.012	81.7°	.953	− 23.7°
2000	.517	− 66.8°	2.06	71.3°	.013	83.4°	.956	− 25.4°

Sony Corporation

Application Engineering Division : Semiconductor Group
4-14-1 Asahi-cho Atsugi-shi Kanagawa-ken 243 Japan
☎ : (0462) 30-5399
Fax : (0462) 30-6143

International Sales & Marketing Division : Semiconductor Marketing Group
4-10-18 Takanawa Minato-ku Tokyo 108 Japan
☎ : (03) 3448-3426
Fax : (03) 3448-7493
Telex : Sony Corp J24666

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