

# SONY®

## Semiconductor IC

# Data Book 1991

# SPECL Standard Logic



883 N. SHORELINE BLVD.  
MOUNTAIN VIEW, CALIFORNIA 94043  
(415) 960-3880



**SONY®**

**SPECL Standard Logic Family  
Semiconductor Integrated Circuit Data Book  
1991**

**Numerical Index and  
Selection Guide**

**1**

**General Information**

**2**

**Family DC Specification**

**3**

**AC Test Circuit**

**4**

**Data Sheets**

**5**

**Package Data**

**6**

**Application Note**

**7**



## PREFACE

This data book contains device specifications for SONY SPECL\* (SONY Picosecond ECL) Standard Logic Family capable of picosecond and GHz digital signal processing. The Family offers a single gate delay time of 410ps and a Flip-Flop toggle frequency of 3.0GHz while maintaining electrical compatibility to interface with existing 100K standard logic IC's.

SPECL Standard Logic Family was developed for the use of super high speed and high performance standard logic functions in such applications as measuring instruments, automatic testers, optical and wireless communications and computers.

SPECL Standard Logic Family is fabricated using a 0.6 micron emitter process with double poly-silicon electrode structure developed by SONY. The device has a transistor  $f_T$  of 10GHz and the chip has a propagation delay time of 100ps at the internal gate.

The family is designed using SONY E3G70 or E3G200 Gate Arrays. Specific functions can easily be implemented through close consultation with the user and ECL system design engineers.

SPECL Standard Logic Family is offered in a 30mil Quad Flat Package. This package feature reduced parasitics and good thermal conductivity for effective heat sinking. The high density surface mount it provides offers the user potential advantages.

\*SPECL is a trade mark of SONY Corp. and pronounced "Special".

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. **Sony** cannot assume responsibility for any problems arising out of the use of these circuits.



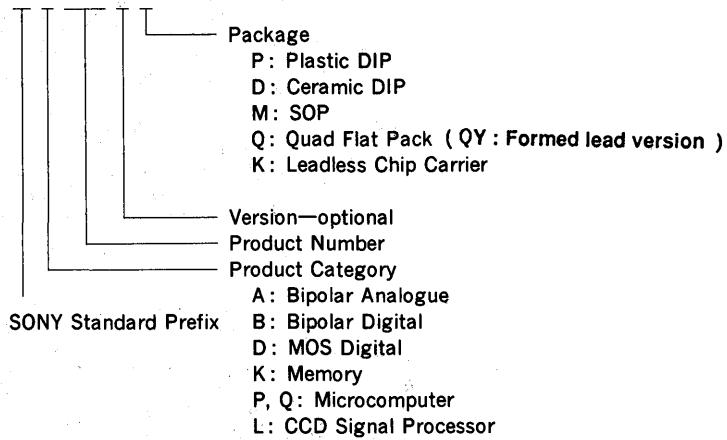


**Numerical Index and  
Selection Guide**



## Nomenclature of IC product name

CX B 1001 A Q





# Numerical Index

** Part Number	Function	*Speed	Number of Pins	Page
CXB1100Q	Quad 3-input OR/NOR Gate	410ps	24	5-4
CXB1101Q	Quad 3-input AND/NAND Gate	490ps	24	5-6
CXB1102Q	Quad EX-OR/NOR Gate	530ps	24	5-8
CXB1103Q	Quint Line Receiver with Differential I/O	430ps	24	5-10
CXB1104Q	Dual D Flip-Flop with Set, Reset and Differential I/O	3.2GHz	24	5-12
CXB1105Q	Triple Fan-out Buffer with Common Enable and Differential Output	660ps	24	5-14
CXB1106Q	4-bit Ripple Down Counter with Enable and Reset	3.0GHz	24	5-16
CXB1107Q	Decision Circuit with Differential I/O	2.3GHz	24	5-18
CXB1108Q	Laser Driver	2.0Gbps	16	5-20
CXB1109Q	Quad D Flip-Flop with Master Reset and Differential I/O	3.1GHz	24	5-24
CXB1110Q	16-Line to 1-Line Data Selector/Multiplexer	1170ps	24	5-26
CXB1111Q	4-bit Look-Ahead Carry Generator	700ps	24	5-28
CXB1112Q	Phase Frequency Detector with Differential I/O	800MHz	24	5-30
CXB1113Q	4-bit Multiplexer	1.8GHz	24	5-32
CXB1114Q	4-bit Demultiplexer	2.1GHz	24	5-38
CXB1115Q	Clock Distributor with Enable and 10 Differential Outputs	760ps	32	5-42
CXB1116Q	4-bit Ripple Counter with Enable and Reset	3.0GHz	24	5-44
CXB1119Q	Programmable Delay Line/Duty Cycle Controller	870 ~2240ps	24	5-46
CXB1130Q	9, 8, Dual 4-bit Multiplexer	1.6GHz	32	5-52
CXB1131Q	9, 8, Dual 4-bit Demultiplexer	1.5GHz	32	5-58
CXB1132Q	9, 8, Dual 4-bit Universal Shift Register	1.3GHz	32	5-66
CXB1133Q	22, 15, 7 Stage Data Scrambler with Differential I/O	1.4GHz	24	5-70
CXB1134Q	22, 15, 7 Stage Descrambler with Differential I/O	1.4GHz	24	5-74
CXB1135Q	8 to 16-bit Serial Data Comparator	1.4GHz	32	5-78
CXB1136Q	8-bit Universal Counter with Preset and Master Reset	1.1GHz	32	5-82
CXB1137Q	8-bit Shift Matrix	1450ps	24	5-86
CXB1138Q	4-bit Arithmetic Logic Unit (ALU)	1440ps	24	5-90
CXB1139Q	Programmable Delay Line/Duty Cycle Controller	775 ~4650ps	24	5-96
CXB1140Q	Hex 2: 1 Multiplexer with Latch	2.6GHz	32	5-102
CXB1141Q	Hex 2: 1 Multiplexer with D-FF	2.6GHz	32	5-106
CXB1142Q	Quad 4: 1 Multiplexer with Latch	2.6GHz	32	5-110
CXB1143Q	Quad 4: 1 Multiplexer with D-FF	2.6GHz	32	5-114
CXB1144Q	Dual 8: 1 Multiplexer with Latch	2.6GHz	32	5-118
CXB1145Q	Dual 8: 1 Multiplexer with D-FF	2.6GHz	32	5-122

Note: \* ; Typical value.

\*\* ; Formed lead version is available. (ex. CXB1100QY)

# Functional Index

## Gates

Function	Part Number	Page
Quad 3-input OR/NOR Gate	CXB1100Q	5-4
Quad 3-input AND/NAND Gate	CXB1101Q	5-6
Quad EX-OR/NOR Gate	CXB1102Q	5-8

## Buffers/Inverters

Function	Part Number	Page
Quint Line Receiver with Diff. I/O	CXB1103Q	5-10
Triple Fan-Out Buffer with Common Enable and Diff. Output	CXB1105Q	5-14
Clock Distributor with Enable and 10 Diff. Outputs	CXB1115Q	5-42

## Flip-Flops

Function	Part Number	Page
Dual D-FF with Set, Reset and Diff. I/O	CXB1104Q	5-12
Decision Circuit with Diff. I/O	CXB1107Q	5-18
Quad D-FF with Master Reset and Diff. I/O	CXB1109Q	5-24

## Multiplexers

Function	Part Number	Page
16 Line to 1 Line Data Selector/Multiplexer	CXB1110Q	5-26
4-bit Multiplexer	CXB1113Q	5-32
9, 8, Dual 4-bit Multiplexer	CXB1130Q	5-52
Hex 2 : 1 Multiplexer with Latch	CXB1140Q	5-102
Hex 2 : 1 Multiplexer with D-FF	CXB1141Q	5-106
Quad 4 : 1 Multiplexer with Latch	CXB1142Q	5-110
Quad 4 : 1 Multiplexer with D-FF	CXB1143Q	5-114
Dual 8 : 1 Multiplexer with Latch	CXB1144Q	5-118
Dual 8 : 1 Multiplexer with D-FF	CXB1145Q	5-122

## Demultiplexers

Function	Part Number	Page
4-bit Demultiplexer	CXB1114Q	5-38
9, 8, Dual 4-bit Demultiplexer	CXB1131Q	5-58

## Counters

Function	Part Number	Page
4-bit Ripple Down Counter with Enable and Reset	CXB1106Q	5-16
8-bit Universal Counter with Preset and Master Reset	CXB1136Q	5-82
4-bit Ripple Counter with Enable and Reset	CXB1116Q	5-44

## Arithmetic Operators

Function	Part Number	Page
4-bit Look-Ahead Carry Generator	CXB1111Q	5-28
4-bit Arithmetic Logic Unit (ALU)	CXB1138Q	5-90
8-bit Shift Matrix	CXB1137Q	5-86

## Shift Registers

Function	Part Number	Page
9, 8, Dual 4-bit Universal Shift Register	CXB1132Q	5-66

## Parallel to Serial Converters

Function	Part Number	Page
4-bit Multiplexer	CXB1113Q	5-32
9, 8, Dual 4-bit Multiplexer	CXB1130Q	5-52

## Serial to Parallel Converters

Function	Part Number	Page
4-bit Demultiplexer	CXB1114Q	5-38
9, 8, Dual 4-bit Demultiplexer	CXB1131Q	5-58

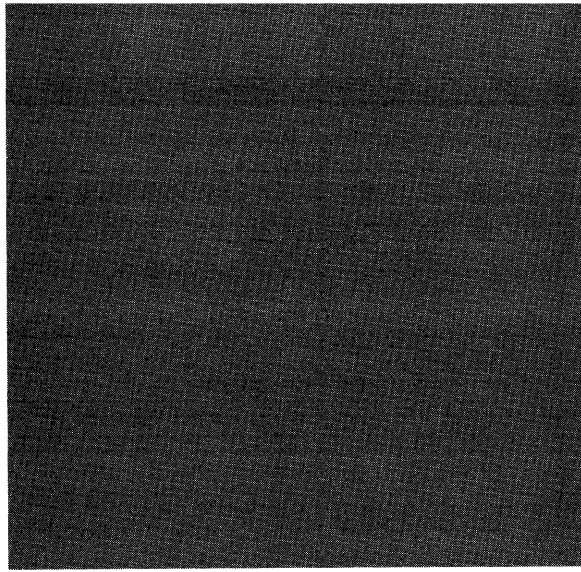
## Data Scrambler/Descrambler

Function	Part Number	Page
22, 15, 7 Stage Data Scrambler with Diff. I/O	CXB1133Q	5-70
22, 15, 7 Stage Descrambler with Diff. I/O	CXB1134Q	5-74

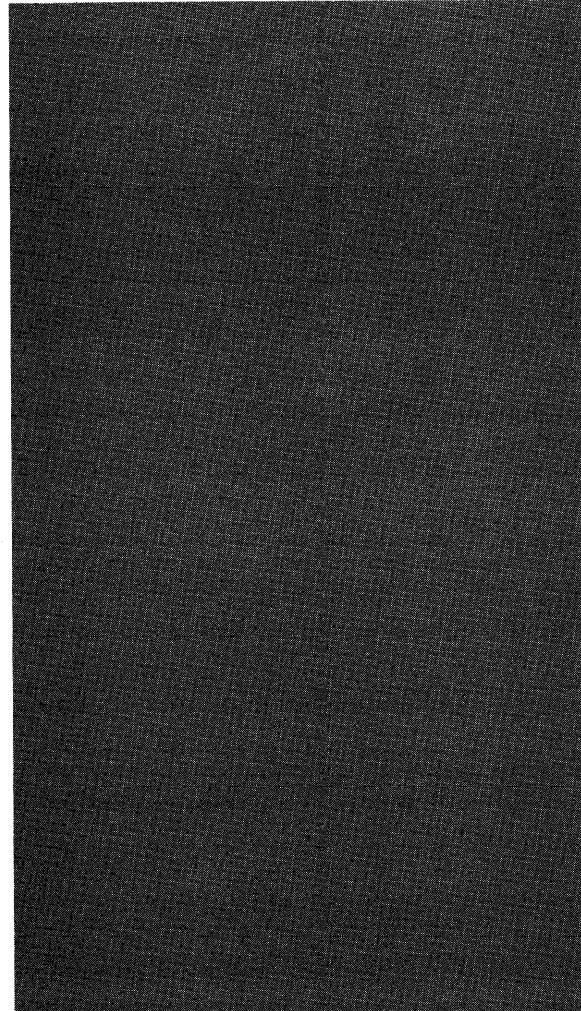
## Special Functions

Function	Part Number	Page
Decision Circuit with Diff. I/O	CXB1107Q	5-18
Laser Driver	CXB1108Q	5-20
Phase Frequency Detector with Diff. I/O	CXB1112Q	5-30
Programmable Delay Line/Duty Cycle Controller	CXB1119Q	5-46
8 to 16-bit Serial Data Comparator	CXB1135Q	5-78
Programmable Delay Line/Duty Cycle Controller	CXB1139Q	5-96





## **General Information**



## General Information

<b>General Information</b>	<b>Page</b>
1. SPECL Standard Logic Family	2-3
2. Fabrication Process of SPECL	2-4
3. Definition of Letter Symbols and Terms	2-6
4. Technical Data	2-7
5. Handling Precautions	2-10
6. Quality Assurance and Reliability	2-15

# General Information

## 1. SPECL Standard Logic Family

SPECL Standard Logic Family was designed to meet engineers' requirements in which the existing 10K/10KH and 100K ECL (Emitter Coupled Logic) families are not sufficient in their propagation delay time and edge rate to realize state of the art systems.

SPECL Standard Logic Family operates with  $-4.5V$  power supply and has a capability of driving  $50 \Omega$  load into  $-2V$  termination voltage. The logic circuit employs an emitter coupled logic with reduced voltage swing in internal gates to increase speed, while maintaining direct interface compatibility to existing ECL logics. The internal gate utilizes two stage series gating and is biased by a stabilized reference voltage source.

### The family has the following characteristics:

- Low propagation delay time ...100ps internal gate
- Fast edge rate ...200ps tr and tf
- Very small pin-to-pin time skew ...40ps
- Excellent AC characteristics ...3.0GHz Flip-Flop toggle frequency
- Compatibility with existing ECL logics and memories
- Temperature compensation over wide temperature range
- Wide operation voltage range
- Simultaneous complementary outputs
- Good noise immunity
- Internal series gating and reduced internal voltage swing
- High gain transfer characteristics
- Low input capacitance ...3pF
- External wired-OR capability
- Internal  $27K\Omega$  input termination

A basic ECL inverter circuit used in the family is shown in Figure 1. All input ports of the family IC have termination resistors as shown in the figure.

When an input terminal is left open, this resistor network pulls down this terminal voltage to  $-2V$ , keeping it to logic Low voltage level.

Input voltage of standard ECL logic level is translated into internal logic level by the input buffer. The internal logic level is designed to be 400mV to obtain higher speed in internal circuit.

The internal voltage swing is again translated into standard ECL logic level and buffered to drive an external circuit in the output buffer stage. Data outputs are provided by emitter follower transistors.

An internal temperature stabilized voltage reference is implemented in the circuit to provide a threshold voltage for interfacing with the external circuit and internal biasing.

Input and output terminals are guarded against an ESD (Electro Static Discharge) by protection diodes and resistors.

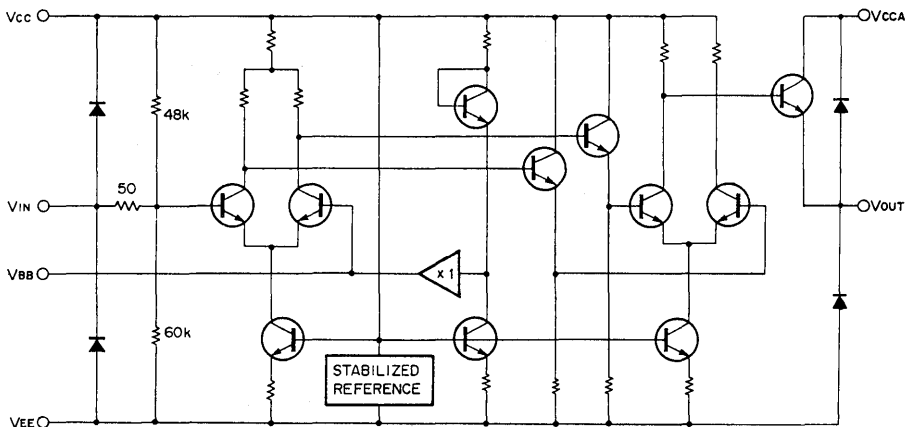


Figure 1. Basic ECL Inverter Circuit

## 2. Fabrication Process of SPECL

SPECL Standard Logic Family is fabricated on a double poly-silicon electrode process developed by SONY. This process realizes an emitter width of 0.6microns, a base dimension of 2.4microns  $\times$  3.0 microns and a transistor cell size of 9.6  $\times$  16microns for the minimum geometry. Very small size and dimensions offer very high transistor  $f_T$  of 10GHz and very low parasitic capacitances. Furthermore, the process offers a poly-silicon resistor with very low parasitics and a low temperature coefficient.

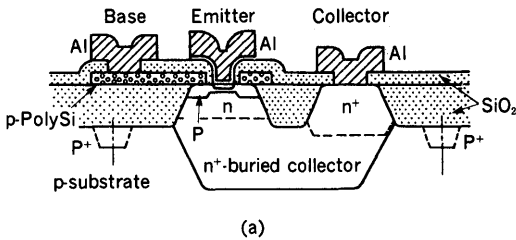
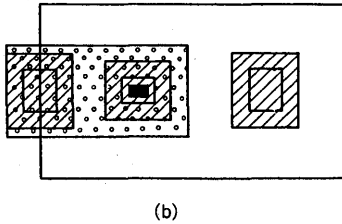


Figure 2.

Figures 2-a and 2-b show the cross section and minimum geometry of the transistor.

This structure has three excellent features in comparison with a conventional structure.

- (1) The emitter is self-aligned to the base poly-silicon electrode, and has a width of 0.6microns. A spacer dielectric 0.3microns thick separates base and emitter electrode reducing extrinsic base region.
- (2) The base electrode is formed by the poly-silicon encircling the emitter region to make contact with the external circuit. This structure makes a base resistance small and also reduces extrinsic base region and base parasitics.
- (3) The emitter electrode is formed by a thin poly-silicon to reduce junction depth and enhance an emitter efficiency.

Figure 3 shows a transistor  $f_T$  as a function of collector current.

The maximum  $f_T$  of 10GHz is attained by this structure. Table 1 shows electric characteristics of the transistor.

Table 1. Transistor Parameters

$h_{FE}$	100
$BV_{CEO}$	6.5V
$BV_{CBO}$	20V
$BV_{EBO}$	4.0V
$C_{CB}$	10fF
$C_{BE}$	8fF
$C_{CS}$	30fF
$f_T$	10GHz
$t_{pd}$ (Ring Osc.)	75ps



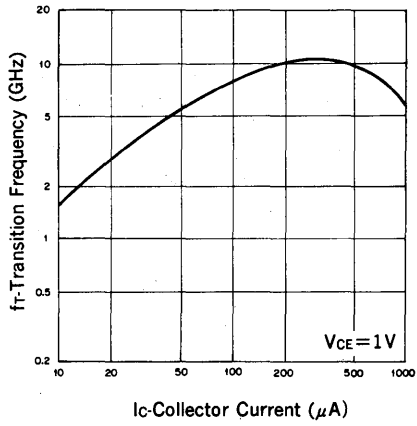


Figure 3.  $f_T$  vs  $I_C$

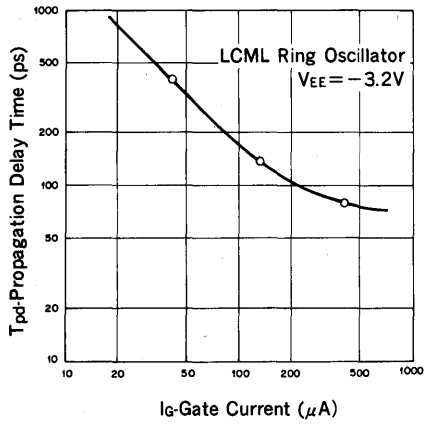


Figure 4. Propagation Delay Time measured by an LCML Ring oscillator

### 3. Definition of Letter Symbols and Terms

I <sub>EE</sub>	Total power supply current drawn from the negative power supply V <sub>EE</sub> .	T <sub>H</sub>	Hold time: The minimum time (50% to 50%) after the transition of the clock pulse that information must remain unchanged at the Data input terminal to insure proper operation.
I <sub>I</sub>	Current into the input pin of the device.	T <sub>SG-G</sub>	Gate to gate time skew
I <sub>IH</sub>	HIGH level input current into the input pin with a specific HIGH level (V <sub>IHMAX</sub> ) voltage applied.	T <sub>R</sub>	Release time: The minimum time (50% to 50%) before transition of the clock pulse where Set or Reset must be released at the Set or Reset input terminal to insure proper operation.
I <sub>O</sub>	Output current from the device.	T <sub>PW</sub>	Pulse width: The minimum pulse width (50% to 50%) of Set or Reset pulse at the Set or Rest input terminal to insure proper operation.
V <sub>CC</sub>	Circuit ground for the device. This is the most positive potential of the system and is used as the reference level for other voltages.	f <sub>MAX</sub>	Maximum Toggle frequency of a flip-flop or counter device, maximum Shift frequency of a shift register, or maximum frequency at that the output waveform level decreases 3dB down from DC level with specified condition applied to input terminal.
V <sub>CCA</sub>	Circuit ground for output emitter follower transistor.	T <sub>stg</sub>	Maximum temperature at which device may be stored without damage or performance degradation.
V <sub>EE</sub>	Negative power supply voltage for the device (usually -4.5V for the family). This is the most negative potential in the system.	T <sub>j</sub>	Junction temperature of the device.
V <sub>BB</sub>	Reference bias voltage which is used as input and output threshold level.	T <sub>a</sub>	Ambient (environment) temperature.
V <sub>IN</sub>	Input voltage to the device.	θ <sub>ja</sub>	Thermal resistance of an IC package, junction to ambient.
V <sub>IH</sub>	Input logic HIGH voltage level.	θ <sub>jc</sub>	Thermal resistance of an IC package, junction to case.
V <sub>IL</sub>	Input logic LOW voltage level.	C <sub>IN</sub>	Input capacitance at input terminal.
V <sub>OH</sub>	Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current or load, with the specified conditions applied to establish a HIGH level at the output.	C <sub>OUT</sub>	Output capacitance at output terminal.
V <sub>OL</sub>	Output logic LOW voltage level: The voltage level at the output terminal for a specified output current or load, with the specified condition applied to establish a LOW level at the output terminal.	R <sub>L</sub>	Load resistance for output.
V <sub>TT</sub>	Line load-resistor terminating voltage (usually -2V for the Family) for outputs from the device.	R <sub>P</sub>	An input pull-down resistor.
T <sub>pd</sub>	Propagation delay time, input to output.	R <sub>T</sub>	Termination load resistor to V <sub>TT</sub> .
T <sub>PLH</sub>	Propagation delay time, input to output rising edge from the 50% point of input waveform at the pin to the 50% point of output waveform at the pin.		
T <sub>PHL</sub>	Propagation delay time, input to output falling edge from the 50% point of input waveform at the pin to the 50% point of output waveform at the pin.		
T <sub>TLH</sub>	Waveform rise time from 20% to 80%.		
T <sub>THL</sub>	Waveform fall time from 80% to 20%.		
T <sub>S</sub>	Setup time: The minimum time (50% to 50%) before transition of the clock pulse that information must be present at the Data input terminal to insure proper operation of the device.		

## 4. Technical Data

### VOLTAGE TRANSFER CURVES

SPECL Standard Logic Family permits direct interface with slower prevailing ECL logic families and ECL memories.

The typical voltage swing is 780mV and all voltage levels are specified with a 50Ω load to -2V at all outputs to provide transmission line drive capability.

The voltage transfer characteristics for the differential outputs are represented by two curves: one to describe OR output and one to describe NOR output.

Typical transfer curves are shown in Figure 5-a for case temperature ranges of 0°C to +125°C.

An IC has a temperature stabilized voltage reference source inside it, and has very small temperature coefficient for switching threshold ( $V_{BB}$ ).  $V_{OH}$  and  $V_{OL}$  depend slightly on temperature. This is because the compensation network for an output stage is eliminated to provide maximum transition speed at the output terminal. In spite of this compromise, the noise margin is maintained over a wide temperature range.

Figure 5-b shows the change in transfer curves vs. change in supply voltage.

The voltage gain at the transition point of OR/NOR gate is typically 15 in contrast to the small gain of 4 in prevailing ECL families. The high voltage gain and good temperature stability of threshold voltage ensures a large noise margin.

### OUTPUT CHARACTERISTICS

As the output terminal has an inherently low output impedance, a relatively constant output level is maintained for the change of output current.

Figure 8 shows output characteristic vs. output termination.

### CHANGE IN $I_{EE}$ vs. CHANGE IN $V_{EE}$ and TEMPERATURE

As shown in Figure 10,  $V_{EE}$  power supply current also remains relatively constant over the specified voltage range (-4.2V to -4.8V); therefore the propagation delay time is relatively constant versus power supply voltage.

Figure 11 shows change in  $I_{EE}$  vs. change in temperature.

### CHANGES IN TRANSITION CHARACTERISTICS vs. LOAD CAPACITANCE

All of the AC characteristics are measured using a strip-line test fixture and a sampling oscilloscope. The load capacitance of the fixture is less than 2pF. Figure 12 shows the typical characteristics of a dependence of the propagation delay time and rise/fall time on the load capacitance.

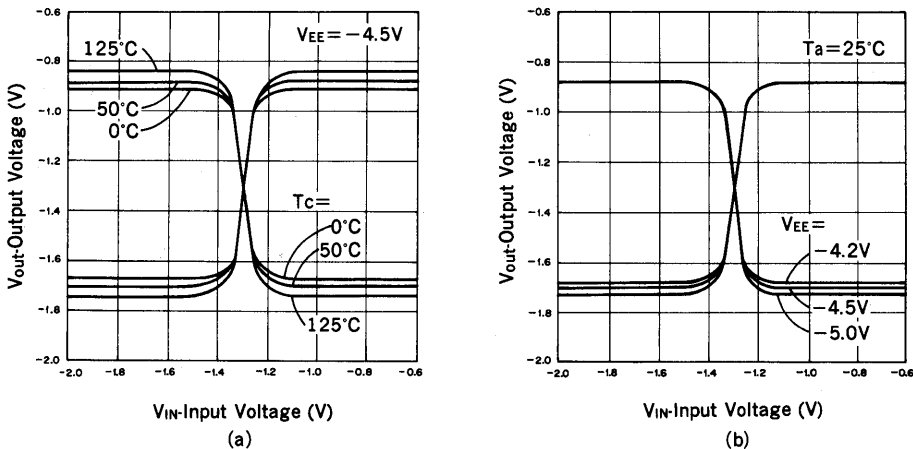


Figure 5. Transfer characteristics

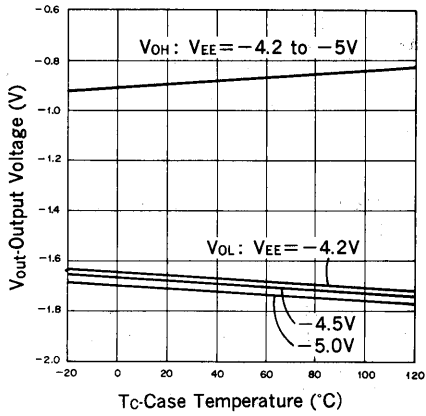


Figure 6. Change in Output Voltage vs Change in Case Temperature

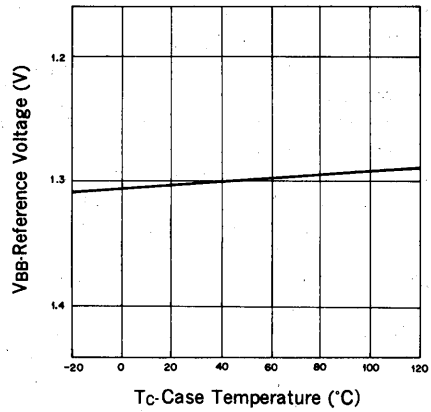


Figure 7. Change in Reference Voltage vs Change in Case Temperature

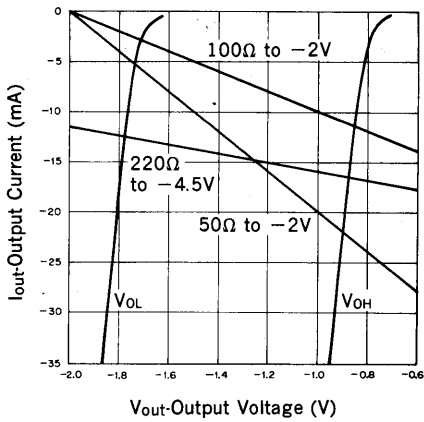


Figure 8. Output characteristics vs Output Termination

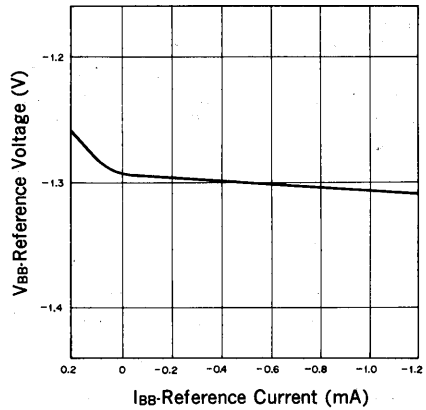


Figure 9. Change in Reference Voltage vs Reference current

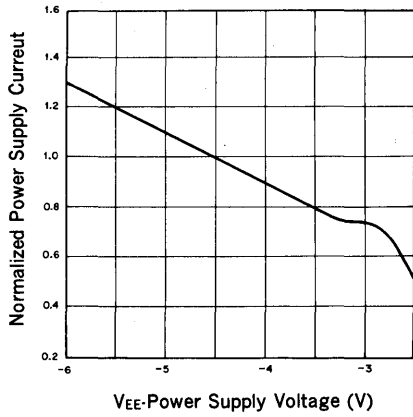


Figure 10. Change in I<sub>EE</sub> vs. Change in V<sub>EE</sub>

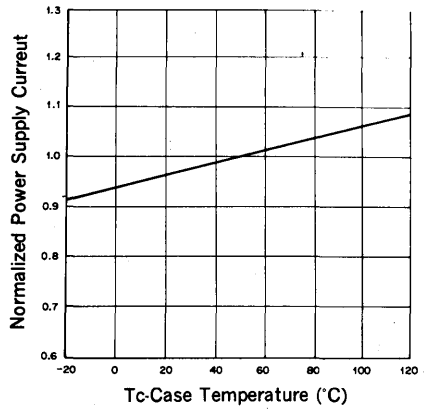


Figure 11. Change in I<sub>EE</sub> vs Change in Case Temperature

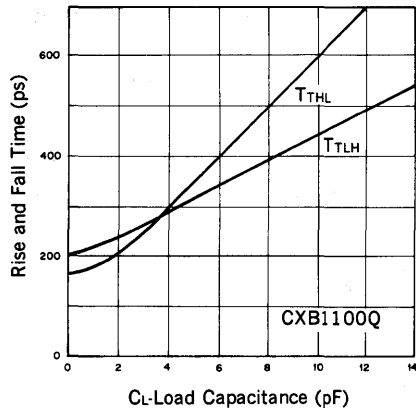
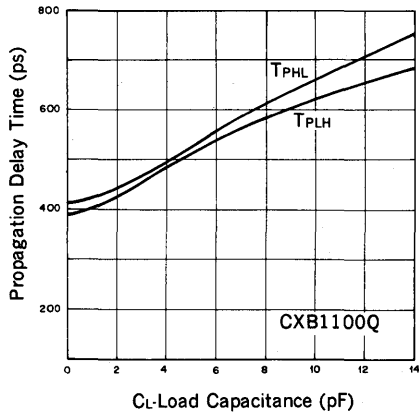


Figure 12. Transition Characteristics vs. Load Capacitance

## 5. Handling Precautions

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

- ① Equalize potentials of terminals when transporting or storing.
- ② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.
- ③ Prepare an environment that does not generate static electricity.

One method is keeping relative humidity in the work room to about 50%.

### Operator

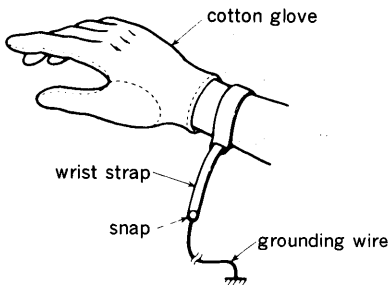
#### (1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

#### (2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

#### example of grounding band

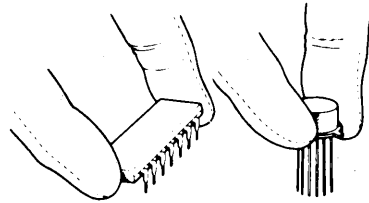


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

#### (3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

#### holding of semiconductor device



DIP type

can type

### Equipment and tools

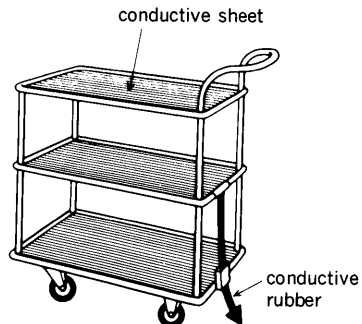
#### (1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

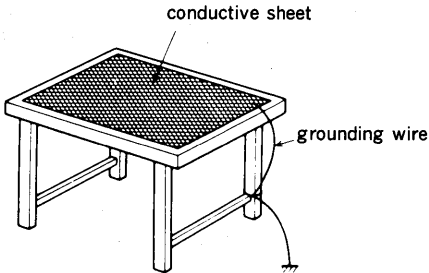
#### grounding of carrier



**(2) Grounding of work table**

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

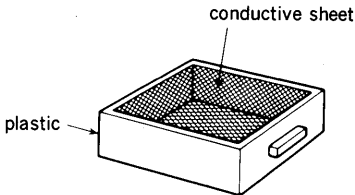
**grounding of work table**



**(3) Semiconductor device case**

Use a metal case, or an antistatic plastic case (lined with conductive sheet).

**plastic case for semiconductor devices**



**(4) Insertion of semiconductor device**

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

**(5) Operation in energized state**

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

**(6) Other points of caution**

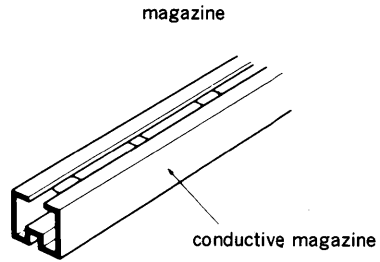
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

**Transporting, storing and packaging methods**

**(1) Magazine**

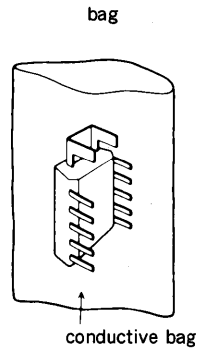
Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



**(2) Bag**

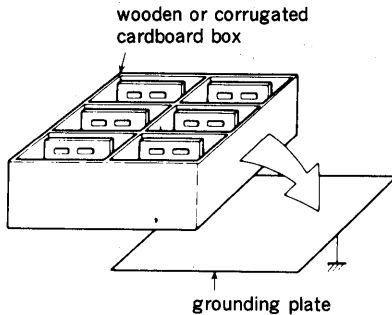
Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



### (3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

#### handling of delivery box



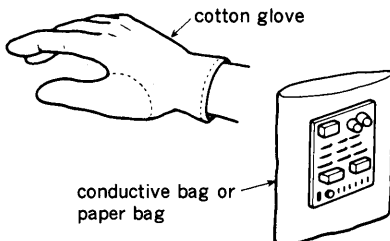
### (4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

### (5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

#### handling of mounted substrate



### Soldering operation

#### (1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than  $10M\Omega$  (DC 500V) after five minutes from energizing.

#### (2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

#### (3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

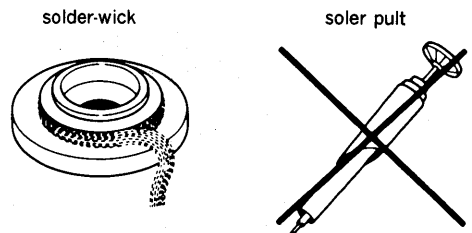
#### (4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

#### (5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

#### solder remover



### (6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.



### 3) Mounting method

#### Soldering and solderability

##### (1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2".

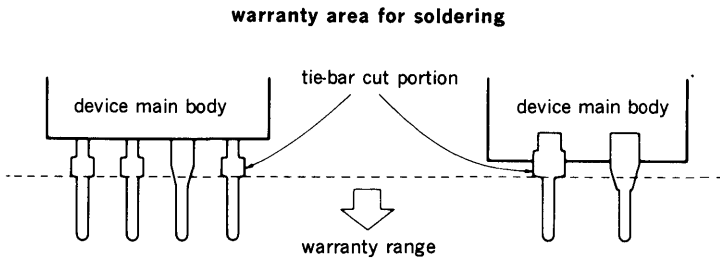
An abstract of this standard follows:

- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to  $230^{\circ}\text{C}\pm 5^{\circ}\text{C}$  for  $5\pm 1$  seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

##### (2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.



#### Resistance to soldering heat

##### (1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for  $10\pm 1$  seconds in a solder bath of  $260^{\circ}\text{C}\pm 5^{\circ}\text{C}$ , or for  $3\pm 0.5$  seconds in a solder bath of  $350^{\circ}\text{C}\pm 10^{\circ}\text{C}$ , for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be  $260^{\circ}\text{C}\pm 5^{\circ}\text{C}$ . To solder by soldering iron temperature should be  $350^{\circ}\text{C}\pm 10^{\circ}\text{C}$ .

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at  $260^{\circ}\text{C}\pm 5^{\circ}\text{C}$ . The distance between the device main body and solder bath is 1.6 mm.

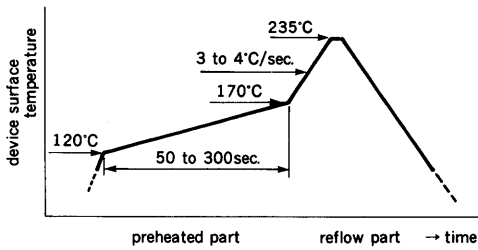
**(2) Resistance to soldering heat when mounting infrared reflow.**

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



## 6. Quality Assurance and Reliability

### The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

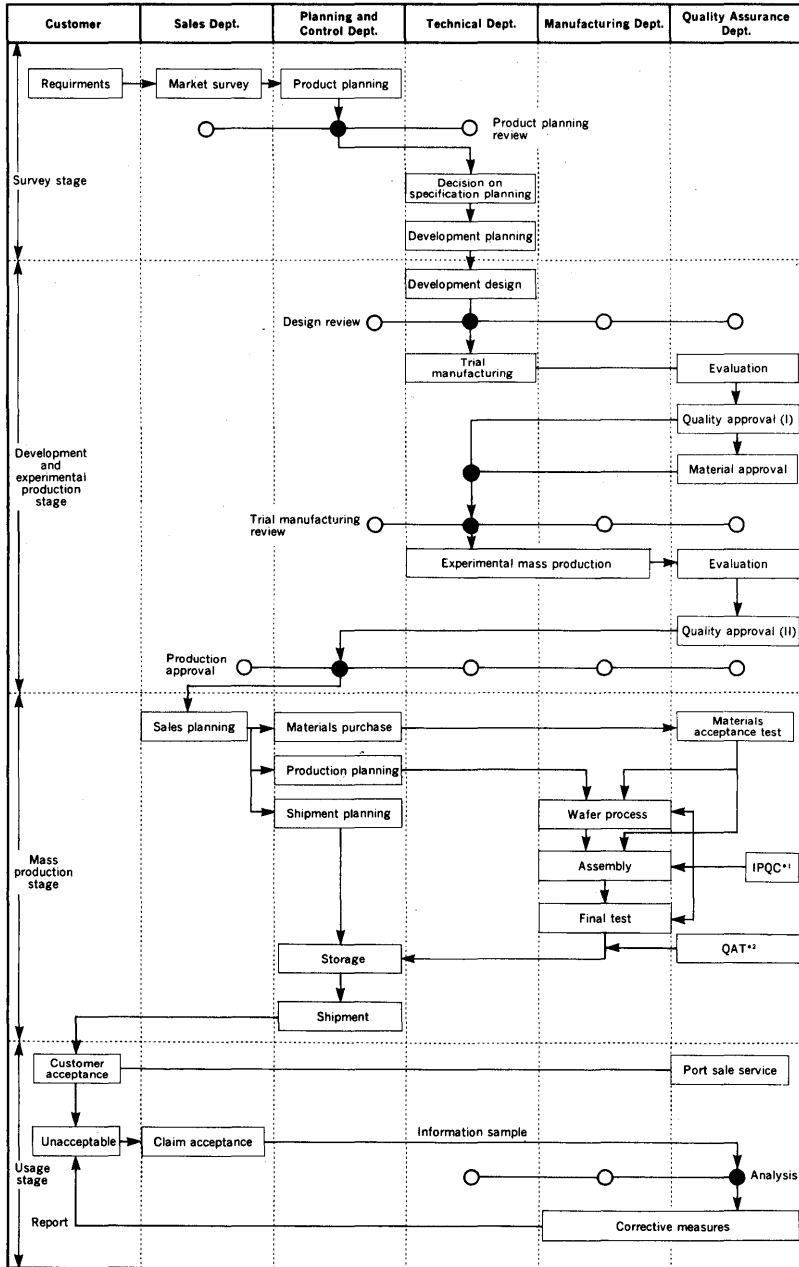
To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing,

orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

# Quality assurance system of semiconductor products



\*1. IPQC: In Process Quality Control  
 \*2. QAT: Quality Assurance Test

**Quality assurance criteria and reliability test criteria**

**1) Quality assurance in shipping**

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-

inspected" at the final fabrication stage, thus ensuring no defective items. This sampling inspection is done in accordance with MIL-STD-105D.

**2) Reliability**

The reliability test is done, periodically, to confirm reliability level.

**Periodic Reliability Test**

Item		Testing time	LTPD
<b>Electrical Characteristics Test</b>		In order to know the initial quality level, some types are selected and tested again.	
<b>Life Test</b>	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
<b>Environmental Test</b>	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
<b>Mechanical Test</b>	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
<b>Other Tests</b>	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

\*These tests are selected by sampling standard.

**LTPD**: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

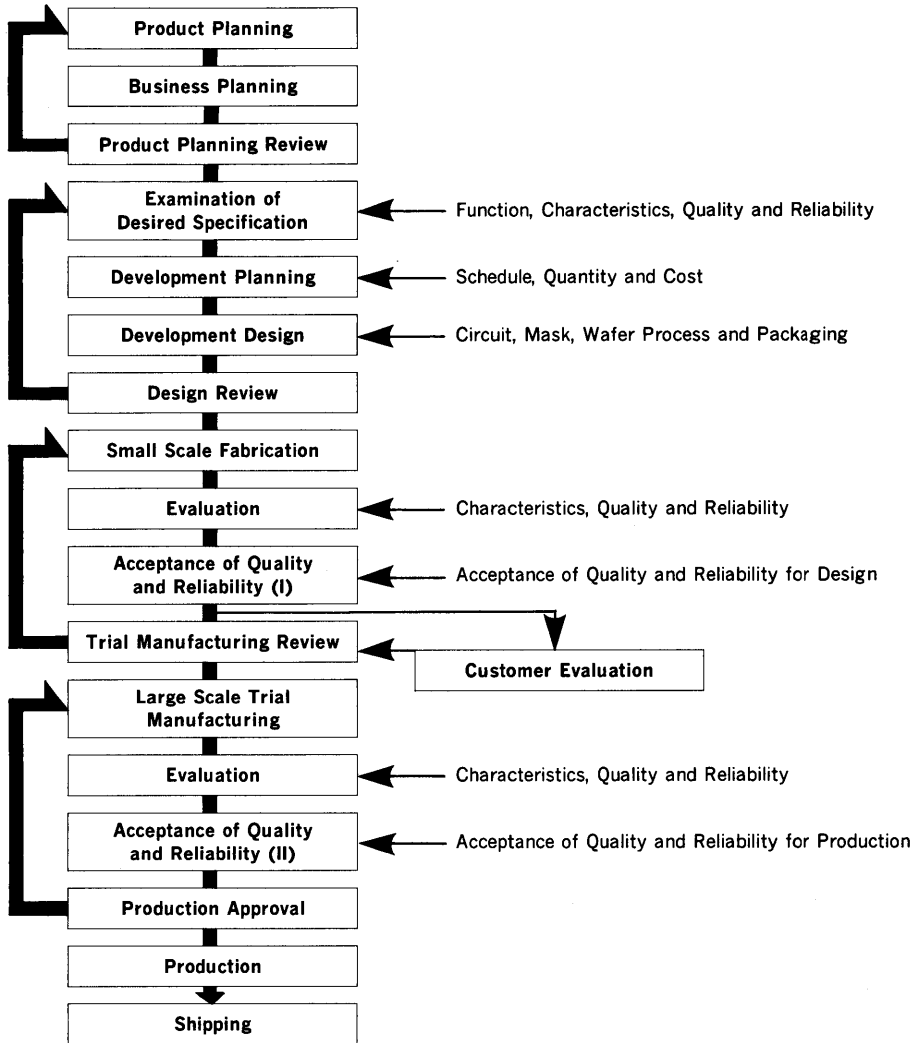
## Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta= -65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta= -65°C to +150°C		100c	10%
Heat shock	Ta= -65°C to +150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

LTPD: Lot Tolerance Percent Defective

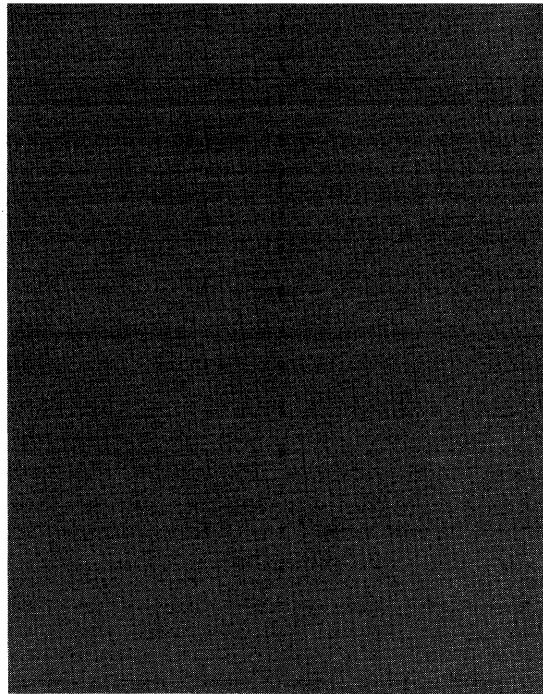
## Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.

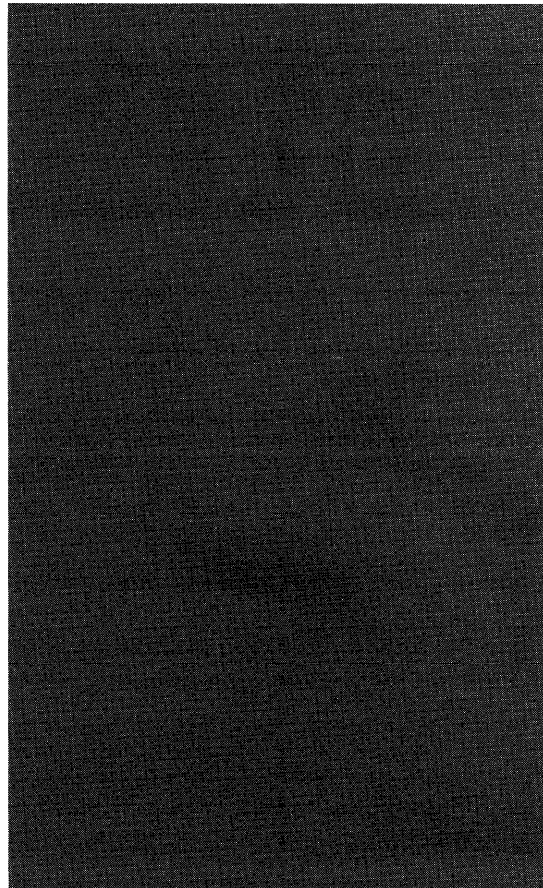








## **Family DC Specification**



**Family DC Specification**

<b>Family DC Specification</b>	<b>Page</b>
1. Absolute Maximum Ratings	3-3
2. Recommended Operating Conditions	3-3
3. DC Electrical Characteristics	3-4

# Family DC Specification

DC characteristics specified in this section apply to each member of the Family unless otherwise specified on the individual device data sheet.

Each member of the Family is electrically compatible with existing ECL 100K.

## Absolute Maximum Ratings

$V_{CC}=V_{CCA}=0V$

Characteristic	Symbol	Rating	Unit
Supply voltage	$V_{EE}$	+0.3 to -7	V
Input voltage	$V_I$	0 to -4	V
Output current — Continuous — Surge	$I_O$	0 to 50 0 to 100	mA
Operating case temperature	$T_C$	-55 to 125	°C
Storage temperature	$T_{stg}$	-65 to 150	°C

Stresses greater than these conditions may cause permanent damage to the devices or affect their reliability.

Input terminal should not be connected to  $V_{EE}$  for logic LOW level. LOW voltage level is maintained with input pins left open.

## Recommended Operating Conditions

$V_{CC}=V_{CCA}=0V$

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_{EE}$	-4.2	-4.5	-4.8	V
Output termination to $V_{TT}=-2V$	$R_T$	45	50		$\Omega$
Operating case temperature	$T_C$	0		85	°C

The devices should be operated under these conditions, beyond which the parametric values are not specified.

### DC Electrical Characteristics

$V_{EE} = -4.5V$  ( $V_{CC} = V_{CCA} = GND$ ,  $T_c = 0^\circ C$  to  $85^\circ C$ ,  $R_L = 50\Omega$  to  $V_{TT} = -2V$ )

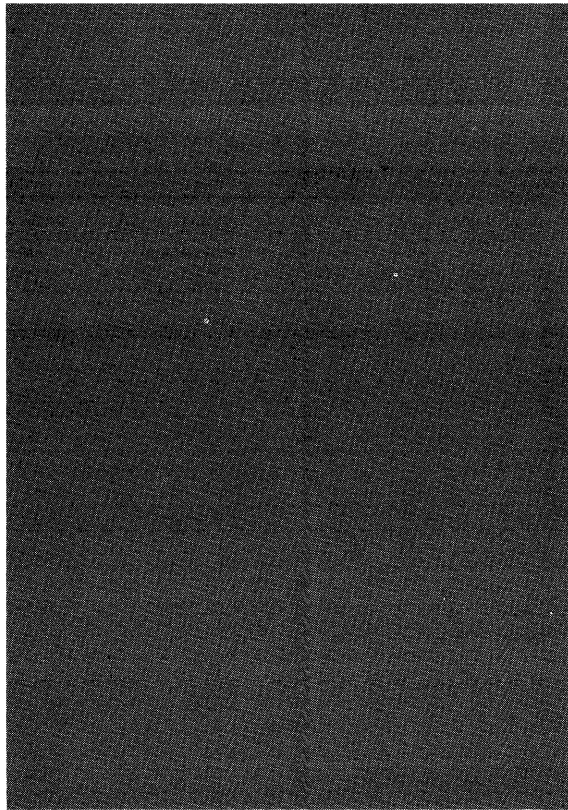
Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	Output HIGH voltage	$V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min)	-1025	-880	-810	mV
$V_{OL}$	Output LOW voltage		-1810	-1700	-1620	mV
$V_{IH}$	Input HIGH voltage		-1165		-810	mV
$V_{IL}$	Input LOW voltage		-1810		-1475	mV
$I_{IH}$	Input HIGH current	$V_{IN} = V_{IH}$ (max)			230	$\mu A$
$V_{BB}$	Reference bias voltage		-1380	-1320	-1260	mV

$V_{EE} = -4.2V$  ( $V_{CC} = V_{CCA} = GND$ ,  $T_c = 0^\circ C$  to  $85^\circ C$ ,  $R_L = 50\Omega$  to  $V_{TT} = -2V$ )

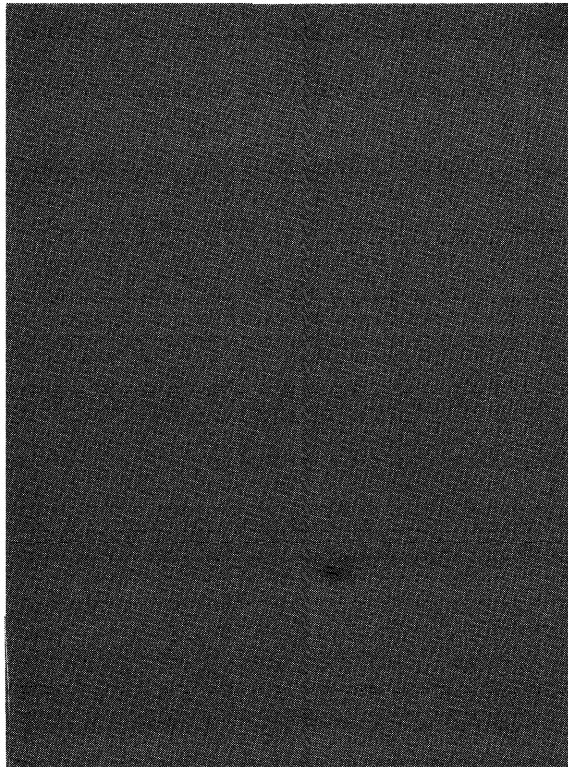
Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	Output HIGH voltage	$V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min)	-1020	-880	-810	mV
$V_{OL}$	Output LOW voltage		-1790	-1680	-1605	mV
$V_{IH}$	Input HIGH voltage		-1165		-810	mV
$V_{IL}$	Input LOW voltage		-1790		-1475	mV
$I_{IH}$	Input HIGH current	$V_{IN} = V_{IH}$ (max)			230	$\mu A$
$V_{BB}$	Reference bias voltage		-1380	-1320	-1260	mV

$V_{EE} = -4.8V$  ( $V_{CC} = V_{CCA} = GND$ ,  $T_c = 0^\circ C$  to  $85^\circ C$ ,  $R_L = 50\Omega$  to  $V_{TT} = -2V$ )

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	Output HIGH voltage	$V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min)	-1035	-880	-810	mV
$V_{OL}$	Output LOW voltage		-1840	-1730	-1620	mV
$V_{IH}$	Input HIGH voltage		-1165		-810	mV
$V_{IL}$	Input LOW voltage		-1840		-1475	mV
$I_{IH}$	Input HIGH current	$V_{IN} = V_{IH}$ (max)			230	$\mu A$
$V_{BB}$	Reference bias voltage		-1400	-1340	-1280	mV



## AC Test Circuit

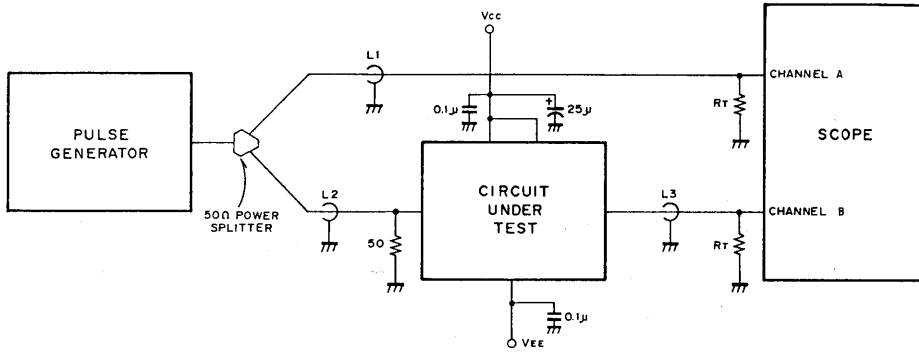


**AC Test Circuit**

<b>AC Test Circuit</b>	<b>Page</b>
1. Propagation Delay and Transition Time	4-3
2. Propagation Delay (Clock, Set, Reset), Transition Time, Data Setup/Hold Time and Release Time	4-4

# AC Test Circuit

## Propagation Delay and Transition Time



$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

$L1 = L2 + L3$  50Ω coaxial cables

$R_T = 50\Omega$  terminator

Complementary input is connected to  $V_{BB} = +0.68V$ .

All unused outputs are loaded with 50Ω to GND.

$C_L = \text{Fixture and stray capacitance} \leq 2pF$

Figure 1. AC Test Circuit

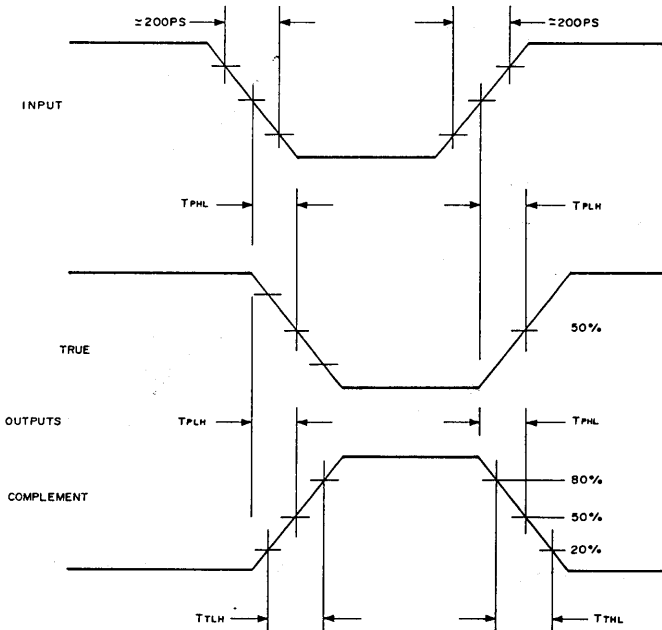
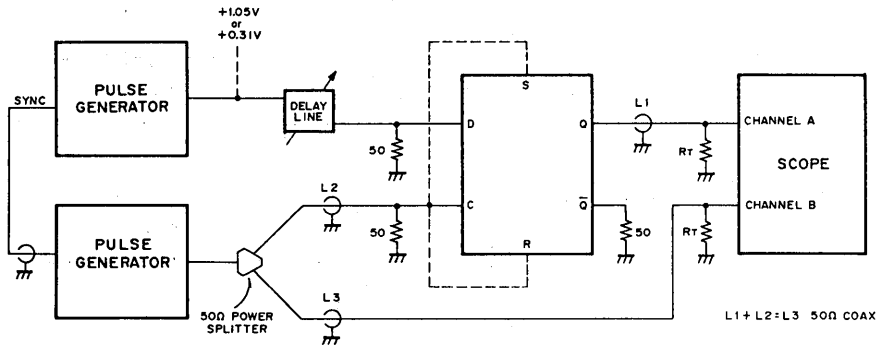
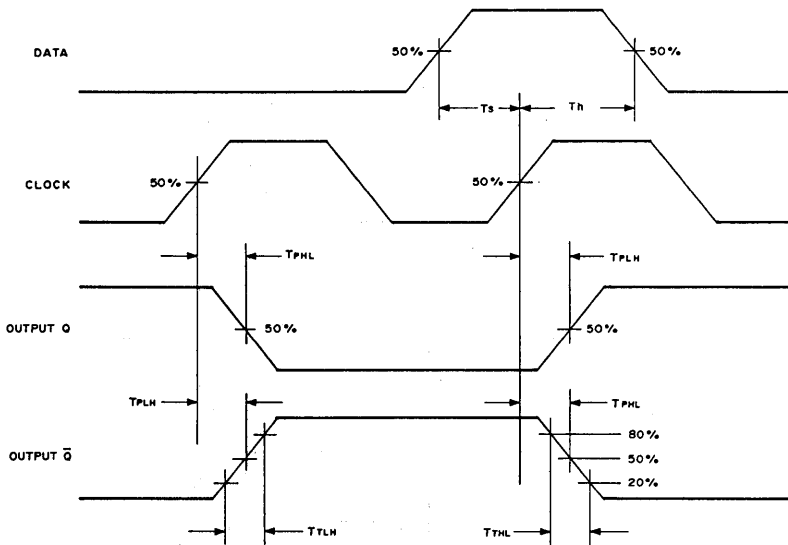


Figure 2. Propagation Delay and Transition time

**Propagation Delay (Clock, Set, Reset), Transition Time, Data Setup/Hold Time and Release Time**

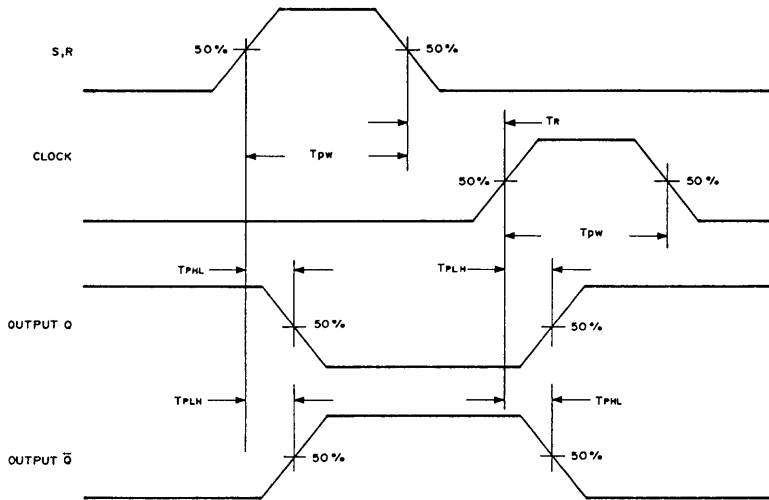


**Figure 3. AC Test Circuit (Flip-Flop, Latch)**



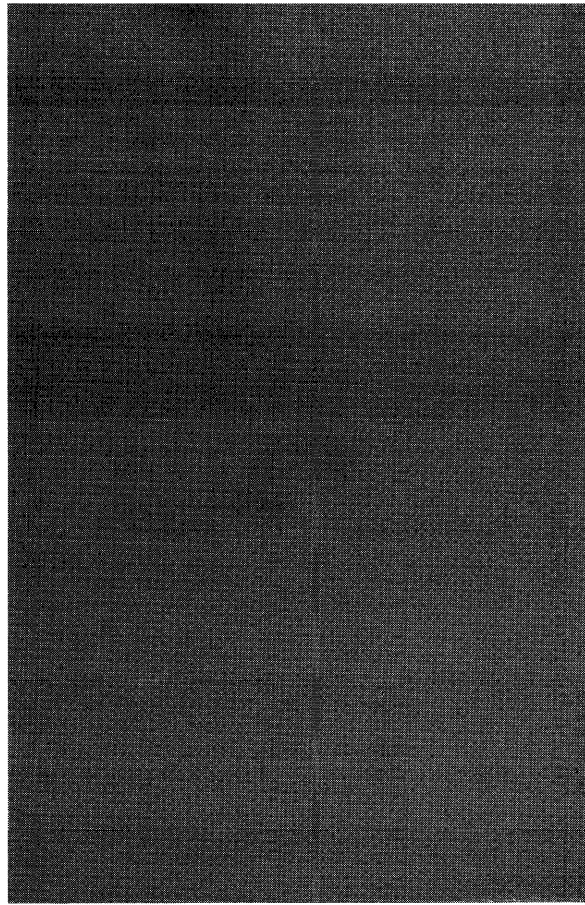
**Figure 4. Propagation Delay (Clock), Transition Time and Data Setup/Hold Time**



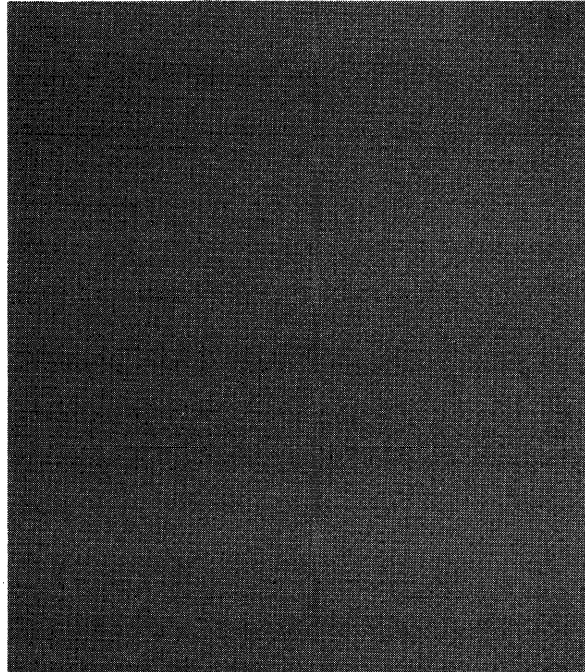


**Figure 5. Propagation Delay (Set, Reset) and Release Time**





**Data Sheets**





**Data Sheets**

	<b>Data Sheets</b>	<b>Page</b>
CXB1100Q	Quad 3-input OR/NOR Gate	5-4
CXB1101Q	Quad 3-input AND/NAND Gate	5-6
CXB1102Q	Quad EX-OR/NOR Gate	5-8
CXB1103Q	Quint Line Receiver with Differential I/O	5-10
CXB1104Q	Dual D Flip-Flop with Set, Reset and Differential I/O	5-12
CXB1105Q	Triple Fan-out Buffer with Common Enable and Differential Output	5-14
CXB1106Q	4-bit Ripple Down Counter with Enable and Reset	5-16
CXB1107Q	Decision Circuit with Differential I/O	5-18
CXB1108Q	Laser Driver	5-20
CXB1109Q	Quad D Flip-Flop with Master Reset and Differential I/O	5-24
CXB1110Q	16-Line to 1-Line Data Selector/Multiplexer	5-26
CXB1111Q	4-bit Look-Ahead Carry Generator	5-28
CXB1112Q	Phase Frequency Detector with Differential I/O	5-30
CXB1113Q	4-bit Multiplexer	5-32
CXB1114Q	4-bit Demultiplexer	5-38
CXB1115Q	Clock Distributor with Enable and 10 Differential Outputs	5-42
CXB1116Q	4-bit Ripple Counter with Enable and Reset	5-44
CXB1119Q	Programmable Delay Line/Duty Cycle Controller	5-46
CXB1130Q	9, 8, Dual 4-bit Multiplexer	5-52
CXB1131Q	9, 8, Dual 4-bit Demultiplexer	5-58
CXB1132Q	9, 8, Dual 4-bit Universal Shift Register	5-66
CXB1133Q	22, 15, 7 Stage Data Scrambler with Differential I/O	5-70
CXB1134Q	22, 15, 7 Stage Descrambler with Differential I/O	5-74
CXB1135Q	8 to 16-bit Serial Data Comparator	5-78
CXB1136Q	8-bit Universal Counter with Preset and Master Reset	5-82
CXB1137Q	8-bit Shift Matrix	5-86
CXB1138Q	4-bit Arithmetic Logic Unit (ALU)	5-90
CXB1139Q	Programmable Delay Line/Duty Cycle Controller	5-96
CXB1140Q	Hex 2: 1 Multiplexer with Latch	5-102
CXB1141Q	Hex 2: 1 Multiplexer with D-FF	5-106
CXB1142Q	Quad 4: 1 Multiplexer with Latch	5-110
CXB1143Q	Quad 4: 1 Multiplexer with D-FF	5-114
CXB1144Q	Dual 8: 1 Multiplexer with Latch	5-118
CXB1145Q	Dual 8: 1 Multiplexer with D-FF	5-122

**Quad 3-input OR/NOR Gate**

**Description**

The CXB1100Q is an ultra high speed monolithic ECL IC, which contains four 3-input OR/NOR gates.

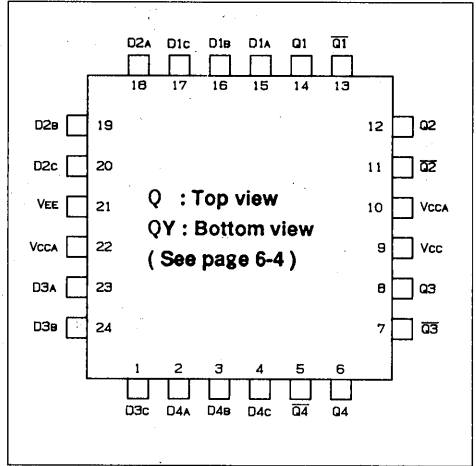
**Features**

- Typical AC characteristics
  - $T_{pd}=410ps$
  - $T_{TLH}=210ps$
  - $T_{THL}=160ps$
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential output

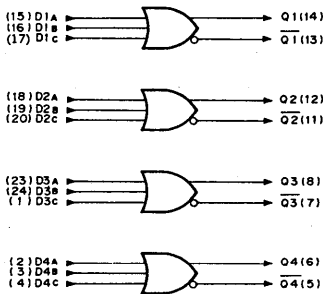
**Pin Names**

$D_{nA}, D_{nC}$	Data inputs
$Q_n, \overline{Q}_n$	Data outputs
Vcc	Circuit ground
VCCA	Circuit ground for outputs
VEE	Negative power supply

**Pin Assignment**



**Logic Symbol**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-127	-93	-65	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	Dn	Qn		300	410	520	ps	
	$T_{PHL}$				300	410	520		
Rise time	$T_{TLH}$			20% to 80%		210	270		
Fall time	$T_{THL}$					160	210		

Note: AC test circuit; See page 4-3.

**Quad 3-input AND/NAND Gate**

**Description**

The CXB1101Q is an ultra high speed monolithic ECL IC, which contains four 3-input AND/NAND gates.

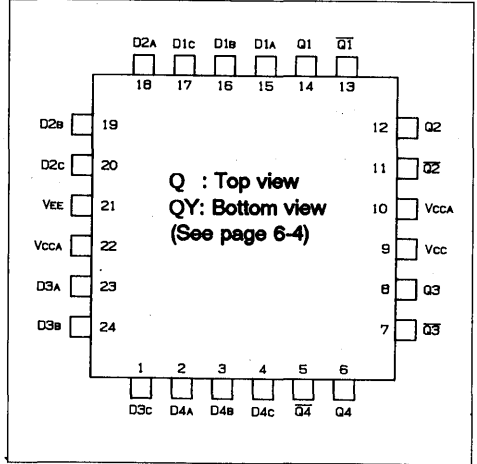
**Features**

- Typical AC characteristics
  - $T_{pd} = 490ps$
  - $T_{TLH} = 230ps$
  - $T_{THL} = 170ps$
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential output

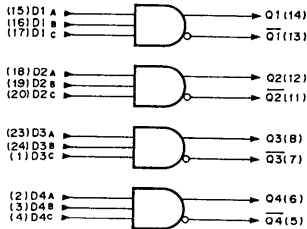
**Pin Names**

D <sub>nA-DnC</sub>	Data inputs
Q <sub>n</sub> , Q <sub><math>\bar{n}</math></sub>	Data outputs
V <sub>CC</sub>	Circuit ground
V <sub>CCA</sub>	Circuit ground for outputs
V <sub>EE</sub>	Negative power supply

**Pin Assignment**



**Logic Symbol**





**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-179	-131	-91	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	Dn	Qn		350	460	580	ps
	$T_{PHL}$				370	490	620	
Rise time	$T_{TLH}$			20% to 80%		230	290	
Fall time	$T_{THL}$					170	220	

Note: AC test circuit; See page 4-3.

## Quad Exclusive OR/NOR Gate

### Description

The CXB1102Q is an ultra high speed monolithic ECL IC, which contains four Exclusive OR/NOR gates.

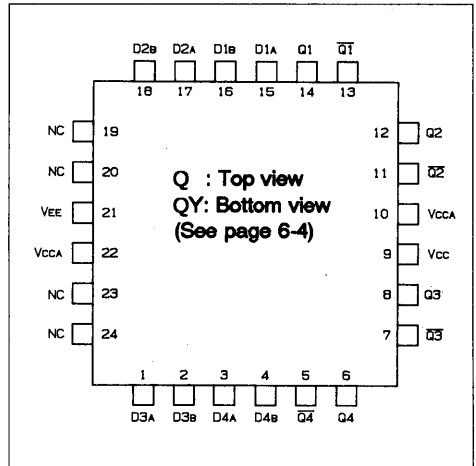
### Features

- Typical AC characteristics
  - $T_{pd} = 530\text{ps}$
  - $T_{TLH} = 220\text{ps}$
  - $T_{THL} = 170\text{ps}$
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential output

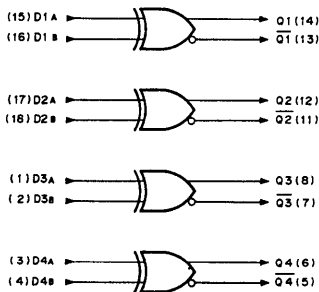
### Pin Names

- $D_{nA}, D_{nB}$  Data inputs
- $Q_n, \overline{Q}_n$  Data outputs
- $V_{CCA}$  Circuit ground for outputs
- $V_{EE}$  Negative power supply

### Pin Assignment



### Logic Symbol



### Truth Table

INPUT		OUTPUT	
$D_{nA}$	$D_{nB}$	$Q_n$	$\overline{Q}_n$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

Note: H; HIGH voltage level  
L; LOW voltage level

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-170	-125	-87	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	D <sub>nA</sub> , D <sub>nB</sub>	Q <sub>n</sub>		400	530	670	ps
	$T_{PHL}$				380	510	650	
Rise time	$T_{TLH}$			20% to 80%		220	280	
Fall time	$T_{THL}$					170	220	

Note: AC test circuit; See page 4-3.

**Quint Line Receiver with Differential I/O**

**Description**

The CXB1103Q is an ultra high speed monolithic ECL IC, which contains five differential line receivers with a built-in reference voltage supply ( $V_{BB}$ ). With  $V_{BB}$  tied to one of the input pins of each differential input pair, each gate can be used as a single input line receiver.

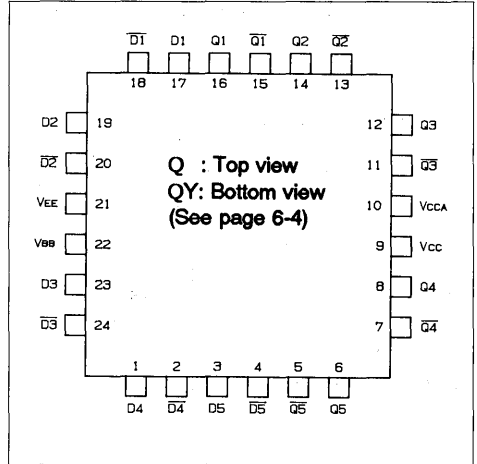
**Features**

- Typical AC characteristics
  - $T_{pd} = 430ps$
  - $T_{TLH} = 220ps$
  - $T_{THL} = 170ps$
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential I/O

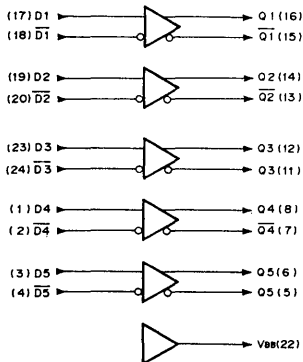
**Pin Names**

- $D_n, \overline{D}_n$  Data inputs
- $Q_n, \overline{Q}_n$  Data outputs
- $V_{BB}$  Reference voltage output
- $V_{CC}$  Circuit ground
- $V_{CCA}$  Circuit ground for outputs
- $V_{EE}$  Negative power supply

**Pin Assignment**



**Logic Symbol**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-154	-113	-79	mA
Min. differential input voltage*1	$V_{p-p}$			50		mVpp

Note: Other DC characteristics; See pages 3-3 and 3-4.

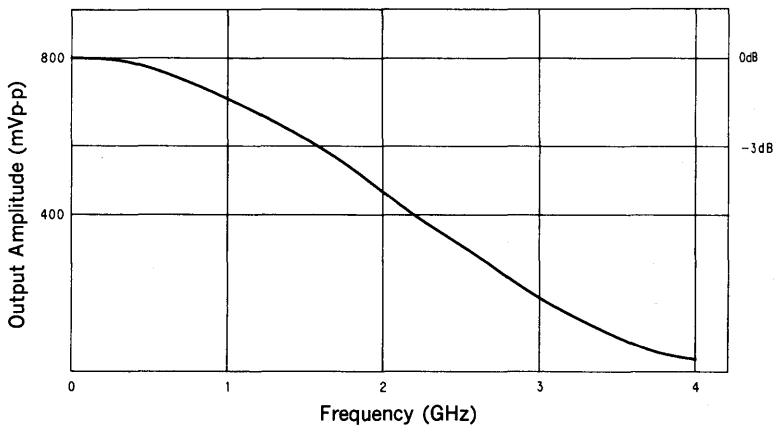
\*1: Minimum voltage required to obtain full logic swing on output

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit			
Propagation delay time	$T_{PLH}$	Dn	Qn		310	410	520	ps			
	$T_{PHL}$				320	430	540				
Gate-to-Gate skew	$T_{SGG}$								50	90	
Rise time	$T_{TLH}$					20% to 80%			220	280	
Fall time	$T_{THL}$				170		220				

Note: AC test circuit; See page 4-3.



**Figure 1. Frequency characteristics**

**Dual D Flip-Flop with Set, Reset and Differential I/O**

**Description**

The CXB1104Q is an ultra high speed monolithic ECL IC, which contains two D type Flip-Flops with separate direct Set (Sn) and Reset (Rn). Data inputs have differential input pins Dn and  $\overline{Dn}$ . Separate clock inputs also have differential input pins Cn and  $\overline{Cn}$ . Built-in reference voltage is provided at V<sub>BB</sub> pin to facilitate single input operation.

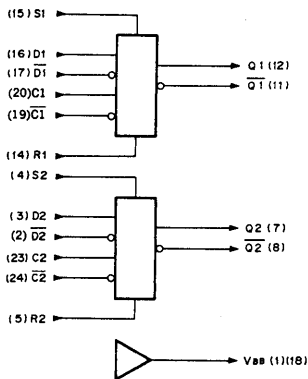
**Features**

- Typical clock rate up to 3.2GHz
- Differential Data and Clock inputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

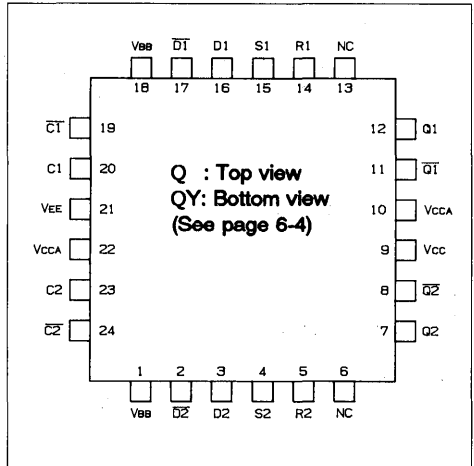
**Pin Names**

- |                     |                                      |
|---------------------|--------------------------------------|
| Dn, $\overline{Dn}$ | Data inputs                          |
| Qn, $\overline{Qn}$ | Data outputs                         |
| Sn                  | Direct Set inputs                    |
| Rn                  | Direct Reset inputs                  |
| Cn, $\overline{Cn}$ | Clock inputs (positive edge trigger) |
| V <sub>BB</sub>     | Reference voltage output             |
| V <sub>CC</sub>     | Circuit ground                       |
| V <sub>CCA</sub>    | Circuit ground for outputs           |
| V <sub>EE</sub>     | Negative power supply                |

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Input				Output	
S	R	C	D	Q	$\overline{Q}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	X	X
L	L	J	L	L	H
L	L	J	H	H	L

Note: H ; HIGH voltage Level  
 L ; LOW voltage Level  
 X ; Don't care  
 J ; Positive transition edge

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-146	-107	-74	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	Cn	Qn		450	610	810	ps
	$T_{PHL}$				460	630	830	
	$T_{PLH}$	Sn			600	760	990	
	$T_{PHL}$				600	760	990	
	$T_{PLH}$	Rn			570	720	940	
	$T_{PHL}$				580	730	950	
Set up time	$T_s$	Dn, Cn			40			
Hold time	$T_h$	Cn, Dn			240			
Release time	$T_r$	Sn, Cn			310			
		Rn, Cn			320			
Min. Pulse width	$T_{PW}$	Sn			270			
		Rn			270			
Max. Clock frequency	$f_{max}$	Cn			2.4	3.2		GHz
Rise time	$T_{TLH}$	Cn	Qn	20% to 80%		200	280	ps
Fall time	$T_{THL}$					160	240	

Note: AC test circuit; See pages 4-4 and 4-5.

## Triple Fan-Out Buffer with Common Enable and Differential Output

### Description

The CXB1105Q is an ultra high speed monolithic ECL IC, which contains three Line Drivers. Each driver has two pairs of differential output pins ( $Q_{nA}$ ,  $Q_{nB}$ ,  $\overline{Q}_{nA}$ ,  $\overline{Q}_{nB}$ ).

Enable ( $\overline{E}$ ) input enables data (D1-D3) input. With D1-D3 maintained LOW,  $\overline{E}$  acts as a fan-out buffer with six differential outputs.

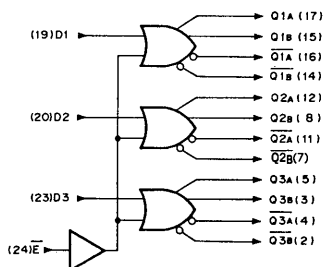
### Features

- Typical propagation delay time:  
 $T_{pd}=620ps$  (Dn to  $Q_{nA}$ ,  $Q_{nB}$ )
- Small time skew: 50ps ( $\overline{E}$  to  $Q_{nA}$ ,  $Q_{nB}$ )
- Enable input
- Six differential fan-out capability
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential output.

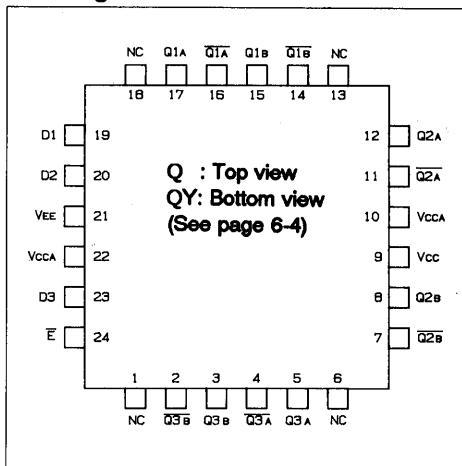
### Pin Names

Dn	Data inputs
$Q_{nA}$ , $\overline{Q}_{nA}$ , $Q_{nB}$ , $\overline{Q}_{nB}$	Data outputs
$\overline{E}$	Data enable (active LOW)
VCC	Circuit ground
VCCA	Circuit ground for outputs
VEE	Negative power supply

### Logic Symbol



### Pin Assignment



### Truth Table

Input		Output	
$\overline{E}$	Dn	Qn	$\overline{Q}_n$
L	L	L	H
L	H	H	L
H	X	H	L

Note: H; HIGH voltage level  
L; LOW voltage level  
X; Don't care



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-164	-120	-84	mA

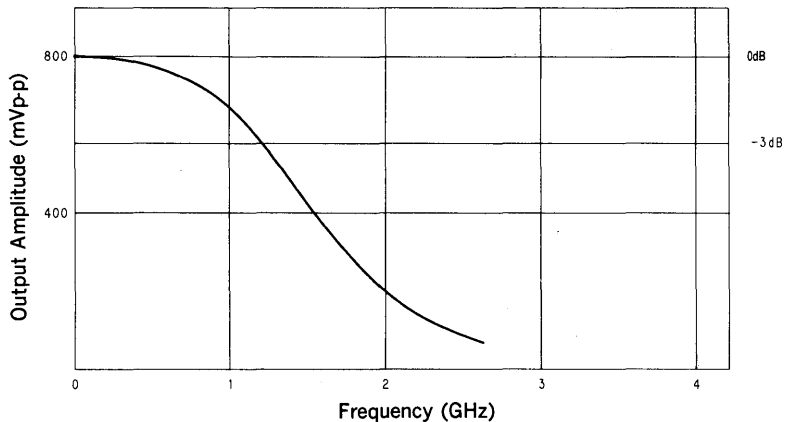
Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	Dn	QnA, QnB		470	620	790	ps
	$T_{PHL}$				440	590	750	
	$T_{PLH}$	$\bar{E}$			500	660	840	
	$T_{PHL}$				500	630	800	
Gate-to-Gate time skew	$T_{SG-G}$	$\bar{E}$				50		
Rise time	$T_{TLH}$	Dn, $\bar{E}$		20% to 80%		250	320	
Fall time	$T_{THL}$					220	280	

Note: AC test circuit; See page 4-3.



**Figure 1. Frequency characteristics**

**4-bit Ripple Down Counter with Enable and Reset**

**Description**

The CXB1106Q is an ECL ultra high speed monolithic Binary Ripple Down Counter with divide-by-2/4/8/16 outputs.

Clock input has differential input pins C and  $\bar{C}$ . Built-in reference voltage  $V_{BB}$  is provided to facilitate the use of single clock input. Enable input (E) enables clock input. Common direct reset input (R) resets the counter and separate Set inputs (Sn) set each stage of the counter.

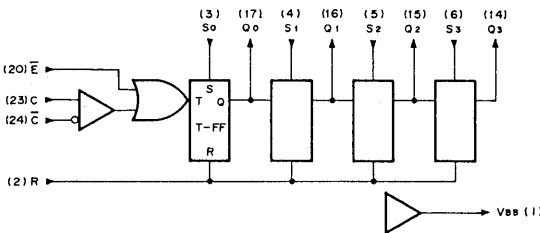
**Features**

- Typical clock rate up to 3.0GHz
- Differential Clock input (positive edge trigger)
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

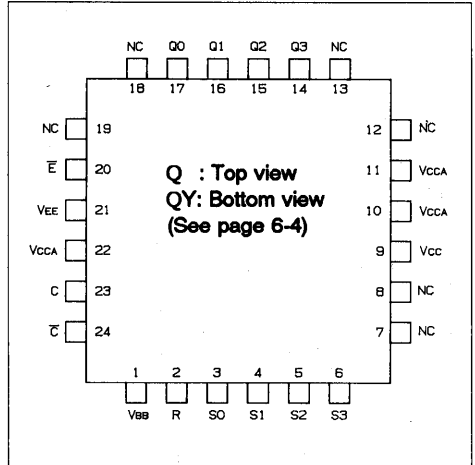
**Pin Names**

- C,  $\bar{C}$  Clock inputs
- Qn Data outputs
- Sn Direct set inputs
- R Common direct Reset input
- $\bar{E}$  Clock enable (active LOW)
- $V_{BB}$  Reference voltage output
- $V_{CC}$  Circuit ground
- $V_{CCA}$  Circuit ground for outputs
- $V_{EE}$  Negative power supply

**Logic Symbol**



**Pin Assignment**



**Sequential Truth Table**

Inputs							Outputs			
R	$\bar{E}$	S0	S1	S2	S3	C	Q0	Q1	Q2	Q3
H	X	L	L	L	L	X	L	L	L	L
H	H	L	L	L	L	X	L	L	L	L
L	H	L	L	L	L	X	L	L	L	L
L	L	L	L	L	L	J	H	H	H	H
L	L	L	L	L	L	J	L	H	H	H
L	L	L	L	L	L	J	L	L	H	H
L	L	L	L	L	L	J	H	H	L	H
L	L	L	L	L	L	J	L	H	L	H
L	L	L	L	L	L	J	H	L	L	H
L	L	L	L	L	L	J	L	L	L	H
L	L	L	L	L	L	J	H	H	H	L
L	L	L	L	L	L	J	L	H	H	L
L	L	L	L	L	L	J	H	L	H	L
L	L	L	L	L	L	J	L	H	L	L
L	L	L	L	L	L	J	H	L	L	L
L	L	L	L	L	L	J	L	H	L	L
L	L	L	L	L	L	J	H	L	L	L
L	L	L	L	L	L	J	L	L	L	L
L	L	L	L	L	L	J	H	L	L	L
L	L	L	L	L	L	J	L	L	L	L
L	X	L	L	H	H	X	L	L	H	H
L	X	L	H	L	H	X	L	H	H	H
L	J	L	L	L	L	L	H	L	H	H
L	J	L	L	L	L	L	L	L	H	H
H	X	H	H	H	H	X	X	X	X	X

Note: H; HIGH voltage level  
 L; LOW voltage level  
 X; Don't care

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-202	-148	-103	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	C, $\bar{E}$	Q0		540	870	1100	ps	
	$T_{PHL}$				550	880	1110		
	$T_{PLH}$		Q1		710	1040	1270		
	$T_{PHL}$				720	1050	1280		
	$T_{PLH}$		Q2		830	1160	1390		
	$T_{PHL}$				840	1170	1400		
	$T_{PLH}$		Q3		1140	1470	1700		
	$T_{PHL}$				1150	1480	1710		
	$T_{PLH}$		Sn		Qn	560	810		1130
	$T_{PHL}$		R			640	890		1180
Release time	$T_R$	S0, C	Q0		160			ps	
		S1, C	Q1		-20				
		S2, C	Q2		-230				
		S3, C	Q3		-450				
		R, C	Q0		430				
		$\bar{E}$ , C			170				
Min. Pulse width	$T_{PW}$	Sn	Qn		330			ps	
		R			390				
Max. Clock frequency	$f_{MAX}$				2.4	3.0		GHz	
Rise time	$T_{TLH}$	C	Qn	20% to 80%		270	320	ps	
Fall time	$T_{THL}$					220	270		

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

**Decision Circuit with Differential I/O**

**Description**

The CXB1107Q is an ECL ultra high speed monolithic Decision Circuit, which contains a D Flip-Flop with High Gain Slicer at the input stage.

Differential data input is amplified by the High Gain Slicer and stored in the D Flip-Flop at the positive transition of the Clock. The stored data is held at Q and  $\bar{Q}$  pins until the next positive transition of the Clock occurs. The Clock input has differential input pins C and  $\bar{C}$ . Built-in reference voltage is provided at  $V_{BB}$  pins to facilitate the use of single input operation.

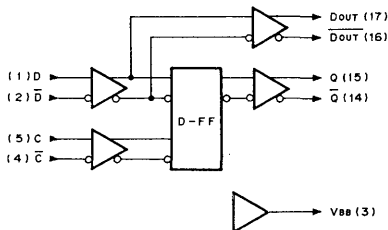
**Features**

- Typical AC characteristics: Clock rate up to 3.2GHz  
Clock rate up to 2.3GHz at an input level of 50mV
- Differential Data and Clock inputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

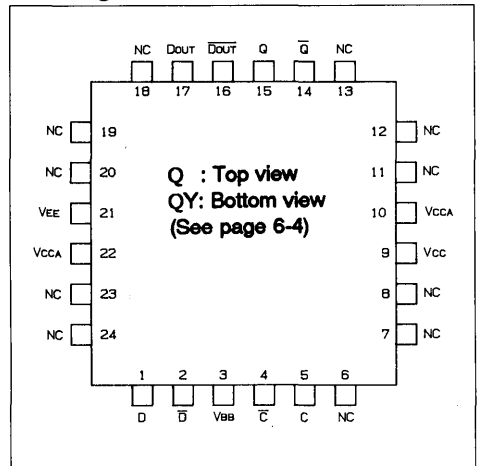
**Pin Names**

- D,  $\bar{D}$  Data input
- C,  $\bar{C}$  Clock inputs (positive edge trigger)
- Q,  $\bar{Q}$  Data output
- DOUT,  $\bar{DOUT}$  Buffered input data outputs
- $V_{BB}$  Reference voltage output
- VCC Circuit ground
- VCCA Circuit ground for outputs
- $V_{EE}$  Negative power supply

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Input		Output	
D	C	Q	DOUT
L	L	Hold	L
H	L	Hold	H
L	$\uparrow$	L	L
H	$\uparrow$	H	H
L	H	Hold	L
H	H	Hold	H

Note: H; HIGH voltage level  
L; LOW voltage level  
 $\uparrow$ ; Positive transition edge  
Hold; Means no-change in the output

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-116	-85	-59	mA
Input voltage range	$V_{IN}$		-2.0	-1.3	-0.5	V
Min. Decision voltage	$V_D$	$f_{CLOCK} = 1.8GHz$			50	mVpp

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	C	Q		460	610	770	ps
	$T_{PHL}$				440	590	750	
	$T_{PLH}$	D	DOUT		420	570	730	
	$T_{PHL}$				400	550	710	
Set up time	$T_S$	D, C	Q		220			GHz
Hold time	$T_H$	C, D			120			
Max. Clock frequency	$f_{MAX}$	D	Q	$V_{in} = 50mV_{pp}$	1.8	2.3		GHz
				$V_{in} = 800mV_{pp}$	2.6	3.2		
Rise time	$T_{TLH}$	C	Q	20% to 80%		220	280	ps
Fall time	$T_{THL}$					170	220	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Laser Driver

Description

The CXB1108Q is an ultra high speed monolithic Laser Driver/Current Switch Circuit with ECL input level.

Open collector output is provided at the output pin and has a capability of driving peak-to-peak current of 60mA up to a data rate of 2Gbps (NRZ). AMP input controls the peak-to-peak current amplitude, and BIAS input sets a current bias level. Open collector output  $I_{OUT}$  sinks current of  $2 \times I_{AMP} + I_B$ . Data input has differential input pins ( $V_{IN}$  and  $\overline{V}_{IN}$ ). Built-in reference voltage is provided at  $V_{BB}$  pin to facilitate the use of single input operation.

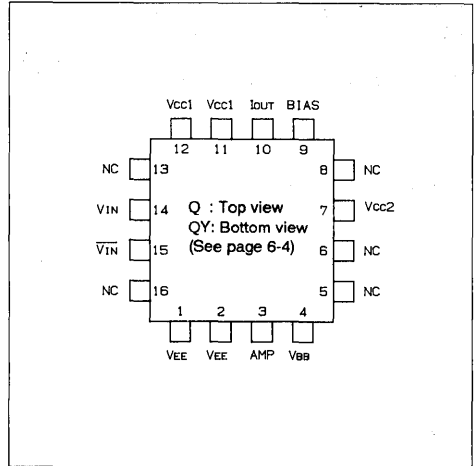
Features

- Typical data rate up to 2.0Gbps (NRZ)
- Differential Data input
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible Input level

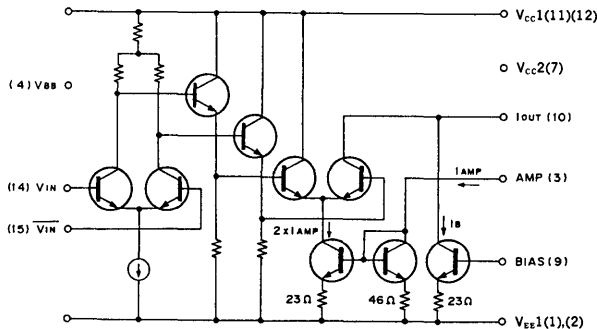
Pin Names

- $V_{IN}, \overline{V}_{IN}$  Data input
- $I_{OUT}$  Current output
- AMP Current amplitude control input
- BIAS Bias Current control input
- $V_{BB}$  Reference voltage output
- $V_{CC1}$  Circuit ground
- $V_{EE}$  Negative power supply
- $V_{CC2}$  Reference voltage generation circuit ground

Pin Assignment



Circuit Diagram



**DC Characteristics**
 $V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC1} = V_{CC2} = GND$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_L = 10\Omega$  to  $V_{CC1}$ 

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$	$V_{IN} = H$ , $\bar{V}_{IN} = L$ , $I_{OUT} = 100mA$ , $I_{AMP} = 25mA$	-224	-164	-114	mA
Output Current	$I_{OUT}$		0		120	mA
		$I_{AMP} = 0$ $V_{AMP} = V_{EE}$	0		60	
		$I_B = 0$ $V_{BIAS} = V_{EE}$	0		60	
Input voltage range	$V_{IN}$		-2.0		-0.5	V
Reference bias voltage	$V_{BB}$		-1380	-1320	-1160	mV

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**
 $V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC1} = V_{CC2} = GND$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ 

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Max. Data rate	$f_{DMAX}$	$V_{IN}$	$I_{OUT}$	NRZ	1.7	2.0		Gbps
Rise time	$T_{TLH}$			20% to 80%		200	240	ps
Fall time	$T_{THL}$					200	240	

Note: AC test circuit; See page 4-3.

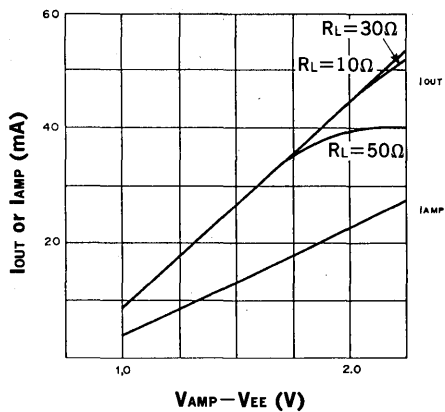


Figure 1.  $V_{AMP} - V_{EE}$  vs  $I_{out}$   
(BIAS=Open)

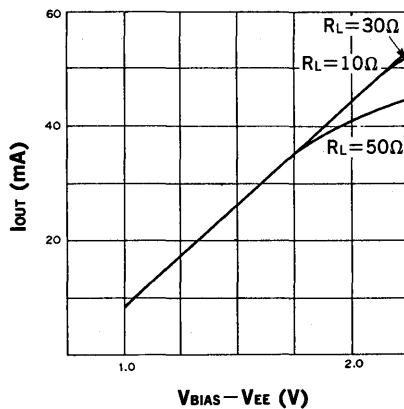


Figure 2.  $V_{BIAS} - V_{EE}$  vs  $I_{out}$   
(AMP=Open)

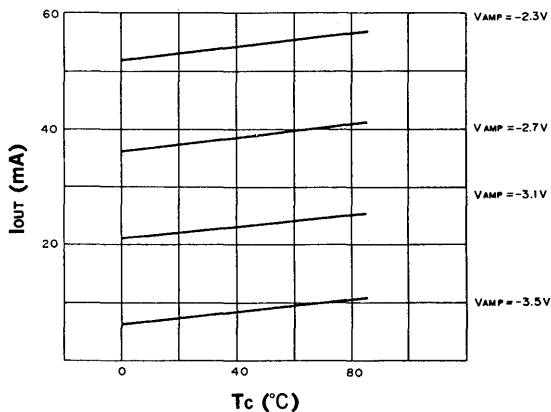


Figure 3.  $T_c$  vs  $I_{out}$





**Quad D Flip-Flop with Master Reset and Differential I/O**

**Description**

The CXB1109Q is an ultra high speed monolithic ECL IC, which contains four D Flip-Flop's.

Positive edge of Master Clock CA and CB triggers the Flip-Flop's, and Master Reset (MR) resets them. Data inputs have differential input pins Dn and  $\overline{Dn}$ . Built-in reference voltage is provided at VBB pin to facilitate the use of single input operation.

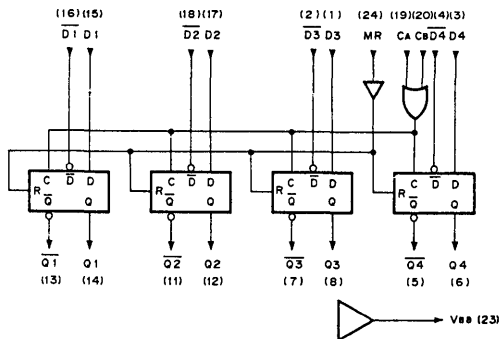
**Features**

- Typical data rate up to 3.1GHz
- Differential data inputs and outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

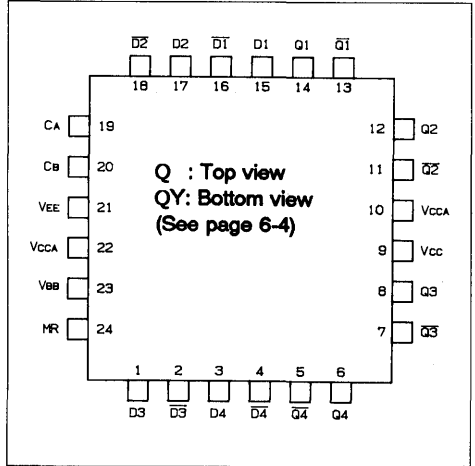
**Pin Names**

- Dn,  $\overline{Dn}$  Data inputs
- CA, CB Common Clock inputs (positive edge trigger)
- MR Direct Master Reset input
- Qn,  $\overline{Qn}$  Data outputs
- VBB Reference voltage output
- VCC Circuit ground
- VCCA Circuit ground for outputs
- VEE Negative power supply

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Input			Output			
MR	CA	CB	Q1	Q2	Q3	Q4
H	X	X	L	L	L	L
L	┌	L	D1	D2	D3	D4
L	L	┌	D1	D2	D3	D4
L	┌	┌	D1	D2	D3	D4

Note: H; HIGH voltage level  
 L; LOW voltage level  
 X; Don't care  
 ┌; Positive transition edge

**DC Characteristics**

$$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C$$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-204	-150	-105	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation delay time	$T_{PLH}$	$C_A, C_B$	Qn		560	710	890	ps		
	$T_{PHL}$				560	710	890			
	$T_{PLH}$	MR			510	790	990			
	$T_{PHL}$				520	800	1000			
Set up time	$T_S$	$D_n \rightarrow C_A, C_B$				150				
Hold time	$T_H$	$C_A, C_B \rightarrow D_n$				250				
Min. Pulse width	$T_{PW}$	MR				430				
Release time	$T_R$	$MR \rightarrow C_A, C_B$				500				
Max. Clock frequency	$f_{MAX}$			2.5	3.1		GHz			
Rise time	$T_{TLH}$	$C_A, C_B$		20% to 80%		210	260	ps		
Fall time	$T_{THL}$					180	230			

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

**16-Line to 1-Line Data Selector/Multiplexer**

**Description**

The CXB1110Q is an ultra high speed monolithic ECL 16-Line to 1-Line Data Selector/Multiplexer.

The IC select 1 out of 16 inputs for the output. The data present at inputs (In) is selected and sent to the output (Z) in accordance with four bit Select inputs (Sn).

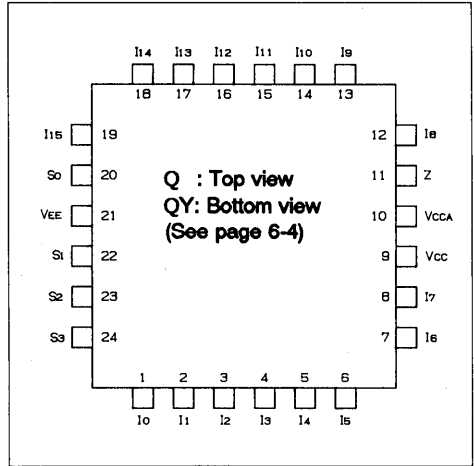
**Features**

- Typical AC characteristics:  $T_{pd}=620ps$  (In)
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

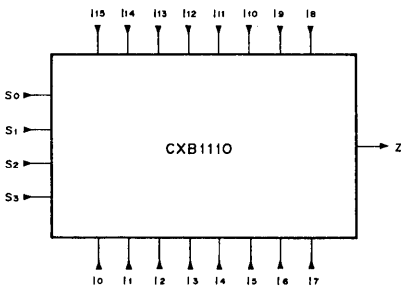
**Pin Names**

- In Data inputs
- Z Data output
- Sn Select inputs
- VCC Circuit ground
- VCCA Circuit ground for output
- VEE Negative power supply

**Pin Assignment**



**Logic Symbol**



**Truth Table**

Select Inputs				Output
S0	S1	S2	S3	Z
L	L	L	L	I0
H	L	L	L	I1
L	H	L	L	I2
H	H	L	L	I3
L	L	H	L	I4
H	L	H	L	I5
L	H	H	L	I6
H	H	H	L	I7
L	L	L	H	I8
H	L	L	H	I9
L	H	L	H	I10
H	H	L	H	I11
L	L	H	H	I12
H	L	H	H	I13
L	H	H	H	I14
H	H	H	H	I15

Note: H; HIGH voltage level  
L; LOW voltage level

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-204	-150	-105	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

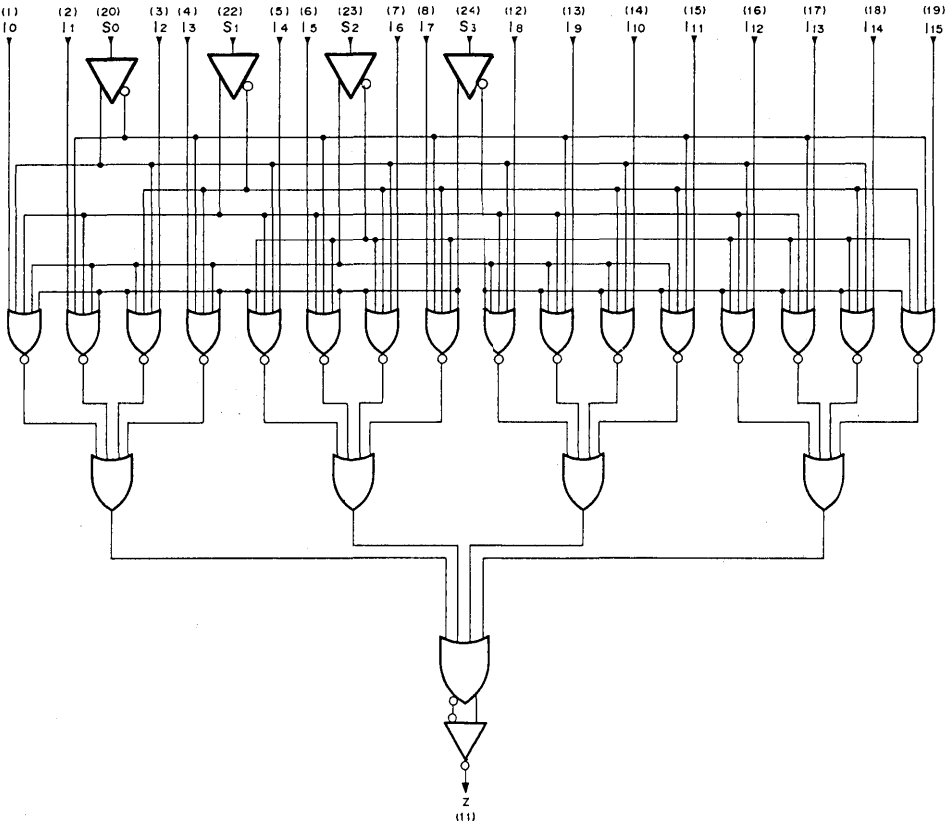
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_C = 0^\circ C \text{ to } +85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T <sub>PLH</sub>	In	Zn		460	610	770	ps
	T <sub>PHL</sub>				470	620	780	
	T <sub>PLH</sub>	Sn			680	830	990	
	T <sub>PHL</sub>				1010	1170	1330	
Rise time	T <sub>TLH</sub>	In, Sn		20% to 80%		270	340	
Fall time	T <sub>THL</sub>					180	230	

Note: AC test circuit; See page 4-3.

**Logic Diagram**



**4-bit Look-Ahead Carry Generator**

**Description**

The CXB1111Q is an ultra high speed monolithic ECL 4bit Look-Ahead Carry Generator.

When used with the CXB1138Q (4-bit ALU), this IC functions as an ultra fast second order or higher look ahead.

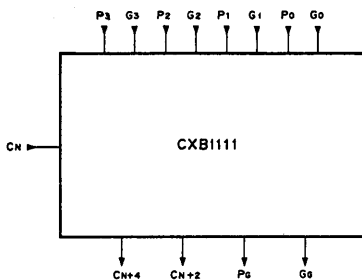
**Features**

- Typical AC characteristics:  $T_{pd}=700ps$
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

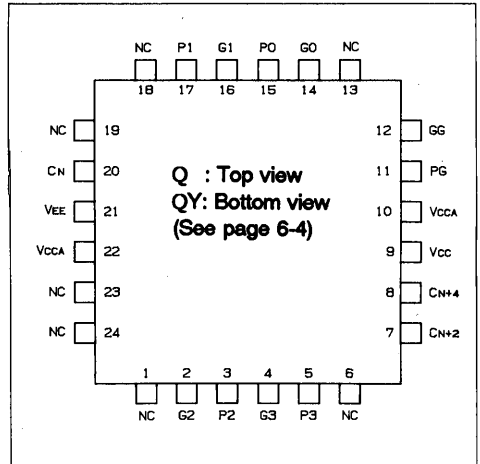
**Pin Names**

- CN Carry input
- P<sub>n</sub> Carry Propagate inputs
- G<sub>n</sub> Carry Generate inputs
- C<sub>N+2</sub>, C<sub>N+4</sub> Carry outputs
- P<sub>G</sub> Group carry Propagate output
- G<sub>G</sub> Group carry Generate output
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative power supply

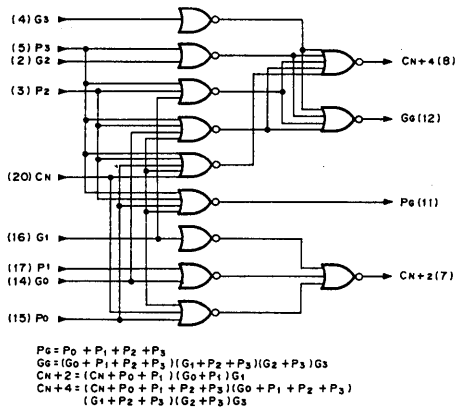
**Logic Symbol**



**Pin Assignment**



**Logic Diagram**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-170	-125	-87	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	$P_3$	$C_{N+4}$		520	690	880	ps
	$T_{PHL}$				480	640	810	
	$T_{PLH}$	$P_1$	$C_{N+2}$		530	700	890	
	$T_{PHL}$				530	680	850	
	$T_{PLH}$		$G_G$		530	700	890	
	$T_{PHL}$				530	680	850	
	$T_{PLH}$		$P_G$		480	650	840	
	$T_{PHL}$				480	640	810	
Rise time	$T_{TLH}$	All Inputs	All Outputs	20% to 80%		310	390	
Fall time	$T_{THL}$					210	270	

Note: AC test circuit; See page 4-3.

**Phase Frequency Detector with Differential I/O**

**Description**

The CXB112Q is an ultra high speed monolithic ECL Phase Frequency Detector capable of 800MHz operation.

The IC detects the difference of both phase and frequency between the data present at two differential input pins, R and V. In combination with a voltage controlled oscillator, this IC is used in an application for Phase-Locked-Loop.

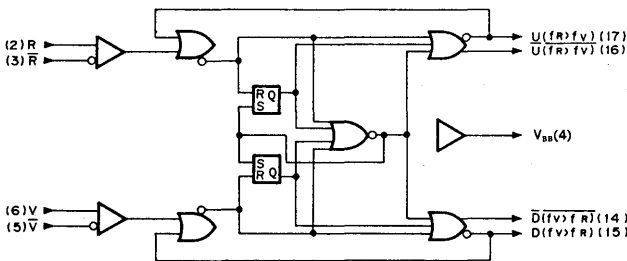
**Features**

- Typical Data rate up to 800MHz
- Differential inputs and outputs
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

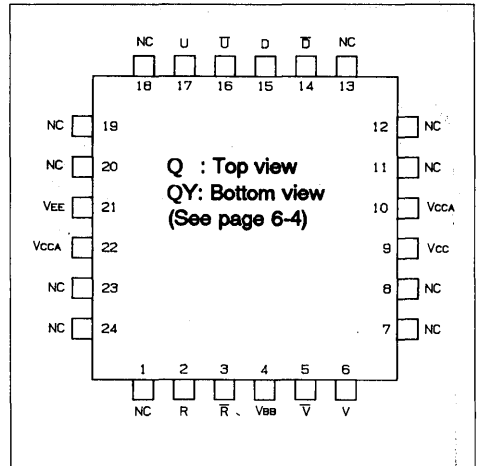
**Pin Names**

- V,  $\bar{V}$ , R,  $\bar{R}$  Data inputs
- U,  $\bar{U}$  Outputs ( $f_R > f_V$ )
- D,  $\bar{D}$  Outputs ( $f_V > f_R$ )
- V<sub>BB</sub> Reference voltage output
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative power supply

**Logic Diagram**



**Pin Assignment**



**Truth Table (for Test)**

Input		Output			
R	V	U	D	$\bar{U}$	$\bar{D}$
L	L	X	X	X	X
L	H	X	X	X	X
H	H	X	X	X	X
L	H	X	X	X	X
H	H	H	L	L	H
L	H	H	L	L	H
H	H	H	L	L	H
H	L	H	L	L	H
H	H	L	L	H	H
H	L	L	L	H	H
H	H	L	H	H	L
H	L	L	H	H	L
H	H	L	H	H	L
L	H	L	L	H	H
H	H	L	L	H	H

Note: H; HIGH voltage  
L; LOW voltage  
X; Don't care



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-134	-98	-68	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

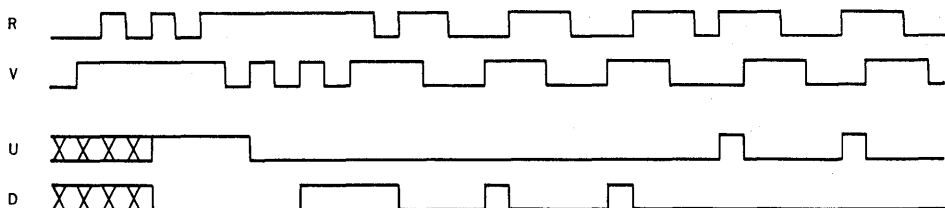
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	R	U		450	640	840	ps
	$T_{PHL}$				450	640	850	
	$T_{PLH}$		D		590	780	980	
	$T_{PHL}$				590	780	990	
	$T_{PLH}$	V	U		590	780	980	
	$T_{PHL}$				590	780	990	
	$T_{PLH}$		D		450	640	840	
	$T_{PHL}$				450	640	850	
Max. Clock frequency	$f_{MAX}$	R, V	U, D		600	800		MHz
Rise time	$T_{TLH}$	R, V	U, D	20% to 80%		340	430	ps
Fall time	$T_{THL}$					200	250	

Note: AC test circuit; See page 4-5.

**Timing Diagram**



## 4-bit Multiplexer

### Description

The CXB1113Q is an ultra high speed monolithic ECL Multiplexer which functions as a 4bit Parallel to Serial Converter.

The IC fetches 4bit parallel data present at the inputs (Dn) and converts them to serial data. Multiplexing is carried out in sequence from D0 to D3.

With Load Select (LS) input set to Low, internal load pulse loads parallel data. Start load pulse (ST), which starts multiplexing, has to be maintained High for at least 3 clock periods.

With LS set to High, External Load pulse ( $\overline{EL}$ ) loads parallel data.

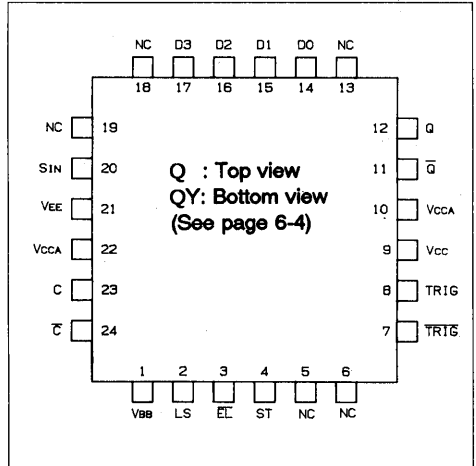
### Features

- Typical clock rate up to 1.8GHz
- Differential clock input and output
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

### Pin Names

Dn	Parallel Data inputs
LS	Load Select input
ST	Load Start input
$\overline{EL}$	External Load input
SIN	Serial data input
C, $\overline{C}$	Clock inputs (positive edge trigger)
Q, $\overline{Q}$	Multiplexed serial data outputs
TRIG, $\overline{TRIG}$	Trigger pulse outputs
V <sub>BB</sub>	Reference voltage output
V <sub>CC</sub>	Circuit ground
V <sub>CCA</sub>	Circuit ground for outputs
V <sub>EE</sub>	Negative power supply

### Pin Assignment

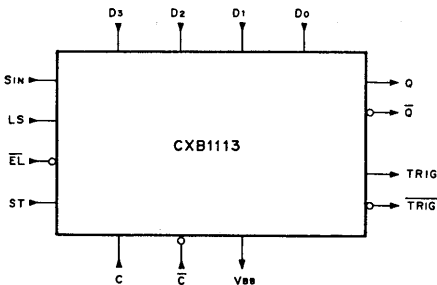


### Truth Table

LS	ST	$\overline{EL}$	C		
L	L	X	┘	Internal Load	Parallel data load, shift right
L	H	X	┘		Initialize (3clock period min.)
H	X	L	┘	External Load	Parallel data load
H	X	H	┘		Shift right, serial data output

Note: H; HIGH voltage level  
L; LOW voltage level  
X; Don't care  
┘; Positive transition edge

### Logic Symbol



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CCA} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } 85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-272	-200	-140	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

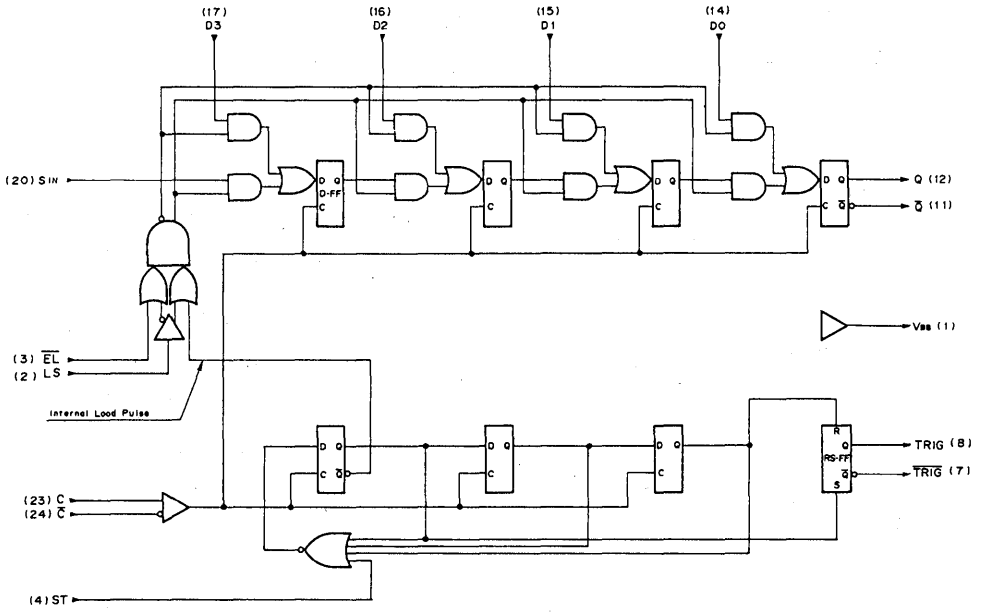
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } 85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$

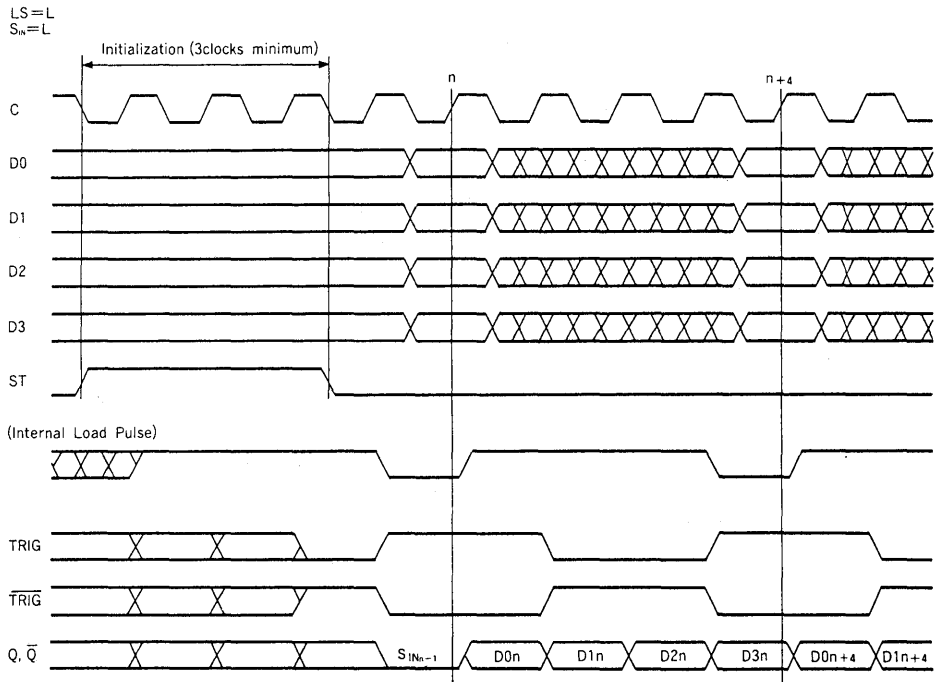
Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	T <sub>PLH</sub>	C	Q		900	1050	1220	ps	
	T <sub>PHL</sub>				900	1050	1220		
	T <sub>PLH</sub>		TRIG		560	710	880		
	T <sub>PHL</sub>				570	720	890		
Set up time	T <sub>s</sub>	D <sub>n</sub> , S <sub>IN</sub> → C	Q		-110				
		$\overline{EL}, C$			-170				
Hold time	T <sub>h</sub>	C → D <sub>n</sub> , S <sub>IN</sub>	Q		810				
		$\overline{EL}, C$			450				
Max. Clock frequency	f <sub>MAX</sub>	C	/	1.4	1.8		GHz		
Release time	T <sub>R</sub>	ST, C		-50					
Rise time	T <sub>TLH</sub>	C	Q, TRIG	20% to 80%		230	290	ps	
Fall time	T <sub>THL</sub>						170		220

Note: AC test circuit; See pages 4-4 and 4-5.

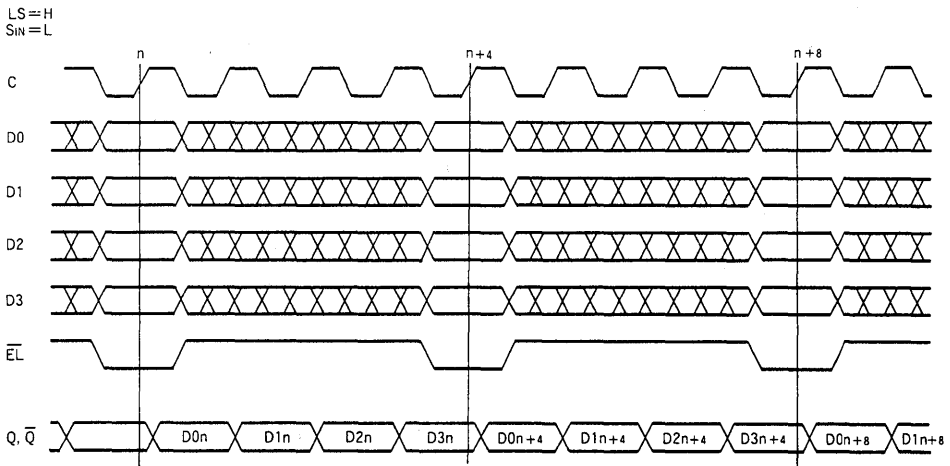
Logic Diagram



**Timing Diagram : Internal Load**



**Timing Diagram : External Load**



Typical Application

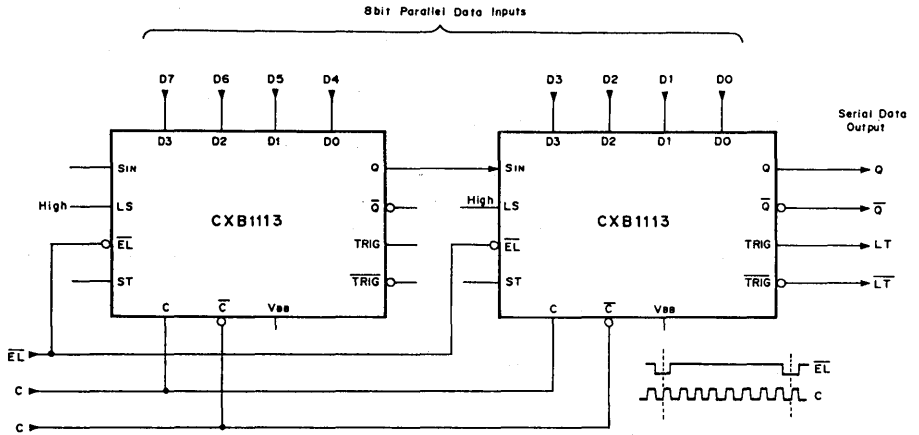


Figure 1. 8 to 1 Multiplexer/Parallel to Serial Converter

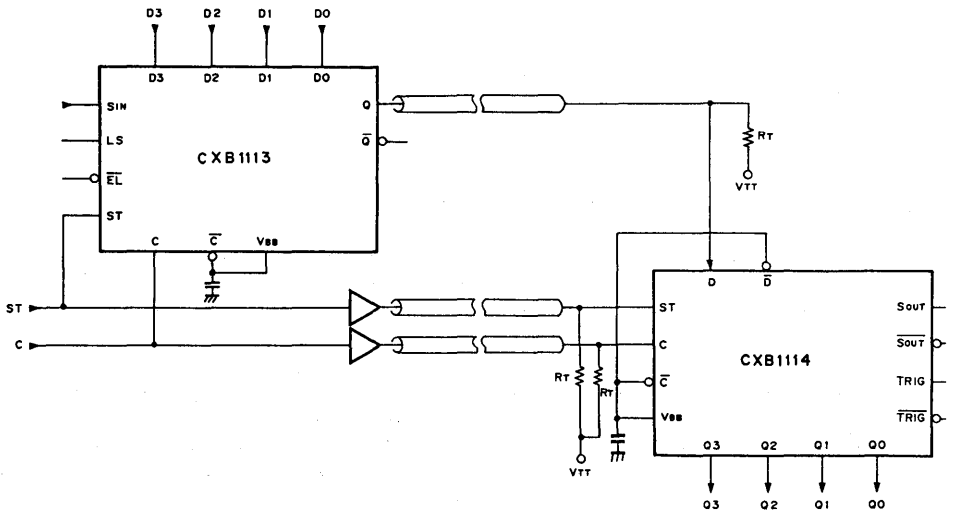


Figure 2. Serial Data Transmission



## 4-bit Demultiplexer

### Description

The CXB1114Q is an ultra High speed monolithic ECL Demultiplexer which functions as a 4-bit Serial to Parallel Converter.

The IC converts serial data into 4-bit demultiplexed parallel data. Load Start (ST) input, which starts the demultiplexing, has to be maintained High for at least 3 clock periods. Trigger (TRIG) pulse is provided for an external circuit to fetch the output data.

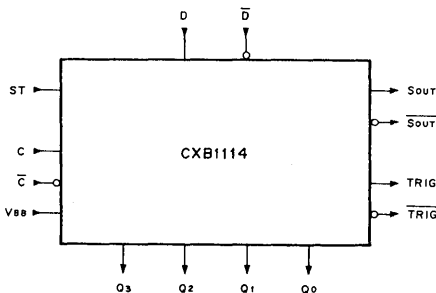
### Features

- Typical clock rate up to 2.1GHz
- Differential Clock and Data inputs
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

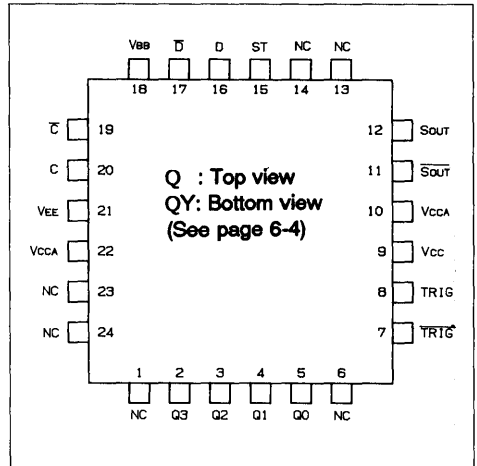
### Pin Names

- D,  $\bar{D}$  Serial Data inputs
- ST Load Start input
- C,  $\bar{C}$  Clock inputs (positive edge trigger)
- Qn Demultiplexed parallel data outputs
- TRIG,  $\overline{\text{TRIG}}$  Trigger pulse outputs
- SOUT,  $\overline{\text{SOUT}}$  Serial data outputs
- V<sub>BB</sub> Reference voltage output
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative power supply

### Logic Symbol



### Pin Assignment



### Truth Table

ST	C	Function
L	$\lrcorner$	Serial data input, parallel data out
H	$\lrcorner$	Initialize (3 clock period min.)

Note: H; HIGH voltage level  
 L; LOW voltage level  
 $\lrcorner$ ; Positive transition edge



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-297	-218	-152	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

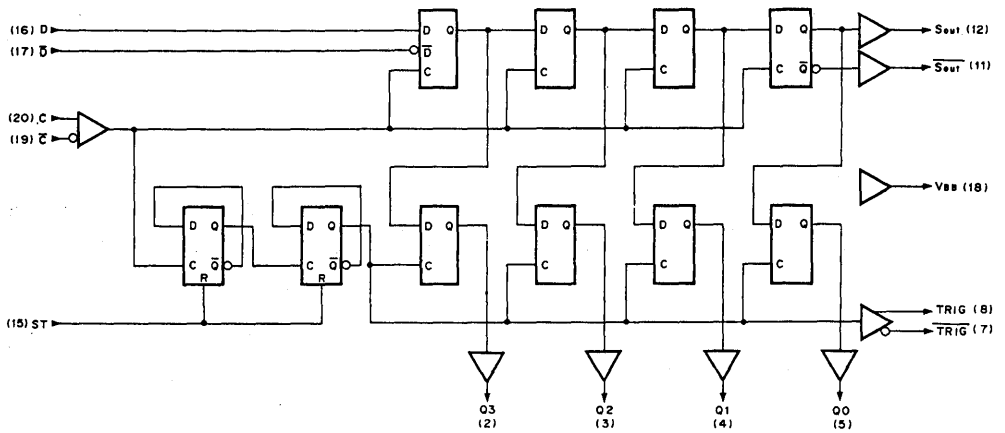
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

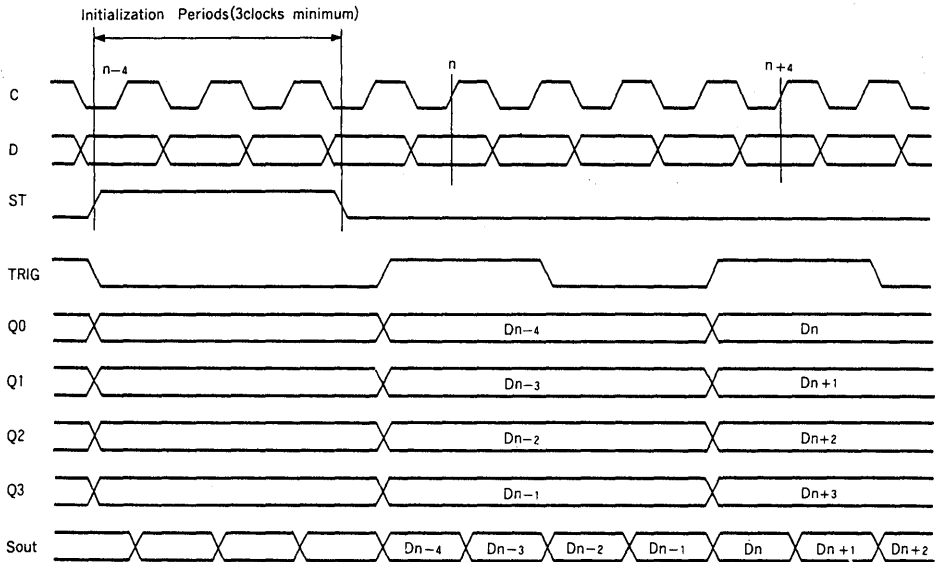
Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	C	Qn		1280	1430	1600	ps
	$T_{PHL}$				1270	1420	1590	
	$T_{PLH}$		SOUT		790	940	1110	
	$T_{PHL}$				820	970	1180	
	$T_{PLH}$		TRIG		1090	1260	1430	
	$T_{PHL}$				1150	1320	1490	
Set up time	$T_S$	D, C	Qn		-20			
Hold time	$T_H$	C, D			520			
Release time	$T_R$	R, C			320			
Min. Pulse width	$T_{PW}$	R			TRIG	330		
Max. Clock frequency	$f_{MAX}$		Qn		1.6	2.1		GHz
Rise time	$T_{TLH}$	C	Qn, SOUT TRIG	20% to 80%		400	500	ps
Fall time	$T_{THL}$					350	430	

Note: AC test circuit; See pages 4-4 and 4-5.

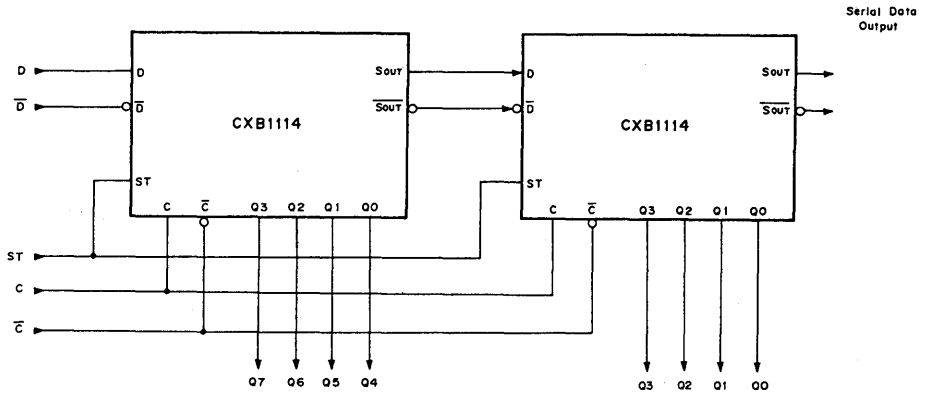
Logic Diagram



Timing Diagram



Typical Application 1 to 8 Demultiplexer/Serial to Parallel Converter



**Clock Distributor with Enable and 10 Differential Outputs**

**Description**

The CXB115 is an ultra high speed monolithic clock distributor, with low skew. Clock input has differential input pins C and  $\bar{C}$ . The input signal is fanned out to 10 differential outputs.

Enable inputs ( $\overline{EN1-EN3}$ ) control clock inputs. Built-in reference voltage is provided at  $V_{BB}$  pin to facilitate the use of single input operation.

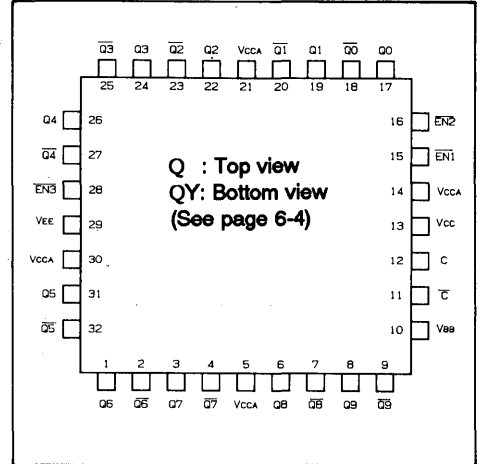
**Feature**

- Small gate-to-gate skew: 30ps
- Differential clock input and output
- Built-in reference voltage for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

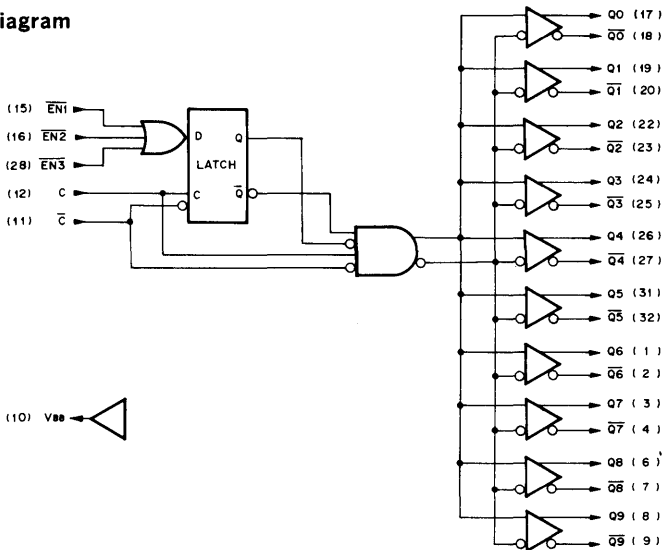
**Pin Names**

- C,  $\bar{C}$  Clock inputs
- $Q_n, \bar{Q}_n$  Clock outputs
- $\overline{EN}_n$  Clock enables (active LOW)
- $V_{BB}$  Reference voltage output
- Vcc Circuit ground
- VCCA Circuit ground for outputs
- VEE Negative power supply

**Pin Assignment**



**Block Diagram**



**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-244	-178	-124	mA

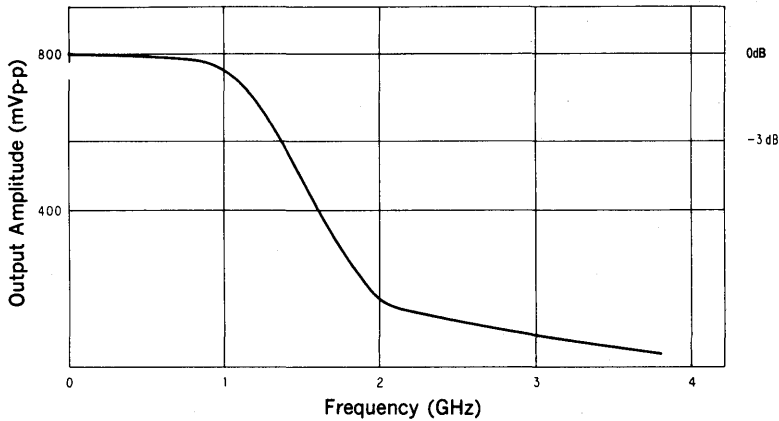
Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation Delay time	$T_{PLH}$	C	Qn		570	760	970	ps		
	$T_{PHL}$				570	760	970			
Gate-to-Gate Skew	$T_{SG-G}$								30	50
Set up time	$T_S$						150			
Hold time	$T_H$						260			
Rise time	$T_{TLH}$					20% to 80%			180	230
Fall time	$T_{THL}$									180

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.



**Figure 1. Frequency characteristics**



**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-213	-155	-108	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	C, $\bar{E}$	Q <sub>0</sub>		540	730	940	ps	
	$T_{PHL}$				540	730	940		
	$T_{PLH}$		Q <sub>1</sub>		670	900	1150		
	$T_{PHL}$				680	910	1160		
	$T_{PLH}$		Q <sub>2</sub>		810	1090	1390		
	$T_{PHL}$				830	1110	1410		
	$T_{PLH}$		Q <sub>3</sub>		930	1240	1580		
	$T_{PHL}$				940	1260	1600		
	$T_{PLH}$	S <sub>n</sub>	Q <sub>n</sub>		570	760	970		
	$T_{PHL}$	R			670	900	1150		
Release time	$T_R$	S <sub>0</sub> , C	Q <sub>0</sub>		160			ps	
		S <sub>1</sub> , C	Q <sub>1</sub>		-30				
		S <sub>2</sub> , C	Q <sub>2</sub>		-230				
		S <sub>3</sub> , C	Q <sub>3</sub>		-390				
		R, C	Q <sub>0</sub>		430				
		$\bar{E}$ , C			-10				
Min. Pulse width	$T_{PW}$	S <sub>n</sub>	Q <sub>n</sub>		330			ps	
		R			330				
Max. Clock Frequency	$f_{MAX}$	C	Q <sub>n</sub>	20% to 80%	2.4	3.0		GHz	
Rise time	$T_{TLH}$					200	250		ps
Fall time	$T_{THL}$					160	200		ps

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

**Programmable Delay Line/Duty Cycle Controller**

**Description**

The CXB1119Q is an ultra high speed monolithic ECL Delay Line/Duty Cycle Controller IC.

Four binary inputs,  $S_0$  to  $S_3$ , program the delay time from input  $D_{IN}$  to output  $Q_d$  in 16 steps.

A pulse with plus (long) duty cycle is provided at output  $Q_p$ , and a pulse with minus (short) duty cycle at output  $Q_m$ . The duty cycle is also controlled by the input data.

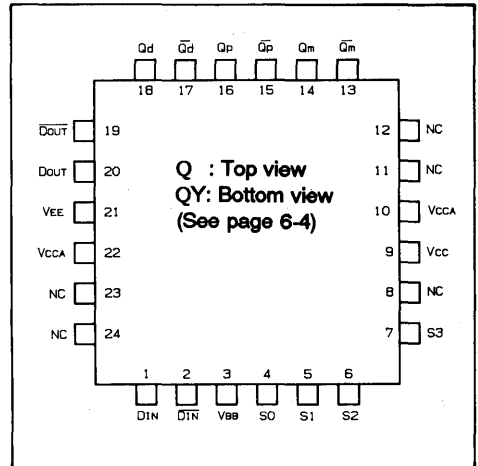
**Features**

- Programmable delay time: 870ps to 2240ps
- Programmable duty cycle
- Plus and minus duty cycle outputs
- Typical AC characteristics:  $T_{TLH}=185ps$   
 $T_{THL}=175ps$
- Differential data input and output
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

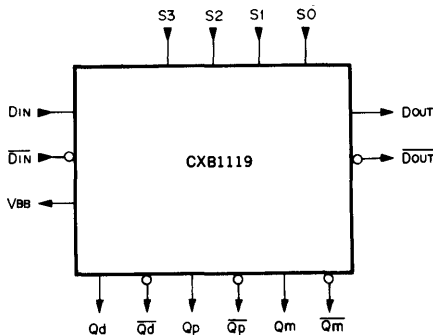
**Pin Names**

- $D_{IN}$ ,  $\overline{D}_{IN}$  Data inputs
- $S_n$  Digital data input
- $D_{OUT}$ ,  $\overline{D}_{OUT}$  Buffered data outputs
- $Q_d$ ,  $\overline{Q}_d$  Delayed data outputs
- $Q_p$ ,  $\overline{Q}_p$  Plus duty cycle outputs
- $Q_m$ ,  $\overline{Q}_m$  Minus duty cycle outputs
- $V_{BB}$  Reference voltage output
- $V_{CC}$  Circuit ground
- $V_{CCA}$  Circuit ground for outputs
- $V_{EE}$  Negative power supply

**Pin Assignment**



**Logic Symbol**





**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-325	-239	-167	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

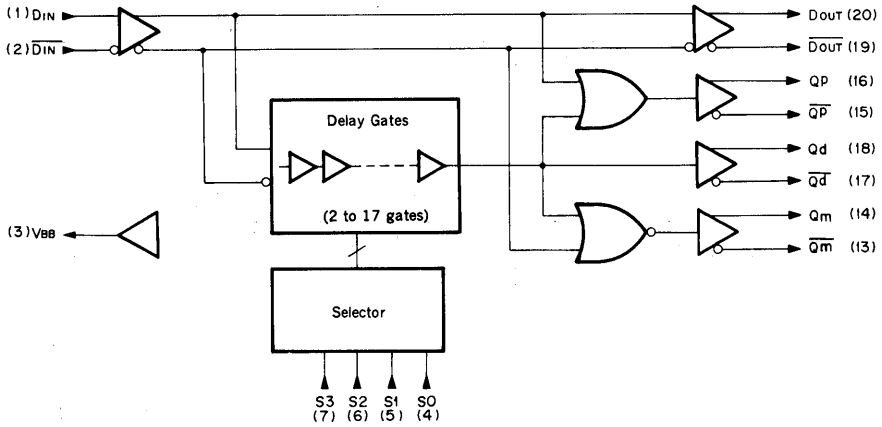
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation delay time	$T_{dLH}$	D <sub>IN</sub>	Q <sub>d</sub>	$S_0 - S_3 = LOW$	700	870	1090	ps		
	$T_{dHL}$				680	850	1065			
	$T_{dLH}$			$S_0 - S_3 = HIGH$	1570	2240	2800			
	$T_{dHL}$				1570	2240	2800			
	TO <sub>LH</sub>		D <sub>OUT</sub>		320	400	500			
					305	380	475			
	T <sub>pLH</sub>		Q <sub>p</sub>	D <sub>IN</sub>		$S_0 - S_3 = LOW$	472		590	740
						$S_0 - S_3 = HIGH$	444		555	695
Rise time	$T_{TLH}$	Q <sub>d</sub> , D <sub>OUT</sub> Q <sub>p</sub> , Q <sub>m</sub>		20% to 80%		185	230			
Fall time	$T_{THL}$					175	220			
Minimum pulse width	$T_{pw}$			$S_0 - S_3 = LOW$	285	305	330			
Jitter ( $\sigma$ )	$T_{uc}$			$S_0 - S_3 = HIGH$		5	12			

Note: AC test circuit; See page 4-3.

**Block Diagram**



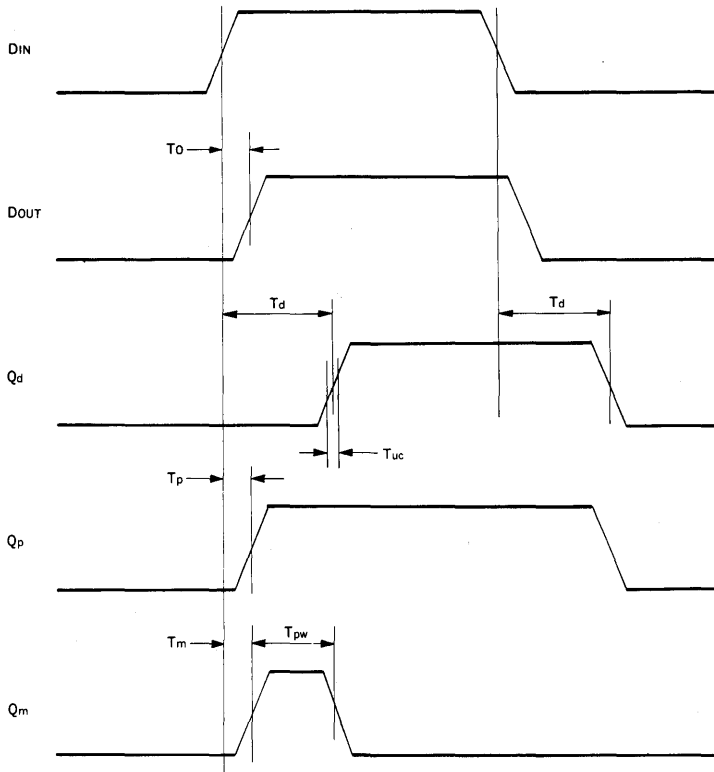
**Truth Table**

N	Input				Number of Gate	Output: Qd	
	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>		Typical Delay	
0	L	L	L	L	1	870ps	
1	L	L	L	H	2	945ps	
2	L	L	H	L	3	1095ps	
3	L	L	H	H	4	1155ps	
4	L	H	L	L	5	1255ps	
5	L	H	L	H	6	1305ps	
6	L	H	H	L	7	1460ps	
7	L	H	H	H	8	1520ps	

N	Input				Number of Gate	Output: Qd	
	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>		Typical Delay	
8	H	L	L	L	9	1645ps	
9	H	L	L	H	10	1690ps	
10	H	L	H	L	11	1805ps	
11	H	L	H	H	12	1855ps	
12	H	H	L	L	13	1990ps	
13	H	H	L	H	14	2045ps	
14	H	H	H	L	15	2210ps	
15	H	H	H	H	16	2240ps	

Typical delay time is calculated approximately by formula ;  
 $T_d = (880 + 92N \text{ ps} \pm 70\text{ps}) \pm 25\%$

Timing Diagram



$$T_d \approx (880 + 92N) \text{ ps} \pm 70\text{ps} \pm 25\%$$

$$\begin{aligned} D_{out}(T) &= D_{in}(T - T_o) \\ Q_d(T) &= D_{in}(T - T_d) \\ Q_p(T) &= D_{out}(T) + Q_d(T) \\ Q_m(T) &= D_{out}(T) \cdot Q_d(T) \end{aligned}$$

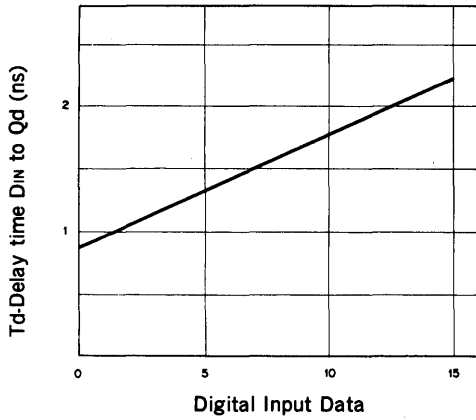


Figure1. Input Data vs Delay Time

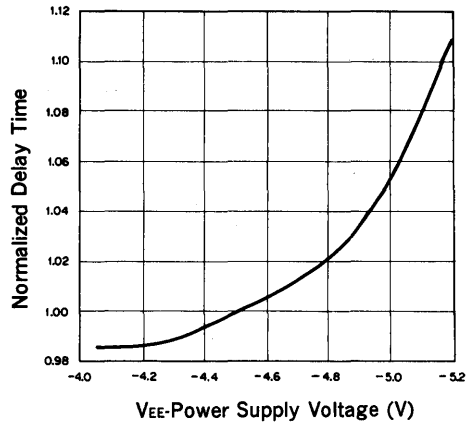


Figure2. Change in Delay Time vs. Change in Supply Voltage

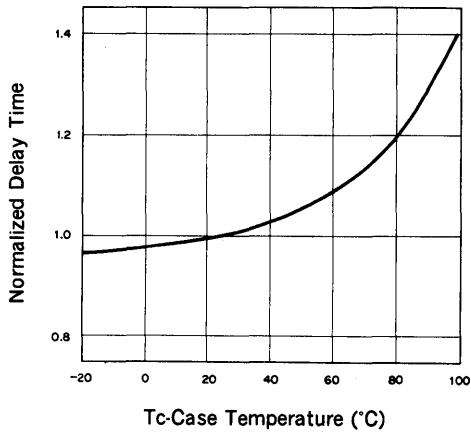


Figure3. Change in Delay Time vs. Change in Case Temperature

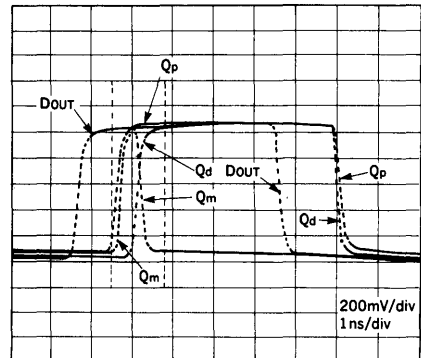


Figure4. Output Waveforms (N=0)



**9, 8, Dual 4-bit Multiplexer**

**Description**

The CXB1130Q is an ultra high speed monolithic ECL Multiplexer which functions as a 9-bit, 8-bit or dual 4-bit Parallel to Serial Converter.

The IC fetches a parallel data (D0-D8) present at the inputs and converts it into a serial data. Multiplexing is carried out in sequence from D0 to D8. S1 and S2 select a bit length.

With Load Select (LS) input set to LOW, internal load pulse loads parallel data. Start Load pulse (ST), which starts multiplexing, has to be maintained HIGH for at least (bit length-1) clock periods.

With LS set to HIGH, External Load pulse (EL) loads parallel data. The bit length is determined by a period of EL.

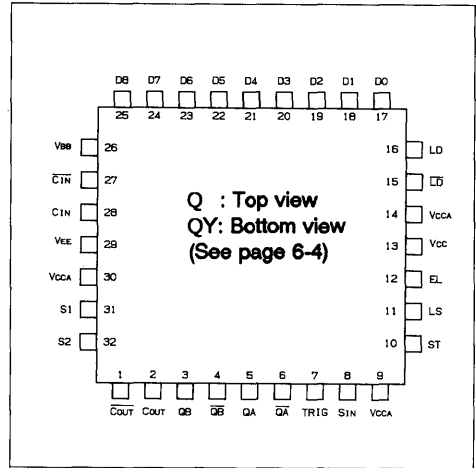
**Features**

- Typical clock rate up to 1.6 GHz
- Variable bit length: 9-bit, 8-bit and dual-4-bit
- Internal pull down resistors on input pins to maintain logic Low level with the pins left open
- ECL 100K compatible I/O levels

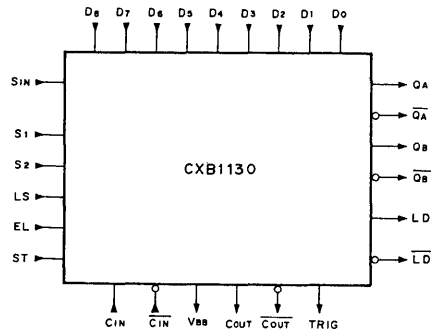
**Pin Names**

Dn	Parallel Data inputs
Sn	Bit length Select inputs
LS	Load Select input
ST	Load Start input
EL	External Load pulse input
SIN	Serial data input
CIN, $\overline{CIN}$	Clock inputs (positive edge trigger)
QA, $\overline{QA}$	Multiplexed serial data outputs (9, 8 and 4-bit)
QB, $\overline{QB}$	Multiplexed serial data outputs (4bit)
TRIG	Trigger pulse output
COUT, $\overline{COUT}$	Buffered Clock outputs
LD, $\overline{LD}$	Load pulse outputs
VCC	Circuit ground
VCCA	Circuit ground for outputs
VEE	Negative power supply

**Pin Assignment**



**Logic Symbol**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-190	-140	-98	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	$C_{IN}$	$Q_A, Q_B$		1000	1330	1690	ps	
	$T_{PHL}$				1010	1350	1710		
	$T_{PLH}$		$C_{OUT}$		760	1010	1280		
	$T_{PHL}$				760	1010	1280		
	$T_{PLH}$		TRIG	ST=L	970	1290	1640		
	$T_{PHL}$				1100	1470	1870		
	$T_{PLH}$		LD	LS=L	970	1290	1640		
	$T_{PHL}$				1000	1330	1690		
	$T_{PLH}$			EL	LS=H	650	860		1090
	$T_{PHL}$					660	880		1110
Set up time	$T_S$	$D_n, S_{IN} \rightarrow C_{IN}$		LS=L	-290				
		EL, $C_{IN}$		LS=H	100				
Hold time	$T_H$	$C_{IN} \rightarrow D_n, S_{IN}$		LS=L	640				
		$C_{IN}, EL$		LS=H	220				
Release time	$T_R$	$ST, C_{IN}$	$Q_A, Q_B$		100				
Max. Clock frequency	9Bit	$f_{MAX}$	$C_{IN}$		1.5	1.9		GHz	
	8Bit				1.3	1.6			
	4Bit				1.3	1.6			
	External				1.7	2.1			
Rise time	$T_{TLH}$		$Q_A, Q_B, LD$	20% to 80%		400	500	ps	
Fall time	$T_{THL}$		TRIG, $C_{OUT}$			360	460		

Note: AC test circuit; See pages 4-4 and 4-5.

**Function Table**

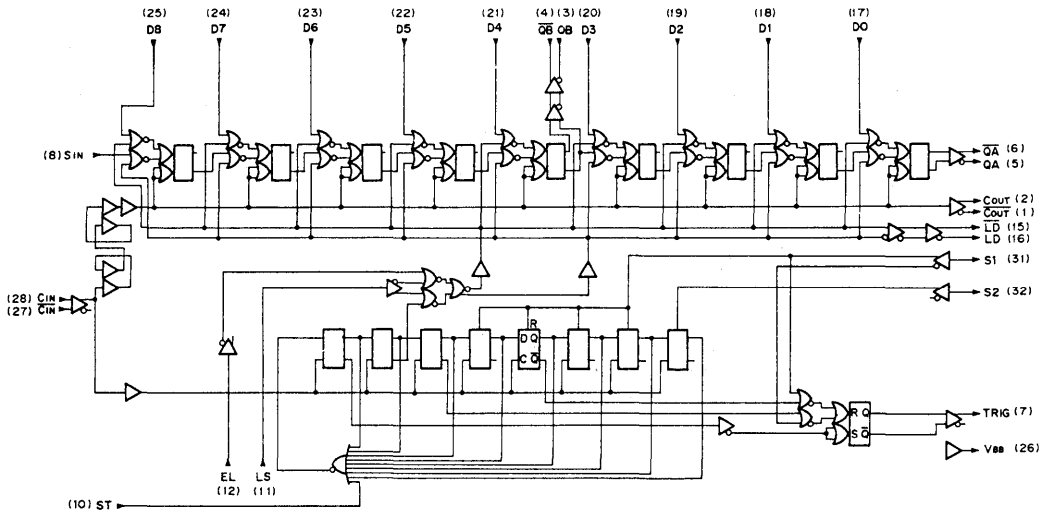
LS	S1	S2	ST	EL	C <sub>IN</sub>	Function		
L	L	L	L	X	J	Internal Load	9bit	Load and Shift Right, D0-D8 → QA
L	L	L	H	X	J		Initialize	
L	L	H	L	X	J		8bit	Load and Shift Right, D0-D7 → QA
L	L	H	H	X	J			Initialize
L	H	X	L	X	J		4bit ×2	Load and Shift Right, D0-D3 → QA D4-D7 → QB
L	H	X	H	X	J			Initialize
H	X	X	X	L	J	External Load	Shift Right	$\geq 9\text{bit}$ D0-D8 → QA $\leq 4\text{bit}$ { D0-D3 → QA D4-D7 → QB
H	X	X	X	H	J		Load Data	

H: HIGH level voltage, L: LOW level voltage, J: Positive transition edge, X: Don't care

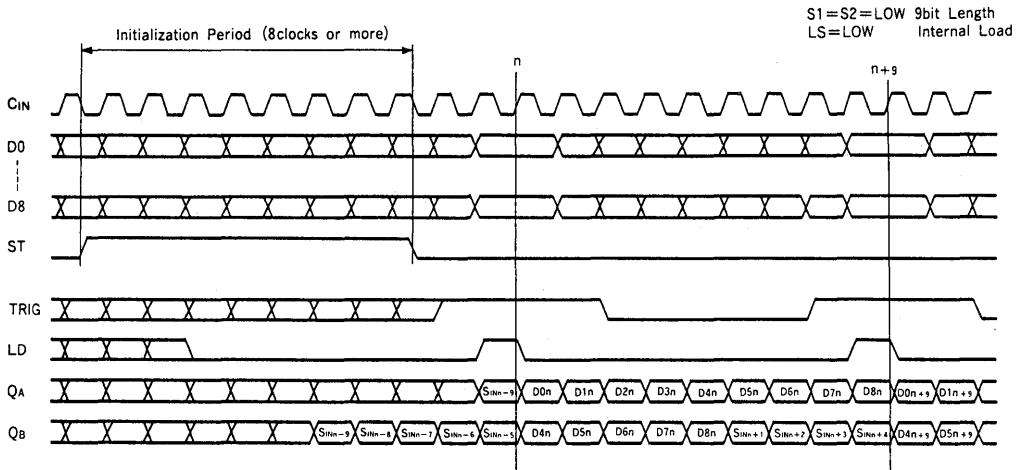
In the External Load mode, any bit length can be selected by the period of the External Load (EL) pulse. See Timing Diagram.



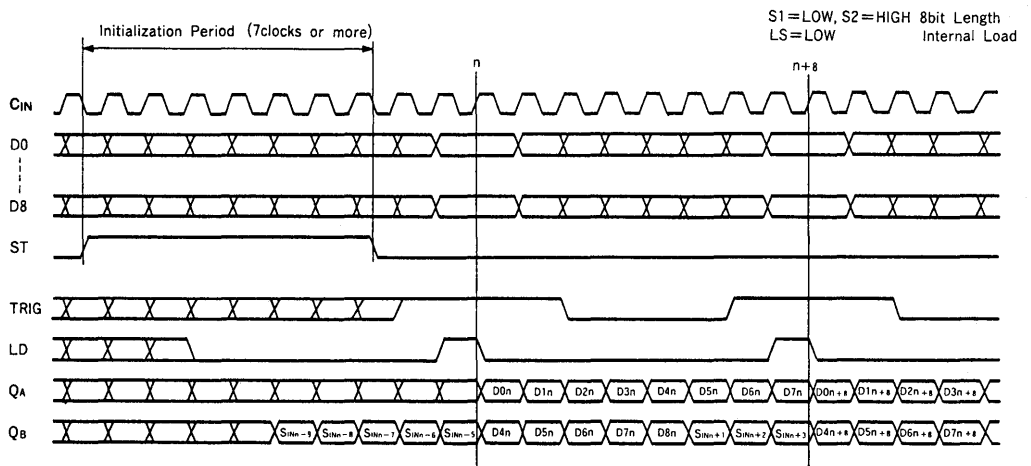
Logic Diagram



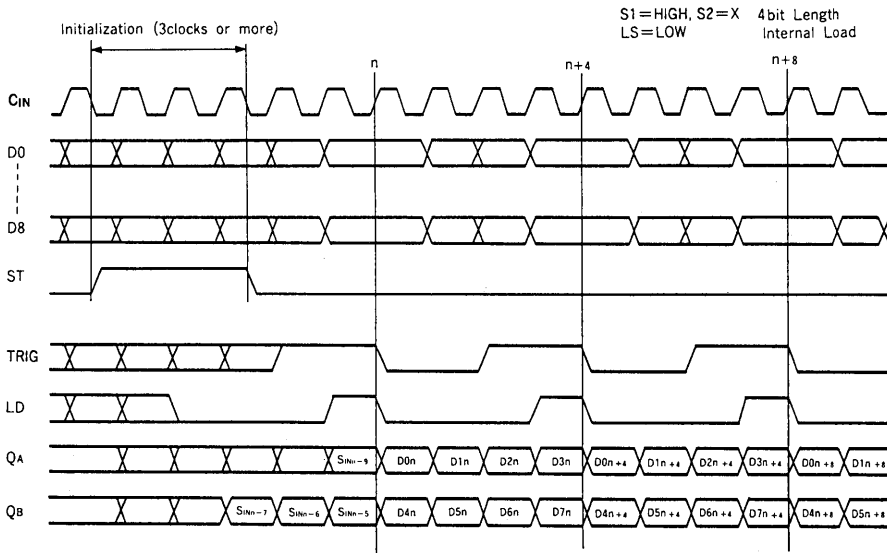
**Timing Diagram—9bit**



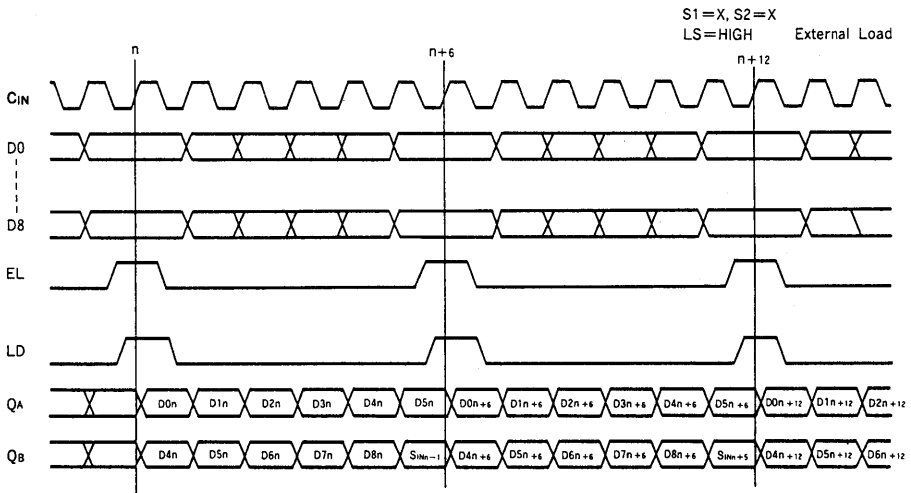
**Timing Diagram—8bit**



Timing Diagram—4bit×2



Timing Diagram—6bit External Load



## 9, 8, Dual 4-bit Demultiplexer

### Description

The CXB1131Q is an ultra high speed monolithic ECL Demultiplexer which functions as a 9-bit, 8-bit or dual 4-bit Serial to Parallel Converter. S1 and S2 select a bit length.

With Load Select (LS) input set to LOW, start Load pulse (ST) starts loading of the data. ST has to be maintained High for at least (bit length - 1) clock periods.

With LS set to HIGH, External Load (EL) pulse loads parallel data. The bit length is determined by a period of EL.

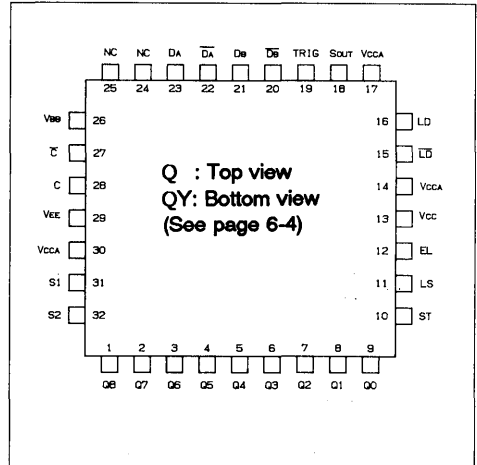
### Features

- Typical clock rate up to 1.5 GHz
- Variable bit length: 9-bit, 8-bit and Dual 4-bit
- Internal pull down resistors on input pins to maintain logic Low level with the pins left open
- ECL 100K compatible I/O levels
- Differential clock, data input and latch pulse output

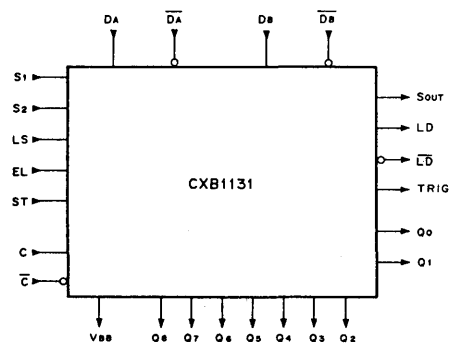
### Pin Names

DA, $\overline{DA}$	Serial Data inputs (9, 8 and 4-bit operation)
DB, $\overline{DB}$	Serial Data inputs (4-bit operation)
S <sub>n</sub>	Bit length Select inputs
LS	Load Select input
ST	Load Start input
EL	External Load pulse input
C, $\overline{C}$	Clock inputs (positive edge trigger)
Q <sub>n</sub>	Demultiplexed parallel data outputs (9, 8 and 4-bit)
S <sub>OUT</sub>	Serial data output
TRIG	Trigger pulse output
LD, $\overline{LD}$	Load pulse outputs
V <sub>CC</sub>	Circuit ground
V <sub>CCA</sub>	Circuit ground for outputs
V <sub>EE</sub>	Negative voltage supply

### Pin Assignment



### Logic Symbol



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-258	-190	-133	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	C	Qn	ST=L	1380	1840	2340	ps	
	$T_{PHL}$				1350	1800	2290		
	$T_{PLH}$		SOUT		890	1180	1500		
	$T_{PHL}$				870	1160	1470		
	$T_{PLH}$		TRIG		1140	1520	1930		
	$T_{PHL}$				1130	1500	1900		
	$T_{PLH}$		LD		LS=L	1240	1650		2050
	$T_{PHL}$					1030	1370		1740
	$T_{PLH}$	LS=H		750	970	1200			
	$T_{PHL}$			750	970	1200			
Set up time	$T_S$	DA,C	Qn	LS=L	-110			ps	
		DB,C			260				
		C,EL			50				
Hold time	$T_H$	C,DA	Qn	LS=L	390			ps	
		C,DB			130				
		EL,C			400				
Release time	$T_R$	ST,C			150				
Max. Clock frequency	9Bit	$f_{MAX}$	C		1.4	1.7		GHz	
	8Bit				1.2	1.5			
	4Bit				1.3	1.6			
	External				1.4	1.7			
Rise time	$T_{TLH}$		Qn,LD	20% to 80%		420	530	ps	
Fall time	$T_{THL}$		SOUT,TRIG			360	460		

Note: AC test circuit; See pages 4-4 and 4-5.

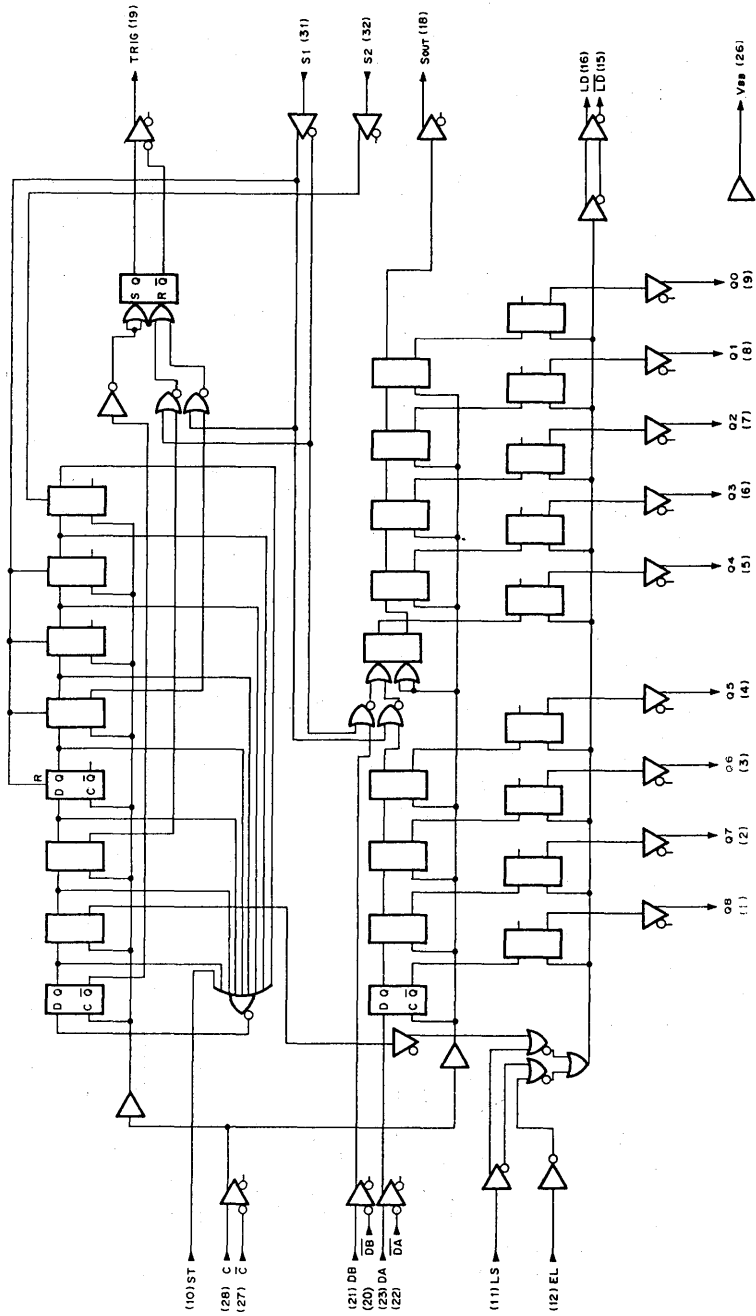
Function Table

LS	S1	S2	ST	EL	C	Function		
L	L	L	L	X	J	Internal Load	9bit	Load and output, DA → Q0-Q8
L	L	L	H	X	J			Initialize (8 clock period minimum)
L	L	H	L	X	J		8bit	Load and output, DA → Q1-Q8
L	L	H	H	X	J			Initialize (7 clock period minimum)
L	H	X	L	X	J		4bit ×2	Load and Shift DA → Q5-Q8
L	H	X	H	X	J			Initialize (3 clock period minimum)
H	L	X	X	X	J	External Load	5 ≤ bit length ≤ 9	Serial Data Load
H	L	X	X	J	X			Parallel Data Output
H	H	X	X	X	J		bit length ≤ 4	Serial Data Load
H	H	X	X	J	X			Parallel Data Output

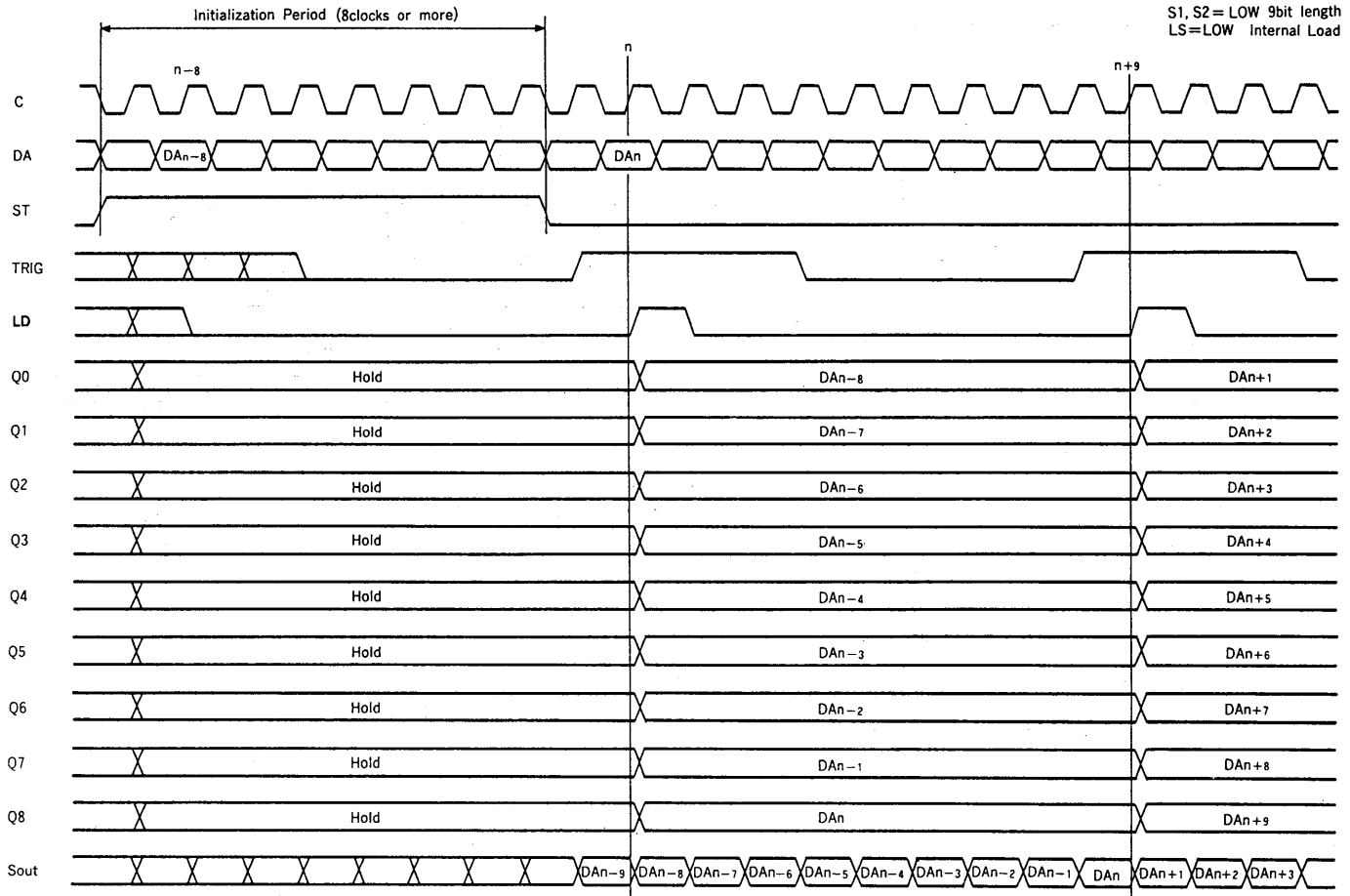
H: HIGH voltage level, L: LOW voltage level, J: Positive transition edge, X: Don't care

In the External Load mode, serial input data is entered synchronously with clock (C) and parallel output data is output to output pins synchronously with External Load (EL). The bit length can be determined by the period of EL pulse. See Timing Diagram.

Block Diagram

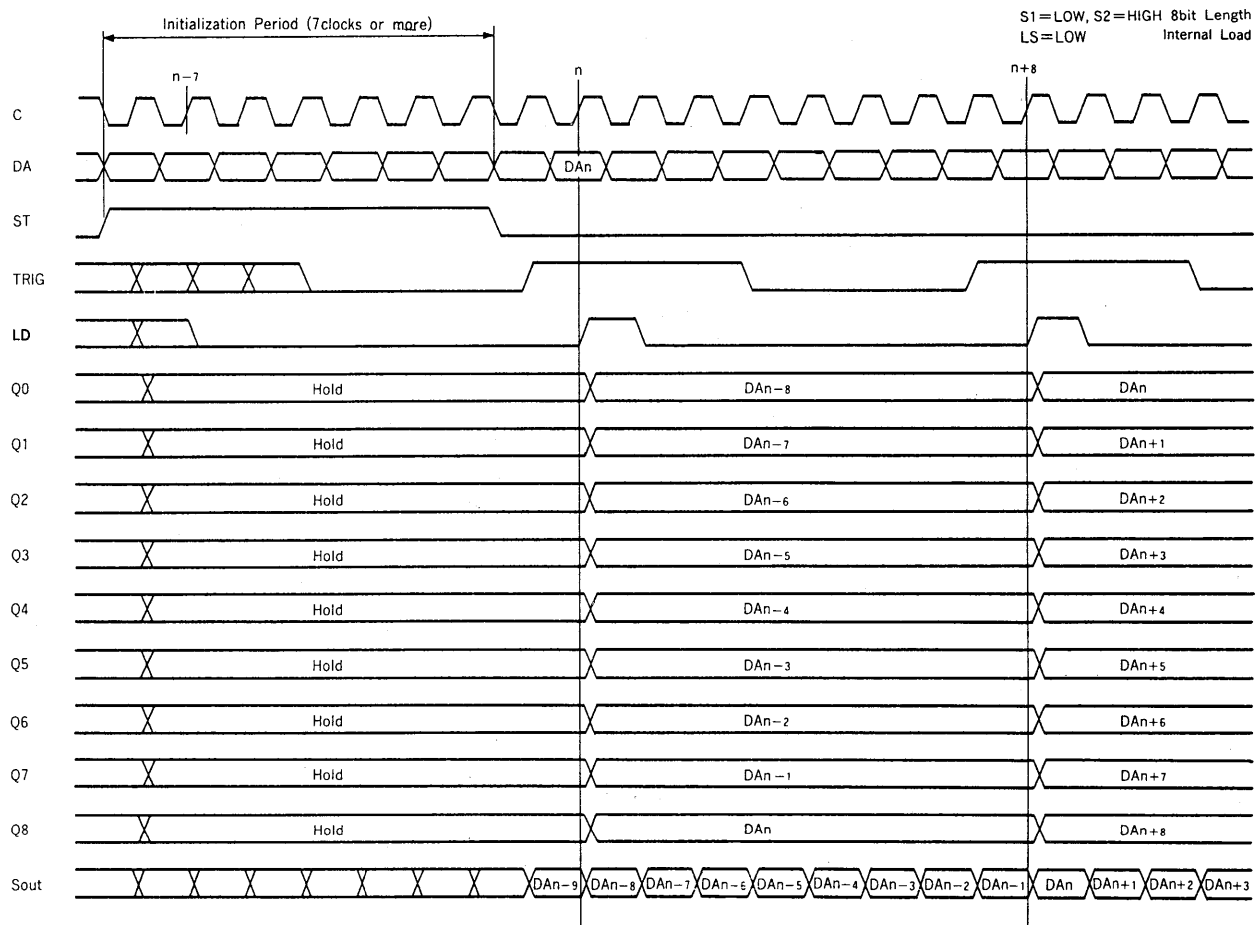


# Timing Diagram — 9-bit

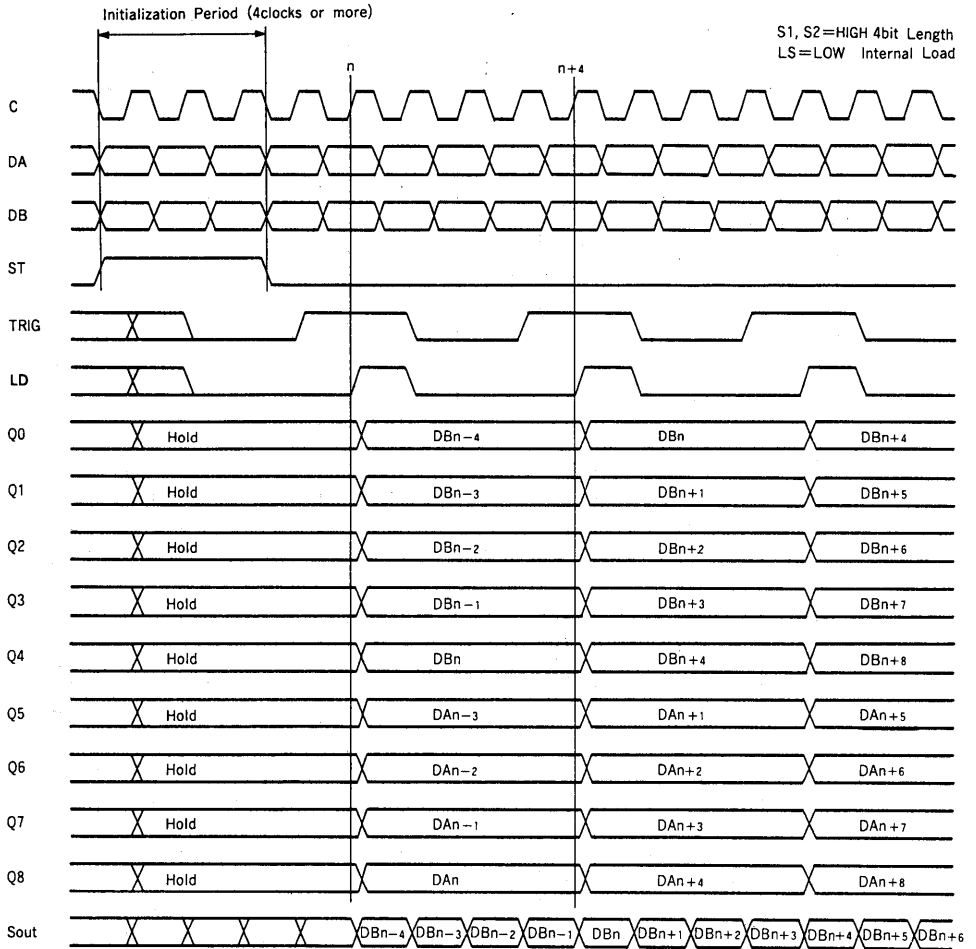




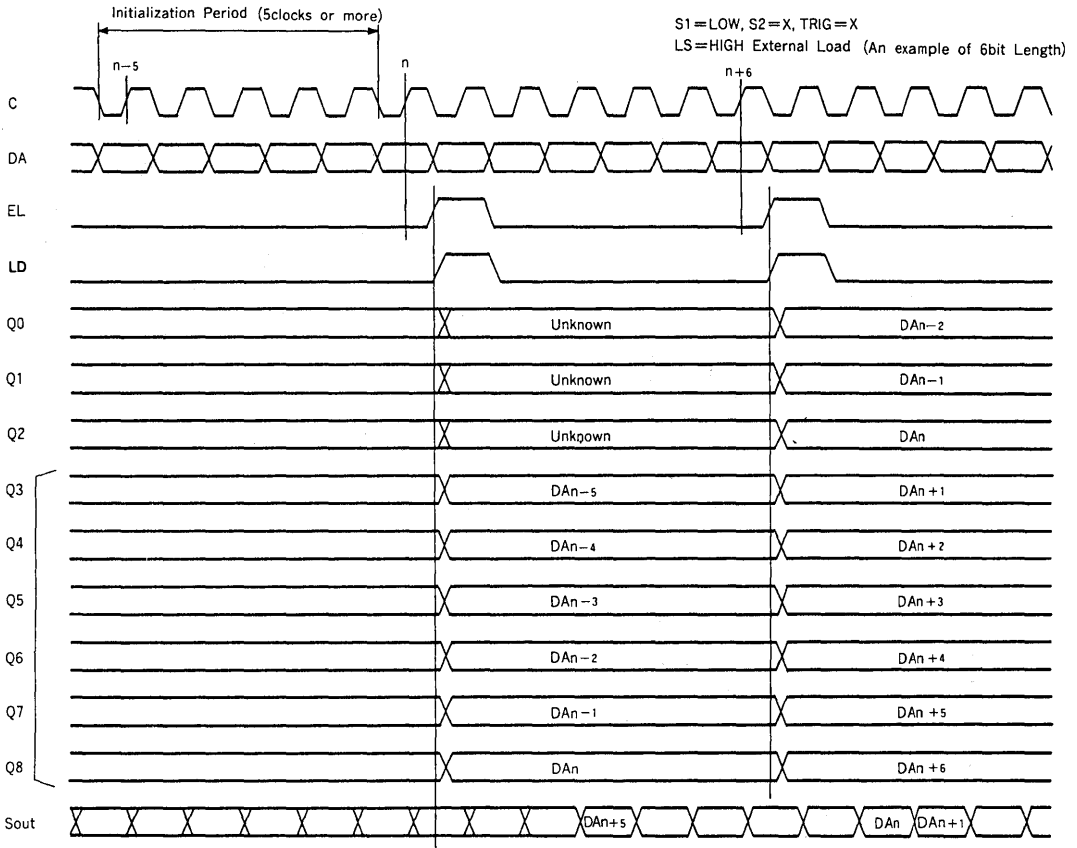
Timing Diagram — 8-bit



Timing Diagram — 4-bit × 2



**Timing Diagram — 6-bit External Load**



**9, 8, Dual 4-bit Universal Shift Register**

**Description**

The CXB1132Q is an ultra high speed monolithic Universal Shift Register with variable bit length.

Select inputs S1 and S2 select a function mode from parallel load, hold, shift right, and shift left. S3 and S4 select a bit length. The operation is shown in Function Table.

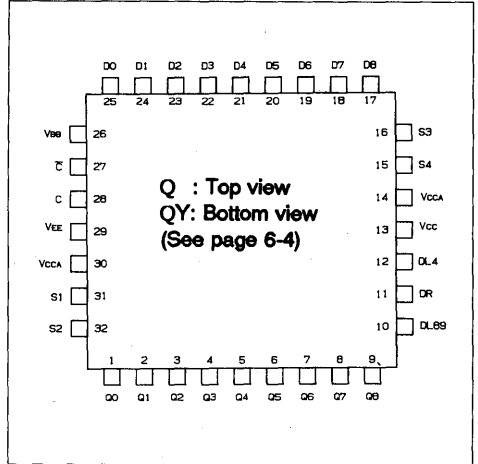
**Features**

- Typical clock rate up to 1.3GHz
- Variable bit length: 9-bit, 8-bit and 4-bit
- Internal pull down resistors on input pins to maintain logic LOW level the pins left open
- ECL 100K compatible I/O levels
- Differential clock input

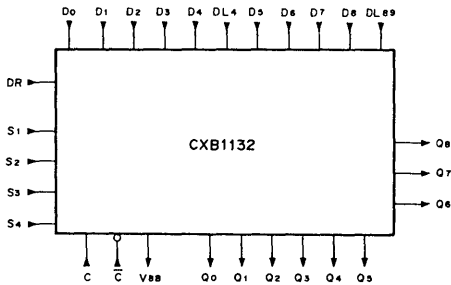
**Pin Names**

- |               |                                      |
|---------------|--------------------------------------|
| Dn            | Data inputs                          |
| DR, DL4, DL89 | Data inputs                          |
| Sn            | Select inputs                        |
| C, $\bar{C}$  | Clock inputs (positive edge trigger) |
| Qn            | Data outputs                         |
| VBB           | Reference voltage output             |
| VCC           | Circuit ground                       |
| VCCA          | Circuit ground for outputs           |
| VEE           | Negative voltage supply              |

**Pin Assignment**



**Logic Symbol**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-236	-173	-121	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	C	Qn		800	1070	1360	ps	
	$T_{PHL}$				770	1030	1310		
Set up time	$T_S$	Dn, C	Qo		210				
		DR, C	Q4		190				
		DL4, C	Q7, Q8		220				
		DL89, C	Qn		320				
Hold time	$T_H$	S1, S2→C	Qn		650				
		C, Dn	Qo		220				
		C, DR	Q4		160				
		C, DL4	Q7, Q8		230				
		C, DL89	Qn	10					
		C→S1, S2		-30					
Max. Clock frequency	$f_{MAX}$				1.0	1.3		GHz	
Rise time	$T_{TLH}$	C	Qn	20% to 80%		430	550	ps	
Fall time	$T_{THL}$					380	480		

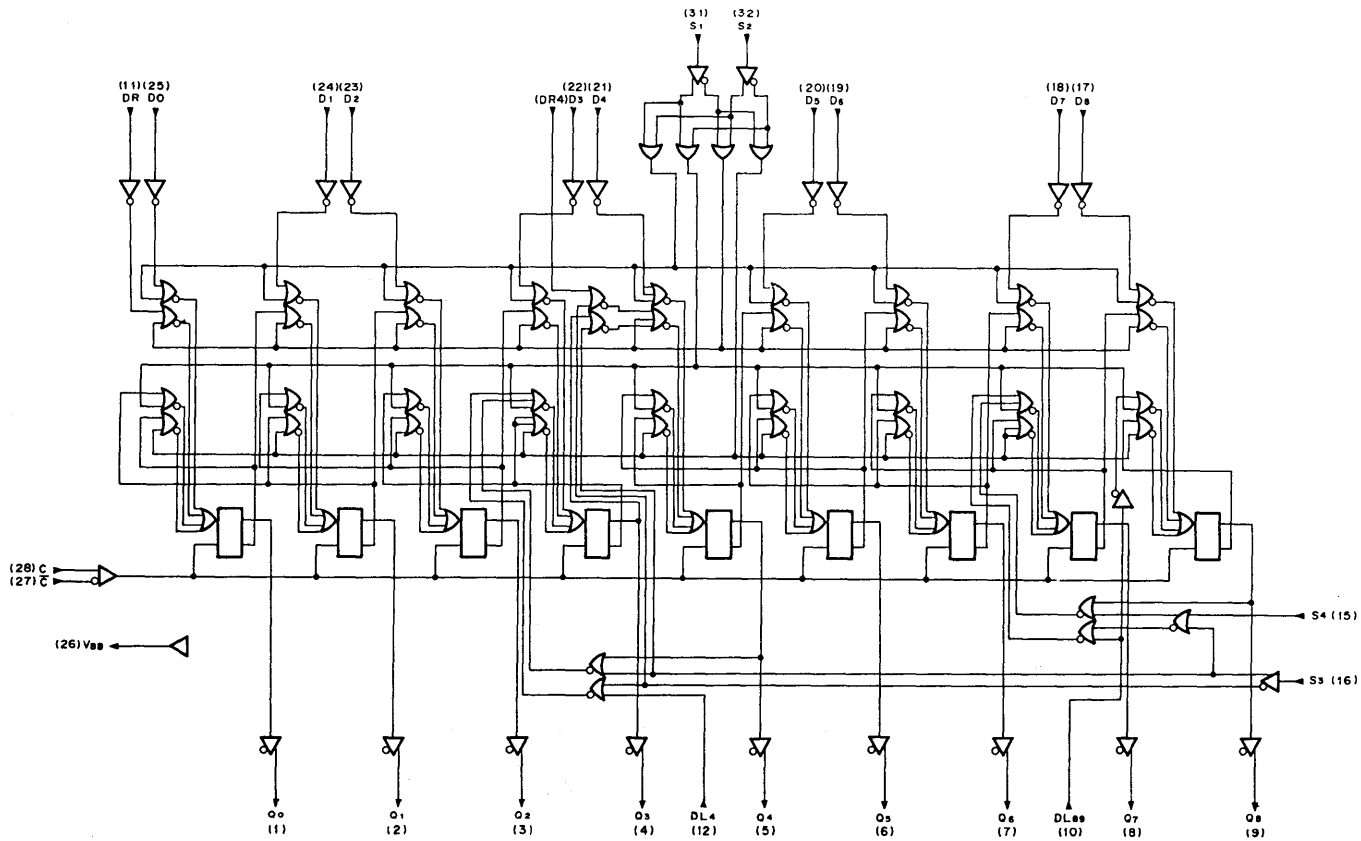
Note: AC test circuit; See pages 4-4 and 4-5.

Function Table

Function \ Pin	Inputs									Outputs							
	DR	DL89	DL4	S1	S2	S3	S4	C	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Load	X	X	X	L	L	X	X	┘	D0	D1	D2	D3	D4	D5	D6	D7	D8
Shift left 9 bit length	X	DL89	X	L	H	L	L	┘	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	DL89
Shift left 8 bit length	X	DL89	X	L	H	L	H	┘	Q1	Q2	Q3	Q4	Q5	Q6	Q7	DL89	DL89
Shift left 4 bit length	X	DL89	DL4	L	H	H	X	┘	Q1	Q2	Q3	DL4	Q5	Q6	Q7	DL89	DL89
Shift right 9 bit length	DR	X	X	H	L	L	L	┘	DR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Shift right 8 bit length	DR	X	X	H	L	L	H	┘	DR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Shift right 4 bit length	DR	X	X	H	L	H	X	┘	DR	Q0	Q1	Q2	L	Q4	Q5	Q6	Q7
Hold	X	X	X	H	H	X	X	X	← No change →								

- X: Don't care
- ┘: Positive transition edge
- H: HIGH voltage level
- L: LOW voltage level

# Block Diagram



DR4 is fixed to "L" level.

22, 15, 7 Stage Data Scrambler with Differential I/O

**Description**

The CXB1133Q is an ultra high speed monolithic ECL Data Scrambler with variable bit length.

Select switch M selects a mode: "scrambler" or "Maximal code sequence generator". In scrambler mode, input data is converted into a quasi-random data sequence. The quasi-random data can be re-converted into the original input data by a Descrambler such as the CXB1134Q. In M-code sequence generator mode, the IC generates a quasi-random number sequence.

Select inputs S1 and S2 select a bit length.

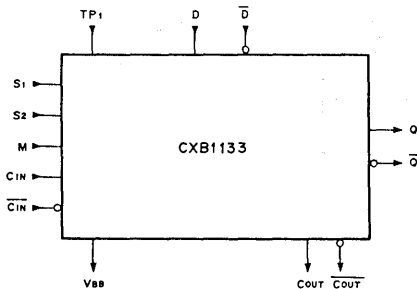
**Features**

- Typical clock rate up to 1.4GHz
- Variable bit length: 22-bit, 15-bit, 7-bit
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential input and output

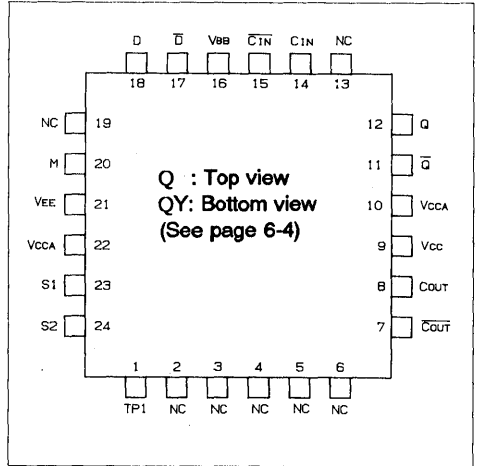
**Pin Names**

- D,  $\bar{D}$  Data inputs in scrambler mode
- M Mode Select input
- S<sub>n</sub> Select inputs
- C<sub>IN</sub>,  $\bar{C}_{IN}$  Clock inputs (positive edge trigger)
- Q,  $\bar{Q}$  Data outputs
- C<sub>OUT</sub>,  $\bar{C}_{OUT}$  Buffered clock outputs
- TP1 Test point (It must be left open)
- V<sub>BB</sub> Reference voltage
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative voltage supply

**Logic Symbol**



**Pin Assignment**



**Stage Select**

S1	S2	Operation
L	L	22 Stage
L	H	15 Stage
H	L	7 Stage
H	H	

**Function Select**

M	Operation
H	Maximal code sequence generator
L	Data scrambler

H: HIGH voltage level, L: LOW voltage level



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-147	-108	-76	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

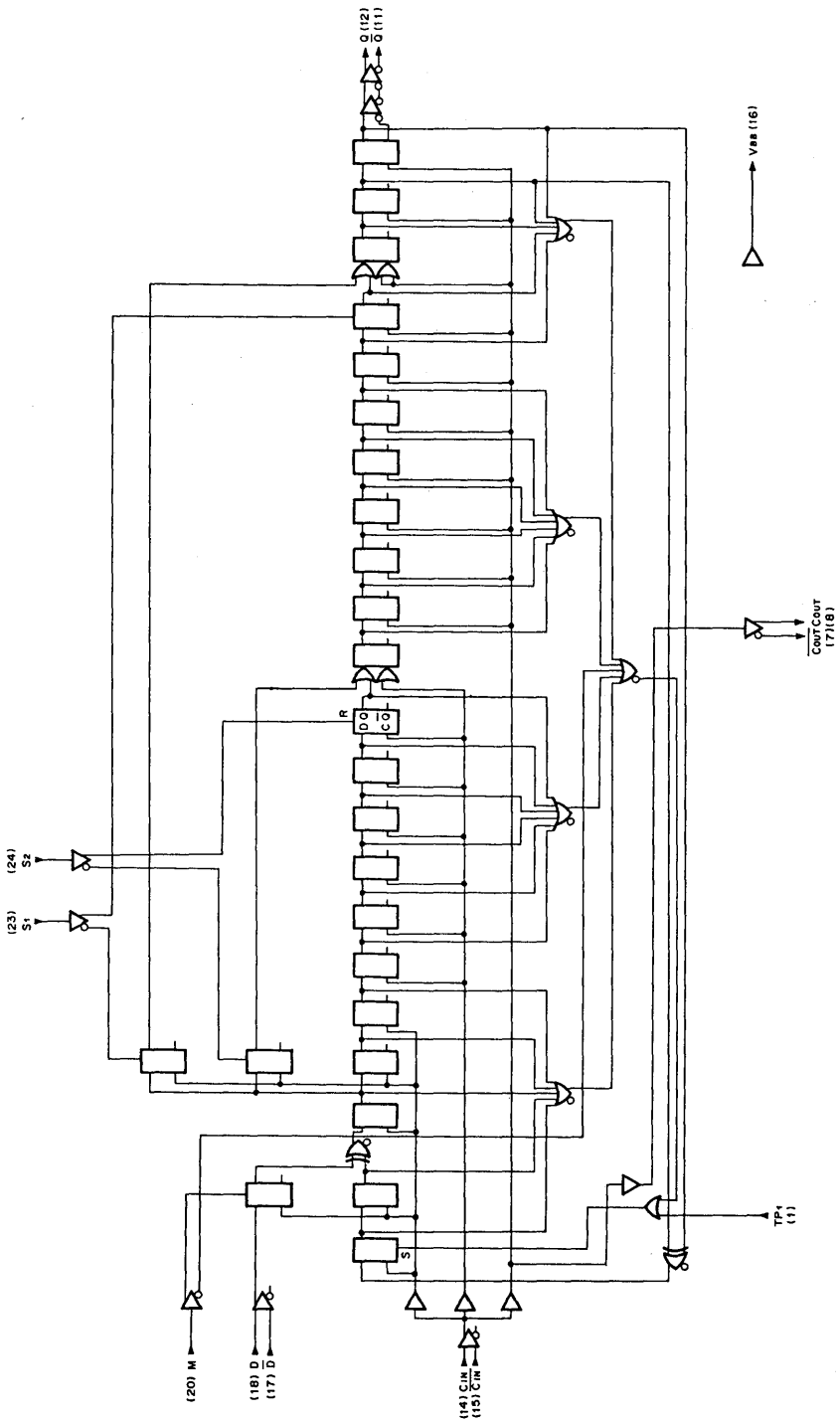
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	$C_{IN}$	Q		1040	1390	1765	ps
	$T_{PHL}$				1030	1370	1740	
	$T_{PLH}$		$C_{OUT}$		650	870	1100	
	$T_{PHL}$				650	870	1100	
Set up time	$T_S$	D, $C_{IN}$	Q	$S1 = S2 = L$	80			
Hold time	$T_H$	$C_{IN}$ , D	Q	$M = L$	290			
Max. Clock frequency	$f_{MAX}$				1.1	1.4		GHz
Rise time	$T_{TLH}$	$C_{IN}$	Q, $C_{OUT}$	20% to 80%		300	380	ps
Fall time	$T_{THL}$					280	355	

Note: AC test circuit; See pages 4-4 and 4-5.

Block Diagram





**22, 15, 7 Stage Descrambler with Differential I/O**

**Description**

The CXB1134Q is an ultra high speed monolithic ECL Date Descrambler with variable bit length.

Select switches S1 and S2 select a bit length. This IC is used in combination with the CXB1133Q Scrambler/Maximal code generator to re-convert a quasi-random data sequence into the original data sequence.

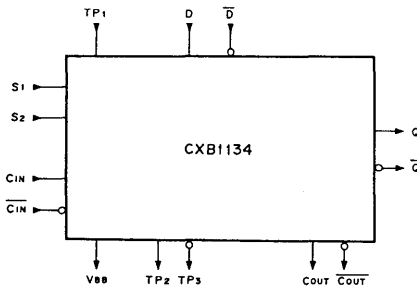
**Features**

- Typical clock rate up to 1.4GHz
- Variable bit length: 22-bit, 15-bit, 7-bit
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential input and output

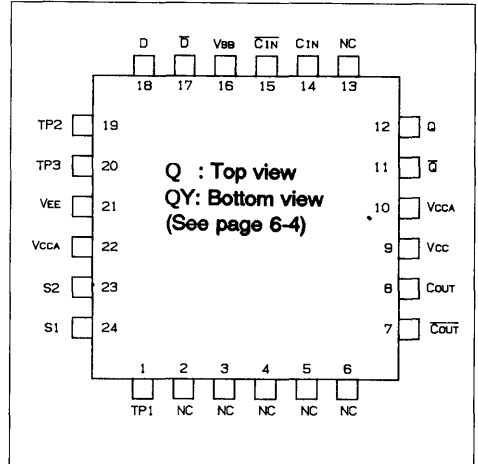
**Pin Names**

- D,  $\bar{D}$  Data inputs
- S<sub>n</sub> Select inputs
- C<sub>IN</sub>,  $\bar{C}_{IN}$  Clock inputs (positive edge trigger)
- Q,  $\bar{Q}$  Data outputs
- C<sub>OUT</sub>,  $\bar{C}_{OUT}$  Buffered clock outputs
- TP<sub>n</sub> Test points (They must be left open)
- V<sub>BB</sub> Reference voltage
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative voltage supply

**Logic Symbol**



**Pin Assignment**



**Stage Select**

S1	S2	Operation
L	L	22 Stage
L	H	15 Stage
H	L	7 Stage
H	H	

H : HIGH voltage level  
L : LOW voltage level

**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-150	-110	-77	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

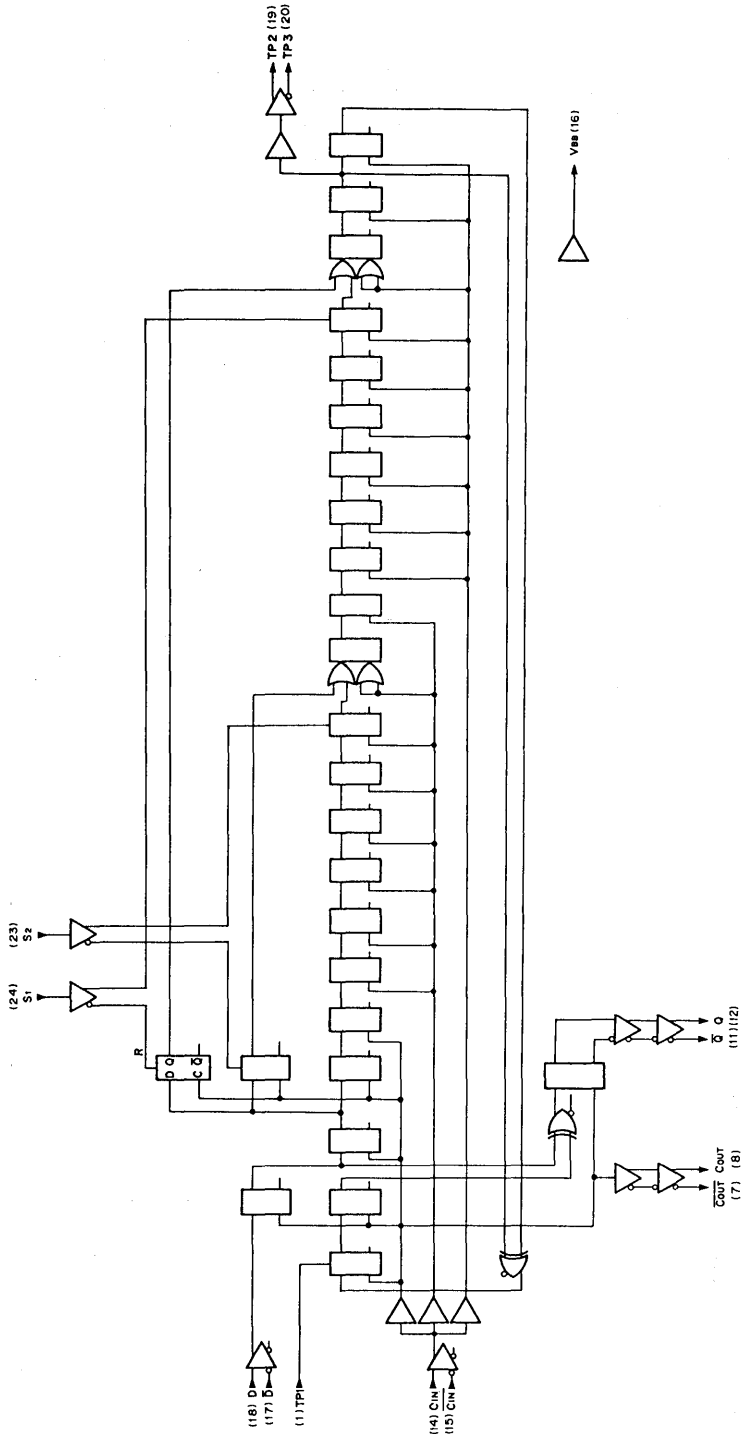
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	$T_{PLH}$	$C_{IN}$	Q		950	1270	1610	ps	
	$T_{PHL}$				920	1220	1550		
	$T_{PLH}$		C <sub>OUT</sub>		680	900	1140		
	$T_{PHL}$				680	910	1150		
Set up time	$T_S$	D, $C_{IN}$	Q		20				
Hold time	$T_H$	$C_{IN}$ , D			340				
Max. Clock frequency	$f_{MAX}$				1.1	1.4			GHz
Rise time	$T_{TLH}$	$C_{IN}$	Q, C <sub>OUT</sub>		20% to 80%		320		410
Fall time	$T_{THL}$					280	360		

Note: AC test circuit; See pages 4-4 and 4-5.

Block Diagram





## 8 to 16-bit Serial Data Comparator

### Description

The CXB1135Q is an ultra high speed monolithic ECL Serial Data Comparator with variable bit length of 8 to 16. This IC compares serial input data (D<sub>IN</sub>) with the preset parallel data (D<sub>n</sub>) and indicates the coincidence of two data at outputs Z<sub>s</sub> and Z<sub>A</sub>.

Select switches (S1-S4) select a bit length.

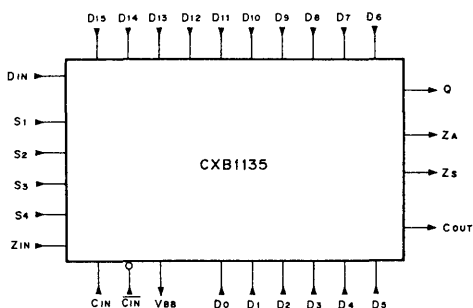
### Features

- Typical clock rate up to 1.4GHz
- Variable bit length: 8-bit to 16-bit
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

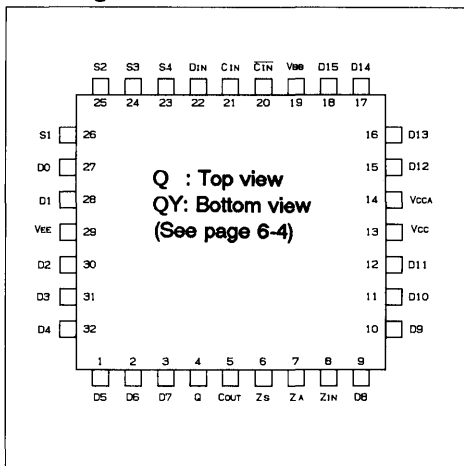
### Pin Names

- D<sub>n</sub> Parallel Data inputs
- D<sub>IN</sub> Serial Data input
- Z<sub>IN</sub> Serial data input for bit length extension
- S<sub>n</sub> Bit length Select inputs
- C<sub>IN</sub>,  $\overline{CIN}$  Clock inputs (positive edge trigger)
- Q Serial output
- Z<sub>s</sub> Synchronous coincidence output
- Z<sub>A</sub> Asynchronous coincidence output
- C<sub>OUT</sub> Buffered clock output
- V<sub>BB</sub> Reference voltage output
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- VEE Negative voltage supply

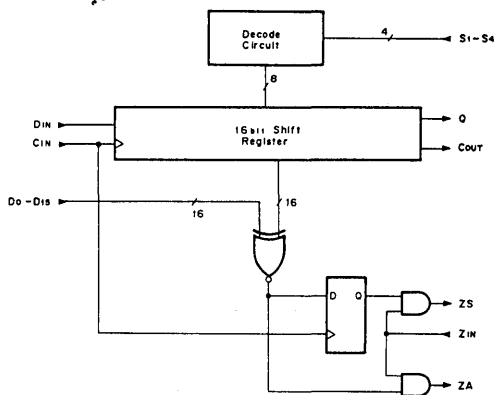
### Logic Symbol



### Pin Assignment



### Block Diagram



### Bit Length Select

S1	S2	S3	S4	Operation	Parallel inputs
L	L	L	L	8bit	D0 to D7
L	L	L	H	9bit	D0 to D8
L	L	H	L	10bit	D0 to D9
L	L	H	H	11bit	D0 to D10
L	H	L	L	12bit	D0 to D11
L	H	L	H	13bit	D0 to D12
L	H	H	L	14bit	D0 to D13
L	H	H	H	15bit	D0 to D14
H	L	L	L	16bit	D0 to D15

H: HIGH voltage level, L: LOW voltage level



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-174	-128	-90	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

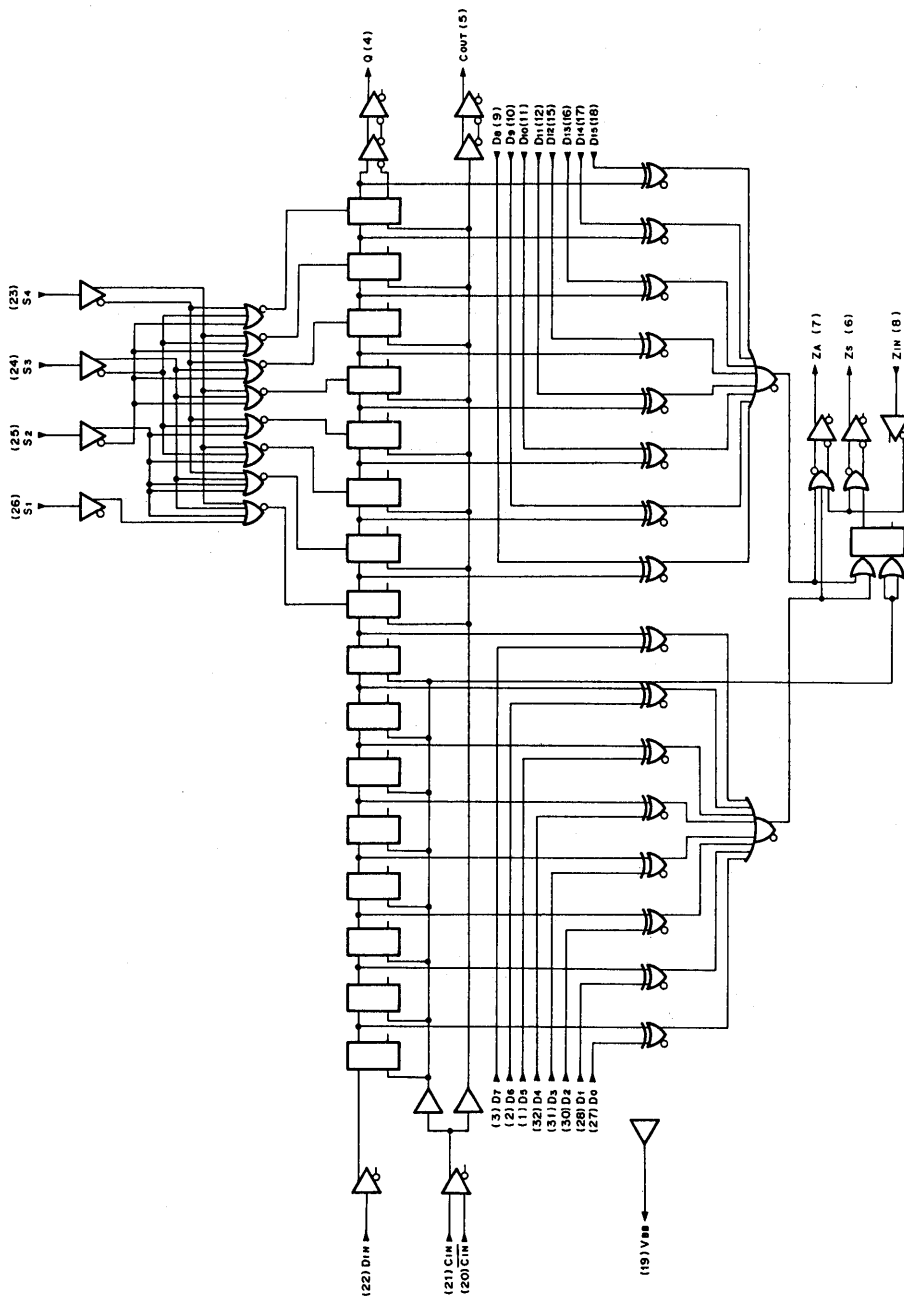
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time	T <sub>PLH</sub>	C <sub>IN</sub>	Z <sub>A</sub>	Z <sub>IN</sub> =H	1420	1890	2400	ps	
	T <sub>PHL</sub>				1120	1490	1890		
	T <sub>PLH</sub>		Z <sub>S</sub>		1140	1520	1930		
	T <sub>PHL</sub>				1080	1440	1830		
	T <sub>PLH</sub>		Q		1060	1410	1790		
	T <sub>PHL</sub>				1030	1370	1740		
	T <sub>PLH</sub>	C <sub>OUT</sub>	850	1130	1430				
	T <sub>PHL</sub>		860	1150	1460				
	T <sub>PLH</sub>	Z <sub>IN</sub>	Z <sub>A</sub>	760	1010	1280			
	T <sub>PHL</sub>			510	680	860			
	T <sub>PLH</sub>		Z <sub>S</sub>	730	970	1230			
	T <sub>PHL</sub>			500	670	850			
Set up time	T <sub>S</sub>	D <sub>IN</sub> , C <sub>IN</sub>	Z <sub>A</sub> , Z <sub>S</sub>	Z <sub>IN</sub> =H	-230			GHz	
		D <sub>n</sub> , C <sub>IN</sub>			240				
Hold time	T <sub>H</sub>	C <sub>IN</sub> , D <sub>IN</sub>			550				
		C <sub>IN</sub> , D <sub>n</sub>			420				
Max. Clcok frequency	8-Bit	f <sub>MAX</sub>			C <sub>IN</sub>	1.1	1.4		
	9to16-Bit					1.1	1.4		
Rise time	T <sub>TLH</sub>	C <sub>IN</sub>	Z <sub>A</sub> , Z <sub>S</sub> , Q, C <sub>OUT</sub>	20% to 80%		500	630	ps	
Fall time	T <sub>THL</sub>					480	580		

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram

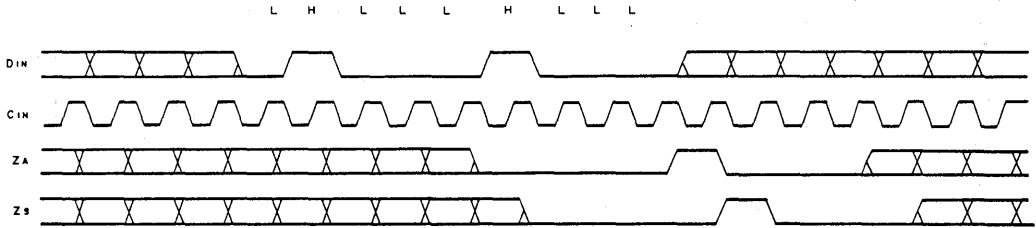


Timing Diagram—9-bit

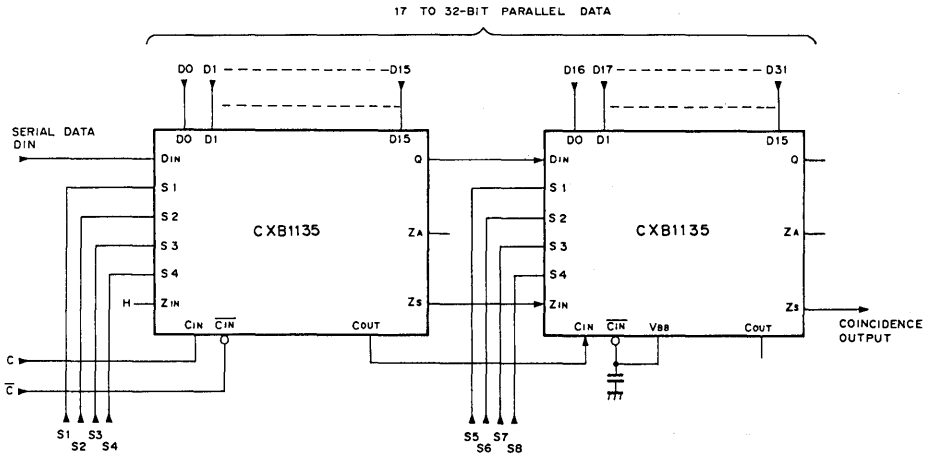
S1 to S3=LOW  
 S4=HIGH  
 9-bit length

D8	D7	D6	D5	D4	D3	D2	D1	D0
L	H	L	L	L	H	L	L	L

Example of 9-bit parallel input data. Parallel data input pins which are not used (D9 to D15) must be open.



Typical Application—17 to 32-bit Serial Data Comparator



**8-bit Universal Counter with Preset and Master Reset**

**Description**

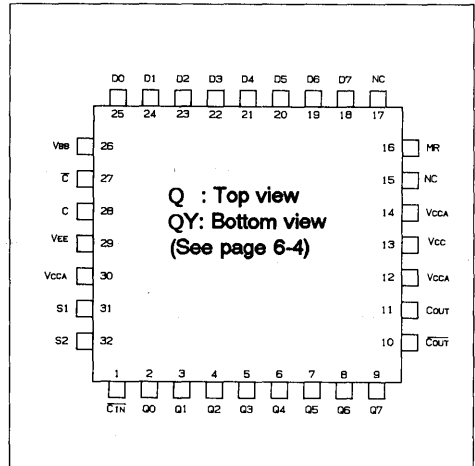
The CXB1136Q is an ultra high speed monolithic ECL 8-bit Universal Counter.

Two Select (S1, S2) inputs select modes: up count, down count, preset and hold. Carry-in ( $\overline{C_{IN}}$ ) and Carry out ( $C_{OUT}$ ) is provided for the expansion of bit length.

**Features**

- Typical clock rate up to 1.1GHz
- Up/Down/Preset/Hold modes
- Differential clock input
- Reference voltage output for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential clock input

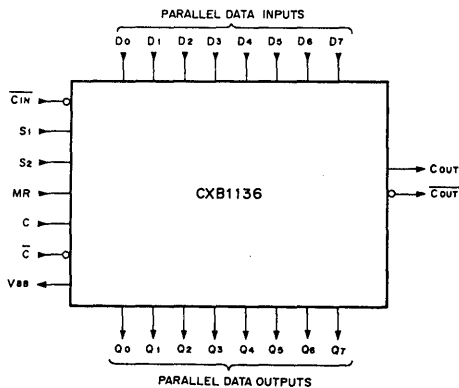
**Pin Assignment**



**Pin Names**

- Dn Parallel Data inputs
- Sn Select inputs
- MR Master direct Reset input
- $\overline{C_{IN}}$  Carry input
- C,  $\overline{C}$  Clock inputs (positive edge trigger)
- Qn Parallel data outputs
- $C_{OUT}$ ,  $\overline{C_{OUT}}$  Carry outputs
- VBB Reference voltage output
- VCC Circuit ground
- VCCA Circuit ground for output
- VEE Negative voltage supply

**Logic Symbol**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-194	-143	-100	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation delay time	$T_{PLH}$	C	Qn		770	1020	1300	ps		
	$T_{PHL}$				770	1020	1300			
	$T_{PLH}$				$\overline{C}_{IN}$	COUT	850		1130	1440
	$T_{PHL}$						910		1210	1540
	$T_{PLH}$	MR	COUT				1210		1610	2040
	$T_{PHL}$						1260		1660	2090
	$T_{PLH}$				1130	1500	1900			
	$T_{PHL}$				1130	1500	1900			
Set up time	$T_S$	Dn, C	Qn		530			ps		
					S1, C	900				
					S2, C	870				
		$\overline{C}_{IN}$ , C	COUT		1150					
Hold time	$T_H$	C, Dn	Qn		200			ps		
					C, S1	-350				
					C, S2	-350				
		C, $\overline{C}_{IN}$	COUT		-30					
Release time	$T_R$	MR, C	Qn		370			ps		
Min. Pulse width	$T_{PW}$	MR			330					
Max. Clock frequency	Count up	$f_{MAX}$			C	1.0	1.3			GHz
	Count down					0.8	1.1			
Rise time	$T_{TLH}$			20% to 80%		500	630	ps		
Fall time	$T_{THL}$					400	500			

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

All output pins are left open except measured output pins.

Sequential Truth Table

Pin Mode	Inputs											Outputs										
	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7	C <sub>IN</sub>	CLK	MR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	C <sub>OUT</sub>
Preset	L	L	L	L	H	H	H	H	H	H	X	┐	L	L	L	H	H	H	H	H	H	L
Count up	L	H	X	X	X	X	X	X	X	X	L	┐	L	H	L	H	H	H	H	H	H	H
	L	H	X	X	X	X	X	X	X	X	L	┐	L	L	H	H	H	H	H	H	H	H
	L	H	X	X	X	X	X	X	X	X	L	┐	L	H	H	H	H	H	H	H	H	L
	L	H	X	X	X	X	X	X	X	X	H	X	L	H	H	H	H	H	H	H	H	H
Hold	H	H	X	X	X	X	X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	H
Preset	L	L	H	H	L	L	L	L	L	L	X	┐	L	H	H	L	L	L	L	L	L	L
Count down	H	L	X	X	X	X	X	X	X	X	L	┐	L	L	H	L	L	L	L	L	L	H
	H	L	X	X	X	X	X	X	X	X	L	┐	L	H	L	L	L	L	L	L	L	H
	H	L	X	X	X	X	X	X	X	X	L	┐	L	L	L	L	L	L	L	L	L	L
	H	L	X	X	X	X	X	X	X	X	H	X	L	H	H	H	H	H	H	H	H	H
Master reset	L	L	X	X	X	X	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	L
	L	L	X	X	X	X	X	X	X	X	H	X	H	L	L	L	L	L	L	L	L	L
	L	H	X	X	X	X	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	H
	L	H	X	X	X	X	X	X	X	X	H	X	H	L	L	L	L	L	L	L	L	H
	H	L	X	X	X	X	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	L
	H	L	X	X	X	X	X	X	X	X	H	X	H	L	L	L	L	L	L	L	L	H
	H	H	X	X	X	X	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	H
	H	H	X	X	X	X	X	X	X	X	H	X	H	L	L	L	L	L	L	L	L	H

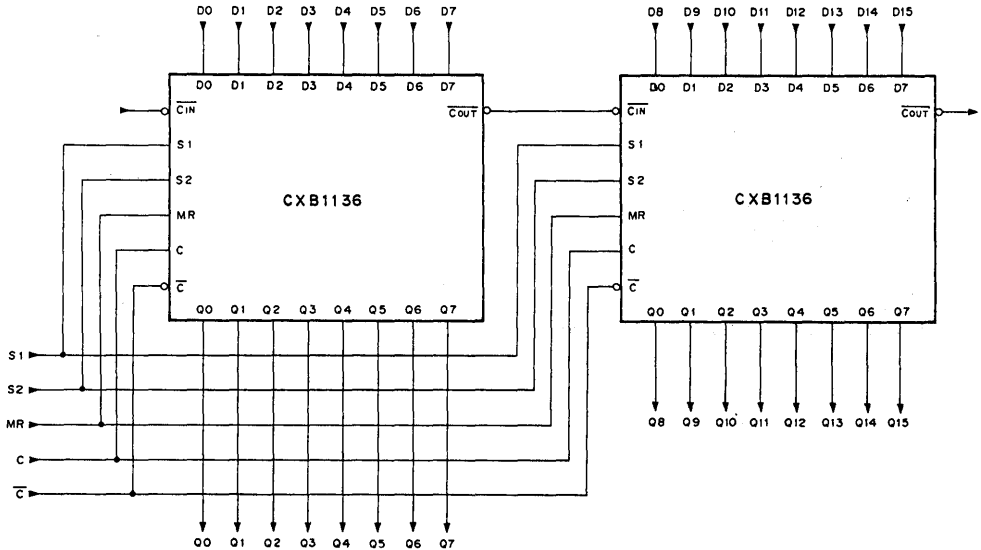
H: HIGH voltage level

L: LOW voltage level

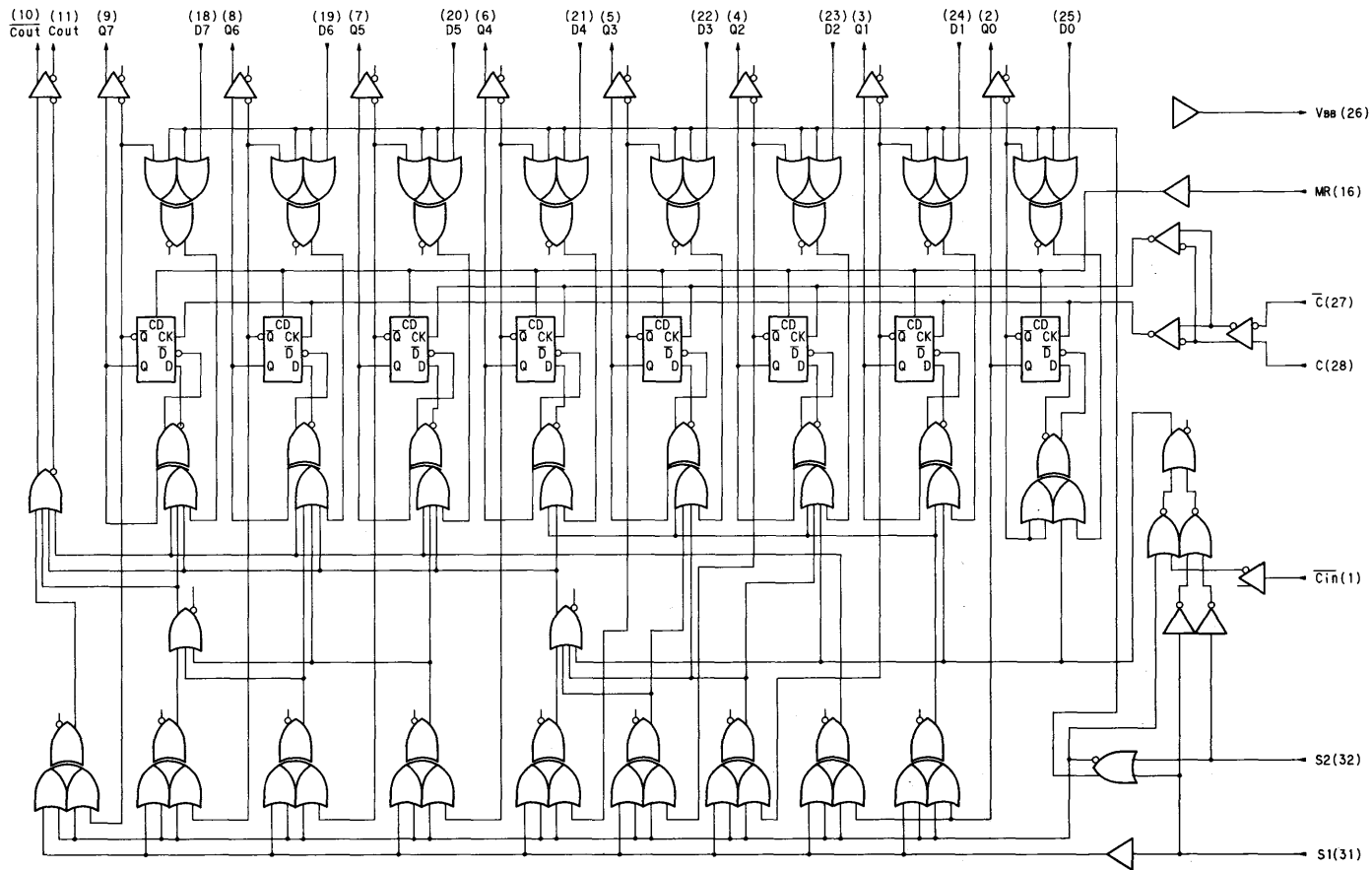
X: Don't care

┐: Positive transition edge

Typical Application — 16bit Up/Down Counter



# Block Diagram



**8-bit Shift Matrix**

**Description**

The CXB1137Q is an ultra high speed monolithic ECL 8-bit Shift Matrix. Three Select ( $S_n$ ) inputs define the number of places which an 8-bit word ( $D_n$ ) present at the inputs is shifted to the left and presented at the outputs ( $Z_n$ ). A mode control ( $M$ ) input determines the mode: "low back fill" or "barrel shifting".

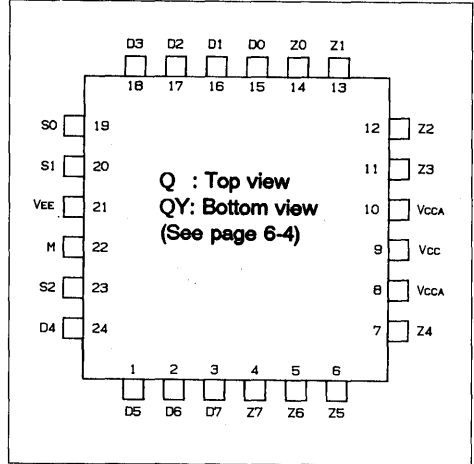
**Features**

- Typical propagation delay time 1.45ns ( $D$  to  $Z_n$ )
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

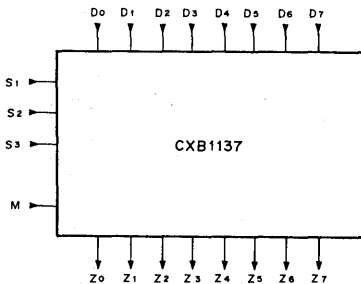
**Pin Names**

$D_n$	Word inputs
$S_n$	Shift control inputs
$M$	Mode select input
$Z_n$	Data outputs
$V_{CC}$	Circuit ground
$V_{CCA}$	Circuit ground for output
$V_{EE}$	Negative voltage supply

**Pin Assignment**



**Logic Symbol**





**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-178	-131	-92	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	Dn	Zn		1020	1450	1840	ps
	$T_{PHL}$				760	1100	1400	
	$T_{PLH}$	S0			1010	1340	1700	
	$T_{PHL}$				980	1310	1660	
	$T_{PLH}$	S1, S2			990	1320	1680	
	$T_{PHL}$				920	1230	1560	
	$T_{PLH}$	M			830	1110	1410	
	$T_{PHL}$				810	1080	1370	
Rise time	$T_{TLH}$	Dn, Sn, M		20% to 80%		400	510	
Fall time	$T_{THL}$					340	430	

Note: AC test circuit; See page 4-3.

**Truth Table**

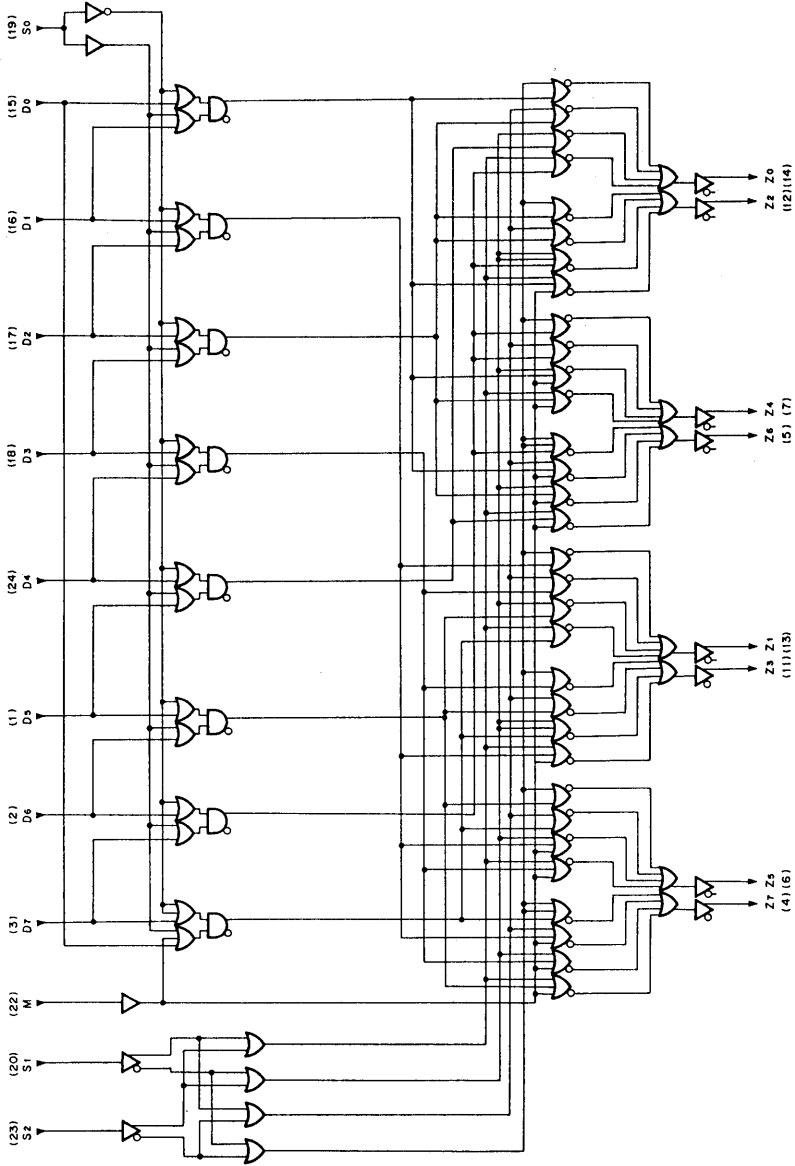
Inputs				Outputs							
M	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	Z <sub>0</sub>	Z <sub>1</sub>	Z <sub>2</sub>	Z <sub>3</sub>	Z <sub>4</sub>	Z <sub>5</sub>	Z <sub>6</sub>	Z <sub>7</sub>
X	L	L	L	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
L	H	L	L	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	L
L	L	H	L	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	L	L
L	H	H	L	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	L	L	L
L	L	L	H	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	L	L	L	L
L	H	L	H	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	L	L	L	L	L
L	L	H	H	D <sub>6</sub>	D <sub>7</sub>	L	L	L	L	L	L
L	H	H	H	D <sub>7</sub>	L	L	L	L	L	L	L
H	H	L	L	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>
H	L	H	L	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>
H	H	H	L	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>
H	L	L	H	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
H	H	L	H	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>
H	L	H	H	D <sub>6</sub>	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>
H	H	H	H	D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>

H : HIGH voltage level

L : LOW voltage level

X : Don't care

Block Diagram



## 4-bit Arithmetic Logic Unit (ALU)

### Description

The CXB1138Q is an ultra high speed monolithic ECL IC, which contains an 8-bit Arithmetic Logic Unit capable of 16 arithmetic operations on two 4-bit words.

Arithmetic logic operations are selected by function Select (S0-S3) inputs as indicated in Function Table. This IC uses internal look-ahead carry to minimize delay to the Function (Fn) output and to the ripple Carry (CN+4) output.

Group Carry Generate (Gg) and Group Carry Propagate (Pg) are provided to obtain fast operation on very long words in combination with the CXB1111Q Look-Ahead Carry Generator.

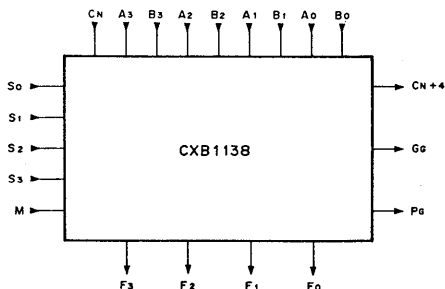
### Features

- Typical propagation delay time 1.44ns (Bn to Fn)
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

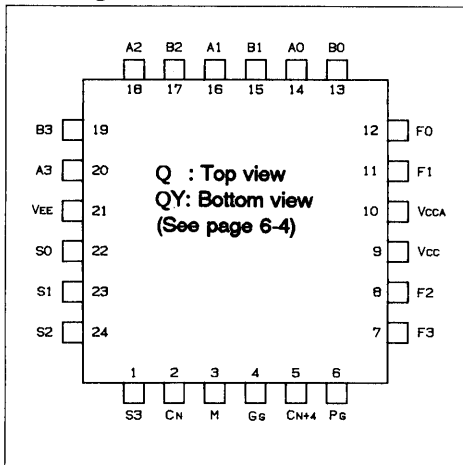
### Pin Names

An-Bn	Word A and B operand inputs
CN	Carry input
M	Mode select input
Sn	Function Select inputs
Fn	Function outputs
CN+4	Carry output
Gg	Group carry Generate output
Pg	Group carry Propagate output
Vcc	Circuit ground
VCCA	Circuit ground for output
VEE	Negative voltage supply

### Logic Symbol



### Pin Assignment



**DC Characteristics**

$$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } +85^\circ C$$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-175	-129	-90	mA

Note: Other DC characteristics: See pages 3-3 and 3-4.

**AC Characteristics**

$$V_{EE} = -4.5 \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } +85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	Bn	Fn	20% to 80%	700	1440	1830	ps
	$T_{PHL}$				820	1370	1740	
	$T_{PLH}$		Pg		750	1000	1270	
	$T_{PHL}$				910	1210	1540	
	$T_{PLH}$	Bo	Gg		790	1050	1330	
	$T_{PHL}$				980	1310	1660	
	$T_{PLH}$		C <sub>N+4</sub>		890	1180	1500	
	$T_{PHL}$				990	1320	1680	
Rise time	$T_{TLH}$	All Inputs	All Outputs		500	630		
Fall time	$T_{THL}$				400	510		

Note: AC test circuit; See page 4-3.

All output pins are left open except measured output pins.

**Function Table**

**1. Positive Logic**

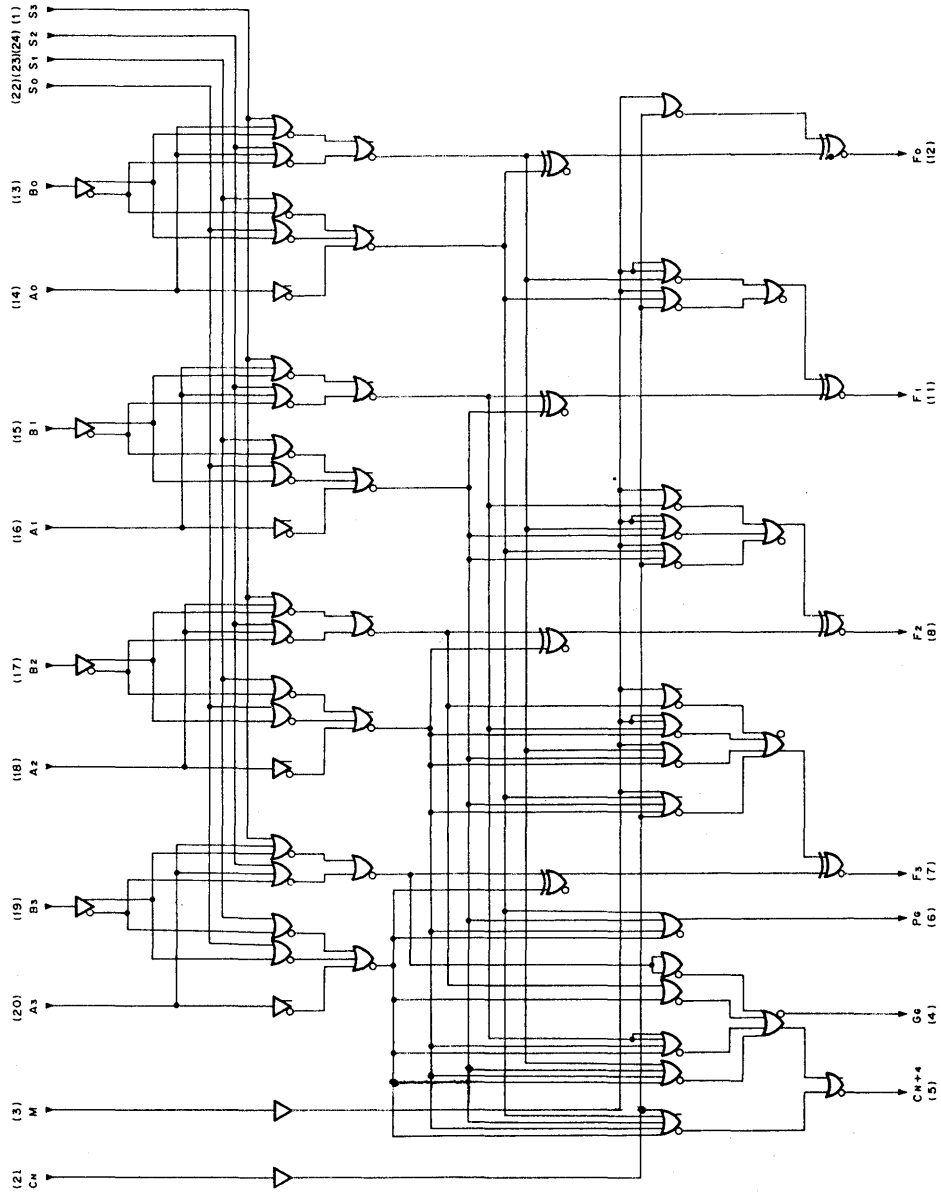
Function select				Logic function (M= "H") F	Arithmetic operation (M= "L", C <sub>N</sub> = "L") F
S3	S2	S1	S0		
L	L	L	L	$F=\bar{A}$	$F=A+0$
L	L	L	H	$F=\bar{A}+\bar{B}$	$F=A+(A\cdot\bar{B})$
L	L	H	L	$F=\bar{A}+B$	$F=A+(A\cdot B)$
L	L	H	H	F= "H"	$F=A\times 2$
L	H	L	L	$F=\bar{A}\cdot\bar{B}$	$F=(A+B)+0$
L	H	L	H	$F=\bar{B}$	$F=(A+B)+(A\cdot\bar{B})$
L	H	H	L	$F=\bar{A}\oplus\bar{B}$	$F=A+B$
L	H	H	H	$F=A+\bar{B}$	$F=A+(A+B)$
H	L	L	L	$F=\bar{A}\cdot B$	$F=(A+\bar{B})+0$
H	L	L	H	$F=A\oplus B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A+\bar{B})+(A\cdot B)$
H	L	H	H	$F=A+B$	$F=(A+\bar{B})+A$
H	H	L	L	F= "L"	$F=-1$ (two's complement)
H	H	L	H	$F=A\cdot\bar{B}$	$F=(A\cdot\bar{B})-1$
H	H	H	L	$F=A\cdot B$	$F=(A\cdot B)-1$
H	H	H	H	$F=A$	$F=A-1$

**2. Negative Logic**

Function select				Logic function (M= "H") F	Arithmetic operation (M= "L", C <sub>N</sub> = "H") F
S3	S2	S1	S0		
L	L	L	L	$F=\bar{A}$	$F=A-1$
L	L	L	H	$F=\bar{A}+\bar{B}$	$F=A+(A+\bar{B})$
L	L	H	L	$F=\bar{A}\cdot B$	$F=A+(A+B)$
L	L	H	H	F= "L"	$F=A\times 2$
L	H	L	L	$F=\bar{A}\cdot\bar{B}$	$F=(A\cdot B)-1$
L	H	L	H	$F=\bar{B}$	$F=(A\cdot B)+(A+\bar{B})$
L	H	H	L	$F=A\oplus B$	$F=A+B$
L	H	H	H	$F=A\cdot\bar{B}$	$F=A+(A\cdot B)$
H	L	L	L	$F=\bar{A}+B$	$F=(A\cdot\bar{B})-0$
H	L	L	H	$F=\bar{A}\oplus\bar{B}$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A\cdot\bar{B})+(A+B)$
H	L	H	H	$F=A\cdot B$	$F=(A\cdot\bar{B})+A$
H	H	L	L	F= "H"	$F=-1$ (two's complement)
H	H	L	H	$F=A+\bar{B}$	$F=(A+\bar{B})+0$
H	H	H	L	$F=A+B$	$F=(A+B)+0$
H	H	H	H	$F=A$	$F=A+0$

H: HIGH voltage level  
L: LOW voltage level

Block Diagram



Typical Application

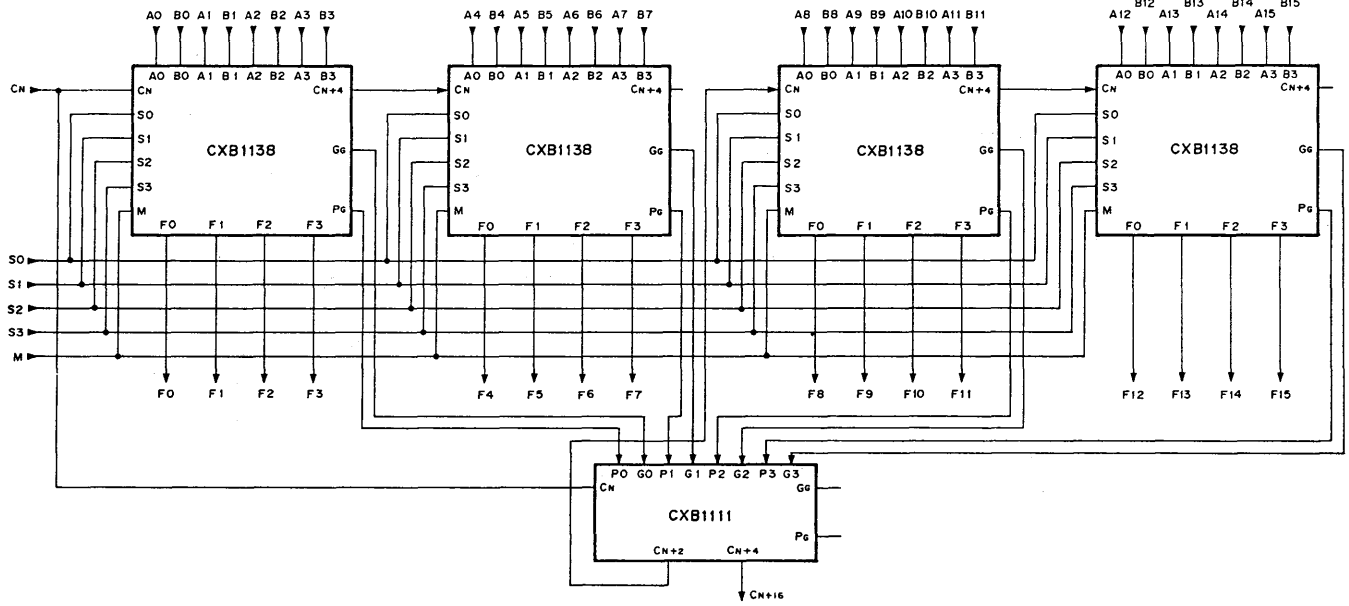


Figure 1. 16-bit ALU with Carry Look Ahead

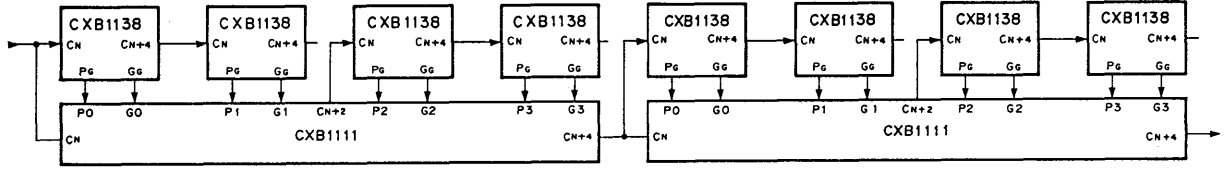


Figure 2. 32-bit ALU with Carry Look Ahead





Programmable Delay Line/Duty Cycle Controller

**Description**

The CXB1139Q is an ultra high speed monolithic ECL Delay Line/Duty Cycle Controller IC.

Five binary inputs, S<sub>0</sub> to S<sub>4</sub>, program the delay time from input D<sub>IN</sub> to output Q<sub>d</sub> in 23 steps. Binary input code 00001 through 00110 provides a delay of 125ps for each increment of the code, while 00111 through 10111 provides a delay of 190ps for each step.

A pulse with plus (long) duty cycle is provided at output Q<sub>p</sub>, and a pulse with minus (short) duty cycle at output Q<sub>m</sub>. The duty cycle is also controlled by the input data.

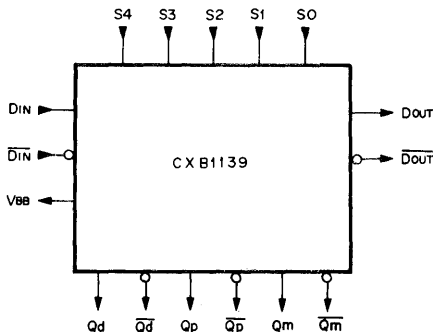
**Features**

- Programmable delay time: 775ps to 4650ps
- Programmable duty cycle
- Plus and minus duty cycle outputs
- Typical AC characteristics : T<sub>TLH</sub>=230ps  
T<sub>THL</sub>=195ps
- Differential data input and output
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

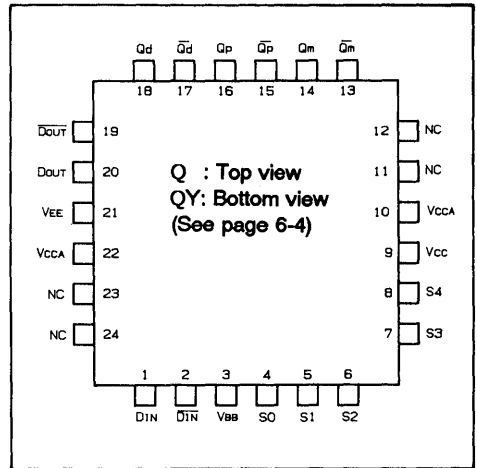
**Pin Names**

D <sub>IN</sub> , $\overline{D}_{IN}$	Data inputs
S <sub>n</sub>	Digital data inputs
D <sub>OUT</sub> , $\overline{D}_{OUT}$	Buffered data outputs
Q <sub>d</sub> , $\overline{Q}_d$	Delayed data outputs
Q <sub>p</sub> , $\overline{Q}_p$	Plus duty cycle outputs
Q <sub>m</sub> , $\overline{Q}_m$	Minus duty cycle outputs
V <sub>BB</sub>	Reference voltage output
V <sub>CC</sub>	Circuit ground
V <sub>CCA</sub>	Circuit ground for outputs
V <sub>EE</sub>	Negative power supply

**Logic Symbol**



**Pin Assignment**



**DC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-198	-144	-100	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

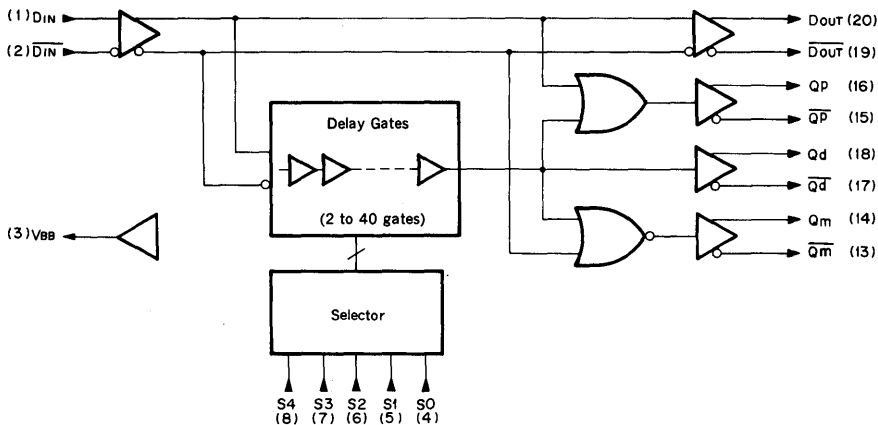
**AC Characteristics**

$V_{EE} = -4.5 \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{dLH}$	D <sub>IN</sub>	Q <sub>d</sub>	$S_0 = HIGH$ $S_1 - S_4 = LOW$	620	775	970	ps
	$T_{dHL}$			$S_4 = S_2 = S_1$ $= S_0 = HIGH$ $S_3 = LOW$	610	760	950	
	$T_{dLH}$				4220	4650	5050	
	$T_{dLH}$				4220	4650	5050	
	$T_{OLH}$		D <sub>OUT</sub>		350	440	550	
	$T_{OHL}$				345	430	540	
	$T_{PLH}$		Q <sub>p</sub>	$S_0 = HIGH$ $S_1 - S_4 = LOW$	510	640	800	
	$T_{PHL}$				500	630	785	
	$T_{MLH}$		Q <sub>m</sub>	$S_4 = S_2 = S_1$ $= S_0 = HIGH$ $S_3 = LOW$	520	650	810	
	$T_{MHL}$				510	640	800	
Rise time	$T_{TLH}$	Q <sub>d</sub> , D <sub>OUT</sub> Q <sub>p</sub> , Q <sub>m</sub>		20% to 80%		230	285	
Fall time	$T_{THL}$					195	245	
Minimum pulse width	$T_{pw}$	Q <sub>m</sub>		$S_0 = HIGH$ $S_1 - S_4 = LOW$	247	265	285	
Jitter ( $\sigma$ )	$T_{uc}$	Q <sub>d</sub>		$S_4 = S_2 = S_1$ $= S_0 = HIGH$ $S_3 = LOW$		5	12	

Note: AC test circuit; See page 4-3.

Block Diagram



Truth Table

N	Input					Number of Gate	Output: Qd
	S4	S3	S2	S1	S0		Typical Delay
0	L	L	L	L	L		Qd=LOW
1	L	L	L	L	H	2	775ps
2	L	L	L	H	L	3	915ps
3	L	L	L	H	H	4	1015ps
4	L	L	H	L	L	5	1175ps
5	L	L	H	L	H	6	1305ps
6	L	L	H	H	L	7	1405ps
7	L	L	H	H	H	8	1595ps
8	L	H	L	L	L	10	1795ps
9	L	H	L	L	H	12	2010ps
10	L	H	L	H	L	14	2165ps
11	L	H	L	H	H	16	2385ps

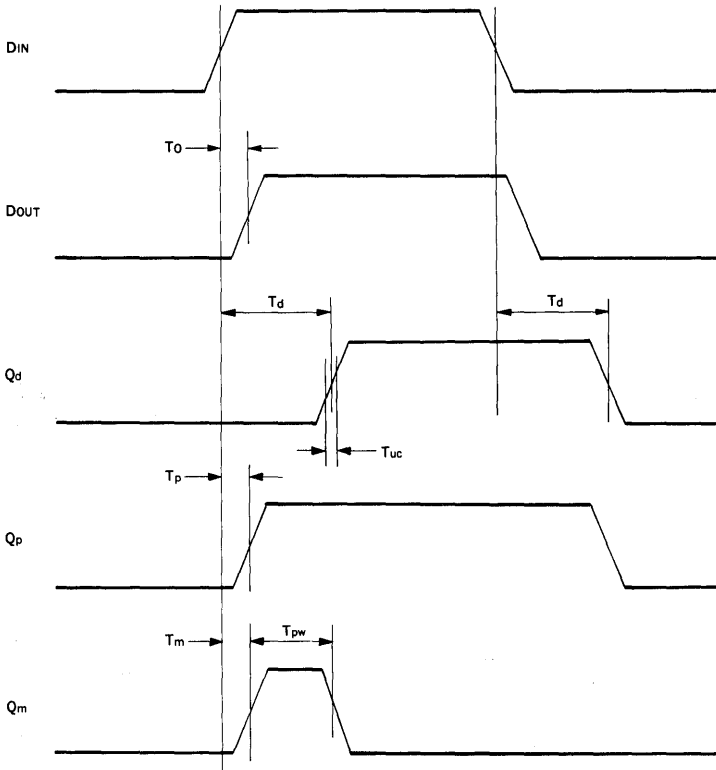
N	Input					Number of Gate	Output: Qd
	S4	S3	S2	S1	S0		Typical Delay
12	L	H	H	L	L	18	2580ps
13	L	H	H	L	H	20	2800ps
14	L	H	H	H	L	22	2950ps
15	L	H	H	H	H	24	3165ps
16	H	L	L	L	L	26	3295ps
17	H	L	L	L	H	28	3510ps
18	H	L	L	H	L	30	3665ps
19	H	L	L	H	H	32	3880ps
20	H	L	H	L	L	34	4080ps
21	H	L	H	L	H	36	4295ps
22	H	L	H	H	L	38	4455ps
23	H	L	H	H	H	40	4650ps

Typical delay time is calculated approximately by formula ;

$$T_d = (650 + 125N \pm 50) \text{ps} \pm 7\% \quad (N \leq 6)$$

$$T_d = (1400 + 190(N - 6) \pm 90) \text{ps} \pm 7\% \quad (7 \leq N \leq 23)$$

Timing Diagram



$$T_d \approx (650 + 125N \pm 50\text{ps}) \pm 7\% \quad (N \leq 6)$$

$$T_d \approx \{1400 + 190(N - 6) \pm 90\text{ps}\} \pm 7\% \quad (7 \leq N \leq 23)$$

$$D_{out}(T) = D_{in}(T - T_o)$$

$$Q_d(T) = D_{in}(T - T_d)$$

$$Q_p(T) = D_{out}(T) + Q_d(T)$$

$$Q_m(T) = D_{out}(T) \cdot Q_d(T)$$

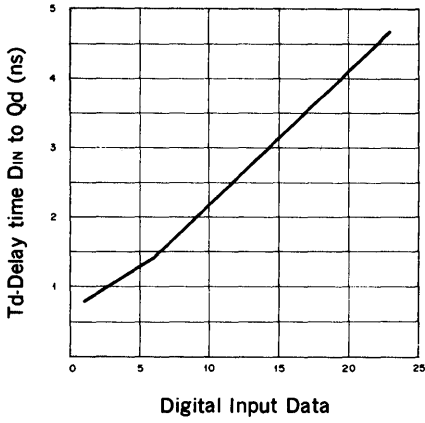


Figure1. Input Data vs. Delay Time

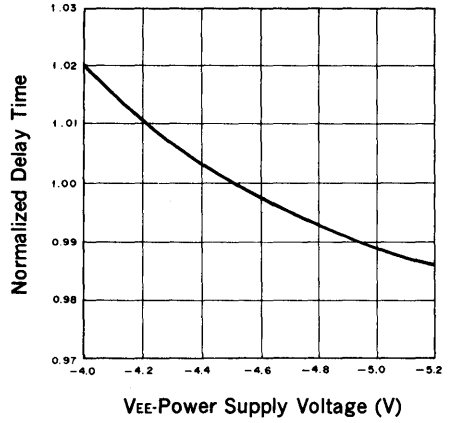


Figure2. Change in Delay Time vs. Change in Supply Voltage

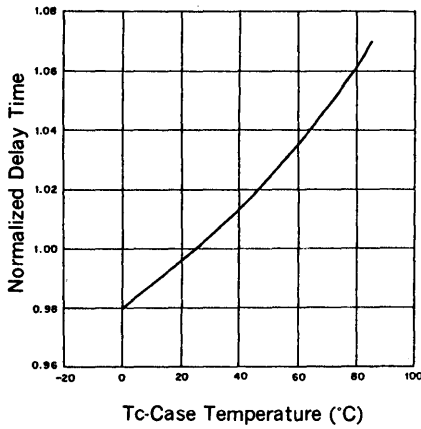


Figure3. Change in Delay Time vs. Change in Case Temperature

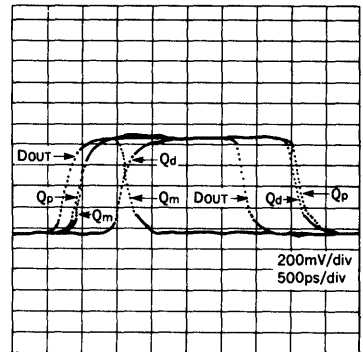


Figure4. Output Wave Forms (N=4)



**Hex 2 : 1 Multiplexer with Latch**

**Description**

The CXB1140Q is an ultra high speed monolithic ECL IC, which contains six 2 : 1 multiplexers with transparent Latched outputs. The data select (SEL) input determines which data input is enabled. When both Latch enable (LEN1, LEN2) inputs are LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

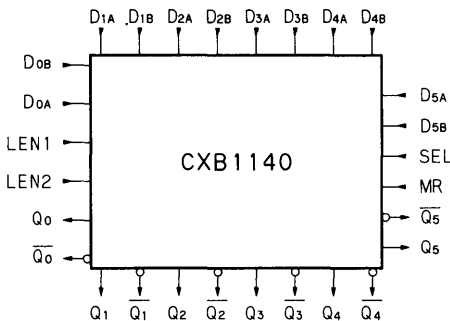
**Features**

- Typical propagation delay time:  
Tpd=780ps (Dn to Qn)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

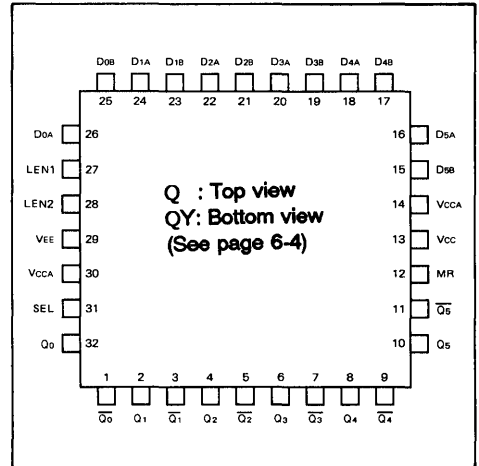
**Pin Names**

- DnA, DnB Data inputs
- Qn, Qn Data outputs
- SEL Data Select input
- LENn Latch enable inputs
- MR Direct Master Reset input
- Vcc Circuit ground
- VCCA Circuit ground for outputs
- VEE Negative power supply

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select input	Outputs
SEL	Qn
L	DnA
H	DnB

Inputs		Latch
LEN1	LEN2	
L	L	Transparent
H	X	Latch
X	H	Latch

Note : H ; HIGH voltage Level  
L ; LOW voltage Level  
X ; Don't care



**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-133	-98	-68	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

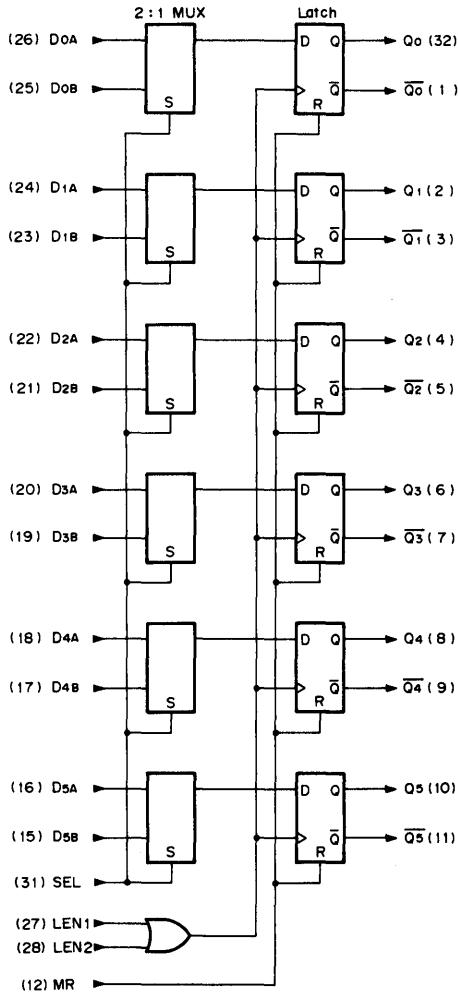
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_t = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	$T_{PLH}$	$D_{nA}$	$Q_n$	$LEN_n=L$	570	770	1000	ps
	$T_{PHL}$	$D_{nB}$			580	780	1020	
	$T_{PLH}$	SEL			700	940	1220	
	$T_{PHL}$				720	960	1250	
	$T_{PLH}$	$LEN_n$		640	860	1120		
	$T_{PHL}$			640	860	1120		
	$T_{PLH}$	MR		700	930	1210		
	$T_{PHL}$			670	900	1170		
Gate-to-Gate skew	$T_{SG-G}$	$D_{nA}$ , $D_{nB}$		$LEN_n=L$		60	100	
Set Up time	$T_s$	$D$ , $LEN_n$			80			
		SEL, $LEN_n$			320			
Hold time	$T_h$	$LEN_n$ , $D$			170			
		$LEN_n$ , SEL			-70			
Release time	$T_r$	MR, $LEN_n$			310			
Min. Pulse width	$T_{PW}$	MR			430			
Rise time	$T_{TLH}$	$D_{nA}$		20% to 80%		290	380	
Fall time	$T_{THL}$	$D_{nB}$		20% to 80%		270	340	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Hex 2 : 1 Multiplexer with D-FF**

**Description**

The CXB1141Q is an ultra high speed monolithic ECL IC, which contains six 2 : 1 multiplexers followed by D type flip flops. The data select (SEL) input determines which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clock (C1,C2) inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

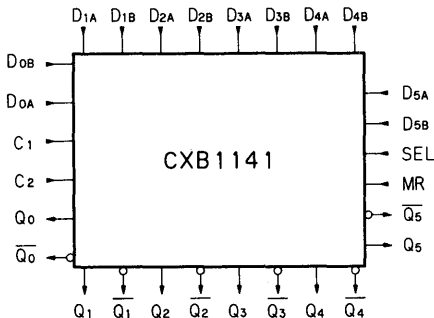
**Features**

- Typical clock rate up to 2.6 GHz
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

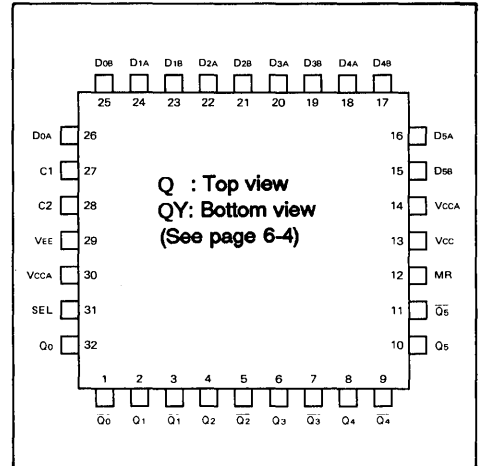
**Pin Names**

- |          |                            |
|----------|----------------------------|
| DnA, DnB | Data inputs                |
| Qn, Qn   | Data outputs               |
| SEL      | Data select input          |
| Cn       | Clock inputs               |
| MR       | Direct Master Reset input  |
| Vcc      | Circuit ground             |
| VCCA     | Circuit ground for outputs |
| VEE      | Negative power supply      |

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select input	Outputs
SEL	Qn
L	DnA
H	DnB

Note : H ; HIGH voltage Level  
L ; LOW voltage Level

**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	$I_{EE}$		-196	-144	-100	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

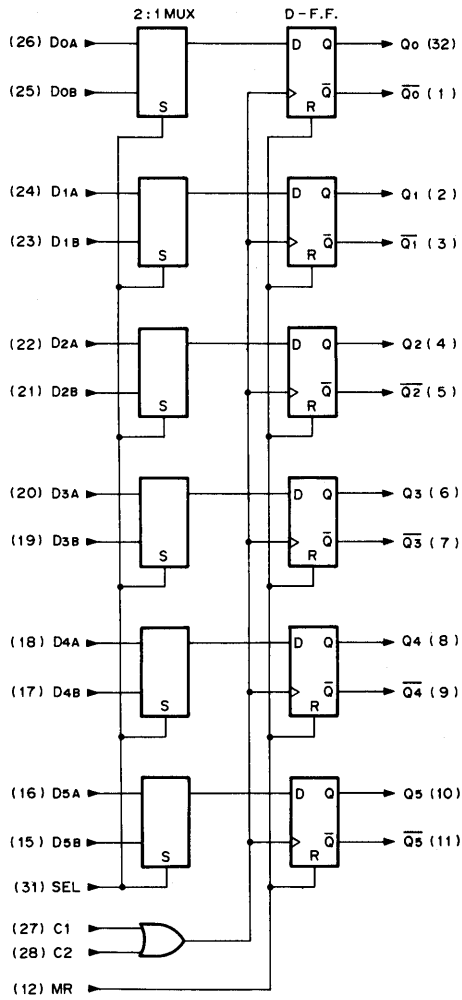
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit			
Propagation delay time	$T_{PLH}$	Cn	Qn		650	870	1130	ps			
	$T_{PHL}$				670	900	1170				
	$T_{PLH}$	MR			780	1050	1370				
	$T_{PHL}$				780	1050	1370				
Gate-to-Gate skew	$T_{SG-G}$	Cn					50		100		
Set up time	$T_s$	D, Cn					100				
		SEL, Cn					300				
Hold time	$T_h$	Cn, D					150				
		Cn, SEL					-50				
Release time	$T_r$	MR, Cn					340				
Min. Pulse width	$T_{PW}$	MR			610						
Max. Clock frequency	$f_{MAX}$				2.0	2.6		GHz			
Rise time	$T_{TLH}$	Cn		20% to 80%		320	420	ps			
Fall time	$T_{THL}$					290	380				

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Quad 4 : 1 Multiplexer with Latch**

**Description**

The CXB1142Q is an ultra high speed monolithic ECL IC, which contains four 4 : 1 multiplexers with transparent Latched outputs. The data select (S<sub>0</sub>, S<sub>1</sub>) inputs determine which data input is enabled. When Latch enable (LEN) input is LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable input. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

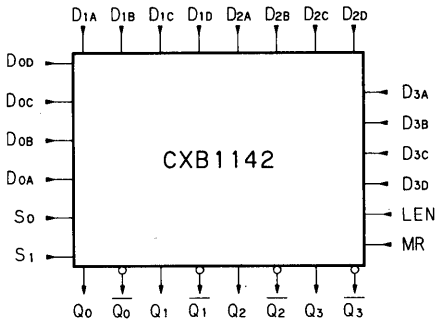
**Features**

- Typical propagation delay time:  
T<sub>pd</sub>=830ps (D<sub>nA</sub>-D<sub>nD</sub> to Q<sub>n</sub>)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

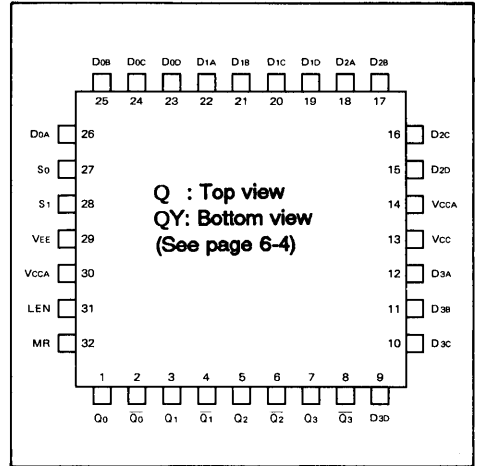
**Pin Names**

- D<sub>nA</sub> - D<sub>nD</sub>, Data inputs
- Q<sub>n</sub>,  $\overline{Q}_n$  Data outputs
- S<sub>n</sub> Data select inputs
- LEN Latch enable input
- MR Direct Master Reset input
- V<sub>CC</sub> Circuit ground
- V<sub>CCA</sub> Circuit ground for outputs
- V<sub>EE</sub> Negative power supply

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select inputs		Outputs
S <sub>0</sub>	S <sub>1</sub>	Q <sub>n</sub>
L	L	D <sub>nA</sub>
H	L	D <sub>nB</sub>
L	H	D <sub>nC</sub>
H	H	D <sub>nD</sub>

Note : H ; HIGH voltage Level  
L ; LOW voltage Level



**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-125	-92	-64	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

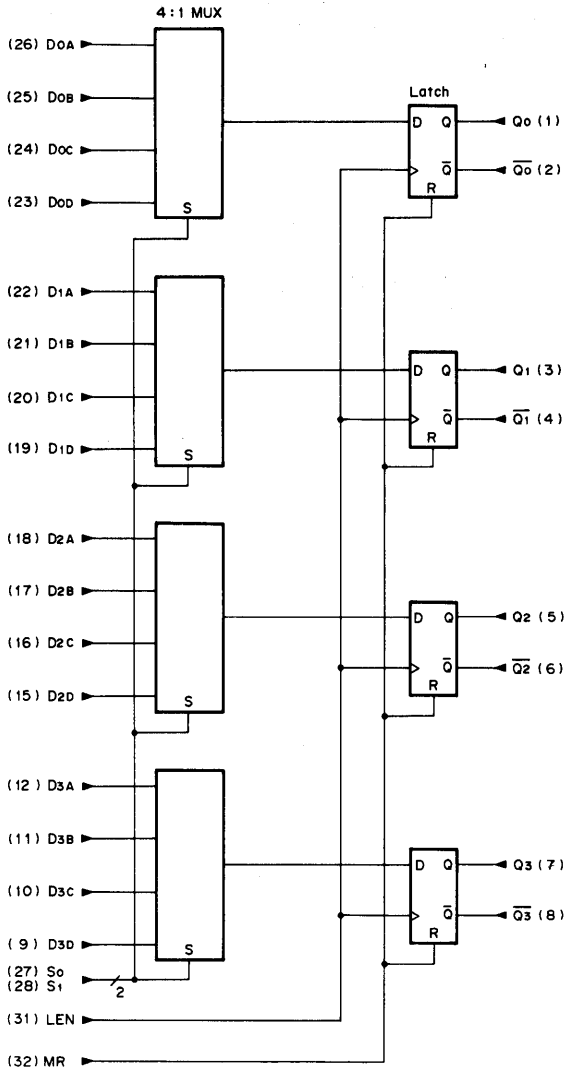
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_c = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T <sub>PLH</sub>	D <sub>nA</sub> to D <sub>nD</sub>	Q <sub>n</sub>	LEN=L	610	820	1070	ps
	T <sub>PHL</sub>				620	830	1080	
	T <sub>PLH</sub>	S <sub>n</sub>			780	1050	1370	
	T <sub>PHL</sub>				800	1070	1390	
	T <sub>PLH</sub>	LEN		650	870	1130		
	T <sub>PHL</sub>			660	880	1140		
	T <sub>PLH</sub>	MR		770	1030	1340		
	T <sub>PHL</sub>			790	1060	1380		
Gate-to-Gate skew	T <sub>SG-G</sub>	D		LEN=L		60	100	
Set up time	T <sub>S</sub>	D, LEN			150			
		S <sub>n</sub> , LEN			390			
Hold time	T <sub>H</sub>	LEN, D			100			
		LEN, S <sub>n</sub>			140			
Release time	T <sub>R</sub>	MR, LEN			340			
Min. Pulse width	T <sub>PW</sub>	MR			520			
Rise time	T <sub>TLH</sub>	D		20% to 80%		250	330	
Fall time	T <sub>THL</sub>						240	320

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Quad 4 : 1 Multiplexer with D-FF**

**Description**

The CXB1143Q is an ultra high speed monolithic ECL IC, which contains four 4 : 1 multiplexers followed by D type flip flops. The data select (S<sub>0</sub>, S<sub>1</sub>) inputs determine which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clock (C) input. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

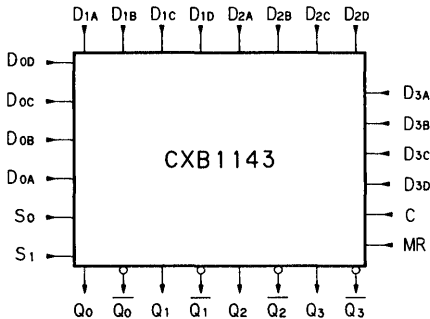
**Features**

- Typical clock rate up to 2.6 GHz
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

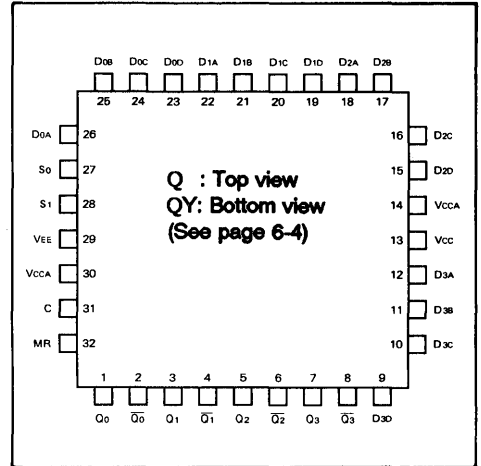
**Pin Names**

- |                                   |                            |
|-----------------------------------|----------------------------|
| D <sub>1A</sub> —D <sub>1D</sub>  | Data inputs                |
| Q <sub>n</sub> , $\overline{Q}_n$ | Data outputs               |
| S <sub>n</sub>                    | Data select inputs         |
| C                                 | Clock input                |
| MR                                | Direct Master Reset input  |
| V <sub>CC</sub>                   | Circuit ground             |
| V <sub>CCA</sub>                  | Circuit ground for outputs |
| V <sub>EE</sub>                   | Negative power supply      |

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select inputs		Outputs
S <sub>0</sub>	S <sub>1</sub>	Q <sub>n</sub>
L	L	D <sub>nA</sub>
H	L	D <sub>nB</sub>
L	H	D <sub>nC</sub>
H	H	D <sub>nD</sub>

Note : H ; HIGH voltage Level  
L ; LOW voltage Level

**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-177	-130	-90	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

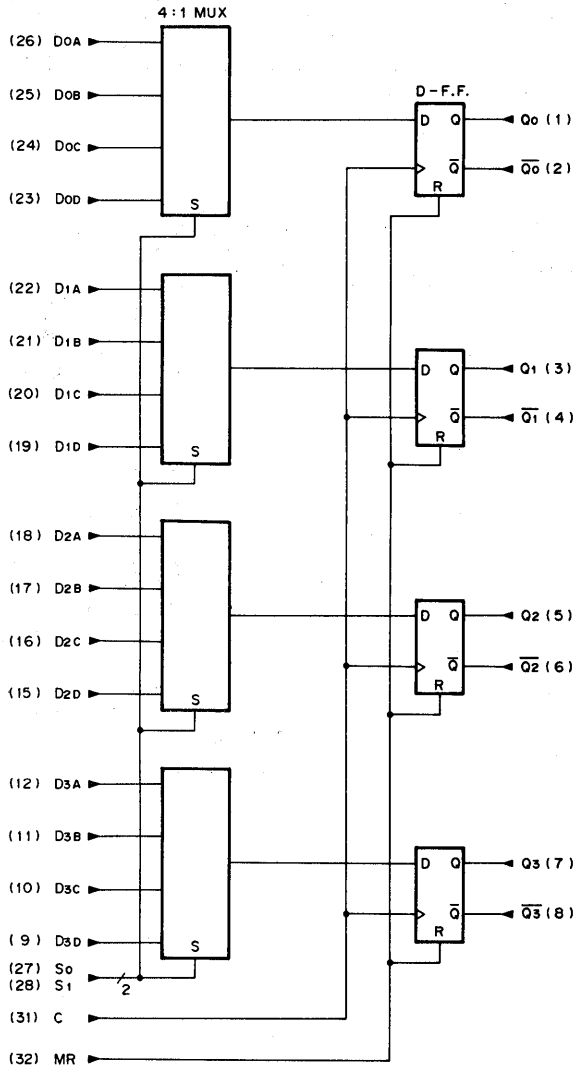
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit		
Propagation delay time	T <sub>PLH</sub>	C	Q <sub>n</sub>		630	840	1090	ps		
	T <sub>PHL</sub>				660	880	1150			
	T <sub>PLH</sub>	MR			770	1030	1340			
	T <sub>PHL</sub>				780	1050	1370			
Gate-to-Gate skew	T <sub>SG-G</sub>	C					30		80	
Set up time	T <sub>S</sub>	D, C				200				
		SEL, C				450				
Hold time	T <sub>H</sub>	C, D				50				
		C, SEL		-200						
Release time	T <sub>R</sub>	MR, C		260						
Min. Pulse width	T <sub>PW</sub>	MR		390						
Max. Clock frequency	f <sub>MAX</sub>			2.0	2.6		GHz			
Rise time	T <sub>TLH</sub>	C		20% to 80%	250	330				
Fall time	T <sub>THL</sub>				200	260	ps			

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Dual 8 : 1 Multiplexer with Latch**

**Description**

The CXB1144Q is an ultra high speed monolithic ECL IC, which contains two 8 : 1 multiplexers with transparent Latched outputs. The data select (S<sub>0</sub>-S<sub>2</sub>) inputs determine which data input is enabled. When both Latch enable (LEN1, LEN2) inputs are LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

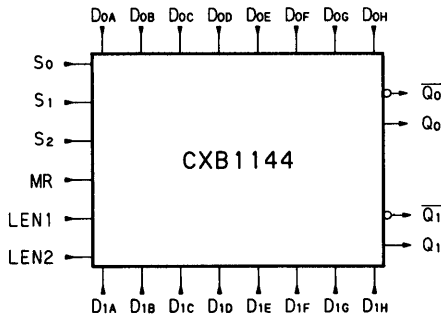
**Features**

- Typical propagation delay time:  
T<sub>pd</sub>=1000 ps (D<sub>nA</sub>-D<sub>nH</sub> to Q<sub>n</sub>)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

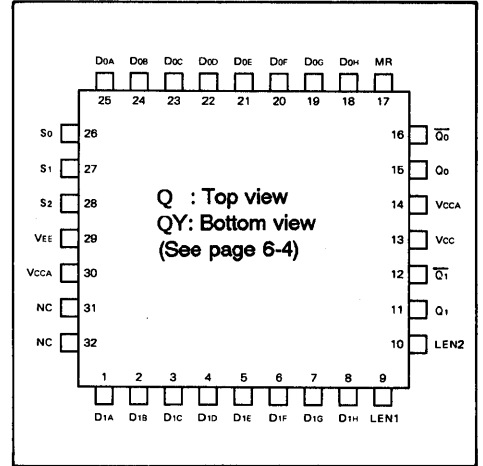
**Pin Names**

- |                                  |                            |
|----------------------------------|----------------------------|
| D <sub>nA</sub> -D <sub>nH</sub> | Data inputs                |
| Q <sub>n</sub> , Q <sub>n</sub>  | Data outputs               |
| S <sub>n</sub>                   | Data select inputs         |
| LEN <sub>n</sub>                 | Latch enable inputs        |
| MR                               | Direct Master Reset input  |
| V <sub>CC</sub>                  | Circuit ground             |
| V <sub>CCA</sub>                 | Circuit ground for outputs |
| V <sub>EE</sub>                  | Negative power supply      |

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select inputs			Outputs
S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	Q <sub>n</sub>
L	L	L	D <sub>nA</sub>
H	L	L	D <sub>nB</sub>
L	H	L	D <sub>nC</sub>
H	H	L	D <sub>nD</sub>
L	L	H	D <sub>nE</sub>
H	L	H	D <sub>nF</sub>
L	H	H	D <sub>nG</sub>
H	H	H	D <sub>nH</sub>

Inputs		Operation
LEN1	LEN2	
L	L	Transparent
H	X	Latch
X	H	Latch

Note : H ; HIGH voltage Level  
L ; LOW voltage Level  
X ; Don't care



**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-102	-75	-52	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

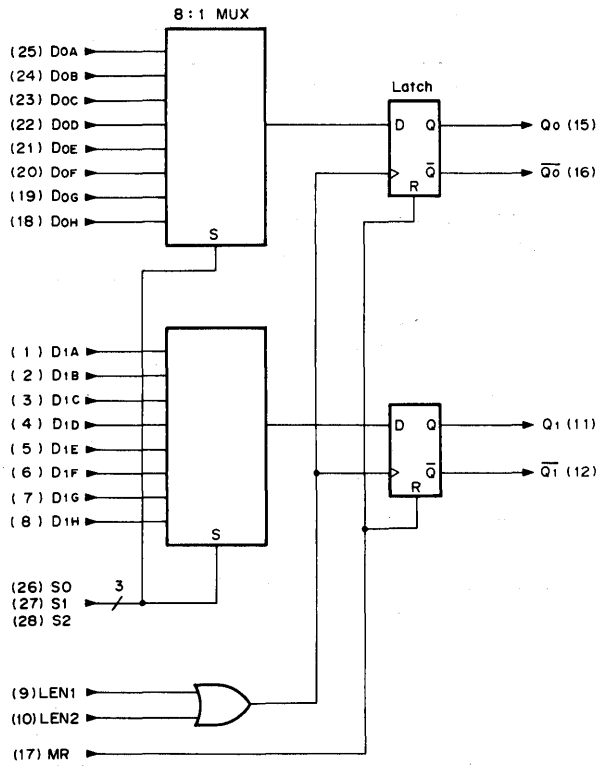
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TT} = -2.0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $R_T = 50\Omega$  to  $V_{TT}$

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T <sub>PLH</sub>	D <sub>NA</sub> to D <sub>NH</sub>	Q <sub>n</sub>	LEN1=L LEN2=L	710	950	1240	ps
	T <sub>PHL</sub>				750	1000	1300	
	T <sub>PLH</sub>	S <sub>n</sub>			900	1200	1560	
	T <sub>PHL</sub>				920	1230	1600	
	T <sub>PLH</sub>	LEN <sub>n</sub>		600	810	1060		
	T <sub>PHL</sub>			630	850	1110		
	T <sub>PLH</sub>	MR		720	970	1260		
	T <sub>PHL</sub>			740	990	1290		
Gate-to-Gate skew	T <sub>SG-G</sub>	D		LEN <sub>n</sub> =L		70	120	
Set up time	T <sub>S</sub>	D, LEN <sub>n</sub>			320			
		S <sub>n</sub> , LEN <sub>n</sub>			540			
Hold time	T <sub>H</sub>	LEN <sub>n</sub> , D			-70			
		LEN <sub>n</sub> , S <sub>n</sub>			-290			
Release time	T <sub>R</sub>	MR, LEN <sub>n</sub>			330			
Min. Pulse width	T <sub>pw</sub>	MR			550			
Rise time	T <sub>TLH</sub>	D <sub>NA</sub> to D <sub>NH</sub>		20% to 80%		300	390	
Fall time	T <sub>THL</sub>					250	330	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Dual 8 : 1 Multiplexer with D-FF**

**Description**

The CXB1145Q is an ultra high speed monolithic ECL IC, which contains two 8 : 1 multiplexers followed by D type flip flops. The data select (S<sub>0</sub>-S<sub>2</sub>) inputs determine which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clocks (C<sub>1</sub>, C<sub>2</sub>) input. The Master Reset overrides all other control inputs and turns Q outputs to LOW.

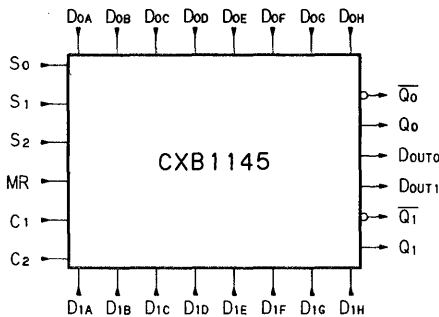
**Features**

- Typical clock rate up to 2.6 GHz
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

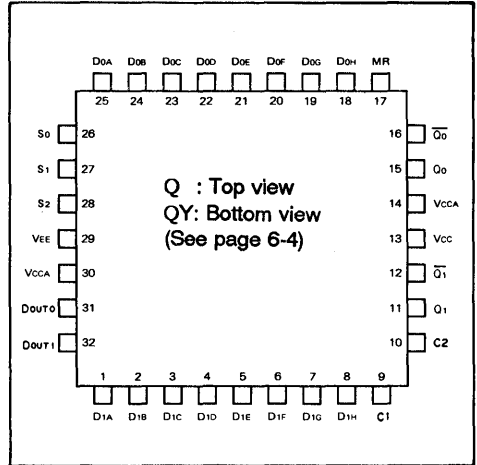
**Pin Names**

- |                                  |                            |
|----------------------------------|----------------------------|
| D <sub>nA</sub> -D <sub>nH</sub> | Data inputs                |
| Q <sub>n</sub> , Q <sub>n</sub>  | Data outputs               |
| S <sub>n</sub>                   | Data select inputs         |
| C <sub>n</sub>                   | Clock inputs               |
| Dout <sub>n</sub>                | Data sense outputs         |
| MR                               | Direct Master Reset input  |
| V <sub>CC</sub>                  | Circuit ground             |
| V <sub>CCA</sub>                 | Circuit ground for outputs |
| V <sub>EE</sub>                  | Negative power supply      |

**Logic Symbol**



**Pin Assignment**



**Truth Table**

Select inputs			Outputs
S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	Q <sub>n</sub>
L	L	L	D <sub>nA</sub>
H	L	L	D <sub>nB</sub>
L	H	L	D <sub>nC</sub>
H	H	L	D <sub>nD</sub>
L	L	H	D <sub>nE</sub>
H	L	H	D <sub>nF</sub>
L	H	H	D <sub>nG</sub>
H	H	H	D <sub>nH</sub>

Note : H ; HIGH voltage Level  
L ; LOW voltage Level

**DC Characteristics**

$V_{EE} = -4.5V \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } +85^\circ C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I <sub>EE</sub>		-130	-95	-66	mA

Note: Other DC Characteristics; See pages 3-3 and 3-4.

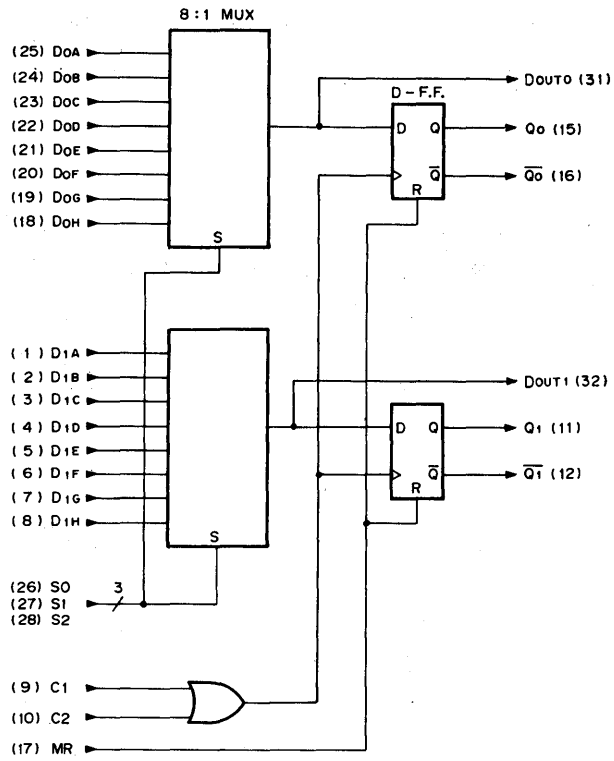
**AC Characteristics**

$V_{EE} = -4.5V \pm 0.3V, V_{CC} = V_{CCA} = GND, V_{TT} = -2.0V, T_c = 0^\circ C \text{ to } +85^\circ C, R_T = 50\Omega \text{ to } V_{TT}$

Item	Symbol	Input	Output	Test Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T <sub>PLH</sub>	Cn	Qn		570	760	990	ps
	T <sub>PHL</sub>				590	790	1030	
	T <sub>PLH</sub>	MR			710	950	1240	
	T <sub>PHL</sub>				720	970	1270	
	T <sub>PLH</sub>	D	Doutn		670	900	1170	
	T <sub>PHL</sub>				660	880	1150	
	T <sub>PLH</sub>	Sn			850	1140	1490	
	T <sub>PHL</sub>				840	1120	1460	
Gate-to-Gate skew	T <sub>SG-G</sub>	Cn			30	80		
Set up time	T <sub>S</sub>	D, Cn	Qn	330				
		Sn, Cn		520				
Hold time	T <sub>H</sub>	Cn, D		-80				
		Cn, Sn		-270				
Release time	T <sub>R</sub>	MR, Cn		380				
Min. Pulse width	T <sub>PW</sub>	MR		540				
Max. Clock frequency	f <sub>MAX</sub>			2.0	2.6		GHz	
Rise time	T <sub>TLH</sub>	Cn		20% to 80%		250	330	
Fall time	T <sub>THL</sub>				210	280	ps	

Note: AC Test Circuit; See pages 4-3, 4-4 and 4-5.

Block Diagram





**Package Data**



**Package Data**

<b>Package Data</b>		<b>Page</b>
<b>1.</b>	<b>16 pin QFP</b>	<b>6-3</b>
<b>2.</b>	<b>24 pin QFP</b>	<b>6-3</b>
<b>3.</b>	<b>32 pin QFP</b>	<b>6-3</b>
<b>4.</b>	<b>24 pin QFP with formed lead</b>	<b>6-4</b>
<b>5.</b>	<b>32 pin QFP with formed lead</b>	<b>6-4</b>

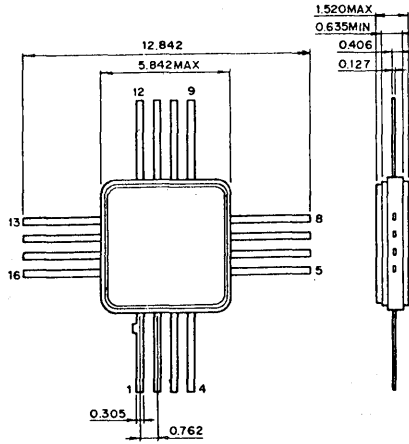


# Package Data

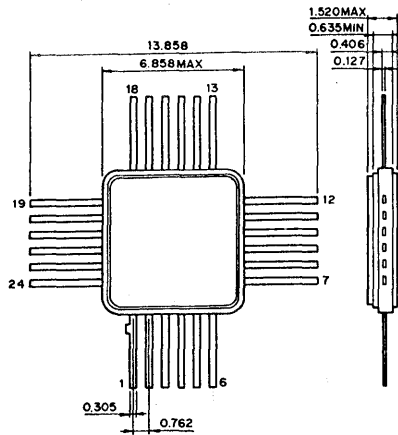
## Package Outline

Unit: mm

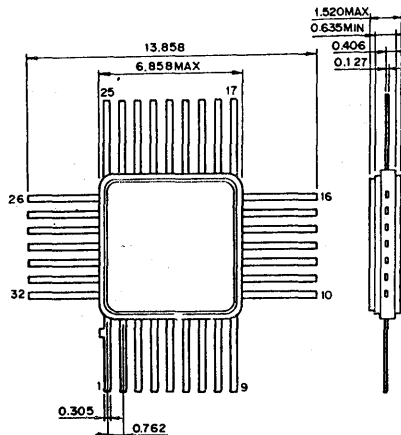
16pin QFP



24pin QFP



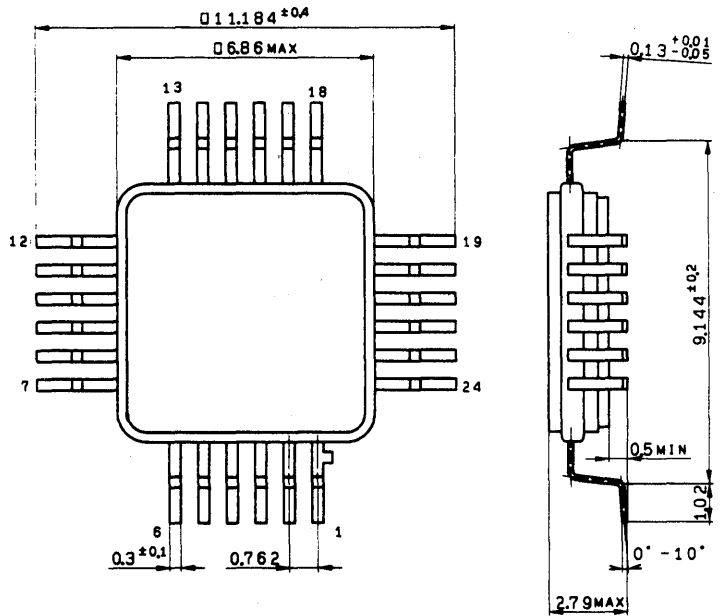
32pin QFP



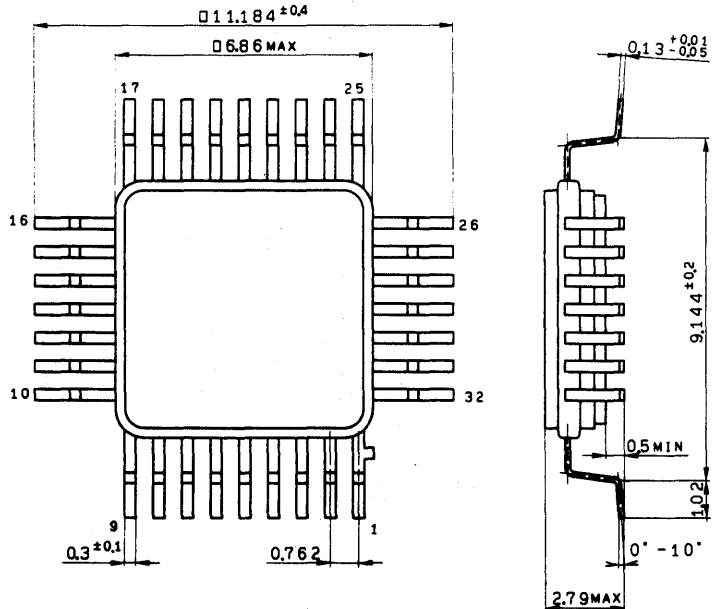
Package Outline

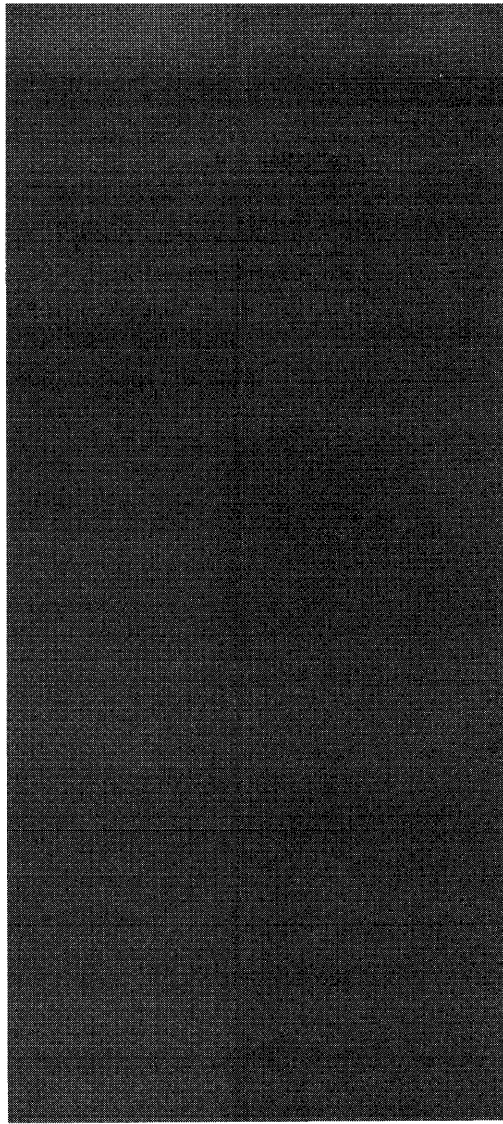
Unit: mm

24pin QFP

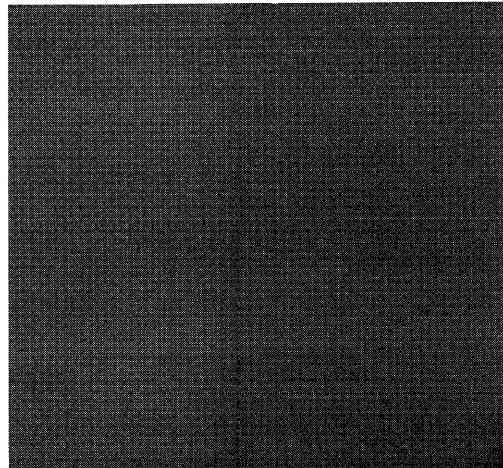


32pin QFP





**Application Note**



**Application Note**

<b>Application Note</b>	<b>Page</b>
1. Advantages of the Family Logic	7-3
2. Design Consideration	7-3
Power Supply/Ground Plane	7-3
Circuit Interconnections	7-4
Matched Impedance Termination	7-5

# Application Note

## 1. Advantages of the Family Logic

SPECL Standard Logic Family specifications can be found in both AC and DC parameters under full operating conditions. (supply voltage and operating case temperature range).

The family devices have the same features as common ECL logic IC's. That is:

- Complementary output
- Wired OR capability
- High common mode noise rejection
- Low output impedance
- High current drive capability
- High input impedance
- Low cross talk.

Furthermore, the family have the advantages over the existing ECL families in the following features.

**Low Propagation Delay:** Family devices have an internal delay time of 50ps and a pin-to-pin transition delay time of 410ps for a simple gate.

**Fast edge rate:** The rise and the fall time at the output pin are 200ps from 20% to 80% of the waveform. Very high speed transition capability makes the device applicable to data processing at GHz rate. Most ECL logic ICs to date have a limitation in data rate because of the decrease in amplitude at the output waveform.

**Complementary Input Capability:** Most of the Family devices have differential input pins for high speed signal inputs in clocks or data.

**Small time Skew:** With very small internal delay time and a careful routing design inside the chip, the time skew at the outputs is very small. For a Fanout buffer CXB1105, the time skew is 50ps at the output.

## 2. Design Consideration

As family devices have a very fast transition time, a careful design of the circuit board is required for their utilization.

### Power Supply/Ground Plane

SPECL Family devices are characterized by the Vcc at ground potential and the VEE at -4.5V.

The devices have very good noise immunity. Any noise induced on the VEE line is applied to the circuit as a common-mode signal which in turn is rejected by the differential operation of the ECL circuit. The differential input stage also provides a good noise immunity even at GHz data rate. Noise induced on the Vcc line, however, is not cancelled out that way. Hence, a good system ground at the Vcc bus line is required for best noise immunity. A circuit board should have two or three level metallizations at least, with wide ground plane to prevent voltage drop between supply and device and to produce a low source inductance.

SPECL devices have two Vcc pins. VCCA supplies current to the output transistors and VCC is connected to the internal circuit ground. The separate Vcc pins reduce cross coupling between individual devices when the outputs are driving heavy loads. A large source impedance in ground bus line produces significant noise when the transition current flows from the ground VCCA into the loads. All Vcc pins should be connected to the ground plane as close to the package as possible to reduce inductances.

Although little noise is generated on VEE line because the major switching current does not flow into the line, power supply bypass capacitors are recommended to suppress the switching noise caused by stray capacitance and asymmetric circuit loading.

Power supply with a regulation of 7% or better is recommended.

The -4.5V power supply will result in best circuit speed - power consumption performance. A more negative supply voltage will increase speed and noise margin at a cost of increased power dissipation. A less negative supply voltage will have just the opposite effect. A parallel combination of a 1.0μF and a 100nF capacitor at the entrance to the board, and a 10nF low-inductance capacitors such as ceramic chip capacitors between ground and the -4.5V line for each device are recommended.

## Circuit Interconnections

The multilayer printed circuit boards offer a number of advantages in the development of very high speed logic cards. Not only multilayer boards achieve a much higher package density, but they also provide the minimized propagation delay time between individual devices owing to a shorter lead length. Moreover, the multilayer circuit boards offer unbroken ground plane to minimize ground plane impedance and permit a precise control of transmission line impedances. In handling a waveform with very fast rise and fall time, it is very important to design the transmission line impedance and to terminate the line with a load which has the same impedance as the line impedance. When the two impedances are unmatched, the waveform will show an overshoot and an undershoot at the rising and falling edge which result in a ringing in the waveform.

In ECL circuits, pull-down resistors are required at the end point of the interconnections because the output stages of the ECL are of the simple open emitter type. These resistors are not only simple pull-down resistors but also termination resistors with proper matched impedance which terminate the line to prevent reflections on the line, and hence prevent overshoot, undershoot and ringings.

When the wire length of point-to-point wiring is kept short, the matched line termination is not so much important in existing ECL logics. However in very high speed logics such as SPECL, the rise and fall time is very small and the line length permissible without proper termination is very short.

Figure 1 shows an equivalent circuit of the wiring between the output and input of the devices. If a proper termination is not provided at the receiving end point of the line, the wave propagating in the line reflects at the receiving point coming back to sending point, and reflects back again at the sending point. This reflection eventually gives overshoot and undershoots at both points. If the propagation delay time along the line is shorter than the rise and the fall time, the reflection has little effect on the waveform. Be sure that the reflection effect depends on the rise and fall time but not on the frequency or the cycle time of the signal.

Figure 2 shows several ways of connecting pull-down resistors.

Resistor values for the connection in Figure 2(a) may range from 170Ω to 600Ω depending on line impedance. This way is suitable for wiring on a back plane because the line impedance is around 200Ω (refer to the next paragraph).

The best power-speed performance is obtained by pulling down by 50Ω to 150Ω to -2V termination voltage  $V_{TT}$ , as shown in Figure 2(b). This way is suitable for strip line transmission or coaxial transmission line in which the line impedance can be determined precisely.

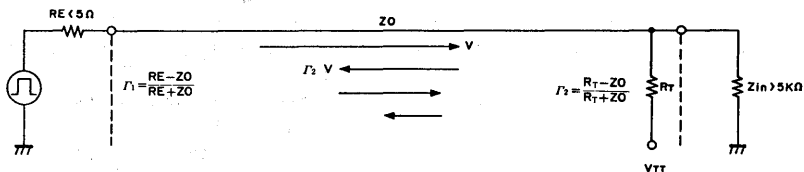


Figure 1. Equivalent Circuit of Interconnection

Figure 2(c) shows a parallel termination scheme where the termination voltage is not available. This way is electrically equivalent to that of Figure 2(b), but it costs an increased power dissipation.

Use of series damping resistor, Figure 2(d), will extend permissible length of unmatched-impedance interconnections with some loss of edge speed. With proper choice of the series damping resistor, line length can be extended to any length, while limiting overshoot and undershoot to a predetermined amount.

Power dissipation in termination resistors and output emitter follower transistor is shown in table 1 for Figure 2(b) and in Table 2 for Figure 2(c), for various termination resistor values.

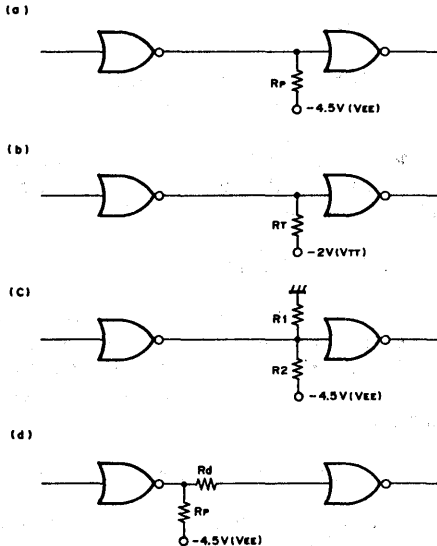


Figure 2. Pull-down Techniques

Table 1. Termination to  $V_{TT}$

$R_T(\Omega)$ to $-2V$	Power Dissipation (mW)		
	$R_T$	Output $T_r$	Total
25	20	36	56
50	10	18	28
75	6.5	12.1	18.6
100	4.9	9.1	14.0
150	3.3	6.1	9.4

One major advantage of ECL over other logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The SPECL emitter follower output transistor can drive a  $50\Omega$  transmission line terminated to  $-2.0V$  DC. This is equivalent to a load current of  $-22mA$  in the HIGH state and  $-6mA$  in the LOW state.

### Matched Impedance Termination

The line impedance of the wire over a ground plane, as shown in Figure 3, is given by the equation

$$Z_0 = 60 / \sqrt{\epsilon_r} \cdot \ln(4h/d)(\Omega)$$

where  $\epsilon_r$  is the effective dielectric constant surrounding the wire. The wire over a ground plane is most useful for breadboard layout or/and for back plane wiring. By choosing  $d=0.3$  to  $0.5mm$ ,  $h=3$  to  $6mm$  and  $\epsilon_r=1$  (air),  $Z_0$  ranges from  $190$  to  $260\Omega$ . The line impedance will decrease a little with the existence of an insulator of the wire and the board. The termination technique shown in Figure 2(a) may be used in this back plane wiring, with some degradation of the waveform.

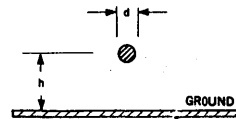


Figure 3. Wire Over Ground

Table 2. Parallel Termination to  $V_{ee}$

$Z_0$ ( $\Omega$ )	Resistor ( $\Omega$ )		Power Dissipation (mW)		
	$R_1$	$R_2$	$R_L$	Output $T_r$	Total
25	45	56	220	36	256
50	90	113	110	18	128
75	135	170	73	12	85
100	180	225	55	9	64
150	270	340	36	6	42

A coaxial cable is one of the ideal transmission lines. The characteristic impedance of the cable is

$$Z_0 = 60 / \sqrt{\epsilon_r} \cdot \ln(D/d)$$

Some common types of coaxial cables have the characteristic impedances of 50, 75 or 125Ω. Figure 4 shows the way of the termination. The propagation delay along the cable depends on the dimension and the dielectric constant of the insulating material used for the cable. Common coaxial cables have a delay time of 5 to 7 ns/m.

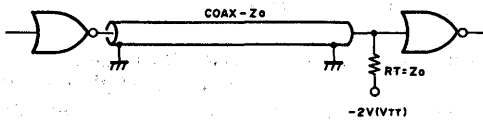


Figure 4. Coax Transmission Line

A micro-strip line is also an ideal transmission line because the characteristic line impedance can be determined precisely.

The characteristic impedance of this transmission line is indicated by the following formula.

i) Where  $\frac{W}{H} < 1$

$$Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} \ln \left( \frac{8H}{W} + \frac{W}{4H} \right) (\Omega)$$

ii) Where  $\frac{W}{H} \geq 1$

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{W}{H} + 2.42 - 0.44 \frac{H}{W} + \left(1 - \frac{H}{W}\right)^2} (\Omega)$$

$$\text{With } \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + \frac{10H}{W}\right)^{-\frac{1}{2}}$$

Figure 5 shows the cross section of the strip line. Fiber-glass epoxy boards ( $\epsilon_r = 4.5 - 5.0$ ) is the most popular material.

Teflon<sup>a1</sup> board is an excellent material with good frequency characteristics, but it is not so suitable for strip line application because of its low dielectric constant and resulting wide strip line width. Ep-silam-10<sup>a2</sup> has a dielectric constant of 10.2 and may be used for the strip line board.

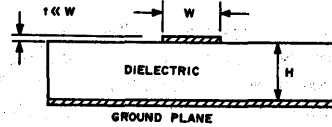


Figure 5. Micro-strip Line

The characteristic impedance of micro-strip lines for various geometries and insulators is plotted in Figure 7.

Figure 8 shows curves for the characteristic impedance of fiber-glass epoxy board which has the dielectric constant 4.7.

Figures 9 and 10 show curves for the micro-strip capacitance per meter as a function of line width and insulator thickness. The inductance per meter may be calculated using the formula,

$$L_0 = Z_0^2 C_0$$

where  $Z_0$  = characteristic impedance,  
 $C_0$  = capacitance per meter.

The propagation delay of the line depends only on the dielectric constant and may be calculated by the following formula;

$$T_{pd} = 3.34 \sqrt{0.48 \epsilon_r + 0.67} \text{ (ns/m)}$$

A strip line consisting of a conductive ribbon centered in a dielectric medium between two conductive planes is shown in Figure 6. The characteristic impedance of the line is given by the following formula;

$$Z_0 = 94.15 / \sqrt{\epsilon_r} [W / (h-t) + 0.45 + 1.18t/h] (\Omega)$$

The propagation delay time of the strip line is indicated by the following formula.

$$T_{pd} = 3.34 \sqrt{\epsilon_r} \text{ (ns/m)}$$

Figures 11 and 12 show the curves of the characteristic impedance and capacitance per meter of strip line for fiber-glass epoxy board.

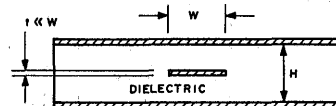


Figure 6. Strip Line



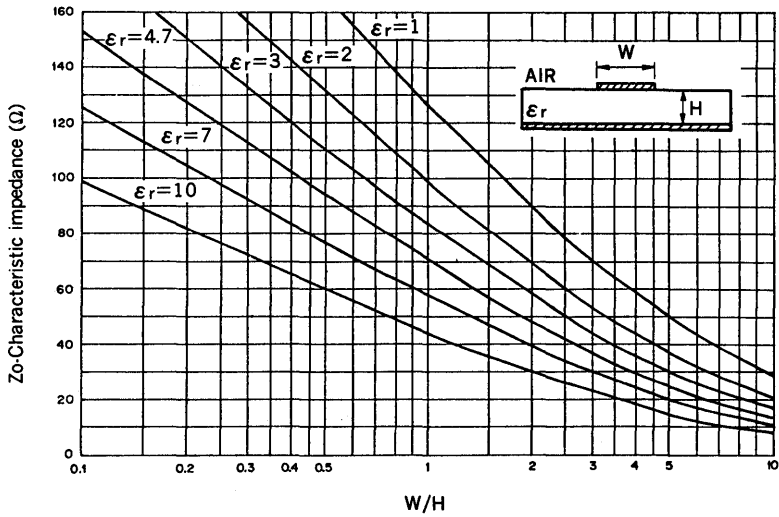


Figure 7. Characteristic Impedance vs. Strip Line Width/Dielectric Thickness

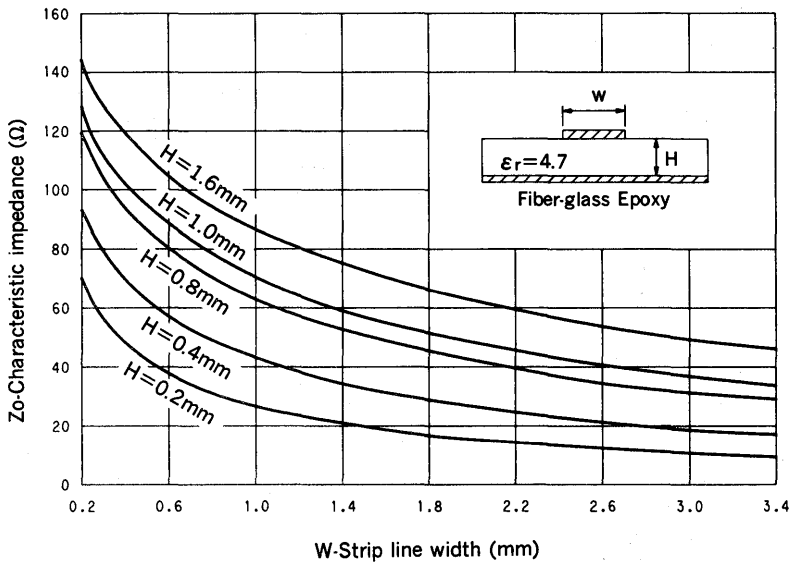


Figure 8. Characteristic Impedance vs. Strip Line Width

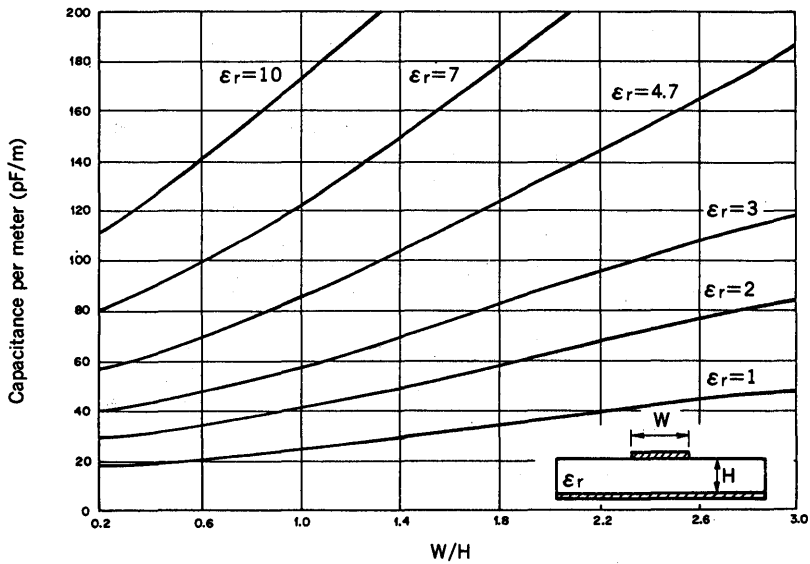


Figure 9. Capacitance vs. Strip Line Width/Dielectric Thickness

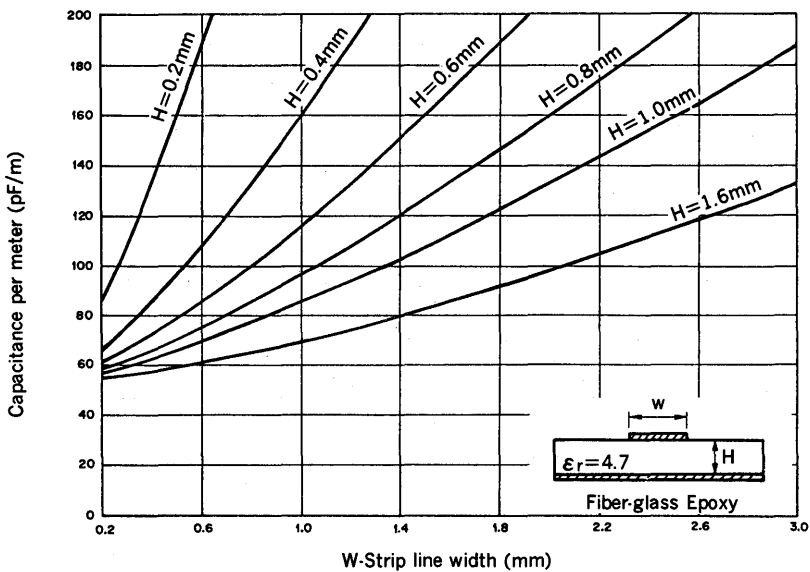


Figure 10. Capacitance vs. Strip Line Width

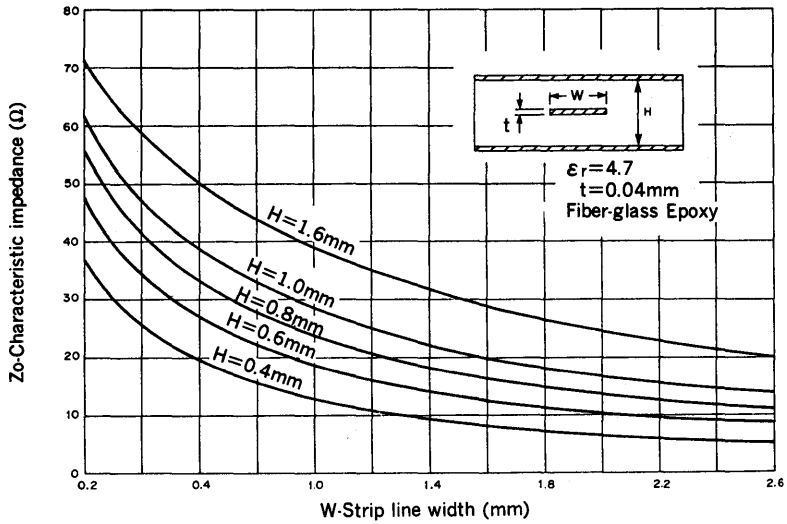


Figure 11. Characteristic Impedance vs. Strip Line Width

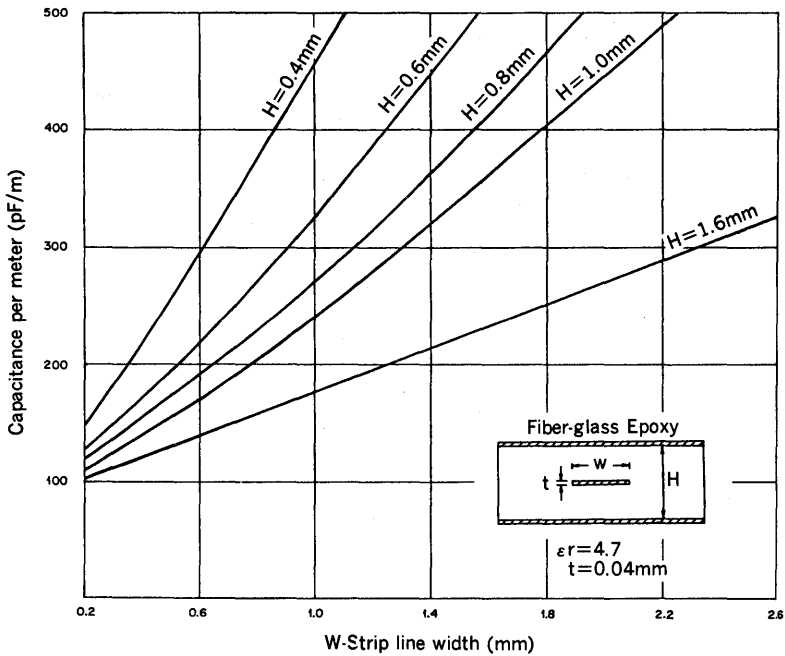


Figure 12. Capacitance vs. Strip Line Width

### Interface to Other Logic

To interface to a slower circuit, a circuit with hysteresis (which is known as Schmitt Trigger) may be used to prevent multiple triggering at the rising and falling edge. Figure 13 shows an example of Schmitt Trigger circuit with a hysteresis of 100mV.

Figure 14 shows a way of interfacing to low level signals. As the circuit is AC coupled and self biased, it can be used as the interface circuit to signals that have non-ECL threshold voltage.

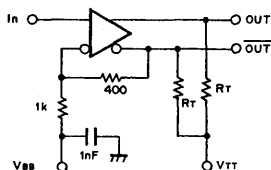


Figure 13. Schmitt Trigger Circuit

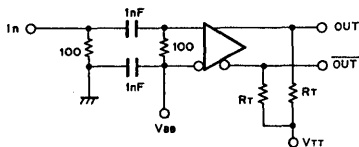


Figure 14. Low Level Input Amplifier

### 3. Thermal Consideration

Although SPECL devices are assembled in packages which have good thermal characteristics, appropriate thermal design is required to assure the circuit performance and long-term circuit reliability. Normally, both are affected by die temperature and are improved by keeping the IC junction temperature ( $T_j$ ) low.

The junction temperature is estimated using formulas:

$$T_j = T_a + (\theta_{jc} + \theta_{ca}) \cdot P_d$$

or

$$T_j = T_a + \theta_{ja} \cdot P_d$$

where

$T_j$  = junction temperature

$T_a$  = ambient temperature

$P_d$  = power dissipation including effects of external load

$\theta_{jc}$  = thermal resistance, junction to case

$\theta_{ca}$  = thermal resistance, case to ambient

$\theta_{ja}$  = thermal resistance, junction to ambient

$\theta_{jc}$  is the thermal resistance inherent to the package, and is essentially independent of mount assembly method and air flow.  $\theta_{ca}$  and  $\theta_{ja}$  can be varied by the user.

For applications where the case is held at an ambient temperature by mounting on a large or temperature-controlled heat sink, the junction temperature is calculated by the formula:

$$T_j = T_a + \theta_{jc} \cdot P_d$$

Table 3. Thermal Resistance of SPECL Devices

Package	$\theta_{jc}$ (°C/W)	$\theta_{ja}$ (°C/W)	
		Free air*1	On board*2
16PIN	20.0	329	106
24PIN	17.5	276	102
32PIN	16.0	261	99

\* 1 No board assembly

\* 2 Still air without heat sink

In Table 3, thermal resistances of SPECL devices are shown, where  $\theta_{jc}$  is measured both in free air (with no heat-sinking, no board assembly and no air flow) and on a fiber-glass epoxy board (with no heat-sinking and no air flow). On the board, the IC leads are soldered to board conductors and thermal-conductive grease is applied between the IC and the board.  $\theta_{jc}$  is improved drastically by board assembly.

It is recommended to apply thermal-conductive grease between the IC and the board or to bond the IC to the board by epoxy to reduce the thermal resistance, because the air between the IC and the board is not a good thermal conductor. If thermal-conductive materials are not in use, the air gap between the IC and the board should be made as small as possible. The existence of a conductor beneath the IC, too, improves thermal resistance.

An appropriate heat-sink-fin and air flow are effective for reduction of thermal resistance.

Figure 15 shows an example of the fin and assembly method. As the Flat Packages can be mounted upside down, the Face-Down mounting can be employed with effective heat-sink-fin.

The effect of the fin and air flow is illustrated in figure 16 where the test set-up of thermal resistance measurement is the same as that shown in Figure 15. In the face-down mounting, the thermal resistance is larger than that of normal mounting because the heat can not be removed through the board. With the fin used in face-down mounting, the thermal resistance is almost the same as normal mounting. This result suggests that the thermal resistance can be reduced more effectively with larger heat-sink-fin used in face-down mount.

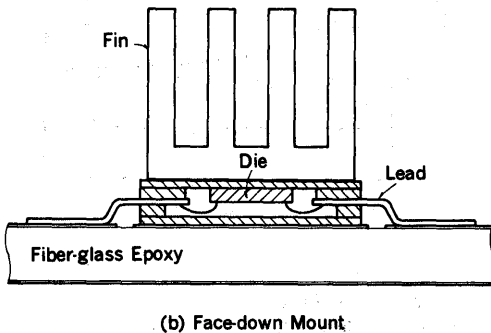
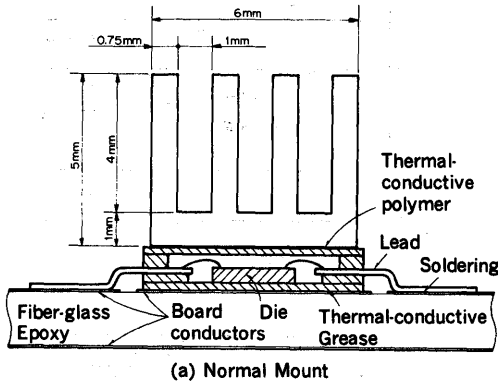
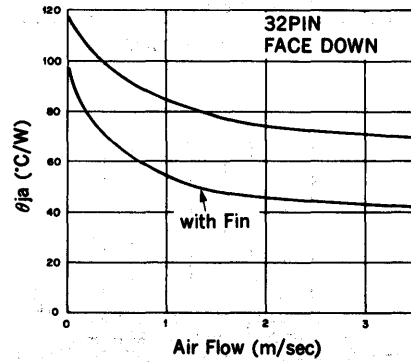
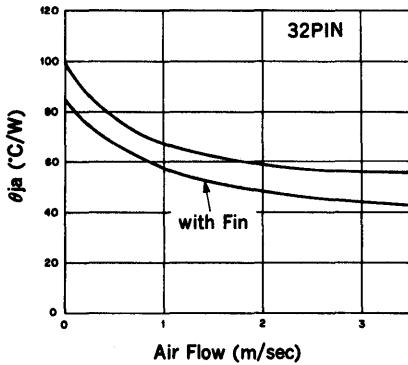
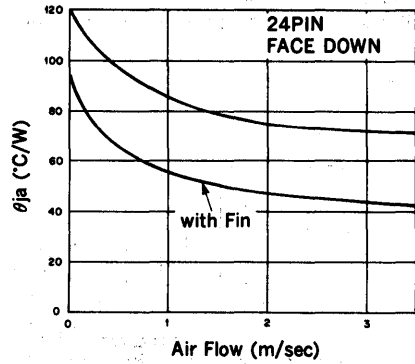
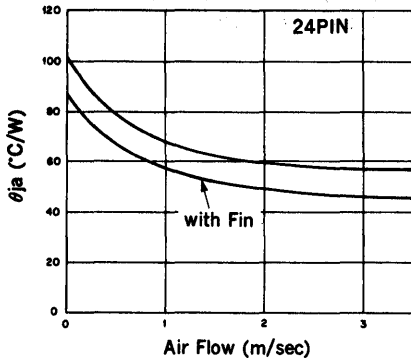
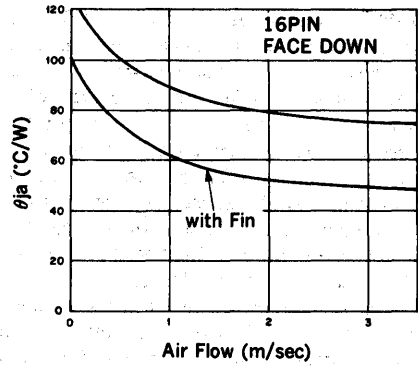
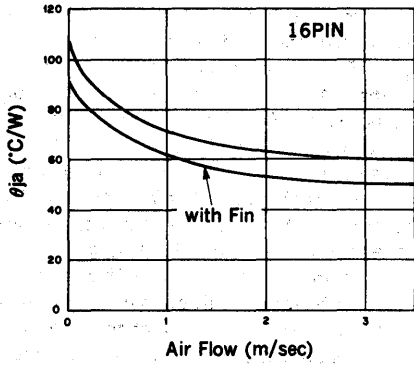
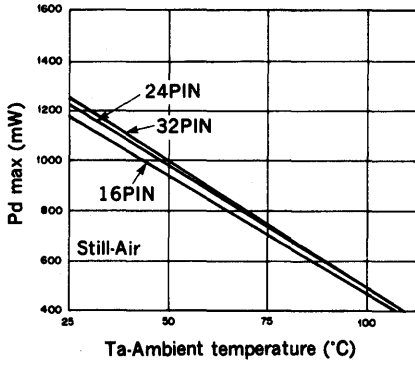


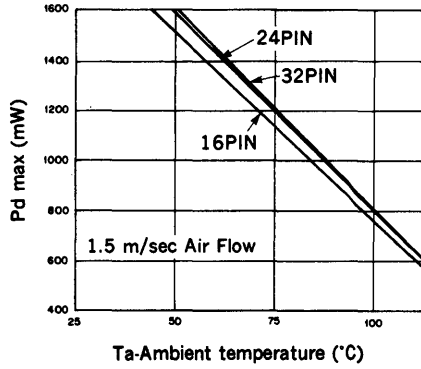
Figure 15. Mount Assembly Method



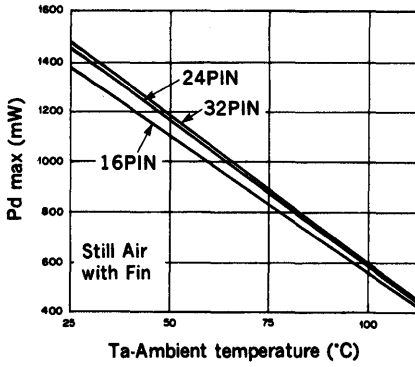
**Figure 16. Thermal Resistance vs. Air Flow**  
 (Heat-Sink-Fin is Shown in Figure 15)



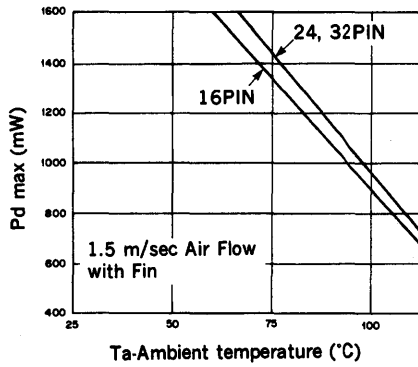
(a) Still-Air



(b) 1.5 m/sec Air Flow



(c) Still-Air, with Fin



(d) 1.5 m/sec Air Flow, with Fin

**Figure 17. Maximum Allowed Power Dissipation vs. Ambient Temperature**  
(Heat-Sink-Fin is shown in Figure 15 (a))





## Sony Component Products Company Sales Offices

Area Office	Address	Phone	Fax
Southwest	10833 Valley View Street Cypress, CA 90630-0016	714/229-4442	714/229-4333
Northwest	655 River Oaks Parkway San Jose, CA 95134	408/944-4314	408/433-0834
North Central	1200 N. Arlington Heights Road Itasca, IL 60143	708/773-6072	708/773-6068
Northeast	85 Wells Avenue Newton, MA 02159	617/527-4560	617/527-1783
Canada	1602 Tricot Ave. Whitby, Ontario LIN 5S6	416/686-2201	416/686-4802

### Semiconductor & Image Sensing Divisions Sales Representative Offices:

<b>Alabama:</b> Rep, Inc., 205/881-9270	<b>Nebraska:</b> Centech, 816/358-8100
<b>Alaska:</b> Sony, 408/432-0190	<b>Nevada:</b> (Northern) Brooks, 415/960-3880 (Southern) FP Sales, 602/894-5303
<b>Arkansas:</b> B-P Sales, 214/234-8438	<b>New Hampshire:</b> Tech Rep, 617/272-5965
<b>Arizona:</b> FP Sales, 602/894-5303	<b>New Jersey:</b> (Northern) S-J Assoc., 516/536-4242 (Southern) S-J Assoc., 609/866-1234
<b>California:</b> (San Diego) Addem, 619/729-9216 (Los Angeles) HT Sales, 714/583-1488 (Semi. only) (Los Angeles) Varigon, 818/594-5080, (I.S. only) (San Francisco) Brooks, 415/960-3880 (Sacramento) Brooks, 916/676-2025	<b>New Mexico:</b> FP Sales, 505/345-5553
<b>Colorado:</b> Electrodyne, 303/695-8903	<b>New York:</b> (Metropolitan) S-J Assoc., 516/536-4242 (Upstate) Tri Tech, 716/385-6500
<b>Connecticut:</b> Tech Rep, 617/272-5965	<b>North Carolina:</b> (East) Rep, Inc., 919/469-9997 (West) Rep, Inc., 704/563-5554
<b>Delaware:</b> S-J Assoc., 703/533-2233	<b>North Dakota:</b> High Tech Sales, 612/944-7274
<b>District of Columbia:</b> S-J Assoc., 703/533-2233	<b>Ohio:</b> (Cleveland) Giesting, 216/261-9705 (Cincinnati) Giesting, 513/385-1105
<b>Florida:</b> Sigma, 813/789-5522	<b>Oklahoma:</b> B-P Sales, 214/234-8438
<b>Georgia:</b> Rep, Inc., 404/938-4358	<b>Oregon:</b> Vantage, 503/620-3280
<b>Hawaii:</b> Brooks, 415/960-3880	<b>Pennsylvania:</b> (East) S.J. Assoc., 609/866-1234 (West) Giesting, 412/828-3553
<b>Idaho:</b> Electrodyne, 801/264-8050	<b>Rhode Island:</b> Tech Rep, 617/272-5965
<b>Illinois:</b> (Northern) Micro-Tex, 708/382-3001 (Southern) Centech, 314/291-4230	<b>South Carolina:</b> Rep, Inc., 704/563-5554
<b>Indiana:</b> Giesting, 317/844-5222	<b>South Dakota:</b> High Tech Sales, 612/944-7274
<b>Iowa:</b> J.R. Sales, 319/393-2232	<b>Texas:</b> (Austin) B-P Sales, 512/346-9186 (Dallas) B-P Sales, 214/234-8438 (Houston) B-P Sales, 713/782-4144
<b>Kansas:</b> Centech, 816/358-8100	<b>Tennessee:</b> Rep, Inc., 615/475-9012
<b>Kentucky:</b> Giesting, 513/385-1105	<b>Utah:</b> Electrodyne, 801/264-8050
<b>Louisiana:</b> B-P Sales, 214/234-8438	<b>Vermont:</b> Tech Rep, 617/272-5965
<b>Maine:</b> Tech Rep, 617/272-5965	<b>Virginia:</b> S-J Assoc., 703/533-2233
<b>Maryland:</b> S-J Assoc., 703/533-2233	<b>Washington:</b> Vantage, 206/455-3460
<b>Massachusetts:</b> Tech Rep, 617/272-5965	<b>West Virginia:</b> Giesting, 513/385-1105
<b>Michigan:</b> Giesting, 313/478-8106	<b>Wisconsin:</b> (Northern) High Tech, 612/944-7274 (Southern) Micro-Tex, 414/542-5352
<b>Minnesota:</b> High Tech Sales, 612/944-7274	<b>Wyoming:</b> Electrodyne, 801/264-8050
<b>Mississippi:</b> Rep, Inc., 205/881-9270	
<b>Missouri:</b> (Western) Centech, 816/358-8100 (Eastern) Centech, 314/291-4230	
<b>Montana:</b> Electrodyne, 801/264-8050	

## Distributor Offices:

---

<b>Alabama:</b>		
Huntsville	Marshall, 205/881-9235	
<b>Arizona:</b>		
Phoenix	Marshall, 602/496-0290	
<b>California:</b>		
Los Angeles	Milgray, 805/484-4055	
El Monte	Marshall, 818/459-5500	
Ft. Valley	Bell Micro, 714/963-0667	
Saratoga	Western Micro, 408/725-1660	
Irvine	Marshall, 714/458-5395	
Los Angeles	Marshall, 818/407-0101	
Los Angeles	Western Micro, 818/707-0377	
Milpitas	Bell Micro, 408/434-1150	
Orange	Western Micro, 714/637-0200 or 818/356-0180	
Sacramento	Marshall, 916/635-9700	
San Diego	Ageis, 619/729-2026	
San Diego	Marshall, 619/578-9600	
San Diego	Western Micro, 619/453-8430	
San Jose	Merit, 408/434-0800 (Semiconductor)	
San Francisco	Marshall, 408/942-4600	
<b>Colorado:</b>		
Denver	Marshall, 303/451-8444	
Denver	Robert Waxman, 303/623-1200 (Cameras)	
<b>Connecticut:</b>		
Danbury	Phase I, 203/791-9042	
Milford	Milgray, 203/878-5538 or 800/922-6911	
Monroe	Western Micro, 203/452-0533	
Wallingford	Marshall, 203/265-3822	
<b>Florida:</b>		
Deerfield	Vantage, 305/429-1001 (Semiconductor)	
Ft. Lauderdale	Marshall, 305/977-4880	
Orlando	Marshall, 407/767-8585	
Tampa	Marshall, 813/576-1399	
Winter Park	Milgray, 407/647-5747 or 800/432-0645	
<b>Georgia:</b>		
Atlanta	Marshall, 404/923-5750	
Norcross	Milgray, 404/446-9777 or 800/241-5523	
<b>Illinois:</b>		
Chicago	Milgray, 708/253-1212	
Chicago	Marshall, 708/490-0155	
<b>Indiana:</b>		
Indianapolis	Marshall, 317/297-0483	
<b>Kansas:</b>		
Kansas City	Marshall, 913/492-3121	
Overland Park	Milgray, 913/236-8800	
<b>Maryland:</b>		
Columbia	Milgray, 301/621-8169 or 800/638-6656	
Columbia	Vantage, 301/720-5100 (Semiconductor)	
Silver Springs	Marshall, 301/622-1118	
<b>Massachusetts:</b>		
Andover	Vantage, 508/687-3900 (Semiconductor)	
Boston	Marshall, 508/658-0810	
Burlington	Western Micro, 617/273-2800 or 800/345-2921	
Wilmington	Bell Micro, 508/658-0222	
Wilmington	Milgray, 508/657-5900	
<b>Michigan:</b>		
Livonia	Marshall, 313/525-5850	
<b>Minnesota:</b>		
Minneapolis	Marshall, 612/559-2211 or 1014	
<b>Missouri:</b>		
St. Louis	Marshall, 314/291-4650	
<b>New Jersey:</b>		
Clifton	Vantage, 201/777-4100 (Semiconductor)	
Fairfield	Marshall, 201/882-0320	
Fairfield	Western Micro, 201/882-4999	
Garfield	Phase 1, 201/403-0002	
Mt. Laurel	Marshall, 609/234-9100	
Marlton	Milgray, 609/983-5010 or 800/257-7111	
Marlton	Western Micro, 609/596-7775	
Parsippany	Milgray, 201/335-1766	
<b>New York:</b>		
Binghamton	Marshall, 607/798-1611	
Farmingdale	Milgray, 516/420-9800 or 800/MILGRAY	
Long Island	Marshall, 516/273-2424	
N. Lindenhurst	Phase I, 516/957-4900	
New York	Chori, 212/563-3264 (Cameras)	
Rochester	Marshall, 716/235-7620	
Pittsford	Milgray, 716/834-9405	
Smithtown	Vantage, 516/543-2000 (Semiconductor)	
<b>North Carolina:</b>		
Raleigh	Marshall, 919/878-9882	
Raleigh	Merit, 919/790-8094	
<b>Ohio:</b>		
Cleveland	Marshall, 216/248-1788	
Cleveland	Milgray, 216/447-1520 or 800/321-0006	
Columbus	Marshall, 614/891-7580	
Dayton	Marshall, 513/898-4480	
<b>Oklahoma:</b>		
Tulsa	Marshall, 918/622-7151	
<b>Oregon:</b>		
Tigard	Daitron, 503/620-2870	
Beaverton	Western Micro, 503/629-2082	
Portland	Marshall, 503/644-5050	
<b>Pennsylvania:</b>		
Pittsburgh	Marshall, 412/788-0441	
<b>Texas:</b>		
Austin	Marshall, 512/837-1991	
Brownsville	Marshall, 512/542-4589	
Dallas	Marshall, 214/233-5200	
Dallas	Milgray, 214/248-1603 or 800/637-7227	
Houston	Marshall, 713/895-9200	
<b>Utah:</b>		
Salt Lake City	Marshall, 801/485-1551	
Salt Lake City	Milgray, 801/272-4999	
<b>Washington:</b>		
Redmond	Western Micro, 206/881-6737	
Redmond	Merit, 206/869-7557 (Semiconductor)	
Seattle	Marshall, 206/486-5747	
<b>Wisconsin:</b>		
Milwaukee	Marshall, 414/797-8400	
<b>Canada:</b>		
Ontario	Marshall, 416/458-8046 (Semiconductor)	



**SONY®**

**Sony Semiconductor**

