SONY® CXK784861Q-33

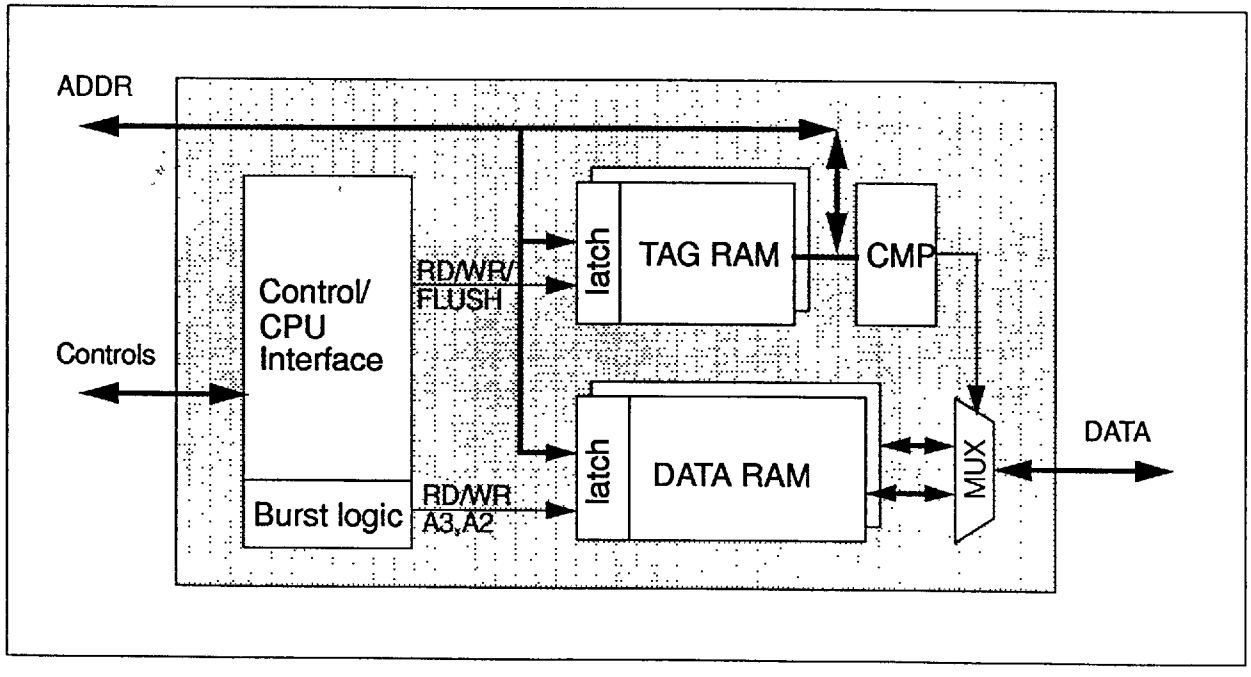
FEATURES

- Single Chip Cache Subsystem for 486 CPU
- Look-aside Architecture
- Write-back and Write-through Cache Operations
- 33 Mhz Operating Frequency
- 128K byte two-way-set associativity
- Supports MESI protocol
- Cascadable to 256K bytes
- Enhanced Cascade Mode
- Zero Wait State Burst Mode (2-1-1-1)
- Single 5V power supply
- Power-down mode
- PC compatible
- 160-pin PQFP

DESCRIPTION

The SONY Cache-1C is a single chip cache subsystem designed to work with the 486 microprocessor. This device is designed utilizing SONY's proprietary Memory-intensive ASIC (MASIC™) technology. Using MASIC, the SONY Cache-1C integrates 128K bytes of cache memory, tag ram and associated control logic on a single chip. As a look-aside secondary cache, this device can be incorporated into various systems. This device can be designed onto a motherboard as a standard or an upgradeable feature. Two SONY Cache-1C chips can be cascaded to provide 256K bytes of secondary cache without using external glue logic. The write back mode reduces data traffic on the memory bus and at the same time provides zero wait state for hit cycles. High performance, high integration and low power characteristics render this device ideal for high performance desktop and mobile computing applications

SONY Cache-1C BLOCK DIAGRAM



1 SONY Cache-1C Pinout

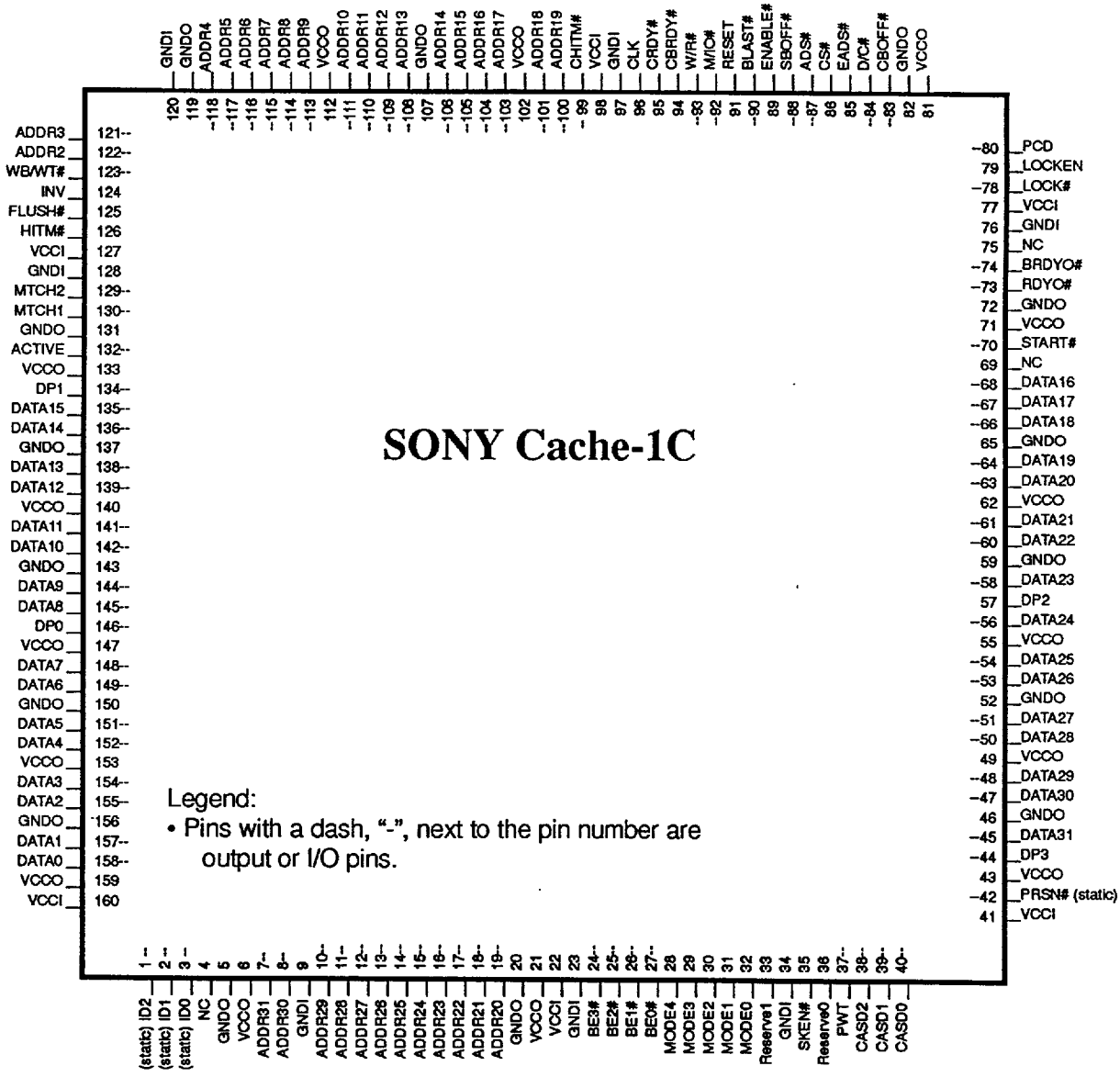


Figure 1.1. SONY Cache-1C Pin Assignment (160-pin PQFP)

Top View

1.1 Table of Package Pin Numbers & Pin Names

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	(static) ID2	41	VCCI	81	VCCO	121	ADDR3
2	(static) ID1	42	PRSN#	82	GNDO	122	ADDR2
3	(static) ID0	43	VCCO	83	CBOFF#	123	WB/WT#
4	NC	44	DP3	84	D/C#	124	INV
5	GNDO	45	DATA31	85	EADS#	125	FLUSH#
6	VCCO	46	GNDO	86	CS#	126	HITM#
7	ADDR31	47	DATA30	87	ADS#	127	VCCI
8	ADDR30	48	DATA29	88	SBOFF#	128	GNDI
9	GNDI	49	VCCO	89	ENABLE#	129	MTCH2
10	ADDR29	50	DATA28	90	BLAST#	130	MTCH1
11	ADDR28	51	DATA27	91	RESET	131	GNDO
12	ADDR27	52	GNDO	92	M/IO#	132	ACTIVE
13	ADDR26	53	DATA26	93	W/R#	133	VCCO
14	ADDR25	54	DATA25	94	CBRDY#	134	DP1
15	ADDR24	55	VCCO	95	CRDY#	135	DATA15
16	ADDR23	56	DATA24	96	CLK	136	DATA14
17	ADDR22	57	DP2	97	GNDI	137	GNDO
18	ADDR21	58	DATA23	98	VCCI	138	DATA13
19	ADDR20	59	GNDO	99	CHITM#	139	DATA12
20	GNDO	60	DATA22	100	ADDR19	140	VCCO
21	VCCO	61	DATA21	101	ADDR18	141	DATA11
22	VCCI	62	VCCO	102	VCCO	142	DATA10
23	GNDI	63	DATA20	103	ADDR17	143	GNDO
24	BE3#	64	DATA19	104	ADDR16	144	DATA9
25	BE2#	65	GNDO	105	ADDR15	145	DATA8
26	BE1#	66	DATA18	106	ADDR14	146	DP0
27	BE0#	67	DATA17	107	GNDO	147	VCCO
28	MODE4	68	DATA16	108	ADDR13	148	DATA7
29	MODE3	69	NC	109	ADDR12	149	DATA6
30	MODE2	70	START#	110	ADDR11	150	GNDO
31	MODE1	71	VCCO	111	ADDR10	151	DATA5
32	MODE0	72	GNDO	112	VCCO	152	DATA4
33	Reserve1	73	RDYO#	113	ADDR9	153	VCCO
34	GNDI	74	BRDYO#	114	ADDR8	154	DATA3
35	SKEN#	75	NC	115	ADDR7	155	DATA2
36	Reserve0	76	GNDI	116	ADDR6	156	GNDO
37	PWT	77	VCCI	117	ADDR5	157	DATA1
38	CASD2	78	LOCK#	118	ADDR4	158	DATA0
39	CASD1	79	LOCKEN	119	GNDO	159	VCCO
40	CASD0	80	PCD	120	GNDI	160	VCCI

2 PIN LIST

2.1 Address:

ADDR[31:2]	I/O	Address pins shared by the CPU and the cache subsystem on the host bus.
BE#[3:0]	I/O	Byte enable. These signals allows individual bytes within a double-word to be written independently. They are ignored in all read cycles. They are also used by the SONY Cache-1C to decode flush special bus cycle driven by the CPU.

2.2 Data:

DATA[31:0]	I/O	Data pins on the host bus.
DP[3:0]	I/O	Data parity. One parity bit for each data byte. The SONY Cache-1C does not perform parity check. These bits are read and written like other data bits.

2.3 Control (input and I/O):

ADS#	I/O	Address strobe. Should be connected to the ADS# signal of the CPU. Used by the CPU to indicate the beginning of an memory or I/O cycle. During write-back operation, ADS# is driven by the SONY Cache-1C to indicate the beginning of a write-back cycle.
BLAST#	I/O	End-of-Burst indicator. Indicates the end of a burst cycle. This signal is driven by the SONY Cache-1C during write-back cycles.
BRDYO#	I/O	Burst data ready. It is asserted during read hit to indicate that data is available to the CPU. It is also asserted during write hit to write back lines to indicate that the SONY Cache-1C is ready to receive the next burst data. It can be connected externally with CBRDY# to form an IO pin. When BRDYO# is not asserted, it is driven high for one cycle and then tri-stated.
CASD[2:0]	I/O	These pins are reserved for communications between the SONY Cache-1C chips when used in cascade mode. Currently only CASD[1] and CASD[0] are used. See section 4.12 for more detail.
CBOFF#	I/O	This signal is driven by the SONY Cache-1C to indicate that it needs to acquire the host bus in order to start a write-back cycle.

CBRDY#	I	Cache data burst ready. Generated by the system logic to indicate that data is available from the system memory and that burst mode transfer is used. This pin can be connected externally to BRDYO# to form an I/O pin that can be directly connected to the BRDY# input of the CPU. See section 4.1 for more detail.
CLK	I	System clock. Same as the 486 1X clock.
CRDY#	I	Cache data ready. Terminates the current bus cycle and stops the burst transfer. CRDY# can be connected externally to RDYO# to form an I/O pin. See section 4.2 for more detail.
CS#	I	Chip Select. This signal is must be asserted with ADS# and EADS#; otherwise ADS# and EADS# are ignored. During cascade mode, CS# must be tied low.
D/C#	I/O	Data/Code select. This signal is used together with M/IO#, W/R# and BE#'s to decode special bus cycles for flush. In other memory accesses, this signal is ignored. This signal is driven high during SONY Cache-1C generated write-back cycles.
EADS#	I	External Address Strobe. The SONY Cache-1C performs a snoop cycle when EADS# is active. The snoop address is sampled at the same time as EADS# is sampled low. If the snoop address hits a cache line that contains modified data, the cache line is written back to the system memory.
ENABLE#	I	If this signal inactive, the cache is in power down mode; otherwise the system is in normal operation mode. During power down, all external signals including RESET are ignored.
FLUSH#	I	This signal sets an internal flush-pending flag. After the internal flag is set, the next CPU IO access will trigger a flush sequence. The internal flag is clear when the flush sequence is completed.
HITM#	I	This signal is driven by the CPU to indicate snoop hit on modified data within the CPU's internal cache. HITM# is sampled two cycles after EADS# is asserted. If it is active, the SONY Cache-1C cancels its snoop write-back cycle and allows the CPU to proceed with its own write-back. HITM# is also sampled during write cycles. If it is active, the SONY Cache-1C assumes that the CPU is performing a modified data write-back. It updates the cache line and forces the cache line to write-through state after the write cycle is completed. If the previous snoop cycle was driven with INV active, the modified cache line within the SONY Cache-1C is invalidated.
INV	I	Snoop and invalidate. It is sampled at the same time as EADS#. If INV is active and the snoop address is hit, the cache line is invalidated. If write back is required due to modified data, invalidation takes place after write-back is completed. If INV is inactive, the cache line is converted to write-through (shared) state.
LOCK#	I/O	LOCK# is driven by the CPU to indicate bus lock cycles.

LOCKEN	I	Enable Lock cycle. If inactive, LOCK# signal is ignored.
M/IO#	I/O	Memory and I/O selector. Memory is selected if this signal is high, otherwise I/O is selected.
MODE[4:0]	I	Operation mode selector. Selects between normal, cascade and test mode. In normal mode, all the MODE pins should be tied low. In cascade mode, one of the SONY Cache-1C chip should have MODE[4:0]=01100 while the other SONY Cache-1C chip should have MODE[4:0]=01101. All other combinations of MODE pins are reserved internal uses.
NC		"No connect" pins. The NC pins should not be driven by any external logic. Some of the NC pins may be driven by the SONYC-1M
PCD	I/O	Page Cache Disable. This signal is connected to the PCD output of the CPU. If PCD is active during line fill, the cache line is not cacheable in SONY Cache-1C. PCD is ignored during read hit cycles. If it is active during write hit, the write cycle is handled by the SONY Cache-1C like a write-through cycle, regardless of the cache line status. PCD is ignored during write miss. This signal is driven by the CPU and is sampled at the same time as ADS#. During write-back cycles initiated by the SONY Cache-1C, PCD is driven inactive.
PWT	I/O	Page Write-through. If PWT is active during line fill, the data is cached in as write-through (shared), regardless of the status of the WB/WT# signal. A line fill is cached in as write-back (exclusive) only if PWT sampled low and WB/WT# sampled high. If PWT is active during write hit, the write cycle is treated as write-through regardless of cache line status. It is ignored in write miss cycles. This signal is driven by the CPU and is sampled at the same time as ADS#. During write-back cycles initiated by the SONY Cache-1C, PWT is driven inactive.
RESET	I	Resets the SONY Cache-1C to the initial state and invalidates all the tag entries. Modified data, if any, are not written back to system memory.
Reserve0	I	This pin must be tied low.
Reserve1	I	This pin must be tied high.
SBOFF#	I	The SBOFF# signal is driven active by the system when it need to back off both the CPU and the SONY Cache-1C. The system should not back off the CPU and the SONY Cache-1C if it is running a burst sequence after one or more data transfer has taken place. ADS# is ignored when SBOFF# is active.

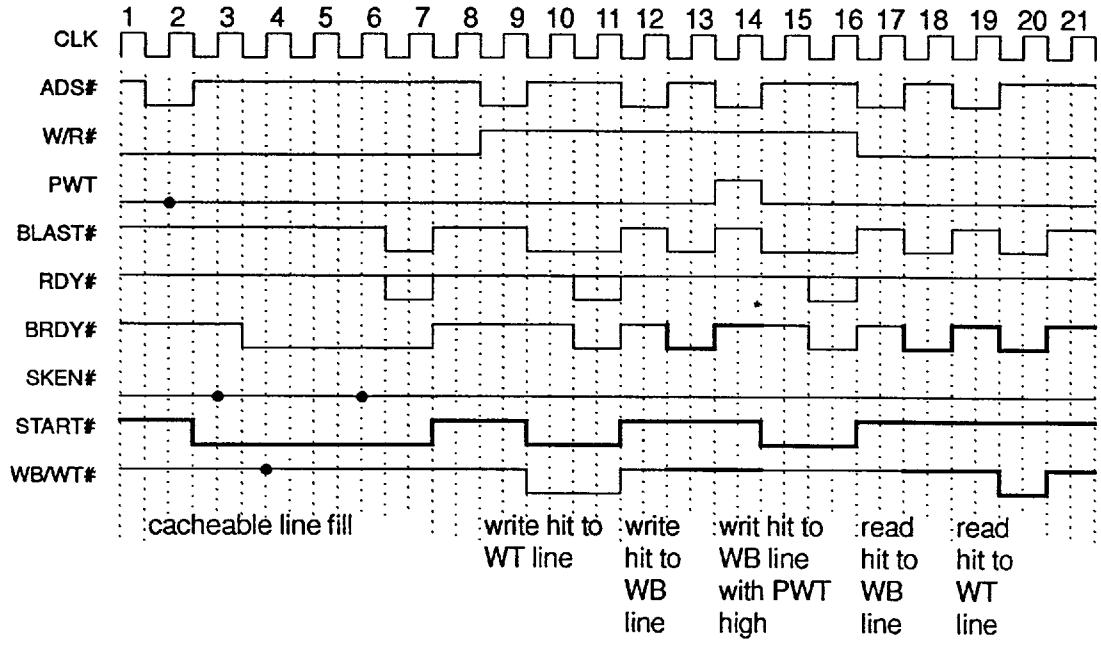
SKEN#	I	Cacheability indicator. This signal is sampled by the SONY Cache-1C to determine if a line fill is cacheable. It is sampled twice during a line fill. It is first sampled during the clock cycles between ADS# and the first CBRDY#. It is sampled again one clock cycles before the last CBRDY# of the line fill. SKEN# must be active during both sampling point; otherwise the line fill is not cacheable.
START#	I/O	Driven by the SONY Cache-1C to start a memory access for read miss, write miss, or write-through cycles.
W/R#	I/O	Read/Write select. High indicates a write cycle and low indicates a read cycle. It is driven high during a SONY Cache-1C initiated write-back.
WB/WT#	I/O	WB and WT indicator. This signal is driven by the system memory during line fill to indicate the cache policy. It is also driven by the SONY Cache-1C during read hit or write hit to write back lines to indicate the cache policy of the cache line. When SONY Cache-1C releases this signal, it is first driven high for one cycle and then tri-stated. This signal is sampled at the same time as the first CBRDY#/CRDY# of the line fill by the SONY Cache-1C. If it is sampled low, the cache line is write-through (shared).

2.4 Control (output):

ACTIVE	O	This pin is low if the chip is in cascade mode and is inactive. It is used for system debug only.
CHITM#	O	Cache hit indicator. This signal indicates if a cache access hits a modified cache line in the SONY Cache-1C cache. It should be sample one cycle after an ADS# cycle or two cycles after an EADS# cycle.
ID2, ID1, ID0	O	Static output, ID2=0, ID1=1, ID0=1
MTCH1, MTCH2	O	Indicates cache hit during ADS# cycles.
PRSN#	O	Static output, always low.
RDYO#	O	Data ready. Generated during the last cycle of a read hit or write hit to write-back lines to indicate that the burst sequence is completed. It can be connected externally with CRDY# to form an I/O pin. When RDYO# is not asserted, it is driven high for one cycle and then tri-stated.

3 Functional Descriptions

3.1 Line fill, write hit and read hit cycles



* A thick signal line indicates that the signal is driven by the SONY Cache-1C
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.1. Line fill and hit cycles

Line fills are initiated by the CPU as memory read. The accessed data is not in the SONY Cache-1C so it generates a read miss. The SONY Cache-1C samples SKEN# during the cycles between ADS# and the first BRDY# to determine if the line fill is cacheable. If the memory read is cacheable, the SONY Cache-1C stores the return data at each BRDY#/RDY# in its internal data ram. The line fill ends when the fourth BRDY#/RDY# is sampled. If the CPU terminates the line fill by asserting BLAST# before reading the last data, the SONY Cache-1C would also abort its line fill. SKEN# is sampled again one cycle before the last BRDY#/RDY# to determine the cacheability of the line fill.

In order for the cache line to be stored as a write-back line, the PWT signals must be low when ADS# is sampled and the WB/WT# signals must be high with the first BRDY#. If either one of these requirement is not met, the line is stored as a write-through line.

When the CPU generates a write cycle, the SONY Cache-1C checks to see if it is a write hit. If it is a write hit to a write through line, as indicated in cycle 9, the SONY Cache-1C asserts START# to activate the system memory. When the system memory returns BRDY# or RDY#, the SONY Cache-1C updates its internal data ram and the cache line remains as write through. The above example shows a write through with one wait state. The SONY Cache-1C can also handle write cycles with zero wait state. In that case, the BRDY# signal is asserted one cycle earlier than what is shown in the above example.

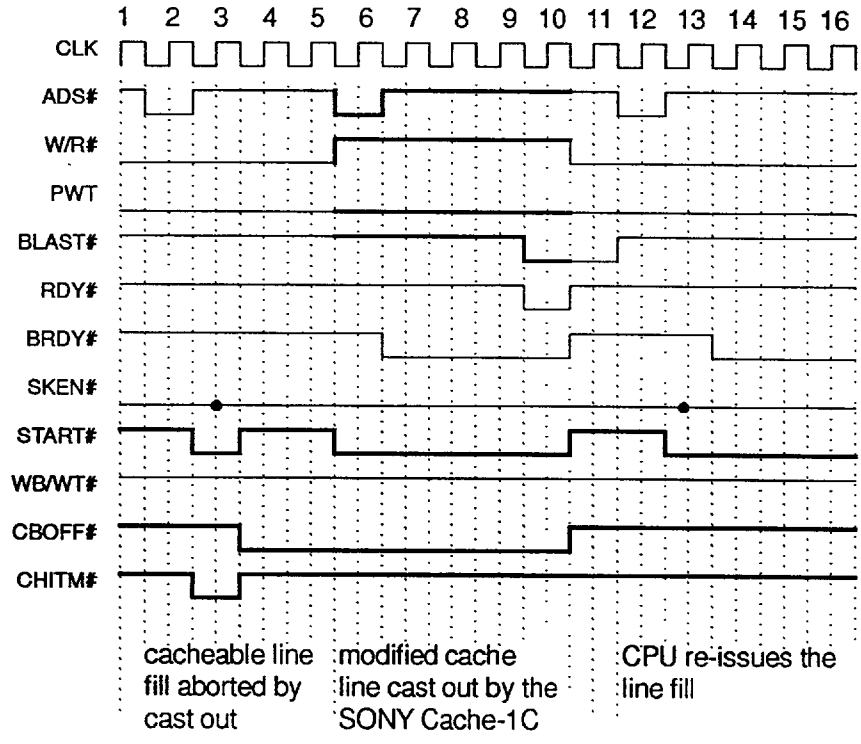
In cycle 12, the write cycle generates a write hit to a write back line. The SONY Cache-1C asserts BRDY# in the following cycle to complete the write cycle. The BLAST# signal indicates to the SONY

Cache-1C that only one doubleword is written by the CPU. If BLAST# is not asserted, the SONY Cache-1C process the write cycle as a burst write and continue to write to the cache line until either four doublewords has been written or BLAST# is asserted, whichever occurs earlier. WB/WT# is driven high by the SONY Cache-1C to indicate a write back hit.

In cycle 14, the write cycle also generates a write hit to a write-back line. But since PWT is driven high by the CPU, the SONY Cache-1C process the write cycle as write through

When the CPU reads from the memory, the SONY Cache-1C looks up the address to determine if it is a read hit. If it is a read hit, as indicated in cycle 17 and cycle 19, the SONY Cache-1C provides the read data, asserts BRDY#, and drives WB/WT# according to the write policy of the cache line. The read cycle is terminated when the CPU asserts BLAST# or after four doublewords has been returned by the SONY Cache-1C, whichever occurs earlier.

3.2 Line fill with cast out due to modified data



* A thick signal line indicates that the signal is driven by the SONY Cache-1C
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

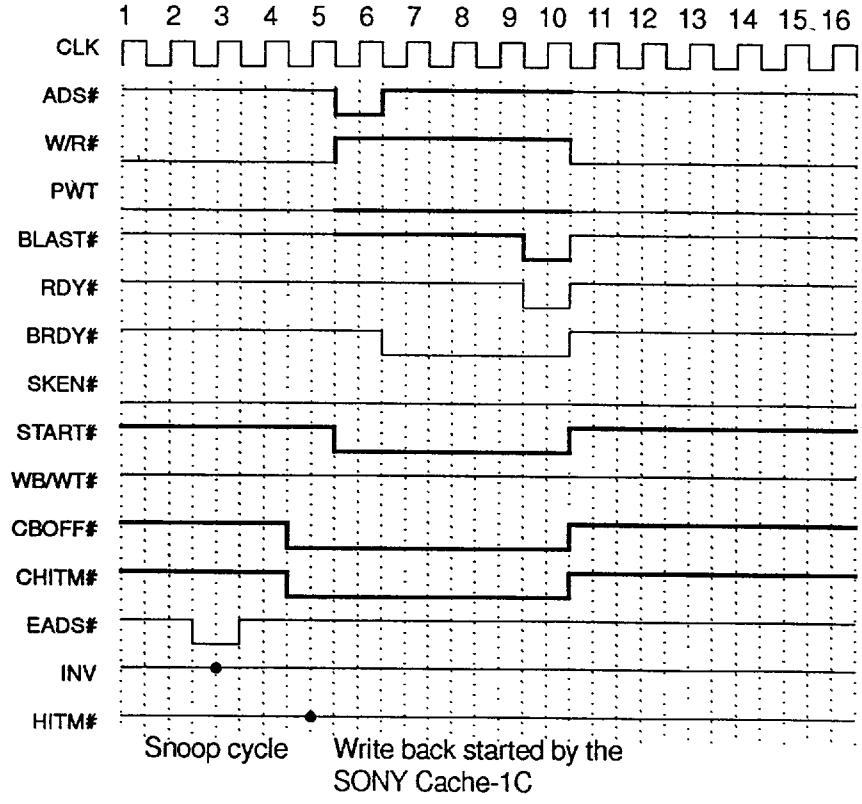
Figure 3.2. Line fill with cast out

When the CPU starts a cacheable line fill, the SONY Cache-1C writes the new data into its internal data ram. If the same entry in the data ram already contains modified data, the SONY Cache-1C must first cast out the modified line to the system memory before processing the line fill. When this condition is detected, the SONY Cache-1C asserts CBOFF# as soon as cacheability can be determined. In the example shown in figure 3.2, CBOFF# is asserted at cycle 3 after SKEN# is sampled active at the end of cycle 2.

CBOFF# should be directed to the BOFF# input of the CPU so it aborts the read cycle and relinquish control of the host bus to the SONY Cache-1C. The SONY Cache-1C asserts ADS# and START# in cycle 6 to start the cast out cycle. It samples CBRDY# and CRDY# to determine when the write data is accepted by the system memory. BLAST# is asserted when the last doubleword is cast out to the system memory.

CBOFF# is de-asserted after the cast out is completed. Upon seeing CBOFF# becomes inactive, the CPU re-issues the memory read. Since the modified cache line is already cast out, the line fill proceeds normally.

3.3 EADS cycle



* A thick signal line indicates that the signal is driven by the SONY Cache-1C
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.3. EADS cycle

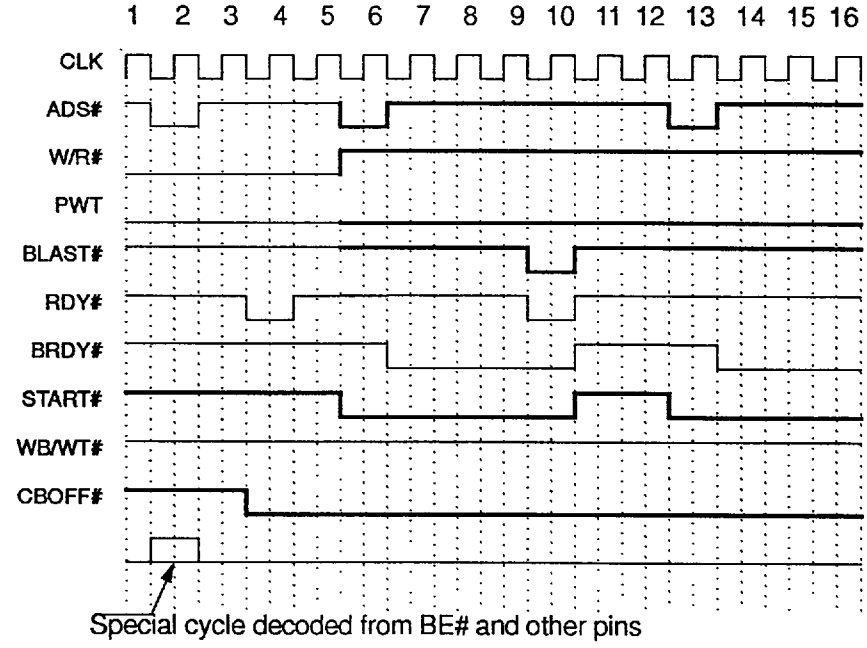
The SONY Cache-1C supports EADS# snoop in back off cycles and in normal cycles when the SONY Cache-1C is not processing a burst operation. The figure 3.3 shows the timing of a snoop cycle. When EADS# is sampled active, the SONY Cache-1C looks up the address to determine if it is a hit and if the cache line contains modified data. If it is a snoop miss, the SONY Cache-1C would not take any action. If it is a snoop hit, the way it is handled is determined by the state of INV pin when EADS# is sampled and by whether the cache line contains modified data.

If the cache line is modified, the SONY Cache-1C will write-back the entire cache line to the system memory. The SONY Cache-1C indicates a write-back cycle by asserting both CHITM# and CBOFF# in cycle 4. The SONY Cache-1C samples HITM# at the end of the same cycle. HITM# is driven by the CPU to indicate modified cache line hit in the L1 cache. If it is active, the SONY Cache-1C aborts the write-back immediately because the CPU contains the most updated data of the cache line. The CPU will perform a write-back cycle and keeps HITM# asserted until the write-back is completed. The SONY Cache-1C monitors the write-back cycle like all other ADS# cycles and updates the cache line during the write-back cycle.

If HITM# is sampled inactive, the write-back cycle is continued by the SONY Cache-1C. It asserts ADS# and START# and other control signals to indicate a memory write cycle. All four doubleword of the cache line are written back to the system memory. CBOFF# and CHITM# are de-asserted when write-back is completed.

The status of the cache line is updated after the write-back cycle. If INV is active, the cache line is invalidated after the write-back is completed by either the CPU or the SONY Cache-1C. If INV is not active, the cache line is changed to write-through.

3.4 Flush cycle



* A thick signal line indicates that the signal is driven by the SONY Cache-1C
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.4. FLUSH cycle

The SONY Cache-1C decodes the flush special bus cycle. The flush special bus cycle is identified by BE#[3:0] = 1101, D/C# = 0, M/IO# = 0, W/R# = 1, and ADDR[2] = 0. The SONY Cache-1C asserts CBOFF# as soon as the flush cycle is detected. It then wait until the system logic returns either the RDY# or BRDY# signals. The SONY Cache-1C then sequences through its internal tag ram looking for modified data. It writes back each modified cache line by initiating a burst write sequence. Each cache line requires two clock cycles to verify and the cache entry is invalidated regardless whether write back is required. After all the cache lines has been verified or written back, CBOFF# is de-asserted to return to normal state. The SONY Cache-1C does not start the flush write back sequence if it has not created any modified cache line since the last reset or flush, but the internal cache line is always flushed.

Flush sequence can be interrupted by SBOFF# to process snoop cycles. After SBOFF# is de-asserted, the flush cycle resumes.

3.5 Power down mode

Power-down mode is controlled by the ENABLE# input signal. During normal operation, ENABLE# must be asserted (low). If ENABLE# is de-asserted, the SONY Cache-1C will enter power down mode in four cycles. During power down, the SONY Cache-1C does not respond to any external inputs, including RESET. Most of the internal blocks, including the clock buffer, are shut down to conserve power. The SONY Cache-1C returns to normal operation mode two cycles after ENABLE# is re-asserted.

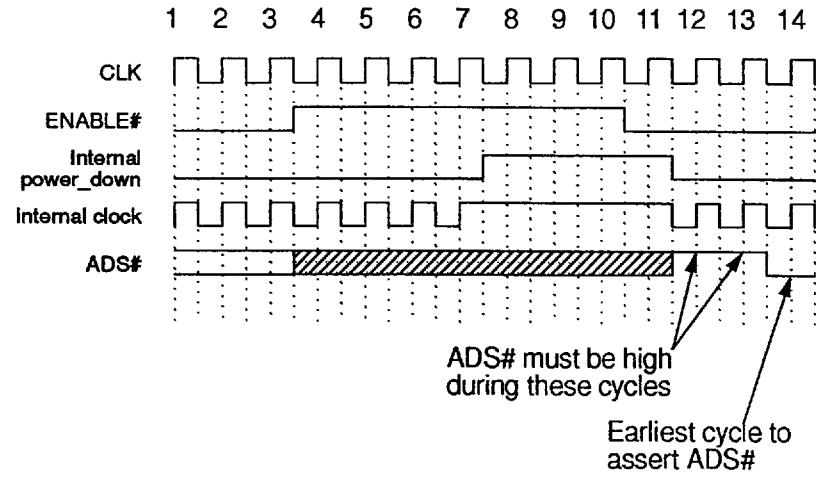


Figure 3.5. Power-down Timing

4 I/O Signals Generation

This section describes most of the control signals in typical system configurations.

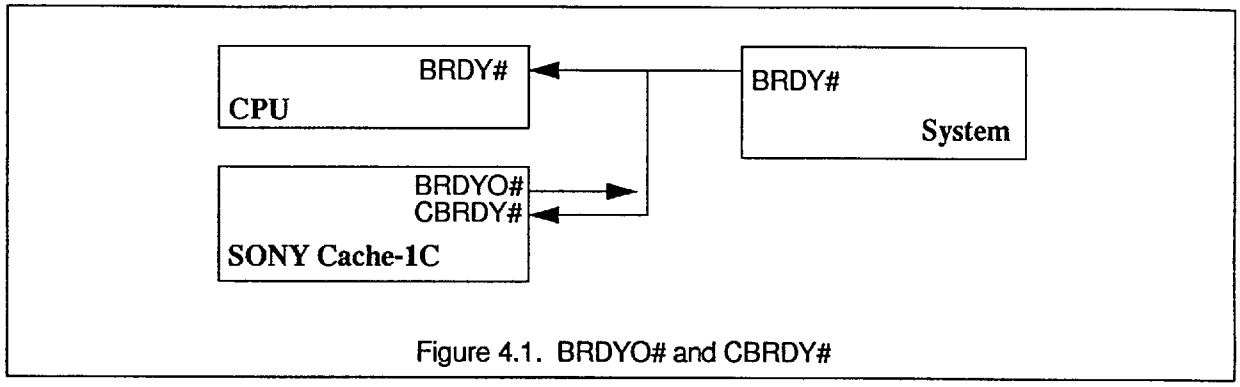


Figure 4.1. BRDYO# and CBRDY#

4.1 CBRDY# and BRYO#

The CBRDY# and BRDYO# pins of the SONY Cache-1C should be connected together externally to form an I/O pin. This pair of I/O pin should be wired-OR with the BRDY# pin driven by the system memory. The BRDYO# output of the SONY Cache-1C is normally tri-stated. During read hit and write hit to write back lines, the SONY Cache-1C drives this signal low to indicate a hit cycle. At the end of the hit cycle, this signal is driven high for one cycle and then tri-stated. The system logic should tri-state its BRDY# output when it is driven by the SONY Cache-1C cycles. In read miss and write-through cycles, the SONY Cache-1C samples CBRDY# at the same time as the CPU samples BRDY#.

4.2 CRDY# and RDYO#

The CRDY# and RDYO# pins of the SONY Cache-1C should be connected together externally to form an I/O pin in the same way CBRDY# and BRDYO# are connected together. These signals are used to indicate non-burst ready for external access cycles.

4.3 START#

START# is used by the SONY Cache-1C to signal any cycle that requires services from the system memory. These cycles are read miss, write miss and write through cycles. The system memory controller can monitor this signal instead of the ADS# signal from the CPU to activate the system memory. The system logic should still monitor the ADS# signal from the CPU to detect I/O cycles.

4.4 SKEN#

The signal is driven by the system logic and sampled by both the CPU and the SONY Cache-1C to determine cacheability of any read data. The system logic should drive this signal low during read hit cycles so that read hit in the SONY Cache-1C become cacheable in the CPU's internal cache.

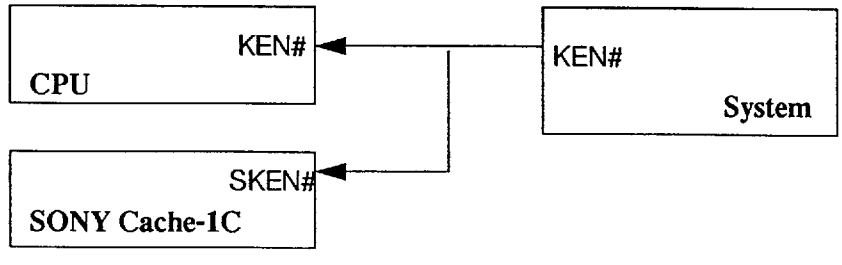


Figure 4.2. SKEN# and KEN#

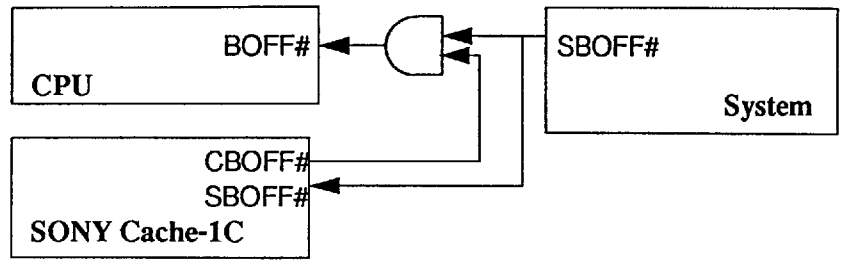


Figure 4.3. SBOFF# and CBOFF#

4.5 CS#

The Chip Select signal should be tied low (active) during normal operation. If CS# is driven high, the SONY Cache-1C does not responds to any memory access or snoop cycle.

4.6 CBOFF# and SBOFF#

CBOFF# is driven by the SONY Cache-1C when it needs to control the host bus to write-back a cache line. Write-back is required when a snoop or flush cycle hits a modified cache line or data eviction is needed before a line fill. If the system logic also needs to back-off the CPU, it should drives the SBOFF# input to indicate to the SONY Cache-1C that the CPU is back-off. The CBOFF# and SBOFF# signals should be combined together externally to form the BOFF# input to the CPU.

4.7 HITM#

This is an input signal designed to used with CPU that contains internal write-back cache. Since the 486 has write-through internal cache, this signal should be tied high at all time.

4.8 CHITM#

The CHITM# signal is driven active by the SONY Cache-1C to indicate that a snoop cycle hits a modified cache line. It should be sampled by the system logic two cycles after EADS# is asserted.

4.9 INV

The INV input controls the type of snoop cycle to be performed. It is sampled at the same time as EADS#. If it is active (high) and the snoop cycle is hit, the cache line will be invalidated. If INV is low, the snooped cache line will be changed to write-through. Regardless of INV, the snooped cache line is always written-back to the system memory if it contains modified data.

4.10 MODE[4:0]

The mode pins are used to select between cascade or stand-alone mode. The cascade mode allows two SONY Cache-1C chips to work together to provide 256K bytes of cache memory. Stand-alone mode requires only one SONY Cache-1C chip and it provides 128K bytes of cache memory. In cascade mode, the mode pins of one of the SONY Cache-1C chip should be set to

MODE[4:0] = 01100

while the second SONY Cache-1C chip should have the mode pins set to

MODE[4:0] = 01101

In stand-alone mode, the mode pins should be set to

MODE[4:0] = 00000

All other combinations are reserved.

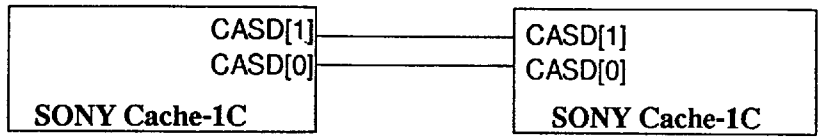


Figure 4.4. CASD signals

4.11 CASD[1:0]

The CASD pins are used for communication between the SONY Cache-1C chips during cascade mode. They should be connected together as shown in Figure 4.4. When the SONY Cache-1C is operating in stand-alone mode, the CASD[1:0] pins should be left unconnected.

4.12 Signals in Cascade Mode

When two SONY Cache-1C chips connected together in Cascade Mode to form a 256K cache subsystem, most of the pins are connected in parallel to both SONY Cache-1C chips. From the system hardware's point of view, the two chip subsystem has the same interface as a single SONY Cache-1C chip. The MODE pins connected to both SONY Cache-1C chip should indicate Cascade Mode and one of the chip is designated as chip1 while the other is designated as chip0. The static output and the debug outputs, PRSN#, ID[2:0], CASD[2] and ACTIVE, should not be connected. The CASD[1] and CASD[0] pins should be connected between the SONY Cache-1C chips. These pins are used for inter-chip communication and are not used by the system logic.

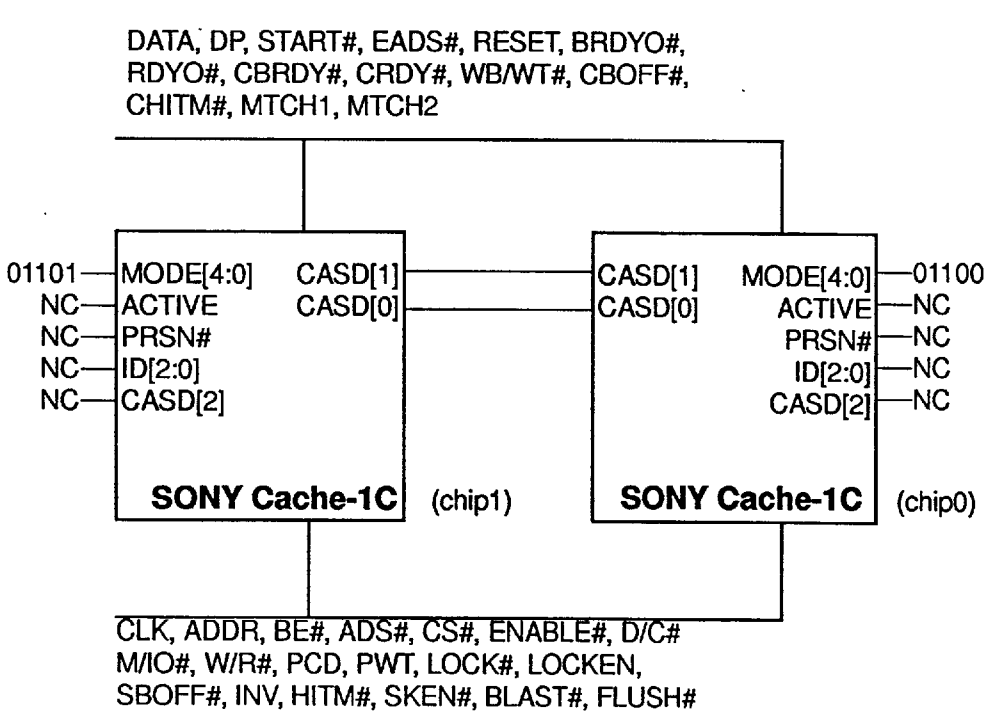


Figure 4.5. Two SONY Cache-1C chips connected in Cascade

5 Electrical Characteristics

5.1 Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-1.0 to +7	V
Input Voltage	VIN	-0.5 to Vcc + 0.5	V
Junction (Operating) Temperature	T_J	0 to +125	°C
Ambient (Operating) Temperature	TOPR	0 to +70	°C
Storage Temperature	TSTG	-65 to +150	°C

5.2 DC Characteristics

Item	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Input low voltage	V_{IL}	-0.3	+0.8	V
Input high voltage	V_{IH}	2.2	Vcc + 0.3	V
Output low voltage @4.5mA	V_{OL}		0.4	V
Output high voltage @-1.0mA	V_{OH}	2.4		V
Input leakage current	I_{LI}	-1	1	µA
Output leakage current	I_{LO}	-1	1	µA
Supply current @ 33 MHz, read hit †	I_{CC1}		450	mA
Supply current @ 33 MHz, line fill †	I_{CC2}		400	mA
Supply current @ 33 MHz, write hit †	I_{CC3}		350	mA
Supply current @ 33 MHz, idle †	I_{CC4}		325	mA
Power down current	I_{CC5}		100	mA
Capacitance: CQFP	Cin			
Clock pin			9	pF
Other input pins			7	pF
Output pins			9	pF
I/O pins			9	pF

† All Icc are measured with 0pF loading on the data pins and 30 pF on all control pins

5.3 A.C. Characteristics

Symbol	Parameter	33MHz		Fig
		Min (ns)	Max (ns)	
t_1	CLK Period	30		5.1
t_2	CLK High Time	11		5.1
t_3	CLK Low Time	11		5.1
t_4	CLK Fall Time		3	5.1
t_5	CLK Rise Time		3	5.1
t_{6a}	ADDR, BE0#-BE3# Setup	13		5.2
t_{6b}	ADDR, BE0#-BE3# Hold	3		5.2
t_{7a}	ADS#, M/IO#, W/R#, D/C# Setup	13		5.2
t_{7b}	ADS#, M/IO#, W/R#, D/C# Hold	3		5.2
t_{8a}	LOCK#, LOCKEN, PCD, PWT Setup	13		5.2
t_{8b}	LOCK#, LOCKEN#, PCD, PWT Hold	3		5.2
t_{9a}	BLAST# Setup	9		5.2
t_{9b}	BLAST# Hold	3		5.2
t_{10a}	CRDY#, CBRDY# Setup	8		5.2
t_{10b}	CRDY#, CBRDY# Hold	3		5.2
t_{11a}	SKEN# Setup	5		5.2
t_{11b}	SKEN# Hold	3		5.2
t_{12a}	DATA, DP0-DP3 Setup	5		5.2
t_{12b}	DATA, DP0-DP3 Hold	3		5.2
t_{13a}	WB/WT# Setup	8		5.2
t_{13b}	WB/WT# Hold	3		5.2
t_{14a}	SBOFF#, ENABLE#, INV Setup	8		5.2
t_{14b}	SBOFF#, ENABLE#, INV Hold	3		5.2
t_{15a}	EADS#, RESET, FLUSH# Setup	8		5.2
t_{15b}	EADS#, RESET, FLUSH# Hold	3		5.2
t_{16a}	HITM# setup	10		5.2
t_{16b}	HITM# Hold	3		5.2
t_{17a}	CS# Setup	6		5.2
t_{17b}	CS# Hold	3		5.2

Symbol	Parameter	33MHz		Fig
		Min (ns)	Max (ns)	
t_{19a}	ADDR, BE# Valid delay	3	18	5.3,5.4
t_{19b}	ADDR, BE# Float delay	3	20	5.5
t_{20a}	ADS#, M/IO#, W/R#, D/C# Valid delay	3	16	5.3,5.4
t_{20b}	ADS#, M/IO#, W/R#, D/C# Float delay	3	20	5.5
t_{21a}	LOCK#, LOCKEN, PCD, PWT Valid delay	3	16	5.3,5.4
t_{21b}	LOCK#, LOCKEN, PCD, PWT Float delay	3	20	5.5
t_{22a}	BLAST# Valid delay	3	20	5.3,5.4
t_{22b}	BLAST# Float delay	3	20	5.5
t_{23a}	BRDYO#, RDYO# Valid delay	3	18	5.3,5.4
t_{23b}	BRDYO#, RDYO# Float delay	3	20	5.5
t_{24a}	DATA, DP Valid delay	3	20	5.3,5.4
t_{24b}	DATA, DP Float delay	3	20	5.5
t_{25}	CBOFF# Valid delay	3	20	5.3,5.4
t_{27}	START# Valid delay	3	17	5.3,5.4
t_{28}	CHITM# Valid delay	3	19	5.3,5.4
t_{29a}	WB/WT# Valid delay	3	18	5.3,5.4
t_{29b}	WB/WT# Float delay	3	20	5.5

Notes:

All AC characteristics are measured with input voltage switching from 0V to 3V. Input and Output references are at 1.5V, except float delay.

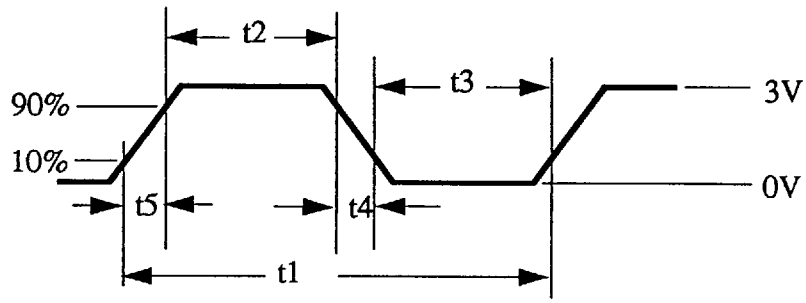
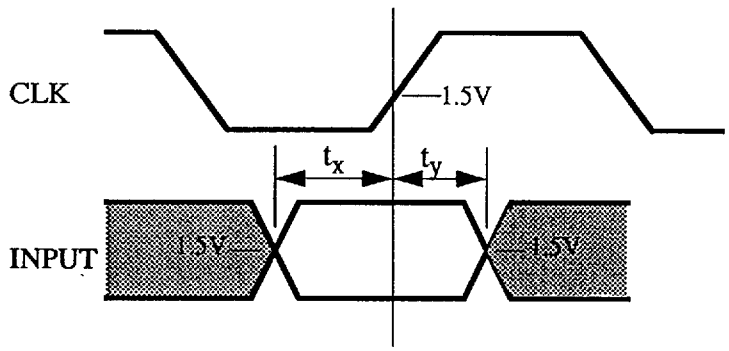
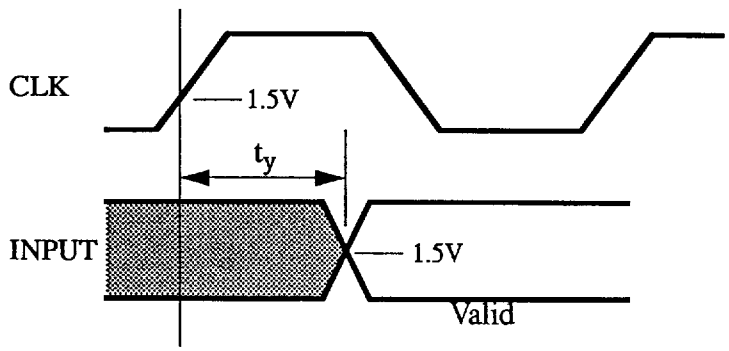


Figure 5.1. Clk Waveform



$t_x = t_{6a,7a,8a,9a,10a,11a,12a,13a,14a,15a,16a,17a}$
$t_y = t_{6b7b,8b,9b,10b,11b,12b,13b,14b,15b,16b,17b}$

Figure 5.2. Setup and Hold Timings



$t_y = t_{19a,20a,21a,22a,23a,24a,25,27,28,29a}$

Figure 5.3. Valid Delay Timings

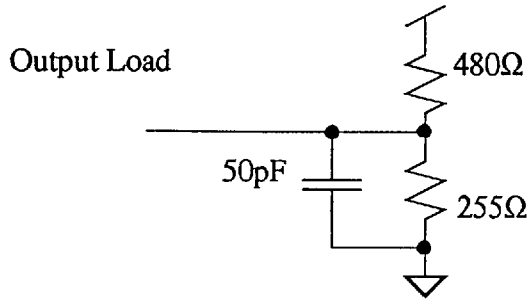
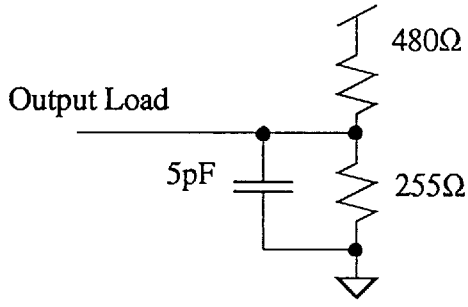


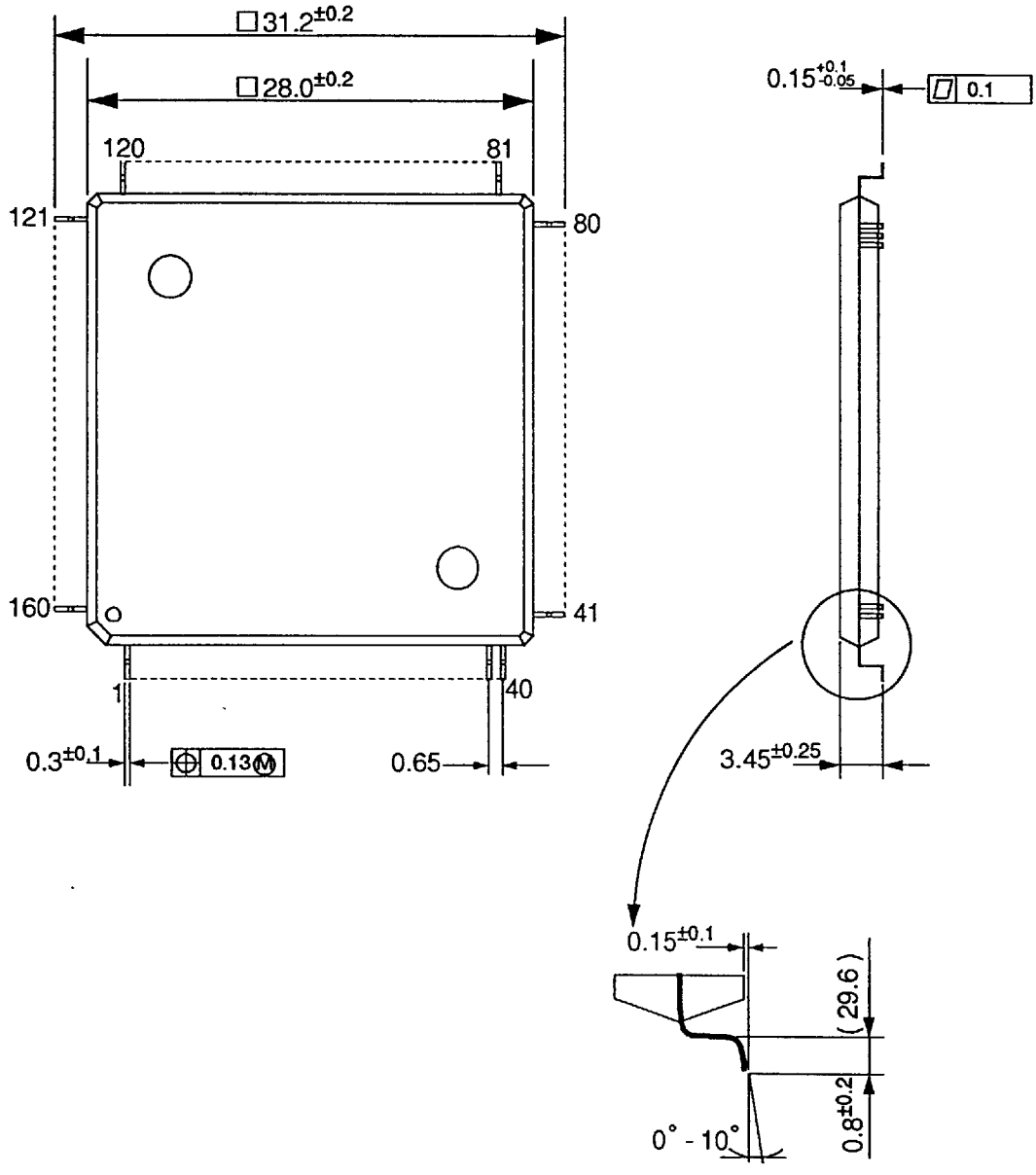
Figure 5.4. Output Load for Valid Delay



- Transition is measured ±200mV from steady voltage with specified loading
- Float delay is not tested.

Figure 5.5. Output Load for Float Delay

6 Mechanical Specification



SONY NAME	QFP-160P-L01
EIAJ NAME	*QFP160-P-2828-A
JEDEC CODE	

Package Thermal Resistance

Parameter	Air Flow (Meters/Second)			
	0	1 m/s	2 m/s	3 m/s
$Ø_{JA}$ (°C/W)	30.5	22.6	20.4	17.7
$Ø_{JC}$ (°C/W)	6.3			

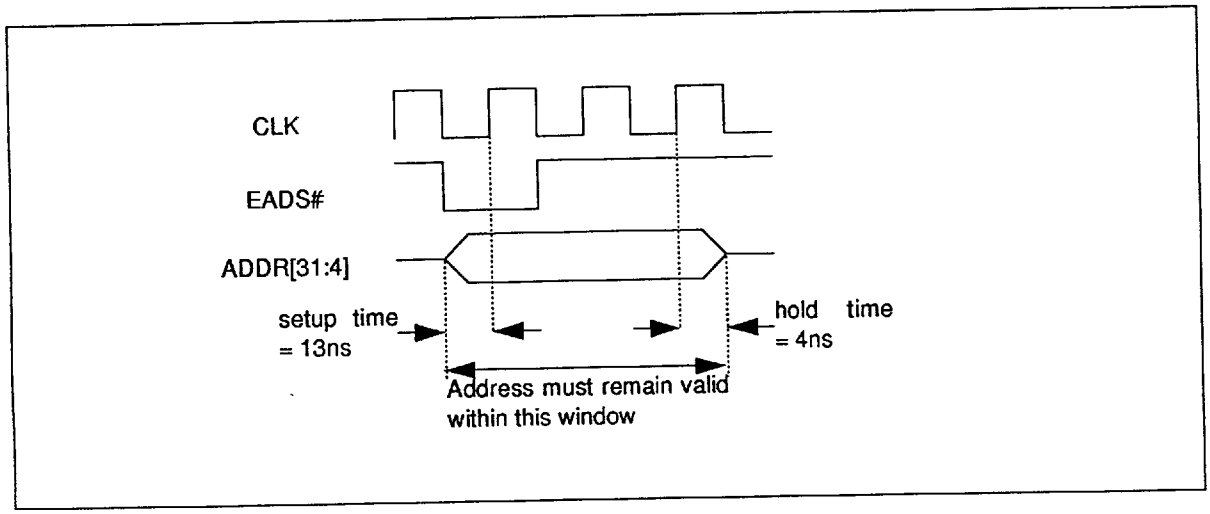
Errata (This applies to Rev. I stepping only)

The current Rev.I stepping of the SONY Cache-1C has one known errata. Previous stepping of the SONY Cache-1C was never moved into production.

1 Snoop address hold time

Description: Two internal problems at the snoop address input flip-flop contribute to this errata. They are caused by the gating voltage level of an internal latch and the hold time violation of another latch in the address path. As a result of this problem, the SONY Cache-1C does not hold the snoop address internally.

Work around: During snoop cycles, the system must hold the snooping address for two extra cycles after EADS# is asserted. The following diagram shows the required address timing with this errata.



Disposition: This errata will be fixed in the next stepping and in SONY Cache-1CA