Data Book

F Logic (SN54/74F)

1989

TEXAS INSTRUMENTS

F Logic (SN54/74F)

Data Book

2nd Edition

1989

General Information 1

Data Sheets 2

Application Report 3

Mechanical Data 4

F Logic Data Book

2nd Edition

TEXAS INSTRUMENTS

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INTRODUCTION

In this volume, Texas Instruments presents technical information on the SN54F/SN74F TTL logic family. The combination of the SN54F/SN74F family with Texas Instruments other advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS) and Advanced Schottky (AS), offers the industry the broadest spectrum of advanced bipolar logic products available from any supplier. In addition, the SN54F/SN74F TTL logic family provides the system designer with a pin-for-pin compatible alternate source for 54F/74F devices in standard 300-mil plastic dual-in-line packages (DIPs) along with plastic "small outline" (SO) packages, ceramic chip carriers, and ceramic DIPs. Texas Instruments offers all of the above packages with the service levels, quality, and reliability that users have come to expect in a logic family.

The SN54F/SN74F TTL data sheets have been configured for ease of use. They stand alone and require a minimum of reference to other sections for supporting information. Each data sheet has complete absolute maximum ratings, recommended operating conditions, timing requirements (if applicable), and electrical characteristics. The input/output loading and fan-out characteristics of each circuit are specified in terms of actual load-current value in amperes. Pin-outs are specified using Texas Instruments TTL name conventions.

The following definitions are for the system design engineer who prefers to use unit loads. One unit load in the high state is defined to be 20 microamperes. One unit load in the low state is defined to be 0.6 milliamperes.

Logic symbols prepared in accordance with IEEE and IEC standards, logic diagrams, and pinout assignments are provided for all SN54F/SN74F TTL devices. The logic diagrams are provided for the understanding of the logic operation of the device and should not be used to estimate propagation delays.Package dimensions given in the Mechanical Data section of this book are in metric measurements with inches in parenthesis. This is to simplify board layout for designers involved in metric conversion and new designs.

The Texas Instruments SN54F/74F TTL logic family offers several new SN54F/SN74F logic devices. Included among the new functions are:

'F286	—	9-bit parity generator with bus driver parity I/O port
'F518, 'F519, 'F520	—	8-bit identity comparators with input pull-up resistors and open-collector outputs
'F621, 'F622	—	Open-collector octal-bus transceivers.

The devices offered can be characterized into distinct logic functions that address several different application areas. The following functional group table summarizes these groups and lists specific application areas that the functions address.

†The integrated Schottky-barrier diode-clamped transistor is patented by Texas Instruments Incorporated (U.S. Patent Number 3,463,975).

FUNCTIONAL GROUPS

FUNCTION	APPLICATIONS
Binary/Decade Counters	Synchronous dividers and multipliers Timing circuits and state machine sequencers Pulse and sync generation Code conversion circuits Analog-to-digital and digital-to-analog conversion circuits Modulo-n event counters and rate multipliers
Decoders	Memory, board, processor, and component enable generation Minterm generation and data-flow control Clock phase splitter and decoder trees Demultiplexing for clock distribution and scanning switch encoders Program counters and digital-display systems
Dual Flip-Flops	Extra register bits (e.g., guard bits and carry bits) Synchronizing asynchronous inputs, interrupts, and control signals Finite or algorithmic state machine "state" bits Customized modulo-n event counters
Gates	Combinational logic
Identity Comparators	Peripheral and board enables, address decodes, and cache tag comparisons Page memory boundary detection, page fault detection, and error detection and correction
Multiplexers/Demultiplexers	Implementing combinational logic (function) tables Data flow control and parallel-to-serial converters Multiplexing trees, asynchronous shifting, and sorting
Octal Buffers/Transceivers	Error detection and correction circuits Hamming code generation
Octal Flip-Flops	Bus interface, pipeline registers, and customized shift registers Ring counters, Johnson counters, pattern generators, and custom modulo-n event counters Synchronizing asynchronous inputs, interrupts, and control signals
Shifters/Shift Registers	Serial-to-parallel conversion or parallel-to-serial conversion Clock phase generation, custom counters, and random-number generators Pipeline registers, accumulators, and digital filters On-board diagnostics and multiply and divide by 2**N CPU design and array processors

This volume provides design and specification data for SN54F/SN74F TTL components. Complete technical data for any TI semiconductor product is available from the nearest TI field sales ofice, local authorized TI distributor, or directly by writing to:

Marketing and Information Services
Texas Instruments Incorporated
P.O. Box 655012, MS 308
Dallas, Texas 75265

ATTENTION

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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†For more information on these devices, contact the factory.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

*Current out of a terminal is given as a negative value.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**

The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state output, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a three-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

*Current out of a terminal is given as a negative value.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital cirucit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

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The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎏	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high, then without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect, and as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

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functional testing

Functional testing is performed on all logic devices by the execution of a set of functional patterns located in the test program. These patterns are used to guarantee conformance to the truth table and simulate operation in an actual system.

Problems are frequently discovered in functional testing when V_{IH} min and V_{IL} max are used as the input conditions to exercise the function table. V_{IH} min and V_{IL} max are input conditions that are used in parametric testing. The problems occur because of the noise that is present on the test heads of automated test equipment with long cables. Parametric test such as V_{OH}, V_{OL}, I_{OZH}, or I_{OZL} are done at a relatively slow repetition rate, and any noise that is present on the test head will have settled out before the outputs are measured. But during functional testing, the outputs are sensed much sooner, before the noise on the the inputs has settled out and the output has reached its final and correct state.

The functional patterns that are applied to the device under test are 0-volt to 3-volt transitions as defined in the parameter measurement section. The use of V_{IH} = 3 volts and V_{IL} = 0 volts during functional testing does not imply that the devices are noise sensitive since the environment that the device sees on a system's printed circuit board is much less severe than a noisy production test environment. Therefore, V_{IH} min and V_{IL} max should not be used to test functionality of 54/74 devices.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the SN54F/SN74F Family. In general, junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} (V_{CC} \cdot I_{CC} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to ambient air
V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum)
I_{CC} = supply current
N = the number of outputs
I_{OL} = the low-level output current
V_{OL} = the low-level output voltage
T_A = the ambient air temperature

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

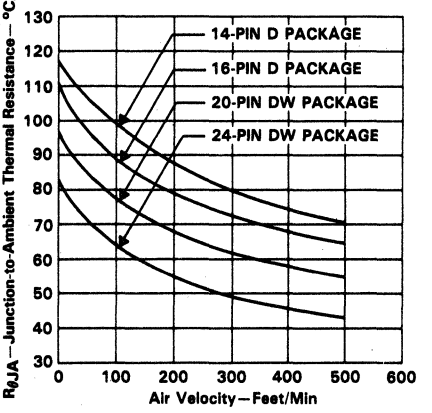


FIGURE 1

Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and V_{CC} = 5 volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population. Due to the specification practices that have been followed, it is useful to use slightly different calculations for SN54F and SN74F devices.

Maximum junction temperature for SN54 parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and V_{CC} = 5.5 volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of −55 °C to 125 °C will be higher than for a SN74F device at the temperature extremes of 0 °C to 70 °C.

The SN54F/74F family data sheets give a single maximum value for I_{CC}. If that value is used to calculate maximum junction temperature for SN74F devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of I_{CC} up to a practical maximum value for process variations and thermal effects.

Thus, for SN74F devices:

$$T_{Jmax} = R_{\theta JA} (5.5 \cdot 1.31 \cdot I_{CCtyp} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (2)$$

SERIES SN54F/SN74F DEVICES

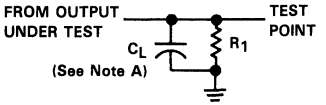


FIGURE 1. LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

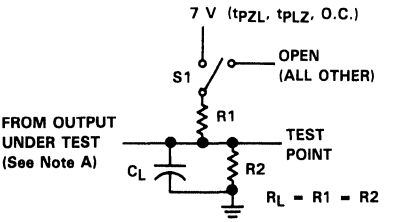
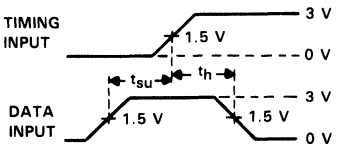
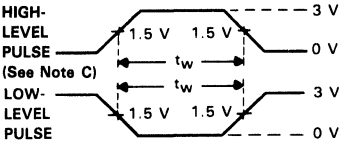


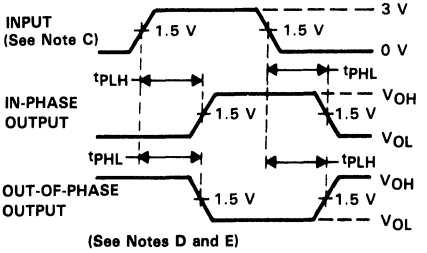
FIGURE 2. LOAD CIRCUIT FOR THREE STATE AND OPEN-COLLECTOR OUTPUTS



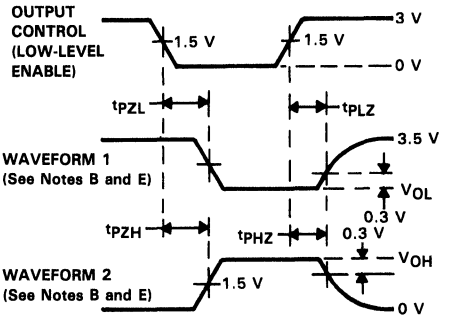
A. SETUP AND HOLD TIMES



B. PULSE WIDTHS



C. PROPAGATION DELAY TIMES



D. THREE-STATE OUTPUT ENABLE TIMES

FIGURE 3. VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics; PRR = 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
D. When measuring propagation delay times of three-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one transition per measurement.

General Information 1

Data Sheets 2

Application Report 3

Mechanical Data 4

D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

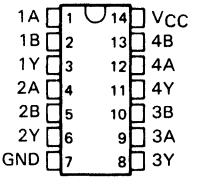
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54F00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F00 is characterized for operation from 0°C to 70°C.

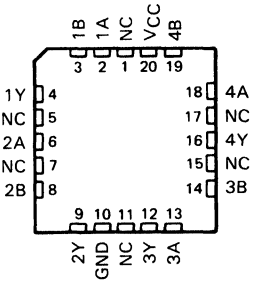
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54F00 . . . J PACKAGE
SN74F00 . . . D OR N PACKAGE
(TOP VIEW)

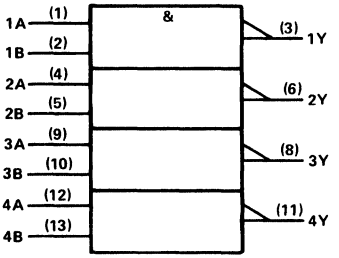


SN54F00 . . . FK PACKAGE
(TOP VIEW)



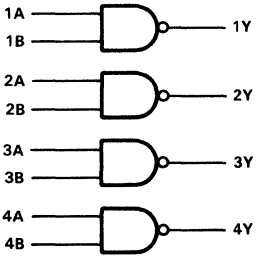
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F00 . . . . . −55°C to 125°C
SN74F00 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F00			SN74F00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F00			SN74F00			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		1.9	2.8		1.9	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		6.8	10.2		6.8	10.2	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F00			SN54F00		SN74F00		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.6	3.3	5	1.2	7	1.6	6	ns
t_{PHL}	A or B	Y	1	2.8	4.3	1	6.5	1	5.3	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

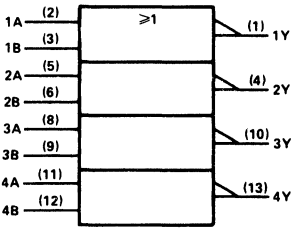
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54F02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F02 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

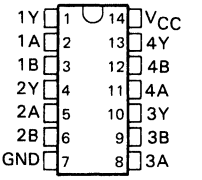
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

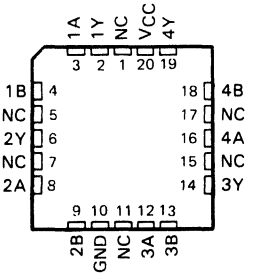


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F02 . . . J PACKAGE
SN74F02 . . . D OR N PACKAGE
(TOP VIEW)

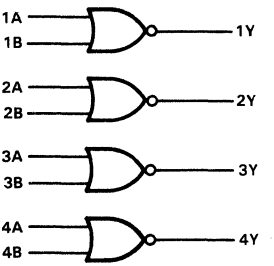


SN54F02 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F02 . . . . . −55°C to 125°C
SN74F02 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F02			SN74F02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F02			SN74F02			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		3.7	5.6		3.7	5.6	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 1		8.7	13		8.7	13	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F02			SN54F02		SN74F02		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.7	4	5.5	1.7	7.5	1.7	6.5	ns
t_{PHL}	A or B	Y	1	2.8	4.3	1	6.5	1	5.3	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CCL} is measured with one input at 4.5 V and all others grounded.
2. Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

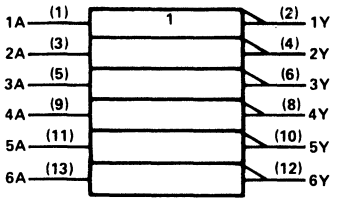
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54F04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F04 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

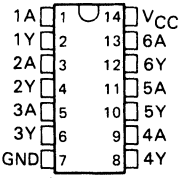
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

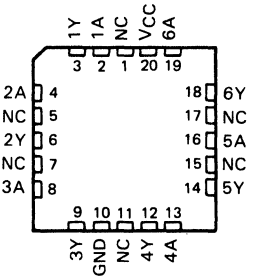


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F04 . . . J PACKAGE
SN74F04 . . . D OR N PACKAGE
(TOP VIEW)

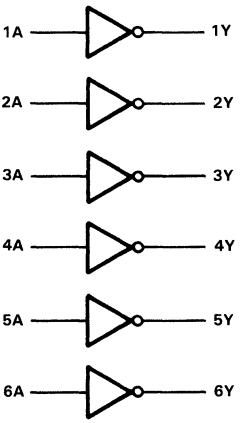


SN54F04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage[†] . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F04 . . . . . −55°C to 125°C
SN74F04 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

[†]The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F04			SN74F04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F04			SN74F04			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}[§]	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		2.8	4.2		2.8	4.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.2	15.3		10.2	15.3	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX[¶]				UNIT
			'F04			SN54F04		SN74F04		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.6	3.3	5	1.2	7	1.6	6	ns
t_{PHL}	A or B	Y	1	2.8	4.3	1	6.5	1	5.3	ns

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
[¶]For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

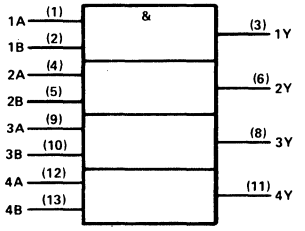
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54F08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F08 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

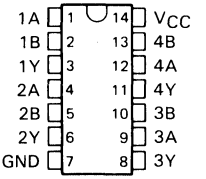
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

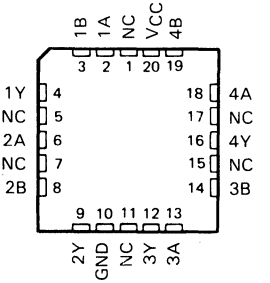


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F08 . . . J PACKAGE
SN74F08 . . . D OR N PACKAGE
(TOP VIEW)

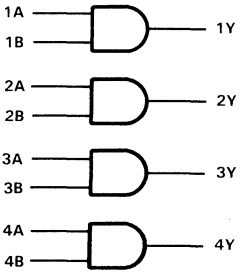


SN54F08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F08 . . . . . −55°C to 125°C
SN74F08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F08			SN74F08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F08			SN74F08			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.5	8.3		5.5	8.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		8.6	12.9		8.6	12.9	mA

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F08			SN54F08		SN74F08		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.2	3.8	5.6	1.7	7.5	2.2	6.6	ns
t_{PHL}	A or B	Y	1.7	3.6	5.3	1.2	7.5	1.7	6.3	ns

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

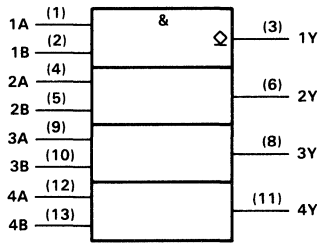
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54F09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F09 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

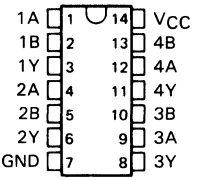
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

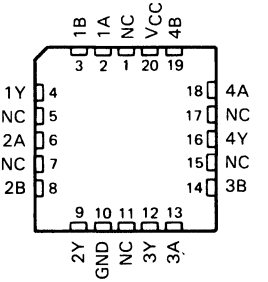


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F09 . . . J PACKAGE
SN74F09 . . . D OR N PACKAGE
(TOP VIEW)

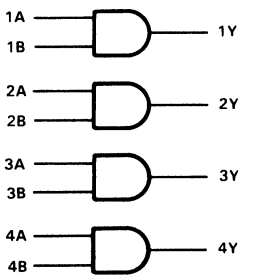


SN54F09 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 Data Sheets

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F09 . . . . . −55°C to 125°C
SN74F09 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F09			SN74F09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F09			SN74F09			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5	7.8		5	7.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		8.1	12.8		8.1	12.8	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F09			SN54F09		SN74F09		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	8	9.2	5	10.5	5	9.6	ns
t_{PHL}	A or B	Y	1.5	3.4	4.6	1.5	6	1.5	4.8	ns

‡All typical values are at V_{CC} = 5 v, T_A = 25°C.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

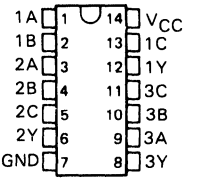
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54F10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F10 is characterized for operation from 0°C to 70°C.

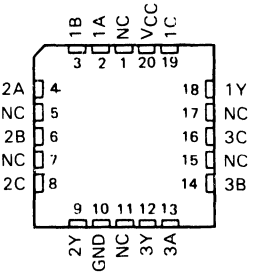
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54F10 . . . J PACKAGE
SN74F10 . . . D OR N PACKAGE
(TOP VIEW)

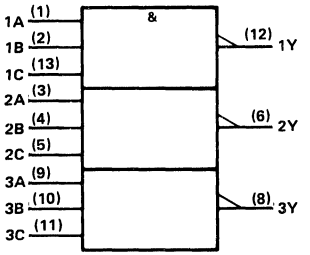


SN54F10 . . . FK PACKAGE
(TOP VIEW)



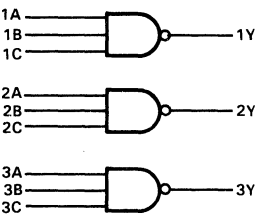
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F10 . . . . . −55°C to 125°C
SN74F10 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F10			SN74F10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F10			SN74F10			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		1.4	2.1		1.4	2.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.1	7.7		5.1	7.7	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F10			SN54F10		SN74F10		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.6	3.3	5	1.2	7	1.6	6	ns
t_{PHL}	A or B	Y	1	2.8	4.3	1	6.5	1	5.3	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

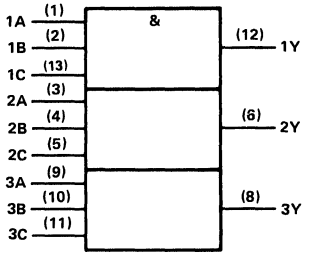
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ positive logic.

The SN54F11 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F11 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

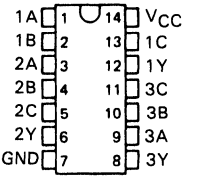
logic symbol†



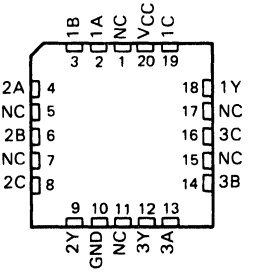
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54F11 . . . J PACKAGE
SN74F11 . . . D OR N PACKAGE
(TOP VIEW)

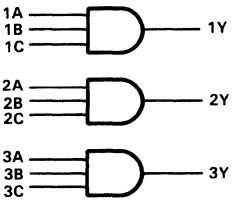


SN54F11 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 Data Sheets

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F11 . . . . . −55°C to 125°C
SN74F11 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F11			SN74F11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F11			SN74F11			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.1	6.2		4.1	6.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		6.5	9.7		6.5	9.7	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F11			SN54F11		SN74F11		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.2	3.8	5.6	1.7	7.5	2.2	6.6	ns
t_{PHL}	A or B	Y	1.7	3.7	5.5	1.2	7.5	1.7	6.5	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

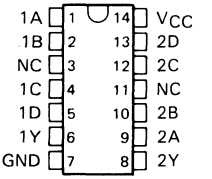
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F20 is characterized for operation from 0°C to 70°C.

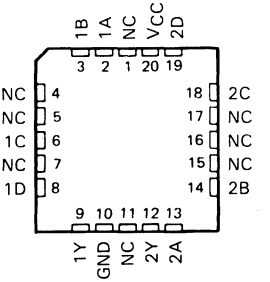
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54F20 . . . J PACKAGE
SN74F20 . . . D OR N PACKAGE
(TOP VIEW)

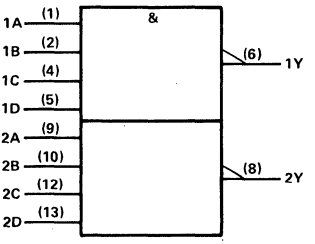


SN54F20 . . . FK PACKAGE
(TOP VIEW)



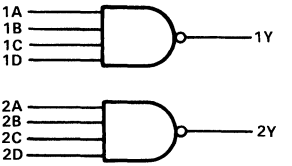
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F20 . . . . . −55°C to 125°C
SN74F20 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F20			SN74F20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F20			SN74F20			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.9	1.4		0.9	1.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.4	5.1		3.4	5.1	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F20			SN54F20		SN74F20		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.6	3.3	5	1.2	7	1.6	6	ns
t_{PHL}	A or B	Y	1	2.8	4.3	1	6.5	1	5.3	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

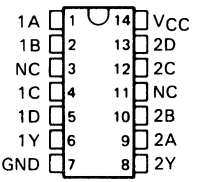
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F21 is characterized for operation from 0°C to 70°C.

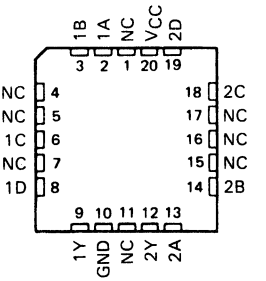
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

SN54F21 . . . J PACKAGE
SN74F21 . . . D OR N PACKAGE
(TOP VIEW)

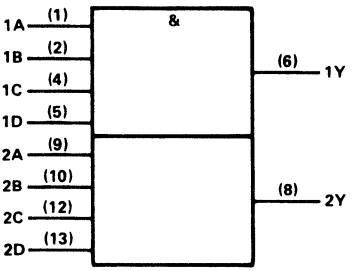


SN54F21 . . . FK PACKAGE
(TOP VIEW)



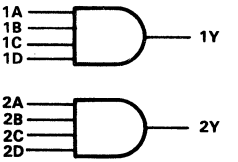
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F21 . . . . . −55°C to 125°C
SN74F21 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F21			SN74F21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F21			SN74F21			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.8	4.3		2.8	4.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		4.7	7.3		4.7	7.3	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F21			SN54F21		SN74F21		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	3.2	4.7	1	5.6	1	5.3	ns
t_{PHL}	A or B	Y	1.5	3.4	5.1	1.5	5.9	1.5	5.5	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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D2932, MARCH 1986—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

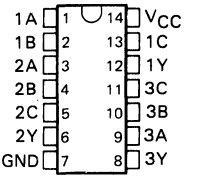
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A}\cdot\overline{B}\cdot\overline{C}$ in positive logic.

The SN54F27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F27 is characterized for operation from 0°C to 70°C.

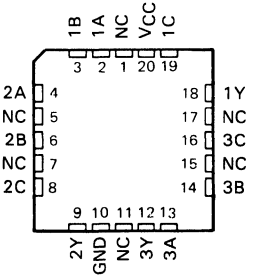
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

SN54F27 . . . J PACKAGE
SN74F27 . . . D OR N PACKAGE
(TOP VIEW)

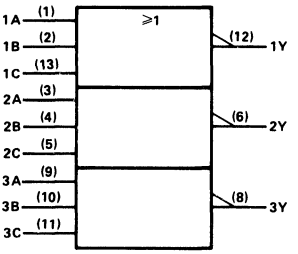


SN54F27 . . . FK PACKAGE
(TOP VIEW)



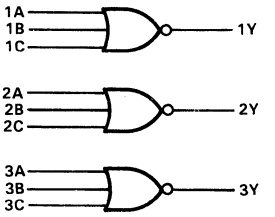
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F27 . . . . . −55°C to 125°C
SN74F27 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F27			SN74F27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F27			SN74F27			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		3.8	5.5		3.8	5.5	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 1		8.4	12		8.4	12	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F27			SN54F27		SN74F27		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.2	3.1	5	1	6	1	5.5	ns
t_{PHL}	A or B	Y	1	2.1	4.5	1	5.5	1	4.5	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CCL} is measured with one input at 4.5 V and all others grounded.
2. Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ or}$$

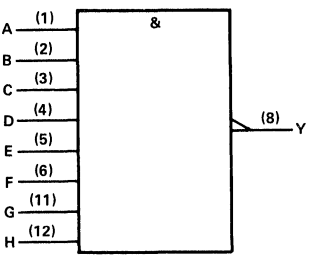
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54F30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F30 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

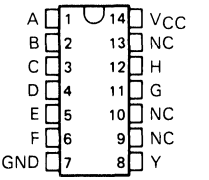
logic symbol†



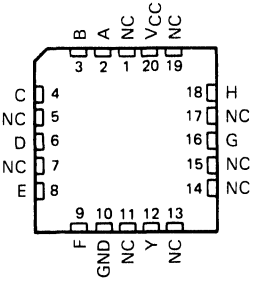
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54F30 . . . J PACKAGE
SN74F30 . . . D OR N PACKAGE
(TOP VIEW)

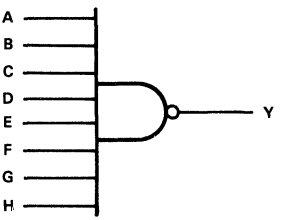


SN54F30 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F30 . . . . . −55°C to 125°C
SN74F30 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F30			SN74F30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F30			SN74F30			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.7	1.5		0.7	1.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.2	4		2.2	4	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F30			SN54F30		SN74F30		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A thru H	Y	1	3.1	5	1	6	1	5.5	ns
t_{PHL}			1	2.6	4.5	1	6	1	5	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

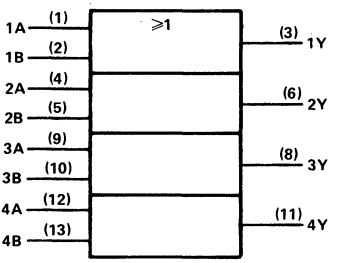
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54F32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F32 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

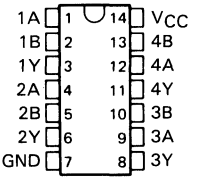
OUTPUT	INPUTS
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

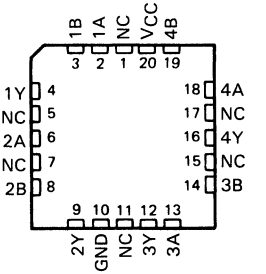


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F32 . . . J PACKAGE
SN74F32 . . . D OR N PACKAGE
(TOP VIEW)

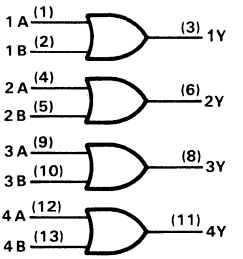


SN54F32 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F32 . . . . . −55°C to 125°C
SN74F32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F32			SN74F32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F32			SN74F32			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 1		6.1	9.2		6.1	9.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		10.3	15.5		10.3	15.5	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F32			SN54F32		SN74F32		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.2	3.8	5.6	2.2	7.5	2.2	6.6	ns
t_{PHL}			2.2	3.6	5.3	1.7	7.5	2.2	6.3	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CCH} is measured with one input per gate at 4.5 V and all others at ground.
2. Load circuits and waveforms are shown in Section 1.

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D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

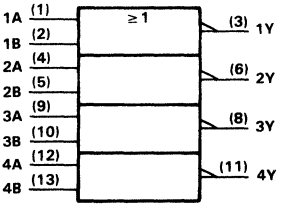
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54F36 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F36 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

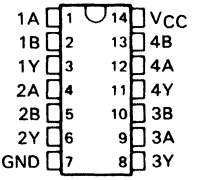
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

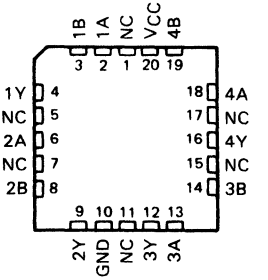


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F36 . . . J PACKAGE
SN74F36 . . . D OR N PACKAGE
(TOP VIEW)

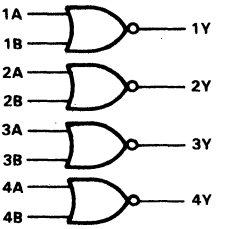


SN54F36 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 Data Sheets

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F36 . . . . . −55°C to 125°C
SN74F36 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F36			SN74F36			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F36			SN74F36			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		3.7	5.6		3.7	5.6	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 1		8.7	13		8.7	13	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶			UNIT
			'F36			SN54F36		SN74F36	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.7	4	5.5	1.7	7.5	1.7	6.5	ns
t_{PHL}			1	2.8	4.3	1	6.5	1	5.3	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CCL} is measured with one input per gate at 4.5 V and all others grounded.
2. Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3206, JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

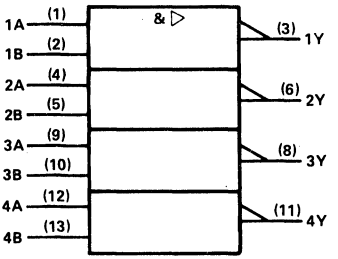
These devices contain four independent 2-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54F37 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F37 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

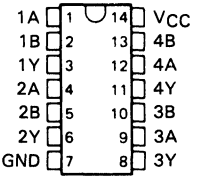
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

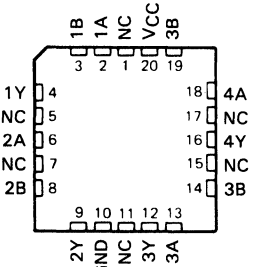


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F37 . . . J PACKAGE
SN74F37 . . . D OR N PACKAGE
(TOP VIEW)

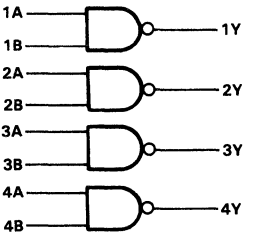


SN54F37 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −0.5 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range: SN54F37 . . . . . −55°C to 125°C
SN74F37 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F37			SN74F37			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−15			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F37			SN74F37			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA		−0.73	−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			2			
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.35	0.5				V
		I_{OL} = 64 mA					0.40	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		23	33		23	33	mA

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F37			SN54F37		SN74F37	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	3.1	5.5			1.5	6.5	ns
t_{PHL}			1	2.1	4.5			1	5	

PRODUCT PREVIEW

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

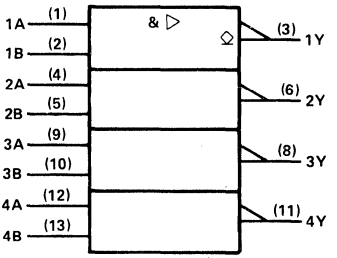
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54F38 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F38 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

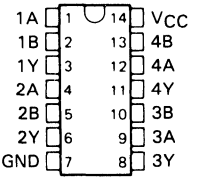
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

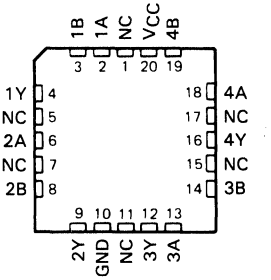


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F38 . . . J PACKAGE
SN74F38 . . . D OR N PACKAGE
(TOP VIEW)

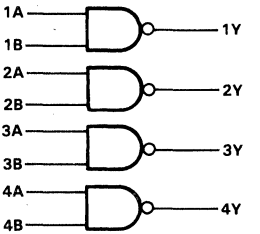


SN54F38 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −0.5 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range: SN54F38 . . . . . −55°C to 125°C
SN74F38 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F38			SN74F38			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
V_{OH}	High-level output voltage			4.5			4.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F38			SN74F38			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA		−0.73	−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V				250			250	μA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.4	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		4	7		4	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		22	30		22	30	mA

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡			UNIT
			'F38			SN54F38		SN74F38	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	6.7	9.6	12.5			6.7	13	ns
t_{PHL}			1	2.6	5			1	5.5	

PRODUCT PREVIEW

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3208, JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

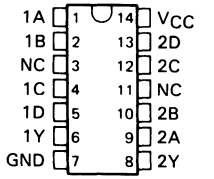
These devices contain two independent 4-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F40 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F40 is characterized for operation from 0°C to 70°C.

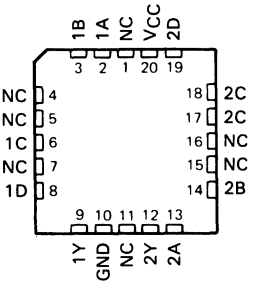
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54F40 . . . J PACKAGE
SN74F40 . . . D OR N PACKAGE
(TOP VIEW)

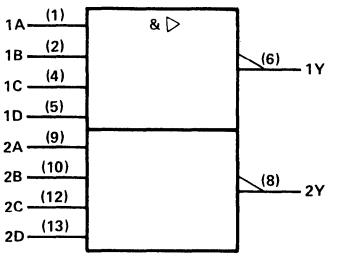


SN54F40 . . . FK PACKAGE
(TOP VIEW)



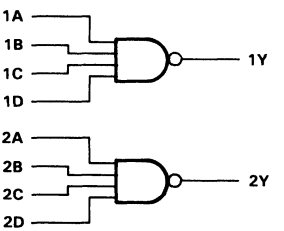
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −0.5 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range: SN54F40 . . . . . −55°C to 125°C
SN74F40 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F40			SN74F40			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−15			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F40			SN74F40			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA		−0.73	−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			2			
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.35	0.5				V
		I_{OL} = 64 mA					0.4	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		1.75	4		1.75	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶			UNIT
			'F40			SN54F40		SN74F40	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	3.6	6			1.5	7	ns
t_{PHL}			1	2.6	5			1	5.5	

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3209, JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

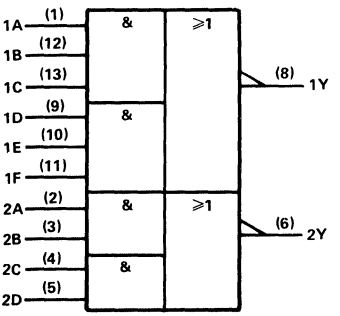
The F51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The devices perform the following Boolean functions:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}.$$

The SN54F51 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F51 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLES

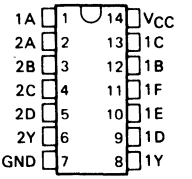
GATE 1

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

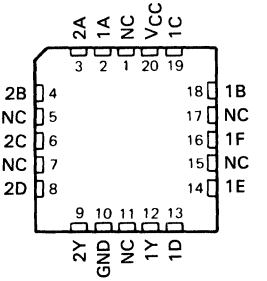
GATE 2

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

SN54F51 . . . J PACKAGE
SN74F51 . . . D OR N PACKAGE
(TOP VIEW)

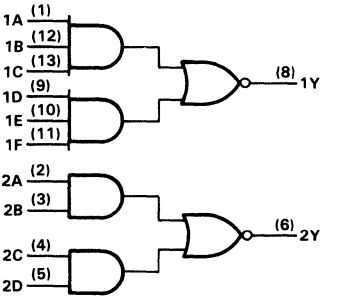


SN54F51 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 Data Sheets

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absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F51 . . . . . −55°C to 125°C
SN74F51 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F51			SN74F51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54F51			SN74F51			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V, I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V, V_I = 7 V			100			100	μA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V, V_I = 0 V		1.8	3		1.8	3	mA
I_{CCL}	V_{CC} = 5.5 V, V_I = 4.5 V		5.5	7.5		5.5	7.5	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F51			SN54F51		SN74F51		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	3.5	5.5	1.5	7.5	1.5	6.5	ns
t_{PHL}			1	2.5	4	1	5	1	4.5	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3178, AUGUST 1988—REVISED JANUARY 1989

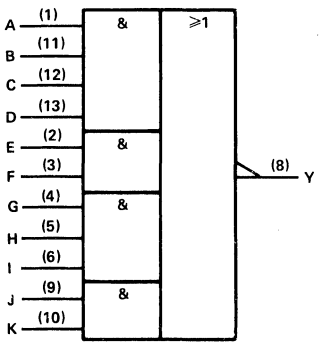
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain 4-2-3-2 input AND-OR-INVERT gates. They perform the Boolean function $Y = \overline{ABCD + EF + GHI + JK}$. The 'F64 has totem-pole outputs.

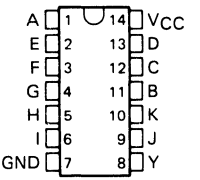
The SN54F64 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F64 is characterized for operation from 0°C to 70°C.

logic symbol†

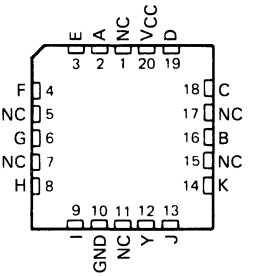


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F64 . . . J PACKAGE
SN74F64 . . . D OR N PACKAGE
(TOP VIEW)

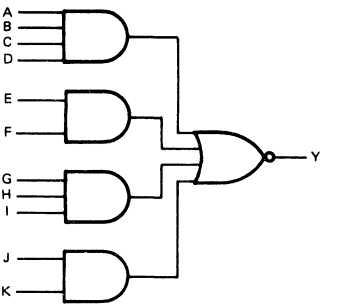


SN54F64 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (each device) (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F64 . . . . . −55°C to 125°C
SN74F64 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F64			SN74F64			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F64			SN74F64			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		1.9	2.8		1.9	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 1		3.1	4.7		3.1	4.7	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶			UNIT
			'F64			SN54F64		SN74F64	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.7	4.6	6	1.7	8.5	1.7	7	ns
t_{PHL}			1.2	3.2	4.5	1.2	6.5	1.2	5.5	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CCL} is measured with one input per gate at 4.5 V and all others grounded.
2. Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D inputs may be changed without affecting the levels at the outputs.

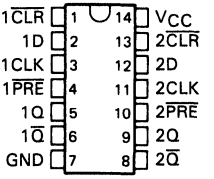
The SN54F74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F74 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

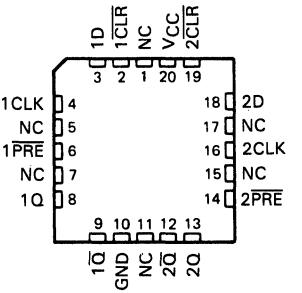
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F74 . . . J PACKAGE
SN74F74 . . . D OR N PACKAGE
(TOP VIEW)

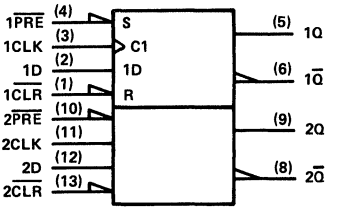


SN54F74 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F74 . . . . . −55°C to 125°C
SN74F74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F74			SN74F74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F74			SN74F74			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Data, CLK	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		10.5	16		10.5	16	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F74		SN54F74		SN74F74		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	80	0	100	MHz
t_{su}	Setup time before CLK ↑	Data high	2		3		2		ns
		Data low	3		4		3		
t_h	Hold time after CLK ↑	Data high	1		2		1		ns
		Data low	1		2		1		
t_w	Pulse duration	CLK high, $\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low	5		6		5		
t_{su}	Inactive-state setup time before CLK↑‡	$\overline{PRE}$ or CLR to CLK	2		3		2		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F74			SN54F74		SN74F74		
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	145		80		100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3	4.9	6.8	3	8.5	3	7.8	ns
t_{PHL}			3.6	5.8	8	3.6	10.5	3.6	9.2	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.4	4.2	6.1	2.4	8	2.4	7.1	ns
t_{PHL}			2.7	6.6	9	2.7	11.5	2.7	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ Inactive-state setup time is also referred to as "recovery time".
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and waveforms are shown in Section 1.

D3210, JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

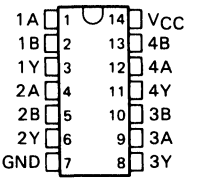
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54F86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F86 is characterized for operation from 0°C to 70°C.

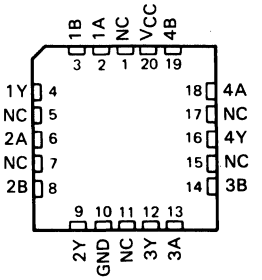
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54F86 . . . J PACKAGE
SN74F86 . . . D OR N PACKAGE
(TOP VIEW)

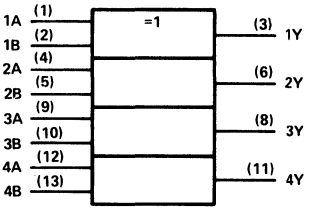


SN54F86 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F86 . . . . . −55°C to 125°C
SN74F86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F86			SN74F86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F86			SN74F86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		15	23		15	23	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		18	28		18	28	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶			UNIT
			'F86			SN54F86		SN74F86	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.2	3.6	5.5			2.2	6.5	ns
t_{PHL}	(other input low)		2.2	3.8	5.5			2.2	6.5	
t_{PLH}	A or B	Y	2.7	4.9	7			2.7	8	ns
t_{PHL}	(other input high)		2.2	4.3	6.5			2.2	7.5	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

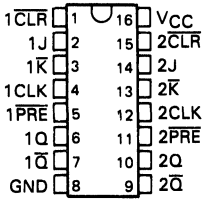
The SN54F109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F109 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

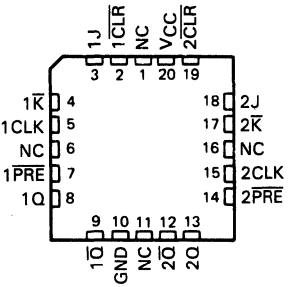
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F109 . . . J PACKAGE
SN74F109 . . . D OR N PACKAGE
(TOP VIEW)

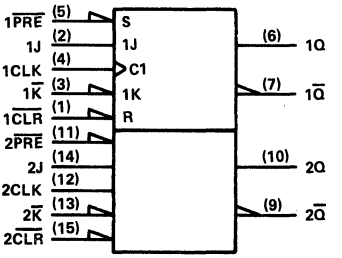


SN54F109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current† . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F109 . . . . . −55°C to 125°C
SN74F109 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54F109			SN74F109			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V, I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I		V_{CC} = 5.5 V, V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
I_{IL}	J, $\overline{K}$, CLK	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$				−1.8			−1.8	
I_{OS}§		V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1		11.7	17		11.7	17	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F109		SN54F109		SN74F109		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	70	0	90	MHz
t_{su}	Setup time before CLK ↑	Data high	3		3		3		ns
		Data low	3		3		3		
t_h	Hold time after CLK ↑	Data high	1		1		1		ns
		Data low	1		1		1		
t_w	Pulse duration	CLK high, $\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low	5		5		5		
t_{su}	Inactive-state setup time before CLK↑	$\overline{PRE}$ or CLR to CLK	2		2		2		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F109			SN54F109		SN74F109		
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	150		70		90		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3	4.9	7	3	9	3	8	ns
t_{PHL}			3.6	5.8	8	3.6	10.5	3.6	9.2	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.4	4.8	7	2.4	9	2.4	8	ns
t_{PHL}			2.7	6.6	9	2.7	11.5	2.7	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

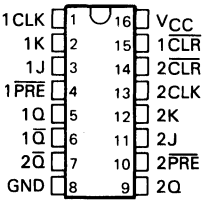
The SN54F112 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F112 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

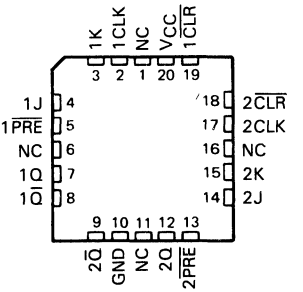
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F112 . . . J PACKAGE
SN74F112 . . . D OR N PACKAGE
(TOP VIEW)

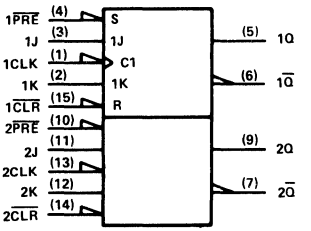


SN54F112 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordancea with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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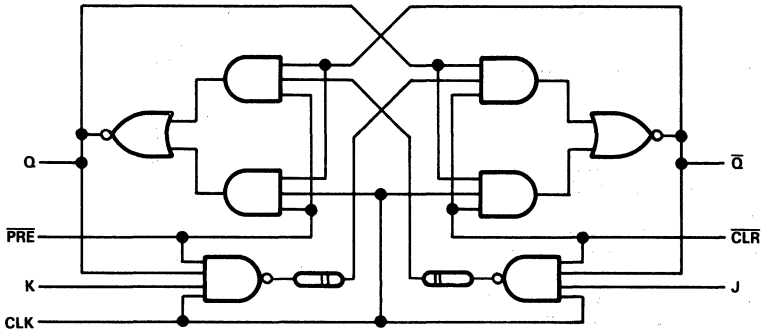
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F112 . . . . . −55°C to 125°C
SN74F112 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F112			SN74F112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F112			SN74F112			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$					−3			−3	
	CLK					−2.4			−2.4	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§			UNIT
			'F112	SN54F112		SN74F112	
			MIN MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0 110			0	100	MHz
t_{su}	Setup time before CLK↓	Data high	4			5		ns
		Data low	3			3.5		
t_h	Hold time after CLK↓	Data high	0			0		ns
		Data low	0			0		
t_w	Pulse duration	CLK high or low	4.5			5		ns
		$\overline{CLR}$ or $\overline{PRE}$ low	4.5			5		
t_{su}	Inactive-state setup time before CLK↓¶	$\overline{PRE}$ or $\overline{CLR}$ high	4			5		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F112			SN54F112		SN74F112		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}			110	130				100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	1.2	4.6	6.5			1.2	7.5	ns
t_{PHL}			1.2	4.6	6.5			1.2	7.5	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.2	4.1	6.5			1.2	7.5	ns
t_{PHL}			1.2	4.1	6.5			1.2	7.5	

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
¶ Inactive-state setup time is also referred to as "recovery time".
NOTES: 1. I_{CC} is measured with all outputs open, the Q and $\overline{Q}$ outputs alternately high and the clock input grounded at the time of measurement.
2. Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

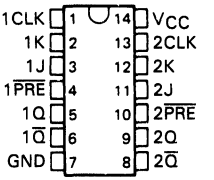
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54F113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F113 is characterized for operation from 0°C to 70°C.

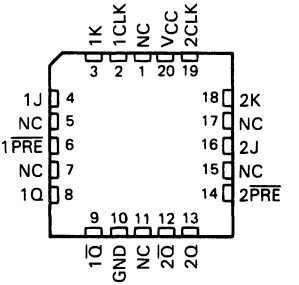
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

SN54F113 . . . J PACKAGE
SN74F113 . . . D OR N PACKAGE
(TOP VIEW)

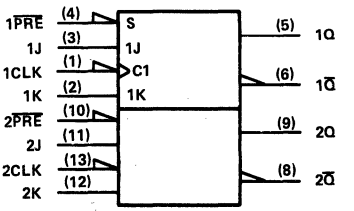


SN54F113 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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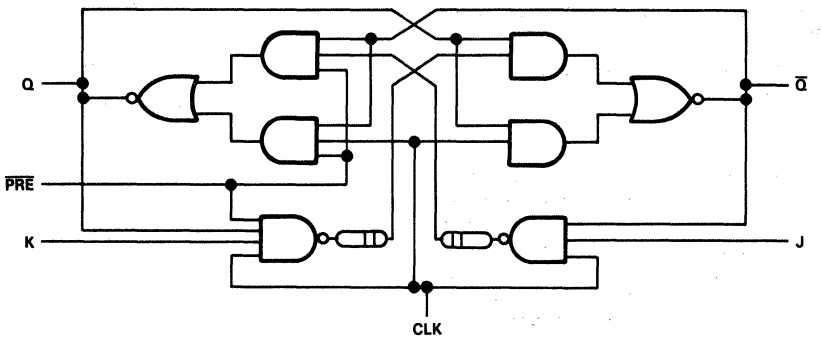
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F113 . . . . . −55°C to 125°C
SN74F113 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F113			SN74F113			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54F113			SN74F113			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V, I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V, V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V			20			20	μA
I_{IL}	J or K	V_{CC} = 5.5 V, V_I = 0.5 V			−0.6			−0.6	mA
	$\overline{PRE}$				−3			−3	
	CLK				−2.4			−2.4	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1		12	19		12	19	mA

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			'F113	SN54F113	SN74F113	
			MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency		0 110		0 100	MHz
t_{su}	Setup time before CLK↓	Data high	4		5	ns
		Data low	3		3.5	
t_h	Hold time after CLK↓	Data high or low	0		0	ns
t_w	Pulse duration	CLK high or low	4.5		5	ns
		$\overline{PRE}$ low	4.5		5	
t_{su}	Inactive-state setup time¶ before CLK↓	$\overline{PRE}$ high	4		5	ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F113			SN54F113		SN74F113	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			110	125				100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	1.2	3.6	6			1.2	7	ns
t_{PHL}			1.2	3.6	6			1.2	7	
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$	1.2	4.1	6.5			1.2	7.5	ns
t_{PHL}			1.2	4.1	6.5			1.2	7.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all outputs open with the Q and $\overline{Q}$ outputs alternately at high level; at the time of measurement, the clock input is grounded.
2. Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

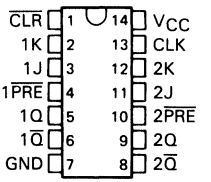
The SN54F114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F114 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

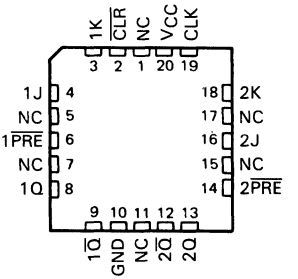
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F114 . . . J PACKAGE
SN74F114 . . . D OR N PACKAGE
(TOP VIEW)

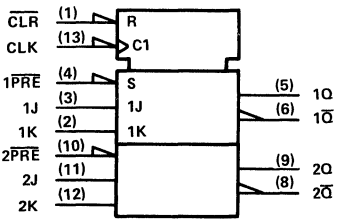


SN54F114 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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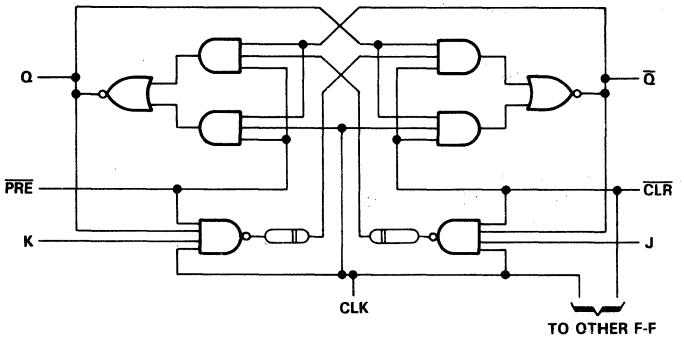
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F114 . . . . . −55°C to 125°C
SN74F114 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F114			SN74F114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F114			SN74F114			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$					−3			−3	
	CLK					−2.4			−2.4	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA

PRODUCT PREVIEW

timing requirements

			V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'F114	SN54F114		SN74F114		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100			0	90	MHz
t_{su}	Setup time before CLK↓	Data high	4				5		ns
		Data low	3				3.5		
t_h	Hold time after CLK↓	Data high or low	0				0		ns
t_w	Pulse duration	CLK high or low	4.5				5		ns
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5				5		ns
t_{rec}	Recovery time	$\overline{PRE}$ or $\overline{CLR}$ to CLK	4				5		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F114			SN54F114		SN74F114		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125				90		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	2.2	4.6	6.5			2.2	7.5	ns
t_{PHL}			2.2	5.1	7.5			2.2	8.5	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.2	4.1	6.5			2.2	7.5	ns
t_{PHL}			2.2	4.1	6.5			2.2	7.5	

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTES: 1. I_{CC} is measured with all outputs open, the Q and $\overline{Q}$ outputs alternately at high level and at the time of measurement, the clock is grounded.
2. Load circuits and waveforms are shown in Section 1.

D3211, JANUARY 1989

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

This bus buffer features independent line drivers with three-state outputs. Each output is disabled when the associated $\overline{G}$ is high.

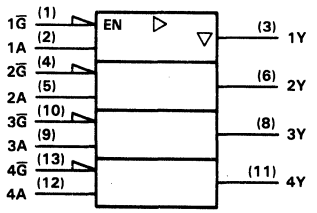
The SN54F125 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F125 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

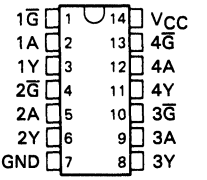
H = high level
L = low level
X = irrelevant

logic symbol†

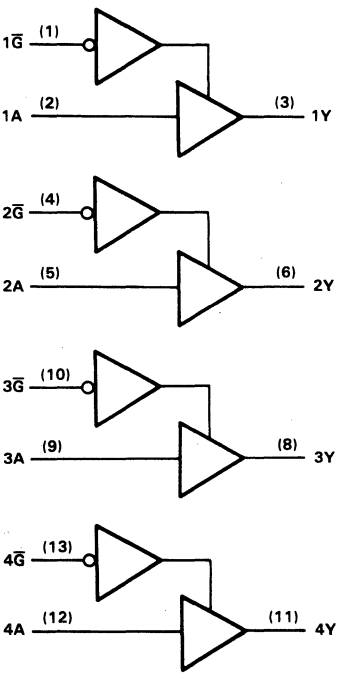


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54F125 . . . J PACKAGE
SN74F125 . . . D OR N PACKAGE
(TOP VIEW)



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F125 . . . . . 96 mA
SN74F125 . . . . . 128 mA
Operating free-air temperature range: SN54F125 . . . . . −55°C to 125°C
SN74F125 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54F125			SN74F125			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−15			−15	mA
I_{OL}	Low-level output current			64			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F125			SN74F125			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
	V_{CC} = 4.75 V	I_{OH} = −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.35	0.5				V
		I_{OL} = 64 mA					0.40	0.55	
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−20			−20	μA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		17	24		17	24	mA
I_{CCL}				28	40		28	40	
I_{CCZ}				25	35		25	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F125			SN54F125		SN74F125		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	3.6	6			1.2	6.5	ns
t_{PHL}			2.2	5.1	7.5			2.2	8	
t_{PZH}	$\overline{G}$	Y	2.7	5.1	7.5			2.7	8.5	ns
t_{PZL}			3.2	5.6	8			3.2	9	
t_{PHZ}	$\overline{G}$	Y	1	3.1	5			1	6	ns
t_{PLZ}			1	3.1	5.5			1	6	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D3212 JANUARY 1989

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

This bus buffer features independent line drivers with three-state outputs. Each output is disabled when the associated G is low.

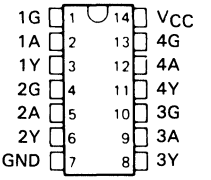
The SN54F126 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F126 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each buffer)

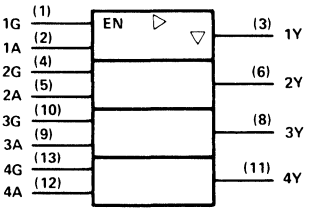
INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

H = high level
L = low level
X = irrelevant

SN54F126 . . . J PACKAGE
SN74F126 . . . D OR N PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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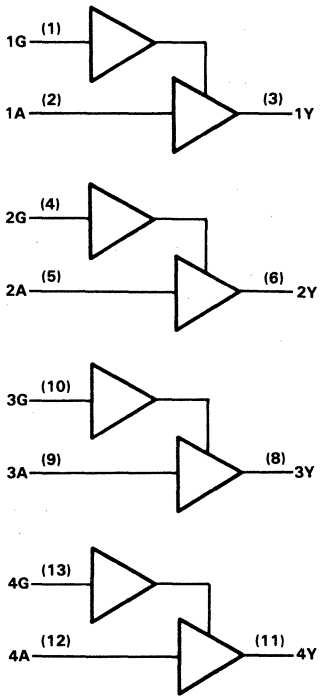
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage	−1.2 V to 7 V
Input current	−30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state: SN54F126	96 mA
SN74F126	128 mA
Operating free-air temperature range: SN54F126	−55°C to 125°C
SN74F126	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

		SN54F126			SN74F126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−15			−15	mA
I_{OL}	Low-level output current			64			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F126			SN74F126			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.35	0.5				V
		I_{OL} = 64 mA					0.4	0.55	
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−20			−20	μA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		20	30		20	30	mA
I_{CCL}				32	48		32	48	
I_{CCZ}				26	39		26	39	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F126			SN54F126		SN74F126	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.6	6.5			1.2	7	ns
t_{PHL}			2.2	5.1	8			2.2	8.5	
t_{PZH}	G	Y	3.2	5.6	7.5			2.7	8.5	ns
t_{PZL}			3.2	5.6	8			2.7	8.5	
t_{PHZ}	G	Y	1.2	4.1	6.5			1.2	7.5	ns
t_{PLZ}			2.2	5.1	7.5			2.2	8	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditons.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

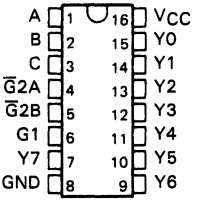
description

The SN54F138 and SN74F138 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced is negligible.

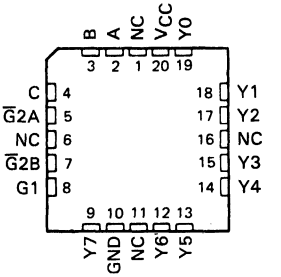
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54F138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F138 is characterized for operation 0°C to 70°C.

SN54F138 . . . J PACKAGE
SN74F138 . . . D OR N PACKAGE
(TOP VIEW)



SN54F138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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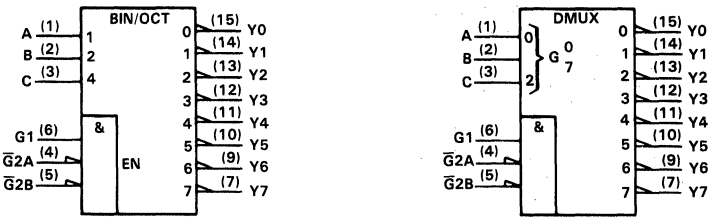
FUNCTION TABLE

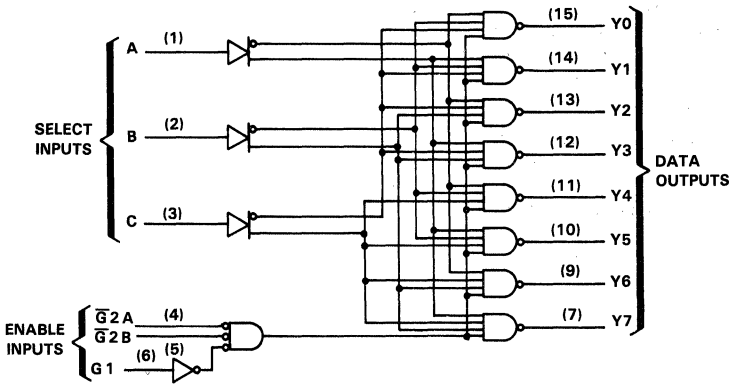
ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F138 . . . . . −55°C to 125°C
SN74F138 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F138			SN74F138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F138			SN74F138			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	μA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		13	20		13	20	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with outputs enabled and open.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F138			SN54F138		SN74F138		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	2.7	5.2	7.5	2.7	12	2.7	8.5	ns
t_{PHL}			3.2	5.7	8	3.2	9.5	3.2	9	
t_{PLH}	$\overline{G}$2A or $\overline{G}$2B	Y	2.7	5	7	2.7	11	2.7	8	ns
t_{PHL}			2.2	4.9	7	2.2	8	2.2	7.5	
t_{PLH}	G1	Y	3.2	5.8	8	3.2	12.5	3.2	9	ns
t_{PHL}			2.7	5.2	7.5	2.7	8.5	2.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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- **8-Line to 1-Line Multiplexers can Perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality Reliability**

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

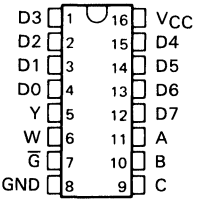
The SN54F151A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F151A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

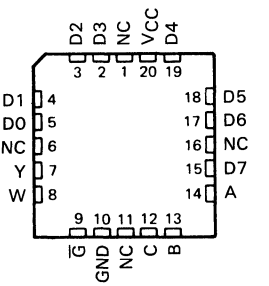
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level,
X = irrelevant
D0,D1 . . . D7 = the level of the respective input

SN54F151A . . . J PACKAGE
SN74F151A . . . D OR N PACKAGE
(TOP VIEW)

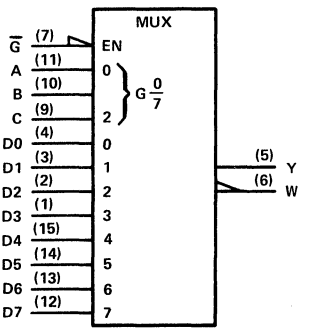


SN54F151A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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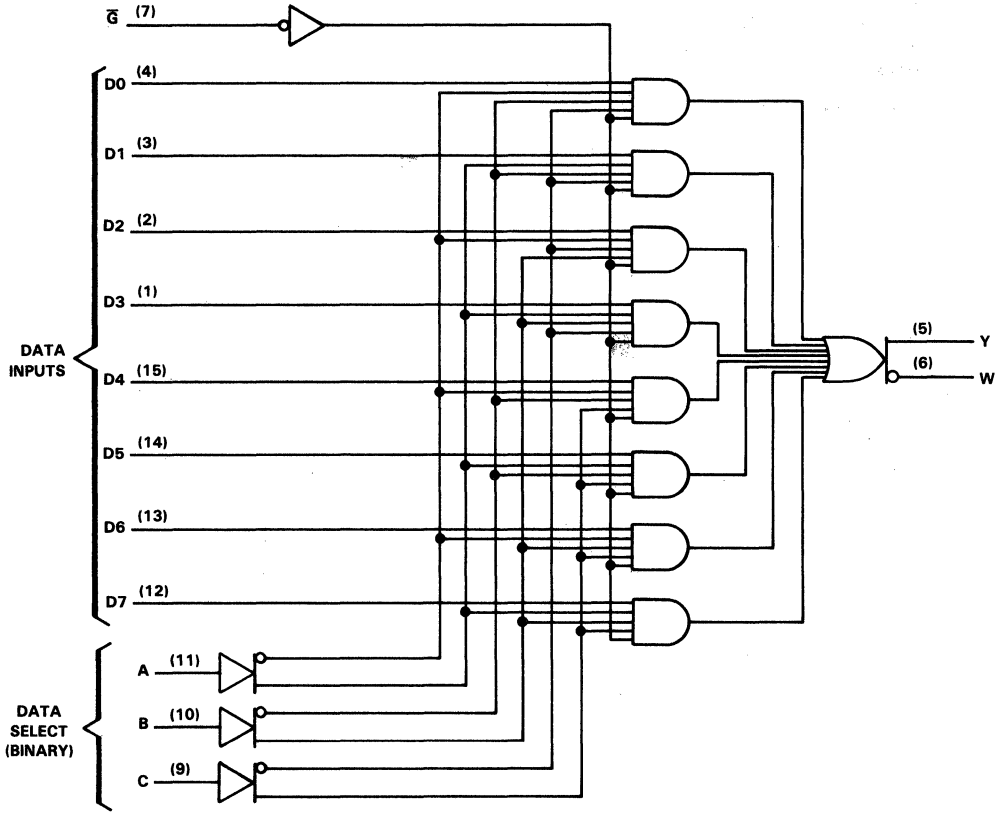
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F151A . . . . . −55°C to 125°C
SN74F151A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F151A			SN74F151A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F151A			SN74F151A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 4.5 V		13.5	21		13.5	21	mA

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F151A			SN54F151A		SN74F151A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	W	3.2	5.8	9	2.7	11.5	2.7	9.5	ns
t_{PHL}			2.4	4.8	7.5	2.2	8	2.4	7.5	
t_{PLH}	A, B, or C	Y	3.7	7.1	10.5	3.7	13.5	3.7	12	ns
t_{PHL}			3.2	5.8	9	3.2	9.5	3.2	9	
t_{PLH}	$\overline{G}$	W	2.2	4.3	6.1	2.2	7.5	2.2	7	ns
t_{PHL}			2.2	4	6	1.7	6.5	1.7	6	
t_{PLH}	$\overline{G}$	Y	4.2	6.6	9.5	3.2	12	3.2	10.5	ns
t_{PHL}			2.7	4.9	7	2.2	8	2.2	7.5	
t_{PLH}	D	W	2.2	4.4	6.5	1.7	7.5	2.2	7	ns
t_{PHL}			1	2.1	4	1	6	1	5	
t_{PLH}	D	Y	2.2	4.4	6.5	1.7	8.5	1.7	7.5	ns
t_{PHL}			2.9	5.1	7	2.7	9	2.9	7.5	

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: See General Information for load circuits and waveforms.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

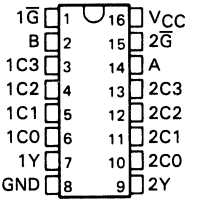
The SN54F153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F153 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

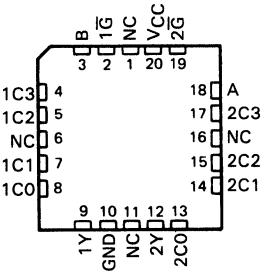
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

SN54F153 . . . J PACKAGE
SN74F153 . . . D OR N PACKAGE
(TOP VIEW)

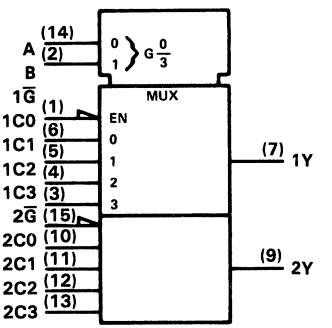


SN54F153 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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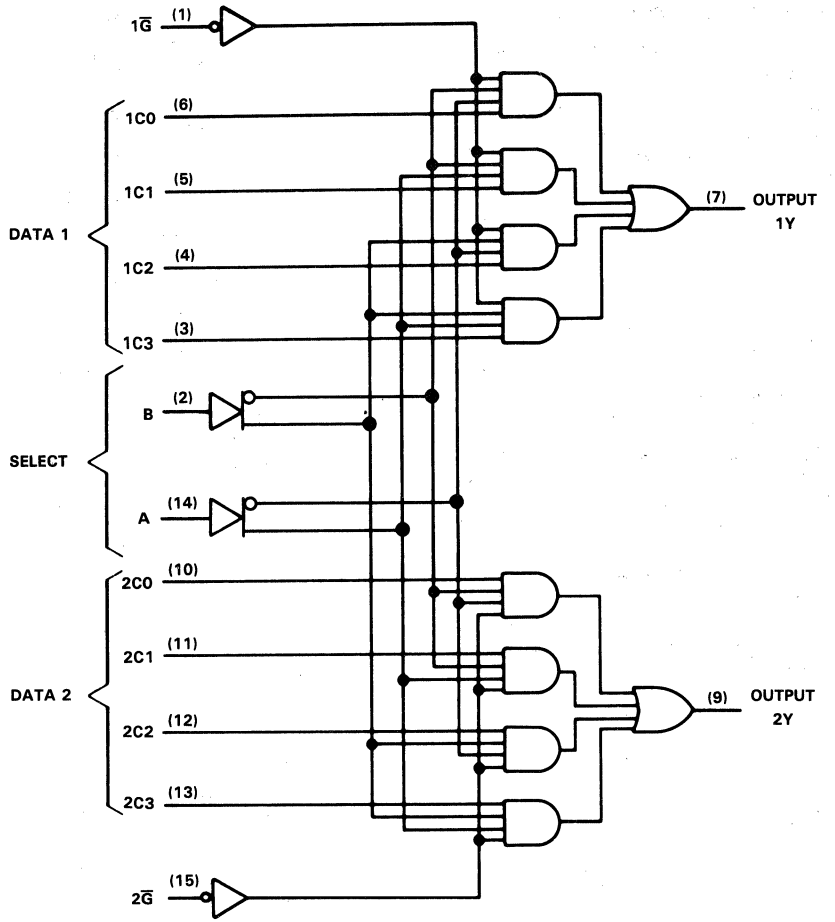
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F153 . . . . . −55°C to 125°C
SN74F153 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F153			SN74F153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54F153			SN74F153			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 0		12	20		12	20	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F153			SN54F153		SN74F153		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3.7	7.7	10.5	3.7	14	3.7	12	ns
t_{PHL}			2.7	6.6	9	2.7	11	2.7	10.5	
t_{PLH}	$\overline{G}$	Y	3.7	6.7	9	3.7	11.5	3.7	10.5	ns
t_{PHL}			2.2	5.3	7	1.7	9	1.7	8	
t_{PLH}	C	Y	2.2	4.9	7	1.7	9	2.2	8	ns
t_{PHL}			2.2	4.7	6.5	1.7	8	1.7	7.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

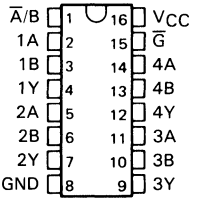
The 'F157A is a quadruple 2-input multiplexer/data selector featuring a common strobe input ($\overline{G}$). When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The 'F157A presents true data.

The SN54F157A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F157A is characterized for operation from 0°C to 70°C.

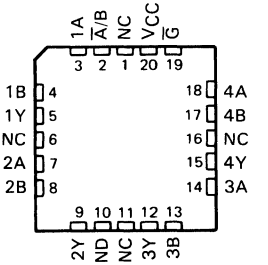
FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54F157A . . . J PACKAGE
SN74F157A . . . D OR N PACKAGE
(TOP VIEW)

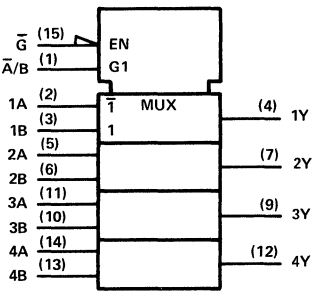


SN54F157A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

2 Data Sheets

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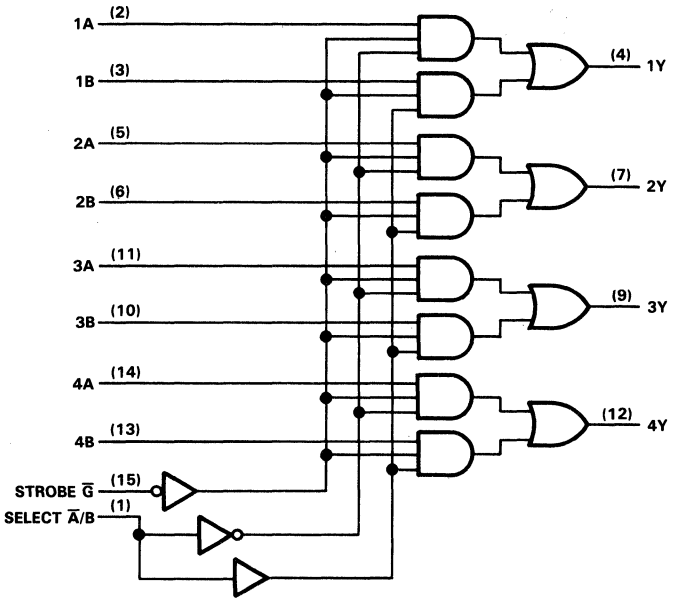
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F157A . . . . . −55°C to 125°C
SN74F157A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F157A			SN74F157A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F157A			SN74F157A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 4.5 V		15	23		15.5	23	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F157A			SN54F157A		SN74F157A	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{A}$/B	Y	3.2	6.6	10	3.2	12	3.2	11	ns
t_{PHL}			2.2	4.6	7	2.2	9	2.2	8	
t_{PLH}	$\overline{G}$	Y	4.2	6.6	9.5	4.2	13	4.2	11	ns
t_{PHL}			1.7	4.1	6.5	1.7	7.5	1.7	7	
t_{PLH}	A or B	Y	1.7	4.1	6	1.7	7.5	1.7	6.5	ns
t_{PHL}			1.7	3.6	5.5	1	7.5	1.2	7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

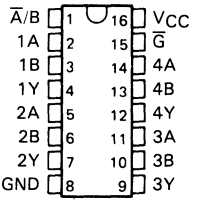
The SN54F158A and SN74F158A are quadruple 2-input multiplexer/data selectors each featuring a direct strobe input ($\overline{G}$). When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The data presented is inverted.

The SN54F158A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F158A is characterized for operation from 0°C to 70° C.

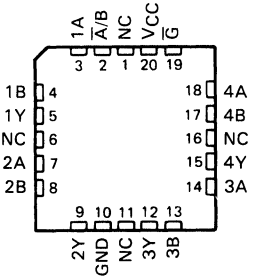
FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	DATA		
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54F158A . . . J PACKAGE
SN74F158A . . . D OR N PACKAGE
(TOP VIEW)

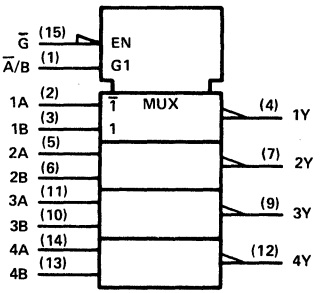


SN54F158A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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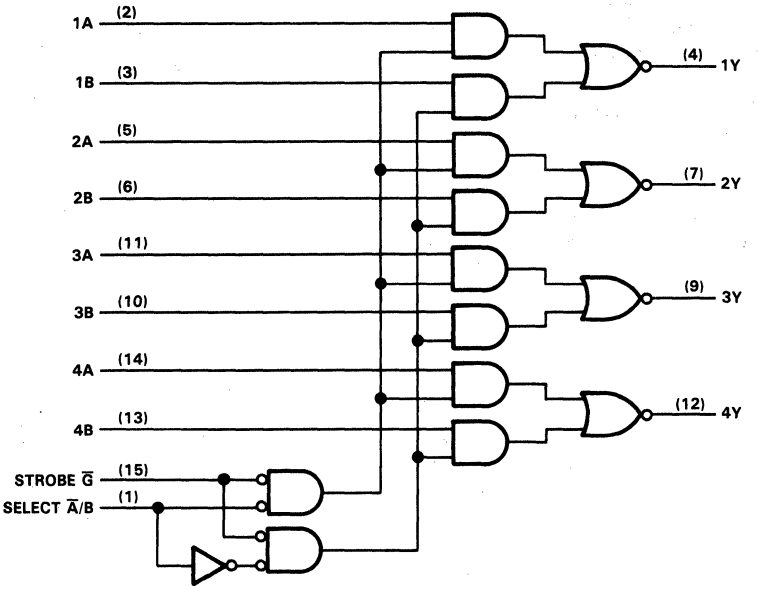
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F158A . . . . . −55°C to 125°C
SN74F158A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F158A			SN74F158A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54F158A			SN74F158A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 4.5 V		10	15		10	15	mA

switching characteristics (see Note 1)

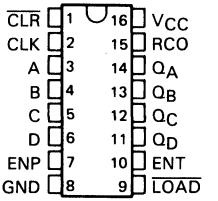
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F158A			SN54F158A		SN74F158A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{A}$/B	Y	2.2	5.1	8.5	2.2	10.5	2.2	9.5	ns
t_{PHL}			1.7	4.1	6.5	1.7	8	1.7	7	
t_{PLH}	$\overline{G}$	Y	1.7	4.1	6	1.7	8	1.7	7	ns
t_{PHL}			1.2	3.6	6	1.2	7	1.2	6.5	
t_{PLH}	A or B	Y	1.7	3.6	5.9	1.7	8.5	1.7	7	ns
t_{PHL}			1	2.1	4	1	5	1	4.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: Load circuits and waveforms are shown in Section 1.

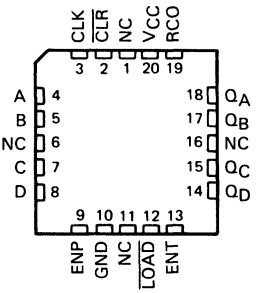
D2932, MARCH 1987—REVISED JANUARY 1989

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F160A, SN54F162A . . . J PACKAGE
SN74F160A, SN74F162A . . . D OR N PACKAGE
(TOP VIEW)



SN54F160A, SN54F162A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable decade counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters; however, counting spikes may occur on the ripple carry output (RCO). A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

The counters are fully programmable; that is, they may be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

If one of these decade counters is preset to a number between 10 and 15 or assumes such an invalid state when power is applied, it will progress to the normal sequence within two counts as shown in the State Diagram.

The clear function for the 'F160A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'F162A is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output (RCO). RCO thus enabled will produce a high-level pulse while the count is 9 (HLLH). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

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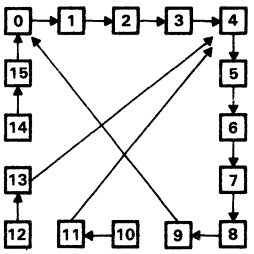
description (continued)

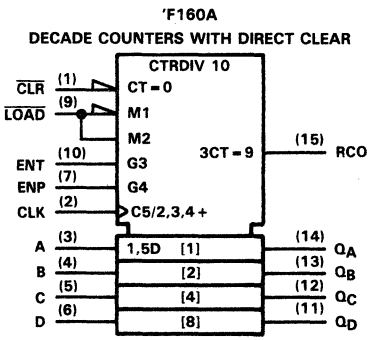
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

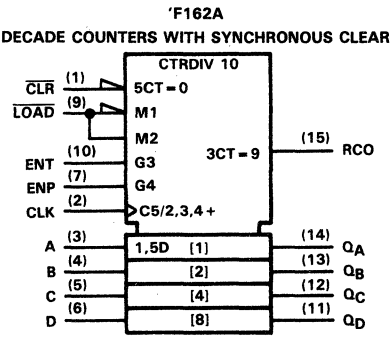
The SN54F160A and SN54F162A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F160A and SN74F162A are characterized for operation from 0°C to 70°C.

state diagram



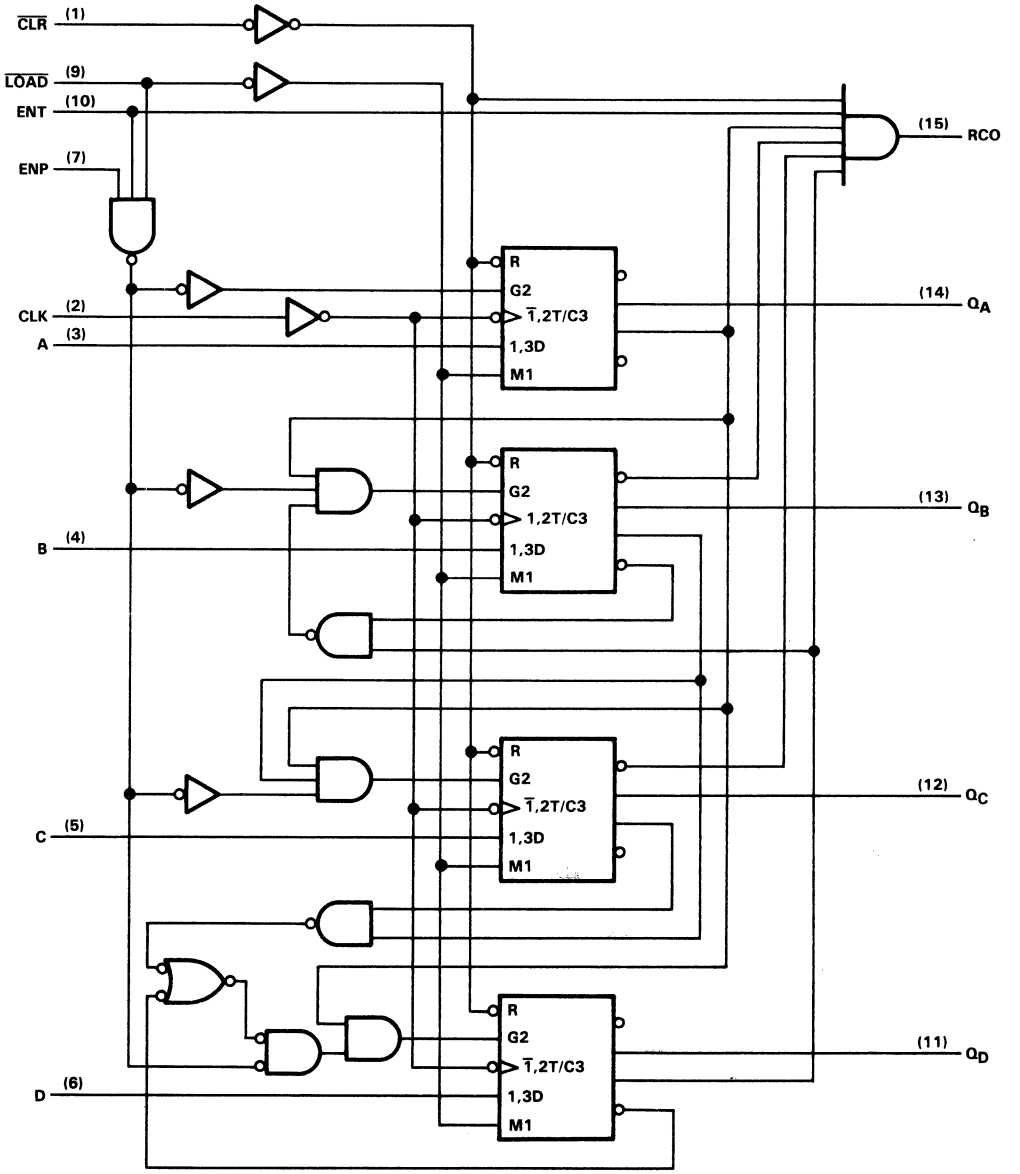
logic symbols†



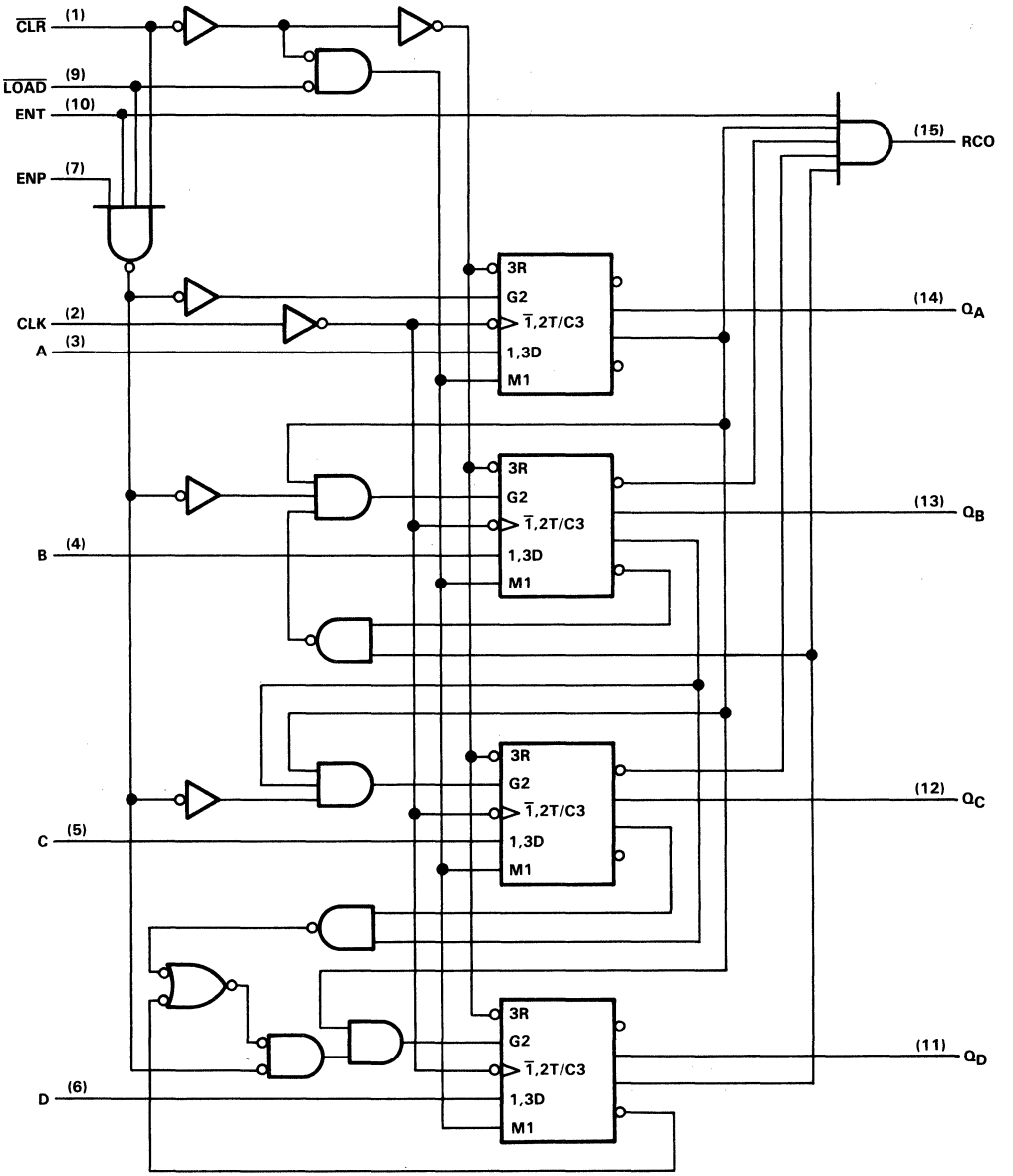


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'F160A logic diagram (positive logic)



'F162A logic diagram (positive logic)



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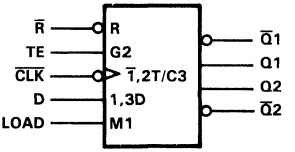
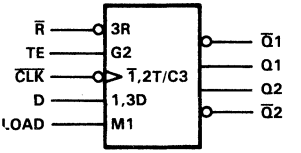
logic symbol, each flip-flop (positive logic)

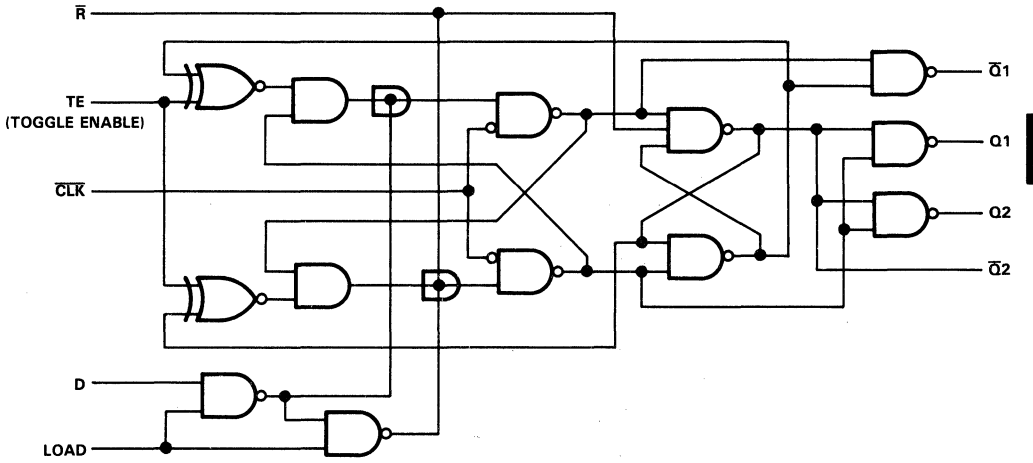
IN 'F160A
WITH DIRECT CLEAR



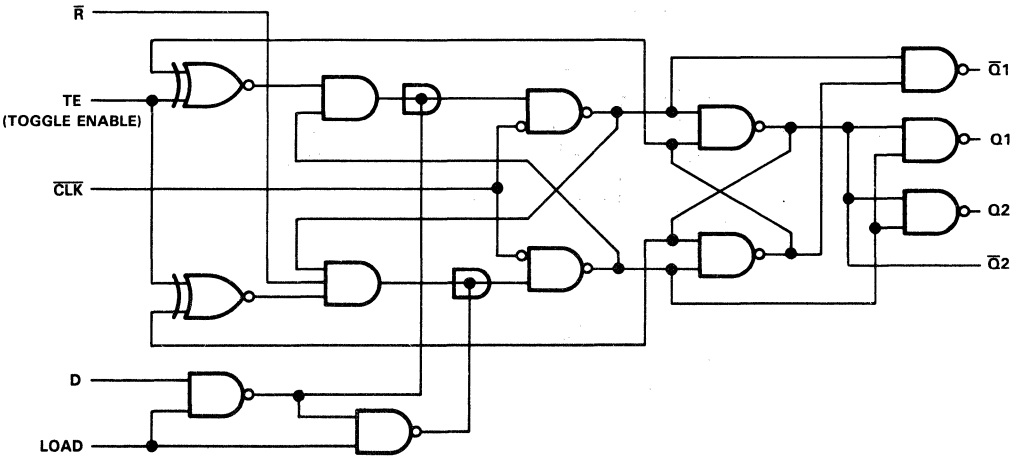
IN 'F162A
WITH SYNCHRONOUS CLEAR



logic diagram, each flip-flop in 'F160A (positive logic)



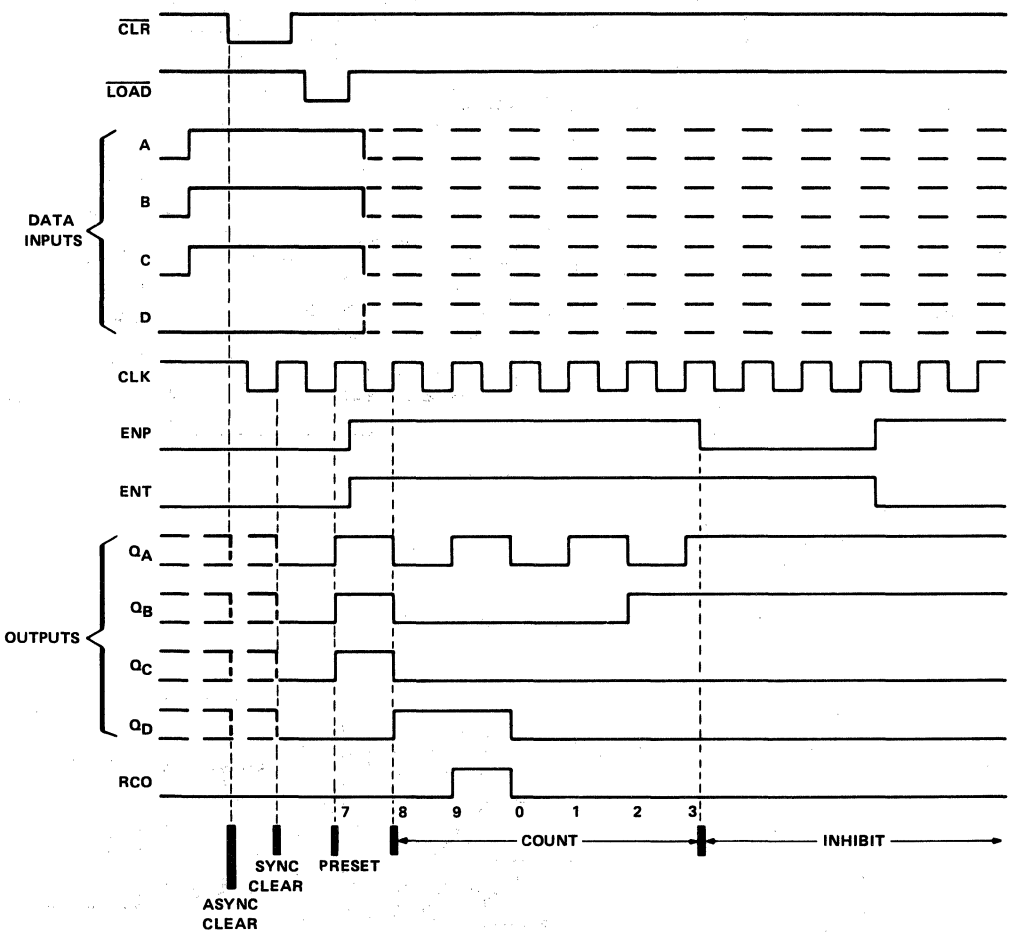
logic diagram, each flip-flop in 'F162A (positive logic)



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('F160A is asynchronous; 'F162A is synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F160A, SN54F162A . . . . . −55°C to 125°C
SN74F160A, SN74F162A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F160A SN54F162A			SN74F160A SN74F162A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level outut current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F160A SN54F162A			SN74F160A SN74F162A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	ENP, CLK, A, B, C, D	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	ENT, $\overline{LOAD}$					−1.2			−1.2	
	$\overline{CLR}$ ('F160A)					−0.6			−0.6	
	$\overline{CLR}$ ('F162A)					−1.2			−1.2	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V			37	55		37	55	mA

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F160A, 'F162A			SN54F160A SN54F162A		SN74F160A SN74F162A		
			MIN		MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		100			0	90	MHz
t_{su}	Setup time, data (A, B, C, D) high or low before CLK↑		5					5		ns
t_{hold}	Hold time, data (A, B, C, D) high or low after CLK↑		2					2		ns
t_{su}	Setup time, $\overline{LOAD}$ and (for 'F162A) $\overline{CLR}$ before CLK↑	High	11					11.5		ns
		Low	8.5					9.5		
t_{hold}	Hold time, $\overline{LOAD}$ and (for 'F162A) $\overline{CLR}$ after CLK↑	High	2					2		ns
		Low	0					0		
t_{su}	Setup time, ENP and ENT before CLK↑	High	11					11.5		ns
		Low	5					5		
t_{hold}	Hold time, ENP and ENT high or low after CLK↑		0					0		ns
t_w	Pulse duration, CLK high or low (loading)		5					5		ns
t_w	Pulse duration, CLK (counting)	High	4					4		ns
		Low	6					7		
t_w	Pulse duration, $\overline{CLR}$ low ('F160A)		5					5		ns
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑ ('F160A)‡		6					6		ns

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F160A, 'F162A			SN54F160A SN54F162A		SN74F160A SN74F162A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	120				90		MHz
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	2.7	5.1	7.5			2.7	8.5	ns
t_{PHL}			2.7	7.1	10			2.7	11	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	3.2	5.6	8.5			3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5			3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14			4.2	15	ns
t_{PHL}			4.2	9.6	14			4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5			1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5			1.7	8.5	
t_{PHL}	$\overline{CLR}$ ('F160A)	Any Q	4.7	8.6	12			4.7	13	ns
t_{PHL}	$\overline{CLR}$ ('F160A)	RCO	3.7	7.6	10.5			3.7	11.5	ns

PRODUCT PREVIEW

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ Inactive-state setup time is also referred to as "recovery time".
NOTE 1: Load circuits and waveforms are shown in Section 1.

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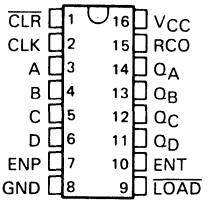
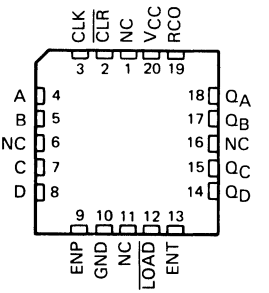
D2932, MARCH 1987—REVISED JANUARY 1989

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F161A, SN54F163A . . . J PACKAGE
SN74F161A, SN74F163A . . . D OR N PACKAGE
(TOP VIEW)



SN54F161A, SN54F163A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable 4-bit binary counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters; however, counting spikes may occur on the ripple carry output (RCO). A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

The counters are fully programmable; that is, they may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'F161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'F163A is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output (RCO). RCO thus enabled will produce a high-level pulse while the count is 15 (HHHH). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

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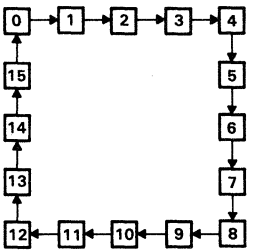
description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

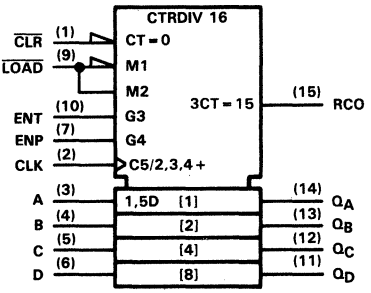
The SN54F161A and SN54F163A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F161A and SN74F163A are characterized for operation from 0°C to 70°C.

state diagram

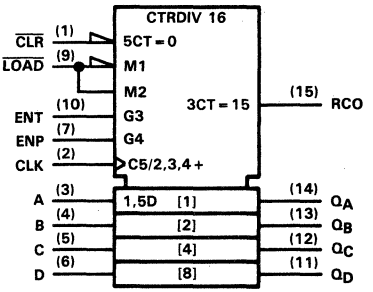


logic symbols†

'F161A
BINARY COUNTERS WITH DIRECT CLEAR

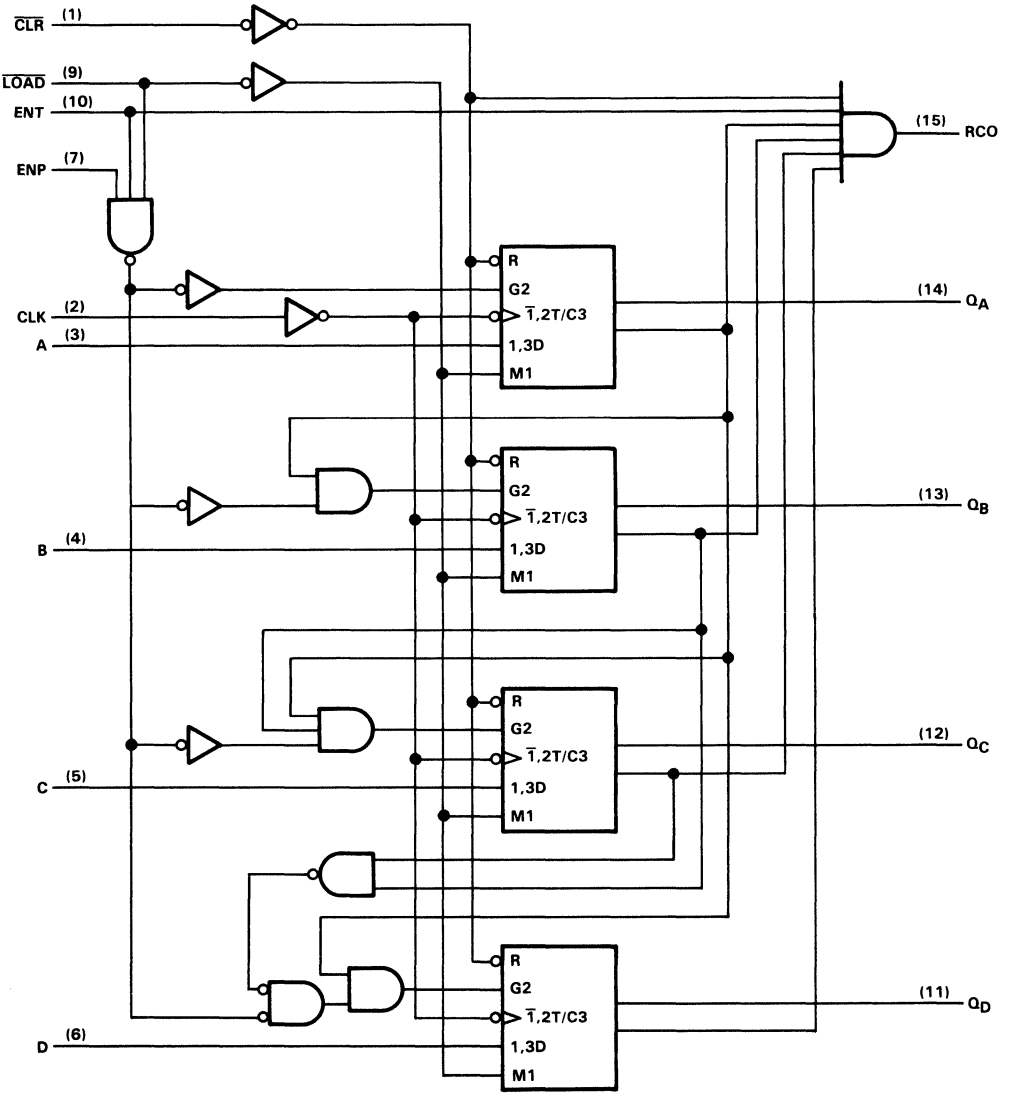


'F163A
BINARY COUNTERS WITH SYNCHRONOUS CLEAR

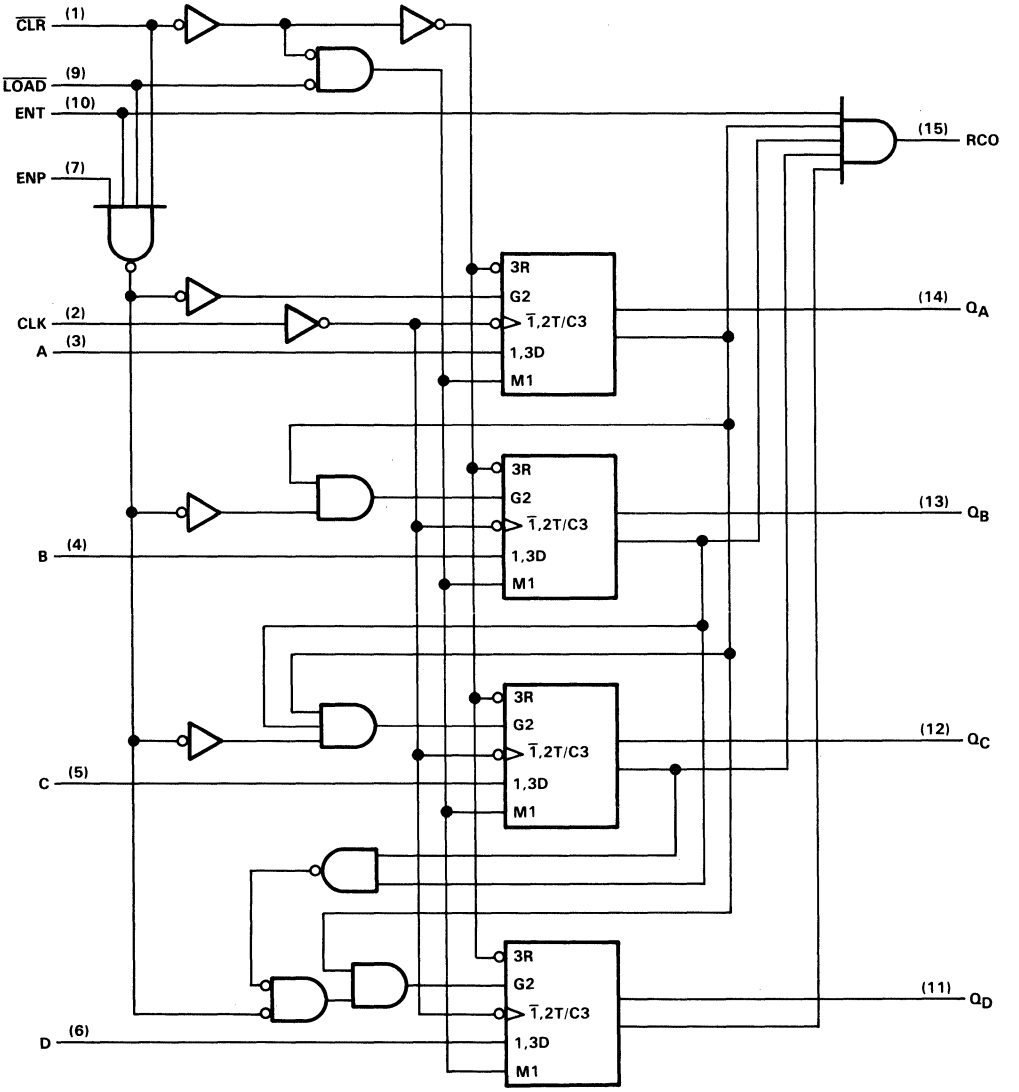


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'F161A logic diagram (positive logic)

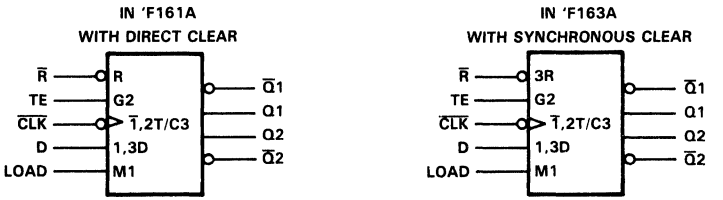


'F163A logic diagram (positive logic)

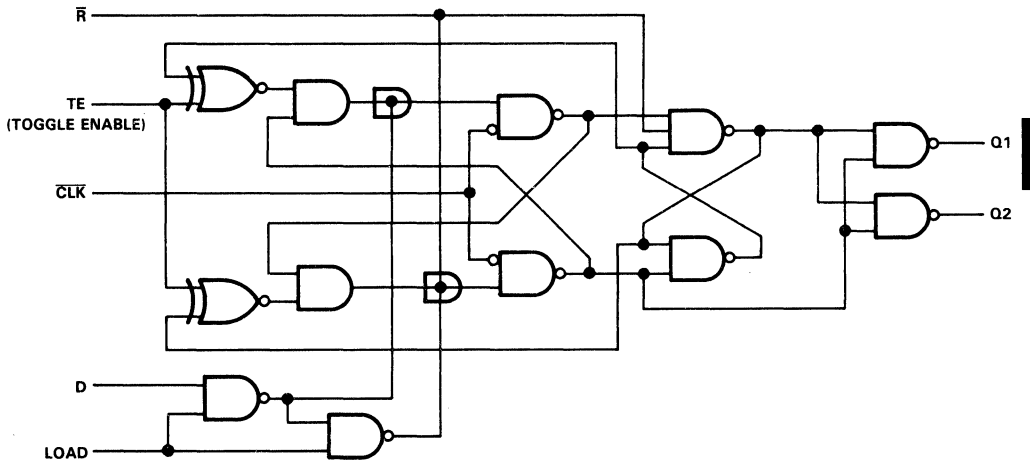


TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

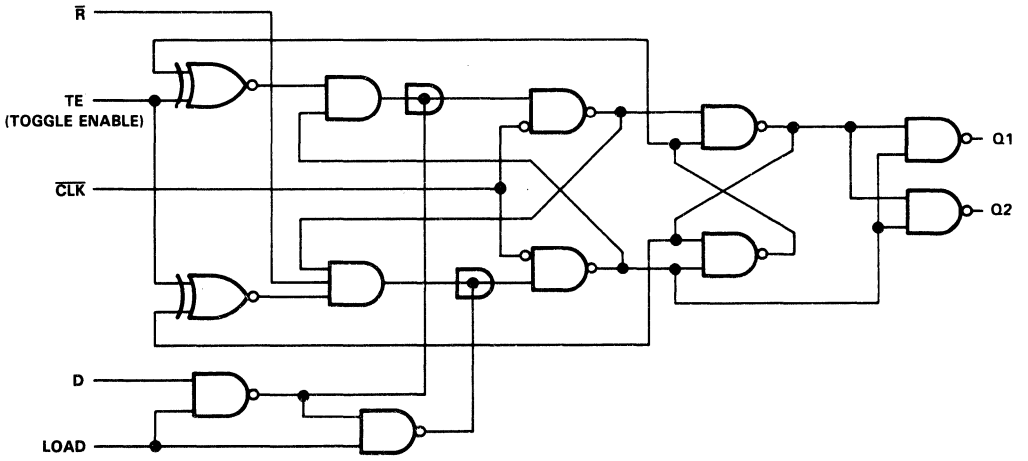
logic symbol, each flip-flop (positive logic)



logic diagram, each flip-flop in 'F161A (positive logic)



logic diagram, each flip-flop in 'F163A (positive logic)

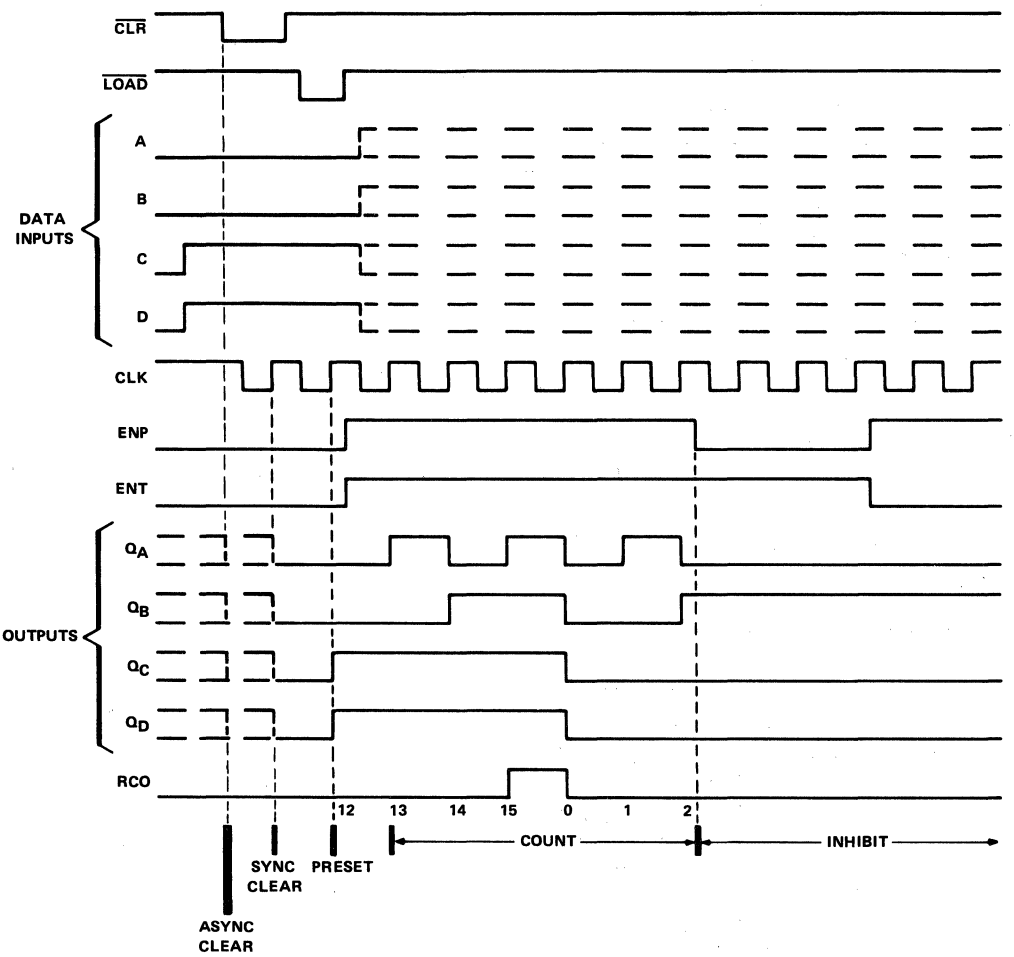


2 Data Sheets

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('F161A is asynchronous; 'F163A is synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one and two
4. Inhibit



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage[†] . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F161A, SN54F163A . . . . . −55°C to 125°C
SN74F161A, SN74F163A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

[†]The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F161A SN54F163A			SN74F161A SN74F163A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level outut current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F161A SN54F163A			SN74F161A SN74F163A			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	ENP, CLK, A, B, C, D	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	ENT, $\overline{LOAD}$					−1.2			−1.2	
	$\overline{CLR}$ ('F161A)					−0.6			−0.6	
	$\overline{CLR}$ ('F163A)					−1.2			−1.2	
I_{OS}[§]		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V			37	55		37	55	mA

PRODUCT PREVIEW

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F161A, 'F163A			SN54F161A SN54F163A		SN74F161A SN74F163A		
			MIN		MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		100	0	75	0	90	MHz
t_{su}	Setup time, data (A, B, C, D) high or low before CLK↑		5			5.5		5		ns
t_{hold}	Hold time, data (A, B, C, D) high or low after CLK↑		2			2.5		2		ns
t_{su}	Setup time, $\overline{LOAD}$ and (for 'F163A) $\overline{CLR}$ before CLK↑	High	11			13.5		11.5		ns
		Low	8.5			10.5		9.5		
t_{hold}	Hold time, $\overline{LOAD}$ and (for 'F163A) $\overline{CLR}$ after CLK↑	High	2			2		2		ns
		Low	0			0		0		
t_{su}	Setup time, ENP and ENT before CLK↑	High	11			13		11.5		ns
		Low	5			6		5		
t_{hold}	Hold time, ENP and ENT high or low after CLK↑		0			0		0		ns
t_w	Pulse duration, CLK high or low (loading)		5			5		5		ns
t_w	Pulse duration, CLK (counting)	High	4			5		4		ns
		Low	6			8		7		
t_w	Pulse duration, $\overline{CLR}$ low ('F161A)		5			5		5		ns
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑ ('F161A)‡		6			6		6		ns

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F161A, 'F163A			SN54F161A SN54F163A		SN74F161A SN74F163A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	120		75		90		MHz
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	2.7	5.1	7.5	2.7	9	2.7	8.5	ns
t_{PHL}			2.7	7.1	10	2.7	11.5	2.7	11	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	3.2	5.6	8.5	3.2	10	3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5	3.2	10	3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14	4.2	16.5	4.2	15	ns
t_{PHL}			4.2	9.6	14	4.2	15	4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5	1.7	9	1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5	1.7	9	1.7	8.5	
t_{PHL}	$\overline{CLR}$ ('F161A)	Any Q	4.7	8.6	12	4.7	14	4.7	13	ns
t_{PHL}	$\overline{CLR}$ ('F161A)	RCO	3.7	7.6	10.5	3.7	12.5	3.7	11.5	ns

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† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ Inactive-state setup time is also referred to as "recovery time".
NOTE 1: Load circuits and waveforms are shown in Section 1.

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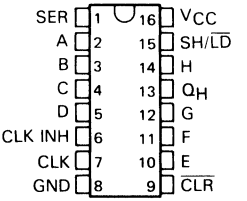
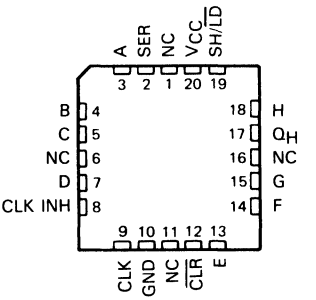
D3213, JANUARY 1989

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F166 . . . J PACKAGE
SN74F166 . . . D OR N PACKAGE
(TOP VIEW)



SN54F166 . . . FK PACKAGE
(TOP VIEW)



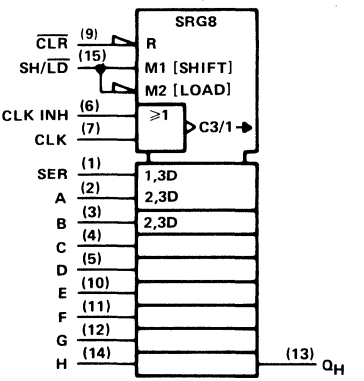
NC—No internal connection

description

The 'F166 parallel-in or serial-in, serial-out registers feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input overrides all other inputs, including the clock, and resets all flip-flops to zero.

The SN54F166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F166 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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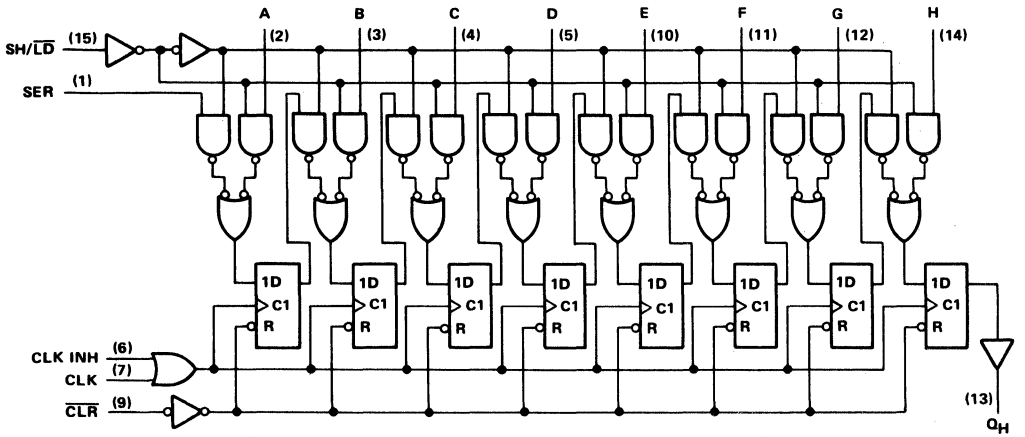
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLR	SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . .h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	H	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	G_{A0}	Q_{B0}	Q_{H0}

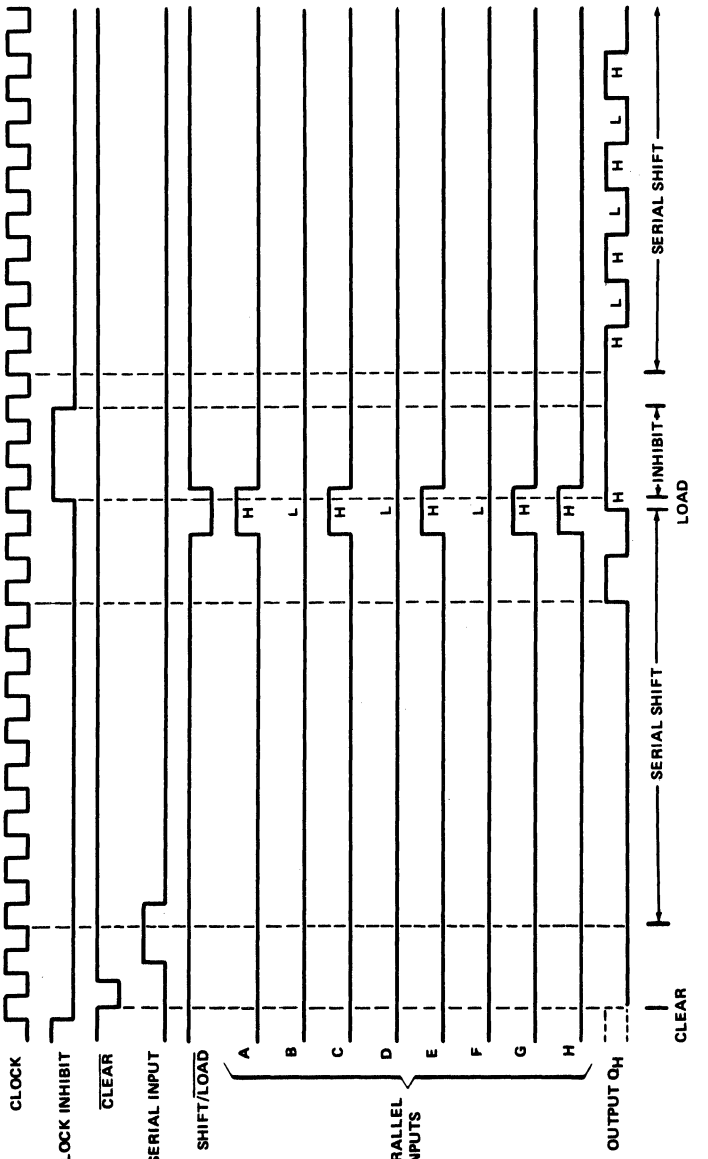
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F166 . . . . . −55°C to 125°C
SN74F166 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F166			SN74F166			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54F166			SN74F166			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V, I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 0, V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{CLR}$, SER	V_{CC} = 5.5 V, V_I = 2.7 V			40			40	μA
	Others				20			20	
I_{IL}	$\overline{CLR}$, SER	V_{CC} = 5.5 V, V_I = 0.5 V			−40			−40	μA
	Others				−20			−20	
I_{OS}§		V_{CC} = 5.5 V, V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V		41	60		41	60	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		SN54F166		SN74F166		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		135				110		MHz
t_w	Pulse duration	$\overline{CLR}$ low	4				4		ns
		CLK high	3.5				3.5		
		CLK low	5.5				6.5		
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$ high	3				4		ns
		SER	25				3		
		CLK INH low	5				6		
		Data	2.5				3		
		$\overline{CLR}$ inactive	4				4.5		
t_h	Hold time after CLK↑	SH/$\overline{LD}$ high	0				0		ns
		SER	0				0		
		CLK INH high	0				0		
		Data	0				0		

switching characteristics (see Note 1)

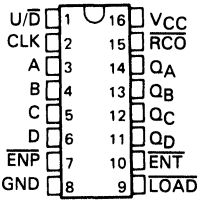
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F166			SN54F166		SN74F166		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			135	175				110		MHz
t_{PHL}	$\overline{CLR}$	Q_H	3.2	6.1	8.5			3.2	9.5	ns
t_{PLH}	CLK	Q_H	4.2	7.1	10			4.2	14	ns
t_{PHL}			3.2	5.6	8			2.7	9	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

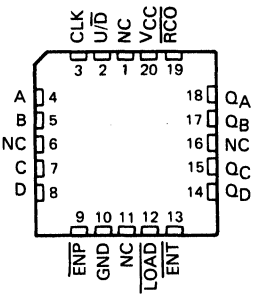
D2932, MARCH 1987—REVISED JANUARY 1989

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic "Small Outline" DIPs and Ceramic Chip Carriers in Addition to the Standard 300-mil Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F168, SN54F169 . . . J PACKAGE
SN74F168, SN74F169 . . . D OR N PACKAGE
(TOP VIEW)



SN54F168, SN54F169 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'F168 is a decade counter and the 'F169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and their maximum count. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54F168 and SN54F169 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F168 and SN74F169 are characterized for operation from 0°C to 70°C.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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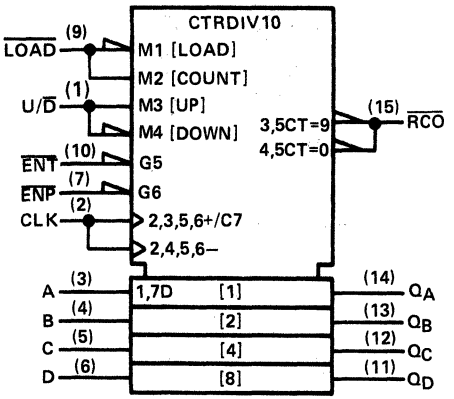
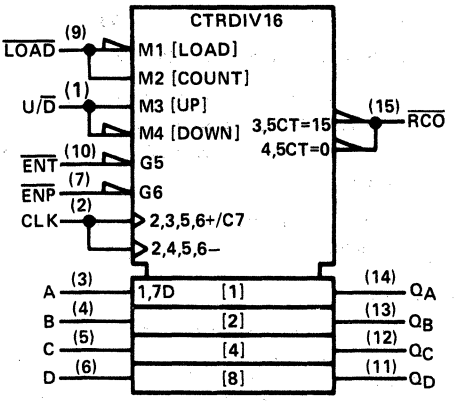
logic symbols†

'F168



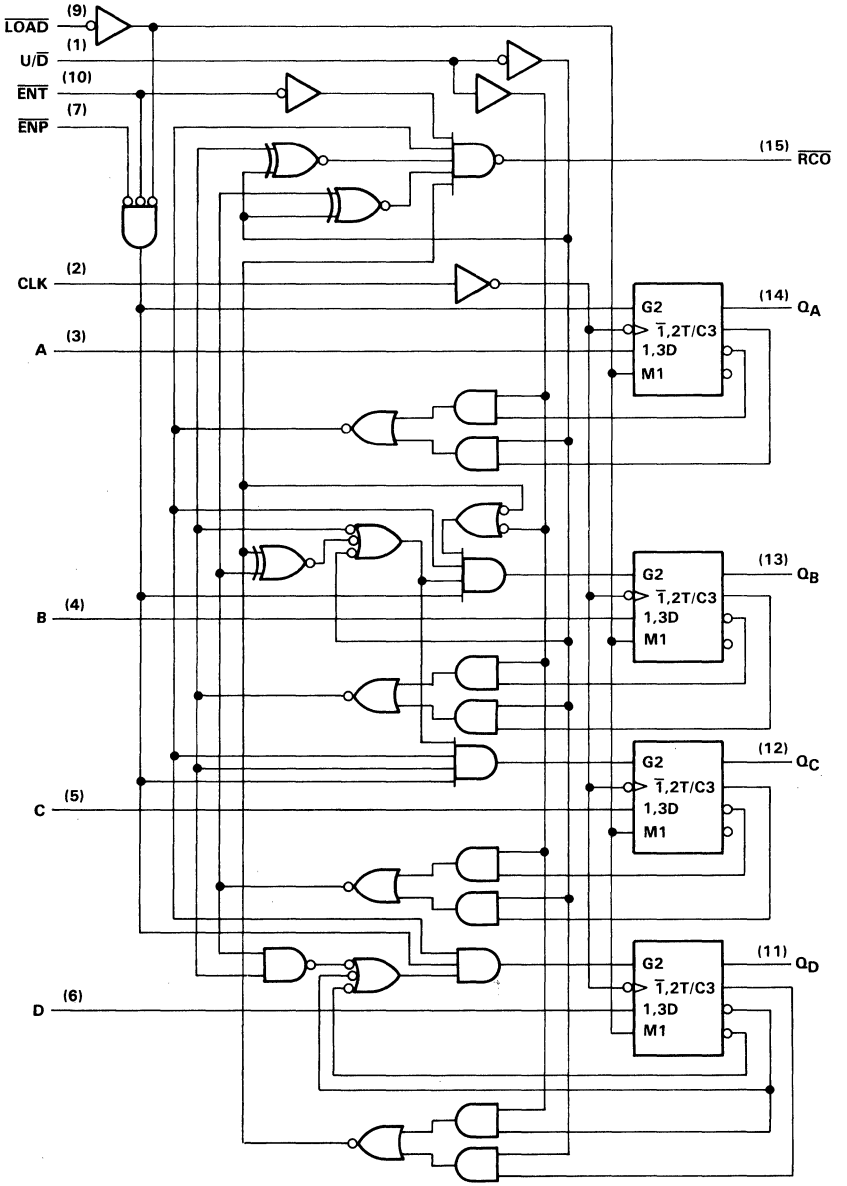
'F169



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

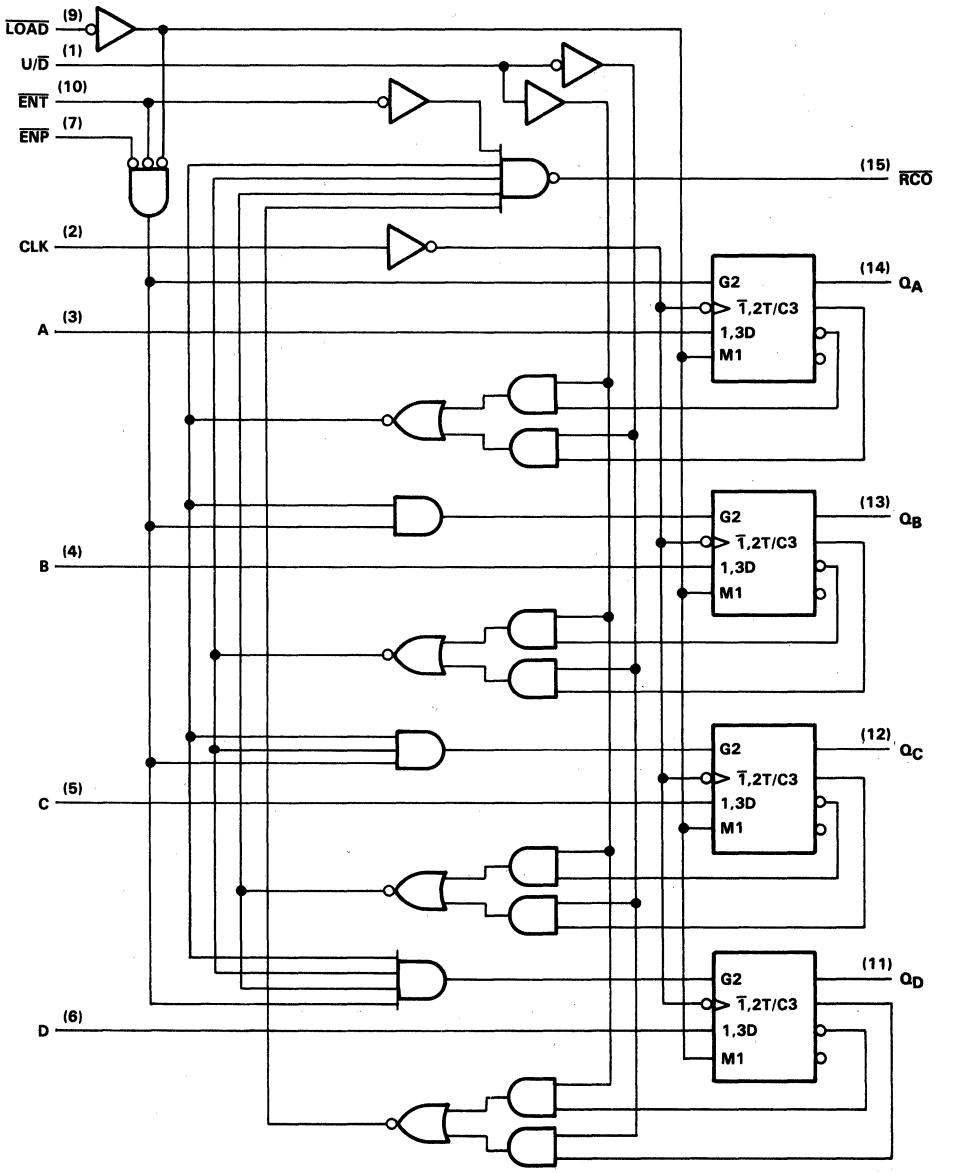
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'F168 logic diagram (positive logic)



Logic diagrams for the four flip-flops are shown separately.
Pin numbers shown are for D, J, and N packages.

'F169 logic diagram (positive logic)



Logic diagrams for the four flip-flops are shown separately.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
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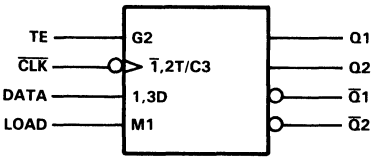
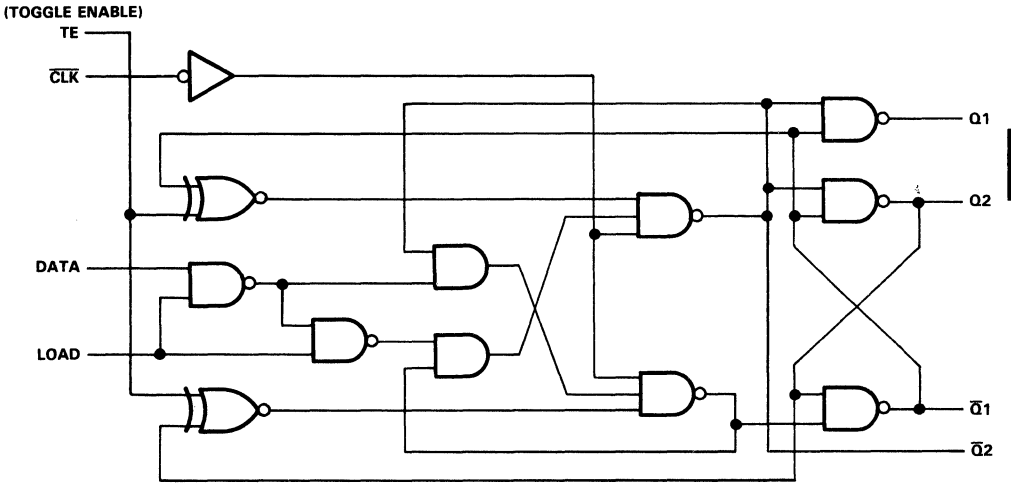
logic symbol, each flip-flop in 'F168 and 'F169 (positive logic)



logic diagram, each flip-flop in 'F168 and 'F169 (positive logic)



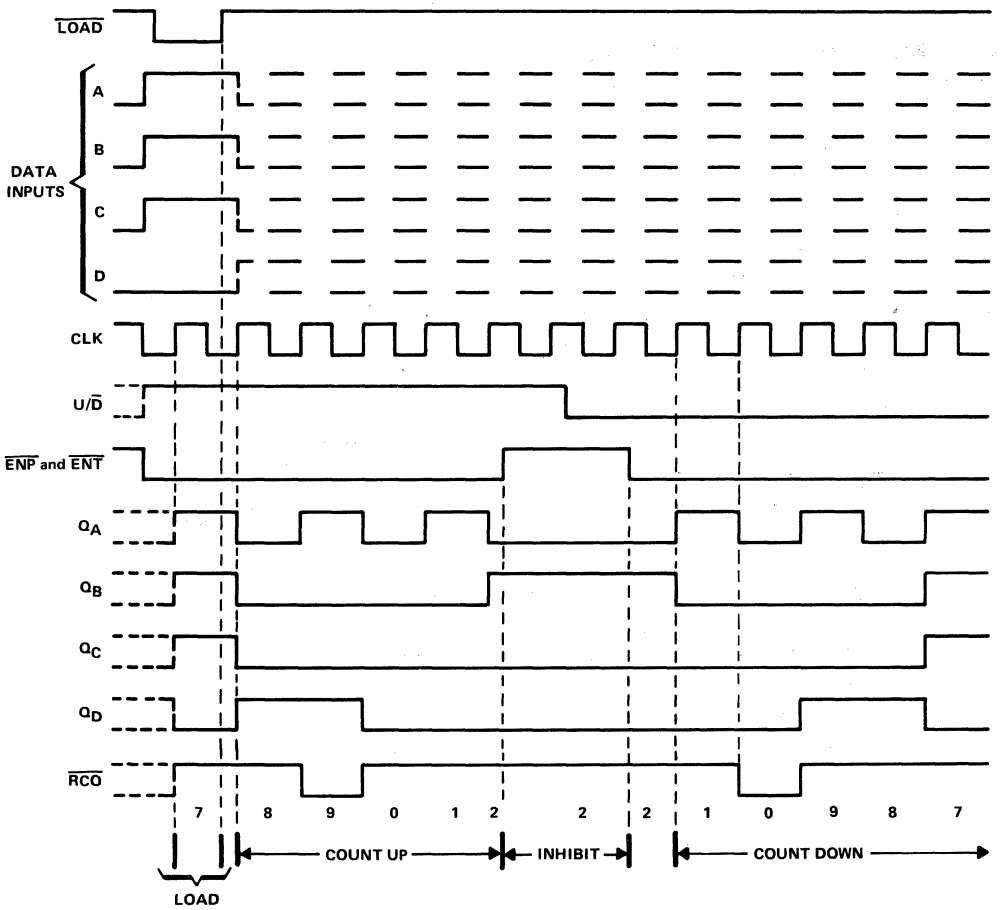
FUNCTION TABLE, EACH FLIP-FLOP

COUNTER INPUTS		FLIP-FLOP INPUTS				OUTPUTS	
$\overline{\text{LOAD}}$	CLK	LOAD	TE	$\overline{\text{CLK}}$	DATA	Q	$\overline{\text{Q}}$
L	↑	H	L	↓	H	H	L
L	↑	H	L	↓	L	L	H
H	↑	L	H	↓	X	$\overline{Q}_0$	Q_0
H	↑	L	L	↓	X	Q_0	$\overline{Q}_0$

'F168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



TEXAS INSTRUMENTS
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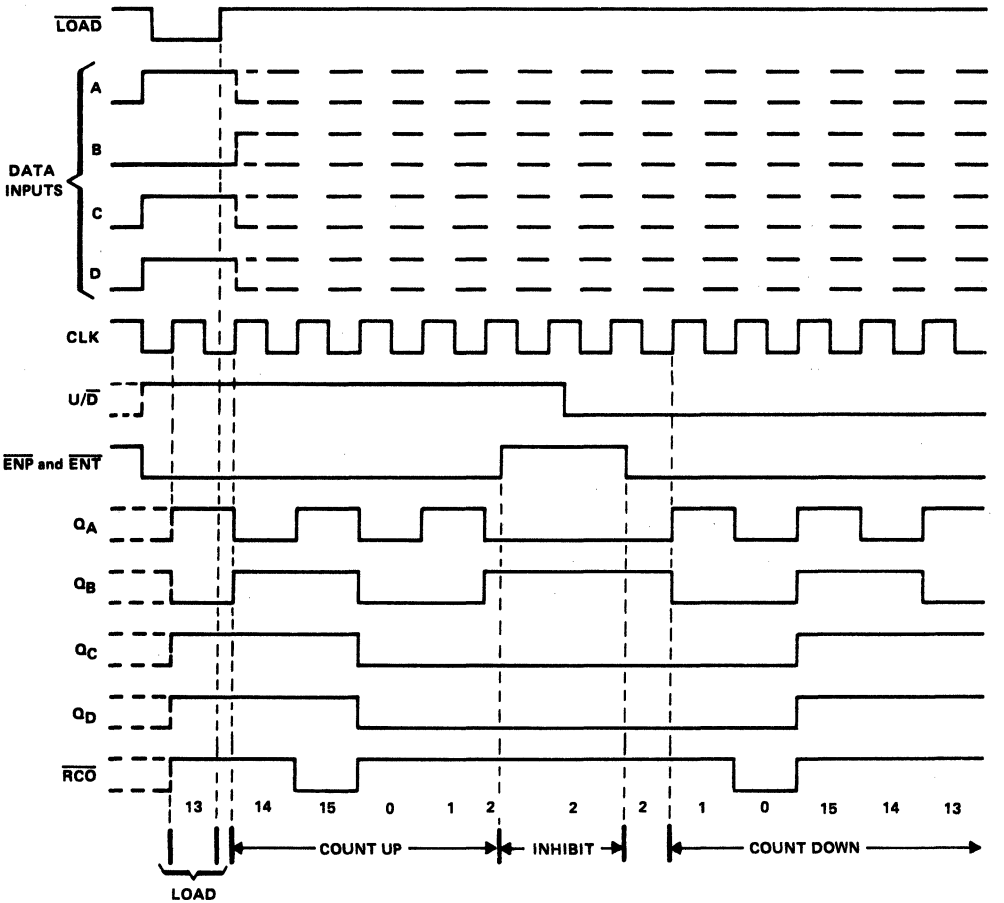
'F169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F168, SN54F169 . . . . . −55°C to 125°C
SN74F168, SN74F169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F'			SN74F'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5		5		V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F'			SN74F'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.5 V			−1.2			−1.2	mA
	All others					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38	52		38	52	mA

PRODUCT PREVIEW

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with B and $\overline{ENT}$ inputs high and all other inputs low.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = MIN to MAX†, T_A = MIN to MAX†				UNIT
			'F168, 'F169		SN54F'		SN74F'		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100			0	90	MHz
t_{su}	Setup time, data (A, B, C, D) high or low before CLK↑		4				4.5		ns
t_{hold}	Hold time, data (A, B, C, D) high or low after CLK↑		3				3.5		ns
t_{su}	Setup time, $\overline{ENP}$ and $\overline{ENT}$ high or low before CLK↑		5				6		ns
t_{hold}	Hold time, $\overline{ENP}$ and $\overline{ENT}$ high or low after CLK↑		0				0		ns
t_{su}	Setup time, $\overline{LOAD}$ high or low before CLK↑		8				9		ns
t_{hold}	Hold time, $\overline{LOAD}$ high or low after CLK↑		0				0		ns
t_{su}	Setup time, U/$\overline{D}$ before CLK↑	'F168, high	11				12.5		ns
		'F168, low	16.5				18		
		'F169, high	11				12.5		
		'F169, low	7				8		
t_{hold}	Hold time, U/$\overline{D}$ high or low after CLK↑		0				0		ns
t_w	Pulse duration, CLK high or low		5				5.5		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = MIN to MAX†, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†						UNIT
			'F168, 'F169			SN54F'			SN74F'			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			100	115					90			MHz
t_{PLH}	CLK	Q	2.2	6.1	8.5				2.2		9.5	ns
t_{PHL}			3.2	8.6	11.5				3.2		13	
t_{PLH}	CLK	$\overline{RCO}$	4.7	11.6	15.5				4.7		17	ns
t_{PHL}			3.2	8.1	11				3.2		12.5	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.7	4.1	6				1.7		7	ns
t_{PHL}			1.7	5.6	8				1.7		9	
t_{PLH}	U/$\overline{D}$ ('F168)	$\overline{RCO}$	2.7	8.1	11				2.7		12.5	ns
t_{PHL}			3.2	12.1	16				3.2		17.5	
t_{PLH}	U/$\overline{D}$ ('F169)	$\overline{RCO}$	2.7	8.1	11				2.7		12.5	ns
t_{PHL}			3.2	7.6	10.5				3.2		12	

PRODUCT PREVIEW

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Contains Six Flip-Flops with Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Fully-Buffered Outputs for Maximum Isolation from External Disturbances**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

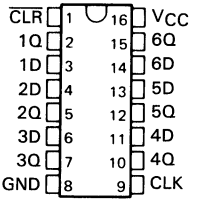
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54F174 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F174 is characterized for operation from 0°C to 70°C.

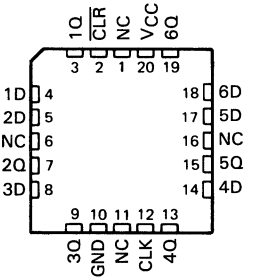
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	L	Q_0

SN54F174 . . . J PACKAGE
SN74F174 . . . D OR N PACKAGE
(TOP VIEW)

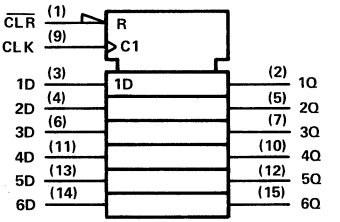


SN54F174 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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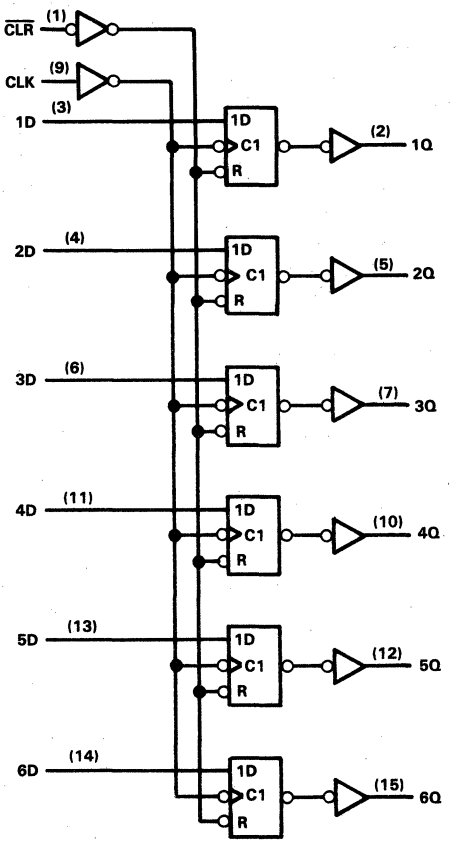
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage†	−1.2 V to 7 V
Input current	−30 mA to 5 mA
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F174	−55°C to 125°C
SN74F174	0°C to 70°C
Storage temperature range	−65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F174			SN74F174			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F174			SN74F174			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		30	45		30	45	mA

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'F174		SN54F174		SN74F174		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100			0	80	MHz
t_{su}	Setup time data high or low before CLK↑		4				4		ns
t_h	Hold time data high or low after CLK↑		0				0		ns
t_w	Pulse duration	CLK high	4				4		ns
		CLK low	6				6		
		$\overline{CLR}$ low	5				5		
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑¶		5				5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
¶ Inactive-state setup time is also referred to as "recovery time".
NOTE 1: With all outputs open and 4.5 V applied to all data and enable inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to CLK.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F174			SN54F174		SN74F174		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	140				80		MHz
t_{PLH}	CLK	Q	2.7	5.1	8			2.7	9	ns
t_{PHL}			3.7	6.6	10			3.7	11	ns
t_{PHL}	$\overline{CLR}$	Q	4.2	9.6	14			4.2	15	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- **Contains Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

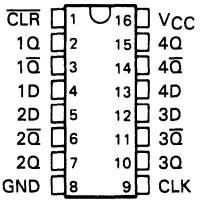
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54F175 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F175 is characterized for operation from 0°C to 70°C.

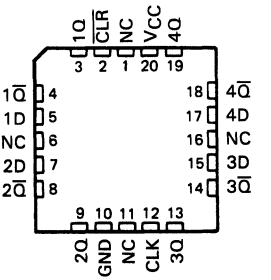
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	L	Q_0	$\overline{Q}_0$

SN54F175 . . . J PACKAGE
SN74F175 . . . D OR N PACKAGE
(TOP VIEW)

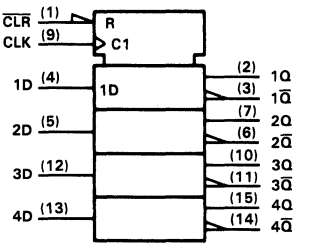


SN54F175 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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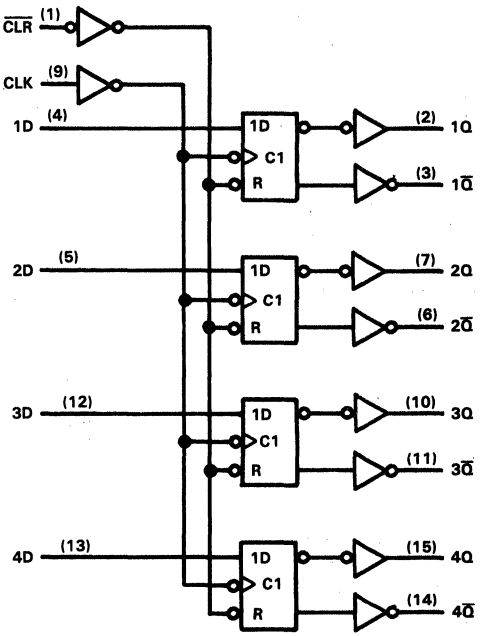
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F175 . . . . . −55°C to 125°C
SN74F175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F175			SN74F175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F175			SN74F175			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		22.5	34		22.5	34	mA

PRODUCT PREVIEW

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'F175		SN54F175		SN74F175		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_{su}	Setup time data high or low before CLK↑		3		3		3		ns
t_h	Hold time data high or low after CLK↑		1		1		1		ns
t_w	Pulse duration	CLK high	4		4		4		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Inactive-state setup time $\overline{CLR}$ high before CLK↑¶		5		5		5		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F175			SN54F175		SN74F175		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	140		100		100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3.2	4.6	6.5	2.7	8.5	3.2	7.5	ns
t_{PHL}			3.2	6.1	8.5	3.2	10.5	3.2	9.5	
t_{PHL}	$\overline{CLR}$	Q	3.7	8.6	11.5	3.7	15	3.7	13	ns
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	3.2	6.1	8.5	3.2	10	3.2	9	ns

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
¶ Inactive-state setup time is also referred to as "recovery time".

NOTES: 1. I_{CC} is measured with outputs open with 4.5 V applied to all data inputs, after a momentary ground followed by 4.5 V applied to CLK.
2. Load circuits and waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2932, MARCH 1987—REVISED JANUARY 1989

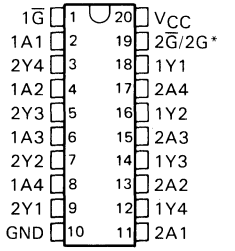
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

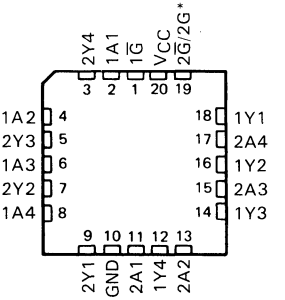
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The SN54F240 and SN54F241 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F240 and SN74F241 are characterized for operation from 0°C to 70°C.

SN54F240, SN54F241 . . . J PACKAGE
SN74F240, SN74F241 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F240, SN54F241 . . . FK PACKAGE
(TOP VIEW)



*$2\overline{G}$ for 'F240 or 2G for 'F241

FUNCTION TABLES

'F240

OUTPUT CONTROL $\overline{G}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	H
L	H	L

'F241

OUTPUT CONTROL $1\overline{G}$	DATA INPUT 1A	OUTPUT 1Y
H	X	Z
L	L	L
L	H	H

'F241

OUTPUT CONTROL 2G	DATA INPUT 2A	OUTPUT 2Y
L	X	Z
H	L	L
H	H	H

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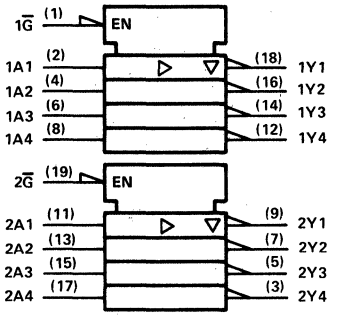
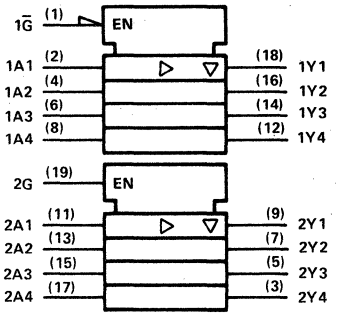
logic symbols†

'F240



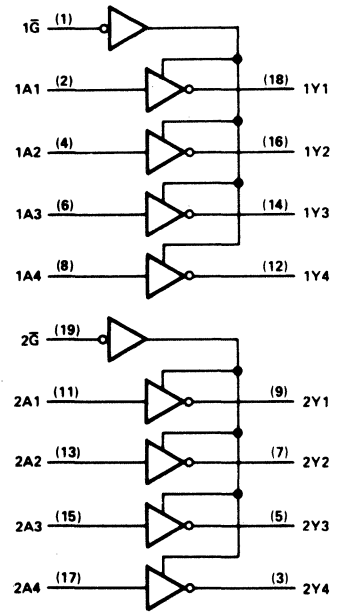
'F241



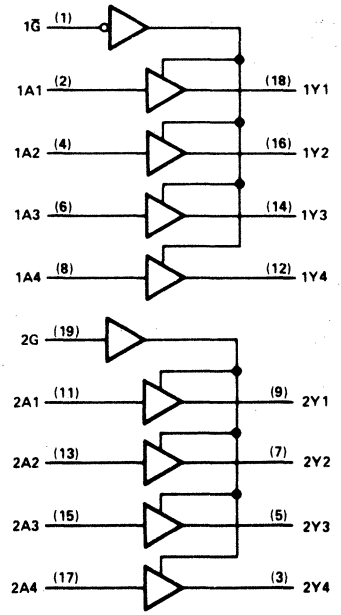
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'F240



'F241



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F240, SN54F241 . . . . . 96 mA
SN74F240, SN74F241 . . . . . 128 mA
Operating free-air temperature range: SN54F240, SN54F241 . . . . . −55°C to 125°C
SN74F240, SN74F241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F240 SN54F241			SN74F240 SN74F241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F240			SN74F240			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
	V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		19	29		19	29	mA
		Outputs low		50	75		50	75	
		Outputs disabled		42	63		42	63	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = MIN to MAX†, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F240			SN54F240		SN74F240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data	Y	2.2	4.7	7	2.2	9	2.2	8	ns
t_{PHL}	(Any A)		1.2	3.1	4.7	1.2	6	1.2	5.7	
t_{PZH}	$\overline{G}$	Y	1.2	3.1	5.3	1.2	6.7	1.2	6.1	ns
t_{PZL}			3.2	6.5	9	3.2	10.5	3.2	10	
t_{PHZ}	$\overline{G}$	Y	1.2	3.6	5.3	1.2	6.5	1.2	6.3	ns
t_{PLZ}			1.2	5.6	8	1.2	12.5	1.2	9.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: See Section 1 for load circuits and waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F241			SN74F241			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.7	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	G or $\overline{G}$ input	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
	Any A input					−1.6			−1.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		40	60		40	60	mA
			Outputs low		60	90		60	90	
			Outputs disabled		60	90		60	90	

switching characteristics (see Note 1)

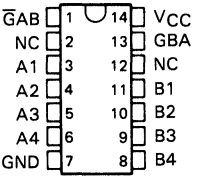
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = MIN to MAX†, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F241			SN54F241		SN74F241		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data	Y	1.7	3.6	5.2	1.2	6.5	1.7	6.2	ns
t_{PHL}	(Any A)		1.7	3.6	5.2	1.2	7	1.7	6.5	
t_{PZH}	1$\overline{G}$ or 2G	Y	1.2	3.9	5.7	1.2	7	1.2	6.7	ns
t_{PZL}			1.2	5	7	1.2	8.5	1.2	8	
t_{PHZ}	1$\overline{G}$ or 2G	Y	1.2	4.1	6	1.2	7	1.2	7	ns
t_{PLZ}			1.2	4.1	6	1.2	7.5	1.2	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: See Section 1 for load circuits and waveforms.

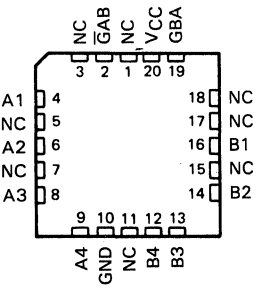
D2932, MARCH 1987—REVISED AUGUST 1988

- **2-Way Asynchronous Communication Between Data Buses**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F242, SN54F243 . . . J PACKAGE
SN74F242, SN74F243 . . . D OR N PACKAGE
(TOP VIEW)



SN54F242, SN54F243 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These quadruple bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing.

Each device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs GBA and $\overline{G}$AB. The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous activation of GBA and $\overline{G}$AB. Each output sustains its input in this transceiver configuration. Thus, when both control inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) will remain at their states. The 4-bit codes appearing on the two sets of buses will be identical for the 'F243, or complementary for the 'F242.

The SN54F242 and SN54F243 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F242 and SN74F243 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE INPUTS		'F242	'F243
$\overline{G}$AB	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

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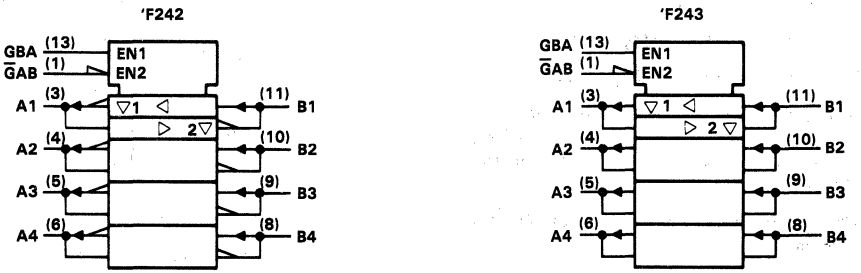
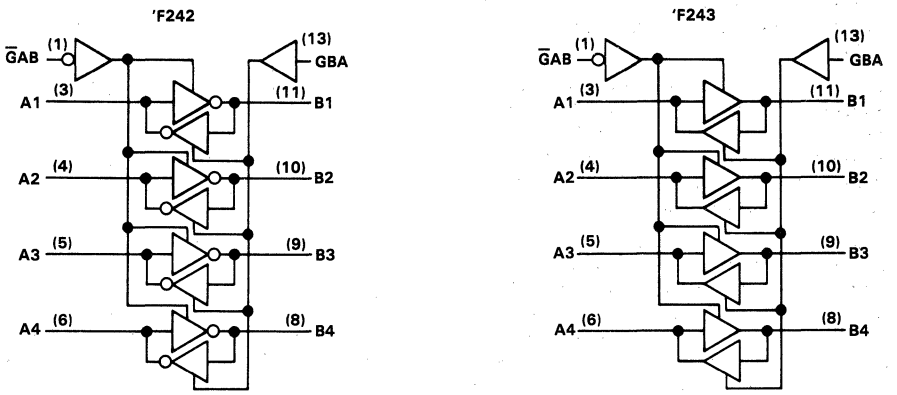
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F242, SN54F243 . . . . . 96 mA
SN74F242, SN74F243 . . . . . 128 mA
Operating free-air temperature range: SN54F242, SN54F243 . . . . . −55°C to 125°C
SN74F242, SN74F243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54F242			SN74F242			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F242			SN74F242			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.42	0.55	
I_I	A or B port	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	A or B port‡	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1	Outputs high		30	46		30	46	mA
			Outputs low		46	69		46	69	
			Outputs disabled		42	63		42	63	

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F242			SN54F242		SN74F242		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	4.1	6.5	2.2	9	2.2	7.5	ns
t_{PHL}			1	2.6	4.5	0.5	5	1	4.5	ns
t_{PZL}	Enable	A or B	2.7	5.6	7.5	2.2	10	2.7	8.5	ns
t_{PZH}			2.7	6.1	9	2.2	12	2.7	10.5	ns
t_{PHZ}	Disable	A or B	1.8	6.6	9	1.8	11	1.8	9.5	ns
t_{PLZ}			2.7	5.6	9.5	2.3	13.5	2.7	11	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured either with all transceivers enabled in only one direction or all transceivers disabled.
2. Load circuits and waveforms are shown in Section 1.

recommended operating conditions

		SN54F243			SN74F243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F243			SN74F243			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.42	0.55	
I_I	A or B port	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	A or B port‡	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1.6	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1	Outputs high		64	80		64	80	mA
			Outputs low		64	90		64	90	
			Outputs disabled		71	90		71	90	

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F243			SN54F243		SN74F243		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	3.6	5.2	1.2	6.5	1.2	6.2	ns
t_{PHL}			1.7	3.6	5.2	1.2	8.5	1.2	6.5	ns
t_{PZH}	Enable	A or B	1.2	3.9	5.7	1.2	8	1.2	6.7	ns
t_{PZL}			1.2	5.4	7.5	1.2	10.5	1.2	8.5	ns
t_{PHZ}	Disable	A or B	1.2	4.1	6	1	7.5	1	7	ns
t_{PLZ}			2	4.5	6	2	8.5	2	7	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured either with all transceivers enabled in only one direction or all transceivers disabled.
2. Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

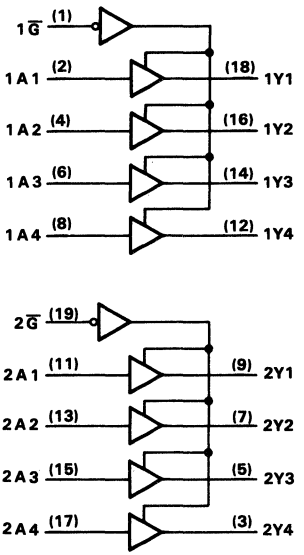
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

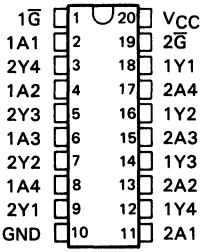
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F240 and 'F241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control inputs, and complementary G and $\overline{G}$ inputs.

The SN54F244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F244 is characterized for operation from 0°C to 70°C.

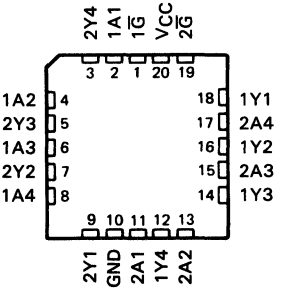
logic diagram (positive logic)

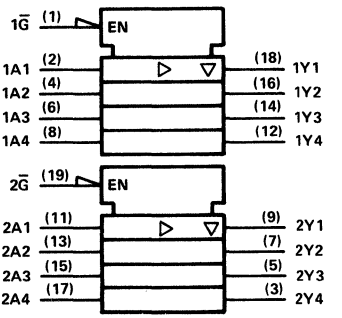


SN54F244 . . . J PACKAGE
SN74F244 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F244 . . . FK PACKAGE
(TOP VIEW)





† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION TABLE

OUTPUT CONTROL $1\overline{G}$, $2\overline{G}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	L
L	H	H

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F244 . . . . . 96 mA
SN74F244 . . . . . 128 mA
Operating free-air temperature range: SN54F244 . . . . . −55°C to 125°C
SN74F244 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F244			SN74F244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54F244			SN74F244			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.38	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Any $\overline{G}$ input	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
	Any A input					−1.6			−1.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		40	60		40	60	mA
			Outputs low		60	90		60	90	
			Outputs disabled		60	90		60	90	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F244			SN54F244		SN74F244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.7	3.6	5.2	2	6.5	1.7	6.2	ns
t_{PHL}			1.7	3.6	5.2	2	7	1.7	6.5	
t_{PZH}	$1\overline{G}$ or $2\overline{G}$	Y	1.2	3.9	5.7	2	7	1.2	6.7	ns
t_{PZL}			1.2	5	7	2	8.5	1.2	8	
t_{PHZ}	$1\overline{G}$ or $2\overline{G}$	Y	1.2	4.1	6	2	7	1.2	7	ns
t_{PLZ}			1.2	4.1	6	2	7.5	1.2	7	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

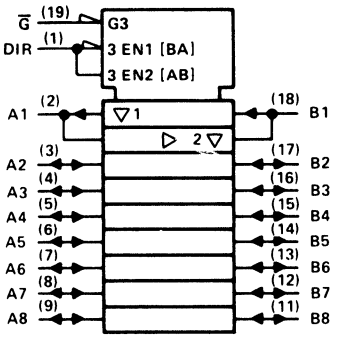
description

The SN54F245 and SN74F245 are octal bus transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

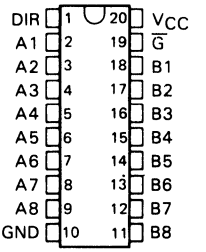
The SN54F245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F245 is characterized for operation from 0°C to 70°C.

logic symbol†

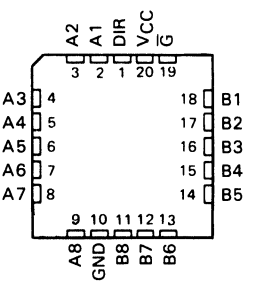


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54F245 . . . J PACKAGE
SN74F245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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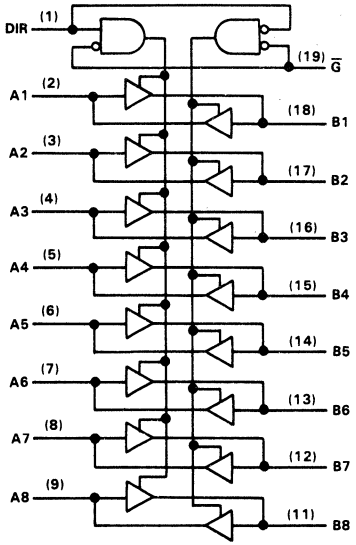
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (excluding I/O ports)† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F245 (A1 thru A8) . . . . . 40 mA
SN54F245 (B1 thru B8) . . . . . 96 mA
SN74F245 (A1 thru A8) . . . . . 48 mA
SN74F245 (B1 thru B8) . . . . . 128 mA
Operating free-air temperature range: SN54F245 . . . . . −55°C to 125°C
SN74F245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F245			SN74F245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54F245			SN74F245			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any output	V_{CC} = 4.75 V, I_{OH} = −1 mA to −3 mA					2.7			V
	A1 thru A8	V_{CC} = MIN	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8		I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	A1 thru A8	V_{CC} = MIN	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	DIR and $\overline{G}$	V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
	A and B		V_I = 5.5 V			1			1	
I_{IH}§	A and B	V_{CC} = MAX, V_I = 2.7 V				70			70	μA
	DIR and $\overline{G}$					20			20	
I_{IL}§	A and B	V_{CC} = MAX, V_I = 0.5 V				−0.65			−0.65	mA
	DIR and $\overline{G}$					−1.2			−1.2	
I_{OS}¶	A1 thru A8	V_{CC} = MAX, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8			−100		−225	−100		−225	
I_{CCH}		V_{CC} = MAX			70	90		70	90	mA
I_{CCL}		V_{CC} = MAX			95	120		95	120	mA
I_{CCZ}		V_{CC} = MAX			85	110		85	110	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F245			SN54F245		SN74F245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	3.8	6	1.2	7.5	1.7	7	ns
t_{PHL}			1.7	4.2	6	1.2	7.5	1.7	7	
t_{PZH}	$\overline{G}$	A or B	2.2	4.9	7	1.7	9	2.2	8	ns
t_{PZL}			2.7	5.6	8	2.2	10	2.7	9	
t_{PHZ}	$\overline{G}$	A or B	2.2	4.6	6.5	1.7	9	2.2	7.5	ns
t_{PLZ}			1.2	4.6	6.5	1.2	10	1.2	7.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- **Three-State Versions of SN54F151A and SN74F151A**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

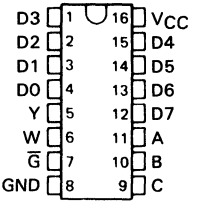
The SN54F251A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F251A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

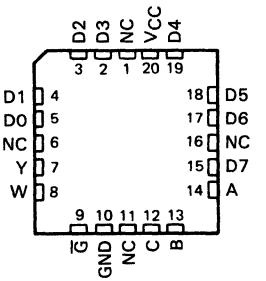
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input

SN54F251A . . . J PACKAGE
SN74F251A . . . D OR N PACKAGE
(TOP VIEW)

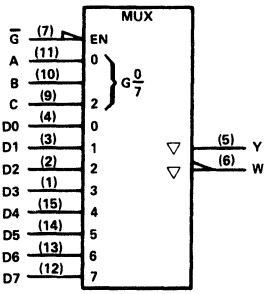


SN54F251A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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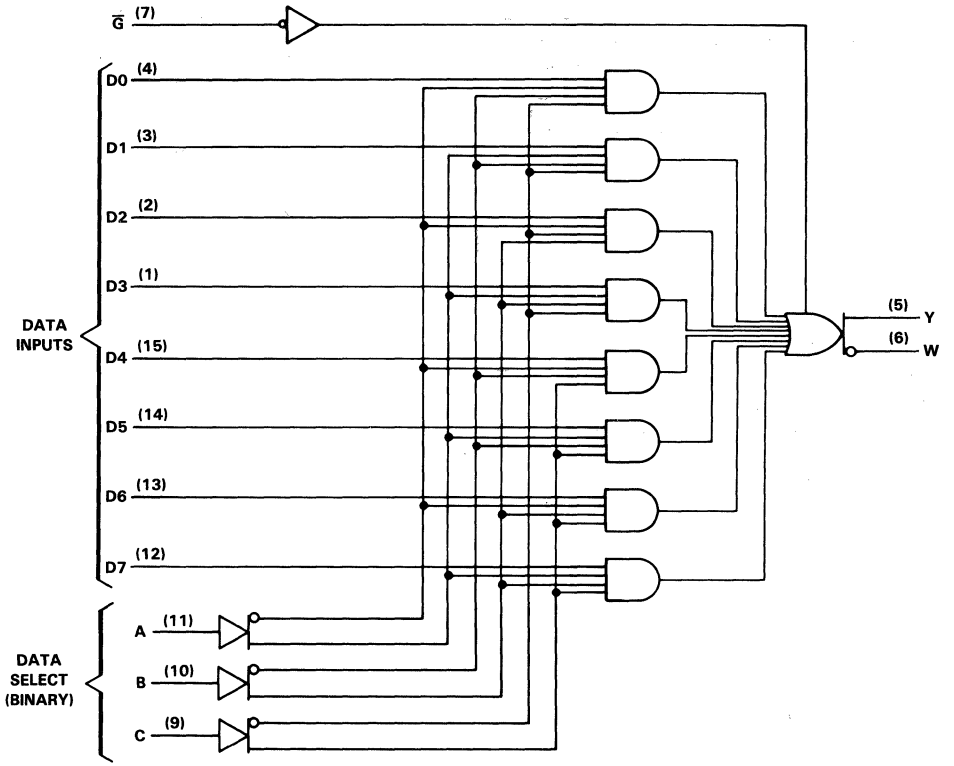
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F251A . . . . . 40 mA
SN74F251A . . . . . 48 mA
Operating free-air temperature range: SN54F251A . . . . . −55°C to 125°C
SN74F251A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F251A			SN74F251A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F251A			SN74F251A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.30	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1	Condition A		15	22		15	22	mA
		Condition B		16	24		16	24	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with the outputs open under the following conditions:
A. Select input and data input at 4.5 V, output control grounded.
B. All inputs at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F251A			SN54F251A		SN74F251A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	W	2.7	5.4	9	2.7	11.5	2.7	9.5	ns
t_{PHL}			2.4	4.6	7.5	2.4	8	2.4	7.5	
t_{PLH}	A, B, or C	Y	3.7	7.1	10.5	2.7	14	3.7	12.5	ns
t_{PHL}			3.2	5.6	8.5	2.2	10.5	3.2	9	
t_{PLH}	Data (Any D)	W	2.2	4.6	6.5	1.7	8	2.2	7	ns
t_{PHL}			1	2.1	4	1	6	1	5	
t_{PLH}	Data (Any D)	Y	2.7	4.6	7	1.7	9	1.7	8	ns
t_{PHL}			2.7	5.1	7	2.7	9	2.7	7.5	
t_{PZH}	$\overline{G}$	W	1.7	3.9	6	1.3	7	1.7	7	ns
t_{PZL}			1.7	3.9	6	1.7	7.5	1.7	6.5	
t_{PHZ}	$\overline{G}$	W	1.7	3.6	5.5	1.7	6	1.7	6	ns
t_{PLZ}			1	2.6	4.5	1	5	2.9	4.5	
t_{PZH}	$\overline{G}$	Y	2.7	4.4	7	2.3	8.5	2.3	7.5	ns
t_{PZL}			2.7	5.1	7.5	2.7	9	2.7	8	
t_{PHZ}	$\overline{G}$	Y	1.3	3.4	5.5	1.3	5.5	1.3	5.5	ns
t_{PLZ}			2	2.6	4.5	1	5.5	1	4.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Three-State Versions of SN54F153 and SN74F153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

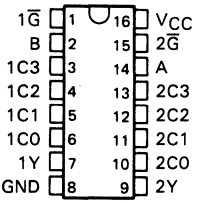
The SN54F253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F253 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

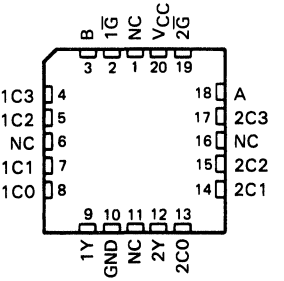
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

SN54F253 . . . J PACKAGE
SN74F253 . . . D OR N PACKAGE
(TOP VIEW)

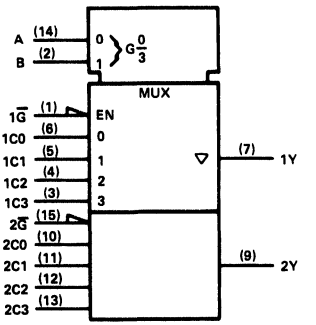


SN54F253 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

2 Data Sheets

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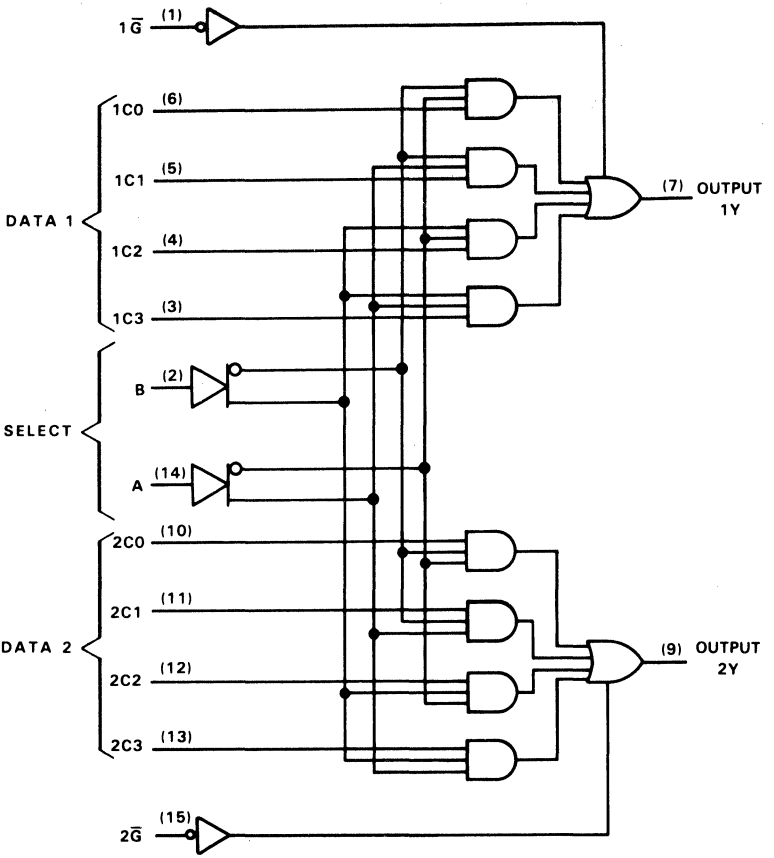
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F253 . . . . . 40 mA
SN74F253 . . . . . 48 mA
Operating free-air temperature range: SN54F253 . . . . . −55°C to 125°C
SN74F253 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F253			SN74F253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F253			SN74F253			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.30	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V, See Note 1		Condition A		11.5	16		11.5	16	mA
I_{CCL}			Condition B		16	23		16	23	
I_{CCZ}			Condition C		16	23		16	23	

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with the outputs open under the following conditions:
A. Inputs A, B, 1C3, and 2C3 at 4.5 V, other inputs grounded
B. All inputs grounded
C. Inputs $1\overline{G}$ and $2\overline{G}$ at 4.5 V, other inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F253			SN54F253		SN74F253		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	3.7	8.1	11.5	2.7	15	3.7	13	ns
t_{PHL}			2.2	6.1	9	1.7	11	2.2	10	
t_{PLH}	Data (Any C)	Any Y	2.2	5.1	7	1.7	9	2.2	8	ns
t_{PHL}			1.7	4.1	6	1.7	8	1.7	7	
t_{PZH}	$\overline{G}$	Any Y	2.2	5.6	8	1.7	10	2.2	9	ns
t_{PZL}			2.2	5.6	8	1.7	10	2.2	9	
t_{PHZ}	$\overline{G}$	Any Y	1.2	3.3	5	1.2	6.5	1.2	6	ns
t_{PLZ}			1.2	4	6	1.2	8	1.2	7	

PRODUCT PREVIEW

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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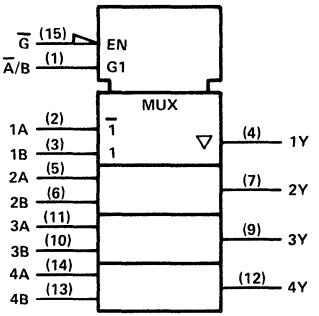
- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

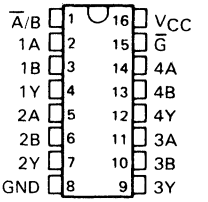
The SN54F257 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F257 is characterized for operation from 0°C to 70°C.

logic symbol†

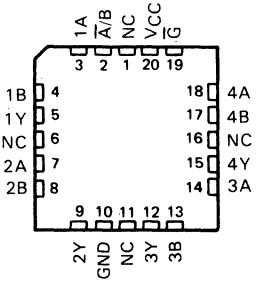


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F257 . . . J PACKAGE
SN74F257 . . . D OR N PACKAGE
(TOP VIEW)



SN54F257 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS				OUTPUT
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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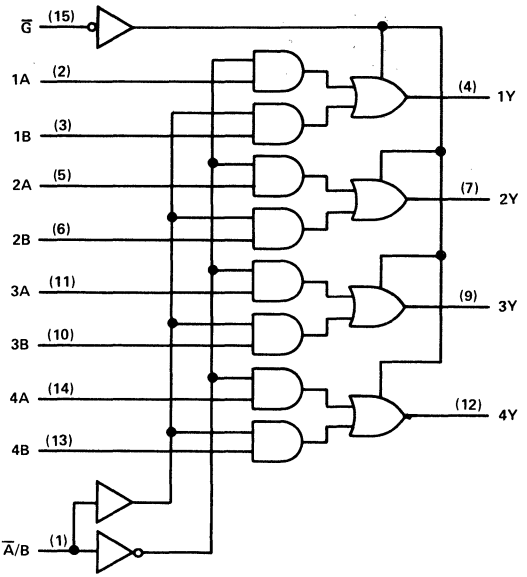
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F257 . . . . . 40 mA
SN74F257 . . . . . 48 mA
Operating free-air temperature range: SN54F257 . . . . . −55°C to 125°C
SN74F257 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F257			SN74F257			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F257			SN74F257			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.30	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V, See Note 1		Condition A		9	15		9	15	mA
I_{CCL}			Condition B		14.5	22		14.5	22	
I_{CCZ}			Condition C		15	23		15	23	

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'F257			SN54F257		SN74F257		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data (A or B)	Any Y	2.2	4.1	6	2.2	8	2.2	7	ns
t_{PHL}			1.2	3.8	5.5	1	8	1.2	6.5	
t_{PLH}	$\overline{A}$/B	Any Y	3.7	9.7	13	3.7	15.5	3.7	15	ns
t_{PHL}			2.7	6.1	8.5	2.7	10.5	2.7	9.5	
t_{PZH}	$\overline{G}$	Any Y	2.2	5.5	7.5	2.2	9.5	2.2	8.5	ns
t_{PZL}			2.2	5.1	7.5	2.2	10	2.2	8.5	
t_{PHZ}	$\overline{G}$	Any Y	1.2	3.9	6	1.2	7	1.2	7	ns
t_{PLZ}			1.2	4.1	6	1.2	9.5	1.2	7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with the outputs open under the following conditions:
A. $\overline{A}$/B and all B inputs at 4.5 V, other inputs grounded.
B. All B inputs at 4.5 V, other inputs grounded.
C. $\overline{G}$ and all B data inputs at 4.5 V, other inputs grounded.
2. Load circuits and waveforms are shown in Section 1.

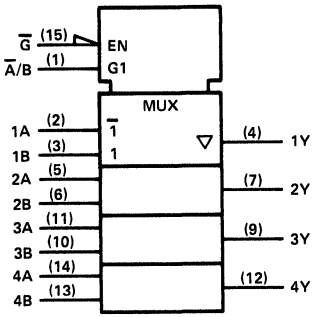
- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

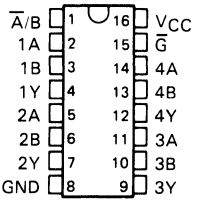
The SN54F258 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F258 is characterized for operation from 0°C to 70°C.

logic symbol†

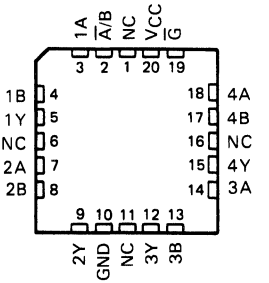


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F258 . . . J PACKAGE
SN74F258 . . . D OR N PACKAGE
(TOP VIEW)



SN54F258 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS				OUTPUT
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	OUTPUT Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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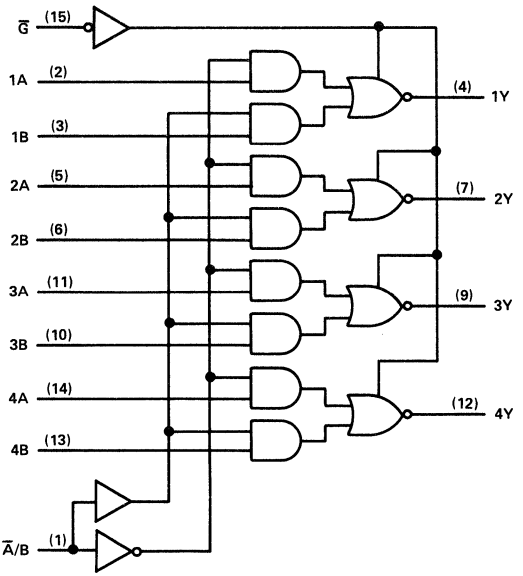
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F258 . . . . . 40 mA
SN74F258 . . . . . 48 mA
Operating free-air temperature range: SN54F258 . . . . . −55°C to 125°C
SN74F258 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F258			SN74F258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F258			SN74F258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.30	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V, See Note 1		Condition A		6.2	9.5		6.2	9.5	mA
I_{CCL}			Condition B		15.1	23		15.1	23	
I_{CCZ}			Condition C		11.3	17		11.3	17	

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'F258			SN54F258		SN74F258		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data (A or B)	Any Y	1	3.6	5.3	1	7.5	1	6	ns
t_{PHL}			1	3.1	4.7	1	6	1	5.5	
t_{PLH}	$\overline{A}$/B	Any Y	3.2	6.1	8.5	3.2	12	3.2	9.5	ns
t_{PHL}			3.2	6.9	9.5	3.2	11.5	3.2	11	
t_{PZH}	$\overline{G}$	Any Y	2.2	5.5	7.5	2.2	11	2.2	8.5	ns
t_{PZL}			2.2	5.1	7.5	2.2	9.5	2.2	8.5	
t_{PHZ}	$\overline{G}$	Any Y	1.2	3.9	6	1	7	1.2	7	ns
t_{PLZ}			1.2	4.1	6	1.2	9	1.2	7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with the outputs open under the following conditions:
A. All B inputs at 4.5 volts, other inputs grounded.
B. $\overline{A}$/B and all B inputs at 4.5 V, other inputs grounded.
C. $\overline{G}$ and all B inputs at 4.5 V, other inputs grounded.
2. Load circuits and waveforms are shown in Section 1.

D3214, JANUARY 1989

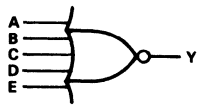
- **Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

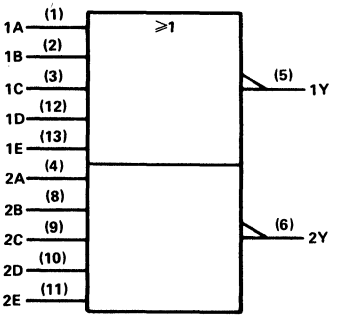
These devices contain two independent 5-input positive-NOR gates. They perform the Boolean function $Y = \overline{A+B+C+D+E}$ in positive logic.

The SN54F260 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F260 is characterized for operation from 0°C to 70°C.

logic diagram (each gate)

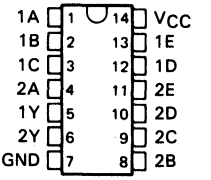


logic symbol†

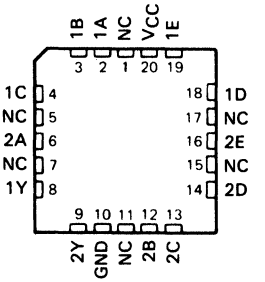


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F260 . . . J PACKAGE
SN74F260 . . . D OR N PACKAGE
(TOP VIEW)



SN54F260 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F260 . . . . . −55°C to 125°C
SN74F260 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F260			SN74F260			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F260			SN74F260			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		4.6	6.5		4.6	6.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.3	9.5		7.3	9.5	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F260			SN54F260		SN74F260		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C, D, E	Y	1.7	3.6	5.5			1.2	6.5	ns
t_{PHL}			1	2.1	4			1	4.5	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
¶ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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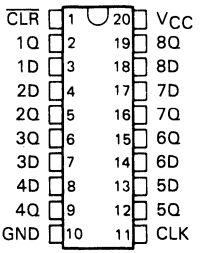
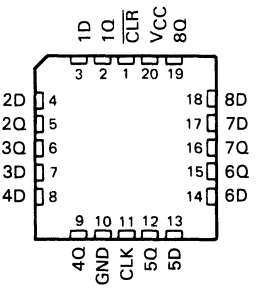
D2932, APRIL 1986—REVISED JANUARY 1989

- **Contains Eight D-Type Flip-Flops with Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Register
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F273 . . . J PACKAGE
SN74F273 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F273 . . . FK PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops implement D-type flip-flop logic with a direct clear input.

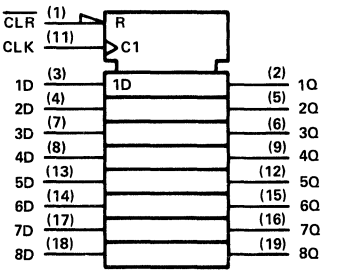
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54F273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F273 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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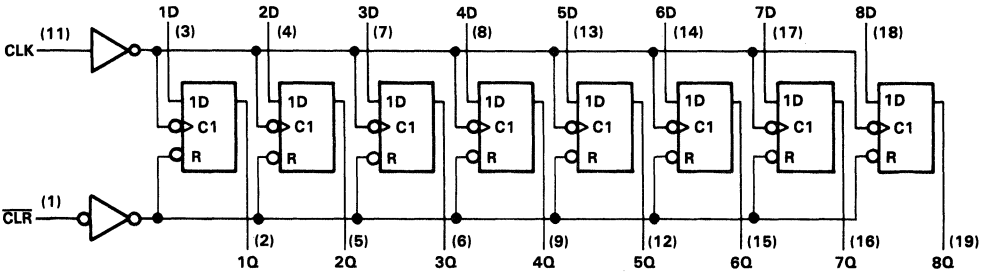
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F273 . . . . . −55°C to 125°C
SN74F273 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F273			SN74F273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F273			SN74F273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−20			−20	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 1		65	85		65	85	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 2		68	88		68	88	mA

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§		UNIT
			'F273	SN54F273	SN74F273	
			MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency					MHz
t_{su}	Setup time, data high or low before CLK↑		1.5			ns
t_h	Hold time, data high or low after CLK↑		0			ns
t_w	Pulse duration	CLK high	4			ns
		CLK low	5			
		$\overline{CLR}$ low	3.5			
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑¶		8			ns

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			'F273	SN54F273	SN74F273	
			MIN TYP MAX	MIN MAX	MIN MAX	
f_{max}			145			MHz
t_{PLH}	CLK	Any Q	7.5			ns
t_{PHL}			7.5			ns
t_{PHL}	$\overline{CLR}$	Any Q	7			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
¶ Inactive-state setup time is also referred to as "recovery time".

NOTES: 1. I_{CCH} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the $\overline{CLR}$ input at 4.5 V.
2. I_{CCL} is measured with CLR and DATA at ground.
3. Load circuits and waveforms are shown in Section 1.

D2932, APRIL 1986—REVISED JANUARY 1989

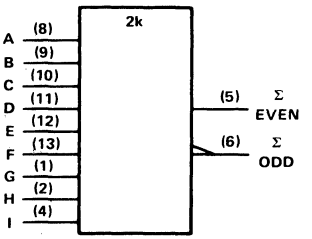
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These universal, monolithic, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

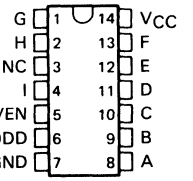
The SN54F280B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F280B is characterized for operation from 0°C to 70°C.

logic symbol†

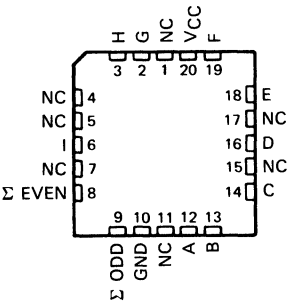


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54F280B . . . J PACKAGE
SN74F280B . . . D OR N PACKAGE
(TOP VIEW)



SN54F280B . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

2 Data Sheets

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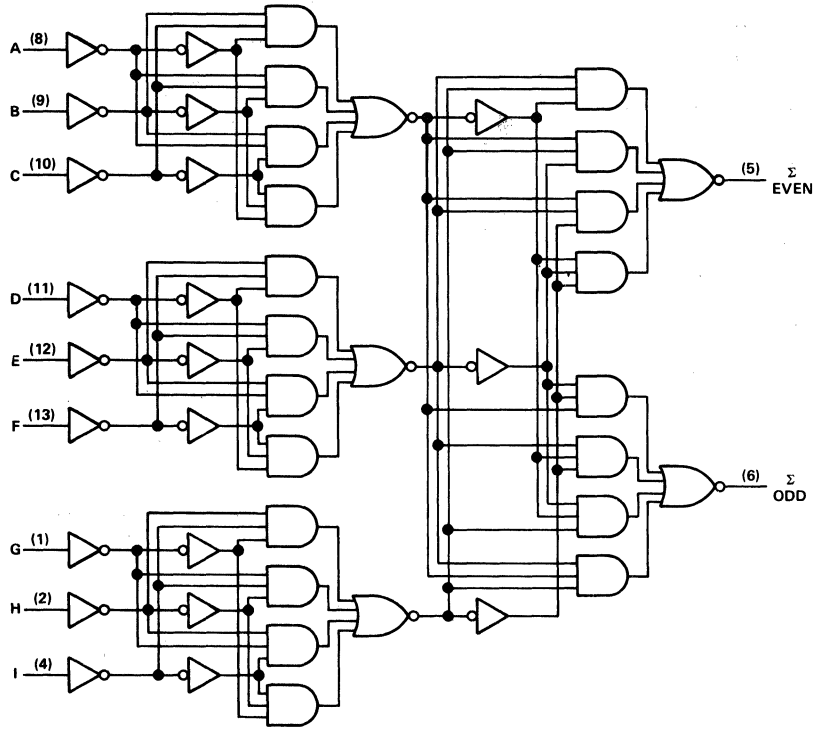
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F280B . . . . . −55°C to 125°C
SN74F280B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

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recommended operating conditions

		SN54F280B			SN74F280B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54F280B			SN74F280B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = MAX,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = MIN,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−20			−20	μA
I_{OS}‡	V_{CC} = MAX,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = MAX,	V_I = 0		26	35		26	35	mA

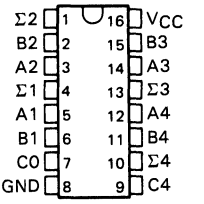
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F280B			SN54F280B		SN74F280B	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any input	EVEN	3.2	6.1	9	2.7	13	2.7	10	ns
t_{PHL}			3.2	6.6	10	2.7	15	2.7	11	
t_{PLH}	Any input	ODD	3.2	6.1	9	2.7	14	2.7	10	ns
t_{PHL}			3.2	6.6	10	2.7	14	2.7	11	

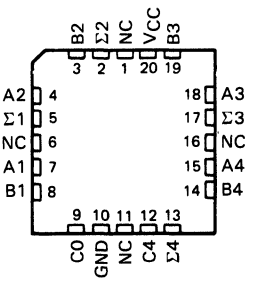
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F283 . . . J PACKAGE
SN74F283 . . . D OR N PACKAGE
(TOP VIEW)



SN54F283 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54F283 and SN74F283 are full adders that perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

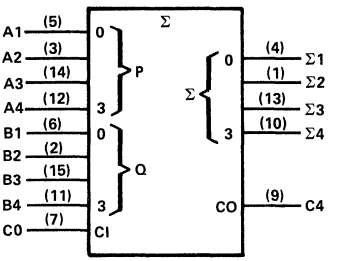
These adders feature full internal look-ahead across all four bits generating the carry term C4 in typically 5.7 nanoseconds. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End-around carry can be accomplished without the need for logic or level inversion.

The 'F283 can be used with either all-active-high (positive logic) or all-active-low (negative logic) operands.

The SN54F283 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F283 is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

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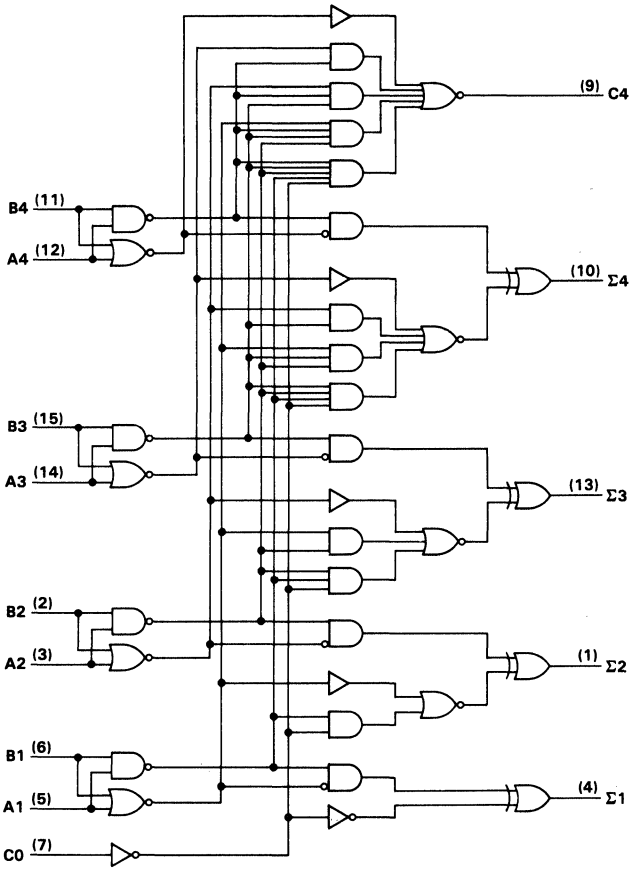
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F283 . . . . . −55°C to 125°C
SN74F283 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F283			SN74F283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F283			SN74F283			
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_{IK} = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Any A or B	V_{CC} = 5.5 V,	V_I = 0.5 V			−1.2			−1.2	mA
	CO					−0.6			−0.6	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 4.5 V		36	55		36	55	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F283			SN54F283		SN74F283		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CO	Σi	2.7	6.6	9.5	2.7	14	2.7	10.5	ns
t_{PHL}			3.2	6.6	9.5	3.2	14	3.2	10.5	
t_{PLH}	Ai or Bi	Σi	3.2	6.6	9.5	3.2	14	3.2	10.5	ns
t_{PHL}			2.7	6.6	9.5	2.7	14	2.7	10.5	
t_{PLH}	CO	C4	2.7	5.3	7.5	2.7	10.5	2.7	8.5	ns
t_{PHL}			2.2	5	7	2.2	10	2.2	8	
t_{PLH}	Ai or Bi	C4	2.7	5.3	7.5	2.7	10.5	2.7	8.5	ns
t_{PHL}			2.2	4.9	7	2.2	10	2.2	8	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: See General Information for load circuits and waveforms.

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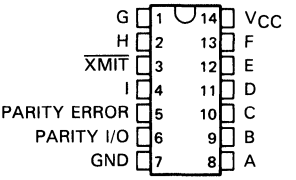
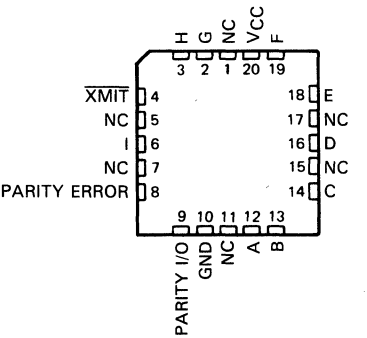
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F286 . . . J PACKAGE
SN74F286 . . . D OR N PACKAGE
(TOP VIEW)



SN54F286 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54F286 and SN74F286 universal nine-bit parity generators/checkers feature a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low, the parity tree is disabled and the Parity Error output will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

The SN54F286 is characterized for operation over the full military range of −55°C to 125°C. The SN74F286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

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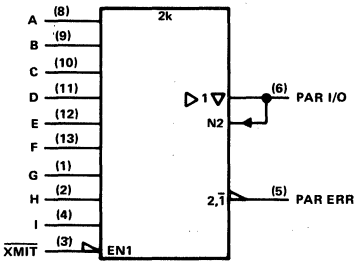
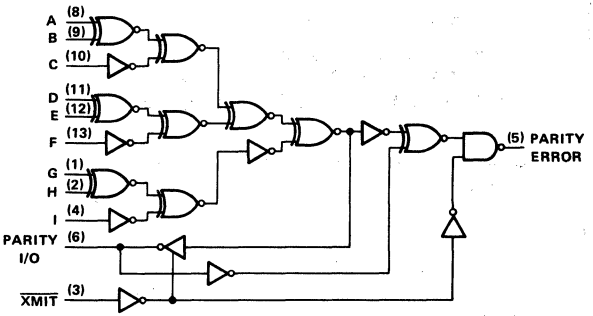
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to Parity I/O in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to either output in the high state . . . . . −0.5 V to V_{CC}
Current into either output in the low state: SN54F286 (Parity Error) . . . . . 40 mA
SN54F286 (Parity I/O) . . . . . 96 mA
SN74F286 (Parity Error) . . . . . 40 mA
SN74F286 (Parity I/O) . . . . . 128 mA
Operating free-air temperature range: SN54F286 . . . . . −55°C to 125°C
SN74F286 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F286			SN74F286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Parity Error			−1			−1	mA
		Parity I/O			−12			−15	
I_{OL}	Low-level output current	Parity Error			20			20	mA
		Parity I/O			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F286			SN74F286			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Parity Error	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	Parity I/O		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	Parity Error	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Parity I/O		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}‡	Parity I/O	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	Any other input					20			20	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	Parity I/O	V_{CC} = 5.5 V,	V_I = 0.5 V	−100		−225	−100		−225	mA
	Parity Error			−60		−150	−60		−150	
I_{CCH}		V_{CC} = 5.5 V,			27			27	44	mA
I_{CCL}		V_{CC} = 5.5 V			28			28	45	mA
I_{CCZ}		V_{CC} = 5.5 V			27			27	44	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F286			SN54F286		SN74F286		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O		8.3						ns
t_{PHL}				8.6						
t_{PLH}	Any A thru I	Parity Error		10.8						ns
t_{PHL}				10						
t_{PLH}	Parity I/O	Parity Error		4.9						ns
t_{PHL}				5						
t_{PZH}	$\overline{XMIT}$	Parity I/O		3.8						ns
t_{PZL}				5.8						
t_{PHZ}	$\overline{XMIT}$	Parity I/O		3.8						ns
t_{PLZ}				3.3						

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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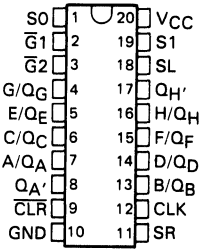
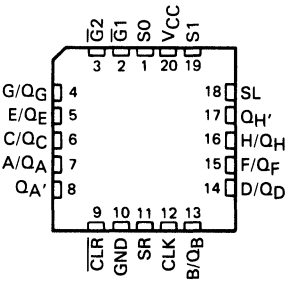
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **Operates with Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F299 . . . J PACKAGE
SN74F299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F299 . . . FK PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G1}$ or $\overline{G2}$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54F299 is characterized for operation over the full military range of −55°C to 125°C. The SN74F299 is characterized for operation from 0°C to 70°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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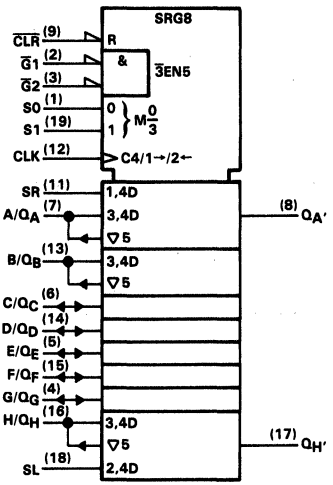
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$†	OUTPUT CONTROL $\overline{G2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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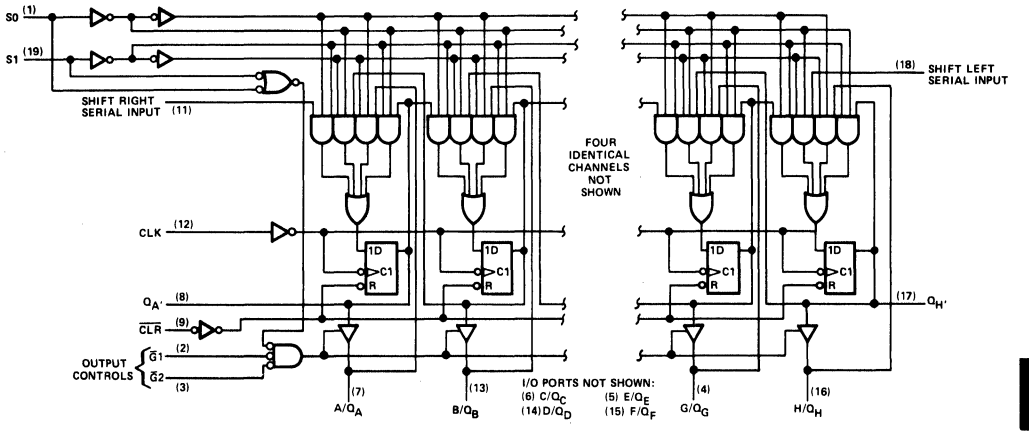
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: ($Q_{A'}$ or $Q_{H'}$) . . . . . 40 mA
SN54F299 (Q_A thru Q_H) . . . . . 40 mA
SN74F299 (Q_A thru Q_H) . . . . . 48 mA
Operating free-air temperature range: SN54F299 . . . . . −55°C to 125°C
SN74F299 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F299			SN74F299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$			−1			−1	mA
		Q_A thru Q_H			−3			−3	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$			20			20	mA
		Q_A thru Q_H			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F299			SN74F299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	Q_A thru Q_H		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Q_A thru Q_H		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	Any other		V_I = 7 V			0.1			0.1	
I_{IH}‡	A thru H	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	Any other					20			20	
I_{IL}‡	A thru H	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	S0 or S1					−1.2			−1.2	
	Any other					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		68	95		68	95	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{G}1$, $\overline{G}2$, and CLK at 4.5 V.

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timing requirements over recommended operating free-air temperature range (see Note 2)

PARAMETER			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F299		SN54F299		SN74F299		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	70	0	65	0	70	MHz
t_{su}	Setup time before CLK↑	S0 or S1 high or low	8.5		9.5		8.5		ns
t_h	Hold time after CLK↑	S0 or S1 high or low	0		0		0		ns
t_{su}	Setup time before CLK↑	A/Q_A thru H/Q_H, SR, or SL high or low	5.5		6.5		5.5		ns
t_h	Hold time after CLK↑	A/Q_A thru H/Q_H, SR, or SL high or low	2		1		2		ns
t_w	Pulse duration	CLK high or low	7		8		7		ns
t_w	Pulse duration	$\overline{CLR}$ low	7		8		7		ns
t_{su}‡	Inactive-state setup time before CLK↑	$\overline{CLR}$ high	7		13		7		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70	100		65		70		MHz
t_{PLH}	CLK	$Q_{A'}$ or $Q_{H'}$	3.2	6.6	9	2.7	10.5	3.2	10	ns
t_{PHL}			2.7	6.1	8.5	2.2	10	2.7	9.5	
t_{PLH}	CLK	Q_A thru Q_H	3.2	6.6	9	2.7	11	3.2	10	ns
t_{PHL}			4.2	8.1	11	3.7	12.5	4.2	12	
t_{PHL}	$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q_A thru Q_H	5.7	10.6	14	5	15.5	5.7	15	
t_{PZH}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	2.7	5.6	8	2.2	10.5	2.7	9	ns
t_{PZL}			3.2	6.6	10	2.7	12	3.2	11	
t_{PHZ}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	1.7	4.1	6	1.7	9	1.7	7	ns
t_{PLZ}			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Inactive-state setup time is also referred to as "recovery time".
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **Operates with Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can be Cascaded for N-Bit Word Lengths**
- **Synchronous Clear**
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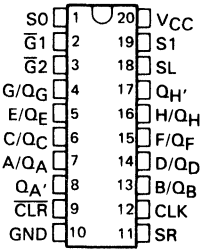
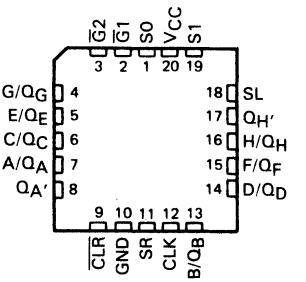
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F323 . . . J PACKAGE
SN74F323 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F323 . . . FK PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when $\overline{CLR}$ is low. Taking either of the output controls $\overline{G1}$ or $\overline{G2}$ high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54F323 is characterized for operation over the full military range of −55°C to 125°C. The SN74F323 is characterized for operation from 0°C to 70°C.

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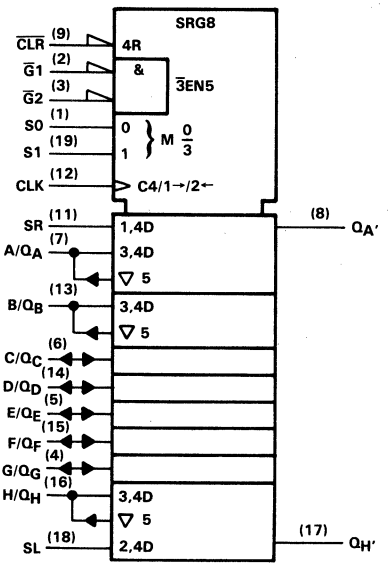
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$†	OUTPUT CONTROL $\overline{G2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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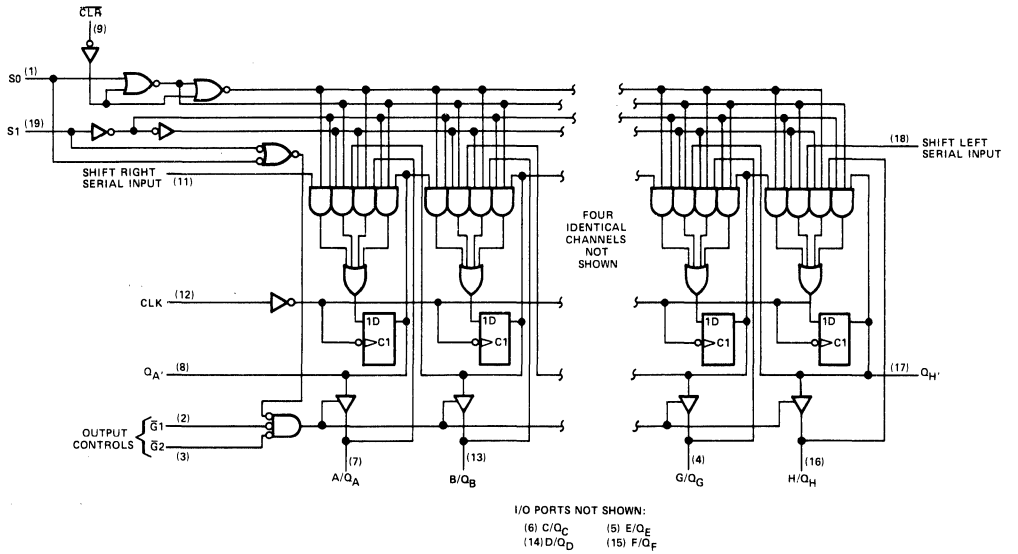
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: ($Q_{A'}$ or $Q_{H'}$) . . . . . 40 mA
SN54F323 (Q_A thru Q_H) . . . . . 40 mA
SN74F323 (Q_A thru Q_H) . . . . . 48 mA
Operating free-air temperature range: SN54F323 . . . . . −55°C to 125°C
SN74F323 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F323			SN74F323			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$			−1			−1	mA
		Q_A thru Q_H			−3			−3	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$			20			20	mA
		Q_A thru Q_H			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F323			SN74F323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
	Q_A thru Q_H		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Q_A thru Q_H		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	Any other		V_I = 7 V			0.1			0.1	
I_{IH}‡	A thru H	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	
	Any other					20			20	
I_{IL}‡	A thru H	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	S0 or S1					−1.2			−1.2	
	Any other					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = MAX,	See Note 1		68	95		68	95	mA

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ No more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{G}1$, $\overline{G}2$, and CLK at 4.5 V.

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timing requirements over recommended operating free-air temperature range (see Note 2)

PARAMETER			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F323			SN54F323		SN74F323		
			MIN		MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		70			0	70	MHz
t_{su}	Setup time before CLK↑	S0 or S1 high or low	8.5					8.5		ns
t_h	Hold time after CLK↑	S0 or S1 high or low	0					0		ns
t_{su}	Setup time before CLK↑	A/Q_A thru H/Q_H, SR, or SL high or low	5					5		ns
t_h	Hold time after CLK↑	A/Q_A thru H/Q_H, SR, or SL high or low	2					2		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$ high or low	10					10		ns
t_h	Hold time after CLK↑	$\overline{CLR}$ high or low	0					0		ns
t_w	Pulse duration	CLK high or low	7					7		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F323			SN54F323		SN74F323		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70	100				70		MHz
t_{PLH}	CLK	Q_A' or Q_H'	3.2	6.6	9			3.2	10	ns
t_{PHL}			2.7	6.1	8.5			2.7	9.5	
t_{PLH}	CLK	Q_A thru Q_H	3.2	6.6	9			3.2	10	ns
t_{PHL}			4.2	8.1	11			4.2	12	
t_{PZH}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	2.7	5.6	8			2.7	9	ns
t_{PZL}			3.2	6.6	10			3.2	11	
t_{PHZ}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	1.7	4.1	6			1.7	7	ns
t_{PLZ}			1.2	3.6	5.5			1.2	6.5	

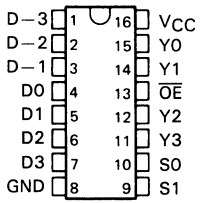
PRODUCT PREVIEW

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

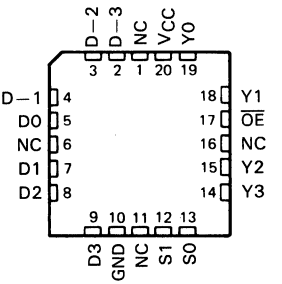
D2932, MARCH 1987– REVISED JANUARY 1989

- **Shifts 4-Bits of Data to 0, 1, 2 or 3 Places Under Control of Two Select Lines**
- **Three-State Outputs for Bus Organized Systems**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F350 . . . J PACKAGE
SN74F350 . . . D OR N PACKAGE
(TOP VIEW)



SN54F350 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

This device is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes shifts of the data word. This makes it possible to perform shifts of 0, 1, 2, or 3 places on words of any length, with suitable interconnection.

A 7-bit data word is introduced at the D inputs and is shifted according to the code applied to the select inputs S0 and S1. Y0 through Y3 are 3-state outputs controlled by an output enable, $\overline{OE}$. When $\overline{OE}$ is low, the outputs follow the selected data inputs; when $\overline{OE}$ is high, the outputs are in a high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical with zeroes pulled in at either or both ends of the shifting field, arithmetic with the sign bit repeated during a shift down, or end-around with the data word forming a continuous loop.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	S1	S0	Y0	Y1	Y2	Y3
H	X	X	Z	Z	Z	Z
L	L	L	D0	D1	D2	D3
L	L	H	D–1	D0	D1	D2
L	H	L	D–2	D–1	D0	D1
L	H	H	D–3	D–2	D–1	D0

logic equations

$$Y0 = \overline{S0}\,\overline{S1}\,D0 + S0\,\overline{S1}\,D{-}1 + \overline{S0}\,S1\,D{-}2 + S0\,S1\,D{-}3$$
$$Y1 = \overline{S0}\,\overline{S1}\,D1 + S0\,\overline{S1}\,D0 + \overline{S0}\,S1\,D{-}1 + S0\,S1\,D{-}2$$
$$Y2 = \overline{S0}\,\overline{S1}\,D2 + S0\,\overline{S1}\,D1 + \overline{S0}\,S1\,D0 + S0\,S1\,D{-}1$$
$$Y3 = \overline{S0}\,\overline{S1}\,D3 + S0\,\overline{S1}\,D2 + \overline{S0}\,S1\,D1 + S0\,S1\,D0$$

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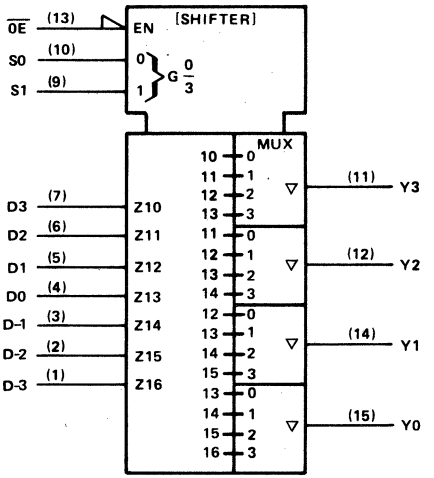
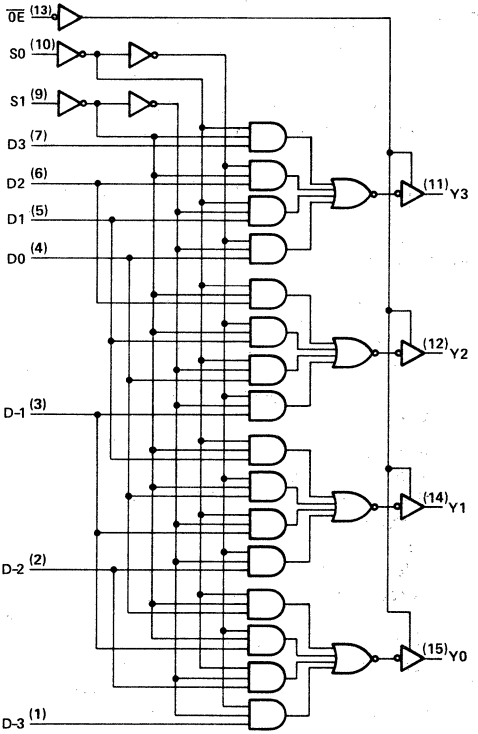
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F350 . . . . . 40 mA
SN74F350 . . . . . 48 mA
Operating free-air temperature range: SN54F350 . . . . . −55°C to 125°C
SN74F350 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F350			SN74F350			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characterisitcs over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F350			SN74F350			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA		2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA		2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V,	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA			0.30	0.5				V
		I_{OL} = 24 mA						0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				−1.2			−1.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0		−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V	Outputs high			22	35		22	35	mA
I_{CCL}		Outputs low			27	41		27	41	
I_{CCZ}		Outputs off			26	42		26	42	

switching characteristics (see Note 1)

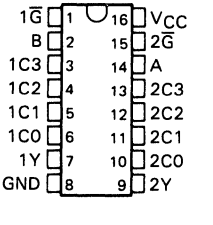
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'F350			SN54F350		SN74F350		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data	Any Y	2.2	4.1	6	3	7.5	2.2	7	ns
t_{PHL}	Any D		1.7	3.6	5.5	2.5	7	1.7	6.5	
t_{PLH}	S0, S1	Any Y	3.2	7.4	10	4	13	3.2	11	ns
t_{PHL}			2.2	6.1	8.5	3	10	2.2	9.5	
t_{PZH}	$\overline{OE}$	Any Y	1.7	4.6	7	2.5	8.5	1.7	8	ns
t_{PZL}			3.2	6.6	9	4	11	3.2	10	
t_{PHZ}	$\overline{OE}$	Any Y	1.2	3.5	5.5	2	7	1,2	6.5	ns
t_{PLZ}			1.2	3.6	5.5	2	8.5	1.2	6.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

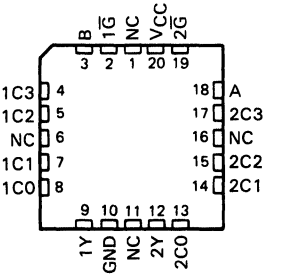
D2932, MARCH 1987—REVISED JANUARY 1989

- **Inverting Versions of SN54F153 and SN74F153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F352 . . . J PACKAGE
SN74F352 . . . D OR N PACKAGE
(TOP VIEW)



SN54F352 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

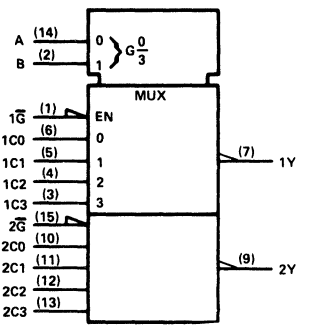
The SN54F352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F352 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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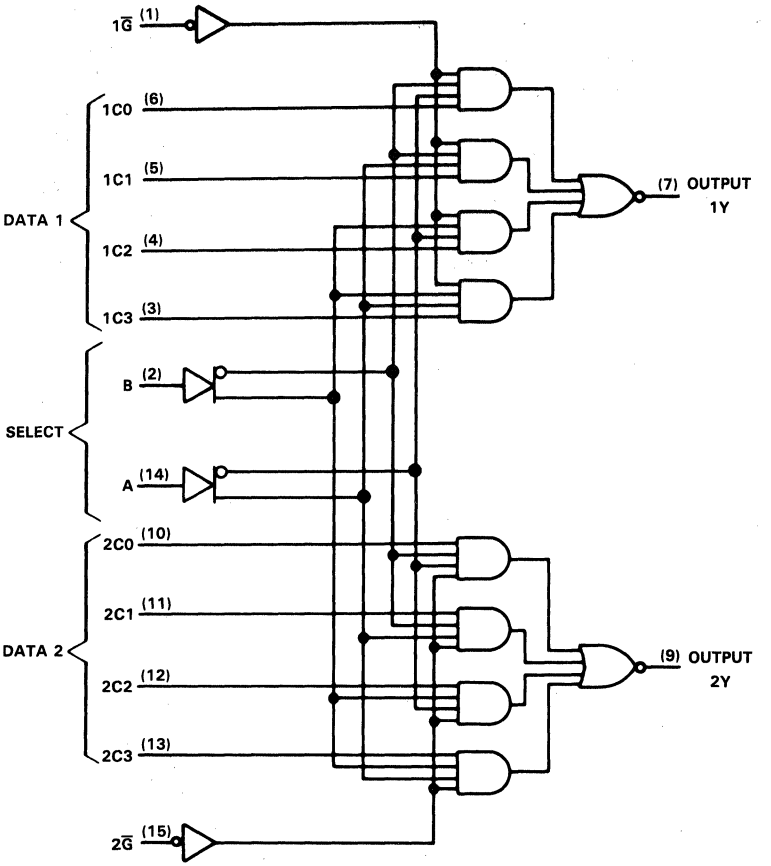
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F352 . . . . . −55°C to 125°C
SN74F352 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F352			SN74F352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F352			SN74F352			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,			9.3	14		9.3	14	mA
I_{CCL}	V_{CC} = 5.5 V,			13.3	20		13.3	20	

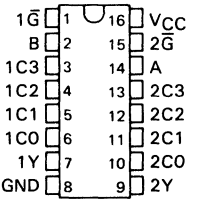
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F352			SN54F352		SN74F352		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.7	7.6	11	2.2	14	2.2	12.5	ns
t_{PHL}			2.2	6.1	8.5	1.7	11	1.7	9.5	
t_{PLH}	G	Y	1.7	4.1	6	1.2	8	1.2	7	ns
t_{PHL}			2.2	4.6	7	1.7	9	1.7	8	
t_{PLH}	Data	Y	1.7	4.8	7	1.2	9	1.2	8	ns
t_{PHL}	(Any C)		1	2.1	3.5	1	5	1	4	

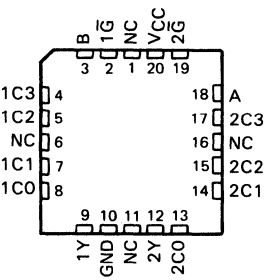
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

- **Inverting Versions of SN54F253 and SN74F253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F353 . . . J PACKAGE
SN74F353 . . . D OR N PACKAGE
(TOP VIEW)



SN54F353 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

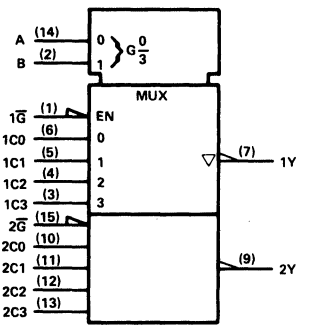
The SN54F353 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F353 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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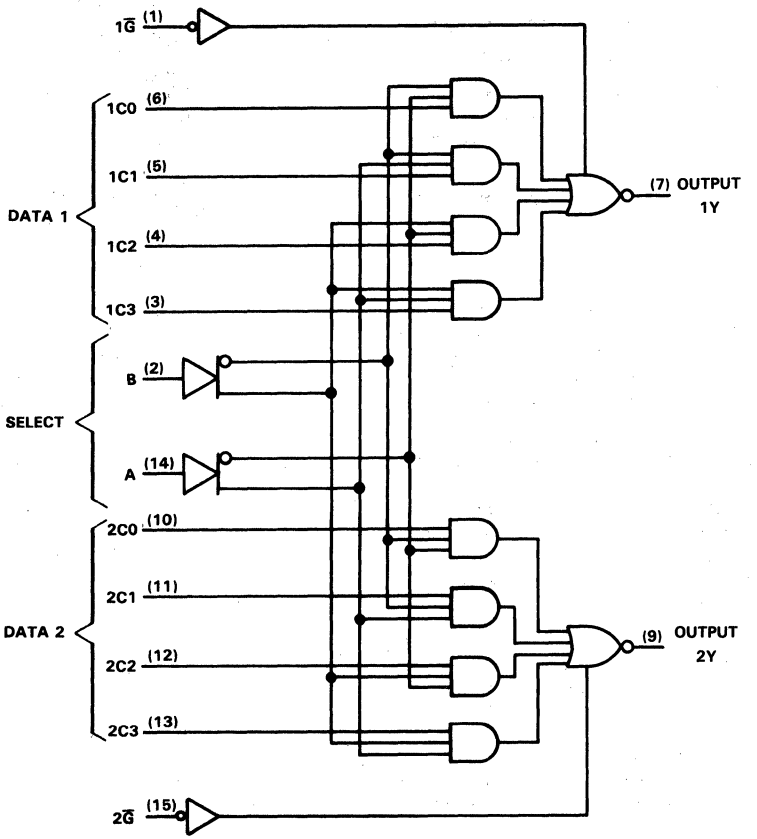
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F353 . . . . . 40 mA
SN74F353 . . . . . 48 mA
Operating free-air temperature range: SN54F353 . . . . . −55°C to 125°C
SN74F353 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F353			SN74F353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54F353			SN74F353			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.30	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH} (see Note 1)	V_{CC} = 5.5 V,	Condition A		9.3	14		9.3	14	mA
I_{CCL}	V_{CC} = 5.5 V,	Condition B		13.3	20		13.3	20	
I_{CCZ}	V_{CC} = 5.5 V,	Condition C		15	23		15	23	

PRODUCT PREVIEW

† For conditions shown as MIN or 5.5 V, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with the outputs open under the following conditions:
A. All inputs grounded.
B. Output control grounded, other inputs at 4.5 V.
C. Output control at 4.5 V, other inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F353			SN54F353		SN74F353		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2.7	7.6	11	2.2	14	2.2	12.5	ns
t_{PHL}			2.2	6.1	8.5	1.7	11	1.7	9.5	
t_{PLH}	Data (Any C)	Any Y	1.7	4.8	7	1.2	9	1.2	8	ns
t_{PHL}			1	2.1	3.5	1	5	1	4	
t_{PZH}	$\overline{G}$	Any Y	2.2	5.1	8	2.2	10.5	2.2	9	ns
t_{PZL}			2.7	5.6	8	2.2	10.5	2.2	9	
t_{PLZ}	$\overline{G}$	Any Y	1.2	3.3	5	1.2	7	1	6	ns
t_{PHZ}			1.2	4	6	1	8	1	7	

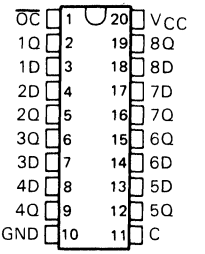
PRODUCT PREVIEW

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

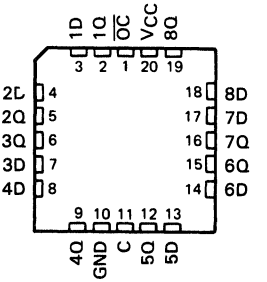
NOTE 2: Load circuits and waveforms are shown in Section 1.

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54F373 . . . J PACKAGE
SN74F373 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F373 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'F373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54F373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	ENABLE C		D	Q
L	H		H	H
L	H		L	L
L	L		X	Q_0
H	X		X	Z

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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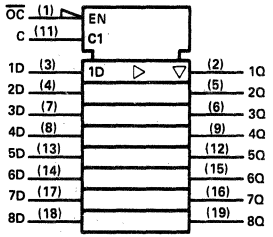
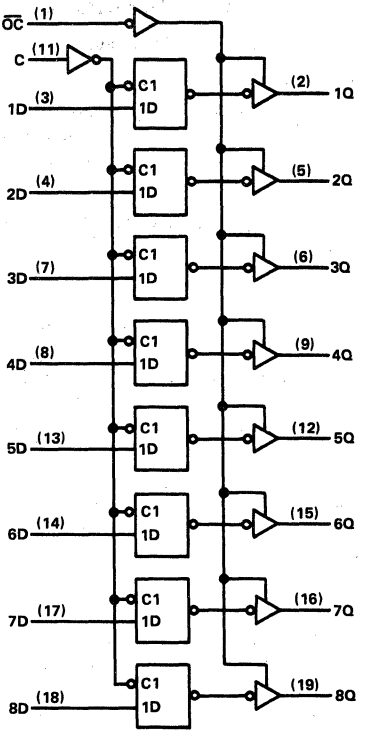
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F373 . . . . . 40 mA
SN74F373 . . . . . 48 mA
Operating free-air temperature range: SN54F373 . . . . . −55°C to 125°C
SN74F373 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F373			SN74F373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F373			SN74F373			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
	V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,		See Note 1		38	55		38	55	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ at 4.5 V and all other inputs grounded.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'F373		SN54F373		SN74F373		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, Data before Enable C↓	2		2		2		ns
t_h	Hold time, Data before Enable C↓	3		3		3		ns
t_w	Pulse duration, Enable C high	6		6		6		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F373			SN54F373		SN74F373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.2	4.9	7	2.2	8.5	2.2	8	ns
t_{PHL}			1.2	3.3	5	1.2	7	1.2	6	
t_{PLH}	C	Q	4.2	8.6	11.5	4.2	15	4.2	13	ns
t_{PHL}			2.2	4.8	7	2.2	8.5	2.2	8	
t_{PZH}	$\overline{OC}$	Q	1.2	4.6	11	1.2	13.5	1.2	12	ns
t_{PZL}			1.2	5.2	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.1	6.5	1.2	10	1.2	7.5	ns
t_{PLZ}			1.2	3.4	6	1.2	7	1.2	6	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2932, MARCH 1987—REVISED JANUARY 1989

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

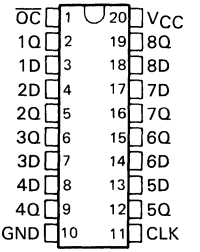
The eight flip-flops of the 'F374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

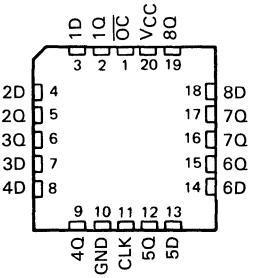
The output control does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54F374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F374 is characterized for operation from 0°C to 70°C.

SN54F374 . . . J PACKAGE
SN74F374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F374 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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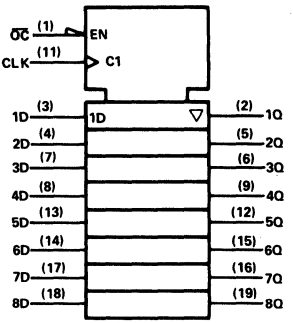
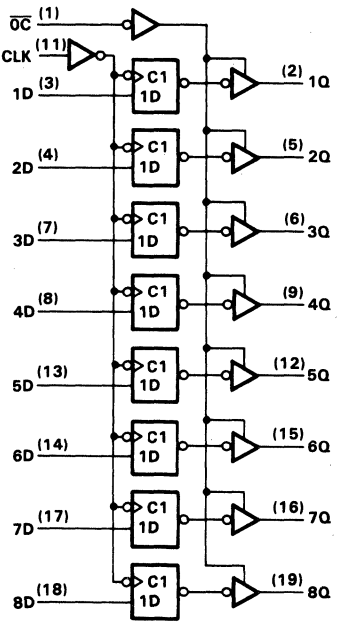
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F374 . . . . . 40 mA
SN74F374 . . . . . 48 mA
Operating free-air temperature range: SN54F374 . . . . . −55°C to 125°C
SN74F374 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F374			SN74F374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F374			SN74F374			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,		See Note 1		55	86		55	86	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{OC}$ at 4.5 V and the data inputs grounded.

timing requirements

PARAMETER			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F374		SN54F374		SN74F374		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	60	0	70	MHz
t_{su}	Setup time before CLK↑	Data high	2		2.5		2		ns
		Data low	2		2		2		
t_h	Hold time after CLK↑	Data high	2		2		2		ns
		Data low	2		2.5		2		
t_w	Pulse duration	CLK high	7		7		7		ns
		CLK low	6		6		6		

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F374			SN54F374		SN74F374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	Q	3.2	6.1	8.5	3.2	10.5	3.2	10	ns
t_{PHL}			3.2	6.1	8.5	3.2	11	3.2	10	
t_{PZH}	$\overline{OC}$	Q	1.2	8.6	11.5	1.2	14	1.2	12.5	ns
t_{PZL}			1.2	5.4	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.9	7	1.2	8	1.2	8	ns
t_{PLZ}			1.2	3.9	5.5	1.2	7.5	1.2	6.5	

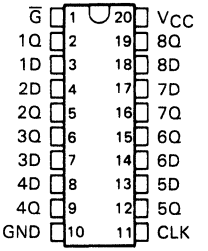
† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

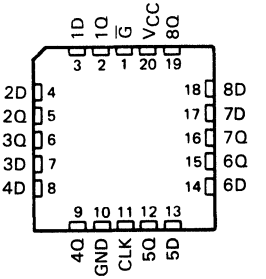
D2932, MARCH 1987—REVISED JANUARY 1989

- **Contains Eight D-Type Flip-Flops with Single-Rail Outputs**
- **Buffered Common Enable Input**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Register
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F377 . . . J PACKAGE
SN74F377 . . . D OR N PACKAGE
(TOP VIEW)



SN54F377 . . . FK PACKAGE
(TOP VIEW)



description

The SN54F377 and SN74F377 are monolithic, positive-edge-triggered D-type flip-flops with a clock enable input. The 'F377 is similar to the 'F273, but features a common clock enable instead of a common clear.

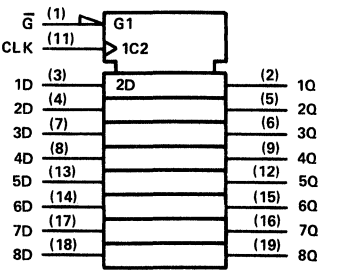
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

The SN54F377 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F377 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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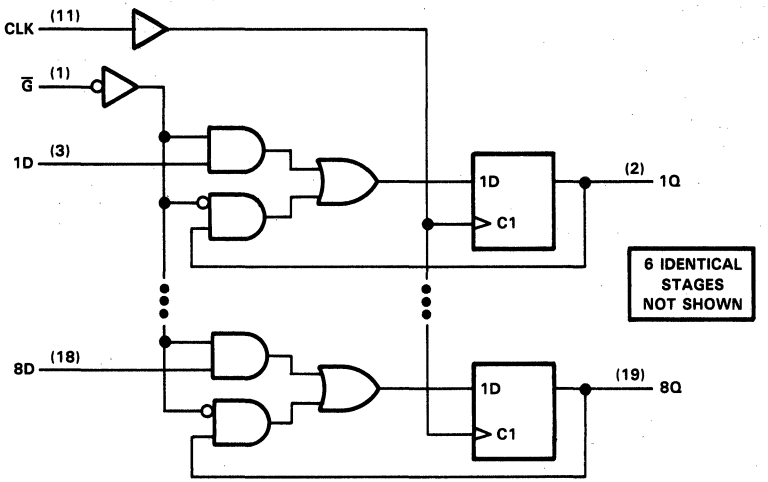
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F377 . . . . . −55°C to 125°C
SN74F377 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F377			SN74F377			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F377			SN74F377			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 1		55	72		55	72	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 2		70	90		70	90	mA

timing requirements

			V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			'F377	SN54F377	SN74F377	
			MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency					MHz
t_{su}	Setup time before CLK↑	Data high or low	2			ns
t_h	Hold time after CLK↑	Data high or low	0			ns
t_{su}	Setup time before CLK↑	$\overline{G}$ high	2.5			ns
		$\overline{G}$ low	3			
t_h	Hold time after CLK↑	$\overline{G}$ high or low	0			ns
t_w	Pulse duration	CLK low	4			ns

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F377			SN54F377		SN74F377	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				125						MHz
t_{PLH}	CLK	Any Q		6.5						ns
t_{PHL}				7						

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ No more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

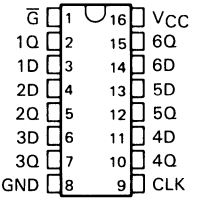
NOTES: 1. I_{CC} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the enable input at ground.
2. I_{CCL} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data and enable inputs at ground.
3. Load circuits and waveforms are shown in Section 1.

D2932, MARCH 1987—REVISED JANUARY 1989

- **Contains Six D-Type Flip-Flops with Single-Rail Outputs**
- **Buffered Common Enable Input**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Register
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

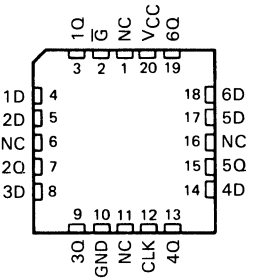
SN54F378 . . . . J PACKAGE
SN74F378 . . . . . D OR N PACKAGE

(TOP VIEW)



SN54F378 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

description

The SN54F378 and SN74F378 are positive-edge-triggered D-type flip-flops with a clock enable input. The 'F378 is similar to the 'F174, but features a common clock enable instead of a common clear.

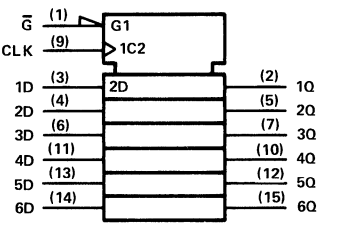
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54F378 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F378 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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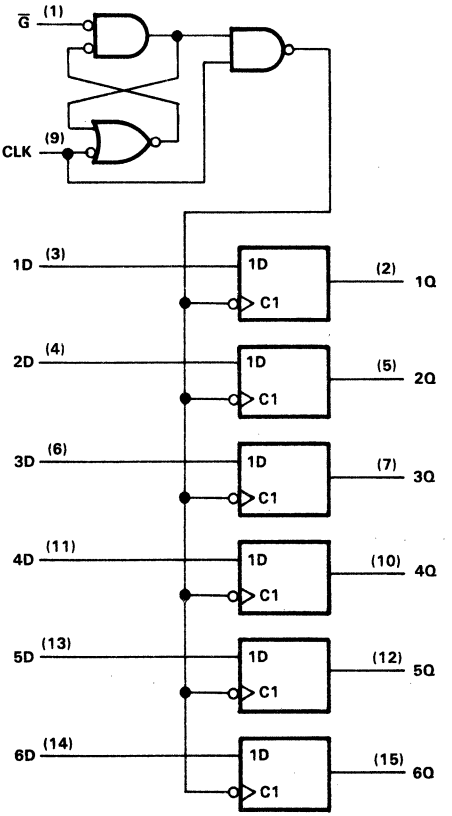
logic diagram



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage†	−1.2 V to 7 V
Input current	−30 mA to 5 mA
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F378	−55°C to 125°C
SN74F378	0°C to 70°C
Storage temperature range	−65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F378			SN74F378			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F378			SN74F378			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		30			30	45	mA

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'F378		SN54F378		SN74F378		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	80	0	70	0	80	MHz
t_{su}	Setup time before CLK↑	Data high or low	4		5		4		ns
t_h	Hold time after CLK↑	Data high or low	0		2		0		ns
t_{su}	Setup time before CLK↑	$\overline{G}$ high	4		4.5		4		ns
		$\overline{G}$ low	10		13		10		
t_h	Hold time after CLK↑	$\overline{G}$ high or low	0		0		0		ns
t_w	Pulse duration	CLK high	4		5		4		ns
		CLK low	6		7.5		6		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: I_{CC} is measured with all outputs open, all data inputs and the enable input grounded, and the CLK input at 4.5 V after being momentarily grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F378			SN54F378		SN74F378		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			80	100				80		MHz
t_{PLH}	CLK	Any Q	2.2	5.1	7.5			2.2	8.5	ns
t_{PHL}			2.7	5.6	8.5			2.7	9.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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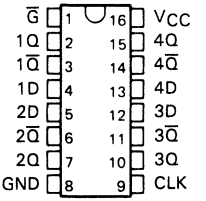
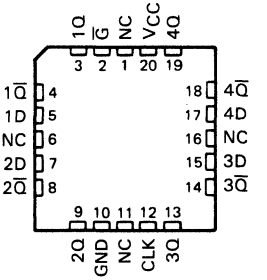
D2932, MARCH 1987—REVISED JANUARY 1989

- **Contains Four D-Type Flip-Flops with Double-Rail Outputs**
- **Buffered Common Enable Input**
- **Applications Include:**
  Buffer/Storage Registers
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F379 . . . J PACKAGE
SN74F379 . . . D OR N PACKAGE
(TOP VIEW)



SN54F379 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54F379 and SN74F379 are monolithic, positive-edge-triggered D-type flip-flops with a clock enable input. The 'F379 is similar to the 'F175, but features a common clock enable instead of a common clear.

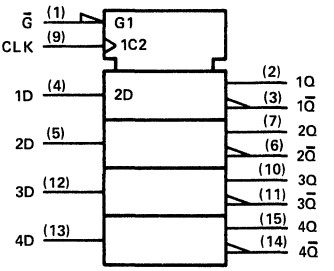
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54F379 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F379 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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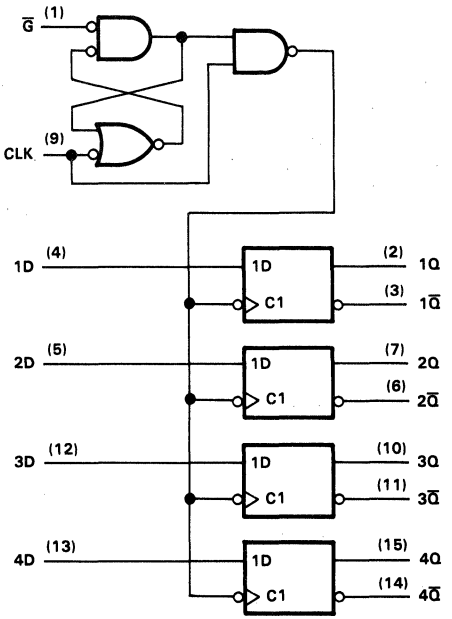
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F379 . . . . . −55°C to 125°C
SN74F379 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F379			SN74F379			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F379			SN74F379			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		28	40		28	40	mA

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
			'F379		SN54F379		SN74F379		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100			0	100	MHz
t_{su}	Setup time before CLK↑	Data high or low	3				3		ns
t_h	Hold time after CLK↑	Data high or low	1				1		ns
t_{su}	Setup time before CLK↑	$\overline{G}$ high or low	6				6		ns
t_h	Hold time after CLK↑	$\overline{G}$ high or low	0				0		ns
t_w	Pulse duration	CLK high	4				4		ns
		CLK low	5				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: I_{CC} is measured with all outputs open, all data inputs and the enable input grounded, and the CLK input at 4.5 V after being momentarily grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F379			SN54F379		SN74F379		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	140				100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3.2	4.6	6.5			3.2	7.5	ns
t_{PHL}			4.2	6.1	8.5			4.2	9.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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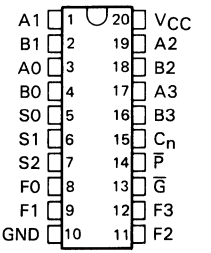
D2932, MARCH 1987—REVISED JUNE 1988

- **Fully Parallel 4-Bit ALUs in 20-Pin Package**
- **Ideally Suited for High-Density Economical Processors**
- **$\overline{G}$ and $\overline{P}$ Outputs for Look-Ahead Carry Cascading**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  - **A Minus B**
  - **B Minus A**
  - **A Plus B**
  - **and Five Other Functions**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

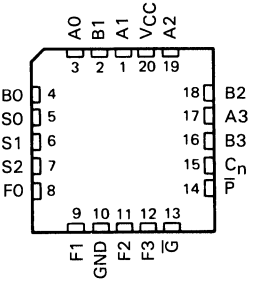
PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$	14	ACTIVE-LOW CARRY PROPAGATE OUTPUT
$\overline{G}$	13	ACTIVE-LOW CARRY GENERATE OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

SN54F381 . . . J PACKAGE
SN74F381 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F381 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

description

The SN54F381 and SN74F381 are arithmetic logic units (ALU)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, and OR functions of the two Boolean variables are provided without the use of external circuits. In addition, the outputs can be cleared (low) or preset (high) as desired. The 'F381 provides two cascade outputs ($\overline{P}$ and $\overline{G}$) for expansion utilizing 'AS182 look-ahead carry generators.

The SN54F381 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F381 is characterized for operation from 0°C to 70°C.

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function table

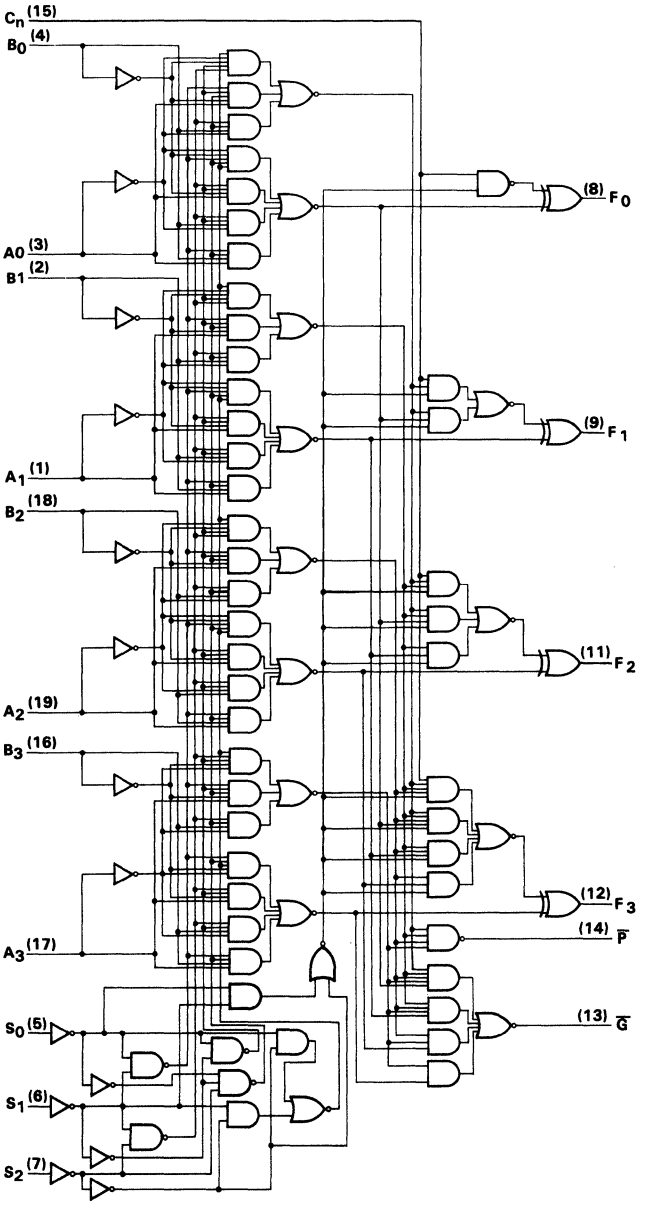
Certain differences exist in the $\overline{G}$ and $\overline{P}$ function table compared with similar parts from other technologies. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions. There are slight differences in the other modes (CLEAR, A + B, A ⊕ B, AB, and PRESET), in which these outputs are strictly "don't care." There are no functional differences between 'F381 parts built by Texas Instruments and Fairchild.

This function table is a condensed version and assumes for A_n that A0, A1, A2, and A3 inputs all agree and for B_n that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these $\overline{G}$ and $\overline{P}$ outputs in all modes of operation to facilitate incoming inspection.

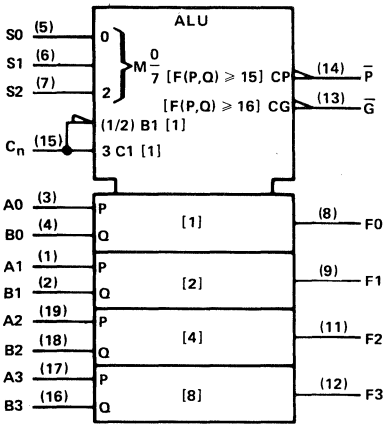
FUNCTION TABLE

ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				$\overline{G}$	$\overline{P}$
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0		
CLEAR	L	L	L	X	X	X	L	L	L	L	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L
				L	L	H	H	H	H	L	L	L
				L	H	L	L	L	L	L	H	H
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	H	H	H	H	L	L
				H	H	L	L	L	L	H	H	H
				H	H	H	L	L	L	L	H	L
A MINUS B	L	H	L	L	L	L	H	H	H	H	H	L
				L	L	H	L	L	L	L	H	H
				L	H	L	H	H	H	L	L	L
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	L	L	L	H	H	H
				H	H	L	H	H	H	H	L	L
				H	H	H	L	L	L	L	H	L
A PLUS B	L	H	H	L	L	L	L	L	L	L	H	H
				L	L	H	H	H	H	H	H	L
				L	H	L	H	H	H	H	H	L
				L	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	H	H	H
				H	L	H	L	L	L	L	H	L
				H	H	L	L	L	L	L	H	L
				H	H	H	H	H	H	H	L	L
A ⊕ B	H	L	L	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	L
				X	H	H	L	L	L	L	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L
AB	H	H	L	X	L	L	L	L	L	L	L	L
				X	L	H	L	L	L	L	H	H
				X	H	L	L	L	L	L	L	L
				X	H	H	H	H	H	H	H	L
PRESET	H	H	H	X	L	L	H	H	H	H	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L

logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F381 . . . . . −55°C to 125°C
SN74F381 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F381			SN74F381			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F381			SN74F381			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −1 mA					2.7			V
	V_{CC} = 4.5 V, I_{OH} = −1 mA		2.5	3.4		2.5	3.4		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V	Any A or B			−2.4			−2.4	mA
		Any S			−0.6			−0.6	
		C_n			−2.4			−2.4	
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1			59	89		59	89	mA

switching characteristics (see Note 2)

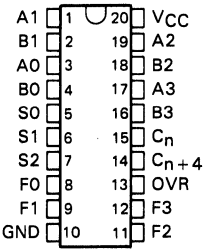
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F381			SN54F381		SN74F381		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	Any F	2.5	5.1	8.5	3	15	2.5	9.5	ns
t_{PHL}			2	4.3	7	2.5	12	2	7.5	
t_{PLH}	Any A or B	Any F	3	6.7	11.5	3.5	19	3	12.5	ns
t_{PHL}			2.5	5.8	9.5	3	16	2.5	10	
t_{PLH}	S0, S1, S2	Any F	3.5	8.1	15	3	16	3.5	16	ns
t_{PHL}			3.5	7.3	14	3	16	3.5	15	
t_{PLH}	Any A or B	$\overline{G}$	2.5	5.2	9	3	13	2.5	10	ns
t_{PHL}			2	4.6	7.5	3	14	2	7.5	
t_{PLH}	Any A or B	$\overline{P}$	2.5	5	9	3	15	2.5	10	ns
t_{PHL}			3.5	6	9	3	13	3.5	9.5	
t_{PLH}	S0, S1, S2	$\overline{G}$ or $\overline{P}$	4.5	7.4	12.5	3	15	4.5	13.5	ns
t_{PHL}			3	6	13	3	19	3	13.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all outputs open, S0, S1 and S2 grounded, and all other inputs at 4.5 V.
2. Load circuits and waveforms are shown in Section 1.

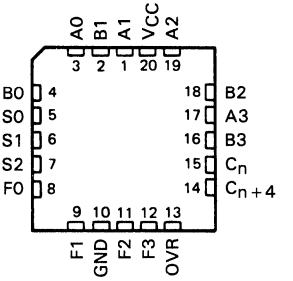
D2932, MARCH 1987—REVISED JANUARY 1989

- **Fully Parallel 4-Bit ALUs in 20-Pin Package**
- **Ideally Suited for High-Density Economical Processors**
- **Ripple Carry (C_n+4) and Overflow (OVR) Outputs**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  - **A Minus B**
  - **B Minus A**
  - **A Plus B**
  - **and Five Other Functions**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F382 . . . J PACKAGE
SN74F382 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F382 . . . FK PACKAGE
(TOP VIEW)



PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
C_{n+4}	14	RIPPLE-CARRY OUTPUT
OVR	13	OVERFLOW OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

description

The SN54F382 and SN74F382 are arithmetic logic units (ALU)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, and OR functions of the two Boolean variables are provided without the use of external circuits. In addition, the outputs can be cleared (low) or preset (high) as desired. The 'F382 provides a C_{n+4} output to ripple the carry to the C_n input of the next stage. The 'F382 detects and indicates the two's complement overflow condition via the OVR output. The overflow output is logically equivalent to $C_{n+3} \oplus C_{n+4}$. When the 'F382 is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54F382 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F382 is characterized for operation from 0°C to 70°C.

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function table

Certain differences exist in the OVR and C_{n+4} function table compared with similar parts from other technologies and other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions. There are slight differences in the other modes (CLEAR, A + B, A ⊕ B, AB, and PRESET), in which these outputs are strictly "don't care." There are no functional differences between 'F382 parts built by Texas Instruments and Fairchild.

This function table is a condensed version and assumes for A_n that A0, A1, A2, and A3 inputs all agree and for B_n that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these OVR and C_{n+4} outputs in all modes of operation to facilitate incoming inspection.

FUNCTION TABLE

ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				OVR	C_{n+4}
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0		
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H
B MINUS A	L	L	H	L	L	L	H	H	H	H	L	L
				L	L	H	H	H	H	L	L	H
				L	H	L	L	L	L	L	L	L
				L	H	H	H	H	H	H	L	L
				H	L	L	L	L	L	L	L	H
				H	L	H	H	H	H	H	L	H
				H	H	L	L	L	L	H	L	L
				H	H	H	L	L	L	L	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	L	L
				L	L	H	L	L	L	L	L	L
				L	H	L	H	H	H	L	L	H
				L	H	H	H	H	H	H	L	L
				H	L	L	L	L	L	L	L	H
				H	L	H	L	L	L	H	L	L
				H	H	L	H	H	H	H	L	H
				H	H	H	L	L	L	L	L	H
A PLUS B	L	H	H	L	L	L	L	L	L	L	L	L
				L	L	H	H	H	H	H	L	L
				L	H	L	H	H	H	H	L	L
				L	H	H	H	H	H	L	L	H
				H	L	L	L	L	L	H	L	L
				H	L	H	L	L	L	L	L	H
				H	H	L	L	L	L	L	L	H
				H	H	H	H	H	H	H	L	H
A ⊕ B	H	L	L	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				L	H	L	H	H	H	H	L	L
				H	H	L	H	H	H	H	H	H
				X	H	H	L	L	L	L	H	H
A + B	H	L	H	X	L	L	L	L	L	L	L	L
				X	L	H	H	H	H	H	L	L
				X	H	L	H	H	H	H	L	L
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H
AB	H	H	L	X	L	L	L	L	L	L	H	H
				X	L	H	L	L	L	L	L	L
				X	H	L	L	L	L	L	H	H
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H
PRESET	H	H	H	X	L	L	H	H	H	H	L	L
				X	L	H	H	H	H	H	L	L
				X	H	L	H	H	H	H	L	L
				L	H	H	H	H	H	H	L	L
				H	H	H	H	H	H	H	H	H

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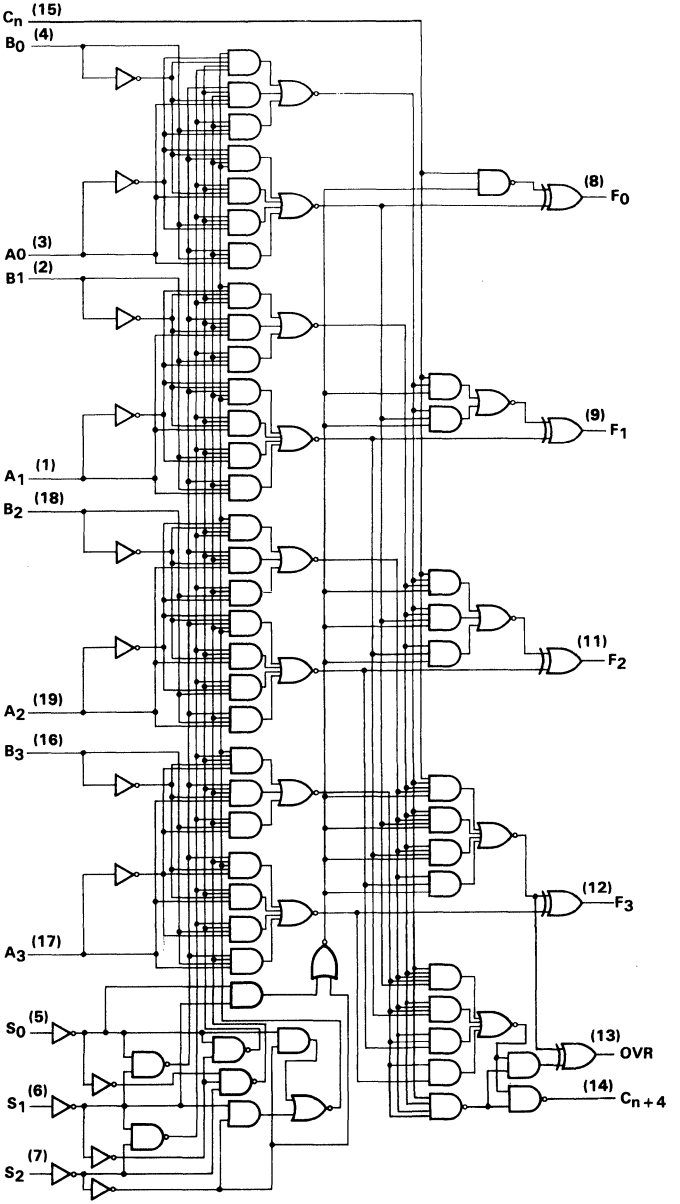
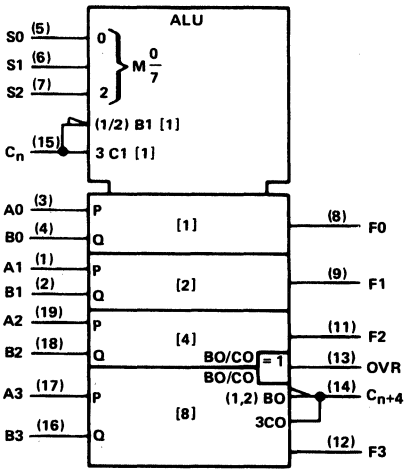
logic diagram (positive logic)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F382 . . . . . −55°C to 125°C
SN74F382 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F382			SN74F382			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F382			SN74F382			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −1 mA		2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V, I_{OH} = −1 mA					2.7			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V	Any A or B			−2.4			−2.4	mA
		Any S			−0.6			−0.6	
		C_n			−3			−3	
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1			54	81		54	81	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F382			SN54F382		SN74F382		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	C_n	Any F	2.3	5.3	11			2.3	12	ns
t_{PHL}			2.2	4.6	7.5			2.2	8.5	
t_{PLH}	Any A or B	Any F	2.7	6.9	12			2.4	13	ns
t_{PHL}			2.5	6.1	10			2.3	11	
t_{PLH}	S0, S1, S2	Any F	4.7	8.3	15			4.3	17	ns
t_{PHL}			3.3	7.5	14			3.3	15	
t_{PLH}	Any A or B	C_{n+4}	3.3	6.6	10			3.3	11	ns
t_{PHL}			3.4	6.3	10			3	10.5	
t_{PLH}	S0, S1, S2	OVR or C_{n+4}	3.6	9.8	16.5			3	17.5	ns
t_{PHL}			5	8.6	13			4.6	14	
t_{PLH}	C_n	C_{n+4}	2.2	3.9	5.5			2	6.5	ns
t_{PHL}			3	4.8	6.5			2.6	7.5	
t_{PLH}	C_n	OVR	3.3	7	11			3	12.5	ns
t_{PHL}			3	5	6.5			3	8	
t_{PLH}	Any A or B	OVR	5.1	8.8	13			4.7	15	ns
t_{PHL}			3.3	6.9	10.5			3.3	11.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all outputs open, SO and C_n inputs at 4.5 V, and all other inputs grounded.
2. Load circuits and waveforms are shown in Section 1.

PRODUCT PREVIEW

D2932, MARCH 1987—REVISED JANUARY 1989

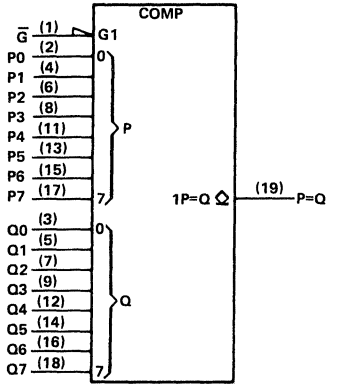
- Compares Two 8-Bit Words
- 'F518 Has 20-kΩ Pull-up Resistors on Q Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These identity comparators perform comparisons on two eight-bit binary or BCD words. The 'F518 and F519 provide P = Q open-collector outputs. The 'F518 devices feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

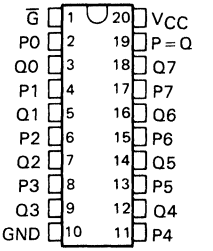
The SN54F518 and SN54F519 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F518 and SN74F519 are characterized for operation from 0°C to 70°C.

logic symbol†

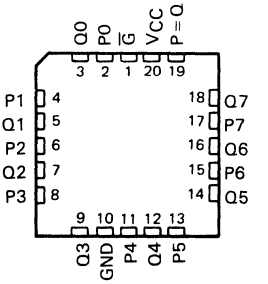


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54F518, SN54F519 . . . J PACKAGE
SN74F518, SN74F519 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F518, SN54F519 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	P = Q
P = Q	L	H
P ≠ Q	X	L
X	H	L

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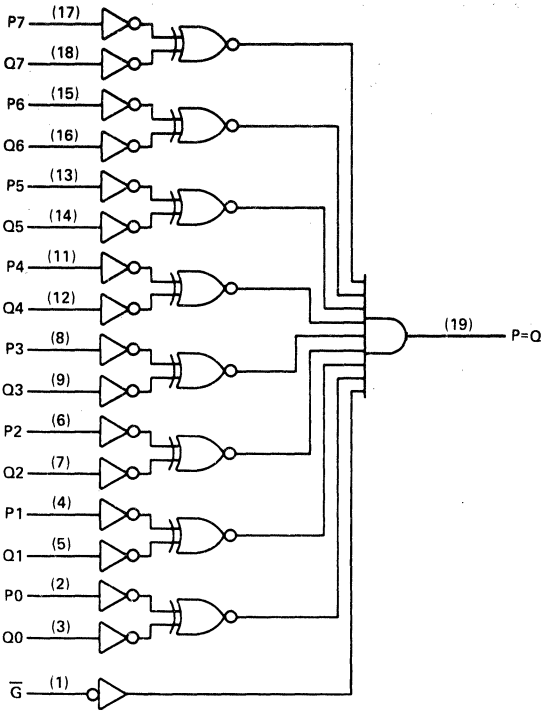
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to 5.5 V
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F518, SN54F519 . . . . . −55°C to 125°C
SN74F518, SN74F519 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F518			SN74F518			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F518			SN74F518			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Q inputs					−0.3			−0.3	mA
I_{IL}	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	Q inputs					−1			−1	
I_{CC}		V_{CC} = 5.5 V,	See Note 1		24	39		24	39	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			'F518			SN54F518		SN74F518		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	P = Q	4	11.5	14.5	4	15.5	4	10	ns
t_{PHL}			2	6.2	9	2	11.5	2	10	
t_{PLH}	$\overline{G}$	P = Q	4.5	11.5	14	4.5	15.5	4.5	14.5	ns
t_{PHL}			2	5.1	6.5	2	9.5	2	7.5	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all inputs at 4.5 V.
2. Load circuits and waveforms are shown in Section 1.

recommended operating conditions

		SN54F519			SN74F519			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F519			SN74F519			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.30	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		24	39		24	39	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡			UNIT
			'F519			SN54F519		SN74F519	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	P = Q	4	11.5	14.5	4	15.5	4	15	ns
t_{PHL}			2	6.2	9	2	11.5	2	10	
t_{PLH}	$\overline{G}$	P = Q	4.5	11.5	14	4.5	15.5	4.5	14.5	ns
t_{PHL}			2	5.1	6.5	2	9.5	2	7.5	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with inputs at 4.5 V.
2. Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2932, MARCH 1987—REVISED JANUARY 1989

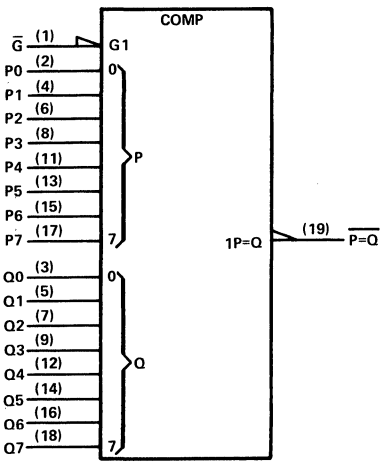
- **Compares Two 8-Bit Words**
- **'F520 has 20-kΩ Pull-up Resistors on Q Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These identity comparators perform comparisons on two eight-bit binary or BCD words. The 'F520 and F521 provide $\overline{P=Q}$ outputs. The 'F520 devices feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

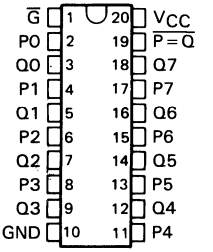
The SN54F520 and SN54F521 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F520 and SN74F521 are characterized for operation from 0°C to 70°C.

logic symbol†

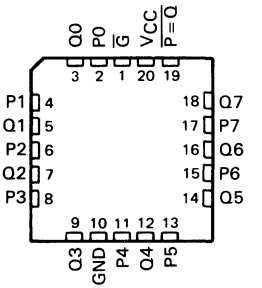


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54F520, SN54F521 . . . J PACKAGE
SN74F520, SN74F521 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F520, SN54F521 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	X	H
X	H	H

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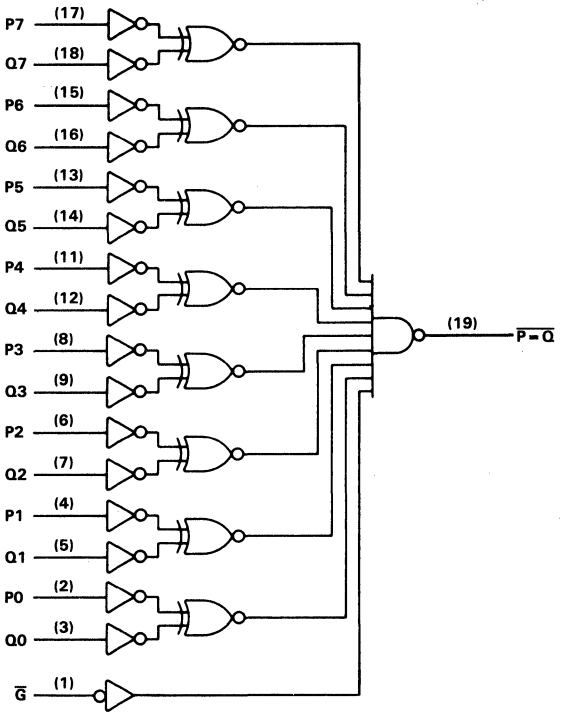
logic diagram (positive logic)



NOTE: The 'F520 has a 20-kΩ pullup resistors on the Q inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F520, SN54F521 . . . . . −55°C to 125°C
SN74F520, SN74F521 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F520			SN74F520			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		SN54F520			SN74F520			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.30	0.5		0.3	0.5	V
I_I	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Q inputs					−0.3			−0.3	mA
I_{IL}	$\overline{G}$ and P inputs	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	Q inputs					−1			−1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		21	32		21	32	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F520			SN54F520		SN74F520		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	3.9	5.7	7.7	3.7	10.2	3.7	8.7	ns
t_{PHL}			4.7	7	9.3	4.4	11.3	4.4	10.3	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	3.5	4.6	5.8	3.4	7	3.4	6.4	ns
t_{PHL}			5.2	7.5	9.5	4.9	11.2	4.9	10.4	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all inputs at 4.5 V.
2. Load circuits and waveforms are shown in Section 1.

recommended operating conditions

		SN54F521			SN74F521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F521			SN74F521			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			100			100	μA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		21	32		21	32	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§			UNIT
			'F521			SN54F521		SN74F521	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	2.7	6.6	10	2.7	15	2.7	11	ns
t_{PHL}			3.7	6.6	10	3.2	12	3.2	11	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	2.2	4.6	6.5	2.2	8.5	2.2	7.5	ns
t_{PHL}			2.7	6.1	9	2.7	13.5	2.7	10	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTES: 1. I_{CC} is measured with all inputs at 4.5 V.
2. Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

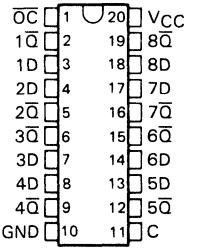
The eight latches of the 'F533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'F533 is functionally equivalent to the 'F373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

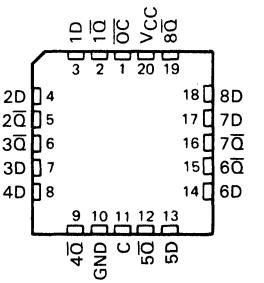
The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54F533 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F533 is characterized for operation from 0°C to 70°C.

SN54F533 . . . J PACKAGE
SN74F533 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F533 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

2 Data Sheets

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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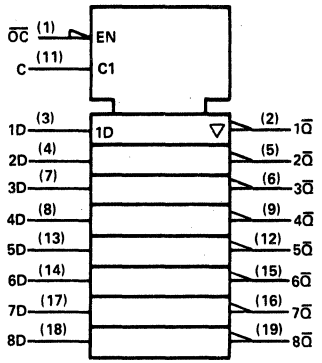
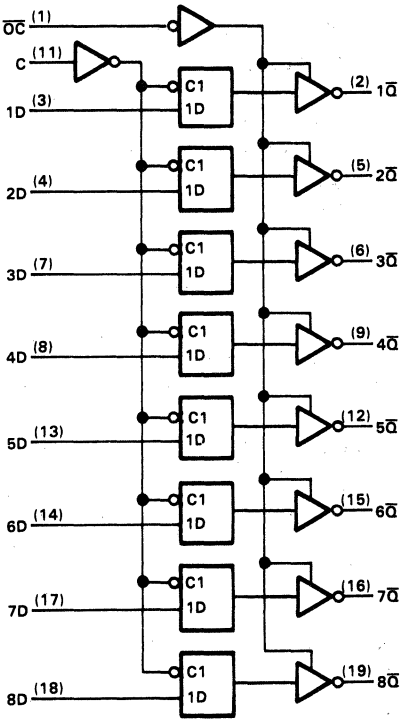
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 to V_{CC}
Current into any output in the low state: SN54F533 . . . . . 40 mA
SN74F533 . . . . . 48 mA
Operating free-air temperature range: SN54F533 . . . . . −55°C to 125°C
SN74F533 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F533			SN74F533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F533			SN74F533			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,		I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,		V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,		V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,		V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,		V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,		V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,		See Note 1		41	61		41	61	mA

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{OC}$ at 4.5 V, all other inputs grounded.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F533		SN54F533		SN74F533		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time before enable C↓	Data high or low	2		2		2		ns
t_h	Hold time after enable C↓	Data high or low	3		3		3		ns
t_w	Pulse duration	Enable C high	6		6		6		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F533			SN54F533		SN74F533		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Any $\overline{Q}$	3.2	6.5	9	3.2	12	3.2	10	ns
t_{PHL}			2.2	4.8	7	2.2	9	2.2	8	
t_{PLH}	C	Any $\overline{Q}$	4.2	8.1	11	4.2	14	4.2	13	ns
t_{PHL}			2.2	5.2	7	2.2	9	2.2	8	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.2	7.3	10	1.2	12.5	1.2	11	ns
t_{PZL}			1.2	4.7	6.5	1.2	9	1.2	7.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.2	4.3	6	1.2	8.5	1.2	7	ns
t_{PLZ}			1.2	3.7	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'F534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs. The 'F534 is equivalent to the 'F374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

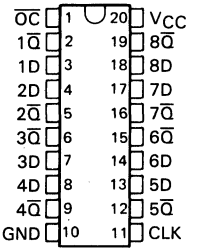
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54F534 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F534 is characterized for operation from 0°C to 70°C.

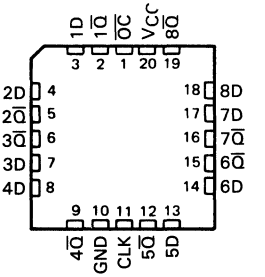
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

SN54F534 . . . J PACKAGE
SN74F534 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F534 . . . FK PACKAGE
(TOP VIEW)



2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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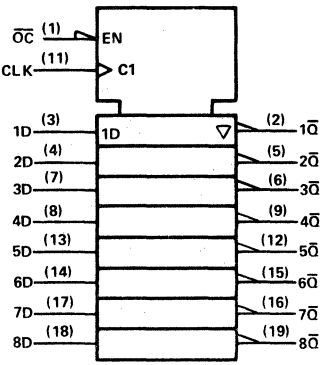
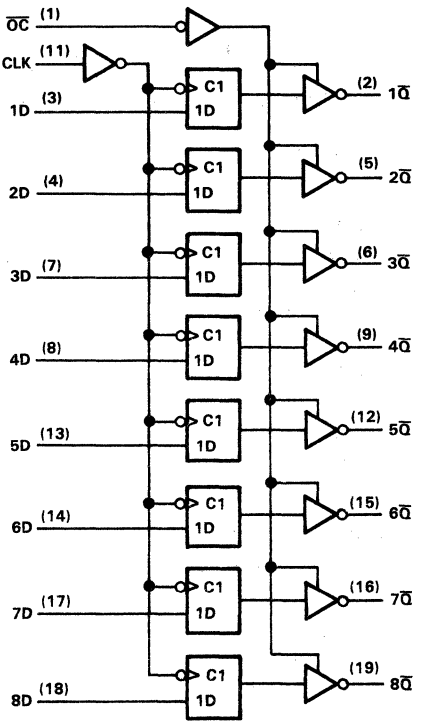
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F534 . . . . . 40 mA
SN74F534 . . . . . 48 mA
Operating free-air temperature range: SN54F534 . . . . . −55°C to 125°C
SN74F534 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F534			SN74F534			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F534			SN74F534			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		55	86		55	86	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with $\overline{OC}$ at 4.5 V, all other inputs grounded.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Note 2)

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F534			SN54F534		SN74F534		
			MIN		MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		100	0	60	0	70	MHz
t_{su}	Setup time before CLK↑	Data high	2			2.5		2		ns
		Data low	2			2		2		
t_h	Hold time after CLK↑	Data high	2			2		2		ns
		Data low	2			2.5		2		
t_w	Pulse duration	CLK high	7			7		7		ns
		CLK low	6			6		6		

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F534			SN54F534		SN74F534		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	Q	3.2	6.1	8.5	3.2	10.5	3.2	10	ns
t_{PHL}			3.2	6.1	8.5	3.2	11	3.2	10	
t_{PZH}	$\overline{OC}$	Q	1.2	8.6	11.5	1.2	14	1.2	12.5	ns
t_{PZL}			1.2	5.4	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.9	7	1.2	8	1.2	8	ns
t_{PLZ}			1.2	3.9	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed to have the performance of the popular SN54F240/SN74F240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

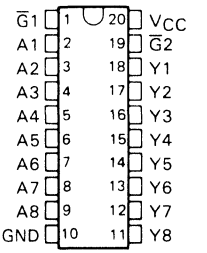
The SN54F540 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F540 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

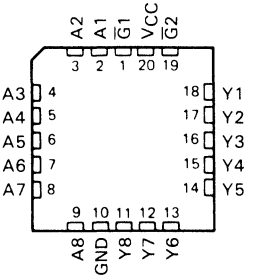
INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

SN54F540 . . . J PACKAGE
SN74F540 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F540 . . . FK PACKAGE
(TOP VIEW)



2 Data Sheets

PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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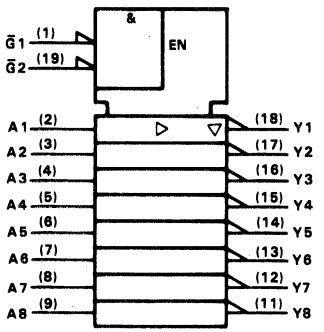
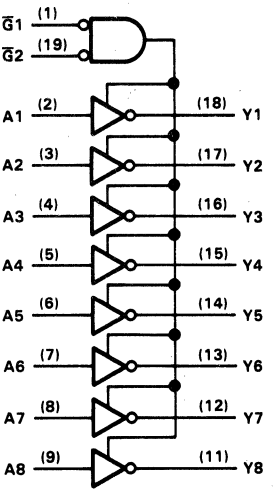
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F540 . . . . . 96 mA
SN74F540 . . . . . 128 mA
Operating free-air temperature range: SN54F540 . . . . . −55°C to 125°C
SN74F540 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F540			SN74F540			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F540			SN74F540			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
	V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		59	75		59	75	mA
		Outputs low		12	20		12	20	
		Outputs disabled		35	45		35	45	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§			UNIT
			'F540			SN54F540		SN74F540	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data	Y	1	2.6	5	1	6	1	5.5	ns
t_{PHL}	(Any A)		1	1.6	4	1	4.5	1	4	
t_{PZH}	$\overline{G}$	Y	1.7	4.5	8	1.7	9	1.7	8.5	ns
t_{PZL}			2.7	5.4	10	2.7	11	2.7	10.5	
t_{PHZ}	$\overline{G}$	Y	1	3	6	1	7	1	6.5	ns
t_{PLZ}			1	2.1	5.6	1	7.5	1	6	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D3126, JANUARY 1989

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed to have the performance of the popular SN54F240/SN74F240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

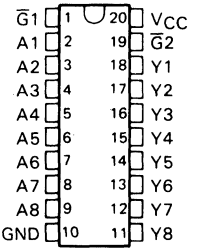
The SN54F541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F541 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

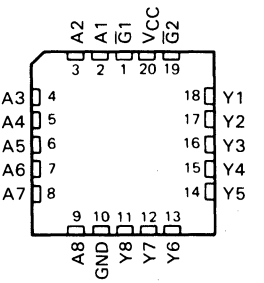
INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance

SN54F541 . . . J PACKAGE
SN74F541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F541 . . . FK PACKAGE
(TOP VIEW)



2 Data Sheets

PRODUCT PREVIEW

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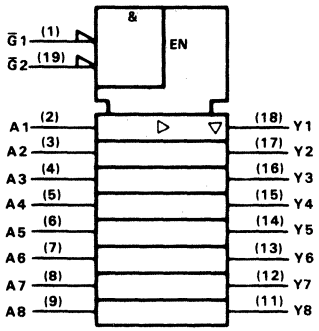
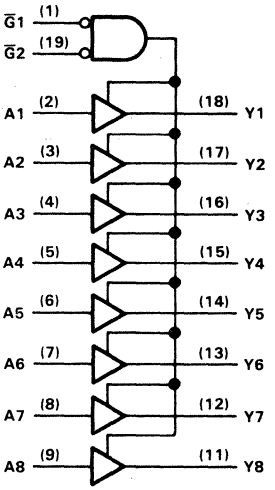
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F541 . . . . . 96 mA
SN74F541 . . . . . 128 mA
Operating free-air temperature range: SN54F541 . . . . . −55°C to 125°C
SN74F541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F541			SN74F541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F541			SN74F541			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.7	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
	V_{CC} = 4.75 V,	I_{OH} = −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	75		62	75	mA
		Outputs low		28	35		28	35	
		Outputs disabled		40	55		40	55	

switching characteristics (see Note 1)

PARAMETER	FROM (INTPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'F541			SN54F541		SN74F541		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Data	Y	1	2.9	5.5	1	6.5	1	6	ns
t_{PHL}	(Any A)		1	2.3	5.5	1	6.5	1	6	
t_{PZH}	$1\overline{G}$ or 2G	Y	2.2	5.4	8	1.7	10	1.7	9.5	ns
t_{PZL}			2.7	5.7	8.5	2.2	10	2.2	9.5	
t_{PHZ}	$1\overline{G}$ or 2G	Y	1	3	6	1	7	1	6.5	ns
t_{PLZ}			1	2.5	5.5	1	7.5	1	6	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

D2942, MARCH 1987—REVISED JANUARY 1989

- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

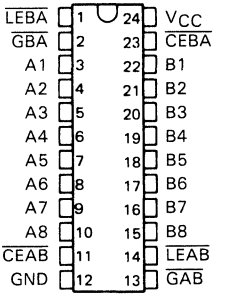
description

The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For the SN54F543 and SN74F543, respectively, the A outputs are characterized to sink 20 or 24 milliamperes while the B outputs are characterized for 48 or 64 milliamperes.

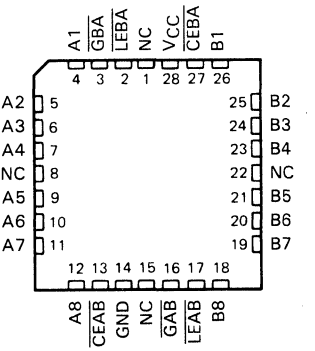
The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The SN54F543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F543 is characterized for operation from 0°C to 70°C.

SN54F543 . . . JT PACKAGE
SN74F543 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54F543 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$	A TO B†	B1 THRU B8
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

†A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡Before low-to-high transition of $\overline{LEAB}$.

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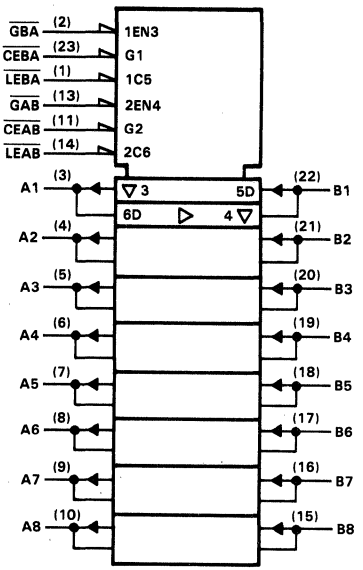
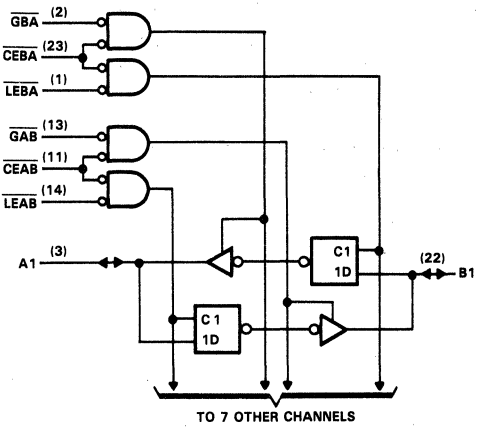
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (excluding I/O ports)‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F543 (A1 thru A8) . . . . . 40 mA
SN54F543 (B1 thru B8) . . . . . 96 mA
SN74F543 (A1 thru A8) . . . . . 48 mA
SN74F543 (B1 thru B8) . . . . . 128 mA
Operating free-air temperature range: SN54F543 . . . . . −55°C to 125°C
SN74F543 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F543			SN74F543			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F543			SN74F543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1 thru A8	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V,	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A and B		V_I = 5.5 V			1			1	
I_{IH}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A and B					70			70	
I_{IL}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V,	V_I = 0.5 V			−1.2			−1.2	mA
	A and B					−0.65			−0.65	
I_{OS}§	A1 thru A8	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
	B1 thru B8			−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V			67	100		67	100	mA
I_{CCL}		V_{CC} = 5.5 V			83	125		83	125	mA
I_{CCZ}		V_{CC} = 5.5 V			83	125		83	125	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F543		SN54F543		SN74F543		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable	High or low	3				3.5		ns
t_h	Hold time, data after latch enable	High or low	3				3.5		ns

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F543			SN54F543		SN74F543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	5.1	7.5			2.2	8.5	ns
t_{PHL}			2.2	4.6	6.5			2.2	7.5	
t_{PLH}	$\overline{LEBA}$	A	3.7	8.1	11			4.1	12.5	ns
t_{PHL}			3.7	8.1	11			4.1	12.5	
t_{PLH}	$\overline{LEAB}$	B	3.7	8.1	11			4.1	12.5	ns
t_{PHL}			3.7	8.1	11			4.1	12.5	
t_{PZH}	$\overline{G}$ or $\overline{CE}$	A or B	2.2	6.6	9			2.2	10	ns
t_{PZL}			3.2	7.1	10.5			3.2	12	
t_{PHZ}	$\overline{G}$ or $\overline{CE}$	A or B	1.7	5.6	8			1.7	9	ns
t_{PLZ}			1.7	5.1	7.5			1.7	8.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2942, MARCH 1987—REVISED JANUARY 1989

- **3-State Inverted Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

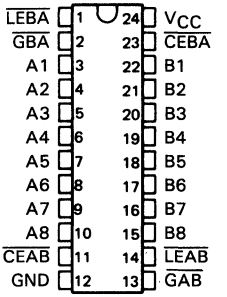
description

The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For the SN54F544 and SN74F544, respectively, the A outputs are characterized to sink 20 or 24 milliamperes while the B outputs are characterized for 48 or 64 milliamperes. The 'F544 inverts data in both directions.

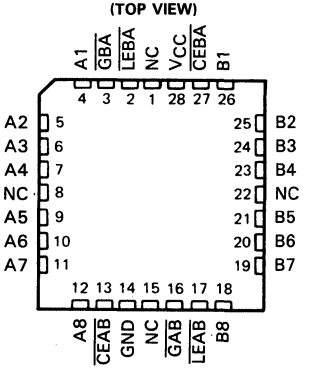
The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The SN54F544 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F544 is characterized for operation from 0°C to 70°C.

SN54F544 . . . JT PACKAGE
SN74F544 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54F544 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$	A to B†	B1 THRU B8
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current $\overline{A}$ Data
L	H	L	Storing	Previous‡ $\overline{A}$ Data

†A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$
‡Before low-to-high transition of $\overline{LEAB}$.

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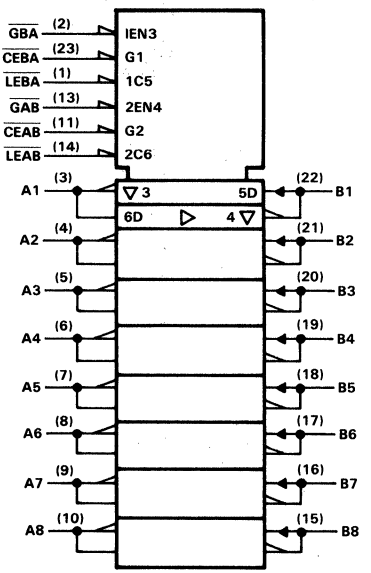
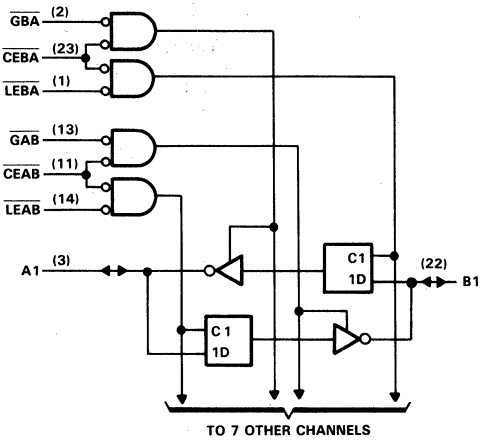
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (excluding I/O ports)‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F544 (A1 thru A8) . . . . . 40 mA
SN54F544 (B1 thru B8) . . . . . 96 mA
SN74F544 (A1 thru A8) . . . . . 48 mA
SN74F544 (B1 thru B8) . . . . . 128 mA
Operating free-air temperature range: SN54F544 . . . . . −55°C to 125°C
SN74F544 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F544			SN74F544			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F544			SN74F544			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	A1 thru A8	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V, I_{OH} = −1 mA to −3 mA					2.7			
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A and B		V_I = 5.5 V			1			1	
I_{IH}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A and B					70			70	
I_{IL}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V, V_I = 0.5 V				−1.2			−1.2	mA
	A and B					−0.65			−0.65	
I_{OS}§	A1 thru A8	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8			−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V			67	100		67	100	mA
I_{CCL}		V_{CC} = 5.5 V			83	125		83	125	mA
I_{CCZ}		V_{CC} = 5.5 V			83	125		83	125	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F544		SN54F544		SN74F544		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable	High or low	3				3		ns
t_h	Hold time, data after latch enable	High or low	3				3		ns

PRODUCT PREVIEW

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F544			SN54F544		SN74F544		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	6.6	9.5			2.2	10.5	ns
t_{PHL}			2.2	4.6	6.5			2.2	7.5	
t_{PLH}	$\overline{LEBA}$	A	5.2	9.6	13			5.2	14.5	ns
t_{PHL}			3.2	6.6	9.5			3.2	10.5	
t_{PLH}	$\overline{LEAB}$	B	5.2	9.6	13			5.2	14.5	ns
t_{PHL}			3.2	6.6	9.5			3.2	10.5	
t_{PZH}	$\overline{G}$ or $\overline{CE}$	A or B	2.2	6.6	9			2.2	10	ns
t_{PZL}			3.2	7.1	10.5			3.2	12	
t_{PHZ}	$\overline{G}$ or $\overline{CE}$	A or B	1.7	5.6	8			1.7	9	ns
t_{PLZ}			1.7	5.1	7.5			1.7	8.5	

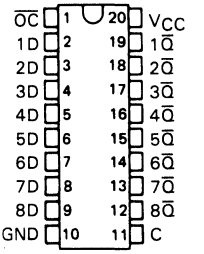
PRODUCT PREVIEW

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

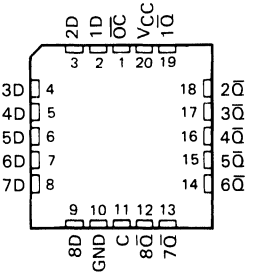
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- 8 Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN54F563 . . . J PACKAGE
SN74F563 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F563 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. When the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low, the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54F563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F563 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

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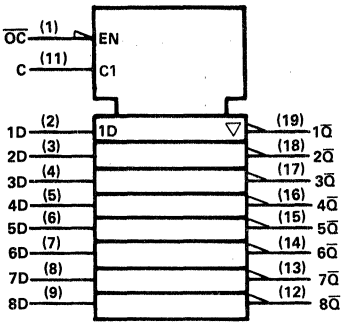
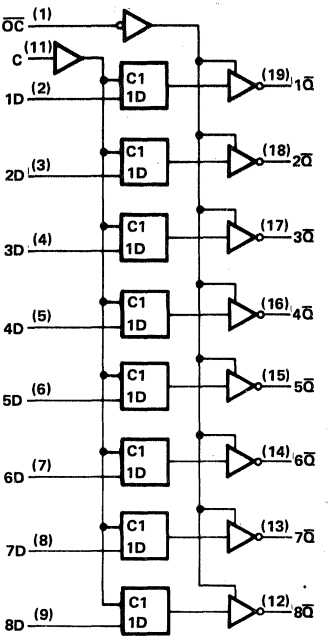
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

abolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F563 . . . . . 40 mA
SN74F563 . . . . . 48 mA
Operating free-air temperature range: SN54F563 . . . . . −55°C to 125°C
SN74F563 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F563			SN74F563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperatuare range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F563			SN74F563			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.30	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		38	61		38	61	mA

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ at 4.5 V and all other inputs grounded.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'F563		SN54F563		SN74F563		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before enable C↓	2		2		2		ns
t_h	Hold time, data before enable C↓	3		3		3		ns
t_w	Pulse duration, enable C high	6		6		6		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F563			SN54F563		SN74F563		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.2	6.5	9	3.2	12	3.2	10	ns
t_{PHL}			2.2	4.8	7	2.2	9	2.2	8	
t_{PLH}	C	Q	4.2	8.1	11	4.2	14	4.2	13	ns
t_{PHL}			2.2	5.2	7	2.2	9	2.2	8	
t_{PZH}	$\overline{OC}$	Q	1.2	7.3	10	1.2	12.5	1.2	11	ns
t_{PZL}			1.2	4.7	6.5	1.2	9	1.2	7.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.3	6	1.2	8.5	1.2	7	ns
t_{PLZ}			1.2	3.7	5.5	1.2	7.5	1.2	6.5	

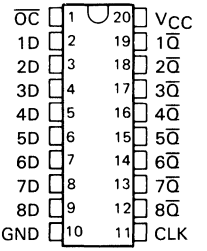
PRODUCT PREVIEW

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

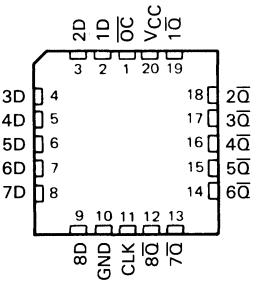
D3034, SEPTEMBER 1987—REVISED JANUARY 1989

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F564 . . . J PACKAGE
SN74F564 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F564 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'F564 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs. The 'F564 is equivalent to the 'F574 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the flip-flops. Old data can be retained, or new data can be entered while the outputs are off.

The SN54F564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F564 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

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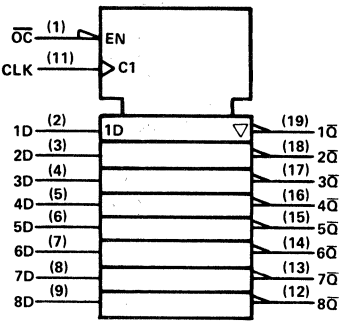
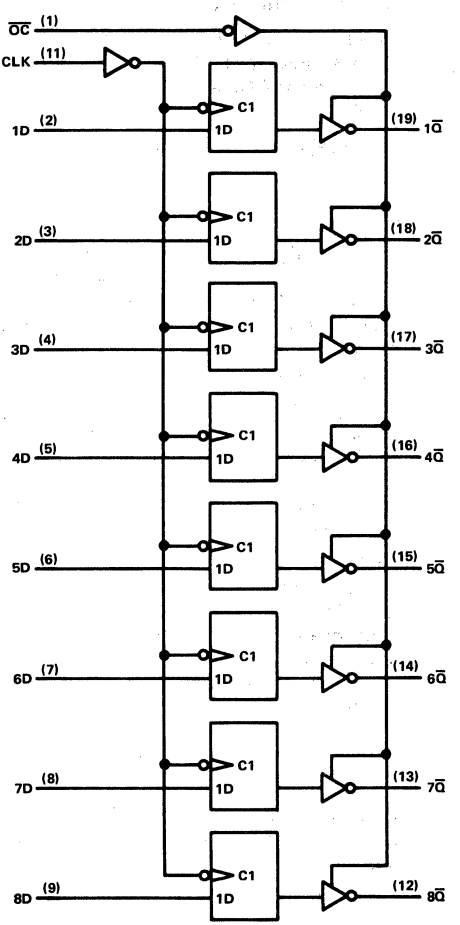
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F564 . . . . . 40 mA
SN74F564 . . . . . 48 mA
Operating free-air temperature range: SN54F564 . . . . . −55°C to 125°C
SN74F564 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F564			SN74F564			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F564			SN74F564			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		55	86		55	86	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 1 second.
NOTE 1: I_{CC} is measured with $\overline{OC}$ at 4.5 V, all other inputs grounded.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Note 2)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F564		SN54F564		SN74F564		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	60	0	70	MHz
t_{su}	Setup time before CLK↑	Data high	2		2.5		2		ns
		Data low	2		2		2		
t_h	Hold time after CLK↑	Data high	2		2		2		ns
		Data low	2		2.5		2		
t_w	Pulse duration	CLK high	5		7		7		ns
		CLK low	5		6		6		

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F564			SN54F564		SN74F564		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	$\overline{Q}$	3.2	6.1	8.5	3.2	10.5	3.2	10	ns
t_{PHL}			3.2	6.1	8.5	3.2	11	3.2	10	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	1.2	8.6	11.5	1.2	14	1.2	12.5	ns
t_{PZL}			1.2	5.4	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	1.2	4.9	7	1.2	8	1.2	8	ns
t_{PLZ}			1.2	3.9	5.5	1.2	7.5	1.2	6.5	

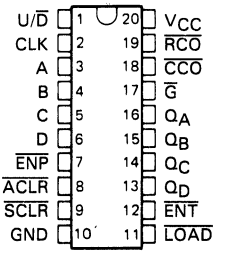
PRODUCT PREVIEW

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

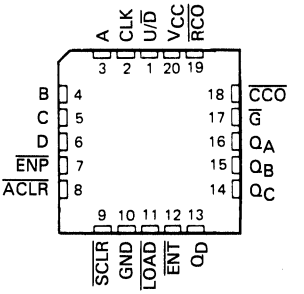
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Also Provided
- Fully Cascadable
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54F568, SN54F569 . . . J PACKAGE
SN74F568, SN74F569 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F568, SN54F569 . . . FK PACKAGE
(TOP VIEW)



description

The 'F568 decade counters and 'F569 binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load ($\overline{LOAD}$) low during a positive-going clock transition. The counting function is enabled only when Enable P ($\overline{ENP}$) and Enable T ($\overline{ENT}$) are low and $\overline{ACLR}$, $\overline{SCLR}$, and $\overline{LOAD}$ are high. The Up/Down U/$\overline{D}$) input controls the direction of the count. These counters count up when U/$\overline{D}$ is high and count down when U/$\overline{D}$ is low.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{G}$. $\overline{ENT}$ is fed forward to enable the Ripple Carry Output ($\overline{RCO}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output ($\overline{CCO}$) produces a low level pulse for a duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled (both $\overline{ENP}$ and $\overline{ENT}$ are low); otherwise, $\overline{CCO}$ is high as shown in the $\overline{CCO}$ function table. $\overline{CCO}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplishd by connecting $\overline{RCO}$ or $\overline{CCO}$ of the first counter to $\overline{ENT}$ of the next counter. However, for very-high-speed counting, $\overline{RCO}$ should be used for cascading since $\overline{CCO}$ does not become active until the clock returns to the low level.

The SN54F568 and SN54F569 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F568 and SN74F569 are characterized for operation from 0°C to 70°C.

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$\overline{CCO}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	$\overline{TC}$*	CLK	$\overline{CCO}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊔	⊔

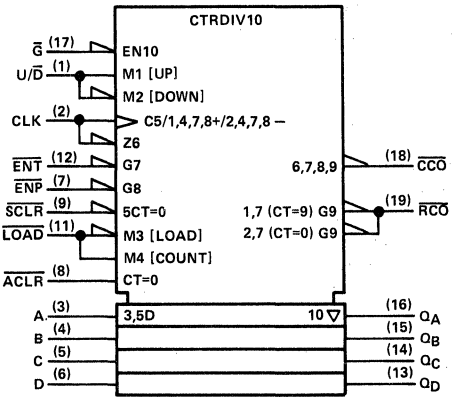
* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE

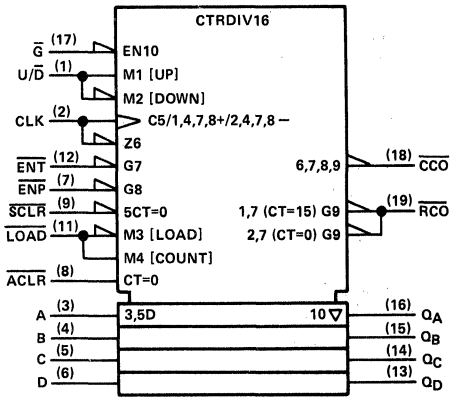
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	↑	Synchronous Clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count Up
L	H	H	H	L	L	L	↑	Count Down
L	H	H	H	H	X	X	X	Inhibit Count
L	H	H	H	X	H	X	X	Inhibit Count

logic symbols†

'F568



'F569



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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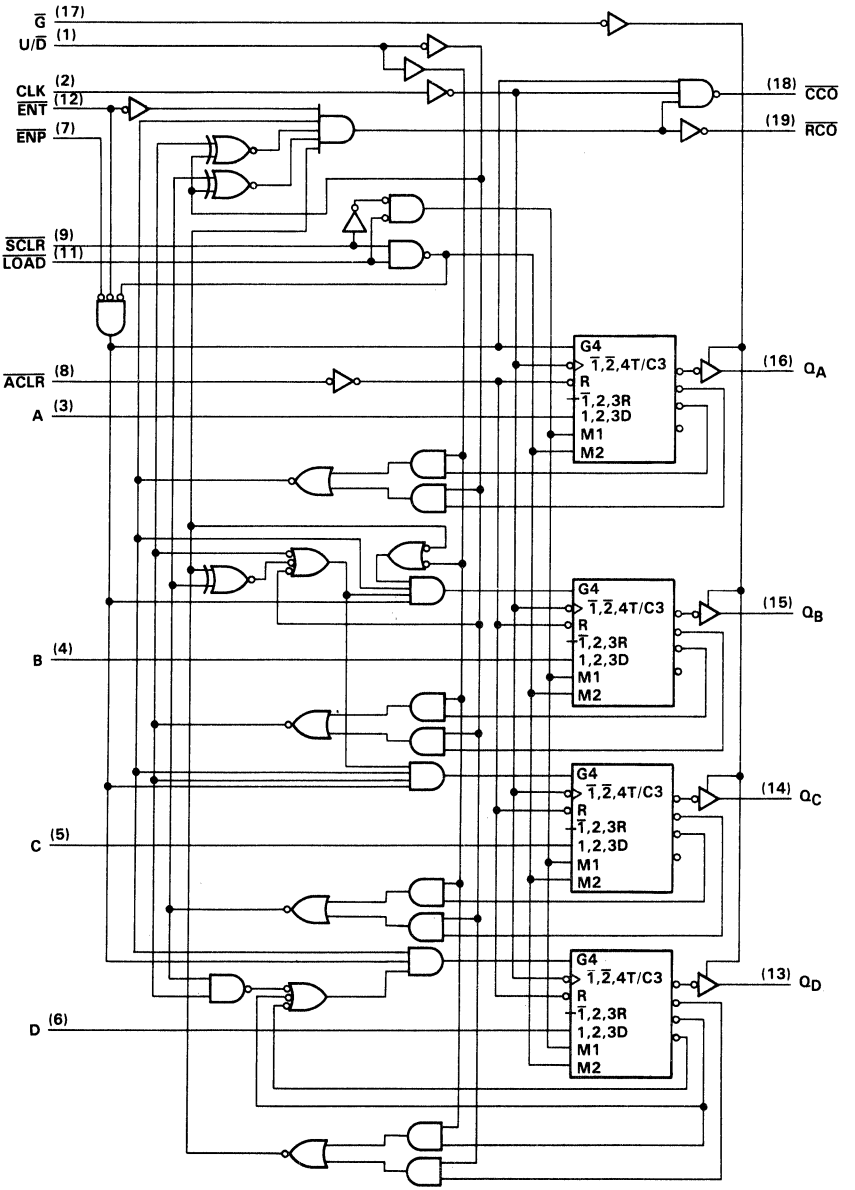
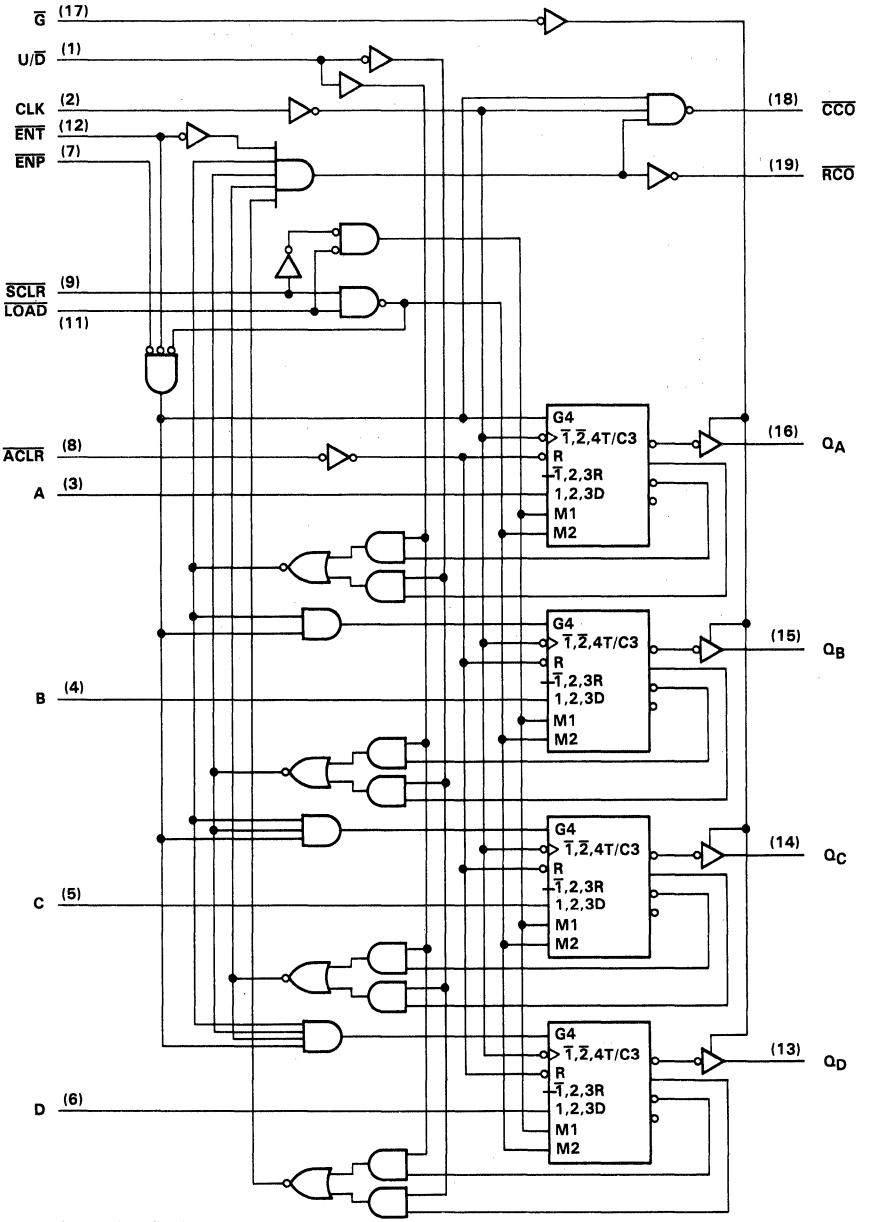
'F568 logic diagram (positive logic)



Logic diagrams for the four flip-flops are shown separately.

'F569 logic diagram (positive logic)



Logic diagrams for the four flip-flops are shown separately.

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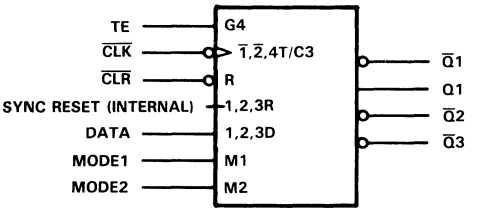
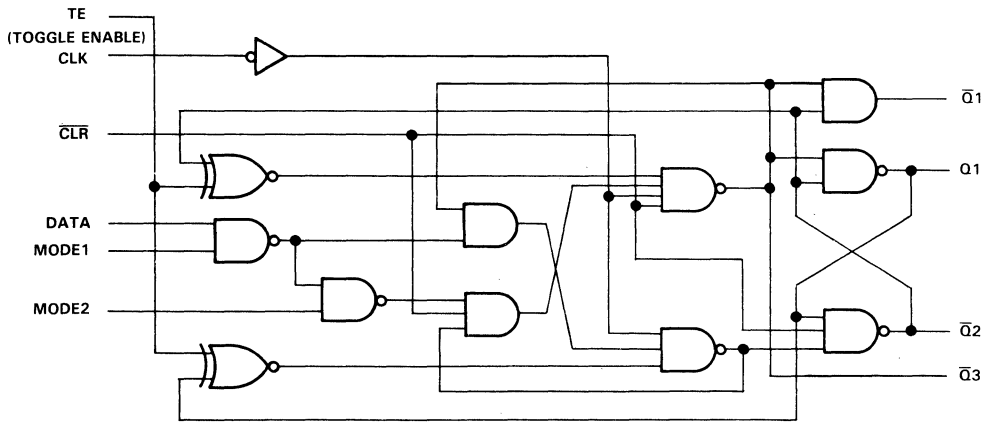
logic symbol, each flip-flop in 'F568 and 'F569 (positive logic)



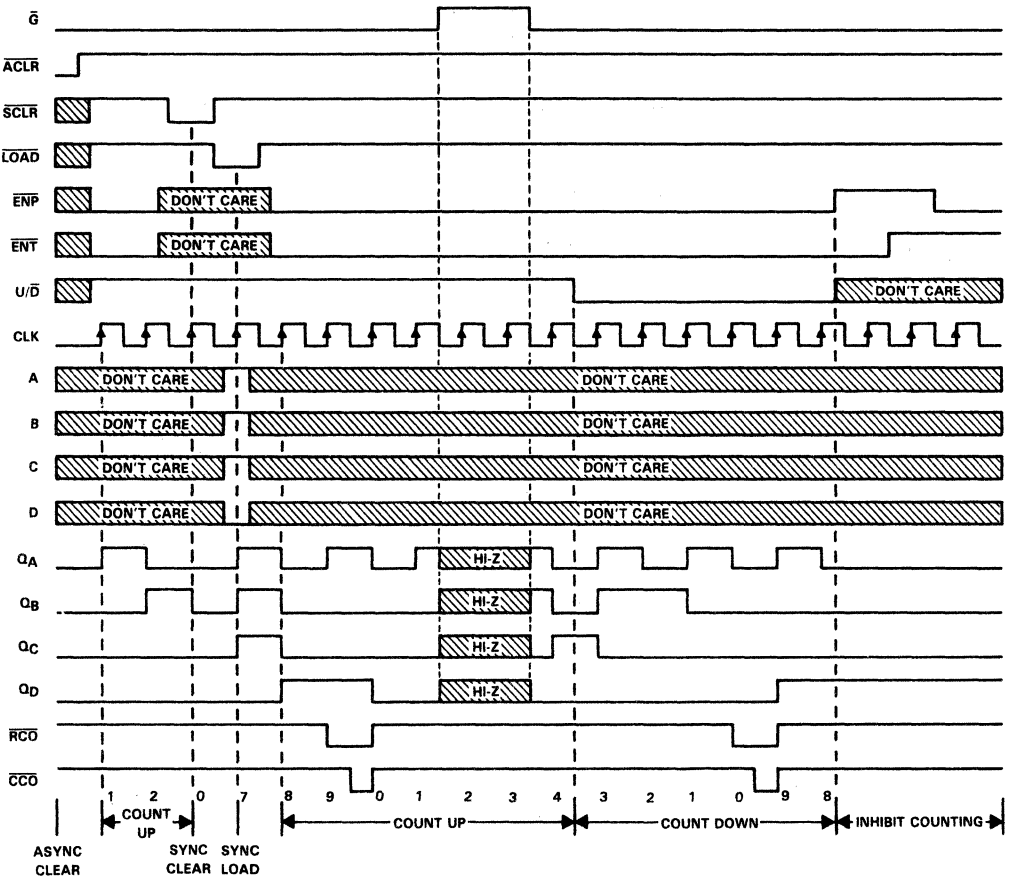
logic diagram, each flip-flop in 'F568 and 'F569 (positive logic)



FUNCTION TABLE, EACH FLIP-FLOP

COUNTER INPUTS				FLIP-FLOP INPUTS						OUTPUTS	
$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	CLK	$\overline{CLR}$	MODE1	MODE2	TE	$\overline{CLK}$	DATA	Q	$\overline{Q}$
L	X	X	X	L	X	X	X	X	X	L	H
H	L	X	↑	H	L	H	X	↓	X	L	H
H	H	L	↑	H	H	H	X	↓	H	H	L
H	H	L	↑	H	H	H	X	↓	L	L	H
H	H	H	↑	H	L	L	H	↓	X	$\overline{Q}_0$	Q_0
H	H	H	↑	H	L	L	L	↓	X	Q_0	$\overline{Q}_0$

'F568 typical load, count, and inhibit sequences



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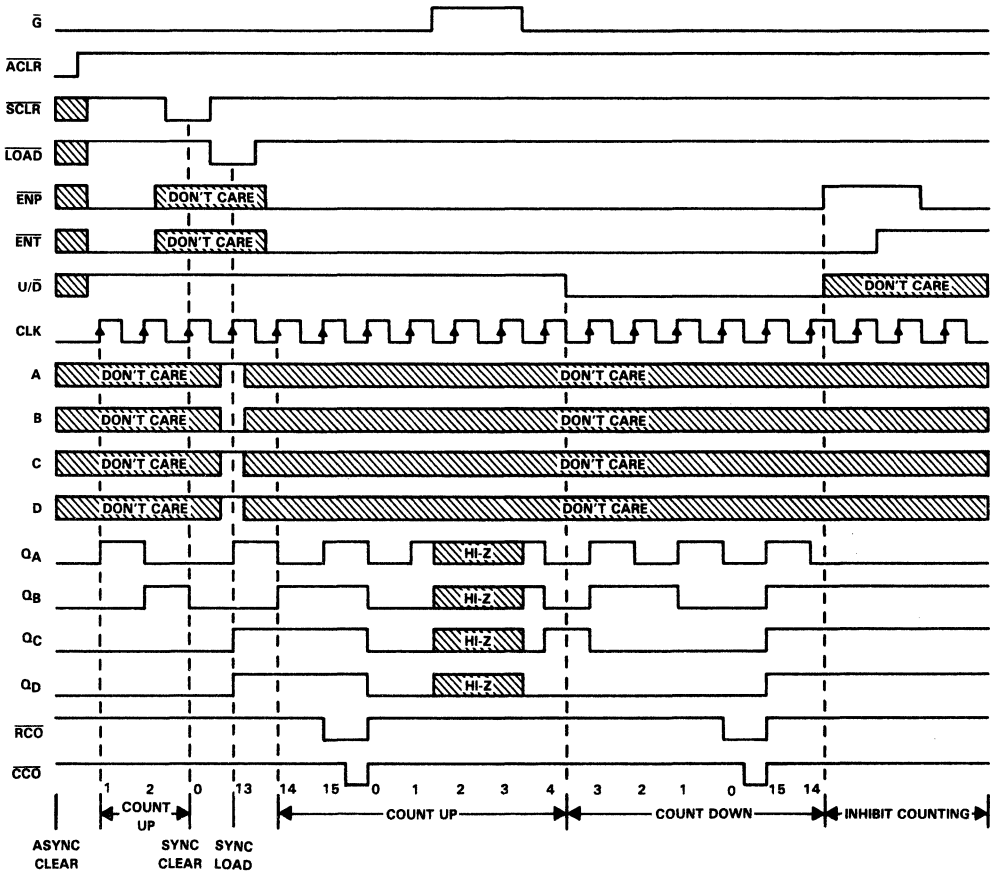
'F569 typical load, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into outputs in the low state: $\overline{RCO}$, $\overline{CCO}$ . . . . . 40 mA
Any Q; SN54F568, SN54F569 . . . . . 40 mA
Any Q; SN74F568, SN74F569 . . . . . 48 mA
Operating free-air temperature range: SN54F568, SN54F569 . . . . . −55°C to 125°C
SN74F568, SN74F569 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F'			SN74F'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	$\overline{RCO}$, $\overline{CCO}$			−1			−1	mA
		Any Q			−3			−3	
I_{OL}	Low-level output current	$\overline{RCO}$, $\overline{CCO}$			20			20	mA
		Any Q			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F'			SN74F'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = −1 mA to −3 mA				2.7			
	Any Q	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
V_{OL}	$\overline{RCO}$, $\overline{CCO}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Any Q	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{ENT}$, $\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.5 V			−1.2			−1.2	mA
	All other					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		45	67		45	67	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with B and $\overline{ENT}$, $\overline{ACLR}$, and $\overline{SCLR}$ inputs high and all other inputs low.

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timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F568, 'F569		SN54F'		SN74F'		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100			0	90	MHz
t_{su}	Setup time, data (A, B, C, D) high or low before CLK↑		4				4.5		ns
t_{hold}	Hold time, data (A, B, C, D) high or low after CLK↑		3				3.5		ns
t_{su}	Setup time, $\overline{ENP}$ and $\overline{ENT}$ high or low before CLK↑		5				6		ns
t_{hold}	Hold time, $\overline{ENP}$ and $\overline{ENT}$ high or low after CLK↑		0				0		ns
t_{su}	Setup time, $\overline{LOAD}$ high or low before CLK↑		8				9		ns
t_{hold}	Hold time, $\overline{LOAD}$ high or low after CLK↑		0				0		ns
t_{su}	Setup time, U/$\overline{D}$ before CLK↑	'F568, high	11				12.5		ns
		'F568, low	16.5				17.5		
		'F569, high	11				12.5		
		'F569, low	7				8		
t_{hold}	Hold time, U/$\overline{D}$ high or low after CLK↑		0				0		ns
t_{su}	Setup time, $\overline{SCLR}$ before CLK↑	High	9.5				10.5		ns
		Low	8.5				9.5		
t_{hold}	Hold time, $\overline{SCLR}$ high or low after CLK↑		0				0		ns
t_w	Pulse duration, CLK	High	4				4.5		ns
		Low	6				6.5		
t_w	Pulse duration, $\overline{ACLR}$ low		4.5				5		ns
t_{su}	Inactive-state setup time, $\overline{ACLR}$ high before CLK↑‡		6				7		ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ Inactive-state setup time is also referred to as "recovery time".

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F568, 'F569			SN54F'		SN74F'		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	115				90		MHz
t_{PLH}	CLK	Q	2.2	6.1	8.5			2.2	9.5	ns
t_{PHL}			3.2	8.6	11.5			3.2	13	
t_{PLH}	CLK	$\overline{RCO}$	4.7	11.6	15.5			4.7	17.5	ns
t_{PHL}			3.2	8.1	11			3.2	12.5	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.7	4.1	6			1.7	7	ns
t_{PHL}			1.7	5.6	8			1.7	9	
t_{PLH}	U/$\overline{D}$ ('F568)	$\overline{RCO}$	2.7	8.1	11			2.7	12.5	ns
t_{PHL}			3.2	12.1	16			3.2	18	
t_{PLH}	U/$\overline{D}$ ('F569)	$\overline{RCO}$	2.7	8.1	11			2.7	12.5	ns
t_{PHL}			3.2	7.6	10.5			3.2	12	
t_{PLH}	CLK	$\overline{CCO}$	1.7	5.1	7			1.7	8	ns
t_{PHL}			1.2	4.1	6			1.2	7	
t_{PLH}	$\overline{ENP}$, $\overline{ENT}$	$\overline{CCO}$	1.7	4.6	6.5			1.7	7.5	ns
t_{PHL}			3.2	8.1	11			3.2	12.5	
t_{PHL}	$\overline{ACLR}$	Q	4.2	9.6	13			4.2	14.5	ns
t_{PZH}	$\overline{G}$	Q	1.7	5.1	7			1.7	8	ns
t_{PZL}			2.2	5.6	8			2.2	9	
t_{PHZ}	$\overline{G}$	Q	1	4.6	6.5			1	7.5	ns
t_{PLZ}			1.2	4.1	6			1.2	7	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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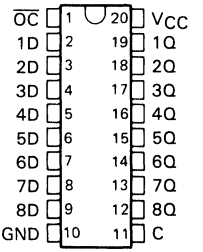
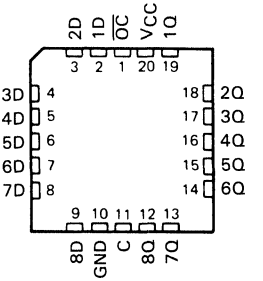
D3034, JULY 1987—REVISED JANUARY 1989

- **8 Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F573 . . . J PACKAGE
SN74F573 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F573 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'F573 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained, or new data can be entered while the outputs are off.

The SN54F573 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F573 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

2 Data Sheets

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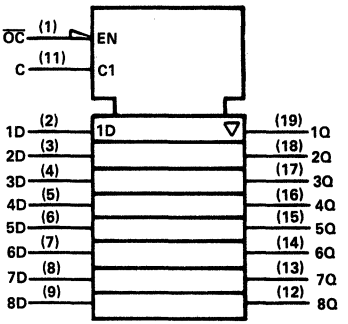
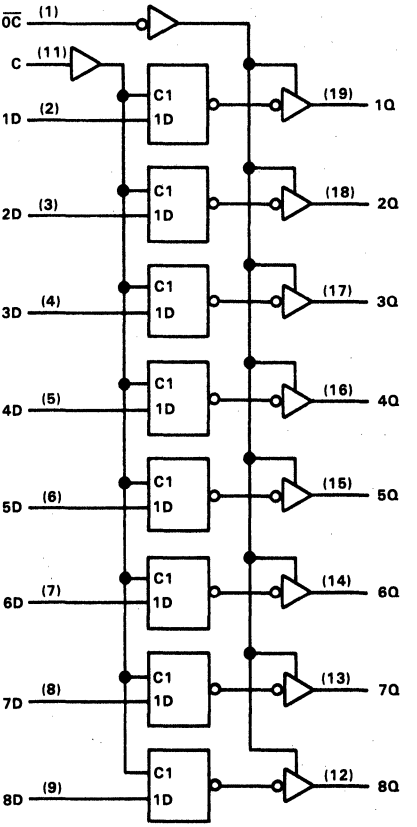
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F573 . . . . . 40 mA
SN74F573 . . . . . 48 mA
Operating free-air temperature range: SN54F573 . . . . . −55°C to 125°C
SN74F573 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F573			SN74F573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F573			SN74F573			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.30	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		38	55		38	55	mA

PRODUCT PREVIEW

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 1 second.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ at 4.5 V and all other inputs grounded.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†			UNIT
		'F573		SN54F573		SN74F573	
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, Data before Enable C↓	2				2		ns
t_h	Hold time, Data before Enable C↓	3				3		ns
t_w	Pulse duration, Enable C high	6				6		ns

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F573			SN54F573		SN74F573		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	4.9	7			2.2	8	ns
t_{PHL}			1.2	3.3	5			1.2	6	
t_{PLH}	C	Q	4.2	8.6	11.5			4.2	13	ns
t_{PHL}			2.2	4.8	7			2.2	8	
t_{PZH}	$\overline{OC}$	Q	1.2	4.6	11			1.2	12	ns
t_{PZL}			1.2	5.2	7.5			1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.1	6.5			1.2	7.5	ns
t_{PLZ}			1.2	3.4	6			1.2	6	

PRODUCT PREVIEW

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3034, SEPTEMBER 1987—REVISED JANUARY 1989

- **8 D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

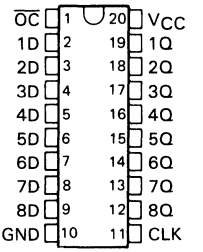
The eight flip-flops of the 'F574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

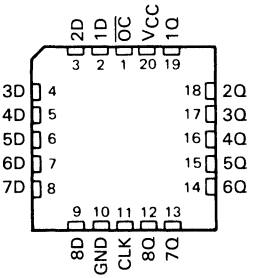
The output control does not affect the internal operations of the flip-flops. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

The SN54F574 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F574 is characterized for operation from 0°C to 70°C.

SN54F574 . . . J PACKAGE
SN74F574 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F574 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

2 Data Sheets

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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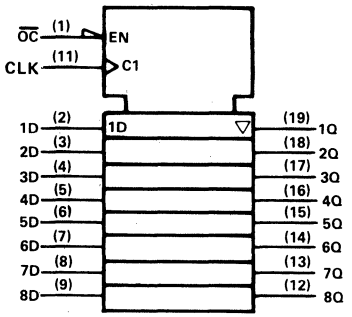
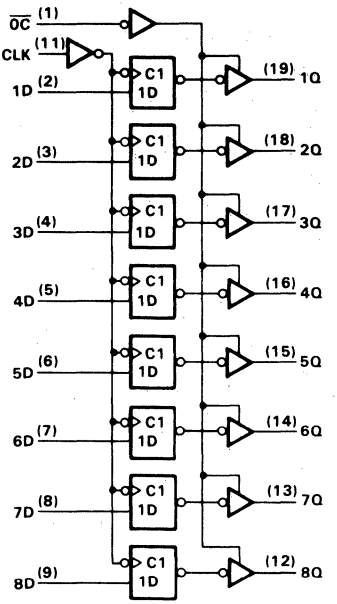
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F574 . . . . . 40 mA
SN74F574 . . . . . 48 mA
Operating free-air temperature range: SN54F574 . . . . . −55°C to 125°C
SN74F574 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ The input voltage ratings may be exceeded provided the input current ratings are observed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54F574			SN74F574			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F574			SN74F574			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		55	86		55	86	mA

PRODUCT PREVIEW

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 1 second.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ and CLK at 4.5 V and the data inputs grounded.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F574		SN54F574		SN74F574		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	60	0	70	MHz
t_{su}	Setup time before CLK↑	Data high	2		2.5		2		ns
		Data low	2		2		2		
t_h	Hold time after CLK↑	Data high	2		2		2		ns
		Data low	2		2.5		2		
t_w	Pulse duration	CLK high	7		7		7		ns
		CLK low	6		6		6		

PRODUCT PREVIEW

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F574			SN54F574		SN74F574		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			60		70		MHz
t_{PLH}	CLK	Q	3.2	6.1	8.5	3.2	10.5	3.2	10	ns
t_{PHL}			3.2	6.1	8.5	3.2	11	3.2	10	
t_{PZH}	$\overline{OC}$	Q	1.2	8.6	11.5	1.2	14	1.2	12.5	ns
t_{PZL}			1.2	4.9	7.5	1.2	10	1.2	8.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.9	7	1.2	8	1.2	8	ns
t_{PLZ}			1.2	3.9	5.5	1.2	7.5	1.2	6.5	

PRODUCT PREVIEW

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

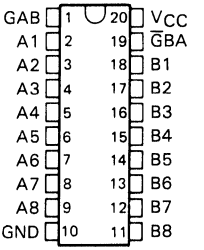
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2932, MARCH 1987—REVISED JANUARY 1989

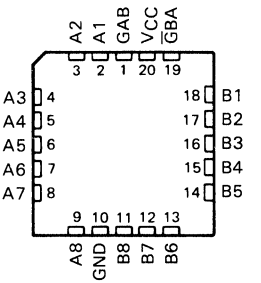
- **Local Bus-Latch Capability**
- **Choice of Inverting or Noninverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'F620	3-State	Inverting
'F621	Open-Collector	Noninverting
'F622	Open-Collector	Inverting
'F623	3-State	Noninverting

SN54F' . . . J PACKAGE
SN74' . . . DW OR N PACKAGE
(TOP VIEW)



SN54F' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous activation of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. When both control inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for 'F621 and 'F623, or complementary for the 'F620 and 'F622.

The SN54F620 through SN54F623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F620 and SN74F623 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'F620, 'F622	'F621, 'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

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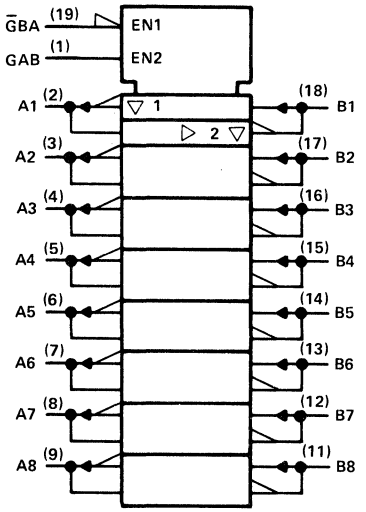
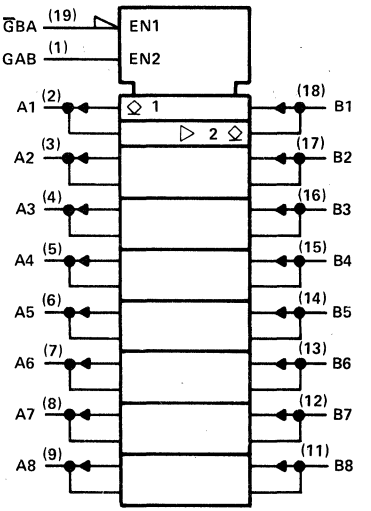
logic symbols†

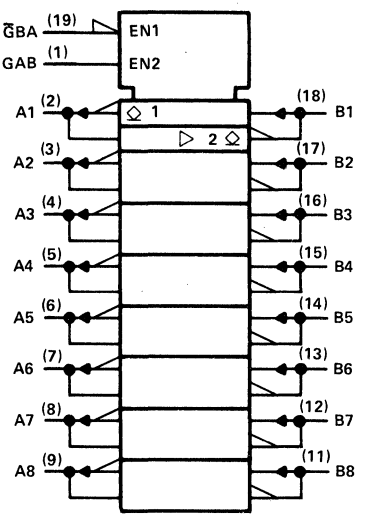
'F620



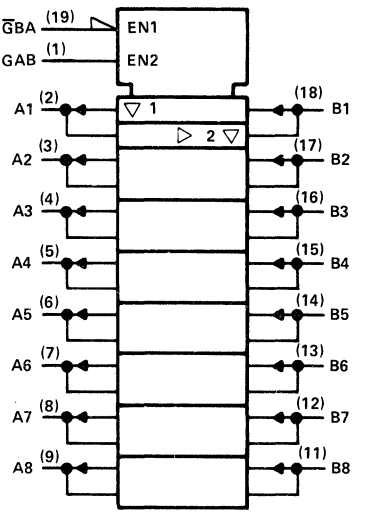
'F621



'F622



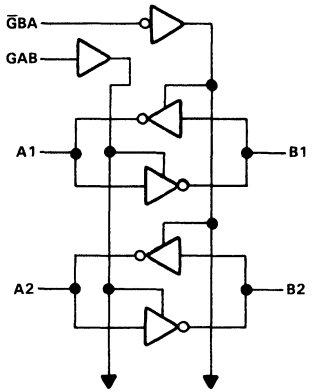
'F623



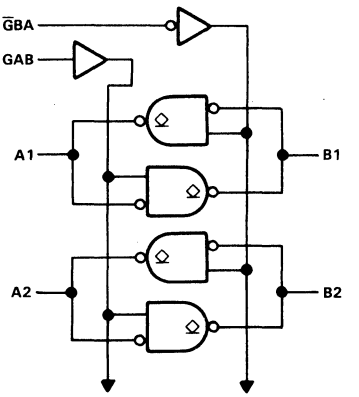
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

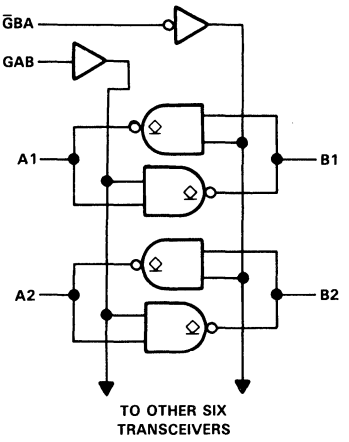
'F620



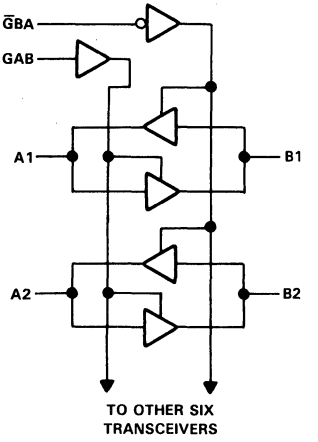
'F621



'F622



'F623



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F620, SN54F623 (Any A) . . . . . 40 mA
(Any B) . . . . . 96 mA
SN74F620, SN74F623 (Any A) . . . . . 128 mA
(Any B) . . . . . 48 mA
Operating free-air temperature range: SN54F620, SN54F623 . . . . . −55°C to 125°C
SN74F620, SN74F623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F620 SN54F623			SN74F620 SN74F623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Any A			−3			−3	mA
		Any B			−12			−15	
I_{OL}	Low-level output current	Any A			20			24	mA
		Any B			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54F620 SN54F623			SN74F620 SN74F623			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	A and B	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA					2.7			V
	Any A	V_{CC} = 4.5 V	I_{OH} = −1 mA		2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA		2.4	3.3		2.4	3.3		
	Any B		I_{OH} = −3 mA		2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA		2	3.2					
			I_{OH} = −15 mA					2	3.1		
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA			0.3	0.5				V
			I_{OL} = 24 mA						0.35	0.5	
	Any B		I_{OL} = 48 mA			0.38	0.55				
			I_{OL} = 64 mA						0.42	0.55	
I_I	A and B	V_{CC} = 5.5 V	V_I = 5.5 V				1			1	mA
	GAB or $\overline{GBA}$		V_I = 7 V				0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V				70			70	μA
	GAB or $\overline{GBA}$						20			20	
I_{IL}‡	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V				−0.65			−0.65	mA
	GAB or $\overline{GBA}$						−0.6			−0.6	
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0		−60		−150	−60		−150	mA
	Any B				−100		−225	−100		−225	
I_{CC}	'F620	V_{CC} = 5.5 V	I_{CCH}	$\overline{GBA}$ = GAB = 4.5 V, $A_1 - A_8$ = GND		70	92		70	92	mA
			I_{CCL}	$\overline{GBA}$ = GAB = 4.5 V, $A_1 - A_8$ = 4.5 V		84	110		84	110	
			I_{CCZ}	GAB = GND, $\overline{GBA} = A_1 - A_8$ = 4.5 V		70	92		70	92	
	'F623		I_{CCH}	$\overline{GBA}$ = GAB = 4.5 V, $A_1 - A_8$ = 4.5 V		110	140		110	140	
			I_{CCL}	$\overline{GBA}$ = GAB = 4.5 V, $A_1 - A_8$ = GND		110	140		110	140	
			I_{CCZ}	GAB = GND, $\overline{GBA} = A_1 - A_8$ = 4.5 V		99	130		99	130	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

'F620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = MIN to MAX[1], C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			'F620			SN54F620		SN74F620		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.7	4.1	6.5	1.2	8.5	1.2	7.5	ns
t_{PHL}			1	2.1	4.5	1	5.5	1	5	
t_{PLH}	B	A	1.7	4.1	6.5	1.2	8.5	1.2	7.5	ns
t_{PHL}			1	2.1	4.5	1	5.5	1	5	
t_{PZH}	$\overline{G}$BA	A	2.2	7.1	10.5	1.7	12	1.7	11.5	ns
t_{PZL}			3.2	7.1	10.5	2.7	12.5	2.7	11.5	
t_{PHZ}	$\overline{G}$BA	A	1.7	4.1	7.5	1.2	9	1.2	8	ns
t_{PLZ}			1.2	4.1	7	1	8.5	1	7.5	
t_{PZH}	GAB	B	3.7	7.1	10.5	2.5	12	3.2	11.5	ns
t_{PZL}			3.7	7.1	10	3.2	12	3.2	11	
t_{PHZ}	GAB	B	2.2	6.1	9.5	1.7	11	1.7	10.5	ns
t_{PLZ}			3.2	6.1	9.5	2.7	11.5	2.7	10.5	

'F623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = MIN to MAX[†], C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			'F623			SN54F623		SN74F623		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.6	5.5	1.1	6.8	1.2	6.5	ns
t_{PHL}			2.2	4.6	7	1.6	8	1.7	7.5	
t_{PLH}	B	A	1.2	3.6	5.5	1.1	6.8	1.2	6.5	ns
t_{PHL}			1.7	4.1	6.5	1.6	8	1.7	7.5	
t_{PZH}	$\overline{G}$BA	A	3.1	8.1	10.5	2.7	12.4	3.1	12	ns
t_{PZL}			2.8	7.1	9.5	2.5	10.3	2.8	10	
t_{PHZ}	$\overline{G}$BA	A	1.7	4.1	6.5	1.6	8.3	1.7	7.5	ns
t_{PLZ}			1.7	4.1	6.5	1.5	7.4	1.7	7	
t_{PZH}	GAB	B	2.8	7.6	10	2.7	12	2.8	11.5	ns
t_{PZL}			2.8	6.6	9	2.8	10	2.9	9.5	
t_{PHZ}	GAB	B	2.2	5.6	8.5	1.9	10	2.2	10	ns
t_{PLZ}			3.2	6.6	9	3.1	10.7	3.2	10	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditons.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to 5.5 V
Current into any output in the low state: SN54F621 (Any A) . . . . . 40 mA
(Any B) . . . . . 96 mA
SN74F621 (Any A) . . . . . 48 mA
(Any B) . . . . . 128 mA
Operating free-air temperature range: SN54F621 . . . . . −55°C to 125°C
SN74F621 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F621			SN74F621			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
V_{OH}	High-level output voltage				5.5			5.5	mA
I_{OL}	Low-level output current	Any A			20			24	mA
		Any B			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F621			SN74F621			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	A and B	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	GAB or $\overline{GBA}$		V_I = 7 V			0.1			0.1	
I_{IH}§	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	GAB or $\overline{GBA}$					20			20	
I_{IL}§	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	GAB or $\overline{GBA}$					−0.6			−0.6	
I_{CC}		V_{CC} = 5.5 V	I_{CCH}		105	140		105	140	mA
			I_{CCL}		105	140		105	140	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to 5.5 V
Current into any output in the low state: SN54F622 (Any A) . . . . . 40 mA
(Any B) . . . . . 96 mA
SN74F622 (Any A) . . . . . 48 mA
(Any B) . . . . . 128 mA
Operating free-air temperature range: SN54F622 . . . . . −55°C to 125°C
SN74F622 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F622			SN74F622			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
V_{OH}	High-level output voltage				5.5			5.5	mA
I_{OL}	Low-level output current	Any A			20			24	mA
		Any B			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F622			SN74F622			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	A and B	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	GAB or $\overline{GBA}$		V_I = 7 V			0.1			0.1	
I_{IH}§	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	GAB or $\overline{GBA}$					20			20	
I_{IL}§	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	GAB or $\overline{GBA}$					−0.6			−0.6	
I_{CC}		V_{CC} = 5.5 V	I_{CCH}		37	48		37	48	mA
			I_{CCL}		68	90		68	90	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

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'F621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F621			SN54F621		SN74F621		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	6	9.5	12	5.5	13	5.5	13	ns
t_{PHL}			2.5	3.8	8	2	8.5	2	8.5	
t_{PLH}	B	A	6	9	12	5.5	12.5	5.5	12.5	ns
t_{PHL}			2.5	4	7.5	2	8	2	8	
t_{PLH}	$\overline{G}$BA	A	6	10	13.5	5.5	14	5.5	14	ns
t_{PHL}			3.5	6.5	10.5	2.5	11	2.5	11	
t_{PLH}	GAB	B	7	12	15	6	17	6	17	ns
t_{PHL}			3.5	6.5	9.5	3	10	3	10	

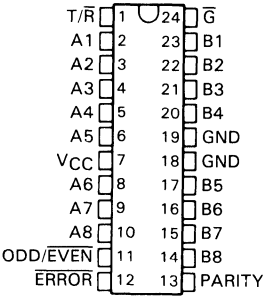
'F622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F622			SN54F622		SN74F622		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	7.2	10.6	12.5			7.2	13.5	ns
t_{PHL}			1	3.6	5.5			1	6	
t_{PLH}	B	A	6.7	9.6	12			6.7	12.5	ns
t_{PHL}			1	3.1	5			1	5.5	
t_{PLH}	$\overline{G}$BA	A	7.2	10.1	12			7.2	12.5	ns
t_{PHL}			4	7.6	10			4	10.5	
t_{PLH}	GAB	B	9.2	12.1	14.5			9.2	15.5	ns
t_{PHL}			4	7.1	9			4	9.5	

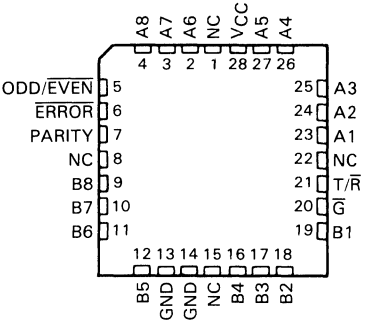
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

- **Combines 'F245 and F280B Functions in One Package**
- **High-Impedance N-P-N Inputs for Reduced Loading (70 μA in Low and High States)**
- **High Output Drive and Light Bus Loading**
- **3-State B Outputs Sink 48 mA or 64 mA and Source 12 mA or 15 mA**
- **Input Diodes for Termination Effects**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F657 . . . JT PACKAGE
SN74F657 . . .DW OR NT PACKAGE
(TOP VIEW)



SN54F657 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'F657 contains 8 noninverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a specified current sinking capability of 20 mA or 24 mA at the A port and 48 mA or 64 mA at the B port.

The T/$\overline{R}$ input determines the direction of the data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data is transmitted from the A port to the B port. When T/$\overline{R}$ is low, data is received at the A port from the B port.

When the $\overline{G}$ input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/$\overline{EVEN}$ input allows the user to select between odd or even parity systems. When transmitting from port A to port B (T/$\overline{R}$ high), PARITY is an output from the generator/checker. When receiving from port B to port A (T/$\overline{R}$ low), PARITY is an input.

When transmitting (T/$\overline{R}$ high), the parity-select (ODD/$\overline{EVEN}$), input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by the parity-select (ODD/$\overline{EVEN}$) input and the number of high bits on port A. When ODD/$\overline{EVEN}$ is low (for even parity) and the number of high bits on port A is odd, then PARITY will be high, transmitting even parity. If the number of high bits on port A is even, the PARITY will be low, keeping even parity.

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description (continued)

When in the receive mode (T/$\overline{R}$ low), the B port is polled to determine the number of high bits. If ODD/$\overline{EVEN}$ is low (for even parity) and the number of highs on port B is:

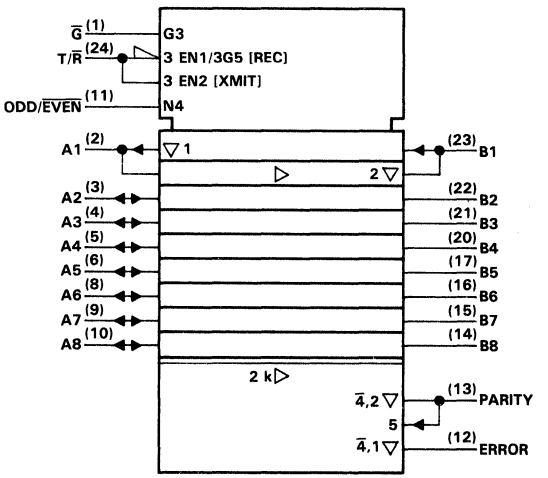
1. Odd and PARITY input is high, then $\overline{ERROR}$ will be high signifying no error.
2. Even and the PARITY input is high, then $\overline{ERROR}$ will be low indicating an error.

The SN54F657 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F657 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT	OUTPUTS	
	$\overline{G}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
DON'T CARE	H	X	X	Z	Z	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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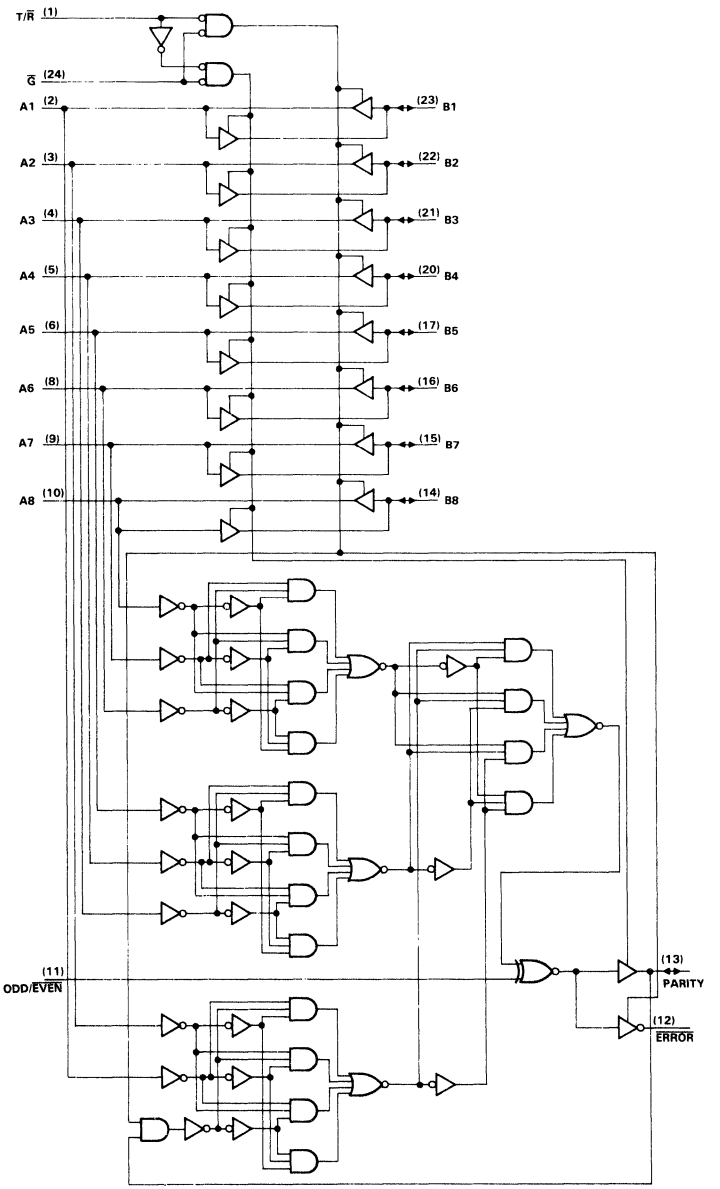
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (excluding I/O ports)† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F657 (A1 thru A8) . . . . . 40 mA
SN54F657 (B1 thru B8) . . . . . 96 mA
SN74F657 (A1 thru A8) . . . . . 48 mA
SN74F657 (B1 thru B8) . . . . . 128 mA
Operating free-air temperature range: SN54F657 . . . . . −55°C to 125°C
SN74F657 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F657			SN74F657			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1-A8			−3			−3	mA
		B1-B8, PARITY, $\overline{\text{ERROR}}$			−12			−15	mA
I_{OL}	Low-level output current	A1-A8			20			24	mA
		B1-B8 PARITY, $\overline{\text{ERROR}}$			48			64	mA
T_A	Operating free-air temperature range		−55		125	0		70	°C

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electrical characterisitcs over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F657			SN74F657			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−0.73	−1.2	V
V_{OH}	Any output	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
	B1 thru B8, PARITY, $\overline{ERROR}$		I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V	I_{OH} = −3 mA				2.7			
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8, PARITY, $\overline{ERROR}$		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	T/$\overline{R}$	V_{CC} = 0, V_I = 7 V, $\overline{G}$ = 4.5 V				0.1			0.1	mA
	$\overline{G}$	V_{CC} = 0, V_I = 7 V, T/$\overline{R}$ = 4.5 V				0.1			0.1	
	ODD/$\overline{EVEN}$	V_{CC} = 0, V_I = 7 V				0.1			0.1	
	A1 thru A8	V_{CC} = 5.5 V, V_I = 5.5 V				2			2	
	B1 thru B8					1			1	
I_{IH}‡	A, B, and PARITY	V_{CC} = 5.5 V, V_I = 2.7 V				70			70	μA
	T/$\overline{R}$ and $\overline{G}$					40			40	
	ODD/$\overline{EVEN}$					20			20	
I_{IL}‡	A, B, and PARITY	V_{CC} = 5.5 V, V_I = 0.5 V				−70			−70	μA
	T/$\overline{R}$ and $\overline{G}$					−40			−40	
	ODD/$\overline{EVEN}$					−20			−20	
I_{OZH}	$\overline{ERROR}$	V_{CC} = 5.5 V, V_I = 2.7 V				50			50	μA
I_{OZL}	$\overline{ERROR}$	V_{CC} = 5.5 V, V_I = 0.5 V				−50			−50	μA
I_{OS}§	A1 thru A8	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8			−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V			90	125		90	125	mA
I_{CCL}		V_{CC} = 5.5 V			106	150		106	150	mA
I_{CCZ}		V_{CC} = 5.5 V			98	145		98	145	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F657			SN54F657		SN74F657		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	5.1	7.5			1.7	8	ns
t_{PHL}			2.2	5.6	7.5			2.2	8	
t_{PLH}	A_n	PARITY	6.2	9.6	14			6.2	16	ns
t_{PHL}			6.2	9.6	15			6.2	16	
t_{PLH}	ODD/$\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERROR}}$	3.7	7.1	11			3.7	12	ns
t_{PHL}			3.7	7.6	11.5			3.7	12.5	
t_{PLH}	B_n	$\overline{\text{ERROR}}$	7.2	13.6	20.5			6.7	22.5	ns
t_{PHL}			7.2	13.6	20.5			6.7	22.5	
t_{PLH}	PARITY	$\overline{\text{ERROR}}$	7.2	11.1	15.5			6.7	16.5	ns
t_{PHL}			7.2	11.6	15.5			7.2	17	
t_{PZH}	$\overline{G}$	A_n, B_n, or PARITY	2.2	5.1	8			2.7	9	ns
t_{PZL}			3.2	6.6	9.5			3.2	11	
t_{PHZ}	$\overline{G}$	$\overline{\text{ERROR}}$	1.2	4.1	7.5			1.2	8	ns
t_{PLZ}			1.2	3.6	6			1.2	6.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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Introduction

Military system functionality in a radiation environment is becoming more of a design criteria. System designers have a need for comparative IC radiation tolerance data, because exposure to gamma radiation degrades the performance of integrated circuits. The amount of performance degradation for various manufacturers' logic families is variable as process technologies differ. So comparison studies that expose various vendors' logic devices to radiation can be used to determine a logic family's suitability for use in a system. These studies may, in fact, influence the selection of product for design-in.

There are numerous guidelines/methods for radiation testing. Also, there is room for interpretation regarding the failure modes of logic devices. Some IC manufacturers choose to define radiation induced failure as the total-dose level at which a logic error occurs. Others define failure at the point at which data sheet parametrics are exceeded. In addition, variable test methodologies make direct comparisons of existing studies difficult. Therefore, many OEMs have developed their own radiation test schemes to assure program compliance.

However, it is helpful to have some generic radiation data to use as comparisons for initial selection of logic families for new designs. To that end, the following is offered as a guide for that selection process. The data is presented in two sections . . . (1) Results of testing done by Texas Instruments and (2) Results of testing done by a third-party OEM and printed herein with their permission. The comparisons are necessarily generic and any conclusions that are drawn from the data may warrant further investigation. Results of the tests do indicate that TI's F Logic product is more radiation tolerant than currently available FAST™ product.

Testing Performed by TI

Failure to meet data sheet parametric specifications is one consequence of exposing devices to radiation. After a device is irradiated, typically the first parametric specification to be violated is the input leakage current, as it will increase beyond the maximum data book limit. Therefore, for the radiation tolerance tests done by TI, the parameter monitored was I_{IH}. The data book maximum limit for this parameter is 20 μA for the F Logic family. In typical system applications with 10 unit loads, 200 μA is considered a representative value for I_{IH}. Test conditions simulated a total dose radiation environment.

FAST is a registered trademark of National Semiconductor Corporation.

Both the supply voltage (V_{CC}) and the inputs were kept at 5.5 V during irradiation. The dose rate was 201.9 rad(Si)/second and the highest readings in each sample of four units of each device type ('54F00, '54F74, '54F244) are tabulated below (see Table 1). Initial tests were done with total doses of 50, 100, 200, and 1000 krads(Si). However, some devices were beyond the 20 μA data book limit at the 50 krad(Si) total dose level, so an additional test point of 20 krads(Si) was added. A few tests were stopped at 200 krads(Si) because the devices read over the full-scale tester capability of 3031 μA. Full MIL-STD-883C compliant product from each vendor was used, except where indicated.

The following specific devices and date codes were subjected to the radiation testing:

Texas Instruments	Date Code
'54F00	B8735Z
'54F74	8647
'54F244	8706

Fairchild Semiconductor	Date Code
'54F00	8430, Recertification tested 8604
'54F74	Non-883C compliant P-DIP, 8718
'54F244	8641

Motorola Inc.	Date Code
'54F00	8513B
'54F74	8640A
'54F244	8619B

Signetics Corporation	Date Code
'54F00	8717
'54F74	8648
'54F244	8644

Table 1. Relative Radiation Tolerance

'54F00				
PARAMETER	**TEXAS INSTRUMENTS**	**FAIRCHILD**	**MOTOROLA**	**SIGNETICS**
I_{IH} at 20 krad(Si)	–	<0.1 μA	380.1 μA	–
I_{IH} at 50 krad(Si)	14.3 μA	2.4 μA	1231.1 μA	2725 μA
I_{IH} at 100 krad(Si)	174.4 μA	283.7 μA	2214.3 μA	>3031 μA
I_{IH} at 200 krad(Si)	526.2 μA	840.1 μA	>3031 μA	>3031 μA
I_{IH} at 500 krad(Si)	834.9 μA	1408.3 μA	>3031 μA	–
I_{IH} at 1000 krad(Si)	739.5 μA	1570.8 μA	>3031 μA	–
'54F74				
I_{IH} at 20 krad(Si)	–	597.8 μA	6.95 μA	192.7 μA
I_{IH} at 50 krad(Si)	7.2 μA	>3031 μA	230.9 μA	1648.9 μA
I_{IH} at 100 krad(Si)	138.0 μA	>3031 μA	389.3 μA	>3031 μA
I_{IH} at 200 krad(Si)	475.4 μA	>3031 μA	713.1 μA	>3031 μA
I_{IH} at 500 krad(Si)	732.5 μA	–	1417.2 μA	–
I_{IH} at 1000 krad(Si)	648.4 μA	–	1528.3 μA	–
'54F244				
I_{IH} at 20 krad(Si)	–	48.6 μA	350.9 μA	59.4 μA
I_{IH} at 50 krad(Si)	0.7 μA	583.1 μA	1062 μA	280.7 μA
I_{IH} at 100 krad(Si)	64.7 μA	2972.1 μA	1650.1 μA	751.9 μA
I_{IH} at 200 krad(Si)	296.7 μA	>3031 μA	2644 μA	1296.8 μA
I_{IH} at 500 krad(Si)	560.2 μA	–	>3031 μA	1545 μA
I_{IH} at 1000 krad(Si)	525.5 μA	–	–	1395.5 μA

Supply voltage V_{CC} and input voltage V_{IH} were both 5.5 V during irradiation.
Dose rate = 201.9 rad(Si)/second
Tester full-scale limit for I_{IH} = 3031 μA MAX
Table listings were the highest I_{IH} readings obtained in each sample of four units.

Third-Party OEM Test Results†

Eight samples of the '54F04 Hex inverters and '54F11 Triple 3-input AND gates along with four samples of a '54F20 Dual 4-input NAND gate were tested in a total dose environment. They were exposed to gamma radiation and irradiated at approximately 500 rads(Si)/minute or 8 rads(Si)/second. Test data was taken every 2 krads(Si) up to 30 krads total dose. If the first four samples showed no significant degradation, then the remaining parts were irradiated at 1000 rads(Si)/minute or 16.7 rads(Si)/second and data was taken every 5 krads(Si) up to 100 krads(Si). All devices were exercised, both functionally and parametrically, using the Eagle Multiplexer with the NUGPMUX test package on the EAGLE LSI-4 Automated Test Equipment.

In addition to monitoring I_{IH}, the propagation delay (t_{pd}) of four samples of each device type was measured independently at baseline and following exposure to the highest total dose level tested . . . between 60 and 80 krads(Si). A custom propagation delay fixture was used. In all cases, one input received a 3-V amplitude square wave while the other inputs were tied to 5 V or 0 V so that the output yielded a positive square wave. The propagation delay was then measured using the 50% points of the input and output waveforms as reference. **No significant degradation was observed in any of the devices tested.**

During irradiation, the parts were statically biased with "H"s and "L"s as seen in Table 2, and dc parametric test conditions were selected according to data book specifications.

Table 2. Biasing Schemes for Devices

PART	S/N	PIN NUMBER													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
'54F04	1-4	H	X	L	X	H	X	GND	X	L	X	H	X	L	V_{CC}
	5-8	H	X	L	X	H	X	GND	X	L	X	H	X	L	V_{CC}
'54F11	1-4	H	L	H	L	H	X	GND	X	L	H	L	X	L	V_{CC}
	5-8	H	L	H	L	H	X	GND	X	L	H	L	X	L	V_{CC}
'54F20	1-4	H	L	NC	H	L	X	GND	X	H	H	NC	H	H	V_{CC}

Dosimetry data showed that each device received radiation at a slightly different dose rate due to its positioning on the multiplexer. The actual exposure is shown in Table 3.

†Only Texas Instruments Incorporated product was used in the study.

Table 3. Actual Dose Rates

DEVICE TYPE	S/N	DOSE RATE (rads(Si))	AVERAGE	Δ%—POSITION
'54F04	1	472	496	12.5
	2	498		
	3	484		
	4	531		
	5	939	1011	16
	6	1003		
	7	1016		
	8	1089		
'54F11	1	472	496	12.5
	2	498		
	3	484		
	4	531		
	5	1038	1144	25.5
	6	1090		
	7	1145		
	8	1303		
'54F20	1	1038	1144	25.5
	2	1090		
	3	1145		
	4	1303		

The minimum, mean, and maximum values for all parameters are shown for all device types in Tables 4 through 9. Table 4 and Figure 1 exhibit the input leakage current for the '54F04. Similarly, Tables 5 and 6 and Figures 2 and 3 represent the parametric performance for the I_{IH} and I_{CC} for the '54F20 respectively. And finally, Tables 7 thru 9 and Figures 4 thru 9 correspond to I_{IH}, I_{CC} and V_{OH} of the '54F11.

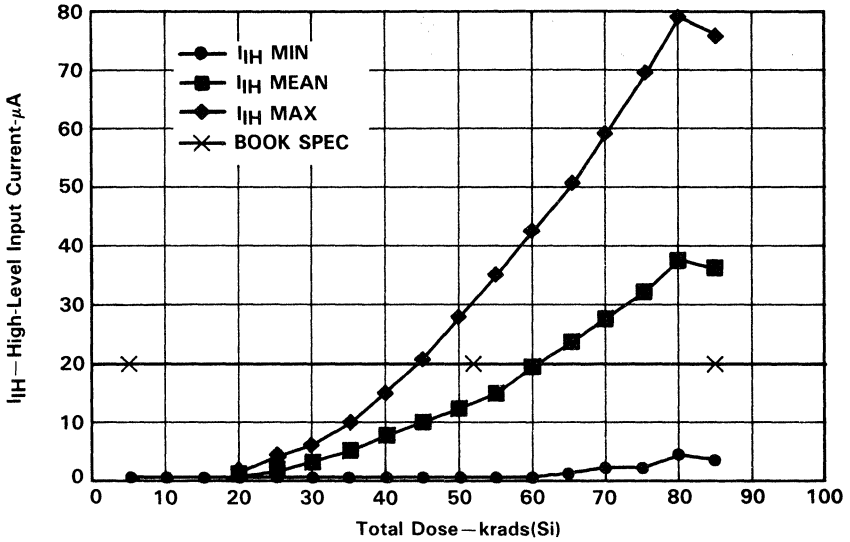

Figure 1. High-Level Input Current vs Total Dose — '54F04

Table 4. High-Level Supply Current vs Total Dose — '54F04

TOTAL DOSE	I_{IH} (μA) @ V_I = 2.7 V		
IN krads(Si)	MIN	MEAN	MAX
00	0.20	0.20	0.20
05	0.20	0.20	0.20
10	0.20	0.20	0.20
15	0.20	0.20	0.20
20	0.20	0.30	0.60
25	0.20	1.10	2.60
30	0.20	2.50	5.80
35	0.20	4.50	10.30
40	0.20	6.80	15.30
45	0.20	9.50	21.10
50	0.20	12.40	27.50
55	0.50	15.70	34.50
60	0.80	19.30	42.20
65	1.20	23.30	50.40
70	1.80	27.70	59.30
75	2.60	32.30	68.60
80	3.60	37.20	77.80
85	3.20	35.90	75.50
BOOK SPEC	—	—	20.00

PART NUMBER: '54F04 S/N 5-8
DATE CODE: A8709
VENDOR: TI
TEST DATE: 3-OCT-88

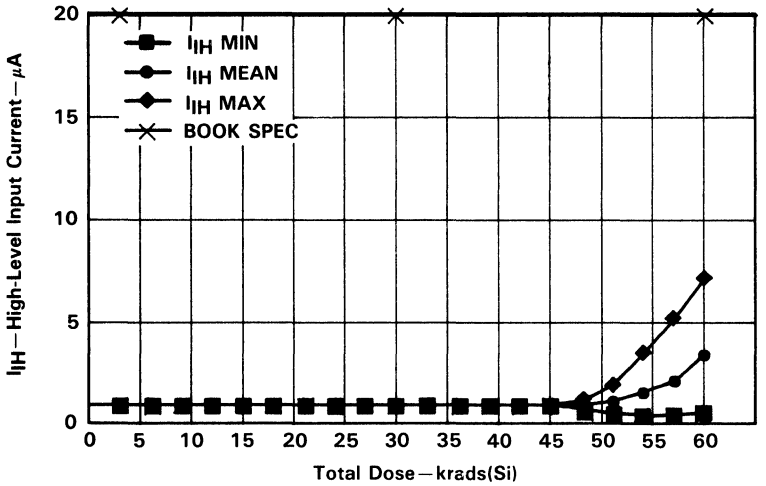

Figure 2. High-Level Input Current vs Total Dose — '54F20

Table 5. High-Level Input Current vs Total Dose — '54F20

TOTAL DOSE	I_{IH} (μA) @ V_I = 2.7 V		
IN krads(Si)	MIN	MEAN	MAX
00	0.50	0.50	0.50
03	0.50	0.50	0.50
06	0.50	0.50	0.50
09	0.50	0.50	0.50
12	0.50	0.50	0.50
15	0.40	0.50	0.50
18	0.50	0.50	0.50
21	0.50	0.50	0.50
24	0.50	0.50	0.50
27	0.50	0.50	0.50
30	0.50	0.50	0.50
33	0.50	0.50	0.50
36	0.50	0.50	0.50
39	0.40	0.50	0.50
42	0.40	0.50	0.50
45	0.40	0.40	0.40
48	0.30	0.50	0.90
51	0.30	0.80	1.80
54	0.30	1.40	3.20
57	0.30	2.20	4.90
60	0.50	3.30	7.20
BOOK SPEC	—	—	20.00

PART NUMBER: '54F20 S/N 1-4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

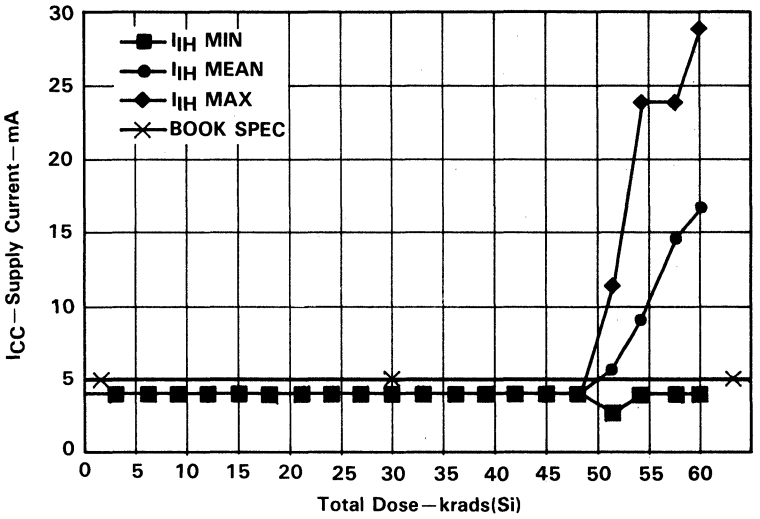

Figure 3. Supply Current vs Total Dose — '54F20

Table 6. Supply Current vs Total Dose — '54F20

TOTAL DOSE IN krads(Si)	I_{CCH} (mA) @ V_{CC} = 5.5 V		
	MIN	MEAN	MAX
00	3.962	4.007	4.042
03	3.958	4.003	4.040
06	3.954	4.000	4.037
09	3.946	3.996	4.043
12	3.948	3.994	4.032
15	3.945	3.992	4.029
18	3.941	3.990	4.028
21	3.940	3.988	4.026
24	3.941	3.987	4.024
27	3.937	3.985	4.023
30	3.936	3.983	4.021
33	3.936	3.983	4.020
36	3.933	3.981	4.019
39	3.932	3.979	4.017
42	3.932	3.979	4.017
45	3.931	3.979	4.017
48	3.930	3.978	4.015
51	3.078	5.667	11.629
54	3.974	8.782	23.159
57	4.015	14.447	23.243
60	4.015	16.910	28.721
BOOK SPEC	—	—	5.100

PART NUMBER: '54F20 S/N 1-4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

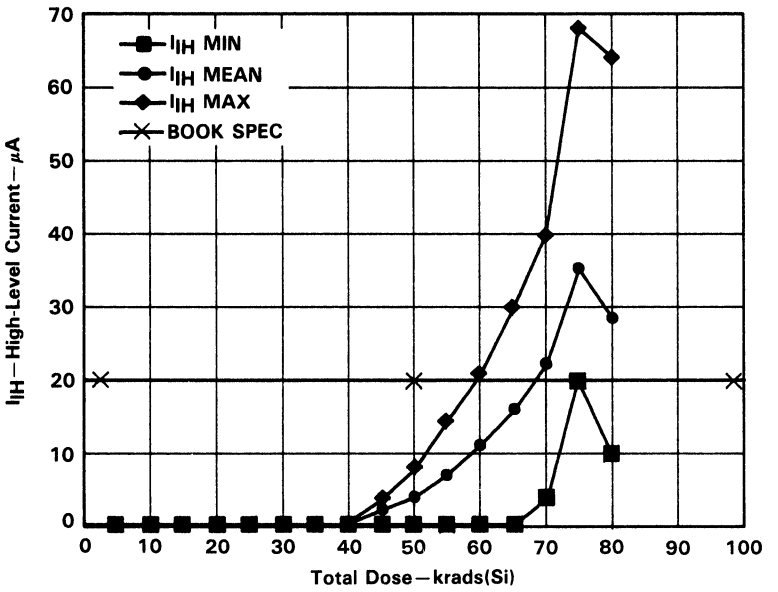

Figure 4. High-Level Input Current vs Total Dose — '54F11

Table 7. High-Level Input Current vs Total Dose — '54F11

TOTAL DOSE	I_{IH} (μA) @ V_I = 2.7 V		
IN krads(Si)	MIN	MEAN	MAX
00	0.50	0.50	0.50
05	0.50	0.50	0.50
10	0.50	0.50	0.50
15	0.50	0.50	0.50
20	0.50	0.50	0.50
25	0.50	0.50	0.50
30	0.40	0.40	0.50
35	0.40	0.40	0.40
40	0.40	0.70	1.10
45	0.40	1.70	3.60
50	0.40	3.60	7.50
55	0.50	6.80	13.40
60	0.90	11.00	20.90
65	0.70	16.00	29.80
70	4.20	22.70	40.00
75	20.60	45.10	66.80
80	10.40	38.40	64.20
BOOK SPEC	—	—	20.00

PART NUMBER: '54F11 S/N 5-8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

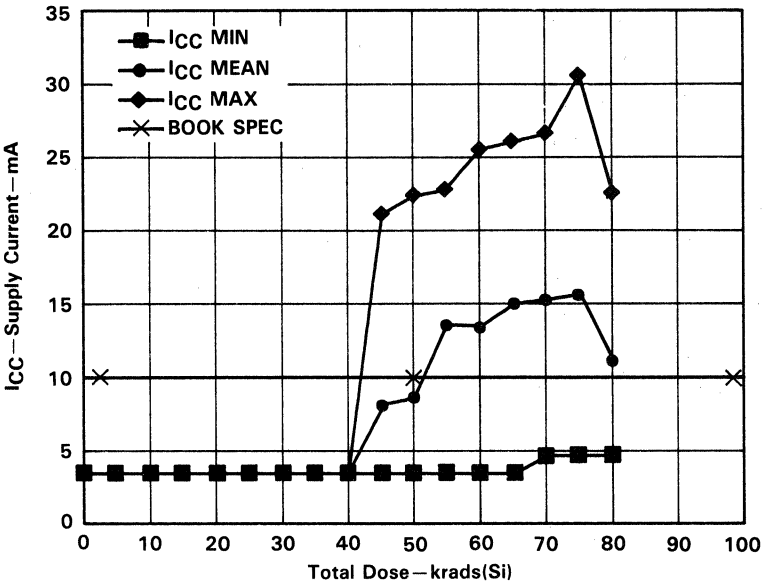

Figure 5. Supply Current vs Total Dose — '54F11

Table 8. Supply Current vs Total Dose — '54F11

TOTAL DOSE	I_{CCH} (mA) @ V_{CC} = 5.5 V		
IN krads(Si)	MIN	MEAN	MAX
00	3.41	3.48	3.55
05	3.41	3.48	3.55
10	3.41	3.47	3.54
15	3.40	3.50	3.53
20	3.39	3.46	3.53
25	3.40	3.47	3.54
30	3.40	3.47	3.54
35	3.39	3.47	3.54
40	3.41	3.46	3.50
45	3.41	7.94	21.43
50	3.37	8.20	22.57
55	3.34	12.94	22.92
60	3.35	12.82	25.49
65	3.36	14.91	26.54
70	4.61	15.16	26.96
75	4.62	15.52	30.53
80	4.63	11.10	22.70
BOOK SPEC	—	—	9.70

PART NUMBER: '54F11 S/N 5-8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

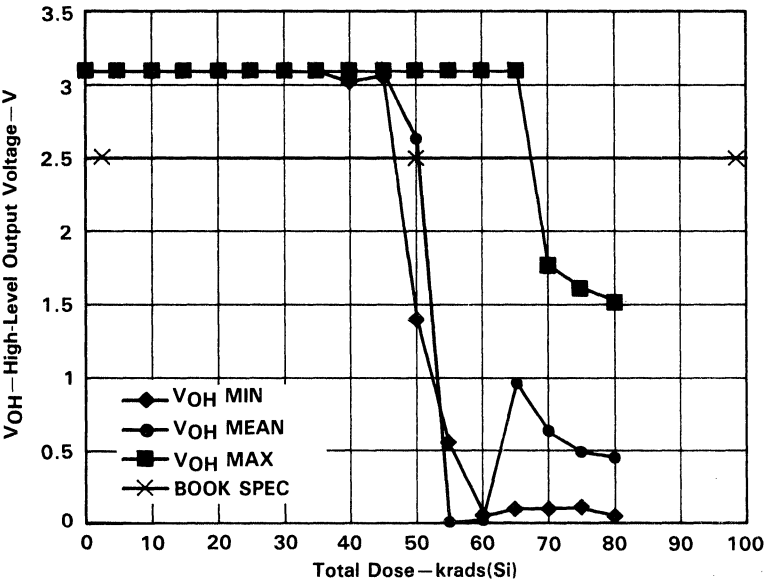

Figure 6. High-Level Output Voltage vs Total Dose — '54F11

Table 9. High-Level Output Voltage vs Total Dose — '54F11

TOTAL DOSE IN krads(Si)	V_{OH} @ I_{OH} = −1 mA		
	MIN	MEAN	MAX
00	3.063	3.066	3.069
05	3.064	3.067	3.072
10	3.064	3.068	3.073
15	3.065	3.069	3.074
20	3.065	3.069	3.074
25	3.065	3.069	3.074
30	3.065	3.069	3.074
35	3.065	3.070	3.077
40	3.011	3.056	3.077
45	3.069	3.073	3.082
50	1.411	2.657	3.075
55	0.551	0.035	3.076
60	0.076	0.032	3.073
65	0.150	0.994	3.073
70	0.150	0.654	1.719
75	0.150	0.512	1.597
80	0.051	0.469	1.523
BOOK SPEC	2.500	—	—

PART NUMBER: '54F11 S/N 5-8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

Summary

The tests performed by Texas Instruments can be used as a gauge of relative radiation tolerance of various vendor's 54F-type logic families. Defining the data sheet parametric failure points, as opposed to defining the points where logic errors occur, was the basis for both studies. Test results do indicate that the TI 54F logic family is more radiation tolerant within the constraints of the parameters monitored. Significantly lower I_{IH} readings were recorded for TI 54F logic devices at several total dose levels. An additional point for comparison is the data contained in the third-party OEM study.

The study that was performed by the third-party OEM gives a definition of radiation tolerance of TI 54F devices that is based on additional data sheet parametrics. Although no functional failure was observed in any of the eight samples of the devices tested, the dc parametrics did show some degradation. Again, the various parameters monitored were the input leakage current (I_{IH}), the supply current (I_{CC}), and the output voltage (V_{OH}). Data sheet parametric failures for input leakage current for the '54F04, '54F11, and '54F20 were exhibited at 65, 60, and 70 krads(Si) total dose, respectively. Also, the supply current exceeded data book specifications at 51 and 55 krads(Si) for the '54F20 and '54F11, respectively. No significant degradation was observed in the supply current for the '54F04 to 85 krads(Si). The output voltage (V_{OH}) for the '54F11 fell below the data book minimum specified value at total dose levels exceeding 45 krads(Si). Finally, no degradation in propagation delays (t_{pd}) was observed in any of the devices irradiated.

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Application Report 3

Mechanical Data 4

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Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54F240 J —00†

1. Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN	Standard Prefix
SNJ	MIL-STD-883 Processed and Screened per JEDEC Standard 101
JANB	MIL-M-38510 Processed

2. Unique Circuit Description

MUST CONTAIN SIX TO NINE CHARACTERS

Examples: 54F620
74F125
74F657

3. Package

MUST CONTAIN ONE OR TWO LETTERS

J, JT, N, NT (Dual-in-line Packages)‡
D, DW ("Small Outline" Packages)
FK (Leadless Ceramic Chip Carriers)
(From pin-connection diagram on individual data sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

—00 No special instructions
—10 Solder-dipped leads (N and NT packages only)

†For tape and reel information contact the factory.
‡These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

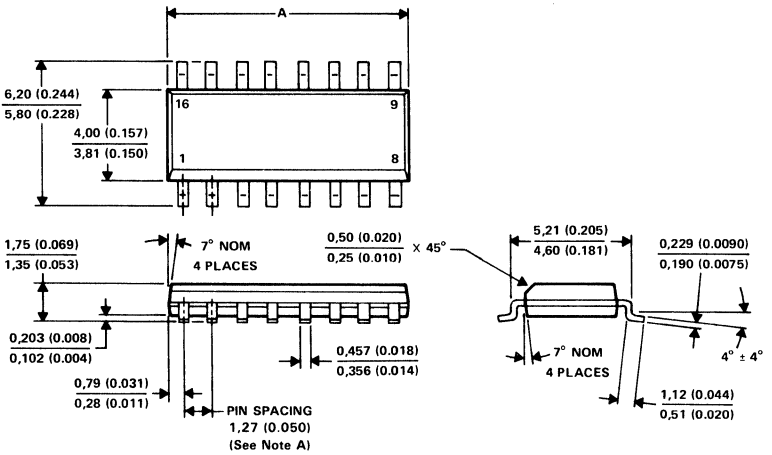
Dual-in-line (J, JT, N, NT)

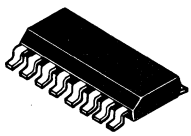
—Slide Magazines
—A-Channel Plastic Tubing
—Barnes Carrier (N only)
—Sectioned Cardboard Box
—Individual Plastic Box

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

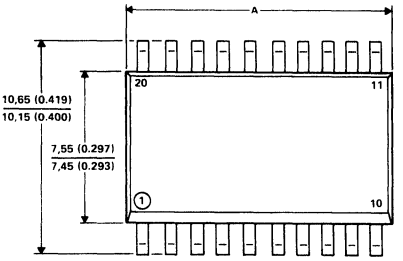
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

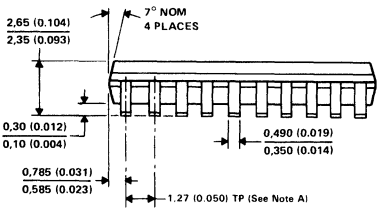
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

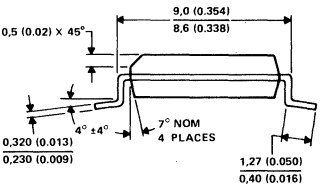
DW016, DW020, DW024, and DW028 plastic "small outline" packages

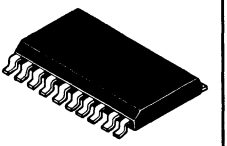
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)









DIM \ PINS	16	20	24	28†
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

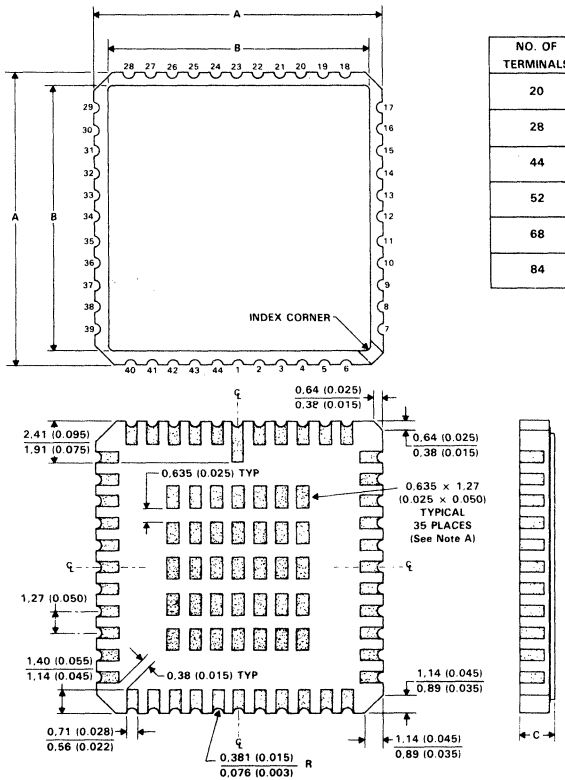
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FD and FK leadless ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC standards 1, 2, and 11.

44-TERMINAL FD and FK



FD AND FK PACKAGES

NO. OF TERMINALS	A MIN	A MAX	B MAX	C MIN	C MAX
20	8,69 (0.342)	9,09 (0.358)	9,09 (0.358)	1,63 (0.064)	2,03 (0.080)
28	11,23 (0.442)	11,63 (0.458)	11,63 (0.458)	1,63 (0.064)	2,03 (0.080)
44	16,26 (0.640)	16,76 (0.660)	14,22 (0.560)	1,75 (0.069)	3,05 (0.120)
52	18,78 (0.739)	19,33 (0.761)	14,22 (0.560)	2,08 (0.082)	3,05 (0.120)
68	23,83 (0.938)	24,43 (0.962)	21,89 (0.862)	2,08 (0.082)	3,05 (0.120)
84	28,83 (1.135)	29,59 (1.165)	27,05 (1.065)	2,08 (0.082)	3,05 (0.120)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: The checkerboard pattern is aligned vertically with the contact pads and is symmetrical horizontally as shown; it is applicable to some 44-terminal packages only.

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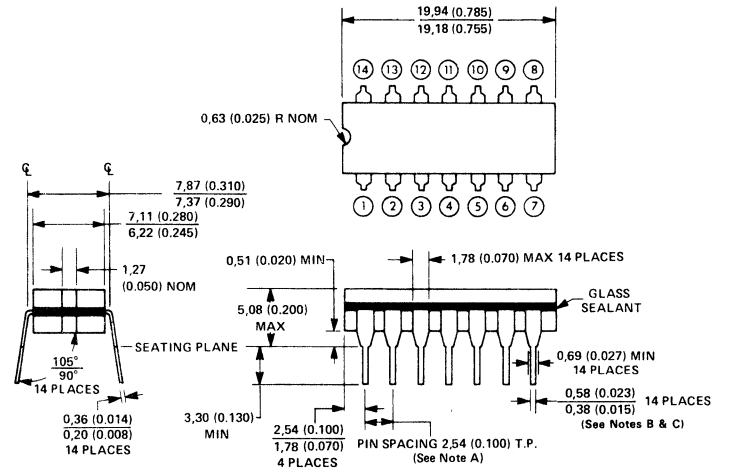
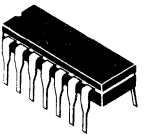
J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

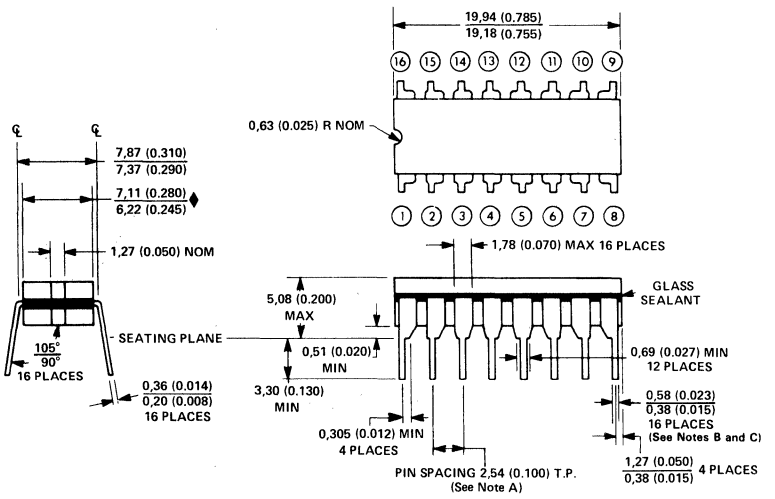
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

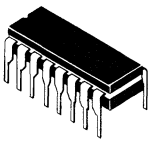
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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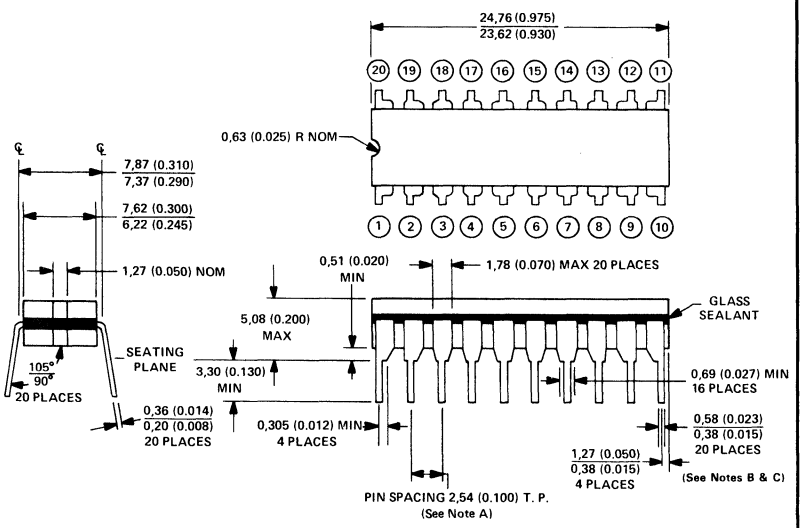
J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J020



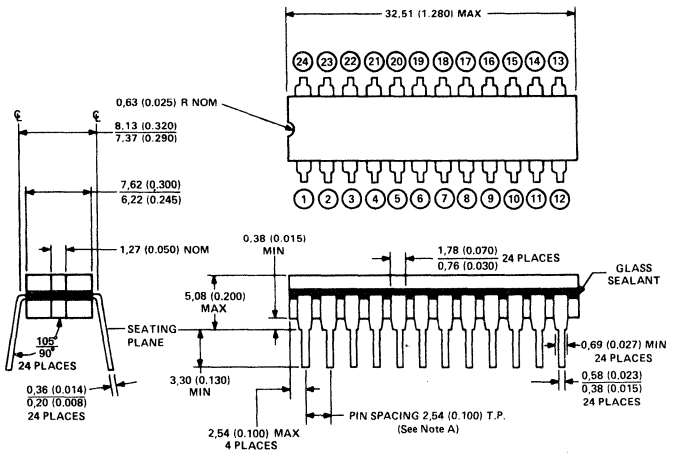
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

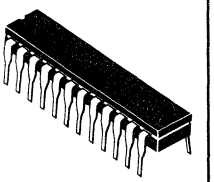
JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') pins require no additional cleaning or processing when used in soldered assembly.

JT024



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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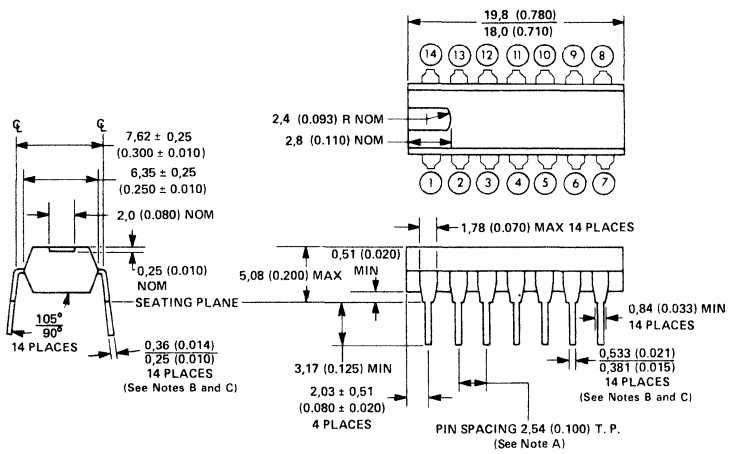
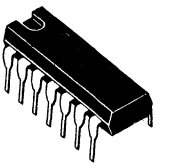
N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





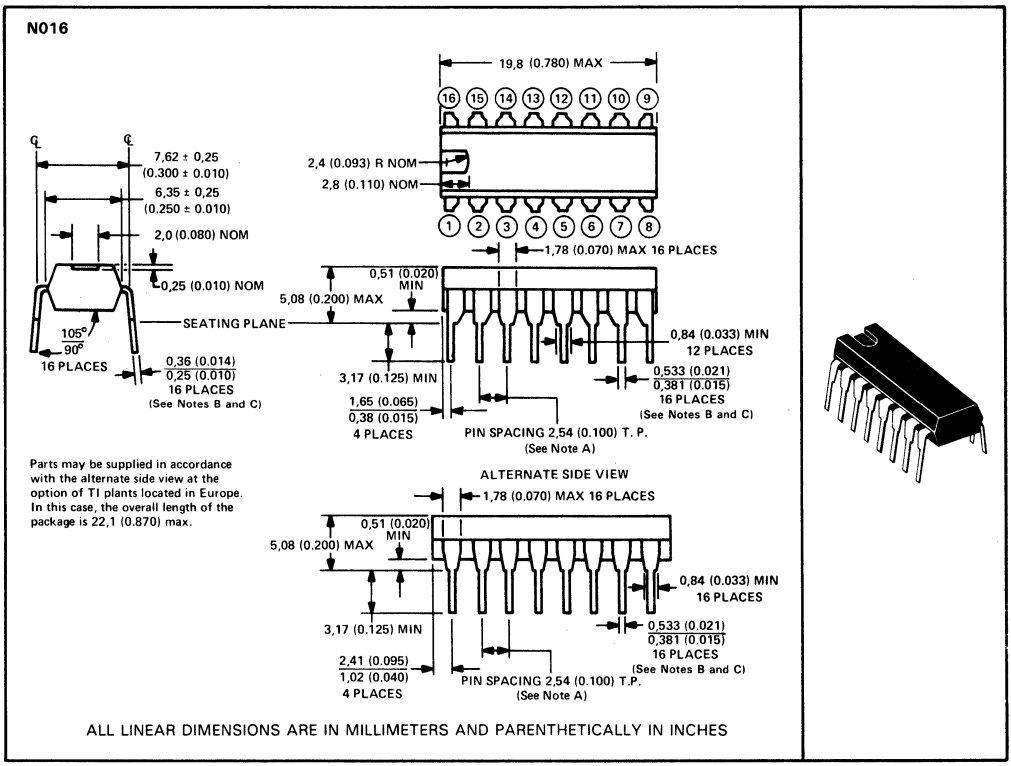
Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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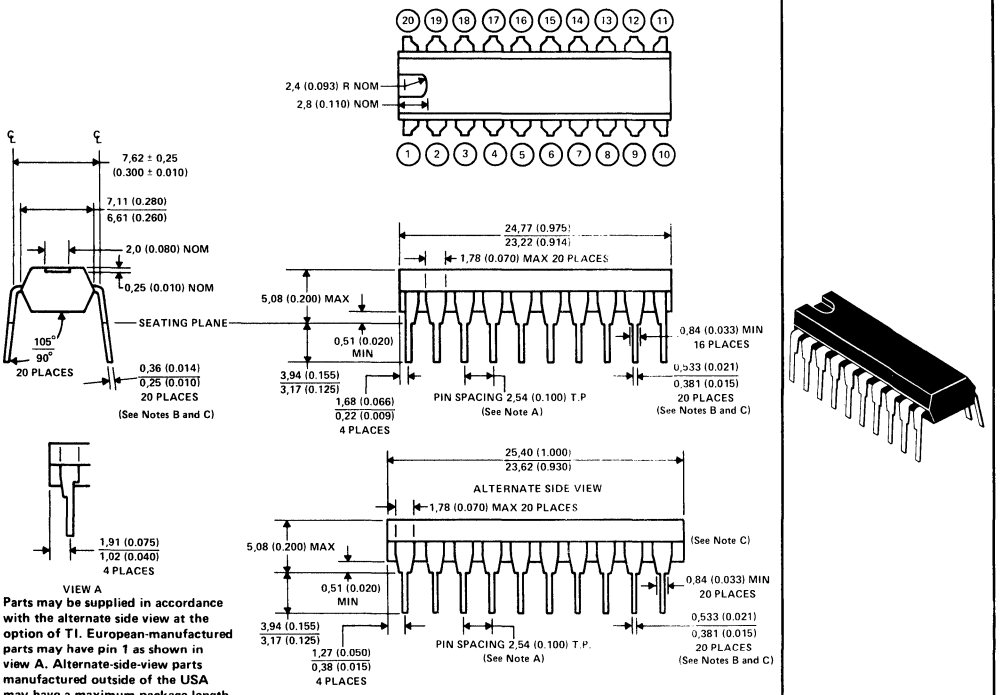
N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N020



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

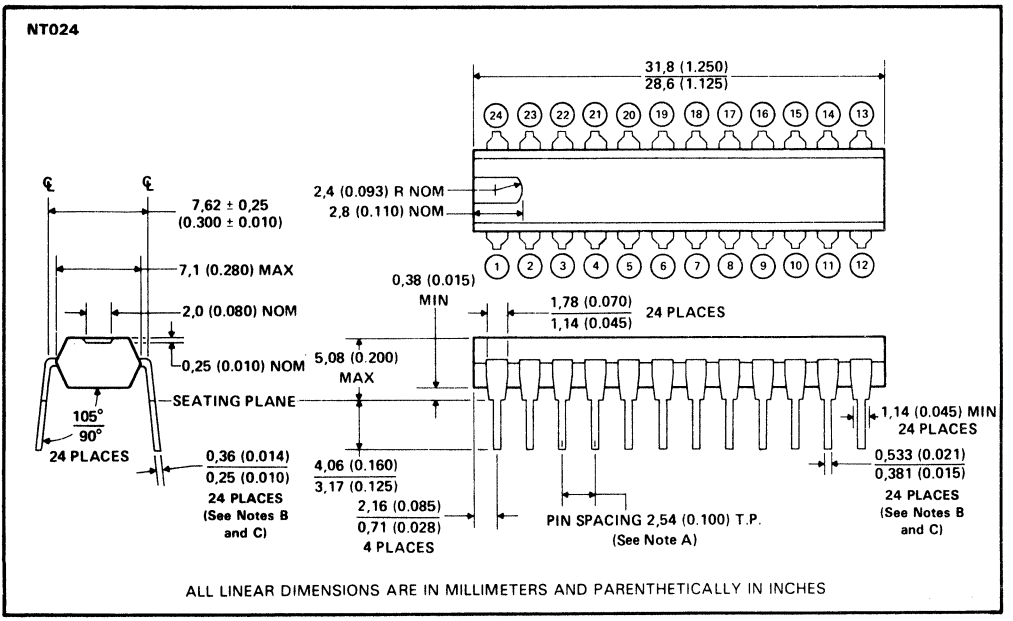
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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Tape and Reel Information

A new packaging system, *SMti*™ Tape and Reel, has emerged along with the introduction of surface-mount semiconductor packages by Texas Instruments.

Benefits

SMti Tape and Reel not only offers a new shipping method that protects components from mechanical and electrical damage, but also includes the benefits of automated inventory control, ship to stock, and total compatibility with today's automated placement systems. *SMti* Tape and Reel continues the trend towards industry automation and cost reduction and contributes to the overall goal of electronic system quality and reliability.

Features

The features of *SMti* Tape and Reel packaging are as follows.

- *SMti* Tape and Reel packaging is in full compliance with EIA Standard RS-481-A, "Taping of Surface-Mount Components for Automatic Placement."
- Industry-compatible tape format allows second sourcing without costly and time-consuming equipment changeovers and record-keeping changes.
- Static-inhibiting materials used in carrier tape manufacture provide device protection from static damage.
- Rigid, dust-free polystyrene reels provide mechanical protection and clean room compatibility for optimum equipment operation and manufacturing yield.
- Completely compatible with dereeling equipment currently available on most high-speed automated placement systems.
- Medium-density Code 39 bar coding enables inventory and manufacturing automation, as well as complete component traceability prior to, during, and after system manufacture.
- Efficient packaging offers savings in storage space and manufacturing overhead.

SMti SURFACE MOUNT TEXAS INSTRUMENTS and *SMti* are trademarks of Texas Instruments Incorporated.

General Description

***SMti* Tape and Reel offers users of surface-mounted semiconductor devices a new and efficient method of component handling. Tape and reel consists of three major elements: a carrier tape, a cover tape, and a reel.**

Carrier Tape

The carrier tape is a conductive material with custom-embossed pockets for a particular surface-mount package. Components are oriented in the embossed pockets per EIA Standard RS-481-A "Taping of Surface-Mount Components for Automatic Placement."

Cover Tape

With each component in its embossment and protected from mechanical and static damage, a continuous transluscent cover tape is heat sealed over the entire length of the carrier tape, isolating each component from the outside environment. This heat-sealing process guarantees sufficient seal strength to prevent components from falling from the pockets before use. The cover tape has a peel strength of 40 ±30 grams in compliance with RS-481-A and sufficient strength to ensure consistency during dereeling operations.

Reel

The entire assemblage is wound on a high-strength polystyrene-based reel. The reel provides a means of easy storage and handling as well as a method for feeding large quantities of packages to high-speed placement systems. In addition, *SMti* Tape and Reel offers a factory-automation alternative through the use of medium-density Code 39 bar coding on all reel assemblies. The bar code provides source, part number, date code, and quantity.

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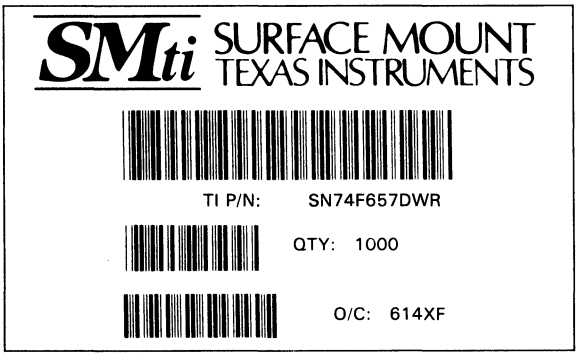
Bar-Code Labeling

Each reel of *SMti* components is labeled with a "man-and-machine" readable label that uses a medium-density Code 39 bar code in combination with alphanumeric characters.

Figure 1 ***Bar-Code Label***



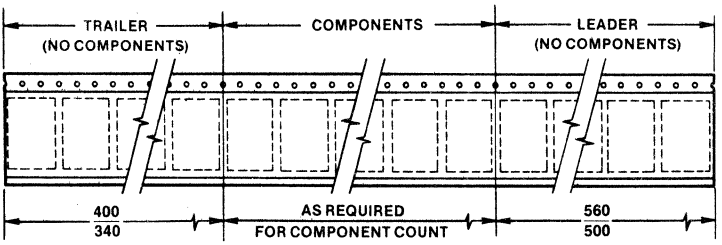
Note

1. Sample labels are available for system compatibility testing.

Specification

SMti **Tape and Reel components are available in formats that are compatible with most industry standard component loading and tape drive equipment. Figures 2 through 5 and Tables 1 through 6 provide information regarding these formats. All dimensions are given in millimeters.**

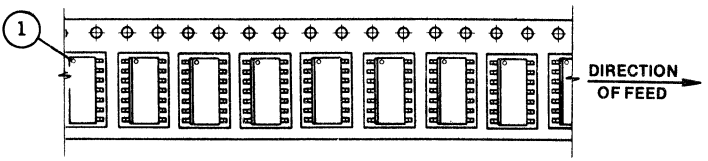
Figure 2 *Tape Format*



Notes

1. Carrier tape is conductive with a resistivity value of less than 1×10^5 ohms per square.
2. Cover tape is sealed over the entire length of the carrier tape.

Figure 3 ***Component Format*** *(All components are packaged per Note 1.)*



Note

1. Pin 1 orientation.

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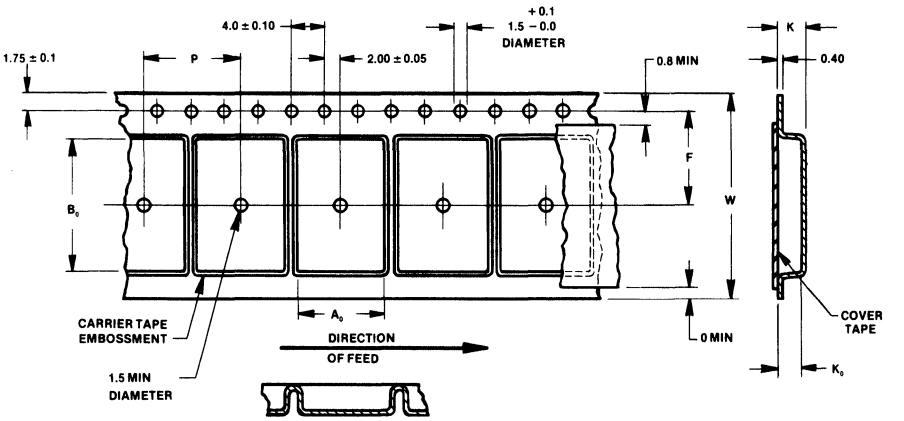
Specification (Continued)

Variables are used in Figure 4 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 4 ***Single-Sprocket Tape Dimensions***



Notes

1. Tape widths are 12, 16, and 24 mm.
2. Camber per EIA Standard RS-481-A.
3. Minimum bending radius per EIA Standard RS-481-A.

Specification (Continued)

Table 1 *Single-Sprocket Variable Tape Dimensions*

Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
SO-14	D	16	8	6.5	9.5	2.1	2.5	7.5
SO-16	D	16	8	6.5	10.3	2.1	2.5	7.5
SO-20L	DW	24	12	10.9	13.2	3.0	3.4	11.5
SO-24L	DW	24	12	10.9	15.8	3.0	3.4	11.5
SO-28L	DW	24	12	10.9	18.3	3.0	3.4	11.5
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

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Specification (Continued)

Variables are used in Figure 5 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Figure 5 *Reel Dimensions*

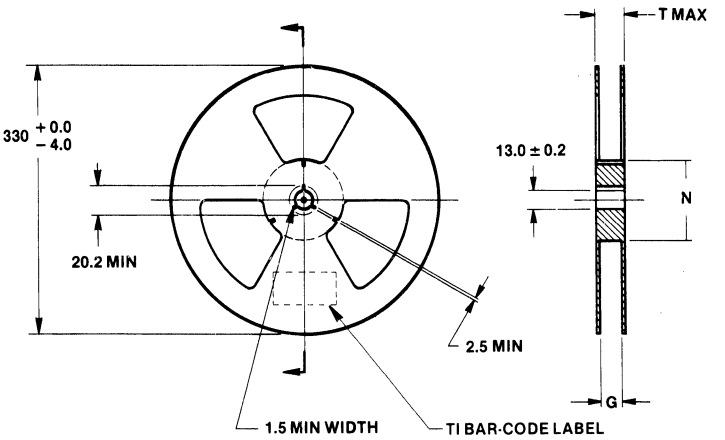

Table 2 *Variable Reel Dimensions*

Package Type	Package Designator	Dimension G	T	N
SO-14	D	16.4	22.4	100
SO-16	D	16.4	22.4	100
SO-20L	DW	24.4	30.4	100
SO-24L	DW	24.4	30.4	100
SO-28L	DW	24.4	30.4	100

Specification (Continued)

All dimensions are given in millimeters.

Table 3 *Tape and Reel Format Summary*

Package Type	Package Designator	Tape Width	Package Pitch	Pocket Width	Dimensions Length	Depth	Reel Diameter	Reel Hub Diameter	Parts Per Reel
SO-14	D	16	8	6.5	9.0	2.1	330	100	2500
SO-16	D	16	8	6.5	10.3	2.1	330	100	2500
SO-20L	DW	24	12	10.9	13.2	3.0	330	100	1000
SO-24L	DW	24	12	10.9	15.8	3.0	330	100	1000
SO-28L	DW	24	12	10.9	18.3	3.0	330	100	1000

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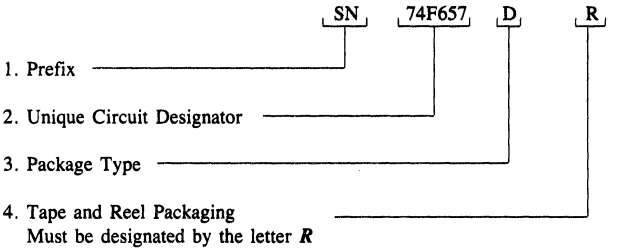
Ordering Information

To order tape and reel components, you need to provide information about part numbers, quantities, shipping, and sample package applications.

Ordering by Part Number

When ordering tape and reel components, add the letter ***R*** as a suffix to the part number. An example of the ordering sequence follows.



Formats and Quantities

All orders for tape and reel packaging **must be for whole reels.** For example, if a customer requires 9,900 TL074s in Tape and Reel packaging, he needs to place the order for a quantity of 10,000 TL074s. The order will be filled and shipped on four reels containing 2,500 parts per reel.

Note: TI reserves the right to provide a smaller quantity of devices per reel to preserve date code integrity.

A list of package and tape formats and the quantity of devices per reel is provided in Table 4.

Shipping

Taped and reeled components are shipped in individual packing boxes measuring approximately 14'' × 14''. The depth of each box is tailored to the tape width. Individual boxes are packed in a larger box whose size depends on the quantity of components ordered.

Ordering Information (Continued)

All dimensions are given in millimeters.

Table 4 *Condensed Tape and Reel Formats*

Package Type	Package Designator	Tape Width	Package Pitch	Reel Diameter	Parts Per Reel
SO-14	D	16	8	330	2500
SO-16	D	16	8	330	2500
SO-20L	DW	24	12	330	1000
SO-24L	DW	24	12	330	1000
SO-28L	DW	24	12	330	1000

Sample Package Applications

Sample components are available for a number of applications, such as standard mechanical sample packages, "daisy-chained" bars, and K-factor bars. Table 5 provides sample ordering information.

Table 5 *Sample Package Applications*

Package Type	Package Designator	Mechanical Sample	Daisy Chain	K Factor
SO-14	D	SN72197	SN200054	SN200060
SO-16	D	SN72198	SN200055	SN200061
SO-20L	DW	SN72199	SN200056	SN200062
SO-24L	DW	SN72200	SN200057	SN200063
SO-28L	DW	SN250013	N/A	N/A

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More Information

As a major manufacturer of SMCs, TI is committed to helping you make the transition to surface-mount as easy and as economical as possible. Getting started in SMT—switching from older and less efficient methods of PCB fabrication—means learning some new manufacturing techniques, and it entails some capital outlay. But in volume production, it can actually reduce your capital and space costs by up to 50 percent.

Ship-to-Stock Eliminates Incoming Inspection

As your usage per surface-mount component (SMC) grows, TI can implement its ship-to stock program for you. With all the necessary quality-control procedures built into our standard testing process, your SMCs can be shipped directly to you in tape and reel or in factory-sealed boxes. Benefits to you:

- Incoming inspection, scrap, and rework reduced or eliminated.
- Inventory reduced.
- Quality levels maximized.

Learn by Doing

To help you realize the advantages of surface-mount technology (SMT), Texas Instruments maintains a surface-mount laboratory. There you can gain hands-on experience and guidance in building a surface-mount board from start to finish. To schedule an appointment, contact your TI Field Sales Engineer or call (800) 232-3200 for the address of the TI Field Sales Office nearest you.

Outside Help Available

You can also find assistance among the growing number of SMT assembly houses, consultants, and associations. They can help you reduce the costs of converting to SMT, while supplying some valuable information on the latest technological advances and industry standards.

Suppliers of assembly equipment such as pick-and-place machines and soldering and test equipment can also help you make the transition to SMT board fabrication.

Want to Learn More?

How to Use Surface Mount Technology is available free of charge from Texas Instruments. This technical summary includes chapters on the process and the tooling required to implement it; the wide variety of available SMCs; inspection, testing, and repair; quality and reliability; and how to mix SMCs with standard DIP packages.

For additional information on the availability of TI's growing line of SMCs, contact your local TI Field Sales Office or distributor.

If you would like to have your name placed on our mailing list for additional SMT information as it becomes available from TI, please write Texas Instruments Incorporated, Dept. SSP05, P.O. Box 809066, Dallas, Texas 75380-9066.

INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-In-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Quad-In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outlilne	J Lead
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3
Attleboro, Massachusetts 02703

Telephone: (617) 699-5242/5375
TELEX: 92-7708

PERFORMANCE SPECIFICATIONS

Mechanical

Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

Electrical

Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

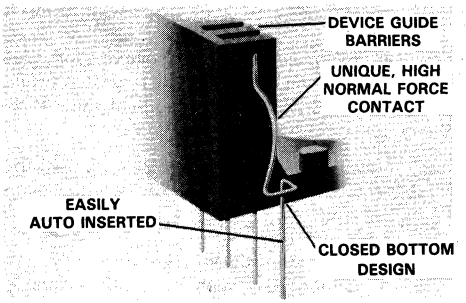
Environmental

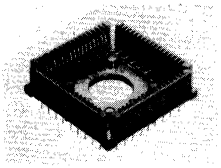
Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS

Body — Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts — CDA 510 spring temper
Contact finish — 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information



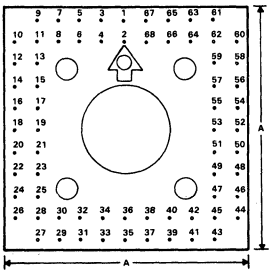


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

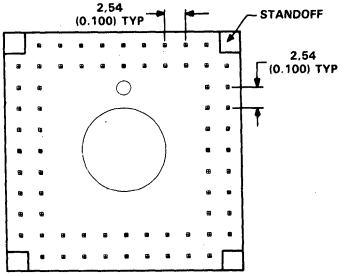
- O — Contact surface 1 — tin/lead plating
- X — Contact spacing 1 - 0.050 in
- XXX — Number of pos (044, 052, 068, 084)
- PH — Plated thru hole, solder tail
- CPR — TI socket Series, Plastic leaded chip carrier

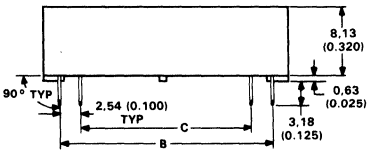
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

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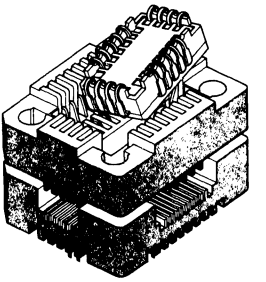
PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design



PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

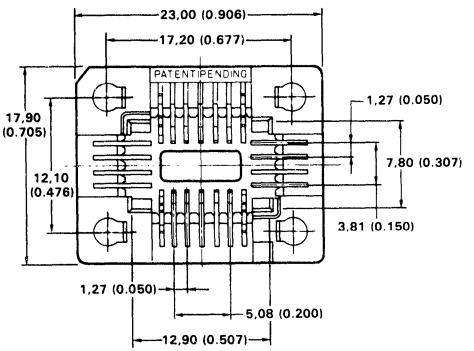
†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PART NUMBER SYSTEM

CPJ XX XX X – XXX – B

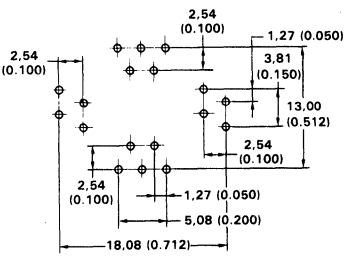
- CPJ: TI Burn-in PLCC series
- XX: Material — AA = copper alloy
- XX: Contact finish — 33 = overall gold plate
- X: Pitch — A = 0.050
- XXX: Number of contacts

PLCC BURN-IN/TEST SOCKETS CPJ SERIES

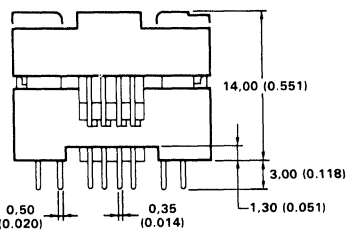


Dimensions in parentheses are inches
Contact factory for detailed information

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



PERFORMANCE SPECIFICATIONS†

Mechanical
Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

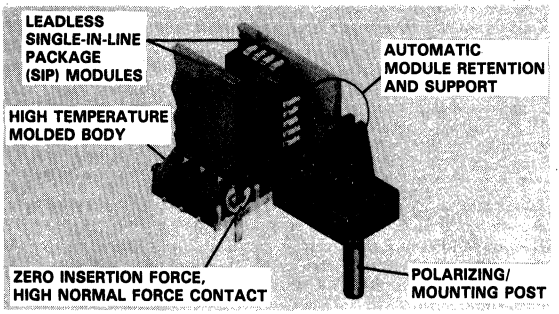
Electrical
Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

Environmental
(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS
Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 µin tin/lead over min 50µin nickel overall
Post plate min 30 µin hard gold over min 75 µin nickel overall

For additional plating options contact the factory.



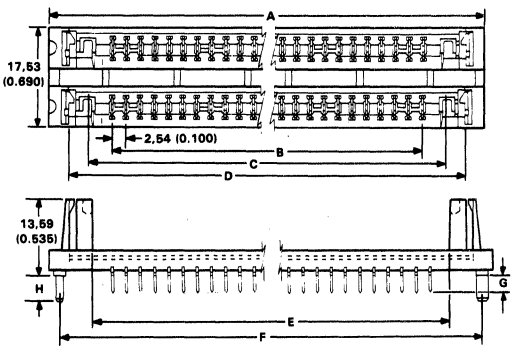
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

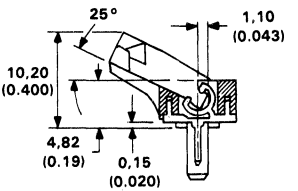
- XX (last) — Variations: 00 — standard product
- XX — Size (number of contacts per row)
- X — Housing material: A — PES
- XX — Contact base material/plating: 01—C17000/30 µin gold; 02—CA510/30 µin gold; 03—C17000/200 µin tin/lead; 04—CA510/200 µin tin/lead
- XX — Configuration/row-to-row spacing: 01—single row/N/A; 03—dual row/0.300 in; 04—dual row/0.400 in; 05—dual row/0.500 in
- TS8X — Series number denotes: 0—0.100 in pitch, vertical mount; 1—0.100 in pitch, low-profile (25°) mount

Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



SINGLE ROW LOW PROFILE



Ckt. Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Contact factory for detailed information

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

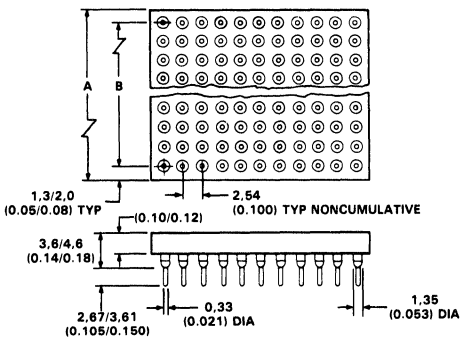
Environmental

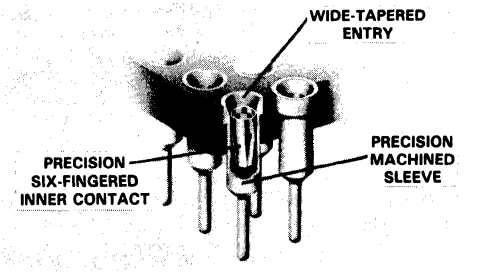
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX – XXX X X – X X

- C — TI Socket
- X — BODY MATERIAL: G — Glass Filled Epoxy; P — PBT Polyester
- G — Pin Grid Array
- XX — Overall Grid Size: 5×5=05 to 18×18=18
- XXX — Number of Pins: 024 to 324
- X — Contact Loading Pattern
- X — Body Style and Orientation

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

- X — Plating

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

- X — Pin Length

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

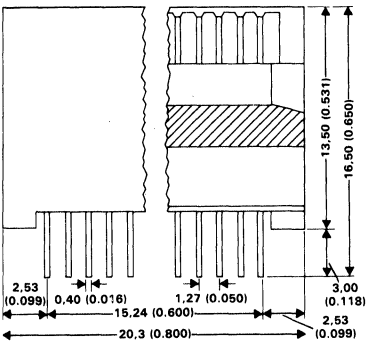
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

Environmental

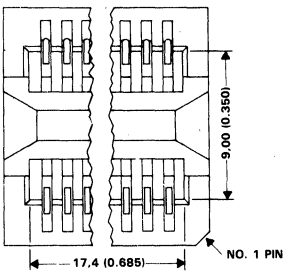
Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

MATERIALS

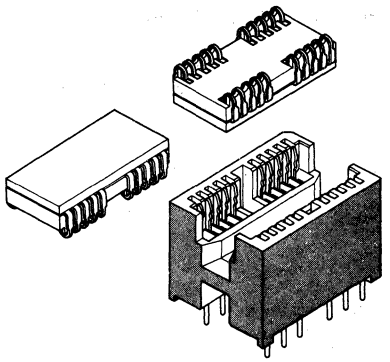
Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating



02 VERSION SHOWN



Dimensions in parentheses are inches
Contact factory for detailed information



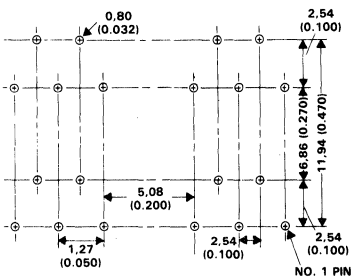
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT — TI SOJ series
- XXX — Number of Contacts
- XX — Contact Finish
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX — Body Variation
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X — Body Material
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

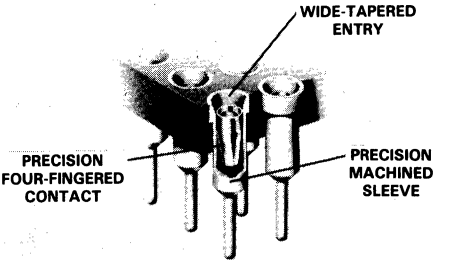
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

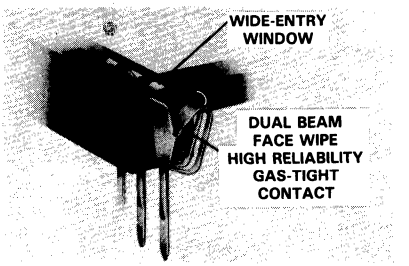


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX − X X

- X: Variations
  - Solder Tail : 9 — Pin length 0.125 Typ
  - Wire Wrap : 3 — Pin length 0.510
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- XX: Number of Positions
- (X): S — Single-in-line package (where applicable)
- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail

C86 SERIES — STAMPED AND FORMED

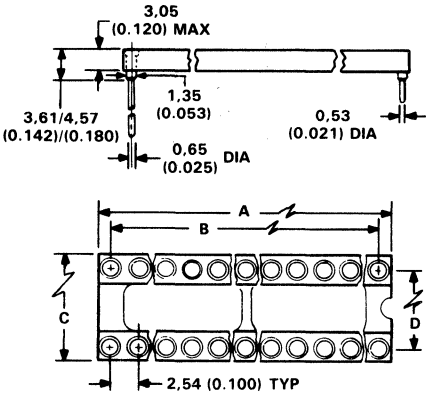


C86 SERIES PART NUMBER SYSTEM

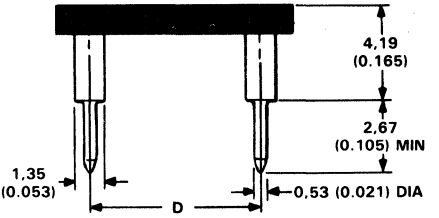
C 86 XX − 01

- 01: Variation
  - 01 — Standard product
- XX: Number of positions
- 86: Tin Dual Beam Face Wipe
- C: TI Socket Series

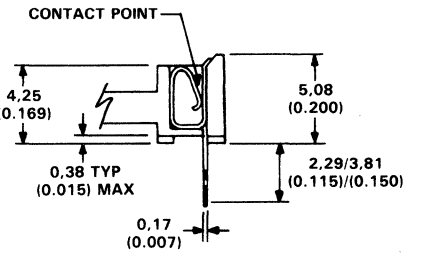
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles – CM Series, 5K cycles – CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

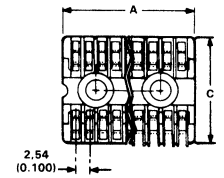
Operating temperature: –65°C to 170°C – CP/CM Series,
–65°C to 150°C – CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

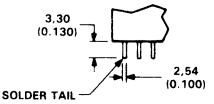
MATERIALS

Body – PPS (polyphenylen sulfide) UL 94 V-0
Contacts – Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

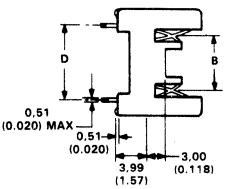
†For additional plating options consult the factory

BURN-IN/TEST DIP SOCKETS

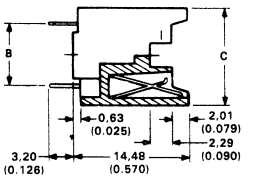




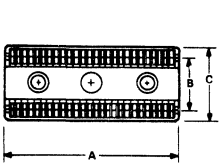
CQ37 SERIES

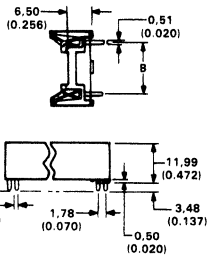


CP37 SERIES



CM37 SERIES





PART NUMBER SYSTEM

C X 37 XX – 22 S X

- X: Pin to pin — A–0.100 centers, B–0.070 centers
- S: PPS high temperature body material
- 22: Copper nickel alloy Soldertail
- XX: Number of positions
- 37: Overall gold plate
- X: Series Features — Q– Auto unloadable, P– High density mounting, M–Shrink 0.070 centers
- C: TI Socket Series

CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)	12,70 (0.500)	15,24 (0.600)	7,62 (0.300)
16	22,35 (0.880)			
18	24,89 (0.980)			
20	27,43 (1.080)			
24	32,51 (1,280)	19,05 (0.750)	22,86 (0.900)	15,24 (0.600)
28	37,59 (1.480)			
40	52,83 (2.080)			
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)	7,62 (0.300)	12,70 (0.500)
14	17,78 (0.700)		
16	20,32 (0.800)		
18	22,86 (0.900)		
20	25,40 (1.000)		
24	30,48 (1.200)	15,24 (0.600)	20,32 (0.800)
28	35,56 (1.400)		
40	50,80 (2.000)		

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)	16,51 (0.650)	23,11 (0.910)
42	39,62 (1.560)		
54	50,29 (1.980)		
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

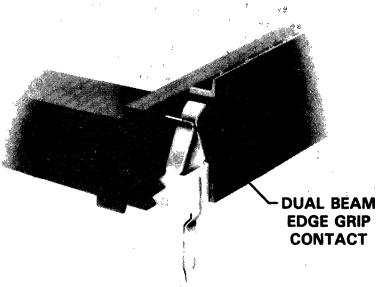
Dimensions in parentheses are inches
Contact factory for detailed information

PERFORMANCE SPECIFICATIONS

Insertion force: 16 oz (454 g) per pin max
Withdrawal force: 1.5 oz (42 g) per pin min
Operating temperature: −40°C to 100°C, tin/lead
Accommodates IC leads 0.011 ± 0.0003 in by 0.018 ± 0.003 in
Contact rating: 1 A per contact

MATERIALS

Body — PBT polyester UL 94 V-0
C4S & CxW Contacts — Copper alloy
Contact finish — Reflow tin plating, 40 μin min



PART NUMBER SYSTEM FOR CxW SERIES

C X W XX − 11

- XX: Number of contacts (42, 52, 64)
- W: Staggered leads
- X: 5 — 64 contacts; 6 — 42, 52 contacts
- C: TI Socket Series

QUAD-IN-LINE (CxW SERIES)

Product Number	A Max Length	B Row to Row	C Max Row to Row
C5W64-11	41,90 (1.65)	22,90 (0.950)	19,05 (0.750)
C6W42-11	27,90 (1.10)	22,90 (0.900)	17,80 (0.700)
C6W52-11	34,30 (1.35)	22,90 (0.900)	17,80 (0.700)

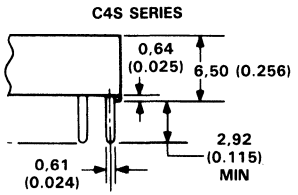
Dimensions in parentheses are inches
Contact factory for detailed information

PART NUMBER SYSTEM† FOR C4S SERIES

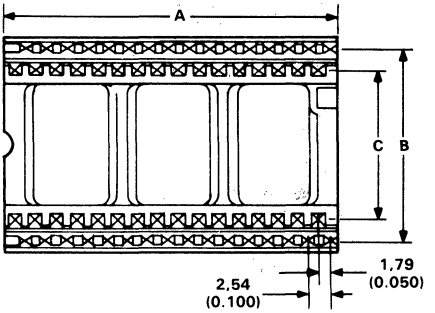
C 4 S XX − 02

- XX: Number of contacts 28, 40, 42, 52, 54, 64
- S: Shrink Pack (0.070 in pin-to-pin contact spacing)
- 4: Reflow tin plating
- C: TI Socket Series

†Also available in screw machine contacts



QUAD-IN-LINE (CxW SERIES)

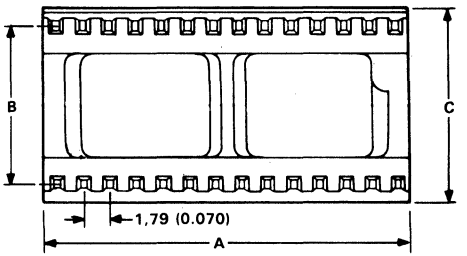


C4S SERIES

Positions	A Max Length	B Row to Row	C Max Width
28	25,02 (0.985)	10,16 (0.400)	13,00 (0.512)
40	35,69 (1.405)	15,24 (0.600)	17,98 (0.708)
64	57,07 (2.247)	19,05 (0.750)	21,62 (0.851)

Dimensions in parentheses are inches

SHRINK PACK DIP (C4S SERIES)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PERFORMANCE SPECIFICATIONS

Mechanical
Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 5000 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016

Electrical
Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

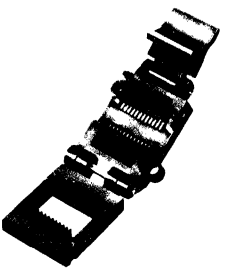
Environmental
Operating temperature: −65°C to 170°C
Humidity: 10 mΩ max contact resistance change when tested per MIL-STD 202, Method 103B
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

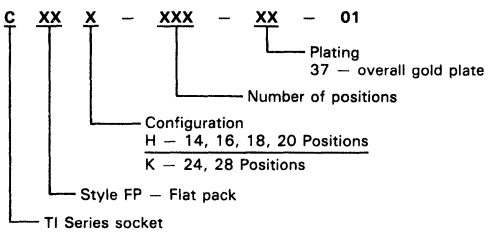
Body — CFP Series — PES (polyether sulfone) glass filled UL 94 V-0
Temperature: −65°C to 170°C
Contact — Beryllium copper
Plating:† Overall gold plate min 4 μin over min 70 μin nickel plating

†For additional plating option consult the factory.
Dimensional drawings available from factory.

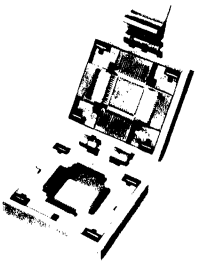
SMALL OUTLINE FLAT PACK (CFPH/K SERIES)



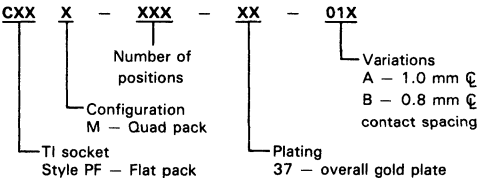
PART NUMBER SYSTEM



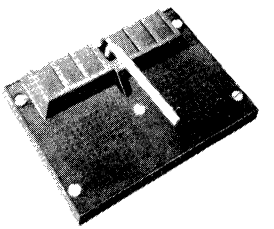
QUAD FLAT PACK (CFPM SERIES)



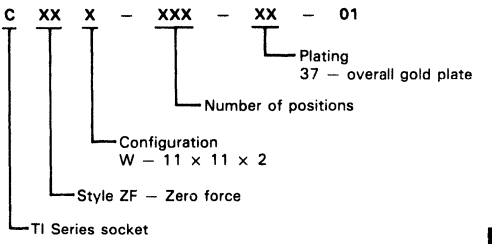
PART NUMBER SYSTEM



PIN GRID ARRAY (CZFW SERIES)



PART NUMBER SYSTEM



AVAILABLE SIZES

CFPH Series 14, 16, 18, 20 CFPK Series 24, 28	Small Outline Flat Pack
CFPM Series 64, 80	Quad Flat Pack
CZFW Series 11 x 11 x 2	Pin Grid Array

Contact factory for detailed information

TI Sales Offices

ALABAMA: Huntsville (205) 837-7530.

ARIZONA: Phoenix (602) 995-1007;
Tucson (602) 292-2640.

CALIFORNIA: Irvine (714) 660-1200;
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San Diego (619) 278-9601;
Santa Clara (408) 980-9000;
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Woodland Hills (818) 704-7759.

COLORADO: Aurora (303) 368-8000.

CONNECTICUT: Wallingford (203) 269-0074.

FLORIDA: Altamonte Springs (305) 260-2116;
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Schweber (205) 895-0480.

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Schweber (602) 431-0030; Wyle (602) 866-2888.

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(714) 458-5395; Schweber (818) 880-9686;
(714) 863-0200, (213) 320-8090; Wyle (818) 880-9000,
(714) 863-9953; Zeus (714) 921-9000; (818) 889-3838;
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Wyle (916) 638-5282;
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