Texas Instruments

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FPGA

Data Manual

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Application Specific Products

Field Programmable Gate Array Data Manual

Texas Instruments

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INTRODUCTION

This data book contains technical information on the Texas Instruments (TI) Field Programmable Gate Array (FPGA) product. This line of products from TI offers designers the ease of use and quick time to market of Programmable Logic Devices, along with performance and high density of gate arrays.

TI FPGAs are based on antifuse technology. The antifuse provides programmability to the device and offers great advantage for high density and performance at low cost.

This family of products contains three series of devices: TPC10, TPC12, and TPC14. The TPC10 Series offers four devices: TPC1010A and TPC1020A (1.2-µm double-level metal technology) and TPC1010B and TPC1020B (1.0-µm double-level metal technology). These devices provide a capacity of 1200 and 2000 gate array equivalent gates respectively. The TPC12 Series offers three devices: TPC1225A with 2500 gates, TPC1240 with 4000 gates, and the TPC1280 with 8000 gates. The TPC14 Series family offers gate capacities ranging from less than 1000 to greater than 10,000 gate array equivalent gates.

At the heart of TI's FPGA devices are the logic modules. These modules can be used to generate an array of logic gates from simple generic gates to more complicated circuits. The TPC10 Series devices use a combinatorial logic module, while the TPC12 and TPC14 Series devices use both a combinatorial and a sequential logic module. The number of logic modules used in each design vary among devices. The family's die architecture consists of rows of logic modules separated by routing tracks.

In addition to innovative hardware technology, designers with TI FPGAs use the Texas Instruments Action Logic™ System (TI-ALS) as their software design environment. Users are able to design with a variety of popular input methods on several different hardware platforms. TI-ALS then provides automatic placement and routing, timing analysis, programming capability, and functional test and debug with the ability to observe internal signals.

This book contains more detailed information on the TPC10, TPC12, and TPC14 Series product data, available TI-ALS hardware and software systems and their product descriptions, TI-ALS design flow, and general applications information.

For more information on TI's FPGA family contact your local TI Field Sales Office, TI Authorized Distributor, or call the Texas Instruments FPGA helpline at (214) 997-5666.

Preface

Read This First

About This Manual

This data manual provides detailed information on the Texas Instruments TPC Series FPGA CMOS devices. The following list summarizes the contents of the chapters in this book.

How to Use This Manual

This document contains the following chapters:

Chapter 1 **General Information**

Includes a glossary of electrical and FPGA-related terms used throughout this manual. Provides a TI FPGA product selection summary and a general overview of the TPC Series architecture.

Chapter 2 **TPC FPGA Series Data**

Presents the TPC10 and TPC12 Series individual datasheets which contain electrical and switching characteristics, mechanical drawings and packaging options, and supported library macro listings and symbols for each of the TPC Series families. Includes the TPC10 and TPC12 macro pin loading tables as well as a product preview of the TPC14 Series.

Chapter 3 **Action Logic System Overview**

Contains an overview of the TI-ALS development system environment, TI third party support, and hardware programming and debug tools. Details a step-by-step design flow through the TI-ALS software.

Chapter 4 **FPGA Design Software and Hardware**

Lists the TI-ALS system configurations and software/hardware options and provides detailed system descriptions of all the available configurations.

Chapter 5 **Quality and Reliability Data**

Provides antifuse reliability studies and graphs, under license from Actel Corporation. Details the Texas Instruments quality and reliability tests and their data reports for the TPC Series FPGA products.

Chapter 6 **Applications**

Discusses the following FPGA applications:

- ❑ Critical Path Analysis for Field-Programmable Gate Arrays
- ❑ Programming Field-Programmable Gate Arrays: Manufacturing Considerations and Options
- ❑ How TI Tests Field-Programmable Gate Arrays
- ❑ IEEE 1149.1 Boundary Scan Library Components

Chapter 7 **Ordering Information**

Includes the ordering information for all the TPC Series development systems, hardware options, and device silicon.

Trademarks

Chapter 1

General Information

Includes a glossary of electrical and FPGA-related terms used throughout this manual. Provides a TI FPGA product selection summary and a general overview of the TPC Series architecture.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART 1 — GENERAL CONCEPTS AND CLASSIFICATIONS OF CIRCUIT COMPLEXITY

ADL

Design language. The format for TI-ALS design data.

ALS

Action Logic System.

Action Logic™ System

The development system for configuring, programming, and debugging TI FPGAs.

Actionprobe™

TI-ALS feature that allows internal circuit nodes to be observed at the external device pin.

Activate

TI-ALS program that programs the TPC device.

Activator™ 1

Programming hardware for TPC10 Series devices.

Activator™ 2

Programming hardware for all current and planned TPC Series devices. Supports programming up to four devices at a time.

Activator™ 2S

Programming hardware for all current and planned TPC Series devices. Supports programming of one device at a time.

Antifuse

A term for the type of programming element used in TPC arrays. An antifuse is an element which is normally open, but converts to a resistive connection when programmed.

Array

The area occupied by the rows of modules and the routing channels.

Assertion

System error causing abnormal program termination. A failure code is written to the \alsuser\user\assert.log file. Errors of this type should be reported to the TI FPGA helpline, (214) 997-5666.

Back Annotation

The process of translating data generated from the TI-ALS system back to the CAE design environment. Postlayout delay information is back annotated to the CAE simulator.

Binning Circuit

Nonuser circuit used to characterize the AC performance of a TPC device. All TPC devices contain a binning circuit that has been tested to an AC test limit to ensure data sheet specifications have been met.

Channel

The area reserved for routing; containing horizontal tracks and horizontal pass transistors.

Clock Network

A system for distributing a global clock signal throughout the array, with minimum skew and large drive capability.

Configure

Process for determining placement and routing for a design.

Critical Net

Net whose signal propagation delay is part of a critical path in the design.

Criticality

Design property. The level of criticality assigned influences the placement and routing of a net and may influence the propagation delay associated with the net. The four levels of criticality are fast critical (F), medium critical (M), uncritical (U) and default critical.

Criticality File

Design constraint file for assigning criticality to nets.

DCLK Pin

Device pin. When MODE = 0, DCLK is a user I/O, and when MODE = 1, DCLK is used by the program/debug hardware to clock data into internal program/test registers.

Debugger

TI-ALS program for debugging programmed TPC devices.

Designer

The component of the TI-ALS system which validates, configures, and generates fuse files for FPGA designs for devices up to 2500 gates.

Designer Advantage

The component of the TI-ALS system which validates, configures, and generates fuse files for FPGA designs for devices up to 10,000 gates.

Error

A design problem that must be corrected before TI-ALS will proceed.

Extract

TI-ALS program that creates postlayout delay information.

Fixed Macro

A hard macro that has a user-assigned location in the array that is not altered by automatic placement.

Fusemap

Design file containing a list of antifuse addresses used by the programming hardware to program the device.

Fuser

TI-ALS program that generates the fusemap for the TPC device.

Gate Equivalent Circuit

A basic unit of measure of relative digital circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

GND

Device pin. All pins labeled GND must be connected to circuit ground.

Hard Macro

Unit-level macros that have a fixed relative placement. Two-module hard macros are always placed in modules which are side by side. All routing between two-module hard macros is predetermined. Hard macros are predefined by Texas Instruments.

Hierarchy

Style of organizing a design where a level of a logic design is expressed in terms of lower-level subcircuits or blocks. Lower-level blocks may, in turn, be expressed in terms of other lower-level blocks.

ICP

In circuit probe debugger command used to assign the Actionprobes to signals internal to a TPC device operating in the end system environment.

I/O Module

Module used to configure I/O macros, like INBUF, TRIBUFF, etc.

I/O Pin

The connection to the package lead that is bonded to the device I/O buffer.

Instance

CAE term. Each placement of a library element or hierarchical block into a design defines a unique instance of that element. The instance may have a default or assigned name that is independent of the library element function.

Instance Pins

An instance pin is a macro pin for a given instance. For example, the A input of an AND2A (2-input and gate) with an instance name of U1 has an instance pin name of U1:A.

Label

CAE term. A label is a method of attaching names, text, etc., to nets or instances in a design.

Level

A property attached to macro symbols indicating which category of macros they belong to. Choices are unit, hard, soft, and user.

Logic Compaction

Logic compression; logic conversion from standard TTL or CMOS technology into TI FPGA technology which combines functions from multiple logic elements into one logic module.

Logic Module

Module used to configure logic macros, like AND, OR, etc. The basic logic building block of the TI-FPGA from which all logical functions are built.

Long Horizontal Track

A horizontal routing track is used to interconnect two (or more) pins on a net that are separated by a substantial horizontal distance. Typically, a long horizontal track occupies more than a third of the columns of the array. Only a limited number of such tracks are available. If more tracks are needed, the placement will fail. Nets using long horizontal tracks may encounter some additional delay.

Long Vertical Track

A vertical routing track is used to interconnect two (or more) pins on a net that are separated by a substantial vertical distance. Typically, a long vertical track occupies more than three to six rows of the array. Only a limited number of tracks are available. If more tracks are needed, the placement will fail. Nets using long vertical tracks may encounter a substantially longer delay than the median.

Macro Pin

Macro pins are connection points to macro functions. For example, the A input of an AND2A (2-input and gate) is a macro pin.

Mode Pin

Device pin which places the device in normal mode (MODE=0) or test/program mode (MODE=1).

Module

Synonym for the basic functional block in a TPC array. Modules are used to construct macros. (See Logic Module).

Net

A logic signal path between macros. A net can be implemented in one or more routing segments connected by two or more antifuses.

PRA, PRB (or MPRA, MPRB)

Device pin. When MODE=1, PRA and PRB function as Actionprobe pins. When MODE=0, PRA and PRB are user-defined I/O pins.

Place

TI-ALS program that determines the placement of the design logic into logic modules in the TPC arrays.

Programmable Array Logic (PAL)

PAL® circuits are user programmable integrated circuits which utilize fuse link technology to implement logic functions. Implements sum of products logic by using a programmable AND array whose outputs feed a fixed OR array.

Route

TI-ALS program that determines the interconnection of logic modules in TPC arrays.

Row

A horizontal tile of logic modules; the lowest row in the array is row 0 (zero). Channel n is always below row n.

SDI

Device pin. When MODE=0, SDI is a user I/O, and when MODE=1, SDI is used by the program/debug hardware as a serial data input for internal program/test registers.

SDO

Device pin. Same as above except SDO in place of SDI and serial data output. TPC12 Series only.

Security Fuse

Special antifuses for providing user security of TPC devices after programming.

Segment

A piece of wire used for routing. It is connected by one or more antifuses to other segments in either the same or perpendicular direction. Horizontal segments run horizontally in the channels. Vertical segments run vertically through the modules and are often dedicated (connected to a module input or output).

Short Path

A chain of a small number (usually less than five) of macros connected by up to three nets. The chain of nets need NOT be a signal path, that is, the path can go from one input pin to another, or the nets can carry signals in opposite directions.

Soft Macro

Predefined blocks consisting of multiple hard and/or unit and/or other soft macros. Placement and routing is not predetermined for soft macros.

Stretched Short Path

A short path where the first and the last macros in the chain are fixed macros and are located so far apart that at least one of the nets in this path must use a long horizontal and/or long vertical routing track..

TI-ALS

Texas Instruments Action Logic System.

TPC10

FPGA family consisting of the TPC1010 and TPC1020 devices.

TPC12

FPGA family consisting of the TPC1225, TPC1240, and TPC1280 devices.

TPC14

FPGA family in preliminary form designed as a third generation TI product.

Timer

TI-ALS program for performing static timing analysis on TPC devices.

Track

A set of segments connected end-to-end, running across the array in the vertical or horizontal direction. The segments may or may not be connected by antifuses.

Unit Macro

A cell from the TI macro library implemented in one logic module. A unit-level macro can be implemented in any of several ways by the configuration software.

User Macro

A customer designed block consisting of multiple and/or unit hard macros and/or soft macros or other user macros. Placement and routing is not predetermined. User is the default if no LEVEL property is attached.

V_{CC}

Device pin. All pins labeled V_{CC} must be connected to the 5-V power supply.

V_{KS}

Device pin. During programming, a "keeper supply" voltage is applied to V_{KS}. During normal operation this pin must be tied to circuit ground.

V_{PP}

Device pin. During programming, high voltage is applied to V_{PP}. During normal operation, this pin must be tied to V_{CC} level.

V_{SV}

Device pin. During programming, a "super" voltage is applied to V_{SV}. During normal operation, this pin must be tied to V_{CC} level.

Warning

A nonfatal message that alerts you to a situation that may cause problems or difficulties, if not corrected.

PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device.

C_o **Output capacitance**
The internal capacitance at an output of the device.

f_{clock} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZ}

The current flowing into* an output having 3-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

* Current out of a terminal is given as a negative value.

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

t_a **Access time**

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a 3-state output)**

The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. ($t_{dis} = t_{PHZ}$ or t_{PLZ}).

* Current out of a terminal is given as a negative value.

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). ($t_{en} = t_{PZH}$ or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES 1: The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

$t_{sk(o)}$ **Output Skew**
The time interval between any two propagation delay times when a single switching input or multiple inputs switching simultaneously causes multiple outputs to switch, as observed across all switching outputs.

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES 1: The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

PRODUCT SELECTION SUMMARY

TPC DEVICE	PACKAGE	NO of PINS	SPEED OPTION	PROCESS	GATE ARRAY GATES
TPC1010A	FN	44	STD, –1	C, I	1200
	FN	68	STD, –1	C, I	1200
	GB	84	STD	M, B	1200
	HT	84	STD	M, B	1200
	VE	100	STD, –1	C, I	1200
TPC1010B	FN	44	STD, –1	C, I	1200
	FN	68	STD, –1	C, I	1200
	VE	100	STD, –1	C, I	1200
TPC1020A	FN	44	STD, –1	C, I	2000
	FN	68	STD, –1	C, I	2000
	FN	84	STD, –1	C, I	2000
	GB	84	STD, –1	M, B	2000
	HT	84	STD, –1	M, B, S	2000
	VE	100	STD, –1	C, I	2000
TPC1020B	FN	44	STD, –1	C, I	2000
	FN	68	STD, –1	C, I	2000
	FN	84	STD, –1	C, I	2000
	VE	100	STD, –1	C, I	2000
TPC1225A	FN	84	STD, –1	C, I	2500
	VE	100	STD, –1	C, I	2500
TPC1240	GB	133	STD	C, I, M	4000
	VE	144	STD	C, I	4000
TPC1280	GB	176	STD, –1	C, I	8000
	GB	177	STD, –1	C, I, M	8000
	HFG	172	STD	M	8000
	VB	160	STD, –1	C, I	8000
TPC1425	FN	84	STD	C	2500
	GB	133	STD	C, I	2500
	VE	160	STD	C	2500
TPC1460	GB	207	STD	C, I	6000
	VE	208	STD	C	6000

Legend:

Package Types:
- VB – Plastic Quad Flat Pack
- VE – Plastic Quad Flat Pack
- GB – Ceramic Pin Grid Array
- FN – Plastic Leaded Chip Carrier
- HT – Ceramic Quad Flat Pack
- HFG – Ceramic Quad Flat Pack with nonconductive tie bar

Speed Options:
- STD – Standard Speed
- –1 – Standard – 15% Faster

Process:
- C – Commercial (0°C to 70°C)
- I – Industrial (–40°C to 85°C)
- M – Military (–55°C to 125°C)
- B – MIL–STD–883C
- S – Space Equivalent

INTRODUCTION

To develop an understanding of the capabilities of a field programmable gate array (FPGA), a knowledge of its architectural elements is needed; see Figure 1–1 and Figure 1–2. TI FPGAs have several characteristic features which define their function. These basic features are the antifuse, the logic module, the clock distribution network, routing channels, and diagnostic circuits.

Figure 1–1. Device Architecture

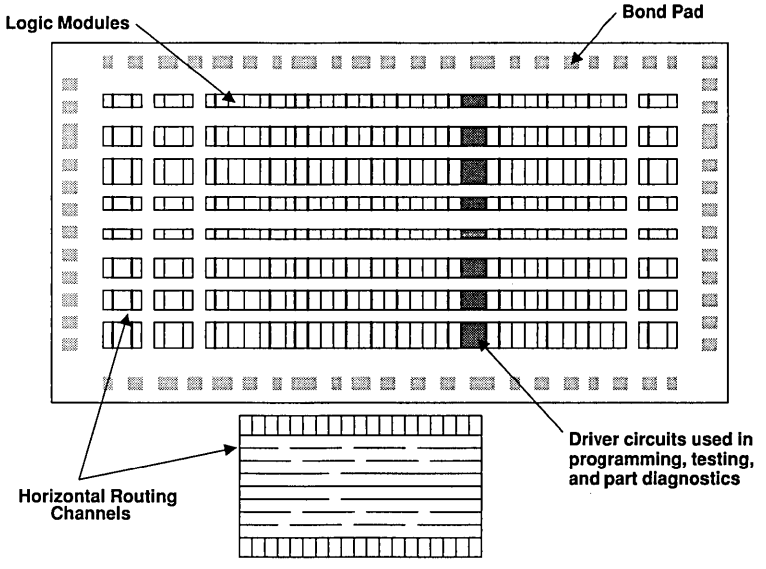
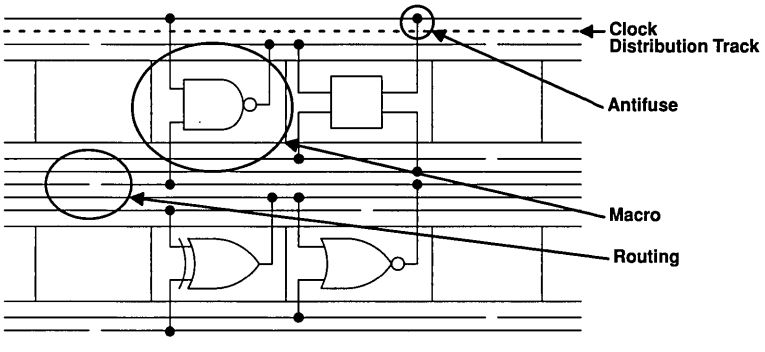


Figure 1–2. Architecture Detail

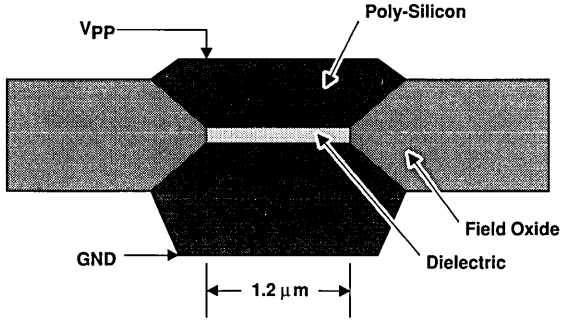


Architectural Overview

The Antifuse

The element which provides programmability to the device is the antifuse, which is shown in Figure 1–3. An antifuse is a normally open device which becomes conductive when a high voltage pulse is applied to it. This is opposite to the action of a fuse which becomes nonconductive when a large voltage or current is applied to it. As Figure 1–3 shows, the antifuse consists of two conducting layers separated by a thin isolation layer. Another important feature is the small size which is up to 19 times smaller than other types of programmable elements such as EEPROM or SRAM.

Figure 1–3. FPGA Antifuse



Metal routing tracks run horizontally and vertically over the die, with an antifuse at each intersection. The unprogrammed resistance of the antifuse is greater than 100 MΩ and the programmed resistance is approximately 500 Ω.

Routing

As Figure 1–1 and Figure 1–2 shows, the FPGA architecture is analogous to that of a channeled gate array with routing tracks running horizontally between the logic modules and vertically over them. These tracks connect the macro functions implemented in the logic modules. The number of routing tracks per channel is family dependent and the segmentation of these tracks varies from device to device. Segmentation refers to the varying length of tracks in a routing channel.

Logic Module

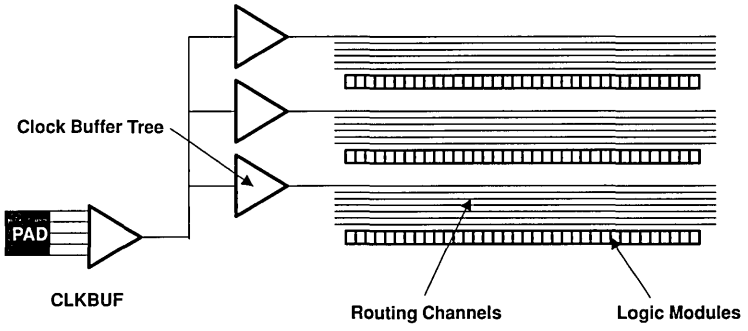
A prominent feature of the architecture is the rectangular array of logic modules which contain generic logic circuits. These circuits can be programmed to perform a variety of functions. Each logic module is multiplexer based. A TPC10 Series device has only one type of combinatorial logic module. Sequential TPC10 Series functions are implemented using combinatorial modules. The TPC12 and TPC14 Series device families have both the combinatorial module and an enhanced sequential module.

The macro functions implemented in the logic modules are generated in several ways. They come from TI-supplied hard and soft macro libraries or can be created by the user.

Clock Distribution

High drive requirements for the clock signal are met by a dedicated clock buffer network which is shown in Figure 1–4. This network consists of an assigned input pin and row buffers to provide additional drive for the large fan-out requirements of the clock signal. The network can connect to any logic module but only to clock and gated inputs of sequential macro functions.

Figure 1–4. Dedicated Clock Buffer Network



Test and Debug Diagnostics

Special circuitry is built into the device for diagnostics. This circuitry consists of shift registers which allow the user to address and probe any internal node of the programmed device. Four special I/O pins are provided for this function. These pins are multiplexed so that they can be configured as diagnostic or normal I/O pins and are controlled by the debug function of the TI Action Logic™ System (TI-ALS). This function allows any two internal nodes to be probed simultaneously while the device is operating in an actual circuit board.

Inputs/Outputs

The I/O count depends on the device and the packaging of the device. The I/O function can be programmed as either input, output, 3-state, or bidirectional.

2 TPC FPGA Series Data

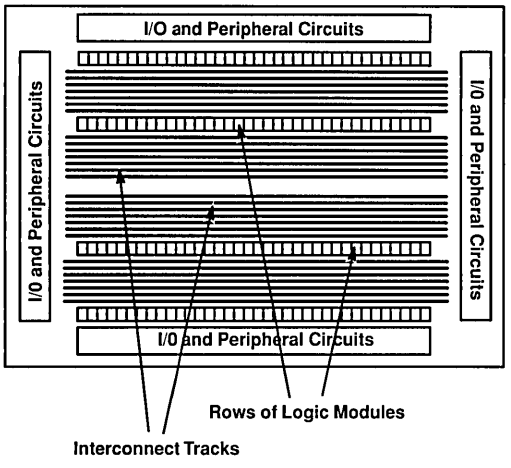
Chapter 2

TPC FPGA Series Data

Presents the TPC10 and TPC12 Series individual datasheets which contain electrical and switching characteristics, mechanical drawings and packaging options, and supported library macro listings and symbols for each of the TPC Series families. Includes the TPC10 and TPC12 macro pin loading tables as well as a product preview of the TPC14 Series.

SRFS001F – D3864, DECEMBER 1989 – REVISED FEBRUARY 1993

- **Four Arrays With up to 2000 Usable Equivalent Gates**
- **TI Action Logic™ System (TI-ALS) Software for:**
  - **View*Logic*™**
  - **Mentor™**
  - **OrCAD/SDT III™**
  - **Cadence™/Valid™**
- **Reliable Antifuse Interconnect**
- **Built-In Clock Distribution Network**
- **Silicon-Gate CMOS Technology**
- **Desktop TI-ALS Creates Design Files for:**
  - **I/O Pin Assignment**
  - **Design Validation**
  - **Place and Route**
  - **Circuit Timing Analysis**
  - **Array Antifuse Programming**
  - **Test and Debug**



TPC10 Series FPGA Die Architecture

description

The Texas Instruments (TI) TPC10 Series comprises four field-programmable gate arrays (FPGAs). The TPC1010A, TPC1010B, TPC1020A, and TPC1020B FPGAs are fabricated using the TI silicon-gate CMOS process. The process features polysilicon gate, source, drain elements, and two levels of copper-doped-aluminum metallization to reduce internal resistance and enhance performance. Typical die architecture is illustrated above.

These field-programmable devices combine gate-array flexibility with desktop programmability. This combination allows the designer to avoid fabrication cycle times and nonrecurring engineering charges associated with conventional mask-programmed gate arrays. The FPGAs are unique in that the arrays are fabricated, tested, and shipped to the user for programming. The FPGA contains user-configurable inputs, outputs, logic modules, and minimum-skew clock driver with hardwired distribution network. The FPGA also includes on-chip diagnostic probe capabilities and security fuses to protect the proprietary design.

Table 1. Product Family Profile

DEVICE	TPC1010A	TPC1020A	TPC1010B	TPC1020B
Capacity				
Gate array equivalent gates	1200	2000	1200	2000
TTL equivalent packages	34	53	34	53
CMOS Process	1.2 µm	1.2 µm	1.0 µm	1.0 µm
Logic Modules	295	547	295	547
Flip-Flops (maximum)	130	273	130	273
Antifuses	112,000	186,000	112,000	186,000
Horizontal Tracks	22	22	22	22
Vertical Tracks	13	13	13	13

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Cadence/Valid are trademarks of Cadence Design Systems, Inc.
Mentor is a trademark of Mentor Graphics Corporation.
OrCAD/SDT III is a trademark of OrCad Systems Corporation.
View*Logic* is a trademark of Viewlogic System, Incorporated.

Action Logic System (ALS) and Activator

TPC10 Series FPGAs are supported by the ALS software and Activator™ programming hardware. The combination facilitates logic design and FPGA programming on popular CAE workstations with minimum effort. ALS interfaces to the resident CAE system providing a complete library of TPC10 Series functions. The ALS includes automatic place and route, timing verification, and FPGA device programming. The ALS and Activator are available for View*Logic* or OrCAD (SDT III) 386/486 based PC systems, Mentor-equipped Apollo workstations, and View*Logic*- or Valid/Cadence-equipped Sun-4 workstations.

library functions

The TPC10 Series FPGA library contains over 250 logic building blocks of hardwired and soft macros. The hardwired macros provide a wide selection of predesigned, fully characterized functions. The soft macros provide popular MSI functions that can be called into the design. Additional user-defined soft macros can be created using the TPC10 library macros. The library contains the following classes of macros:

- Primitive Gates, Booleans, and Buffers
- CMOS, TTL, and Clock Buffer Inputs and Totem-Pole, 3-State, and I/O Output Buffers
- Adders and Multiplexers
- D-Type Flip-Flops
- J-$\overline{K}$ Flip-Flops
- Latches
- MSI Complexity Soft Macros

design flow

Custom logic functions, designed in conjunction with the TPC10 Series FPGA library, can be simulated and verified prior to creating the ALS design data base and programming files. Figure 1 provides an overview of the design flow.

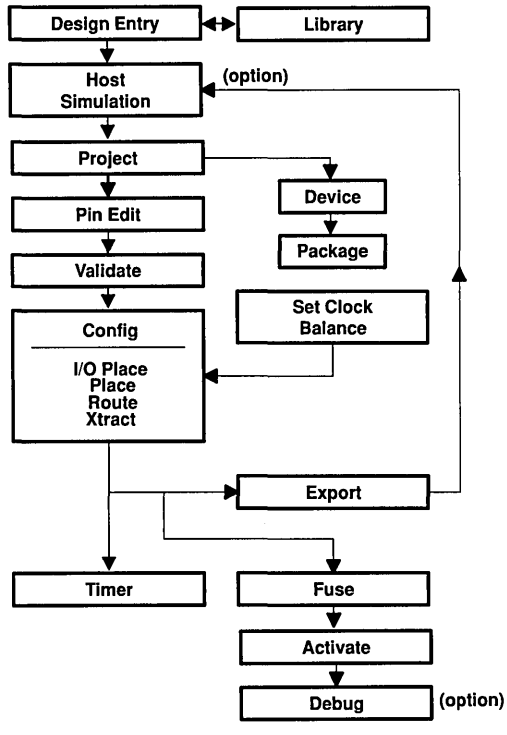


Figure 1. Design Flow

Table 2. TI-ALS Design Configurations (see Note 1)

HARDWARE PLATFORM	LIBRARY/CAE HOST ENVIRONMENT	DESIGN SUPPORT (gates)		TI SUSTEM PART NUMBER
		UP TO 2500	UP TO 10000	
386/486-based PC	View*Logic*	X		TPC-ALS-DS–PC-VL
	View*Logic*		X	TPC-ALS-DA–PC-VL
	OrCAD	X		TPC-ALS-DS–PC-OR
	OrCAD		X	TPC-ALS-DA–PC-OR
Sun	Cadence		X	TPC-ALS-DA–SN-CD
	Mentor		X	TPC-ALS-DA–SN-MG
	Valid		X	TPC-ALS-245†
	View*Logic*		X	TPC-ALS-DA–SN-VL
HP700	Mentor		X	TPC-ALS-DA-HP7-MG
DN4000/ HP400				TPC-ALS-235†

NOTE 1: Authorization codes for design systems are supplied upon request, after receipt of the system.

† The TPC-ALS-235 and TPC-ALS-245 systems only provide support for the TPC10 and TPC12 series, and will not be supported in Revision 3.0 scheduled for release in the fourth quarter of 1993. These systems are being replaced by TPC-ALS-DA-HP7-MG and TPC-ALS-DA-SN-CD, respectively.

Table 3. TI-ALS Programming Configurations (see Note 2)

HARDWARE PLATFORM	CAE HOST ENVIRONMENT	DESIGN SUPPORT		TI SUSTEM PART NUMBER
		ONE DEVICE	FOUR DEVICES	
386/486-based PC	View*Logic* /OrCAD	X		TPC-ALS-DS–P2S-PC
			X	TPC-ALS-219
Sun	Cadence/Mentor/ Valid/View*Logic*	X		TPC-ALS-DS–P2S-SN
			X	TPC-ALS-249
HP700	Mentor	X		TPC-ALS-DS–P2S-HP7
			X	TPC-ALS-DS–P2-HP7
HP400	Mentor	X		TPC-ALS-DS–P2S-HP4
			X	TPC-ALS-DS–P2-HP4
DN Series	Mentor		X	TPC-ALS-239

NOTE 2: Programming units are compatible with both high (10000 gates) and low (2500 gates) density systems.

architecture

device organization

Each FPGA consists of a matrix of logic modules arranged in rows separated by channels containing interconnect tracks. The matrix is surrounded with peripheral inputs, outputs, I/Os, and diagnostic circuits. A partial view of the TPC10 Series logic modules with examples of interconnections is illustrated in Figure 2.

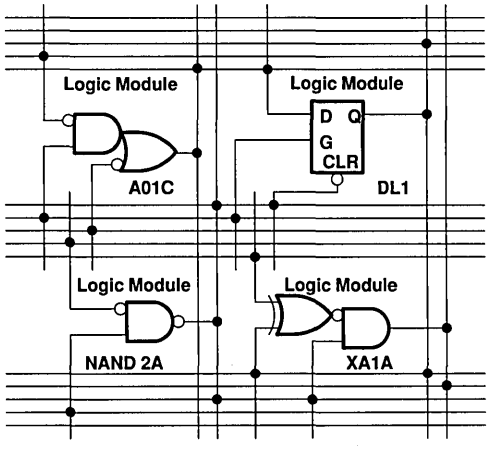


Figure 2. Partial View of TPC10 Series Interconnection Capability

logic module

Each core logic module has the equivalent complexity of four 2-input NAND gates. The module shown in Figure 3, is an 8-input, 1-output gate cluster that can implement hardwired primitive gates, Booleans, latches, flip-flops, multiplexers, half or full adder slices, or multiplexed-input flip-flops. The TI-ALS library contains a full spectrum of 2-, 3-, and 4-input AND, NAND, OR, and NOR gate macros covering all derivatives of true and/or complement input combinations. Similar modular implementations, covering the spectrum of true and/or complement input combinations, are included for each functional category of macros in the library. Latches and flip-flops are created by connecting two or more logic modules in the appropriate circuit configuration. The macros are captured, simulated, placed, analyzed, and programmed using the TPC10 design library.

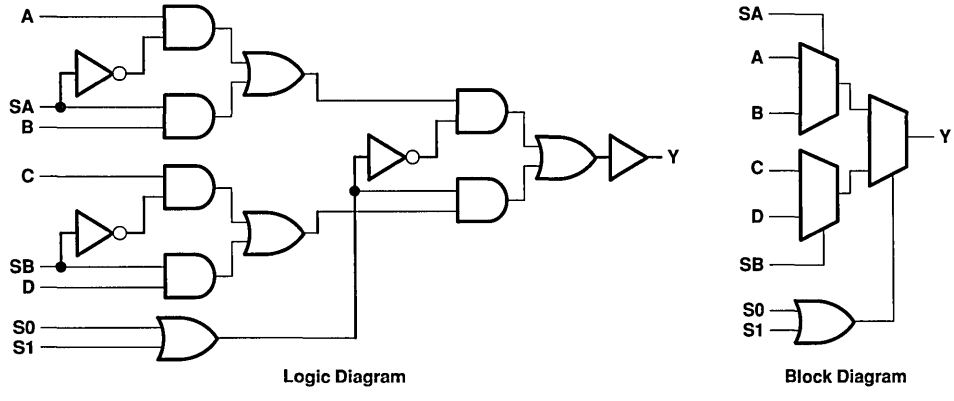


Figure 3. TPC10 Series Logic Module

interconnect tracks

The channeled interconnect tracks consist of isolated metal segments that can be connected by addressing and programming antifuses. Each channel has 25 horizontal routing tracks, 22 are for logic, one is for clock, one is for power, and one is for ground. In addition, there are 13 vertical routing tracks per logic module column. Both horizontal and vertical tracks, in combination with the approximately 340 antifuses per logic module, produce a network that is capable of interconnecting up to 90 percent of the equivalent gates. Based on the placement of macros, the programming process selects and activates antifuses that both create the logic module macros and I/Os, and interconnect the entire array.

I/O buffers

Each I/O pin is configurable as an input or an output. In addition, I/O pins configured as outputs can be defined as totem-pole, 3-state, or bidirectional. Inputs can be driven by CMOS or TTL levels and output levels are compatible with standard CMOS and TTL specifications. Outputs sink or source a current of 4 mA at TTL output levels. See the dc characteristics for additional I/O buffer specifications. The I/Os can be manually assigned to any available package pin, or the ALS software can automatically place the I/Os in the optimum configuration.

diagnostic probe pins

TPC10 Series devices have two independent diagnostic probe pins, PRA and PRB. The pins allow the user to observe any internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on an oscilloscope, logic analyzer, or with the workstation diagnostics using the Actionprobe diagnostic tools. The probe pins can also be used as user-defined I/Os, depending on the level of the mode control pin. When configured as user-defined I/Os, the pins have the same characteristics as other I/O pins.

security fuses

The TPC10 Series security fuses can be used to permanently disable further diagnostics and testing. After the security fuses are programmed, access to the architecture is not available. This makes the FPGA design difficult to copy.

FPGA array performance

logic module size

A mask-programmed gate array cell with four transistors usually implements only one logic level. The TPC10 Series array logic module is more complex and typically implements multiple logic levels within a single module. This reduces intermodule wiring and associated RC delays. In effect, the TPC10 logic module implements the equivalent of a net compression that enhances performance.

TERMINAL FUNCTIONS

PIN NAME	I/O	DESCRIPTION
CLK	I	Clock. TTL clock input for global clock distribution network. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
DCLK	I	Diagnostic clock. TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
GND	I	Ground. Input low supply voltage.
I/O	I/O	Input/output. I/O pin functions as an input, output, 3-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically set low by the ALS software.
MODE	I	Mode. The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is high, the special functions are active. When the MODE pin is low, the pins function as I/Os.
NC		No connection. This pin is not connected to circuitry within the device.
PRA	O	Probe A. The probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe B pin to allow real-time diagnostic output of any signal path within the device. The probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
PRB	O	Probe B. The probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe A pin to allow real-time diagnostic output of any signal path within the device. The probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDI	I	Serial data input. Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
V_{CC}	I	Supply voltage. Input high supply voltage.
V_{PP}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 to V_{CC} + 0.5 V
Output voltage range, V_O ..... – 0.5 to V_{CC} + 0.5 V
Input clamp current‡ , I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current§, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 20 mA
Continuous output current§, (V_O = 0 to V_{CC}) ..... ± 25 mA
Operating free-air temperature range, T_A: Commercial ..... 0°C to 70°C
Industrial ..... – 40°C to 85°C
Operating case temperature range, T_C: Military ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Applies for input and bidirectional buffers
§ Applies for bidirectional and output buffers

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
		Military	4.5	5	5.5	
V_{PP}	Program pin voltage (while not programming)		V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage		2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
T_A	Operating free-air temperature	Commercial	0	25	70	°C
		Industrial	−40	25	85	
T_C	Operating case temperature	Military	−55	25	125	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (see Note 3)	I_{OH} = −4 mA	3.84									V
		I_{OH} = −3.2 mA				3.7			3.7			
V_{OL}	Low-level output voltage (see Note 3)	I_{OL} = 4 mA			0.33			0.4			0.4	V
I_I	Input current	$V_I = V_{CC}$ or 0			±10			±10			±10	µA
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±10			±10	µA
I_{OS}	Short-circuit output current (see Note 4)	$V_O = V_{CC}$	20		140	20		140	20		140	mA
		V_O = 0	−10		−100	−10		−100	−10		−100	
I_{CC}	Standby supply current	$V_I = V_{CC}$ or 0, Outputs open		3	10		3	20		3	25	mA
C_{io}	Input/output capacitance (see Note 5)	V_O = 0, f = 1 MHz		7			7			7		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. These limits apply when all other outputs are open.
4. When testing TPC1010A and TPC1020A, not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second. The I_{OS} parameter does not apply to TPC1010B or TPC1020B.
5. These limits apply for each user I/O pin.

switching characteristics

The following tables summarize switching characteristics of various classes of TPC10 Series logic module hardwired macros. An unloaded logic module propagation delay time is 4 ns. All other delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization. Module utilization above 95% can result in performance degradation. Actual delay values are determined after place and route is accomplished using the ALS. ALS provides for assigning criticality to nets, automatic balancing of clock buffer loads, and utilizing long horizontal or vertical nets for connecting noncritical functions. For specific timing parameters pertaining to a hardwired logic module, refer to the individual macro library specification.

The ALS provides a capability to assign one of four levels of criticality to logic module output nets. The switching characteristics reflect the delay time differences for nets with criticality and without criticality assigned. Nets assigned as critical will be limited to a fan-out of 6 loads by the ALS. Clock load balancing, selectable by the designer, can be specified as moderate, strong, or very strong to control clock skew.

timing requirements over recommended operating conditions, no further derating required

				MIN	MAX	UNIT
f_{clock}	Clock frequency				100	MHz
t_w	Pulse duration	CLK, PRE, or CLR	FO = 1	7.7		ns
			FO = 2	8.5		
			FO = 3	9.2		
			FO = 4	10		
			FO = 8	14		
t_{su}	Setup time, flip-flop	All synchronous inputs before clock transition		3.9		ns
t_{su}	Setup time, latch	All synchronous inputs before clock transition	FO = 1	3.5		ns
			FO = 2	3.9		
			FO = 3	4.2		
			FO = 4	4.5		
			FO = 8	4.8		
t_h	Hold time, flip-flop or latch	All synchronous inputs after clock transition		0		ns

typical switching characteristics

single-level logic module hardwired macro (module count = 1), V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	5.4	5.8	6.2	8.5	See Note 7	ns
t_{pd}	Not critical	6.3	6.7	7.7	8.6	10.8	ns

double-level logic module hardwired macro (module count = 2), V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	9.2	9.6	10	12.3	See Note 7	ns
t_{pd}	Not critical	10.2	10.6	11.6	12.5	14.6	ns

flip-flop and latch hardwired macro, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	5.4	5.8	6.2	8.5	See Note 7	ns
t_{pd}	Not critical	6.3	6.7	7.7	8.6	10.8	ns

NOTES: 6. An unloaded logic module propagation delay time is 4 ns. All delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization.
7. Critical nets are limited to a fan-out of 6 loads.

long net, V_{CC} = 5 V, T_J = 25°C, typical process

Long nets include long horizontal and vertical routing resources used for noncritical signals and interconnecting logic macros separated by large distances. Long nets are used by the autorouter when no other means exist to complete the interconnection. Delays due to the use of long nets range from 15 ns to 35 ns. Typically less than one percent of all nets in a design require the use of a long net.

typical switching characteristics

input buffer and bidirectional-input buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	DELAY TIME					UNIT
			FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{PHL}	Pad	Y	6.9	7.6	8.9	10.7	14.3	ns
t_{PLH}			5.9	6.5	7.7	8.4	12.4	

output buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PHL}	D	Pad	C_L = 50 pF	3.9	4.9	ns
t_{PLH}				7.2	5.7	
Δt_{PHL}	D	Pad		0.03	0.046	ns/pF
Δt_{PLH}				0.07	0.039	

The BIBUF macro's output section exhibits the same delays as the OUTBUF macro. The delta numbers can be extrapolated down to 15 pF minimum.

Example: Delay for an OUTBUF output buffer driving a 100-pF TTL load

t_{PHL} = 4.9 + [(0.046 x (100 – 50)] = 4.9 + 2.3 = 7.2 ns

t_{PLH} = 5.7 + [(0.039 x (100 – 50)] = 5.7 + 2.0 = 7.7 ns

3-state and bidirectional output buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PHL}	D	Pad	C_L = 50 pF	3.9	4.9	ns
t_{PLH}				7.2	5.7	
t_{PHZ}	E	Pad	See test loads in Figure 8	5.2	3.4	ns
t_{PZH}				6.5	4.9	
t_{PLZ}	E	Pad		6.9	5.2	ns
t_{PZL}				4.9	5.9	
Δt_{PHL}	D	Pad		0.03	0.046	ns/pF
Δt_{PLH}				0.07	0.039	
Δt_{PHZ}	E	Pad		0.08	0.046	ns/pF
Δt_{PZH}				0.07	0.039	
Δt_{PLZ}	E	Pad		0.07	0.039	ns/pF
Δt_{PZL}				0.03	0.039	

clock buffer, V_{CC} = 5 V, T_J = 25°C, typical process (see Note 8)

PARAMETER	FROM	TO	DELAY TIME			UNIT
			FO = 40	FO = 160	FO = 320	
t_{PHL}	Pad	Y	9	12	15	ns
t_{PLH}			9	12	15	

NOTE 8: The ALS software provides user-selectable options for choosing four levels of automatic clock load balancing. There is no limit to the number of loads that may be connected to the clock buffer (CLKBUF) macro.

extended output current operation

The TPC10 Series devices are capable of driving larger sink current loads by derating the low-level output voltage to 0.5 V and high-level output voltage to 2.4 V. The derating factors for commercial and military devices are illustrated in Figure 4 and Figure 5. The commercial devices are derated up to 8 mA and military devices are derated for up to 6 mA.

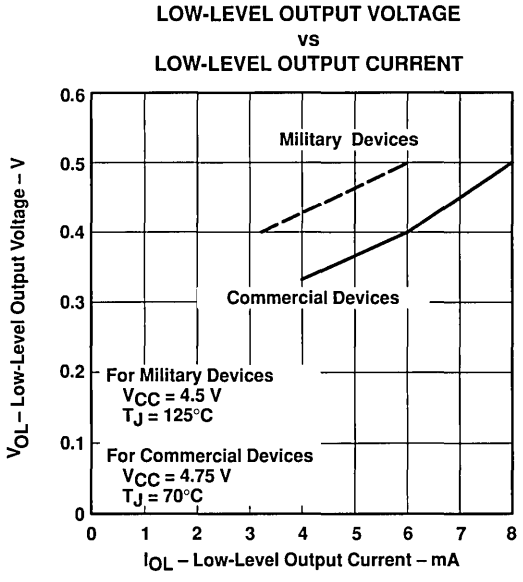


Figure 4

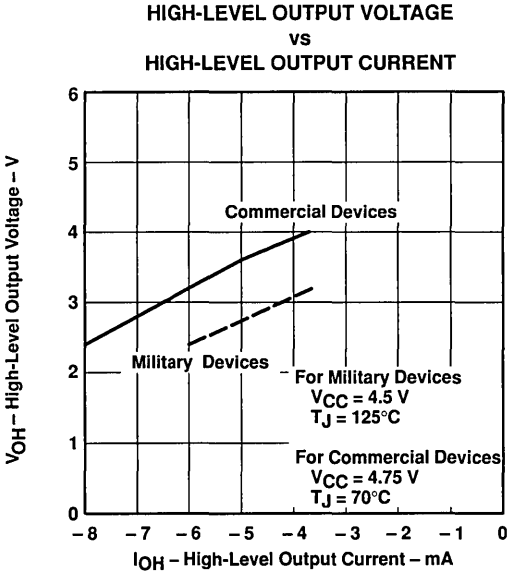


Figure 5

slow input transition (rise and fall) times

Slow signal transition is a condition that commonly occurs even in today's high-performance systems. A typical example is the signal degradation encountered with signals coming off of a highly capacitive bus. These slow signal transitions can cause undesirable results when traveling through the threshold region of a CMOS input. Texas Instruments recommends that input signal transitions be limited to 500 ns or less to ensure device integrity.

worst-case delay time

Unlike mask-programmed gate arrays, performance variations of TPC10 Series arrays caused by voltage and temperature changes are due primarily to the changes in the active elements. Voltage and temperature delay time factors are shown in Figure 6 and Figure 7.

timing derating

Operating temperature, operating voltage, and device processing conditions, along with product revision and speed grade, account for variations in array timing characteristics. These variations are summarized in derating factors for TPC10 array typical timing specifications. The derating factors as shown in Table 4 are based on the recommended operating conditions for TPC10 commercial, industrial, and military applications.

For estimating performance, the delay factors may be used in conjunction with the delay values shown in the typical switching characteristics tables. Temperature and voltage variations are measured according to the curves in the graphs shown in Figure 6 and Figure 7. The ALS timing analyzer can be used to provide actual postlayout timing specifications for each circuit implementation.

Table 4. Timing Derating Factor (x typical) (see Note 9)

TPC1010A, TPC1020A TPC1010B, TPC1020B	C SUFFIX		I SUFFIX		M SUFFIX	
	BEST CASE	WORST CASE	BEST CASE	WORST CASE	BEST CASE	WORST CASE
Standard speed	0.45	1.54	0.40	1.65	0.37	1.79
–1 Speed grade	0.45	1.28	0.40	1.37	0.37	1.49
–2 Speed grade†	0.45	1.13	0.40	1.20	0.37	1.32

† Applies to TPC1010B and TPC1020B only

NOTE 9: Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

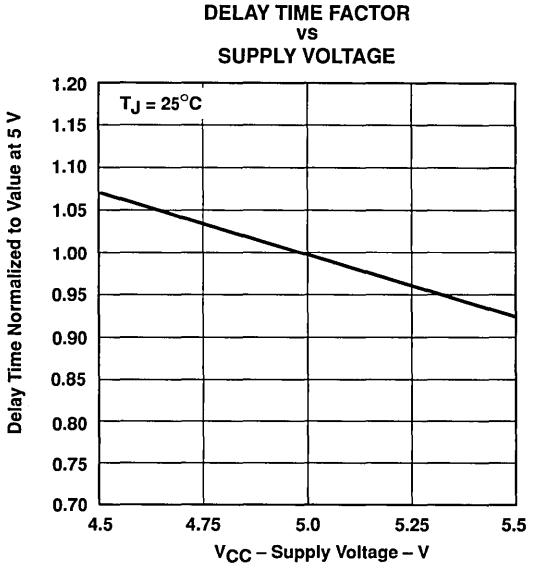


Figure 6

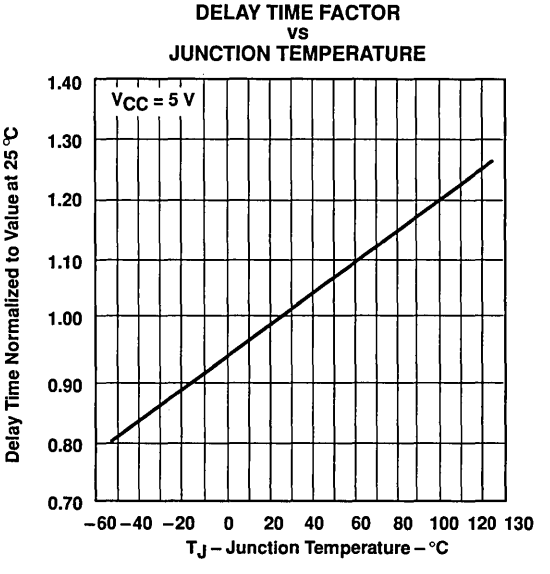
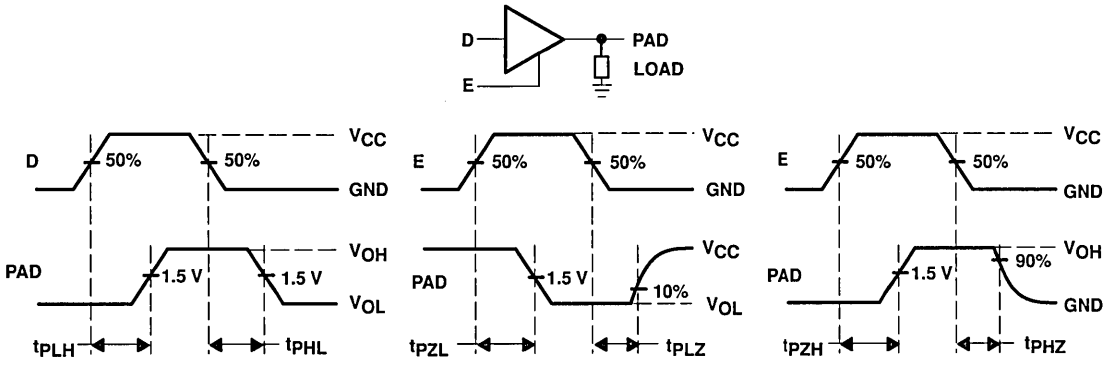
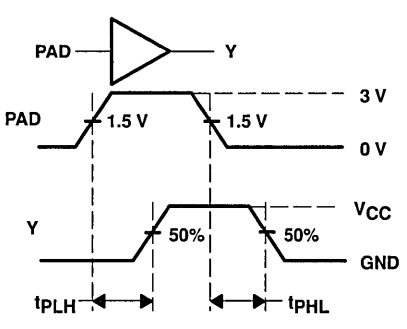


Figure 7

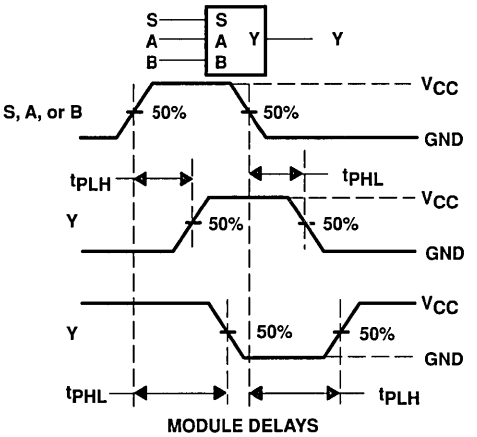
PARAMETER MEASUREMENT INFORMATION



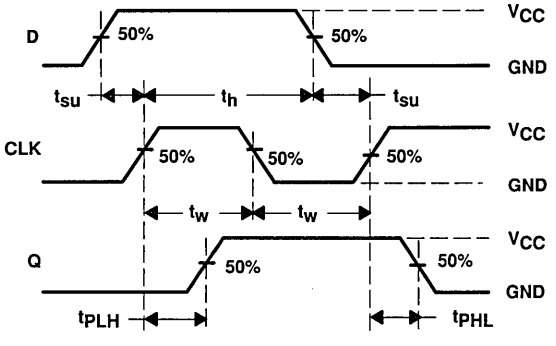
OUTPUT BUFFER DELAYS

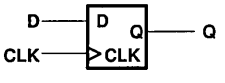


INPUT BUFFER DELAYS



MODULE DELAYS

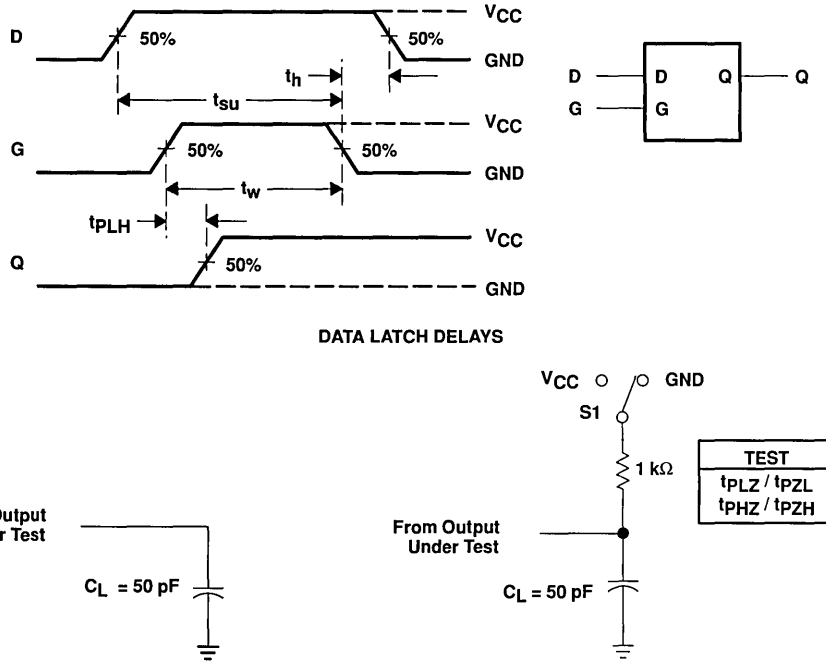




D FLIP-FLOP SHOWING POSITIVE-EDGE TRIGGERED CLOCK

Figure 8. Symbols, Test Loads, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



DATA LATCH DELAYS

LOAD CIRCUIT FOR PROPAGATION DELAY TIMES

LOAD CIRCUIT FOR ENABLE AND DISABLE TIMES

Figure 8. Symbols, Test Loads, and Voltage Waveforms (Continued)

dynamic power calculations

The formula for calculating typical dynamic die power consumption in mW is:

$$\text{Total die power} = (0.20N \times f1) + (0.085M \times f2) + (0.80P \times f3)$$

where:

- f1 = Average logic module switching rate in MHz
- f2 = Average clock pin switching rate in MHz (see Note 10)
- f3 = Average I/O switching rate in MHz
- M = Number of logic modules connected to the clock pin (see Note 10)
- N = Number of logic modules used on the chip (including M)
- P = Number of I/Os used with 50-pF load

NOTE 10: The F2 and M factors can be ignored if the CLKBUF macro is not used.

For example, if a TPC1010A design has 200 logic modules used, 40 of which are connected to the high-fan-out clock buffer running at 20 MHz and the rest running at 4 MHz, plus 50 I/Os (25 outputs, 25 inputs) running at an average of 4 MHz, it will dissipate the following amount of power:

$$\begin{aligned}\text{Total die power} &= (0.20N \times f1) + (0.085M \times f2) + (0.80P \times f3)\\ &= 0.20\ (200 \times 4) + 0.085\ (40 \times 20) + 0.80\ (25 \times 4)\\ &= 308\ \text{mW}\end{aligned}$$

ESD rating

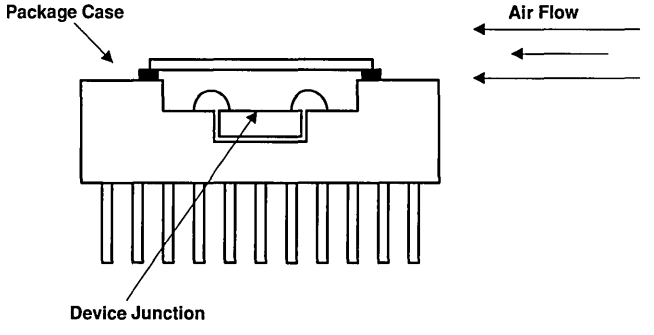
ESD characterization of Texas Instruments FPGAs is performed in accordance with Method 3015 of MIL-STD-883. This calls out the human body model which included discharging a 10-pF capacitor through a 1.5-kΩ resistor. Three positive and three negative pulses are discharged into each pin at each voltage level. After pulsing, the units are tested on a VLSI tester. Testing is performed for initial device qualification and product redesign only. All devices have been designed for ESD protection.

package thermal characteristics

The device junction to case thermal characteristic is $R_{\theta JC}$, and the junction to ambient air characteristic is $R_{\theta JA}$. The thermal characteristics for $R_{\theta JA}$ are shown with two different air-flow rates. Maximum junction temperature is 150°C for short durations. However, a maximum junction temperature of 140°C is recommended for continuing operation. A sample calculation of the maximum power dissipation for a PLCC 84-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{R_{\theta JA}\ (°C/W)} = \frac{150°C - 70°C}{40°C/W} = 2\ W$$

PACKAGE TYPE	PIN COUNT	$R_{\theta JC}$	$R_{\theta JA}$ STILL AIR	$R_{\theta JA}$ 300 FT/MIN	UNIT
Ceramic Pin Grid Array (CPGA)	84	3.5	48	NA	°C/W
Ceramic Quad Flat Package (CQFP)	84	3.5	75	NA	°C/W
Plastic Leaded Chip Carrier PLCC	44 68 84	13 13 10	65 50 40	41 32 27	°C/W
Plastic Quad Flat Package (PQFP)	100	10	60	38	°C/W



TPC1010A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	295	1200	34	R	R
68-pin PLCC			57	R	R
100-pin PQFP			57	R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	295	1200	34	R	R
68-pin PLCC			57	R	R
100-pin PQFP			57	R	R

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin CPGA	295	1200	57	R	R
84-pin CQFP			57	R	R

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1020A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	547	2000	34	R	R
68-pin PLCC			57	R	R
84-pin PLCC			69	R	R
100-pin PQFP			69	R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	547	2000	34	R	R
68-pin PLCC			57	R	R
84-pin PLCC			69	R	R
100-pin PQFP			69	R	R

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin CPGA	547	2000	69	R	R
84-pin CQFP			69	R	R

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1010B device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	295	1200	34	R	R	P
68-pin PLCC			57	R	R	P
100-pin PQFP			57	P	P	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	295	1200	34	R	R	P
68-pin PLCC			57	R	R	P
100-pin PQFP			57	P	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1020B device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	547	2000	34	P	P	P
68-pin PLCC			57	P	P	P
84-pin PLCC			69	P	P	P
100-pin PQFP			69	P	P	P

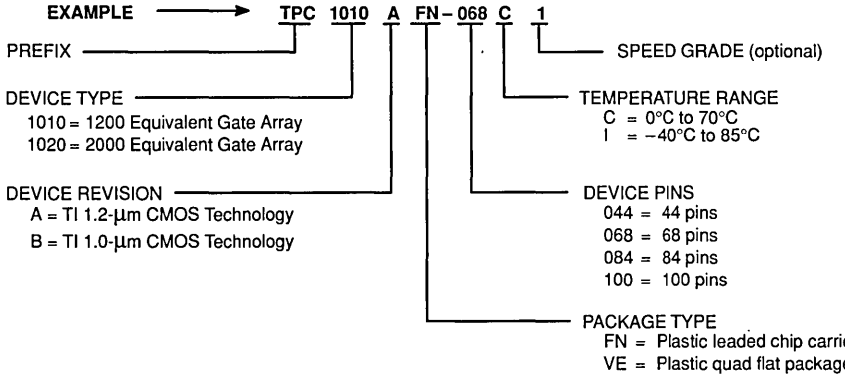
Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	547	2000	34	P	P	P
68-pin PLCC			57	P	P	P
84-pin PLCC			69	P	P	P
100-pin PQFP			69	P	P	P

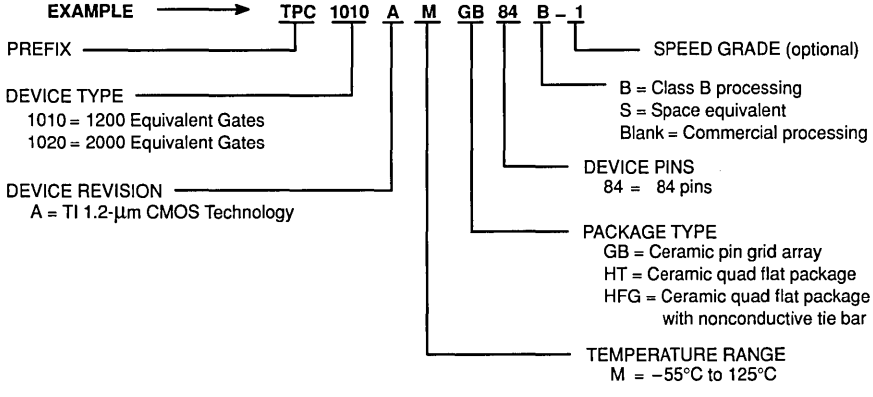
R = released
P = planned, consult your local TI sales representative for current availability.

ordering information

Configurations of the TPC10 Series devices can be ordered using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



Military versions can be ordered as follows:



DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1010AM	Class B	5962-9096401M
TPC1020AM	Class B Space Equivalent	5962-9096501M

macro library

The TPC10 Series is supported by a macro library of more than 250 hardwired and soft macro functions. The macros range from primitive logic gates to MSI-level complex functions such as counters, decoders, and comparators. The hardwired macro characteristics are provided in the electrical and switching characteristics. The software macros have characteristics similar to the components of the macro but need the place and route data back annotated into the design to establish actual performance.

The FPGA logic module implements logic functions with inverted inputs as efficiently as noninverted inputs, without an increase in propagation delay. By taking advantage of the various combinations of input polarity, the use of separate inverters can be virtually eliminated.

TPC10 SERIES SOFTWARE MACROS

MACRO NAME	DESCRIPTION	MODULE COUNT	LOGIC LEVELS
CNT4A	4-Bit Binary Counter With Load and Clear	18	4
CNT4B	4-Bit Presettable Binary Counter With Load and Clear	15	4
DEC2X4	2-Line to 4-Line Decoder	4	1
DEC2X4A	2-Line to 4-Line Inverting Decoder	4	1
DECE2X4	2-Line to 4-Line Decoder With Enable	4	1
DECE2X4A	2-Line to 4-Line Inverting Decoder With Enable	5	1
DEC3X8	3-Line to 8-Line Decoder	8	1
DEC3X8A	3-Line to 8-Line Inverting Decoder	9	1
DECE3X8	3-Line to 8-Line Decoder With Enable	11	2
DECE3X8A	3-Line to 8-Line Inverting Decoder With Enable	11	2
DEC4X16A	4-Line to 16-Line Inverting Decoder	20	2
DLC8A	Octal D-Type Latch With Clear	8	1
DLE8	Octal D-Type Latch With Enable	8	1
DLM8	Octal D-Type Latch With Multiplexed Inputs	8	1
FA1	1-Bit Full Adder	3	3
FADD8	8-Bit Fast Adder	37	4
FADD12	12-Bit Fast Adder	58	5
FADD16	16-Bit Fast Adder	79	5
FADD24	24-Bit Fast Adder	120	6
FADD32	32-Bit Fast Adder	160	7
ICMP4	4-Bit Identity Comparator	5	2
ICMP8	8-Bit Identity Comparator	9	3
MCMPC2	2-Bit Magnitude Comparator With Enable	9	3
MCMPC4	4-Bit Magnitude Comparator With Enable	18	4
MCMPC8	8-Bit Magnitude Comparator With Enable	36	6
MCMP16	16-Bit Magnitude Comparator	93	5
MX8	8-Line to 1-Line Multiplexer	3	2
MX8A	8-Line to 1-Line Inverting Multiplexer	3	2
MX16	16-Line to 1-Line Multiplexer	5	2
REGE8A	Octal Register With Preset and Clear	20	1
REGE8B	Octal Register With Preset and Clear	20	1
SMULT8	8 x 8 Twos Complement Multiplier	241	–
SREG4A	4-Bit Shift Register With Clear	8	1
SREG8A	8-Bit Shift Register With Clear	18	1
TA138	3-Line to 8-Line Decoder/Demultiplexer	12	2
TA139	2-Line to 4-Line Decoder/Demultiplexer	4	1
TA151	8-Line to 1-Line Multiplexer	5	3
TA153†	4-Line to 1-Line Multiplexer	2	2
TA157†	2-Line to 1-Line Multiplexer	1	1
TA161	Synchronous 4-Bit Counter With Direct Clear	22	3
TA164	8-Bit Parallel-Out Shift Register	18	1
TA169	4-Bit Up/Down Counter	25	6
TA194	4-Bit Bidirectional Universal Shift Register	14	1
TA195	4-Bit Parallel-Access Shift Register	11	1
TA269	8-Bit Up/Down Counter	50	8
TA273	Octal D-Type Flip-Flop With Clear	18	1
TA280	9-Bit Odd/Even Parity Generator/Checker	9	4
TA377	Octal D-Type Flip-Flop With Clock Enable	16	1
UDCNT4A	4-Bit Up/Down Counter With Sync Load and Carry	24	6

† These MSI functions are hardwired.

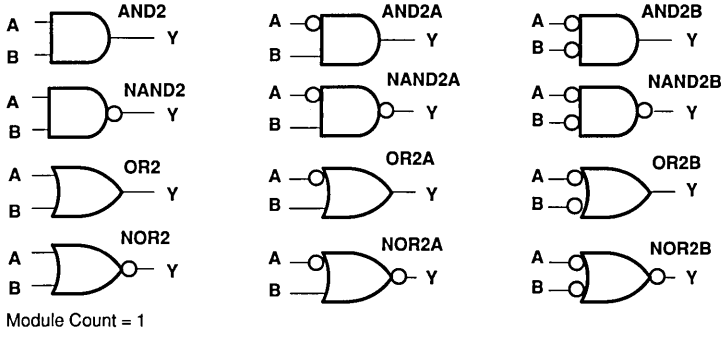


Figure 9. 2-Input Gates

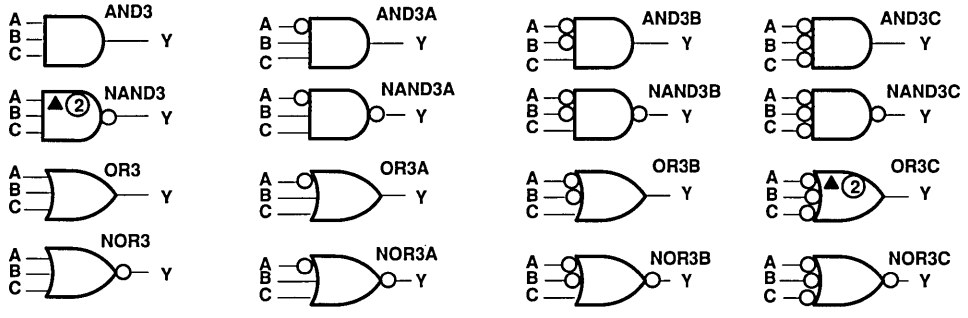
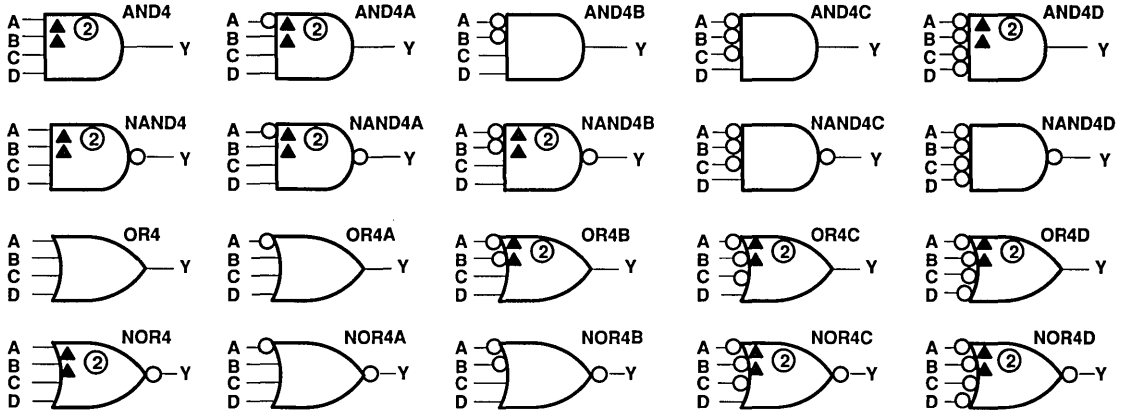


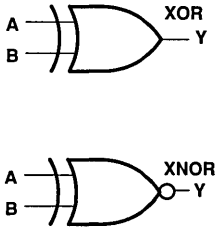
Figure 10. 3-Input Gates



Module Count = 1 (unless otherwise noted)

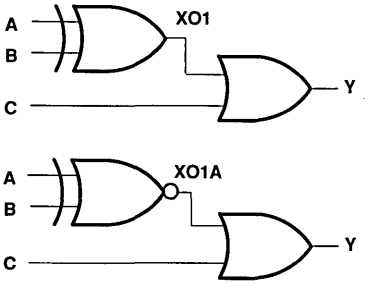
② Indicates Module Count = 2 ▲ Indicates extra delay input

Figure 11. 4-Input Gates



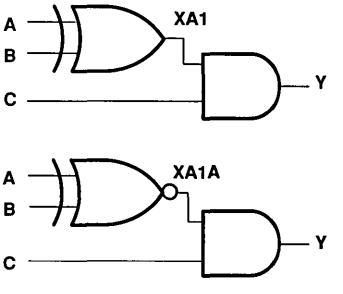
Module Count = 1

Figure 12. XOR/XNOR Gates



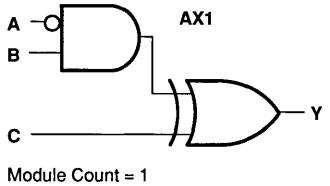
Module Count = 1

Figure 13. XOR-OR/XNOR-OR Gates



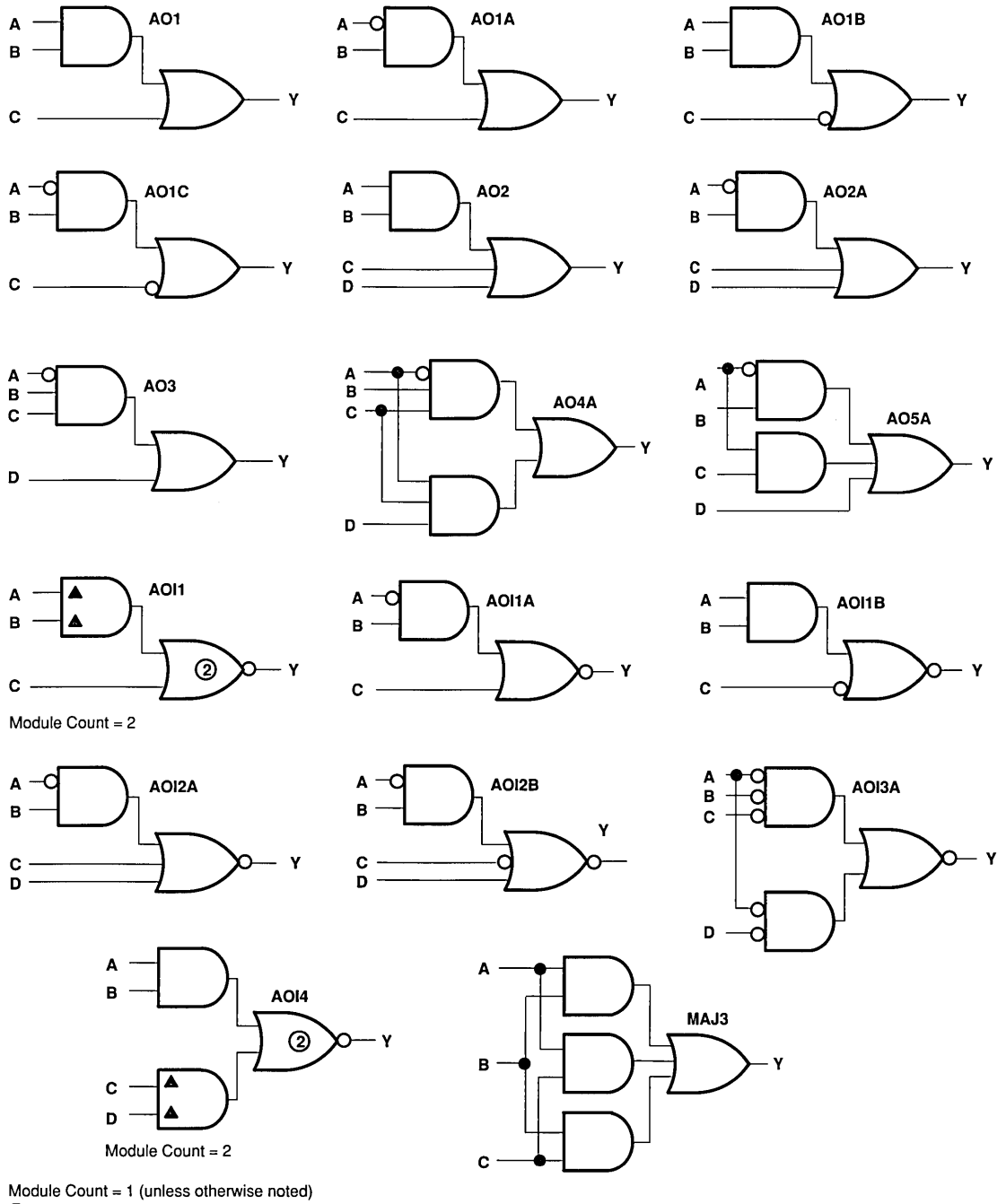
Module Count = 1

Figure 14. XOR-AND/ XNOR-AND Gates



Module Count = 1

Figure 15. AND-XOR/AND-XNOR Gates

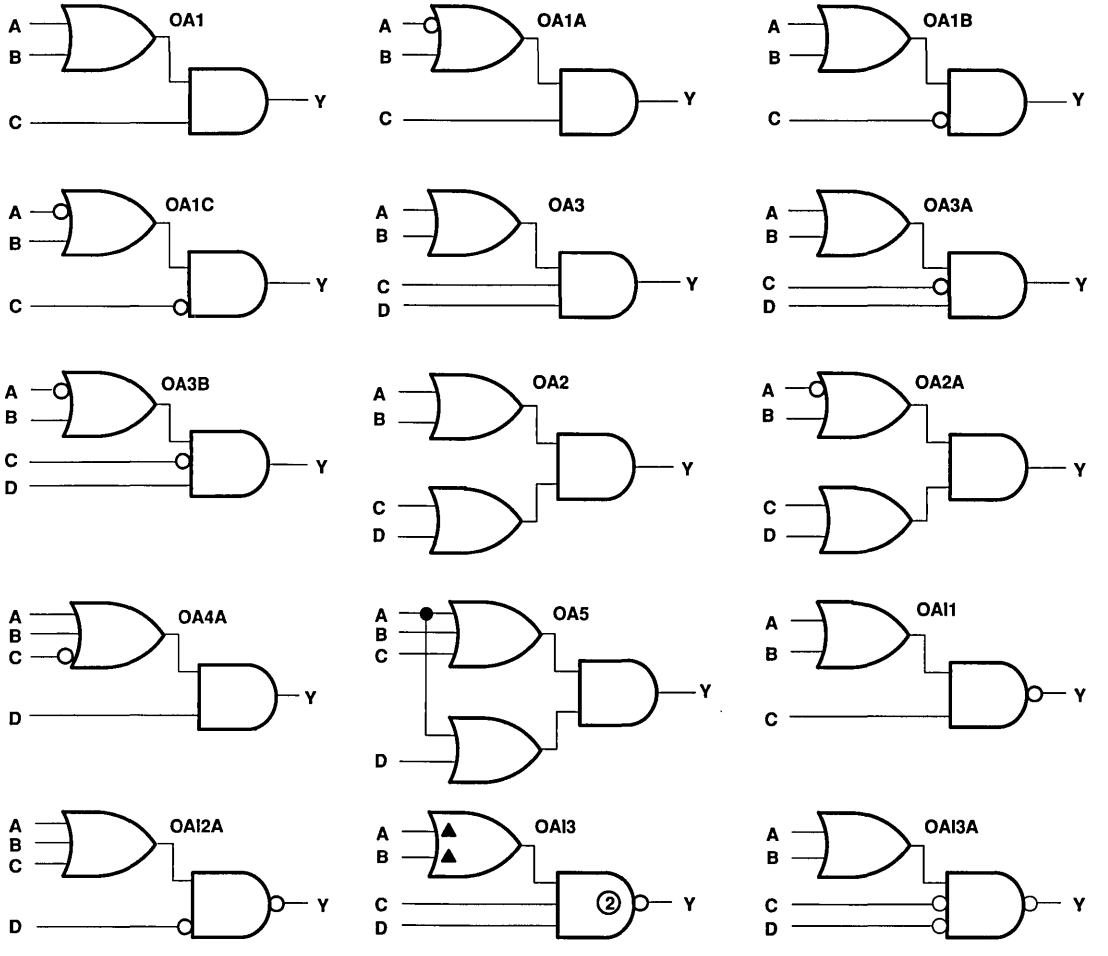


Module Count = 2

Module Count = 2

Module Count = 1 (unless otherwise noted)
② Indicates Module Count = 2
▲ Indicates extra delay input

Figure 16. AND-OR/AND-NOR Gates

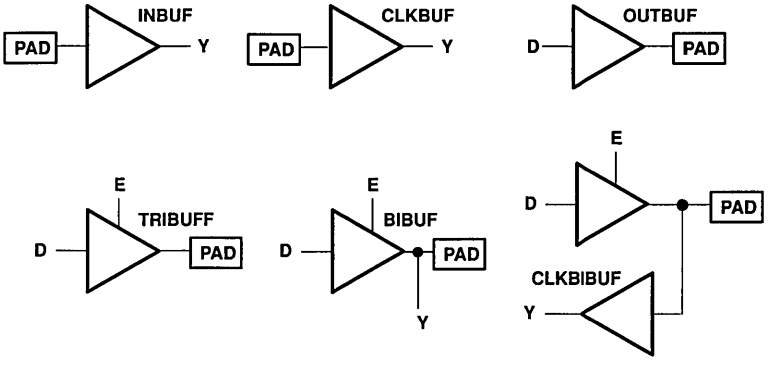


Module Count = 1 (unless otherwise noted)
▲ Indicates extra delay input
② Module Count = 2

Figure 17. OR-AND/OR-NAND Gates

Module Count = 1

Figure 18. Buffers



I/O Module Count = 1

Figure 19. I/O Buffers

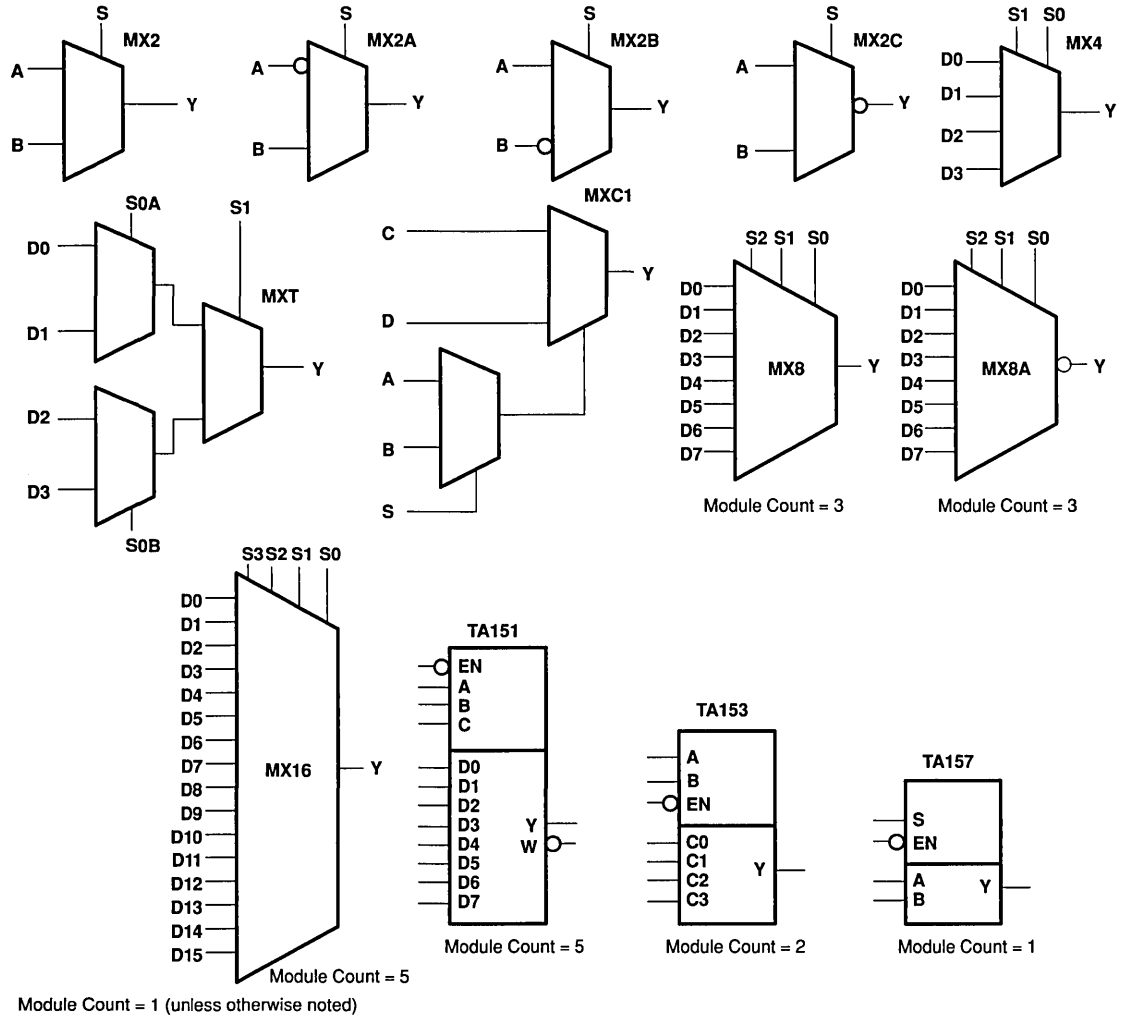
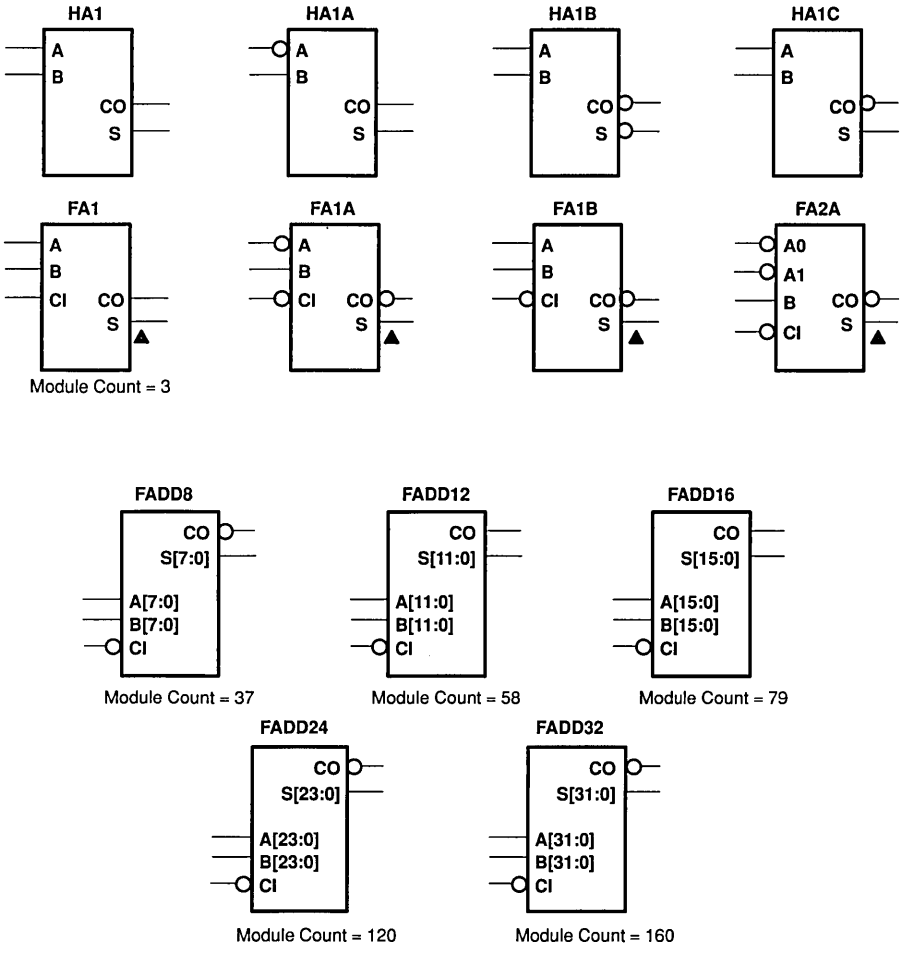


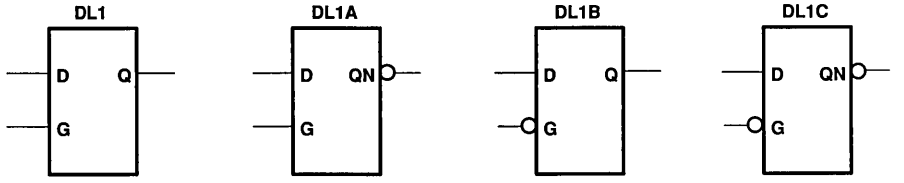
Figure 20. Multiplexers



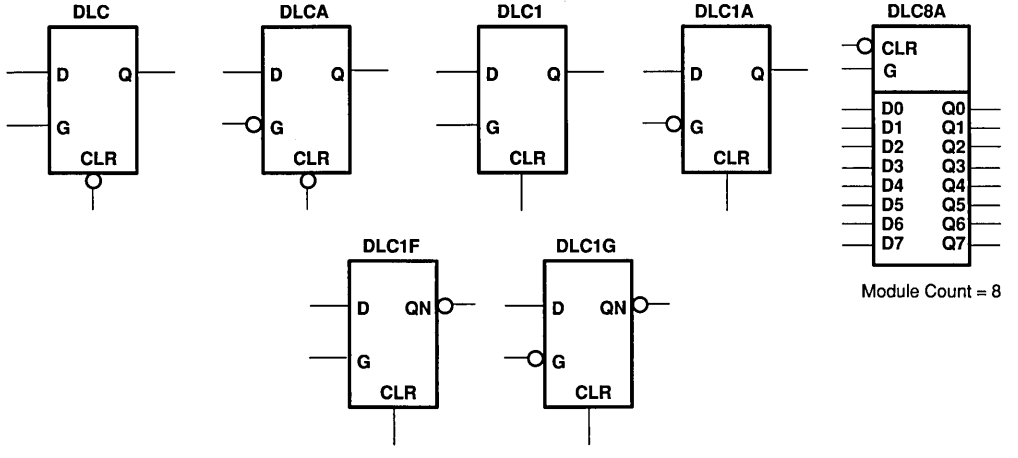
Module Count = 2 (unless otherwise noted)
▲ Indicates two logic module delay path

Figure 21. Adders

D-TYPE LATCHES

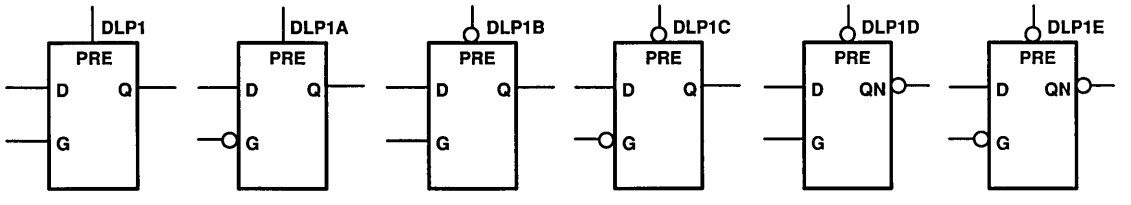


D-TYPE LATCHES WITH CLEAR

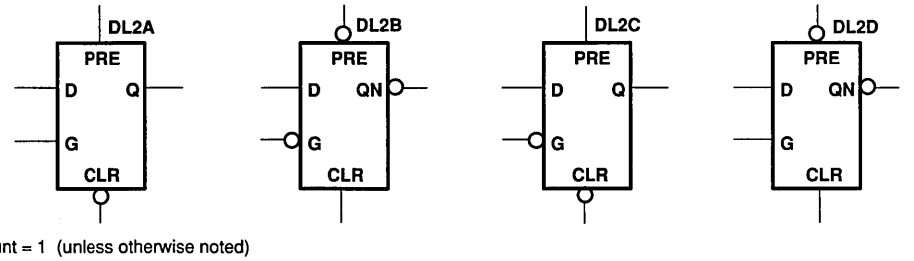


Module Count = 8

D-TYPE LATCHES WITH PRESET



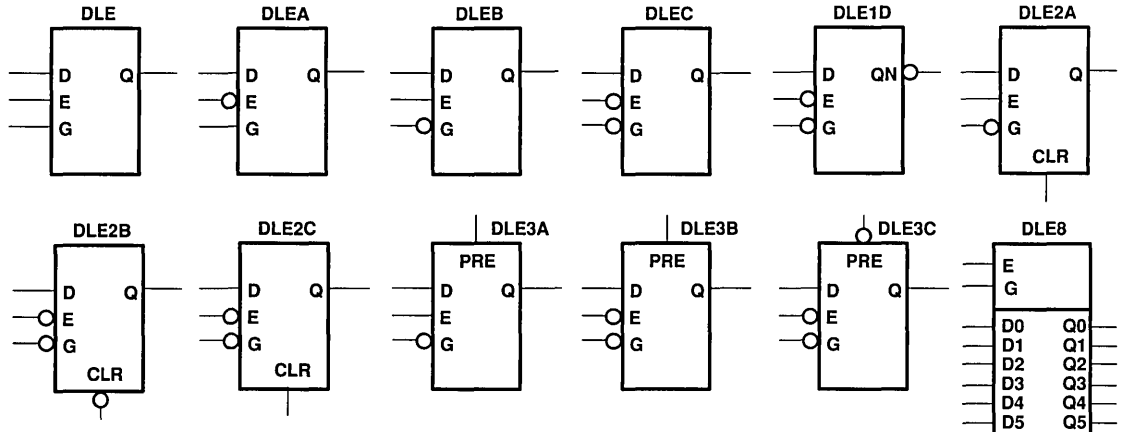
D-TYPE LATCHES WITH CLEAR AND PRESET



Module Count = 1 (unless otherwise noted)

Figure 22. D-Type Latches

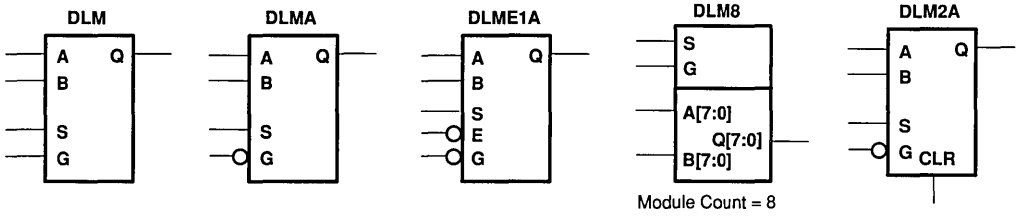
D-TYPE LATCHES WITH ENABLE



Module Count = 1 (unless otherwise noted)

Module Count = 8

D-TYPE LATCHES WITH MULTIPLEXED INPUTS

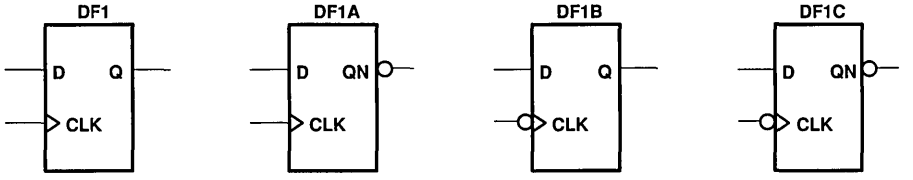


Module Count = 8

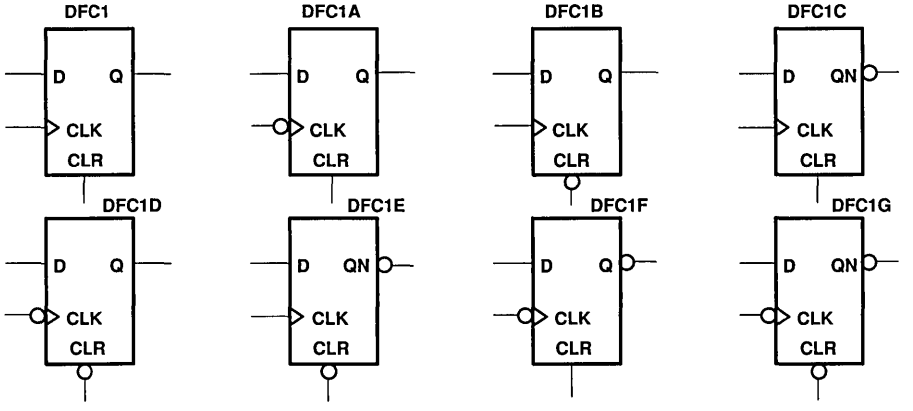
Module Count = 1 (unless otherwise noted)

Figure 22. D-Types Latches (Continued)

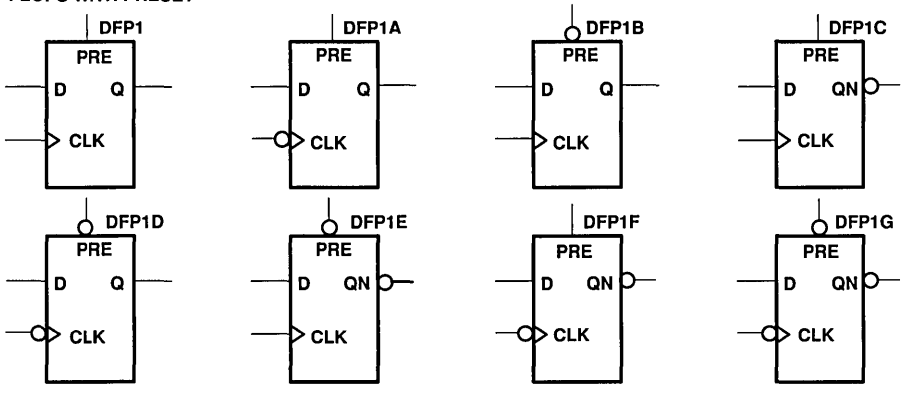
D-TYPE FLIP-FLOPS



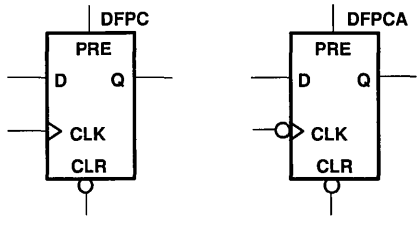
D-TYPE FLIP-FLOPS WITH CLEAR



D-TYPE FLIP-FLOPS WITH PRESET

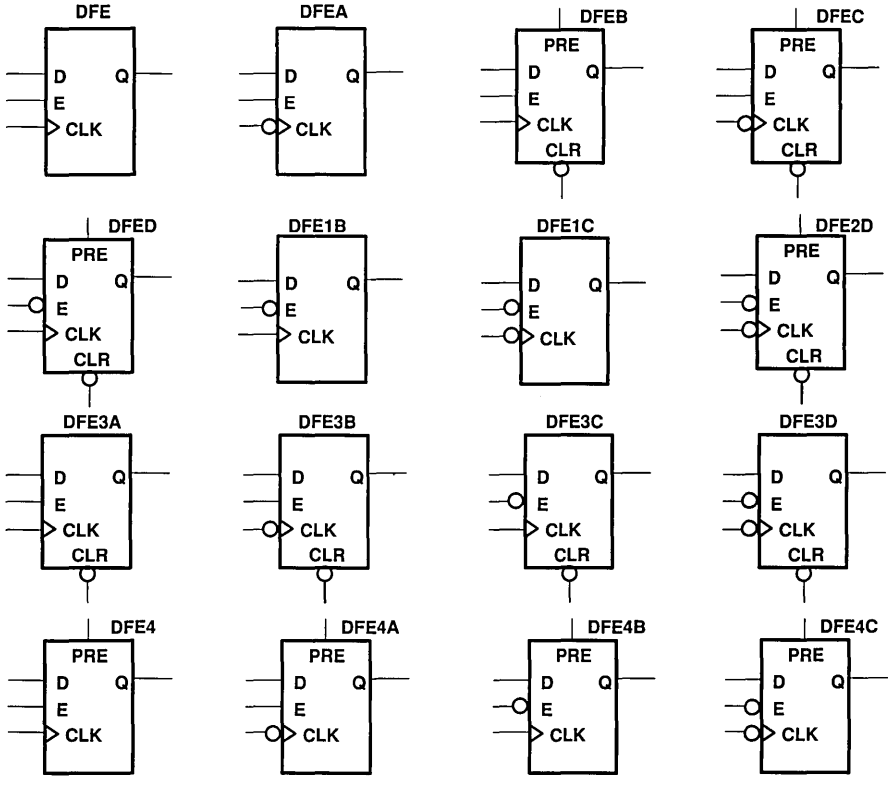


D-TYPE FLIP-FLOPS WITH PRESET AND CLEAR



Module Count = 2

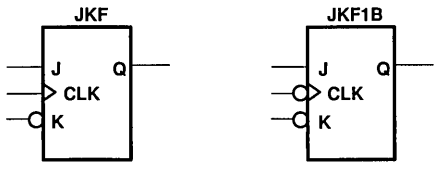
Figure 23. D-Type Flip-Flops



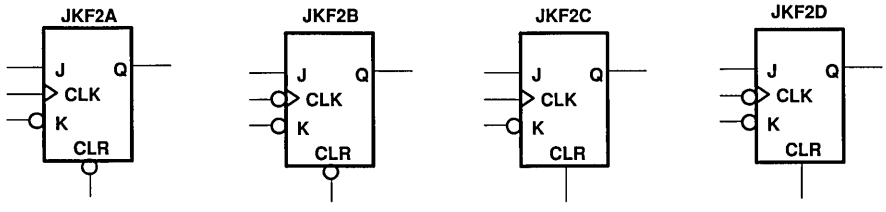
Module Count = 2

Figure 24. D-Type Flip-Flops With Enable

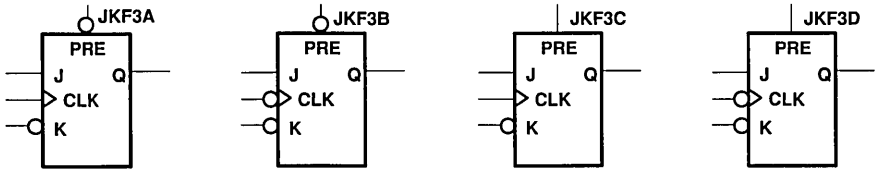
J-$\overline{K}$ FLIP-FLOPS



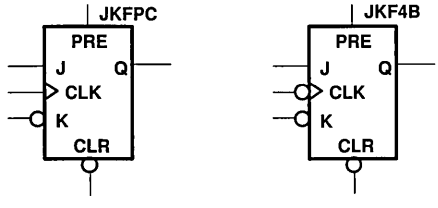
J-$\overline{K}$ FLIP-FLOPS WITH CLEAR



J-$\overline{K}$ FLIP-FLOPS WITH PRESET



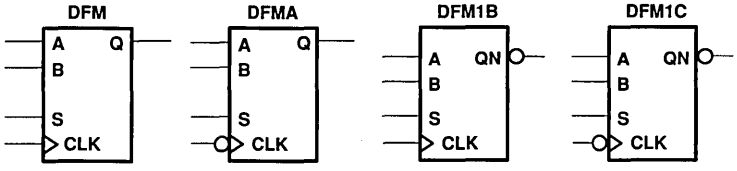
J-$\overline{K}$ FLIP-FLOPS WITH PRESET AND CLEAR



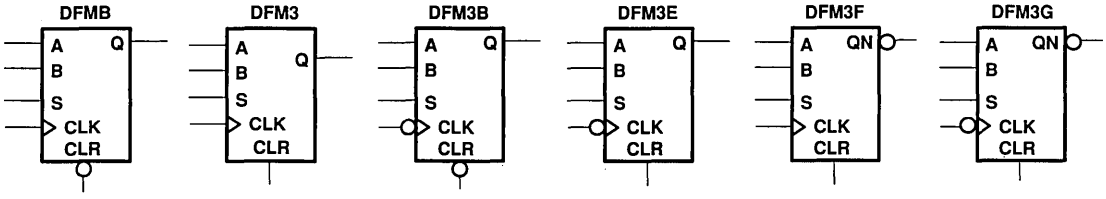
Module Count = 2

Figure 25. J-$\overline{K}$ Flip-Flops

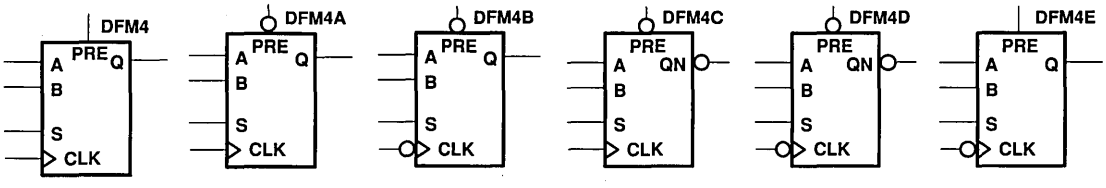
MULTIPLEXED-INPUT FLIP-FLOPS



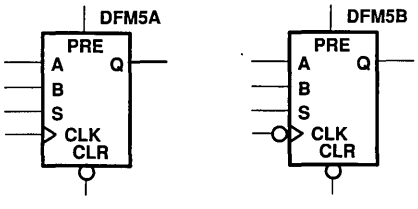
MULTIPLEXED-INPUT FLIP-FLOPS WITH CLEAR



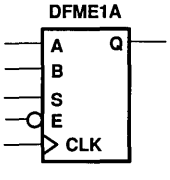
MULTIPLEXED-INPUT FLIP-FLOPS WITH PRESET



MULTIPLEXED-INPUT FLIP-FLOPS WITH PRESET AND CLEAR



MULTIPLEXED-INPUT FLIP-FLOPS WITH ENABLE



Module Count = 2

Figure 26. Multiplexed-Input Flip-Flops

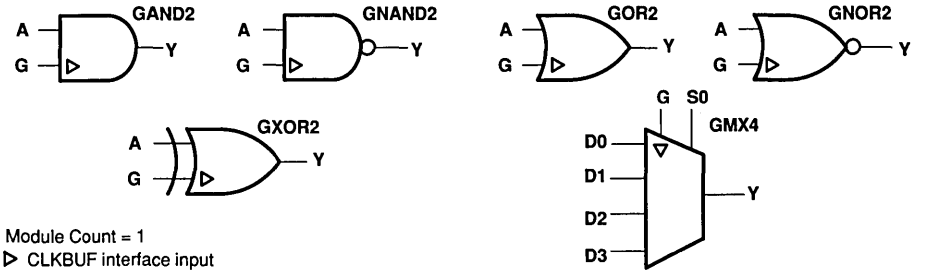


Figure 27. Clock Buffer (CLKBUF) Interface

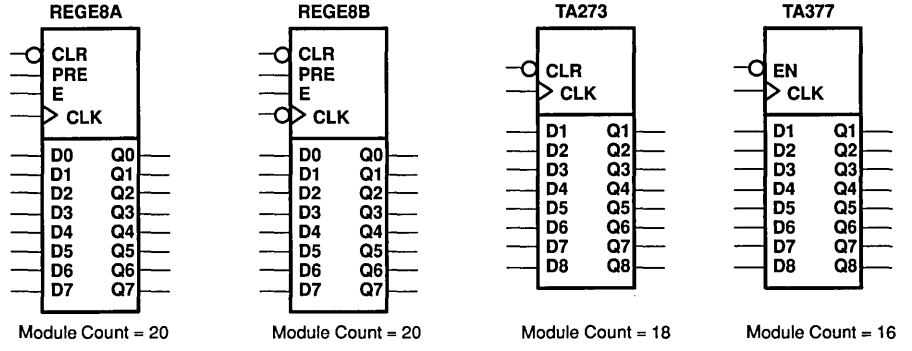


Figure 28. Octal D-Type Flip-Flops and Registers

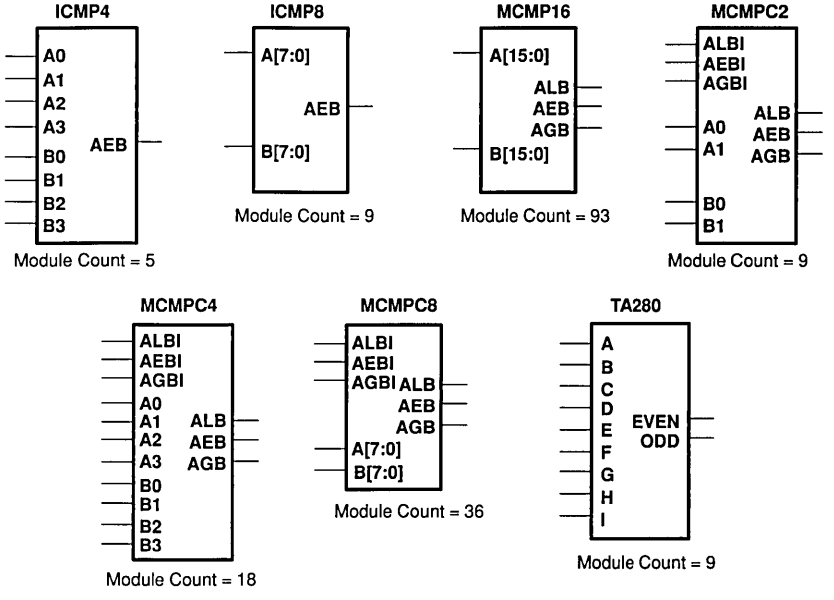


Figure 29. Comparators/Parity Checker

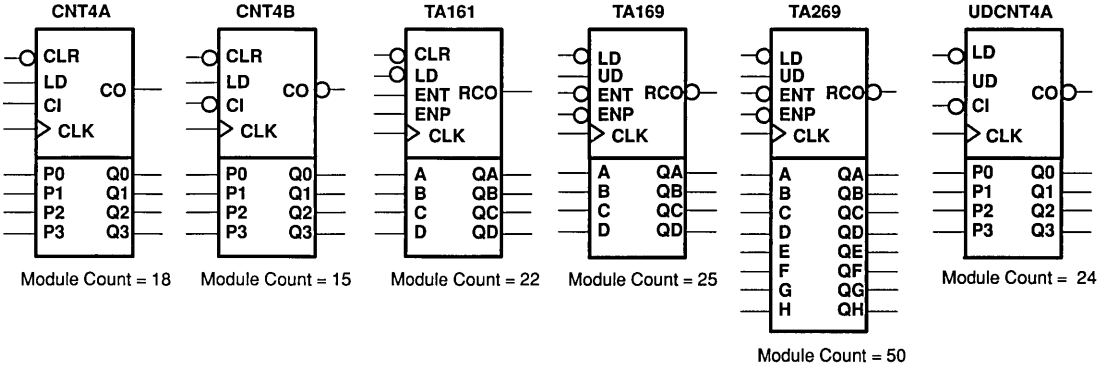


Figure 30. Counters

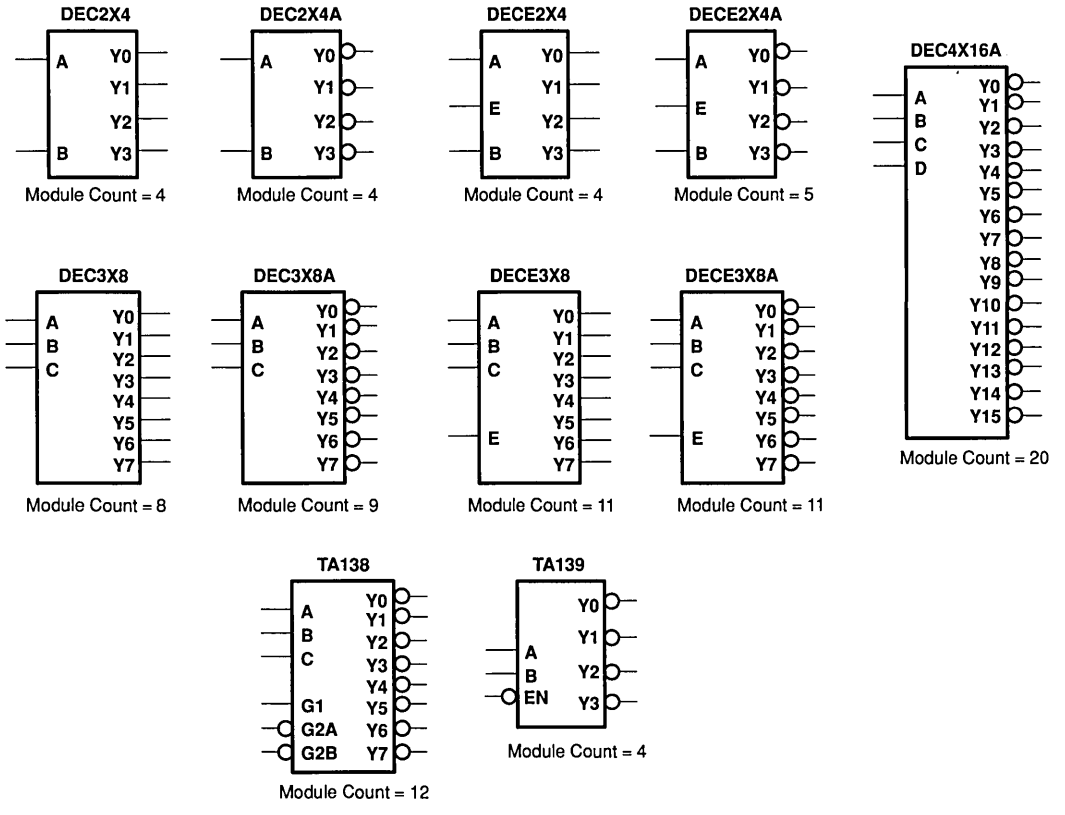


Figure 31. Decoders

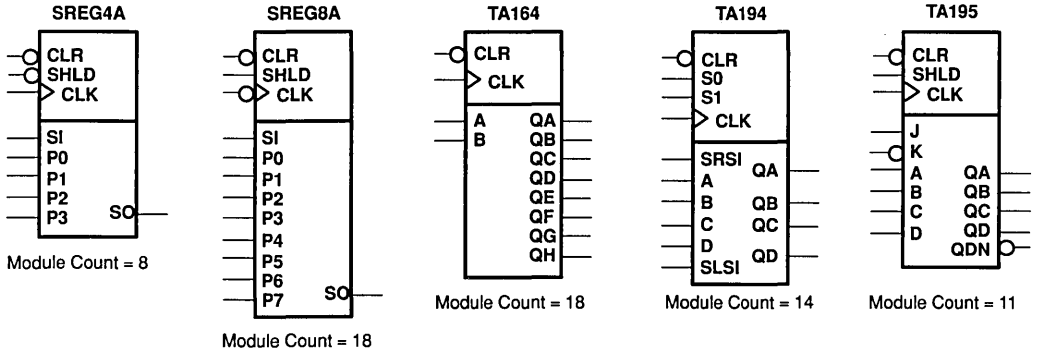


Figure 32. Shift Registers

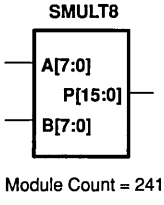


Figure 33. 8-Bit Multiplier

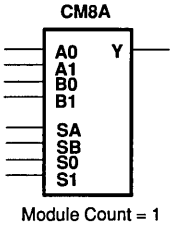
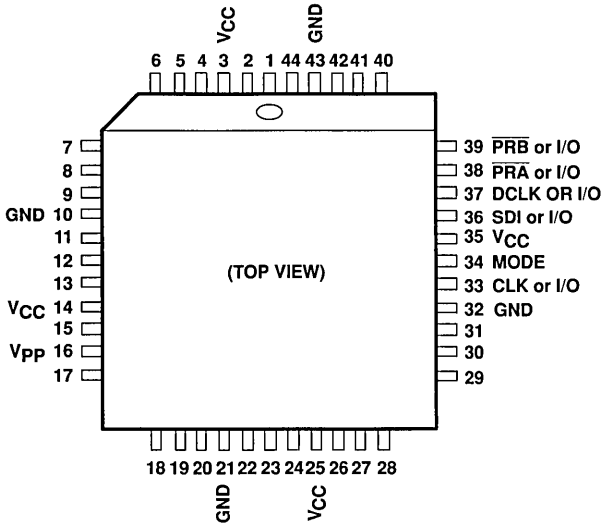


Figure 34. Logic Module

package pin assignments

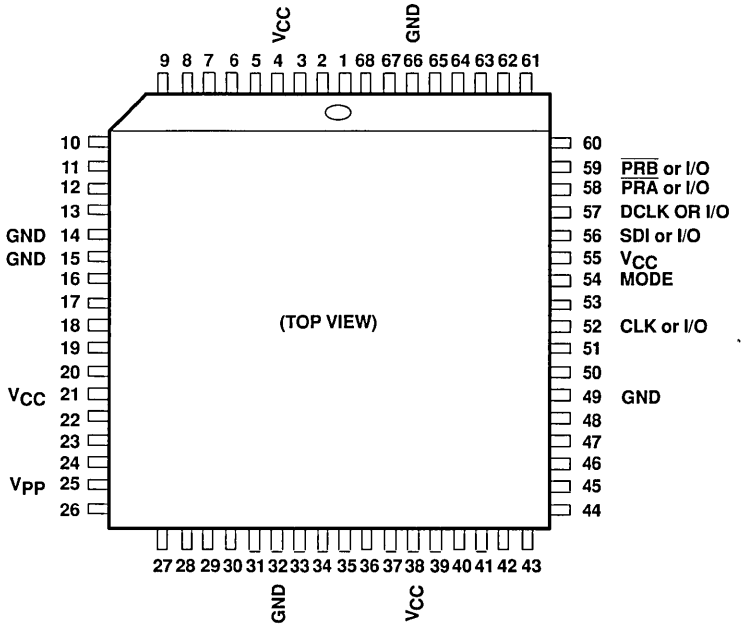


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 35. 44-Pin PLCC Pin Assignment

package pin assignments (continued)

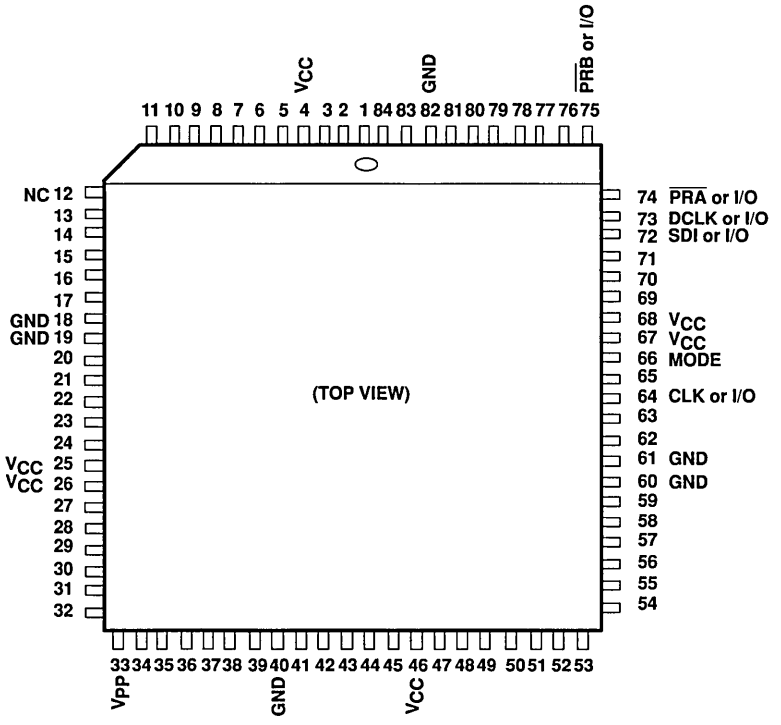


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 36. 68-Pin PLCC Pin Assignment

package pin assignments (continued)

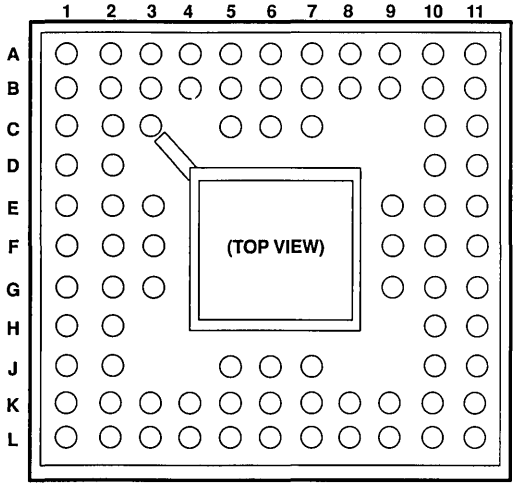


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 37. 84-Pin PLCC Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 84-Pin Ceramic Pin Grid Array Package

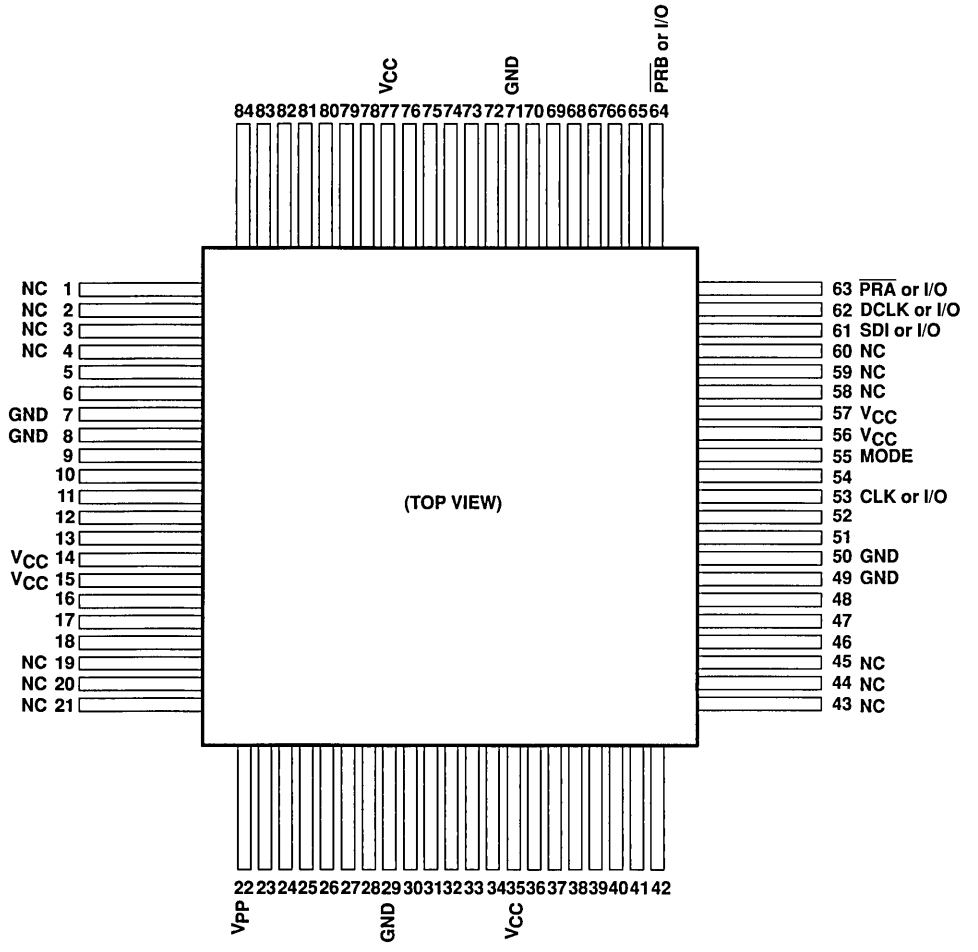
SIGNAL	TPC1010A	TPC1020A
$\overline{PRA}$	A11	A11
$\overline{PRB}$	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
NC (No internal connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. Orientation pin C3 is connected internally to pin C2.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 38. 84-Pin CPGA Pin Assignment

package pin assignments (continued)

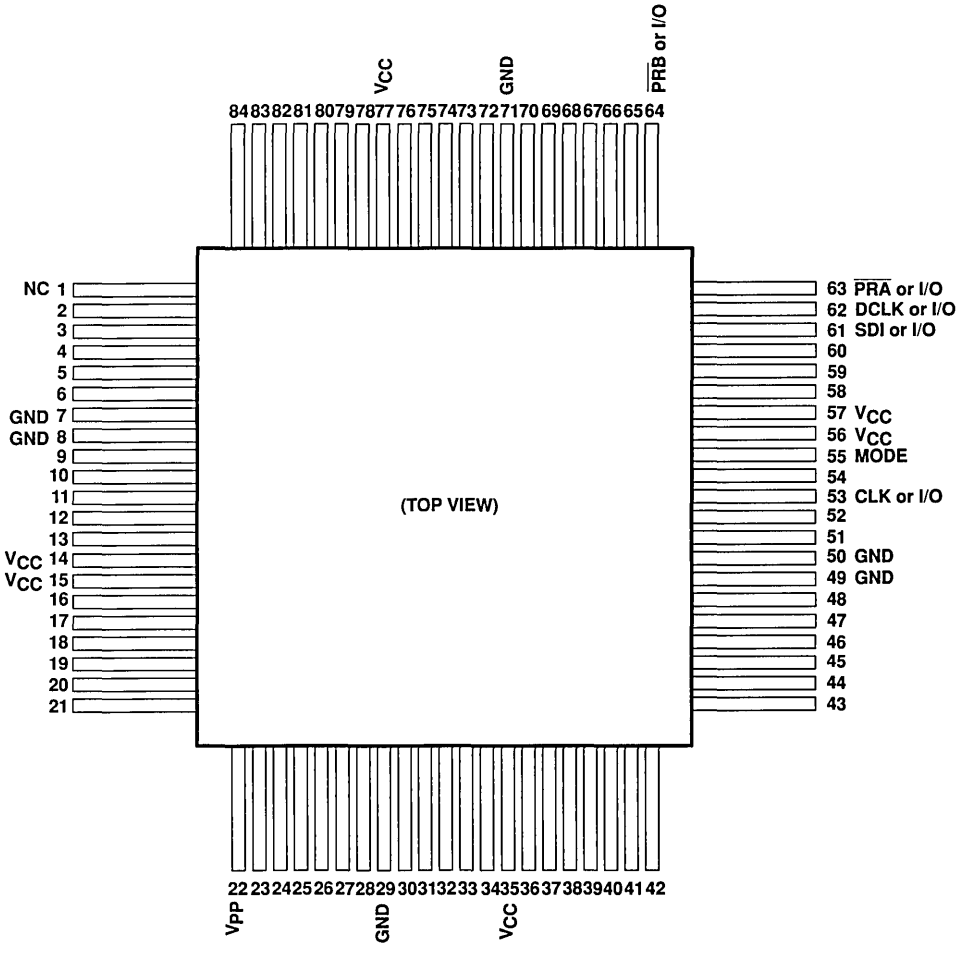


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 39. TPC1010A 84-Pin CQFP Pin Assignment

package pin assignments (continued)

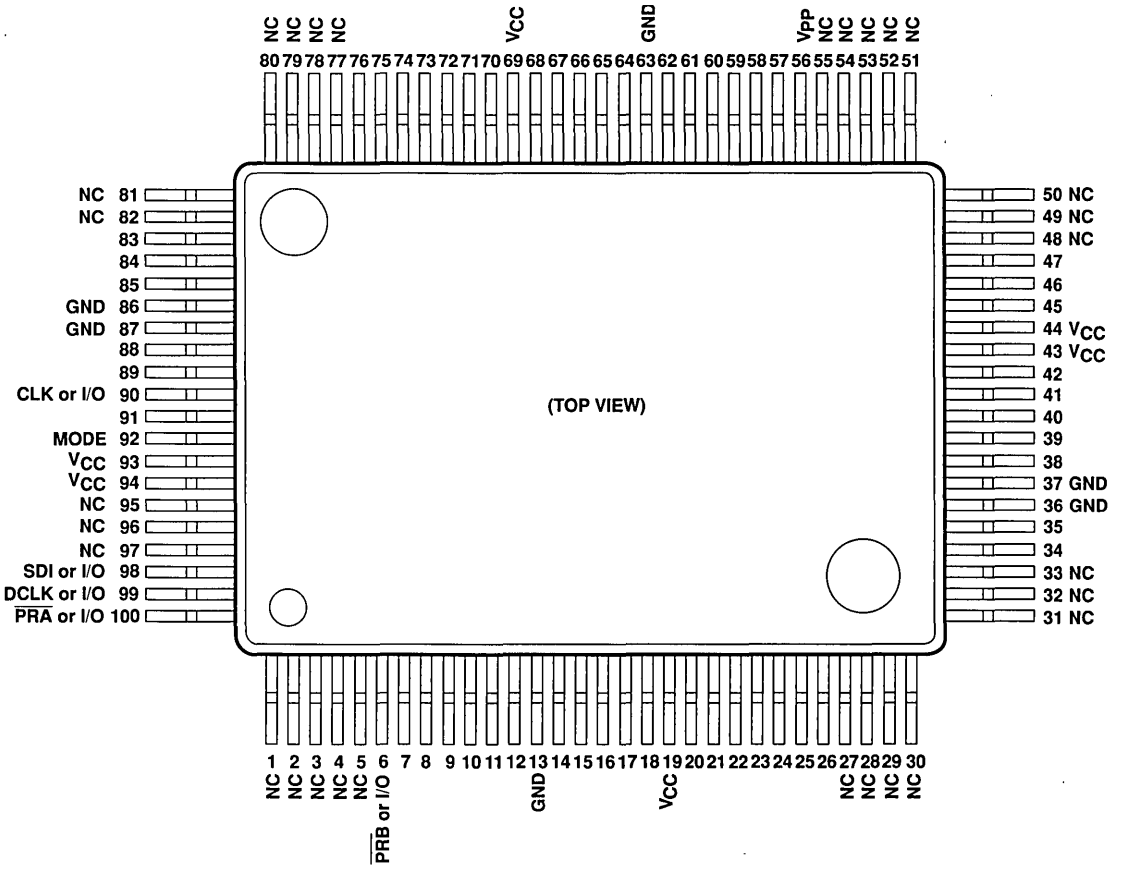


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 40. TPC1020A 84-Pin CQFP Pin Assignment

package pin assignments (continued)

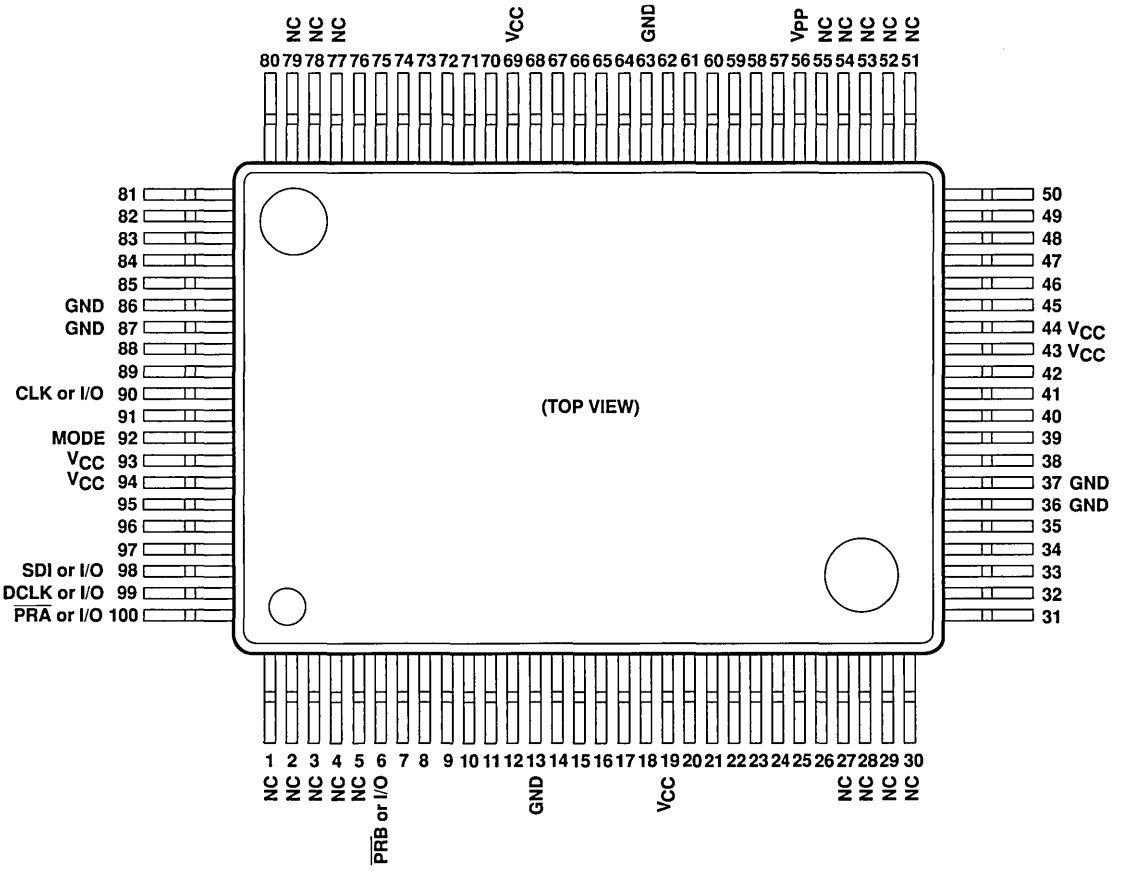


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 41. TPC1010A 100-Pin PQFP Pin Assignment

package pin assignments (continued)



NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 42. TPC1020A 100-Pin PQFP Pin Assignment

actionprobe pin assignments

There are four types of Actionprobes available: 44-, 68-, and 84-pin PLCC, and 84-pin PGA. At the time your order is placed, please specify which Actionprobe you need.

The Actionprobes are detailed in Figure 43 through Figure 46.

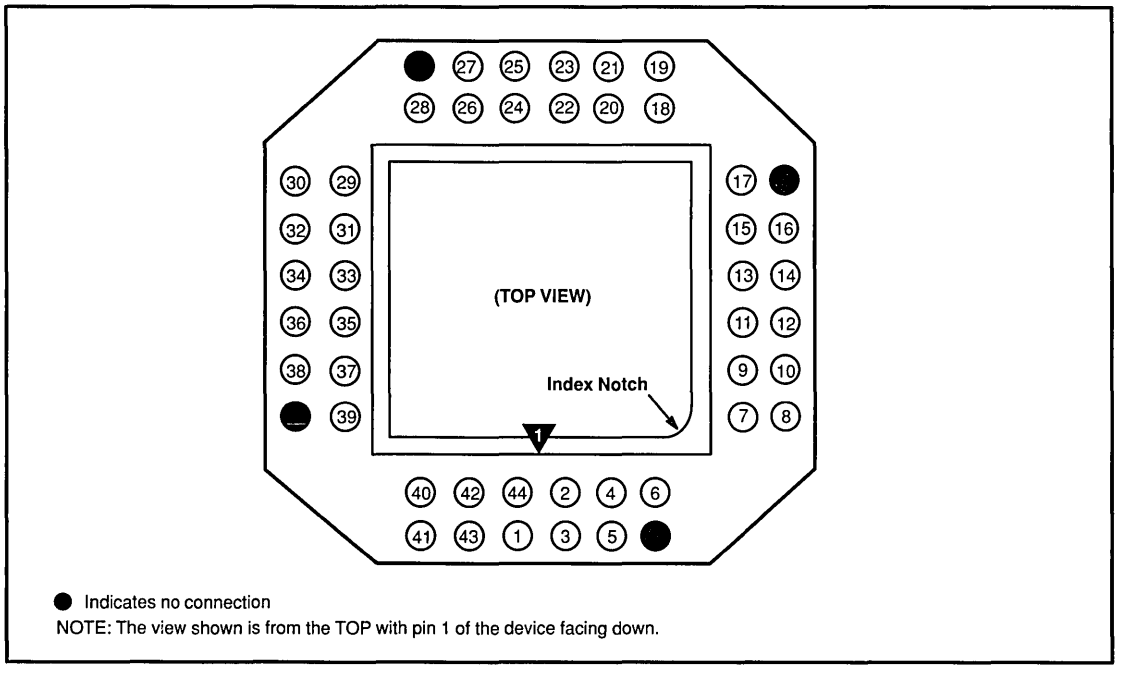
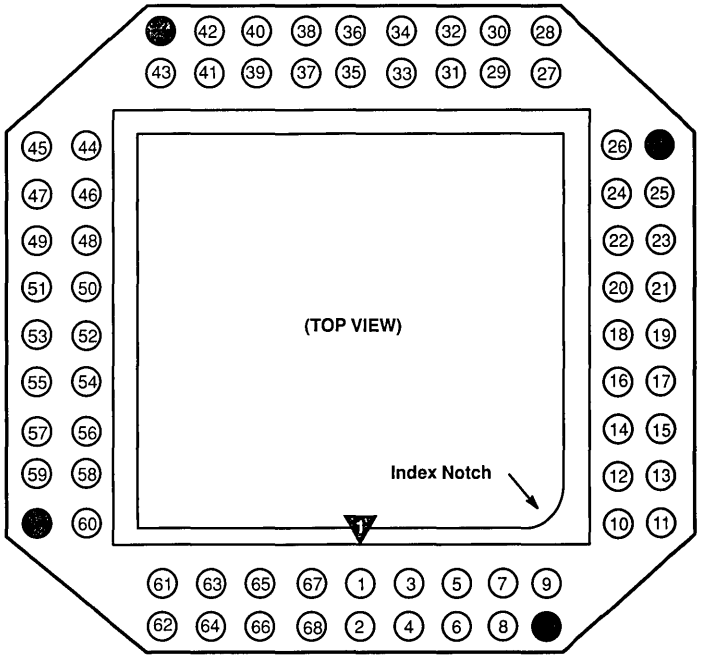


Figure 43. 44-Pin PLCC Actionprobe

actionprobe pin assignments (continued)



● Indicates no connection

NOTE: The view shown is from the TOP with pin 1 of the device facing down.

Figure 44. 68-Pin PLCC Actionprobe

actionprobe pin assignments (continued)

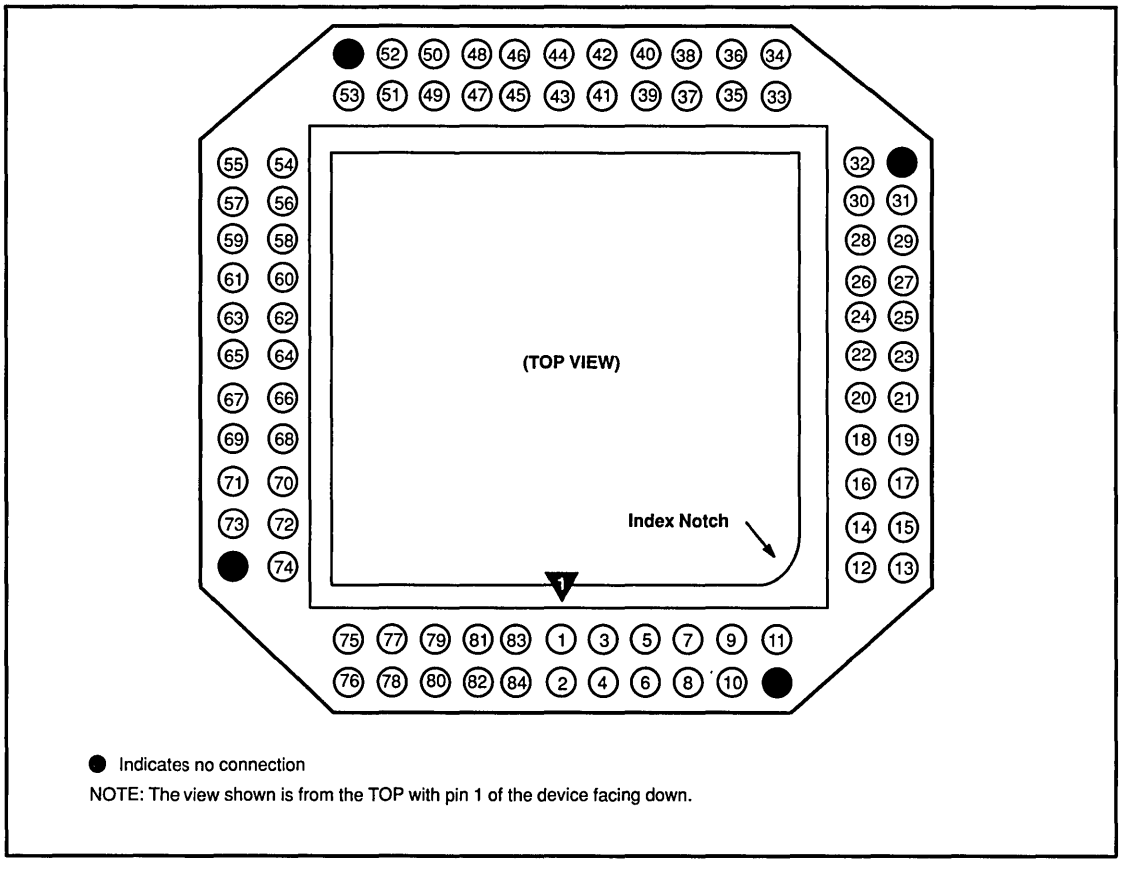


Figure 45. 84-Pin PLCC Actionprobe

actionprobe pin assignments (continued)

The 84-pin pin-grid-array (PGA) Actionprobe has a number of pins around the socket connected to the device pins. The exact ordering of these pins is not obvious.

Figure 46 shows the Actionprobe with the top view up, which is how the device sits in the socket. Pin A1 is at the top left. Looking at the Actionprobe, pin A1 appears on the circuit board for reference.

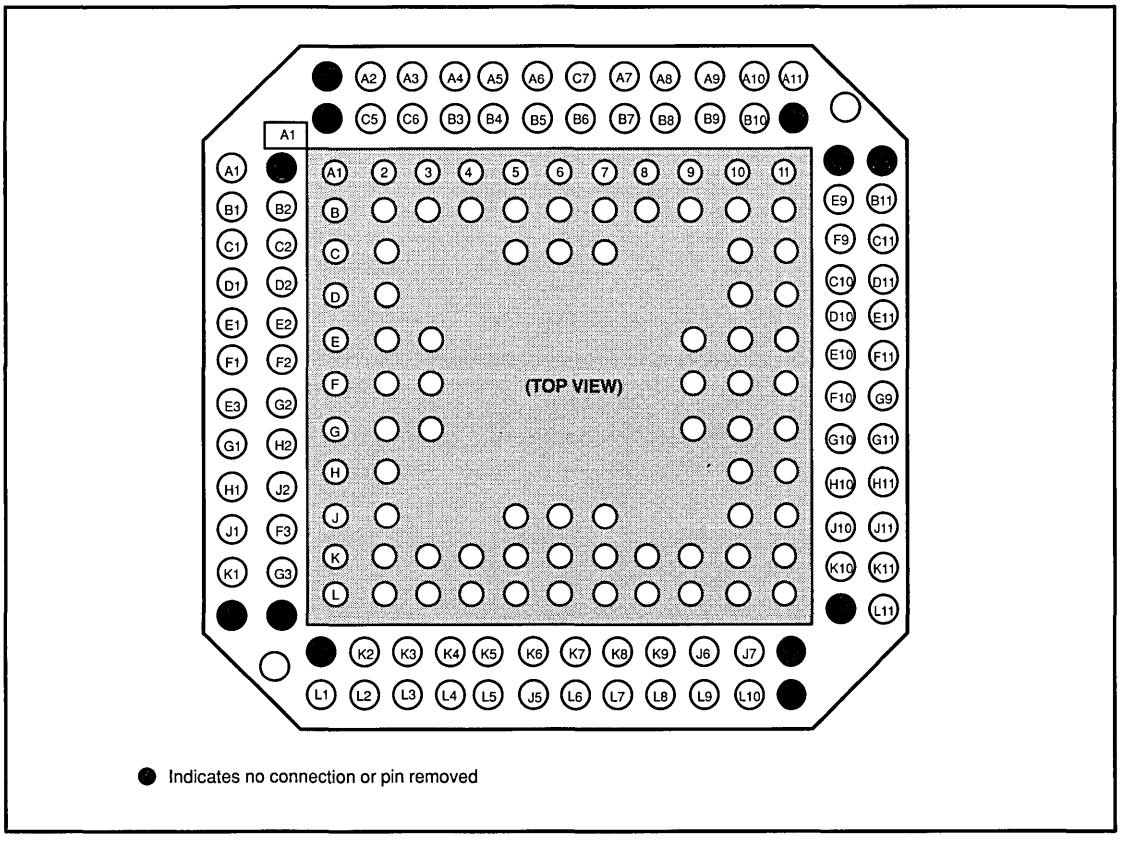
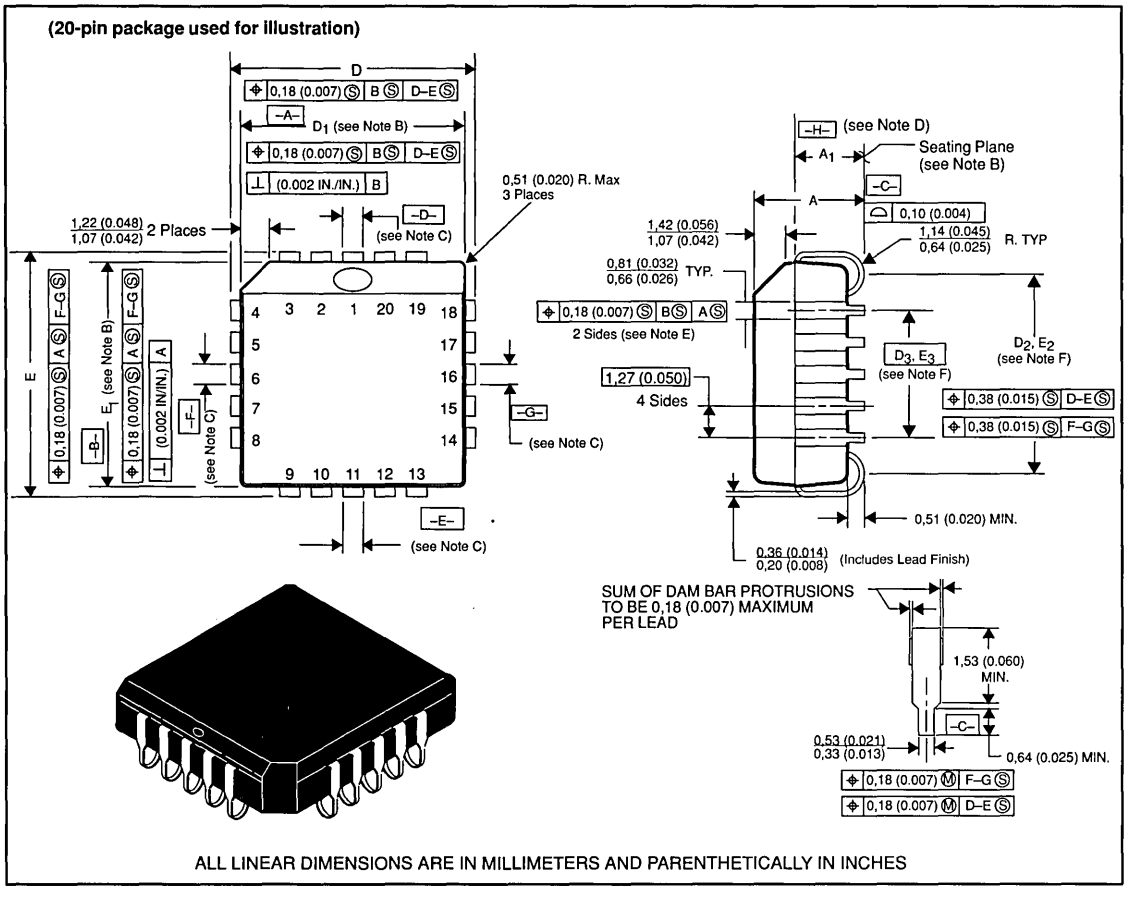


Figure 46. 84-Pin PGA Actionprobe



JEDEC OUTLINE	DIMS / PINS	A MIN	A MAX	A1 MIN	A1 MAX	D, E MIN	D, E MAX	D1, E1 MIN	D1, E1 MAX	D2, E2 MIN	D2, E2 MAX	D3, E3 BASIC
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,04 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

B. Dimension D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (.010) on any side.

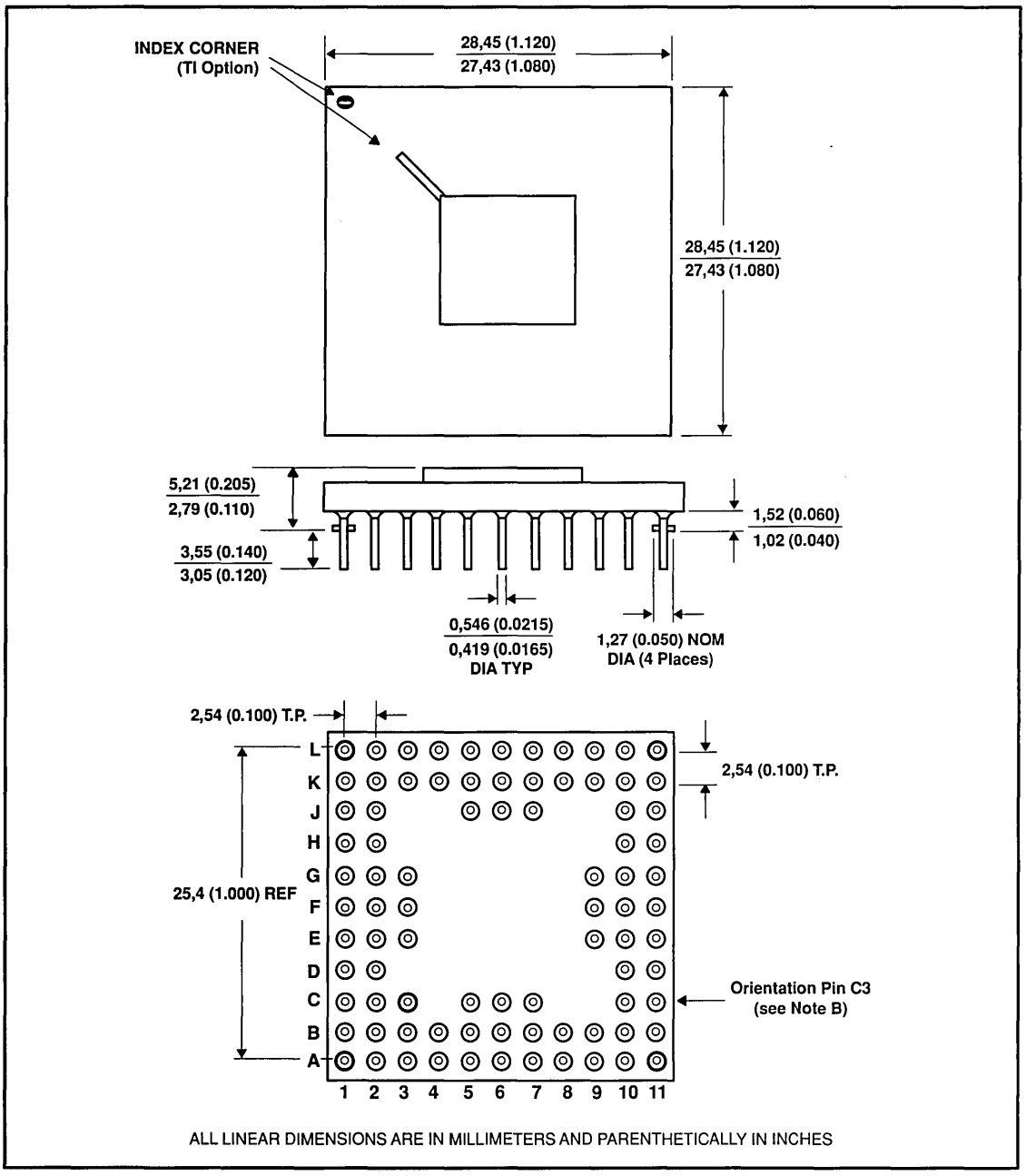
C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

Figure 47. Plastic Leaded Chip Carriers



NOTES: A. Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,381 (0.051) radius relative to the center of the ceramic.
B. Orientation pin C3 is connected internally to pin C2.

Figure 48. 84-Pin Ceramic Pin-Grid-Array Package

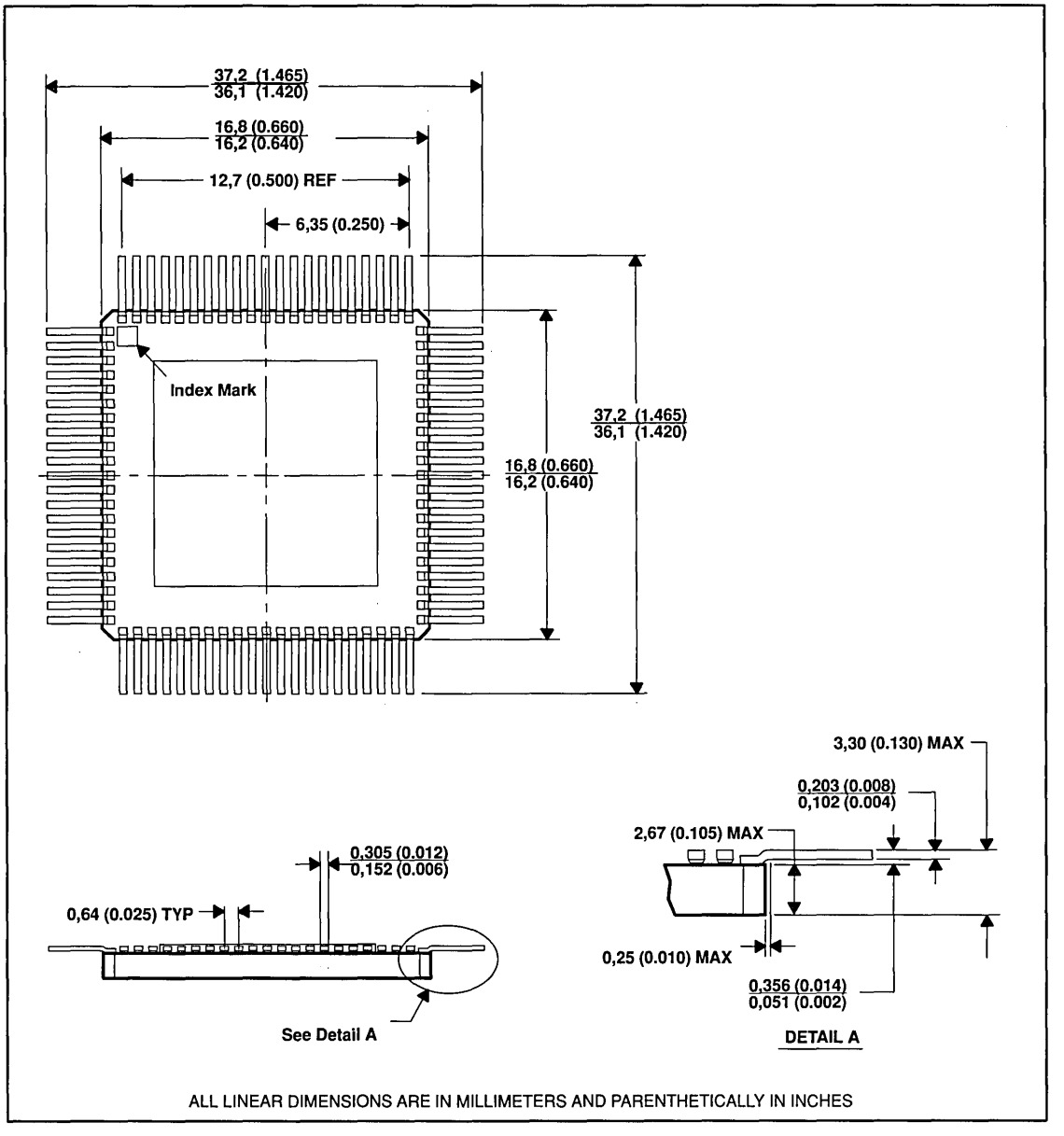


Figure 49. 84-Pin Ceramic Quad Flat Package

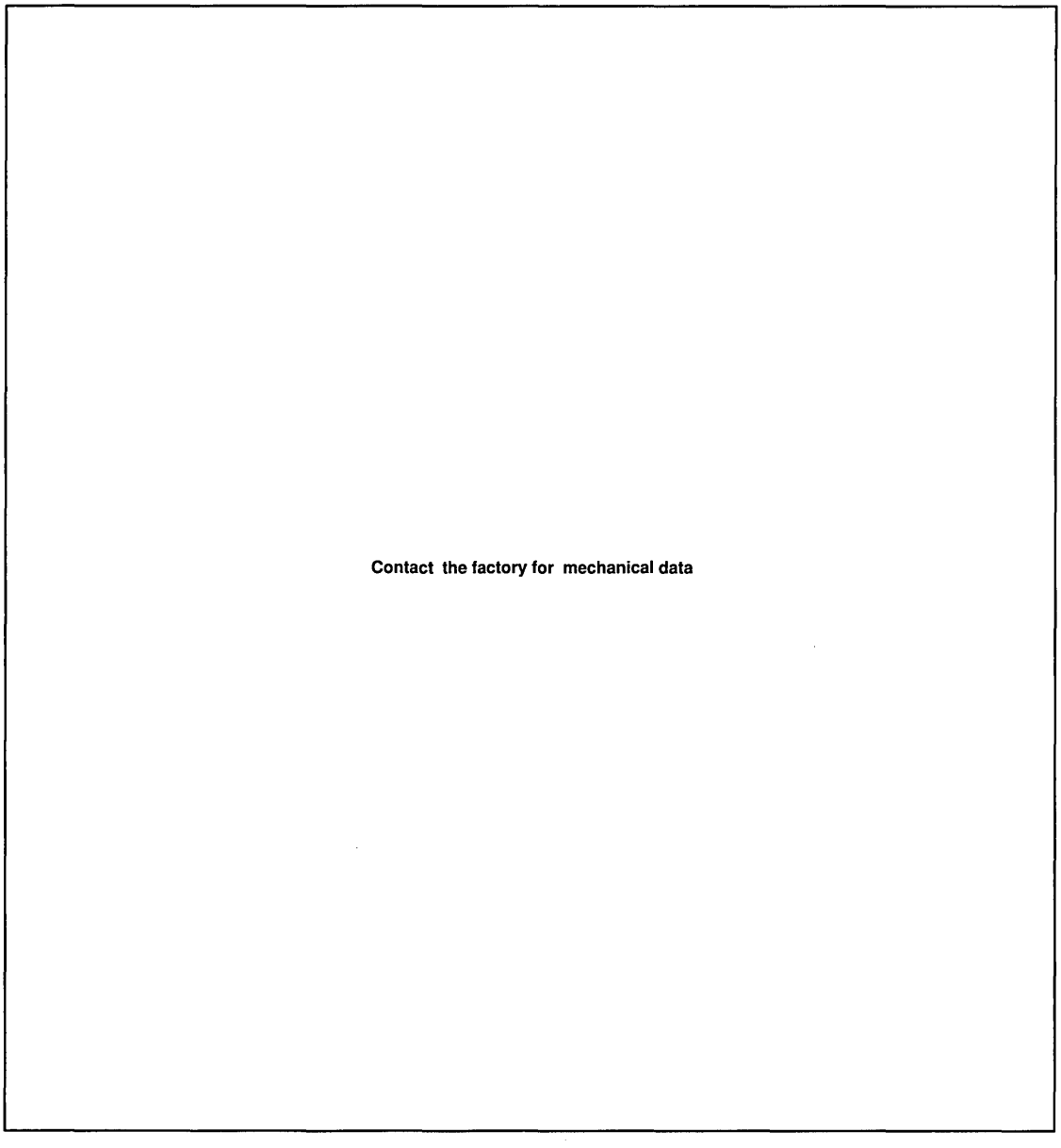


Figure 50. 84-Pin Ceramic Quad Flat Package With Nonconductive Tie Bar

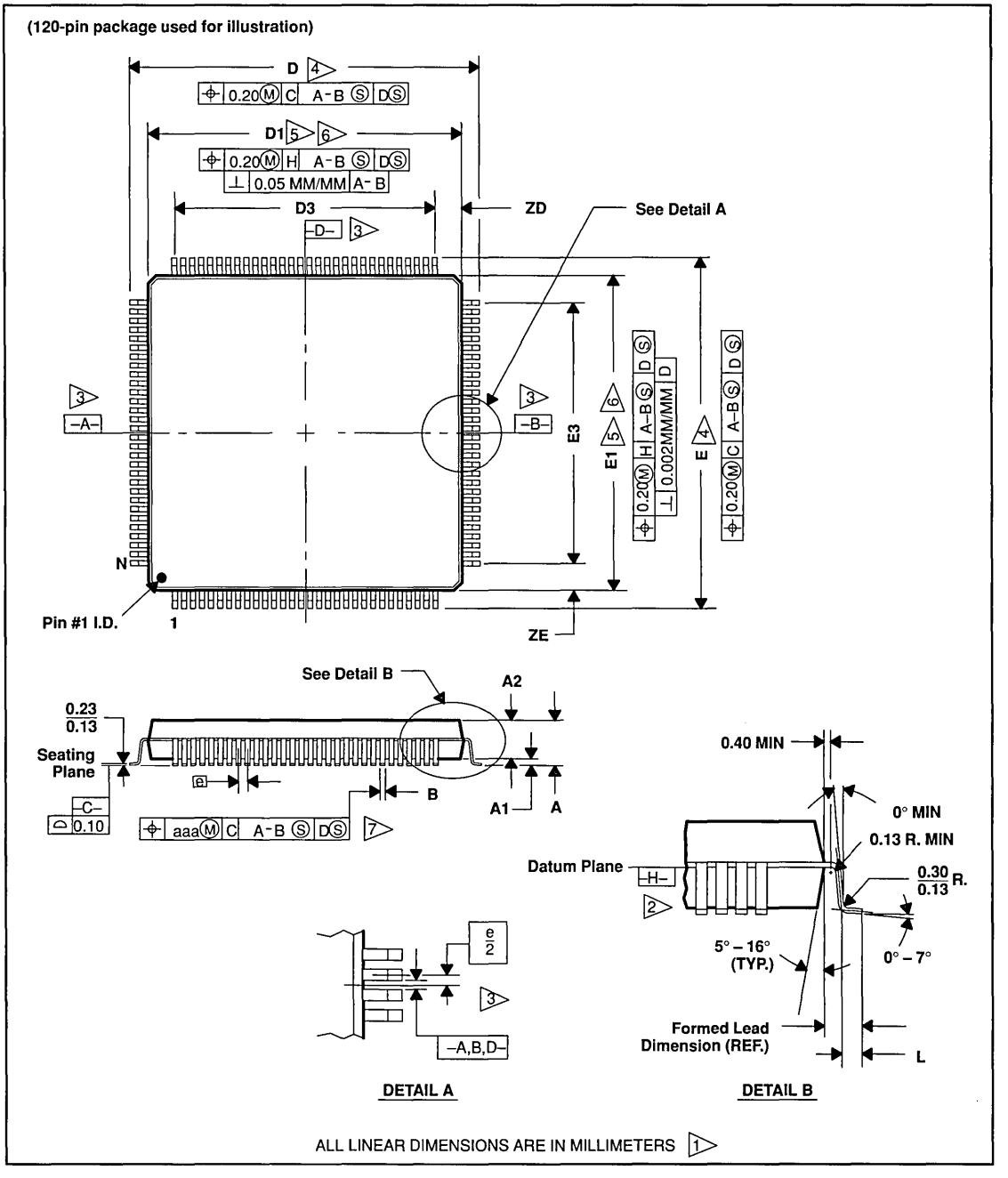


Figure 51. Plastic Quad Flat Packages

JEDEC OUTLINE	# PINS	PKG TYPE	A MAX	A1 MIN	A2 MAX MIN	D MAX MIN	D1 MAX MIN	D3 (REF)	ZD (REF)	E MAX MIN	E1 MAX MIN	E3 (REF)	ZE (REF)	L MAX MIN	e BASIC	B MAX MIN	aaa	ND	NE	FORMED LEAD DIM. (REF)
MO-108/CC-1	100	RECT	3,40	0,25	3,05 2,55	23,45 22,95	20,10 19,90	18,85	0,58	17,45 16,95	14,10 13,90	12,35	0,83	0,95 0,65	0,65	0,38 0,22	0,12	30	20	1,60

NOTES:
1. All dimensions are millimeters (mm), and conform to JEDEC specification MO-108 (issue A/October 1990). Dimensions and tolerancing per ANSI Y14.5M-1982.
2. Datum plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and –D– for center leads are determined at datum –H– .
4. Determined at seating plane –C–
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane –H– .
6. Determined at datum plane –H–
7. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. A minimum solder finish thickness of 0.0051 is guaranteed.

Following are the pin loadings for the TPC10 Series 1.2-μm and 1.0-μm CMOS Field-Programmable Gate Arrays. Use this with the TPC10 Series Data Sheet and the Critical Path Analysis for FPGAs application report located in the Applications Chapter in this manual, to estimate manually the achievable system speed for a design implemented in a TI TPC10 Series FPGA. The index below will help you find the desired item in this supplement.

Name	Page	Table
DLP1D	2-67	32
DLP1E	2-67	32
FA1	2-66	22
FA1A	2-66	22
FA1B	2-66	22
FA2A	2-66	23
FADD12	2-66	25
FADD16	2-66	26
FADD24	2-66	27
FADD32	2-67	28
FADD8	2-66	24
GAND2	2-71	49
GMX4	2-71	50
GNAND2	2-71	49
GNOR2	2-71	49
GOR2	2-71	49
GXOR2	2-71	49
HA1	2-66	21
HA1A	2-66	21
HA1B	2-66	21
HA1C	2-66	21
ICMP4	2-71	53
ICMP8	2-71	53
INBUF	2-65	11
INV	2-64	10
INVA	2-64	10
JKF	2-70	45
JKF1B	2-70	45
JKF2A	2-70	45
JKF2B	2-70	45
JKF2C	2-70	45
JKF2D	2-70	45
JKF3A	2-70	45
JKF3B	2-70	45
JKF3C	2-70	45
JKF3D	2-70	45
JKF4B	2-70	45
JKFPC	2-70	45
MAJ3	2-64	8
MCMP16	2-72	54
MCMPC2	2-72	54
MCMPC4	2-72	54
MCMPC8	2-72	54
MX16	2-65	17
MX2	2-65	12
MX2A	2-65	12
MX2B	2-65	12
MX2C	2-65	12
MX4	2-65	13
MX8	2-65	16
MX8A	2-65	16
MXC1	2-65	15
MXT	2-65	14
NAND2	2-62	1
NAND2A	2-62	1
NAND2B	2-62	1
NAND3	2-62	2
NAND3A	2-62	2
NAND3B	2-62	2
NAND3C	2-62	2
NAND4	2-63	3
NAND4A	2-63	3
NAND4B	2-63	3
NAND4C	2-63	3
NAND4D	2-63	3
NOR2	2-62	1
NOR2A	2-62	1
NOR2B	2-62	1
NOR3	2-62	2
NOR3A	2-62	2
NOR3B	2-62	2
NOR3C	2-62	2
NOR4	2-63	3
NOR4A	2-63	3
NOR4B	2-63	3
NOR4C	2-63	3
NOR4D	2-63	3
OA1	2-64	9
OA1A	2-64	9
OA1B	2-64	9
OA1C	2-64	9
OA2	2-64	9
OA2A	2-64	9
OA3	2-64	9
OA3A	2-64	9
OA3B	2-64	9
OA4A	2-64	9
OA5	2-64	9
OAI1	2-64	9
OAI2A	2-64	9
OAI3	2-64	9
OAI3A	2-64	9
OR2	2-62	1
OR2A	2-62	1
OR2B	2-62	1
OR3	2-62	2
OR3A	2-62	2
OR3B	2-62	2
OR3C	2-62	2
OR4	2-63	3
OR4A	2-63	3
OR4B	2-63	3
OR4C	2-63	3
OR4D	2-63	3
OUTBUF	2-65	11
REGE8A	2-71	51
REGE8B	2-71	51
SMULT8	2-73	67
SREG4A	2-73	63
SREG8A	2-73	63
TA138	2-73	61
TA139	2-72	60
TA151	2-65	18
TA153	2-66	19
TA157	2-66	20
TA161	2-72	57
TA164	2-73	64
TA169	2-72	57
TA194	2-73	65
TA195	2-73	66
TA269	2-72	58
TA273	2-71	52
TA280	2-72	55
TA377	2-71	52
TRIBUFF	2-65	11
UDCNT4A	2-72	59
XO1	2-63	5
XO1A	2-63	5
XA1	2-63	6
XA1A	2-63	6
XNOR	2-63	4
XOR	2-63	4

Table 1. 2-Input Gates

	A	B	Y
AND2	1	1	0
AND2A	1	1	0
AND2B	1	1	0
NAND2	1	1	0
NAND2A	1	1	0
NAND2B	1	1	0
OR2	1	1	0
OR2A	1	1	0
OR2B	1	1	0
NOR2	1	1	0
NOR2A	1	1	0
NOR2B	1	1	0

Table 2. 3-Input Gates

	A	B	C	Y
AND3	1	1	1	0
AND3A	1	1	1	0
AND3B	1	1	1	0
AND3C	1	1	1	0
NAND3	1	1	1	0
NAND3A	1	1	1	0
NAND3B	1	1	1	0
NAND3C	1	1	1	0
OR3	1	1	1	0
OR3A	1	1	1	0
OR3B	1	1	1	0
OR3C	1	1	1	0
NOR3	1	1	1	0
NOR3A	1	1	1	0
NOR3B	1	1	1	0
NOR3C	1	1	1	0

Table 3. 4-Input Gates

	A	B	C	D	Y
AND4	1	1	1	1	0
AND4A	1	1	1	1	0
AND4B	1	1	1	1	0
AND4C	1	1	1	1	0
AND4D	1	1	1	1	0
NAND4	1	1	1	1	0
NAND4A	1	1	1	1	0
NAND4B	1	1	1	1	0
NAND4C	1	1	1	1	0
NAND4D	1	1	1	1	0
OR4	1	1	1	1	0
OR4A	1	1	1	1	0
OR4B	1	1	1	1	0
OR4C	1	1	1	1	0
OR4D	1	1	1	1	0
NOR4	1	1	1	1	0
NOR4A	1	1	1	1	0
NOR4B	1	1	1	1	0
NOR4C	1	1	1	1	0
NOR4D	1	1	1	1	0

Table 4. XNOR/XOR Gates

	A	B	Y
XNOR	1	1	0
XOR	1	1	0

Table 5. XOR-OR/XNOR-OR Gates

	A	B	C	Y
XO1	1	1	2	0
XO1A	1	1	2	0

Table 6. XOR-AND/XNOR-AND Gates

	A	B	C	Y
XA1	1	1	2	0
XA1A	1	1	2	0

Table 7. AND-XOR/AND-XNOR Gates

	A	B	C	Y
AX1	2	2	1	0
AX1A	2	2	1	0
AX1B	1	1	1	0

Table 8. AND-OR/AND-NOR Gates

	A	B	C	D	Y
AO1	1	1	1	NA	0
AO1A	1	1	2	NA	0
AO1B	1	1	1	NA	0
AO1C	1	1	1	NA	0
AO2	1	1	1	1	0
AO2A	1	1	2	2	0
AO3	1	1	1	2	0
AO4A	1	1	1	1	0
AO5A	1	1	1	1	0
AOI1	1	1	1	NA	0
AOI1A	1	1	1	NA	0
AOI1B	1	1	2	NA	0
AOI2A	1	1	1	1	0
AOI2B	1	1	2	2	0
AOI3A	2	1	1	1	0
AOI4	1	1	1	1	0
MAJ3	2	2	2	NA	0

Table 9. OR-AND/OR-NAND Gates

	A	B	C	D	Y
OA1	1	1	1	NA	0
OA1A	1	1	2	NA	0
OA1B	1	1	1	NA	0
OA1C	1	1	1	NA	0
OA3	1	1	1	1	0
OA3A	1	1	1	2	0
OA3B	1	1	2	2	0
OA2	1	1	1	1	0
OA2A	1	1	1	1	0
OA4A	1	1	1	2	0
OA5	2	1	1	1	0
OAI1	1	1	1	NA	0
OAI2A	1	1	1	2	0
OAI3	1	1	1	1	0
OAI3A	1	1	2	2	0

Table 10. Buffers

	A	Y2
BUF	1	0
BUFA	1	0
INV	1	0
INVA	1	0

Table 11. I/O Buffers

	D	E	Y
INBUF	NA	NA	0
CLKBUF	NA	NA	0
OUTBUF	1	NA	0
TRIBUFF	1	1	0
BIBUF	1	1	0
CLKBIBUF	1	1	0

Table 12. 2:1 Multiplexers

	A	B	S	Y
MX2	1	1	1	0
MX2A	1	1	2	0
MX2B	1	1	1	0
MX2C	1	1	2	0

Table 13. 4:1 Multiplexer

	D0	D1	D2	D3	S1	S0	Y
MX4	1	1	1	1	1	1	0

Table 14. 4:1 Multiplexer

	D0	D1	D2	D3	S0A	S0B	S1	Y
MXT	1	1	1	1	1	1	1	0

Table 15. Other Multiplexer

	S	A	B	C	D	Y
MXC1	1	1	1	2	2	0

Table 16. 8:1 Multiplexer

	S2	S1	S0	D0–D7	Y
MX8	1	2	2	1	0
MX8A	2	2	2	1	0

Table 17. 16:1 Multiplexer

	S3	S2	S1	S0	D0–D15	Y
MX16	1	1	4	4	1	0

Table 18. 8:1 Multiplexer

	A	B	C	EN	D0–D7	Y	W
TA151	2	2	1	2	1	0	0

Table 19. 4:1 Multiplexer

	A	B	EN	C0	C1	C2	C3	Y
TA153	1	1	1	1	1	1	1	0

Table 20. 2:1 Multiplexer

	A	B	S	EN	Y
TA157	1	1	1	1	0

Table 21. Half Adders

	A	B	CO	S
HA1	2	2	0	0
HA1A	2	2	0	0
HA1B	2	2	0	0
HA1C	2	2	0	0

Table 22. Full Adders

	A	B	CI	CO	S
FA1	2	4	5	0	0
FA1A	3	3	3	2	0
FA1B	2	3	3	2	0

Table 23. Full Adder

	A0	A1	B	CI	CO	S
FA2A	2	2	3	3	2	0

Table 24. 8-Bit Fast Adder

	A0, A1	A2–A7	B0, B1	B2–B7	CI	S0–S7	CO
FADD8	2	4	3	6	3	0	0

Table 25. 12-Bit Fast Adder

	A0, A1	A2–A11	B0, B1	B2–B11	CI	S0–S11	CO
FADD12	2	4	3	6	3	0	0

Table 26. 16-Bit Fast Adder

	A0, A1	A2–A15	B0, B1	B2–B15	CI	S0–S15	CO
FADD16	2	4	3	6	3	0	0

Table 27. 24-Bit Fast Adder

	A0, A1	A2–A23	B0, B1	B2–B23	CI	S0–S23	CO
FADD24	2	4	3	6	3	0	0

Table 28. 32-Bit Fast Adder

	A0, A1	A2–A31	B0, B1	B2–B31	CI	S0–S31	CO
FADD32	2	4	3	6	3	0	0

Table 29. D-Type Latches

	D	G	Q/QN
DL1	1	1	1
DL1A	1	1	1
DL1B	1	1	1
DL1C	1	1	1

Table 30. D-Type Latches with Clear

	D	G	CLR	Q
DLC	1	1	1	1
DLCA	1	1	1	1
DLC1	1	1	1	1
DLC1A	1	1	1	1
DLC1F	1	1	2	1
DLC1G	1	1	2	1

Table 31. D-Type Latch with Clear

	G	CLR	D0–D7	Q0–Q7
DLC8A	8	8	1	1

Table 32. D-Type Latches with Preset

	D	G	PRE	Q
DLP1	1	1	2	1
DLP1A	1	1	2	1
DLP1B	1	1	1	1
DLP1C	1	1	1	1
DLP1D	1	1	2	1
DLP1E	1	1	2	1

Table 33. D-Type Latches with Clear and Preset

	D	G	PRE	CLR	Q/QN
DL2A	1	1	2	2	1
DL2B	1	1	2	2	1
DL2C	1	1	2	2	1
DL2D	1	1	2	2	1

Table 34. D-Type Latches with Enable

	D	E	G	Q
DLE	1	1	1	2
DLEA	1	1	1	2
DLEB	1	1	1	2
DLEC	1	1	1	2
DLE1D	1	1	1	1

Table 35. D-Type Latches with Enable, Clear, and Preset

	D	E	G	PRE	CLR	Q
DLE2A	1	1	1	NA	2	2
DLE2B	1	1	1	NA	1	1
DLE2C	1	1	1	NA	1	1
DLE3A	1	1	1	2	NA	2
DLE3B	1	1	1	1	NA	1
DLE3C	1	1	1	1	NA	1

Table 36. D-Type Latch with Enable

	G	E	D0–D7	Q0–Q7
DLE8	8	8	1	2

Table 37. D-Type Latches with Multiplexed Inputs

	A	B	S	E	G	Q	CLR
DLM	1	1	1	NA	1	1	NA
DLM2A	1	1	1	NA	1	1	2
DLMA	1	1	1	NA	1	1	NA
DLME1A	1	1	1	1	1	1	NA

Table 38. D-Type Latch with Multiplexed Inputs

	G	S	A0–A7	B0–B7	Q0–Q7
DLM8	8	8	1	1	1

Table 39. D-Type Flip-Flops

	D	CLK	Q/QN
DF1	1	2	1
DF1A	1	2	1
DF1B	1	2	1
DF1C	1	2	1

Table 40. D-Type Flip-Flops with Clear

	D	CLK	CLR	Q/QN
DFC1	1	2	2	1
DFC1A	1	2	2	1
DFC1B	1	2	2	1
DFC1C	1	2	3	1
DFC1D	1	2	2	1
DFC1E	1	2	2	1
DFC1F	1	2	3	1
DFC1G	1	2	2	1

Table 41. D-Type Flip-Flops with Preset

	D	CLK	PRE	Q/QN
DFP1	1	2	3	1
DFP1A	1	2	3	1
DFP1B	1	2	2	1
DFP1C	1	2	2	1
DFP1D	1	2	2	1
DFP1E	1	2	2	1
DFP1F	1	2	2	1
DFP1G	1	2	2	1

Table 42. D-Type Flip-Flops with Preset and Clear

	D	CLR	PRE	CLK	Q
DFPC	1	3	3	2	1
DFPCA	1	3	3	2	1

Table 43. D-Type Flip-Flops with Enable

	D	E	CLK	Q
DFE	1	1	2	2
DFEA	1	1	2	2
DFE1B	1	1	2	2
DFE1C	1	1	2	2

Table 44. D-Type Flip-Flops with Enable, Preset, and Clear

	D	E	CLR	PRE	CLK	Q
DFEB	1	1	3	3	2	2
DFEC	1	1	3	3	2	2
DFED	1	1	3	3	2	2
DFE2D	1	1	3	3	2	2
DFE3A	1	1	2	NA	2	2
DFE3B	1	1	2	NA	2	2
DFE3C	1	1	2	NA	2	2
DFE3D	1	1	2	NA	2	2
DFE4	1	1	NA	3	2	2
DFE4A	1	1	NA	3	2	2
DFE4B	1	1	NA	3	2	2
DFE4C	1	1	NA	3	2	2

Table 45. J-K Flip-Flops

	J	K	PRE	CLR	CLK	Q
JKF	1	1	NA	NA	2	2
JKFPC	1	1	3	3	2	2
JKF1B	1	1	NA	NA	2	2
JKF2A	1	1	NA	2	2	2
JKF2B	1	1	NA	2	2	2
JKF2C	1	1	NA	2	2	2
JKF2D	1	1	NA	2	2	2
JKF3A	1	1	2	NA	2	2
JKF3B	1	1	2	NA	2	2
JKF3C	1	1	3	NA	2	2
JKF3D	1	1	3	NA	2	2
JKF4B	1	1	3	3	2	2

Table 46. Multiplexed-Input Flip-Flops

	A	B	S	CLR	E	CLK	Q
DFM	1	1	1	NA	NA	2	1
DFMA	1	1	1	NA	NA	2	1
DFMB	1	1	1	2	NA	2	1
DFME1A	1	1	1	NA	2	2	2
DFM1B	1	1	1	NA	NA	2	1
DFM1C	1	1	1	NA	NA	2	1
DFM3	1	1	1	2	NA	2	1
DFM3B	1	1	1	2	NA	2	1
DFM3E	1	1	1	2	NA	2	1
DFM3F	1	1	1	3	NA	2	1
DFM3G	1	1	1	3	NA	2	1

Table 47. Multiplexed-Input Flip-Flops with Preset

	A	B	S	PRE	CLK	Q
DFM4	1	1	1	3	2	1
DFM4A	1	1	1	2	2	1
DFM4B	1	1	1	2	2	1
DFM4C	1	1	1	3	2	1
DFM4D	1	1	1	3	2	1
DFM4E	1	1	1	3	2	1

Table 48. Multiplexed-Input Flip-Flops with Preset and Clear

	A	B	S	CLR	PRE	CLK	Q
DFM5A	1	1	1	3	3	3	1
DFM5B	1	1	1	3	3	2	1

Table 49. Clock Buffer (CLKBUF) Interface

	A	G	Y
GAND2	1	1	0
GNAND2	1	1	0
GOR2	1	1	0
GNOR2	1	1	0
GXOR2	1	1	0

Table 50. Clock Buffer (CLKBUF) Interface

	D0	D1	D2	D3	G	S0	Y
GMX4	1	1	1	1	1	1	0

Table 51. Octal D-Type Flip-Flops and Registers

	CLK	CLR	D0–D7	Q0–Q7	PRE	E
REGE8A	16	2	1	2	2	8
REGE8B	16	2	1	2	2	8

Table 52. Octal D-Type Flip-Flops and Registers

	CLK	CLR	EN	D1–D8	Q1–Q8
TA273	16	2	NA	1	1
TA377	16	NA	8	1	2

Table 53. Identity Comparators

	An	Bn	AEB
ICMP4	1	1	0
ICMP8	1	1	0

Table 54. Magnitude Comparators

	An	Bn	ALBI	AEBI	AGBI	ALB	AEB	AGB
MCMP16	3	3	NA	NA	NA	0	0	0
MCMPC2	3	3	1	1	1	0	0	0
MCMPC4	3	3	1	1	1	0	0	0
MCMPC8	3	3	1	1	1	0	0	0

Table 55. Parity Checker

	A	B	C	D	E	F	G	H	I	ODD	EVEN
TA280	1	1	1	1	1	1	1	1	1	0	0

Table 56. Binary Counters

	CLR	CLK	LD	CI	P0–P3	Q0	Q1	Q2	Q3	CO
CNT4A	8	8	4	8	1	6	5	4	3	0
CNT4B	8	8	4	9	1	6	4	3	3	0

Table 57. Synchronous Counters

	LD	UD	ENT	ENP	CLR	CLK	A	B	C	D	QA	QB	QC	QD	RCO
TA161	1	NA	2	1	1	8	1	1	1	1	6	5	4	3	0
TA169	4	5	3	3	NA	8	1	1	1	1	7	6	4	4	0

Table 58. Synchronous Counter

	CLK	LD	UD	ENP	ENT	A–H	QA, QE	QB, QF	QC, QD, QG, QH	RCO
TA269	16	8	1	3	3	1	7	6	4	0

Table 59. Synchronous Counter

	LD	UD	CI	CLK	P0–P3	Q0	Q1	Q2	Q3	CO
UDCNT4A	4	5	9	8	1	7	6	4	4	0

Table 60. 2-to-4 Decoders

	A	B	E/EN	Y0–Y3
DEC2X4	4	4	NA	0
DEC2X4A	4	4	NA	0
DECE2X4	4	4	4	0
DECE2X4A	4	4	4	0
TA139	4	4	4	0

Table 61. 3-to-8 Decoders

	A	B	C	E	G1	G2A	G2B	Y0–77
DEC3X8	8	8	8	NA	NA	NA	NA	0
DEC3X8A	8	8	8	NA	NA	NA	NA	0
DECE3X8	5	5	5	8	NA	NA	NA	0
DECE3X8A	5	5	5	8	NA	NA	NA	0
TA138	5	5	5	NA	1	1	1	0

Table 62. 4-to-16 Decoder

	A	B	C	D	Y0–Y15
DEC4X16A	9	9	9	9	0

Table 63. Shift Registers

	CLR	CLK	SHLD	SI	Pn	SO
SREG4A	8	8	4	1	1	1
SREG8A	2	16	8	1	1	1

Table 64. Shift Register

	CLK	CLR	A	B	QA	QB	QC	QD	QE	QF	QG	QH
TA164	16	2	1	1	2	2	2	2	2	2	2	1

Table 65. Shift Register

	CLK	CLR	S1	S0	SLSI	SRSI	A	B	C	D	QA	QB	QC	QD
TA194	8	8	1	1	1	1	1	1	1	1	3	4	4	3

Table 66. Shift Register

	CLK	CLR	J	K	SHLD	A	B	C	D	QA	QB	QC	QD	QDN
TA195	8	8	1	1	4	1	1	1	1	4	2	2	2	0

Table 67. 8-Bit Multiplier

	A0–A2, A4–A6	A3	A7	B0, B4	B1–B3, B5–B7	P0–P15
SMULT8	6	9	14	8	4	0

Table 68. Logic Module

	A0, A1	B0, B1	SA, SB	S0, S1	Y
CM8A	1	1	1	1	0

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- Three Arrays With Increased Densities
- Up to 8000 Equivalent Gate Array Gates
- Supported by TI Action Logic™ System (TI-ALS) Software
- Desktop Programmable
- Reliable, Nonvolatile Antifuse Interconnect
- Design Library With Over 250 Macros
- User-Programmable I/O Pins
- Enhanced Architecture
  - Supports Single-Module Sequential Functions
  - Supports Wide-Input Combinatorial Functions
- Two In-Circuit Diagnostic Probe Pins Support 50-MHz Analysis
- Low-Power CMOS Technology
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA

description

The TPC12 Series is the next generation of field programmable gate arrays from TI. Based on channeled array architecture, the TPC12 Series provides significant enhancements to gate density and performance while maintaining upward compatibility from TPC10 series designs. The devices are implemented in silicon gate, two-level metal CMOS, and they employ antifuse technology. The unique architecture offers gate array flexibility, high performance and instant turnaround through user programming. Designs of up to 8000 gates can be implemented with the TPC1280 device. The TPC12 Series is supported by the Action Logic System (ALS). ALS is available on Sun™, HP/Apollo™, and 386/486 PC platforms, with CAE interfaces to Cadence™/Valid™, View*logic*™, Mentor Graphics™, and OrCAD™.

Product Family Profile

DEVICE	TPC1280	TPC1240	TPC1225A
Capacity			
Gate array equivalent gates	8000	4000	2500
TTL equivalent packages	210	105	70
CMOS Process	1.2 µm	1.2 µm	1.0 µm
Logic Modules	1232	684	451
Flip-Flops (maximum)	998	565	382
Antifuses	750,000	400,000	250,000

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HP/Apollo is a trademark of HP/Apollo Computer, Inc.
Mentor is a trademark of Mentor Graphics Corporation.
Sun is a trademark of Sun Microsystems, Inc.
OrCAD/SDT III is a trademark of OrCad Systems Corporation.
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enhanced architecture

Routing efficiency with large gate counts is accomplished with increased routing resources, increased antifuse programming elements, and architectural enhancements. Horizontal routing tracks per channel increase to 36 (vs 25 for TPC10); vertical routing tracks per column increase to 15 (vs 13 for TPC10). All speed-critical module-to-module connections are accomplished with only two low-resistance antifuse elements. Most connections are implemented with either two or three antifuse elements (as shown in Figure 1). No connections are allowed with more than four antifuse elements in the path. The result is predictable performance with fully automatic placement and routing. Device utilization is typically 85% to 95% of available logic modules and 80% of gates.

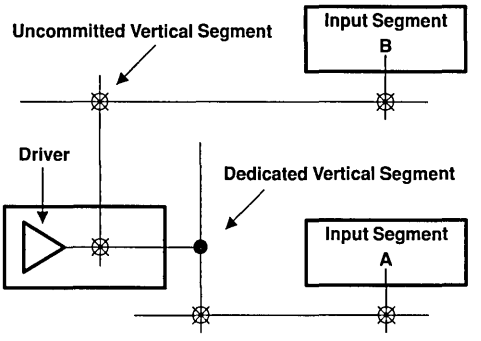


Figure 1. TPC12 Enhanced Routing Architecture

two module design: C modules and S modules

The TPC12 Series offers dedicated combinatorial and combinatorial-sequential modules. The combinatorial module, C Module, has been enhanced to implement high fan-in combinatorial macros, such as 5-input AND, OR, NAND and NOR gates. Additionally, AND-OR gates, XOR gates, AND-XOR gates, and many other combinatorial functions are available.

The combinatorial-sequential module, S Module, has been optimized to implement high-speed flip-flops within a single module. Furthermore, S Modules also include combinatorial logic within the S Module allowing an additional level of logic to be implemented with no additional propagation delay.

hard and soft macros

Designing with TI FPGAs is accomplished through a building-block approach. Over 250 schematic representations of widely used logic functions are stored within the macro library. Each macro represents one of the basic to complex building blocks from which you may build your design. These macros range from simple logic functions such as AND gates to more complex logic functions, such as 16-bit counters and accumulators.

The macros are implemented within the FPGA architecture by utilizing one or more C Modules and/or S Modules. Over 150 of these macros are implemented within single modules, and an additional 25 macros are implemented by connecting only two modules. One-module and two-module macros have a small propagation delay variance providing accurate performance prediction capabilities. These are called hard macros and their propagation delays are specified within the data sheet.

More complex logic functions are also included in the macro library. These soft macros are implemented by using several hard macros. The propagation delays of soft macros are not specified within the data sheet.

programmable I/O pins

Each I/O pin can be configured as an input, output, 3-state, or bidirectional buffer. Inputs are TTL- and CMOS-compatible. Output drive levels meet 10-mA TTL and 6-mA HCT standards.

Optional transparent latches at the I/O pins are provided for both inputs and outputs. I/O latches can be combined with latches in the array to implement master-slave flip-flops as depicted in Figure 2. A selection of registered I/O macros are included in the macro library.

clock distribution network

Two low-skew distribution networks are provided. Each network can be driven by either of two dedicated I/O pins or from internal logic.

enhanced programming and test

The TPC12 Series provides the same type of specifications as the TPC10 Series. All routing tracks, logic modules, program, debug, and test circuits are fully tested prior to customer shipment. Verification of correct antifuse programming is performed automatically with Activator™ 2 programming and debug hardware. The TPC12 Series architecture implements an enhanced programming and test algorithm.

probe pins

TPC12 Series devices have two independent diagnostic probe pins, PRA and PRB. These pins allow the user to observe any internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actionprobe™ diagnostic tools. The probe pins can be used as user-defined I/Os when debugging has been completed.

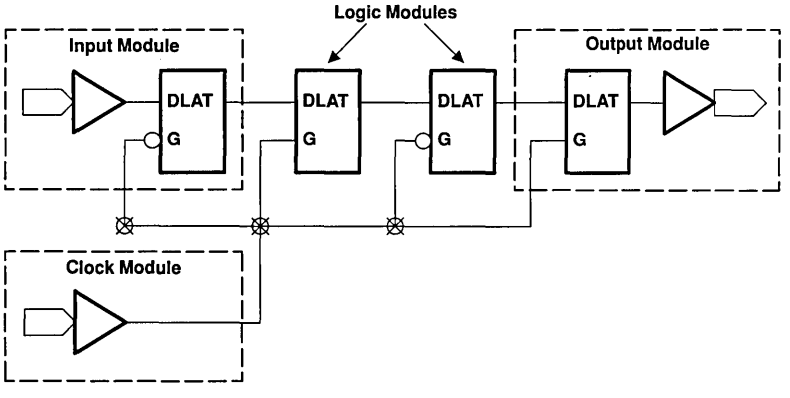


Figure 2. Latched User I/Os

TERMINAL FUNCTIONS

PIN NAME	I/O	DESCRIPTION
CLKA	I	Clock A. TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
CLKB	I	Clock B. TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
DCLK	I	Diagnostic clock. TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
GND	I	Ground. Input low supply voltage.
I/O	I/O	Input/output. I/O pins function as an input, output, 3-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically set low by the ALS software.
MODE	I	Mode. The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI, SDO). When the MODE pin is high, the special functions are active. When the MODE pin is low, the pins function as I/Os.
NC		No connection. This pin is not connected to circuitry within the device.
PRA	O	Probe A. The probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe B pin to allow real-time diagnostic output of any signal path within the device. The probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
PRB	O	Probe B. The probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe A pin to allow real-time diagnostic output of any signal path within the device. The probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDI	I	Serial data input. Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDO	O	Serial data output for diagnostic probe. SDO is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
V_{CC}	I	Supply voltage. Input high supply voltage.
V_{KS}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to GND during normal operation.
V_{PP}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.
V_{SV}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} (see Notes 1, 2, and 3) ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 to V_{CC} + 0.5 V
Output voltage range, V_O ..... – 0.5 to V_{CC} + 0.5 V
Input clamp current‡ , I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current§, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current§, (V_O = 0 to V_{CC}) ..... ± 25 mA
Operating free-air temperature range, T_A: Commercial ..... 0°C to 70°C
Industrial ..... – 40°C to 85°C
Operating case temperature range, T_C: Military ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Applies for input and bidirectional buffers
§ Applies for bidirectional and output buffers
NOTES: 1. $V_{PP} = V_{CC}$ except during device programming
2. $V_{SV} = V_{CC}$ except during device programming
3. V_{KS} = GND except during device programming

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
		Military	4.5	5	5.5	
V_{PP}	Program pin voltage (while not programming)		V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage		2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
T_A	Operating free-air temperature	Commercial	0		70	°C
		Industrial	−40		85	
T_C	Operating case temperature	Military	−55		125	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	COMMERCIAL			INDUSTRIAL			MILITARY			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (see Note 4)	I_{OH} = −10 mA	2.4									V
		I_{OH} = −6 mA	3.84									
		I_{OH} = −4 mA				3.7			3.7			
V_{OL}	Low-level output voltage (see Note 4)	I_{OL} = 10 mA			0.5							V
		I_{OL} = 6 mA			0.33			0.4			0.4	
I_I	Input current	$V_I = V_{CC}$ or 0			±10			±10			±10	µA
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±10			±10	µA
I_{CC}	Standby supply current (see Note 5)				10			20			25	mA
C_{io}	I/O capacitance (see Notes 6 and 7)			7			7			7		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Only one output tested at a time. V_{CC} = minimum value in recommended operating conditions.
5. All outputs unloaded. All inputs = V_{CC} or GND.
6. Not tested, for information only
7. Includes worst-case 176 CPGA package capacitance. V_O = 0, f = 1 MHz

timing characteristics

Timing characteristics for TPC12 Series arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all TPC12 Series devices. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS timer utility or performing simulation with post-layout delays. The macro propagation delays in the switching characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on 90% module utilization.

critical and typical nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to 6% of the nets in a design may be designated critical.

fan-out dependency

Propagation delays are dependent on the fan-out (number of loads) driven by a macro. Delay increases with increasing fan-out due to capacitive loading of the macro inputs and the resistance and capacitance of the interconnect.

long tracks

Some nets in the design will utilize long tracks. Long tracks are special routing resources that span multiple rows or columns of modules. Long tracks are most frequently used in large fan-out (> 10) situations. Long tracks will utilize three and sometimes four antifuse connections. The increased capacitance and resistance will result in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device will require long tracks. Long tracks add an additional 10-ns to 15-ns delay.

slow input transition (rise and fall) times

Slow signal transition is a condition that commonly occurs even in today's high-performance systems. A typical example is the signal degradation encountered with signals coming off of a highly capacitive bus. These slow signal transitions can cause undesirable results when traveling through the threshold region of a CMOS input. Texas Instruments recommends that input signal transitions be limited to 500 ns or less to ensure device integrity.

timing derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for TPC12 array typical timing specifications. The derating factors as shown in table are based on the recommended operating conditions for TPC12 applications. The derating curves in Figure 3 and Figure 4 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curves are based on device junction temperature. Actual junction temperature is determined from ambient temperature, power dissipation, and package thermal characteristics.

Table 1. Timing Derating Factor (x typical) (see Note 8)

C SUFFIX		I SUFFIX		M SUFFIX	
BEST CASE	WORST CASE	BEST CASE	WORST CASE	BEST CASE	WORST CASE
0.40	1.40	0.37	1.50	0.35	1.60

NOTE 8: Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

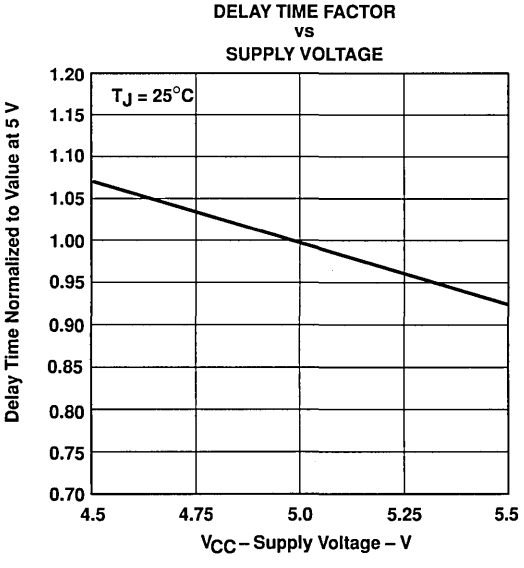


Figure 3

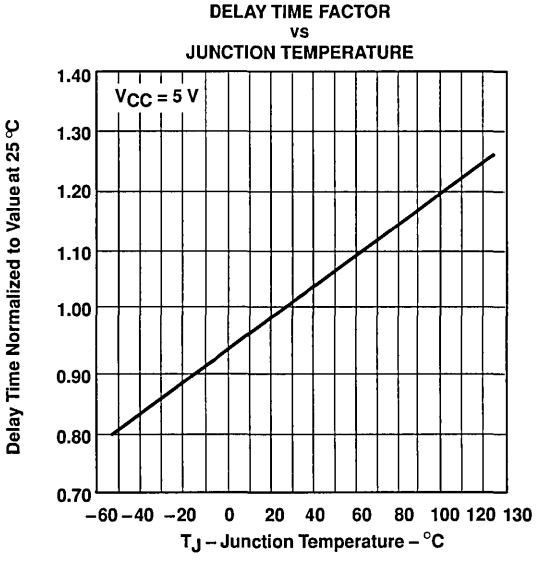


Figure 4

TPC1225A timing requirements over recommended operating conditions, no further derating required (see Note 9)

			COMMERCIAL		INDUSTRIAL		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		75		66	MHz
t_{cp}	Clock period	Flip-flop	13		13		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		ns
		Flip-flop PRE or CLR	4		4.5		
		Latch G	4		4.5		
		Latch PRE or CLR	4		4.5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		
		Flip-flop E before CLK	1		1.5		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		
		Latch PRE or CLR (inactive) before G	1		1.5		
		Latch E before G	1		1.5		
		Input buffer latch pad input	−2.5		−3		
		Output buffer latch D before G	0.4		0.5		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		ns
		Flip-flop E after CLK	0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		
		Latch E after G	0		0		
		Input buffer latch pad input after G	2		2.5		
		Output buffer latch D after G	0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1225A switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1225A switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	9.3	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	9.4	ns
t_{wH}min	Pulse duration, high, minimum	4.5	5.1	5.5	ns
t_{wL}min	Pulse duration, low, minimum	4.5	5.1	5.5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	9.1	9.5	10	ns
f_{max}	Maximum clock frequency	110	105	100	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1225A-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		85		75	MHz
t_{cp}	Clock period	Flip-flop	11.7		13.3		ns
	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		ns
		Flip-flop PRE or CLR	4		4.5		
		Latch G	4		4.5		
		Latch PRE or CLR	4		4.5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		
		Flip-flop E before CLK	1		1.5		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		
		Latch PRE or CLR (inactive) before G	1		1.5		
		Latch E before G	1		1.5		
		Input buffer latch pad input	−2.5		−3		
		Output buffer latch D before G	0.4		0.5		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0		0		ns
		Flip-flop E after CLK	0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		
		Latch E after G	0		0		
		Input buffer latch pad input after G	2		2.5		
		Output buffer latch D after G	0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1225A-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	Single module	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.4	7.8	8.1	9.3	12	ns
t_{pd}	CLK to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	CLK to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	G to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	G to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	PRE or CLR to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.4	4.8	5.1	6.3	9	ns

NOTE 10: FO means fan out.

TPC1225A-1 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	
t_{PLH}	G	Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7	7.8	8.6	ns
t_{PHL}	Propagation delay time, high-to-low output	7	7.8	8.6	ns
t_{wH}min	Pulse duration, high, minimum	4.2	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4.2	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7.0	8	11.2	ns
t_C	Minimum cycle time	9.3	8.7	9.1	ns
f_{max}	Maximum clock frequency	120	115	110	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1240 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		66		55		50	MHz
t_{cp}	Clock period	Flip-flop	15		18		20		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1240 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1240 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	9.1	10.1	11.2	ns
t_{PHL}	Propagation delay time, high-to-low output	9.1	10.2	11.3	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	11.1	11.5	11.8	ns
f_{max}	Maximum clook frequency	90	87	85	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

TPC1240-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		75		66		55	MHz
t_{cp}	Clock period	Flip-flop	13		15		18		ns
	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1240-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	Single module	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.4	7.8	8.1	9.3	12	ns
t_{pd}	CLK to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	CLK to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	G to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	G to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	PRE or CLR to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.4	4.8	5.1	6.3	9	ns

NOTE 10: FO means fan out.

TPC1240-1 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	
t_{PLH}	G	Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	9.3	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	9.4	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	9.1	9.5	10	ns
f_{max}	Maximum clock frequency	110	105	100	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1280 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		48		43		39	MHz
t_{cp}	Clock period	Flip-flop	18		20		22		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1280 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	Single module	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	8.7	9.2	9.7	11.2	14.7	ns
t_{pd}	CLK to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	CLK to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	G to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	G to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	PRE or CLR to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	PRE or CLR to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns

NOTE 10: FO means fan out.

TPC1280 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.7	7.2	7.7	8.2	11.7	ns
t_{PHL}			6.6	7.1	7.6	8.1	11.5	
t_{PLH}	G	Q	6.6	7.2	7.7	8.2	11.7	ns
t_{PHL}			6.4	6.9	7.5	8	11.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	DESCRIPTION	FO = 32	FO = 128	FO = 384	UNIT
t_{PLH}	Propagation delay time, low-to-high output	9.1	10.1	12.3	ns
t_{PHL}	Propagation delay time, high-to-low output	9.1	10.2	12.5	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	13.3	14.3	15.3	ns
f_{max}	Maximum clock frequency	75	70	65	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

TPC1280-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		65		60		50	MHz
t_{cp}	Clock period	Flip-flop	15		18		20		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1280-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8.0	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1280-1 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

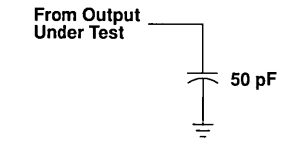
global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 384	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	10.4	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	10.6	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	11.4	12	13	ns
f_{max}	Maximum clook frequency	89	83	77	MHz

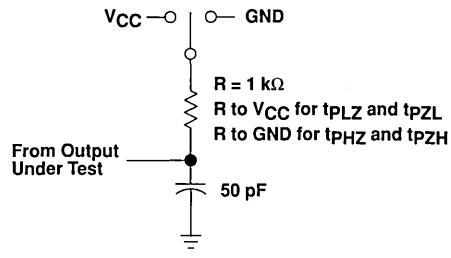
† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

PARAMETER MEASUREMENT INFORMATION

AC test loads



LOAD CIRCUIT 1
Used to measure propagation delay



LOAD CIRCUIT 2
Used to measure rising/falling edges

output buffer delays

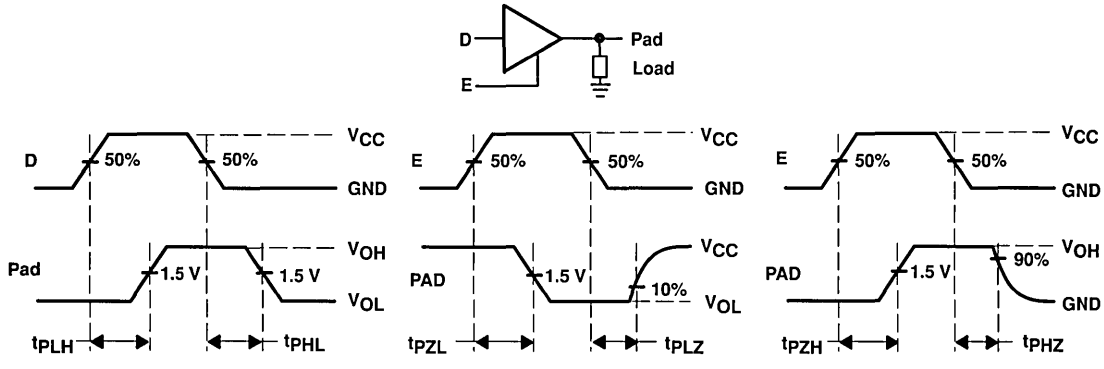
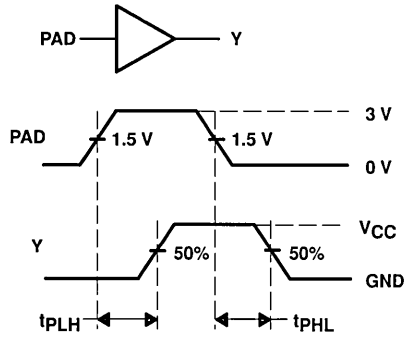


Figure 5. Symbols, Test Loads, and Waveforms

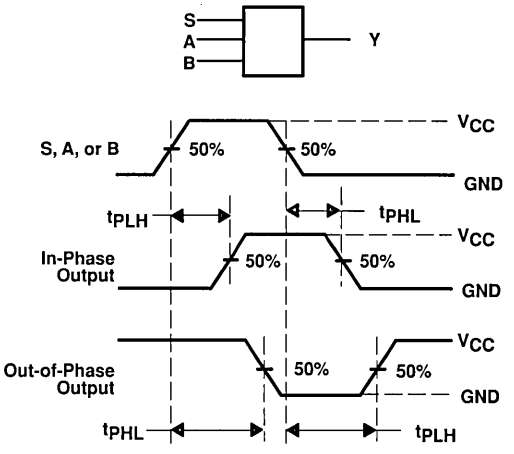
PARAMETER MEASUREMENT INFORMATION

input buffer delays

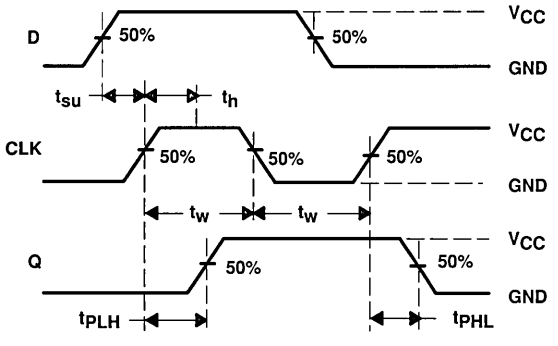


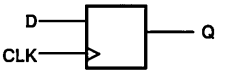
NOTE: Measurements made with $t_r = t_f = 3$ ns to pads only.

module delays



D-type flip-flop and clock delays





D FLIP-FLOP SHOWING POSITIVE-EDGE TRIGGERED CLOCK

Figure 5. Symbols, Test Loads, and Waveforms (continued)

power dissipation

To calculate power consumption, the total device power is broken into two components. These components are:

- Static or nonswitching power
- Active or switching power

$$P = \left[\left(I_{CC} + I_{active}\right) \times V_{CC}\right] + \left(I_{OL} \times V_{OL} \times N\right) + \left[I_{OH} \times \left(V_{CC} - V_{OH}\right) \times M\right]$$

Where:

I_{CC} = current flowing when no inputs or outputs are changing
I_{active} = current flowing due to CMOS switching
I_{OL}, I_{OH} = TTL sink/source currents
V_{OL}, V_{OH} = TTL level output voltages
N = number of outputs driving TTL loads to V_{OL}
M = number of outputs driving TTL loads to V_{OH}

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

static power

Static power dissipation is typically a small component of the overall power. From the values provided in the electrical specifications, the maximum static power (commercial) dissipation is:

$$\text{Static power} = 10\ \text{mA} \times 5.25\ \text{V} = 52.5\ \text{mW}$$

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

active power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

equivalent capacitance

The active power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Active power } (\mu W) = C_{EQ} \times V_{CC}{}^2 \times f \qquad (1)$$

Where:

C_{EQ} = equivalent capacitance in pF
V_{CC} = power supply voltage in volts
f = switching frequency in MHz

equivalent capacitance (continued)

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for TPC12 devices are:

	C_{EQ} (pF)
Modules	7.7
Input buffers	18.0
Output buffers	25.0
Clock buffer loads	2.5

To calculate the average active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic circuit. The exact equation is piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Active power} = \left[\left(n \times 7.7 \times f_1\right) + \left(m \times 18.0 \times f_2\right) + \left(p \times \left(25.0 + C_L\right) \times f_3\right) + \left(q \times 2.5 \times f\right)\right] \times V_{CC}{}^2 \qquad (2)$$

Where:

n = number of logic modules switching at frequency f_1
m = number of input buffers switching at frequency f_2
p = number of output buffers switching at frequency f_3
q = number of clock loads on the global clock network
f = frequency of global clock
f_1 = average logic module switching rate in MHz
f_2 = average input buffer switching rate in MHz
f_3 = average output buffer switching rate in MHz
C_L = output load capacitance

determining average switching frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module utilization = 80% of combinatorial modules
Average module frequency = f/10
1/3 of I/Os are inputs
Average input frequency = f/5
2/3 of I/Os are outputs
Average output frequency = f/10
Clock Net 1 loading = 40% of sequential modules
Clock Net 1 frequency = f
Clock Net 2 loading = 40% of sequential modules
Clock Net 2 frequency = f/2

estimated power

The results of estimating active power based on the preceeding rules are displayed in Figure 6. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

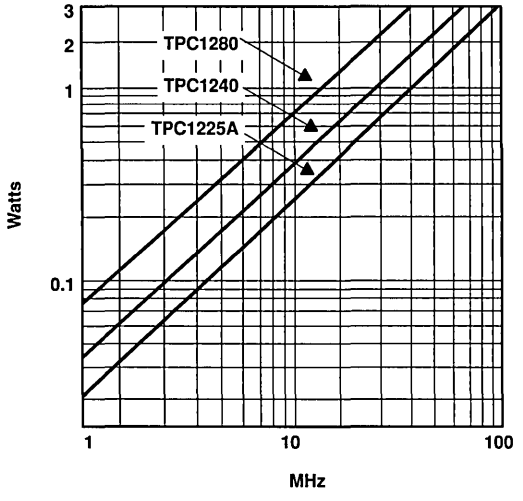


Figure 6. TPC12 Series Power Estimates

ESD rating

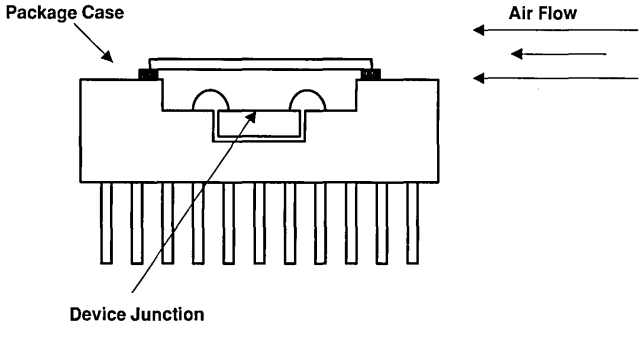
ESD characterization of Texas Instruments FPGAs is performed in accordance with MIL-STD 883C, Method 3015. This calls out the human body model which included discharging a 10-pF capacitor through a 1.5-kΩ resistor. Three positive and three negative pulses are discharged into each pin at each voltage level. After pulsing, the units are tested on a VLSI tester. Testing is performed for initial device qualification and product redesign only. All devices have been designed for ESD protection.

package thermal characteristics

The device junction to case thermal characteristic is $R_{\theta JC}$ and the junction to ambient air characteristic is $R_{\theta JA}$. The thermal characteristics for $R_{\theta JA}$ are shown with two different air-flow rates. Maximum junction temperature is 150°C. However, a maximum junction temperature of 140°C is recommended for continuous operation. A sample calculation of the maximum power dissipation for a CPGA 176-pin package at commercial temperature in still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{R_{\theta JA}\ (°C/W)} = \frac{150°C - 70°C}{20°C/W} = 4\ W$$

PACKAGE TYPE	PIN COUNT	$R_{\theta JC}$	$R_{\theta JA}$ STILL AIR	$R_{\theta JA}$ 300 FT/MIN	UNIT
Ceramic Pin Grid Array (CPGA)	133 160 176 / 177	5 7 2	30 35 20	15 28 8	°C/W
Plastic Quad Flat Package (PQFP)	100 144	10 7	60 35	38 28	°C/W
Plastic Leaded Chip Carrier (PLCC)	84	10	40	27	°C/W



TPC1225A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin PLCC	451	2500	72	P	P
100-pin PQFP			83	P	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
100-pin PQFP	451	2500	83	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1240 device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	R	P
144-pin PQFP			104	R	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	R	P
144-pin PQFP			104	P	P

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1280 device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
160-pin PQFP	1232	8000	140	P	P
176-pin CPGA				R	R
177-pin CPGA				R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
176-pin CPGA	1232	8000	140	R	R
177-pin CPGA				R	R

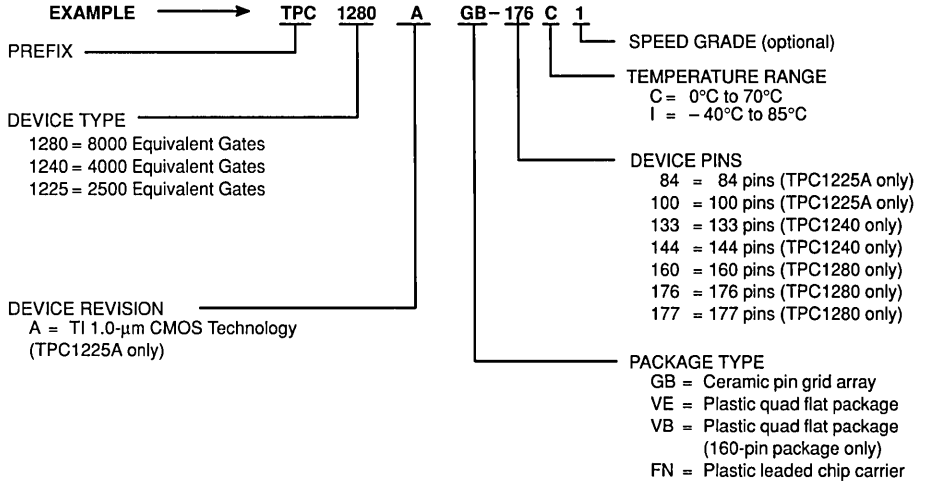
Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
172-pin CQFP	1232	8000	140	P	P
177-pin CPGA				R	P

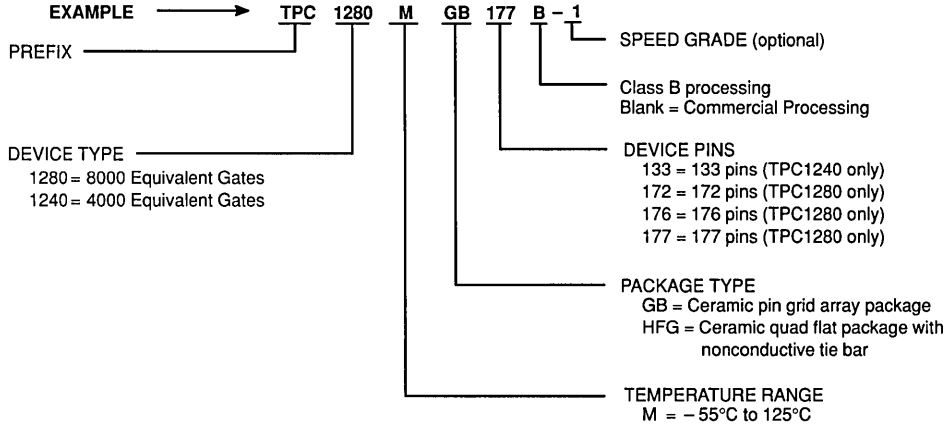
R = released
P = planned, consult your local TI sales representative for current availability.

ordering information

Various configurations of the TPC12 Series devices can be orderd using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



Military versions can be ordered as follows:



DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1240M	Class B	To be determined
TPC1280M	Class B	5962-9215601M

MACRO LIBRARY

overview

This section describes TPC12 Series macros, which are building blocks for designing with TI field programmable gate arrays (FPGAs) with the Texas Instruments Action Logic System (TI-ALS) and your Computer Aided Engineering (CAE) interface.

The macros are divided into five categories: I/O macros, combinable hard marcos, uncombinable hard macros, soft macros, and TTL macros.

equation statement elements

combinational elements

All equations for combinational logic elements use the following operators:

OPERATOR	SYMBOL
AND	See Note 11
NOT	!
OR	+
XOR	^

NOTES: 11. A space between the 'A' and 'B' in the equation Y = A B means A AND B.
12. Order of operators in decreasing precedence is: NOT, AND, XOR and OR,
13. Signals expressed in bold have a dual module delay.

sequential elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	optional inversion
CLK	flip-flop clock pin
G	latch gate pin
CLR	asynchronous clear pin
PRE	asynchronous preset pin

I/O hard macros

MACRO NAME	NO. OF MODULE(S)		DESCRIPTION
	I/O	CLOCK	
INBUF	1		Input
IBDL	1		Input with input latch
BBDLHS	1		Bidirectional with input latch and output latch
BBHS	1		Bidirectional
BIBUF	1		Bidirectional
CLKBIBUF	1	1	Bidirectional with input dedicated to clock network
CLKBUF	1	1	Input for dedicated clock network
OBDLHS	1		Output with output latch
OBHS	1		Output
OUTBUF	1		Output
TBDLHS	1		3-state output with latch
TBHS	1		3-state output
TRIBUFF	1		3-state output

I/O firm macros

MACRO NAME	I/O	DESCRIPTION
ORH	I	Output with register
ORIH	I	Inverted output with register
ORITH	I	3-state inverted output with register
ORTH	I	3-state output with register
IR	I	Input with register

combinable hard macros

DF1, DF1B, DFC1B, DFC1D, DL1, DL1B, DLC, and DLCA

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	2-input AND	AND2	Y = A B		1
		AND2A	Y = !A B		1
		AND2B	Y = !A !B		1
	3-input AND	AND3B	Y = !A !B C		1
AND-OR		AO1A	Y = ((!A) B) + C		1
		AO1D	Y = (!A !B) + C		1
AND-OR-Invert		AOI1D	Y = !((!A !B) + !C)		1
Buffers and Inverters		BUF	Y = A		1
		BUFA	Y = !(!A)		1
		INV	Y = !A		1
		INVA	Y = !A		1
Clock Net Interface		GAND2	Y = A G		1
		GNOR2	Y = !(A + G)		1
		GOR2	Y = A + G		1
Multiplexer	2:1 Multiplexers	MX2	Y = (A !S) + (B S)		1
NAND	2-input NAND	NAND2A	Y = !(!A B)		1
		NAND2B	Y = !(!A !B)		1
	3-input NAND	NAND3C	Y = !(!A !B !C)		1
NOR	2-input NOR	NOR2	Y = !(A + B)		1
		NOR2A	Y = !(!A +B)		1
		NOR2B	Y = !(!A + !B)		1
	3-input NOR	NOR3A	Y = !(!A + B + C)		1
OR-AND		OA1	Y = (A + B) C		1
OR	2-input OR	OR2	Y = A + B		1
		OR2A	Y = !A + B		1
	3-input OR	OR3	Y = A + B + C		1

combinable hard macros (continued)

DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	3-input	AND3	Y = A B C		1
		AND3A	Y = !A B C		1
		AND3C	Y = !A !B !C		1
	4-input	AND4B	Y = !A !B C D		1
		AND4C	Y = !A !B !C D		1
AND-OR		AO1	Y = (A B) + C		1
		AO11	Y = AB + ((A + B) C)		1
		AO1B	Y = (A B) + (!C)		1
		AO1C	Y = ((!A) B) + (!C)		1
		AO1E	Y = (!A!B) + !C		1
		AO2	Y = ((A B) + C + D)		1
		AO2A	Y = ((!A B) + C + D)		1
		AO2B	Y = (!A!B) + C + D		1
		AO2C	Y = (!AB) + !C + D		1
		AO2D	Y = (!A!B) + !C + D		1
		AO3	Y = (!A B C) + D		1
		AO3B	Y = (!A!BC) + D		1
		AO3C	Y = (!A!B!C) + D		1
		AO4A	Y = (!A B C) + (A C D)		1
		AO5A	Y = (!A B) + (A C) + D)		1
AND-OR-Invert		AOI1A	Y = !((!A B) + C)		1
		AOI1B	Y = !((A B) + !C)		1
		AOI1C	Y = !((!A !B) + C)		1
		AOI2A	Y = !((!A B) + C + D)		1
		AOI3A	Y = !((!A !B !C) + (!A !D))		1
Exclusive OR	AND-XOR	AX1B	Y = (!A !B) ^ C		1
Boolean		CS2	Y = !((A + S) B) C + ((A + S) B) D		1
		CY2B	Y = A1 B1 + (A0+B0) A1 + (A0+B0) B1		1
Clock Net Interface		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)		1
		GNAND2	Y = !(A G)		1
		GXOR2	Y = A ^ G		1
AND-OR		MAJ3	Y = (A B) + (B C) + (A C)		1
Multiplexer	2:1 Multiplexers	MX2A	Y = (!A !S) + (B S)		1
		MX2B	Y = (A !S) + (!B S)		1
		MX2C	Y = (!A !S) + (!B S)		1
	4:1 Multiplexers	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)		1

combinable hard macros (continued)

DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
NAND	2-input NAND	NAND2	Y = !(A B)		1
	3-input NAND	NAND3A	Y = !(!A B C)		1
		NAND3B	Y = !(!A !BC)		1
	4-input NAND	NAND4C	Y = !(!A !B C D)		1
		NAND4D	Y = !(!A !B !C !D)		1
NOR	3-input NOR	NOR3	Y = !(A + B + C)		1
		NOR3B	Y = !(!A + !B + C)		1
		NOR3C	Y = !(!A + !B + !C)		1
	4-input NOR	NOR4A	Y = !(!A + B + C + D)		1
		NOR4B	Y = !(!A + !B + C + D)		1
OR-AND		OA1A	Y = (!A + B) C		1
		OA1B	Y = (A + B) (!C)		1
		OA1C	Y = (!A + B) (!C)		1
		OA2	Y = (A + B) (C + D)		1
		OA2A	Y = (!A + B) (C + D)		1
		OA3	Y = ((A + B) C D)		1
		OA3A	Y = ((A + B) !C D)		1
		OA4	Y = (A + B + C) D		1
		OA4A	Y = ((A + B + !C) D)		1
		OA5	Y = (A + B + C) (A + D)		1
OR-AND-Invert		OAI1	Y = !((A + B) C)		1
		OAI2A	Y = !((A + B + C) !D)		1
		OAI3A	Y = !((A + B) !C !D)		1
OR	3-input OR	OR3A	Y = !A + B + C		1
		OR3B	Y = !A + !B + C		1
	4-input OR	OR4	Y = A + B + C + D		1
		OR4A	Y = !A + B + C + D		1
Exclusive OR	XOR, XOR-OR	XOR	Y = A ^ B		1
		XO1	Y = (A ^ B) + C		1
		XO1A	Y = !(A ^ B) + C		1
	XNOR, XOR-AND	XNOR	Y = !(A ^ B)		1
		XA1	Y = (A ^ B) C		1
		XA1A	Y = !(A ^ B) C		1

non-combinable hard macros

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	4-input AND	AND4	Y = A B C D		1
		AND4A	Y = (!A B C D)		1
		AND4D	Y = **!A !B** !C !D		2
	5-input AND	AND5B	Y = !A !B C D E		1
OR	2-input OR	OR2B	Y = !A + !B		1
	3-input OR	OR3C	Y = !A + !B + !C		1
	4-input OR	OR4B	Y = !A + !B + C + D		1
		OR4C	Y = !A + !B + !C + D		1
		OR4D	Y = **!A** + **!B** + !C + !D		2
	5-input OR	OR5B	Y = !A + !B + C + D + E		1
NAND	3-input NAND	NAND3	Y = !(A B C)		1
	4-input NAND	NAND4	Y = !(**A B** C D)		2
		NAND4A	Y = !(!A B C D)		1
		NAND4B	Y = !(!A !B C D)		1
	5-input NAND	NAND5C	Y = !(!A !B !C D E)		1
NOR	4-input NOR	NOR4	Y = !(**A** + **B** + C + D)		2
		NOR4C	Y = !(!A + !B + !C + D)		1
		NOR4D	Y = !(!A + !B + !C + !D)		1
	5-input NOR	NOR5C	Y = !(!A + !B + !C + D + E)		1
Exclusive OR	AND-XOR	AX1	Y = (!A B) ^ C		1
		AX1A	Y = !(!A B) ^ C		2
		AX1C	Y = (A B) ^ C		1
AND-OR		AO10	Y = ((AB) + C) (D + E)		1
		AO2E	Y = (!A!B) + !C + !D		1
		AO3A	Y = (A B C) + D		1
		AO6	Y = A B + C D		1
		AO6A	Y = A B + C !D		1
		AO7	Y = A B C + D + E		1
		AO8	Y = (AB) + (!C!D) + E		1
		AO9	Y = (AB) + C + D + E		1
AND-OR-Invert		AOI1	Y = !(A B + C)		1
		AOI2B	Y = !((!A B) + !C + D)		1
		AOI4	Y = !((A B) + (**C D**))		2
		AOI4A	Y = !(A B + !C D)		1
OR-AND		OA3B	Y = ((!A + B) !C D)		1
OR-AND-Invert		OAI3	Y = !((A + B) C D)		1

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Adders	Half adders	HA1	CO = A B S = A ^ B		2
		HA1A	CO = !A B S = !(A ^ B)		2
		HA1B	CO = !(A B) S = !(A ^ B)		2
		HA1C	CO = !(A B) S = (A ^B)		2
	Full adders	FA1A	CO = (CI !B !A) + (A !B) + (B CI A) S = (B !A !CI) + (CO !A CI) + (CO A !CI) + (B A CI)		2
		FA1B	CO = !A(!B + B CI) + A(!B CI) S = !A(!CI CO + CI B) + A(!CI B + CI CO)		2
		FA2A	CO = (CI !B !(A0+A1)) + (!B (A0+A1)) + (B CI (A0+A1)) S = (B !(A0+A1) !CI) + (CO !(A0+A1) CI) + (CO(A0+A1) !CI) + (B(A0+A1)CI)		2
Boolean		CS1	Y = !(A + S B) C + D (A + S B)		1
		CY2A	Y = A1 B1 + A0 B0 A1 + A0 B0 B1		1
Flip-Flops	D-type	DF1	Q = (CLK, D, –, –)	1	
		DF1A	QN = !(CLK, D, –, –)	1	
		DF1B	Q = (!CLK, D, –, –)	1	
		DF1C	QN = !(!CLK, D, –, –)	1	
	D-type with clear	DFC1	Q = (CLK, D, CLR, –)	1	1
		DFC1A	Q = (!CLK, D, CLR, –)	1	1
		DFC1B	Q = (CLK, D, !CLR, –)	1	
		DFC1D	Q = (!CLK, D, !CLR, –)	1	
		DFC1E	QN = !(CLK, D, !CLR, –)	2	1
		DFC1G	QN = !(!CLK, D, !CLR, –)		2
	D-type with enable	DFE	Q = (CLK, !E Q + E D, –, –)	1	
		DFE1B	Q = (CLK, !E D + E Q, –, –)	1	
		DFE1C	Q = (!CLK, D !E + Q E, –, –)	1	
		DFE3A	Q = (CLK, D E + Q !E, !CLR, –)	1	
		DFE3B	Q = (!CLK, D E + Q !E, !CLR, –)	1	
		DFE3C	Q = (CLK, D !E + Q E, !CLR, –)	1	
		DFE3D	Q = (!CLK, D !E + Q E, !CLR, –)	1	
		DFEA	Q = (!CLK, !E Q + E D, –, –)	1	1
Multiplexers	Logic module	CM8	Y = (D0 !(S00 S01) + D1(S00 S01)) !(S10 + S11) + (D2 !(S00 S01) + D3(S00 S01)) (S10 + S11)		1
		MXT	Y = (!S1 (!S0A D0) + (S0A D1)) + (S1 (!S0B D2 + S0B D3))		2
		MXC1	Y = !(!S A + S B) C + (!S A + S B) D		2

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Flip-Flops (continued)	D-type with multiplexed data	DFM	Q = (CLK, A !S + B S, –, –)	1	
		DFM1B	QN = !(CLK, A !S + B S, –, –)	1	
		DFM1C	QN = !(!CLK, A !S + B S, –, –)	1	
		DFM3	Q = (CLK, A !S + B S, CLR, –)	1	1
		DFM3B	Q = (!CLK, A !S + B S, !CLR, –)	1	
		DFM3E	Q = (!CLK, A !S + B S, CLR, –)	1	1
		DFM4C	QN = !(!CLK, !A !S + !B S, –, !PRE)	1	
		DFM4D	QN = !(!CLK, A !S + B S, –, !PRE)	1	
		DFM6A	Q = (CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM6B	Q = (!CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM7A	Q = (CLK, (0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11), !CLR, –)	1	
		DFM7B	Q = (!CLK, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 +D3 S0) (S10 + S11), !CLR, –)	1	
		DFMA	Q = (!CLK, A !S + B S, –, –)	1	
		DFMB	Q = (CLK, A !S + B S, !CLR, –)	1	
		DFME1A	Q = (CLK, !E A !S + !E B S + E Q, –, –)	1	
	D-type flip-flops with preset	DFP1	Q = (CLK, D, –, PRE)		2
		DFP1A	Q = (!CLK, D, –, PRE)		2
		DFP1B	Q = (CLK, D, –, !PRE)		2
		DFP1C	QN = !(CLK, D, –, PRE)	1	1
		DFP1D	Q = (!CLK, D, –, !PRE)		2
		DFP1E	QN = !(CLK, D, –, !PRE)	1	
		DFP1F	Q = (!CLK, D, –, PRE)	1	1
		DFP1G	QN = !(!CLK, D, –, !PRE)		1
	D-type flip-flops w/ clear and preset	DFPC	Q = (CLK, D, CLR, PRE)		2
		DFPCA	Q = (!CLK, D, !CLR, PRE)		2
	J-$\overline{K}$ flip-flops	JKF	Q = (CLK, !Q J + Q K, –, –)	1	
		JKF1B	Q = (!CLK, !Q J + Q K, –, –)	1	
		JKF2A	Q = (CLK, !Q J + Q K, !CLR, –)	1	
		JKF2B	Q = (!CLK, !Q J + Q K, !CLR, –)	1	
		JKF2C	Q = (CLK, !Q J + Q K, CLR, –)	1	1
		JKF2D	Q = (!CLK, !Q J + Q K, CLR, –)	1	1
	Toggle flip-flops	TF1A	Q = (CLK, T !Q + !T Q, !CLR, –)	1	
		TF1B	Q = (!CLK, T !Q + !T Q, !CLR, –)	1	

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Data Latch	D-type latch	DL1	Q = (G, D, –, –)	1	
		DL1A	QN = !(G, D, –, –)	1	
		DL1B	Q = !(!G, D, –, –)	1	
		DL1C	QN = !(!G, D, –, –)	1	
	With clear	DLC	Q = (G, D, !CLR, –)	1	
		DLC1	Q = (G, D, CLR, –)		1
		DLC1A	Q = (!G, D, CLR, –)		1
		DLC1F	QN = !(G, D, CLR, –)		1
		DLC1G	QN = !(!G, D, CLR, –)		1
		DLCA	Q = (!G, D, !CLR, –)	1	
	With enable	DLE	Q = (G, Q !E + D E, –, –)	1	
		DLE1D	QN = !(!G, !E !D + E QN, –, –)	1	
		DLE2B	Q = (!G, D !E + Q E, !CLR, –)	1	
		DLE2C	Q = (!G, !E D + Q E, CLR, –)		1
		DLE3B	Q = (!G, !E D + Q E, –, PRE)		1
		DLE3C	Q = (!G, !E D + Q E, –, !PRE)		1
		DLEA	Q = (G, Q E + D !E, –, –)	1	
		DLEB	Q = (!G, Q !E + D E, –, –)	1	
		DLEC	Q = (!G, Q E + D !E, –, –)	1	
	With multiplexed data	DLM	Q = (G, A !S + B S, –, –)	1	
		DLM3	Q = (G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, –, –)	1	
		DLM3A	Q = (!G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, –, –)	1	
		DLM4	Q = (G, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11), –, –)	1	
		DLM4A	Q = (!G, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !(S0 + D3 S0) (S10 + S11), –, –)	1	
		DLMA	Q = (!G, A !S + B S, –, –)	1	
	With multiplexed data and enable	DLME1A	Q = (!G, A !S !E + B S !E + E Q, –, –)	1	
	With preset	DLP1	Q = (G, D, –, PRE)		1
		DLP1A	Q = (!G, D, –, PRE)		1
		DLP1B	Q = (G, D, –, !PRE)		1
		DLP1C	Q = (!G, D, –, !PRE)		1
		DLP1D	QN = !(G, D, –, !PRE)	1	
		DLP1E	QN = !(!G, D, –, !PRE)	1	
Clock Net Interface		CLKINT		clock modules = 1	
Tie-Off		V_{CC}		modules = 0	
		GND		modules = 0	

soft macros

FUNCTION	DESCRIPTION	MACRO NAME	LOGIC LEVELS	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Counters	4-bit binary counter with load, clear	CNT4A	4	4	8
	4-bit binary counter with load, clear, carry in, carry out	CNT4B	4	4	7
	Fast 16-bit down counter, parallel loadable	FCTD16C	2	19	33
	Fast 8-bit down counter, parallel loadable	FCTD8A	1	10	18
	Fast 8-bit down counter, parallel loadable	FCTD8B	1	9	13
	Fast 16-bit up counter, parallel loadable	FCTU16C	2	19	31
	Fast 8-bit up counter, parallel loadable	FCTU8A	1	10	17
	Fast 8-bit up counter, parallel loadable	FCTU8B	1	9	12
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	5	4	13
	Very fast 16-bit down counter, delay after load, registered control input	VCTD16C	1	34	41
	2-bit down counter, prescaler, delay after load, use to build VCTD counters	VCTD2CP	1	5	2
	2-bit down counter, upper bits, delay after load, use to build VCTD counters	VCTD2CU	1	2	3
	4-bit down counter, lower bits, delay after load, use to build VCTD counters	VCTD4CL	1	4	7
	4-bit down counter, middle bits, delay after load, use to build VCTD counters	VCTD4CM	1	4	8
Decoders	2-to-4 decoder	DEC2X4	1		4
	2-to-4 decoder with active low outputs	DEC2X4A	1		4
	3-to-8 decoder	DEC3X8	1		8
	3-to-8 decoder with active low outputs	DEC3X8A	1		8
	4-to-16 decoder with active low outputs	DEC4X16A	2		20
	2-to-4 decoder with enable	DECE2X4	1		4
	2-to-4 decoder with enable and active low outputs	DECE2X4A	1		4
	3-to-8 decoder with enable	DECE3X8	2		11
	3-to-8 decoder with enable and active low outputs	DECE3X8A	2		11
Registers	Octal latch with clear	DLC8A	1	8	
	Octal latch with enable	DLE8	1	8	
	Octal latch with multiplexed data	DLM8	1	8	
	4-bit shift register with clear	SREG4A	1	4	
	8-bit shift register with clear	SREG8A	1	8	
Adders	8-bit adder	FADD8	3		44
	9-bit adder	FADD9	3		49
	10-bit adder	FADD10	3		56
	12-bit adder	FADD12	4		69
	16-bit adder	FADD16	5		97
	Very fast 16-bit adder	VAD16C	3		97
	Very fast 16-bit adder with carry in	VADC16C	1		97

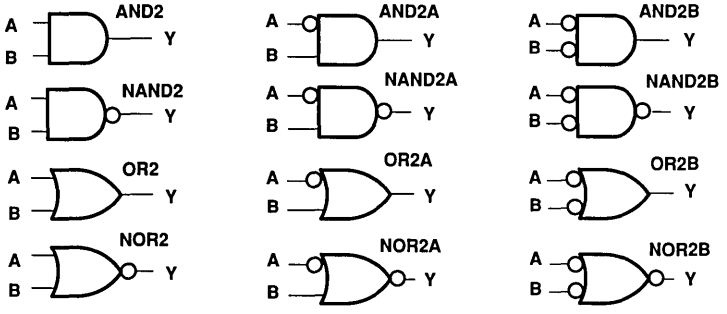
soft macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	LOGIC LEVELS	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Comparators	4-bit identity comparator	ICMP4	2		5
	8-bit identity comparator	ICMP8	3		9
	2-bit magnitude comparator with enable	MCMPC2	3		9
	4-bit magnitude comparator with enable	MCMPC4	4		18
	8-bit magnitude comparator with enable	MCMPC8	6		36
Multiplexer	8-to-1 multiplexer	MX8	2		3
	8-to-1 multiplexer with active low outputs	MX8A	2		3
	16-to-1 multiplexer	MX16	2		5
Multiplier	8-bit by 8-bit multiplier	SMULT8	22		242

TTL macros

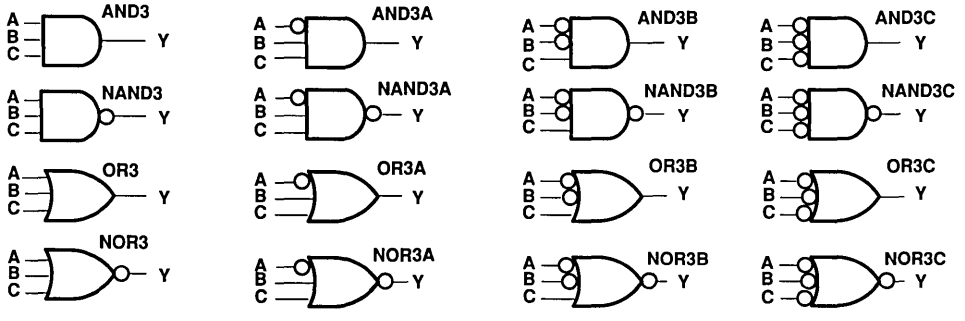
MACRO NAME	DESCRIPTION	LOGIC LEVELS	NO. OF MODULE(S)	
			SEQUENTIAL	COMBINATIONAL
TA00	2-input NAND	1		1
TA02	2-input NOR	1		1
TA04	Inverter	1		1
TA07	Buffer	1		1
TA08	2-input AND	1		1
TA10	3-input NAND	1		1
TA11	3-input AND	1		1
TA20	4-input NAND	1		2
TA21	4-input AND	1		1
TA27	3-input NOR	1		1
TA32	2-input OR	1		1
TA40	4-input NAND	1		2
TA42	4-to-10 decoder	1		10
TA51	AND-OR-Invert	1		2
TA54	4-wide, 2-input AND-OR-Invert	2		5
TA55	2-wide 4-input AND-OR-Invert	2		3
TA86	2-input exclusive OR	1		1
TA138	3-to-8 decoder with enable and active low outputs	2		12
TA139	2-to-4 decoder with enable and active low outputs	1		4
TA150	16-to-1 multiplexer with active low enable	3		6
TA151	8-to-1 multiplexer with enable and active high/low outputs	3		5
TA153	4-to-1 multiplexer	2		2
TA154	4-to-16 decoder with active low select	2		22
TA157	2-to-1 multiplexer with active low enable	1		1
TA160	4-bit decade counter with clear and load	4	4	8
TA161	4-bit binary counter with clear and load	3	4	6
TA164	8-bit serial in, parallel out shift register with clear	1	8	
TA169	4-bit up/down counter	6	4	14
TA174	Hex D-type flip-flop with clear	1	6	
TA175	Quadruple D-type flip-flop with clear	1	4	
TA190	4-bit up/down decade counter with up/down mode	7	4	31
TA191	4-bit up/down binary counter with up/down mode	7	4	30
TA194	4-bit bidirectional universal shift register	1	4	4
TA195	4-bit parallel access shift register	1	4	1
TA269	8-bit up/down binary counter	8	8	28
TA273	Octal register with clear	1	8	
TA280	Parity generator and checker	4		9
TA377	Octal register with active low enable	1	8	
TA688	8-bit identity comparator	3		9

HARD MACRO SYMBOLS



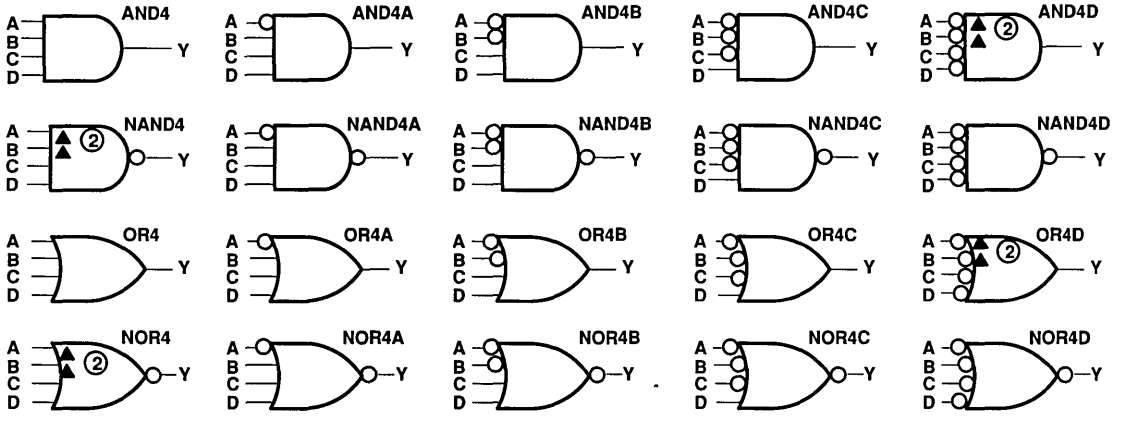
Module Count = 1

Figure 7. 2-Input Gates



Module Count = 1

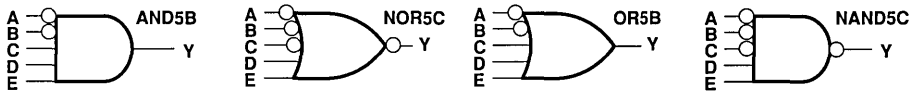
Figure 8. 3-Input Gates



Module Count = 1 (unless otherwise noted)

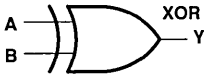
② Indicates Module Count = 2 ▲ Indicates extra delay input

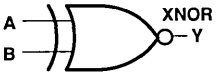
Figure 9. 4-Input Gates



Module Count = 1

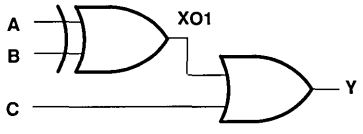
Figure 10. 5-Input Gates

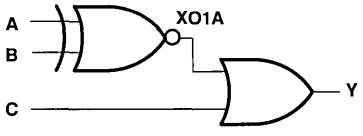




Module Count = 1

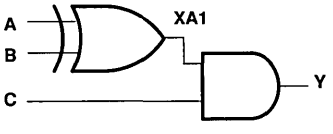
Figure 11. XOR/XNOR Gates

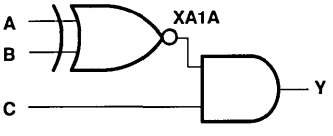




Module Count = 1

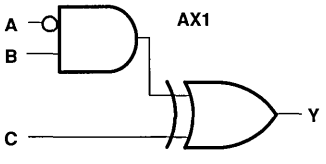
Figure 12. XOR-OR/XNOR-OR Gates



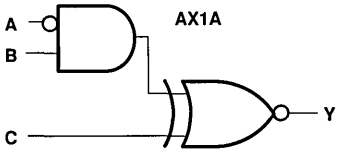


Module Count = 1

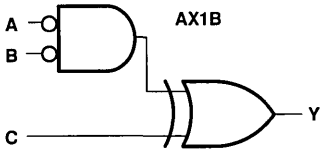
Figure 13. XOR-AND/ XNOR-AND Gates



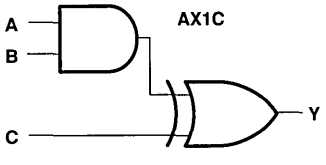
Module Count = 1



Module Count = 2

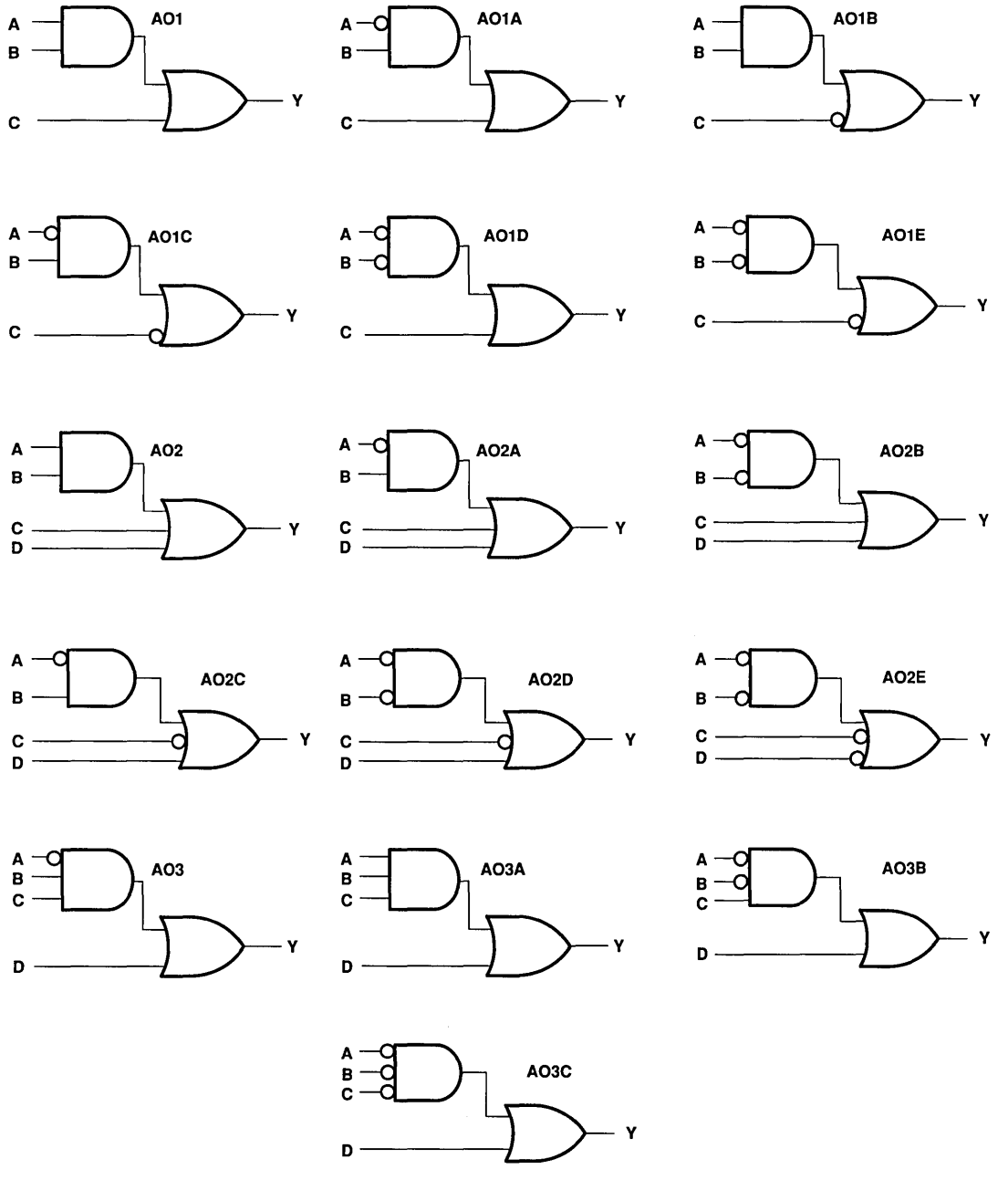


Module Count = 1



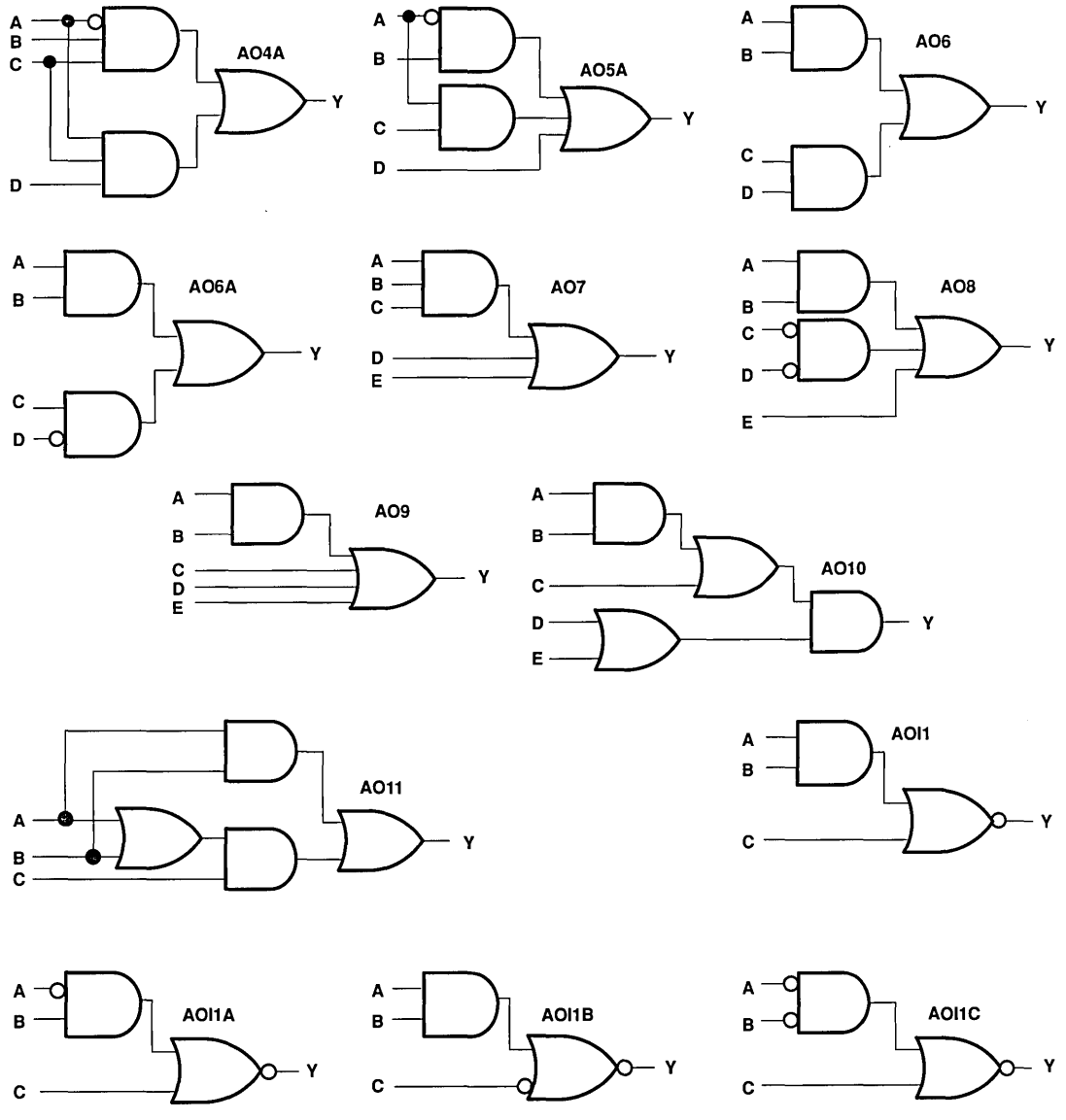
Module Count = 1

Figure 14. AND-XOR/AND-XNOR Gates



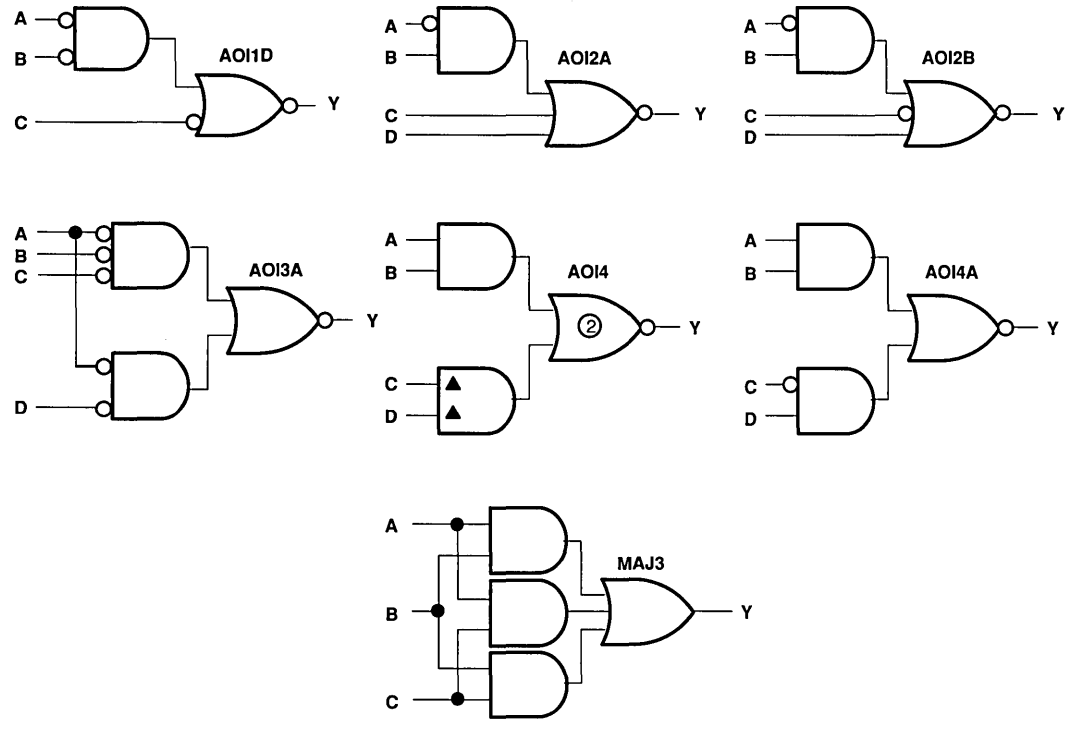
Module Count = 1

Figure 15. AND-OR/AND-NOR Gates



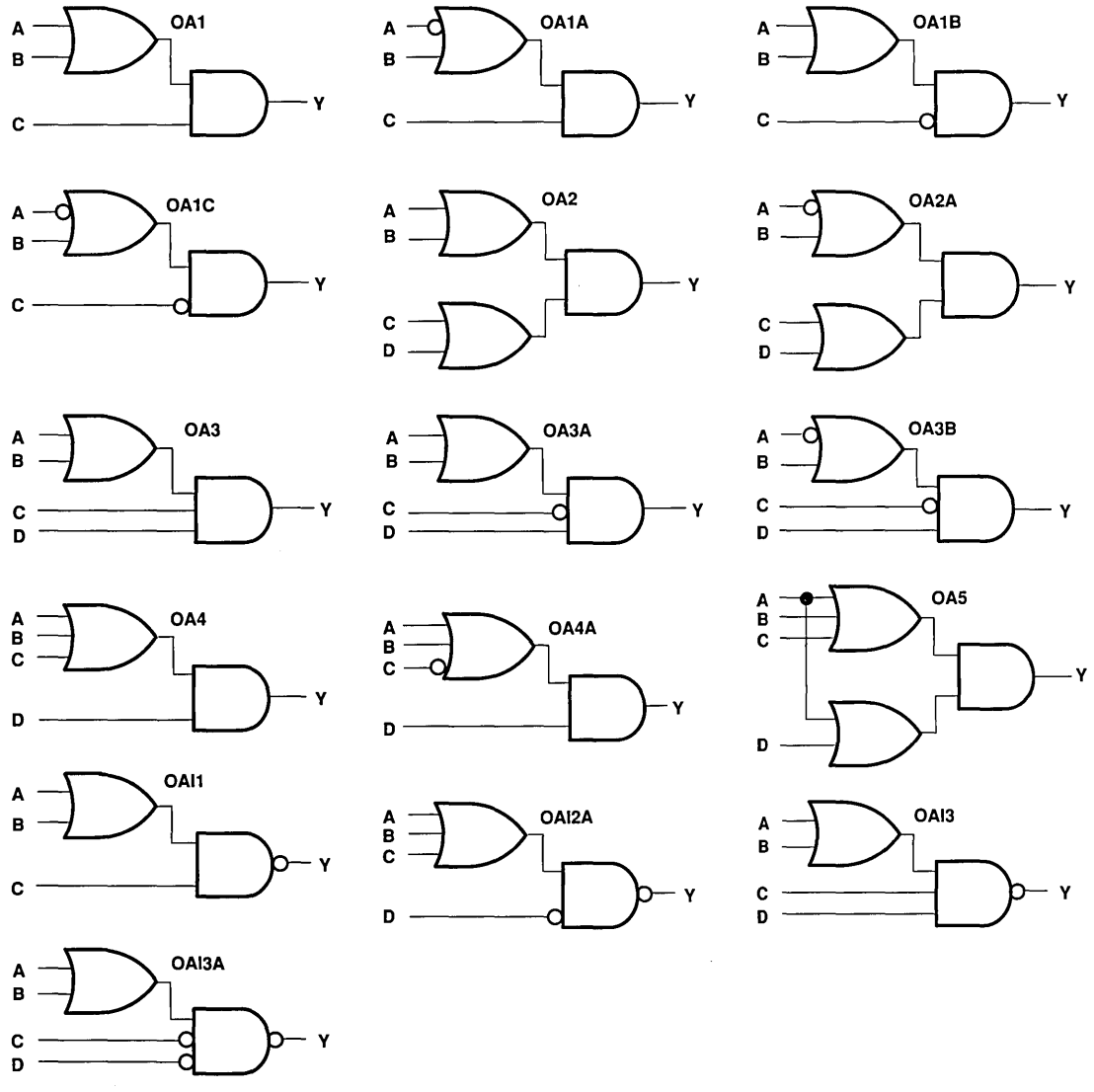
Module Count = 1

Figure 14. AND-OR/AND-NOR Gates (Continued)



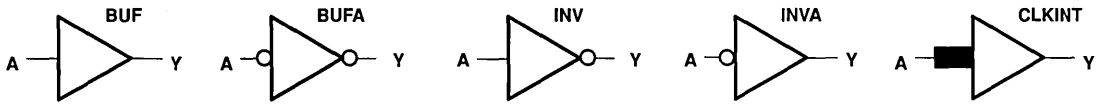
Module Count = 1 (unless otherwise noted)
② Indicates Module Count = 2
▲ Indicates extra delay input

Figure 14. AND-OR/AND-NOR Gates (Continued)



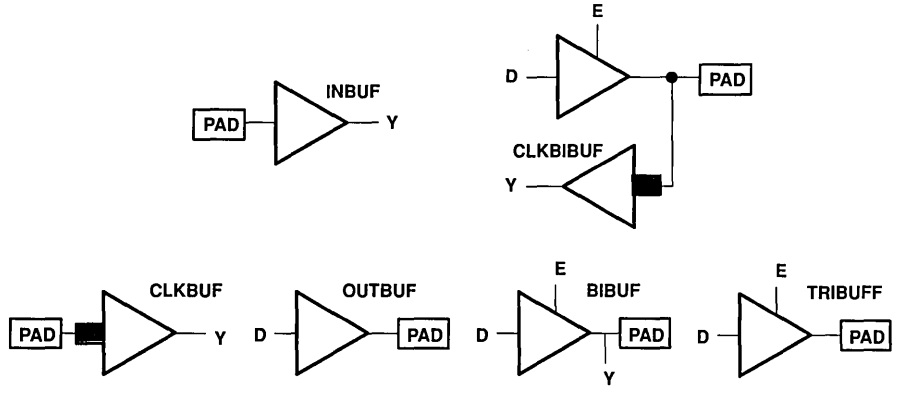
Module Count = 1

Figure 16. OR-AND/OR-NAND Gates



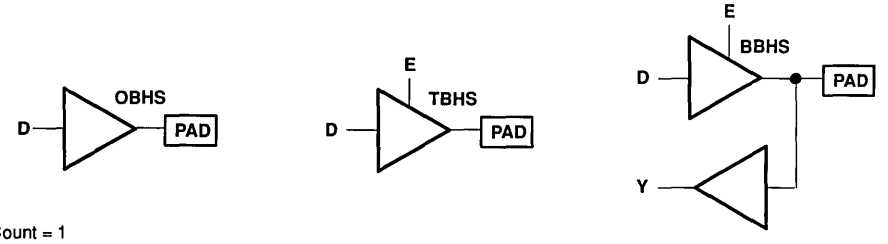
Module Count = 1

Figure 17. Buffers



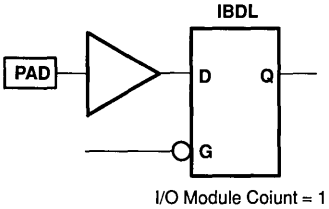
I/O Module Count = 1

Figure 18. I/O Buffers



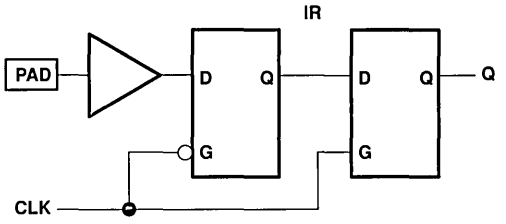
I/O Module Count = 1

Figure 19. High-Slew Output Buffers



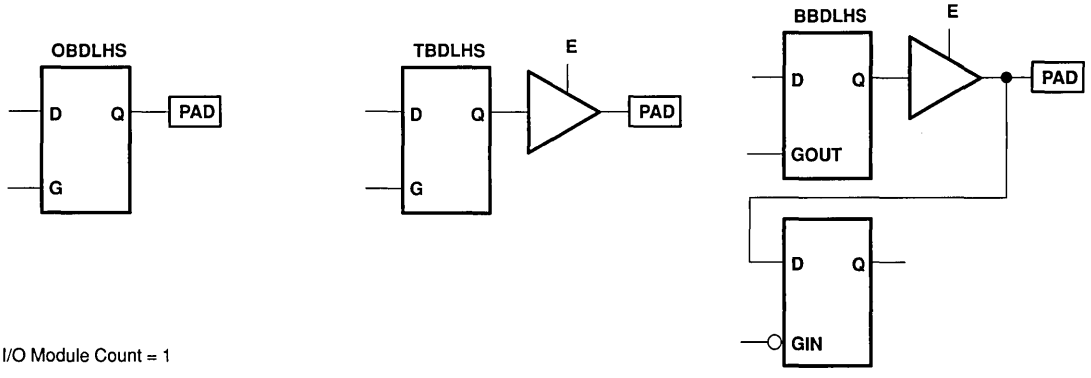
I/O Module Coiunt = 1

Figure 20. Input Buffer With Latch



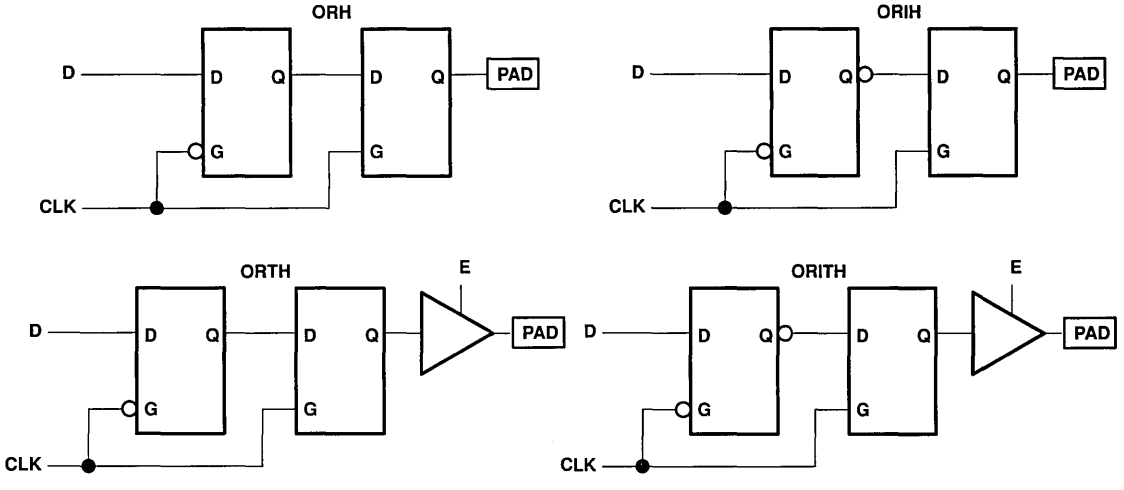
I/O Module Coiunt = 1

Figure 21. Input Buffer With Register



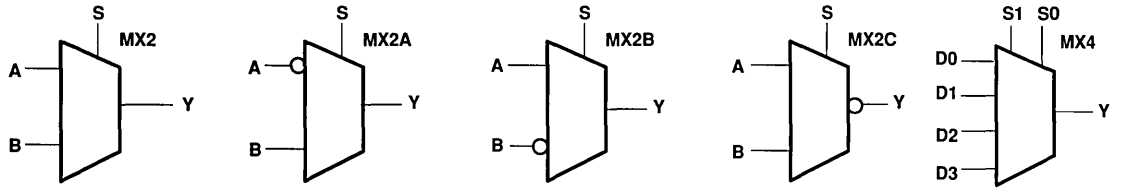
I/O Module Count = 1

Figure 22. High-Slew Output Buffers With Latches

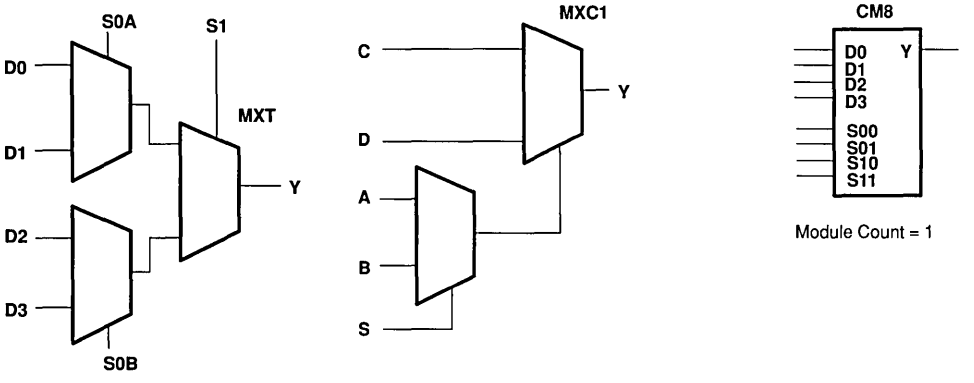


I/O Module Coiunt = 1

Figure 23. Output Buffers With Registers



Module Count = 1

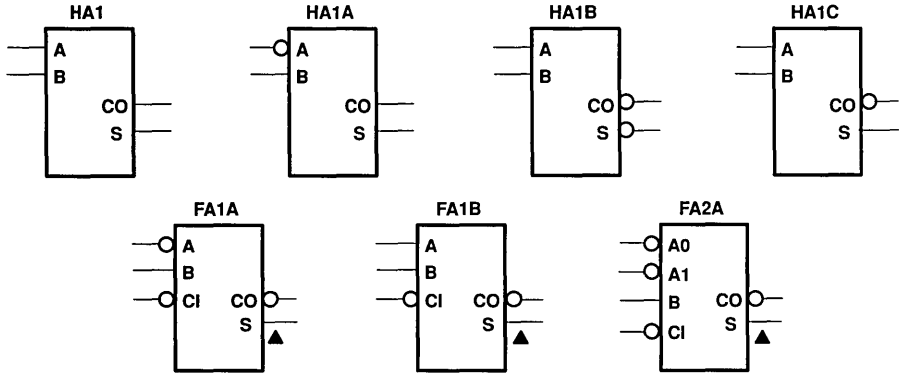


Module Count = 2

Module Count = 2

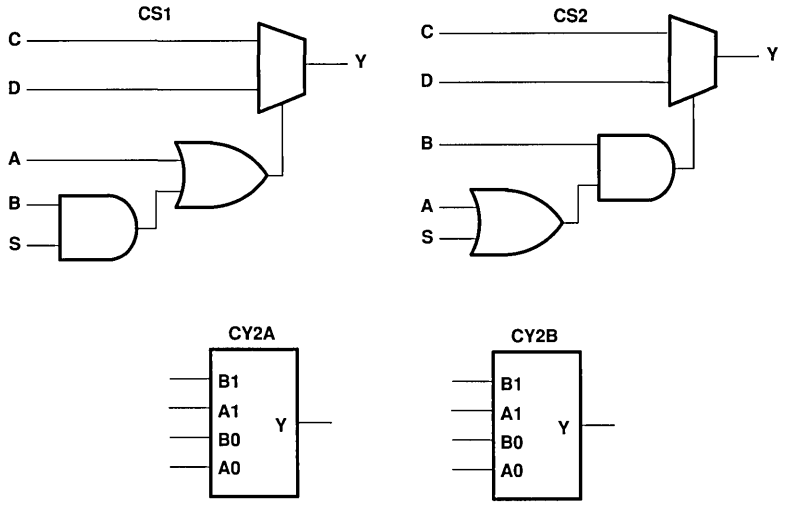
Module Count = 1

Figure 24. Multiplexers



Module Count = 2
▲ Indicates two logic module delay path

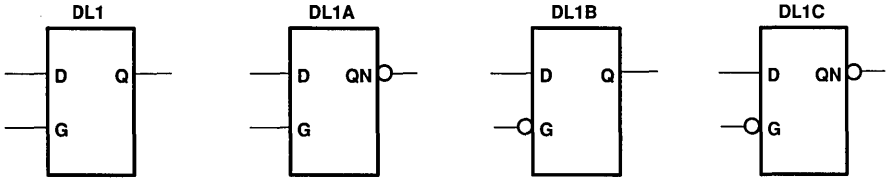
Figure 25. Adders



Module Count = 1

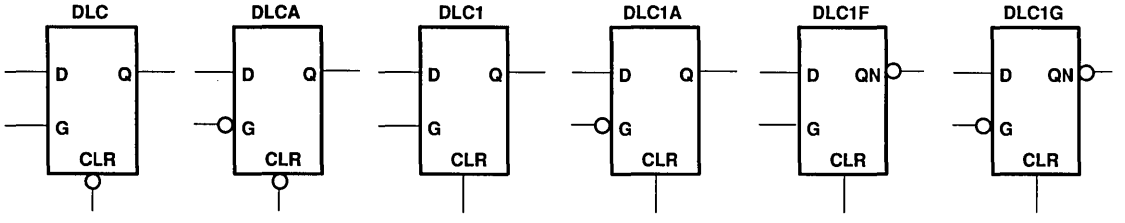
Figure 26. Boolean

D-TYPE LATCHES



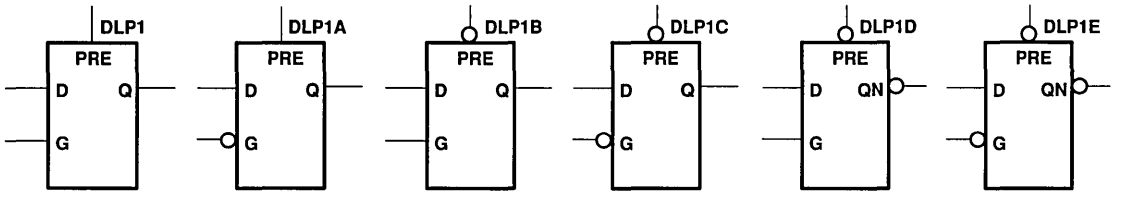
Module Count = 1

D-TYPE LATCHES WITH CLEAR



Module Count = 1

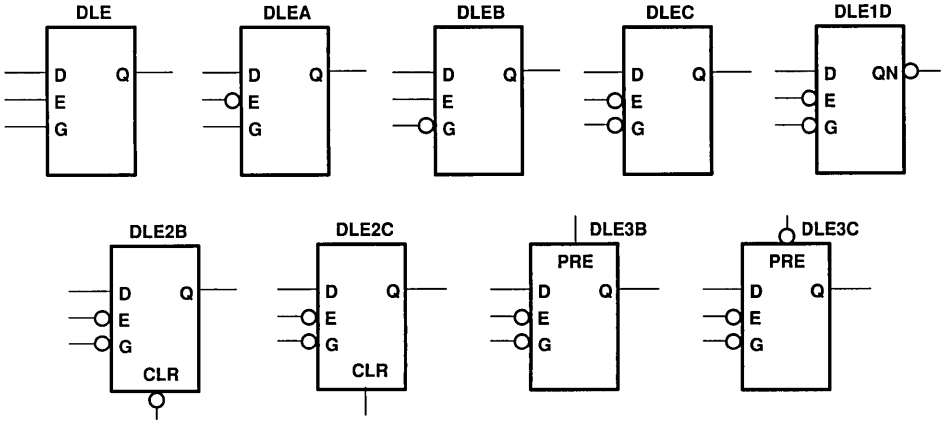
D-TYPE LATCHES WITH PRESET



Module Count = 1

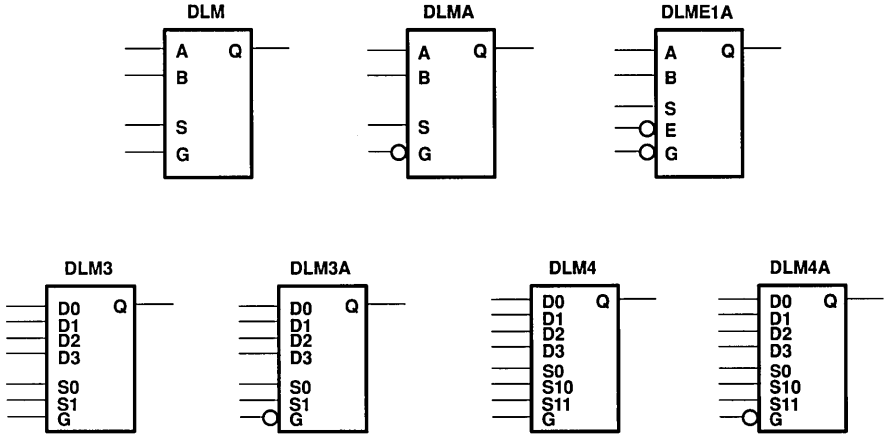
Figure 27. D-Type Latches

D-TYPE LATCHES WITH ENABLE



Module Count = 1

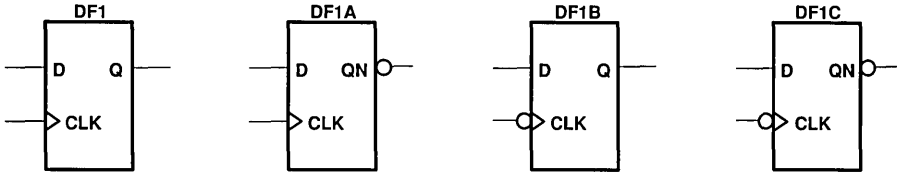
D-TYPE LATCHES WITH MULTIPLEXED INPUTS



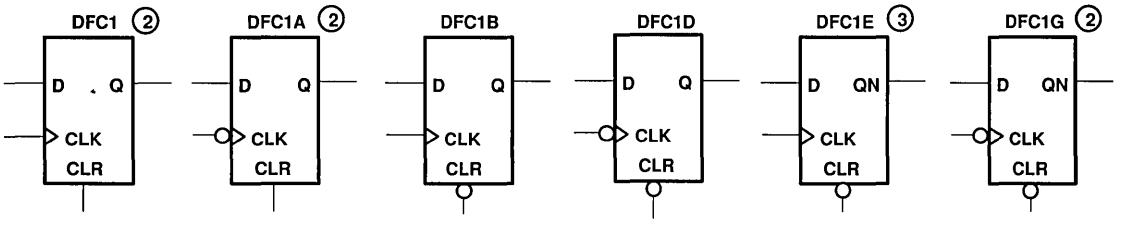
Module Count = 1

Figure 24. D-Type Latches (Continued)

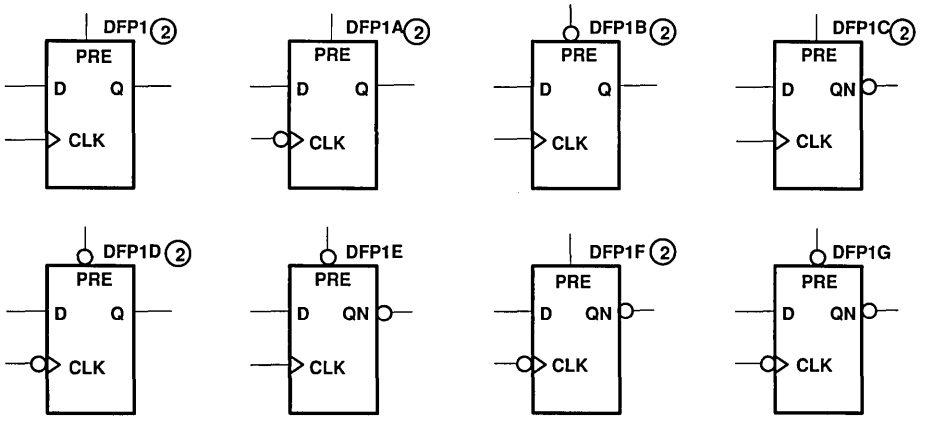
D-TYPE FLIP-FLOPS



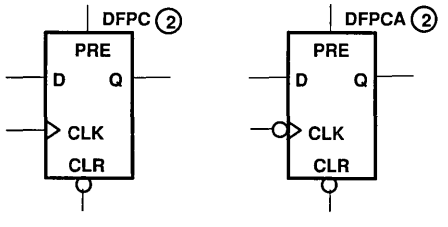
D-TYPE FLIP-FLOPS WITH CLEAR



D-TYPE FLIP-FLOPS WITH PRESET

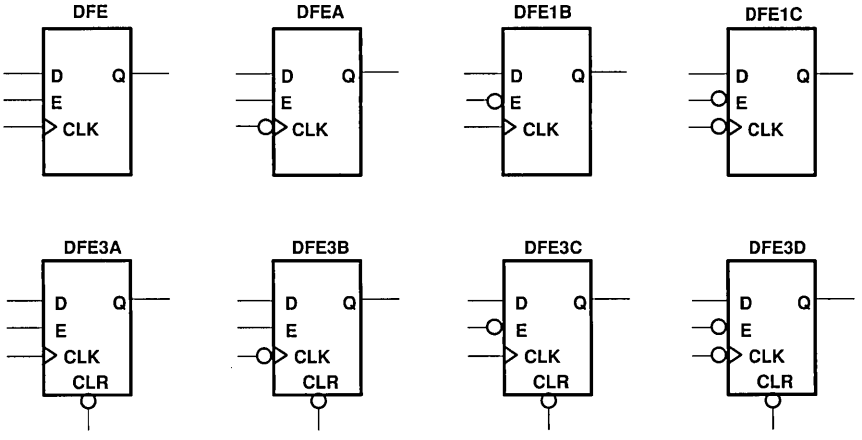


D-TYPE FLIP-FLOPS WITH PRESET AND CLEAR



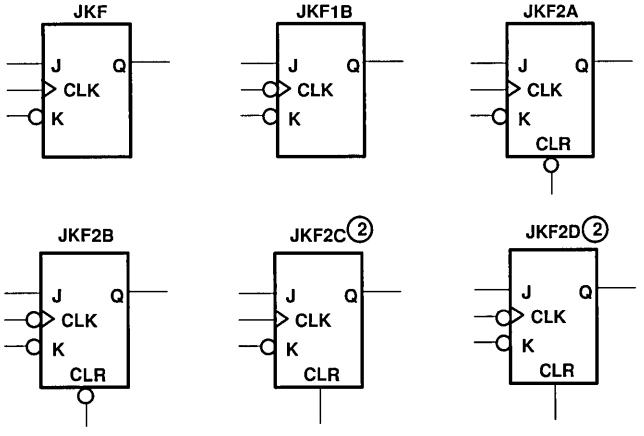
Module Count = 1 (unless otherwise noted)
(2) Indicates Module Count = 2, (3) Indicates Module Count = 3

Figure 28. D-Type Flip-Flops



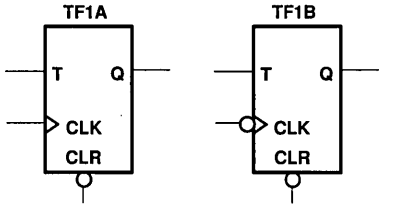
Module Count = 1

Figure 29. D-Type Flip-Flops With Enable



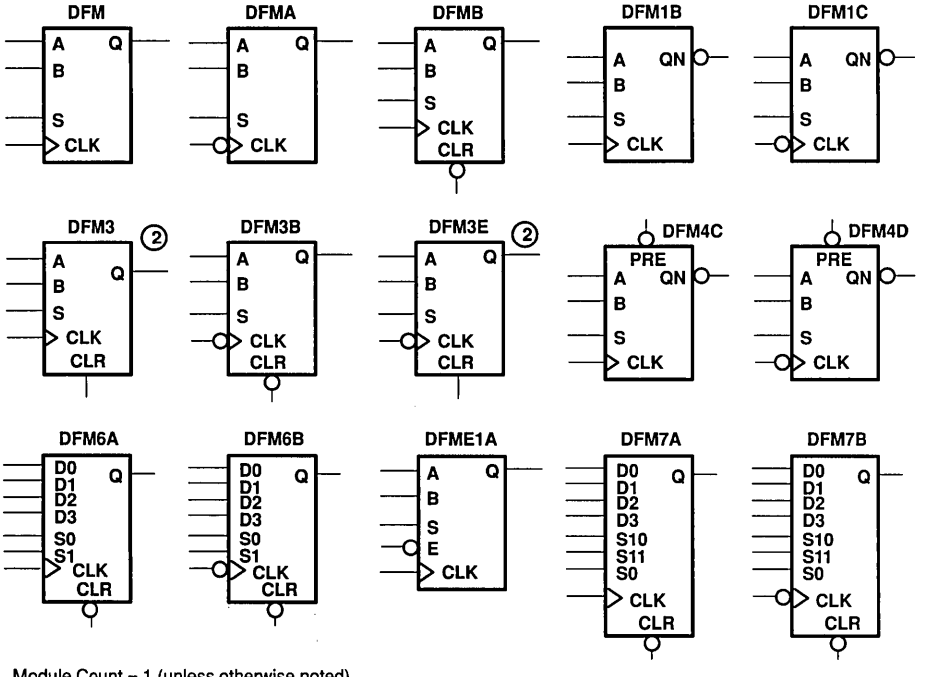
Module Count = 1 (unless otherwise noted)
(2) Indicates Module Count = 2

Figure 30. J-K Flip-Flops



Module Count = 1

Figure 31. Toggle Flip-Flips



Module Count = 1 (unless otherwise noted)
(2) Indicates Module Count = 2

Figure 32. Multiplexed-Input Flip-Flops

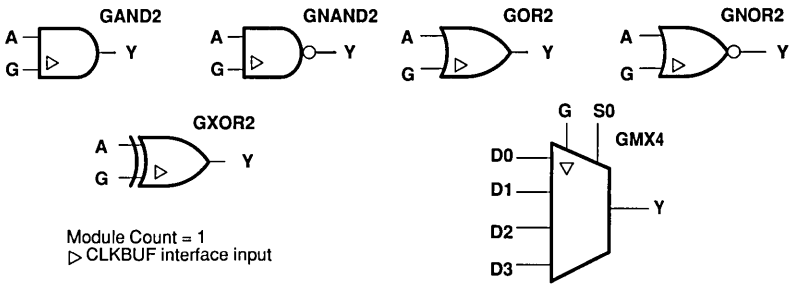
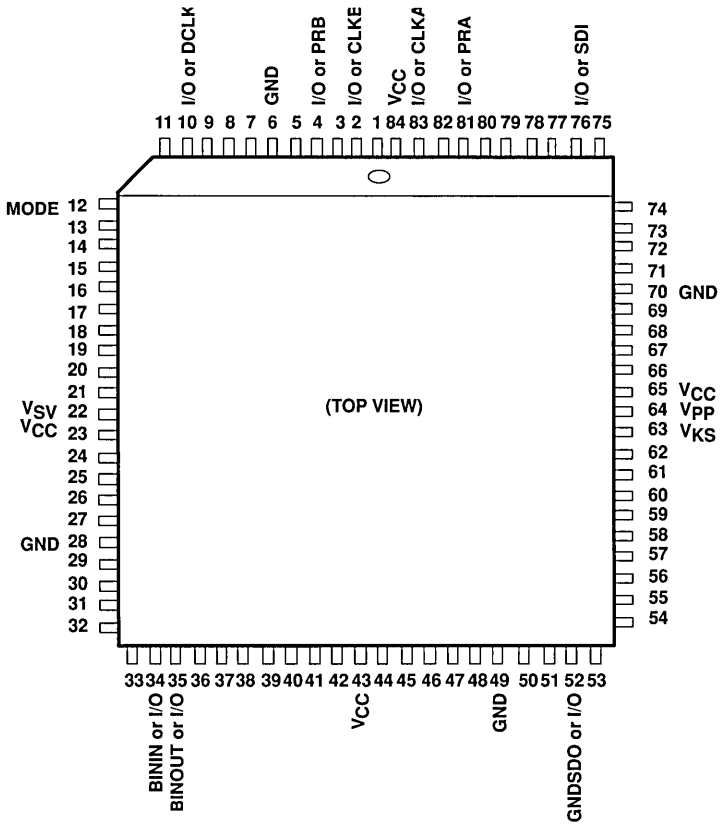


Figure 33. Clock Buffer (CLKBUF) Interface

package pin assignments

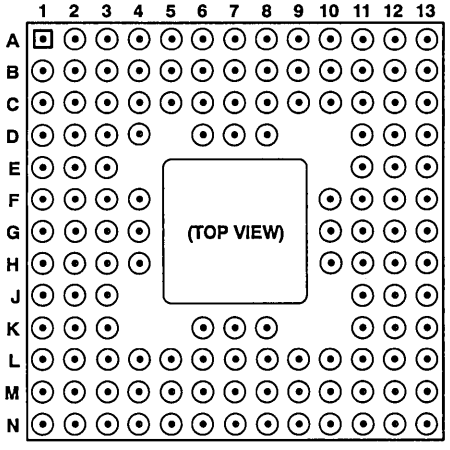


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 34. 84-Pin PLCC Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 133-Pin Ceramic Pin Grid Array Package

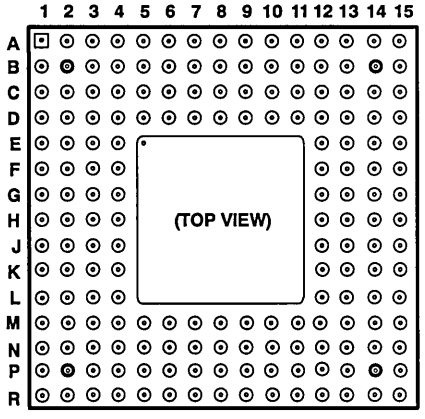
SIGNAL	LOCATION
PRA or I/O	B8
PRB or I/O	C6
MODE	A1
SDI or I/O	B12
SDO or I/O	N12
DCLK or I/O	C3
CLKA or I/O	B7
CLKB or I/O	B6
GND	E3, F4, J2, J3, L5, M9, L9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	G13
V_{SV}	G4, G12
V_{KS}	H13

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.
J. Pin D4 is an orientation pin and is electrically isolated.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 35. 133-Pin CPGA Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 176-Pin and 177-Pin Ceramic Pin Grid Array Package

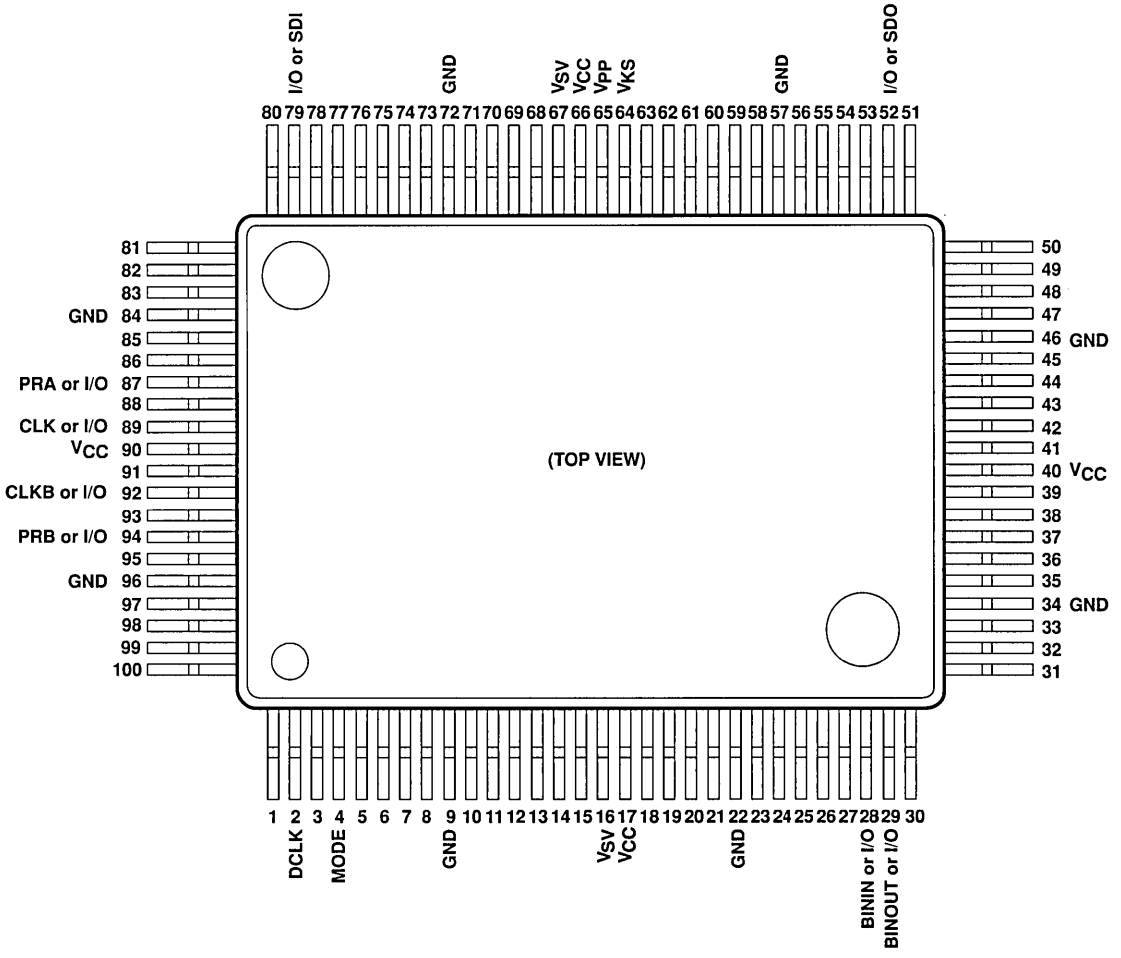
SIGNAL	SIGNALS
PRA or I/O	C9
PRB or I/O	D7
MODE	C3
SDI or I/O	B14
SDO or I/O	P13
DCLK or I/O	B3
CLKA or I/O	A9
CLKB or I/O	B8
GND	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	J14
V_{SV}	H2, H14
V_{KS}	J13

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.
J. Pin E5 is an orientation pin on the 177-pin package only.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 36. 176-Pin and 177-Pin CPGA Pin Assignment

package pin assignments (continued)

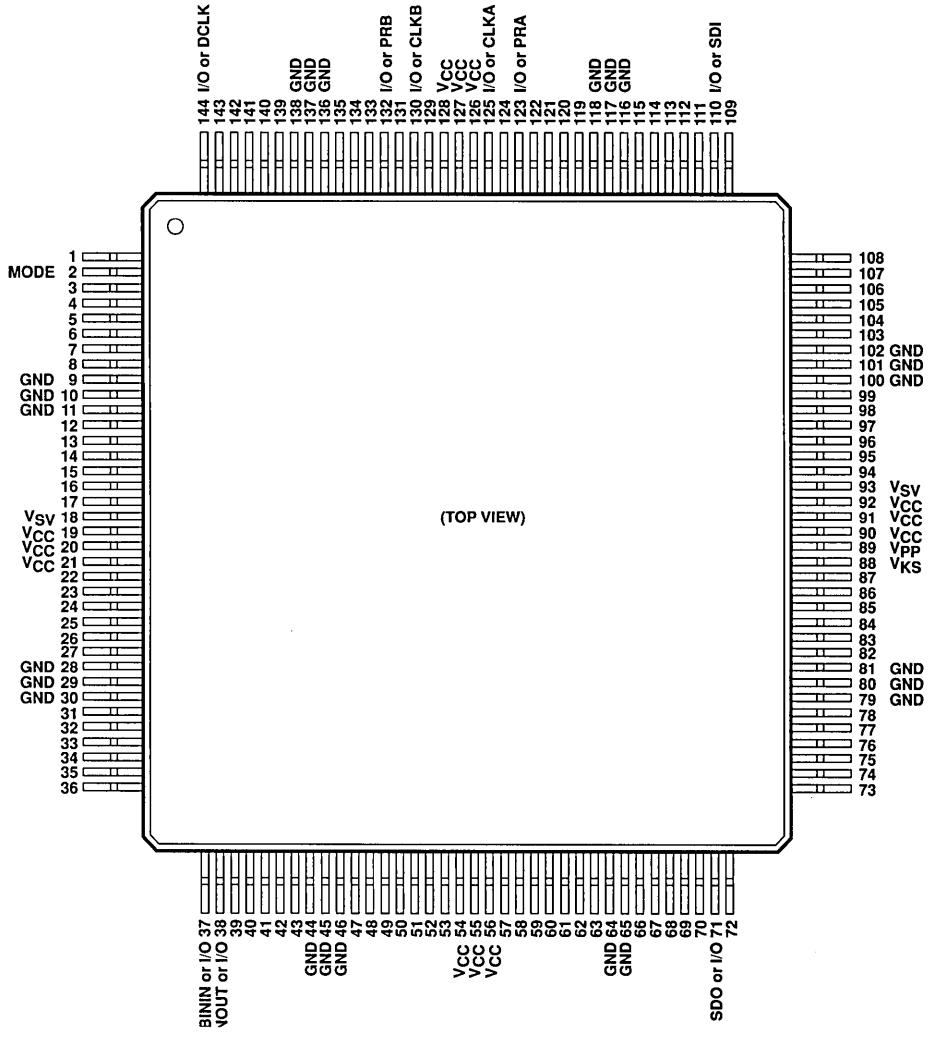


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 37. 100-Pin PQFP Pin Assignment

package pin assignments (continued)

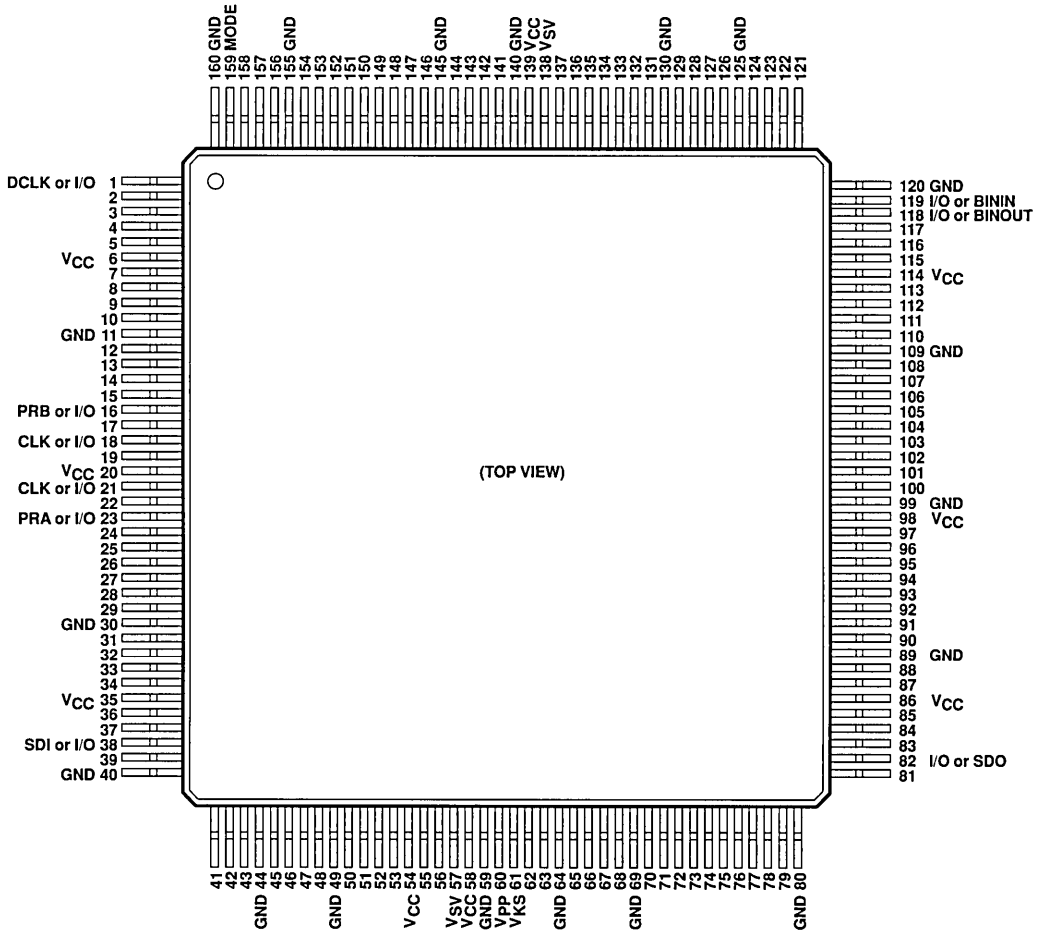


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 38. 144-Pin PQFP Pin Assignment

package pin assignments (continued)



NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 39. 160-Pin PQFP Pin Assignment

package pin assignments (continued)

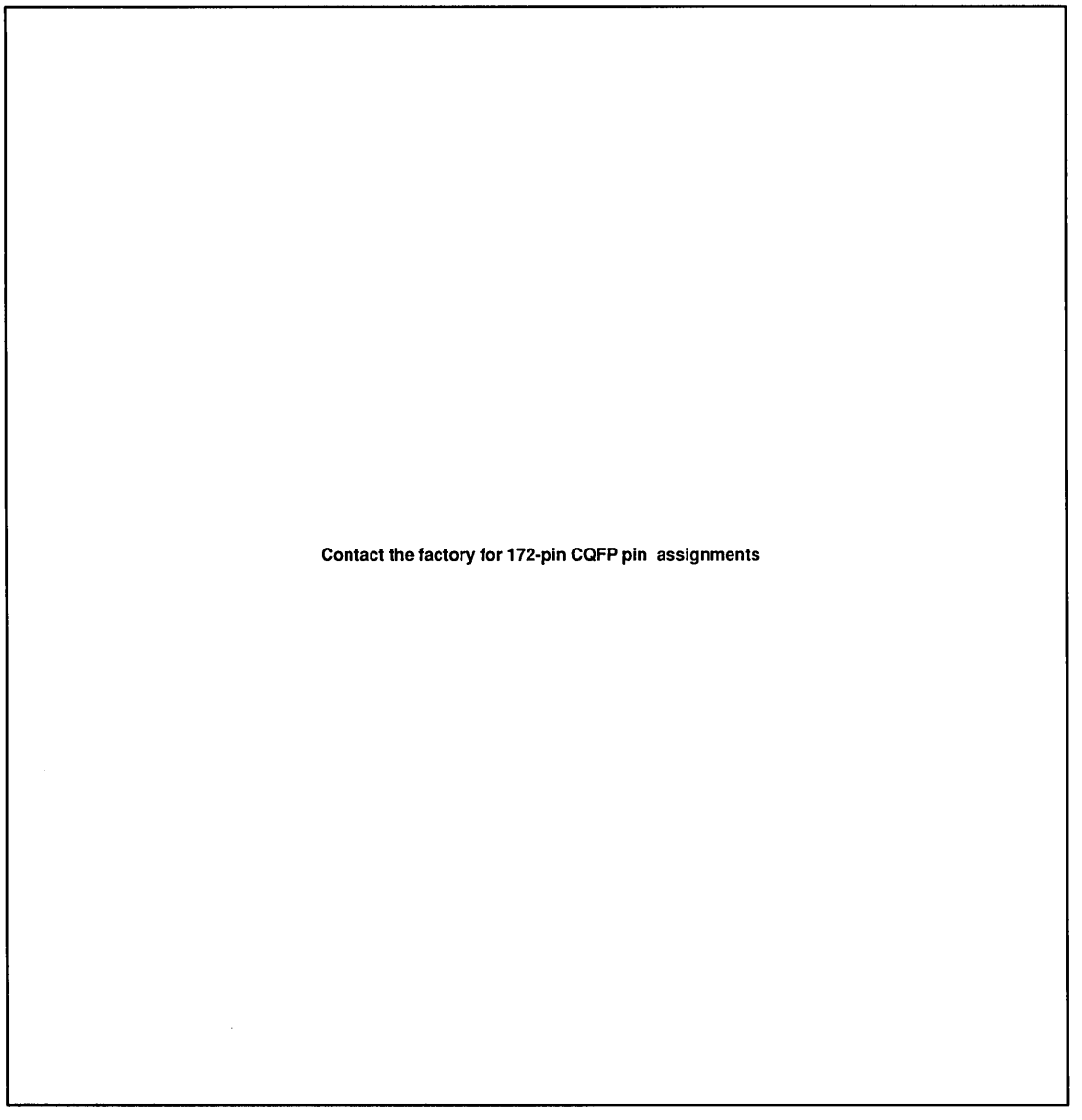
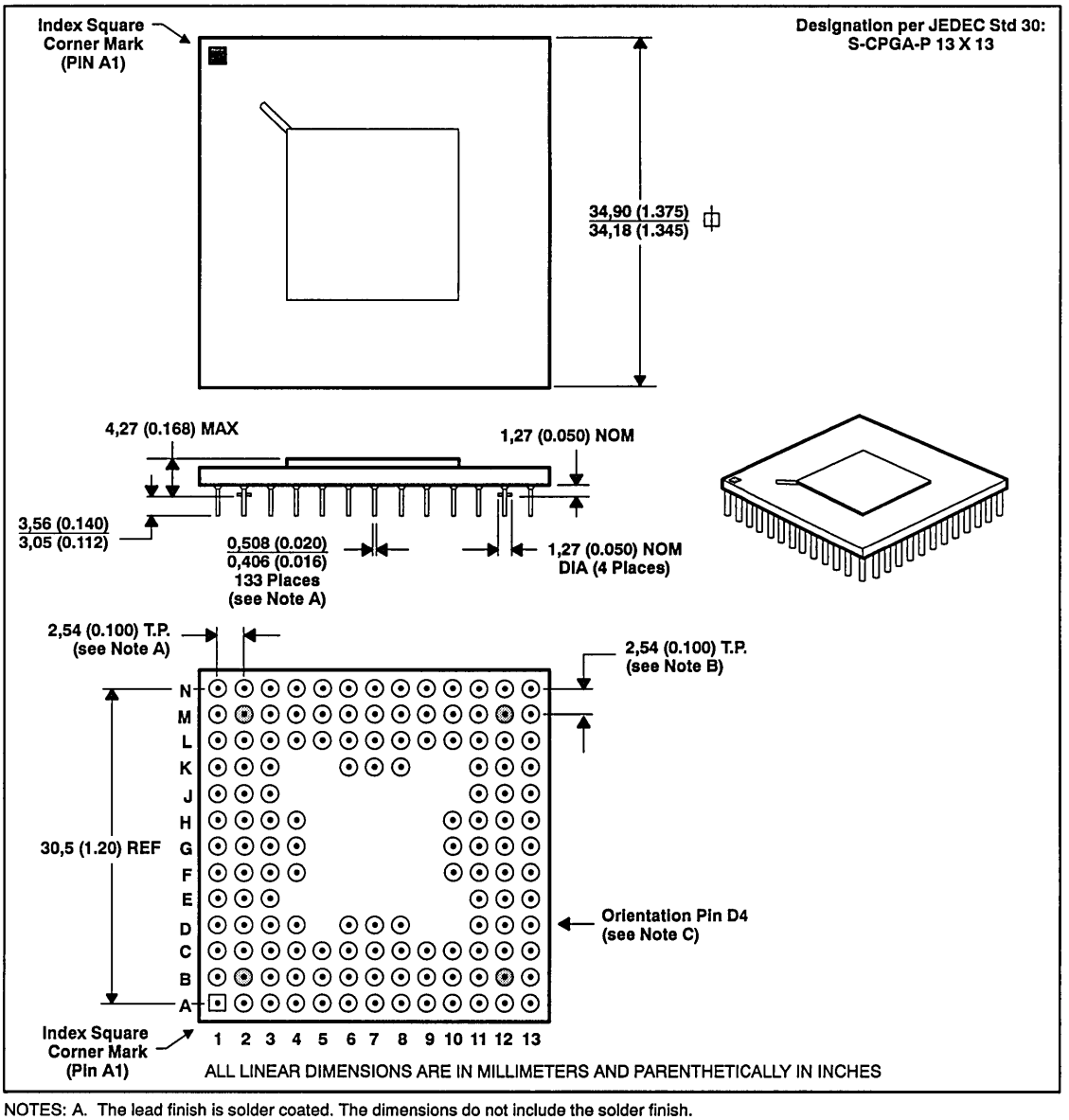


Figure 40. 172-Pin CQFP Pin Assignment

MECHANICAL DATA

133-Pin ceramic pin-grid-array package

This is a hermetically sealed ceramic package with metal cap and solder-coated pins.



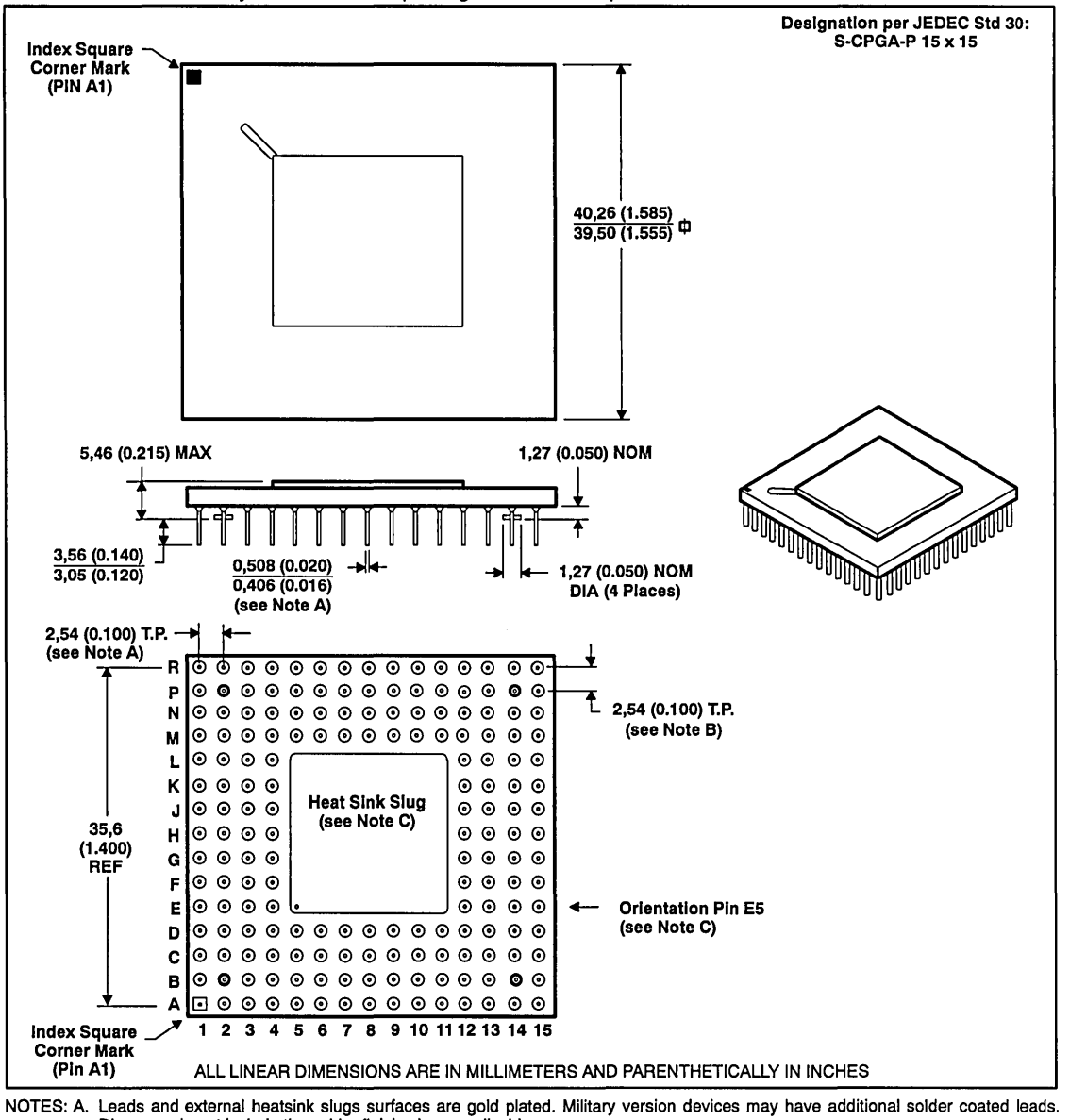
NOTES: A. The lead finish is solder coated. The dimensions do not include the solder finish.
B. Pin tips are located within 0,25 (0.010) diameter relative to each other at maximum material condition. Pin bases are located within 0,76 (0.030) diameter at maximum material condition relative to the center of the ceramic.
C. Orientation pin D4 is electrically isolated.

Figure 41. 133-Pin Ceramic Pin-Grid-Array Package

MECHANICAL DATA

176- and 177-pin ceramic pin-grid-array packages

This is a hermetically sealed ceramic package with metal cap.



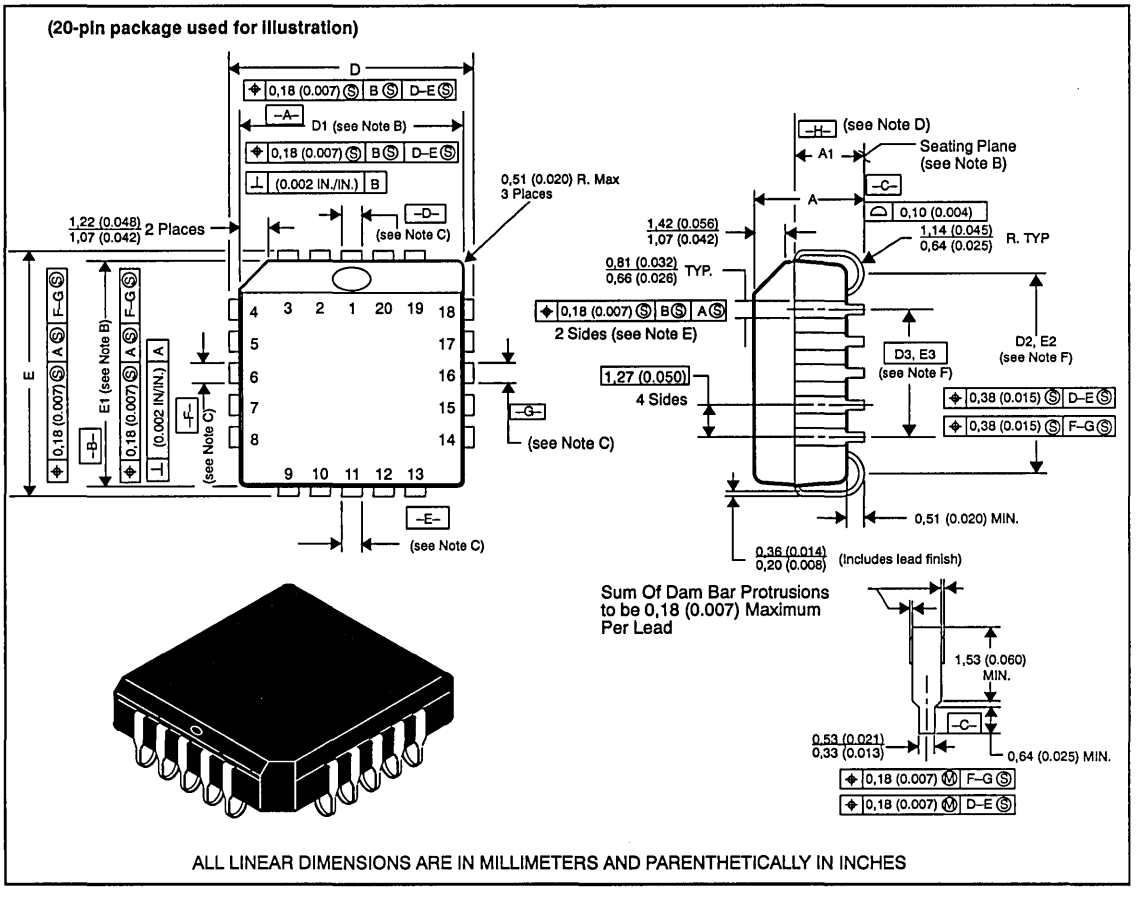
NOTES: A. Leads and external heatsink slugs surfaces are gold plated. Military version devices may have additional solder coated leads. Diagrams do not include the solder finish where applicable.

B. Pin tips are located within 0,25 (0.010) diameter relative to each other at maximum material condition. Pin bases are located within 0,76 (0.030) diameter at maximum material condition relative to the center of the ceramic.

C. Orientation pin E5 and the heat sink slug are at substrate ground. Pin E5 is available only for TPC1280GB-177.

Figure 42. 176- and 177-Pin Ceramic Pin-Grid-Array Packages

MECHANICAL DATA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

JEDEC OUTLINE	DIMS / PINS	A		A1		D, E		D1, E1		D2, E2		D3, E3 BASIC
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

B. Dimension D1 and E1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

Figure 43. Plastic Leaded Chip Carriers

MECHANICAL DATA

Contact the factory for 172-pin CQFP mechanical data.

Figure 44. 172-Pin Ceramic Quad Flat Package

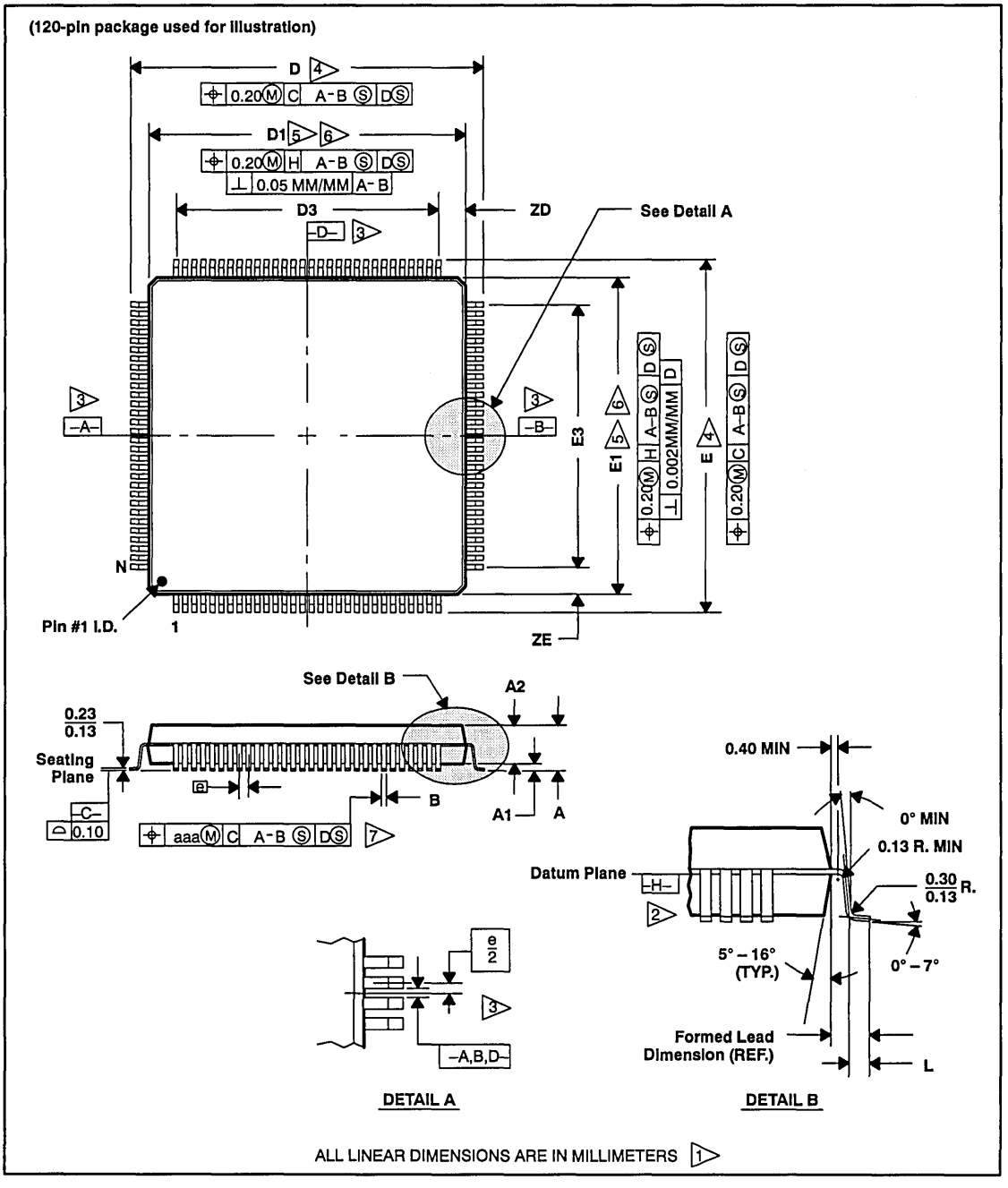


Figure 45. Plastic Quad Flat Packages

JEDEC OUTLINE	# PINS	PKG TYPE	A MAX	A1 MIN	A2 MAX MIN	D MAX MIN	D1 MAX MIN	D3 (REF)	ZD (REF)	E MAX MIN	E1 MAX MIN	E3 (REF)	ZE (REF)	L MAX MIN	e BASIC	B MAX MIN	aaa	ND	NE	FORMED LEAD DIM. (REF)
MO-108/CC-1	100	RECT	3,40	0,25	3,05 2,55	23,45 22,95	20,10 19,90	18,85	0,58	17,45 16,95	14,10 13,90	12,35	0,83	0,95 0,65	0,65	0,38 0,22	0,12	30	20	1,60
MO-108/DC-1	144	Square	4,07	0,25	3,67 3,17	31,45 30,95	28,10 27,90	22,75	2,63	31,45 30,95	28,10 27,90	22,75	2,63	0,95 0,65	0,65	0,38 0,22	0,12	36	36	1,60
MO-112/DD-1	160	Square	4,07	0,25	3,67 3,17	32,15 31,65	28,10 27,90	25,35	1,33	32,15 31,65	28,10 27,90	25,35	1,33	0,95 0,65	0,65	0,38 0,22	0,12	40	40	1,95

NOTES:

1. All dimensions are millimeters (mm), and the 100- and 144-pin packages conform to JEDEC specification MO-108 (issue A/October 1990), and the 160-pin package conforms to JEDEC specification MO-112 (issue A/August 1990). Dimensions and tolerancing per ANSI Y14.5M-1982.
2. Datum plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and –D– for center leads are determined at datum –H–.
4. Determined at seating plane –C–
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane –H–.
6. Determined at datum plane –H–
7. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. A minimum solder finish thickness of 0.0051 is guaranteed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Following are the pin loadings for the TPC12 Series 1.2-µm and 1.0-µm CMOS Field-Programmable Gate Arrays. Use this with the TPC12 Series Data Sheet and the Critical Path Analysis for FPGAs application report located in the Applications Chapter in this manual, to estimate manually the achievable system speed for a design implemented in a TI TPC12 Series FPGA. The index below will help you find the desired item in this supplement.

Name	Page	Table	Name	Page	Table	Name	Page	Table
DLMA	2-155	54	MCMPC2	2-158	73	OAI1	2-149	11
DLME1A	2-155	54	MCMPC4	2-158	73	OAI2A	2-149	11
DLM3	2-155	55	MCMPC8	2-158	73	OAI3	2-149	11
DLM3A	2-155	55	MX16	2-151	27	OAI3A	2-149	11
DLM4	2-155	55	MX2	2-151	21	OBDLHS	2-150	18
DLM4A	2-155	55	MX2A	2-151	21	OBHS	2-150	15
DLM8	2-155	56	MX2B	2-151	21	OR2	2-146	1
DLP1	2-154	50	MX2C	2-151	21	OR2A	2-146	1
DLP1A	2-154	50	MX4	2-151	23	OR2B	2-146	1
DLP1B	2-154	50	MX8	2-151	26	OR3	2-146	2
DLP1C	2-154	50	MX8A	2-151	26	OR3A	2-146	2
DLP1D	2-154	50	MXC1	2-151	25	OR3B	2-146	2
DLP1E	2-154	50	MXT	2-151	24	OR3C	2-146	2
FA1A	2-152	33	NAND2	2-146	1	OR4	2-147	3
FA1B	2-152	33	NAND2A	2-146	1	OR4A	2-147	3
FA2A	2-152	34	NAND2B	2-146	1	OR4B	2-147	3
FADD10	2-152	37	NAND3	2-146	2	OR4C	2-147	3
FADD12	2-153	38	NAND3A	2-146	2	OR4D	2-147	3
FADD16	2-153	39	NAND3B	2-146	2	OR5B	2-147	4
FADD8	2-152	35	NAND3C	2-146	2	ORH	2-154	46
FADD9	2-152	36	NAND4	2-147	3	ORIH	2-150	19
FCTD16C	2-153	42	NAND4A	2-147	3	ORITH	2-150	19
FCTD8A	2-153	43	NAND4B	2-147	3	ORTH	2-150	19
FCTD8B	2-153	43	NAND4C	2-147	3	OUTBUF	2-150	14
FCTU16C	2-153	44	NAND4D	2-147	3	SMULT8	2-160	92
FCTU8A	2-150	20	NAND5C	2-147	4	SREG4A	2-160	88
FCTU8B	2-150	20	NOR2	2-146	1	SREG8A	2-160	88
GAND2	2-157	68	NOR2A	2-146	1	TA00	2-146	1
GMX4	2-158	69	NOR2B	2-146	1	TA02	2-146	1
GNAND2	2-157	68	NOR3	2-146	2	TA04	2-149	13
GNOR2	2-157	68	NOR3A	2-146	2	TA07	2-149	13
GOR2	2-157	68	NOR3B	2-146	2	TA08	2-146	1
GXOR2	2-157	68	NOR3C	2-146	2	TA10	2-146	2
HA1	2-152	32	NOR4	2-147	3	TA11	2-146	2
HA1A	2-152	32	NOR4A	2-147	3	TA20	2-147	3
HA1B	2-152	32	NOR4B	2-147	3	TA21	2-147	3
HA1C	2-152	32	NOR4C	2-147	3	TA27	2-146	2
IBDL	2-150	16	NOR4D	2-147	3	TA32	2-146	1
ICMP4	2-158	71	NOR5C	2-147	4	TA40	2-147	3
ICMP8	2-158	71	OA1	2-149	11	TA42	2-160	86
INBUF	2-150	14	OA1A	2-149	11	TA51	2-149	11
INV	2-149	13	OA1B	2-149	11	TA54	2-149	12
INVA	2-149	13	OA1C	2-149	11	TA55	2-149	12
IR	2-153	45	OA2	2-149	11	TA86	2-147	5
JKF	2-157	63	OA2A	2-149	11	TA138	2-159	85
JKF1B	2-157	63	OA3	2-149	11	TA139	2-159	84
JKF2A	2-157	63	OA3A	2-149	11	TA150	2-151	27
JKF2B	2-157	63	OA3B	2-149	11	TA151	2-151	28
JKF2C	2-157	63	OA4	2-149	11	TA153	2-152	29
JKF2D	2-157	63	OA4A	2-149	11	TA154	2-152	30
MAJ3	2-148	9	OA5	2-149	11	TA157	2-152	31

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TA164	2-160	89
TA169	2-158	77
TA174	2-159	78
TA175	2-159	79
TA190	2-159	80
TA191	2-159	81
TA194	2-160	90
TA195	2-160	91
TA269	2-159	82
TA273	2-158	70
TA280	2-158	74
TA377	2-158	70
TA688	2-158	72
TBDLHS	2-152	18
TBHS	2-152	15
TF1A	2-157	67
TF1B	2-157	67
TRIBUFF	2-150	14
UDCNT4A	2-159	83
VAD16C	2-160	93
VADC16C	2-161	94
VCTD16C	2-161	95
VCTD2CP	2-161	96
VCTD2CU	2-161	97
VCTD4CL	2-161	98
VCTD4CM	2-161	99
XA1	2-148	7
XA1A	2-148	7
XNOR	2-147	5
XO1	2-147	6
XO1A	2-147	6
XOR	2-147	5

Table 1. 2-Input Gates

	A	B	Y
AND2	1	1	0
AND2A	1	1	0
AND2B	1	1	0
NAND2	1	1	0
NAND2A	1	1	0
NAND2B	1	1	0
OR2	1	1	0
OR2A	1	1	0
OR2B	1	1	0
NOR2	1	1	0
NOR2A	1	1	0
NOR2B	1	1	0
TA00	1	1	0
TA02	1	1	0
TA08	1	1	0
TA32	1	1	0

Table 2. 3-Input Gates

	A	B	C	Y
AND3	1	1	1	0
AND3A	1	1	1	0
AND3B	1	1	1	0
AND3C	1	1	1	0
NAND3	1	1	1	0
NAND3A	1	1	1	0
NAND3B	1	1	1	0
NAND3C	1	1	1	0
OR3	1	1	1	0
OR3A	1	1	1	0
OR3B	1	1	1	0
OR3C	1	1	1	0
NOR3	1	1	1	0
NOR3A	1	1	1	0
NOR3B	1	1	1	0
NOR3C	1	1	1	0
TA10	1	1	1	0
TA11	1	1	1	0
TA27	1	1	1	0

Table 3. 4-Input Gates

	A	B	C	D	Y
AND4	1	1	1	1	0
AND4A	1	1	1	1	0
AND4B	1	1	1	1	0
AND4C	1	1	1	1	0
AND4D	1	1	1	1	0
NAND4	1	1	1	1	0
NAND4A	1	1	1	1	0
NAND4B	1	1	1	1	0
NAND4C	1	1	1	1	0
NAND4D	1	1	1	1	0
OR4	1	1	1	1	0
OR4A	1	1	1	1	0
OR4B	1	1	1	1	0
OR4C	1	1	1	1	0
OR4D	1	1	1	1	0
NOR4	1	1	1	1	0
NOR4A	1	1	1	1	0
NOR4B	1	1	1	1	0
NOR4C	1	1	1	1	0
NOR4D	1	1	1	1	0
TA20	1	1	1	1	0
TA21	1	1	1	1	0
TA40	1	1	1	1	0

Table 4. 5-Input Gates

	A	B	C	D	E	Y
AND5B	1	1	1	1	1	0
NAND5C	1	1	1	1	1	0
NOR5C	1	1	1	1	1	0
OR5B	1	1	1	1	1	0

Table 5. XNOR/XOR Gates

	A	B	Y
XNOR	1	1	0
XOR	1	1	0
TA86	1	1	0

Table 6. XOR-OR/XNOR-OR Gates

	A	B	C	Y
XO1	1	1	2	0
XO1A	1	1	2	0

Table 7. XOR-AND/XNOR-AND Gates

	A	B	C	Y
XA1	1	1	2	0
XA1A	1	1	2	0

Table 8. AND-XOR/AND-XNOR Gates

	A	B	C	Y
AX1	2	1	2	0
AX1A	1	1	1	0
AX1B	1	1	1	0
AX1C	1	1	1	0

Table 9. AND-OR/AND-NOR Gates

	A	B	C	D	Y
AO1	1	1	1	NA	0
AO1A	1	1	1	NA	0
AO1B	1	1	1	NA	0
AO1C	1	1	1	NA	0
AO1D	1	1	2	NA	0
AO1E	1	1	1	NA	0
AO2	1	1	1	1	0
AO2A	1	1	1	1	0
AO2B	1	1	1	1	0
AO2C	1	1	1	2	0
AO2D	1	1	1	1	0
AO2E	1	1	1	1	0
AO3	1	1	1	2	0
AO3A	1	1	1	2	0
AO3B	1	1	1	2	0
AO3C	1	1	1	2	0
AO4A	1	1	1	1	0
AO5A	1	1	1	1	0
AO6	1	1	1	1	0
AO6A	1	1	1	1	0
AOI1	1	1	1	NA	0
AOI1A	1	1	1	NA	0
AOI1B	1	1	2	NA	0
AOI1C	1	1	1	NA	0
AOI1D	1	1	1	NA	0
AOI2A	1	1	1	1	0
AOI2B	1	1	2	1	0
AOI3A	2	1	1	1	0
AOI4	1	1	1	1	0
AOI4A	1	1	1	1	0
MAJ3	2	2	2	NA	0

Table 10. AND-OR/AND-NOR Gates

	A	B	C	D	E	Y
AO7	1	1	1	1	1	0
AO8	1	1	1	1	1	0
AO9	1	1	1	1	1	0
AO10	1	1	1	1	1	0
AO11	2	2	2	NA	NA	0

Table 11. OR-AND/OR-NAND Gates

	A	B	C	D	Y
OA1	1	1	1	NA	0
OA1A	1	1	2	NA	0
OA1B	1	1	1	NA	0
OA1C	1	1	1	NA	0
OA2	1	1	1	1	0
OA2A	1	1	1	1	0
OA3	1	1	1	1	0
OA3A	1	1	1	2	0
OA3B	1	1	1	2	0
OA4	1	1	1	2	0
OA4A	1	1	1	2	0
OA5	2	1	1	1	0
OAI1	1	1	1	NA	0
OAI2A	1	1	1	2	0
OAI3	1	1	1	1	0
OAI3A	1	1	1	1	0
TA51	1	1	1	1	0

Table 12. OR-AND/OR-NAND Gates

	A	B	C	D	E	F	G	H	Y
TA54	1	1	1	1	1	1	1	1	0
TA55	1	1	1	1	1	1	1	1	0

Table 13. Buffers

	A	Y2.
BUF	1	0
BUFA	1	0
CLKINT	1	0
INV	1	0
INVA	1	0
TA04	1	0
TA07	1	0

Table 14. I/O Buffers

	D	E	Y
INBUF	NA	NA	0
CLKBUF	NA	NA	0
OUTBUF	1	NA	0
TRIBUFF	1	1	0
BIBUF	1	1	0
CLKBIBUF	1	1	0

Table 15. High-Slew Output Buffers

	D	E	Y
BBHS	1	1	0
OBHS	1	NA	0
TBHS	1	1	0

Table 16. Input Buffer with Latch

	G	Q
IBDL	1	0

Table 17. High-Slew Output Buffer with Latch

	GIN	GOUT	D	E	Q
BBDLHS	1	1	1	1	0

Table 18. High-Slew Output Buffers with Latches

	D	E	G	Y
OBDLHS	1	NA	1	0
TBDLHS	1	1	1	0

Table 19. High-Slew, Firm Output Registers

	CLK	D	E	PAD
ORIH	2	1	NA	0
ORITH	2	1	1	0
ORTH	2	1	1	0

Table 20. Fast 8-Bit Up Counters, Parallel Loadable

	CE	CLK	CLR	D7	D6	D5	D4	D3	D2	D1	D0	LD	TE	T0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
FCTU8A	11	10	10	3	3	3	3	4	4	4	4	11	NA	1	3	3	4	5	4	4	5	6
FCTU8B	9	9	9	2	2	2	2	3	3	3	3	9	2	NA	2	2	3	4	3	3	4	5

Table 21. 2:1 Multiplexers

	A	B	S	Y
MX2	1	1	1	0
MX2A	1	1	2	0
MX2B	1	1	2	0
MX2C	1	1	2	0

Table 22. Multiplexer

	D0	D1	D2	D3	S00	S01	S10	S11	Y
CM8	1	1	1	1	1	1	1	1	0

Table 23. 4:1 Multiplexer

	D0	D1	D2	D3	S1	S0	Y
MX4	1	1	1	1	1	1	0

Table 24. 4:1 Multiplexer

	D0	D1	D2	D3	S0A	S0B	S1	Y
MXT	1	1	1	1	1	1	1	0

Table 25. Other Multiplexer

	S	A	B	C	D	Y
MXC1	1	1	1	1	1	0

Table 26. 8:1 Multiplexer

	S2	S1	S0	D0–D7	Y
MX8	1	2	2	1	0
MX8A	2	2	2	1	0

Table 27. 16:1 Multiplexer

	S3/D	S2/C	S1/B	S0/A	D0–D15	EN	Y/W
MX16	1	1	4	4	1	NA	0
TA150	1	1	4	4	1	1	0

Table 28. 8:1 Multiplexer

	A	B	C	EN	D0–D7	Y	W
TA151	2	2	1	2	1	0	0

Table 29. 4:1 Multiplexer

	A	B	EN	C0	C1	C2	C3	Y
TA153	1	1	1	1	1	1	1	0

Table 30. 4-to-16 Decoder/Demultiplexer

	A	B	C	D	G1	G2	Y0–15
TA154	9	10	8	9	2	2	0

Table 31. 2:1 Multiplexer

	A	B	S	EN	Y
TA157	1	1	1	1	0

Table 32. Half Adders

	A	B	CO	S
HA1	2	2	0	0
HA1A	2	2	0	0
HA1B	2	2	0	0
HA1C	2	2	0	0

Table 33. Full Adders

	A	B	CI	CO	S
FA1A	3	3	3	2	0
FA1B	2	3	3	2	0

Table 34. Full Adder

	A0	A1	B	CI	CO	S
FA2A	2	2	3	3	2	0

Table 35. 8-Bit Fast Adder

	A0	A1	A2, A4, A6	A3, A5, A7	B0	B1	B2, B4, B6	B3, B5, B7	S0–S7	CO
FADD8	3	4	6	8	4	5	8	10	0	0

Table 36. 9-Bit Fast Adder

	A0	A1, A8	A2, A4, A6	A3, A5, A7	B0	B1	B2, B4, B6	B3, B5, B7	B8	S0–S8	CO
FADD9	3	4	6	8	4	5	8	10	6	0	0

Table 37. 10-Bit Fast Adder

	A0	A1	A2, A4, A6, A8	A3, A5, A7, A9	B0	B1	B2, B4, B6, B8	B3, B5, B7, B9	S0–S9	CO
FADD10	3	4	6	8	4	5	8	10	0	0

Table 38. 12-Bit Fast Adder

	A0	A1	A2, A4, A6, A8, A10	A3, A5, A7, A9, A11	B0	B1	B2, B4, B6, B8, B10	B3, B5, B7, B9, B11	S0–S11	CO
FADD12	3	4	6	8	4	5	8	10	0	0

Table 39. 16-Bit Fast Adder

	A0	A1	A2, A4, A7, A10, A13	A3, A5, A6, A8, A9, A11, A12, A14, A15	B0	B1	B2, B4, B7, B10, B13	B3, B5, B6, B8, B9, B11, B12, B14, B15	S0–S15	CO
FADD16	3	4	6	8	4	5	8	10	0	0

Table 40. Boolean

	A	B	C	D	E	Y
CS1	1	1	1	2	1	0
CS2	1	1	2	1	1	0

Table 41. Boolean

	A0	A1	B0	B1	Y
CY2A	1	2	1	2	0
CY2B	1	2	1	2	0

Table 42. Fast 16-Bit Down Counter, Parallel Loadable

FCTD16C INPUTS	CE1	CE2	CLK	CLR	LD1	LD2	D15–D12	D11–D4	D3–D0
	9	3	19	2	11	9	2	3	4

FCTD16C OUTPUTS	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
	2	3	4	4	3	4	5	5	3	4	5	4	4	4	5	6

Table 43. Fast 8-Bit Down Counters, Parallel Loadable

	CE	CLK	CLR	D7	D6	D5	D4	D3	D2	D1	D0	LD	TE	TO	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
FCTD8A	9	10	10	3	3	3	3	4	4	4	4	11	NA	1	3	4	5	4	4	4	5	6
FCTD8B	3	9	9	2	2	2	2	3	3	3	3	9	3	NA	2	3	4	4	3	4	5	5

Table 44. Fast 16-Bit Up Counter, Parallel Loadable

FCTU16C INPUTS	CE1	CE2	CLK	CLR	LD1	LD2	D15–D12	D11–D4	D3–D0
	11	9	19	2	11	9	2	3	4

FCTU16C OUTPUTS	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
	2	2	3	4	3	3	4	5	3	3	4	5	4	4	5	6

Table 45. Firm Input Register

	CLK	PAD	Q
IR	2	0	0

Table 46. Firm Output Register, High Slew

	CLK	D	PAD
ORH	2	1	0

Table 47. D-Type Latches

	D	G	Q/QN
DL1	1	1	0
DL1A	1	1	0
DL1B	1	1	0
DL1C	1	1	0

Table 48. D-Type Latches with Clear

	D	G	CLR	Q
DLC	1	1	1	0
DLCA	1	1	1	0
DLC1	1	1	1	1
DLC1A	1	1	1	1
DLC1F	1	1	2	1
DLC1G	1	1	1	1

Table 49. D-Type Latch with Clear

	G	CLR	D0–D7	Q0–Q7
DLC8A	8	8	1	0

Table 50. D-Type Latches with Preset

	D	G	PRE	Q
DLP1	1	1	1	1
DLP1A	1	1	1	1
DLP1B	1	1	1	1
DLP1C	1	1	1	1
DLP1D	1	1	1	0
DLP1E	1	1	1	0

Table 51. D-Type Latches with Enable

	D	E	G	Q
DLE	1	1	1	1
DLEA	1	1	1	1
DLEB	1	1	1	1
DLEC	1	1	1	1
DLE1D	1	1	1	1

Table 52. D-Type Latches with Enable, Clear, and Preset

	D	E	G	PRE	CLR	Q
DLE2B	1	1	1	NA	1	1
DLE2C	1	1	1	NA	1	1
DLE3B	1	1	1	1	NA	1
DLE3C	1	1	1	1	NA	1

Table 53. D-Type Latch with Enable

	G	E	D0–D7	Q0–Q7
DLE8	8	8	1	2

Table 54. D-Type Latches with Multiplexed Inputs

	A	B	S	E	G	Q	CLR
DLM	1	1	1	NA	1	0	NA
DLMA	1	1	1	NA	1	0	NA
DLME1A	1	1	1	2	1	2	NA

Table 55. D-Type Latches

	D0–D3	S0	S1	S10	S11	G	Q
DLM3	1	1	1	NA	NA	1	0
DLM3A	1	1	1	NA	NA	1	0
DLM4	1	1	NA	1	1	1	0
DLM4A	1	1	NA	1	1	1	0

Table 56. D-Type Latch with Multiplexed Inputs

	G	S	A0–A7	B0–B7	Q0–Q7
DLM8	8	8	1	1	0

Table 57. D-Type Flip-Flops

	D	CLK	Q/QN
DF1	1	1	0
DF1A	1	1	0
DF1B	1	1	0
DF1C	1	1	0

Table 58. D-Type Flip-Flops with Clear

	D	CLK	CLR	Q/QN
DFC1	1	1	1	0
DFC1A	1	1	1	0
DFC1B	1	1	1	0
DFC1D	1	1	1	0
DFC1E	1	1	1	0
DFC1G	1	1	1	0

Table 59. D-Type Flip-Flops with Preset

	D	CLK	PRE	Q/QN
DFP1	2	2	2	1
DFP1A	1	2	2	1
DFP1B	1	2	2	1
DFP1C	1	1	1	0
DFP1D	2	2	2	1
DFP1E	1	1	1	0
DFP1F	1	1	1	0
DFP1G	1	1	1	0

Table 60. D-Type Flip-Flops with Preset and Clear

	D	CLR	PRE	CLK	Q
DFPC	1	2	2	2	1
DFPCA	2	2	2	2	1

Table 61. D-Type Flip-Flops with Enable

	D	E	CLK	Q
DFE	1	1	1	1
DFEA	1	1	1	1
DFE1B	1	1	1	1
DFE1C	1	1	1	1

Table 62. D-Type Flip-Flops with Enable, Preset, and Clear

	D	E	CLR	PRE	CLK	Q
DFE3A	1	1	1	NA	1	1
DFE3B	1	1	1	NA	1	1
DFE3C	1	1	1	NA	1	1
DFE3D	1	1	1	NA	1	1

Table 63. J-K Flip-Flops

	J	K	CLR	CLK	Q
JKF	1	1	NA	1	1
JKF1B	1	1	NA	1	1
JKF2A	1	1	1	1	1
JKF2B	1	1	1	1	1
JKF2C	1	1	1	1	1
JKF2D	1	1	1	1	1

Table 64. Multiplexed-Input Flip-Flops

	A	B	S	CLR	E	CLK	Q
DFM	1	1	1	NA	NA	1	0
DFMA	1	1	1	NA	NA	1	0
DFMB	1	1	1	1	NA	1	0
DFME1A	1	1	1	NA	2	1	2
DFM1B	1	1	2	NA	NA	1	0
DFM1C	1	1	2	NA	NA	1	0
DFM3	1	1	1	1	NA	1	0
DFM3B	1	1	1	1	NA	1	0
DFM3E	1	1	1	1	NA	1	0

Table 65. Multiplexed-Input Flip-Flops with Preset

	A	B	S	PRE	CLK	Q
DFM4C	1	1	2	1	1	0
DFM4D	1	1	2	1	1	0

Table 66. Multiplexed-Input Flip-Flops

	D0–D3	S0	S1	S10	S11	CLR	CLK	Q
DFM6A	1	1	1	NA	NA	1	1	0
DFM6B	1	1	1	NA	NA	1	1	0
DFM7A	1	1	NA	1	1	1	1	0
DFM7B	1	1	NA	1	1	1	1	0

Table 67. Toggle Flip-Flops

	T	CLR	CLK	Q
TF1A	1	1	1	1
TF1B	1	1	1	1

Table 68. Clock Buffer (CLKBUF) Interface

	A	G	Y
GAND2	1	1	0
GNAND2	1	1	0
GOR2	1	1	0
GNOR2	1	1	0
GXOR2	1	1	0

Table 69. Clock Buffer (CLKBUF) Interface

	D0	D1	D2	D3	G	S0	Y
GMX4	1	1	1	1	1	1	0

Table 70. Octal D-Type Flip-Flops and Registers

	CLK	CLR	EN	D1–D8	Q1–Q8
TA273	8	8	NA	1	0
TA377	8	NA	8	1	1

Table 71. Identity Comparators

	An	Bn	AEB
ICMP4	1	1	0
ICMP8	1	1	0

Table 72. 8-Bit Identity Comparator

	G	P7:0	Q7:0	PEQ
TA688	1	1	1	0

Table 73. Magnitude Comparators

	An	Bn	ALBI	AEBI	AGBI	ALB	AEB	AGB
MCMPC2	3	3	1	1	1	0	0	0
MCMPC4	3	3	1	1	1	0	0	0
MCMPC8	3	3	1	1	1	0	0	0

Table 74. Parity Checker

	A	B	C	D	E	F	G	H	I	ODD	EVEN
TA280	1	1	1	1	1	1	1	1	1	0	0

Table 75. Binary Counters

	CLR	CLK	LD	CI	P0–P3	Q0	Q1	Q2	Q3	CO
CNT4A	4	4	4	5	1	5	4	4	3	0
CNT4B	4	4	4	9	1	5	4	3	3	0

Table 76. Decade Counter with Active Low Clear and Load

	A	B	C	CLK	CLR	D	ENP	ENT	LD	QA	QB	QC	QD	RCO
TA160	2	2	2	4	4	2	2	3	4	7	6	4	6	0

Table 77. Synchronous Counters

	LD	UD	ENT	ENP	CLR	CLK	A	B	C	D	QA	QB	QC	QD	RCO
TA161	4	NA	2	1	4	4	2	2	2	2	4	3	3	3	0
TA169	4	5	3	3	NA	8	1	1	1	1	6	6	4	4	0

Table 78. Hex D-Type Flip-Flop with Active Low Clear

	CLK	CLR	D1–6	Q1–6
TA174	6	6	1	0

Table 79. Quadruple D-Type Flip-Flop with Active Low Clear

	CLK	CLR	D1–4	Q1–4
TA175	4	4	1	0

Table 80. 4-Bit Up/Down Decade Counter with Up/Down Mode

	A-D	CLK	CTEN	DU	LOAD	MM	QA	QB	QC	QD	RCO
TA190	1	5	5	10	4	1	12	10	10	12	0

Table 81. 4-Bit Up/Down Binary Counter with Up/Down Mode and Synchronous Load†

	A–D	CLK	CTEN	DU	LOAD	MM	QA	QB	QC	QD	RCO
TA191	1	5	5	12	4	1	11	10	11	10	0

† Note: The TTL function, 74191, has an asynchronous load.

Table 82. Synchronous Counter

	CLK	LD	UD	ENP	ENT	A–H	QC, QD, QG, QH	QA,QB,QE,QF	RCO
TA269	8	8	1	3	3	1	4	6	0

Table 83. Synchronous Counter

	LD	UD	CI	CLK	P0–P3	Q0,Q1	Q2	Q3	CO
UDCNT4A	4	5	9	4	1	6	4	4	0

Table 84. 2-to-4 Decoders

	A	B	E/EN	Y0–Y3
DEC2X4	4	4	NA	0
DEC2X4A	4	4	NA	0
DECE2X4	4	4	4	0
DECE2X4A	4	4	4	0
TA139	4	4	4	0

Table 85. 3-to-8 Decoders

	A	B	C	E	G1	G2A	G2B	Y0–77
DEC3X8	8	8	8	NA	NA	NA	NA	0
DEC3X8A	8	8	8	NA	NA	NA	NA	0
DECE3X8	5	5	5	8	NA	NA	NA	0
DECE3X8A	5	5	5	8	NA	NA	NA	0
TA138	5	5	5	NA	1	1	1	0

Table 86. 4-to-10 Decoder

	A	B	C	D	Y0–Y9
TA42	10	10	10	10	0

Table 87. 4-to-16 Decoder

	A	B	C	D	Y0–Y15
DEC4X16A	9	9	9	9	0

Table 88. Shift Registers

	CLK	CLR	SHLD	SI	Pn	SO
SREG4A	4	4	4	1	1	0
SREG8A	8	8	8	1	1	0

Table 89. Shift Register

	CLK	CLR	A	B	QA	QB	QC	QD	QE	QF	QG	QH
TA164	8	8	1	1	1	1	1	1	1	1	1	0

Table 90. Shift Register

	CLK	CLR	S1	S0	SLSI	SRSI	A	B	C	D	QA	QB	QC	QD
TA194	4	4	4	4	1	1	1	1	1	1	2	2	2	2

Table 91. Shift Register

	CLK	CLR	J	K	SHLD	A	B	C	D	QA	QB	QC	QD	QDN
TA195	4	4	1	1	4	2	1	1	1	2	1	1	1	0

Table 92. 8-Bit by 8-Bit Multiplier

	A0-A2, A4-A6	A3	A7	B0,B4	B1–B3, B5–B7	P0–P15
SMULT8	6	9	14	8	4	0

Table 93. Very Fast 16-Bit Adder

	A15	A14,A12–A6, A3,A2	A13,A5,A4, A1,A0	B15	B14,B12–B6, B3,B2	B13,B5,B4, B1,B0	S15–S0	CO
VAD16C	4	6	5	4	6	5	0	0

Table 94. Very Fast 16-Bit Adder with Carry In

	CIN	A15	A14,A12–A6, A3,A2	A13,A5,A4, A1,A0	B15	B14,B12–B6, B3,B2	B13,B5,B4, B1,B0	S15–S0	CO
VADC16C	5	4	6	5	4	6	5	0	0

Table 95. Fast 16-Bit Down Counter, Parallel Loadable

VCTD16C INPUTS	CLK	COUNT	LOAD	RESET	D15–D2	D1–D0
	34	1	1	1	2	1

VCTD16C OUTPUTS	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
	2	3	3	4	5	6	3	4	5	6	3	4	5	6	4	4

Table 96. 2-Bit Down Counter, Prescaler, Delay After Load, use to build VCTD Counters

	CLEAR	CLK	COUNT	LOAD	P0	P1	LD	CLR	CNT	Q0	Q1
VCTD2CP	1	5	2	1	2	2	2	2	2	2	2

Table 97. 2-Bit Down Counter, Upper Bits, Delay After Load, use to build VCTD Counters

	CI	CLK	CLR	CNT	CT0	CT1	LD	P0	P1	Q0	Q1
VCTD2CU	2	2	2	2	2	2	2	2	2	3	2

Table 98. 4-Bit Down Counter, Lower Bits, Delay After Load, use to build VCTD Counters

	CLK	CLR	CNT	CT0	CT1	LD	P0	P1	P2	P3	CO	Q0	Q1	Q2	Q3
VCTD4CL	4	4	4	4	4	4	2	2	2	2	0	6	5	4	3

Table 99. 4-Bit Down Counter, Middle Bits, Delay After Load, use to build VCTD Counters

	CI	CLK	CLR	CNT	CT0	CT1	LD	P0	P1	P2	P3	CO	Q0	Q1	Q2	Q3
VCTD4CM	4	4	4	4	4	4	4	2	2	2	2	0	6	5	4	3

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- **Gate Capacities from < 1,000 to > 10,000 Gate Array Gates**
- **Gate Capacities from < 2,500 to > 25,000 PLD/LCA™ Equivalent Gates**
- **Replace from 30 to 340 TTL Packages**
- **User I/Os from < 100 to > 200**
- **I/O Performance of 10 ns Clock-to-Out**
- **16-Bit Counter Performance in Excess of 125 MHz**
- **System-Level Performance to 75 MHz**
- **Single-Module Sequential Functions**
- **Wide-Input Combinatorial Functions**
- **Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz**
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description

The TPC14 Series, with devices spanning capacities from less than 1,000 gates to more than 10,000 gates, represents TI's third generation of field-programmable gate arrays (FPGAs). The TPC14 Series provides a group of high-performance system solutions, delivering 16-bit counter designs in excess of 125 MHz operation, and reporting system performance of up to 75 MHz operation. The TPC14 Series offers an abundance of I/Os ranging from less than 100 pins to over 200 pins. The devices are implemented in a silicon-gate, 0.8-µm, scaled double-metal CMOS process using antifuse technology. Implemented in a channeled array architecture, the TPC14 Series provides significant enhancements in gate density and performance while maintaining upward compatibility with the TPC10 and TPC12 Series design environments.

TPC14 Series devices are designed to meet two primary logic integration requirements: high speed and high user I/O. TPC14 Series provides the highest-performance, general-purpose programmable solution available, and the unprecedented design flexibility of the highest pin-to-pin gate ratios available. The high performance of the TPC14 Series has been achieved through evolutionary enhancements in TI's proven two-module general-purpose FPGA architecture. These enhancements include four high-speed clock distribution networks and 10-ns clock-to-out I/O modules. The two-module architecture consists of combinatorial and combinatorial-sequential modules. A diagram of the TPC14 Series architecture is shown in Figure 1.

The TPC14 Series is supported by the TI Action Logic™ System (TI-ALS), which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug and diagnostic probe capabilities. The TI-ALS is available on Sun™, HP/Apollo™ workstations, and on 386/486 PC platforms.

PRODUCT PREVIEW

Product Family Profile

DEVICE	FROM	TO
Capacity		
Gate array equivalent gates	< 1,000	> 10,000
PLD/LCA equivalent gates	< 2,500	> 25,000
TTL equivalent packages	30	340
User I/Os	< 100	> 200
Performance		
System speed		75 MHz
16-bit counters		> 125 MHz
CMOS Process	0.8-µm double-metal CMOS	

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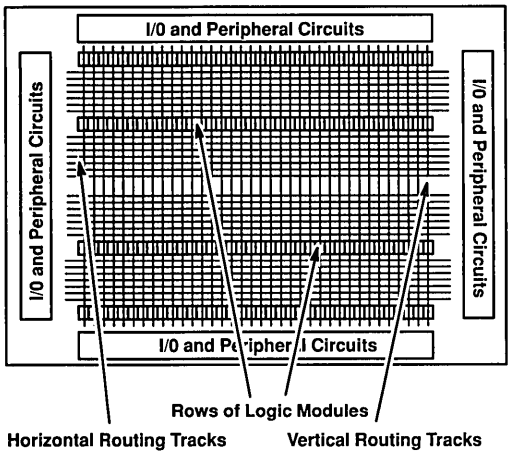


Figure 1. Diagram of TPC14 Series Architecture

TPC14 architecture

The TPC14 Series architecture is an evolutionary upgrade from the TPC12 Series. After extensive research into alternate logic module architectures, The TPC12 Series two-module design was found to be optimal for many applications. The small, simple structure of the logic modules has been retained, with a single enhancement to the sequential logic module. These numerous, general-purpose logic modules constitute a design architecture that provides a high-performance solution for a wide range of applications.

The I/O module is enhanced significantly, allowing more complex logic functions to be implemented in the I/O module. This significantly increases performance of key device parameters, like clock-to-output. Clocking flexibility is also enhanced over the TPC12 Series with the inclusion of two dedicated clocks. A block diagram of the TPC14 Series architecture is shown in Figure 2.

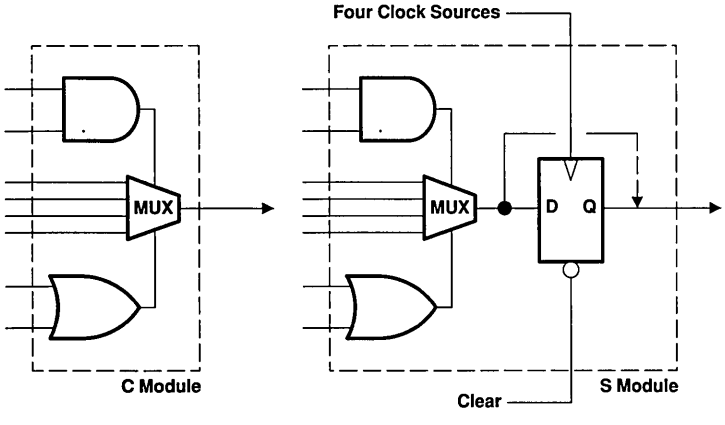


Figure 2. TPC14 Series Logic Modules

TPC14 architecture (continued)

two-module design

TPC14 Series architecture uses the proven multiplexer-based combinatorial module (C-module) of TPC12 Series devices, and an enhanced version of the TPC12 Series multiplexer-based combinatorial-sequential module (S-module). The TPC14 Series S-module combinatorial logic preceding the register is equivalent to the combinatorial logic within the C-module. This allows for more complex logic functions to be implemented in a single level of logic and makes logic synthesis more efficient due to the regular combinatorial structure throughout the device.

interconnect routing using the antifuse

Interconnections between logic modules are made using antifuses. The interconnections use a segmented wiring channel similar to channeled gate arrays. The horizontal and vertical channel segments vary in length, and are tuned to allow automatic place and route of the most interconnect-intensive applications. All speed-critical module-to-module connections are accomplished with only two low-resistance antifuse elements. Most connections are implemented with either two or three antifuse elements. No connections require more than four antifuse elements in a path.

I/O module

The TPC14 Series I/O module provides a significant enhancement over the TPC12 Series latch-based I/O module. The TPC14 Series I/O module contains input and output registers and a register hold function that allows selective updating of the I/O module register. The registers can be used for more complex logic functions in addition to simple timing functions. In particular, microprocessor-based systems will benefit from the selective update capability of the TPC14 Series I/O module. A variety of feedback options on the I/O module allows registered outputs, registered inputs, or direct inputs to be selected as input to the array. Each I/O module contains a slew-control feature, which allows output rise and fall times to be tailored to the particular application. The block diagram for the TPC14 Series I/O module is shown in Figure 3.

TPC14 architecture (continued)

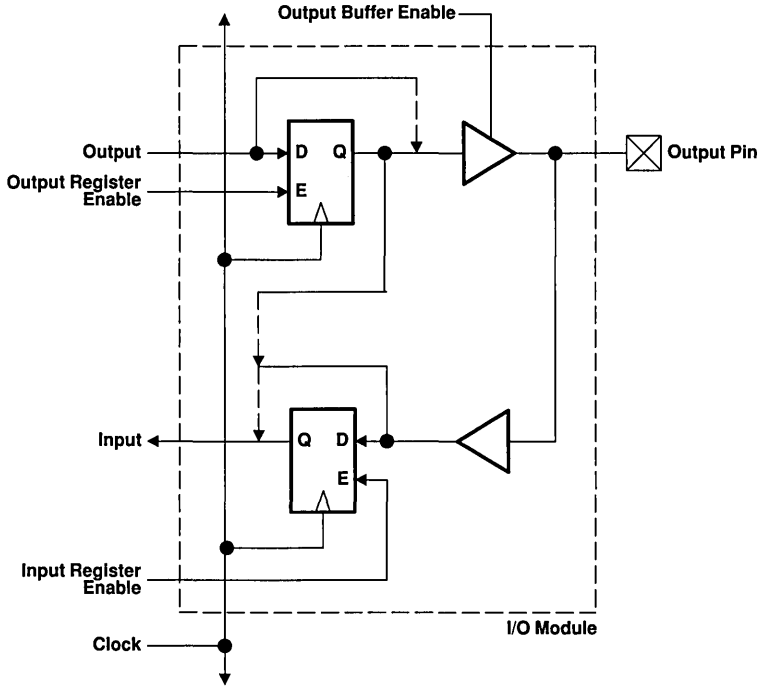


Figure 3. I/O Module With Registered Inputs and Outputs

clocking options

The TPC14 Series provides four clock distribution networks, twice the number of networks offered by the TPC12 Series. In addition to the two routed clocks, TPC14 Series provides two dedicated TPC clocking sources: one for the array and one for the I/O module. The routed clocks are compatible with the ACT12 Series and are optimized for clocking nets with light to medium loading. They can also be used for special high-fan-out nets, such as reset or enable. The dedicated clock networks are optimized for high-fan-out nets in either the array or the I/O module. Since these clocks are dedicated, no special circuitry is required to route the clock signals. This results in a very controlled, high-speed clocking network for the high-fan-out portion of the design. The high-speed clock-to-output capability of the TPC14 Series is a direct result of the dedicated clock in the I/O module.

programmable I/O pins

Each I/O pin is available as an input, output, 3-state, or bidirectional buffer. Inputs are TTL- and CMOS-compatible. Output drive levels meet 12-mA TTL and 6-mA HCT standards.

designing with TPC14

design methodology

The simple, highly regular logic module architecture of the TPC14 Series is ideal for synthesis optimization. The TI-ALS design environment supports a wide variety of popular design approaches via schematic entry and synthesis. Synthesis libraries for top-down design are available. Boolean entry and state machine design are supported with logic optimization tools. In addition, ALS software provides 100 percent automatic placement and routing at up to 95 percent module utilization.

hard and soft macros

Designing with the TI design environment is accomplished through a building block approach. Over 250 logic function macros are provided in the TPC14 Series design libraries. Hard macros range from simple SSI gates such as AND, NOR, and exclusive-OR to more complex functions such as flip-flops with 4 to 1 multiplexed data inputs. Hard macros are implemented within the TPC14 Series architecture by utilizing one or more C-modules and/or S-modules. Over 150 of these macros are implemented within a single logic module, although several two-module macros are available. Accurate performance prediction is possible due to the small propagation delay variance associated with one- and two-module hard macros.

Soft macros comprise multiple hard macros connected to form complex functions ranging from MSI functions to 16-bit counters and accumulators. A large number of TTL-equivalent hard and soft macros also are provided.

design compatibility

The design libraries for TPC14 Series are upward compatible from the TPC10 and TPC12 Series design libraries. TPC10 and TPC12 Series designs can be converted to equivalent-gate-count TPC14 Series arrays. The Activator™2 programmer supports the TPC14 Series; this programming unit also supports TPC10 and TPC12 Series.

PRODUCT PREVIEW

3 Action Logic System Overview

Chapter 3

Action Logic System Overview

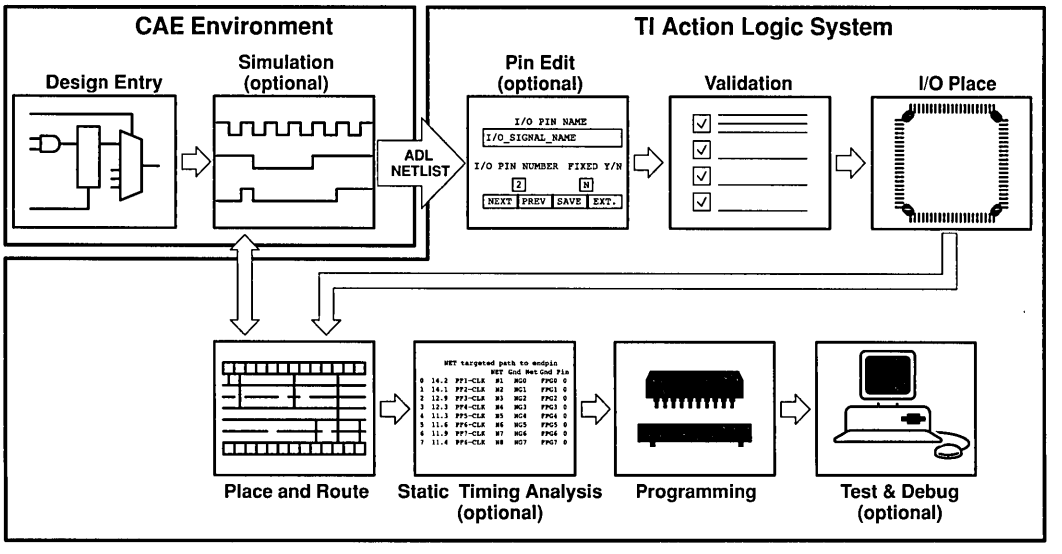
Contains an overview of the TI-ALS development system environment, TI third party support, and hardware programming and debug tools. Details a step-by-step design flow through the TI-ALS software.

3.1 TI-ALS Introduction

The Texas Instruments Action Logic™ System (TI-ALS) consists of user-friendly software and advanced-programming hardware. It operates on '386/486 personal computers, HP/Apollo™ workstations, or Sun™ workstations running such popular CAE systems as Mentor™, View*logic*™, OrCAD™, or Cadence™/Valid™.

TI-ALS enables the user to move quickly from netlist validation through place and route to test and debug. With TI's easy-to-use, yet comprehensive FPGA design process, TI FPGAs can be implemented from concept to programmed-silicon in hours rather than days. Figure 3–1 is a detailed block diagram of the TI-ALS Development System Environment.

Figure 3–1. TI-ALS Development System Environment



❑ Design Entry and Simulation

TI-ALS supports high-level behavioral design input, Boolean entry and state machine definition, and schematic capture design entries performed in familiar host environment. The TPC Series macro library consists of the most frequently used hard and soft macros and offers the capability for additional user-created macros. Post-layout design simulations are also performed within the host environment for functional verificaiton. A transcription utility to generate an ADL netlist is provided with the system.

❑ Pin Edit (optional)

The user can manually assign I/Os to device package pins or let the TI-ALS automatically assign them.

❑ Validation

An electronic design rule check assures that design parameters are met. Any errors in the schematic can be quickly corrected before proceeding. Examples may be excessive fanouts or unconnected pins.

- **I/O Place**

  All unassigned I/Os are automatically assigned for maximum performance and routability.

- **Place and Route**

  Places the functions and routes interconnects between logic modules and I/O pins. This is accomplished automatically and optimized for the specific design with special attention paid to critical paths. Manual placement of components or routing of interconnects is not required, but manual placement may be done. Generally, manual placement is not necessary. Back-annotation exports post-layout delays back to the host environment for device stimulation.

- **Static Timing Analysis**

  Displays the timing characteristics of the FPGA design for inspection of all paths. Postlayout net delays are summarized and automatically ported to the timer for specific circuit timing analysis.

- **Programming**

  The TI-ALS reads the fuse file and Activator™ hardware applies programming pulses in sequence. Each antifuse is verified, and a check on surrounding antifuses assures correct device functionality.

- **Test and Debug (optional)**

  Permits verification of device in the development system environment or target system; 100% observability of all on-chip functions is provided without generating test vectors. Multiple nodes can be addressed simulataneously using two built-in test pins that can later be used as I/Os. In-circuit test and debug are accomplished using an Actionprobe™ which can address any internal node to determine its logical state. Programming security antifuses protects against reverse engineering.

3.2 TI Third Party Support

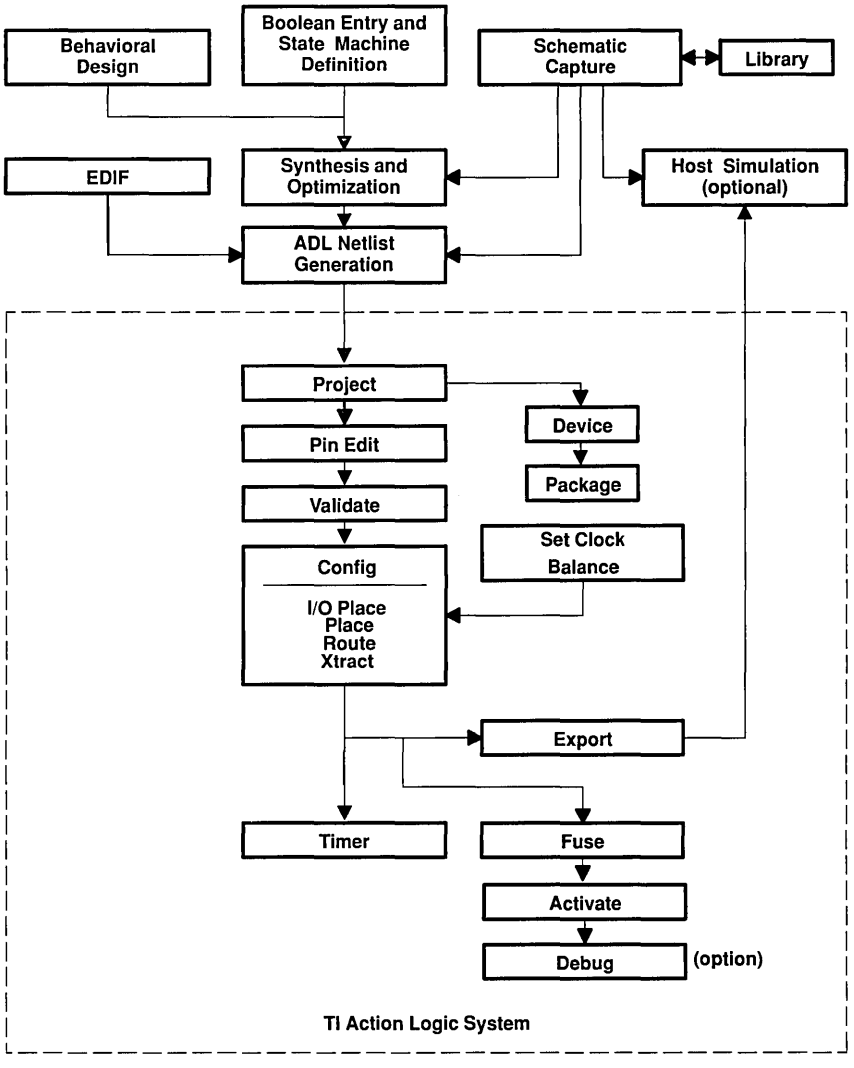
In addition to the FPGA TI-ALS, additional support tools are available from some third parties. These tools, their general description, and their benefit to the FPGA design flow are outlined below in Table 3–1.

Table 3–1. TI Third Party Support

THIRD PARTY TOOLS	GENERAL FUNCTIONS	BENEFITS
Data I/O ABEL4 ABEL-FPGA™ Minc PGADesigner™ Logic Devices AllPRO™	Synthesize from design inputs (usually Booleans) into PLDs and FPGAs. Architecture-specific filters are developed to optimize the design inputs into an FPGA.	Device independent inputs allow designers to consider many technologies while minimizing design time Multiple input formats are supported: Boolean, state machine, truth table, and waveform (Minc only). Benefits include easier designs and shorter cycle times. Tools support various semiconductor suppliers; this allows rapid sourcing and continuity of supply.
Logic Modelling	These models are behavioral descriptions of devices that allow system-level simulation.	Allows end user to verify board design early in the development cycle and therefore minimize risk. Analyzes interface between devices in the system.
Synopsys Design Compile™ Exemplar CORE1	Allows the engineer to design circuits with high-level languages (VHDL and Verilog HDL). The design is then synthesized/targeted to a semiconductor supplier library for gate-level simulation	Designing in high-level languages shortens time to market. The same design can be retargeted to many devices (i.e., first to an FPGA and later to a gate array) thereby increasing engineering productivity. Allows rapid second sourcing.

3.3 Design Flow

Figure 3–2. The FPGA Design Process



The TI FPGA design flow, as illustrated in Figure 3–2, simplifies and speeds design implementation at the user's desktop. The process is initiated within the host system environment in conjunction with the TPC Series macro libraries. Prelayout and postlayout simulations of the design can be performed within the host environment. When the host environment design processes are complete, the TI-ALS files are exported to the TI-ALS.

TI-ALS files are created in the \designs\yourdsgn\directory:

\yourdsgn.adl
\yourdsgn.crt
\yourdsgn.ipf

The file *yourdsgn.adl* contains the TI-ALS formatted netlist. The designer can specify nets as critical for routing purposes by entering the device inputs and outputs in the criticality file, *yourdsgn.crt*. A formatted, empty initial pin assignment file, *yourdsgn.ipf*, is created automatically during netlist generation.

After exporting the data, the design is ready to be processed in the TI-ALS to create the files needed for programming the FPGA. The TI-ALS is entered using the command:

```
als yourdsgn
```

In addition to the files created during export of the design, a number of files will be created when the TI-ALS is used to validate, place and route, and create the files for programming the device. These files will also be located in the *designs\yourdsgn\yourdsgn.ext* path. After the TI-ALS utilities have been executed, the directory will contain the files shown in Table 3–2.

Table 3–2. Files Contained in the \yourdsgn Directory

FILENAME EXTENSION	CONTENTS	CREATED BY
\yourdsgn.ADL	The exported netlist file	ADL netlister
\yourdsgn.CRT	Blank critical path file	ADL netlister
\yourdsgn.PIN	Pin assignment data	Config
\yourdsgn.DEF	Definition file	ADL netlister & Project
\yourdsgn.IPF	Initial pin assignment file	ADL netlister & Pin Edit
\yourdsgn.COB	Validate combine file	Validate
\yourdsgn.VAL	Validation passed file	Validate
\yourdsgn.AFL	Primary source file	Validate
\yourdsgn.VLD	Validation log file	Validate
\yourdsgn.DFR	Design for routability file	Ioplace
\yourdsgn.LOC	Macro location file	Place
\yourdsgn.SEG	Track segment file	Route
\yourdsgn.DEL	Physical delay file	Extract
\yourdsgn.PLI	Placement information file	Place
\yourdsgn.MAP	Macro placement file	Place
\yourdsgn.RTI	Routing information file	Route
\yourdsgn.FUS	Fuse file	Activate
\yourdsgn.AFM	Compiled fusing data	Activate†
\yourdsgn.AVI	Fusing log file	Activate
\yourdsgn.DTB	Back-annotation delay file	Export
\alsuser\user_name\yourdsgn.LOG	Design log file	TI-ALS

† Activator 2 only.

3.4 Hardware

3.4.1 Activator 1 and Activator 2

After a design is processed by the TI-ALS and the programming file (\yourdsgn.FUS) is generated, the user can program TPC Series FPGAs using an Activator 1 or Activator 2 programmer.

The Activator 1 provides programming for TPC10 Series devices only. In addition, the Activator 1 can only be used to program one device at a time. The activator 1 connects to most 386/486-based personal computers offering IBM PC/AT compatibility and IBM PC-style bus structure for add-in cards. The Activate software, accessed using the TI-ALS user interface, is used to control the Activator 1 programmer. The Activator 1 product was discontinued in January, 1993. TI-ALS software continues to support this programming unit. The Activator 1 programmer is shown in Figure 3–3.

The Activator 2 provides programming for TPC10 and TPC12 Series devices. The Activator 2 allows programming of one, two, three, or four devices at a time. The Activator 2 connects to most 386/486-based personal computers, Apollo workstations, or SUN workstations. The APS2 software is used to control the Activator 2 programmer. The Activator 2 programmer is shown in Figure 3–4.

With an FPGA device installed in the appropriate Activator socket, programmation is begun by selecting commands from the TI-ALS or TI Activator Programming Software (APS™) menus. The system responds with choices for *BlankChk*, *Program*, *Security*, and *Exit*.

BlankChk (blank check) ensures that the device is not already programmed.

Even though the *blank check* option is offered separately, the selection for programming a device automatically invokes a blank check. If the device has been programmed, the *Program* command will be aborted. This ensures that the programming sequence is applied to a blank FPGA. FPGAs are one-time programmable. They cannot be reprogrammed or overblown as is permissible with some other one-time programmable devices.

When *Program* is executed, the Activator applies programming pulses in sequence. As each antifuse is programmed, it is dynamically verified to be properly activated.

3.4.2 Test and Debug

Test and debug permits verification of performance in the development system environment or target system; 100% observability of all on-chip functions is provided without generating test vectors. Multiple nodes can be addressed simultaneously using two built-in test pins that can later be used as I/Os. In-circuit test and debug is accomplished using an Actionprobe (one of which is shown in Figure 3–3), which can address any internal node to determine its logical state. The Activator 2 has an accompanying universal probe which performs the same function.

Figure 3–3. Activator 1 Programmer and Actionprobe

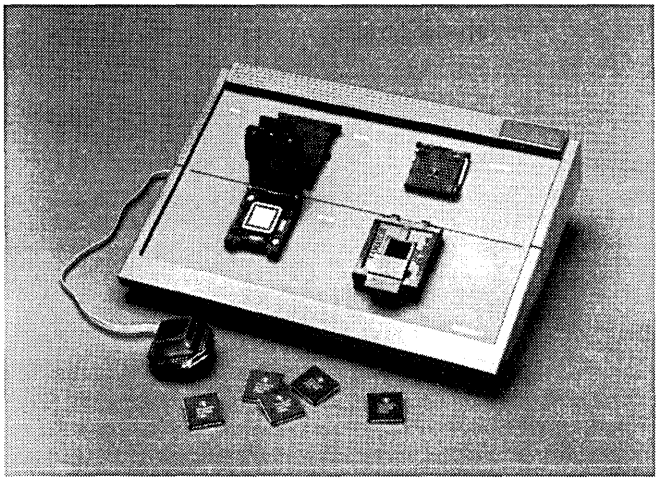
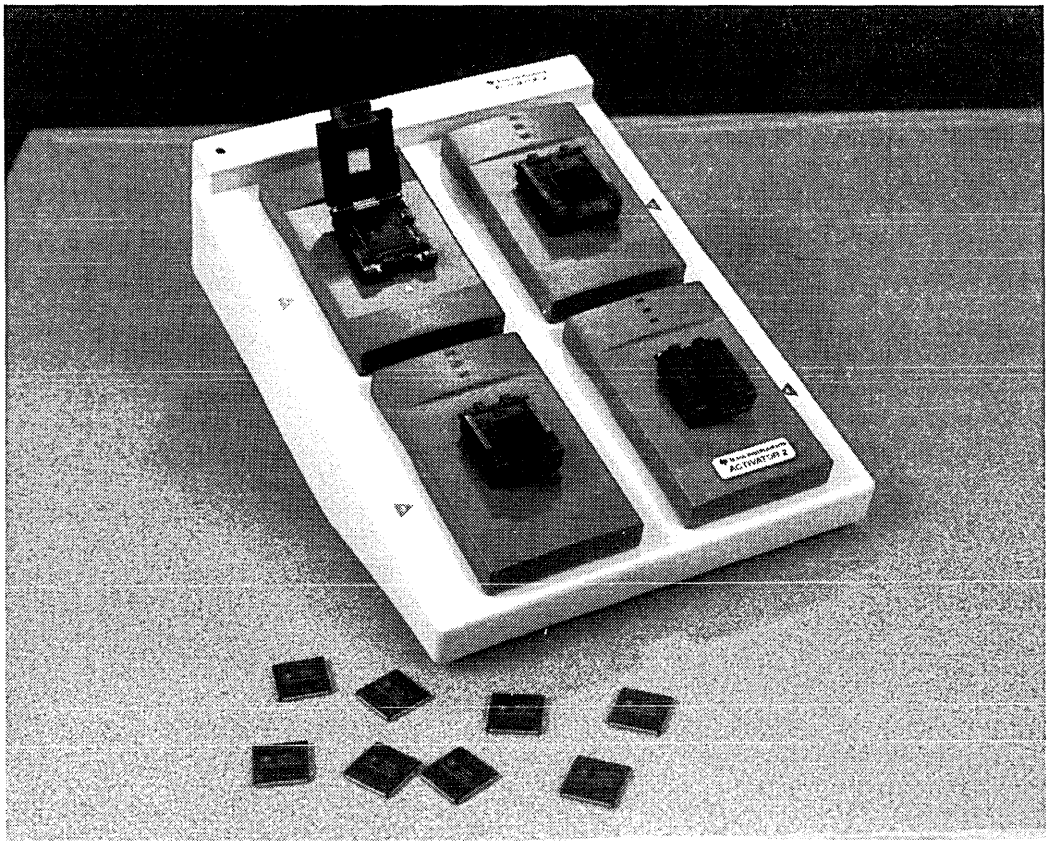


Figure 3–4. Activator 2 Programmer



3.5 Software

3.5.1 Main Menu

When the TI-ALS is invoked, the Main Menu appears. Selections and the command/response from the Main Menu are:

SELECTIONS	COMMAND/RESPONSE
MainMenu	
Project	Change project settings
Pin Edit	Perform manual I/O pin assignments
Validate	Perform design rule checks
Config	Perform automatic I/O pin assignment, place, route, and delay extraction.
Alsrun	Perform Validate, Config, and generate programming file.
Timer	Perform static timing analysis
Export	Generate postlayout delay file
Fuse	Create antifuse file with silicon signature
Activate	Program a device (Activator 1 only, see Note)
Debug	Functional test of in-circuit probe (Activator 1 only, see Note)
Browse	Read-only file viewer
System	Go to DOS
Exit	Exit TI-ALS

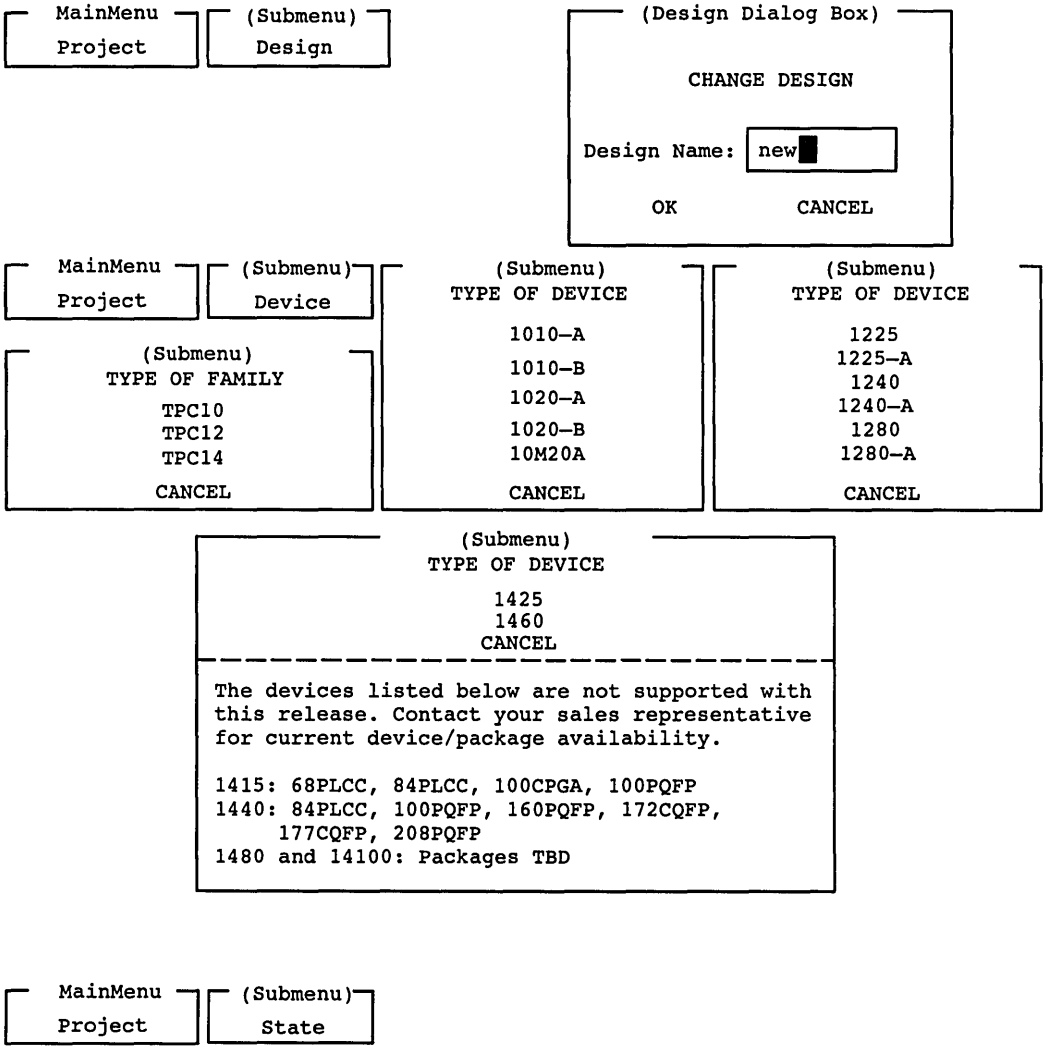
Note:

The Activator 2 is accessed using the DOS command `APS2 yourdsgn`.

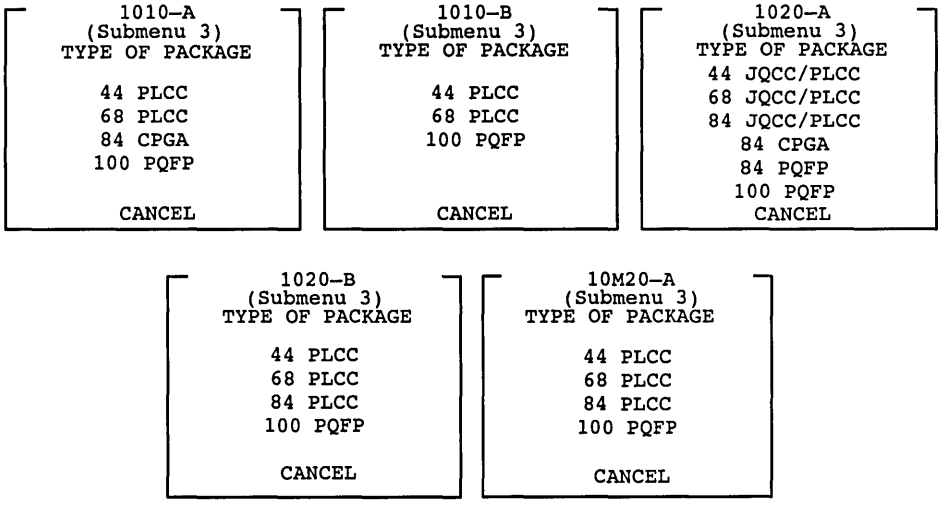
The Main Menu displays the current active design at the bottom of the screen.

3.5.2 Project

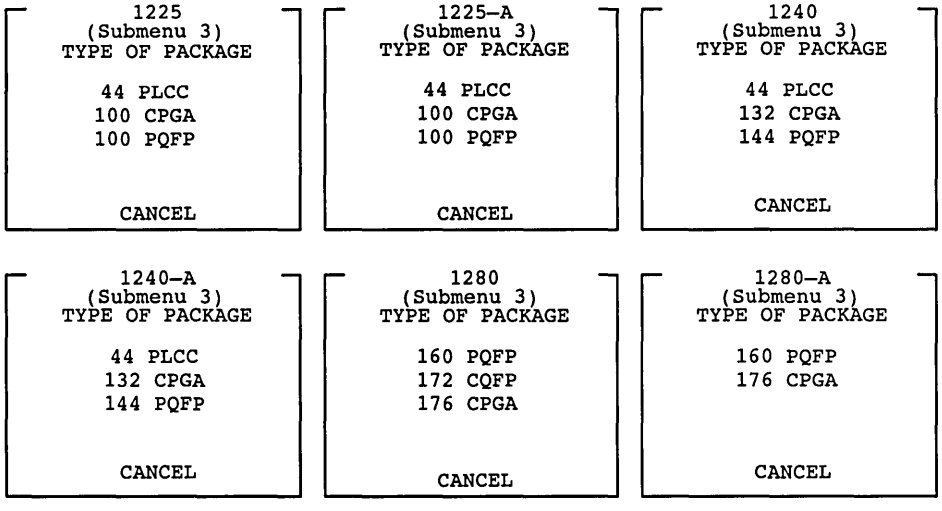
When *Design* is selected from the submenu, TI-ALS responds with an interactive dialog box that permits the user to change the name of the design project. A command to change the design name will direct subsequent TI-ALS commands to be performed on the files pertaining to the newly requested design. When *Device* is selected, submenus are provided to enter or change the FPGA device type. After the device is selected, submenus are provided for package selection. The *State* option displays the status of the TI-ALS design flow.



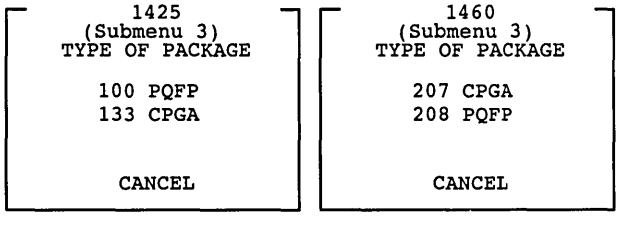
TPC10



TPC12



TPC14



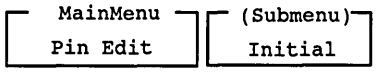
3.5.3 Pin Edit

Pin Edit is an option that facilitates manual pin assignment. The design can be validated with the pins automatically assigned using the *Config* submenu. Selection of the TI-ALS Pin Edit program reads the design data files, responds with an interactive dialog box that displays a device pin label, and then provides a field for entering the package pin numbers (locations). As a pin number is entered, the editor scrolls sequentially through the device I/O labels.

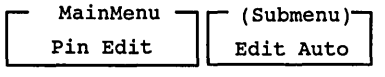
For each pin number entered, the editor ensures that the pin is an available package pin and has not already been assigned to another device I/O. If non-conforming, conflicting, or incomplete pin assignments are attempted, the system responds with dialog options that can be used to modify the assignments. Dialog options exist for reviewing the pin assignments by selecting the previous (*prev*) or *next* options which sequentially displays the pin labels and numbers.

Partial pin assignment can be done manually and the pin locations can be fixed using the *Fix This Pin* command. When predetermined pin locations are required, the *Fix All Currently Assigned Pins* selection may be used. If pin locations are not critical, the *Unfix All Currently Assigned Pins* selection is offered. Data entered using Pin Edit is written to the design file, **\yourdsgn.PIN**, by selecting the *save* option.

Select *Initial* to create the initial pin placement file. The *Edit Auto* command will edit an existing pin file if one already exists.



Initial pin file creation



Edit the existing pin placement file.

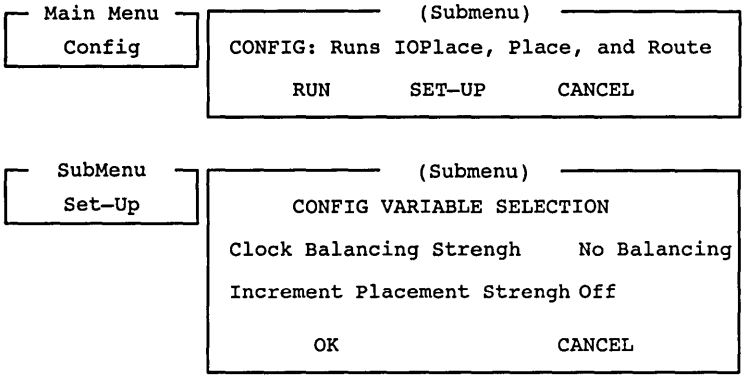
3.5.4 Validate

Validate examines the design's adherence to rules applicable for the selected device and package. Informational messages are displayed indicating that each library macro definition is checked and reporting total logic module utilization. The captured design hierarchical definition, global and external connections, and physical consistencies are checked. The validate process verifies routability and estimates critical path delays and package definitions prior to routing. Validate produces warning messages regarding electronic rules violations such as excessive fan-out. Error messages are generated if shorted outputs, unconnected inputs or other catastrophic oversights are encountered. Before the design is configured, errors must be resolved and *Validate* must be run to completion without error.

Validation can be completed with partial or no pin assignments since automatic pin assignment can be used during configuration. Criticality limits are checked against absolute device limits and a warning will result if the sum of fast (F) and medium (M) critical path assignments exceed 20% of the available routing resources. Validate displays statistical information about logic module count, I/O count, and average fan-out per net. The `als -validate` *`yourdsgn`* command is executable outside of the TI-ALS for use in batch mode.

3.5.5 Configure (Config)

When entered, the *Config* selection responds with a submenu containing choices for Automatic I/O Pin Assignment, Clock balancing strength, and Automatic Place and Route. *Clock balancing* selection should be made prior to the *Automatic Place and Route* command.



3.5.5.1 Automatic I/O Pin Assignment

Automatic I/O assignment and optimization are mandatory steps in the TI-ALS design flow, while manual pin assignment can be optionally performed via Pin Edit. During automatic I/O pin assignment, a utility report (DFR file) containing path and pin location data is created, which can be used to evaluate the design. The designer can use the report to evaluate potential modifications, some as simple as pin reassignments for fixed I/Os; this can significantly simplify the place and route and also enhance the resulting device performance. The report, a text file named `yourdsgn.DFR`, can be acccessed from the *Browse* selection on the Main Menu and printed using commonly available utilities. The `als -Ioplace` ***`yourdsgn`*** command is executable outside of the TI-ALS for use in batch mode.

3.5.5.2 Clock Balancing Strength

The *Clock balancing strength* selection will display a submenu that can be used to select *No balancing*, *Moderate*, *Strong*, or *Very strong* placement rules designed to balance the loads on the dedicated clock network to reduce clock skew. The clock balancing strength variable will affect macro placement during the *place* routine.

3.5.5.3 Automatic Place and Route

Selecting *Automatic Place and Route* will invoke the place, route, and extract commands sequentially. Keyboard commands can be used to perform each of these commands separately, or batch files can be used to execute the combinationals desired. The sequence of place, route, then extract must be observed.

3.5.5.4 Place

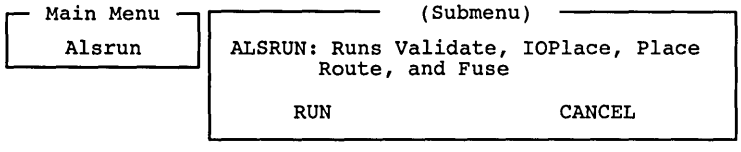
Fully automatic placement is accomplished in two phases. Phase 1 performs an initial placement that produces a layout for which the average wire lengths and long net requirements are displayed. In phase 2, an automatic improvement and optimization routine is invoked to improve the placement by reducing both the average wire length and long net requirement. Phase 2 minimizes propagation delays by assigning macros to optimal logic module locations on the chip. In both phases, hard macros utilizing two logic modules are placed side-by-side in the same module row. An information file, yourdsgn.PLI, is created for the designer's evaluation. The `als -place` *`yourdsgn`* command is executable outside of the TI-ALS for use in batch mode.

3.5.5.5 Route

Using data from the macro placement, netlist, critical path, and I/O assignment data, the router assigns the shortest possible net segments to connect the macros used in the design. The route software takes advantage of the device architecture and abundance of routing resources to route the nets after placement is completed. An information file, *`yourdsgn`*`.RTI`, is created for the designers evaluation. The `als -route` *`yourdsgn`* command is executable outside of the TI-ALS for use in batch mode.

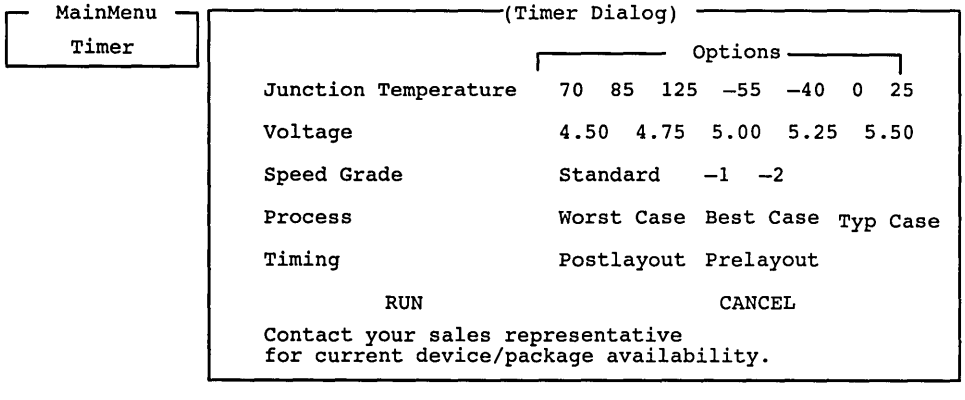
3.5.6 Alsrun

When entered, the *Alsrun* selection responds with a submenu to execute the Validate, automatic I/O pin assignments, automatic place and route, and fuse file generation utilities in a single step.



3.5.7 Timer

Selecting *Timer* from the TI-ALS Main Menu will respond with a dialog box to select the operating conditions, and postlayout or prelayout timing analysis.



The timer is an interactive static timing analysis tool used to analyze path delays. Prior to place and route, delay information is based on statistical estimates. After device configuration, actual net delays are used by the TI-ALS timer. These delay times can also be exported by the user to backannotate the host CAE netlist for performing postlayout simulations. The designer can utilize this path data to verify the device timing or to evaluate options available to improve the device timing specifications. Timer input is the design's netlist and delay information. The user directs the type of analysis and output. Delay reports generated by the timing analyzer using postlayout data provide the actual specifications for the device. Static timing analysis is useful for determining:

- ❑ Internal setup and hold time requirements
- ❑ Maximum operating frequency
- ❑ Maximum register-to-register delay
- ❑ Clock-to-out delay
- ❑ Input-to-output delay
- ❑ External setup and hold time requirements
- ❑ Clock skew

The Timer displays data in either of the following formats:

1) Expanded format showing a single path delay, with the column headings of:

   `Total Delay Typ Load Macro Start Pin Net Name`

   where:

   Total = cumulative path delay time

   Delay = incremental delay due to a particular segment of the path. The delay is measured from the input of the macro to the input of the next macro.

   Typ = category of delay listed (i.e. propagation delay, setup time, skew, etc.)

   Load = the load on the output of that particular macro

   Macro = the library component used at that point of the path

   Start Pin = the instance name of the input pin of the macro

   Net Name = The name of the net attached to the output of the macro. The delay due to this net is added to the macro delay to obtain the *delay* value

2) Listing of multiple delay paths, with the column headings of:

```
Rank  Total  Start Pin  First Net  End Net  End Pin
```

where:

Rank = rank order number for the given path

Total = total path delay

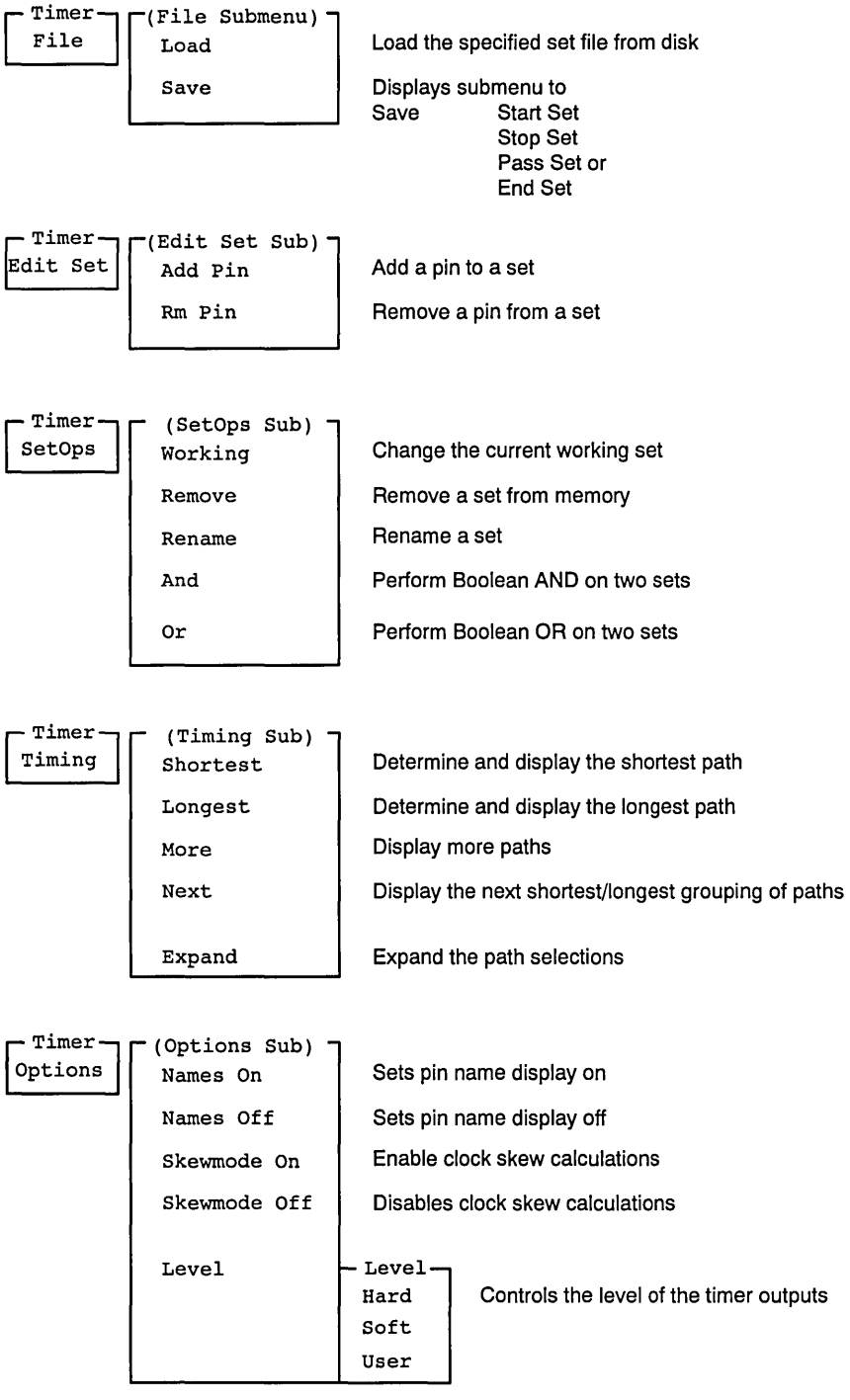
Start Pin = instance name of the input pin of the beginning macro

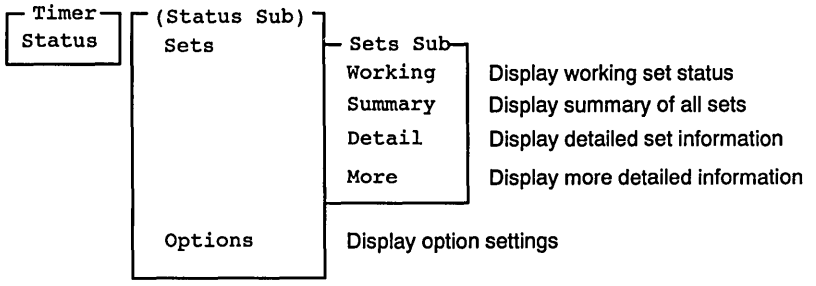
First Net = net attached to the output of the beginning macro

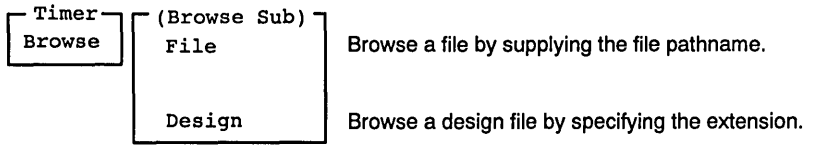
End Net = net attached to the output of the ending macro

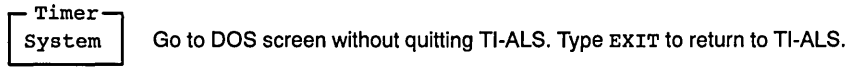
End Pin = instance name of the output pin of the ending macro

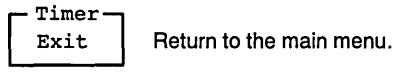
The timer is executable outside of the TI-ALS to invoke a command line version of the timer.


Timer
File
(File Submenu)
Load
Load the specified set file from disk
Save
Displays submenu to
Save
Start Set
Stop Set
Pass Set or
End Set
Timer
Edit Set
(Edit Set Sub)
Add Pin
Add a pin to a set
Rm Pin
Remove a pin from a set
Timer
SetOps
(SetOps Sub)
Working
Change the current working set
Remove
Remove a set from memory
Rename
Rename a set
And
Perform Boolean AND on two sets
Or
Perform Boolean OR on two sets
Timer
Timing
(Timing Sub)
Shortest
Determine and display the shortest path
Longest
Determine and display the longest path
More
Display more paths
Next
Display the next shortest/longest grouping of paths
Expand
Expand the path selections
Timer
Options
(Options Sub)
Names On
Sets pin name display on
Names Off
Sets pin name display off
Skewmode On
Enable clock skew calculations
Skewmode Off
Disables clock skew calculations
Level
Level
Hard
Soft
User
Controls the level of the timer outputs



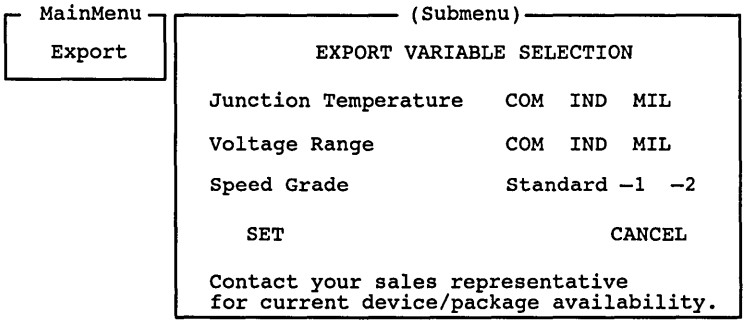






3.5.8 Export

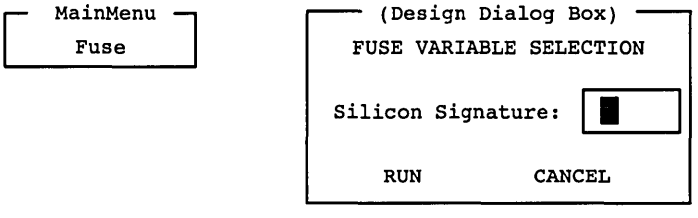
The *Export* function permits the designer to backannotate the host system delay files with FPGA postlayout timing data for use with the host system's simulator. Min/Max delay values reflecting the operating condition (voltage, temperature, and speed) can be specified by the designer.



Using data from the place and route programs, this routine compiles the postlayout delay data needed to produce the delay file. Options are available to specify temperature and voltage ranges as well as the device speed grades offered. The delay file is the source data for postlayout delay time simulations on the host CAE. The delay file is also the source of the timing information when using the Timer in the postlayout mode. The `als -extract` *`yourdsgn`* command is executable outside of the TI-ALS for use in batch mode.

3.5.9 Fuse

The *Fuse* selection, using data from the place and route routines, generates a fuse file that maps the fusing sequence and locations. This file will be utilized to program the FPGA device by either the *Program* selection on the Activate Menu or the *Activate* command on the APS2 menu. When entered, the *Fuse* selection responds with a dialog box to enter a 5-digit hexadecimal user-specified signature. The readable signature can provide the user with permanent device identification. The `als -fuse` *`yourdsgn`* command is executable outside of the TI-ALS for use in batch mode and can also include a user-specified 5-digit hexadecimal signature.



3.5.10 Activate (Activator 1 or 2)

The *Activate* command responds with an Activator 1 menu providing choices for performing device blank check, device programming, or security fuse programming. To perform the activate functions, an Activator programmer containing a blank target device must be installed.

ACTIVATOR 1 SELECTIONS	COMMAND/RESPONSE
`Activate`	
`BlankChk`	Starts the device blank check routine
`Program`	Starts the blank check, then the device programming routines
`Security`	Select or deselect security fuses for programming
`Browse`	Read-only file viewer
`System`	Go to DOS
`Exit`	Returns control to the Main Menu

The Activator 2 is accessed from the DOS command `APS2` *`yourdsgn`*.

ACTIVATOR 1 SELECTIONS	COMMAND/RESPONSE
`MainMenu`	
`Project`	Change design project
`BlankChk`	Starts the device blank check routine
`Activate`	Implements programming based on selected options
`Checksum`	Retrieves the device checksum and silicon signature
`Security`	Select or deselect security fuses for programming
`Debug`	Functional test or in-circuit probe (Activator 2 only)
`Browse`	Read-only file viewer
`System`	Go to DOS
`Exit`	Exit APS2

3.5.10.1 Project (Activator 2)

This command provides an interactive dialog box that permits the designer to change the name of the design project.

3.5.10.2 BlankChk (blank check) (Activator 1 or 2)

This command will initiate a blank check on the installed device.

If the device has already been programmed, the Activator 1 returns a checksum that can be used to identify the device. BlankChk is automatically performed prior to device programming. BlankChk also verifies that the device is inserted properly into the Activator socket.

3.5.10.3 Checksum (Activator 2)

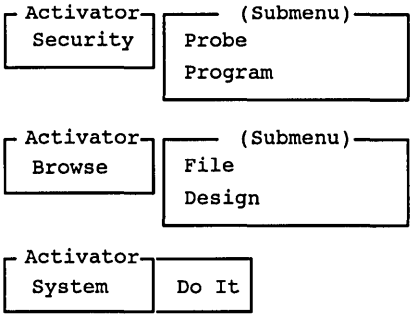
This command retrieves a programmed device's checksum and silicon signature.

3.5.10.4 Program (Activator 1)

Prior to programming, the system verifies that the device has not been programmed. The fuse map file data is the source that the Activator uses for programming. A series of internal address registers are automatically loaded, specifying the antifuse programming element to be programmed. A programming sequence is then initiated, creating a permanent link. The step is repeated until programming sequences are made for both the logic module macros and the netlist interconnect functions.

3.5.10.5 Security (Activator 1 or 2)

Security fuses are provided that can be programmed to permanently disable all further programming, diagnostics, and testing.



3.5.10.6 Activate (Activator 2)

Depending on the selections made in the security menu, one of the following submenus will appear: Array Fuses Only, Array & Security Fuses, or Array, Program Probe Fuses.

Select

Subsequent programming of devices will automatically include the security fuse(s).

Deselect

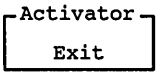
Subsequent programming of devices will exclude the security fuse(s).

Program

This option allows the programming of the security fuse(s) of previously programmed parts.

3.5.10.7 Exit

Returns to the Main Menu.



3.5.11 Debug

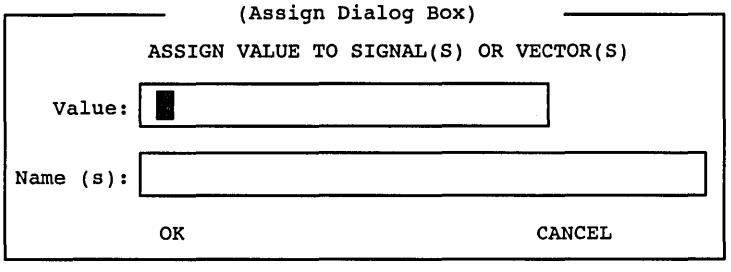
The Debug program provides functional testing using I/O test vectors and the Activator programmer. Two Actionprobe pins on the device provide an interface for enabling interactive device debugging. Prior to inserting the device into a PC board, the designer can apply artificial stimuli to the device and monitor the response on any internal signal. Using this Activator analysis capability, the designer can observe any internal FPGA node. The user also has the option of using the Actionprobe hardware to perform at-speed in-circuit evaluation of the device. The TI-ALS can be used to control the Actionprobe pins and access the proper internal nodes. These internal values can then be monitored by an oscilloscope or logic analyzer.

SELECTIONS	COMMAND/RESPONSE
Debugger	
File	User-created command file options.
Stimulus	Accesse a dialog box to change the signal or specify the logic level.
Output	Allow selection of print options and assignment of signals.
Compare	Compare signal or vector values.
Step	Specify debug cycle(s) to be performed.
Print	Print node values of an active debug sequence.
FPrint	Print node values to a file.
Repeat	Submenu to specify files for loading or saving debug data.
Macro	Define a macro as a sequence of commands.
ICP	Interactive dialog box to assign in-circuit probe pins.
Browse	Read-only file viewer
System	Go to DOS
Exit	Returns control to the Main Menu.

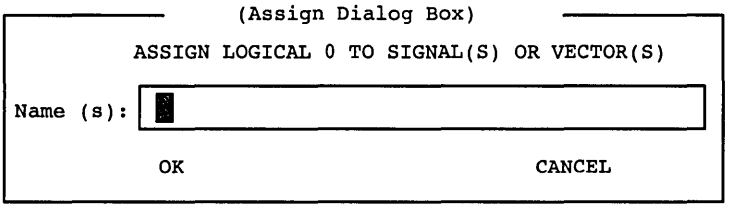
Activator 1 Debug is accessed from the TI-ALS MainMenu.
Activator 2 Debug is accessed from the APS2 MainMenu.

Debugger	(File Submenu)	
File	Load File	Load a user created command file.
	In File	Opens an input file for Fassign.
	Out File	Opens an output file for Fprint.
	Comp File	Opens a compare file for Fcomp.

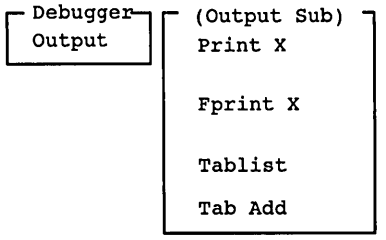
Debugger	(Stimulus Sub)	
Stimulus	Assign	This selection accesses a dialog box to specify or change the signal or vector to be operated on.



Debugger	(Stimulus Sub)	
Stimulus	Low	These selections respond with a dialog box to specify the logic levels that are to be applied to the signal or vector specified.
	High	
	High-Z	



Debugger	(Stimulus Sub)	
Stimulus	Fassign	This selection permits the user to read node and vector values from a specified input file as the source of debug commands to be performed.

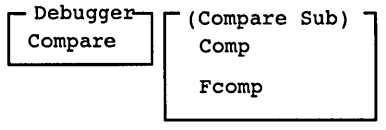


Selection of the print option will print the current values of all nodes on the tablist to the screen.

Selection of Fprint will print the current values of all nodes on the tablist to a file.

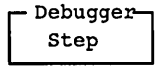
Assign signals to the table list.

Add signals to the table list.

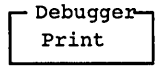


Compare a value to the signals or vectors listed.

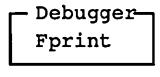
Compares the comp file value to the signals or vectors listed.



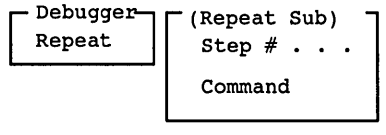
Debug for one cycle.



Print the signals or vectors in the tablist.

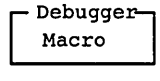


Prints the signals or vectors in the tablist to a file.

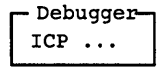


Sets the number of debug cycles.

Set up a command sequence and the number of times to execute it.



Define a macro as a sequence of commands.



This selection responds with a dialog box to specify the internal probe probe points when using debug in the in-circuit mode.

Debugger Browse	(Repeat Sub) File	Browse a file by supplying the file pathname.
	Design	Browse a design file by specifying the extension.

Debugger System	Go to a DOS screen without quitting TI-ALS. Type EXIT to return to TI-ALS.

Debugger Exit	Returns to the Main Menu.

3.5.12 Browse

Browse permits the designer to read ASCII files. Files generated by the TI-ALS can be accessed by typing in the three-character extension and selecting *TI ALS Name* within the dialog box. Any other ASCII file can be accessed by typing the full pathname and selecting *Path Name* within the dialog box.

MainMenu Browse	SubMenu File	(Browse Dialog Box) BROWSE A FILE File Name: OK CANCEL

MainMenu Browse	SubMenu Design	(Browse Dialog Box) BROWSE A DESIGN FILE ALS Name: OK CANCEL

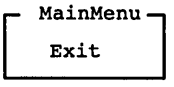
3.5.13 System

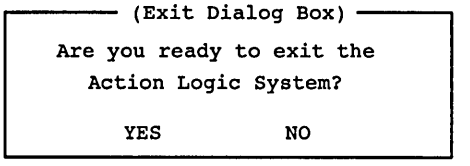
This main menu selection allows the designer to go to a DOS screen without quitting TI-ALS. Type *Exit* to return to TI-ALS.

MainMenu System

3.5.14 Exit

This Main Menu selection responds with a dialog box that confirms the user's decision to continue with or terminate the TI-ALS.





4 FPGA Design Software and Hardware

Chapter 4

FPGA Design Software and Hardware

Lists the TI-ALS system configurations and software/hardware options and provides detailed system descriptions of all the available configurations.

4.1 TI Action Logic System (TI-ALS)

The Texas Instruments Action Logic™ System (TI-ALS), is a high-productivity Computer Aided Engineering (CAE) development tool for implementing TI Field-Programmable Gate Array (FPGA) designs. The designs can be captured and devices programmed at the designer's desk, when utilizing a supported design system in conjunction with TI-ALS and TI FPGAs. The TI-ALS consists of software and hardware added into an existing CAE environment to provide an FPGA design library and device programming. The FPGA designer reduces cost of ownership by avoiding nonrecurring engineering (NRE) fees, device-specific tooling charges, and completes timely designs by customizing an FPGA through device programming at the designer's desk. The TI-ALS configurations offered are summarized in Table 4–1 and described in this section. Figure 4–1 shows a 386/486-based PC with TI-ALS and Activator™ installed.

Figure 4–1. 386/486-Based PC with TI-ALS and Activator Installed

Table 4–1. TI-ALS Design Configurations, see Note 1

HARDWARE PLATFORM	LIBRARY/CAE HOST ENVIRONMENT	DESIGN SUPPORT (gates)		TI SUSTEM PART NUMBER
		UP TO 2500	UP TO 10000	
386/486-based PC	Viewlogic	X		TPC-ALS-DS-PC-VL
	ViewLogic		X	TPC-ALS-DA-PC-VL
	OrCAD	X		TPC-ALS-DS-PC-OR
	OrCAD		X	TPC-ALS-DA-PC-OR
Sun	Cadence		X	TPC-ALS-DA-SN-CD
	Mentor		X	TPC-ALS-DA-SN-MG
	Valid		X	TPC-ALS-245†
	ViewLogic		X	TPC-ALS-DA-SN-VL
HP700	Mentor		X	TPC-ALS-DA-HP7-MG
DN4000/ HP400				TPC-ALS-235†

NOTE 1: Authorization codes for design systems are supplied upon request, after receipt of the system. .

† The TPC-ALS-235 and TPC-ALS-245 systems only provide support for the TPC10 and TPC12 series, and will not be supported in Revision 3.0, scheduled for release in the fourth quarter of 1993. These systems are being replaced by TPC-ALS-DA-HP7-MG and TPC-ALS-DA-SN-CD, respectively.

Table 4–2. TI-ALS Programming Configurations, see Note 2

HARDWARE PLATFORM	CAE HOST ENVIRONMENT	DESIGN SUPPORT		TI SUSTEM PART NUMBER
		ONE DEVICE	FOUR DEVICES	
386/486-based PC	ViewLogic /OrCAD	X		TPC-ALS-DS-P2S-PC
			X	TPC-ALS-219
Sun	Cadence/Mentor/ Valid/ViewLogic	X		TPC-ALS-DS-P2S-SN
			X	TPC-ALS-249
HP700	Mentor	X		TPC-ALS-DS-P2S-HP7
			X	TPC-ALS-DS-P2-HP7
HP400	Mentor	X		TPC-ALS-DS-P2S-HP4
			X	TPC-ALS-DS-P2-HP4
DN Series	Mentor		X	TPC-ALS-239

NOTE 2: Programming units are compatible with both high (10000 gates) and low (2500 gates) density systems.

Table 4–3. Software Options

HARDWARE PLATFORM	LIBRARY/CAE HOST ENVIRONMENT	TI SUSTEM PART NUMBER	DESCRIPTION
386/486-based PC	ViewLogic	TPC-ALS-016	Viewlogic high density simulation
		TPC-ALS-017	Viewlogic low density simulation
		TPC-ALS-VL-005	Viewlogic schematic capture
		TPC-ALS-VL-001	Viewlogic schematic redraw
	Exemplar	TPC-ALS-PLDSYN	Boolean synthesis/FPGA optimization
	TI	TPC-ALS-218	Device debug (In-circuit/Activator)
Sun	Synopsys	TPC-ALS-SYN-S4	TI libraries for design Compiler
	TI	TPC-ALS-218	Device debug (In-circuit/Activator)
HP700	Synopsys	TPC-ALS-SYN-HP	TI libraries for design Compiler
	TI	TPC-ALS-218	Device debug (In-circuit/Activator)
DN4000/HP400	Synopsys	TPC-ALS-SYN-DN	TI libraries for design Compiler
	TI	TPC-ALS-218	Device debug (In-circuit/Activator)

Table 4–4. Hardware Options

The tables below lists hardware adapters for programming and test and debug.

ADAPTERS FOR ACTIVATOR 1	
HARDWARE	**DESCRIPTION**
TPC-ALS-091	68-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-092	84-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-093	44-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-094	84-Pin, Pin Grid Array Diagnostic Probe
TPC-ALS-096	84-Pin, Ceramic Quad Flat Pack Programming Adaptor
TPC-ALS-097	100-Pin, Plastic Quad Flat Pack Programming Adaptor
TPC-ALS-098	100-Pin, Quad Flat Pack Diagnostic Probe

ADAPTERS FOR ACTIVATOR 2/2S†	
HARDWARE	**DESCRIPTION**
TPC10 SERIES	
TPC-ALS-280	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-281	44-Pin, Chip Carrier Programming Module
TPC-ALS-282	68-Pin, Chip Carrier Programming Module
TPC-ALS-283	84-Pin, Chip Carrier Programming Module
TPC-ALS-284	84-Pin, Pin Grid Array Programming Module
TPC-ALS-285	84-Pin, Quad Flat Pack Programming Module
TPC12 SERIES	
TPC-ALS-286	132/133-Pin, Pin Grid Array Programming Module
TPC-ALS-287	176/177-Pin, Pin Grid Array Programming Module
TPC-ALS-288	84-Pin, Chip Carrier Programming Module
TPC-ALS-289	100-Pin, Pin Grid Array Programming Module
TPC-ALS-290	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-292	144-Pin, Quad Flat Pack Programming Module
TPC-ALS-293	160-Pin, Quad Flat Pack Programming Module
TPC-ALS-294	172-Pin, Quad Flat Pack Programming Module
TPC14 SERIES	
TPC-ALS-PL84	84-Pin, Chip Carrier Programming Module
TPC-ALS-QF100	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-QF160	160-Pin, Quad Flat Pack Programming Module
TPC-ALS-QF208	208-Pin, Quad Flat Pack Programming Module
TPC-ALS-PG100	100-Pin, Pin Grid Array Programming Module
TPC-ALS-PG133	133-Pin, Pin Grid Array Programming Module
TPC-ALS-PG177	177-Pin, Pin Grid Array Programming Module
TPC-ALS-PG207	207-Pin, Pin Grid Array Programming Module
TPC-ALS-PG257	257-Pin, Pin Grid Array Programming Module

† All hardware adaptors are platform independent.

4.2 System Maintenance Contracts

TI-ALS software and hardware include a 90-day warranty. In addition, annual factory support packages can be purchased so that the user will have an extended warranty and continuing access to planned periodic updates and enhancements. The annual support period begins at the time of purchase and includes telephone support, bug fixes, workarounds, and periodic updates to the software.

4.3 Authorization Codes

The TI-ALS system software and options are protected by authorization codes to secure license protection. Each product family in the TI-ALS has one authorization code, three total, for TPC10, TPC12, and TPC14 Series. No authorization code is needed for a programming system or design synthesis library. Each software option requires an additional code.

TPC-ALS-DS-PC-VL
TI-ALS Design Software with Viewlogic Library, on PC
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic
Density Supported: Up to 2,500 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C PORT (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
TI-ALS Security Block	MS-DOS 3.30 or later

Description

This system provides the designer with software to complete designs with less than 2500 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DS-PC-VL

TPC-ALS-DA-PC-VL
TI-ALS Design Software with Viewlogic Library, on PC
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C PORT (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
TI-ALS Security Block	MS-DOS 3.30 or later

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-PC-VL

TPC-ALS-DS-PC-OR
TI-ALS Design Software with Orcad Library, on PC
Hardware Platform: 386/486-Based PC
CAE Environment: OrCAD
Density Supported: Up to 2,500 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
OrCAD Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C PORT (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
TI-ALS Security Block	MS-DOS 3.30 or later

Description

This system provides the designer with software to complete designs with less than 2500 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DS-PC-OR

TPC-ALS-DA-PC-OR
TI-ALS Design Software with Orcad Library, on PC
Hardware Platform: 386/486-Based PC
CAE Environment: OrCAD
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
OrCAD Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C PORT (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
TI-ALS Security Block	MS-DOS 3.30 or later

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-PC-OR

TPC-ALS-DA-SN-CD
TI-ALS Design Software with Cadence Library on Sun Workstation
Hardware Platform: Sun-4/Sparcstation2
CAE Environment: Cadence
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Cadence Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis Delay Time Back Annotation	Sun-4/Sparcstation2

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Cadence V4.2A on SUN platform with OS 4.1.1 or later version

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-SN-CD

TPC-ALS-DA-SN-MG
TI-ALS Design Software with Mentor Graphics Library on Sun Workstation
Hardware Platform: Sun-4/Sparcstation2
CAE Environment: Mentor
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Mentor Graphics Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	Sun-4/Sparcstation2

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Mentor V8.1 on SUN Platform with OS 4.1.1 or later version

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-SN-MG

TPC-ALS-245
TI-ALS
Hardware Platform: Sun-4/Sparcstation2
CAE Environment: Valid

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Valid Library TI-ALS for Valid Automatic Placement and Routing Timing Analysis	Sun-4/Sparcstation2 with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Valid Logic Schematic Capture with OS4.1.1

Description

The TPC-ALS-245 includes the TI-ALS FPGA software and macro libraries used to support schematic capture and delay time back annotation. The TPC-ALS-245 system provides the designer with the tools to complete both TPC10 and TPC12 Series FPGA designs including fusing and definition files that can be transferred to an FPGA programming system. Programming services are offered by TI distributors at local programming centers.

Ordering Information **PART NUMBER: TPC-ALS-245**

TPC-ALS-DA-SN-VL
TI-ALS Design Software with Viewlogic Library on Sun Workstation
Hardware Platform: Sun-4/Sparcstation2
CAE Environment: Viewlogic
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	Sun-4/Sparcstation2

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	TI-ALS V2.2 on Sun OS4.1.1 or later version

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-SN-VL

TPC-ALS-DA-HP7-MG
TI-ALS Design Software with Mentor Graphics Library on HP700 Workstation
Hardware Platform: HP700 Workstation
CAE Environment: Mentor
Density Supported: Up to 10,000 gates

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Mentor Graphics 8.1 Library TI-ALS V2.2 Automatic Placement and Routing Timing Analysis	HP700 Workstation

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	TI-ALS V2.2 fpr HP700 Workstation OS; HP-UX

Description

This system provides the designer with software to complete designs with less than 10,000 gates. The software includes capabilities for netlist validation, place and route, timing verification and fuse file generation. Fuse files can be transferred to a TI-ALS programming system or to a TI distributor with a local programming center.

Ordering Information: PART NUMBER: TPC-ALS-DA-HP7-MG

TPC-ALS-235
TI-ALS
Hardware Platform: HP/Apollo
CAE Environment: Mentor

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Mentor ibrary TI-ALS for Mentor: Automatic Placement and Routing Timing Analysis	HP 400 workstation or Apollo DN 3000/4000 workstation

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	NETED Release 7.1, AEGIS Release 10.3.5 Mentor Capture, Design, or IDEA station

Description

The TPC-ALS-235 includes the TI-ALS FPGA software and macro libraries used to support schematic capture and delay time backannotation. The TPC-ALS-235 system provides the designer with the tools to complete both TPC10 and TPC12 Series FPGA designs including fusing and definition files that can be transferred to an FPGA programming system. Programming services are offered by TI distributors at local programming centers.

Ordering Information **PART NUMBER: TPC-ALS-235**

TPC-ALS-DS-P2S-PC
Activator 2S Programmer, PC Interface
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic or OrCAD (Optional)

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS for 386/486-Based PC.	386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C PORT (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card Vacant 1/2 Card AT Bus Slot

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2S Programmer	TI-ALS for 386/486-Based PC MS-DOS 3.30 or later

Description

The activator 2S programming system provides support for all TPC series devices and connects to both the high and low density system configurations or can be used stand alone. The Activator 2S contains the programming circuitry to implement the antifusing sequence used to program a single FPGA. Optional debug and probe capabilities are available , TPC-ALS-218.

Ordering Information: **PART NUMBER: TPC-ALS-DS-P2S-PC.**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-219
Activator 2 Programmer
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic or OrCAD (optional)

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS for 386/486-based PC	Existing TPC-ALS system or 386/486-based PC with: 16 Megabytes RAM One parallel port One RS-232C port (COM1 or COM2) 40 Megabyte Hard Disk 1.2 or 1.44 Megabyte Floppy Drive EGA or Monochrome Graphics Card Vacant 1/2 Card AT Bus Slot

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2 Programmer	Existing TPC-ALS PC system

Description

The TPC-ALS-219 TI-ALS Programming System includes FPGA software and hardware that can be used stand alone or added to an existing TPS-ALS design system to provide the designer with tools to program TI FPGAs. The Activator 2 contains the programming circuitry required to implement the antifusing sequence used to program up to four FPGAs simultaneously.

Optional debug and probe capabilities are available, TPC-ALS-218.

Ordering Information **PART NUMBER: TPC-ALS-219**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-DS-P2S-SN
Activator 2S Programmer, Sun Workstation
Hardware Platform: Sun-4/SparcStation2
CAE Environment: Valid, Viewlogic, Mentor, or Cadence (Optional)

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS for Valid or Viewlogic, Cadence or Mentor	Sun-4/SparcStation2 with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2S Programmer	TPC-ALS Viewlogic, Valid, Cadence, or Mentor on SUN OS4.1.1

Description

The activator 2S programming system provides support for all TPC series devices and connects to the high density system configurations or can be used stand alone. The Activator 2S contains the programming circuitry to implement the antifusing sequence used to program a single FPGA. Optional debug and probe capabilities are available , TPC-ALS-218.

Ordering Information: **PART NUMBER: TPC-ALS-DS-P2S-SN.**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-249
Activator 2 Programmer
Hardware Platform: Sun-4/Sparcstation2
CAE Environment: Valid or Viewlogic (optional)

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS for Valid or Viewlogic	Sun-4/Sparcstation2 CAE with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2 Programmer	Existing TPC-ALS Viewlogic or Valid on Sun OS4.1.1

Description

The TPC-ALS-249 TI-ALS Programming System includes FPGA software and hardware that can be used stand alone or added to an existing TPS-ALS system to provide the designer with the tools to program TI FPGAs. The Activator 2 contains the programming circuitry required to implement the antifusing sequence used to program up to four FPGAs simultaneously.

Ordering Information **PART NUMBER: TPC-ALS-249**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-DS-P2S-HP7
Activator 2S Programmer, HP700 Workstation
Hardware Platform: HP700 Workstation
CAE Environment: Mentor Graphics

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS V2.2 for Mentor	HP700 Workstation with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2S Programmer	TPC-ALS V2.2 for HP700 Workstation OS; HP-UX

Description

The activator 2S programming system provides support for all TPC series devices and connects to the high density system configurations or can be used stand alone. The Activator 2S contains the programming circuitry to implement the antifusing sequence used to program a single FPGA. Optional debug and probe capabilities are available , TPC-ALS-218.

Ordering Information: PART NUMBER: TPC-ALS-DS-P2S-HP7.

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-DS-P2-HP7
Activator 2 Programmer, HP700 Workstation
Hardware Platform: HP700 Workstation
CAE Environment: Mentor Graphics

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS V2.2 for Mentor	HP700 Workstation with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2 Programmer	TPC-ALS V2.2 for HP700 Workstation OS; HP-UX

Description

The activator 2 programming system provides support for all TPC series devices and connects to the high density system configurations or can be used stand alone. The Activator 2 contains the programming circuitry to implement the antifusing sequence used to program up to four FPGAs simultaneously. Optional debug and probe capabilities are available, TPC-ALS-218.

Ordering Information: **PART NUMBER: TPC-ALS-DS-P2-HP7.**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-DS-P2S-HP4
Activator 2S Programmer, HP400 Workstation
Hardware Platform: HP400 Workstation
CAE Environment: Mentor Graphics

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS V2.2 for Mentor	HP400 Workstation with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2S Programmer	Existing TPC-ALS for Mentor System OS; Aegis Release 10.3.5

Description

The activator 2S programming system provides support for all TPC series devices and connects to the high density system configurations or can be used stand alone. The Activator 2S contains the programming circuitry to implement the antifusing sequence used to program a single FPGA. Optional debug and probe capabilities are available , TPC-ALS-218.

Ordering Information: **PART NUMBER: TPC-ALS-DS-P2S-HP4.**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-DS-P2-HP4
Activator 2 Programmer, HP400 Workstation
Hardware Platform: HP400 Workstation
CAE Environment: Mentor Graphics

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS V2.2 for Mentor	HP400 Workstation with SCSI Parallel Port

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2 Programmer	Existing TPC-ALS for Mentor System OS; Aegis Release 10.3.5

Description

The activator 2 programming system provides support for all TPC series devices and connects to the high density system configurations or can be used stand alone. The Activator 2 contains the programming circuitry to implement the antifusing sequence used to program up to four FPGAs simultaneously. Optional debug and probe capabilities are available, TPC-ALS-218.

Ordering Information: **PART NUMBER: TPC-ALS-DS-P2-HP4**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-239
Activator 2 Programmer
Hardware Platform: HP/Apollo
CAE Environment: Mentor (optional)

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS for Mentor	Apollo DN 3000/4000 workstation

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Activator 2 Programmer	Existing TPC-ALS Mentor system AEGIS Release 10.3.5

Description

The TPC-ALS-239 TI-ALS Programming System includes FPGA software and hardware that can be used stand alone or added to an existing TPS-ALS Mentor system to provide the designer with the tools to program TI FPGAs. The Activator 2 contains the programming circuitry required to implement the antifusing sequence used to program up to four FPGAs simultaneously.

Optional debug and probe capabilities are available, TPC-ALS-218.

Note that a SCSI card is provided. Where a SCSI port exists, the add-in card is not needed.

Ordering Information **PART NUMBER: TPC-ALS-239**

Note:

Programming module required for Activator 2, ordered separately, see Table 4–4.

TPC-ALS-016
High Density Viewsim Simulator
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic simulation software Viewlogic Magic Number required to enable software	Existing TI-ALS PC system

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Existing TI-ALS PC system

Description

The TPC-ALS-016 Viewlogic simulation option includes Viewsim and Viewwave™ with the capability to simulate designs of all TPC Series devices. The resident TI-ALS software and hardware provides the designer with the tools to complete FPGA design and simulation. Magic number is supplied upon request, after receipt of the system.

Ordering Information **PART NUMBER: TPC-ALS-016**

TPC-ALS-017
Low Density Viewsim Simulator
Hardware Platform: 386/486-Based PC
CAE Environment: Viewlogic

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic simulation software Viewlogic Magic Number required to enable software	Existing TI-ALS PC system

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Existing TI-ALS PC system

Description

The TPC-ALS-017 Viewlogic simulation option includes Viewsim and Viewwave, with capability to simulate designs of up to 3,000 gate complexities. The resident TI-ALS software and hardware provides the designer with the tools to complete FPGA design and simulation. Magic number is supplied upon request, after receipt of the system.

Ordering Information **PART NUMBER: TPC-ALS-017**

TPC-ALS-VL-005
Viewlogic Schematic Capture, Viewdraw
Hardware Platform: 386/486-Based PC

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic Schematic Capture or Viewdraw	386/486-based PC

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	MS-DOS 3.30 or later

Description

Viewlogic's schematic capture tool, Viewdraw, enables the engineer to design circuits utilizing a graphic format. TI FPGAs libraries based upon TTL functions and optimized for TI's architecture provide designers with over 250 elements to describe their circuits. Each library element is comprised of a graphical symbol, logic description, and timing model. Once the design is captured, it can be simulated with Viewlogic simulation software, or an ALS compatible design data base generated for input into the TI-ALS system.

Ordering Information: PART NUMBER: TPC-ALS-VL-005

TPC-ALS-VL-001
Viewlogic Schematic Generation, Viewgen
Hardware Platform: 386/486-Based PC

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Viewlogic Schematic Generation, Viewgen	386/486-Based PC

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	MS-DOS 3.30 or later

Description

Viewlogic's schematic generation and regeneration give the designer the capability to output a schematic during the design process for easier system debug and documentation. Viewgen is especially helpful for outputting a schematic after synthesis, so that a graphical representation of the gate level circuit can be better analyzed and understood.

Ordering Information: PART NUMBER: TPC-ALS-VL-001

** ADVANCE INFORMATION **

TPC-ALS-PLDSYN
Boolean Synthesis and FPGA Optimization
Hardware Platform: 386/486-Based PC

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
Boolean Synthesis and FPGA Optimization tool	386/486-Based PC

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	MS-DOS 3.30 or later

Description

Developed by Exemplar Logic, the TPC-ALS-PLDSYN is an FPGA logic synthesis and optimization tool. Synthesis algorithms take advantage of TI's unique architecture for significant area reduction compared to other CAE tools. The TPC-ALS-PLDSYN gives the PLD designer access to FPGA technology through familiar design methodologies utilizing PALASM and CUPL (boolean entry) or allows quick and easy conversion of PLD designs to TI FPGAs.

Ordering Information: PART NUMBER: TPC-ALS-PLDSYN

TPC-ALS-218
Universal Actionprobe for Test and Debug
Hardware Platform: 386/486-Based PC
Apollo DN 3000/4000 Workstation and HP 400/700 Workstation
Sun4/Sparcstation2 Workstation
CAE Environment: See Table 4–1

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-ALS software TI-ALS test and debug authorization code	Any of the computer system combinations listed above: Activator 2 programmer TI-ALS security block

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
Universal Actionprobe	Existing TI-ALS PC system

Description

The Universal Actionprobe Diagnostic Tool consists of the Actionprobe adapter hardware and the In-Circuit Probe (ICP) support software. The Actionprobe adapter connects at one end, by a cable, to a port on the Activator 2, and at the other end, by wires and probe clips, to the probe posts set up for a chip on the user's circuit board. ICP support software is accessed from the Debug menu.

Ordering Information **PART NUMBER: TPC-ALS-218**

Note:

Debug systems are delivered without the TI-ALS security block. If a stand alone Activator 2 programmer is the target machine for the Actionprobe option, a TI-ALS security block is needed. Contact the TI Field Programmable Logic (FPL) Customer Support Helpline at (214) 997-5666 to request a TI-ALS security block. All other systems can be configured for the test and debug option at the time of shipment receipt.

TPC-ALS-SYN-S4
TI-Synopsys Libraries for Design Compiler
Hardware Platform: Sun-4/Sparcstation2

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-Synopsys Libraries for Design Compiler	Sun-4/Sparcstation2
HARDWARE SUPPLIED:	**SOFTWARE REQUIREMENTS:**
None	TI-ALS Design software Sun OS4.1.1

Description

Synopsys synthesis library affords the designer the flexibility to design in multiple formats (VHDL and Verilog behavioral design, Boolean equations, state machines, etc.) and output a design to the TI-ALS design software. During synthesis, the designer also has the option of optimizing the design data base to maximize performance and density.

Ordering Information: PART NUMBER: TPC-ALS-SYN-S4

TPC-ALS-SYN-HP
TI-Synopsys Libraries for Design Compiler
Hardware Platform: HP700

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-Synopsys Libraries for Design Compiler	HP700 Workstation

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	HP-UX running on HP700

Description

Synopsys synthesis library affords the designer the flexibility to design in multiple formats (VHDL and Verilog behavioral design, Boolean equations, state machines, etc.) and output a design to the TI-ALS design software. During synthesis, the designer also has the option of optimizing the design data base to maximize performance and density.

Ordering Information: PART NUMBER: TPC-ALS-SYN-HP

TPC-ALS-SYN-DN
TI-Synopsys Libraries for Design Compiler
Hardware Platform: Apollo DN4000

SOFTWARE SUPPLIED:	HARDWARE REQUIREMENTS:
TI-Synopsys Libraries for Design Compiler	Apollo DN4000 Workstation

HARDWARE SUPPLIED:	SOFTWARE REQUIREMENTS:
None	Aegis Release 10.3.5 running on DN4000

Description

Synopsys synthesis library affords the designer the flexibility to design in multiple formats (VHDL and Verilog behavioral design, Boolean equations, state machines, etc.) and output a design to the TI-ALS design software. During synthesis, the designer also has the option of optimizing the design data base to maximize performance and density.

Ordering Information: PART NUMBER: TPC-ALS-SYN-DN

5 Quality and Reliability Data

Chapter 5

Quality and Reliability Data

Provides antifuse reliability studies and graphs, under license from Actel Corporation. Details the Texas Instruments quality and reliability tests and their data reports for the TPC Series FPGA products.

5.1 Introduction

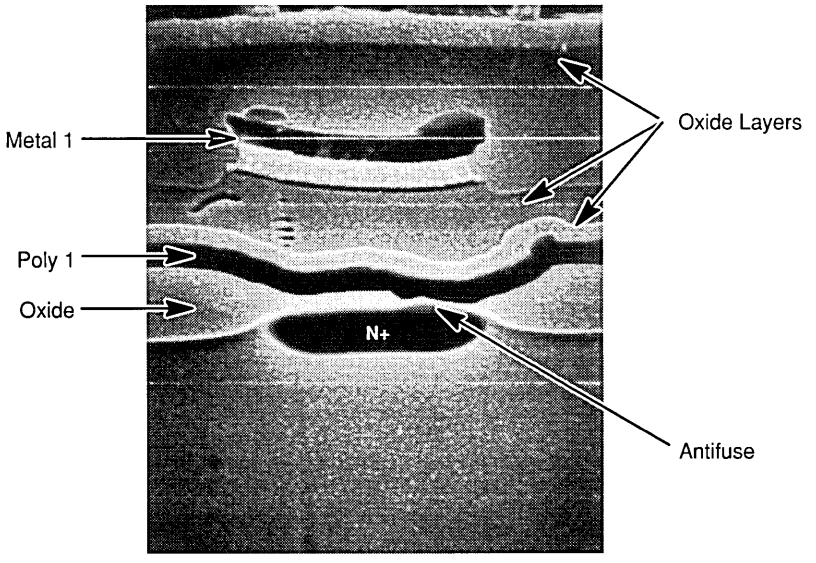
The reliability of Texas Instruments (TI) field-programmable gate arrays (FPGAs) is the result of all phases of the manufacturing processes: design, fabrication, assembly, and test. Since all of these are standard processes, this report will focus on the antifuse structure and describe the methods used to obtain antifuse reliability data. The other FPGA fabrication process steps are consistent with standard CMOS devices.

TI is currently producing FPGAs using TI standard 1.2- and 1.0-μm CMOS technologies. Both of these standard double-level metal (DLM) CMOS processes use three additional mask steps to integrate the antifuse element.

The antifuse is a normally open, vertical, two-terminal structure in which an electrical connection is made by the application of a programming voltage. The programmed on-resistance is typically 500 ohms, and the unprogrammed resistance exceeds 100 megohms. The number of antifuses ranges from 112 k on the TPC1010A device to 750 k on the TPC1280, but only 2% to 3% of the total are programmed for a typical application. In 1.2-μm CMOS technology the antifuse has an area of 1.4 μm^2, and in the 1.0-μm CMOS technology it has an area of 1.0 μm^2.

Because TI uses the PLICE™ antifuse, under license from Actel, the accompanying reliability graphs and studies of the antifuse apply to TI products as well. The antifuse is constructed using an oxide-nitride-oxide, ONO, dielectric layer between polysilicon on the top and N+ diffusion on the bottom. Figure 5–1 shows a cross-section of the antifuse. The results of these studies show that the time-to-failure of the antifuse is much greater than 40 years at normal operating conditions, and therefore compares to the reliability of the CMOS process. The combined contribution of all antifuses to the device's failure rate is less than 10 FITs (Failures-In-Time), or 10 or fewer failures out of 1 million units per 1000 hours of operation.

Figure 5–1. Antifuse SEM Cross-Section



The studies used three different test techniques to determine the antifuse reliability: 1) time-dependent dielectric breakdown, TDDB, of unprogrammed antifuses, 2) high-voltage stressing during production wafer sort for calculated time intervals, and 3) accelerated life testing of FPGAs utilizing programmed antifuses. It is important to note that high-voltage stressing and accelerated burn-in are performed routinely in production. Each die is subjected to high-voltage stress screening at both speed sort and final test, and packaged samples of each wafer lot are programmed and functionally tested. Periodic reliability monitor testing is performed and reported on production material. The process parameters that determine TDDB are monitored throughout the fabrication (fab) process and tightly controlled within specified limits.

5.2 The Unprogrammed Antifuse

Note:

The following information on **The Unprogrammed Antifuse** has been provided by the Actel Corporation.

In order to evaluate antifuse reliability, Actel has developed models and collected data for both unprogrammed and programmed antifuses[1,2]. We'll consider the unprogrammed antifuse first. Since the antifuse is a dielectric sandwiched between polysilicon and silicon, the model for its reliability, in the unprogrammed condition, is the same as that used to evaluate reliability of MOS transistor gate oxides[3]. The parameter we wish to evaluate is the time to breakdown (t_{bd}) of the dielectric. This parameter is a function of the electric field across the dielectric as well as temperature and has the following relationship[3].

$$t_{bd} = t_0 \bullet \exp(G/E) \quad (1)$$

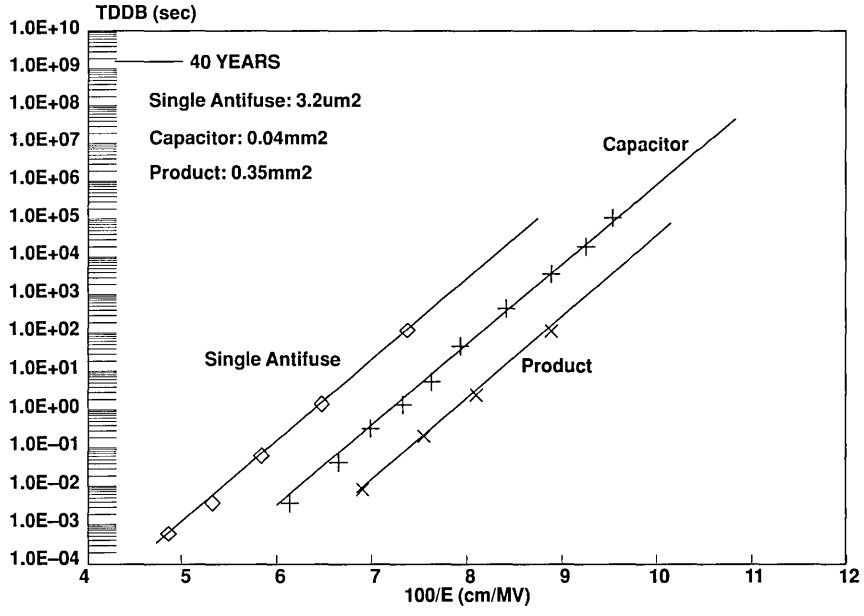
where t_{bd} is the time to breakdown in seconds, t_0 is a constant in seconds, E is the electric field in MV/cm, and G is the field acceleration factor in MV/cm (G is temperature dependent and will be discussed later).

By taking the log of both sides of equation 1 we have:

$$\ln(t_{bd}) = G \bullet (1/E) + \ln(t_0) \quad (2)$$

From experimental data, we can plot the log of the time to breakdown of the antifuse at various temperatures versus the reciprocal of the electric field across it and derive G from the slope and t_0 from the Y intercept. Actel has done this on single antifuses, large antifuse capacitors, test arrays of 28,000 antifuses, and actual A1010/A1020 products. These antifuse areas range from 3.2 μm^2 to 0.35 mm^2. Figure 5–2 shows plots of data collected on these different sized antifuses.

Figure 5–2. Field Accelerated Test



There is some discussion in the referenced literature regarding whether time to breakdown depends on E or 1/E. To verify the validity of equation 2, we conducted the following experiment. Large 200 μm by 200 μm (0.04 mm^2) area capacitors were packaged and then stressed at more than eleven different voltages. Capacitors were chosen from two different wafer runs with thicknesses ranging from a low of 8.0 nm to a high of 9.5 nm. A total of 610 capacitors were used in the experiment. The test splits and sample sizes are summarized in Table 5–1.

Table 5–1. Field Accelerated Test Data for Two Lots with Thicknesses Ranging from 8 nm to 9.5 nm (The test was done on 0.04 mm^2 area capacitor.)

Lot A					Lot B				
Voltage (V)	Tox (nm)	E-Field (MV/cm)	No. of Capacitors	t_{50} (sec)	Voltage (V)	Tox (nm)	E-Field (MV/cm)	No. of Capacitors	t_{50} (sec)
13.5	8.3	16.2	22	4.2 e–3	14.0	8.7	15.9	25	9.8 e–3
12.5	8.3	15.1	22	3.7 e–2	13.0	8.7	14.9	25	5.0 e–2
12.0	8.3	14.4	22	1.5 e–1	12.5	8.7	14.3	25	2.4 e–1
11.5	8.3	13.8	22	8.6 e–1	12.0	8.7	13.7	25	1.3 e0
11.0	8.4	13.1	22	4.7 e0	11.4	8.7	13.1	25	9.0 e0
10.5	8.4	12.5	9	5.8 e1	11.2	8.7	12.5	45	8.0 e1
10.0	8.3	12.0	6	3.2 e2	10.8	9.0	12.0	45	3.52 e2
9.5	8.3	11.4	6	2.5 e3	10.2	9.0	11.3	45	2.88 e3
9.0	8.3	10.7	36	2.5 e4	9.7	9.0	10.8	45	2.07 e4
8.5	8.3	10.2	15	2.3 e5	9.0	8.7	10.3	32	3.35 e5
8.0	8.3	9.6	59	1.5 e6	9.0	9.3	9.7	32	2.22 e6
Subtotal of tested capacitors			241					369	
Total of tested capacitors			610						

The distribution of time to breakdown of the dielectric at each voltage is shown in Figure 5–3. In Figure 5–4, we plot the median of the cumulative failure percentage rates t_{50} from Figure 5–3 versus 1/E. In Figure 5–5 the median failure percentage is plotted versus E. By comparing the two figures, the validity of the 1/E model is clearly established. A more detailed statistical verification of the 1/E model for the ONO antifuse is given in Reference [2].

Figure 5–3. TDDB Distribution

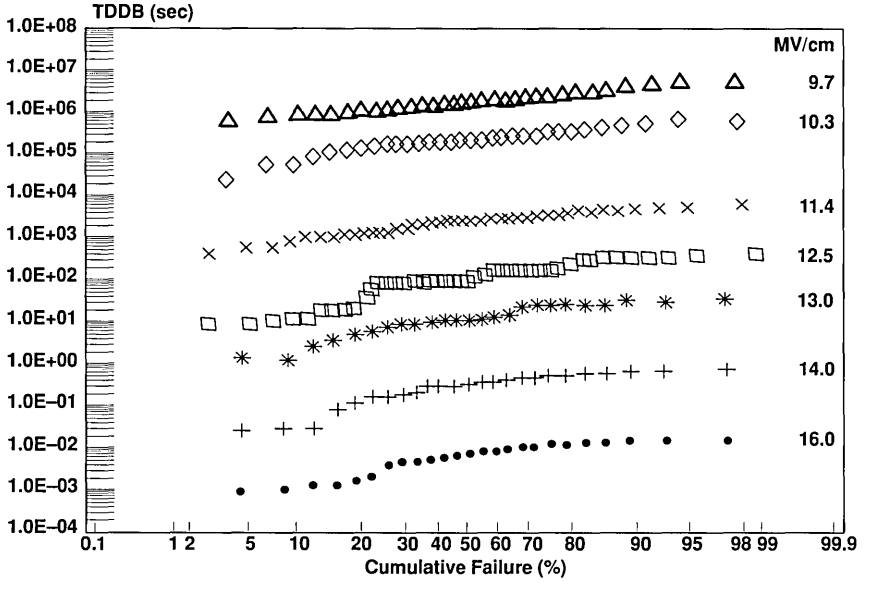


Figure 5–4. ONO Reliability (1 IE Model)

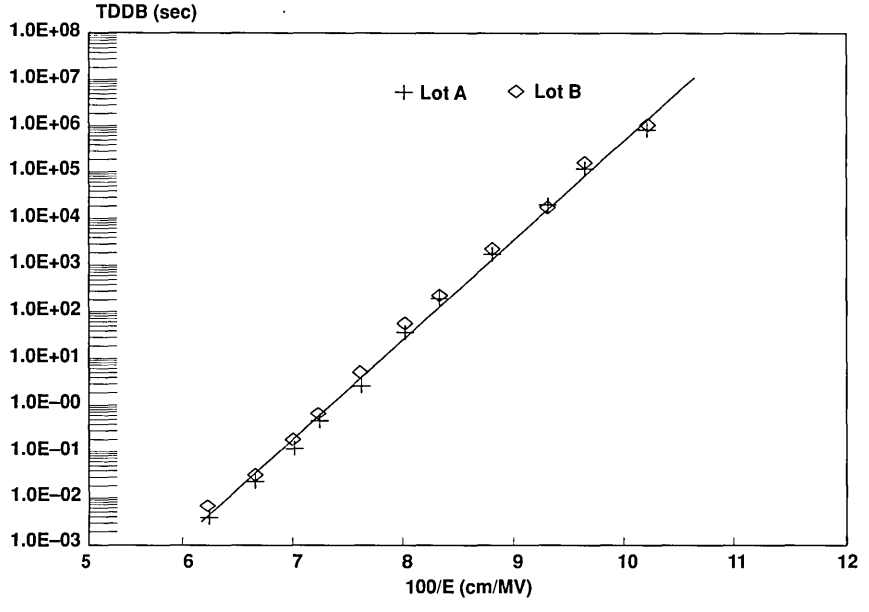
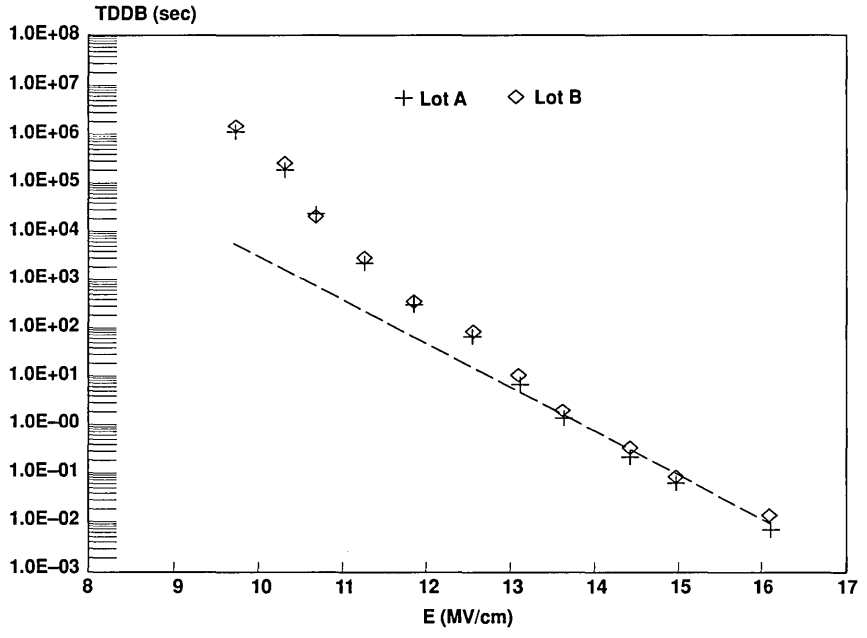


Figure 5–5. ONO Reliability (E Model)



In order to quantify the temperature dependence of the time to breakdown, we use the Arrhenius equation to determine the semiconductor failure rate of a given process (failure mode) over temperature:

$$R = R_0 \bullet \exp(E_a/kT) \quad (3)$$

where R is the failure rate, R_0 is a constant for a particular process, T is the absolute temperature in degrees Kelvin, k is Boltzmann's constant (8.62 X 10^{-5} eV/°K) and E_a is the activation energy for the process in electron volts. To determine the acceleration factor for a given failure mode at temperature T_2 as compared with temperature T_1 we use equation 3 to derive:

$$A(T_1, T_2) = \exp[(E_a/k) \bullet \{(1/T_1) - (1/T_2)\}] \quad (4)$$

where A is the acceleration factor.

In Figure 5–6 we plot t_{50} at different temperatures and electric fields. This plot shows that time to breakdown is dependent on temperature as well as electric field. For a given time to breakdown of a dielectric, the expression,

$$E_a = k \bullet d\ln(t_{bd})/d(1/T) \quad (5)$$

gives us the activation energy[2]. The slope in Figure 5–6 represents the activation energy E_a. E_a also shows a linear correlation with 1/E as shown in Figure 5–7. The field acceleration factor, G, is also temperature dependent, i.e.,

$$G(T) = G(298) \bullet [1 + \delta/k \bullet \{1/T - 1/298\}] \quad (6)$$

where G(298) is the field acceleration factor at room temperature (25°C = 298°K) and δ (in eV) characterizes the temperature dependence of G.

By combining equations 1, 5, and 6, E_a can be related to G(T) by:

$$E_a = G(298) \bullet \delta/E - E_b \quad (7)$$

where δ and E_b are treated as fitting parameters between E_a and G.

From the data shown in Figures 3, 4, 6, and 7 we can obtain values of G(298), δ, E_b, and E_a regardless of antifuse area. Typical values of G(298), δ, E_b, and E_a at 5.5 V are 480 MV/cm, 0.014 eV, 0.43 eV, and 1 X 10^{-16}. By combining equations 1, 6, and 7, we obtain an overall equation for the time to breakdown for a given temperature and E field:

$$t_{bd} = t_0 \bullet \exp\{(G(298)/E)\,[1 + (\delta/k) \bullet (1/T - 1/298)] - (E_{b/k}) \bullet (1/T - 1/298)\} \quad (8)$$

By applying the values for the constants as defined above, the time to breakdown for the antifuse dielectric can be derived for a given temperature and electric field. In Table 5–2, we have used equation 8 to solve for the acceleration factors associated with powering up a device at high voltage and/or temperature and comparing the failure rate with more typical voltages and temperatures. We can see the effect of temperature by comparing 125°C at 5.5 V with 55°C at 5.5 V in which the Actel model (equation 8) gives us an acceleration factor of 55.3 or 6.3 equivalent years for a 1000 hour burn-in at 125°C. Note that this acceleration factor of 55.3 is close to the value of 41.8 derived from the Arrhenius equation (equation 4) using an activation energy of 0.6 eV and the same temperatures. Actel uses 0.6 eV (and 0.9 eV) as a general semiconductor failure mode activation energy when calculating failure rates from high temperature operating life (HTOL) later in this report.

Figure 5–6. Dependence of E-Field Acceleration on Temperature

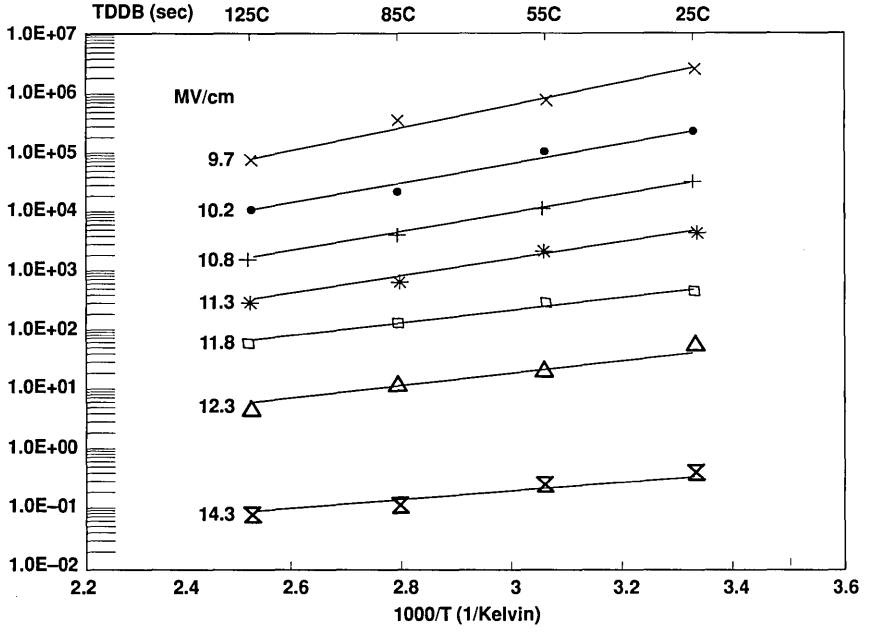


Figure 5–7. Activation Energy versus 1 IE

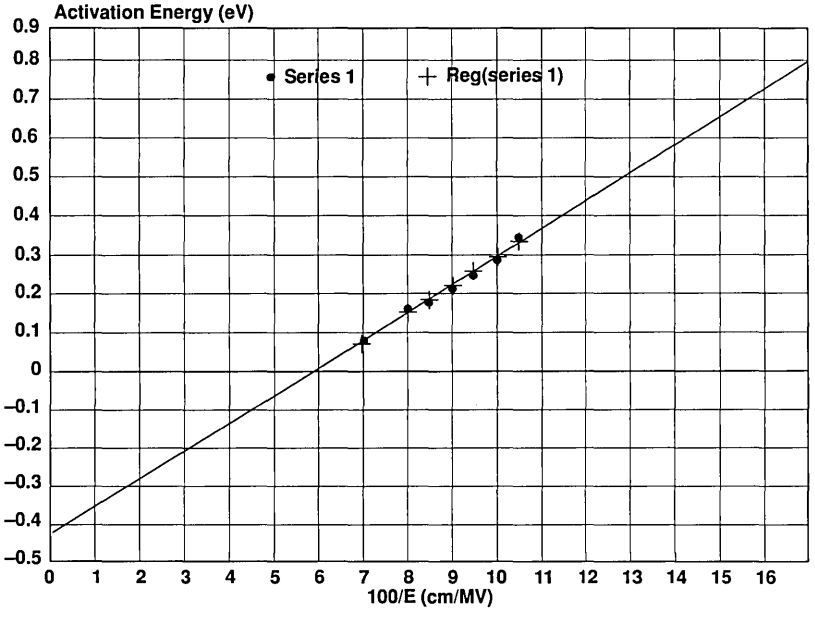


Table 5–2. Acceleration Factor vs Operating Conditions (Unprogrammed Antifuse)
t_0 = 1 X 10^{-16} sec., G = 480 MV/cm, δ = 0.014 eV, E_b = 0.43 eV

Model	Temperature/Voltage		Acceleration Factor	Equivalent Years for 1000 Hour 125°C Burn-In
	High	Typical		
Fixed Voltage	125°C/5.5 V	55°C/5.5 V	55.3	6.3
	125°C/5.5 V	90°C/5.5 V	6.1	0.7
Fixed Temperature	25°C/5.5 V	25°C/5.25 V	38.8	4.4
	25°C/5.75 V	25°C/5.25 V	1092.6	124.7
	25°C/5.75 V	25°C/5.5 V	28.2	3.2
	25°C/6.0 V	25°C/5.25 V	23321	2662
	25°C/6.0 V	25°C/5.5 V	601.8	68.7
Varied Temperature and Voltage	125°C/5.5 V	55°C/5.25 V	1787.2	204.0
	125°C/5.75 V	55°C/5.5 V	987.8	112.8
	125°C/5.75 V	90°C/5.5 V	109.4	12.5
	125°C/6.0 V	55°C/5.5 V	13865	1583
	125°C/6.0 V	90°C/5.5 V	1535.9	175.3
Fixed 0.6 eV Activation Energy Voltage – Independent	150°C/5.5 V	55°C/5.5 V	117.6	13.4
	150°C/5.5 V	90°C/5.5 V	15.2	1.7
	125°C/5.5 V	55°C/5.5 V	41.8	4.8
	125°C/5.5 V	90°C/5.5 V	5.4	0.6

We can also see from Table 5–2 that a small change in voltage is a much more effective reliability screen than is a change in temperature. For example, if we compare 25°C at 5.75 V to 25°C at 5.25 V we see that just a half volt change yields an acceleration factor of 1092.6, or 124.7 equivalent years per 1000 hours at 5.75 V. This strong dependence on voltage allows Actel to screen out antifuse infant mortality failures during normal wafer sort testing simply by performing a special test in which a higher than normal voltage is applied across all antifuses. Because antifuse infant mortality failures can be detected and effectively screened, A1010/A1020 devices have as high a level of reliability as standard CMOS processed products.

In order to establish that the antifuse contributes less than 10 FITs (at 5.5 V, 125°C) to the overall product reliability, Actel has calculated the product failure rates due to the antifuse using three different techniques. In the first case, we evaluated the t_{bd} distribution of 125 A1010 units in which the antifuses received an 11 V stress. Using E_a = 0.9 eV and extrapolating to 5.5 V, we find that the 1% antifuse failure lifetime at 5.5 V is well over 40 years and less than 10 FITs.

The second method of determining product reliability was to look at production wafer sort results. As was mentioned earlier, all antifuses receive a high voltage stress at wafer sort to screen out infant mortality failures. Specifically, all antifuses receive the equivalent of two, 10 V stresses for one second each. The first stress is to screen out clearly defective antifuses. The second stress is to catch weaker antifuses which could cause product programming yield problems or infant mortality failures. Actual failure rates observed on the A1010 over ten runs for these two stresses (FS-1 and FS-2) demonstrate average yield loss at the second stress screen of less than 0.3%. By extrapolating this yield loss to a normal 5.5 V operating voltage, we thus conclude that the contribution of the antifuse to the overall product's lifetime is less than 10 FITs.

The third technique of determining the product's antifuse failure rate is by doing an accelerated burn-in of A1010/A1020 products. The acceleration is accomplished by using both higher voltage (5.75 V to 6.0 V) and high temperature (125°C to 150°C). Units are programmed to a specific design and exercised in a manner similar to what may occur in a real application. Here, too, the conclusion is that the antifuse contributes less than 10 FITs to the product's overall failure rate and it is thus an insignificant factor in product lifetime of 40 years at 5.5 V and 125°C.

References:

1) E. Hamdy, et al, "Dielectric Based Antifuse for Logic and Memory ICs", IEDM Paper, pgs 786–789, 1988.

2) S. Chiang, et al, "Oxide-Nitride-Oxide Antifuse Reliability", Proc. Int. Rel. Phys. Symp., 1990.

3) J. Lee, I-Chen, and C. Hu, "Modeling and Characterization of Gate Oxide Reliability", IEEE Trans. of Elec. Dev., December 1988.

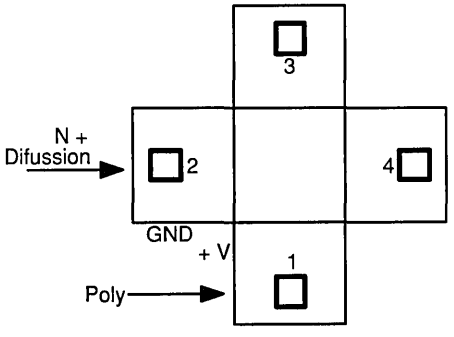
5.3 The Programmed Antifuse

Note:

The following information on **The Programmed Antifuse** has been provided by the Actel Corporation.

A Kelvin test structure as shown in Figure 5–8 was used to evaluate reliability of a programmed antifuse. Here, a strip of polysilicon crosses an N+ diffusion. The antifuse is located at their intersection. There are metal-to-poly contacts at nodes 1 and 3 as well as metal-to-N+ contacts at nodes 2 and 4. A four terminal Kelvin structure is useful should a failure occur, because antifuse opens can be separated from other problems (such as polysilicon or contact opens) simply by checking for continuity on appropriate pairs of nodes.

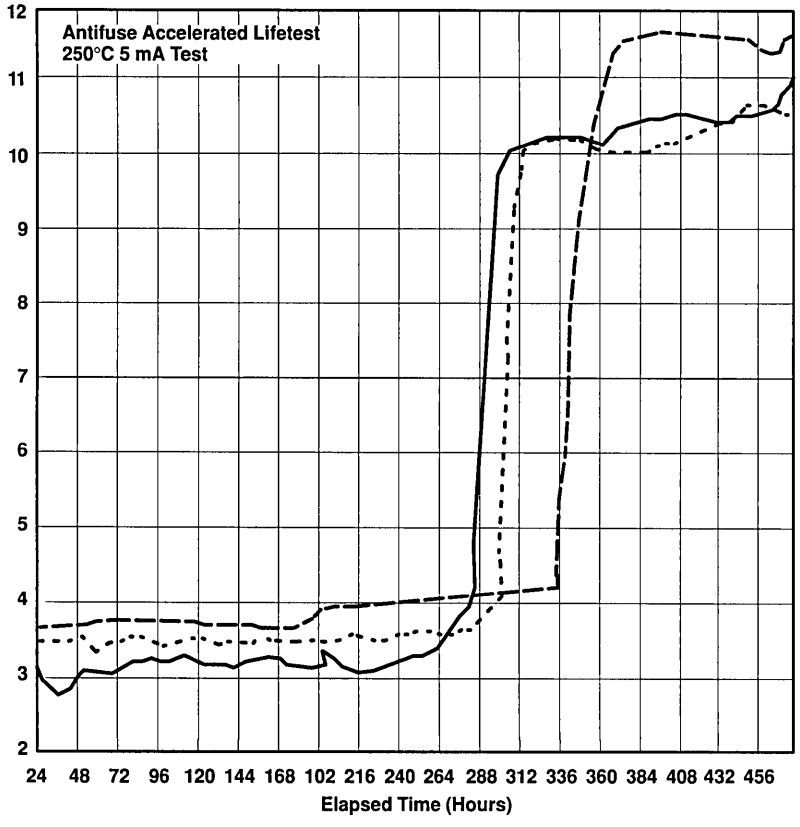
Figure 5–8. Antifuse Kelvin Structure



Test devices were stressed by forcing a constant 5 mA current from polysilicon to N+ through the antifuse at 250°C. Note that this stress is far greater than a programmed antifuse would see in a device under normal operating conditions. Because the antifuse is used to connect two networks together, there is usually no voltage across it and hence no current passes through. A voltage will appear across the antifuse only momentarily while a network switches from low-to-high or high-to-low.

During the 5 mA, 250°C stress, the voltage across the antifuse was monitored. Figure 5–9 is a plot of the monitored voltage as a function of stress time. A sudden increase in voltage indicates that an open occurred. As can be seen from Figure 5–9, failures occurred at about 300 hours of stress. However, by probing on nodes 3 and 4 of the Kelvin structure, we were able to measure continuity and determine that the cause of failure was not the antifuse. The failed units were then examined on an SEM, where the cause of failure was revealed as metal-to-poly contact electromigration. This is a well-known failure mode in CMOS, which has been determined to have an activation energy of 0.9 eV. Using equation 4 we can predict a lifetime under normal operating conditions in excess of 40 years for this failure mode. The lifetime of the programmed antifuse is even longer.

Figure 5–9. Voltage Across Antifuse vs Stress Time



5.4 Texas Instruments Quality and Reliability of FPGA Products

Texas Instruments commitment to providing products of the highest quality and reliability is implemented through an established program that includes qualification and characterization testing of new products and processes, reliability monitor testing of existing product, lot acceptance testing of production material, and the use of statistical process monitors to control critical parameters in the wafer fab and assembly sites.

5.4.1 Qualification and Reliability Monitor Testing

All new FPGA products must undergo stringent qualification testing to ensure their reliability. The testing is governed by TI specification QSS 009-401 which defines the tests required for each product type along with minimum sample sizes and any special requirements. In addition, any major change to the wafer fab process or assembly and test process must undergo similar qualification testing along with adequate customer notification. Changes which are considered major are listed in TI specification QSS 009-001.

The following chart shows the minimum testing required for a standard qualification program for a new device design in a previously qualified plastic encapsulated package.

TEST	CONDITIONS	DURATION/ STRESS	SS/F
Operating Life	Dynamic, 125°C	1000 Hours	129/0
Storage Life	Unbiased, 150°C	1000 Hours	45/0
Biased Humidity	Alternate Pin Bias, 85°C/85% Rh	1000 Hours	76/0
Temperature Cycle	Air- To- Air, –65°C / +150°C	1000 Cycles	76/0
Thermal Shock	Liquid-To-Liquid, –65°C/+150°C	200 Cycles	45/0
Autoclave	121°C,15 PSIG	240 Hours	45/0
ESD	Mil-Std-883C, Cond 3015.7, Notice 8, Human Body Model	2 kV	3/0
Latchup	JEDEC Standard 17	250 mA	6/0

5.4.2 Operating Life Test

Operating life test is a high-temperature test under bias used to accelerate semiconductor failure mechanisms. The bias can be either dynamic or static. During the dynamic test the inputs are switching in such a manner as to cause the internal circuitry to toggle as it would under normal operation. During the static test a fixed voltage is applied to the inputs and the internal circuitry of the device does not switch. The outputs are typically biased in such a manner that they will source or sink current depending on the state of the output.

5.4.3 Storage Life Test

Storage life test is a non-biased high-temperature test. This test is typically performed at a minimum temperature of 150°C. The purpose of this test is to evaluate the integrity and reliability of the bonding systems. In plastic encapsulated packages a degradation of the flame retardant system can accelerate the formation of excessive gold/aluminum ball bond intermetallics. The excessive intermetallic formation can progress to the point of electrical failure of the device. This type of failure is known as Kirkendall voiding.

5.4.4 Biased Humidity

This test is designed to measure a devices susceptibility to electrolysis and electrolytic corrosion.

During this test devices are subjected to a high-temperature/high-humidity environment with bias voltage applied. The temperature and humidity range can vary considerably. Under standard testing the temperature range typically is between 50°C to 85°C while the relative humidity ranges between 30% to 85%.

During normal qualification testing of TI FPGA devices a standard 85°C/85% relative humidity condition is used. An alternate pin bias procedure is used to bias the devices under test. In this procedure, adjacent I/O pins are alternated between a high or low voltage bias, while ground and power pins are held at normal bias. This particular bias procedure has been shown to be a worst-case test for the electrolytic corrosion failure mechanism.

5.4.5 Temperature Cycle and Thermal Shock

These two tests are designed to determine the thermomechanical compatibility of materials used in device construction. These tests require cycling of the ambient temperature of the device environment from a low temperature to a high temperature during a specified time period. These temperature extremes are not intended to simulate actual operation, but rather to exaggerate any thermomechanical mismatches that may exist. The temperature cycle test is performed in a gas environment, while the thermal-shock test is performed in a liquid environment.

Several different standard temperature extremes have been used for testing purposes. For qualification of TI FPGA devices the condition of –65°C to 150°C is used.

5.4.6 Autoclave Testing

This environmental test involves exposing the devices to an atmosphere of high-temperature, saturated steam under pressure. Normally this is performed at 121°C with 100% relative humidity at 15 PSIG. Unlike the biased humidity test, no electrical bias is applied to the devices while under stress. This test is used to indicate the susceptibility of a device to galvanic corrosion. Therefore, the electromotive forces of the elements involved are of great concern. The chemical instability of the encapsulating material, and its tendency to form electrolytes, will influence the number of failures that results from this test.

5.4.7 Electrostatic Discharge (ESD) Testing

This test is used to determine the electrostatic discharge sensitivity threshold of a device. The test consists of applying current pulses of known intensity and duration to individual pins of a device. TI FPGA devices are ESD tested according to Military Standard 883C, Condition 3015.7, Notice 8. This condition simulates the human body model for electrostatic discharge.

5.4.8 Latch Up

Latch-up testing is used to determine a particular device's susceptibility of inherent parasitic transistors from being biased in such a way as to latch at a low-impedance state between V_{CC} and ground, thus causing a high current flow through the device. This high current flow can result in either a nonfunctional device or a severely damaged device.

TI FPGA devices are tested for latch-up susceptibility in accordance with the procedures specified in JEDEC Standard 17.

5.4.9 Reliability Monitor Testing

After TI FPGA devices have undergone qualification and are released to production, periodic reliability tests are run on representative production material to monitor the quality and reliability of the FPGA product line. The reliability monitor tests normally performed are operating life test, biased humidity, temperature cycle, and autoclave. Samples are randomly selected from various device/package types, date codes and die lots in order to gain a representative sample of the outgoing product line. The test results and the failure analyses are compiled on a quarterly basis and published in the FPGA quarterly reliability report. This data can be acquired through any TI field sales office.

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Life Test **Condition:** Dynamic – 125°C, 1000 Hours

Failures/Sample Size: 6/1766

Upper Confidence Level: 60% **Failure Rate Temperature:** 55°C

FAILURE RATE	10.55 FITS	53.26 FITS	184.99 FITS
ACTIVATION ENERGY	0.96 eV	0.7 eV	0.5 eV
ACCELERATION FACTOR	393.78 (125°C)	78.05 (125°C)	22.47 (125°C)
EQUIVALENT DEVICE HOURS	1.055824E–03	5.326886E–03	1.849915E–02
MEAN TIME BETWEEN FAILURES	9.471274E+07 Hours	1.877269E+07 Hours	5405654 Hours
MEAN TIME BETWEEN FAILURES	10811.96 Years	2143.001 Years	617.0838 Years

Stress: Bias Humidity **Condition:** 85°C/85% Relative Humidity, with bias, 1000 Hours

Failures/Sample Size: 1/884 **Failure Rate:** 0.11%/1000 Hours

Stress: Autoclave **Condition:** 15 PSIG, 121°C,240 Hours

Failures/Sample Size: 1/685 **Failure Rate:** 0.14%/240 Hours

Stress: Temperature Cycle **Condition:** –65°C/150°C,1000 Cycles (Per Mil-Std-883C, Method 1010, Condition C)

Failures/Sample Size: 0/1249 **Failure Rate:** 0.00%/1000 Cycles

Stress: Thermal Shock **Condition:** –65°C/150°C,200 Cycles (Per Mil-Std-883C, Method 1010, Condition C)

Failures/Sample Size: 0/559 **Failure Rate:** 0.00%/200 Cycles

Stress: Storage Life **Condition:** 150°C,1000 Hours (Per Mil-Std-883C, Method 1010, Condition C)

Failures/Sample Size: 0/465 **Failure Rate:** 0.00%/1000 Hours

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA LEGEND
3Q92 FINAL REPORT

NOTE: All TPC10XX/TPC12XX FPGA die are fabricated in Lubbock, Texas.

PACKAGE/PIN DESIGNATORS

PKG	PINS	DESCRIPTION
FN	44, 68, 84	PLCC
GB	133, 176, 177	CPGA
QFP	100, 144	PQFP

ASSY/TEST DESIGNATORS		
CODE	**COMPANY**	**LOCATION**
KOREA	ANAM	KOREA
TIPI	TI	PHILLIPINES
TITI	TI	TAIWAN, ROC

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Life Test **Condition:** Dynamic – 125°C, 1000 Hours

Failures/Sample Size: 6/1766

Upper Confidence Level: 60% **Failure Rate Temperature:** 55°C

FAILURE RATE	10.55 FITS	53.26 FITS	184.99 FITS
ACTIVATION ENERGY	0.96 eV	0.7 eV	0.5 eV
ACCELERATION FACTOR	393.78 (125°C)	78.05 (125°C)	22.47 (125°C)
EQUIVALENT DEVICE HOURS	1.055824E–03	5.326886E–03	1.849915E–02
MEAN TIME BETWEEN FAILURES	9.471274E+07 Hours	1.877269E+07 Hours	5405654 Hours
MEAN TIME BETWEEN FAILURES	10811.96 Years	2143.001 Years	617.0838 Years

PART NUMBER	JOB#	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT				DATE CODE
								168 HRS	500 HRS	1k HRS	2k HRS	
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	43	0	0	0	0	9208
TPC1010A	91–12–028	1132132	A	TIPI	FN	68	69	0	0	0	0	9142
TPC1010A	112	6118490	A	TIPI	FN	68	50	0	0	0	–	9213
TPC1010A	112	6118490	A	TIPI	FN	68	50	0	0	0	–	9213
TPC1020A	92–03–003	6100474	A	TIPI	FN	68	129	0	0	1	–	9136
TPC1020A	92–03–003	6088938	A	TIPI	FN	84	50	0	0	0	–	9136
TPC1020A	92–03–004	6168885	B	TIPI	FN	84	127	2	0	0	0	9206
TPC1020A	92–01–001	6142580	B	TIPI	FN	44	129	0	1	0	–	9143
TPC1020A	92–05–007	8194263	A	TIPI	FN	84	129	0	0	0	–	9214
TPC1020A	112	6140487	A	TIPI	FN	68	105	0	0	0	–	9151
TPC1020A	112	6129994	A	TIPI	FN	84	100	0	0	0	–	9203
TPC1020A	100	1070039	A	TIPI	FN	84	100	0	0	0	–	9226
TPC1020A	92–04–005	1199458	B	TIPI	FN	100	129	0	0	0	–	9211
TPC1240	ACTEL	1149935	B	TITL	GB	133	218	0	0	1	–	9135
TPC1280	ACTEL	1149935	B	TITL	GB	177	218	0	0	1	–	9135
TPC1240	92–06–008	1344044	B	KOREA	QFP	144	40	0	0	0	–	9219
TPC1240	92–06–008	1328383	B	KOREA	QFP	144	40	0	0	0	–	9219
TPC1240	92–06–008	1337721	B	KOREA	QFP	144	40	0	0	0	–	9219

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT (CONTINUED)

FAILURE ANALYSIS RESULTS

PART NUMBER	DIE REV	DATE CODE	PINS	FAILS	INTERVAL	FAILURE ANALYSIS RESULTS
TPC1020A	B	9206	84	2	168 HRS	2 IDDH; F/A REP# D13–00144 Mechanical damage.
TPC1020A	B	9143	44	1	500 HRS	1 IDDH; F/A REP# D13–00129 Under review
TPC1020A	A	9136	68	1	1k HRS	1 IDDH; F/A REP# D13–00132 Gate Oxide Defect
TPC1240	B	9135	133	1	1k HRS	1 ICCQ; Under review
TPC1280	B	9135	177	1	1k HRS	1 FUNC; Under review

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Bias Humidity

Condition: 85°C/85% Relative Humidity, with bias, 1000 Hours

Failures/Sample Size: 1/884

Failure Rate: 0.11%/1000 Hours

PART NUMBER	JOB #	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT			DATE CODE
								168 HRS	500 HRS	1k HRS	
TPC1010A	92-03-003	1281371	A	TIPI	FN	68	129	0	0	0	9206
TPC1010A	92-03-003	1281371	A	TIPI	FN	68	43	0	0	0	9208
TPC1010A	92-03-003	6100474	A	TIPI	FN	68	129	0	0	1	9136
TPC1010A	91-12-028	1132132	A	TIPI	FN	68	74	0	0	0	9142
TPC1020A	100	1070039	A	TIPI	FN	84	50	0	0	0	9219
TPC1020A	92-05-007	8194263	A	TIPI	FN	84	77	0	0	0	9214
TPC1020A	92-04-005	1199458	B	KOREA	QFP	100	77	0	0	0	9211
TPC1020A	92-03-004	6168885	B	TIPI	FN	84	76	0	0	0	9206
TPC1020A	92-03-004	6168885	B	TIPI	FN	84	76	0	0	0	9206
TPC1020A	92-01-001	6142580	B	TIPI	FN	44	76	0	0	0	9242
TPC1240	92-06-008	1344044	B	KOREA	QFP	144	77	0	0	0	9219

FAILURE ANALYSIS RESULTS

PART NUMBER	DIE REV	DATE CODE	PINS	FAILS	INTERVAL	FAILURE ANALYSIS RESULTS
TPC1020A	A	9136	68	1	1k HRS	1 IIH

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Autoclave **Condition:** 15 PSIG, 121°C,240 Hours

Failures/Sample Size: 1/685 **Failure Rate:** 0.14%/240 Hours

PART NUMBER	JOB #	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT				DATE CODE
								48 HRS	96 HRS	144 HRS	240 HRS	
TPC1010A	92-01-001	1156316	A	TIPI	FN	44	38	0	0	0	0	9143
TPC1010A	92-01-001	1158390	A	TIPI	FN	44	38	0	0	0	1	9143
TPC1010A	92-03-003	1281371	A	TIPI	FN	68	26	0	0	0	0	9208
TPC1010A	92-03-003	6100474	A	TIPI	FN	68	45	0	0	0	0	9136
TPC1010A	91-12-028	1132132	A	TIPI	FN	68	45	0	0	0	0	9142
TPC1020A	110	1070039	A	TIPI	FN	84	62	0	0	0	0	9226
TPC1020A	92-05-007	8194263	A	TIPI	FN	84	77	0	0	0	0	9214
TPC1020A	112	6129994	A	TIPI	FN	84	66	0	0	0	0	9203
TPC1020A	92-03-003	6100474	A	TIPI	FN	68	45	0	0	0	0	9136
TPC1020A	92-04-005	1199458	B	KOREA	QFP	100	77	0	0	0	0	9211
TPC1020A	92-03-004	6168885	B	TIPI	FN	84	45	0	0	0	0	9206
TPC1020A	92-01-001	6142580	B	KOREA	QFP	44	76	0	0	0	0	9143
TPC1240	92-06-008	1344044	B	KOREA	QFP	144	45	0	0	0	0	9219

FAILURE ANALYSIS RESULTS

PART NUMBER	DIE REV	DATE CODE	PINS	FAILS	INTERVAL	FAILURE ANALYSIS RESULTS
TPC1020A	A	9208	44	1	1k HRS	1 IIH

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Temperature Cycle

Condition: –65°C/150°C,1000 Cycles (Per Mil-Std-883C, Method 1010, Condition C)

Failures/Sample Size: 0/1249

Failure Rate: 0.00%/1000 Cycles

PART NUMBER	JOB #	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT			DATE CODE
								100 CYC	500 CYC	1k CYC	
TPC1010A	92–03–003	6100474	A	TIPI	FN	68	81	0	0	0	9136
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	26	0	0	0	9208
TPC1010A	91–12–028	1132132	A	TIPI	FN	68	69	0	0	0	9142
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	77	0	0	0	9206
TPC1010A	92–01–001	1156316	B	TIPI	FN	44	76	0	0	0	9242
TPC1020A	100	1070039	A	TIPI	FN	84	50	0	0	0	9219
TPC1020A	110	6251051	A	TIPI	FN	84	100	0	0	0	9205
TPC1020A	112	6251051	A	TIPI	FN	68	58	0	0	0	9205
TPC1020A	112	6251051	A	TIPI	FN	84	100	0	0	0	9205
TPC1020A	92–05–007	8194263	A	TIPI	FN	84	76	0	0	0	9214
TPC1020A	92–04–005	1199458	B	KOREA	QFP	100	77	0	0	0	9211
TPC1020A	92–03–004	6168885	B	TIPI	FN	84	76	0	0	0	9206
TPC1020A	92–03–004	6168885	B	TIPI	FN	84	76	0	0	0	9206
TPC1020A	92–01–001	6142580	B	TIPI	FN	44	76	0	0	0	9242
TPC1240	92–06–008	1344044	B	KOREA	QFP	144	77	0	0	0	9219
TPC1240	ACTEL	1143649	B	TITL	GB	133	77	0	–	0	9140
TPC1280	ACTEL	1113608	B	TITL	GB	177	77	0	–	0	9140

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Storage Life

Condition: 150°C,1000 Hours
(Per Mil-Std-883C,
Method 1010, Condition C)

Failures/Sample Size: 0/559

Failure Rate: 0.00%/1000 Hours

PART NUMBER	JOB #	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT			DATE CODE
								100 HRS	500 HRS	1k HRS	
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	15	0	0	0	9208
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	45	0	0	0	9206
TPC1010A	92–03–003	6100474	A	TIPI	FN	68	45	0	0	0	9136
TPC1010A	91–12–028	1132132	A	TIPI	FN	68	76	0	0	0	9142
TPC1020A	92–05–007	8194263	A	TIPI	FN	84	45	0	0	0	9214
TPC1020A	92–04–005	1199458	B	TIPI	FN	84	77	0	0	0	9211
TPC1020A	92–03–004	6168885	B	TIPI	FN	84	76	0	0	0	9206
TPC1020A	92–01–001	6142580	B	TIPI	FN	44	45	0	0	0	9242
TPC1240	92–06–008	1344044	B	KOREA	QFP	144	45	0	0	0	9219
TPC1240	ACTEL	1143649	B	TITL	GB	133	45	0	0	0	9140
TPC1280	ACTEL	1113608	B	TITL	GB	177	45	0	0	0	9140

FIELD PROGRAMMABLE LOGIC
FPGA PRODUCTS

RELIABILITY DATA SUMMARY
3Q92 FINAL REPORT

Stress: Thermal Shock

Condition: –65°C/150°C,200 Cycles
(Per Mil-Std-883C,
Method 1010, Condition C)

Failures/Sample Size: 0/465

Failure Rate: 0.00%/200 Cycles

PART NUMBER	JOB #	LOT#	DIE REV	ASSY SITE	PKG	PINS	QTY	# FAIL @ READPOINT			DATE CODE
								100 CYC	200 CYC	500† CYC	
TPC1010A	92–03–003	281371	A	TIPI	FN	68	45	0	0	0	9206
TPC1010A	92–03–003	6100474	A	TIPI	FN	68	45	0	0	0	9136
TPC1010A	91–12–028	1132132	A	TIPI	FN	68	45	0	0	0	9142
TPC1010A	92–03–003	1281371	A	TIPI	FN	68	15	0	0	0	9208
TPC1020A	92–05–007	8194263	A	TIPI	FN	84	45	0	0	0	9214
TPC1020A	92–04–005	1199458	B	TIPI	FN	84	45	0	0	0	9211
TPC1020A	92–03–004	6168885	B	TIPI	FN	84	45	0	0	0	9206
TPC1020A	92–01–001	6142580	B	KOREA	QFP	44	45	0	0	0	9242
TPC1240	92–06–008	1344044	B	KOREA	QFP	44	45	0	0	0	9219
TPC1240	ACTEL	1143649	B	TITL	GB	133	45	0	0	0	9140
TPC1280	ACTEL	1113608	B	TITL	GB	177	45	0	0	0	9140

† 500 cycles data shown for information only.

6 Applications

Chapter 6

Applications

Discusses the following FPGA applications:

- ❑ Critical Path Analysis for Field-Programmable Gate Arrays
- ❑ Programming Field-Programmable Gate Arrays: Manufacturing Considerations and Options
- ❑ How TI Tests Field-Programmable Gate Arrays
- ❑ IEEE 1149.1 Boundary Scan Library Components

Critical Path Analysis for Field-Programmable Gate Arrays

Product Application

TEXAS INSTRUMENTS

Critical Path Analysis for Field-Programmable Gate Arrays

INTRODUCTION

Device speed, or timing, is a critical aspect of system design. A realistic estimate of the achievable system speed is often required early in the design phase to avoid waste of valuable design time. System speed, of course, depends on the operation of all system components. This section describes how to estimate the timing constraints of a field-programmable gate array (FPGA) design. Remember, the FPGA is just one component within the design. Other devices also affect the system speed.

Methodology

Three things are needed to estimate system speed for a TPC10 Series FPGA design:

1. TPC10 Series Family Data Sheet available from Texas Instruments.
2. TPC10 Series Data Sheet Supplement included in Chapter 2 (PIN LOADING).
3. Knowledge of the design's critical path (The critical path is entirely design dependent).

This application note begins by defining terms associated with estimating system speed (critical path, logic levels, and fan-out). It then provides examples of estimating the propagation delay of a combinational path and the system speed of a sequential path.

When following the outlined procedures, remember that all data sheet delays are typical delays. To determine timing delays for a particular application, always consider the voltage and temperature conditions and derate the typical data sheet values accordingly.

Critical Path

What is a critical path? It is a path in the design which must meet certain critical timing requirements in order for the system to function properly. A critical path can be composed of any combination of hardwired or softwired macros, and input and output buffers for either combinatorial or sequential logic paths. This application note addresses each element of the critical path separately.

Logic Levels

After the critical path has been identified, the next step is to determine the hard or soft macros that will be used to implement the critical path from the TPC10 Series Family Data Sheet and to note the respective logic levels for each of those hard or soft macros. The terms "levels of logic" or "logic levels" refers to the number of logic modules that an input must cross to reach the output.

Hard macros have either one or two logic levels. Two levels of logic means that two logic modules are required to implement this function in the TI FPGA architecture. The filled triangle symbol on the inputs of hard macros denotes two levels of logic. Hard macros without the triangle have only one level of logic. Figure 1 shows an example of one- and two-level hardwired macros. For a two-level hard macro, the logic module interconnection is always consistent and the timing characteristics remain unchanged.

A soft macro is a collection of hard macros configured to make a more complex function. Logic levels for soft macros are listed in the TPC10 Series Family Data Sheet. Soft macros can have many logic levels. (Built using many logic modules).

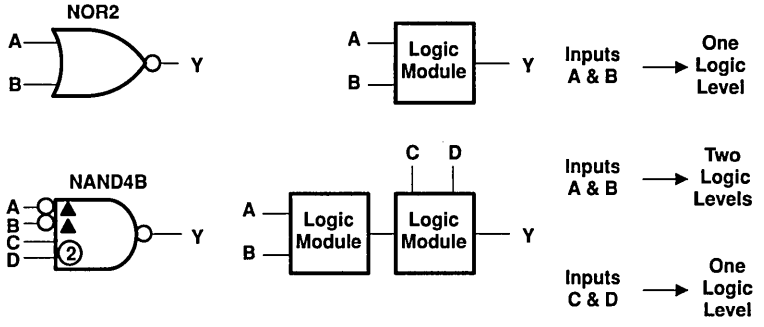


Figure 1.

Fan-out

Fan-out is the sum of the pin loads for all macro inputs connected to the output of a particular macro. The pin loading for every hard and soft macro is listed in the TPC10 series Data Sheet Supplement at the end of this paper (Pin Loading). Figure 2 illustrates the fan-out of an element in a design.

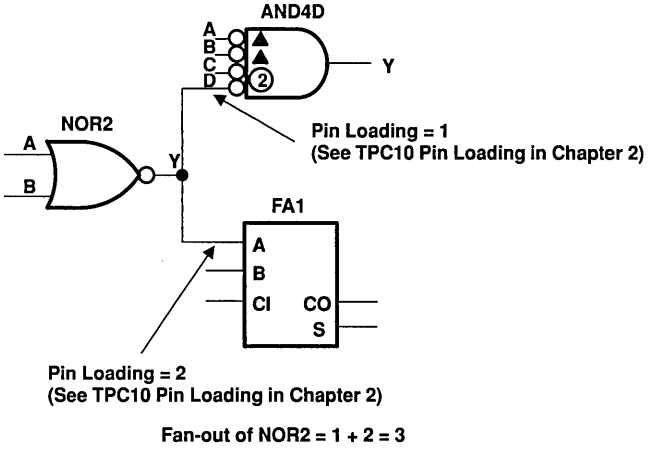


Figure 2.

Example 1. Combinatorial Path

Delay Caused by a Single-Level Hard Macro

With the help of the TPC10 Series Family Data Sheet and the Data Sheet Supplement (Pin Loading), typical delays caused by hard macros can be easily determined. In the example shown in Figure 3, the NOR2 hard macro is used.

Levels of Logic

As a first step, the designer determines the number of logic levels for NOR2, the hard macro. The critical path is through the input A of NOR2. By looking at the NOR2 symbol in the Data Sheet you can see that there is no triangle on input A. This indicates:

Logic levels = 1

NOR2 Fan-out

Next, the fan-out for NOR2 is determined. In this design (Figure 3), the output of NOR2 feeds input A of NAND4A and input A of AND2. The TPC10 Pin Loading in Chapter 2 reveals that input A of the NAND4A macro has a pin loading of 1 and reveals that the A input of AND2 also has a pin loading of 1.

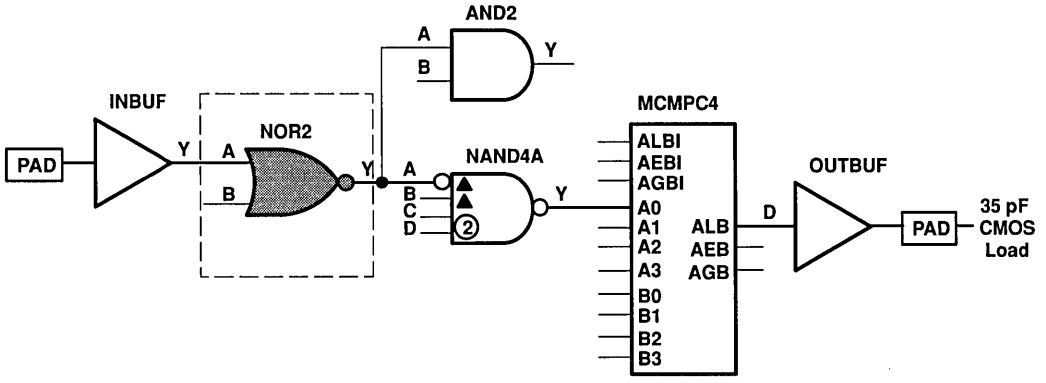


Figure 3.

Simply adding the pin loading of all inputs tied to the output of NOR2, or 1 + 1, provides the fan-out. In this case:

Fan-out=2

The TPC10 Series Family data sheet contains a table with information on the single-level logic module hard-macro switching characteristics. This information is needed to determine the typical delay caused by NOR2. According to that table, a hardwired macro in a critical path with one level of logic and a fan-out of 2 has a delay of 5.8 ns. This value includes a statistical delay estimate for the routing between the NOR2 output and the NAND4A input.

NOTE: Many FPGA vendors do not include delays due to routing in their data sheets.

Delay Caused by a Double-Level hard Macro

LEVELS OF LOGIC

The critical path is through input A of the NAND4A hard macro. By looking in the Data Sheet, you can see that there is a triangle on input A of the NAND4A. This denotes that there are two levels of logic through input A of this hard macro.

Logic levels = 2

NAND4A Fan-out

Next, the fan-out for NAND4A is determined. In this design (Figure 4), the output of NAND4A is connected to input A0 of MCMPC4. The TPC10 Pin Loading in Chapter 2 reveals that input A0 of MCMPC4 has a pin loading of 3. Therefore, the fan-out of the NAND4A is 3.

Fan-out=3

The Data Sheet contains a table with information on double-level logic module hard macro switching characteristics. It shows that a hardwired macro with two levels of logic and a fan-out of 3 has a delay of 10 ns.

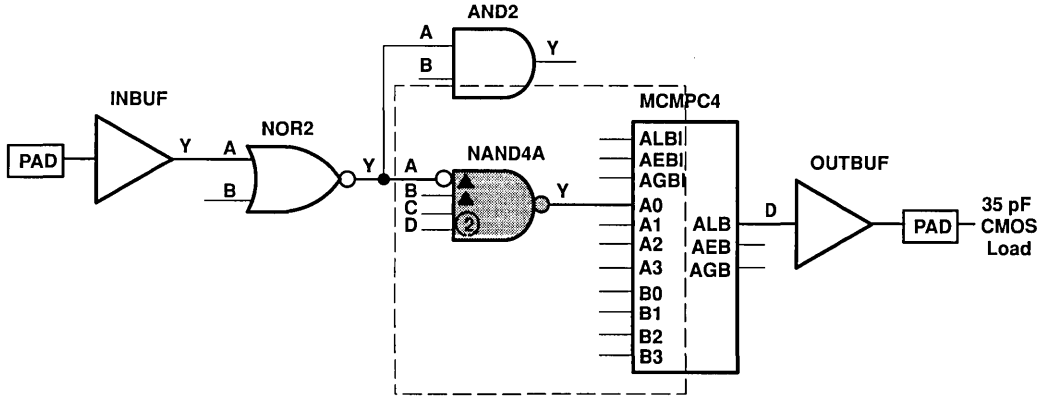


Figure 4.

Delay Caused by a Soft Macro

LEVELS OF LOGIC

The levels of logic for a soft macro are again given in the Data Sheet. The MCMPC4 (Figure 5) soft macro has four logic levels.

Fan-out

It is impossible to determine the load on each of the hard macros within a soft macro without examining the soft macro schematic. Since the soft macro schematics are available only in the CAE environment, the load on the internal hard macros will have to be estimated.

1. Calculate the delay of n–1 levels of logic, where n is the total number of logic levels in the soft macro. A conservative estimate of three loads should be used to calculate the delay of n–1 levels of logic. The delay for the n–1 levels is:

   delay = (n–1) * 6.2

   where 6.2 ns is the delay for a single-level hard macro using critical routing and a fan-out of 3.
2. Determine the load on the output of the macro. The delay on the nth level of logic is simply the delay of a single-level hard macro using critical routing and having the appropriate fan-out.
3. Add the values from steps 1 and 2 to obtain the total delay of the soft macro.

The TPC10 Series Data Sheet shows that the soft macro used in this example (Figure 5) has (n) = 4 logic levels.

1. The calculation for the delay of the first three levels of logic (n–1 levels) is:

   (n–1) * 6.2 = (4–1) * 6.2 = 18.6 ns
2. Determine the fan-out for the fourth logic level in the MCMPC4 soft macro by looking at page 5 of the Data Sheet Supplement (Pin Loading) to find the pin loading on the D input of the OUTBUF macro. The fan-out is 1.

   Determine the delay for the fourth level of logic by looking at page 9 of the TPC10 Series Family Data Sheet. It shows the single-level logic module hard-macro switching characteristics for a critical path with a fan-out of 1. The delay for the fourth logic level is 5.4 ns.
3. Find the total delay by adding the delay of the first three levels, 18.6 ns, to the delay of the fourth level, 5.4 ns. Thus, the total delay in the MCMPC4 soft macro is:

   Total delay = 18.6 ns + 5.4 ns = 24 ns

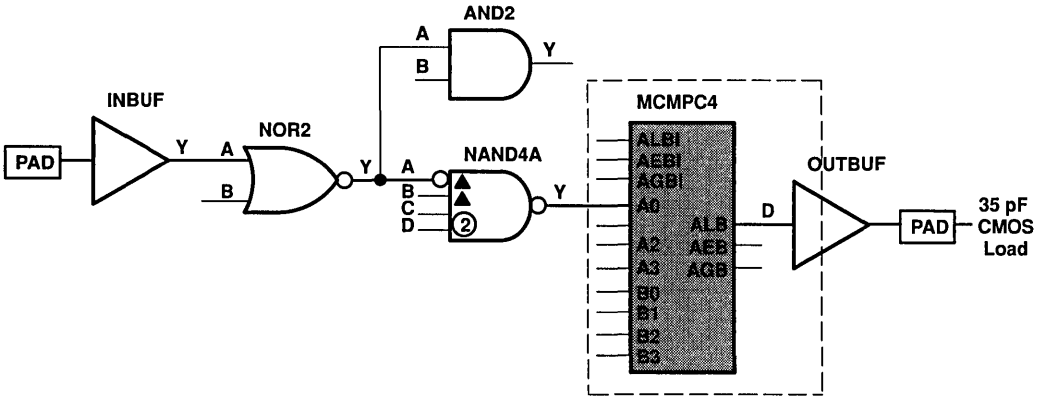


Figure 5.

Delay Caused by an Input Buffer

Input buffer delays (and bidirectional input buffers) are calculated much like hard macro delays (Figure 6). The only difference is that the propagation delay for the high-to-low transition is always used for critical paths. High-to-low transition delays are chosen because they are always greater than low-to-high transition delays as specified in the data sheet.

The Data Sheet lists the delay for an input buffer with a fan-out of 1 as:

Input buffer delay = 6.9 ns

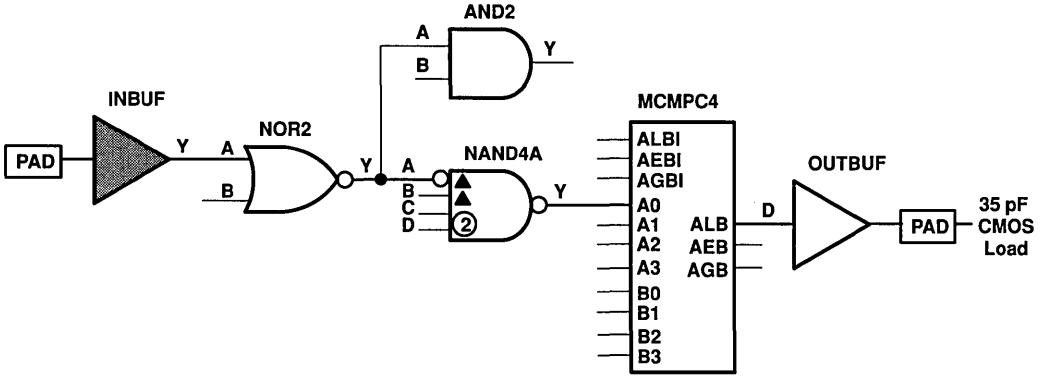


Figure 6.

Delay Caused by an Output Buffer

Output buffer delays (and three-state and bidirectional output buffers) are specified in the TPC10 Series Family Data Sheet for driving CMOS or TTL loads.

The output buffer delays are characterized for a load capacitance of 50 pF. To calculate a propagation delay for an output buffer with a load other than 50 pF, the Δt_{pd} factors from the data sheet must be used.

The delay specified for the critical path evaluation should be the greater of the low-to-high propagation delay, or the high-to-low propagation delay.

The following equation calculates output buffer delay with a load capacitance other than 50 pF.

$$t_{pd}(\text{actual}) = t_{pd}(50\text{pF}) + [\Delta t_{pd} * (C(\text{actual}) - 50)]$$

The delay caused by the output buffer shown in Figure 7 is determined with the help of further information from the TPC10 Series Family Data Sheet.

$t_{PHL} = (3.9) + [.03 * (35 - 50)] = 3.5$ ns

$t_{PLH} = (7.2) + [.07 * (35 - 50)] = 6.2$ ns

Output buffer delay = 6.2 ns

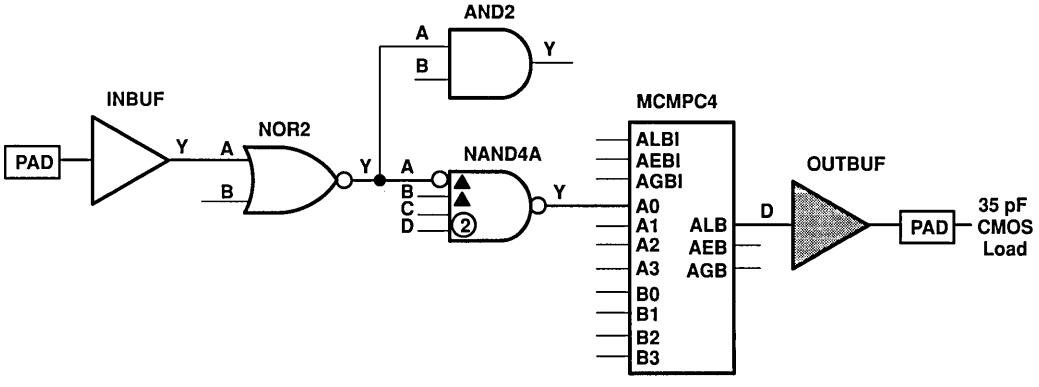


Figure 7.

Combinatorial Critical Path

The components of the critical path have been identified and the delays have been calculated. The next step is to determine the cumulative timing delays of all elements in the critical path (Figure 8).

The critical path delay for a combinatorial path is the sum of all delay elements in the path. Note that the delay caused by the AND2 macro has not been added because AND2 is not in the critical path.

INBUF+NOR2+NAND4A+MCMPC4+OUTBUF = 6.9 + 5.8 + 10 + 24 + 6.2

Total delay = 52.9 ns

The total estimated delay is a typical value. To account for temperature and voltage factors the typical delay is derated with the derating factors shown in the data sheet. For example, to obtain the estimated worst-case delay for a design under commercial operating conditions the typical delay value is multiplied by 1.54.

The following calculation is for the example of a combinatorial path used in this application note:

Worst case delay = 52.9 x 1.54 = 81.5 ns

Example 2. Sequential Critical Path

The technique for analyzing a sequential critical path differs from the technique used for combinational paths. Setup time and hold time characteristics have to be considered and the critical path is broken into segments.

Hold time is the time for which a signal must be held at a specified state after the clock transition. The value is specified as 0 ns for TI FPGAs.

Setup time (t_{su}) is the time for which a signal must be maintained at a constant valid state before the clock transition. Setup times for both flip-flops and latches are given in the Data Sheet.

Propagation delay (t_{pd}) of flip-flops and latches also must be taken into consideration when evaluating the achievable system speed of a sequential path. Propagation delays for flip-flops and latches are also given in the Data Sheet.

Sequential paths must be broken into segments for critical path analysis:

1. Inputs to clocked macros
2. Clocked macros to clocked macros
3. Clocked macros to outputs

The example in Figure 8 is divided into three segments. The first segment is between the input buffer and the first clocked macro. The second segment is from one clocked macro to another. The third segment is from the last clocked macro to the output buffer. The segments are compared and the one with the greatest delay determines the achievable system speed for the device.

With information in the TPC10 Series Family Data Sheet and the Data Sheet Supplement (Pin Loading), delays for the three segments are quite easily determined.

Delay caused by segment 1:

$$t_{seg}\ 1 = t_{pd}(\text{inbuf}) + t_{su}(\text{U1}) = 6.9 + 3.9 = 10.8 \text{ ns}$$

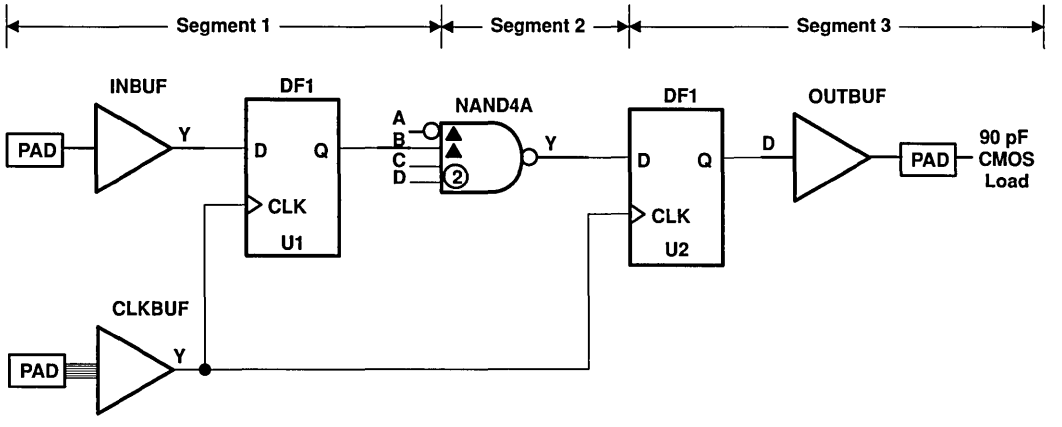


Figure 8.

Delay caused by segment 2:

$$t_{seg}\ 2 = t_{pd}(\text{U1}) + t_{pd}(\text{NAND4A}) + t_{su}(\text{U2}) = 5.4 + 9.2 + 3.9 = 18.5 \text{ ns}$$

Delay caused by segment 3:

$$t_{seg}\ 3 = t_{pd}(\text{U2}) + t_{pd}(\text{outbuf}) = 5.4 + 10 = 15.4 \text{ ns}$$

In the example shown in Figure 8, segment 2 has the greatest path delay with 18.5 ns. Thus, it determines the critical path delay. Again, this is a typical value. To obtain the estimated worst-case delay, multiply by 1.54.

Worst-case delay value = 18.5 x 1.54 = 28.5 ns

System clock frequency is calculated with the following simple equation:

frequency = 1/delay

frequency = 1/28.5 ns

frequency = 35 MHz

In this report, the clock buffer delay has been completely neglected. This is a reasonable assumption for many applications. Generally, the clock buffer delay becomes a consideration only if its delay exceeds the largest segment delay. This is possible in register or latch intensive designs where the clock network is heavily loaded. In such situations, the clock buffer delay could be the limiting factor.

CONCLUSION

This report describes how to estimate the device speed of a Texas Instruments TPC10 series FPGA by calculating the delay caused by the various elements in the design's critical path. Examples of sequential and combinatorial critical paths are used to show how the calculations are performed. The result of the calculations provides an estimate of the speed with which the FPGA is likely to perform. Similar calculations can be made for the TPC12 Series FPGAs.

Alternate Method – 10-ns Rule

A quick method to estimate achievable system speed is to assume 10 ns delay for each hard macro and 10 ns/logic level for each soft macro in the path.

Preferred Method

The most accurate way to estimate achievable system speed for a TI FPGA is to capture the critical path and analyze it using the TI Action Logic System.

Programming Field-Programmable Gate Arrays: Manufacturing Considerations and Options

Product Application

Texas Instruments

Programming Field-Programmable Gate Arrays: Manufacturing Considerations and Options

ABSTRACT

The use of field-programmable gate arrays requires the individual programming of all devices. Programming is accomplished either in-house or by outside sources. A clear understanding of the issues associated with in-house programming and available options is required prior to the decision to establish in-house programming capability. This report describes key manufacturing issues and programming options to aid in the decision making process.

INTRODUCTION

Field Programmable Gate Arrays (FPGAs) provide designers with a flexible tool to reduce design cycle time, package counts, and nonrecurring engineering charges. The desk top design and programming capability allows designers to achieve shorter time to market for new designs. However, the quick turn capability gained by using FPGAs creates unique manufacturing challenges, once designs move from prototype to production.

Since FPGA products must be programmed prior to use, a decision must be made to program in-house or to utilize outside programming sources. This decision can be made only after careful examination of the manufacturing issues involved. Issues that must be considered include:

- Programming time and throughput
- Maintaining lead quality of surface mount components
- Handling moisture-sensitive Plastic Surface Mount Components (PSMCs)
- Manufacturing efficiency

A clear understanding of these manufacturing issues is key in determining the viability of establishing an in-house programming operation.

Texas Instruments is acutely aware of the complexity in establishing an efficient programming process and offers factory programmed FPGAs (P-FPGAs) to help reduce our customer's in-house manufacturing requirements. By allowing TI to program your FPGAs, you are taking advantage of TI worldwide resources, industry leading manufacturing expertise, and quality standards. Devices are delivered fully programmed, symbolized and ready for immediate use. Consider the issues, and then consider TI P-FPGAs for your volume production requirements.

Another programming option is to use facilities/services provided by TI authorized distributors and representatives. Many of them have TI-certified facilities capable of fulfilling your volume production requirements.

TI FPGA programming time is a function of the antifuse technology and fuse density. The antifuse requires multiple programming pulses to successfully form the electrical connection between logic modules. Depending on the device type, 3,000 to 20,000 antifuses are typically programmed. Figure 1 shows typical per unit programming time for TI FPGAs programmed on a TI Activator programmer.

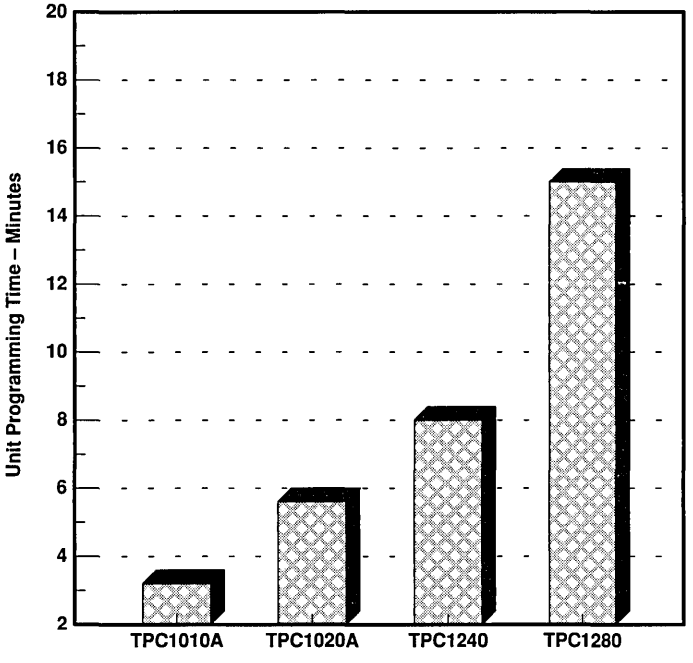


Figure 1. FPGA Per Unit Programming Time

Extended device programming time is not a critical issue for design verification and system prototyping. However, once a design is ready for production, longer cycle times may be incurred if an efficient programming operation is not implemented. Since programming cycle time increases proportionally to the quantity of units programmed, high volume production programming requirements will place a heavy burden on any programming operation. Figure 2 illustrates programming cycle time as a function of the quantity of units programmed. The data shown is based on the use of one TI Activator 2 (gang 4) programmer.

As Figure 2 shows, programming cycle time becomes a significant factor as run rates reach 500 units. For example, the total programming time required to complete 500 units for each device type is:

- TPC1010A = 6.9 hours
- TPC1020A = 11.5 hours
- TPC1240 = 16.7 hours
- TPC1280 = 31.3 hours

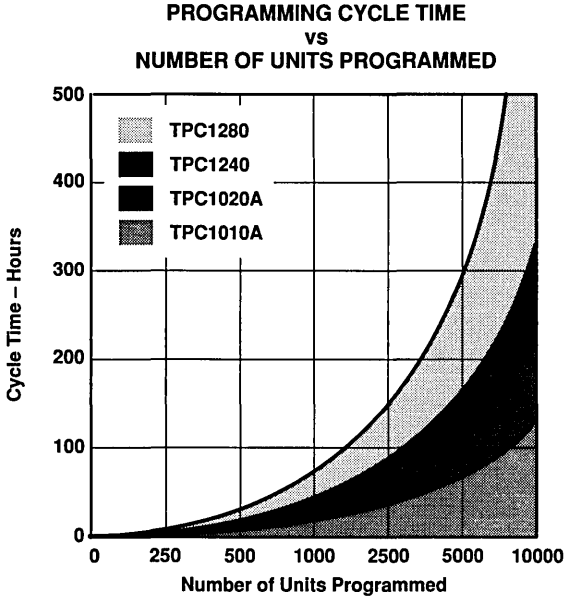


Figure 2. FPGA Programming Cycle Time

Serious consideration must be given to the effect of programming time on production scheduling and capacity. Since programming throughput is directly related to programming time, throughput will degrade as programming time increases. Therefore, a careful analysis of anticipated volume and device mix is needed to determine the amount of capacity required for an in-house programming operation. Based on a 7.3-hour shift and a 22-day month, Figure 3 shows the throughput for a one-shift operation using a single Activator 2 programmer.

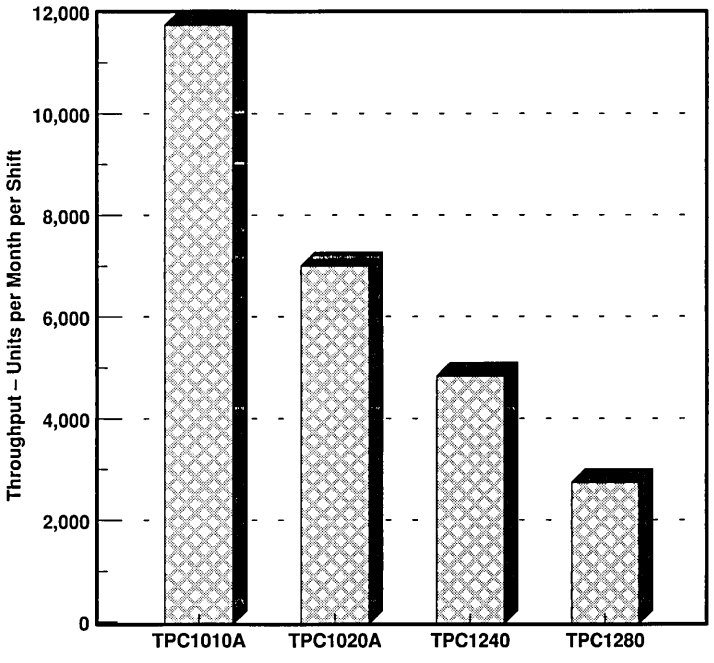


Figure 3. Activator 2 Programmer Throughput

Surface Mount Component Lead Quality

The ability to maintain the lead quality of surface mount components is another key factor to consider before implementation of an in-house programming operation. Handling of surface mount components results in degradation of lead quality. The number of handling-induced defects is dependent on the amount (number of process steps) and type of handling (manual or automated). Based on TI's internal 68- and 84-pin PLCC manufacturing operation, Figure 4 illustrates the effect of device handling on lead quality. By comparison, TI factory-programmed FPGAs undergo extensive lead conditioning and inspection prior to shipment, and therefore result in significantly lower defect levels.

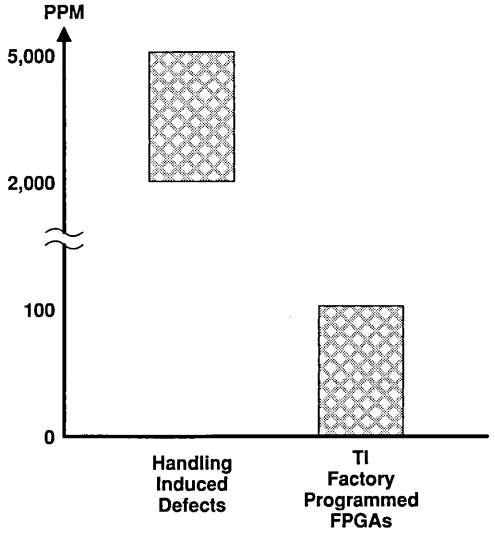


Figure 4. 68-84-Pin PLCC Defect Level Leads

The significance of defect level to the board assembly process is shown in Figure 5. This graph indicates the probability, in percent, that at least one defective, out of spec, device will be found on a single board. The probability is a function of defect level and number of units per board. For example, the probability of one defective unit being found on a board with ten FPGAs is:

- 5% (1 in 20) at 5,000 ppm
- 2% (1 in 50) at 2,000 ppm
- 0.1% (1 in 1000) at 100 ppm

In contrast to the high probability of board assembly problems related to increased lead defects, using TI P-FPGAs virtually eliminates lead defects. As a result, lower cost of ownership and increased manufacturing efficiency is achieved.

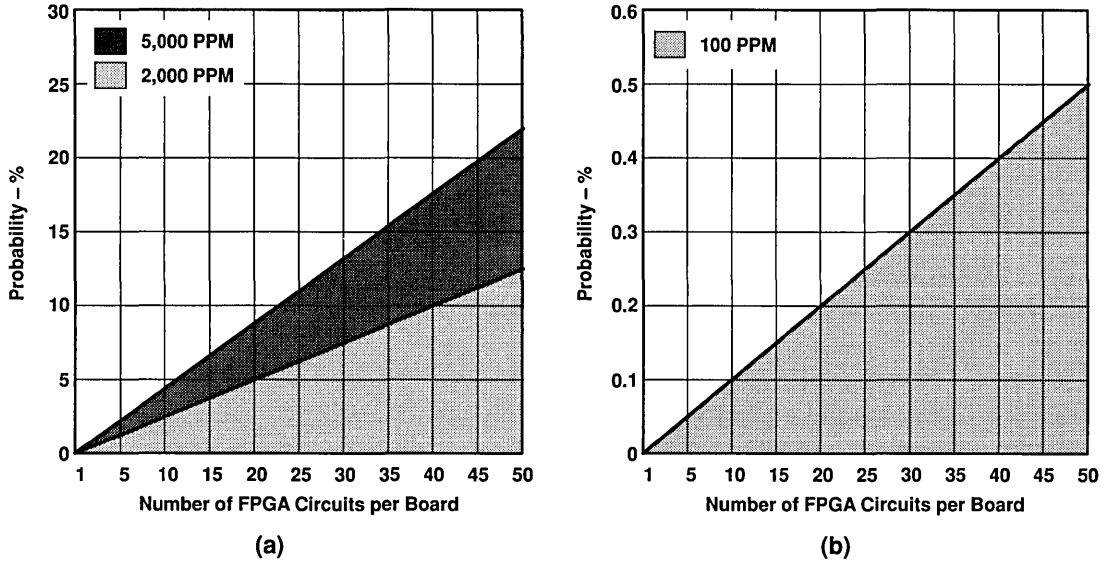


Figure 5. Defect Probability vs PPM Level

Handling Moisture Sensitive Packages

A somewhat obscure, but equally important, manufacturing consideration is the required handling procedure for moisture-sensitive Plastic Surface Mount Components (PSMCs). Moisture is absorbed from the atmosphere by the plastic used to encapsulate integrated circuits. Cracking of the package may occur when moisture trapped inside the plastic vaporizes during the solder reflow process. Therefore, special handling and packing procedures must be followed to prevent PSMC moisture absorption.

All TI plastic surface mountable FPGAs and P-FPGAs are baked to reduce the moisture content of the plastic package to less than or equal to 0.05% and shipped in heat-sealed dry-pack bags. Humidity indicator cards are sealed with the components to serve as a warning in the event of seal failure and exposure to moisture.

Moisture absorption begins immediately upon exposure of PSMCs to the environment. The amount and rate of absorption is a function of temperature and relative humidity. The maximum allowable exposure time at 30 degrees C and 60% relative humidity is 48 hours after the bag is opened.

An in-house programming operation exposes FPGAs to the open air and must consider the exposure time limit. Production programming capacity, scheduling, and cycle time must be appropriately planned to prevent the addition of a rebake process step. In any case, bake and dry-pack equipment is needed in the event maximum exposure time is exceeded or programmed devices are to be inventoried for later use.

Manufacturing Efficiency

A decision to program FPGAs in-house results in an operation that, depending on quality and manufacturing requirements, becomes quickly complicated. In addition to programming, symbolization of programmed devices is needed to prevent different designs from becoming mixed. If pick and place equipment is to be used for PLCC packages, programmed FPGAs may need to be taped and reeled prior to use. Therefore, material must be routed to in-house tape and reel equipment or to an outside subcontractor. Regardless of the method chosen, increased cost and process complexity are the results.

A summary of the in-house programming issues follows:

- Processing requirements and capacity
- Programming equipment
- Symbolization equipment
- Handling procedures to minimize lead degradation
- Handling procedures to minimize rebake
- Handling procedures to minimize EOS and ESD damage
- Outgoing quality
- Staffing requirements
- Nonrecurring, capital, overhead, and labor costs

A decision to purchase TI factory programmed FPGAs requires consideration of the following issues:

- Cost adders
- Volume requirements
- Outgoing quality
- Leadtime

By moving programming, symbolization, and tape and reel back to TI, a substantial reduction in process steps, material handling, and defects is achieved. P-FPGAs are simply received and placed in inventory until needed for production. Figure 6 illustrates the reduction of in-house processing achieved by using TI P-FPGAs. Figure 7 shows the P-FPGA manufacturing flow implemented to provide the highest quality product possible.

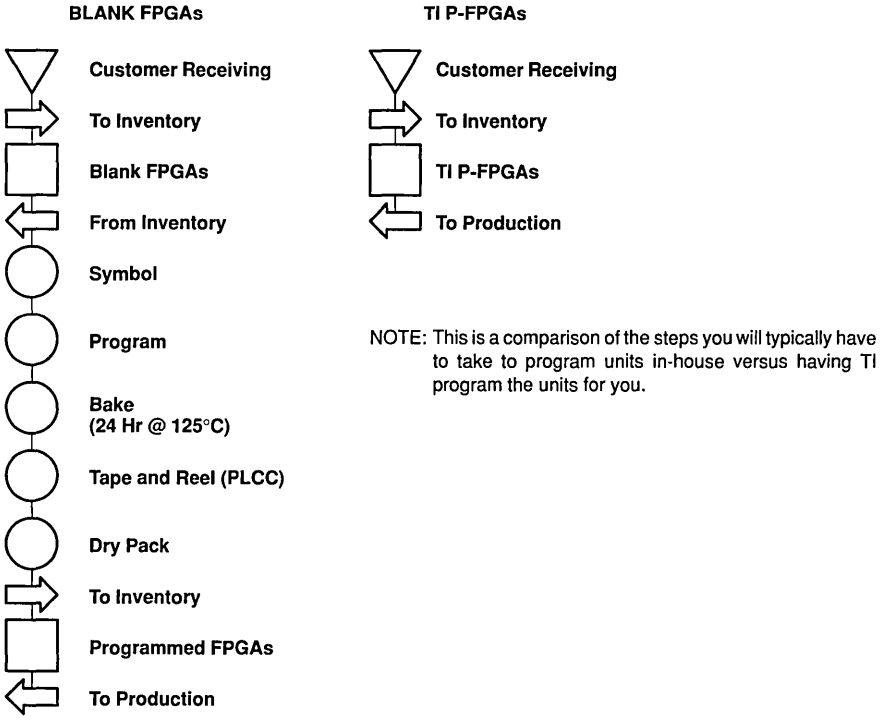


Figure 6. Blank vs TI Programmed FPGA Process Steps

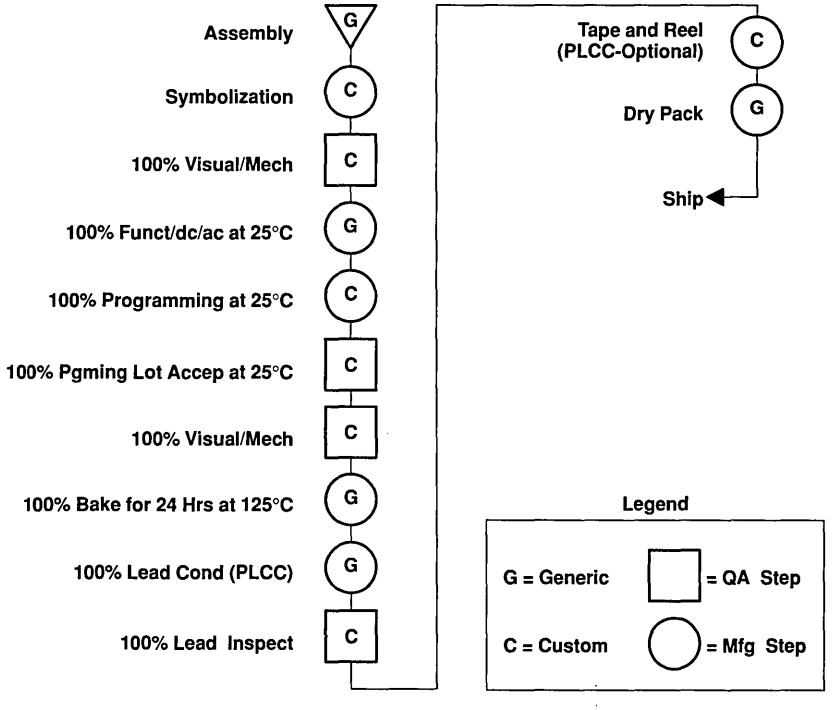


Figure 7. TI P-FPGA Factory Process Flow

How TI Tests Field-Programmable Gate Arrays

Product Application

Texas Instruments

How TI Tests Field-Programmable Gate Arrays

INTRODUCTION

The TPC10 and TPC12 families of field-programmable gate array devices were designed with such a comprehensive and thorough set of testing circuitry that a virtual 100% fault coverage of all the logic prior to programming is achieved. As a result, this makes it unnecessary to functionally test the device after programming. This article will outline and describe the various design-for-testability techniques and how they are used during factory testing.

Serial-Test Circuitry

The internal test observability and controllability of the device is performed via a long serial shift-register chain that surrounds the array. Its length and partitioning is determined by the number of gates and the device type.

There is only one package pin, other than power and ground, that is not programmable by the user. The MODE pin is dedicated for the selection of either test/programming/debug when the pin is at a high-level or V_{CC}, or the normal operation when it is at a low-level or GND. The MODE pin must not be allowed to float and must be tied to ground during normal operation.

The test data is serially shifted into the SDI pin, one bit at a time, by clocking the DCLK pin. The subsequent test results are serially shifted out at either the SDO pin or the MPR pins, by also clocking the DCLK pin. Only the I/O input and output buffer tests are functionally tested at each I/O pin individually.

This shift register is divided into several different groups to give access to the top, bottom, left, right, middle, and center of the array. The first block of registers is the mode control and once loaded, it determines the setup and sequence of events that will occur during that test. The other blocks provide each channel and column track with the ability of being forced or sensed in any combination or direction with V_{PP}, H, L, Z or a precharged condition. The new data, or result, can then be loaded back into the shift registers, shifted out, and read.

Test Flow

The factory testing flow used on the TI FPGA devices in the unprogrammed state is listed below. The major test categories are shown, and each will be described separately.

1. pin-to-pin opens and shorts
2. static power-pin parametric current
3. serial shift register chain functionality
4. channel and column tracks opens/shorts/leakage
5. array transistors functionality/leakage
6. logic modules addressing/functionality/microprobing
7. high-voltage stressing of antifuses and junctions
8. antifuses addressing and shorts tests
9. silicon-signature and bin-circuit programming
10. I/O buffers functionality/parametrics/3-state leakage

Device Pin-to-Pin Opens/Shorts Test

The most basic test performed on any device is the pin-to-pin opens and shorts test. This checks for assembly and handling defects and also ESD/EOS damage near the device's internal bonding pads. The most common problems you may encounter in the programming of FPGAs will probably be caused by mechanical damage to the package pins or leads. The high pin count and finer pitch used on flat-packs and chip-carrier packages will require your close attention during socket insertion on the Activator™.

The other defects found by this test are caused by electrostatic discharge into a device pin due to improper handling or from electrical over stress of the device.

Testing the Power Pins

Each of the power pins are parametrically measured for the amount of static and quiescent current the device uses, to meet the specified maximum value.

Testing the Shift-Register Chain

The functional test of the serial shift register chain is performed first, before any other functional tests can be valid. That is, until the shift register is proven to pass all of its tests, no other addressing or read-back could be relied upon or even possible. Therefore this test must be 100% functional before attempting any further testing.

Column and Channel Tracks Testing

The TI FPGA architecture includes horizontal and vertical metallization that occupies a significant portion of the die area. This is one factor that allows the TPC devices to achieve a 95% module utilization. All of the interconnection and routing tracks must first be 100% tested for connectivity, opens, and every possible short

One of the test techniques used is directly related to the high quality of each device. This is the ability to check for any possible leakage path by precharging the lines. The test charges up each track, and after a predetermined time needed to maintain the level the charge must still be high enough to allow a pass. This discharge rate therefore shows the integrity of the chip and gives a quality indication of many of the key process parameters.

Array Transistors Testing

The horizontal tracks are divided in an optimum way with segmentation transistors. Each of these horizontal pass transistors are in parallel with an antifuse referred to as an 'H' fuse. Also the vertical tracks have many vertical pass transistors in series, along with a 'V' fuse in parallel. The gates of these transistors are turned on and off in accordance with the register sequence and the mode of test. All of these array transistors are therefore fully tested for correct switching.

The track testing and array testing are not entirely independent. This test flow builds upon itself by using previously tested and known working paths and devices to check the next unknown level. The test vectors were designed to isolate and differentiate between many defects such as an open track or open transistor. This also applies to short and leakage problems in a track or a transistor.

Logic Module Testing

We have made sure the entire routing, control, and test 'infrastructure' of the die is functional, and defect/leakage free. Now we are ready to test the full functionality of each logic module in the array.

The proven accessibility of each of the modules eight inputs and one output are now toggled through all of its combinatorial or sequential (if applicable) truth tables and states, again via the serial shift register. The module microprobing and diagnostic capability is also checked at this time. This makes sure that any two module outputs throughout the array can be diagnosed by the user after the device is programmed.

High-Voltage Junction Stress and Antifuse Stress Testing

Stress testing is now done in order to ensure the highest possible antifuse reliability as well as high programming yield. High-level voltages are now used in the 12–21 V range on the V_{PP} pin. Each transistor that will be involved in the device programming is subjected to a junction stress for a predetermined time. This checks for possible low-voltage breakdown conditions.

The antifuse stressing is also performed using about one-half the V_{PP} voltage level required to actually program a fuse. This test detects 'weak' fuses which may have been caused by process defects. This is very important because addressing and selecting a single fuse during programming subjects other fuses on the intersection tracks to a voltage level of $V_{PP}/2$ for a period of time during programming.

Antifuse Shorts Testing

This test is commonly known as the 'blank' test and is identical to the blank-check performed on the Activator.

The previous stress 'tests' do not actually provide data for shifting-out. They simply apply the stressing levels for predetermined times, and the 'check' for any resultant shorting failure during the blank test.

Silicon-Signature and Binning Tests

There are very few differences between the test flow performed on each die during the wafer sort and the final test flow on each package. However, the differences occur on these tests.

In the wafer sort flow, some words of the silicon signature may be programmed with factory-specific codes and information. This provides die traceability to the process fab, lot, and wafer. Also, a code is programmed that establishes the V_{PP} level to be used during programming. At final test or on the ACTIVATOR, this information can be reread when necessary.

The binning circuit consists of several extra testing modules that are configured during sort to produce a simple series of gates between the bin-in pin and the bin-out pin. At final test, ac propagation delay measurements are made to 'bin' each packaged device into various speed-grade categories. Each unit is then symbolized with an add-on dash number representing the overall performance range of each device.

I/O Buffers Testing

The last group of tests performed are the functionality of each input, output, and clock network buffer. The parametric V_{OH}/V_{OL} and 3-state leakage tests are performed also. These are the other tests in which all of the device pins are tested and actually used. All of the previously described functional tests were performed using the 5 pins, MODE, DCLK, SDI, MPRA, and MPRB. The 12XX family also has an SDO pin. The glossary defines the pin names.

CONCLUSION

This purpose of this FPGA testability description is to provide you a basic understanding of the test names, concepts, flow, and methods used during factory testing. For other details like temperature testing, actual parametric specifications, etc., refer to the data sheet.

The fully integrated test, programming, and operational architecture and circuit techniques of the TI FPGA provides the user with the highest possible quality and reliability with the preferred one-time-programmable antifuse technology.

IEEE 1149.1 Boundary Scan Library Components

Product Application

TEXAS INSTRUMENTS

IEEE 1149.1 Boundary Scan Library Components

INTRODUCTION

To facilitate the implementation of the IEEE 1149.1 boundary-scan standard in FPGA devices, a library of test cell components has been developed. This library contains all the test cell components required to construct a boundary-scan test structure. This application note provides a technical overview of the IEEE 1149.1 boundary-scan components offered in TI's FPGA library.

Test Access Port Macro (TAP)

The TAP is the most important component of the IEEE 1149.1 test architecture. A good understanding of the TAP and its operation is essential in the design of IEEE 1149.1 compatible test structures. The library symbol of the TAP component is shown in Figure 1. The TAP symbol has three inputs (TRSTZ, TMS, and TCK), and nine outputs (DRCK, DRSHIFTZ, DRHOLDZ, IRCK, IRSHIFTZ, IRHOLDZ, SELECT, SDOENA, and RESETZ). The TAP's input signals are externally received via input buffers coupled to package pins. The TMS and optional TRSTZ input signals require a pullup resistor so that the TAP receives logic high level inputs in the event the pins are not externally driven. The TAP's output signals are internally routed to control other components within the boundary scan architecture.

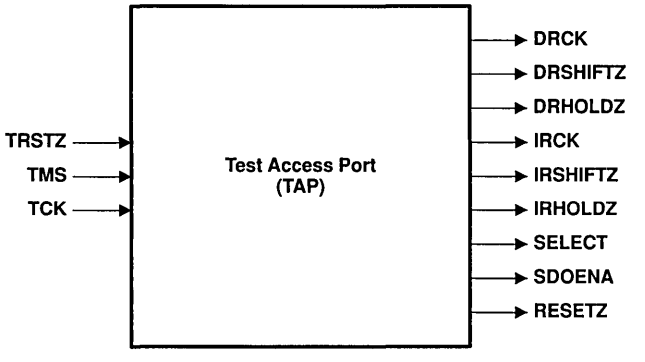


Figure 1. Test Access Port (TAP)

TAP Input and Output Signals

TRSTZ – The Test Reset input is an optional active-low signal used to asynchronously reset the TAP controller.

TMS – The Test Mode Select input is a required signal that controls the operation of the TAP controller.

TCK – The Test Clock input is a required signal that provides the clock input for the TAP controller.

DRCK – The Data Register Clock output becomes active during a data-register scan operation to parallel load then shift data through a selected data register from TDI to TDO.

DRSHIFTZ – The Data Register Shift output is high during the first DRCK of a data-register scan operation to allow the selected data register to capture or preload test data.

DRHOLDZ – The Data Register Hold output is set low during data-register scan operations to cause the output latches of the scan cells in the selected data register to hold their present state.

IRCK – The Instruction Register Clock output becomes active during an instruction-register scan operation to parallel load then shift data through the instruction register from TDI to TDO.

IRSHIFTZ – The Instruction Register Shift output is high during the first IRCK of an instruction-register scan operation to allow the instruction register to capture or preload with status data.

IRHOLDZ – The Instruction Register Hold output is set low during instruction-register scan operations to cause the output latches of the scan cells in the instruction register to hold their present state.

SELECT – The SELECT output controls a multiplexer which inputs serial data to the TDO output pin of the IC during instruction and data scan operations.

SDOENA – The Serial Data Output enable output is an active-low signal that enables the TDO output buffer during instruction and data scan operations.

RESETZ – The RESETZ output is an active-low signal that resets the instruction register when the TAP enters its test logic reset state.

TAP Block Diagram

A block diagram of the TAP component is shown in Figure 2. The TAP is a state machine consisting of three sections; next state logic, state registers, and output control logic. The next state logic provides the Boolean equations for the TAP to operate according to the state diagram of Figure 2. The next state logic receives input from the external TMS signal and the state register outputs (A,B,C,and D). The state register consists of four flip-flops and provides the state storage for the controller. The output control logic consists of state decode logic and flip-flops.

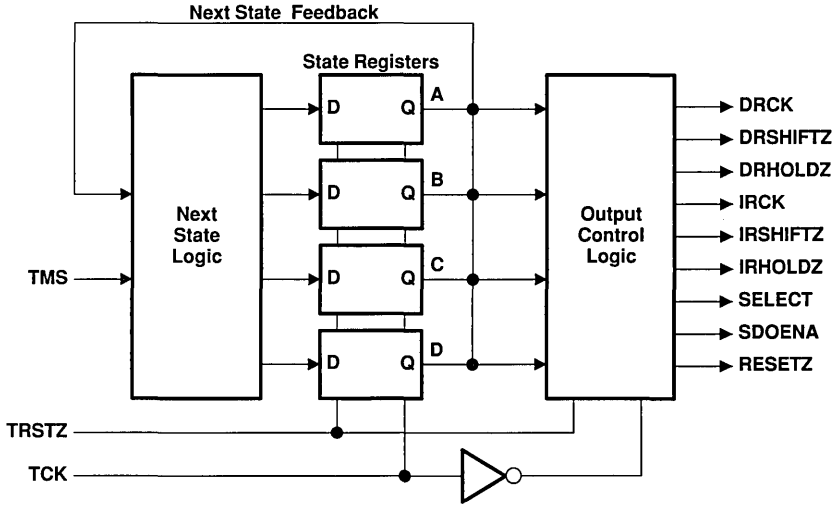


Figure 2. TAP Block Diagram

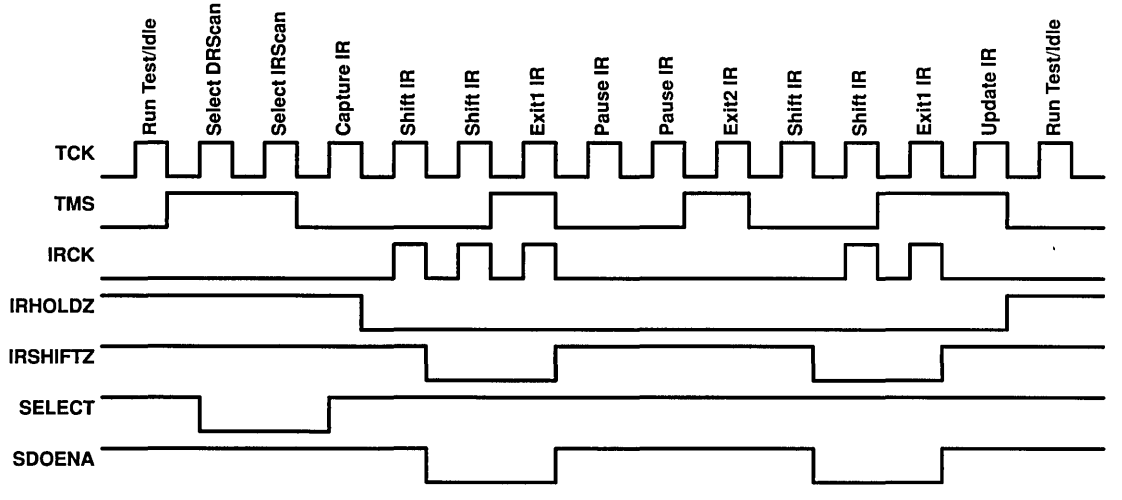
The state register operates on the rising edge of TCK and the flip-flops in the output control logic operate on the falling edge of TCK. The optional TRSTZ input is an active-low asynchronous reset signal that forces the state register and output control flip-flops into an initialized state. Table 1 defines the logic level of each state register flip-flop for each of the states in the TAP's 16-state diagram.

Table 1. TAP State Table

TAP STATES	BINARY	HEX
	"DCBA"	
Exit2 DR state	0000	0
Exit1 DR state	0001	1
Shift DR state	0010	2
Pause DR state	0011	3
Select IR state	0100	4
Update DR state	0101	5
Capture DR state	0110	6
Select DR state	0111	7
Exit2 IR state	1000	8
Exit1 IR state	1001	9
Shift IR state	1010	A
Pause IR state	1011	B
Run test/idle	1100	C
Update IR state	1101	D
Capture IR state	1110	E
Test logic reset state	1111	F

TAP Instruction Register Scan Timing

Figure 3 illustrates the TMS input sequence that causes the TAP to execute an instruction scan operation of a 4-bit instruction register. In response to the TMS input, the TAP exits from the Run Test/Idle state and enters the CAPTUREIR state via the SELECT-DR and SELECT-IR states. Upon entering the SHIFTIR state from the CAPTUREIR state, the instruction register preloads or captures status data, since IRSHIFTZ is high and the first IRCK is present. Also the output latches of the instruction register are latched by the IRHOLDZ signal being set low. On the second and third IRCKs, the instruction register shifts data since IRSHIFTZ is low.



DRCK = Low, DRSHIFTZ = High, and DRHOLDZ = High

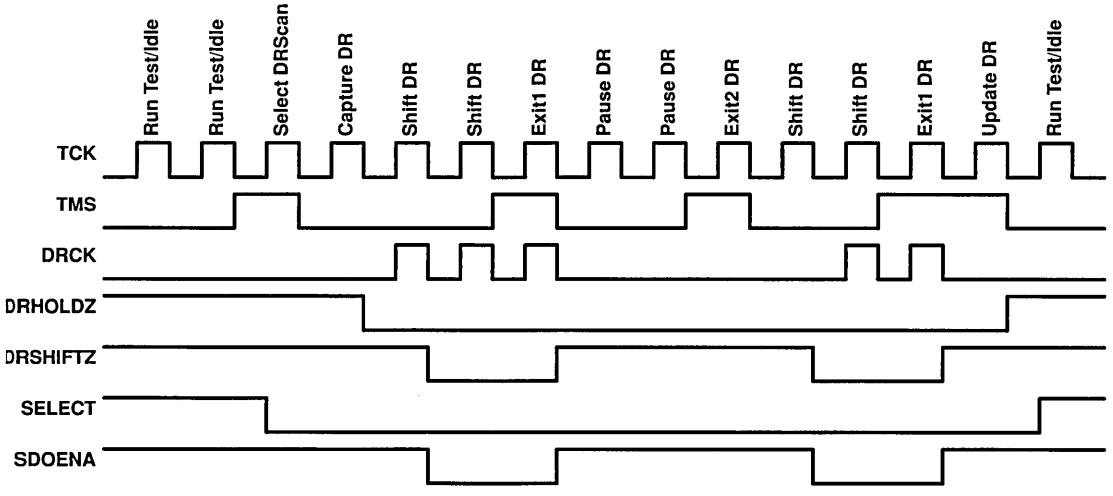
Figure 3. TAP Instruction Register Scan Timing Diagram

To illustrate the pausing capability during instruction-register scan operations, the TMS sequence causes the TAP to transition from the SHIFTIR state into the PAUSEIR state via the EXIT1IR state. In the PAUSEIR state, shifting of data is suspended since the IRCK is gated off. From the PAUSEIR state the TAP transitions back into the SHIFTIR state via the EXIT2IR state. The shifting of data resumes for two IRCKs while the TAP is in the SHIFTIR state. The instruction scan operation is terminated when the TAP transitions to the UPDATEIR state via the EXIT1IR state. In the UPDATEIR state the IRHOLDZ signal is set high to allow the data shifted into the instruction register to be output from the instruction-register output latches. From the UPDATEIR state the TAP transitions to the Run Test/Idle state.

While the TAP is in the SHIFTIR state, the SDOENA signal is low to enable the TDO output buffer. During instruction scan operations, the SELECT signal is high to select the serial output of the instruction register to be output on TDO. When instruction-register scan operations are in progress; DRCK is low, DRSHIFTZ is high and DRHOLDZ is high.

TAP Data Register Scan Timing

Figure 4 illustrates the TMS input sequence that causes the TAP to execute a data-register scan operation. In response to the TMS input, the TAP exits from the Run Test/Idle state and enters the CAPTUREDR state via the SELECT-DR state. Upon entering the SHIFTDR state from the CAPTUREDR state, the selected data register preloads or captures test data, since DRSHIFTZ is high and the first DRCK is present. Also the output latches of the data register are latched by the DRHOLDZ signal being set low. On the second and third DRCKs, the data register shifts data since DRSHIFTZ is low.



IRCK = Low, IRHOLDZ = High, and IRSHIFTZ = High

Figure 4. TAP Data Register Scan Timing Diagram

To illustrate the pausing capability during data-register scan operations, the TMS sequence causes the TAP to transition from the SHIFTDR state to the PAUSEDR state via the EXIT1DR state. In the PAUSEDR state, shifting of data is suspended since the DRCK is gated off. From the PAUSEDR state the TAP transitions back to the SHIFTDR state via the EXIT2DR state. The shifting of data resumes for two DRCKs while the TAP is in the SHIFTDR state. The data-register scan operation is terminated when the TAP transitions to the UPDATEDR state via the EXIT1DR state. In the UPDATEDR state the DRHOLDZ signal is set high to allow the data shifted into the data register to be output from the data-register output latches. From the UPDATEDR state the TAP transitions to the Run Test/Idle state.

While the TAP is in the SHIFTDR state, the SDOENA signal is low to enable the TDO output buffer. During data scan operations, the SELECT signal is low to select the serial output of the selected data register to be output on TDO. When data-register scan operations are in progress; IRCK is low, IRSHIFTZ and IRHOLDZ are high.

TAP Test Logic Reset Timing

Figure 5 illustrates the timing of the RESETZ output from the TAP. At the beginning of the diagram the TMS input is high and the TAP is in the test logic reset state with the RESETZ output set low. Setting the TMS input low causes the TAP to exit the test logic reset state and enter the Run Test/Idle state. The RESETZ output goes high on the falling edge of TCK after the Run Test/Idle state is entered. The TAP can be set back into the test logic reset state by setting the TMS input high. The RESETZ output is set low on the falling edge of the TCK after the test logic reset state has been entered. The state of the other TAP output signals during the test logic reset state is shown in Table 2.

Table 2. TAP Outputs During Test Logic Reset State

IRCK	Low
DRCK	Low
IRHOLDZ	Low
DRHOLDZ	Low
IRSHIFTZ	High
DRSHIFTZ	High
SELECT	High
SDOENA	High

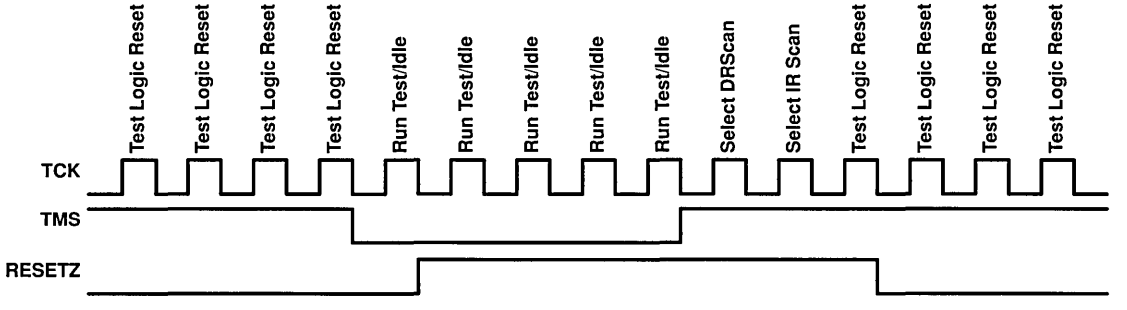


Figure 5. TAP Test Logic Reset Timing Diagram

Unidirectional Boundary Cell 1 (UBCELL1)

The unidirectional boundary cell 1 (UBCELL1) of Figure 6 can be used only with unidirectional input boundary signals since it can only observe, not control, signal data. UBCELL1 supports the required EXTEST and SAMPLE/PRELOAD boundary-test instructions, but does not support the optional INTEST instruction. UBCELL1 only uses two modules, thus this cell can be used to create input boundary register sections with a reduced module count. UBCELL1 has four inputs (DIN, TDI, DRCK, and DRSHIFTZ) and one output (TDO).

Table 3. Unidirectional Boundary Cell 1 Function Table

FUNCTION	INPUTS		OUTPUT
	DRCK	DRSHIFTZ	TDO
Load Data	↑	1	DIN
Shift Data	↑	0	TDI

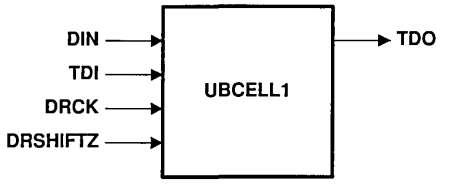


Figure 6. Unidirectional Boundary Cell 1

The function of UBCELL1 is shown in Table 3. When a rising edge occurs on DRCK while DRSHIFTZ is high, the data present on DIN is loaded into the UBCELL1's flip-flop and output on TDO. When a rising edge occurs on DRCK while DRSHIFTZ is low, the data present on TDI is loaded into the UBCELL1's flip-flop and output on TDO.

An example boundary-scan register consisting of a UBCELL1 and UBCELL2 is shown in Figure 7. UBCELL1 and UBCELL2 are serially connected via their TDI and TDO data bus signals and parallel connected to the DRCK, DRSHIFTZ, DRHOLDZ and DMX control bus signals. Since UBCELL1 does not have output test circuitry, it does not require a connection to the DMX and DRHOLDZ control bus signals. UBCELL1 and UBCELL2 form a two-bit boundary-scan register between the circuit's input and output pins and the core logic.

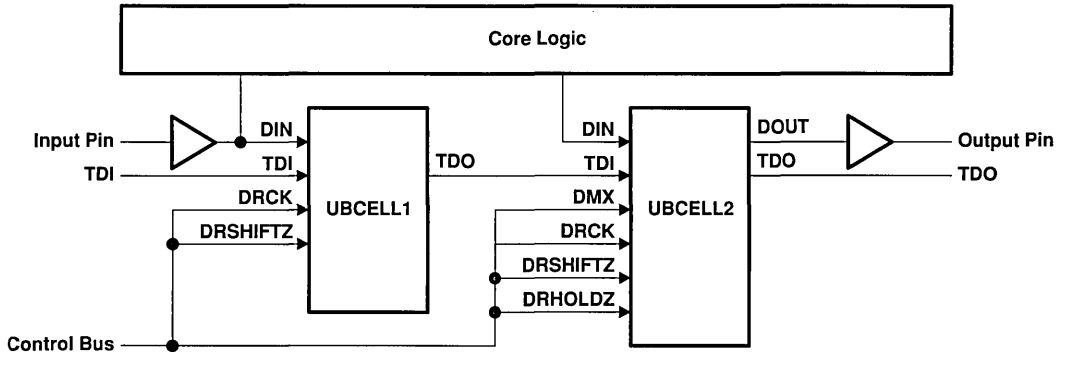


Figure 7. Boundary Register Using UBCELL1

Unidirectional Boundary Cell 2 (UBCELL2)

The unidirectional boundary cell 2 (UBCELL2) of Figure 8 is designed to be used with unidirectional input or output boundary signals. The UBCELL2 cell is also used with signals that are used to control the state of output buffers, i.e., 3-state control signals. In test mode, UBCELL2 can observe and control the boundary signal. UBCELL2 supports the required EXTEST and SAMPLE/PRELOAD boundary test instructions and the optional INTEST instruction. UBCELL1 has six inputs (DIN, TDI, DMX, DRCK, DRSHIFTZ, and DRHOLDZ) and two outputs (TDO and DOUT).

Table 4. Unidirectional Boundary Cell 2 Function Table

FUNCTION	INPUTS				OUTPUTS	
	DRCK	DRSHIFTZ	DRHOLDZ	DMX	DOUT	TDO
Normal mode	0	1	1	0	DIN	FFQ
Load data nm	↑	1	0	0	DIN	DIN
Shift data nm	↑	0	0	0	DIN	TDI
Update data nm	↓	1	0 to 1	0	DIN	FFQ
Test mode	0	1	1	1	FFQ	FFQ
Load data tm	↑	1	0	1	LQ	DIN
Shift data tm	↑	0	0	1	LQ	TDI
Update data tm	↓	1	0 to 1	1	FFQ	FFQ

FFQ = Shift register output, LQ = Latch output, nm = normal mode, tm = Test mode

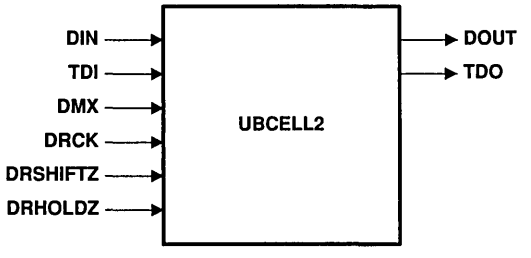


Figure 8. Unidirectional Boundary Cell 2

The function of UBCELL2 is shown in Table 4. While DMX is low the data on DIN transfers to DOUT. When a rising edge occurs on DRCK and while DRSHIFTZ is high and DRHOLDZ and DMX are low, the data present on DIN is loaded into the UBCELL2's flip-flop and output on TDO. When a rising edge occurs on DRCK and while DRSHIFTZ, DRHOLDZ, and DMX are low, the data present on TDI is loaded into the UBCELL2's flip-flop and output on TDO. While DMX is high and DRHOLDZ is low, the data output on DOUT is latched and held during DRCK activations. While DMX is high and when DRHOLDZ transitions from a low to a high, the data output on DOUT becomes the new value stored in the UBCELL2's flip-flop.

An example boundary-scan register consisting of two UBCELL2s is shown in Figure 9. The input UBCELL2 and output UBCELL2 are serially connected via their TDI and TDO data bus signals and parallel connected to the DRCK, DRSHIFTZ, DRHOLDZ, and DMX control bus signals. The input UBCELL2 and output UBCELL2 form a two-bit boundary-scan register between the circuit's input and output pins and core logic.

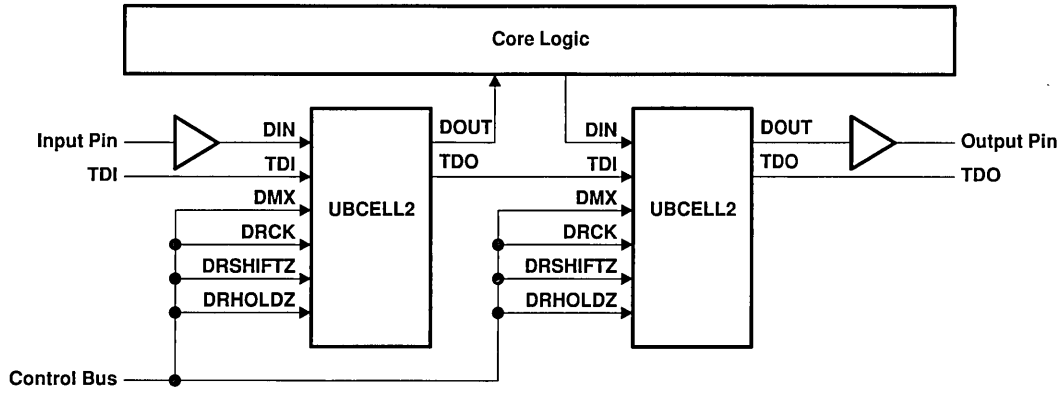


Figure 9. Boundary Register Using UBCELL2

Bidirectional Boundary Cell 1 (BBCELL1)

The bidirectional boundary cell 1 (BBCELL1) of Figure 10 is designed to be used with bidirectional type boundary signals. The BBCELL1 consists of a UBCELL1 and a UBCELL2. The UBCELL1 part of the BBCELL1 is used to observe the input signal of a bidirectional signal pair, and the UBCELL2 part is used to observe and control the output signal of a bidirectional signal pair.

Table 5. Bidirectional Boundary Cell 1 Function Table

FUNCTION	INPUTS				OUTPUTS	
	DRCK	DRSHIFTZ	DRHOLDZ	DMX	DOUT1	TDO
Normal mode	0	1	1	0	DIN1	FFQ2
Load data nm	↑	1	0	0	DIN1	DIN2
Shift data nm	↑	0	0	0	DIN1	FFQ1
Update data nm	↓	1	0 to 1	0	DIN1	FFQ2
Test mode	0	1	1	1	FFQ1	FFQ2
Load data tm	↑	1	0	1	LQ1	DIN2
Shift data tm	↑	0	0	1	LQ1	FFQ1
Update data tm	↓	1	0 to 1	1	FFQ1	FFQ2

FFQ1 = Flip-flop 1 output, FFQ2 = Flip-flop 2 output, LQ1 = Latch 1 output, LQ2 = Latch 2 output, nm = normal mode, tm = Test mode

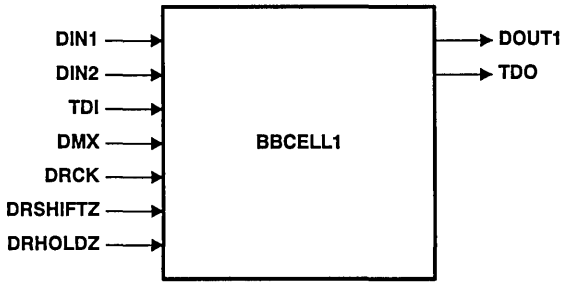


Figure 10. Bidirectional Boundary Cell 1

BBCELL1 supports the required EXTEST and SAMPLE/PRELOAD boundary-test instructions, but does not support the optional INTEST instruction since it cannot control the input signal of a bidirectional signal pair. BBCELL1 has seven inputs (DIN1, DIN2, TDI, DMX, DRCK, DRSHIFTZ, and DRHOLDZ) and two outputs (TDO and DOUT1).

The function of BBCELL1 is shown in Table 5. In the function table, the UBCELL2 part of the BBCELL1 is associated with the DIN1 input and DOUT1 output. The UBCELL1 part is associated DIN2 input. Both UBCELL1 and UBCELL2 receive input from the control inputs. The UBCELL1 and UBCELL2 within the BBCELL1 respond to the control inputs as described in their function tables. During shift operations, UBCELL2 and UBCELL1 form a two-bit shift register.

An example boundary-scan register consisting of a BBCELL1, two UBCELL2s, and a BBCELL2 is shown in Figure 11. BBCELL1, the two UBCELL2s, and BBCELL2 are serially connected via their TDI and TDO data bus signals and parallel connected to the DMX, DRCK, DRSHIFTZ, and DRHOLDZ control bus signals. The boundary-scan cells form a six-bit boundary-scan register between the circuit's two bidirectional pins and the core logic, (BBCELL1 has two bits, each UBCELL2 has a bit, and BBCELL2 has two bits). During normal mode, the output control from the core logic transfers through the UBCELL2 cells, via their DIN inputs and DOUT outputs, to control the state of the output buffers. During test mode, the output control from the UBCELL2's DOUT output is determined by the value shifted in the cell.

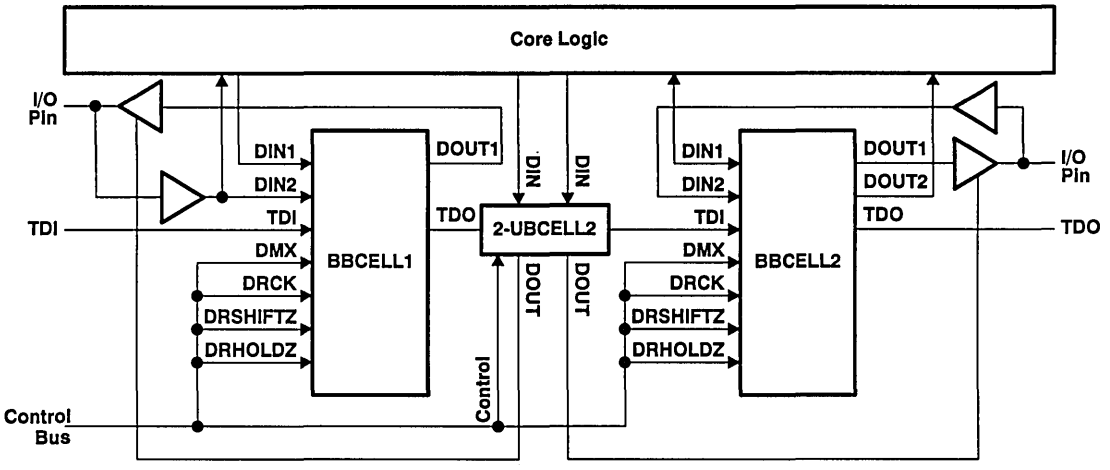


Figure 11. Boundary Register Using BBCELL1

Bidirectional Boundary Cell 2 (BBCELL2)

The bidirectional boundary cell 2 (BBCELL2) of Figure 12 is designed to be used with bidirectional type boundary signals. The BBCELL2 consists of two UBCELL2 cells. One UBCELL2 is used to observe and control the input signal of a bidirectional signal pair, and the other UBCELL2 is used to observe and control the output signal of a bidirectional signal pair. BBCELL2 supports the required EXTEST and SAMPLE/PRELOAD boundary-test instructions and the optional INTEST instruction. BBCELL2 has seven inputs (DIN1, DIN2, TDI, DMX, DRCK, DRSHIFTZ, and DRHOLDZ) and three outputs (TDO, DOUT1, and DOUT2)).

Table 6. Bidirectional Boundary Cell 2 Function Table

FUNCTION	INPUTS				OUTPUTS		
	DRCK	DRSHIFTZ	DRHOLDZ	DMX	DOUT1	DOUT2	TDO
Normal mode	0	1	1	0	DIN1	DIN2	FFQ2
Load data nm	↑	1	0	0	DIN1	DIN2	DIN2
Shift data nm	↑	0	0	0	DIN1	DIN2	FFQ1
Update data nm	↓	1	0 to 1	0	DIN1	DIN2	FFQ2
Test mode	0	1	1	1	FFQ1	FFQ2	FFQ2
Load data tm	↑	1	0	1	LQ1	LQ2	DIN2
Shift data tm	↑	0	0	1	LQ1	LQ2	FFQ1
Update data tm	↓	1	0 to 1	1	FFQ1	FFQ2	FFQ2

FFQ1 = Flip-flop 1 output, FFQ2 = Flip-flop 2 output, LQ1 = Latch 1 output, LQ2 = Latch 2 output, nm = normal mode, tm = Test mode

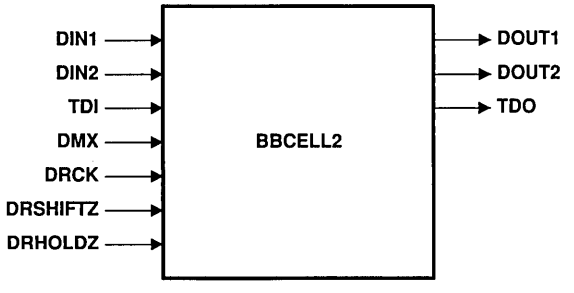


Figure 12. Bidirectional Boundary Cell 2

The function of BBCELL2 is shown in Table 6. In the function table, one of the UBCELL2 cells in the BBCELL2 is associated with the DIN1 input and DOUT1 output, and the other UBCELL2 is associated with the DIN2 input and DOUT2 output. Both UBCELL2 cells receive input from the control inputs. Both UBCELL2 cells within the BBCELL2 respond to the control inputs as described in the UBCELL2 function table.

An example boundary-scan register consisting of two BBCELL2 and two UBCELL2 cells is shown in Figure 13. The BBCELL2 and UBCELL2 cells are serially connected via their TDI and TDO data bus signals and parallel connected to the DMX, DRCK, DRSHIFTZ, and DRHOLDZ control bus signals. The boundary-scan cells form a six-bit boundary-scan register between the circuit's two bidirectional pins and the core logic, (each BBCELL2 has two bits and each UBCELL2 has a bit). During normal mode, the output control from the core logic transfers through the UBCELL2 cells, via their DIN inputs and DOUT outputs, to control the state of the output buffers. During test mode, the output control from the UBCELL2's DOUT output is determined by the value shifted in the cell.

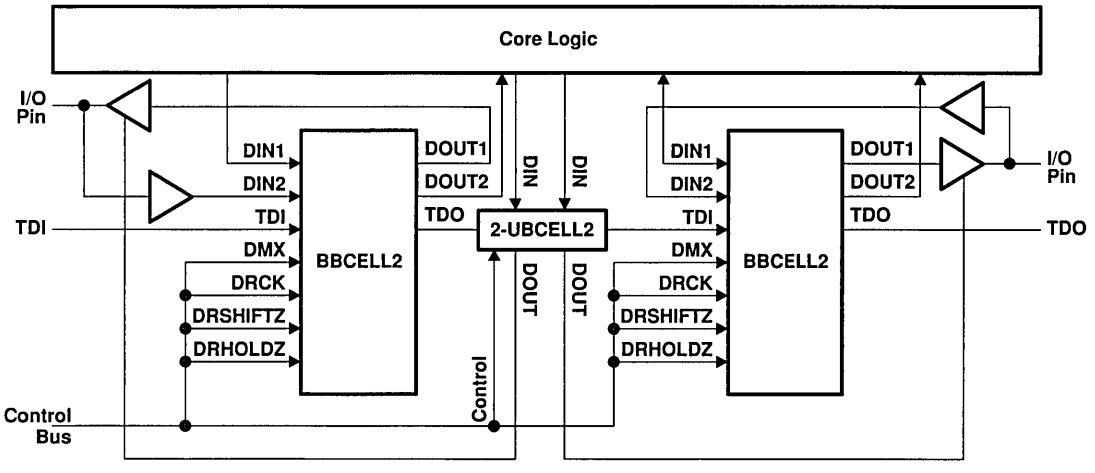


Figure 13. Boundary Register Using BBCELL2

Bypass Register (BYPREG)

The bypass register (BYPREG) of Figure 14 is designed to provide a single-bit shift register path between TDI and TDO when the BYPASS instruction is loaded and the TAP executes a data-register scan operation. The BYPREG has three inputs (TDI, DRCK, and DRSHIFTZ) and one output (TDO).

The function of BYPREG is shown in Table 7. When a rising edge occurs on DRCK while DRSHIFTZ is high, a logic zero is loaded into the BYPREG's flip-flop and output on TDO. When a rising edge occurs on DRCK while DRSHIFTZ is low, the data present on TDI is loaded into the BYPREG's flip-flop and output on TDO.

Table 7. Bypass Register Function Table

FUNCTION	INPUTS		OUTPUT
	DRCK	DRSHIFTZ	TDO
Load Data	↑	1	0
Shift Data	↑	0	TDI

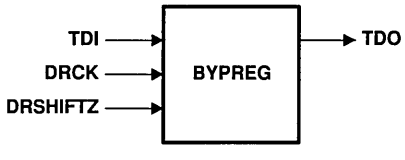


Figure 14. Bypass Register

Instruction Register Cells (IRCELL1 & IRCELL2)

Two instruction register cells, IRCELL1 and IRCELL2, have been designed for simplifying the construction of IEEE 1149.1 instruction registers. The instruction cells are identical in operation with the exception that IRCELL1 is preset when the TAP outputs a RESETZ signal, and IRCELL2 is cleared when the TAP outputs a RESETZ signal. In most instances, the IRCELL1 will be used in instruction register designs. However, if the user implements the optional identification register the IRCELL2 will be used at one or more instruction bit locations to provide a power up IDCODE instruction which is not all ones. By powering up with the IDCODE instruction loaded into the instruction register, immediate access to the circuit's identification register information is available via a data-register scan operation.

Instruction Register Cell 1 (IRCELL1)

The instruction register cell 1 (IRCELL1) of Figure 15 is designed as a bit-slice element to be used in constructing IEEE 1149.1 instruction registers. IRCELL2 has seven inputs (Status, TDI, IRCK, IRSHIFTZ, IRHOLDZ, and RESETZ) and two outputs (IOUT and TDO).

Table 8. Instruction Register Cell 1 Function Table

FUNCTION	INPUTS				OUTPUTS	
	IRCK	IRSHIFTZ	IRHOLDZ	RESETZ	IOUT	TDO
Load data	↑	1	0	1	LQ	Status
Shift data	↑	0	0	1	LQ	TDI
Update data	0	1	0 to 1	1	FFQ	FFQ
Reset	X	X	X	0	1	1

FFQ = Shift register output; LQ = Latch output

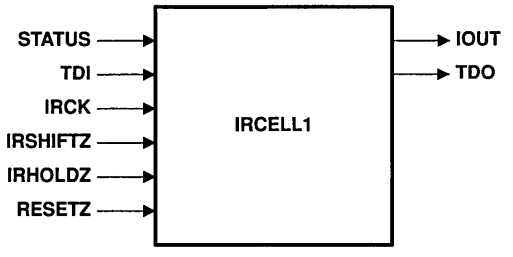


Figure 15. Instruction Register Cell 1

The function of the IRCELL1 is shown in Table 8. In response to a low-level input on RESETZ, the IRCELL1's flip-flop is asynchronously initialized to a high logic state, independent of the other inputs. When a rising edge occurs on IRCK while IRSHIFTZ and RESETZ are high, the data present on the Status input is loaded into the IRCELL1's flip-flop and output on TDO. When a rising edge occurs on IRCK while IRSHIFTZ is low and RESETZ is high, the data present on TDI is loaded into the IRCELL1's flip-flop and output on TDO. While IRHOLDZ is low, the data output on IOUT is latched and held during IRCK activations. When IRHOLDZ transitions from a low to a high, the data output on IOUT becomes the new value stored in the IRCELL1's flip-flop.

Instruction Register Cell 2 (IRCELL2)

The instruction register cell 2 (IRCELL2) of Figure 16 is designed as a bit-slice element to be used in constructing IEEE 1149.1 instruction registers. IRCELL2 has seven inputs (Status, TDI, IRCK, IRSHIFTZ, IRHOLDZ, and RESETZ) and two outputs (IOUT and TDO).

Table 9. Instruction Register Cell 2 Function Table

FUNCTION	INPUTS				OUTPUTS	
	IRCK	IRSHIFTZ	IRHOLDZ	RESETZ	IOUT	TDO
Load data	↑	1	0	1	LQ	Status
Shift data	↑	0	0	1	LQ	TDI
Update data	0	1	0 to 1	1	FFQ	FFQ
Reset	X	X	X	0	0	0

FFQ = Shift register output; LQ = Latch output

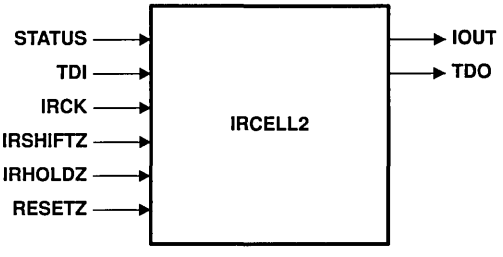


Figure 16. Instruction Register Cell 2

The function of the IRCELL2 is shown in Table 9. In response to a low-level input on RESETZ, the IRCELL2's flip-flop is asynchronously initialized to a low logic state, independent of the other inputs. When a rising edge occurs on IRCK while IRSHIFTZ and RESETZ are high, the data present on the Status input is loaded into the IRCELL2's flip-flop and output on TDO. When a rising edge occurs on IRCK while IRSHIFTZ is low and RESETZ is high, the data present on TDI is loaded into the IRCELL2's flip-flop and output on TDO. While IRHOLDZ is low, the data output on IOUT is latched and held during IRCK activations. When IRHOLDZ transitions from a low to a high, the data output on IOUT becomes the new value stored in the IRCELL2's flip-flop.

Example Instruction Register Using IRCELL1

An example instruction register consisting of two IRCELL1 cells is shown in Figure 17. The first and second IRCELL1 cells are serially connected via their TDI and TDO data-bus signals and parallel connected to the IRCK, IRSHIFTZ, IRHOLDZ and RESETZ control-bus signals. The IEEE 1149.1 standard requires that the status input of the second IRCELL1 (least-significant cell) is connected to a logic high level. By choice, the status input of the first IRCELL1 (most-significant cell) is connected to a low logic level. The two IRCELL1 cells form a two-bit instruction register between the TDI and TDO pins.

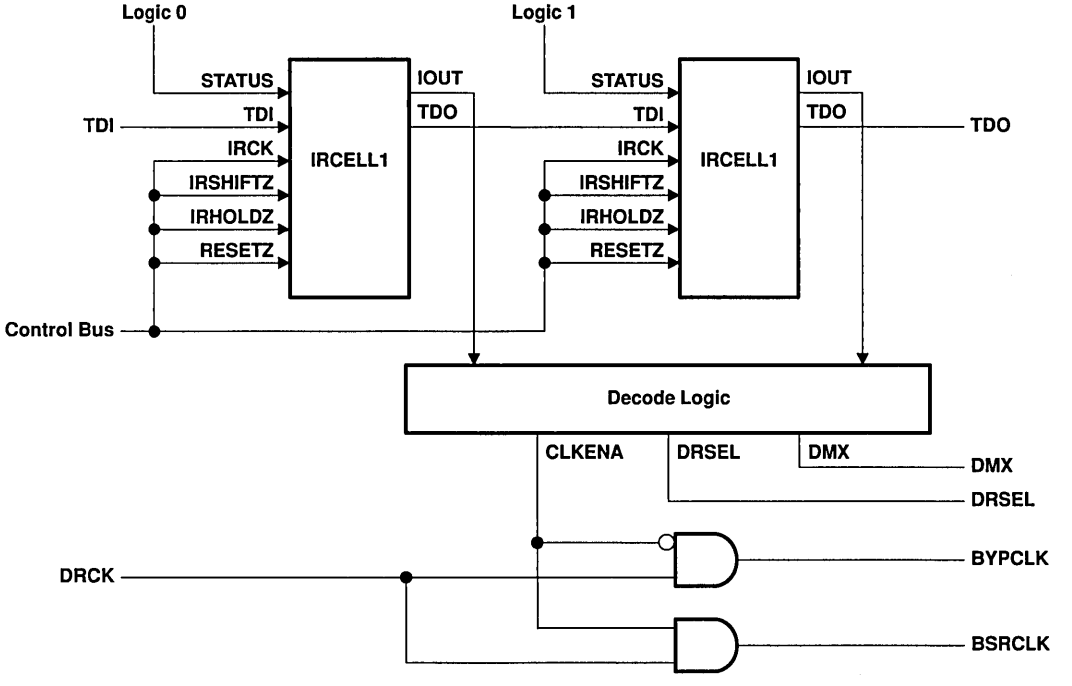


Figure 17. Example Instruction Register

In order to complete the design of the instruction register, the IOUT outputs from each IRCELL1 must be decoded to implement the instruction shifted in. For example purposes, an instruction decode logic section is included in Figure 17. The IOUT outputs from the instruction register are input to a decode logic block. The decode logic block decodes the two-bit instruction input into one of four IEEE 1149.1 instruction types, EXTEST, SAMPLE/PRELOAD, INTEST, and BYPASS. The EXTEST instruction is always decoded as all zeros, and the BYPASS instruction is always decoded as all ones.

In response to the two-bit instruction input, the decode logic outputs control for a serial data multiplexer control (DMX) signal, a data register select (DRSEL) signal, and a data register clock enable (CLKENA) signal. The DMX signal is routed to the boundary register to enable boundary testing using EXTEST or INTEST instructions. The DRSEL signal is routed to a serial data multiplexer that selects the TDO output of the selected data register to be output on TDO, via the TDOCELL. The CLKENA signal enables either the boundary-scan-register clock (BSRCLK) or the bypass-register clock (BYPCLK). Table 10 illustrates which output control signal is enabled for each of the four types of IEEE 1149.1 instructions.

Table 10. Instruction Register Decode Function Table

FUNCTION	INPUTS		OUTPUTS				
	IOUT1	IOUT0	DMX	DRSEL	CLKENA	BYPCLK	BSRCLK
EXTEST	0	0	1	1	1	0	DRCK
Sample/Preload	0	1	0	1	1	0	DRCK
INTEST	1	0	1	1	1	0	DRCK
BYPASS	1	1	0	0	0	DRCK	0

Test Data Output Cell (TDOCELL)

The test-data output cell (TDOCELL) of Figure 18 is designed to simplify the task of routing serial data off the circuit via the TDO output pin. TDOCELL has five inputs (DRTDO, IRTDO, SELECT, DRCK, and IRCK) and one output (TDO). The DRTDO signal comes from the TDO output of the selected data register. The IRTDO signal comes from the TDO output of the instruction register. The SELECT signal comes from the TAP and is used to select either the DRTDO or IRTDO signals to be input to the TDOCELL flip-flop. The DRCK and IRCK signals come from the TAP and are used to clock the selected TDO input into the TDOCELL flip-flop on the falling edge of the clock. The TDO output of the TDOCELL outputs data to the circuits TDO pin.

Table 11. Test Data Output Cell Function Table

FUNCTION	INPUTS			OUTPUT
	DRCK	IRCK	SELECT	TDO
Shift DRTDO	↓	0	0	DRTDO
Shift IRTDO	0	↓	1	IRTDO

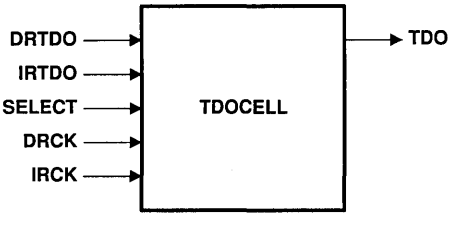


Figure 18. Test Data Output Cell

In the TDOCELL, the DRCK and IRCK signals are input to an OR gate and the output of the OR gate is input to the clock input of the flip flip. When the TAP enables one of the clock signals, during a data or instruction scan operation, the other clock signal is set low enabling the selected clock signal to pass through the OR gate to clock the TDOCELL's flip-flop. Table 11 illustrates the function of the TDOCELL.

Identification Register 1 Macro (IDREG1)

The identification register 1 (IDREG1) of Figure 19 is a 32-bit shift register. IDREG1 has three inputs (TDI, DRCK, and DRSHIFTZ) and one output (TDO). The function of the IDREG1 is shown in Table 12. When a rising edge occurs on DRCK while DRSHIFTZ is high, the identification data is loaded into the 32 IDREG1 flip-flops. When a rising edge occurs on DRCK while DRSHIFTZ is low, data is shifted from TDI, through the 32-bit shift register to TDO.

Table 12. Identification Register 1 Function Table

FUNCTION	INPUTS		OUTPUT
	DRCK	DRSHIFTZ	TDO
Load ID data	↑	1	IDO=1
Shift ID data	↑	0	ID1

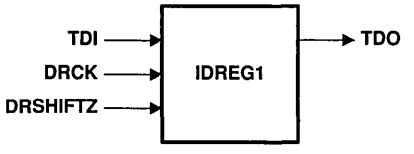


Figure 19. Identification Register 1 Macro

IDREG1 meets the rules in the IEEE 1149.1 standard relating to the optional identification register. IDREG1 can be included in the IEEE 1149.1 architecture to provide information about the IC. The 32-bit shift register of the IDREG1 is broken down into fields. The least-significant bit (the one nearest TDO) must be wired to preload to a logic high level. The next least-significant 11 bits must be wired to preload with the manufacturer's identification code. The next least-significant 16 bits must be wired to preload with the circuit part number. The last 4 bits must be wired to preload with the circuit revision number.

Identification Register 2 Macro (IDREG2)

The identification register 2 (IDREG2) of Figure 20 is a 32-bit shift register. IDREG2 has four inputs (TDI, DRCK, DRSHIFTZ, and U/I) and one output (TDO). The function of the IDREG2 is shown in Table 13. The only difference between IDREG1 and IDREG2 is that IDREG2 has an added User code/Identification code (U/I) input that allows the 32-bit shift register to output either the 32-bit identification code, as described in the IDREG1 section, or a 32-bit user code defined by the customer. In Table 13 it is shown that when the U/I input is low the IDREG2 operates to output the 32-bit identification code. When the U/I input is high the IDREG2 operates to output the 32-bit user code. The U/I signal comes from the instruction register and is set high when a USERCODE instruction is loaded.

Table 13. Identification Register 2 Function Table

FUNCTION	INPUTS			OUTPUT
	DRCK	DRSHIFTZ	U/I	TDO
Load ID data	↑	1	0	ID=1
Shift ID data	↑	0	0	ID1
Load UD data	↑	1	1	UDO=1
Shift UD data	↑	0	1	UD1

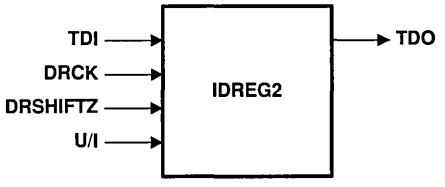


Figure 20. Identification Register 2 Macro

When a rising edge occurs on DRCK while DRSHIFTZ is high and U/I is low, the identification data is loaded into the 32 IDREG2 flip-flops. When a rising edge occurs on DRCK while DRSHIFTZ and U/I are high, the user data is loaded into the 32 IDREG2 flip-flops. When a rising edge occurs on DRCK while DRSHIFTZ is low, data is shifted from TDI, through the 32-bit shift register to TDO.

7 Ordering Information

Chapter 7

Ordering Information

Includes the ordering information for all the TPC Series development systems, hardware options, and device silicon.

7.1 Development Systems Ordering Information

7.1.1 PC Platform

TI-ALS for the PC includes either Viewlogic or Orcad libraries. Viewlogic software may be purchased from TI as detailed below. Orcad and Viewlogic capture tools may be purchased from third party vendors.

TI-ALS software and hardware include a 90-day warranty. In addition, annual factory support packages can be purchased so that the user will have an extended warranty and continuing access to planned periodic updates and enhancements. The annual support period begins at the time of purchase and includes telephone support, bug fixes, workarounds, and periodic updates to the software.

Table 7–1. PC Platform

SYSTEM PART NUMBERS†	DESCRIPTION	SERIES SUPPORTED	DENSITY SUPPORTED (UP TO)
TPC-ALS-DS-PC-VL	TI-ALS, Viewlogic libraries	TPC10, TPC12 & TPC14	2500
TPC-ALS-DS-PC-VL-SP	Annual support contract		
TPC-ALS-DA-PC-VL	TI-ALS, Viewlogic libraries	TPC10, TPC12 & TPC14	10000
TPC-ALS-DA-PC-VL-SP	Annual support contract		
TPC-ALS-DS-PC-OR	TI-ALS, Orcad libraries	TPC10, TPC12 & TPC14	2500
TPC-ALS-DS-PC-OR-SP	Annual support contract		
TPC-ALS-DA-PC-OR	TI-ALS, Orcad libraries	TPC10, TPC12 & TPC14	10000
TPC-ALS-DA-PC-OR-SP	Annual support contract		
TPC-ALS-DS-P2S-PC‡	Single socket programmer	TPC10, TPC12 & TPC14	ALL
TPC-ALS-219‡	Four socket programmer		
TPC-ALS-016	Viewlogic high density simulation	TPC10, TPC12 & TPC14	10000
TPC-ALS-016-SP	Annual support contract		
TPC-ALS-017	Viewlogic low density simulation	TPC10, TPC12 & TPC14	3000
TPC-ALS-017-SP	Annual support contract		
TPC-ALS-VL-005	Viewlogic Schematic capture	TPC10, TPC12 & TPC14	–
TPC-ALS-VL-005-SP	Annual support contract		
TPC-ALS-VL-001	Viewlogic Schematic redraw	TPC10, TPC12 & TPC14	–
TPC-ALS-VL-001-SP	Annual support contract		
TPC-ALS-PLDSYN	Boolean synthesis/FPGA optimization	TPC10 & TPC12	–
TPC-ALS-PLDSYN-SP	Annual support contract		
TPC-ALS-218	Device debug (In-circuit/Activator)	TPC10 & TPC12	8000

† Authorization codes are supplied upon request, after receipt of the TI-ALS system.
‡ Programming units are compatible with all device families: TPC10, TPC12, and TPC14 Series systems. Programming modules are sold separately, see Table 7-4.

7.1.2 HP/APOLLO Platform

TI-ALS includes Mentor libraries. Schematic capture tools are not supplied, but may be purchased from third party vendors.

TI-ALS software and hardware include a 90-day warranty. In addition, annual factory support packages can be purchased so that the user will have an extended warranty and continuing access to planned periodic updates and enhancements. The annual support period begins at the time of purchase and includes telephone support, bug fixes, workarounds, and periodic updates to the software.

Table 7–2. HP/Apollo Platform

SYSTEM PART NUMBERS†	DESCRIPTION	SERIES SUPPORTED	DENSITY SUPPORTED (UP TO)
TPC-ALS-DA-HP7-MG	TI-ALS, HP700, Mentor libraries	TPC10, TPC12 & TPC14	10000
TPC-ALS-DA-HP7-MG-SP	Annual support contract		
TPC-ALS-235§	TI-ALS, DN Series, Mentor libraries	TPC10 & TPC12	8000
TPC-ALS-DS-P2S-HP7‡	Single socket programmer for HP700	TPC10, TPC12 & TPC14	ALL
TPC-ALS-DS-P2-HP7‡	Four socket programmer for HP700		
TPC-ALS-DS-P2S-HP4‡	Single socket programmer for HP400		
TPC-ALS-DS-P2-HP4‡	Four socket programmer for HP400		
TPC-ALS-239‡	Four socket programmer for DN SRS		
TPC-ALS-SYN-HP	TI libraries for Synopsys Design Compiler	TPC10 & TPC12	8000
TPC-ALS-SYN-HP-SP	Annual support contract		
TPC-ALS-SYN-DN	TI libraries for Synopsys Design Compiler		
TPC-ALS-SYN-DN-SP	Annual support contract		
TPC-ALS-218	Device debug (In-circuit/Activator)		

† Authorization codes are supplied upon request, after receipt of the TI-ALS system.
‡ Programming units are compatible with all device families: TPC10, TPC12, and TPC14 Series systems. Programming modules are sold separately, see Table 7-4.
§ The TPC-ALS-235 system provides support for the TPC10 and TPC12 Series, and will not be supported in Revision 3.0, scheduled for release in the fourth quarter of 1993. Annual support is not offered. This system is being replaced by TPC-ALS-DA-HP7-MG.

7.1.3 SUN4 Platform

TI-ALS includes Valid, Viewlogic, Cadence, or Mentor Graphics Libraries. Schematic capture tools are not supplied but may be purchased from third party vendors.

TI-ALS software and hardware include a 90-day warranty. In addition, annual factory support packages can be purchased so that the user will have an extended warranty and continuing access to planned periodic updates and enhancements. The annual support period begins at the time of purchase and includes telephone support, bug fixes, workarounds, and periodic updates to the software.

Table 7–3. SUN4 Platform

SYSTEM PART NUMBERS†	DESCRIPTION	SERIES SUPPORTED	DENSITY SUPPORTED (UP TO)
TPC-ALS-DA-SN-CD	TI-ALS, Cadence libraries	TPC10, TPC12 & TPC14	10000
TPC-ALS-DA-SN-CD-SP	Annual support contract		
TPC-ALS-DA-SN-MG	TI-ALS, Mentor Graphics libraries		
TPC-ALS-DA-SN-MG-SP	Annual support contract		
TPC-ALS-DA-SN-VL	TI-ALS, Viewlogic libraries		
TPC-ALS-DA-SN-VL-SP	Annual support contract		
TPC-ALS-245§	TI-ALS, Valid libraries	TPC10 & TPC12	8000
TPC-ALS-DS-P2S-SN‡	Single socket programmer	TPC10, TPC12 & TPC14	ALL
TPC-ALS-249‡	Four socket programmer		
TPC-ALS-SYN-S4	TI libraries for Synopsys Design Compiler	TPC10 & TPC12	8000
TPC-ALS-SYN-S4-SP	Annual support contract	TPC10 & TPC12	8000
TPC-ALS-218	Device debug (In-circuit/Activator)	TPC10 & TPC12	8000

† Authorization codes are supplied upon request, after receipt of the TI-ALS system.

‡ Programming units are compatible with all device families: TPC10, TPC12, and TPC14 Series systems. Programming modules are sold separately, see Table 7-4.

§ The TPC-ALS-235 system provides support for the TPC10 and TPC12 Series, and will not be supported in Revision 3.0, scheduled for release in the fourth quarter of 1993. Annual support is not offered. This system is being replaced by TPC-ALS-DA-HP7-MG.

Table 7–4. Hardware Options

ADAPTERS FOR ACTIVATOR 1	
HARDWARE	**DESCRIPTION**
TPC-ALS-091	68-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-092	84-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-093	44-Pin, Chip Carrier Diagnostic Probe
TPC-ALS-094	84-Pin, Pin Grid Array Diagnostic Probe
TPC-ALS-096	84-Pin, Ceramic Quad Flat Pack Programming Adaptor
TPC-ALS-097	100-Pin, Plastic Quad Flat Pack Programming Adaptor
TPC-ALS-098	100-Pin, Quad Flat Pack Diagnostic Probe

ADAPTERS FOR ACTIVATOR 2/2S†	
HARDWARE	**DESCRIPTION**
TPC10 SERIES	
TPC-ALS-280	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-281	44-Pin, Chip Carrier Programming Module
TPC-ALS-282	68-Pin, Chip Carrier Programming Module
TPC-ALS-283	84-Pin, Chip Carrier Programming Module
TPC-ALS-284	84-Pin, Pin Grid Array Programming Module
TPC-ALS-285	84-Pin, Quad Flat Pack Programming Module
TPC12 SERIES	
TPC-ALS-286	132/133-Pin, Pin Grid Array Programming Module
TPC-ALS-287	176/177-Pin, Pin Grid Array Programming Module
TPC-ALS-288	84-Pin, Chip Carrier Programming Module
TPC-ALS-289	100-Pin, Pin Grid Array Programming Module
TPC-ALS-290	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-292	144-Pin, Quad Flat Pack Programming Module
TPC-ALS-293	160-Pin, Quad Flat Pack Programming Module
TPC-ALS-294	172-Pin, Quad Flat Pack Programming Module
TPC14 SERIES	
TPC-ALS-PL84	84-Pin, Chip Carrier Programming Module
TPC-ALS-QF100	100-Pin, Quad Flat Pack Programming Module
TPC-ALS-QF160	160-Pin, Quad Flat Pack Programming Module
TPC-ALS-QF208	208-Pin, Quad Flat Pack Programming Module
TPC-ALS-PG100	100-Pin, Pin Grid Array Programming Module
TPC-ALS-PG133	133-Pin, Pin Grid Array Programming Module
TPC-ALS-PG177	177-Pin, Pin Grid Array Programming Module
TPC-ALS-PG207	207-Pin, Pin Grid Array Programming Module
TPC-ALS-PG257	257-Pin, Pin Grid Array Programming Module

† All hardware adaptors are platform independent.

7.2 Product Selection Spectrum

7.2.1 TPC10 Series

Table 7–5. TPC10 Series, 1200 Gates

TPC DEVICE	TECH (µm)	PACKAGE	USER I/O	CONTACT FACTORY
1010AFN-044C	1.2	44PLCC	34	
1010AFN-044C1	1.2	44PLCC	34	
1010AFN-044I	1.2	44PLCC	34	
1010AFN-044I1	1.2	44PLCC	34	
1010AFN-068C	1.2	68PLCC	57	
1010AFN-068C1	1.2	68PLCC	57	
1010AFN-068I	1.2	68PLCC	57	
1010AFN-068I1	1.2	68PLCC	57	
1010AMGB84B	1.2	84CPGA	57	
1010AMHT84B	1.2	84CQFP	57	
1010AVE-100C	1.2	100PQFP	57	
1010AVE-100C1	1.2	100PQFP	57	
1010AVE-100I	1.2	100PQFP	57	
1010AVE-100I1	1.2	100PQFP	57	
1010BFN-044C	1.0	44PLCC	34	✓
1010BFN-044C1	1.0	44PLCC	34	✓
1010BFN-044I	1.0	44PLCC	34	✓
1010BFN-044I1	1.0	44PLCC	34	✓
1010BFN-068C	1.0	68PLCC	57	
1010BFN-068C1	1.0	68PLCC	57	
1010BFN-068I	1.0	68PLCC	57	✓
1010BFN-068I1	1.0	68PLCC	57	✓
1010BVE-100C	1.0	100PQFP	57	✓
1010BVE-100C1	1.0	100PQFP	57	✓
1010BVE-100I	1.0	100PQFP	57	✓
1010BVE-100I1	1.0	100PQFP	57	✓

Table 7–6. TPC10 Series, 2000 Gates

TPC DEVICE	TECH (µm)	PACKAGE	USER I/O	CONTACT FACTORY
1020AFN-044C	1.2	44PLCC	34	
1020AFN-044C1	1.2	44PLCC	34	
1020AFN-044I	1.2	44PLCC	34	
1020AFN-044I1	1.2	44PLCC	34	
1020AFN-068C	1.2	68PLCC	57	
1020AFN-068C1	1.2	68PLCC	57	
1020AFN-068I	1.2	68PLCC	57	
1020AFN-068I1	1.2	68PLCC	57	
1020AFN-084C	1.2	84PLCC	69	
1020AFN-084C1	1.2	84PLCC	69	
1020AFN-084I	1.2	84PLCC	69	
1020AFN-084I1	1.2	84PLCC	69	
1020AMGB84	1.2	84CPGA	69	
1020AMGB84B	1.2	84CPGA	69	
1020AMGB84B-1	1.2	84CPGA	69	
1020AMHT84	1.2	84CQFP	69	
1020AMHT84B	1.2	84CQFP	69	
1020AMHT84B-1	1.2	84CQFP	69	
1020AMHT84S	1.2	84CQFP	69	✓
1020AVE-100C	1.2	100PQFP	69	
1020AVE-100C1	1.2	100PQFP	69	
1020AVE-100I	1.2	100PQFP	69	
1020AVE-100I1	1.2	100PQFP	69	
1020BFN-44C	1.0	44PLCC	34	✓
1020BFN-44C1	1.0	44PLCC	34	✓
1020BFN-44I	1.0	44PLCC	34	✓
1020BFN-44I1	1.0	44PLCC	34	✓
1020BFN-68C	1.0	68PLCC	57	✓
1020BFN-68C1	1.0	68PLCC	57	✓
1020BFN-68I	1.0	68PLCC	57	✓
1020BFN-68I1	1.0	68PLCC	57	✓
1020BFN-84C	1.0	84PLCC	69	✓
1020BFN-84C1	1.0	84PLCC	69	✓
1020BFN-84I	1.0	84PLCC	69	✓
1020BFN-84I1	1.0	84PLCC	69	✓
1020BVE-100C	1.0	100PQFP	69	✓
1020BVE-100C1	1.0	100PQFP	69	✓
1020BVE-100I	1.0	100PQFP	69	✓
1020BVE-100I1	1.0	100PQFP	69	✓

7.2.2 TPC12 Series

Table 7–7. TPC12 Series, 2500 Gates

TPC DEVICE	TECH (µm)	PACKAGE	USER I/O	CONTACT FACTORY
1225AFN-084C	1.0	84PLCC	72	✓
1225AFN-084C1	1.0	84PLCC	72	✓
1225AFN-084I	1.0	84PLCC	72	✓
1225AFN-084I1	1.0	84PLCC	72	✓
1225AVE-100C	1.0	100PQFP	83	✓
1225AVE-100C1	1.0	100PQFP	83	✓
1225AVE-100I	1.0	100PQFP	83	✓
1225AVE-100I1	1.0	100PQFP	83	✓

Table 7–8. TPC12 Series, 4000 Gates

TPC DEVICE	TECH (µm)	PACKAGE	USER I/O	CONTACT FACTORY
1240GB-133C	1.2	133CPGA	92	
1240GB-133I	1.2	133CPGA	92	
1240MGB133B	1.2	133CPGA	104	
1240VE-144C	1.2	144PQFP	104	
1240VE-144I	1.2	144PQFP	104	

Table 7–9. TPC12 Series, 8000 Gates

TPC DEVICE	TECH (µm)	PACKAGE	USER I/O	CONTACT FACTORY
1280GB-176C	1.2	176CPGA	140	
1280GB-176C1	1.2	176CPGA	140	
1280GB-176I	1.2	176CPGA	140	
1280GB-176I1	1.2	176CPGA	140	
1280GB-177C	1.2	177CPGA	140	
1280GB-177C1	1.2	177CPGA	140	
1280GB-177I	1.2	177CPGA	140	
1280GB-177I1	1.2	177CPGA	140	
1280MGB177B	1.2	177CPGA	140	
1280MHFG172B	1.2	172CQFP	140	
1280VB-160C	1.2	160PQFP	125	✓
1280VB-160C1	1.2	160PQFP	125	✓
1280VB-160I	1.2	160PQFP	125	✓
1280VB-160I1	1.2	160PQFP	125	✓

7.2.3 TPC14 Series

Table 7–10. TPC14 Series, 2500 Gates

TPC DEVICE	TECH (μm)	PACKAGE	USER I/O	CONTACT FACTORY
1425FN-84C	0.8	84PLCC	TBD	✓
1425GB-133C	0.8	133CPGA	100	✓
1425GB-133I	0.8	133CPGA	100	✓
1425VE-160C	0.8	160PQFP	100	✓
1460GB-207C	0.8	207CPGA	168	✓
1460GB-207I	0.8	207CPGA	168	✓
1460VE-208C	0.8	208PQFP	167	✓

7.2.4 Legend:

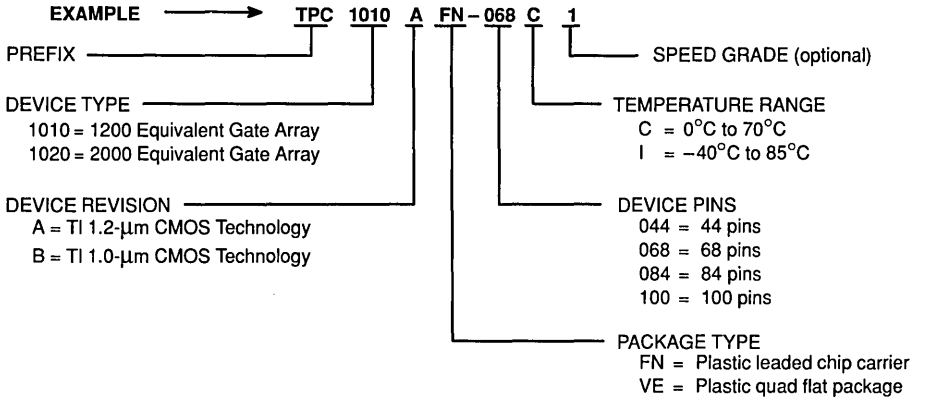
Package Types:
- PQFP – Plastic Quad Flat Pack
- CPGA – Ceramic Pin Grid Array
- PLCC – Plastic Leaded Chip Carrier
- CQFP – Ceramic Quad Flat Pack

Speed Options:
- STD – Standard Speed
- –1 – Standard – 15% Faster

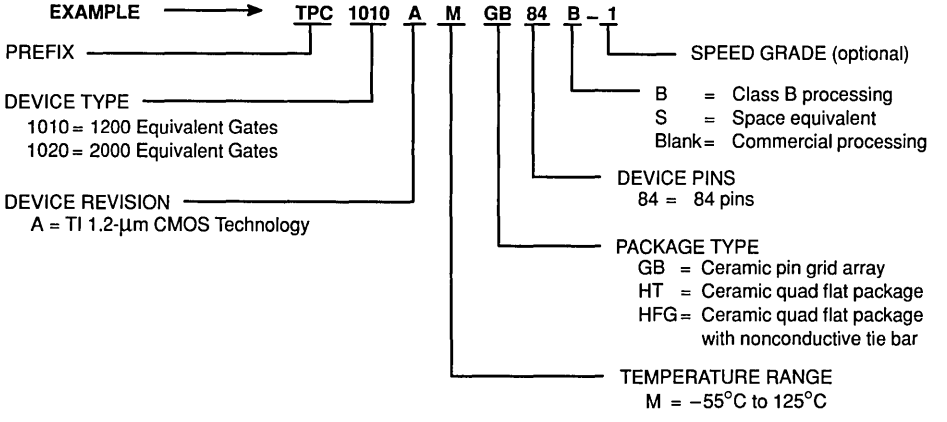
Process:
- C – Commercial (0°C to 70°C)
- I – Industrial (–40°C to 85°C)
- M – Military (–55°C to 125°C)
- B – MIL–STD–883C
- S – Space Equivalent

7.3 TPC10 Series Ordering Information

Configurations of the TPC10 Series devices can be ordered using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



Military versions can be ordered as follows:

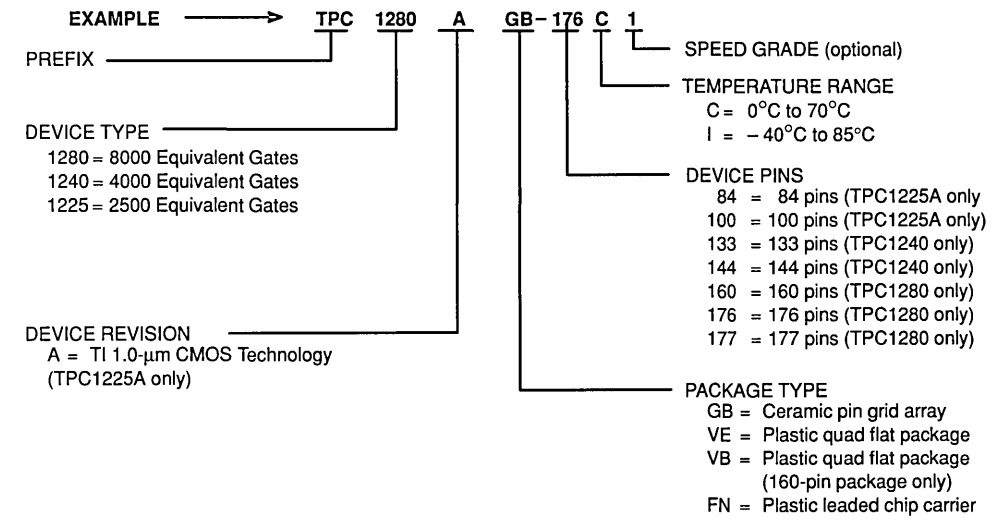


DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

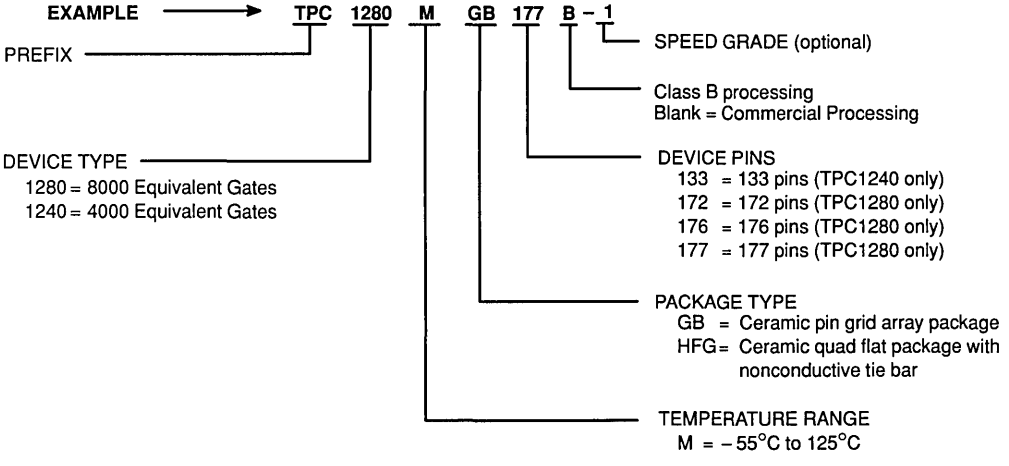
DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1010AM	Class B	5962-9096401M
TPC1020AM	Class B Space Equivalent	5962-9096501M

7.4 TPC12 Series Ordering Information

Various configurations of the TPC12 Series devices can be orderd using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



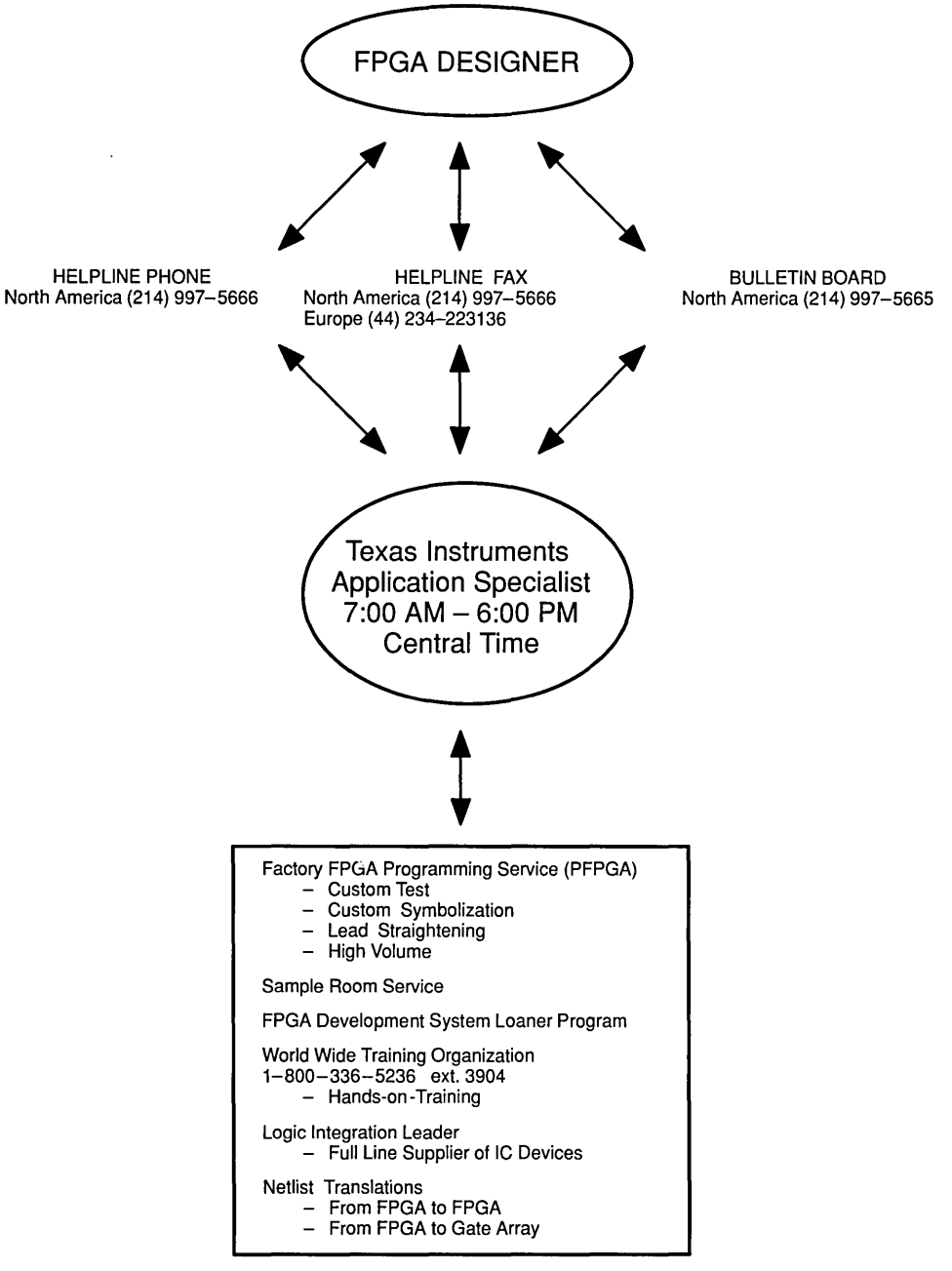
Military versions can be ordered as follows:



DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1240M	Class B	To be determined
TPC1280M	Class B	5962-9215601M

7.5 Texas Instruments Service and Support



7.6 Socket Selection Guide

Socket sources for TI FPGA packages are outlined below. This listing is not a recommendation, but general information of third party suppliers. For information on these sockets, contact the manufacturers directly.

Table 7–11. Production Sockets

	LEAD COUNT	SOURCE	THROUGH-HOLE	SURFACE-MOUNT
PLCC	44	AMP	821551-3	821979-3 or 822035-3
		METHODE	213-44-101	213-044-602
	68	AMP	821574-3	822029-3 or 822073-3
		METHODE	213-068-101	213-068-602
	84	AMP	821573-3	821808-1 (high profile)
		METHODE	213-084-101	213-084-602
PGA(11x11)	85	MILL-MAX	510-91-085-11-041	
		McKENZE	PGA-85H-012B1-1107	
PGA(11X11)	101	McKENZE	PGA-101M-012B-1-11B5	
PGA(13X13)	133	McKENZE	PGA-133H-003B-1-13GO	
PGA(15X15)	176	MILL-MAX	510-91-176-15-061	
		McKENZE	PGA-177M-003B-1-1552	
PQFP	100	YAMAICHI	N/A	IC149-100-05-S5
	144	AMP	822114-3/822115-3	
	160		822114-4/822115-4	

Table 7–12. Zero Insertion Sockets

	LEAD COUNT	SOURCE	THROUGH-HOLE	SURFACE-MOUNT
CQFP	84	WELLS	619-1000311-001	
	132	ENPLAS	OTQ-132-0.635-01	
	172		OTQ-172(196)-0.635-02	
PQFP	100	YAMAICHI	IC51-1004-814-2	
	144		IC51-1014-KS10418	
	160		IC51-1604-845-1	
PGA	85	YAMAICHI	NP35-112-G4-BF85	
	101		NP89-12110-G4-BF101	
	133	NEPENTHE	NEP5-132-RS1311	
	176	YAMAICHI	NP89-22508-G4-BF177	
PLCC	44	YAMAICHI	IC51-0444-400	
	68		IC51-0684-390-1	
	84		IC51-0844-401-1	

Contacts:

AMP	(408) 725-4914
ENPLAS	(415) 572-1683
METHODE	(408) 262-3812
MILL-MAX	(516) 922-6000
McKENZE	(510) 651-2700
NEPENTHE	(415) 856-9332
WELLS	(408) 559-8118
YAMAICHI	(408) 452-0797

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TI Worldwide Sales Offices

ALABAMA: Huntsville: 4960 Corporate Drive, Suite 150, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: Irvine: 1920 Main Street, Suite 900, Irvine, CA 92714, (714) 660-1200; **San Diego:** 5625 Ruffin Road, Suite 100, San Diego, CA 92123, (619) 278-9600; **Santa Clara:** 5353 Betsy Ross Drive, Santa Clara, CA 95054, (408) 980-9000; **Woodland Hills:** 21550 Oxnard Street, Suite 700, Woodland Hills, CA 91367, (818) 704-8100.

COLORADO: Aurora: 1400 S. Potomac Street, Suite 101, Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park So., Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake Boulevard, Suite 1008, Altamonte Springs, FL 32701, (407) 260-2116; **Fort Lauderdale:** 2950 N.W. 62nd Street, Suite 100, Fort Lauderdale, FL 33309, (305) 973-8502; **Tampa:** 4803 George Road, Suite 390, Tampa, FL 33634-6234, (813) 885-7588.

GEORGIA: Norcross: 5515 Spalding Drive, Norcross, GA 30092-2580, (404) 662-7900.

ILLINOIS: Arlington Heights: 515 West Algonquin, Arlington Heights, IL 60005, (708) 640-2925.

INDIANA: Carmel: 550 Congressional Drive, Suite 100, Carmel, IN 46032, (317) 573-6400; **Fort Wayne:** 103 Airport North Office Park, Fort Wayne, IN 46825, (219) 489-4697.

KANSAS: Overland Park: 7300 College Boulevard, Lighton Plaza, Suite 150, Overland Park, KS 66210, (913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Drive, Suite 100, Columbia, MD 21045, (410) 964-2003.

MASSACHUSETTS: Waltham: Bay Colony Corporate Center, 950 Winter Street, Suite 2800, Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Road, Farmington Hills, MI 48018, (313) 553-1581.

MINNESOTA: Eden Prairie: 11000 W. 78th Street, Suite 100, Eden Prairie, MN 55344, (612) 828-9300.

MISSOURI: St. Louis: 12412 Powerscourt Drive, Suite 125, St. Louis, MO 63131, (314) 821-8400.

NEW JERSEY: Iselin: Metropolitan Corporate Plaza, 485 Bldg E. U.S. 1 South, Iselin, NJ 08830, (908) 750-1050.

NEW MEXICO: Albuquerque: 2709 J. Pan American Freeway, N.E., Albuquerque, NM 87107, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Drive, East Syracuse, NY 13057, (315) 463-9291; **Fishkill:** 300 Westage Business Center, Suite 140, Fishkill, NY 12524, (914) 897-2900; **Melville:** 48 South Service Road, Suite 100, Melville, NY 11747, (516) 454-6601; **Pittsford:** 2851 Clover Street, Pittsford, NY 14534, (716) 385-6770.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Suite 100, Charlotte, NC 28217, (704) 527-0930; **Raleigh:** 2809 Highwoods Boulevard, Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Road, Beachwood, OH 44122-5875, (216) 765-7258; **Beavercreek:** 4200 Colonel Glenn Highway, Suite 600, Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 S.W. 105th Street, Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Parkway, Suite 200, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: 615 Mercantile Plaza Building, Suite 505, Hato Rey, PR 00919, (809) 753-8700.

TEXAS: Austin: 12501 Research Boulevard, Austin, TX 78759, (512) 250-6769; **Dallas:** 7839 Churchill Way, Dallas, TX 75251, (214) 917-1264; **Houston:** 9301 Southwest Freeway, Suite 360, Houston, TX 77074, (713) 778-6592; **Midland:** FM 1788 & I-20, Midland, TX 79711-0448, (915) 561-7137.

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