TEXAS INSTRUMENTS

CDC

Clock-Distribution Circuits
A High-Performance Line of 5-V and 3.3-V Products

Data Book

1994

Advanced System Logic

Data Book

CDC Clock-Distribution Circuits 1994

CDC
Clock-Distribution Circuits
Data Book

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INTRODUCTION

Overall system performance is directly related to the quality of the clock distribution network. Virtually all high-performance digital designs subscribe to some form of clock distribution for proper system timing.

The 1994 CDC Clock-Distribution Circuits Data Book provides technical insight into the comprehensive line of clock-distribution circuits (CDC) or *clock drivers* developed by Texas Instruments. CDC products are offered in support of system-clocking layout and design and are targeted for applications in nearly all end equipments. The CDC line of products has been developed in a variety of Texas Instruments silicon processes ranging from Bipolar and CMOS to the latest Advanced BiCMOS technologies. Functionally, the CDC line serves to address a wide spectrum of design requirements with products developed to support 3.3-V and 5-V V_{CC} applications. Texas Instruments is developing new buffer, flip-flop, and phase-locked loop (PLL)-based clock-distribution elements to meet today's higher-performance design requirements. With a large and varied portfolio of products already in production and in development, the designer is able to select the optimal clock driver based on a variety of clocking requirements such as:

- Low skew
- Minimal propagation delay
- TTL, CMOS, differential pseudo ECL (PECL) inputs and outputs
- 3.3-V or 5-V V_{CC} applications
- Selectable true or complementary output configuration
- Output-enable control
- 1/2x, 1x, and 2x frequency multiplication
- Board-space constraints

The products in this book have been designed to meet the stringent requirements of today's advanced system architectures. Due to the increasing requirements to shrink board area, the products in this book are being developed in a variety of surface-mount packaging options such as shrink small-outline packaging (SSOP) and thin shrink small-outline packaging (TSSOP). Texas Instruments also supports the CDC line with an assortment of analytical modeling tools.

The latest high-speed microprocessors, buses, and memories are examples of critical-system components that are spurring a need for higher-performance clock distribution. Texas Instruments is working to provide optimal clock-driver solutions to meet these needs.

Complete technical data for any TI Advanced System Logic product is available from the nearest TI field sales office, local authorized TI distributor, or directly by calling the Advanced System Logic hotline at (214) 997-5202.

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Contents

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**

The internal capacitance at an input of the device

C_o **Output capacitance**

The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V.

$I_{I(hold)}$ **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} **High-level input current**

The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{jitter} **Jitter**

Dispersion of a time parameter of the pulse waveforms in a pulse train with respect to a reference time, interval, or duration. Unless otherwise specified by a mathematical adjective, peak-to-peak jitter is assumed.

$t_{jitter(RMS)}$ **RMS Jitter**

The root mean square jitter, one sixth of the maximum peak-to-peak jitter

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level.

$t_{sk(I)}$ **Input skew**

The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(I)}$ describes the ability of the gate to shape the pulse to the same duration regardless of the input used as the controlling input.

$t_{sk(l)}$ **Limit skew**

The difference between 1) the greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device but rather is calculated from the data sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time will be induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(i)}$ also accounts for process variation. In fact, all other skew specifications [$t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$] are subsets of $t_{sk(i)}$; they will never be greater than $t_{sk(i)}$.

$t_{sk(o)}$ **Output Skew**

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

$t_{sk(p)}$ **Pulse Skew**

The difference between propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. $t_{sk(p)}$ quantifies the duty cycle characteristic of a clock driver. Certain applications require a fixed duty cycle for proper operation. As an example, the CLK2 input of an MC68020 processor operating at 40 MHz requires a duty cycle of 50 ± 5%. $t_{sk(p)}$ is a measure of a clock driver's ability to supply such a precisely controlled pulse.

$t_{sk(pr)}$ **Process Skew**

The difference between identically specified propagation delay times on any two like ICs operating under identical conditions. $t_{sk(pr)}$ quantifies the skew induced by variations in the IC manufacturing process but not by variations in supply voltage, operating temperature, output loading, input edge rate, input frequency, etc. Process skew is commonly specified and production tested under fixed conditions (e.g., V_{CC} = 5.25 V, T_A = 70°C, C_L = 50 pF, all inputs switching simultaneously).

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the ABT family. In general, the junction temperature for any device can be calculated using using the following equation.

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

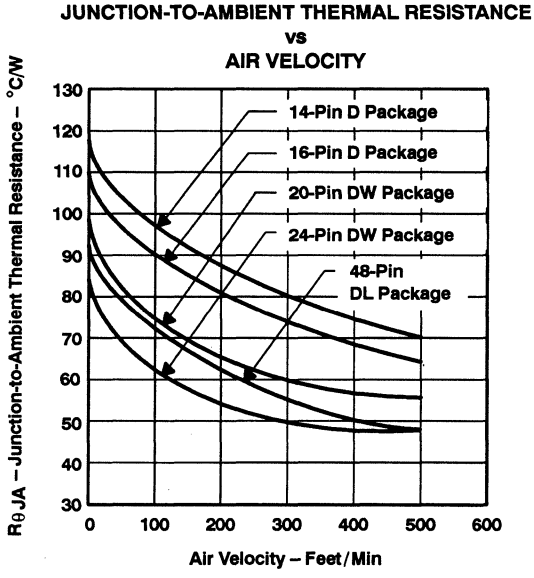


Figure 1

Figures 2 through 5 show power dissipation derating for the 8-, 16,- 20-, and 24-pin DB packages.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

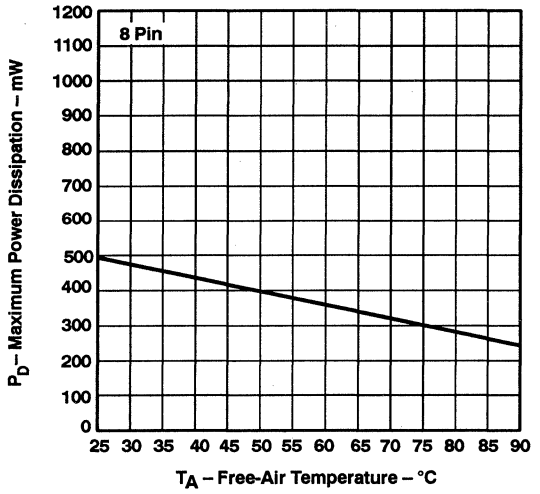


Figure 2

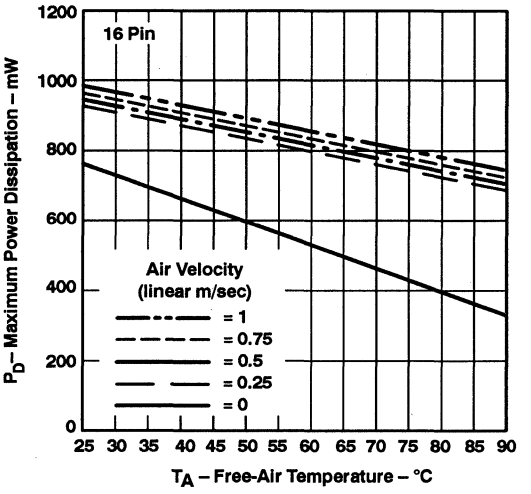


Figure 3

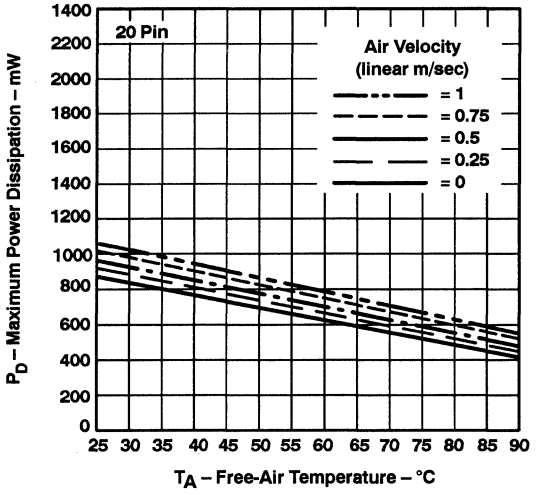


Figure 4

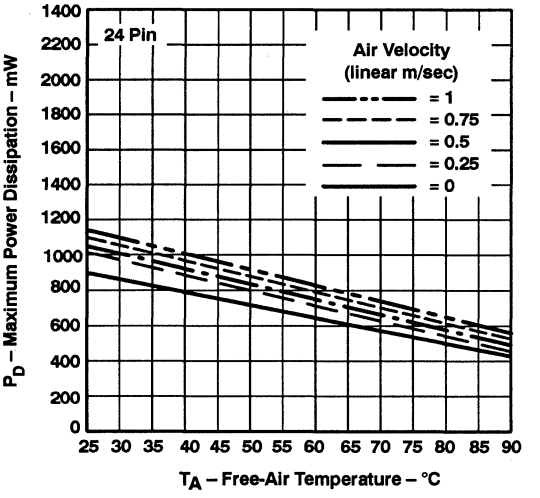


Figure 5

CLOCK-DISTRIBUTION CIRCUITS

5-V Clock-Distribution Circuits (CDC)

DESCRIPTION	I/O LEVELS	TYPE	TECHNOLOGY			
			AS	AC	ACT	ABT
Hex Inverter	CMOS/CMOS	'204		✔		
1-to-6 Exclusive OR	TTL/TTL	'328				✔
	TTL/TTL	'328A				+
	TTL/CMOS	'329A				✔
1-to-6 Exclusive OR With OE	TTL/TTL	'391				✔
	TTL/CMOS	'392				✔
Dual 1-to-4 Buffer (2 inputs, 8 outputs)	TTL/CMOS	'208			✔	
	CMOS/CMOS	'209		✔		
1-to-8 Divide-by-2 Flip-Flop (6 inverting, 2 noninverting)	TTL/TTL	'303	✔			
1-to-8 Divide-by-2 Flip-Flop (8 noninverting)	TTL/TTL	'304	✔			
1-to-8 Divide-by-2 Flip-Flop (4 inverting, 4 noninverting)	TTL/TTL	'305	✔			
1-to-8 Fanout (4 noninverting buffer, 4 divide-by-2 flip-flop)	TTL/CMOS	'337				✔
	TTL/TTL	'339				✔
1-to-8 NAND	TTL/TTL	'340				✔
1-to-8 AND	TTL/TTL	'341				✔
3-Way Fanout Buffer (dual 1-to-3 noninverting buffer, 1-to-4 divide-by-2 flip-flop)	TTL/TTL	'330				✔

3.3-V Clock-Distribution Circuits (CDC)

DESCRIPTION	I/O LEVELS	TYPE	TECHNOLOGY			
			AS	AC	ACT	ABT
Hex Inverter	CMOS/CMOS	'203		✔		
1-to-9 Differential LVPECL Buffer	LVPECL/LVPECL	'111				+
1-to-9 Differential LVPECL Buffer With TTL OE	LVPECL/LVPECL	'112				+
1-to-10 Buffer With OE	TTL/TTL	'351				+
	TTL/TTL	'2351				+
1-to-6 PLL Buffer	TTL/TTL	'536				+
	TTL/TTL	'2536				+
1-to-12 PLL Buffer	TTL/TTL	'586				+
	TTL/TTL	'2586				+
1-to-12 PLL Buffer	LVPECL/TTL	'2582				+

✔ Product available in technology indicated
+ New product planned in technology indicated

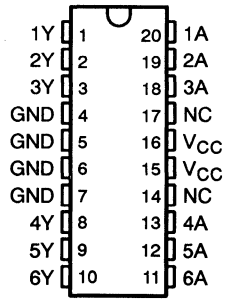
The following table lists military 5-V V_{CC} clock-driver circuits currently targeted for market introduction. Customers interested in learning more about TI's plans for these devices should contact military Advanced System Logic marketing at (915) 561-7289.

DEVICE	PIN/PACKAGE	DESCRIPTION
SN54CDC303	16/J, 16/W, 20/FK	Octal Divide-by-2 Circuit/Clock Driver
SN54CDC328	16/J, 16/W, 20/FK	1-Line to 6-Line Clock Driver With Selectable Polarity

SCAS098C – OCTOBER 1989 – REVISED MARCH 1994

- **CDC204 Replaces 74AC11204**
- **CDC204-7 Replaces 74AC11204-7**
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **CMOS-Compatible Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Package (DW) and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

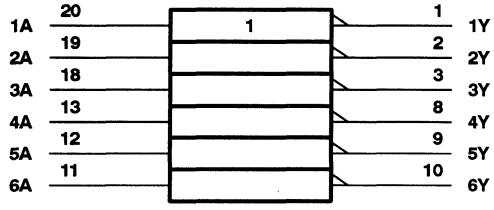
The CDC204/204-7 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC204/204-7 is characterized for operation from 25°C to 70°C.

FUNCTION TABLE

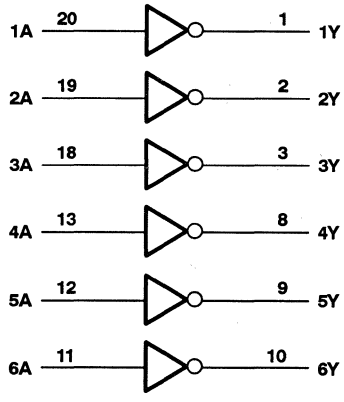
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	V_{CC} = 4.75 V	3.3			V
		V_{CC} = 5.25 V	3.7			
V_{IL}	Low-level input voltage	V_{CC} = 4.75 V			1.4	V
		V_{CC} = 5.25 V			1.6	
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.75 V			−24	mA
		V_{CC} = 5.25 V			−24	
I_{OL}	Low-level output current	V_{CC} = 4.75 V			24	mA
		V_{CC} = 5.25 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				80	MHz
T_A	Operating free-air temperature		25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C			CDC204		CDC204-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.75 V	4.65			4.65		4.65		V
		5.25 V	5.15			5.15		5.15		
	I_{OH} = −24 mA	4.75 V	4.19			4.05		4.05		
		5.25 V	4.68			4.55		4.55		
	I_{OH} = −75 mA†	5.25 V				3.6		3.6		
V_{OL}	I_{OL} = 50 μA	4.75 V			0.1		0.1		0.1	V
		5.25 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.75 V			0.36		0.44		0.44	
		5.25 V			0.36		0.44		0.44	
	I_{OL} = 75 mA†	5.25 V					1.65		1.65	
I_I	V_I = V_{CC} or GND	5.25 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.25 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

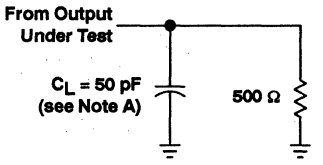
† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.25 V (see Note 2 and Figures 1 and 2)

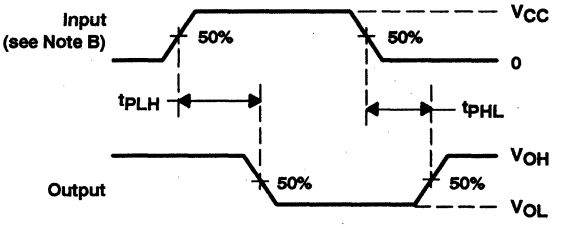
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC204		CDC204-7		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.7	5.7	3.7	5.7	ns
t_{PHL}			3.7	5.7	3.7	5.7	
$t_{sk(o)}$	A	Y		1		0.7	ns

NOTE 2: All specifications are valid only for all outputs switching simultaneously and in phase.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

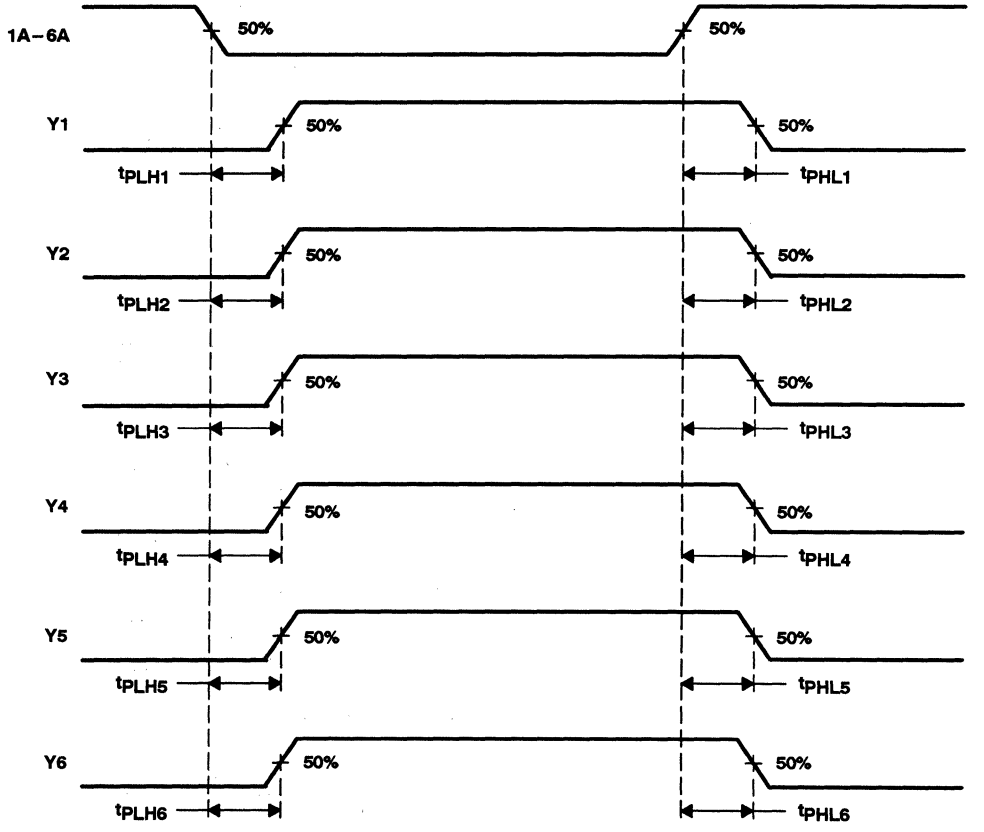


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

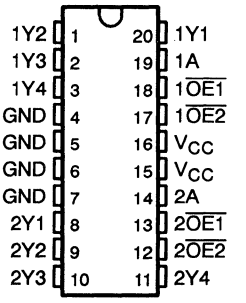


NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 6)
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 6)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **CDC208 Replaces 74ACT11208**
- **CDC208-7 Replaces 74ACT11208-7**
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages and Standard Plastic 300-mil DIPs (N)**

DB, DW, OR N PACKAGE
(TOP VIEW)



description

The CDC208/208-7 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC208/208-7 is characterized for operation from −40°C to 85°C.

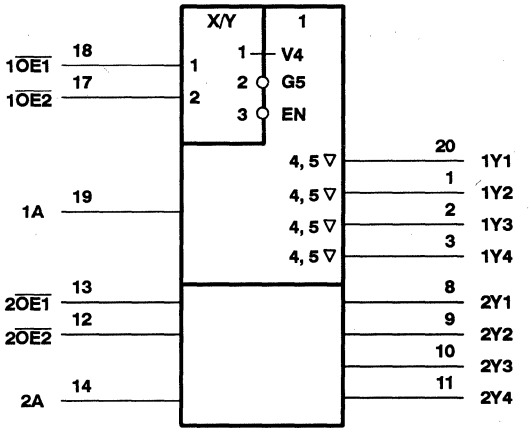
FUNCTION TABLES

INPUTS			OUTPUTS			
$1\overline{OE1}$	$1\overline{OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$2\overline{OE1}$	$2\overline{OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

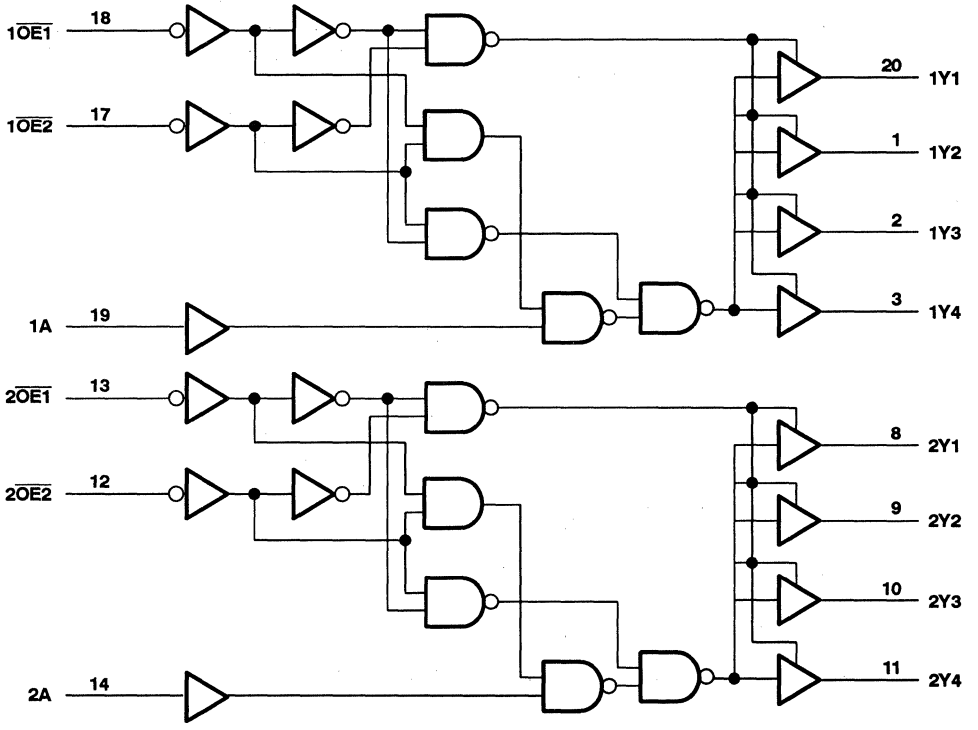
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
f_{clock}	Input clock frequency			60	MHz
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			CDC208		CDC208-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I_{OH} = −50 mA†	5.5 V								
	I_{OH} = −75 mA†	5.5 V				3.85		3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I_{OL} = 50 mA†	5.5 V								
	I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			CDC208		CDC208-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	5.3	8.5	10.9	5.3	11.7	5.3	11.7	ns
t_{PHL}			3.6	7.7	11	3.6	11.5	3.6	11.5	
t_{PLH}	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	4.7	8.5	11.7	4.7	12.8	4.7	12.8	ns
t_{PHL}			4.4	8.4	11.3	4.4	12.4	4.4	12.4	
t_{PZH}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	4.4	8.1	11.3	4.4	12.4	4.4	12.4	ns
t_{PZL}	$1\overline{OE1}$ or $2\overline{OE1}$		5	9.6	13.3	5	14.9	5	14.9	
t_{PHZ}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	4.2	7.4	9.3	4.2	10.2	4.2	10.2	ns
t_{PLZ}	$1\overline{OE1}$ or $2\overline{OE1}$		5.4	7.5	9.2	5.4	9.9	5.4	9.9	

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Note 2 and Figures 1 and 2)

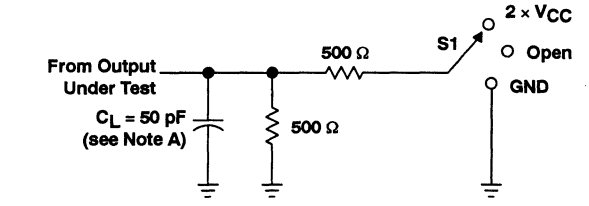
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC208		CDC208-7		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	7.6	10.2	7.6	10.2	ns
t_{PHL}			6.6	9.8	6.6	9.8	
$t_{sk(o)}$	1A and 2A	Any Y		1		0.7	ns

NOTE 2: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

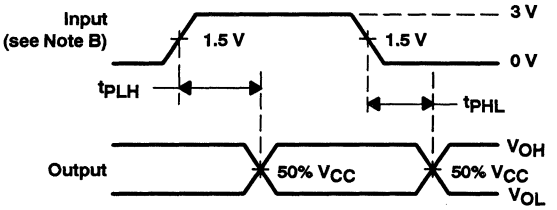
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	96	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

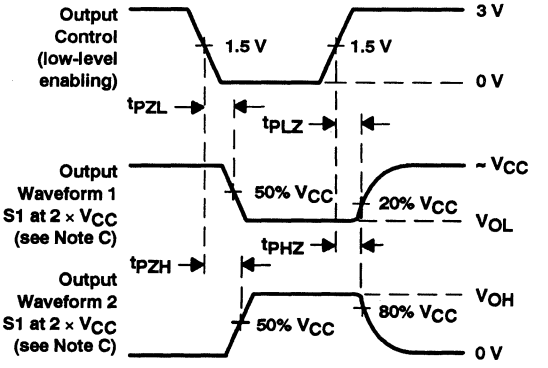


(see Note A) LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

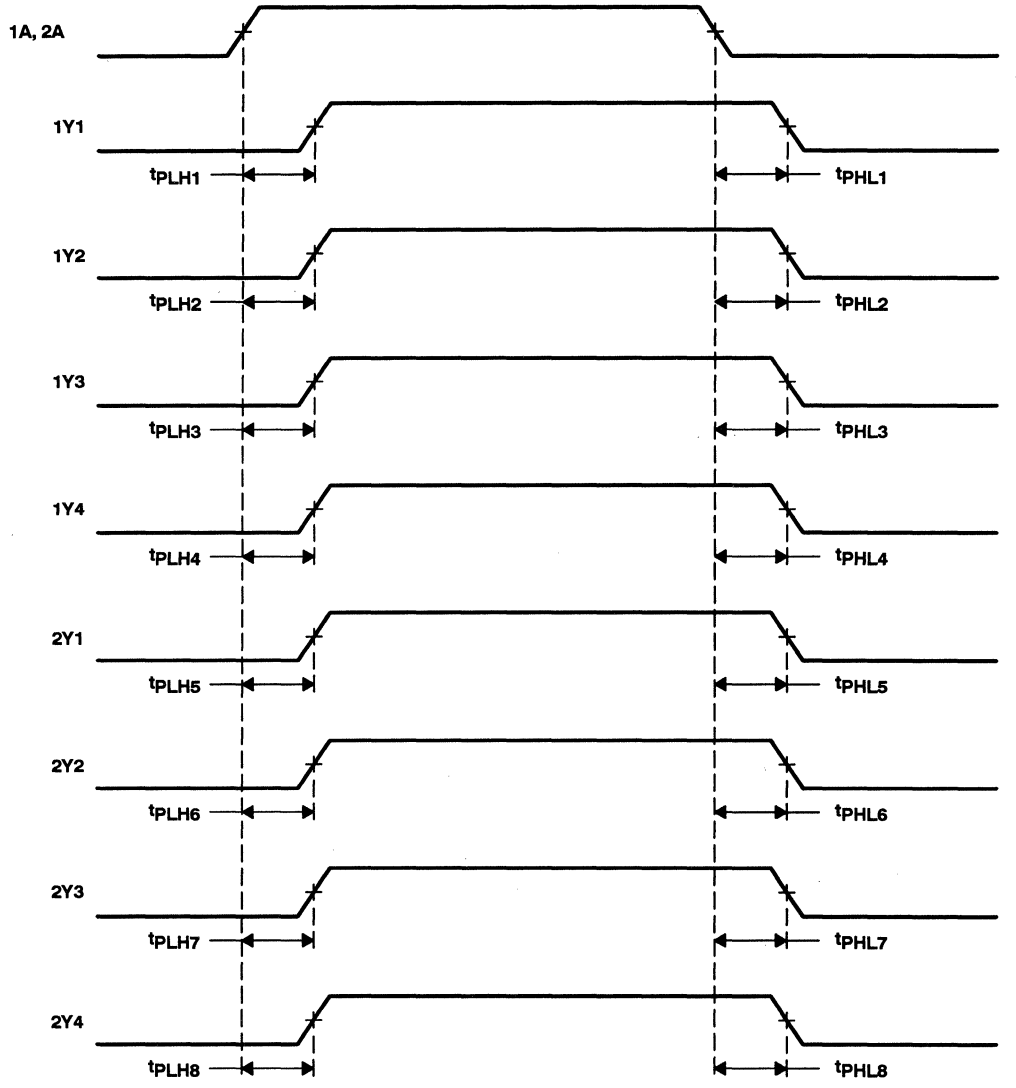


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

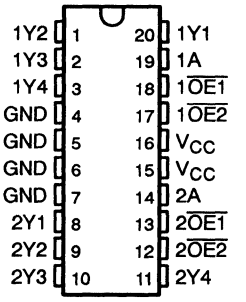


NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **CDC209 Replaces 74AC11208**
- **CDC209-7 Replaces 74AC11208-7**
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **CMOS-Compatible Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Characterized for Operation at 5-V and 3.3-V V_{CC}**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Package (DW) and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



description

The CDC209/209-7 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC209/209-7 is characterized for operation from –40°C to 85°C.

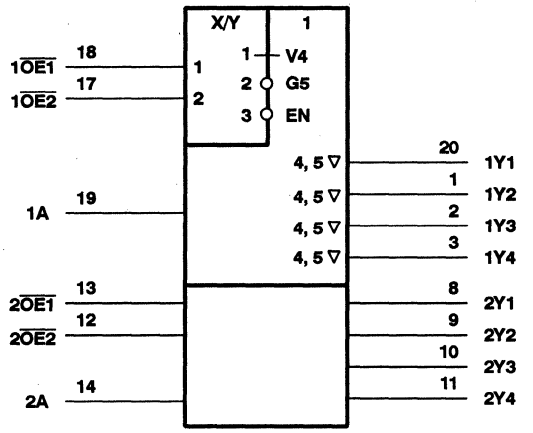
FUNCTION TABLES

INPUTS			OUTPUTS			
$1\overline{OE1}$	$1\overline{OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$2\overline{OE1}$	$2\overline{OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

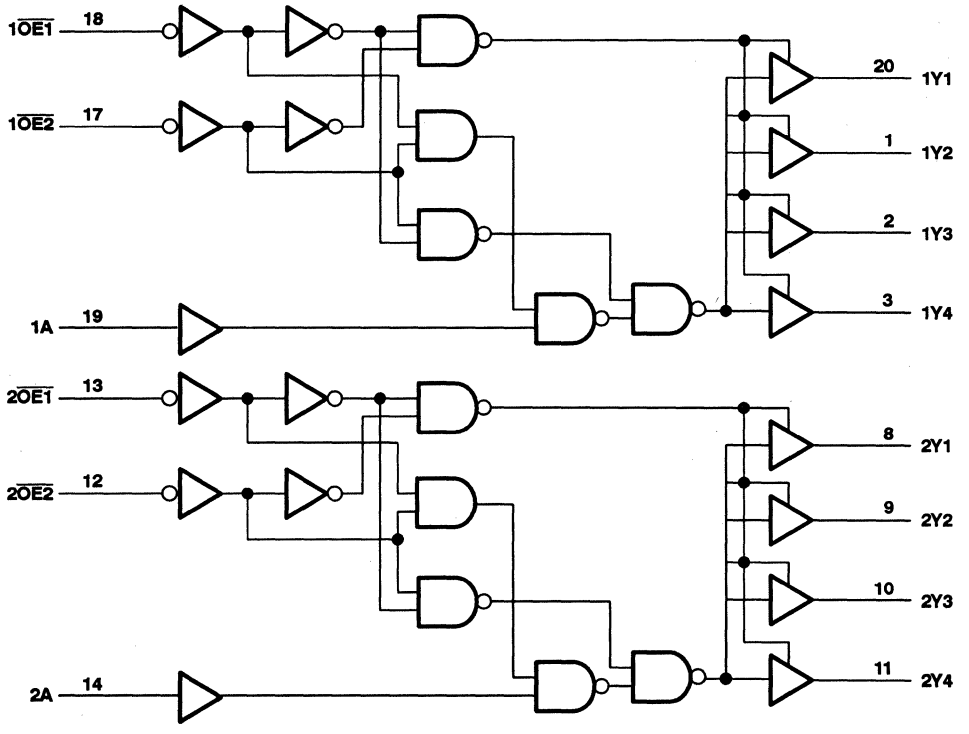
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				60	MHz
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.8	11.1	13.1	4.8	14.6	4.8	14.6	ns
t_{PHL}			5.1	12.2	14.3	5.1	15.6	5.1	15.6	
t_{PLH}	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	5.2	11.9	14.2	5.2	15.8	5.2	15.8	ns
t_{PHL}			7.8	13.3	15.7	7.8	17.4	7.8	17.4	
t_{PZH}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	5.1	11.8	14.2	5.1	15.7	5.1	15.7	ns
t_{PZL}	$1\overline{OE1}$ or $2\overline{OE1}$		6.8	16.3	19.5	6.8	22.8	6.8	22.8	
t_{PHZ}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	3.4	6.9	8.6	3.4	9.2	3.4	9.2	ns
t_{PLZ}	$1\overline{OE1}$ or $2\overline{OE1}$		4.1	7.5	9.4	4.1	10.2	4.1	10.2	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			CDC209		CDC209-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.2	5.5	9	4.2	9.9	4.2	9.9	ns
t_{PHL}			4.2	7	9.3	4.2	10.1	4.2	10.1	
t_{PLH}	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	4.6	7.3	9.6	4.6	10.7	4.6	10.7	ns
t_{PHL}			4.8	7.7	10.2	4.8	11	4.8	11	
t_{PZH}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	4.3	7.2	9.4	4.3	10.4	4.3	10.4	ns
t_{PZL}	$1\overline{OE1}$ or $2\overline{OE1}$		5.3	9	12.2	5.3	13.5	5.3	13.5	
t_{PHZ}	$1\overline{OE2}$ or $2\overline{OE2}$	Any Y	3	5.4	7.5	3	8	3	8	ns
t_{PLZ}	$1\overline{OE1}$ or $2\overline{OE1}$		3.7	5.7	7.5	3.7	8.2	3.7	8.2	

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Note 2 and Figures 1 and 2)

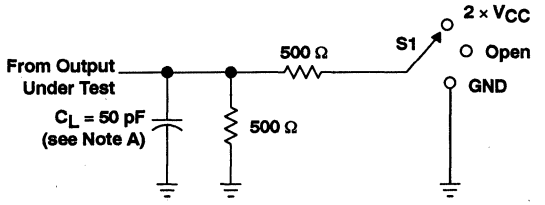
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC209		CDC209-7		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	6	8.5	6	8.5	ns
t_{PHL}			6	8.5	6	8.5	
$t_{sk(o)}$	1A and 2A	Any Y		1		0.7	ns

NOTE 2: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

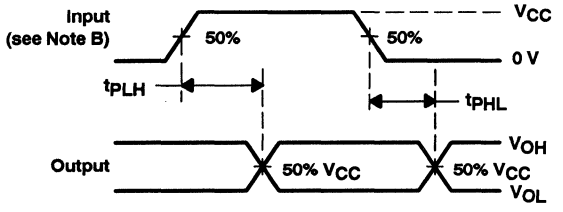
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	95	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

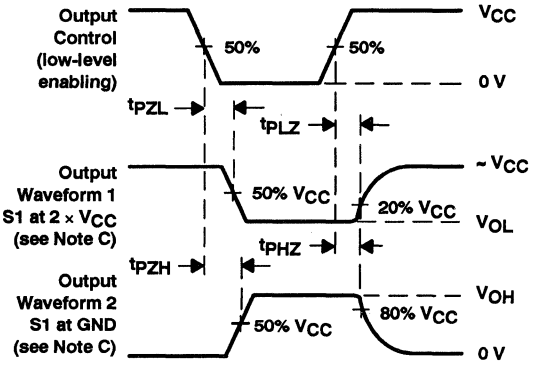


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

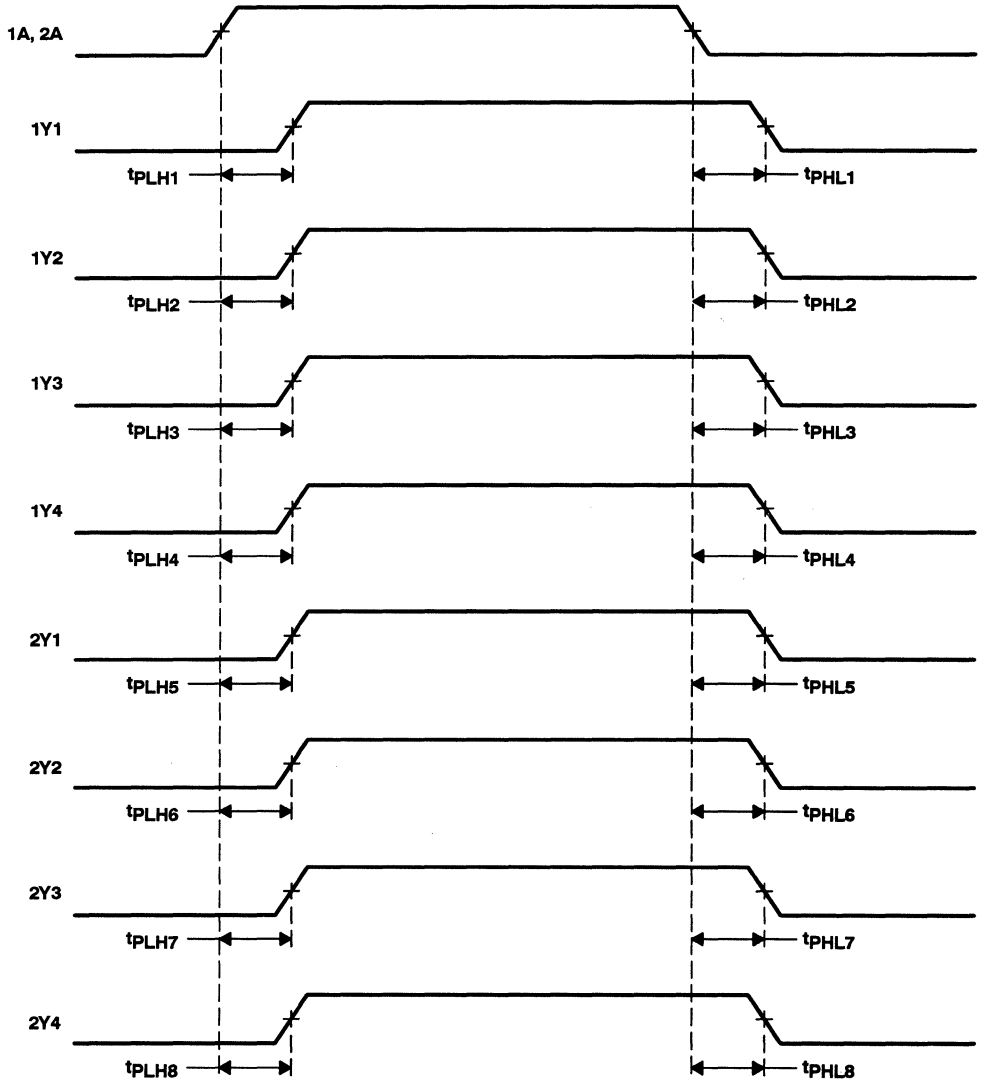


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



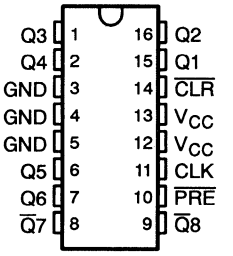
NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

SCAS323 – JULY 1990 – REVISED MARCH 1994

- **Replaces SN74AS303**
- **Maximum Output Skew Between Same Phase Outputs of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **TTL-Compatible Inputs and Outputs**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic Small-Outline Package (D) and Standard Plastic 300-mil DIPs (N)**

D OR N PACKAGE
(TOP VIEW)



description

The CDC303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. Preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the clock (CLK) input.

The CDC303 has output and pulse-skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

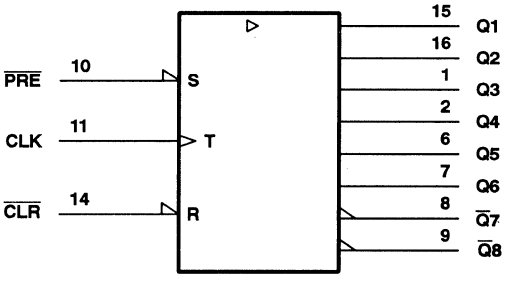
The CDC303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q6	$\overline{Q7}$–$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

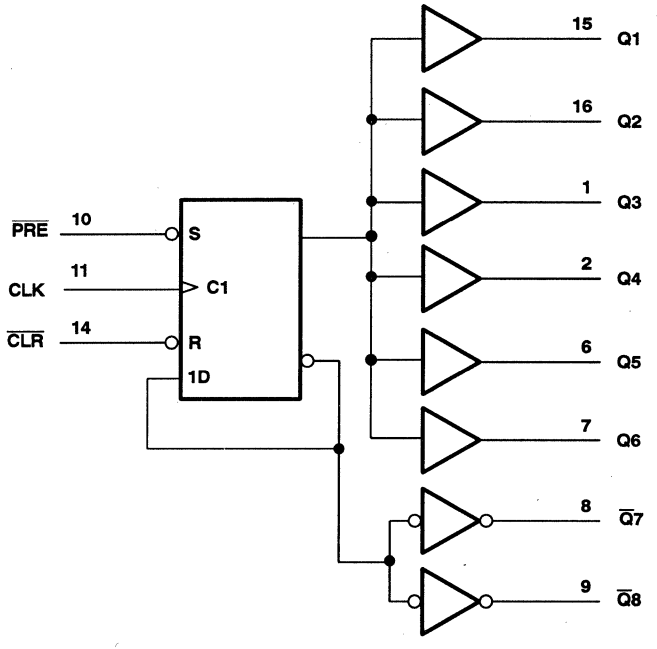
† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
f_{clock}	Input clock frequency			80	MHz
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

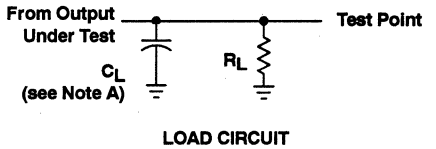
			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

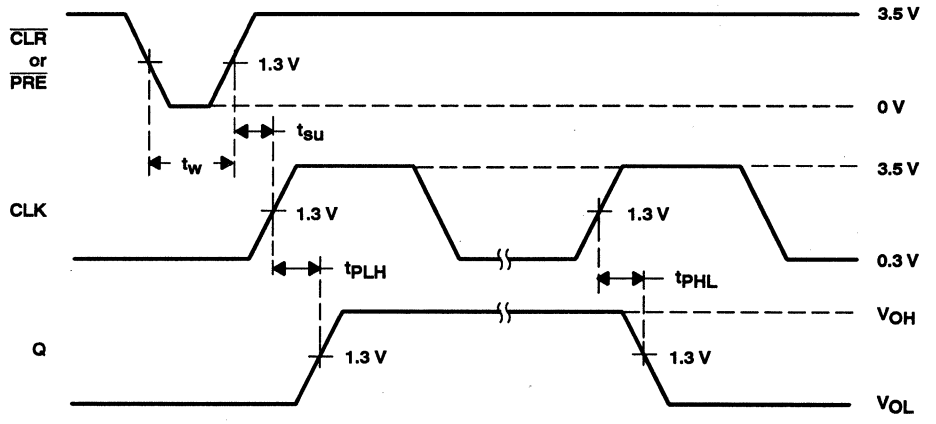
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§				80		MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	9	ns
t_{PHL}				2	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	12	ns
t_{PHL}				3	12	
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF, See Figure 2		1	ns
		$\overline{Q}$			1	
		Q, $\overline{Q}$			2	
$t_{sk(p)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
t_r					4.5	ns
t_f					3.5	ns

§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



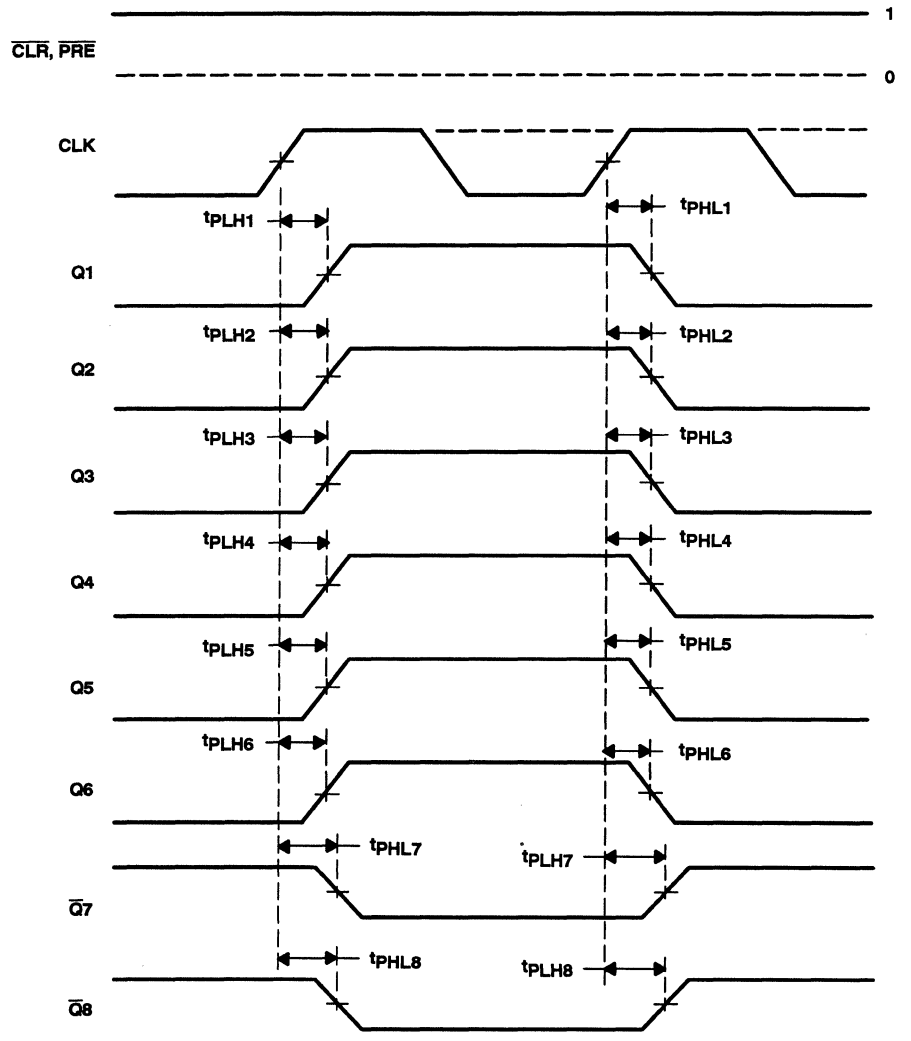
LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6)

B. $t_{sk(o)}$, CLK to $\overline{Q}$, is calculated as the greater of: $|t_{PLH7} - t_{PLH8}|$ and $|t_{PHL7} - t_{PHL8}|$.

C. $t_{sk(o)}$, CLK to Q and $\overline{Q}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6), t_{PHL7}, and t_{PHL8}
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6), t_{PLH7}, and t_{PLH8}

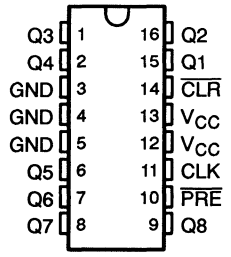
D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, . . ., 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

SCAS325 – JULY 1990 – REVISED MARCH 1994

- **Replaces SN74AS304**
- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1.5 ns**
- **TTL-Compatible Inputs and Outputs**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic Small-Outline Package (D) and Standard Plastic 300-mil DIPs (N)**

D OR N PACKAGE
(TOP VIEW)



description

The CDC304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (in-phase with CLK) toggle on successive CLK pulses. Preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs are provided to set the Q outputs high or low independent of the clock (CLK) input.

The CDC304 has output and pulse-skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

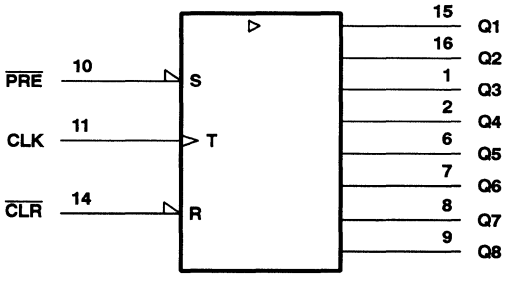
The CDC304 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q8
L	H	X	L
H	L	X	H
L	L	X	L†
H	H	↑	$\overline{Q}_0$
H	H	L	Q_0

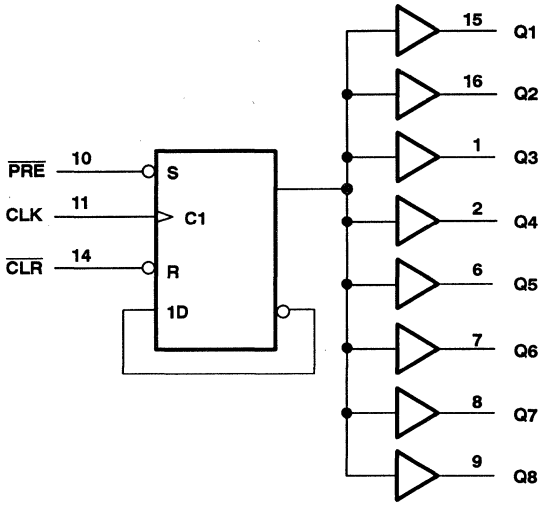
† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
f_{clock}	Input clock frequency			80	MHz
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		45	75	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

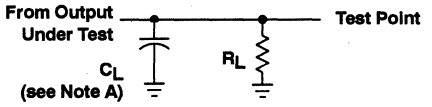
			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

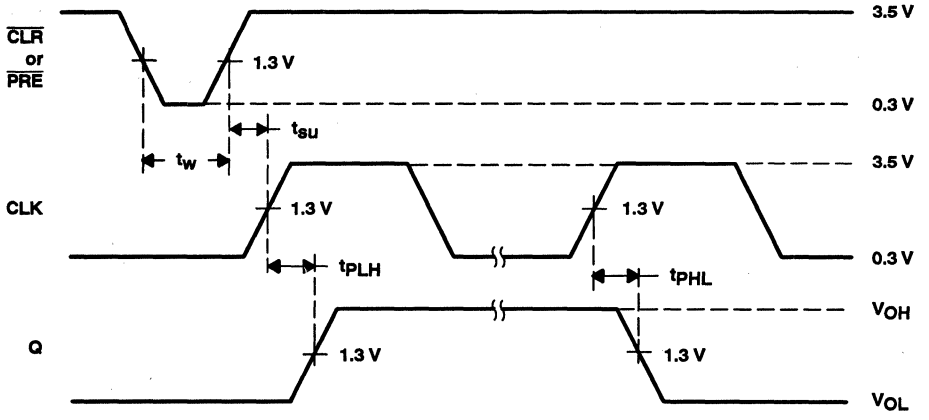
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				80			MHz
t_{PLH}	CLK	Q	R_L = 500 Ω, C_L = 50 pF	2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q	R_L = 500 Ω, C_L = 50 pF	3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF, See Figure 2			1	ns
$t_{sk(p)}$	CLK	Q1, Q8	R_L = 500 Ω, C_L = 10 pF to 30 pF			1	ns
		Q2–Q7				1.5	
t_r						4.5	ns
t_f						3.5	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



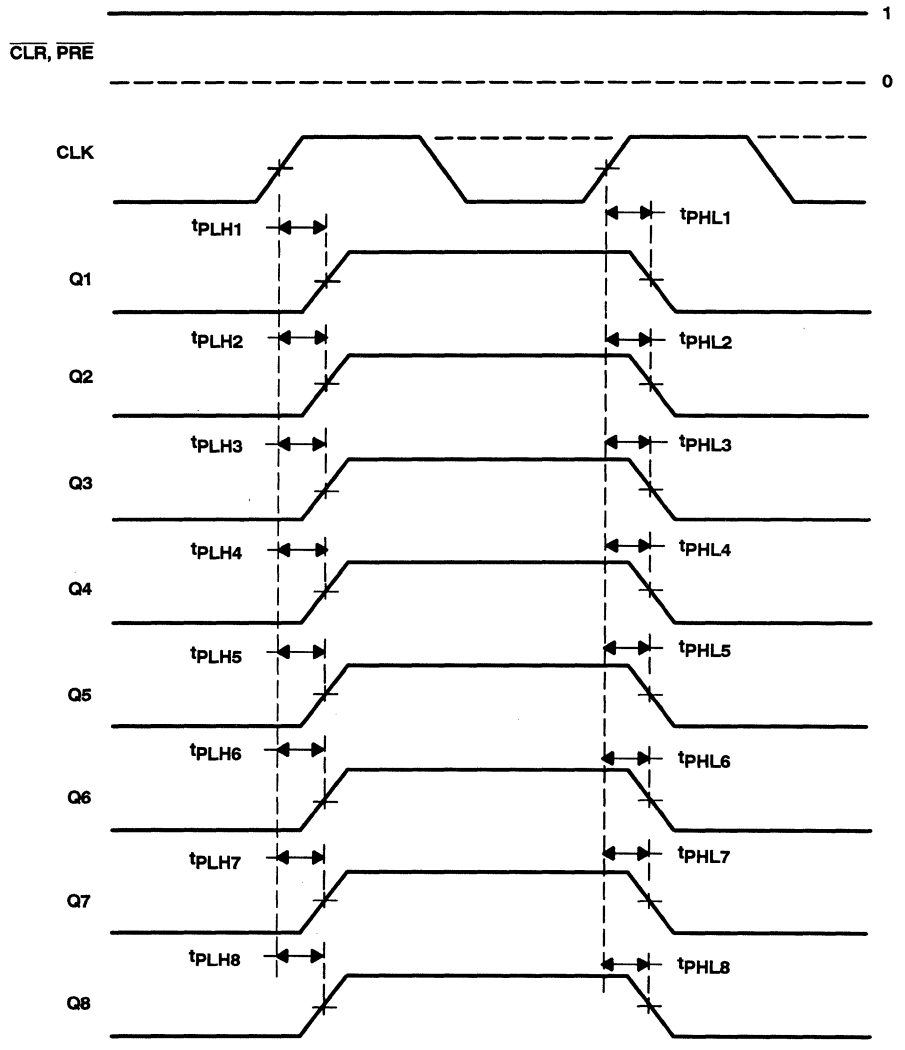
LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of the following:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3 . . ., 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3 . . ., 8)

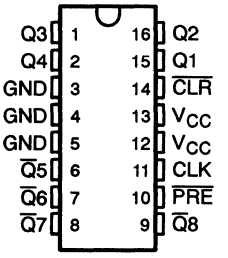
B. $t_{sk(p)}$ is defined at the greater of $| t_{PLHn} - t_{PHLn} |$ (n = 1, 2, 3, . . ., 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

SCAS326 – JUNE 1990 – REVISED MARCH 1994

- **Replaces SN74AS305**
- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **TTL-Compatible Inputs and Outputs**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic Small-Outline Package (D) and Standard Plastic 300-mil DIPs (N)**

D OR N PACKAGE
(TOP VIEW)



description

The CDC305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. Preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the clock (CLK) input.

The CDC305 has output and pulse-skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

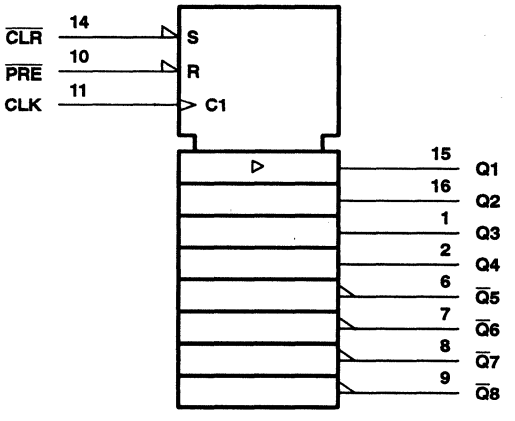
The CDC305 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q4	$\overline{Q5}$–$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	L	Q_0	$\overline{Q}_0$
H	H	↑	$\overline{Q}_0$	Q_0

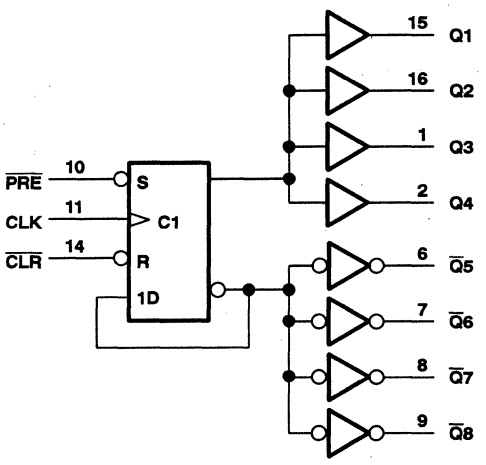
† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

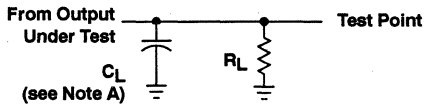
			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

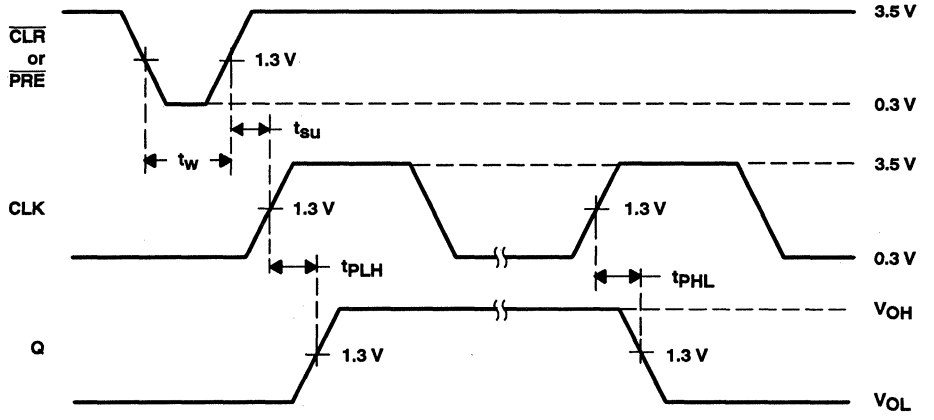
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				80			MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(o)}$	CLK	$\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF, See Figure 2			1	ns
		Q				1	
		Q1–$\overline{Q8}$				1.5	
$t_{sk(p)}$	CLK	Q1, $\overline{Q8}$	R_L = 500 Ω, C_L = 10 pF to 30 pF			1.5	ns
		Q2–$\overline{Q7}$				2	
t_r						4.5	ns
t_f						3.5	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



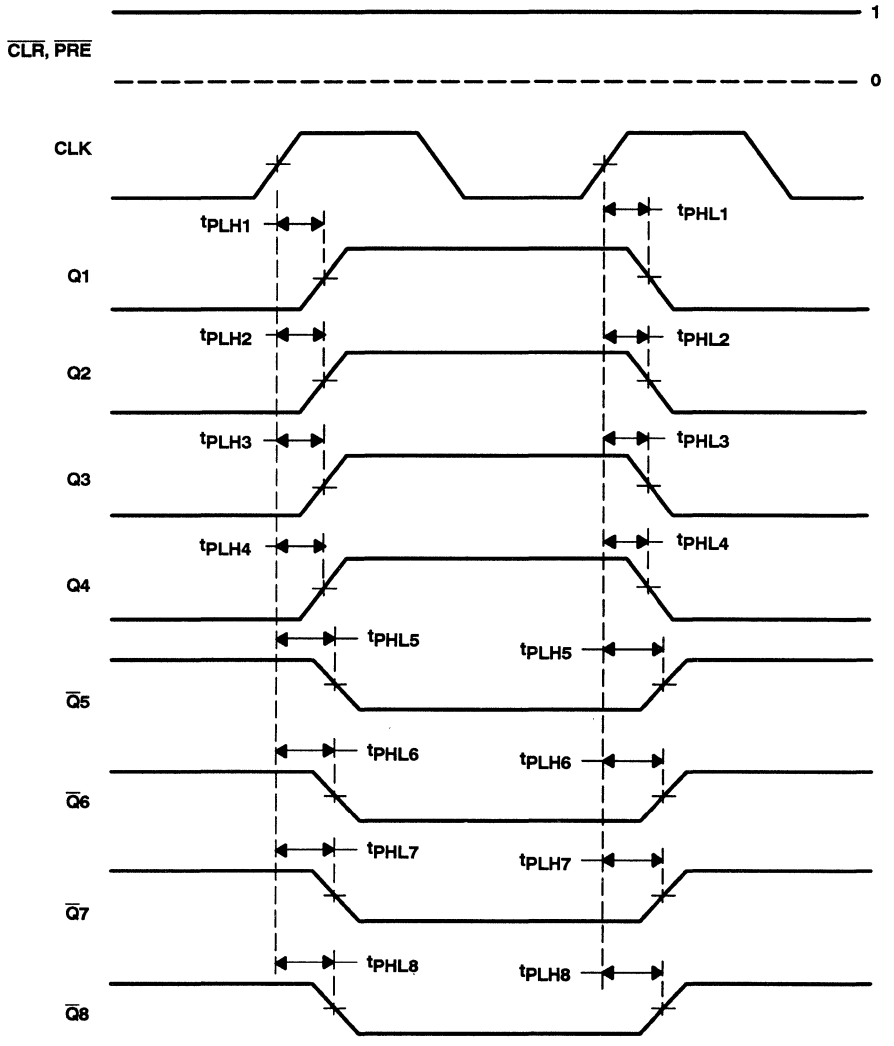
LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_{sk(o)}$ CLK to Q are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4)

B. $t_{sk(o)}$ CLK to $\overline{Q}$ are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 5, 6, 7, 8)

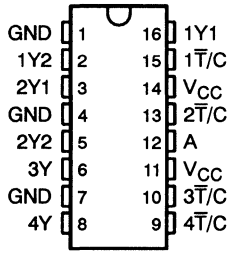
C. $t_{sk(o)}$ CLK to Q and $\overline{Q}$ are calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4), t_{PHLn} (n = 5, 6 , 7, 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4), t_{PLHn} (n = 5, 6, 7, 8)

D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, . . . , 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Replaces SN74ABT328**
- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–15-mA I_{OH}, 64-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B* ™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages**

D OR DB PACKAGE
(TOP VIEW)



description

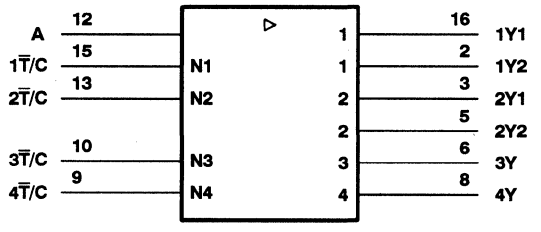
The CDC328 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ($\overline{T}$/C), various combinations of true and complementary outputs can be obtained.

The CDC328 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{T}$/C	A	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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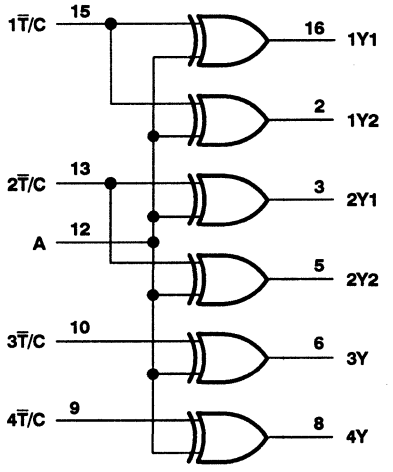
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state
or power-off state, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1000 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			80	MHz
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –15 mA		2.5			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 64 mA				0.55	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	μA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–15		–100	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			50	μA
			Outputs low		20	30	mA
C_i	V_I = 2.5 V or 0.5 V				3		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

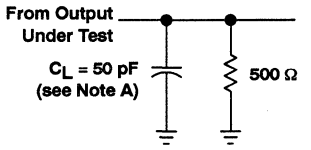
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	A	Any Y	1.7		7	ns
t_{PHL}			1.5		5.4	
t_{PLH}	$\overline{T}$/C	Any Y	1.5		8	ns
t_{PHL}			1.4		6.6	
$t_{sk(o)}$	A	Any Y (same phase)			0.7	ns
		Any Y (any phase)			2.6	
t_r				1.2		ns
t_f				0.5		ns

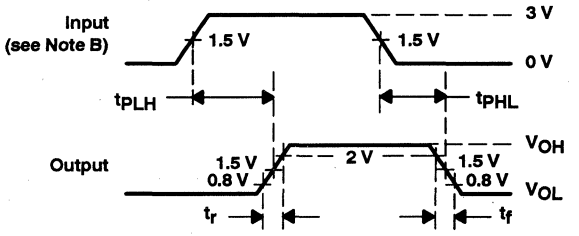
switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Any Y	2.1	6.1	ns
t_{PHL}			1.7	4.8	
$t_{sk(o)}$	A	Any Y (same phase)		0.7	ns
		Any Y (any phase)		2.1	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

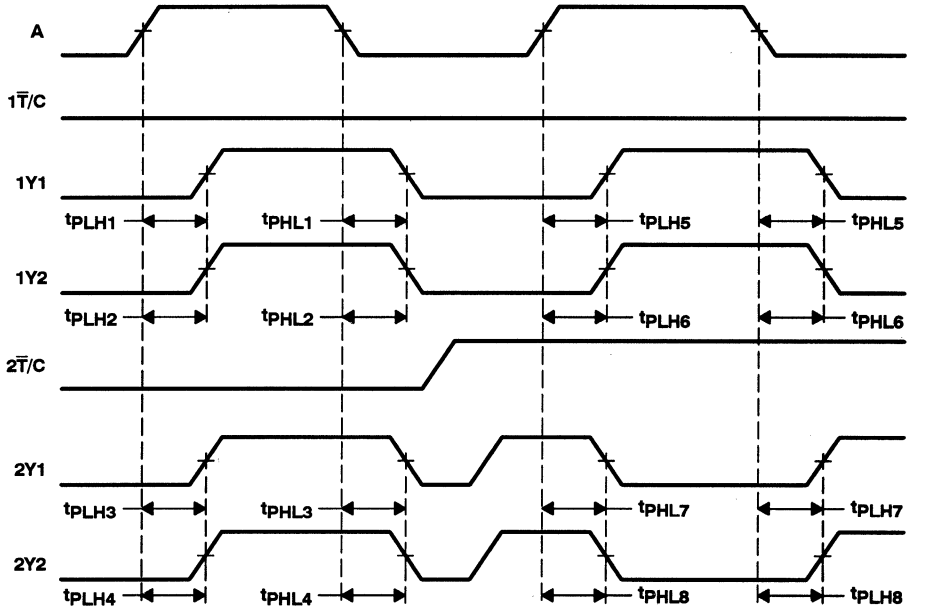


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



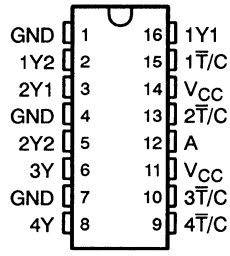
NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages**

D OR DB PACKAGE
(TOP VIEW)



description

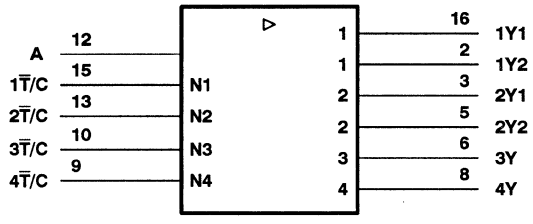
The CDC328A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ($\overline{T}$/C), various combinations of true and complementary outputs can be obtained.

The CDC328A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{T}$/C	A	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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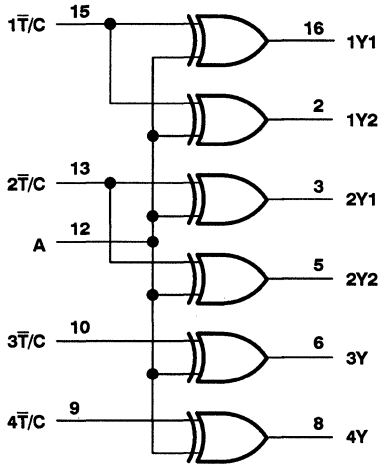
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state
or power-off state, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1000 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−48	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

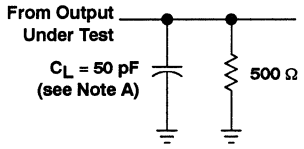
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –48 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA				0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	μA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–15		–100	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			10	mA
			Outputs low			32	
C_i	V_I = 2.5 V or 0.5 V				3		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

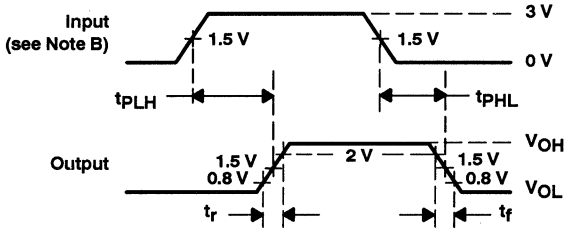
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Any Y	1.7	5.5	ns
t_{PHL}			1.5	5.5	
t_{PLH}	$\overline{T}$/C	Any Y	1.5	5	ns
t_{PHL}			1.4	5	
$t_{sk(o)}$	A	Any Y (same phase)		0.5	ns
		Any Y (any phase)		1.1	
t_r		Any Y		1.5	ns
t_f		Any Y		1.5	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



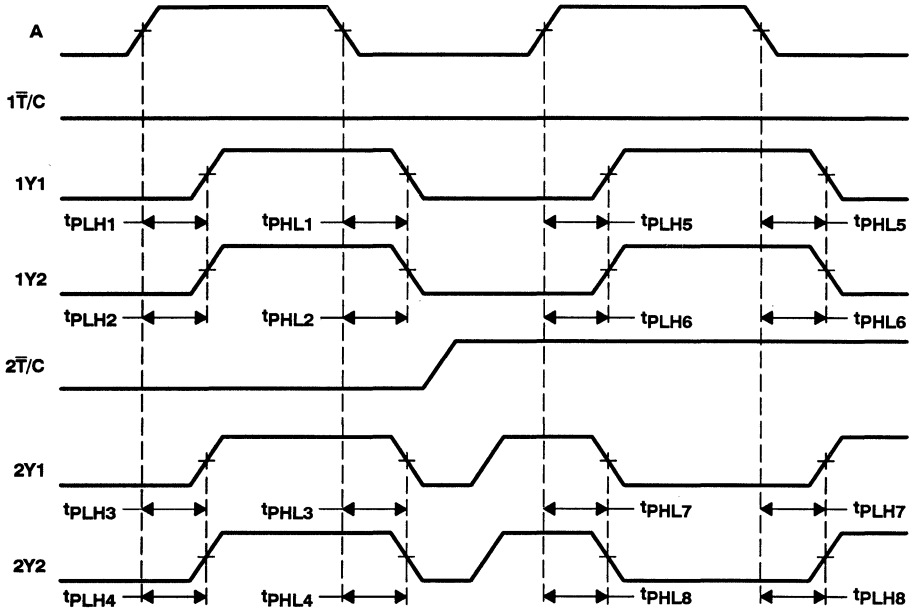
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



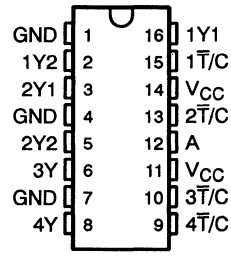
NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaged in Plastic Small-Outline Package**

D PACKAGE
(TOP VIEW)



description

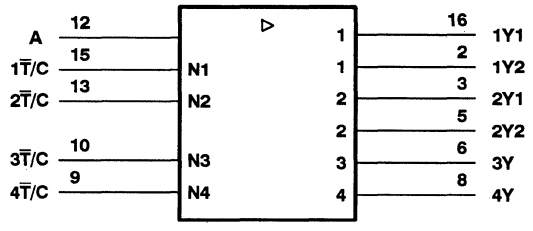
The CDC329A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ($\overline{T}$/C), various combinations of true and complementary outputs can be obtained.

The CDC329A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{T}$/C	A	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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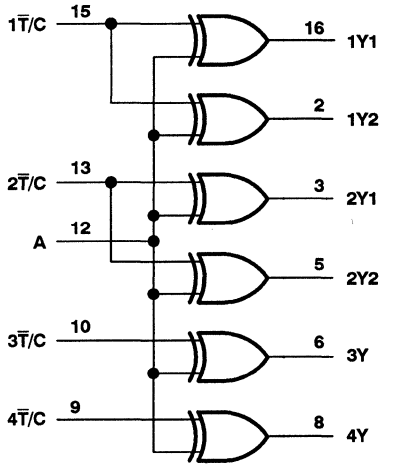
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1000 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−32	mA
I_{OL}	Low-level output current			32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			80	MHz
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

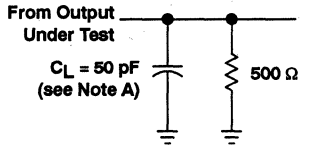
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 32 mA		3.85			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA				0.55	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	µA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			10	mA
			Outputs low			40	
C_i	V_I = 2.5 V or 0.5 V				3		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C

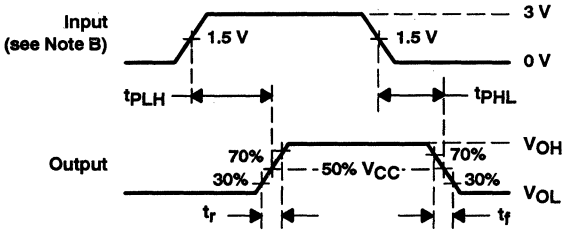
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	A	Any Y	2		5.9	ns
t_{PHL}			1.7		5.9	
t_{PLH}	T/C	Any Y	1.5		5	ns
t_{PHL}			1.5		5	
$t_{sk(o)}$	A	Any Y (same phase)			0.6	ns
		Any Y (any phase)			1.5	
t_r				1.3		ns
t_f				0.85		ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

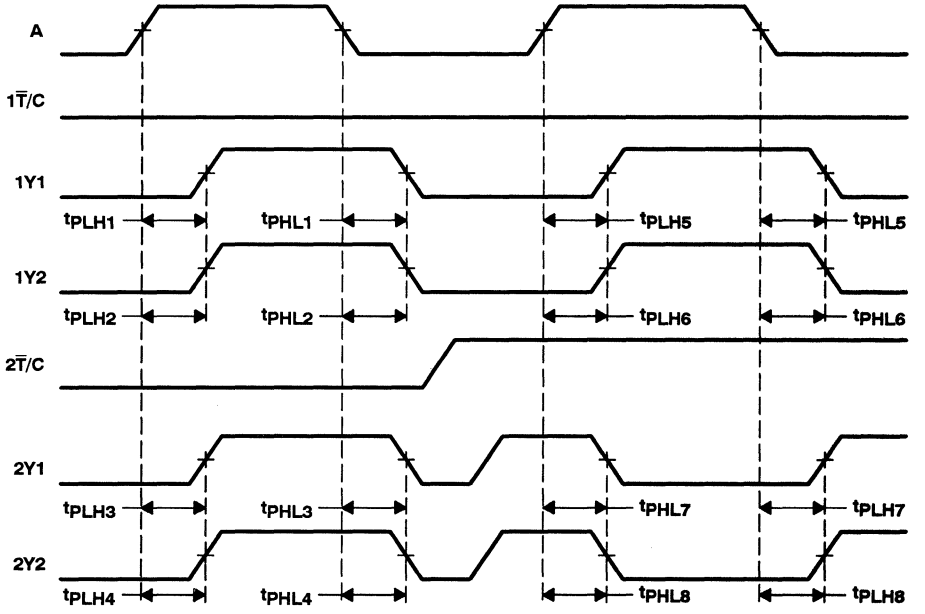


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



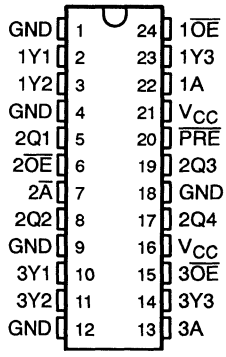
NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Two Banks Distribute One Clock Input to Three Same-Frequency Clock Outputs**
- **One Bank Distributes One Clock Input to Four Half-Frequency Clock Outputs**
- **Internal Power-Up Circuit**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Symmetrical Output Drive (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



description

The CDC330 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring output signals at both the primary clock frequency and one-half the primary clock frequency.

This device contains two banks that fan out one input to three same-frequency outputs and one bank that fans out one input to four half-frequency outputs with minimum skew for clock distribution. Each bank of Y outputs switch in phase and at the same frequency as its clock (A) input. The four Q outputs switch at one-half the frequency of their clock ($2\overline{A}$) input.

When the output-enable ($2\overline{OE}$) input is low and the preset ($\overline{PRE}$) input is high, the Q outputs toggle on high-to-low transitions of $2\overline{A}$. Taking $\overline{PRE}$ low asynchronously presets the Q outputs to the high level. When a bank's $\overline{OE}$ input is high, the outputs are in the high-impedance state.

The CDC330 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

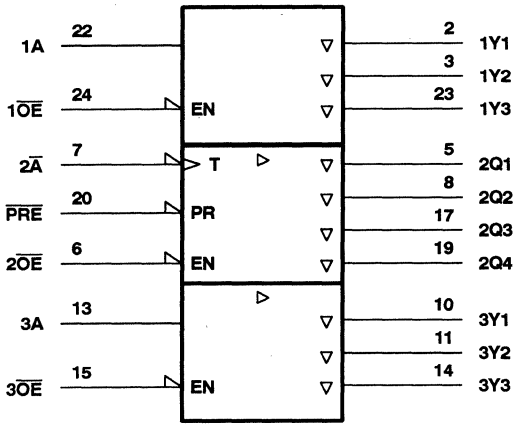
INPUTS		OUTPUTS
$n\overline{OE}$	nA	nY1–nY3
H	X	Z
L	L	L
L	H	H

n = 1, 3

INPUTS			OUTPUTS
$2\overline{OE}$	$\overline{PRE}$	$2\overline{A}$	2Q1–2Q3
H	X	X	Z
L	L	L	H
L	H	↓	Toggle

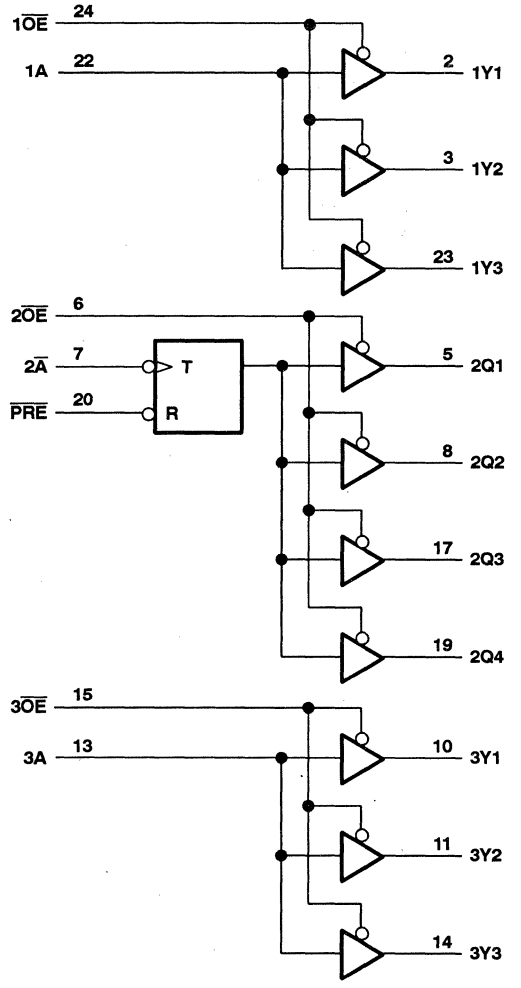
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 32 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA				0.5	V
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				50	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.5 V				–50	µA
I_{OZ}	V_{CC} = 5.25 V,	V_O = V_{CC} or GND				±50	µA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–30		–180	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		11	40	mA
			Outputs low		15	30	
			Outputs disabled		10	30	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = 2.5 V or 0.5 V				9		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	1A/3A (duty cycle 40 – 60%)		67	MHz
		$2\overline{A}$ (duty cycle 40 – 60%)		100	MHz
t_w	Pulse duration	1A/3A low	5.9		ns
		1A/3A high	5.9		
		$2\overline{A}$ low	2.8		
		$2\overline{A}$ high	4.5		
		$\overline{PRE}$ low	3		
t_{su}	Setup time	$\overline{PRE}$ inactive before $2\overline{A}\downarrow$	2		ns

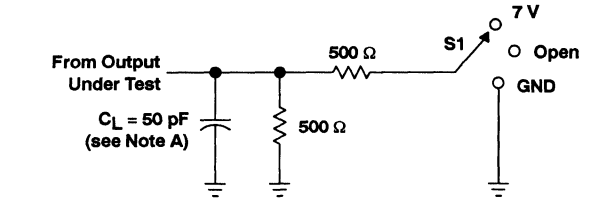
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}†	1A or 3A	Any 1Y or 3Y	67		MHz
	$\overline{2A}$	Any Q	100		
t_{PLH}	Any A or $\overline{A}$	Any Y or Q		11	ns
t_{PHL}				10.5	
t_{PHL}	$\overline{PRE}$	Any Q		12.5	ns
t_{PZH}	Any $\overline{OE}$	Any Y or Q		9	ns
t_{PZL}				8.5	
t_{PHZ}	Any $\overline{OE}$	Any Y or Q		8.5	ns
t_{PLZ}				9	
$t_{sk(o)}$	1A	Any 1Y		0.4	ns
	3A	Any 3Y		0.4	
	1A or 3A	Any 1Y or 3Y		0.5	
	$\overline{2A}$	Any Q		0.4	
$t_{sk(pr)}$	Any A or $\overline{A}$	Any Y or Q		1	ns

† Duty cycle 40 – 60%

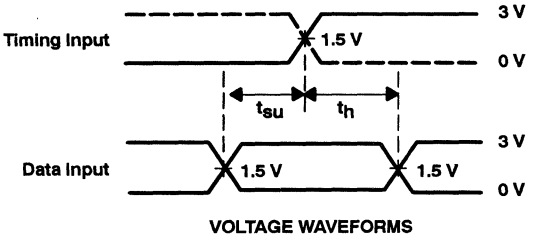
NOTE 3: All specifications are valid only for all outputs switching.

PARAMETER MEASUREMENT INFORMATION

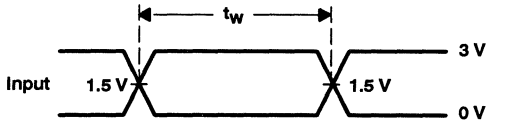


LOAD CIRCUIT

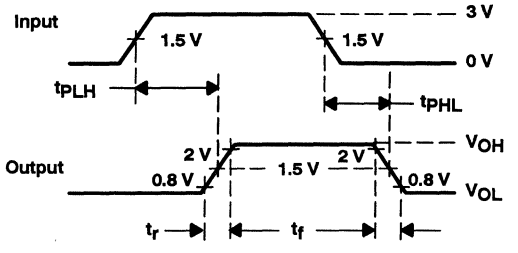
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



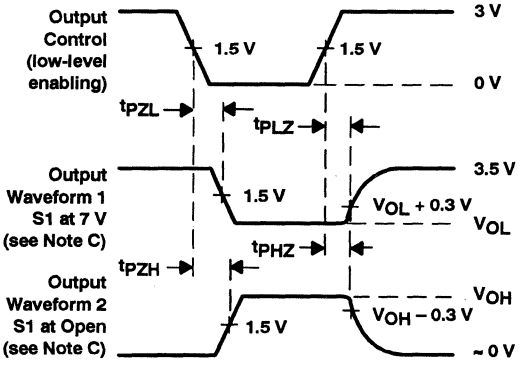
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

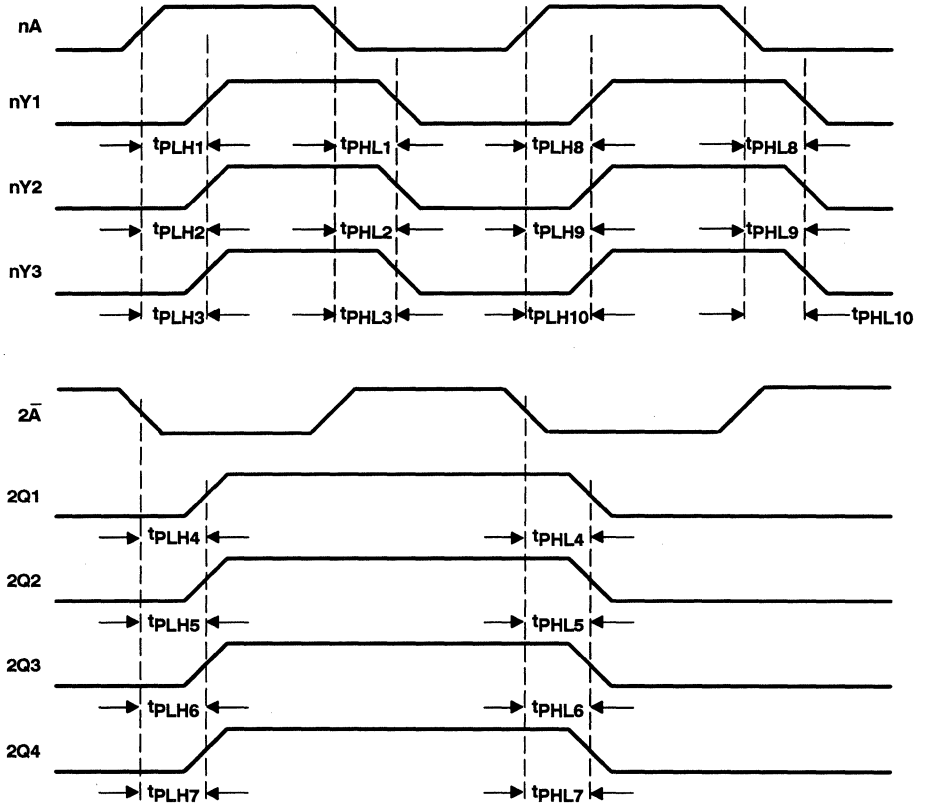


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



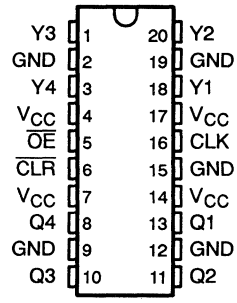
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3)
- The difference between the fastest and slowest of t_{PLHn} (n = 4, 5, 6, 7)
- The difference between the fastest and slowest of t_{PLHn} (n = 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3)
- The difference between the fastest and slowest of t_{PHLn} (n = 4, 5, 6, 7)
- The difference between the fastest and slowest of t_{PHLn} (n = 8, 9, 10)

B. Process skew, $t_{sk(pr)}$, is calculated the same as output skew, $t_{sk(o)}$, across multiple CDC330 devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Distributes One Clock Input to Eight Outputs**
  - **Four Same-Frequency Outputs**
  - **Four Half-Frequency Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC337 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

When the output-enable ($\overline{OE}$) input is low and the clear ($\overline{CLR}$) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions at CLK. Taking $\overline{CLR}$ low asynchronously resets the Q outputs to the low level. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The CDC337 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{CLR}$	CLK	Y1–Y4	Q1–Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q_0†
L	H	↑	H	$\overline{Q}_0$†

† The level of the Q outputs before the indicated steady-state input conditions were established.

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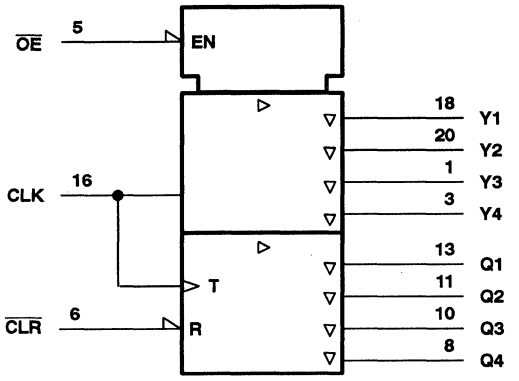
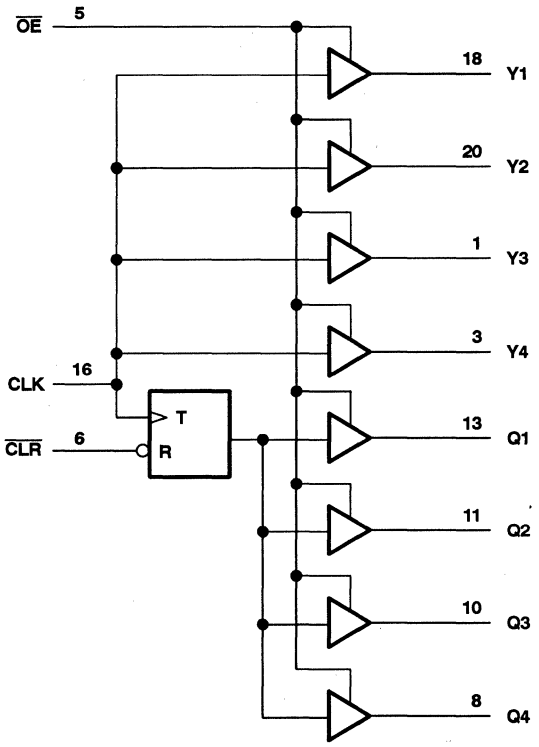
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	−40	85	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = − 32 mA		3.75			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA				0.55	V
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				50	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.5 V				−50	μA
I_{OZ}	V_{CC} = 5.25 V,	V_O = V_{CC} or GND				±50	μA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			70	mA
			Outputs low			85	
			Outputs disabled			70	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = VCC or GND				10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

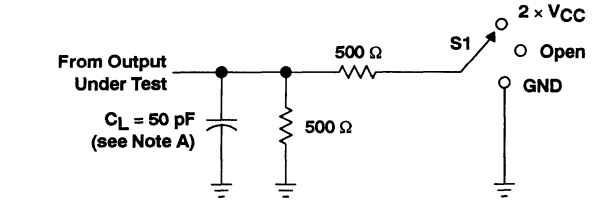
			MIN	MAX	UNIT
f_{clock}	Clock frequency			80	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		ns
		CLK low	4		
		CLK high	4		
t_{su}	Setup time, $\overline{CLR}$ inactive before CLK↑		2		ns
	Clock duty cycle		40%	60%	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			80			MHz
t_{PLH}	CLK	Any Y or Q	4		9	ns
t_{PHL}			4		9	
t_{PHL}	$\overline{CLR}$	Any Q	4		10	ns
t_{PZH}	$\overline{OE}$	Any Y or Q	3		7	ns
t_{PZL}			3		7	
t_{PHZ}	$\overline{OE}$	Any Y or Q	2		7	ns
t_{PLZ}			2		7	
$t_{sk(o)}$	CLK↑	Y↑			0.75	ns
		Q↑			0.9	
		Y↑ and Q↑			0.9	
t_r				0.9		ns
t_f				0.7		ns

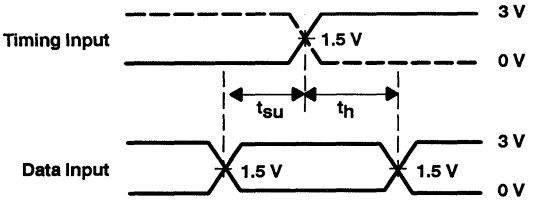
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: All specifications are valid only for all outputs switching.

PARAMETER MEASUREMENT INFORMATION

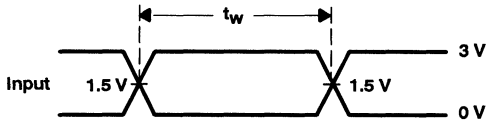


LOAD CIRCUIT

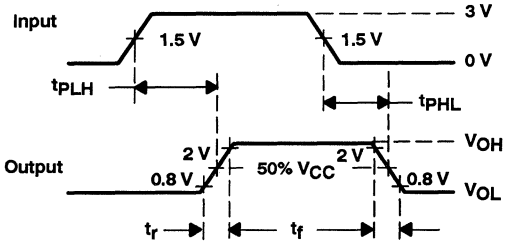
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open



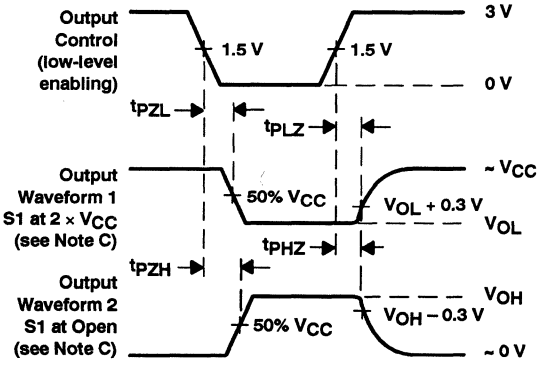
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

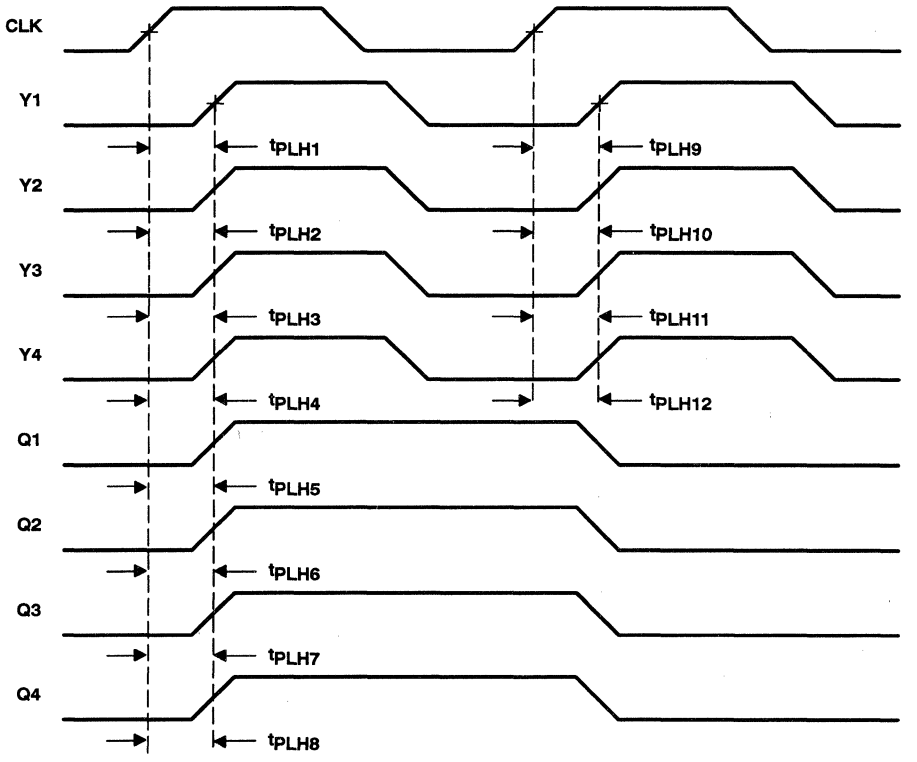


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4) or t_{PLHn} (n = 9, 10, 11, 12).

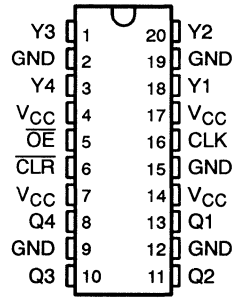
B. Output skew, $t_{sk(o)}$, from CLK↑ to Q↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8).

C. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑ and Q↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8).

Figure 2. Skew Waveforms and Calculations

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
  - **Four Same-Frequency Outputs**
  - **Four Half-Frequency Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC339 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the primary clock frequency and one-half the primary clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

When the output-enable ($\overline{OE}$) input is low and the clear ($\overline{CLR}$) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions of CLK. Taking $\overline{CLR}$ low asynchronously resets the Q outputs to the low level. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The CDC339 is characterized for operation from –40°C to 85°C.

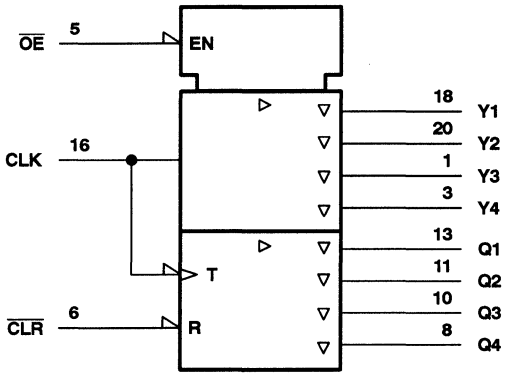
FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{CLR}$	CLK	Y1–Y4	Q1–Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q_0†
L	H	↑	H	$\overline{Q}_0$†

† The level of the Q outputs before the indicated steady-state input conditions were established.

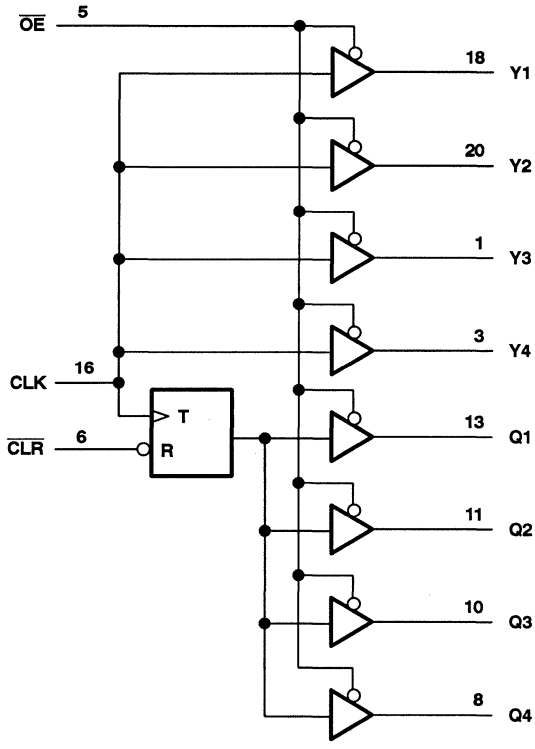
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	−40	85	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = − 48 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA				0.5	V
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				50	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.5 V				−50	μA
I_{OZ}	V_{CC} = 5.25 V,	V_O = 2.7 V or 0.5 V				±50	μA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		−50		−180	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			70	mA
			Outputs low			85	
			Outputs disabled			70	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = 2.5 V or 0.5 V				8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

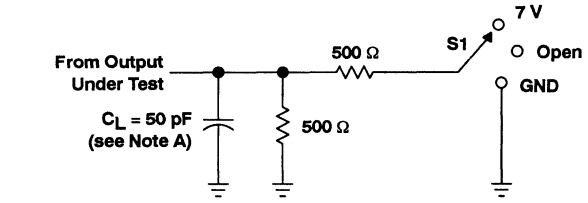
			MIN	MAX	UNIT
f_{clock}	Clock frequency			80	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		ns
		CLK low	4		
		CLK high	4		
t_{su}	Setup time	$\overline{CLR}$ inactive before CLK↑	2		ns
	Clock duty cycle		40%	60%	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			80			MHz
t_{PLH}	CLK	Any Y or Q	3		9	ns
t_{PHL}			3		9	
t_{PHL}	$\overline{CLR}$	Any Q	4		9	ns
t_{PZH}	$\overline{OE}$	Any Y or Q	2		7	ns
t_{PZL}			3		7	
t_{PHZ}	$\overline{OE}$	Any Y or Q	2		7	ns
t_{PLZ}			2		7	
$t_{sk(o)}$	CLK↑	Y↑			0.75	ns
		Q↑			0.9	
		Y↑ and Q↑			0.9	
t_r				0.9		ns
t_f				0.7		ns

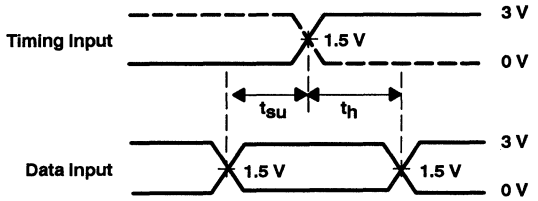
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

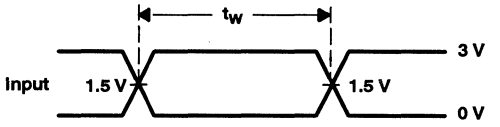


LOAD CIRCUIT

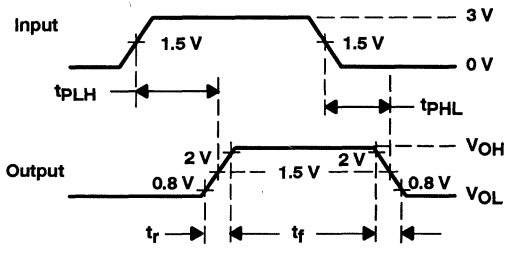
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



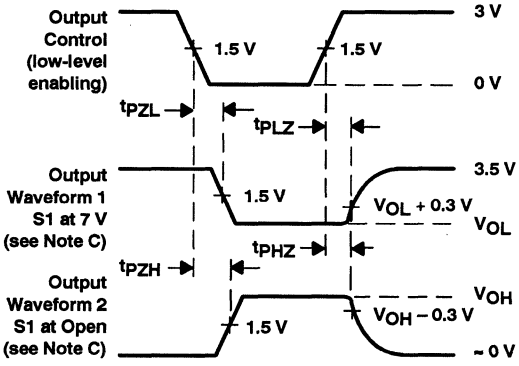
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

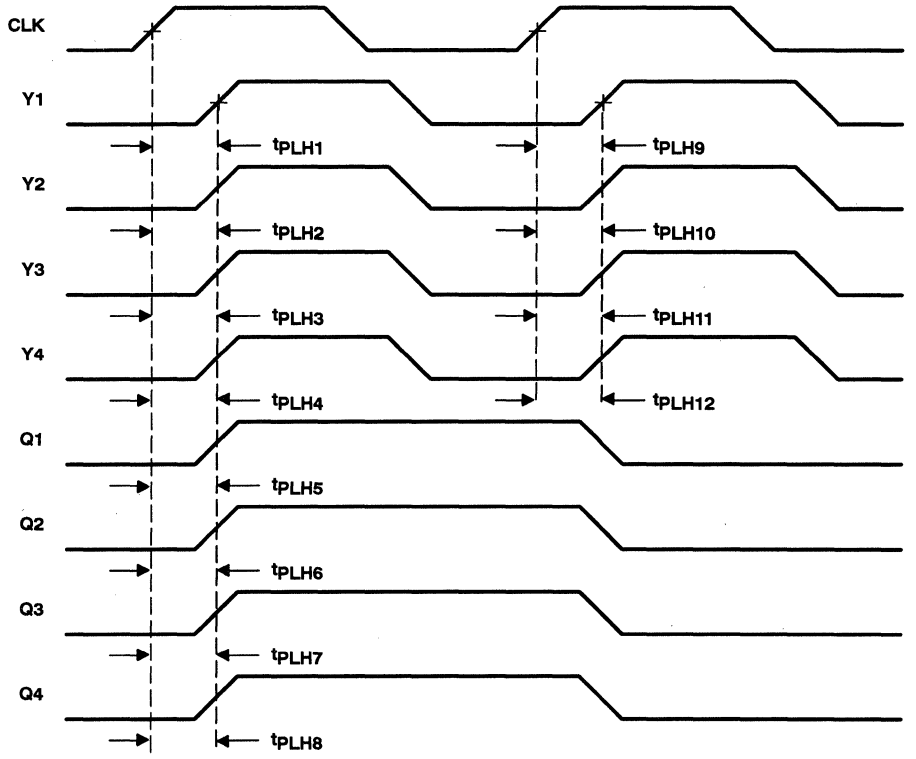


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4) or t_{PLHn} (n = 9, 10, 11, 12).

B. Output skew, $t_{sk(o)}$, from CLK↑ to Q↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8).

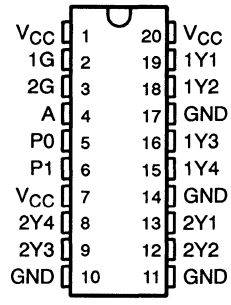
C. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑ and Q↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8).

Figure 2. Skew Waveforms and Calculations

SCAS332 – DECEMBER 1992 – REVISED MARCH 1994

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC340 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a high state regardless of the A input.

The CDC340's propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

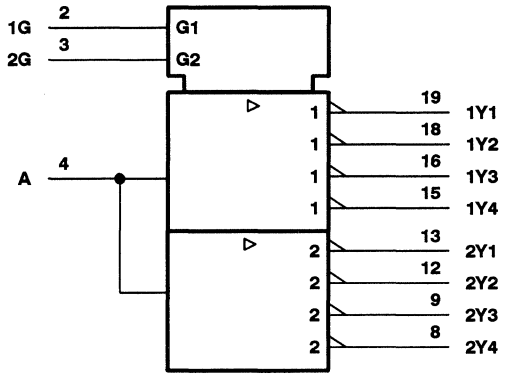
The CDC340 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	H	H
L	L	H	H	H
L	H	H	H	L
H	L	H	L	H
H	H	H	L	L

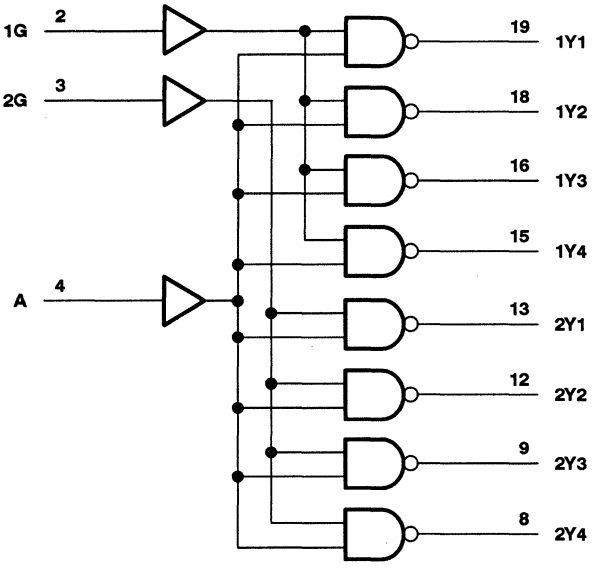
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP‡	MAX			
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2		−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		
	V_{CC} = 4.75 V,	I_{OH} = −48 mA		2			2		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA						0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1		±1	µA
I_O§	V_{CC} = 5.25 V,	V_O = 2.5 V		−50	−100	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2			3.5	mA
			Outputs low		24			33	
C_i	V_I = 2.5 V or 0.5 V				3				pF

‡ All typical values are at V_{CC} = 5 V.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

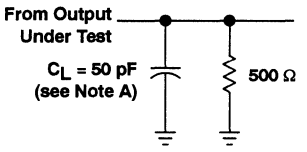
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.4		4.5	3	4.8	ns
t_{PHL}			3.2		4.3	2.8	4.7	
t_{PLH}	G	Y	2		3.8	2	4	ns
t_{PHL}			2		3.8	2	4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.6	ns
$t_{sk(p)}$				0.6	0.8		0.9	
$t_{sk(pr)}$					1.1		1.1	
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 3)

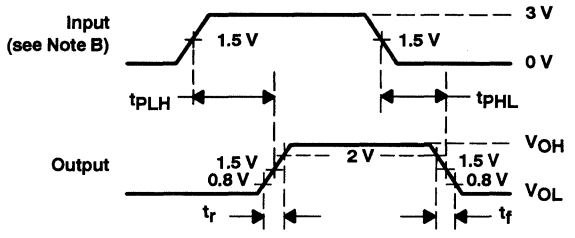
$Dt_{PLH(TA)}$†	Temperature drift of t_{PLH} from 0°C to 70°C	−53 ps/10°C
$Dt_{PHL(TA)}$†	Temperature drift of t_{PHL} from 0°C to 70°C	−58 ps/10°C
$Dt_{PLH(VCC)}$‡	V_{CC} drift of t_{PLH} from 4.75 V to 5.25 V	+43 ps/100 mV
$Dt_{PHL(VCC)}$‡	V_{CC} drift of t_{PHL} from 4.75 V to 5.25 V	−33 ps/100 mV

† Virtually independent of V_{CC}
‡ Virtually independent of temperature
NOTE 3: The data extracted is from a wide range of characterization material.

PARAMETER MEASUREMENT INFORMATION



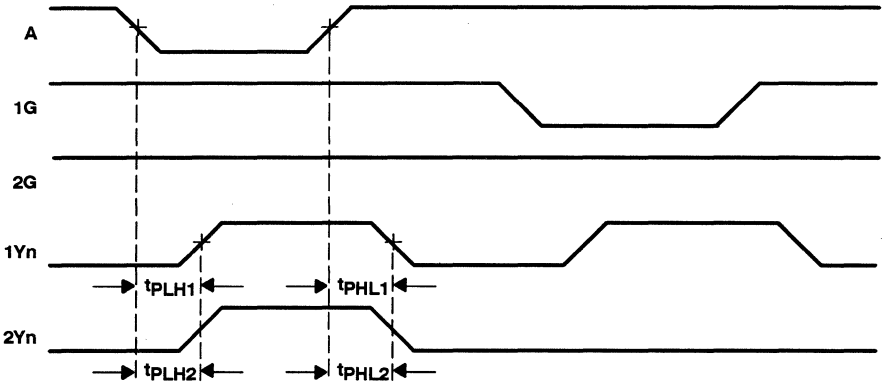
LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2)
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2)
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2).
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2) across multiple devices under identical operating conditions
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
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- **Distributes One Clock Input to Eight Outputs**
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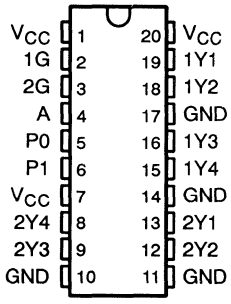
DB OR DW PACKAGE
(TOP VIEW)



description

The CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

The CDC341's propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

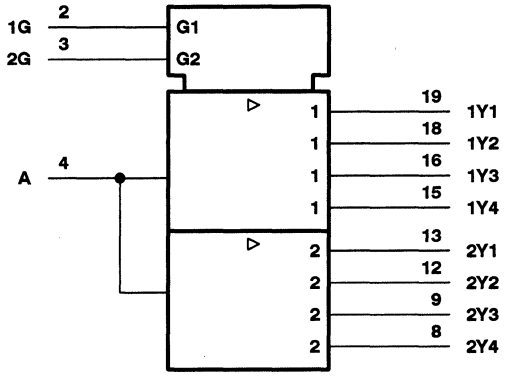
The CDC341 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H

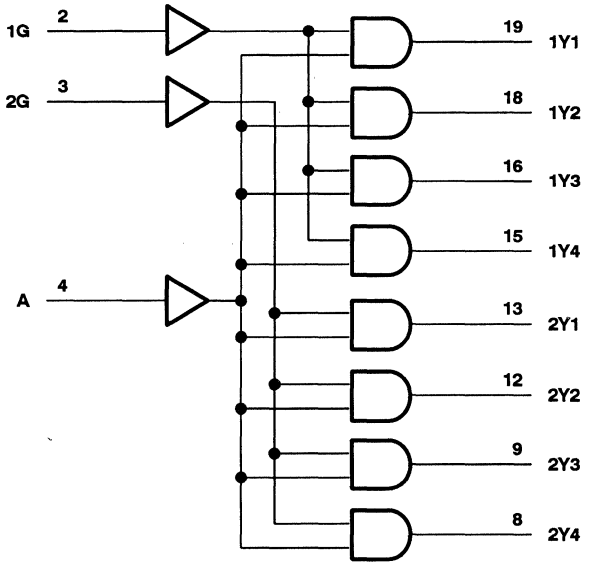
EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		−48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP‡	MAX			
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2		−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		
	V_{CC} = 4.75 V,	I_{OH} = −48 mA		2			2		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA						0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1		±1	µA
I_O§	V_{CC} = 5.25 V,	V_O = 2.5 V		−50	−100	−200	−50	−200	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2			3.5	mA
			Outputs low		24			33	
C_i	V_I = 2.5 V or 0.5 V				3				pF

‡ All typical values are at V_{CC} = 5 V.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

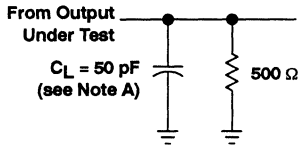
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.5		4.5	3.1	4.9	ns
t_{PHL}			3.5		4.3	3.1	4.9	
t_{PLH}	G	Y	2		3.8	2	4	ns
t_{PHL}			2		3.8	2	4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.6	ns
$t_{sk(p)}$				0.6	0.8		0.9	
$t_{sk(pr)}$					1		1	
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 3)

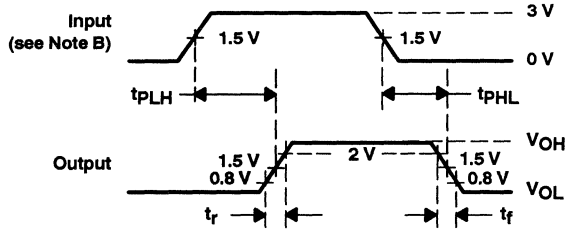
$Dt_{PLH(TA)}$†	Temperature drift of t_{PLH} from 0°C to 70°C	−41 ps/10°C
$Dt_{PHL(TA)}$†	Temperature drift of t_{PHL} from 0°C to 70°C	−52 ps/10°C
$Dt_{PLH(VCC)}$‡	V_{CC} drift of t_{PLH} from 4.75 V to 5.25 V	+28 ps/100 mV
$Dt_{PHL(VCC)}$‡§	V_{CC} drift of t_{PHL} from 4.75 V to 5.25 V	+20 ps/100 mV

† Virtually independent of V_{CC}
‡ Virtually independent of temperature
NOTE 3: The data extracted is from a wide range of characterization material.

PARAMETER MEASUREMENT INFORMATION



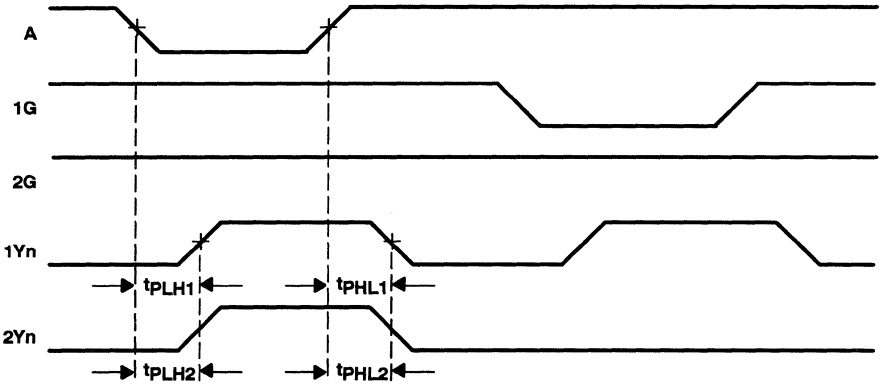
LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

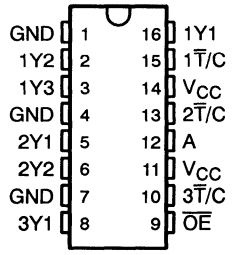


NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2)
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2)
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2).
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2) across multiple devices under identical operating conditions
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, (48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages**

D OR DB PACKAGE
(TOP VIEW)



description

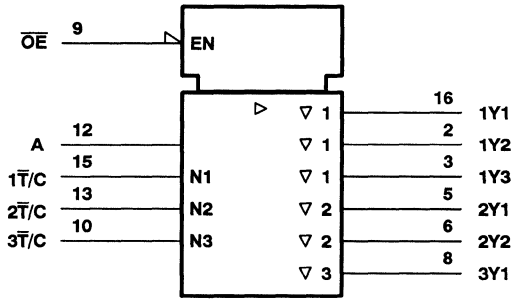
The CDC391 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control ($\overline{T}$/C) inputs, various combinations of true and complementary outputs can be obtained. The output-enable ($\overline{OE}$) input is provided to disable the outputs to a high-impedance state.

The CDC391 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	$\overline{T}$/C	A	Y
H	X	X	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L

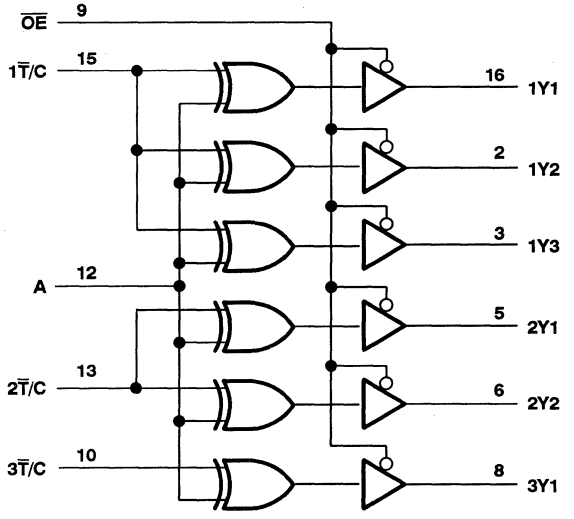
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 96 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1000 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−48	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

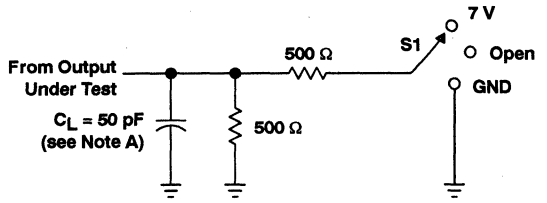
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 48 mA		2			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA				0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	μA
I_{OZ}	V_{CC} = 5.25 V,	V_O = V_{CC} or GND				±50	μA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–15		–100	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			10	mA
			Outputs low			40	
			Outputs disabled			10	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = 2.5 V or 0.5 V				5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

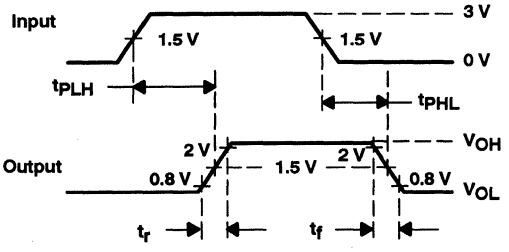
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Any Y	1.5	5	ns
t_{PHL}			1.5	5	
t_{PLH}	$\overline{T}/C$	Any Y	1.5	5	ns
t_{PHL}			1.5	5	
t_{PZH}	$\overline{OE}$	Any Y	1.5	5	ns
t_{PZL}			3	7	
t_{PHZ}	$\overline{OE}$	Any Y		5	ns
t_{PLZ}				5	
$t_{sk(o)}$	A	Any Y (same phase)		0.5	ns
		Any Y (any phase)		1	
$t_{sk(p)}$	A	Any Y		1	ns
t_r				1.5	ns
t_f				1.5	ns

PARAMETER MEASUREMENT INFORMATION

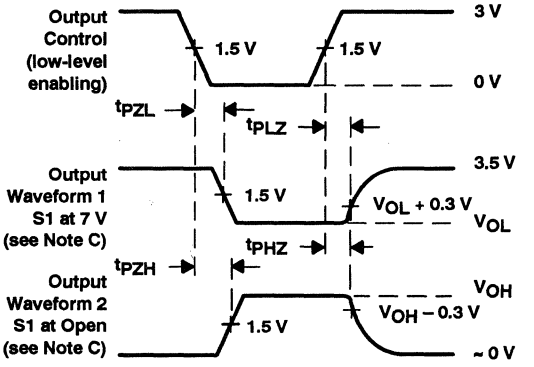


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

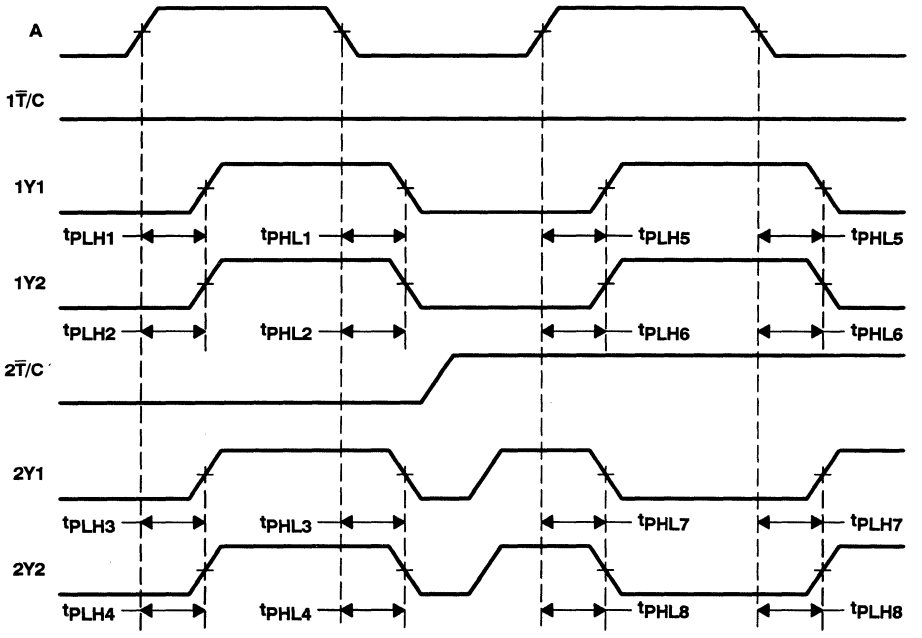


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



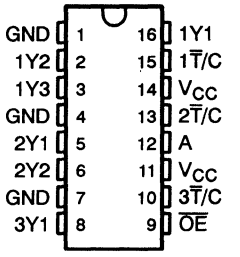
NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Distributes One Clock Input to Six Clock Outputs**
- **Polarity Control Selects True or Complementary Outputs**
- **Distributed V_{CC} and GND Pins Reduce Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages**

D OR DB PACKAGE
(TOP VIEW)



description

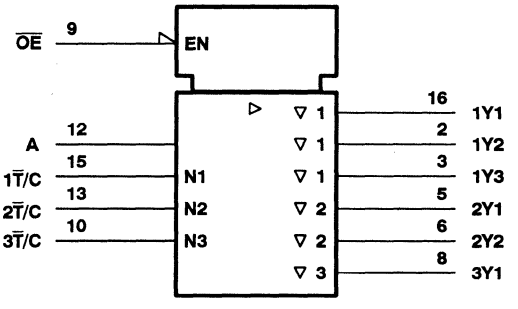
The CDC392 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control ($\overline{T}$/C) inputs, various combinations of true and complementary outputs can be obtained. The output-enable ($\overline{OE}$) input is provided to disable the outputs to a high-impedance state.

The CDC392 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	$\overline{T}$/C	A	Y
H	X	X	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L

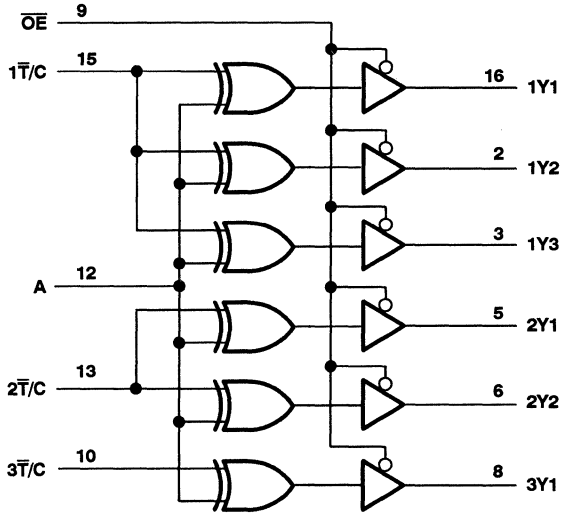
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} (V_I < 0) ..... −18 mA
Output clamp current, I_{OK} (V_O < 0) ..... −50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1000 mW
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−32	mA
I_{OL}	Low-level output current			32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			90	MHz
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

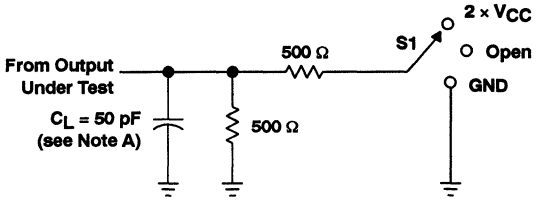
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 32 mA		3.85			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA				0.55	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1	μA
I_{OZ}	V_{CC} = 5.25 V,	V_O = V_{CC} or GND				±50	μA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			10	mA
			Outputs low			40	
			Outputs disabled			10	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = V_{CC} or GND				7		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

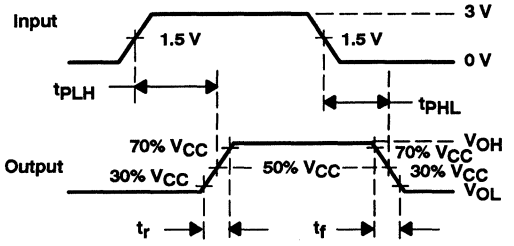
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	A	Any Y	2		6.5	ns
t_{PHL}			1.5		5	
t_{PLH}	$\overline{T}$/C	Any Y	1.5		5	ns
t_{PHL}			1.5		5	
t_{PZH}	$\overline{OE}$	Any Y	1.5		6	ns
t_{PZL}			3		8	
t_{PHZ}	$\overline{OE}$	Any Y	1.5		5	ns
t_{PLZ}			1.5		5	
$t_{sk(o)}$	A	Any Y (same phase)			0.6	ns
		Any Y (any phase)			2.2	
t_r				1.4		ns
t_f				0.83		ns

PARAMETER MEASUREMENT INFORMATION

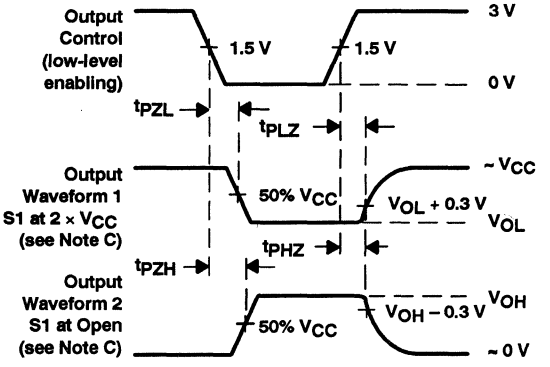


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

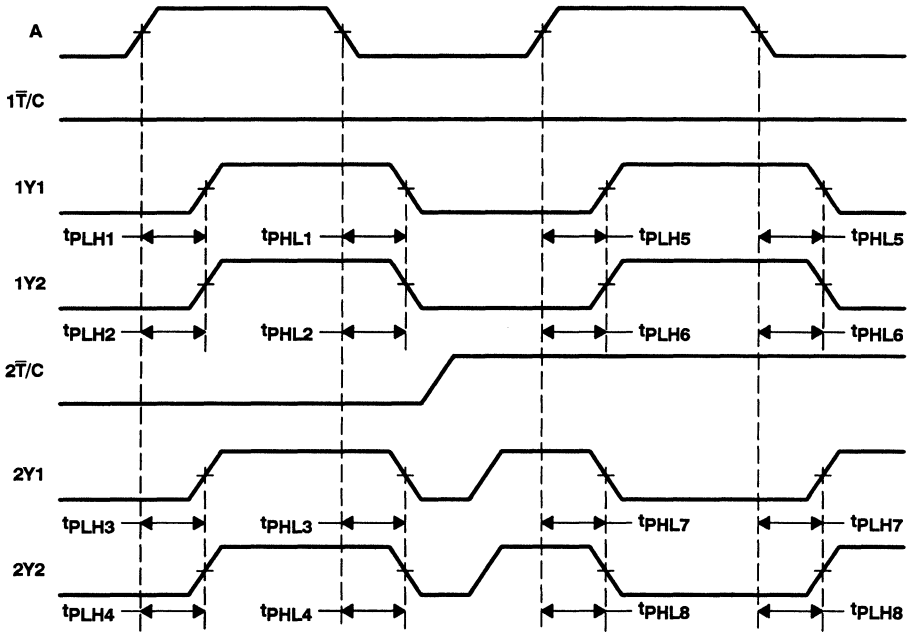


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



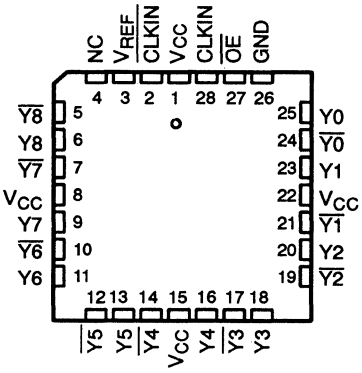
NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6)
- The difference between the fastest and slowest of t_{PLH} from A↓ to any Y (e.g., t_{PLHn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↑ to any Y (e.g., t_{PHLn}, n = 7 to 8)

B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T}$/C) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from A↑ to any Y or t_{PHL} from A↑ to any Y (e.g., t_{PLHn}, n = 1 to 4; or t_{PLHn}, n = 5 to 6, and t_{PHLn}, n = 7 to 8)
- The difference between the fastest and slowest of t_{PHL} from A↓ to any Y or t_{PLH} from A↓ to any Y (e.g., t_{PHLn}, n = 1 to 4; or t_{PHLn}, n = 5 to 6, and t_{PLHn}, n = 7 to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Differential Low Voltage Pseudo ECL (LVPECL)-Compatible Inputs and Outputs**
- **Distributes Differential Clock Inputs to Nine Differential Clock Outputs**
- **Output Reference Voltage, V_{REF}, Allows Distribution From a Single-Ended Clock Input**
- **Single-Ended LVPECL-Compatible Output Enable**
- **Packaged in 28-Pin Plastic Chip Carrier**

FN PACKAGE
(TOP VIEW)



description

The differential LVPECL clock–driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN, $\overline{\text{CLKIN}}$) to nine pairs of differential clock (Y, $\overline{\text{Y}}$) outputs with minimum skew for clock distribution. It is specifically designed for driving 50-Ω transmission lines.

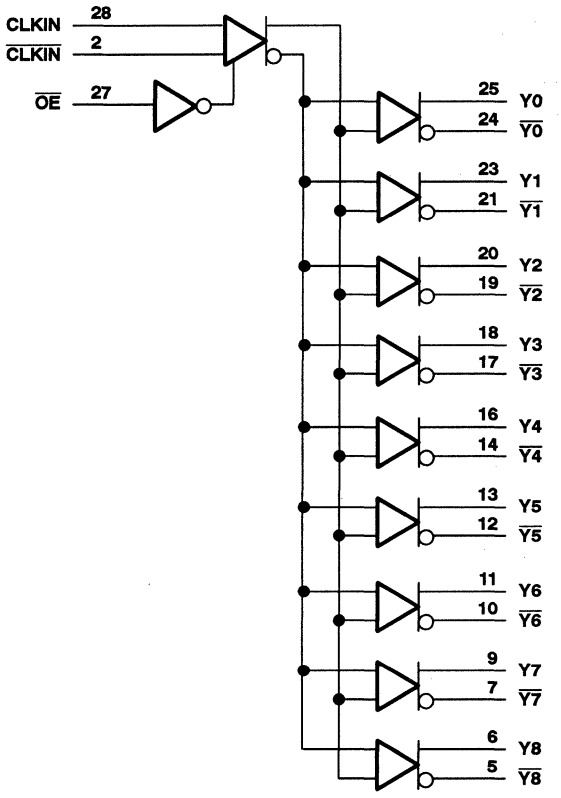
When the output-enable ($\overline{\text{OE}}$) input is in the low state, the nine differential outputs switch at the same frequency as the differential clock inputs. When $\overline{\text{OE}}$ is in the high state, the nine differential outputs will be in static states (Y outputs will be in the low state, $\overline{\text{Y}}$ outputs will be in the high state).

The V_{REF} output can be strapped to the $\overline{\text{CLKIN}}$ input for a single-ended CLKIN input.

The CDC111 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−18 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	−18 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	−50 mA
Continuous current through V_{CC} or GND	± 70 mA
Maximum power dissipation at T_A = 55°C (in still air)	525 mW
Maximum operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.165	V_{CC}–0.88	V
		V_{CC} = 3.3 V	2.135	2.420	
V_{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.81	V_{CC}–1.475	V
		V_{CC} = 3.3 V	1.490	1.825	
T_A	Operating free-air temperature		0	70	°C

NOTE 2: $V_{CC} = V_{CCO}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

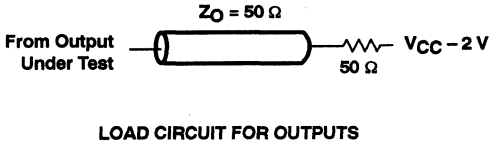
PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V_{REF}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.38	V_{CC}–1.26	V
	V_{CC} = 3.3 V		1.925	2.075	
V_{OH}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.025	V_{CC}–0.88	V
	V_{CC} = 3.3 V		2.275	2.42	
V_{OL}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.81	V_{CC}–1.62	V
	V_{CC} = 3.3 V		1.49	1.68	
I_I	V_I = 2.4 V,	V_{CC} = 3 .6 V		150	µA
I_{CC}	I_O = 0,	V_{CC} = 3 .6 V		70	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figures 1 and 2)

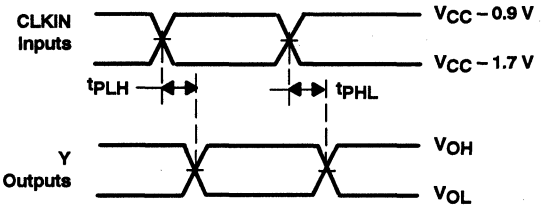
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	CLKIN, $\overline{CLKIN}$	Y, $\overline{Y}$			ps
t_{PHL}					
t_{PLH}	$\overline{OE}$	Y or $\overline{Y}$			ps
t_{PHL}		Y or $\overline{Y}$			
$t_{sk(o)}$		Y, $\overline{Y}$		50	ps
$t_{sk(pr)}$		Y, $\overline{Y}$		100	ps

PRODUCT PREVIEW

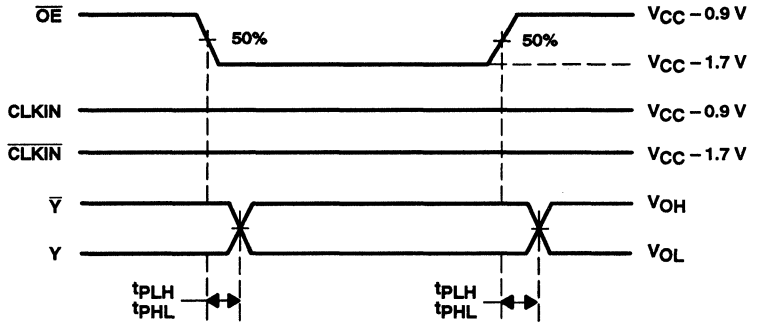
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



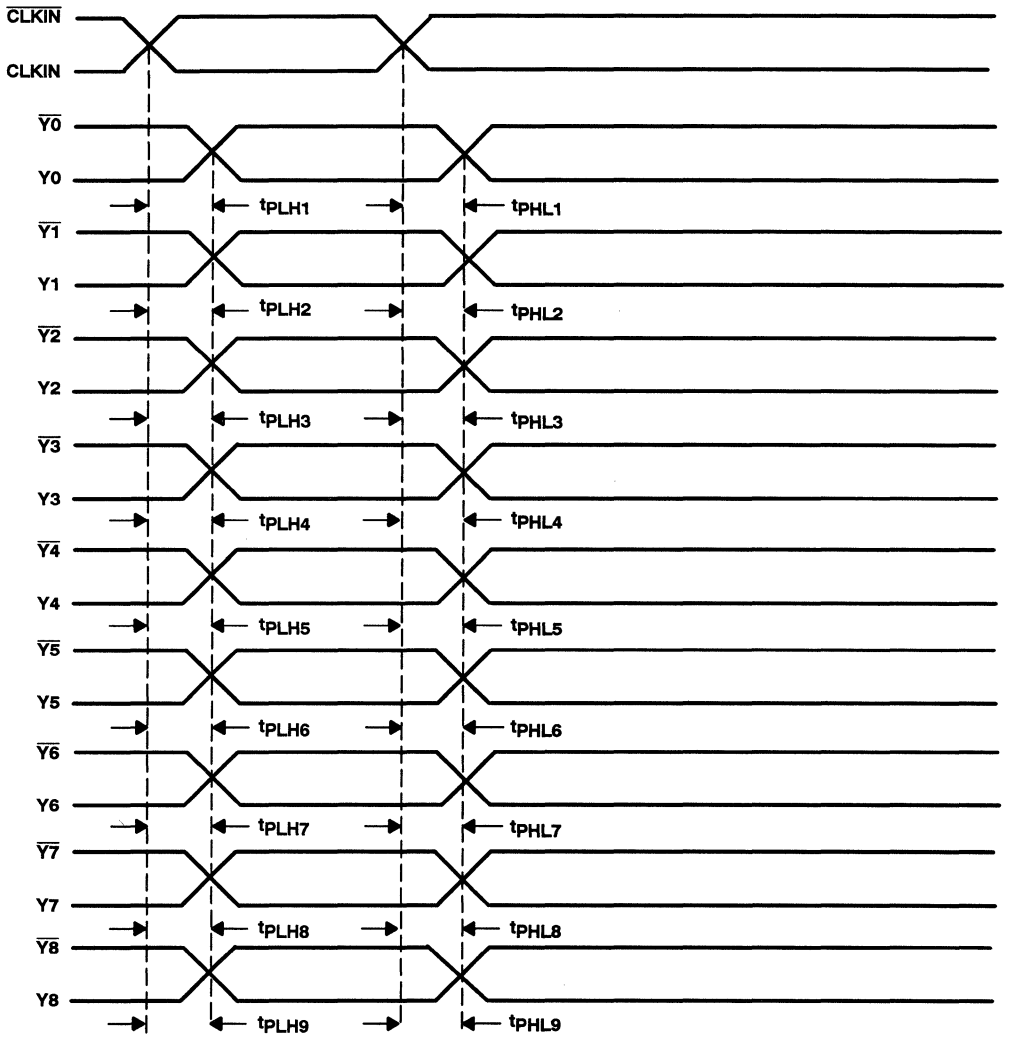
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 45 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9)

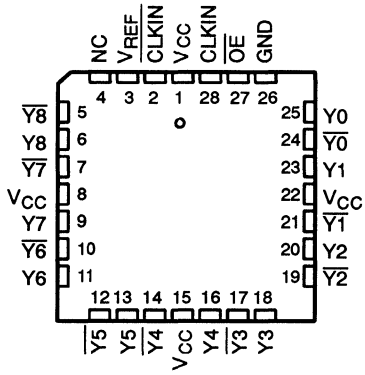
B. Process skew, $t_{sk(pr)}$, is calculated as:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9) across multiple devices

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PRODUCT PREVIEW

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Differential Low Voltage Pseudo ECL (LVPECL)-Compatible Inputs and Outputs**
- **Distributes Differential Clock Inputs to Nine Differential Clock Outputs**
- **Output Reference Voltage, V_{REF}, Allows Distribution From a Single-Ended Clock Input**
- **LVTTL-Compatible Output Enable**
- **Packaged in 28-Pin Plastic Chip Carrier**

FN PACKAGE
(TOP VIEW)



description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN, $\overline{\text{CLKIN}}$) to nine pairs of differential clock (Y, $\overline{\text{Y}}$) outputs with minimum skew for clock distribution. It is specifically designed for driving 50-Ω transmission lines.

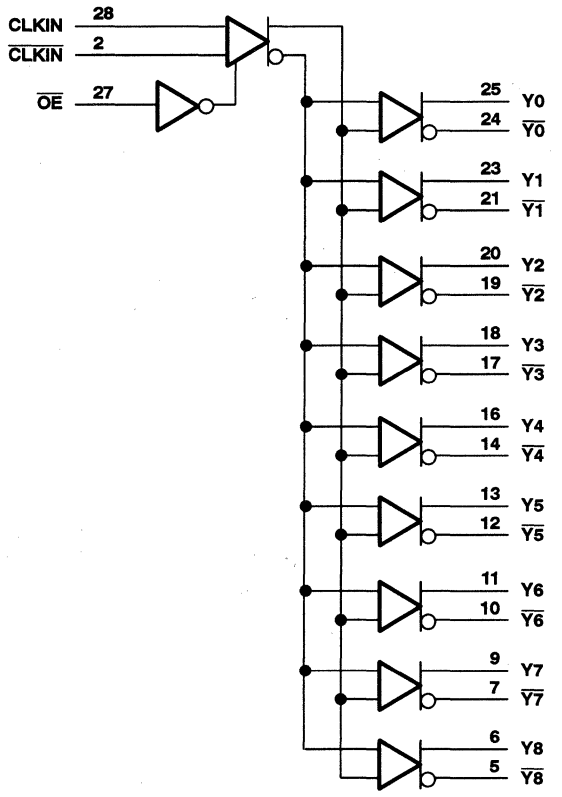
When the output-enable ($\overline{\text{OE}}$) input is in the low state, the nine differential outputs switch at the same frequency as the differential clock inputs. When $\overline{\text{OE}}$ is in the high state, the nine differential outputs will be in static states (Y outputs will be in the low state, $\overline{\text{Y}}$ outputs will be in the high state).

The V_{REF} output can be strapped to the $\overline{\text{CLKIN}}$ input for a single-ended CLKIN input.

The CDC112 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−18 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	−18 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	−50 mA
Continuous current through V_{CC} or GND	± 70 mA
Maximum power dissipation at T_A = 55°C (in still air)	525 mW
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage, (CLKIN, $\overline{CLKIN}$ only)	V_{CC} = 3 V to 3.6 V	V_{CC}–1.165	V_{CC}–0.88	V
		V_{CC} = 3.3 V	2.135	2.42	
V_{IL}	Low-level input voltage, (CLKIN, $\overline{CLKIN}$ only)	V_{CC} = 3 V to 3.6 V	V_{CC}–1.81	V_{CC}–1.475	V
		V_{CC} = 3.3 V	1.49	1.825	
V_{IH}	High-level input voltage, ($\overline{OE}$ only)		2		V
V_{IL}	Low-level input voltage, ($\overline{OE}$ only)			0.8	V
T_A	Operating free-air temperature		0	70	°C

NOTE 2: $V_{CC} = V_{CCO}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

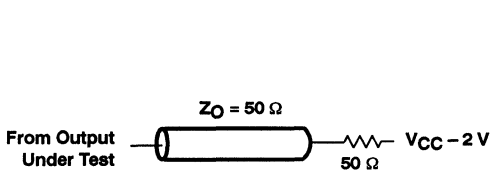
PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.025	V_{CC}–0.88	V
	V_{CC} = 3.3 V		2.275	2.42	
V_{OL}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.81	V_{CC}–1.62	V
	V_{CC} = 3.3 V		1.49	1.68	
V_{REF}	V_{CC} = 3 V to 3.6 V		V_{CC}–1.38	V_{CC}–1.26	V
	V_{CC} = 3.3 V		1.925	2.075	
I_I	V_I = 2.4 V,	V_{CC} = 3 .6 V		150	µA
I_{CC}	I_O = 0,	V_{CC} = 3 .6 V		70	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figures 1 and 2)

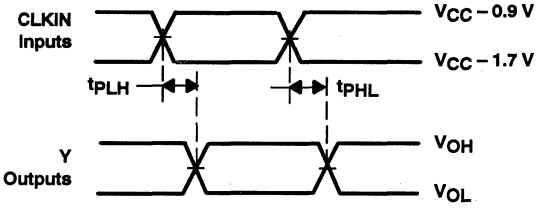
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	CLKIN, $\overline{CLKIN}$	Y, $\overline{Y}$			ps
t_{PHL}					
t_{PLH}	$\overline{OE}$	Y or $\overline{Y}$			ps
t_{PHL}		Y or $\overline{Y}$			
$t_{sk(o)}$		Y, $\overline{Y}$		50	ps
$t_{sk(pr)}$		Y, $\overline{Y}$		100	ps

PRODUCT PREVIEW

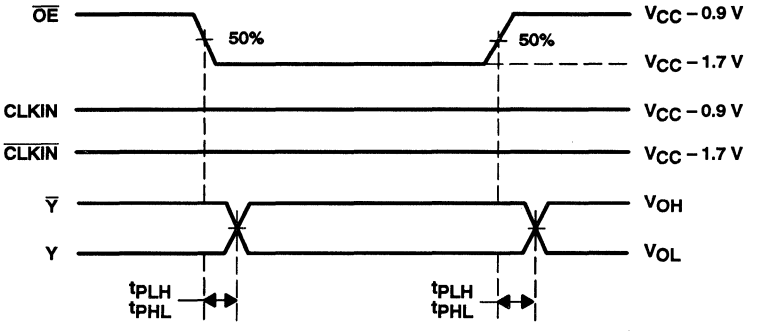
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



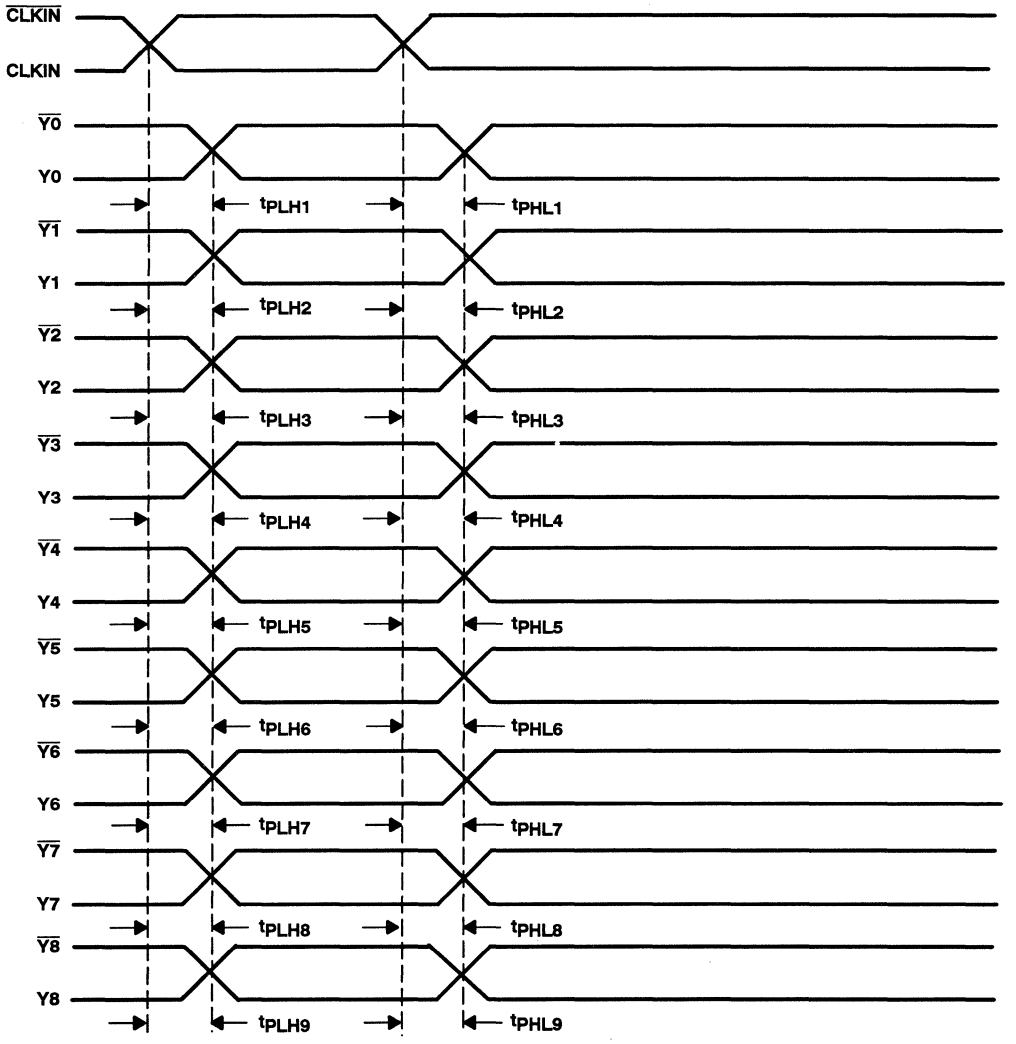
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 45 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9)

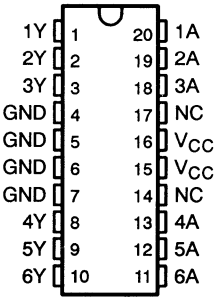
B. Process skew, $t_{sk(pr)}$, is calculated as as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9) across multiple devices

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PRODUCT PREVIEW

- **Replaces 74AC11203**
- **Low-Skew Propagation Delay Specifications for Clock Driver Applications**
- **Operates at 3.3-V V_{CC}**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

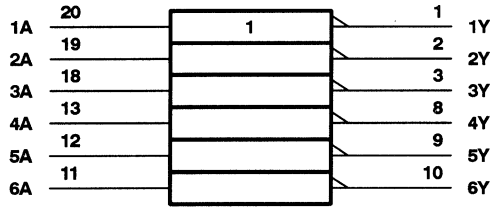
The CDC203 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC203 is characterized for operation from 25°C to 70°C.

FUNCTION TABLE

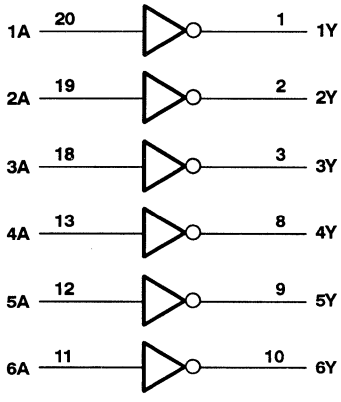
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 3.6 V	2.5			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 3.6 V			1.1	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−12	mA
		V_{CC} = 3.6 V			−12	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 3.6 V			12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				40	MHz
T_A	Operating free-air temperature		25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

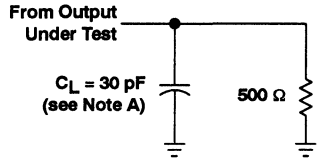
PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA	3 V	2.9			2.9		V
		3.6 V	3.5			3.5		
	I_{OH} = − 12 mA	3 V	2.58			2.48		
		3.6 V	3.18			3.08		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		3.6 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
		3.6 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	3.6 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			4		40	μA
C_i	V_I = V_{CC} or GND	3.3 V		4				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Note 2 and Figures 1 and 2)

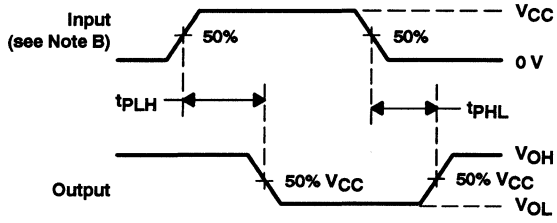
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Y	3.5	6.1	ns
t_{PHL}			3.5	6.1	
$t_{sk(o)}$	A	Y		0.7	ns

NOTE 2: All specifications are valid only for all outputs switching simultaneously and in phase.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

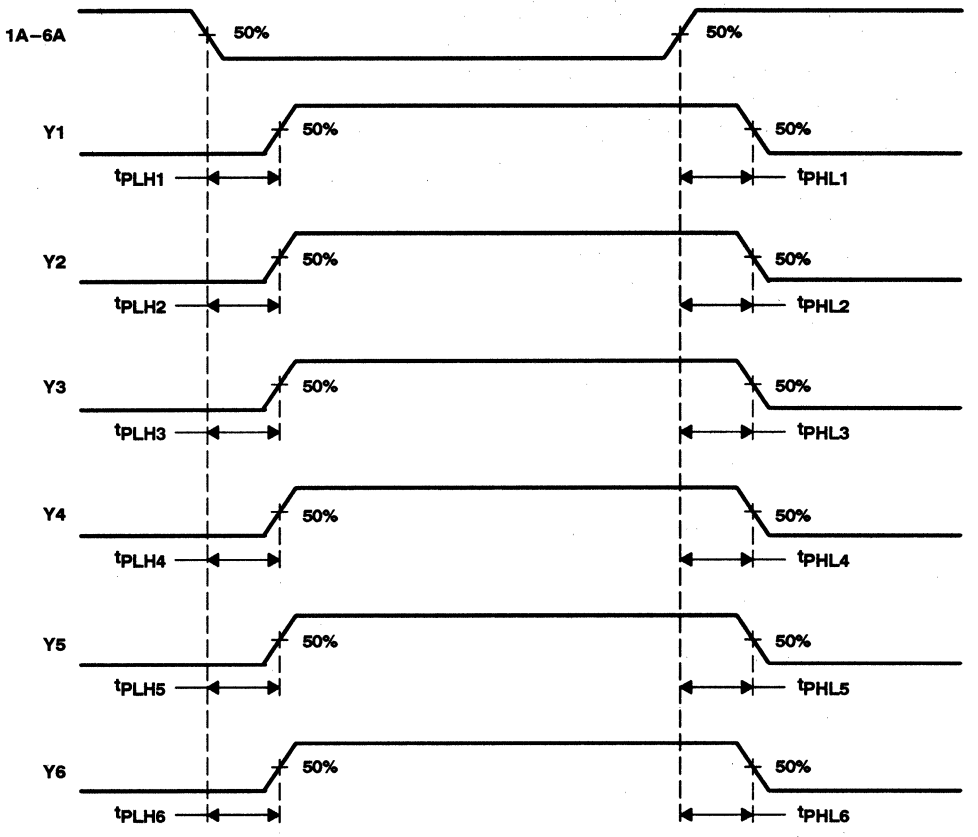


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

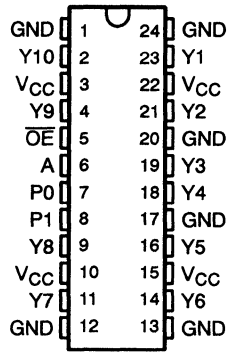


NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 6)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 6)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3 V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Ten Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BICMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input is provided to disable the outputs to a high-impedance state.

The CDC351 propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part to part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC351 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	Yn
L	H	Z
H	H	Z
L	L	L
H	L	H

PRODUCT PREVIEW

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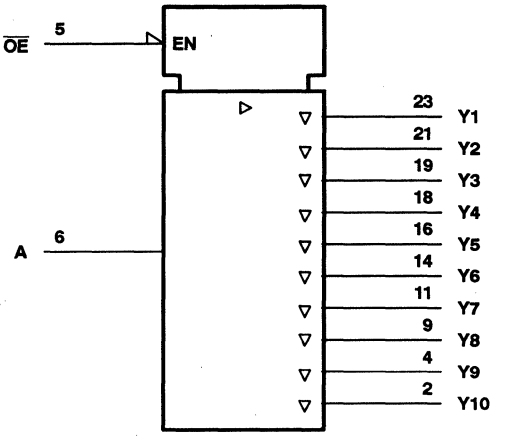
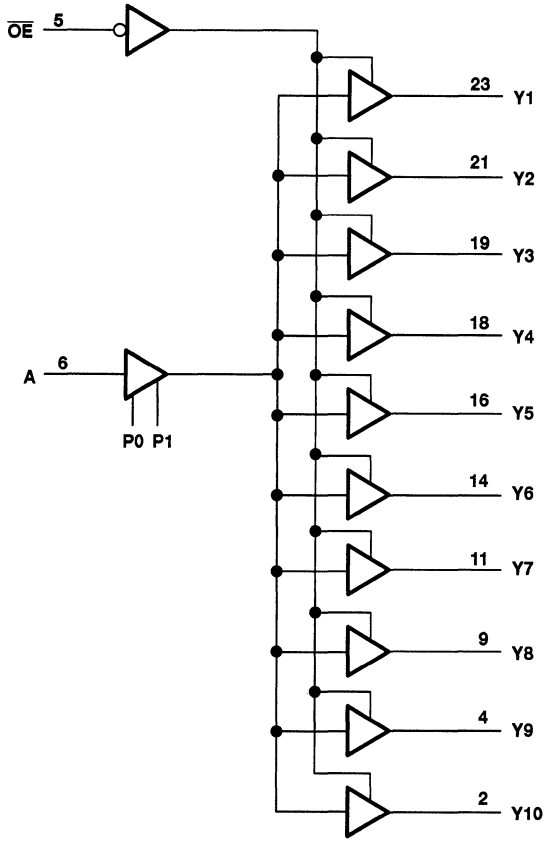
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 3.6 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_I < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
f_{clock}	Input clock frequency		100	MHz
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	MIN	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 32 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 32 mA					0.5	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1		±1	µA
I_O†	V_{CC} = 3.6 V,	V_O = 2.5 V						mA
I_{OZ}	V_{CC} = 3.6 V	V_O = 3 V or 0						µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					mA
			Outputs low					
			Outputs disabled					
C_i	V_I = V_{CC} or GND							pF
C_o	V_O = V_{CC} or GND							pF

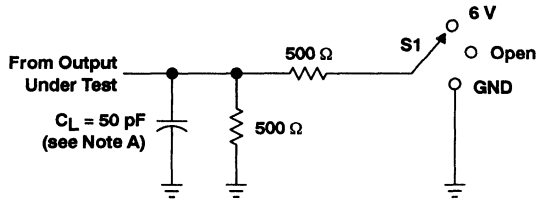
† Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V, T_A = 25°C MIN	TYP	MAX	V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C MIN	MAX	UNIT
t_{PLH}	A	Y						ns
t_{PHL}								
t_{PZH}	$\overline{OE}$	Y						ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y						ns
t_{PLZ}								
$t_{sk(o)}$	A	Y		0.3	0.5		0.5	ns
$t_{sk(p)}$	A	Y		0.6	0.8		0.8	ns
$t_{sk(pr)}$	A	Y			1		1	ns
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

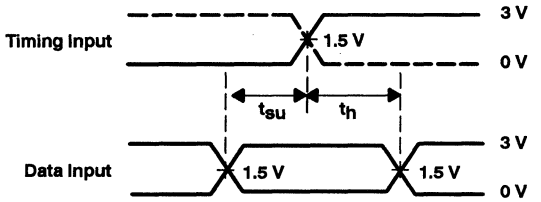
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

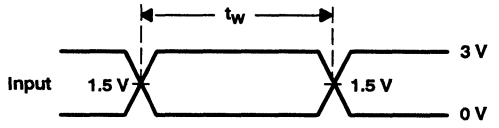


LOAD CIRCUIT

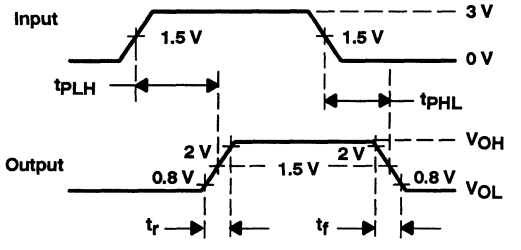
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



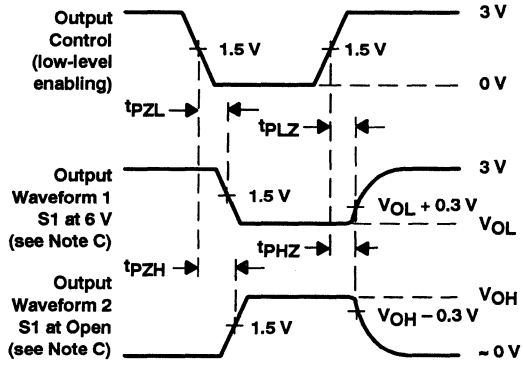
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



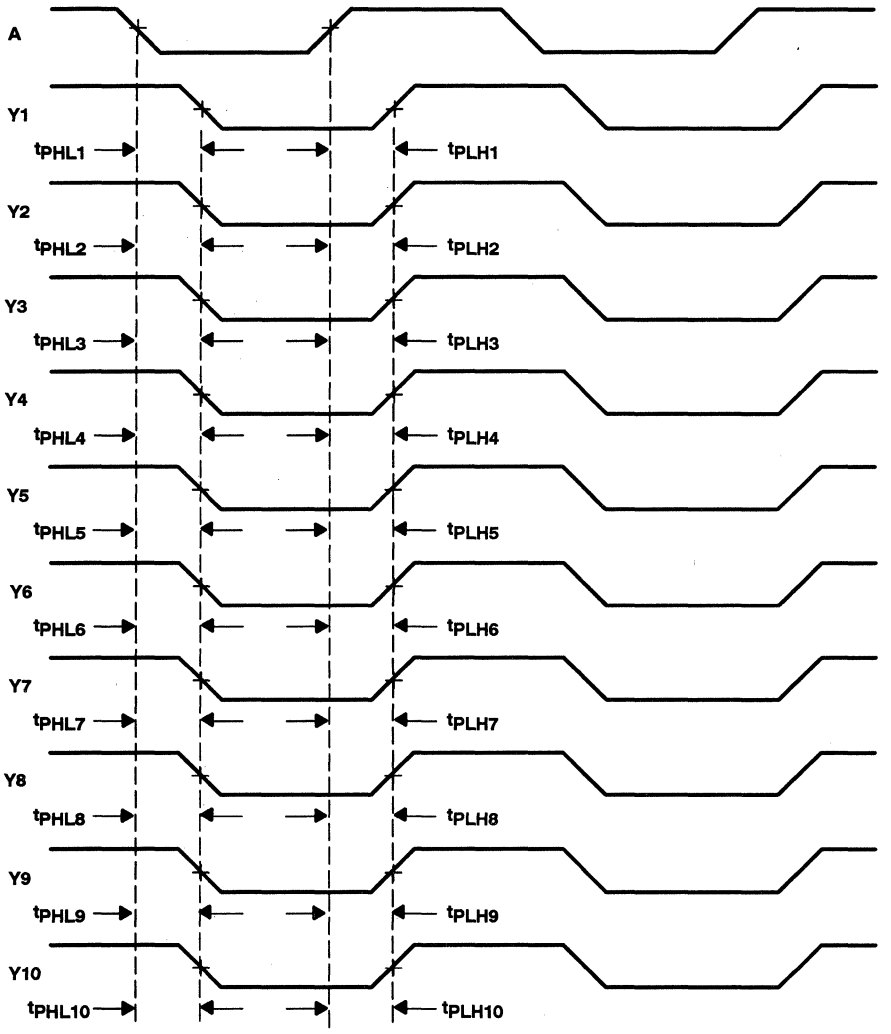
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

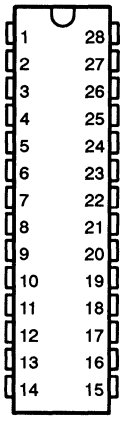
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Up to Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Pin (FBIN) is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **Edge-Triggered Clear for Half-Frequency Outputs**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic 28-Pin Shrink Small Outline Package (SSOP)**

DL PACKAGE
(TOP VIEW)



description

The CDC536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with syncronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC536 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to the FBIN input for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select input (SEL) configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) and clear ($\overline{CLR}$) inputs are also provided for output control and synchronization. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. The $\overline{CLR}$ input is negative edge triggered and is provided to allow phase synchronization of the outputs operating at half frequency on multiple CDC536 devices. The TEST input is used for factory testing of the device and is not intended for customer use. The TEST pin should be strapped to GND.

Unlike many products containing PLLs, the CDC536 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

PRODUCT PREVIEW

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description (continued)

Because it is based on PLL circuitry, the CDC536 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon phase reset of the half-frequency outputs and upon enable of all outputs; therefore, stabilization is also required when switching from the clear or high-impedance state to the active state.

The CDC536 is characterized for operation from 0°C to 70°C.

detailed decription of output configurations

The voltage-controlled oscillator (VCO) used in the CDC536 phase-lock loop has a frequency range of 100 MHz to 200 MHz, twice the operating frequency of the CDC536 outputs. A two–bit counter is used to divide the VCO frequency. The two outputs of this counter (divide-by-two and divide-by-four) operate at one-half and one-fourth the VCO frequency, respectively, at a duty cycle of 50%. The SEL input selects which of these two counter outputs is buffered to each bank of device outputs.

One device output must be externally wired to the feedback input (FBIN) to complete the phase-lock loop. The VCO operates such that the frequency and phase of this output matches that of the CLKIN signal. In the case that a divide-by-two output is wired to FBIN, the VCO must operate at twice the CLKIN frequency resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a divide-by-four output is wired to FBIN, the device outputs operate at twice the frequency or the same frequency as the CLKIN input.

output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to the FBIN input. The input frequency range for the CLKIN input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as the CLKIN input.

Table 1. Output Configuration A

INPUTS	OUTPUTS	
SEL	1/2x FREQUENCY	1x FREQUENCY
L	None	All
H	1Yn	2Yn

NOTE: n = 1, 2, 3

output configuration B

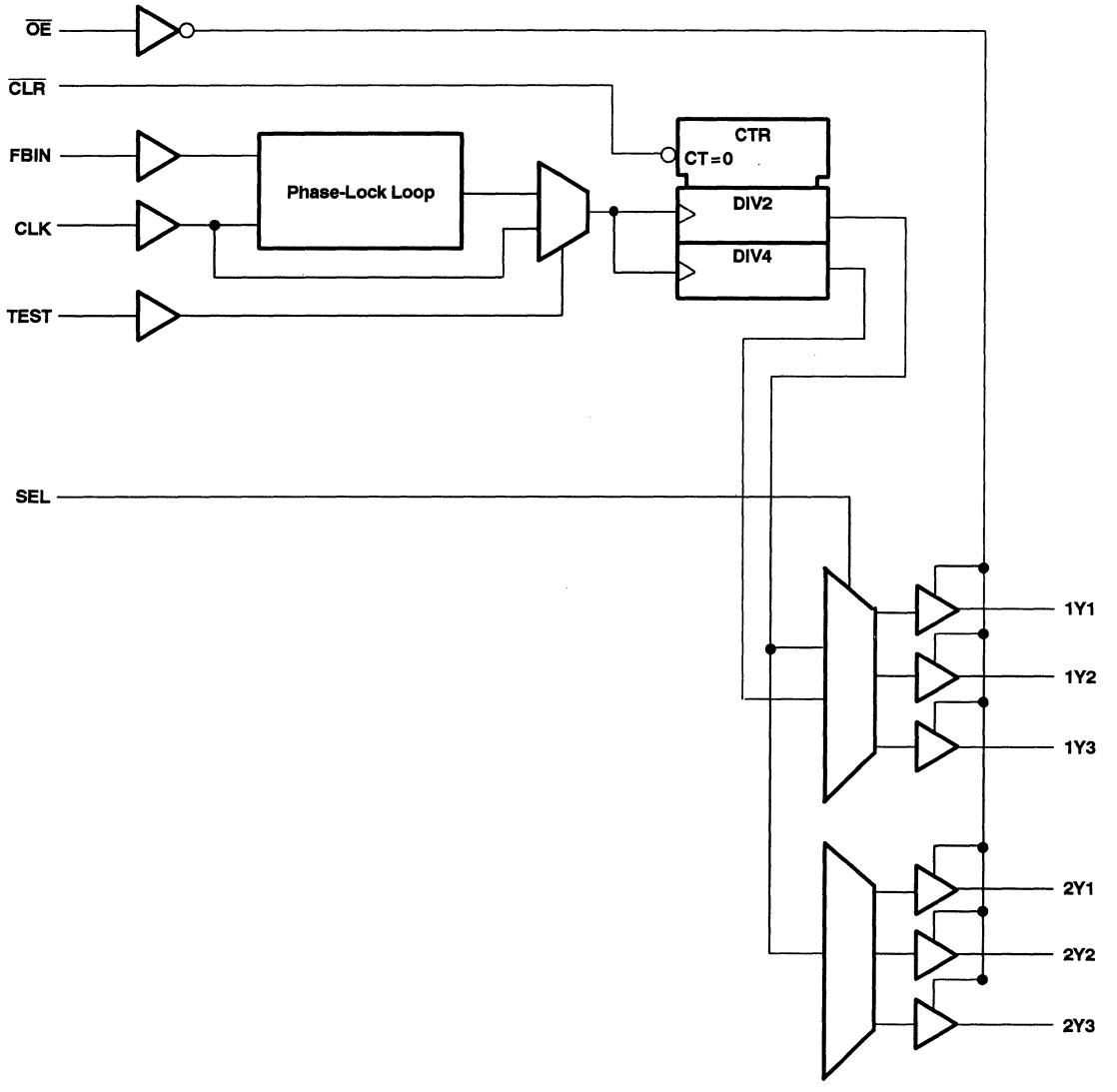
Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to the FBIN input. The input frequency range for the CLKIN input is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of the CLKIN input.

Table 2. Output Configuration B

INPUTS	OUTPUTS	
SEL	1x FREQUENCY	2x FREQUENCY
L	1Yn	2Yn
H	All	None

NOTE: n = 1, 2, 3

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	TBD	I	Clock input. CLKIN provides the clock signal to be distributed by the CDC536 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	TBD	I	Clear. $\overline{CLR}$ is used to reset the Y outputs configured as half-frequency outputs to a known phase. $\overline{CLR}$ is useful to ensure that the half-frequency output signals of multiple CDC536 circuits are all in the same phase. The $\overline{CLR}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{CLR}$, the flip-flop that divides the CLKIN signal is asynchronously cleared to a low level. Following the required stabilization time, half-frequency output signals for all CDC536 units that receive the same CLKIN and $\overline{CLR}$ signals have the same phase.
FBIN	TBD	I	Feedback input. FBIN provides the feedback signal to the internal PLL. The FBIN terminal must be hard wired to one of the six clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and differential CLKIN inputs.
$\overline{OE}$	TBD	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL	TBD	I	Counter output select. SEL selects the output configuration (see Tables 1 and 2).
TEST	TBD	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be grounded for normal operation.
1Y1–1Y3	TBD	O	Four-bit output ports. These outputs are configured by the select input (SEL) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select input. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, the $\overline{CLR}$ input is provided to allow the outputs of multiple CDC536 circuits operating at half-frequency to be reset to the same phase.
2Y1–2Y3	TBD	O	Four-bit output ports. These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the CLKIN signal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .. −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = − 32 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	mA
			Outputs low		1	
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND					pF
C_o	V_O = V_{CC} or GND					pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	When VCO is operating at four times the CLKIN frequency	25	50	MHz
		When VCO is operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
t_w	Pulse duration	$\overline{CLR}$ low			ns
	Stabilization time†	After SEL		50	µs
		After $\overline{CLR}\downarrow$		50	
		After $\overline{OE}\downarrow$		50	
		After power up		50	

† Time required for the integrated phase-lock loop circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

NOTE 3: Preliminary specifications based on SPICE analysis.

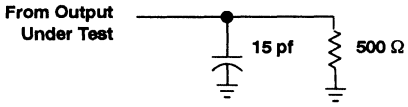
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
$t_{phase\ error}$‡	CLKIN↑	Y		±500	ps
$t_{sk(o)}$ (see Figure 3)	CLKIN	Y		0.5	ns
$t_{sk(pr)}$	CLKIN	Y		1	ns
t_{jitter} (RMS)	CLKIN↑	Y		25	ps
Duty cycle		Y	45%	55%	
t_r				1.4	ns
t_f				1.4	ns

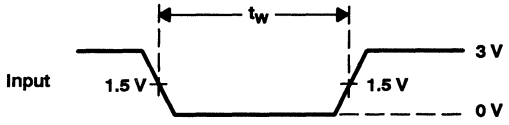
‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the feedback input FBIN.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

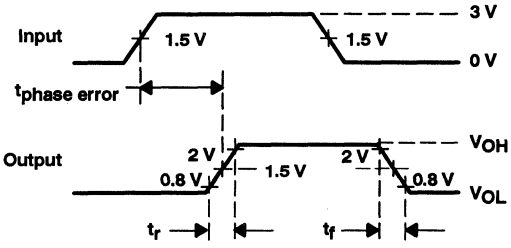
PARAMETER MEASUREMENT INFORMATION



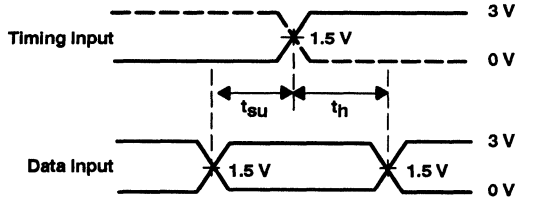
LOAD CIRCUIT FOR OUTPUTS



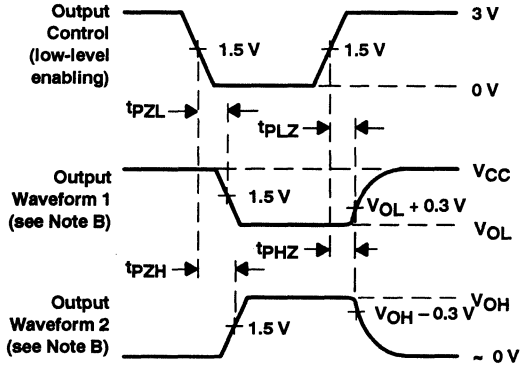
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



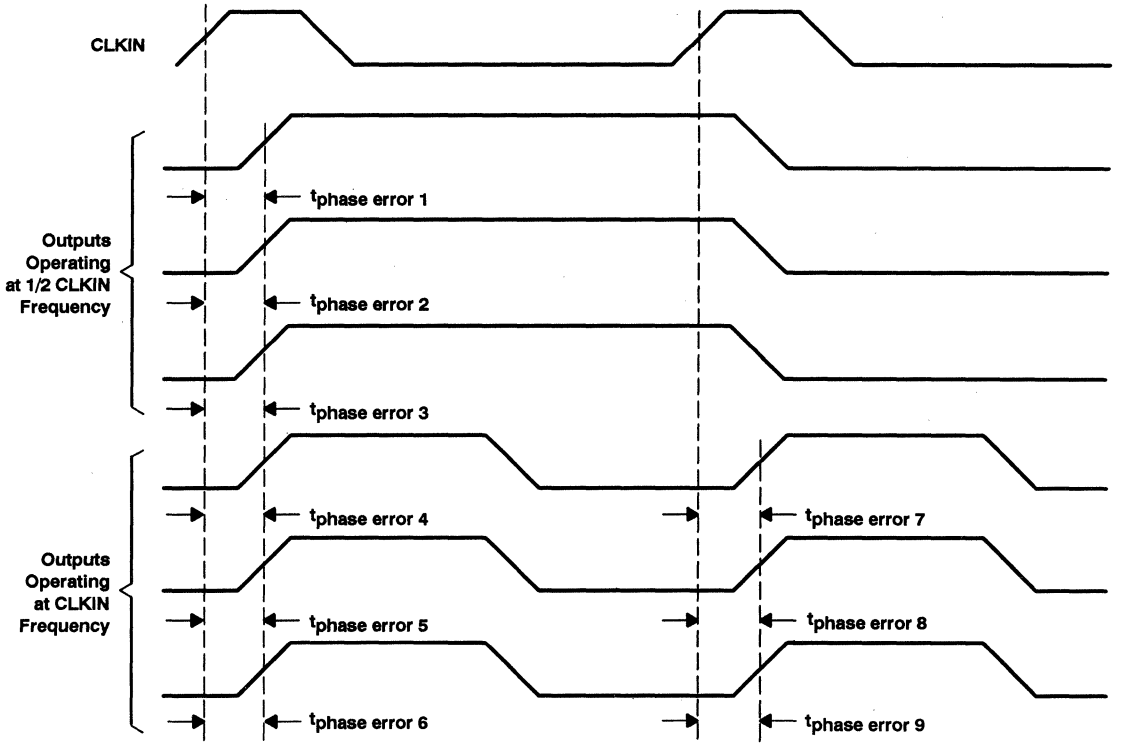
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

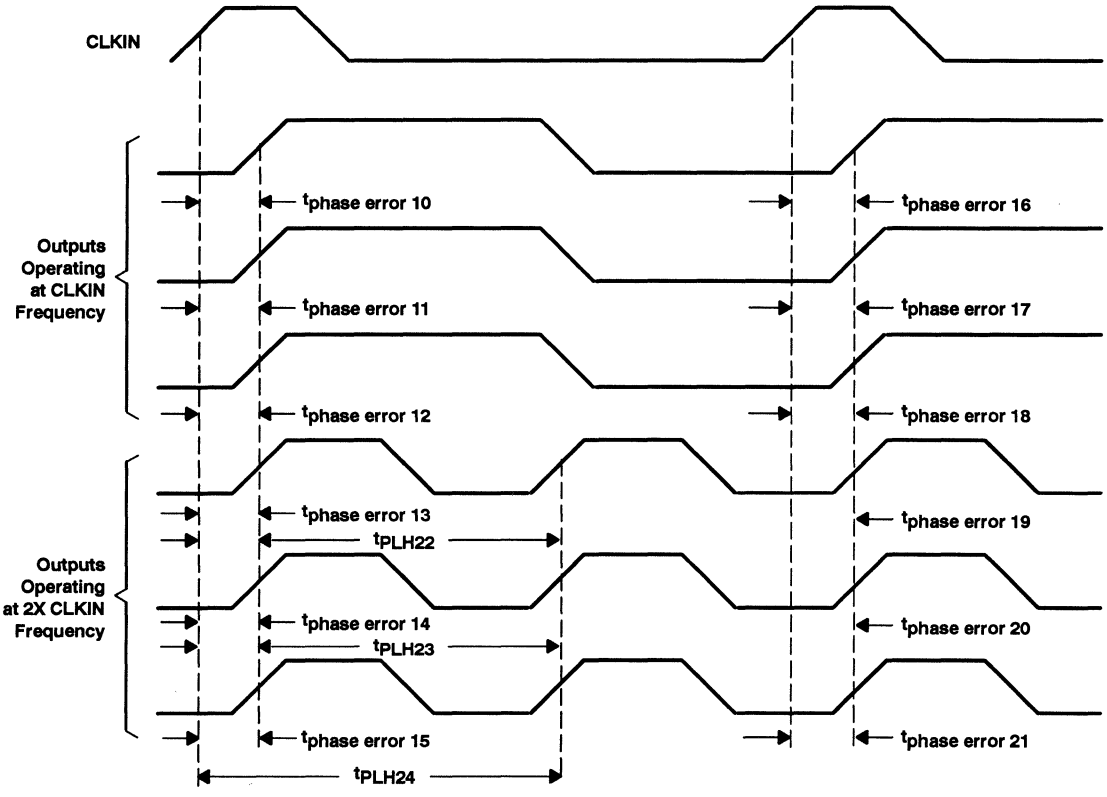
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

Figure 2. Skew Waveforms and Calculations

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 16, 17, . . . 21)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 22, 23, 24)

where:

$$t_{phase\ error\ 22} = t_{PLH22} - \frac{1}{2 \times (2f_{clock})}$$

$$t_{phase\ error\ 23} = t_{PLH23} - \frac{1}{2 \times (2f_{clock})}$$

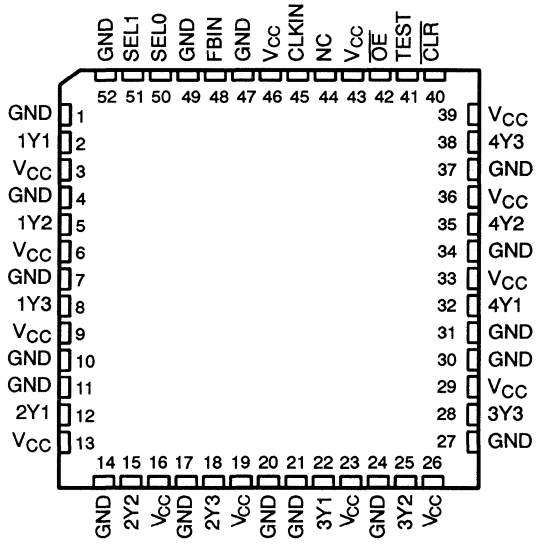
$$t_{phase\ error\ 24} = t_{PLH24} - \frac{1}{2 \times (2f_{clock})}$$

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

PRODUCT PREVIEW

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- Edge-Triggered Clear for Half-Frequency Outputs
- TTL-Compatible Inputs and Outputs
- Outputs Drive 50-Ω Parallel-Terminated Transmission Lines
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package

PBG PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC586 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

PRODUCT PREVIEW

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description (continued)

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the twelve output clocks must be fed back to the FBIN input for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) and clear ($\overline{CLR}$) inputs are also provided for output control and synchronization. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. The $\overline{CLR}$ input is negative edge triggered and is provided to allow phase synchronization of the outputs operating at half frequency on multiple CDC586 devices. The TEST input is used for factory testing of the device and is not intended for customer use. The TEST pin should be strapped to GND.

Unlike many products containing PLLs, the CDC586 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC586 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon phase reset of the half-frequency outputs and upon enable of all outputs; therefore, stabilization is also required when switching from the clear or high-impedance state to the active state.

The CDC586 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the CDC586 phase-lock loop has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the CDC586 outputs. A 2-bit counter is used to divide the VCO frequency. The two outputs of this counter (divide-by-two and divide-by-four) operate at one-half and one-fourth the VCO frequency, respectively, at a duty cycle of 50%. The SEL0 and SEL1 inputs select which of these two counter outputs is buffered to each bank of device outputs.

One device output must be externally wired to the feedback input (FBIN) to complete the phase-lock loop. The VCO operates such that the frequency and phase of this output will match that of the CLKIN signal. In the case that a divide-by-two output is wired to FBIN, the VCO must operate at twice the CLKIN frequency resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a divide-by-four output is wired to FBIN, the device outputs operate at twice or the same as the CLKIN frequency.

output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to the FBIN input. The input frequency range for the CLKIN input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as the CLKIN input.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2x FREQUENCY	1x FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to the FBIN input. The input frequency range for the CLKIN input is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of the CLKIN input.

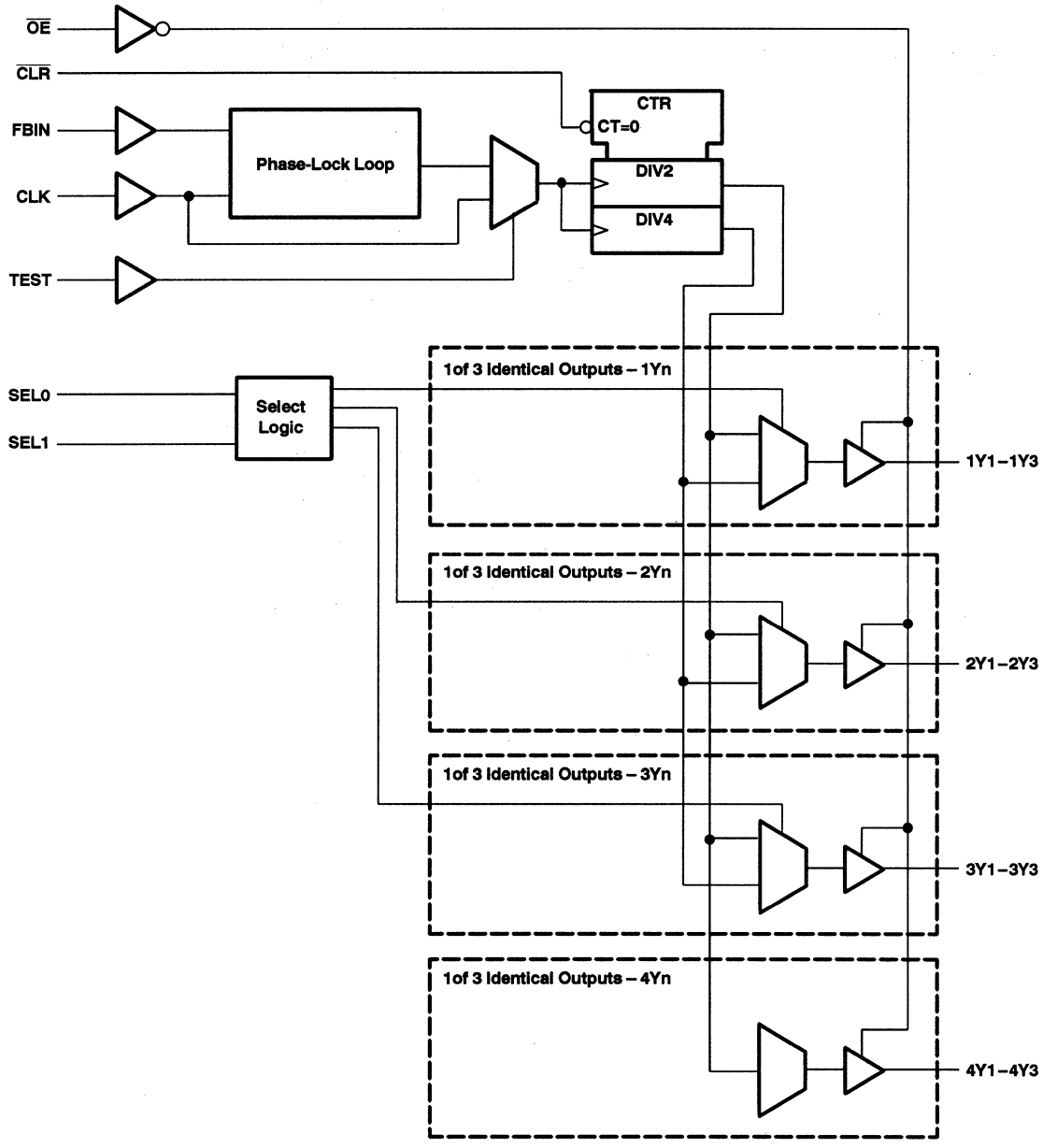
Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1x FREQUENCY	2x FREQUENCY
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn
L	L	N/A	N/A

NOTE: n = 1, 2, 3

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal to be distributed by the CDC586 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	40	I	Clear. $\overline{CLR}$ is used to reset the Y outputs configured as half-frequency outputs to a known phase. It is useful to ensure that the half-frequency output signals of multiple CDC586 circuits are all in the same phase. The $\overline{CLR}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{CLR}$, the flip-flop that divides the CLKIN signal is asynchronously cleared to a low level. Following the required stabilization time, half-frequency output signals for all CDC586 units that receive the same CLKIN and $\overline{CLR}$ signals have the same phase.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. The FBIN terminal must be hard wired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and CLKIN inputs.
$\overline{OE}$	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL1, SEL0	51, 50	I	Counter output select. These inputs select up to nine outputs in banks of three to operate at half or double the frequency of the CLKIN signal (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	Four-bit output ports. These outputs are configured by the select inputs (SEL1, SEL0) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select inputs and the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals will be nominally 50% independent of the duty cycle of the CLKIN signal. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, the $\overline{CLR}$ input is provided to allow the outputs of multiple CDC586 circuits operating at half-frequency to be reset to the same phase.
4Y1–4Y3	32, 35, 38	O	Four-bit output ports. These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the CLKIN signal.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .. −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = −32 mA		2		
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA			0.2	V
		I_{OL} = 32 mA			0.5	
I_I	V_{CC} = 0 or MAX†,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	mA
			Outputs low		1	
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND				4	pF
C_o	V_O = V_{CC} or GND				8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
		VCO is operating at double the CLKIN frequency	50	100	
t_w	Pulse duration	$\overline{CLR}$ low			ns
	Input clock duty cycle		40	60	%
	Stabilization time†	After SEL1, SEL0		50	μs
		After $\overline{CLR}\downarrow$		50	
		After $\overline{OE}\downarrow$		50	
		After power up		50	

† Time required for the integrated phase-lock loop circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

NOTE 3: Preliminary specifications based on SPICE analysis.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 thru 3)

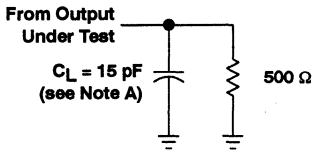
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
$t_{phase\ error}$‡	CLKIN↑	Y		±500	ps
$t_{sk(o)}$	CLKIN	Y		0.5	ns
$t_{sk(pr)}$	CLKIN	Y		1	ns
$t_{jitter(RMS)}$	CLKIN↑	Y		25	ps
Duty cycle		Y	45%	55%	
t_r				1.4	ns
t_f				1.4	ns

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the feedback input FBIN.

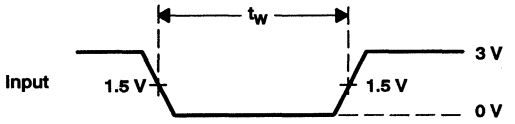
NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PRODUCT PREVIEW

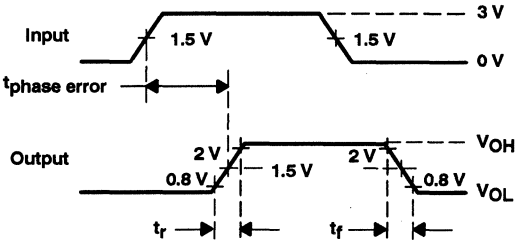
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



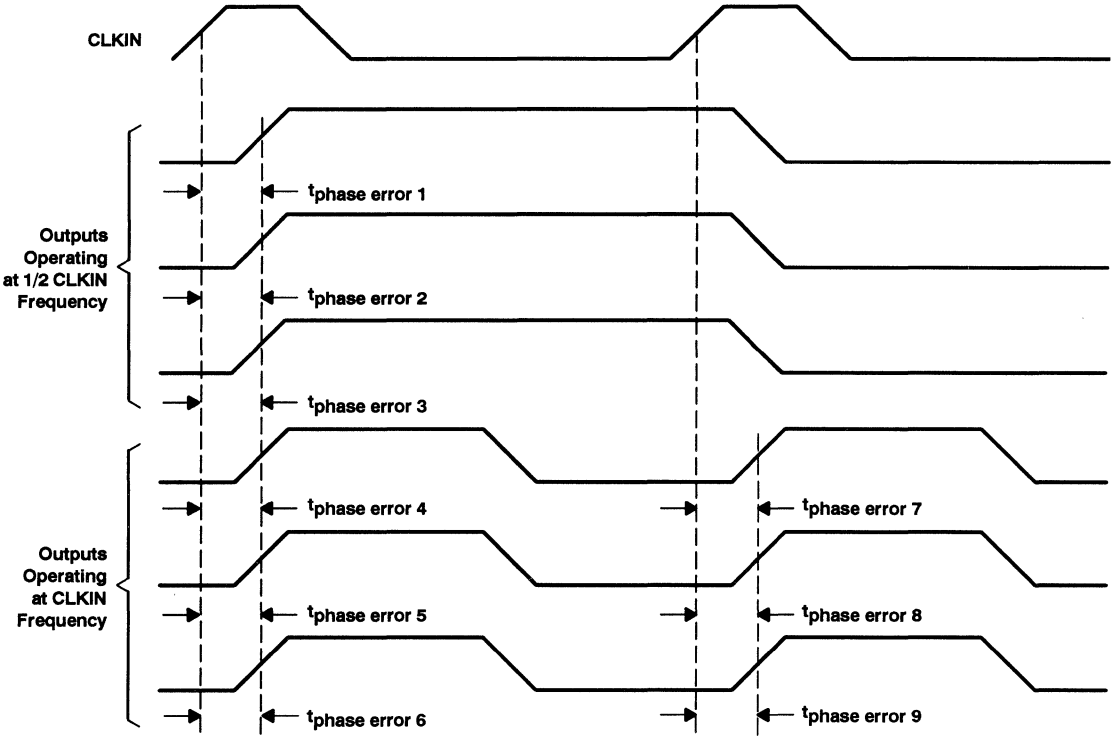
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

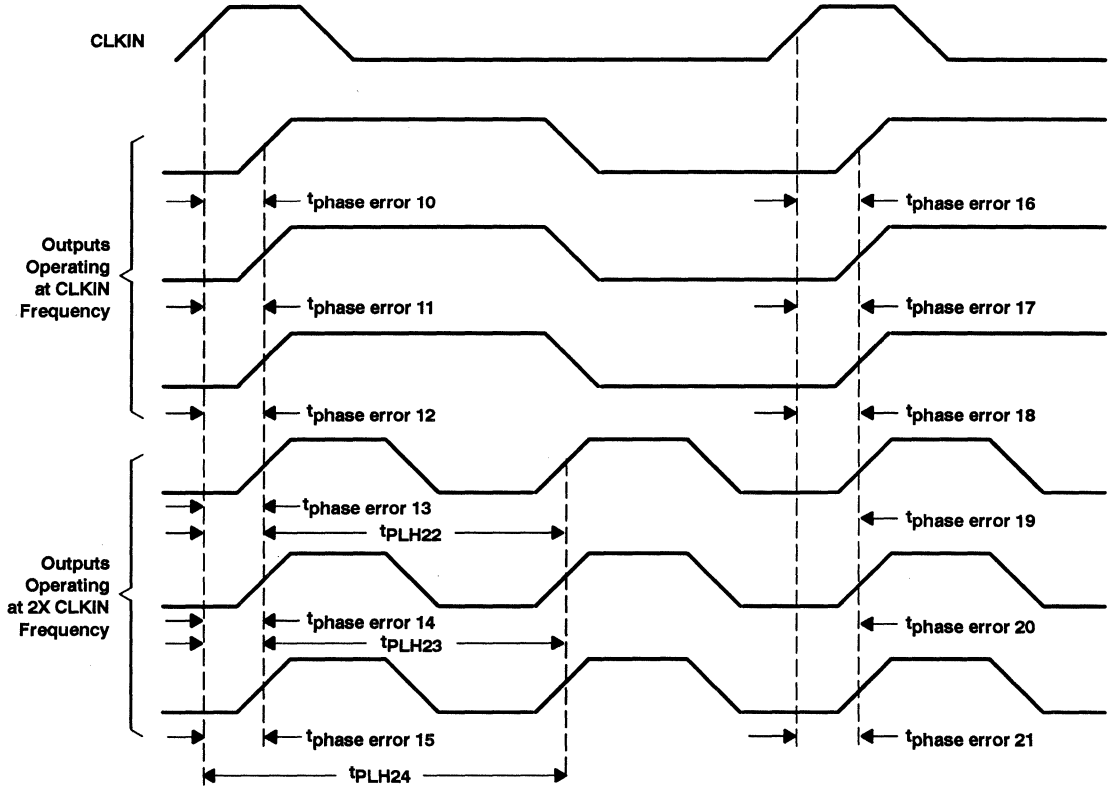
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 16, 17, . . . 21)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 22, 23, 24)

where:

a. $t_{phase\ error\ 22} = t_{PLH22} - \frac{1}{2 \times (2f_{clock})}$

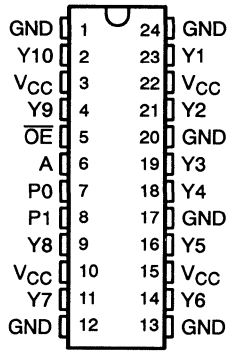
b. $t_{phase\ error\ 23} = t_{PLH23} - \frac{1}{2 \times (2f_{clock})}$

c. $t_{phase\ error\ 24} = t_{PLH24} - \frac{1}{2 \times (2f_{clock})}$

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Ten Outputs**
- **Outputs Have Internal Series Damping Resistor To Reduce Transmission Line Effects**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC2351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input is provided to disable the outputs to a high-impedance state. Each output has an internal series damping resistor to improve signal integrity at the load. The CDC2351 operates at 3.3-V V_{CC}.

The CDC2351 propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part to part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

The CDC2351 is characterized for operation from 0°C to 70°C.

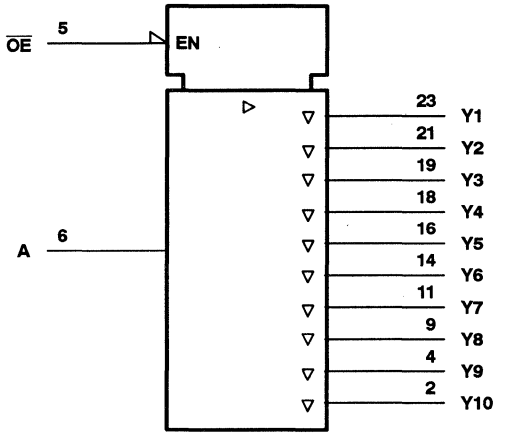
FUNCTION TABLE

INPUTS		OUTPUTS
A	$\overline{OE}$	Yn
L	H	Z
H	H	Z
L	L	L
H	L	H

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

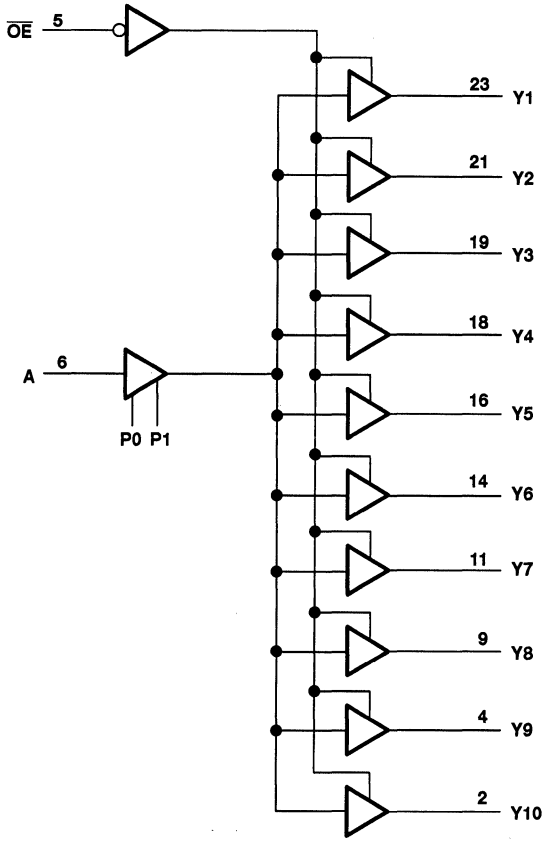
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 3.6 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_I < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and negative-voltage rating may be exceeded if the input clamp-current rating is observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−12	mA
I_{OL}	Low-level output current		12	mA
f_{clock}	Input clock frequency		100	MHz
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	MIN	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 32 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 32 mA					0.5	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1		±1	µA
I_O†	V_{CC} = 3.6 V,	V_O = 2.5 V						mA
I_{OZ}	V_{CC} = 3.6 V,	V_{CC} = 3 V or 0						µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high					mA
			Outputs low					
			Outputs disabled					
C_i	V_I = V_{CC} or GND							pF
C_o	V_O = V_{CC} or GND							pF

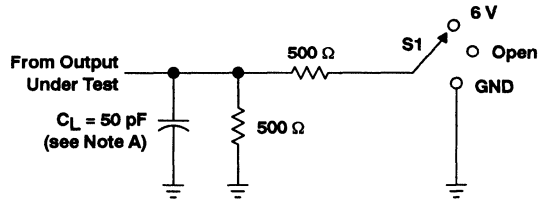
† Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V, T_A = 25°C MIN	TYP	MAX	V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C MIN	MAX	UNIT
t_{PLH}	A	Y						ns
t_{PHL}								
t_{PZH}	$\overline{OE}$	Y						ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y						ns
t_{PLZ}								
$t_{sk(o)}$	A	Y		0.3	0.5		0.5	ns
$t_{sk(p)}$	A	Y		0.6	0.8		0.8	ns
$t_{sk(pr)}$	A	Y			1		1	ns
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

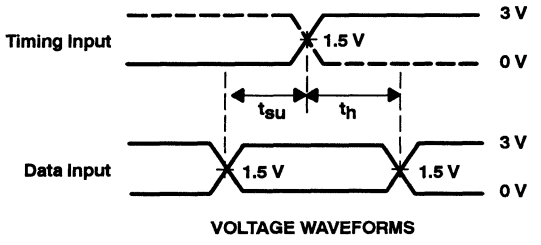
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

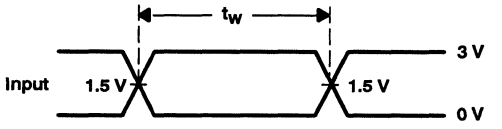


LOAD CIRCUIT

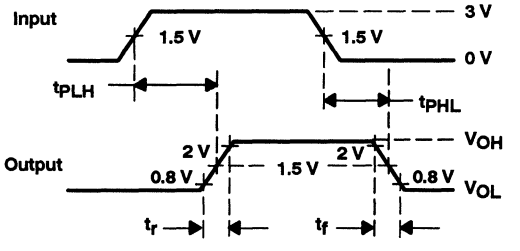
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



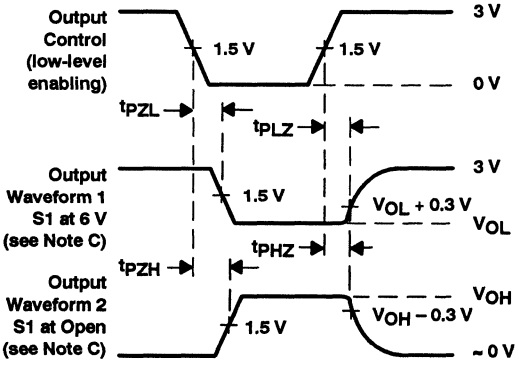
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



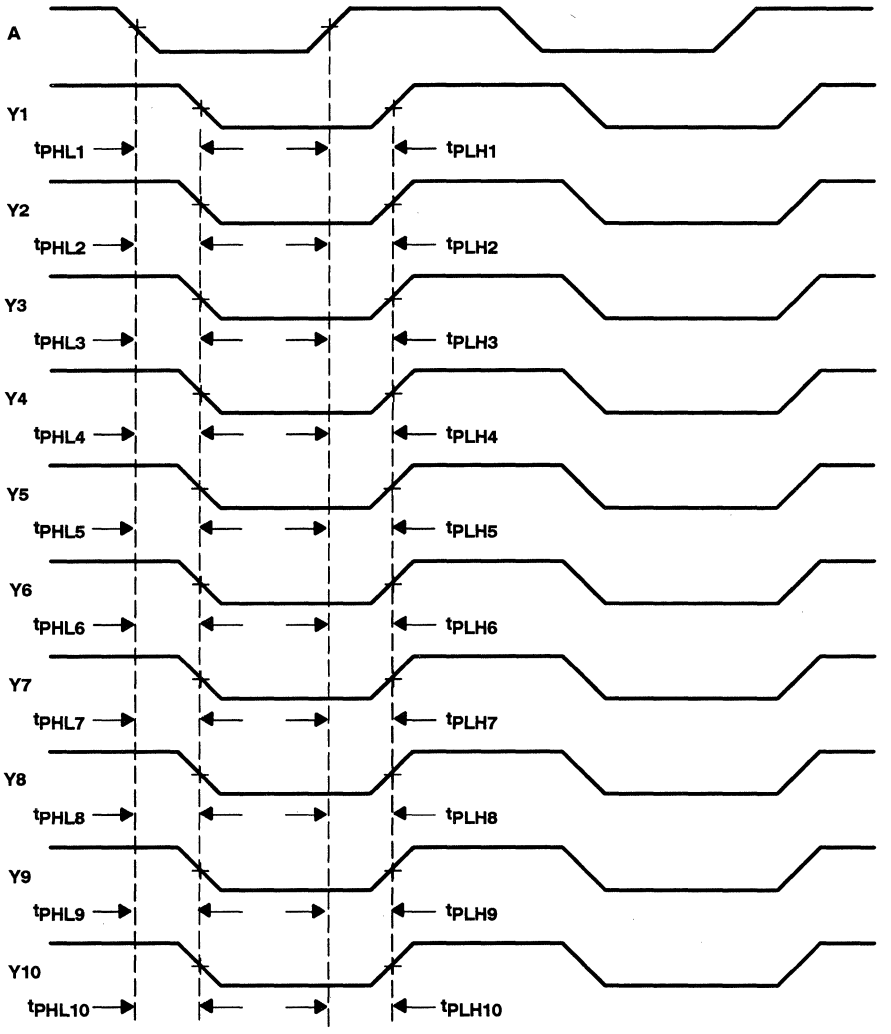
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

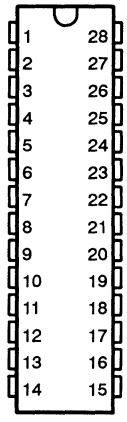
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Up to Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **On-Chip Series Damping Resistors**
- **External Feedback Pin (FBIN) is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **Edge-Triggered Clear for Half-Frequency Outputs**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Platic 28-Pin Shrink Small Outline Package (SSOP)**

DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The CDC2536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with syncronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC2536 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line. The CDC2536 also provides on-chip series damping resistors, eliminating the need for external termination components.

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to the FBIN input for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select input (SEL) configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) and clear ($\overline{CLR}$) inputs are also provided for output control and synchronization. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. The $\overline{CLR}$ input is negative edge triggered and is provided to allow phase synchronization of the outputs operating at half frequency on multiple CDC2536 devices. The TEST input is used for factory testing of the device and is not intended for customer use. The TEST pin should be strapped to GND.

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description (continued)

Unlike many products containing PLLs, the CDC2536 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2536 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon phase reset of the half-frequency outputs and upon enable of all outputs; therefore, stabilization is also required when switching from the clear or high-impedance state to the active state.

The CDC2536 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the CDC2536 phase-lock loop has a frequency range of 100 MHz to 200 MHz, twice the operating frequency of the CDC2536 outputs. A two–bit counter is used to divide the VCO frequency. The two outputs of this counter (divide-by-two and divide-by-four) operate at one-half and one-fourth the VCO frequency, respectively, at a duty cycle of 50%. The SEL input selects which of these two counter outputs is buffered to each bank of device outputs.

One device output must be externally wired to the feedback input (FBIN) to complete the phase-lock loop. The VCO operates such that the frequency and phase of this output matches that of the CLKIN signal. In the case that a divide-by-two output is wired to FBIN, the VCO must operate at twice the CLKIN frequency resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a divide-by-four output is wired to FBIN, the device outputs operate at twice the frequency or the same frequency as the CLKIN input.

output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to the FBIN input. The input frequency range for the CLKIN input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as the CLKIN input.

Table 1. Output Configuration A

INPUTS	OUTPUTS	
SEL	1/2x FREQUENCY	1x FREQUENCY
L	None	All
H	1Yn	2Yn

NOTE: n = 1, 2, 3

PRODUCT PREVIEW

output configuration B

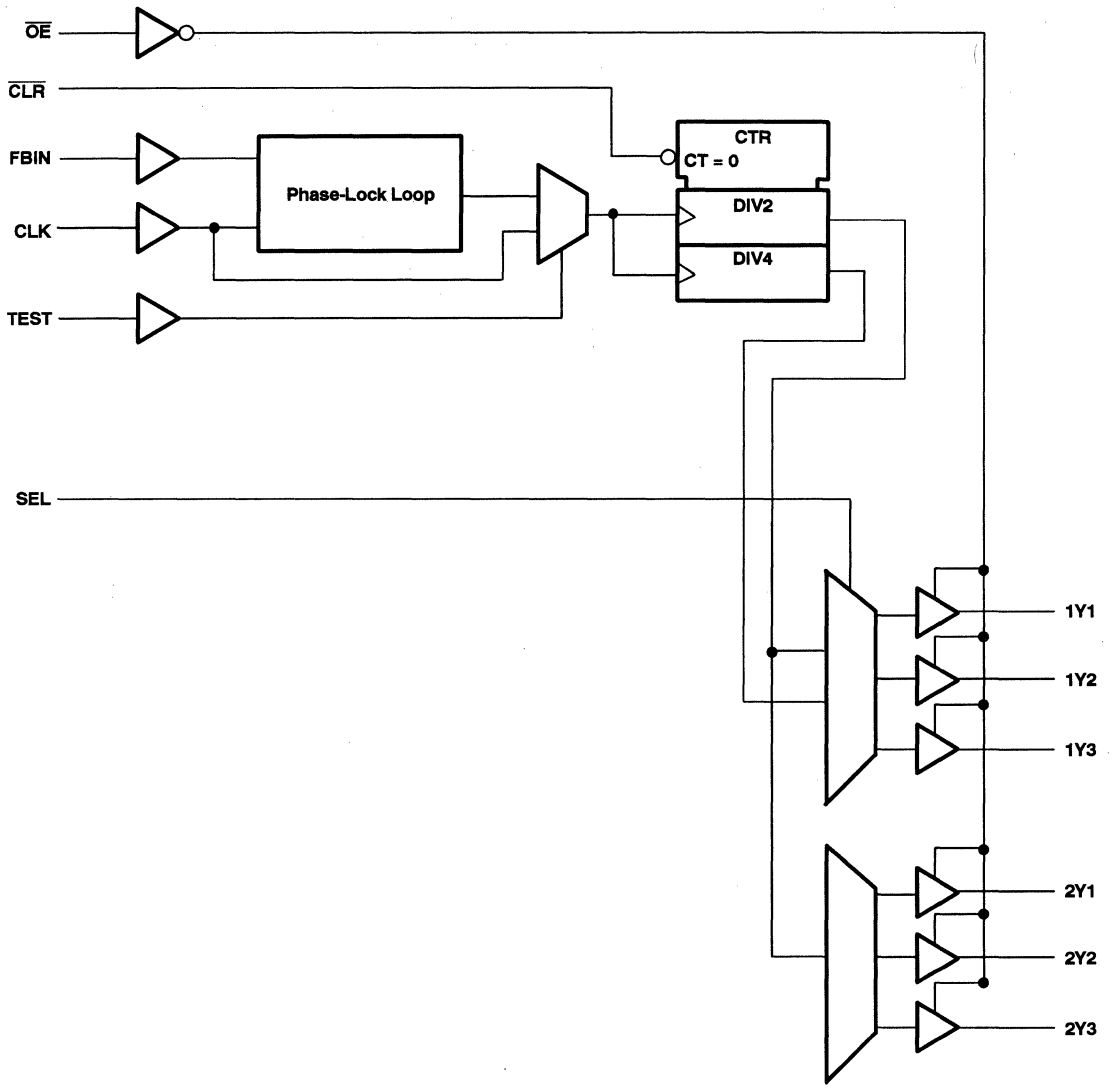
Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to the FBIN input. The input frequency range for the CLKIN input is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of the CLKIN input.

Table 2. Output Configuration B

INPUTS	OUTPUTS	
SEL	1x FREQUENCY	2x FREQUENCY
H	All	None
L	1Yn	2Yn

NOTE: n = 1, 2, 3

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	TBD	I	Clock input. CLKIN provides the clock signal to be distributed by the CDC2536 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	TBD	I	Clear. $\overline{CLR}$ is used to reset the Y outputs configured as half-frequency outputs to a known phase. $\overline{CLR}$ is useful to ensure that the half-frequency output signals of multiple CDC2536 circuits are all in the same phase. The $\overline{CLR}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{CLR}$, the flip-flop that divides the CLKIN signal is asynchronously cleared to a low level. Following the required stabilization time, half-frequency output signals for all CDC2536 units that receive the same CLKIN and $\overline{CLR}$ signals have the same phase.
FBIN	TBD	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard wired to one of the six clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and differential CLKIN inputs.
$\overline{OE}$	TBD	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL	TBD	I	Counter output select. SEL selects the output configuration (see Tables 1 and 2 for details).
TEST	TBD	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be grounded for normal operation.
1Y1–1Y3	TBD	O	Four-bit output ports. These outputs are configured by the select input (SEL) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select input. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, the $\overline{CLR}$ input is provided to allow the outputs of multiple CDC2536 circuits operating at half-frequency to be reset to the same phase.
2Y1–2Y3	TBD	O	Four-bit output ports. These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .. −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 24 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = − 32 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.8	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	mA
			Outputs low		1	
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND					pF
C_o	V_O = V_{CC} or GND					pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	When VCO is operating at four times the CLKIN frequency	25	50	MHz
		When VCO is operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
t_w	Pulse duration	$\overline{CLR}$ low			ns
	Stabilization time†	After SEL		50	µs
		After $\overline{CLR}\downarrow$		50	
		After $\overline{OE}\downarrow$		50	
		After power up		50	

NOTE 3: Preliminary specifications based on SPICE analysis.

† Time required for the integrated phase-lock loop circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

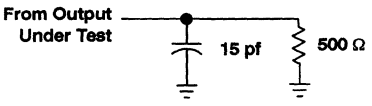
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
$t_{phase\ error}$‡	CLKIN↑	Y		±500	ps
$t_{sk(o)}$ (see Figure 3)	CLKIN	Y		0.5	ns
$t_{sk(pr)}$	CLKIN	Y		1	ns
$t_{jitter\ (RMS)}$	CLKIN↑	Y		25	ps
Duty cycle		Y	45%	55%	
t_r				1.4	ns
t_f				1.4	ns

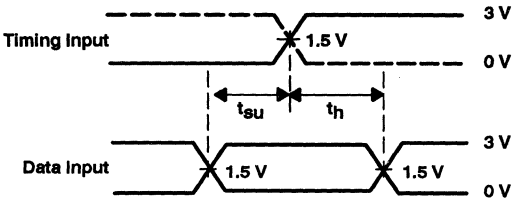
NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the feedback input FBIN.

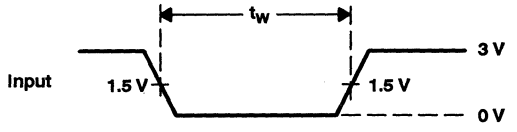
PARAMETER MEASUREMENT INFORMATION



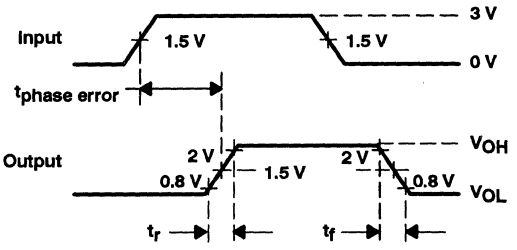
LOAD CIRCUIT FOR OUTPUTS



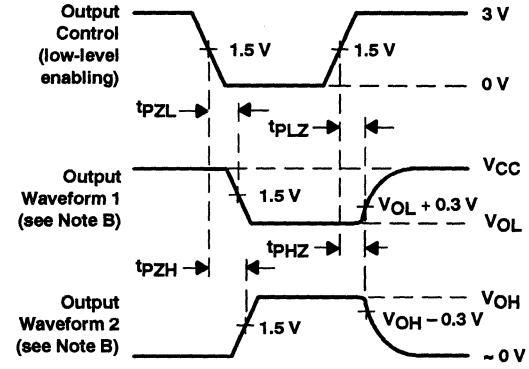
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

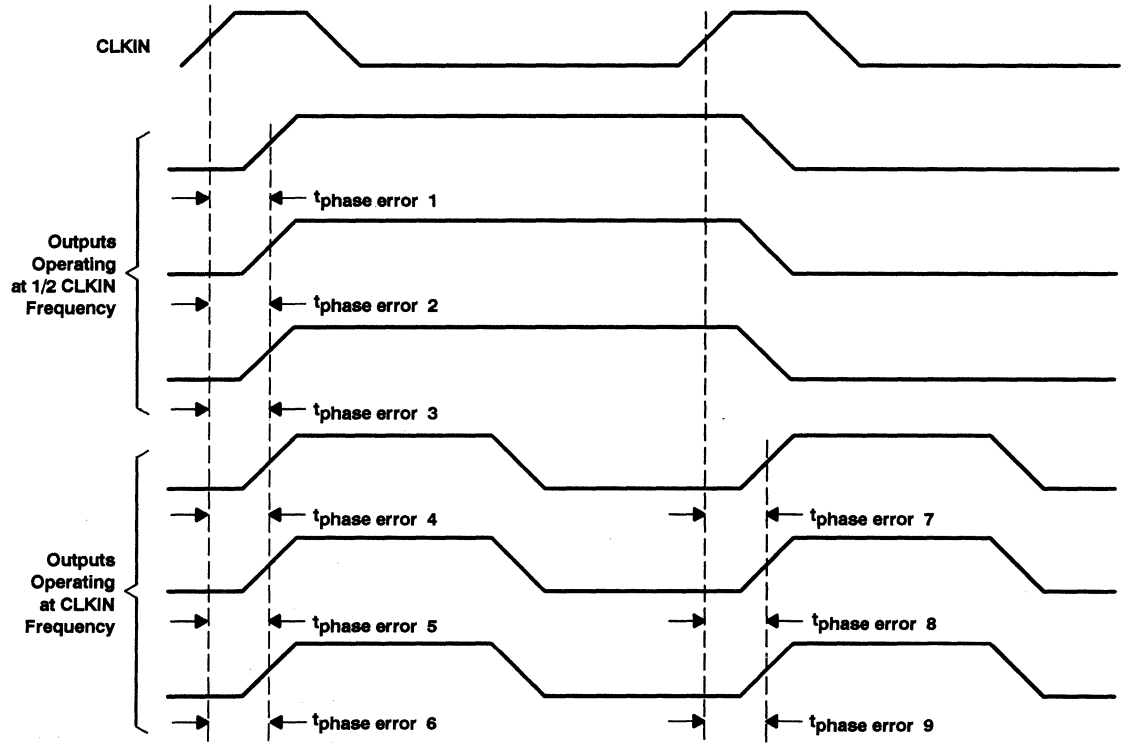


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

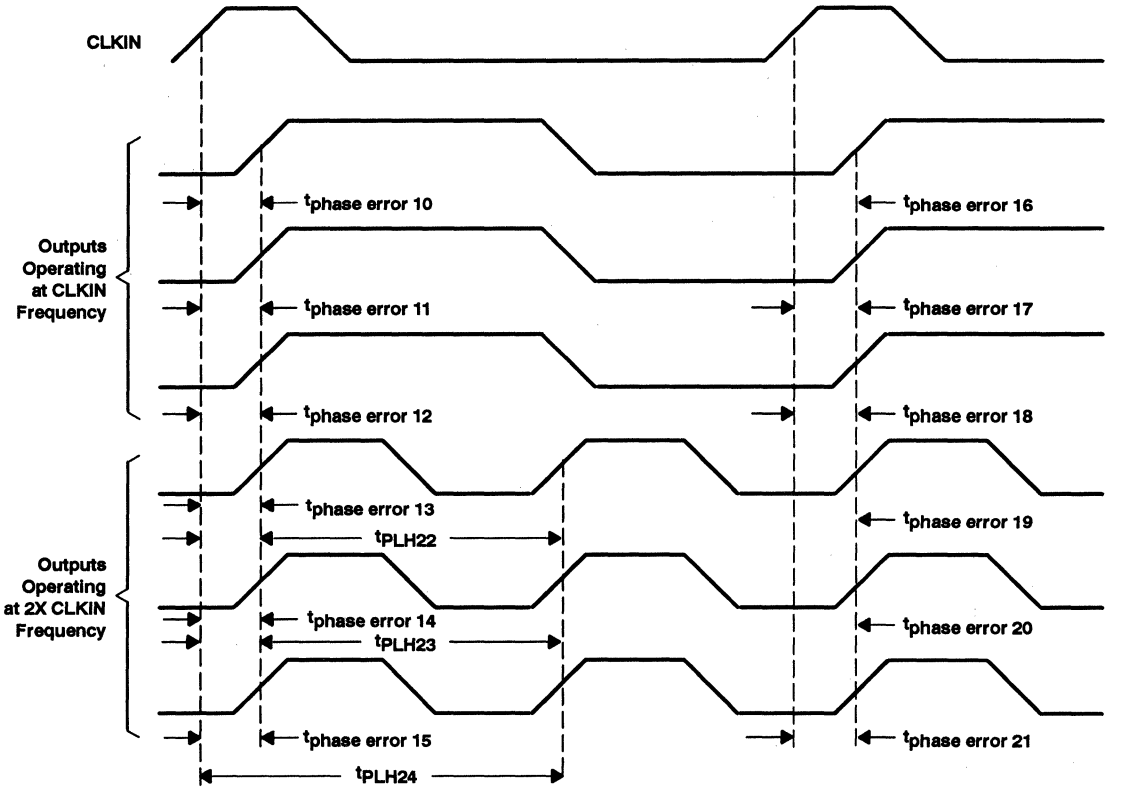
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

Figure 2. Skew Waveforms and Calculations

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 16, 17, . . . 21)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 22, 23, 24)

where:

a. $t_{phase\ error\ 22} = t_{PLH22} - \frac{1}{2 \times (2f_{clock})}$

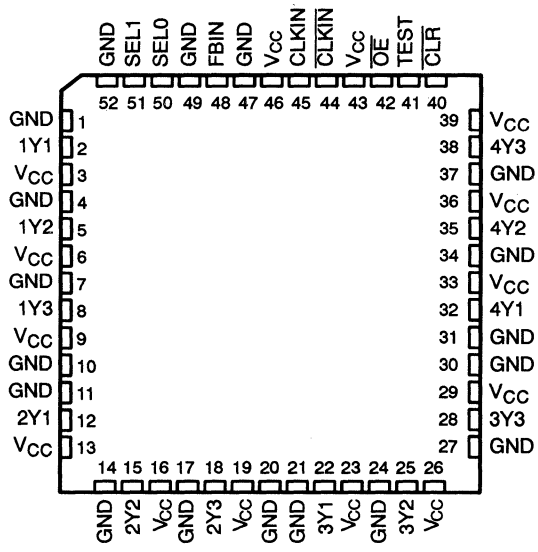
b. $t_{phase\ error\ 23} = t_{PLH23} - \frac{1}{2 \times (2f_{clock})}$

c. $t_{phase\ error\ 24} = t_{PLH24} - \frac{1}{2 \times (2f_{clock})}$

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes Differential LVPECL Clock Inputs to Twelve TTL-Compatible Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) is Used to Synchronize the Outputs With the Clock Inputs
- Application for Synchronous DRAMs
- Outputs Have Internal 26-Ω Series Resistors To Dampen Transmission Line Effects
- Edge-Triggered Clear for Half-Frequency Outputs
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Quad Flat Package

PBG PACKAGE
(TOP VIEW)



description

The CDC2582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, $\overline{\text{CLKIN}}$) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. Each output has an internal 26-Ω series resistor that improves the signal integrity at the load. The CDC2582 operates at 3.3-V V_{CC}.

The feedback (FBIN) input is used to synchronize the output clocks frequency with the input clock signals (CLKIN, $\overline{\text{CLKIN}}$). One of the twelve output clocks must be fed back to the FBIN input for the PLL to maintain synchronization between the differential CLKIN and $\overline{\text{CLKIN}}$ inputs and the outputs. The output used as the feedback pin is syncronized to the same frequency as the clock inputs (CLKIN and $\overline{\text{CLKIN}}$).

PRODUCT PREVIEW

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description (continued)

The Y outputs can be configured to switch in phase and at the same frequency as differential clock inputs (CLKIN and $\overline{\text{CLKIN}}$). Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the differential clock input frequency, depending upon the feedback configuration (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clocks.

Output-enable ($\overline{\text{OE}}$) and clear ($\overline{\text{CLR}}$) inputs are also provided for output control and synchronization. When $\overline{\text{OE}}$ is high, the outputs are in the low state. When $\overline{\text{OE}}$ is low, the outputs are active. The $\overline{\text{CLR}}$ input is negative-edge-triggered and is provided to allow phase synchronization of the outputs operating at half frequency on multiple CDC2582 devices. The test input is used for factory testing of the device and is not intended for customer use. The test pin should be connected to GND.

Unlike many products containing a PLL, the CDC2582 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2582 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN and $\overline{\text{CLKIN}}$ as well as following any changes to the PLL reference or feedback signal. Such changes occur upon phase reset of the half-frequency outputs and upon enable of all outputs. Therefore, stabilization is also required when switching from the clear or low state to the active state.

The CDC2582 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the CDC2582 phase-lock loop has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the CDC2582 outputs. A 2-bit counter is used to divide the VCO frequency. The two outputs of this counter (divide-by-two and divide-by-four) operate at one-half and one-fourth the VCO frequency, respectively, at a duty cycle of 50%. The SEL0 and SEL1 inputs select which of these two counter outputs is buffered to each bank of device outputs.

One device output must be externally wired to the feedback input (FBIN) to complete the phase-lock loop. The VCO operates such that the frequency and phase of this output will match that of the differential clock inputs. In the case that a divide-by-two output is wired to FBIN, the VCO must operate at twice the differential clock inputs frequency resulting in device outputs that operate at either the same or one-half the frequency of the differential clock inputs. If a divide-by-four output is wired to FBIN, the device outputs operate at twice or the same as the CLKIN frequency.

output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to the FBIN input. The frequency range for the differential clock input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the input clock frequency, while outputs configured as 1x outputs operate at the same frequency as the differential clock input.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2x FREQUENCY	1x FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to the FBIN input. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the input clock frequency, while outputs configured as 2x outputs operate at double the frequency of the differential clock inputs.

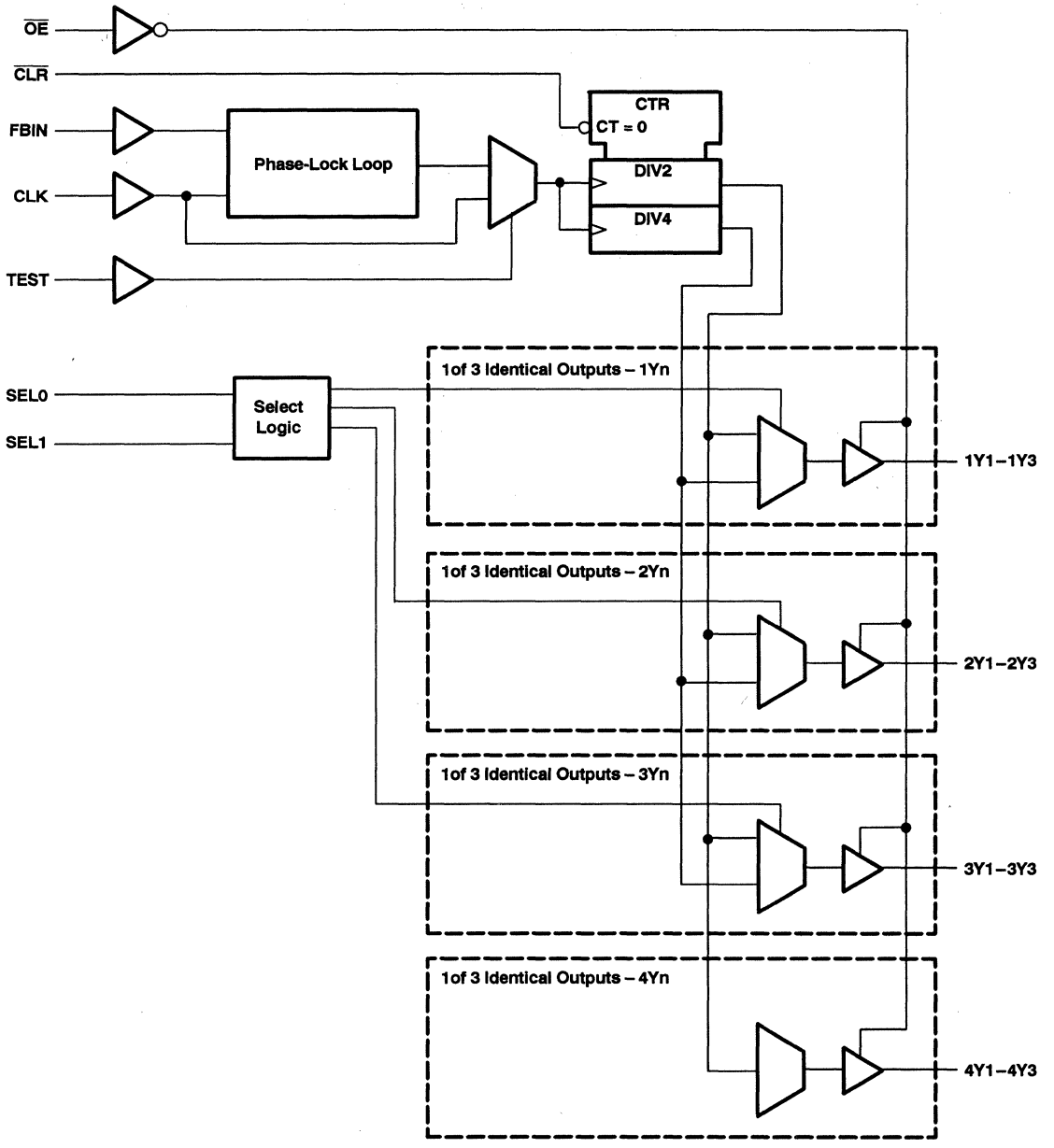
Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1x FREQUENCY	2x FREQUENCY
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn
L	L	N/A	N/A

NOTE: n = 1, 2, 3

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN $\overline{\text{CLKIN}}$	44, 45	I	Clock input. CLKIN and $\overline{\text{CLKIN}}$ are the clock signals to be distributed by the CDC2582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN and $\overline{\text{CLKIN}}$ must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and valid CLKIN and $\overline{\text{CLKIN}}$ signals are applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	40	I	Clear. $\overline{\text{CLR}}$ is used to reset the Y outputs configured as half-frequency outputs to a known phase. It is useful to ensure that the half-frequency output signals of multiple CDC2582 circuits are all in the same phase. The $\overline{\text{CLR}}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{\text{CLR}}$, the flip-flop that divides the CLKIN signal is asynchronously cleared to a low level. Following the required stabilization time, half-frequency output signals for all CDC2582 units that receive the same CLKIN, $\overline{\text{CLKIN}}$, and $\overline{\text{CLR}}$ signals will have the same phase.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. The FBIN terminal must be hard wired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and the differential clock input (CLKIN and $\overline{\text{CLKIN}}$).
$\overline{\text{OE}}$	42	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL1, SEL0	51, 50	I	Counter output select. These inputs select up to nine outputs in banks of three to operate at half or double the frequency of the input clock signals (CLKIN and $\overline{\text{CLKIN}}$). See Tables 1 and 2.
TEST	41	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	Four-bit output ports. These output terminals are configured by the select inputs (SEL1, SEL0) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the select inputs and the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the input clock signals. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, the $\overline{\text{CLR}}$ input is provided to allow the outputs of multiple CDC2582 circuits operating at half-frequency to be reset to the same phase. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1–4Y3	32, 35, 38	O	Four-bit output ports. These output terminals transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the CLKIN signal. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .. −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	Other inputs	2		V
		CLKIN, $\overline{CLKIN}$	$V_{CC}-1.025$		
V_{IL}	Low-level input voltage	Other inputs		$V_{CC}-1.62$	V
		CLKIN, $\overline{CLKIN}$		1.6	
V_I	Input voltage		0	5.5	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature		0	70	°C

NOTE 2: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = −100 µA		$V_{CC}-0.2$		V
	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA			0.2	V
		I_{OL} = 12 mA			0.8	
I_I	V_{CC} = 0 or MAX†,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		5	mA
			Outputs low		1	
C_i	V_I = 3 V or 0				4	pF
C_o	V_O = 3 V or 0				8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN/$\overline{\text{CLKIN}}$ frequency	25	50	MHz
		VCO is operating at double the CLKIN/$\overline{\text{CLKIN}}$ freque	50	100	
t_w	Pulse duration	$\overline{\text{CLR}}$ low			ns
	Input clock duty cycle		40	60	%
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{\text{CLR}}\downarrow$		50	
		After $\overline{\text{OE}}\downarrow$		50	
		After power up		50	

† Time required for the integrated phase-lock loop circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

NOTE 3: Preliminary specifications based on SPICE analysis.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
$t_{phase\ error}$‡	CLKIN↑	Y		±500	ps
$t_{sk(o)}$ (see Figure 3)	CLKIN	Y		0.5	ns
$t_{sk(pr)}$	CLKIN	Y		1	ns
$t_{jitter(RMS)}$	CLKIN	Y		25	ps
Duty cycle		Y	45	55	%
t_r				1.4	ns
t_f				1.4	ns

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the feedback input FBIN.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

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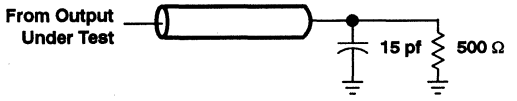
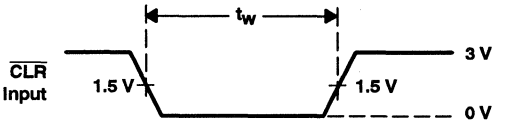
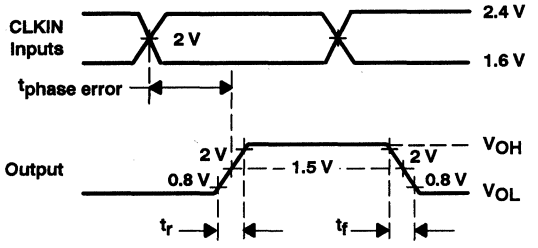
PARAMETER MEASUREMENT INFORMATION



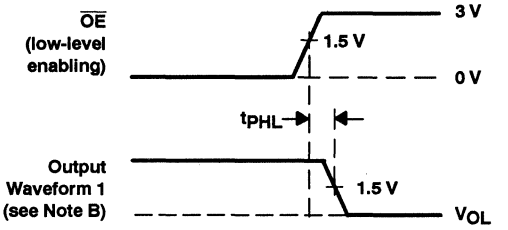
LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



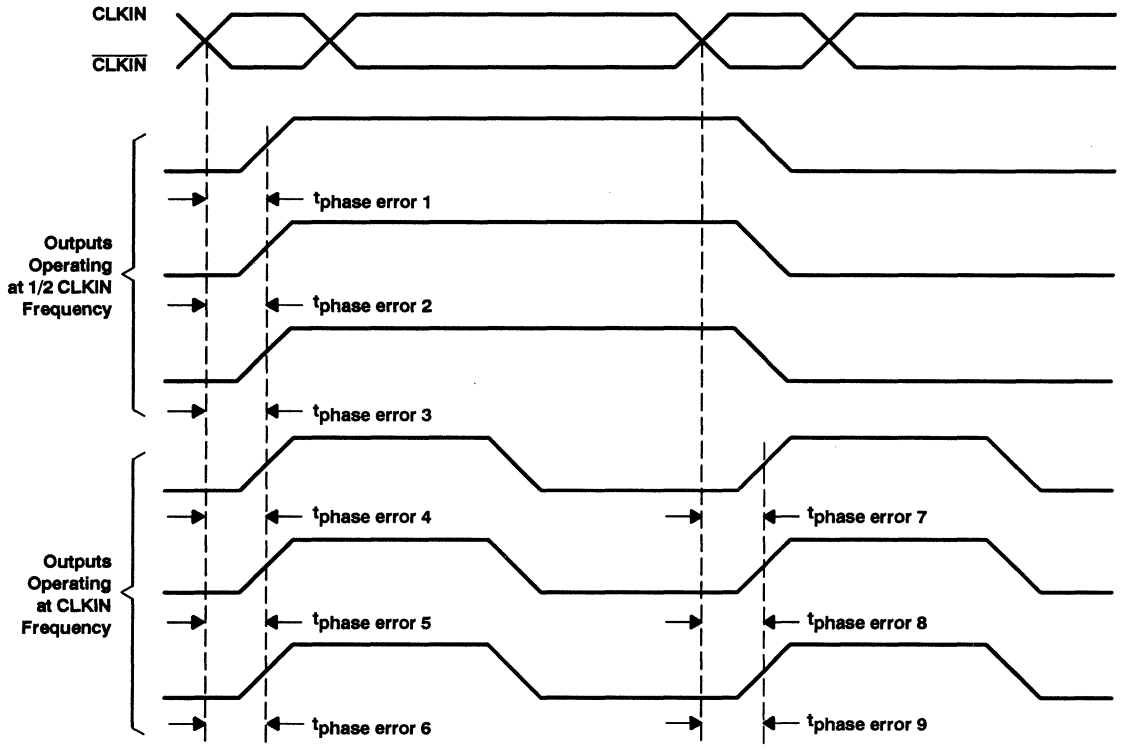
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 75 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

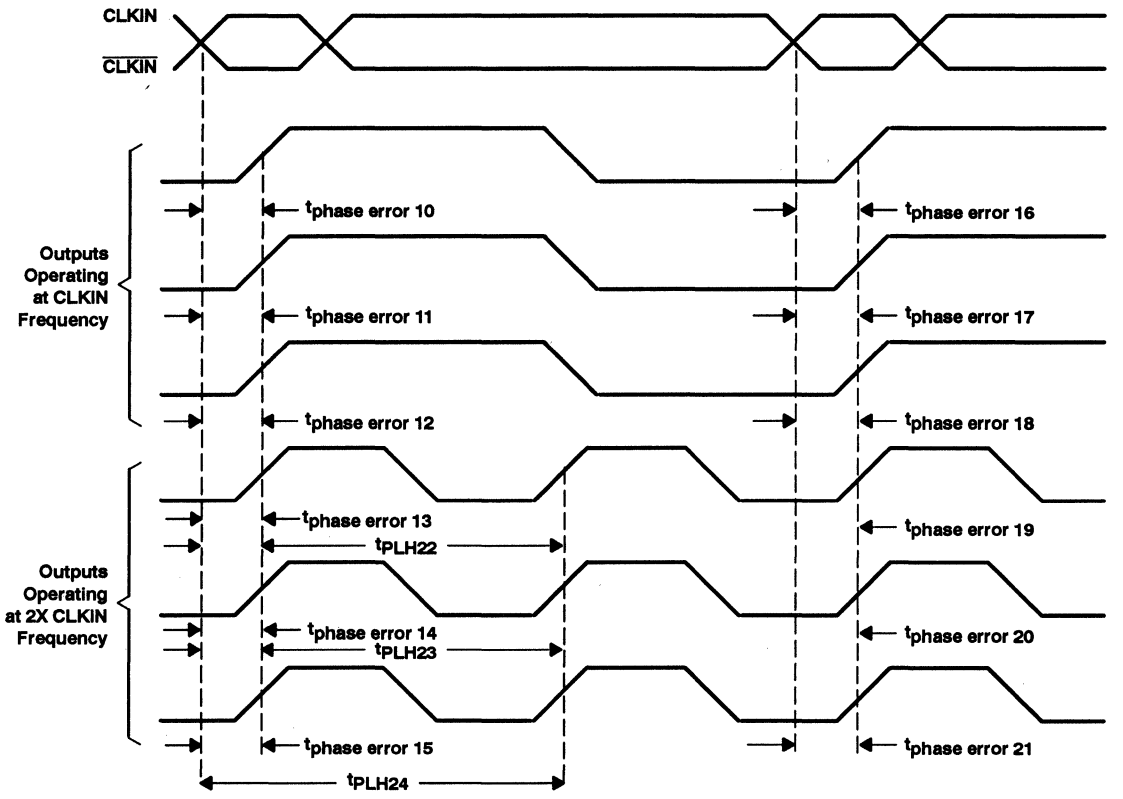


NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

Figure 2. Skew Waveforms and Calculations

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 16, 17, . . . 21)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 22, 23, 24)

where:

$$t_{phase\ error\ 22} = t_{PLH22} - \frac{1}{2 \times (2f_{clock})}$$

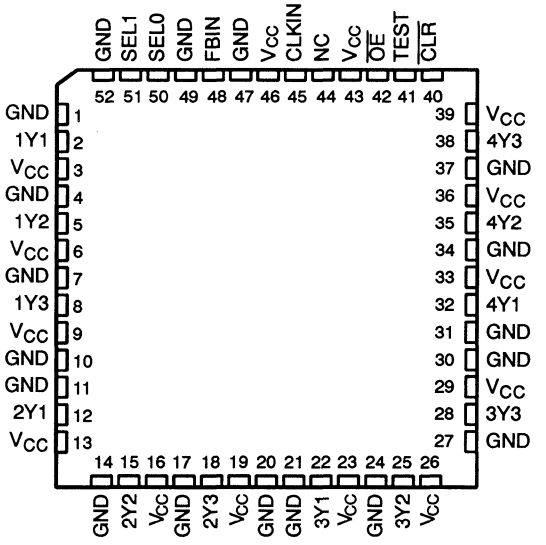
$$t_{phase\ error\ 23} = t_{PLH23} - \frac{1}{2 \times (2f_{clock})}$$

$$t_{phase\ error\ 24} = t_{PLH24} - \frac{1}{2 \times (2f_{clock})}$$

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- Edge-Triggered Clear for Half-Frequency Outputs
- TTL-Compatible Inputs and Outputs
- Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission Line Effects
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package

PBG PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC2586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. Each output has an internal 26-Ω series resistor that improves the signal integrity at the load. The CDC2586 operates at 3.3-V V_{CC}.

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

description (continued)

The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the twelve output clocks must be fed back to the FBIN input for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) and clear ($\overline{CLR}$) inputs are also provided for output control and synchronization. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. The $\overline{CLR}$ input is negative edge triggered and is provided to allow phase synchronization of the outputs operating at half frequency on multiple CDC2586 devices. The TEST input is used for factory testing of the device and is not intended for customer use. The TEST pin should be strapped to GND.

Unlike many products containing PLLs, the CDC2586 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2586 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon phase reset of the half-frequency outputs and upon enable of all outputs; therefore, stabilization is also required when switching from the clear or high-impedance state to the active state.

The CDC2586 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the CDC2586 phase-lock loop has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the CDC2586 outputs. A 2-bit counter is used to divide the VCO frequency. The two outputs of this counter (divide-by-two and divide-by-four) operate at one-half and one-fourth the VCO frequency, respectively, at a duty cycle of 50%. The SEL0 and SEL1 inputs select which of these two counter outputs is buffered to each bank of device outputs.

One device output must be externally wired to the feedback input (FBIN) to complete the phase-lock loop. The VCO operates such that the frequency and phase of this output will match that of the CLKIN signal. In the case that a divide-by-two output is wired to FBIN, the VCO must operate at twice the CLKIN frequency resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a divide-by-four output is wired to FBIN, the device outputs operate at twice or the same as the CLKIN frequency.

output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to the FBIN input. The input frequency range for the CLKIN input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as the CLKIN input.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2x FREQUENCY	1x FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to the FBIN input. The input frequency range for the CLKIN input is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of the CLKIN input.

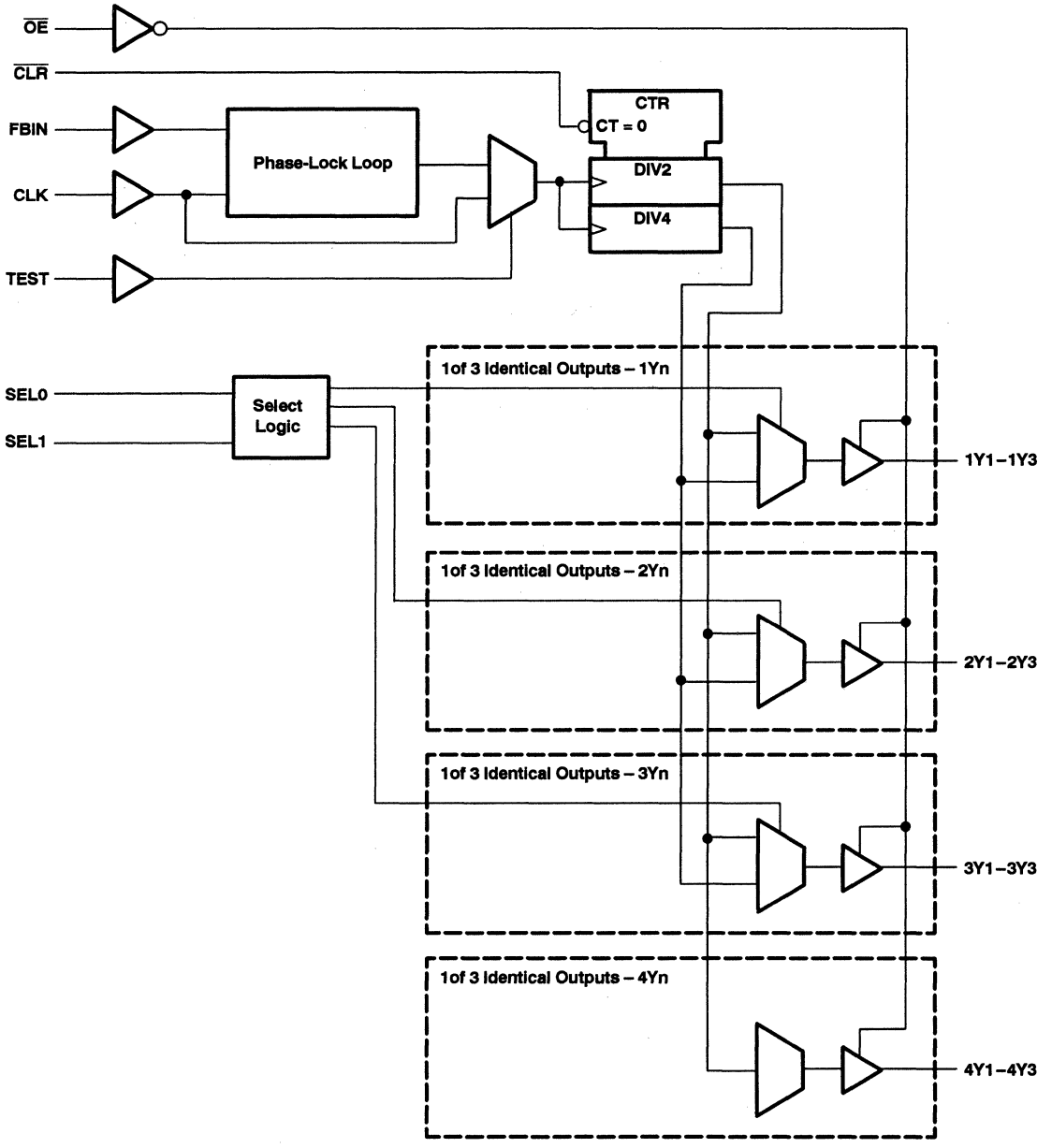
Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1x FREQUENCY	2x FREQUENCY
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn
L	L	N/A	N/A

NOTE: n = 1, 2, 3

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal to be distributed by the CDC2586 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	40	I	Clear. $\overline{CLR}$ is used to reset the Y outputs configured as half-frequency outputs to a known phase. $\overline{CLR}$ is useful to ensure that the half-frequency output signals of multiple CDC2586 circuits are all in the same phase. The $\overline{CLR}$ signal is a negative-edge-triggered signal. When a high-to-low edge occurs at $\overline{CLR}$, the flip-flop that divides the CLKIN signal is asynchronously cleared to a low level. Following the required stabilization time, half-frequency output signals for all CDC586 units that receive the same CLKIN and $\overline{CLR}$ signals have the same phase.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. The FBIN terminal must be hard wired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and CLKIN inputs.
$\overline{OE}$	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL1, SEL0	51, 50	I	Counter output select. These inputs select up to nine outputs in banks of three to operate at half or double the frequency of the CLKIN signal (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	Four-bit output ports. These outputs are configured by the select inputs (SEL1, SEL0) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select inputs and the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the CLKIN signal. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, the $\overline{CLR}$ input has been provided to allow the outputs of multiple CDC2586 circuits operating at half-frequency to be reset to the same phase. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1–4Y3	32, 35, 38	O	Four-bit output ports. These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to the FBIN input. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .. −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 2: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA			0.2	V
		I_{OL} = 12 mA			0.8	
I_I	V_{CC} = 0 or MAX†,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 0 or 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 0 or 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		1	mA
			Outputs low		1	
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND				4	pF
C_o	V_O = V_{CC} or GND				8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
		VCO is operating at double the CLKIN frequency	50	100	
t_w	Pulse duration	$\overline{CLR}$ low			ns
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{CLR}$↓		50	
		After $\overline{OE}$↓		50	
		After power up		50	

† Time required for the integrated phase-locked loop circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

NOTE 3: Preliminary specifications based on SPICE analysis.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 thru 3)

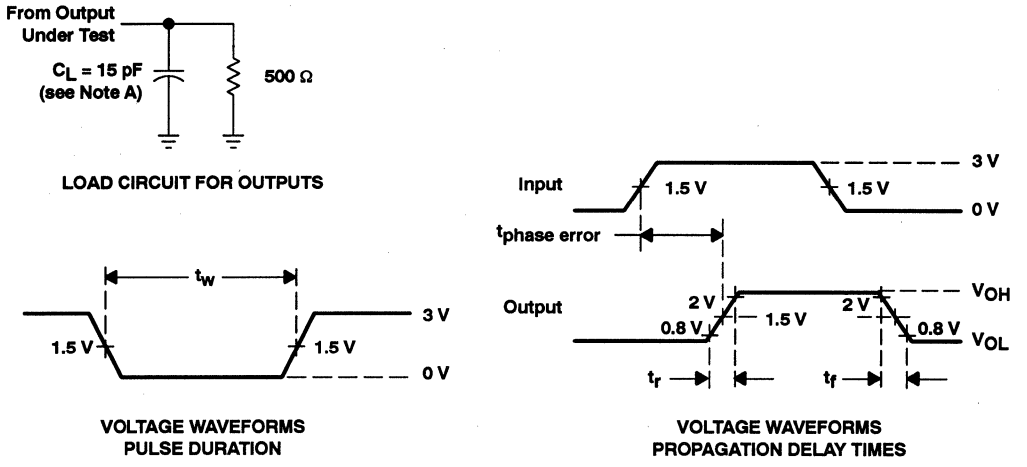
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
$t_{phase\ error}$‡	CLKIN↑	Y		±500	ps
$t_{sk(o)}$	CLKIN	Y		0.5	ns
$t_{sk(pr)}$	CLKIN	Y		1	ns
$t_{jitter(RMS)}$	CLKIN↑	Y		25	ps
Duty cycle		Y	45%	55%	
t_r				1.4	ns
t_f				1.4	ns

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the feedback input FBIN.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

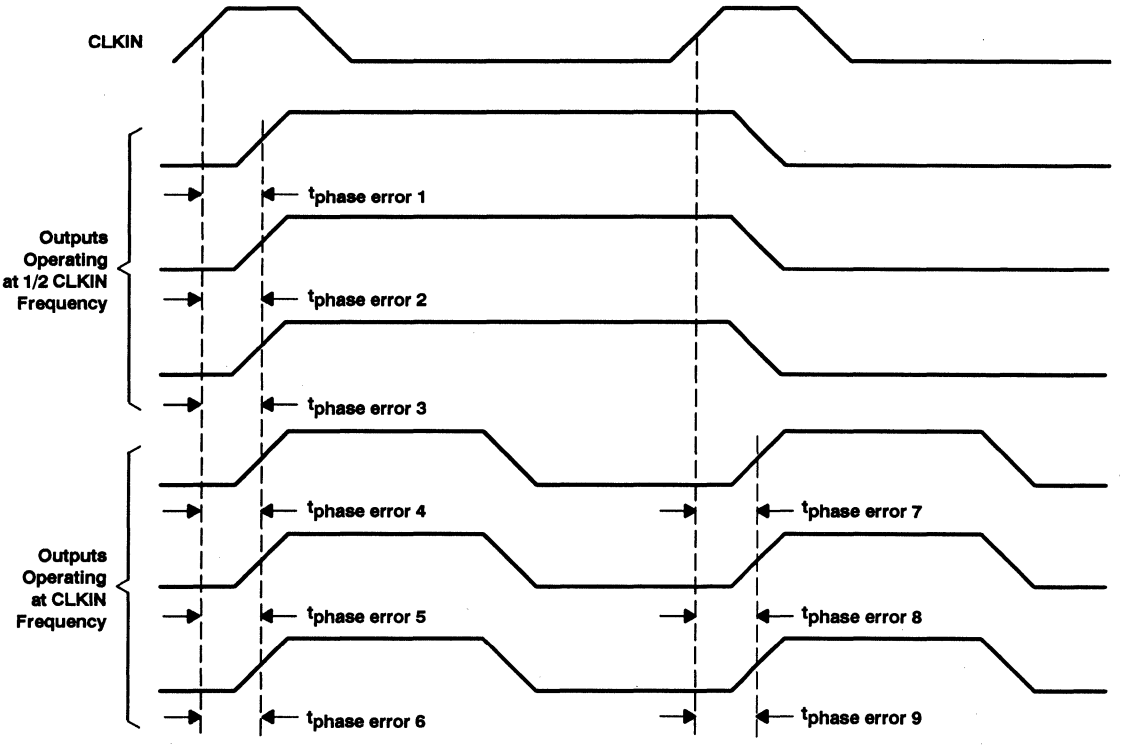


NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

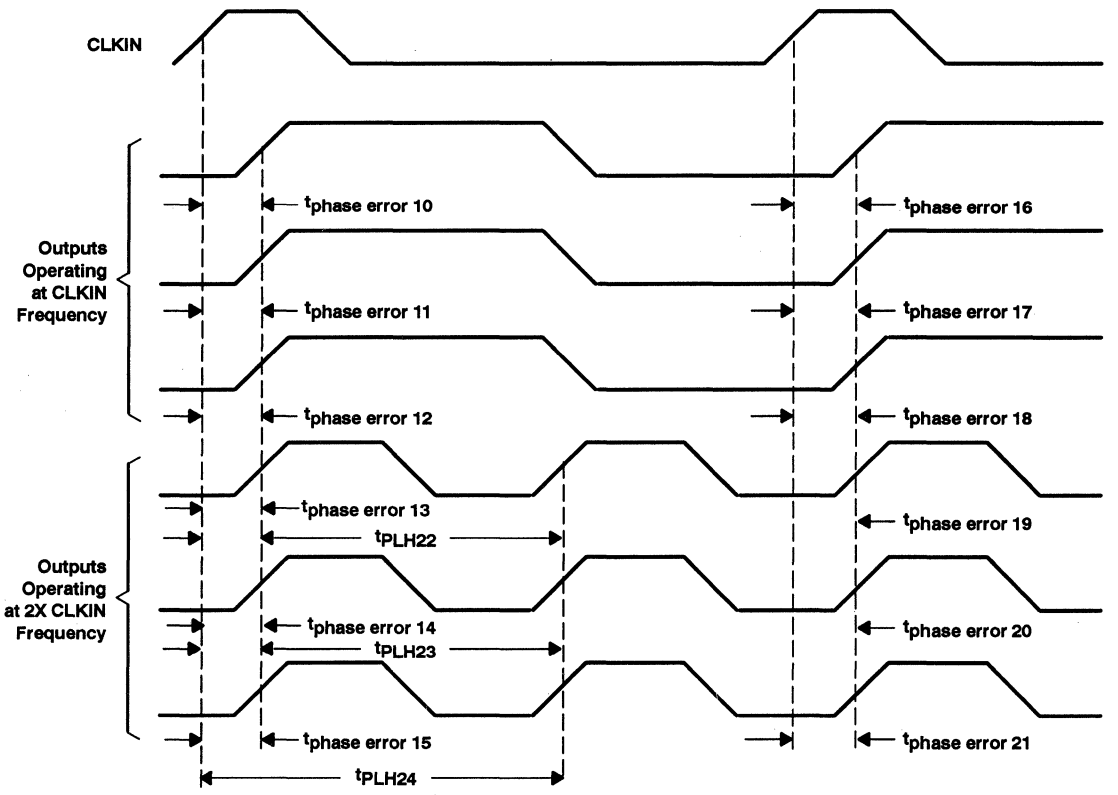
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 16, 17, . . . 21)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 22, 23, 24)

where:

a. $t_{phase\ error\ 22} = t_{PLH22} - \frac{1}{2 \times (2f_{clock})}$

b. $t_{phase\ error\ 23} = t_{PLH23} - \frac{1}{2 \times (2f_{clock})}$

c. $t_{phase\ error\ 24} = t_{PLH24} - \frac{1}{2 \times (2f_{clock})}$

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

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Clock Distribution In High-Performance PCs

A.R. Austin
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TEXAS INSTRUMENTS

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Contents

Introduction

Personal computer and workstation designers are pushing the operating speeds of new equipment to ever-higher frequencies with technological advances in areas such as RISC/CISC microprocessors, high-speed SRAMs, and cache memories. At higher frequencies, the timing delays and uncertainties associated with clock signal generation and distribution in a system become critical factors in determining the system's overall performance and reliability. System performance is optimized by carefully considering the attributes of the components used in designing the clock circuit. The clocking network is the heart of any system. There are two main aspects to this network: clock generation and clock distribution. Clock generation is accomplished by taking the output of some source (a crystal oscillator, for example) and manipulating it to obtain pulses with a specific frequency, duty cycle, and amplitude. These signals are then fanned out to the various system components by a clock-distribution network. As system speeds rise to 33, 40, or 50 MHz and clock periods grow shorter, the uncertainties of meeting setup, hold, and pulse duration requirements become critical due to a narrowing time window. A clocking system that does not fully consider these uncertainties will suffer degraded performance and reliability.

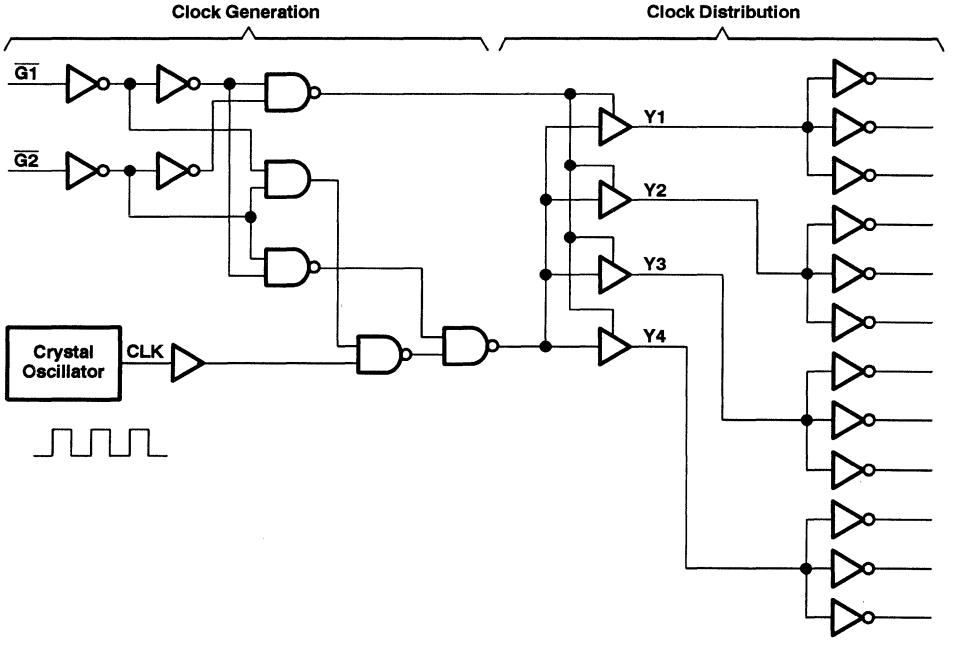


Figure 1. Clock Network

Texas Instruments, as well as several of the other major integrated-circuit (IC) vendors, offers the designer a choice of clock generation and distribution circuits commonly referred to as clock drivers. Clock driver ICs are able to provide clock generation functions (frequency multiplication, division, and duty-cycle control) as well as clock-distribution functions (buffering and fanout) with timing specifications unavailable on older CMOS and TTL logic families. Advances in process technology have allowed IC vendors to offer circuits with tight specifications on switching speeds and skew parameters. The high speed, fast edge rates, and tight skew specs offered on clock driver data sheets give the designer additional flexibility, but component selections must be closely tied to proper board layout techniques. The purpose of this application report is to discuss considerations in the design of clocking networks for high-performance systems wherein proper clock generation and distribution are essential.

What Is Skew?

Any discussion of clock-driver attributes ultimately centers around skew. Simply defined, skew is the difference between the expected and actual arrival time of a clock pulse. In an ideal clock circuit, propagation delays remain fixed and equal for high-to-low and low-to-high transitions over the entire ranges of supply voltage, operating temperature, and output loading and are independent of the number of outputs switching. However, the world is not ideal, and definitions have evolved to help the designer deal with the various types of skew that can be encountered. Clock-driver performance can be described in terms of five types of skew as defined in JEDEC Standard 99, clause 2.3.5 (refer to Figure 3).

Output Skew

Output skew, $t_{sk(o)}$, is the difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

Input Skew

Input skew, $t_{sk(i)}$, is the difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(i)}$ describes the ability of the gate to shape the pulse to the same duration regardless of the input used as the controlling input.

Pulse Skew

Pulse skew, $t_{sk(p)}$, is the difference between propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. $t_{sk(p)}$ quantifies the duty-cycle characteristic of a clock driver. Certain applications require a fixed duty cycle for proper operation. As an example, the CLK2 input of an MC68020 processor operating at 40 MHz requires a duty cycle of 50 ± 5%. $t_{sk(p)}$ is a measure of a clock driver's ability to supply such a precisely controlled pulse.

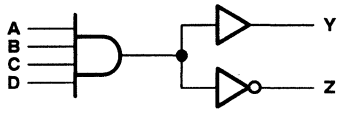


Figure 2. Example of a Gate With Input Skew

Process Skew

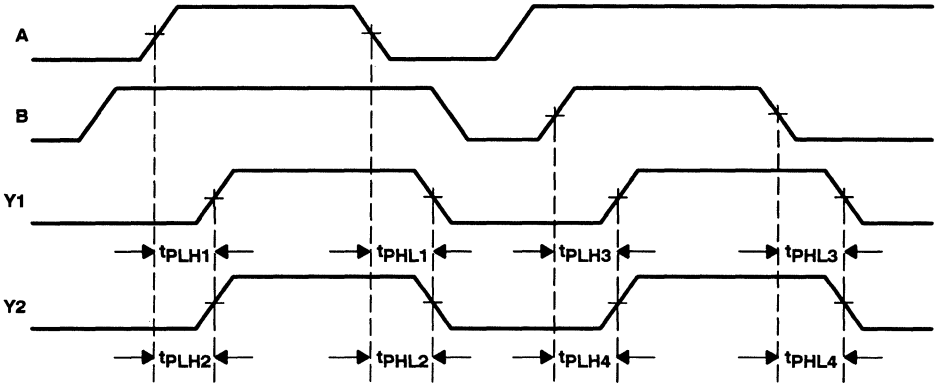
Process skew, $t_{sk(pr)}$, is the difference between identically specified propagation delay times on any two like ICs operating under identical conditions. $t_{sk(pr)}$ quantifies the skew induced by variations in the IC manufacturing process but not by variations in supply voltage, operating temperature, output loading, input edge rate, input frequency, etc. Process skew is commonly specified and production tested under fixed conditions (e.g., V_{CC} = 5.25 V, T_A = 70°C, C_L = 50 pF, all inputs switching simultaneously).

Limit Skew

Limit skew, $t_{sk(l)}$, is the difference between 1) the greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device but rather is calculated from the data sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time will be induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, tsk(l) also accounts for process variation. In fact, all other skew specifications [$t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$] are subsets of $t_{sk(l)}$; they will never be greater than $t_{sk(l)}$.

In general, not all skew parameters are of interest on a device, but their discussion is included for illustration. The designer's goal is to minimize skew to an acceptably small fraction of the system clock period. A design rule of thumb is that clock skew should be less than 10% of the system clock period.

The desired operating frequency determines the designer's *skew budget*, or the maximum amount of skew allowed. For example, a system operating at 33 MHz has a period of 30.3 ns, and the allowable skew budget is 3 ns using the 10% rule. At 50 MHz, the period is reduced to 20 ns and the permissible skew is now a scant 2 ns. Components in the clock network must be carefully selected in order to meet the shrinking skew budget as operating frequencies increase.



$t_{sk(o)}$ is calculated from the following expressions:
$|t_{PLH1} - t_{PLH2}|$
$|t_{PHL1} - t_{PHL2}|$
$|t_{PLH3} - t_{PLH4}|$
$|t_{PHL3} - t_{PHL4}|$

$t_{sk(l)}$ is calculated from the following expressions:
$|t_{PLH1} - t_{PLH3}|$
$|t_{PHL1} - t_{PHL3}|$
$|t_{PLH2} - t_{PLH4}|$
$|t_{PHL2} - t_{PHL4}|$

$t_{sk(p)}$ is calculated from the following expressions:
$|t_{PLH1} - t_{PLH1}|$
$|t_{PLH2} - t_{PHL2}|$
$|t_{PLH3} - t_{PHL3}|$
$|t_{PLH4} - t_{PHL4}|$

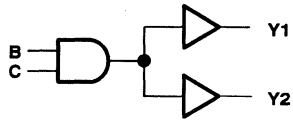


Figure 3. Skew Definitions

Power Dissipation

Power consumption becomes an important consideration as operating frequencies rise but is often overlooked as a designer tackles other issues. A much-touted aspect of devices fabricated in CMOS and BiCMOS technologies is low power consumption, especially when compared to equivalent devices fabricated in a purely bipolar process. At lower frequencies, this generalization holds true but power consumption at higher frequencies becomes less a function of process technology and more a function of output loading. To illustrate this point, the dynamic power (P_d) consumed by a CMOS device will be examined. The dynamic power consumed consists of two components:

1. Power used by the device as it switches states
2. Power required to charge any load capacitance

P_d is easily calculated using the following expression:

$$P_d = [C_{pd} \times V_{CC}^2 \times f_i] + n[C_L \times V_{CC}^2 \times f_o]$$

Where:

C_{pd} = power dissipation capacitance of the device as specified on the data sheet
f_i = input switching frequency
f_o = output switching frequency
C_L = load capacitance on each output
n = the number of outputs switching

This example assumes all outputs are equally loaded. Power consumed by the device switching logic states occurs because fabricated transistors on a chip are not ideal. Parasitic capacitances are present, and they must be charged and discharged. C_{pd} quantifies the magnitude of these parasitic capacitances and is in the range of 24–30 pF for clock-driver devices fabricated using Texas Instruments EPIC™ Advanced CMOS process. Power needed to charge the load capacitance, C_L, makes up the second half of the equation. The designer has some control over C_L, while C_{pd} is strictly a property of the device chosen. Power consumed by both is a direct function of the frequency at which the system operates and is usually fixed by the processor speed. The designer's goal is to reduce and evenly distribute the load that a device must drive. The SPICE data shown in Figure 4 for the CDC337 clock driver graphically illustrates the power-consumption tradeoffs that can be made between switching frequency and output loading.

The CDC337 is fabricated in Texas Instruments EPIC-IIB™ BiCMOS process and contains four buffered outputs that switch at the clock frequency and four divide-by-two outputs that toggle at one-half the clock frequency. It is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. Power consumption also has implications for packaging at both the component and system levels. The general trend is that the system box shrinks with each advance in performance. This in turn requires smaller power supplies, closer board-to-board spacing, and reduced capacity for free air flow, all of which are not compatible with power-hungry designs. Increased system packaging density usually requires the use of surface-mount components that do not have the higher heat dissipation properties of larger DIP devices but do allow closer board-to-board spacing and component placement on both sides of the circuit board. All of these factors can drive up system operating temperature and cost. Power consumption can make or break a system design and should not be treated lightly.

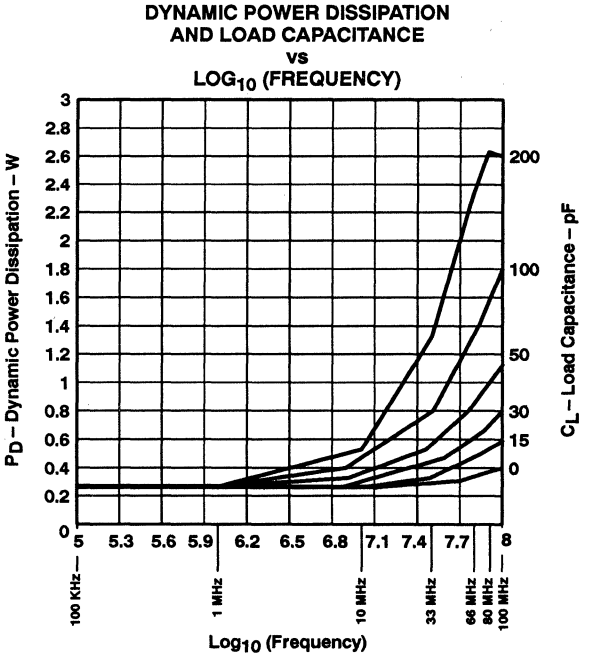


Figure 4. CDC337 Power Dissipation

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High-Speed Design Considerations

A number of tightly specified, high-speed, high-drive clock-driver circuits are available to aid the designer in developing a system-clocking network. By carefully following established high-speed circuit design techniques, the designer can achieve superior performance from standard components and not incur the high cost of custom components. Transmission line effects take over in high-speed, high-drive designs, and attention to detail during board layout is critical. A sound high-speed design uses all of the following techniques and rules of thumb:

Keep output loading as light as possible. This reduces power consumption, allows switching at higher frequencies, and reduces skew.

Equally load all outputs where possible

Use short, equal-length etch runs

Avoid sharp corners that may induce unwanted reflections, ringing, and overshoot due to discontinuities

Properly decouple all device V_{CC} pins as close to the pins as possible. The best high-frequency filtering is often accomplished with a combination of capacitors. An effective combination is 0.1 μF in parallel with 0.01 μF or 0.005 μF. Use RF-quality (low-inductance) capacitors.

Use a multilayer board with low-impedance power and ground planes to minimize circuit noise

Select components with low noise characteristics. Components optimized for low noise usually have multiple V_{CC} and GND pins interspersed among the device outputs to help reduce noise.

Summary

High-performance systems demand a carefully designed clock-generation and distribution network. The designer has the challenge of outlining a design that meets tighter timing, lower power consumption, smaller space, lower operating temperature, and lower cost requirements. Timing performance is optimized by reducing clock skew. Skew can be minimized by selecting components optimized for low-skew applications and by tightening power-supply requirements to ± 5% instead of ± 10%. Power consumption is largely a function of operating frequency but can be reduced by making output loading as light as possible. The use of surface-mount components saves board and system box space but requires analyzing tradeoffs in power consumption, air flow, and operating temperature. High-performance, low-cost clock-driver components are now available that can help the designer with this performance juggling.

Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs

Stevan Plote
Advanced System Logic – Semiconductor Group

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Introduction

Today, system clock frequencies continue to increase; we are now approaching the 50–100-MHz range. The clock period with which systems designers must work is shrinking, as is the tolerance for high propagation delays (t_{pd}) and high output skew ($t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$) in clock-distribution systems:

$t_{sk(o)}$ is output-to-output skew in the same device.

$t_{sk(p)}$ is the difference between the low-to-high and high-to-low transition for a given output terminal:

$$t_{sk(p)} = |t_{PHL} - t_{PLH}|$$

$t_{sk(pr)}$/$t_{sk(pv)}$ is process skew or part-to-part skew and is a measure of the difference between the minimum low-to-high or high-to -low transition and the maximum high-to-low or low-to-high transition on the same terminal of two different clock drivers under the same operating conditions:

$$t_{sk(pv)} = |\min t_{pd}\ \text{LH (device 1)} - \max t_{pd}\ \text{HL (device 2)}|$$

Some manufacturers specify this parameter as:

$$t_{sk(pv)} = |\min t_{pd}\ \text{LH (device 1)} - \max t_{pd}\ \text{LH (device 2)}|$$

This is a less-stringent specification.

Table 1. Clock-Driver Timing Requirements

	SYSTEM CLOCK		
	50 MHz	66 MHz	100 MHz
Clock cycle time, t_c†	20 ns	15 ns	10 ns
Clock pulse duration, t_w‡	10 ns	7.5 ns	5 ns

† Clock cycle time ≥ 1/system clock frequency
‡ Assumes a 50% duty cycle

These timing requirements imply that the t_{PLH} and t_{PHL} through the clock buffer and the maximum allowable output skews $t_{sk(o)}$ and $t_{sk(pr)}$ in a given system need to be less than or equal to the clock-pulse duration to not violate system timing specifications:

$$|t_{PLH} + t_{PHL} + t_{sk(o)} + t_{sk(pr)}|$$

Maximum allowable $t_{sk(o)}$ for a 50% duty-cycle clock system is 10% of the clock cycle time. This is an estimate.

None of the very fastest gate- and buffer-based clock-distribution devices can meet this timing. A system designer must therefore turn to a PLL-based clock driver as shown in Figure 1.

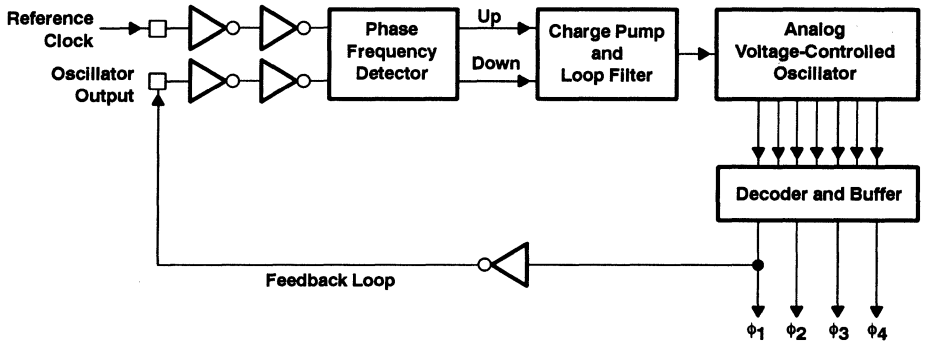

Figure 1. Block Diagram of a Clock Generator Based on a Charge-Pump PLL

The beauty of phase-lock loops is that they receive an input signal, compare this to the feedback of their internal clock generated by a voltage-controlled oscillator (VCO), and adjust the VCO by way of the charge pump to match the new input frequency and synchronize the internal and external clocks.

In Figure 1, the analog VCO is either a ring-oscillator type or a multivibrator type. The VCO can also be designed using a multistage tapped delay line that is calibrated to a precise delay per stage (a digital approach). The charge-pump design has various approaches using inverters, switches, and a passive RC low-pass filter. The phase detector is the second most important element (see Figure 2). The input from the external clock enters the phase detector, which is a set of balancing buffers and highly balanced D-type flip-flops. The phase detector must always be active. This clock input is compared to the feedback input D from the VCO.

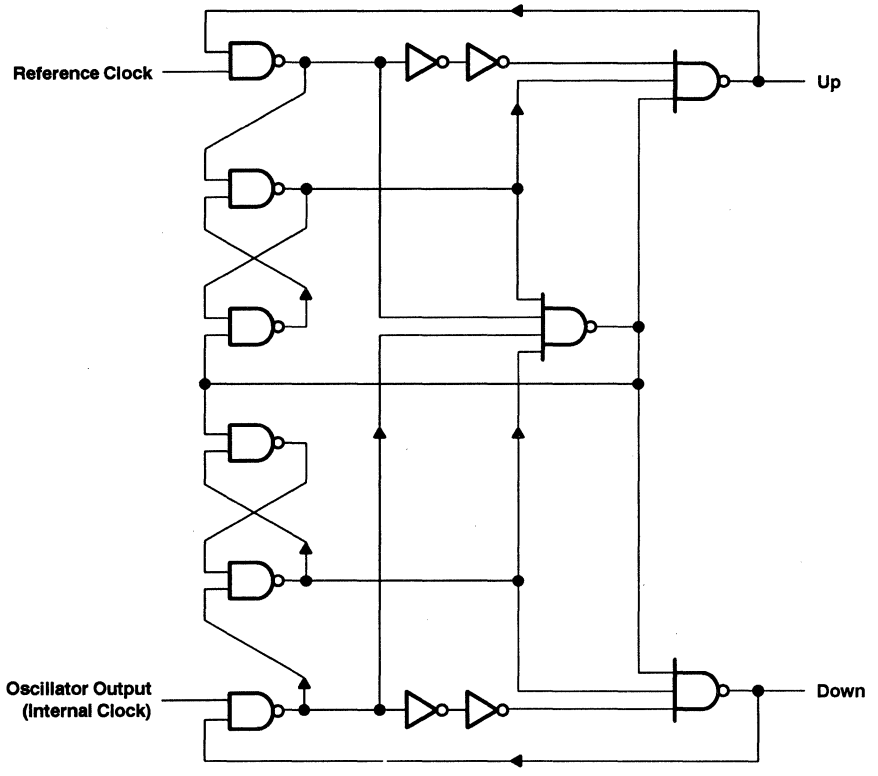

Figure 2. Phase-Detector Block

If the D input to the flip-flop is high before the rising edge of the clock, then D is phase advanced, the voltage to the VCO is reduced via the charge pump, and the internal clock is slowed.

If the D input to the flip-flop is low before the rising edge of the clock, then D is phase retarded and the voltage to the VCO is increased through the charge pump to speed up the VCO.

This process is repeated with every external input-clock pulse so that the feedback clock and the external clock are synchronized; the circuit then locks onto itself within a narrow frequency band. If the input clock slightly varies (within that frequency band), the PLL frequency does not vary. This narrow frequency band is known as the *dead zone* of the phase detector. Within this zone, the feedback clock and the external clock are so close in phase that there are no correction pulses out of the phase-detector circuit. Once the phase drifts out of this frequency band, the phase detector starts correcting again.

Circuit designers have tried to design nondead zone phase detectors such that the phase detector is always active and correcting. This, however, is very difficult to implement due to t_{jitter}, an important specification that results from the phase-detector circuit and noise in the VCO:

t_{jitter} of the phase detector = dead zone + correction pulse

The phase detector must be very accurate and balanced to reduce the dead zone and keep the correction pulses small. The design result is a more analog than digital implementation.

The phase-lock loop locks in a very short time (less than 50 ms). In fact, after lock, many PLL-based clock drivers are termed *zero delay*. The reality is that most have a t_{pd} of ±1 ns from the input frequencies. Comparing this to the 3- to 12-ns t_{pd} of other gate-based or divider clock drivers, there is a great advantage to a high-performance system designer in using a PLL-based clock driver.

Another feature of a PLL is the skew control of the device. Since the input signal is locked onto and regenerated at the output of the device, the variation of the signal from output to output is no longer a function of the chip layout and process as it is in gate- and flip-flop-based devices. PLL designs achieve maximum output skew [$t_{sk(o)}$] of 500 ps or less and process skew [$t_{sk(pr)}$] of < 1 ns; very important features from the designer's point of view.

Two other aspects of a PLL design allow for additional functionality. One of these is external feedback (not all PLL devices have this). This allows a designer to use an external gate- or flip-flop-based clock driver to drive multiple loads off of one PLL output. The PLL output drives the input of the external clock driver and, by feeding one output of that external buffer back into the PLL-based clock driver through the feedback terminal, one can synchronize the remaining PLL outputs with the remaining external buffer outputs and the input clock to the PLL-based clock driver. The other aspect is output jitter (t_{jitter}). Jitter occurs when a signal deviates in phase or frequency from that of an ideal clock. This shows up as noise on the outputs of the device. When a PLL locks into the input frequency, there is a limited variation of that signal at the outputs. This provides for good, low t_{jitter} specifications both on individual outputs and the entire device.

Multiple-board systems derive a huge benefit from this feature. A designer can use a master PLL based on a motherboard and synchronize the other boards in the system by driving the oscillator signal through the master PLL and out through the backplane, than recovering it on each of the boards via a PLL-based clock driver on each of the system boards. This works best because the master PLL has the lowest signal loss/output skew and can have high-drive outputs. Each system board is then synchronized to the master clock, and each board individually drives the clock via its own clock driver. This application also works best when the oscillator signal is divided down, driven across the backplane, and multiplied back up through the clock recovery PLLs to the system operating frequency desired across all of the boards. By reducing the clock frequency driven across the backplane, the level of extraneous noise in the signal is also reduced.

The main drawback to the PLL-based clock driver is cost. Due to the complexity of the circuitry and speeds at which the VCO needs to run, PLLs are expensive. In general, a PLL-based clock diver costs two to five times the price of a gate-based clock driver. This price is based upon the value of the product. If the accuracy and speed of the PLL is not needed, other solutions can be used.

Other disadvantages of PLLs are:

1. They are inherently very noise sensitive.
2. They are untestable by the end user, but can have the VCO bypassed in a system to allow examination of other parts of the device circuitry (mainly inputs) during debug stages of board-level design.
3. Some PLLs can require expensive, high-quality external components to implement the loop-filter design.
4. The external loop filter may have to be modified from part to part due to processing variations in a vendor's PLL silicon.
5. t_{jitter} can also occur due to substrate conditions. Isolation of key components such as the VCO and charge pump from the outputs and on-chip digital circuitry can reduce t_{jitter}. t_{jitter} is also increased if an external feedback terminal is implemented in the design along with the reference clock terminal. If the feedback terminals is tied to a separate V_{CC} and ground from the analog circuitry, it can increase jitter via shifting rail and ground levels between the feedback and the analog VCO and reference input. This can be combatted by tying the feedback terminals/clock input/ VCO/charge pump to the same V_{CC} and ground.

Texas Instruments has developed a group of three low-voltage, high-performance, PLL-based clock drivers. These devices are targeted at the high-performance (50 MHz–100 MHz), 3.3-V power-supply markets for RISC processors, Intel Pentium™ microprocessors, and synchronous DRAMs.

Each of these markets require multiple outputs, twelve on each device, and a way to configure the device outputs to be one half the input frequency, two times the input frequency, and the same frequency at the input frequency. Some of the devices also incorporate dampening resistors on the outputs to reduce reflections caused by transmission-line effects and increase the integrity of the signal at the load.

The TI devices incorporate a five-stage ring oscillator VCO, and internal loop filter, and an external feedback terminal (which allows for doubling the input-clock frequency at the outputs). The VCO, charge pump, reference-clock input, and feedback terminal are all tied to the same V_{CC} and GND and fully isolated from the remaining on-chip logic and outputs of the device.

This design is inherently stable and exhibits low t_{jitter} on each of its outputs. Measured t_{jitter} in spice simulation is 48 ps or less with a typical number of 23 ps.

The CDC2582, CDC2586, and CDC586 are very competitive solutions for the telecommunications, workstation, and PC-equipment clock distribution requirements.

Acknowledgements

Tim Ten Eyck for suggestions and design work.
Brett Clark for his dedicated lab work.
Craig Spurlin for his design work.

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Minimizing Output Skew Using Ganged Outputs

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Introduction

The purpose of this application report is to help designers use existing clock-driver products to drive large loads and maintain a minimum amount of skew between outputs of the device. The emphasis of this report will be on using parallel, or ganged, outputs to drive loads.

Skew Definitions

Output Skew – $t_{sk(o)}$

Output skew is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs. This parameter is useful when considering the distribution of a clock signal to multiple targets.

Pulse Skew – $t_{sk(p)}$

Pulse skew is defined as the difference between the propagation delay times t_{PLH} and t_{PHL} on the same pin at identical operating conditions. This parameter is useful when considering the output duty cycle characteristics of a device.

Process Skew – $t_{sk(pr)}$

Process skew is defined as the difference between propagation delay times on any two samples of an integrated circuit at identical operating conditions. This parameter addresses the difference in propagation delay times due to process variations.

Board Skew

Board skew is introduced into the clock system by unequal trace lengths and loads. It is independent of the skew generated by the clock driver. It is important to keep line lengths equal to minimize board skew.

When measuring propagation delays to determine the parameters $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$, the device(s) must be tested under identical operating conditions such as temperature, power supply voltage (V_{CC}), output loading, and input edge rates.

Ganged Outputs

As system frequencies increase, the need to minimize skews of clock drivers becomes critical to overall system performance. Existing non-PLL-based clock driver products deliver guaranteed output skews ($t_{sk(o)}$) in the 500-ps to 1-ns range. It is possible to use these low-skew clock drivers in a way that eliminates the output skew of the device. This can be achieved by using parallel, or ganged, outputs. Two or more outputs ganged (connected to a single transmission line) create a single clock source for all the target devices. Output skew of the clock driver is eliminated, and the drive capability is increased.

Performance Evaluation

To evaluate the impact of connecting all the outputs of a device to a single transmission line, a test board with traces of equal length to and from the inputs and outputs of the device was constructed. Using traces of equal length prevents board skew from being introduced into the system.

Various tests were performed on the CDC209 and CDC208 to evaluate their changes in performance when one output was used to drive a load versus four or eight ganged outputs. The dc-drive capability increases as more outputs are used to drive the load. Figures 1 and 2 show V_{OH}/I_{OH} and V_{OL}/I_{OL} curves displaying the difference between one, four, and eight outputs.

CDC209
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

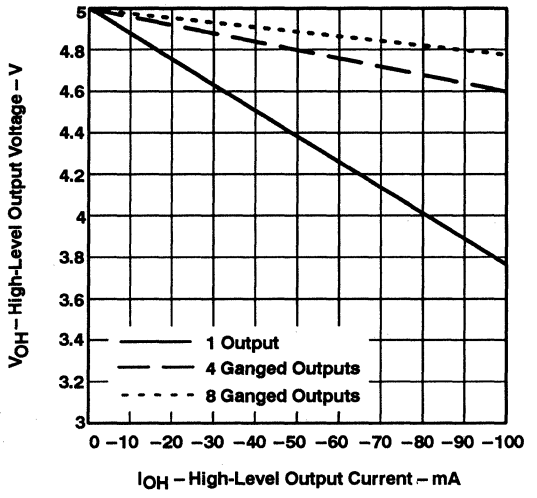


Figure 1

CDC209
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

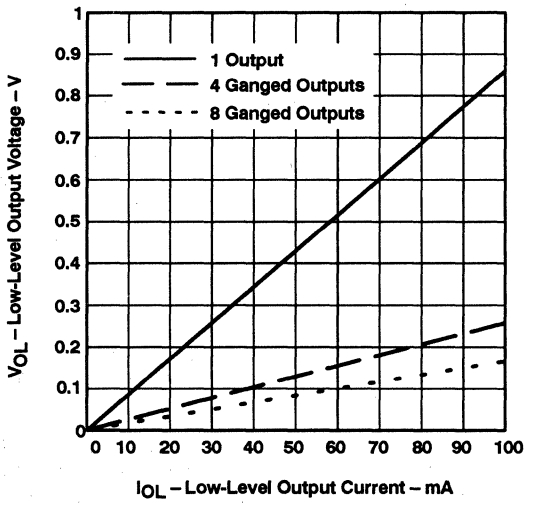


Figure 2

Figure 3 shows the difference in supply current versus operating frequency for four and eight ganged outputs.

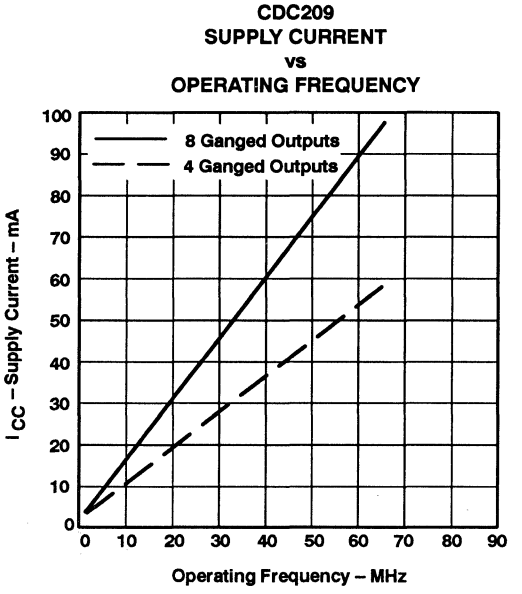


Figure 3

Figures 4 and 5 show the difference in t_{PLH} and t_{PHL} versus capacitive loading for one, four, and eight ganged outputs.

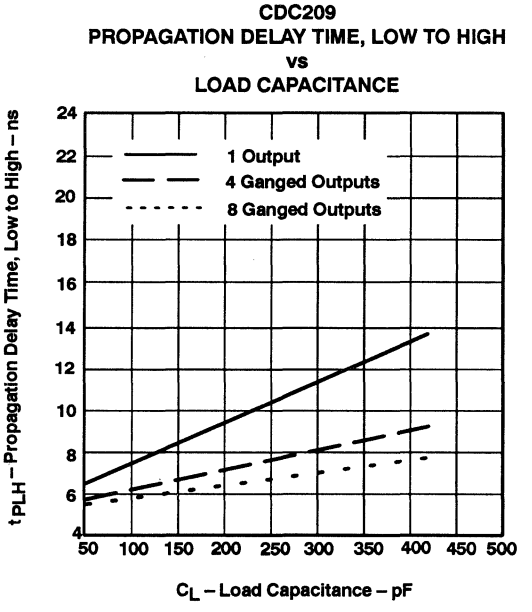


Figure 4

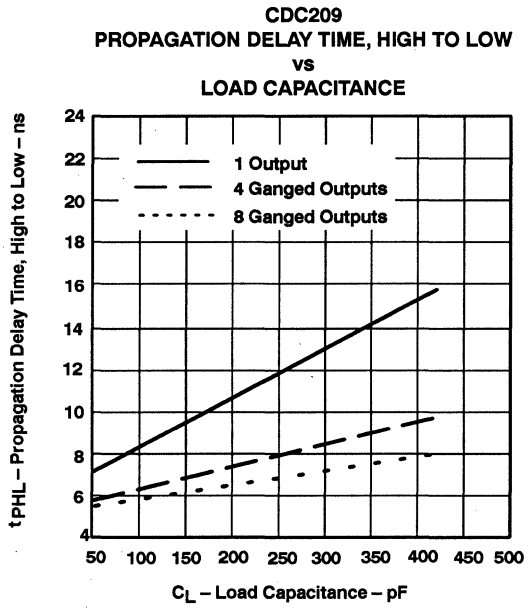


Figure 5

Figure 6 shows the difference in output waveforms of a CDC209 for one, four, and eight ganged outputs driving a 470-pF load in parallel with 500 Ω.

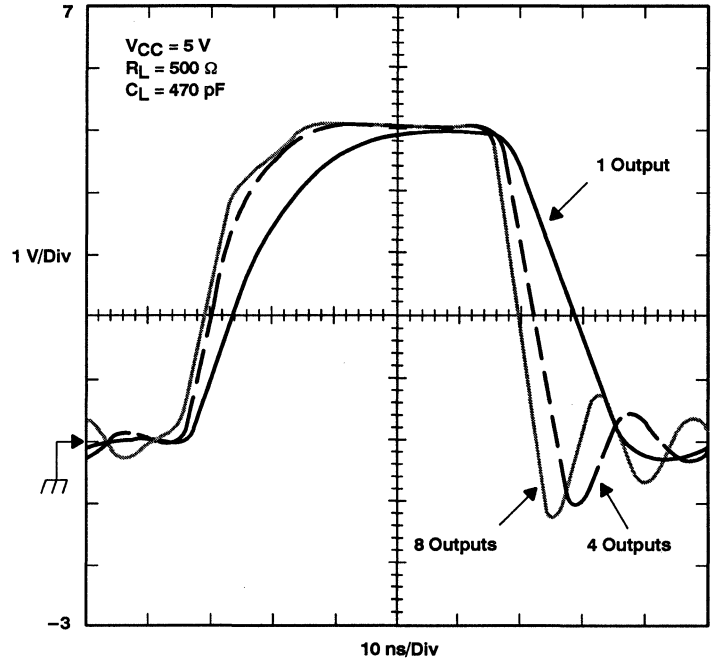
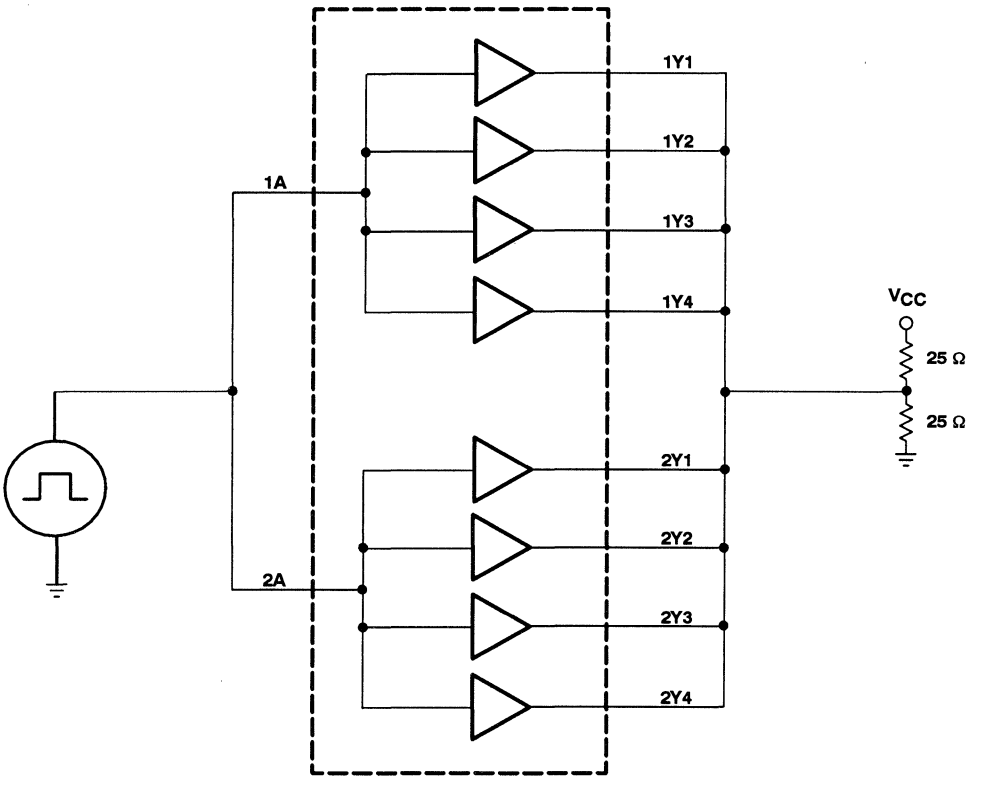


Figure 6. CDC209 Output Waveforms

Reliability

A life test of 1000 hours was also performed on 52 devices using the circuit shown in Figure 7. No failures were observed.



NOTES: A. Life test conditions: V_{CC} = 7 V, T_A = 150°C, input frequency = 10 MHz
B. It is very important to keep all of the input and output transmission lines equal length to prevent skew from being introduced.

Figure 7. Test Circuit

Applications

One application for ganged outputs is a backplane or bus on a motherboard. A backplane usually requires a single system clock capable of driving multiple plug-in boards. Ganged outputs are very effective at driving capacitive loads distributed along a single transmission line.

Great care must be taken when connecting more than one output to a single transmission line. The length and impedance of the transmission lines from each output to the point of intersection must be matched. The same attention must be given to the input traces if the outputs are driven from multiple inputs. If the lengths and impedances are not matched, a shelf may be visible in the output waveform.

EMI Prevention in Clock-Distribution Circuits

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Texas Instruments Incorporated – Japan

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Introduction

Although the importance of electromagnetic interference (EMI) has been recognized, most system designers have tended to handle the problem by shielding via metal cabinets or through RC networks to limit the rise and fall times of digital pulse waveforms. These design practices were motivated by 1) a lack of EMI-prevention design rules and by 2) designers' tendencies to prioritize apparent system performance only to have that performance subsequently degraded through the later addition to the system of EMI-prevention devices such as metal chassis or RC networks.

With the current trend towards lighter, more compact personal computers and engineering workstations, system designers can no longer rely upon after-the-fact EMI shielding techniques; rather, they must learn to build in EMI protection at the design stage. This application report discusses EMI protection for a clock distributor, an application characterized by multiple simultaneously switching bits and relatively long transmission lines.

Higher-Harmonic Components of Digital Waveforms

In general, the decay rate of a Fourier-spectrum envelope is greater for a waveform with slow rise and fall times than for a waveform with fast rise and fall times. Figures 1 and 2 show a triangular waveform and its spectrum envelope. The 12 dB/octave decay rate shown in Figure 2 means that if two x-axis values of 1X frequency and 2X frequency are considered, the corresponding y-axis values are 1X and 1/4X amplitude, respectively.

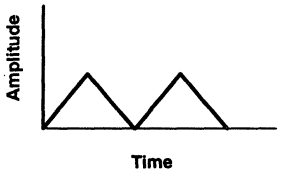


Figure 1. Triangle Wave

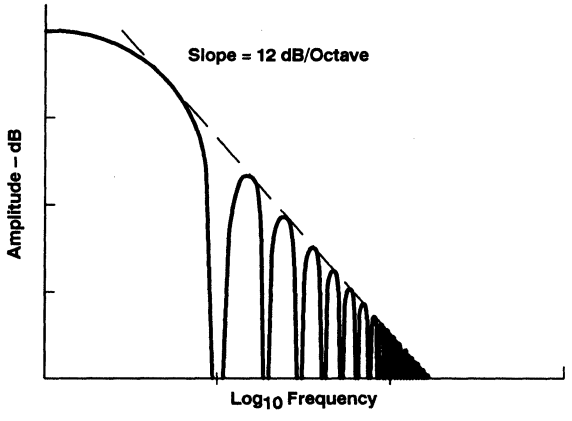


Figure 2. Spectrum Envelope for Triangle Wave of Figure 1

Figures 3 and 4 show an ideal square waveform (0-ns rise and fall times) and its spectrum envelope. Comparing 1X frequency and 2X frequency x-axis values, the corresponding y-axis values are 1X and 1/2X, respectively.

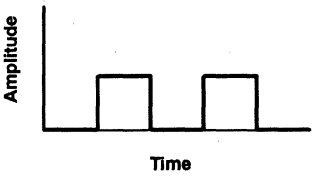


Figure 3. Square Wave

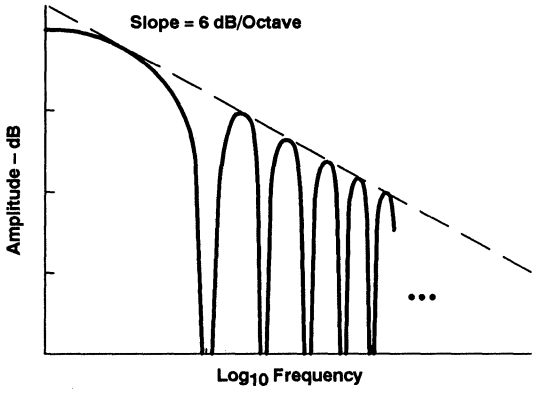


Figure 4. Spectrum Envelope for Square Wave Shown in Figure 3

By comparing Figures 1 and 2 with Figures 3 and 4, it is evident that the ideal square wave, with its sharp discontinuities (0-ns rise and fall times), contains many more higher harmonics than does the triangle wave. Hence, an electronic circuit stimulated by an ideal square wave would require employment of more EMI-protection design techniques than a circuit stimulated by a triangle wave of the form shown in Figure 1.

In real digital-circuit applications, square waves are not ideal but instead have finite rise and fall times. Although the decay rate of the spectrum envelope for a real square wave will be greater than the 6 dB/octave rate of the ideal square-wave spectrum envelope, its decay rate will still be small enough to cause EMI problems. The spectrum-envelope decay rate for a square wave is also dependent on its pulse duration, as shorter pulse durations equate to frequency spectra exhibiting higher amplitudes at higher frequencies. In comparing Figures 5 and 6 (time and frequency plots for a 50% duty-cycle square wave) with Figures 7 and 8 (time and frequency plots for a less-than-50% duty-cycle square wave), the following may be observed:

- The amplitude-vs-frequency plot remains flat up to a frequency equal to the inverse of the pulse duration, or $1/t_w$. This first node in the frequency plot occurs at a higher frequency for the less-than-50% duty-cycle waveform than for the 50% duty-cycle waveform.
- Beyond this first node in the frequency plot, both frequency plots have spectrum envelopes that decay at the 6 dB/octave rate.

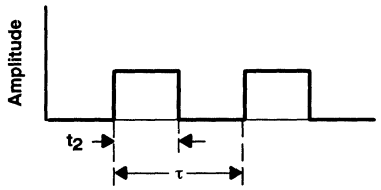


Figure 5. Square Wave, Duty Cycle = 50%

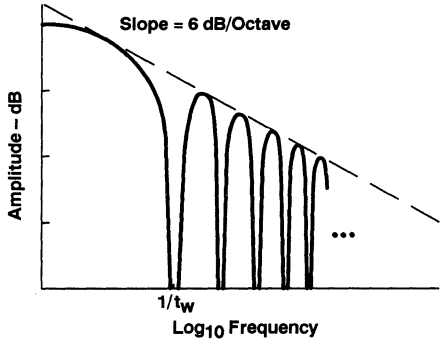


Figure 6. Spectrum Envelope for Square Wave Shown in Figure 5

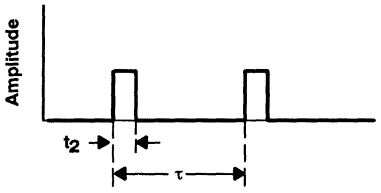


Figure 7. Square Wave, Duty Cycle < 50%

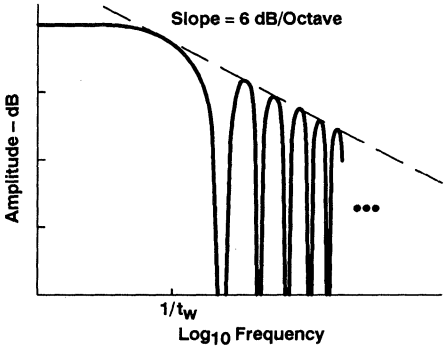
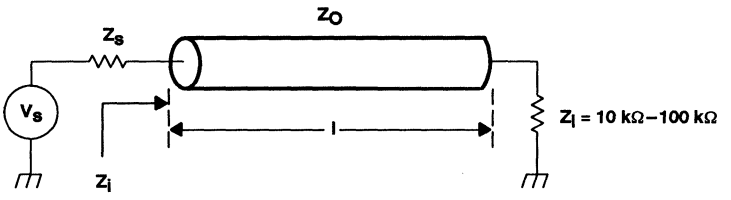


Figure 8. Spectrum Envelope for Square Wave Shown in Figure 7

Transmission Line and Radiated Emissions

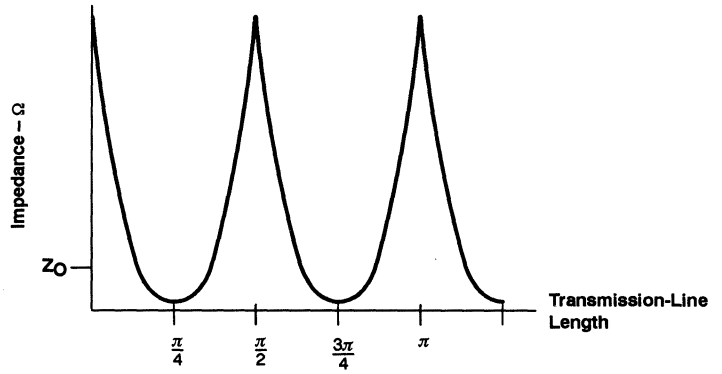
The transmission lines connected to clock drivers or bus drivers are often relatively long. When transient currents flow on such transmission lines, the transmission lines act as efficient antennae, radiating high-frequency electromagnetic waves. If such a transmission line is unterminated, its radiated spectrum shows maximum peak voltage.

In the transmission line shown in Figure 9, the input impedance of the receiver is high (10 kΩ to 100 kΩ) relative to the transmission-line characteristic impedance (Z_O). The transmission-line input impedance versus length can be represented by a cotangent function. For a particular signal frequency, the transmission-line input impedance is at a minimum when the transmission-line length is an odd multiple of 1/4 of the wavelength of the signal. When the frequency spectrum of the output waveform of the driver shown in Figure 9 contains such frequency components, current through the transmission line and radiated emissions from the transmission line are maximized.



$$Z_i = -jZ_o cot\left(\frac{2\pi l}{\pi}\right)$$

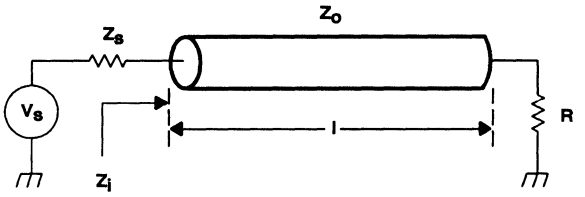
(a) MODEL OF TRANSMISSION LINE SHOWING HIGH INPUT IMPEDANCE OF RECEIVER



(b) PLOT OF TRANSMISSION-LINE INPUT IMPEDANCE VERSUS LENGTH

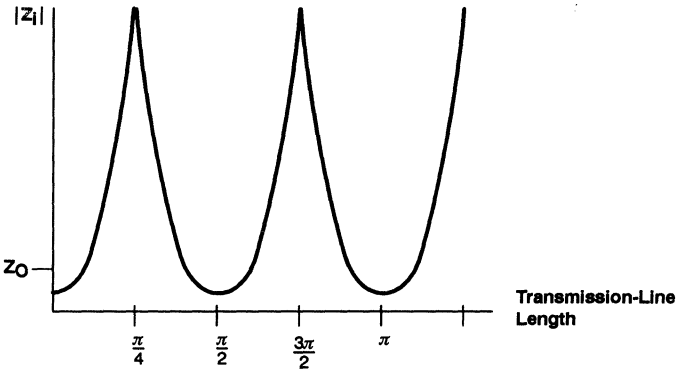
Figure 9. Transmission Line With a Driver and a Receiver

On the other hand, if the transmission line is terminated with less impedance than the transmission-line characteristic impedance (Z_O) (see Figure 10), the transmission-line input impedance versus length can be represented by a tangent function. For a particular signal frequency, the transmission-line input impedance is minimized when the transmission-line length is an integer multiple of 1/2 of the wavelength of the signal. Radiated emissions are maximized at these frequencies.



$$Z_i = -jZ_o \tan\left(\frac{2\pi l}{\pi}\right)$$

(a) MODEL OF TRANSMISSION LINE SHOWING TERMINATION RESISTOR R < Z_O

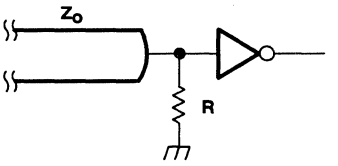


(b) PLOT OF TRANSMISSION-LINE INPUT IMPEDANCE VERSUS LENGTH

Figure 10. Transmission Line With a Termination Resistor Value Less Than Z_O

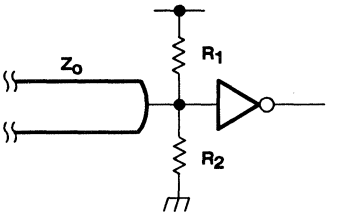
In summary, impedance mismatching causes a maximum current flow on the transmission line, thus maximizing radiated emissions. It is obviously desirable to assure impedance matching to minimize radiated emissions. There are two basic methods of assuring impedance matching: 1) termination at a line end point, and 2) termination at a line start point.

Terminating the end of a transmission line can be done either by use of a pulldown resistor (see Figure 11) or through parallel resistors (the so-called Thevenin's termination; see Figure 12). Termination at a transmission-line start point is done via a damping resistor (see Figure 13).



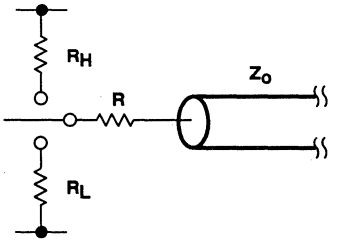
$$Z_o = R$$

Figure 11. Impedance Matching Through a Pulldown Resistor



$$Z_o = \frac{R_1 \times R_2}{R_1 + R_2}$$

Figure 12. Impedance Matching Through Parallel Resistors (Thevenin's Termination)



$$Z_o = \frac{R_H + R_L}{2} + R$$

Figure 13. Impedance Matching Through a Damping Resistor

For a clock-distribution circuit, in which transmission is restricted to a single direction, termination at the transmission-line start point (i.e., through a damping resistor) is recommended as this approach minimizes power consumption (albeit at the cost of a slight increase in the clock signal rise and fall times). In contrast, a Thevenin (end-of-transmission-line) termination is recommended for bus interface circuits wherein bidirectional signal flow is assumed.

The Antenna Effect

When relatively long transmission lines have a high characteristic impedance, they tend to mimic antennae, both receiving and radiating noise easily, so it is desirable to design transmission lines with as low a characteristic impedance as possible. When a multilayered printed-circuit board (PCB) is used, transmission lines can be laid out on an intermediate layer; the shielding effects of the V_{CC} and GND planes of the PCB will then suppress vertically polarized waves.

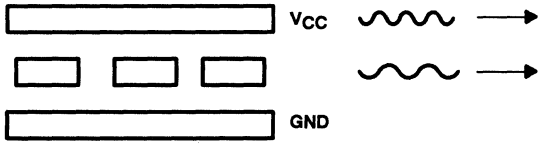
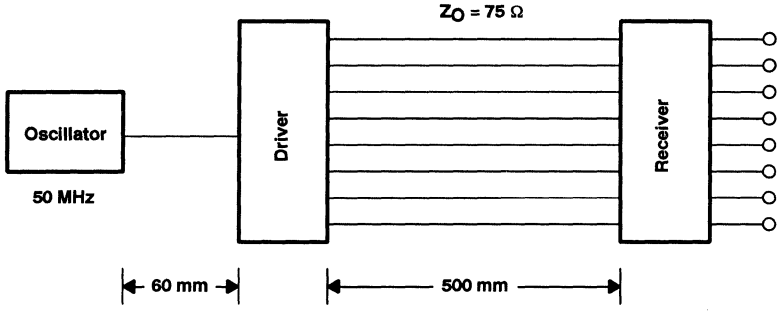


Figure 14. Antenna Effect of Transmission Lines

Spectrum Analyzer Results

Data from the test setup shown in Figure 15 was examined via a spectrum analyzer to determine which element of the test setup was most critical relative to radiated emissions (the oscillator, the shielded line, the driver, the transmission lines, or the receiver) and to observe the effects of line terminations. The data as plotted in Figure 16 showed that the oscillator exhibits a maximum value of 47dBμV/m at 150 MHz and that the oscillator has high shielding capability. Table 1 gives the mean and maximum values for the four plots in Figure 16. It is clear from Figure 16 that the transmission line is the most significant contributor to radiated emissions.



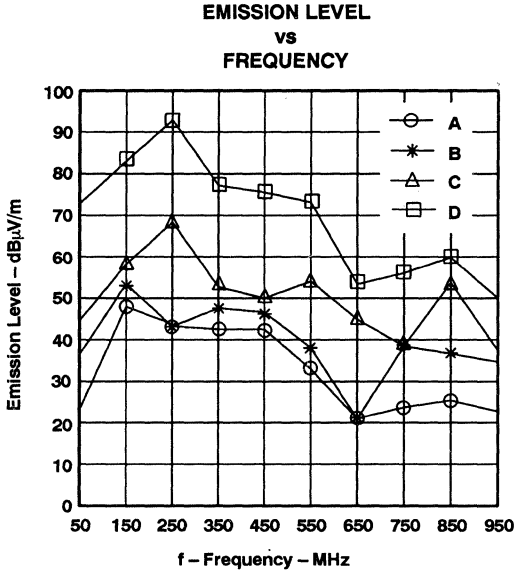
DRIVER	RECEIVER
CDC209	CDC204
CDC204	CDC204
CDC303	AS245
ABT240	ABT240

Figure 15. Block Diagram of Test Setup for Measuring Radiated Emissions

Table 1. Comparison of Radiated Emissions

	MEAN	MAX
A	33	47
B	38	54
C	49	68
D	67	93

Units: dBμV/m
Driver: CDC208
Receiver: CDC204



A = Oscillator
B = Oscillator + Shielded Line
C = Oscillator + Shielded Line + Driver
D = Oscillator + Shielded Line + Driver + Transmission Line + Receiver

Figure 16

Effects of Impedance Matching

Practically speaking, impedance matching is the easiest way to minimize radiated emissions. Figures 17 and 18 show test setups (transmitter = CDC208; receiver = CDC204) with unterminated transmission lines and with transmission lines terminated with 56-Ω damping resistors, respectively. The oscilloscope display for the transmitted waveform from the test setup of Figure 17 showed significant overshoot and undershoot due to signal reflections, and a spectrum analyzer showed a maximum value of 90 dBμV/m. In contrast, the transmitted waveform from the test setup of Figure 18 showed no overshoot and undershoot, and the amplitudes of higher-harmonic components were reduced.

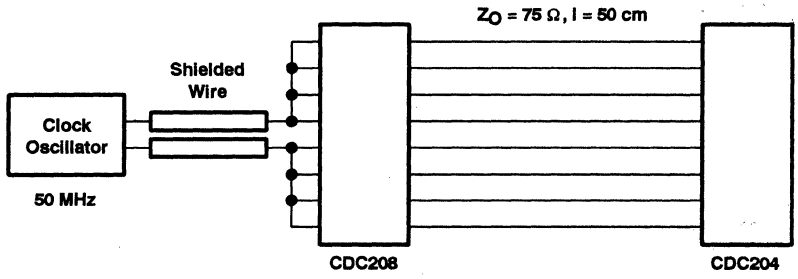


Figure 17. Test Setup With Unterminated Transmission Lines

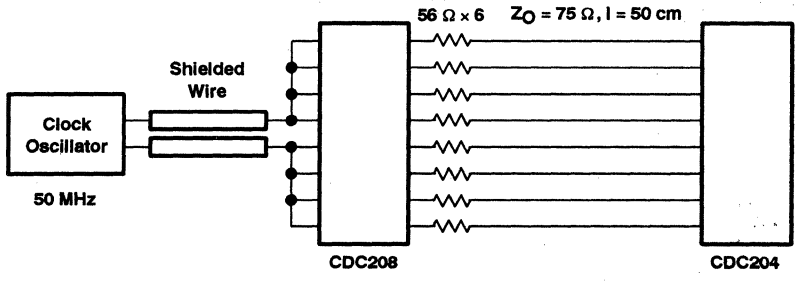


Figure 18. Test Setup With 56-Ω Damping-Resistor Terminations

Similar analyses were made using CDC204/CDC204 and ABT240/ABT240 transmitter/receiver pairs. The results for all three transmitter/receiver pairs for unterminated transmission lines are summarized in Table 2.

Table 2

INTERFACE	MIN	MAX
CDC208–CDC204	8.8	17
CDC204–CDC204	4.9	9.2
ABT240–ABT240	7.3	13

Units: dBμV/m
NOTE: MIN and MAX values at higher harmonics

In the case of transmission lines terminated with 56-Ω damping resistors, the data values in Table 2 could be expected to improve by 5 to 9 dBμV/m (means) and 9 to 17 dBμV/m (maximums).

Figures 19 through 22 show EMI evaluation results for CDC208, CDC204, ABT240, and CDC303 devices in both unterminated and damping-resistor-terminated configurations. The x-axis (frequency) values in these figures are odd higher harmonics for the given transmission lines. The radiated emission values in these figures are relatively high for the following reasons:

- The transmission lines were up to 500 mm in length.
- The transmission lines were laid out on a surface layer of the PCB.
- The PCBs were not shielded by metal cabinets.

Figures 19 through 22 clearly show that when signal reflections are controlled by impedance matching, the radiated emissions are reduced.

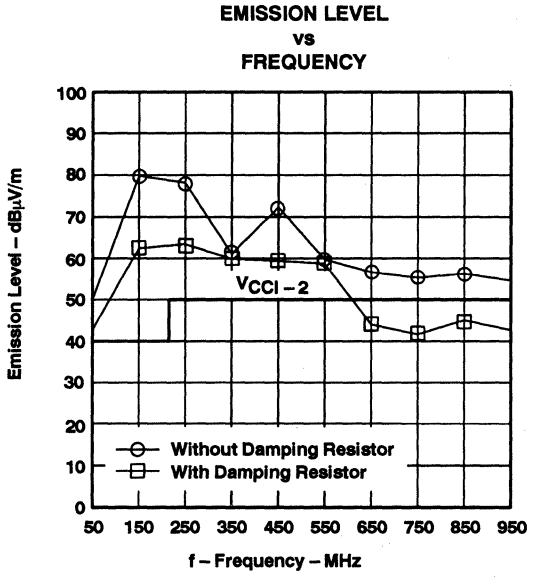


Figure 19. EMI Evaluation Results (Device Under Test = CDC208)

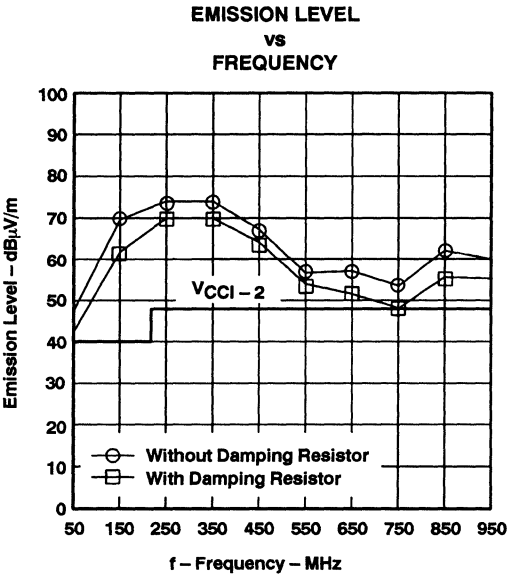


Figure 20. EMI Evaluation Results (Device Under Test = CDC204)

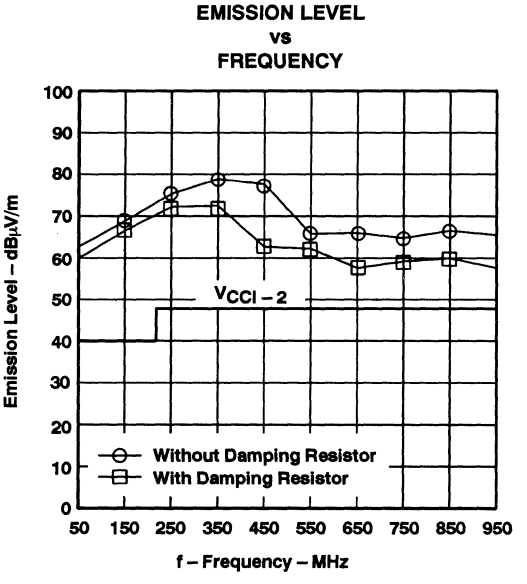


Figure 21. EMI Evaluation Results (Device Under Test = ABT240)

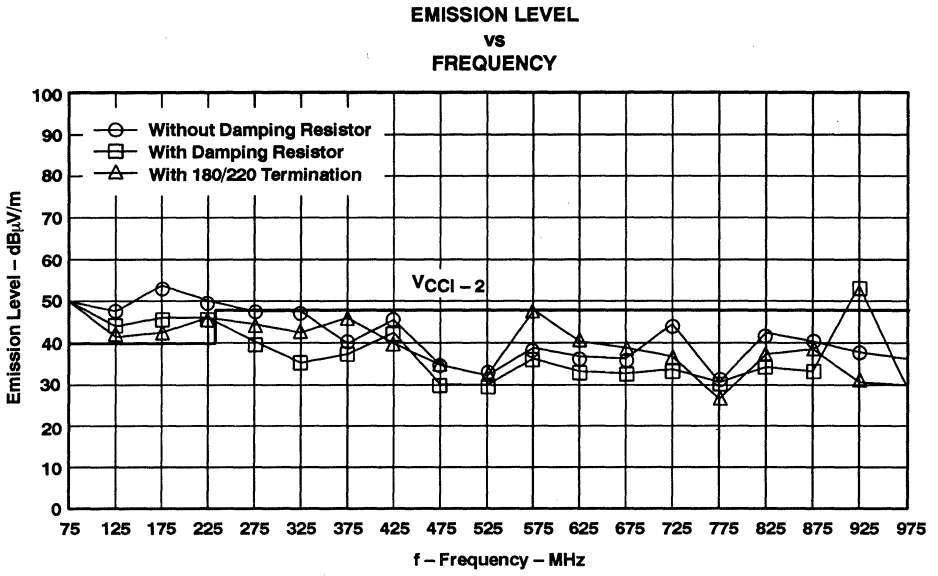


Figure 22. EMI Evaluation Results (Device Under Test = CDC303)

Summary of Methods for EMI Prevention

Characteristic Impedance of the Transmission Line

A transmission line should be designed with as low a characteristic impedance as possible to reduce the antenna effect. Long transmission lines such as those in clock-driver or bus-interface circuits should be laid out in intermediate PCB layers rather than surface layers (the characteristic impedance of intermediate-layer lines is on the order of 50 Ω, while surface-layer lines have 75-Ω characteristic impedances).

PCB Shielding Effects

Laying out transmission lines between PCB V_{CC} and GND planes both reduces their characteristic impedance and reduces horizontal polarization through shielding by PCB copper planes. The metal stiffeners at the PCB edges also shield against horizontal polarization.

Impedance Matching

Radiated emissions are high when transmitted signals exhibit overshoot, undershoot, and ringing. Careful impedance matching must be maintained between drivers and transmission lines and between transmission lines and receivers to minimize these effects. For clock-distribution circuits, use of 10-Ω damping resistors between the drivers and transmission lines or pulldown resistors, Thevenin's terminations, or clamp diodes between the transmission lines and receiver inputs is recommended.

Conclusion

As the data in this application report shows, unsuitable transmission-line terminations both contribute to radiated emissions and cause signal distortion. The evaluations described in this report seek not to measure exact values of radiated emissions but rather to demonstrate the effectiveness of impedance matching for reducing both radiated emissions and signal distortion.

Analysis of Clock-Driver Circuit Output Drive Capability and Incident-Wave Switching

The recommended I_{OH} and I_{OL} are −48 mA and 48 mA, respectively, for many CDC devices. However, these devices are capable of driving beyond these limits, an important factor when considering switching a low-impedance load on the incident wave.

Incident-wave switching ensures that for a given transition (either high-to-low or loW-to-high) the output will reach a valid level on the initial wavefront (i.e., does not require reflections). Figure 1 shows the possible problems a designer can encounter when a device does not switch on the incident wave. A shelf below $V_{IL(max)}$ on signal A causeS the propagation delay of the signal to slow by the amount of time it takes for the signal to reach the end-of-line receiver and reflect back. This effect can increase the board skew of a clock tree (e.g., when loads on a given output switch on the incident wave and loads on a given output switch on the reflected wave). Signal B shows the case where there is a shelf in the threshold region. When this phenomenon occurs, the input to the receiver is in an unknown state which could cause several problems associated with slow input edges such as output oscillations. Signal C is an example of incident-wave switching. This signal will not cause problems or increase the propagation delay because the shelf occurs after the necessary V_{IH} level has been attained.

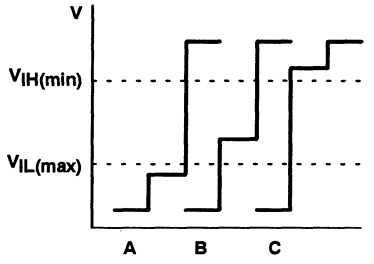


Figure 1. Reflected Wave Switching

The I_{OH} and I_{OL} curves for typical CDC outputs are shown in Figures 2 through 23. The recommended operating I_{OH} and I_{OL} can be found on the individual CDC data sheets.

Worst-case incident-wave switching analysis can be performed for the CDC341 using the data sheet specifications. For a low-to-high transition (V_{OH} = 2 V @ I_{OH} = −48 mA), the CDC341 can meet a $V_{IH(min)}$ requirement of 2 V @ IOH = −48 mA, providing incident-wave switching for loads as heavy as 37.5Ω (Equation 1).

$$Z_{LH} = \frac{V_{OLq} - V_{IH(min)}}{I_{OH}} = \frac{0.2\ V - 2\ V}{-48\ mA} = 37.5\ \Omega \quad (1)$$

For a high-to-low transition (V_{OL} = 0.5 V @ I_{OL} = 48 mA), the device can meet a $V_{IL(min)}$ requirement of 0.8 V @ I_{OH} = 48 mA, providing incident-wave switching for loads as heavy as 60 Ω (Equation 2).

$$Z_{HL} = \frac{V_{OHq} - V_{IL(max)}}{I_{OL}} = \frac{3.7\ V - 0.8\ V}{48\ mA} = 60\ \Omega \quad (2)$$

Using typical V_{OH} and V_{OL} values along with data points from the curves, it can be shown that the CDC341 can be used to switch greater loads. From the CDC341 curves of Figures 16 and 17, an analysis can be performed to determine the load capability for the CDC341 (Equations 3 and 4).

For a low-to-high transition (V_{OH} = 2.7 V @ I_{OH} = −96 mA):

$$Z_{LH} = \frac{V_{OLq} - V_{OH}}{I_{OH}} = \frac{0.2\ V - 2.7\ V}{-96\ mA} = 26\ \Omega \quad (3)$$

For a high-to-low transition (V_{OL} = 0.4 V @ I_{OL} = 96 mA):

$$Z_{HL} = \frac{V_{OHq} - V_{OL}}{I_{OL}} = \frac{3.7\ V - 0.4\ V}{96\ mA} = 34\ \Omega \quad (4)$$

CDC203
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

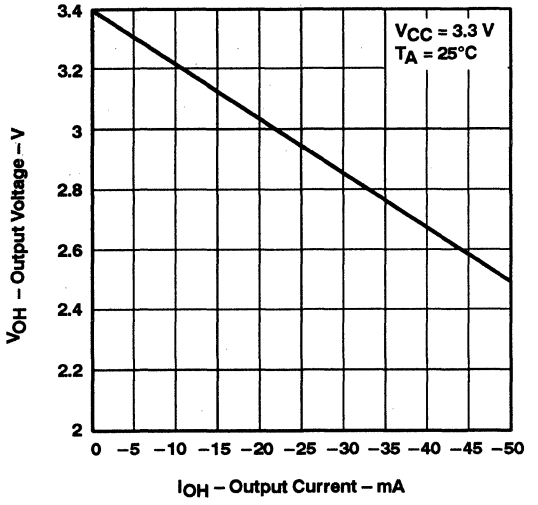


Figure 2

CDC203
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

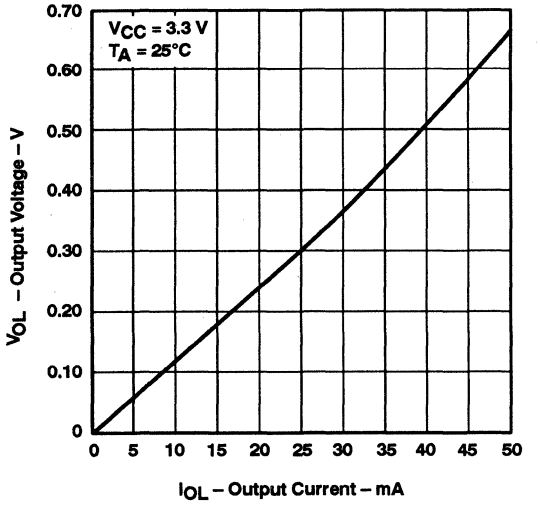


Figure 3

CDC204
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

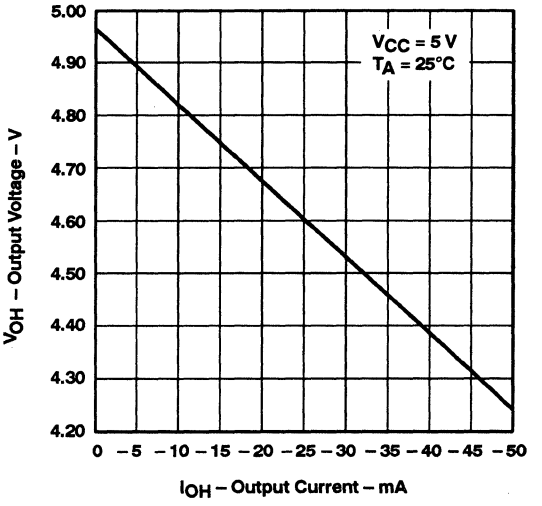


Figure 4

CDC204
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

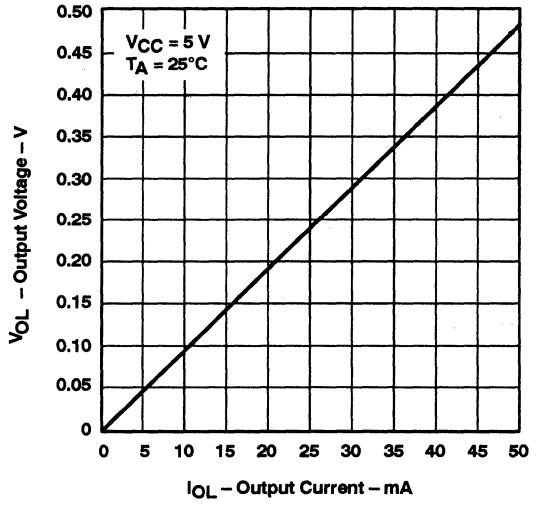


Figure 5

CDC208
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

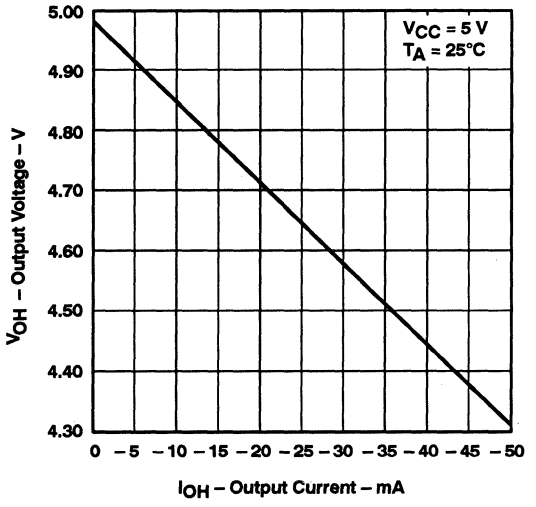


Figure 6

CDC208
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

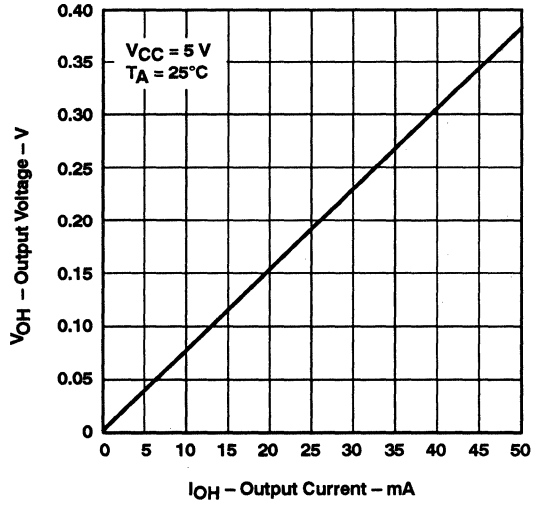


Figure 7

CDC303, CDC304, CDC305
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

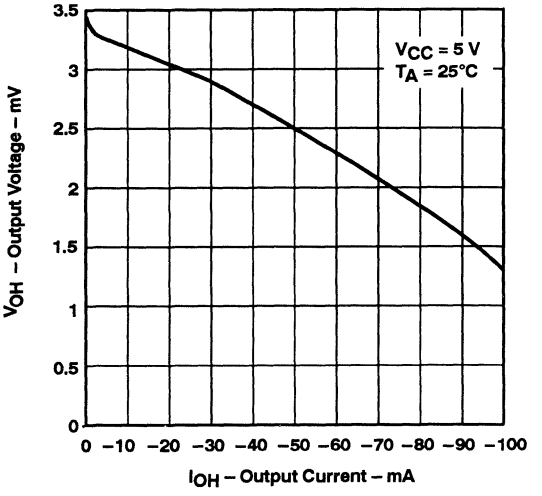


Figure 8

CDC303, CDC304, CDC305
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

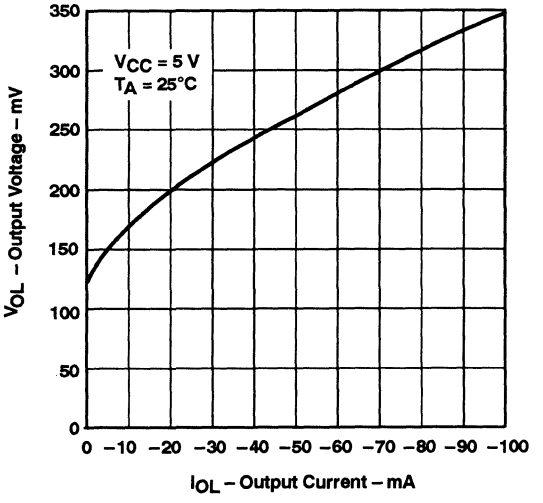


Figure 9

CDC328A, CDC391
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

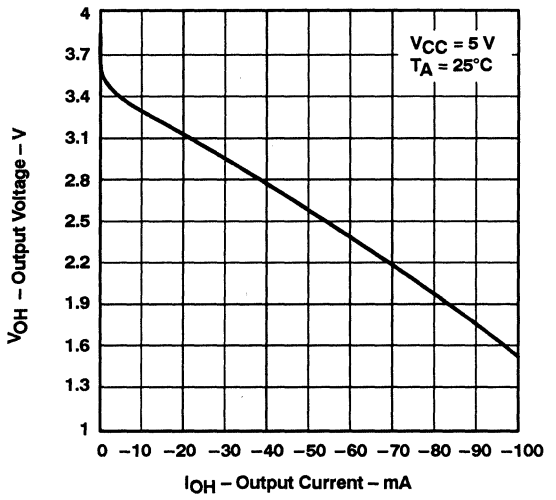


Figure 10

CDC328A, CDC391
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

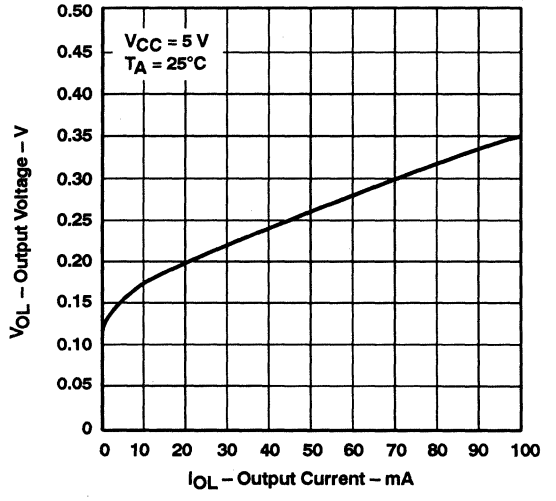


Figure 11

CDC329A, CDC392
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

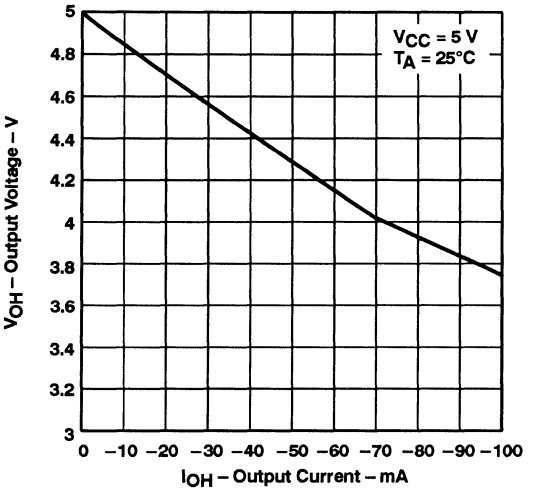


Figure 12

CDC329A, CDC392
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

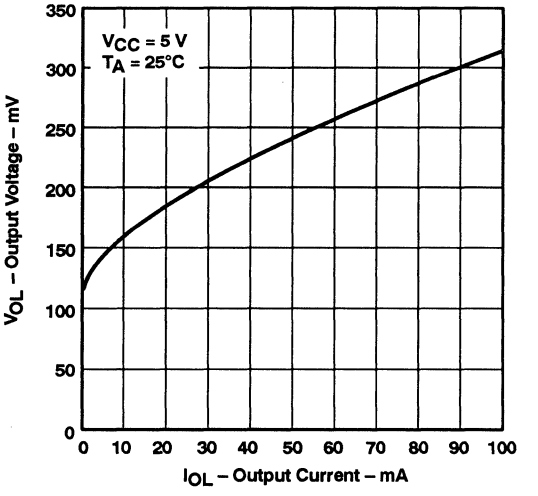


Figure 13

CDC337
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

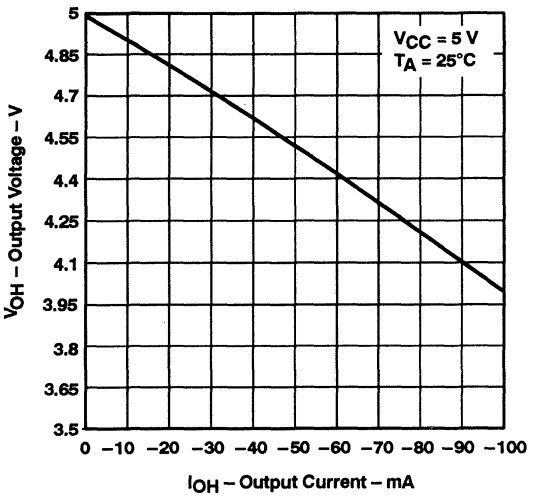


Figure 14

CDC337
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

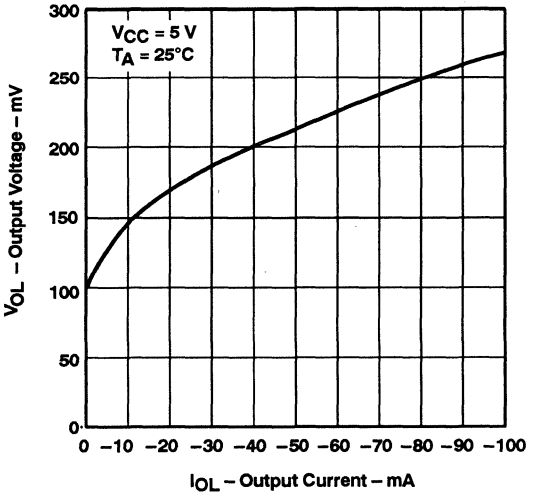


Figure 15

CDC339
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

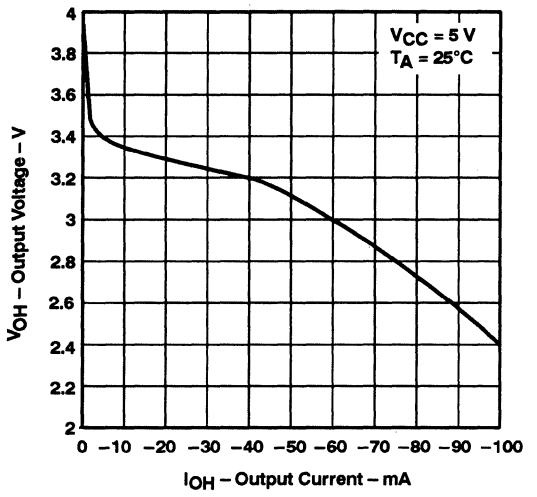


Figure 16

CDC339
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

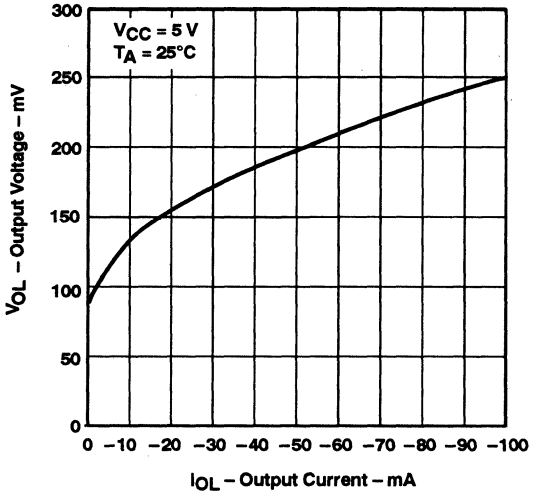


Figure 17

CDC340, CDC341
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

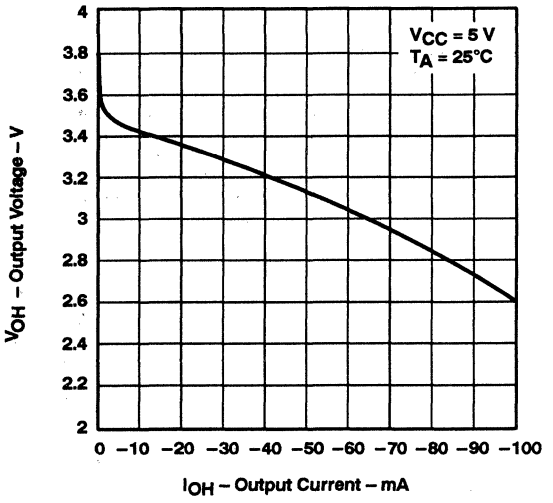


Figure 18

CDC340, CDC341
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

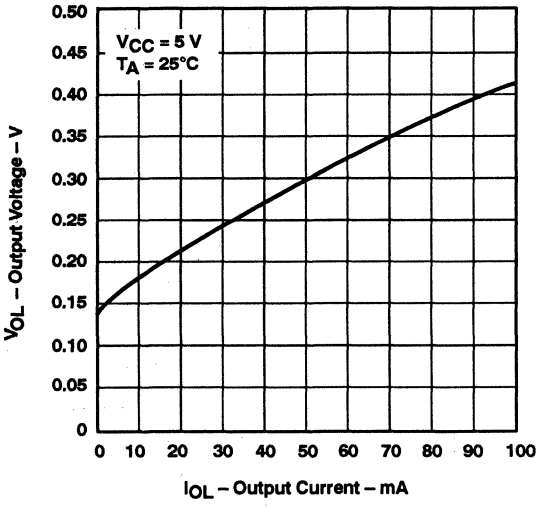


Figure 19

CDC586
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

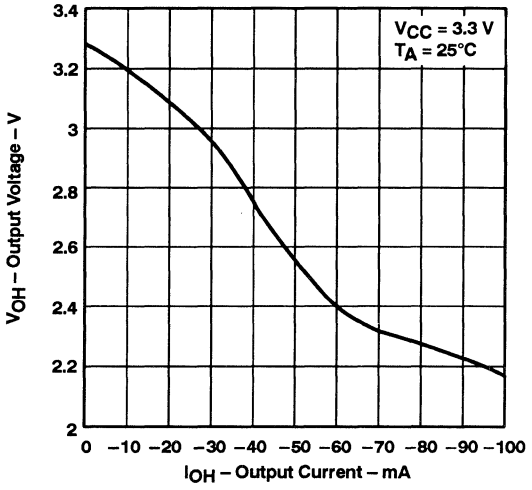


Figure 20

CDC586
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

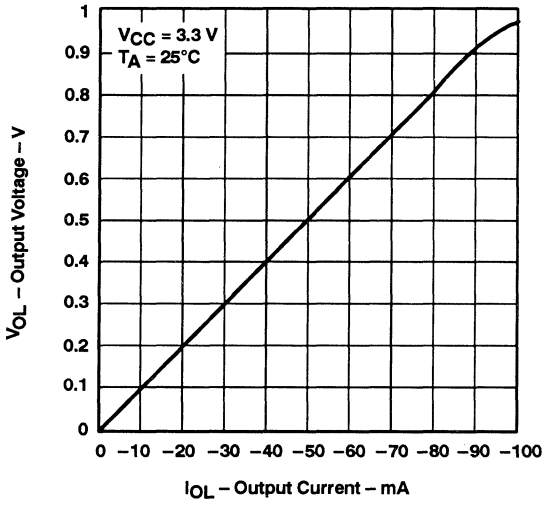


Figure 21

CDC2582, CDC2586
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

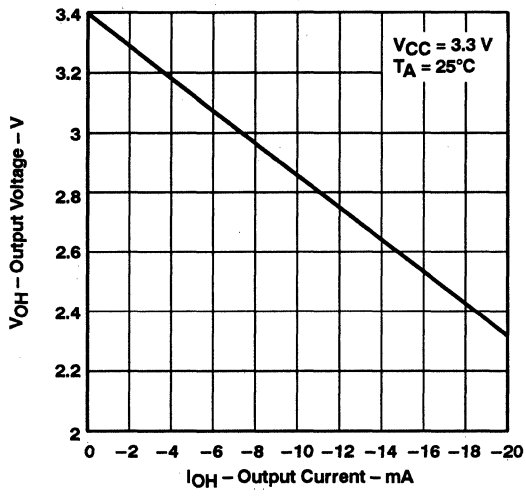


Figure 22

CDC2582, CDC2586
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

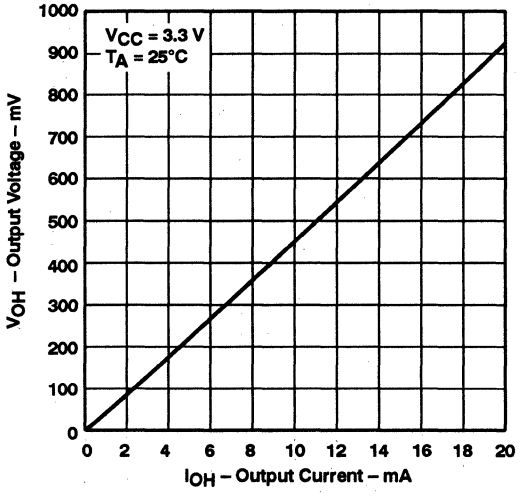
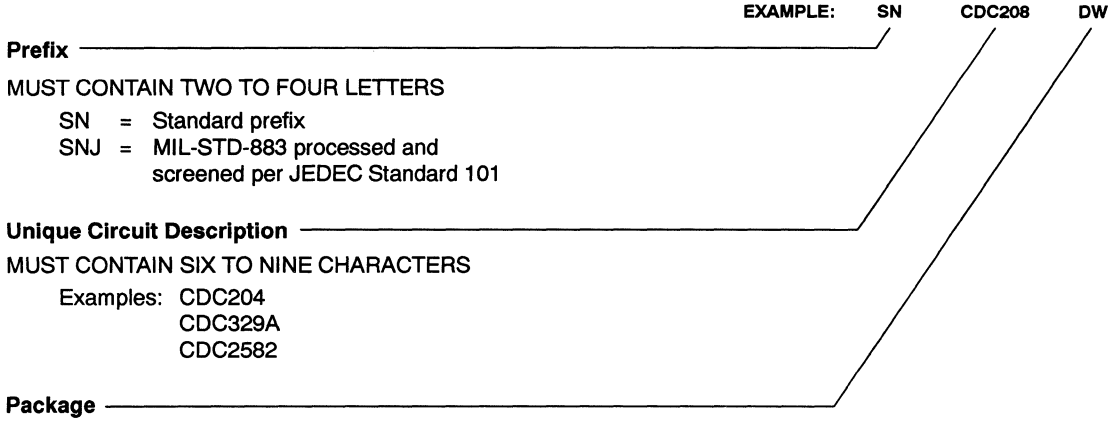


Figure 23

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

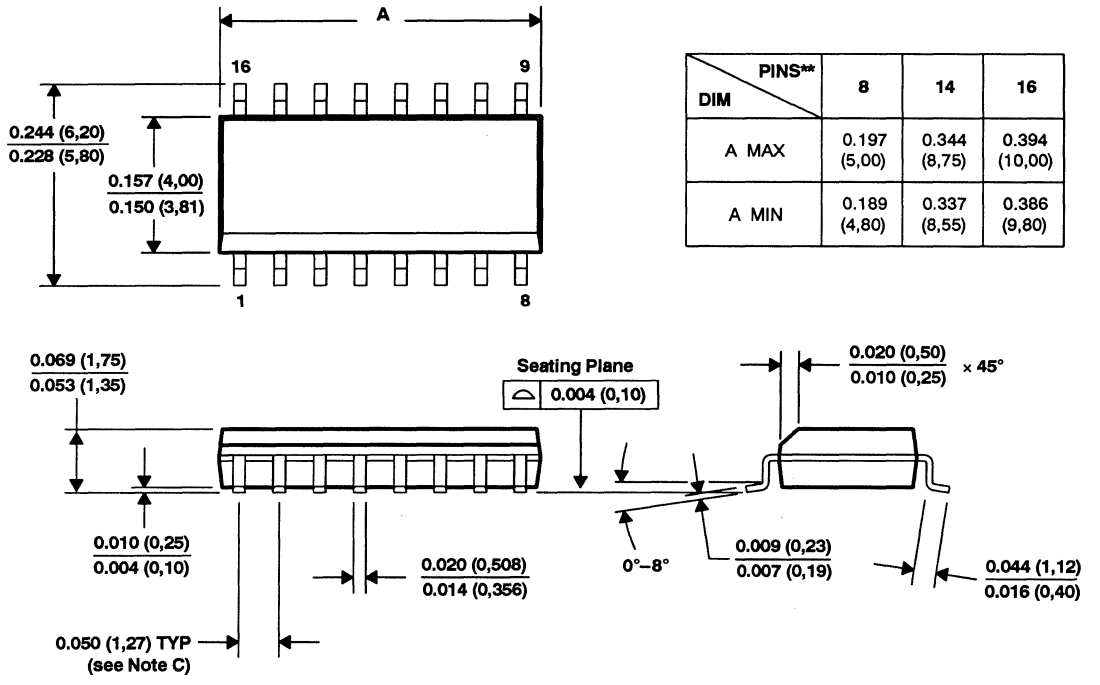
Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.



D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16 PIN SHOWN



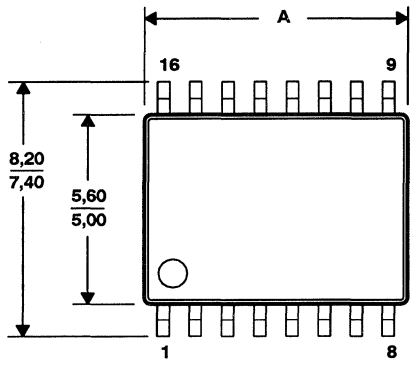
DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

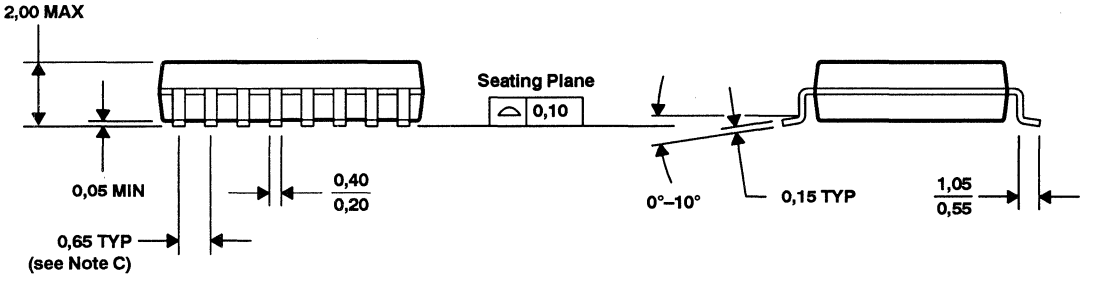
DB/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



DIM \ PINS**	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

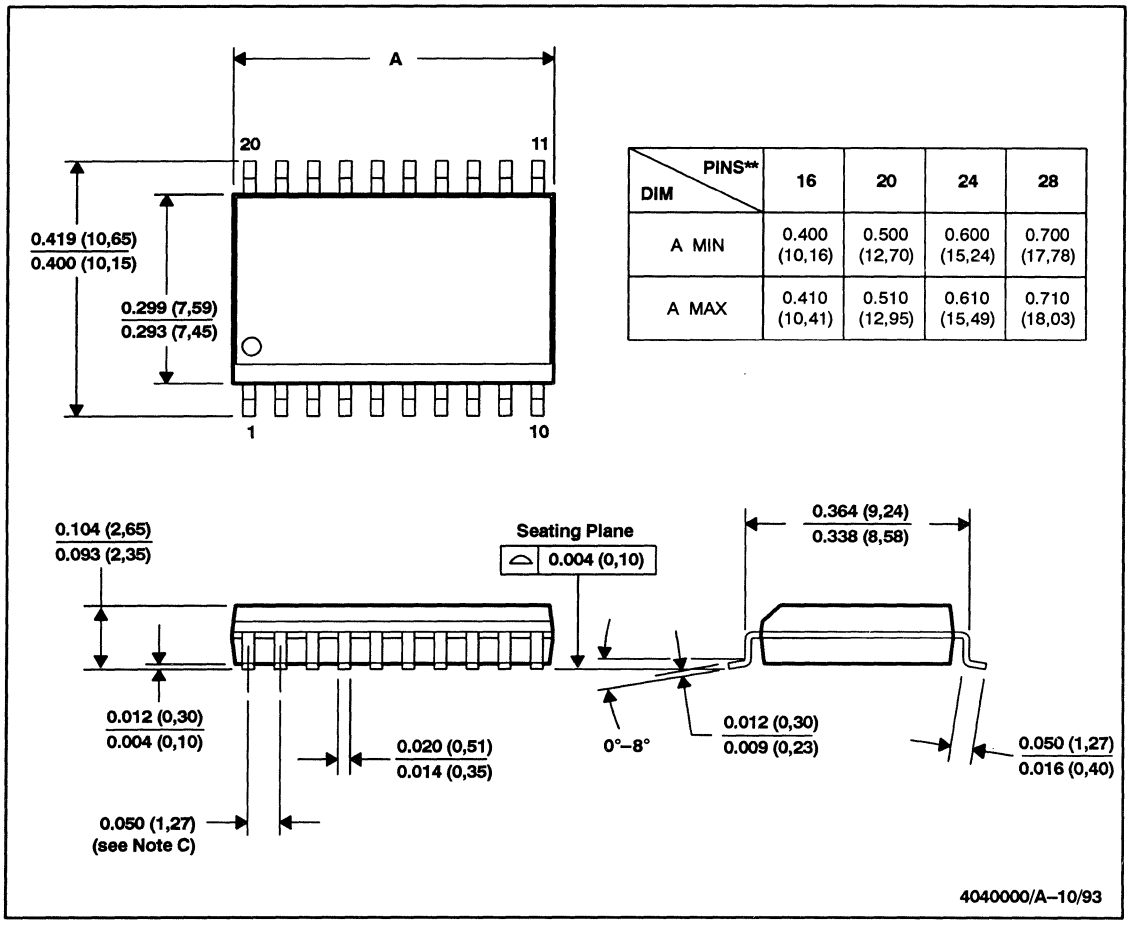


4040065/A–10/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

DW/R-PDSO-G**
20 PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



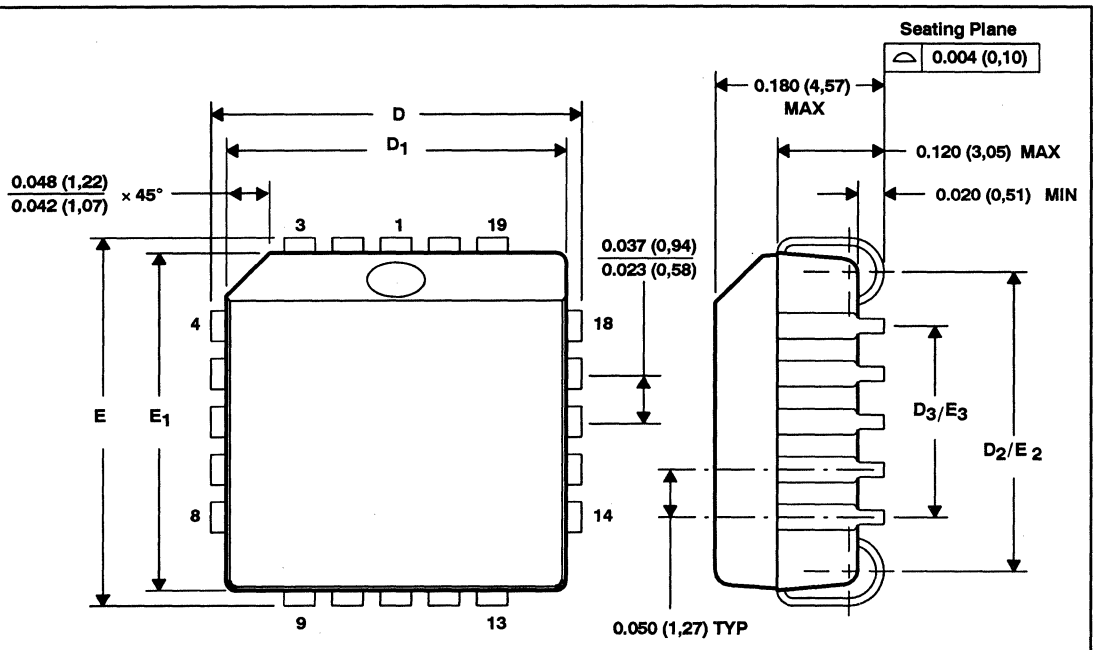
DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

FN/S-PQCC-J**

PLASTIC J-LEADED CHIP CARRIER

20-PIN SHOWN



JEDEC OUTLINE	NO. OF PINS**	D/E		D_1/E_1		D_2/E_2		D_3/E_3
		MIN	MAX	MIN	MAX	MIN	MAX	TYP
MO-047AA	20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.290 (7,34)	0.330 (8,38)	0.200 (5,08)
MO-047AB	28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.390 (9,91)	0.430 (10,92)	0.300 (7,62)
MO-047AC	44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.590 (14,99)	0.630 (16,00)	0.500 (12,70)
MO-047AD	52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.690 (17,53)	0.730 (18,54)	0.600 (15,24)
MO-047AE	68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.890 (22,61)	0.930 (23,62)	0.800 (20,32)
MO-047AF	84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	1.090 (27,69)	1.130 (28,70)	1.000 (25,40)

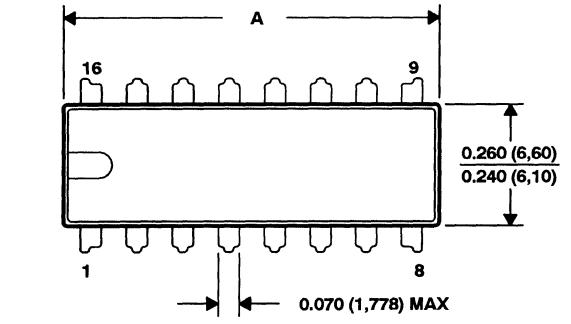
4040005/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-047.

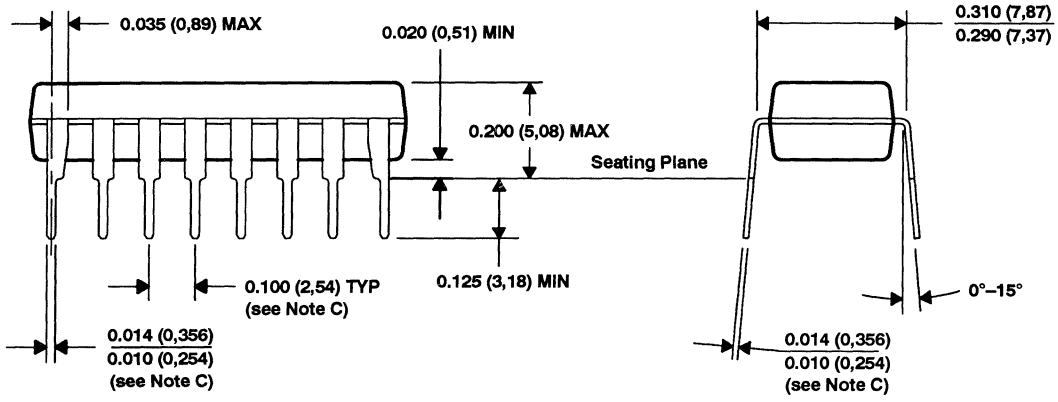
N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)



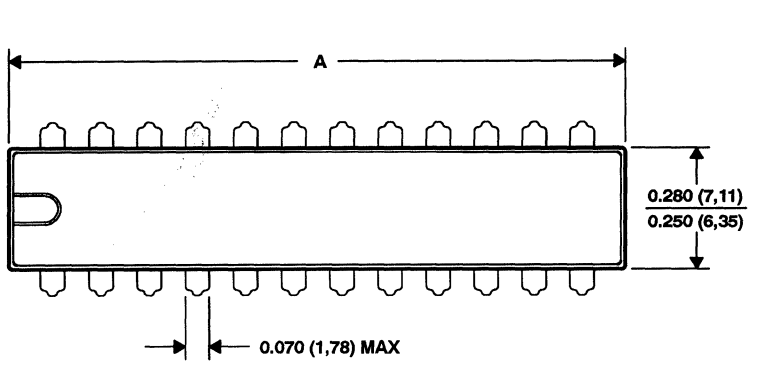
4040049/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

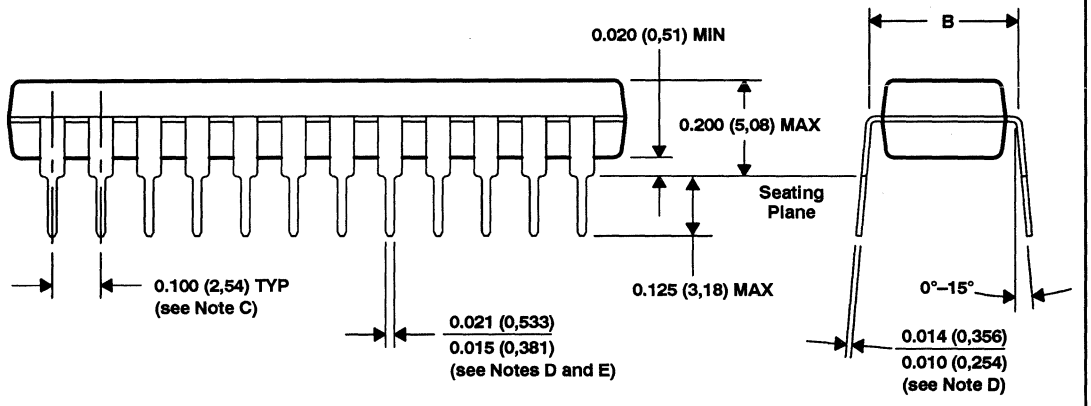
NT/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



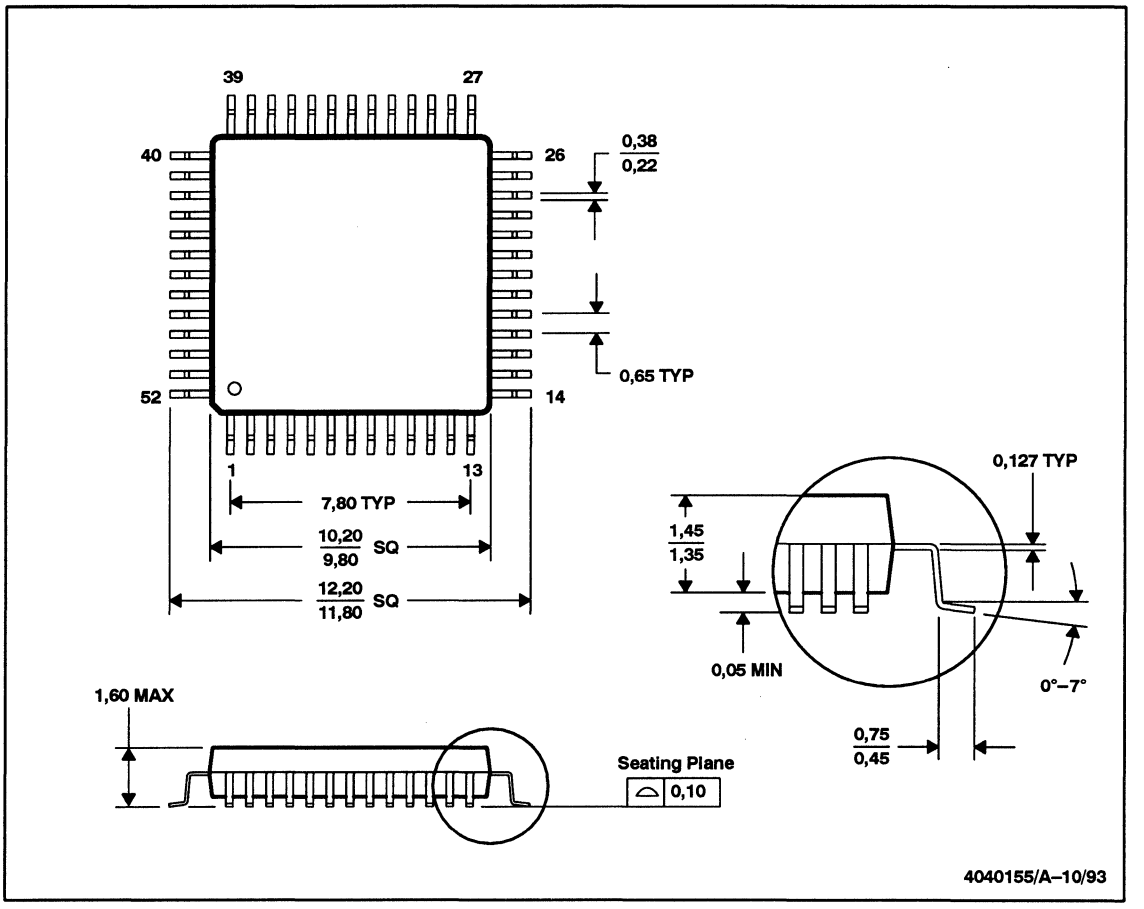
DIM \ PINS**	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder-dipped leads.
E. For solder-dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

PBG/S-PQFP-G52 **PLASTIC QUAD FLATPACK**

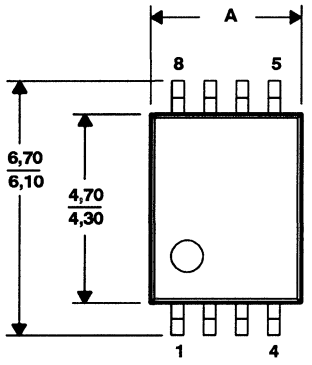


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

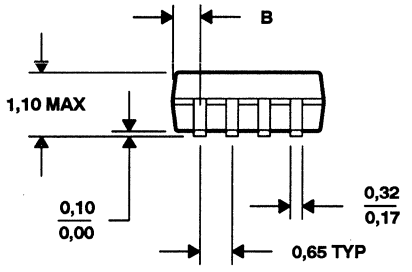
PW/R-PDSO-G**

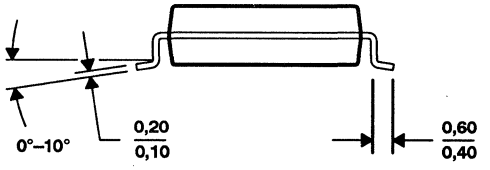
PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
B MAX	0,65	0,70	0,38	0,48	0,48	0,78





4040064/A–07/93

NOTES: D. All linear dimensions are in millimeters.
E. This drawing is subject to change without notice.
F. Drawing source: SCJ Package Handbook, 1990

NOTES

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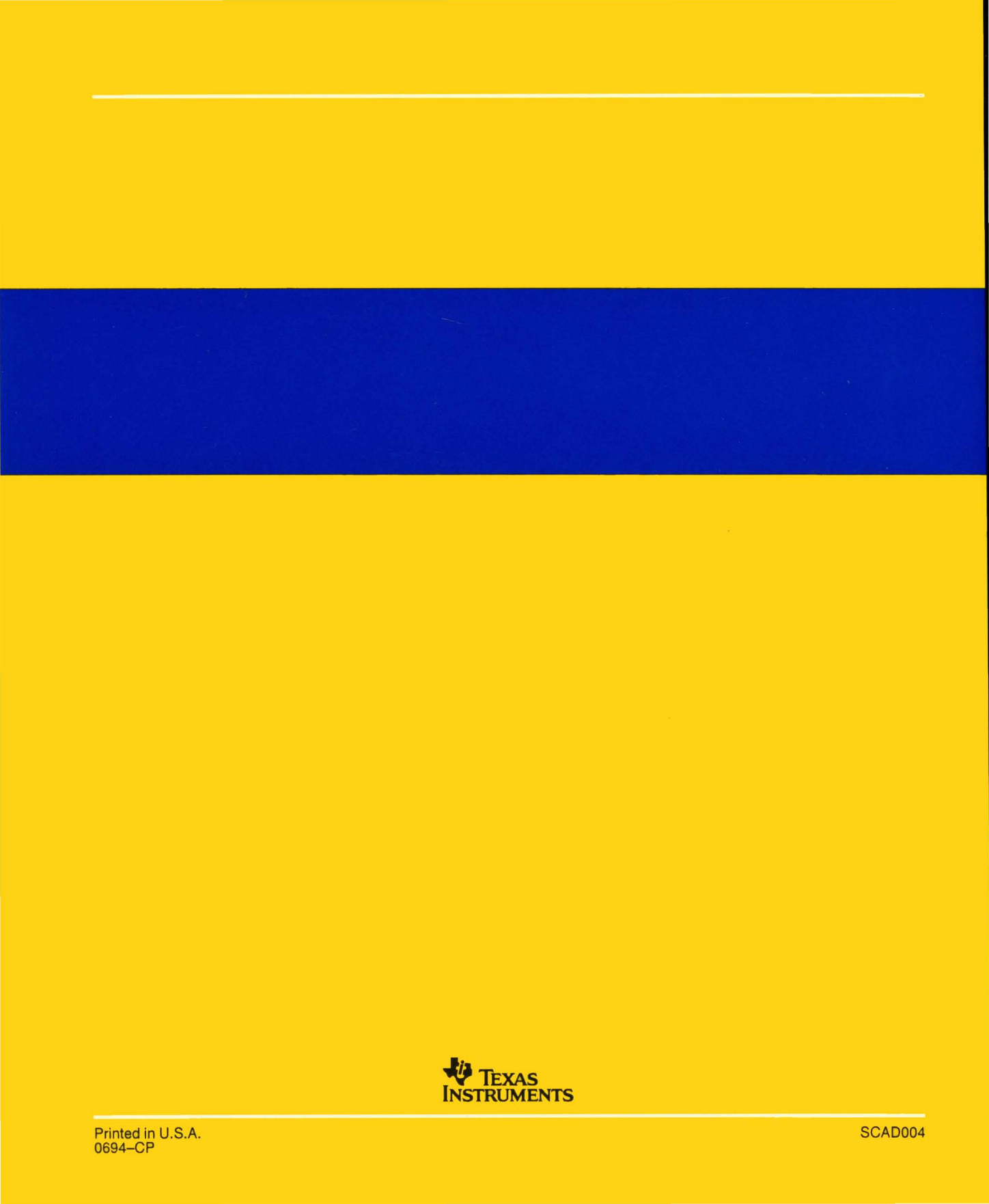

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