TEXAS
INSTRUMENTS

Power Supply Circuits

Voltage References, Voltage Regulators, PWM Controllers, Supervisors, Switches, Optoisolators, and Special Functions

Data Book

1996

Mixed-Signal Products

Data
Book

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Voltage References, Voltage Regulators,
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INTRODUCTION

The Texas Instruments **1996 Power Supply Circuits Data Book** has been created to showcase our growing line of analog components for power-supply designs. Featured in this data book are most of the components previously found in the **1992 Linear Circuits Data Book, Volume 3**, the many new and exciting power supply products introduced since then, and other components useful for power-supply designs.

This new data book is more than a collection of data sheets; it is a tool for locating the best power supply components for a successful design effort. It has been completely restructured to help you quickly find the devices best suited to your application.

A complete **alphanumeric index** at the beginning of the book makes finding specifications for known part numbers simple. You no longer have to search through chapter indexes when you don't know a device function.

The **new device index** includes a description to highlight TI's newest devices. These products include new families of PMOS high-side switches and personal computer memory card international association (PCMCIA) power distribution switches, extremely low dropout (LDO) voltage regulators, advanced pulse-width-molulation (PWM) controllers, and integrated power supply building blocks. Product-preview data sheets are included for devices not completely released when this book was printed. Contact your local TI sales office for complete data sheets and product availability.

Redesigned **product selection guides** give a condensed view of parametric information, organized to help you choose the devices that most closely fit your needs. Key specifications and/or features are presented for easy comparison.

An extensive **glossary** is provided for reference, defining and clarifying terms used by Texas Instruments and the semiconductor industry that might be new or unfamiliar.

The data sheets have been organized into several chapters by product function.

- Voltage references
- Voltage regulators
- PWM controllers and dc-to-dc converters
- Supply voltage supervisors
- PMOS and PCMCIA power distribution switches
- Optoisolators
- Building blocks and special functions

Each chapter has its own table of contents that includes descriptions of the devices, which makes finding a specific device much easier to find.

For convenience, a chapter for **optoisolators** is included in the **1996 Power Supply Circuits Data Book**. This eliminates the need to flip back and forth between two data books for your total power-supply solution.

In section 9 of this data book there is a collection of **application notes**. Texas Instruments is committed to providing designers with detailed application notes for our newest power-supply components. This section represents the beginning of this effort. These applications are fully tested and, in some cases, evaluation boards may be available (contact your local TI sales office). More applications notes will be available from the factory soon.

The last section of this data book contains complete **mechanical specifications** for all packages used with Texas Instruments power supply circuits. This includes the latest innovations in surface-mount power packages. Designers of space-critical systems may want to investigate new products offered in SOT-23 (DBV suffix), power TSSOP (PWP suffix), and the PowerFlex™ (KTD, KTG, and KTP suffixes) packages.

PowerFlex is a trademark of Texas Instruments Incorporated.

While this data book offers design and specification data only for power-supply products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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or telephone the TI Literature Response number: 1-800-477-8924.

We sincerely believe the new **1996 Power Supply Circuits Data Book** will be a valuable addition to your collection of technical literature.

Contents

Devices in **bold type** are new to this data book.

ALPHANUMERIC INDEX

† This is a product preview data sheet.

fixed output voltage series pass regulators

DEVICE	V_O (V) NOM	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
POSITIVE OUTPUT VOLTAGE											
TPS7233	3.3	250	2	155 µA	0.14 – 0.18	10	X	X		–40°C to 125°C	Very low dropout PMOS
TPS7333			2	340 µA	0.044 – 0.06	10	X	X	X	–40°C to 125°C	Lowest dropout PMOS with SVS
TLV2217–33		500	1	19	0.4 – 0.5	12	X			0°C to 125°C	Low dropout pnp
TPS7133			2	285 µA	0.047 – 0.060	10	X	X		–40°C to 125°C	Lowest droput PMOS
TPS7248	4.85	250	2	155 µA	0.09 – 0.1	10	X	X		–40°C to 125°C	Very low dropout PMOS
TPS7348			2	340 µA	0.028 – 0.037	10	X	X	X	–40°C to 125°C	Lowest dropout PMOS with SVS
TL75LP48		300	2	4	0.12 – 0.2	23	X	X		–40°C to 125°C	Low dropout pnp
TPS7148		500	2	285 µA	0.03 – 0.037	10	X	X		–40°C to 125°C	Lowest dropout PMOS
µA78L05A	5	100	5	380	2.5 – 3	20				–40°C to 125°C	General purpose, low current
µA78L05			10	3.8	2 – 3	20				–40°C to 125°C	General purpose, low current
TL750L05		150	4	10	0.2 – 0.6	26	X			–40°C to 150°C	Low dropout pnp, low current
TL751L05			4	10	0.2 – 0.6	26	X	X		–40°C to 150°C	Low dropout pnp, low current, shutdown
LM2930-5			10	18	0.32 – 0.6	26	X			–40°C to 150°C	3-terminal low-dropout pnp
TPS7250		250	2	155 µA	0.76 – 0.85	10	X	X		–40°C to 125°C	Very low dropout PMOS
TPS7350			2	340 µA	0.27 – 0.035	10	X	X	X	–40°C to 125°C	Lowest dropout PMOS with SVS
TL75LP05		300	2	4	0.12 – 0.2	23	X	X		–40°C to 125°C	Low dropout pnp
TPS7150		500	2	285 µA	0.27 – 0.033	10	X	X		–40°C to 125°C	Lowest dropout PMOS
µA78M05			5	4.5	2 – 3	25				0°C to 125°C	General purpose, medium current
TL750M05		750	1	60	0.5 – 0.6	26	X			–40°C to 125°C	Low dropout pnp, high current
TL751M05			1	60	0.5 – 0.6	26	X	X		–40°C to 125°C	Low dropout pnp, high current, shutdown
TL780-05		1500	1	5	2 – 3	25				0°C to 125°C	High current, upgrade for µA7805
µA7805			10	4.2	2 – 3	25				–40°C to 125°C	General purpose, high current
µA78L06A	6	100	5	3.9	2.5 – 3	20				0°C to 125°C	General purpose, low current
µA78L06			10	3.9	2.5 – 3	20				0°C to 125°C	General purpose, low current
µA78M06		500	5	4.5	2 – 3	25				0°C to 125°C	General purpose, medium current
µA7806		1500	10	4.3	2 – 3	25				0°C to 125°C	General purpose, high current

† Supply-voltage supervisor

fixed output voltage series pass regulators (continued)

DEVICE	V_O (V) NOM	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
POSITIVE OUTPUT VOLTAGE (CONTINUED)											
µA78L08A	8	100	5	4	2.5 – 3	23				0°C to 125°C	General purpose, low current
µA78L08			10	4	2.5 – 3	23				0°C to 125°C	General purpose, low current
TL750L08		150	4	10	0.2 – 0.7	26	X			−40°C to 150°C	Low dropout pnp, low current
TL751L08			4	10	0.2 – 0.7	26	X	X		−40°C to 150°C	Low dropout pnp, low current, shutdown
LM2930-8			10	18	0.32 – 0.6	26	X			−40°C to 150°C	3-terminal low-dropout pnp
TL75LP08		300	2	4	0.12 – 0.2	23	X	X		−40°C to 125°C	Low dropout pnp
µA78M08		500	5	4.6	2.5 – 3	25				0°C to 125°C	General purpose, medium current
TL750M08		750	1	60	0.5 – 0.7	26	X			−40°C to 125°C	Low dropout pnp, high current
TL751M08			1	60	0.5 – 0.7	26	X	X		−40°C to 125°C	Low dropout pnp, high current, shutdown
µA7808		1500	10	4.3	2.5 – 3	25				0°C to 125°C	General purpose, high current
µA7885	8.5		10	4.3	2 – 3	25				0°C to 125°C	General purpose, high current
µA78L08A	9	100	5	4.1	2.5 – 3	24				0°C to 125°C	General purpose, low current
µA78L09			10	4.1	2.5 – 3	24				0°C to 125°C	General purpose, low current
µA78M09		500	5	4.6	2.5 – 3	26				0°C to 125°C	General purpose, medium current
µA78L10A	10	100	5	4.2	2.5 – 3	25				0°C to 125°C	General purpose, low current
µA78L10			10	4.2	2.5 – 3	25				0°C to 125°C	General purpose, low current
TL750L10		150	4	10	0.2 – 0.8	26	X			−40°C to 150°C	Low dropout pnp, low current
TL751L10			4	10	0.2 – 0.8	26	X	X		−40°C to 150°C	Low dropout pnp, low current, shutdown
TL75LP10		300	2	4	0.12 – 0.2	23	X	X		−40°C to 125°C	Low dropout pnp
µA78M10		500	5	4.6	2.5 – 3	28				0°C to 125°C	General purpose, medium current
TL750M10		750	1	60	0.5 – 0.8	26	X			−40°C to 125°C	Low dropout pnp, high current
TL751M10			1	60	0.5 – 0.8	26	X	X		−40°C to 125°C	Low dropout pnp, high current, shutdown
µA810		1500	10	4.3	2.5 – 3	28				0°C to 125°C	General purpose, high current

† Supply-voltage supervisor

fixed output voltage series pass regulators (continued)

DEVICE	V_O (V) NOM	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
POSITIVE OUTPUT VOLTAGE (CONTINUED)											
μA78L12A	12	100	5	4.3	2.5 – 3	27				–40°C to 125°C	General purpose, low current
μA78L12			10	4.3	2.5 – 3	27				–40°C to 125°C	General purpose, low current
TL750L12		150	4	10	0.2 – 0.9	26	X			–40°C to 150°C	Low dropout pnp, low current
TL751L12			4	10	0.2 – 0.9	26	X	X		–40°C to 150°C	Low dropout pnp, low current, shutdown
TL75LP12		300	2	4	0.12 – 0.2	23	X	X		–40°C to 125°C	Low dropout pnp
μA78M12		500	5	4.8	2.5 – 3	30				0°C to 125°C	General purpose, medium current
TL750M12		750	1	60	0.9 – 0.9	26	X			–40°C to 125°C	Low dropout pnp, high current
TL751M12			1	60	0.9 – 0.9	26	X			–40°C to 125°C	Low dropout pnp, high current, shutdown
TL780-12		1500	1	5.5	2.5 – 3	30				0°C to 125°C	High current, upgrade for μA7812
μA7812			10	4.3	2.5 – 3	30				–40°C to 125°C	General purpose, high current
μA78L15A	15	100	5	4.6	2.5 – 3	30				0°C to 125°C	General purpose, low current
μA78L15			10	4.6	2.5 – 3	30				0°C to 125°C	General purpose, low current
μA78M15		500	5	4.8	2.5 – 3	30				0°C to 125°C	General purpose, medium current
TL780-15		1500	1	5.5	2.5 – 3	30				0°C to 125°C	High current, upgrade for μA7815
μA7815			10	4.4	2.5 – 3	30				0°C to 125°C	General purpose, high current
μA7818	18		10	4.5	3 – 3	33				0°C to 125°C	General purpose, high current
μA78M20	20	500	5	4.9	3 – 3	35				0°C to 125°C	General purpose, medium current
μA78M24	24		5	5	3 – 3	38				0°C to 125°C	General purpose, medium current
μA7824		1500	10	4.6	3 – 3	38				0°C to 125°C	General purpose, high current

† Supply-voltage supervisor

fixed output voltage series pass regulators (continued)

DEVICE	V_O (V) NOM	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
NEGATIVE OUTPUT VOLTAGE											
MC79L05A	−5	100	5	5	2 − 3	−20				0°C to 125°C	Negative low current
MC79L05			10	10	2 − 3	−20				0°C to 125°C	Negative low current
µA79M05		500	5	1	2 − 3	−25				0°C to 125°C	Negative general purpose, medium current
µA79M06	−6	500	5	1	2 − 3	−25				0°C to 125°C	Negative general purpose, medium current
µA79M08	−8	500	5	1	2.5 − 3	−25				0°C to 125°C	Negative general purpose, medium current
MC79L12A	−12	100	5	5	2.5 − 3	−27				0°C to 125°C	Negative low current
MC79L12			10	10	2.5 − 3	−27				0°C to 125°C	Negative low current
µA79M12		500	5	1.5	2.5 − 3	−30				0°C to 125°C	Negative general purpose, medium current
MC79L15A	−15	100	5	5	2.5 − 3	−30				0°C to 125°C	Negative low current
MC79L15			10	10	2.5 − 3	−30				0°C to 125°C	Negative low current
µA79M15		500	5	1.5	2.5 − 3	−30				0°C to 125°C	Negative general purpose, medium current
µA79M20	−20	500	5	1.5	3 − 3	−35				0°C to 125°C	Negative general purpose, medium current
µA79M24	−24	500	5	1.5	3 − 3	−38				0°C to 125°C	Negative general purpose, medium current

† Supply-voltage supervisor

adjustable series pass regulators

DEVICE	V_O (V) MIN–MAX	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
TL317	1.2 – 32	100	4	1.5	2.5 – 3	35				0°C to 125°C	General purpose low current adjustable
TPS7201	1.2 – 9.75	250	3	155 µA	0.16–0.27	10	X	X		–40°C to 125°C	Very low dropout PMOS adjustable
TPS7301	1.2 – 9.75	250	3	340 µA	0.052–0.085	10	X	X	X	–40°C to 125°C	Lowest dropout PMOS with SVS
TPS7101	1.2 – 9.75	500	3	285 µA	0.052–0.085	10	X	X		–40°C to 125°C	Lowest dropout PMOS adjustable
TL783	1.2 – 125	700	6	15	10 – 15	125				0°C to 125°C	High voltage high current adjustable

† Supply-voltage supervisor

adjustable shunt regulators

DEVICE	V_{ref} (V)	I_Z (mA) MIN–MAX	V_O (V) MIN–MAX	TOL (%)	$V_I$max (V)	TEMP CO (ppm/°C) TYP	DESCRIPTION
TLV431	1.24	0.1 – 15	V_{ref} – 6	1	6	46	Low voltage adjustable shunt reference
TL1431	2.5	1 – 100	V_{ref} – 36	0.40	36	30	Precision adjustable shunt reference
TL431	2.5	1 – 100	V_{ref} – 36	2	36	30	Adjustable shunt reference
TL431A	2.5	1 – 100	V_{ref} – 36	1	36	30	Precision adjustable shunt reference
TL430	2.75	2 – 100	V_{ref} – 30	9	30	120	Adjustable shunt reference

voltage references

DEVICE	V_{ref} (V)	TOL (%)	$I_Z$min (µA)	$I_Z$max (mA)	DESCRIPTION
LT1004-1.2	1.2	0.30	10	20	Micropower precision reference
LM385B-1.2		1	10	20	Micropower reference
LM385-1.2		2	10	20	Micropower reference (LM185/285 temperature grades also available)
LT1004-2.5	2.5	0.80	20	20	Micropower precision reference
LM336B-2.5		01	400	10	Precision voltage reference (LM236 temperature grade also available)
LM385B-2.5		1.5	20	20	Micropower precision reference
LT1009		2	400	20	Voltage reference
LM385-2.5		3	20	20	Micropower reference (LM185/285 temperature grades also available)
LM336-2.5		4	400	10	Voltage reference (LM236 temperature grade also available)

supply voltage supervisors

DEVICE	V_t (V)	TOL (%)	I_{CC} (mA) MAX	V_I min (V)	OVS‡	PROGRAMMABLE TIME DELAY	COMPLEMENTARY OUTPUTS	DESCRIPTION
TL7702A	pgm†	2	3	3.60		X	X	Single SVS with programmable undervoltage threshold and reset time delay
TL7702B	pgm†	2	3	1		X	X	Single SVS with programmable undervoltage threshold and reset time delay
TLC7705	4.55	1.5	25 μA	1		X	X	Single micropower SVS (5 V) with programmable time delay and push-pull outputs
TL7705A	4.55	2	3	3.60		X	X	Single SVS for 5 V systems with programmable time delay
TL7705B	4.55	2	3	1		X	X	Single SVS for 5 V systems with programmable time delay
TL7757	4.55	3	40 μA	1				3-terminal SVS for 5 V systems
TL7759	4.55	3	40 μA	1			X	4-terminal SVS for 5 V systems
TL7770-5	4.55	1	5	1	X	X	X	Dual SVS, 5 V and programmable with programmable time delay
TL7709A	7.60	2	3	3.60		X	X	Single SVS for 9 V systems with programmable time delay
TL7712A	10.80	2	3	3.60		X	X	Single SVS for 12 V systems with programmable time delay
TL7770-12	10.90	1	5	1	X	X	X	Dual SVS, 12 V and programmable with programmable time delay
TL7715A	13.50	2	3	3.60		X	X	Single SVS for 15 V systems with programmable time delay
TL7770-15	13.64	1	5	1	X	X	X	Dual SVS, 15 V and programmable with programmable time delay

† Programmable using external resistor divider.
‡ Overvoltage sense (programmable)

switching power supply controllers

										OUTPUTS									
										MODE		TYPE							
CONTROL TOPOLOGY	V_{IN} RANGE (VDC)	OUTPUT CURRENT (mA)	MAX FREQUENCY (kHz)	REFERENCE VOLTAGE (V)	V_{REF} TOLERANCE (%)	SHUTDOWN	OPERATING/STANDBY CURRENT (mA)	DEAD TIME CONTROL	MAX DUTY CYCLE (%)	SINGLED ENDED	FIXED PUSH-PULL	SINGLE SWITCH OUTPUTS	TOTEM POLE	PROGRAMMABLE OUTPUTS	UNDERVOLTAGE LOCKOUT	ON-BOARD AMPLIFIERS	CURRENT-SENSE AMPLIFIERS	PULSE-BY-PULSE I_{sense}	DEVICES
Voltage-Mode PWM	7–40	200	300	5	5		6/NA	Y	90	Y	Y	Y	—	Y		2	—		TL494, 494M
	8–40	100	1000	5	4	Y	?/8	N	90	—	Y	Y	—			1	1		SG2524
	7–40	200	300	5	1		12.4/9	Y	90	Y	Y	Y	—	Y	Y	2	—		TL594
	7–40	±250	300	5	1		15/NA	Y	90	Y	Y	—	Y	Y	Y	2	—		TL598, 598M
	3.6–50	20	500	2.5	4		1.7/1.3	Y	100	Y	—	Y	—		Y	2	—		TL1451A
	3.6–20	±40	2000	1.25	2.5		3.5/3.1	Y	100	Y	—	—	Y		Y	2	—		TL1454
	3.6–40	20	400	1	5		1.1/1	Y	100	Y	—	Y	—		Y	1	—		TL5001
	9.5–40	150		7.15	5		2.3/NA	N	—	Y	—	Y	—			1	1	Y	μA723
Current-Mode PWM	5–12	225	170	1.23	4	Y	1.2/0.003	N	—	Y	—	Y	—			1	1	Y	TPS6734
	30†	±200	500	5	1		11/NA	N	97	Y	—	—	Y		Y	1	1	Y	UC284X
	30†	±200	500	5	2		11/NA	N	97	Y	—	—	Y		Y	1	1	Y	UC384X
Fixed On-Time V-Mode	1.1–20	1200	40	‡	10		—	N	—	Y	—	Y	—			1	—		TL496C
	1.1–35	500	40	1.26	5		0.8/NA	N	—	Y	—	Y	—			1	—		TL499A
	4.5–12	500	50	1.2	5	Y	11/6	N	—	Y	—	Y	—			1	1		TL497A

† Low-level voltage varies with UVLO value.
‡ Fixed 9-V output.

optoisolators

DEVICE	VISO (PEAK) (kV)	LED VF† (MAX) (V)	VCE (SAT) (MAX) (V)	RISE TIME (TYP) (µs)	FALL TIME (TYP) (µs)	BASE CONNECTION	CTR (MIN) (%)	PACKAGE
4N25	2.5	1.5	0.5	2‡	2‡	Yes	20	6 Pin DIP
4N26	1.5	1.5	0.5	2‡	2‡	Yes	20	6 Pin DIP
4N27	1.5	1.5	0.5	2‡	2‡	Yes	10	6 Pin DIP
4N28	0.5	1.5	0.5	2‡	2‡	Yes	10	6 Pin DIP
4N35	3.5	1.5	0.3	10	10	Yes	100	6 Pin DIP
4N36	2.5	1.5	0.3	10	10	Yes	100	6 Pin DIP
4N37	1.5	1.5	0.3	10	10	Yes	100	6 Pin DIP
6N135	3	1.7	0.4	1	0.7	Yes	7	8 Pin DIP
6N136	3	1.7	0.4	0.6	0.6	Yes	19	8 Pin DIP
HCPL4502	3	1.7	0.4	0.6	0.6	No	19	8 Pin DIP
MCT2	1.5	1.5	0.4	5‡	5‡	Yes	20	6 Pin DIP
MCT2E	3.5	1.5	0.4	5‡	5‡	Yes	20	6 Pin DIP
TIL191	3.5	1.4	0.4	6	6	No	20	4 Pin DIP
TIL191A	3.5	1.4	0.4	6	6	No	50	4 Pin DIP
TIL191B	3.5	1.4	0.4	6	6	No	100	4 Pin DIP
TIL192	3.5	1.4	0.4	6	6	No	20	8 Pin DIP
TIL192A	3.5	1.4	0.4	6	6	No	50	8 Pin DIP
TIL192B	3.5	1.4	0.4	6	6	No	100	8 Pin DIP
TIL193	3.5	1.4	0.4	6	6	No	20	16 Pin DIP
TIL193A	3.5	1.4	0.4	6	6	No	50	16 Pin DIP
TIL193B	3.5	1.4	0.4	6	6	No	100	16 Pin DIP

† At 10 mA
‡ Phototransistor operation

optoisolators with triac output

DEVICE	VISO (PEAK) (kV)	LED VF (MAX)	IFT (MAX) (mA)	dv/dt (TYP) (V/μs)	VTM (MAX) (V)	VDRM (V)	PACKAGE
MOC3009	7.5	1.5	30	12	3	250	6 Pin DIP
MOC3010	7.5	1.5	15	12	3	250	6 Pin DIP
MOC3011	7.5	1.5	10	12	3	250	6 Pin DIP
MOC3012	7.5	1.5	5	12	3	250	6 Pin DIP
MOC3020	7.5	1.5	30	100	3	400	6 Pin DIP
MOC3021	7.5	1.5	15	100	3	400	6 Pin DIP
MOC3022	7.5	1.5	10	100	3	400	6 Pin DIP
MOC3023	7.5	1.5	5	100	3	400	6 Pin DIP
TIL3009	3.5	1.5	30	12	3	250	6 Pin DIP
TIL3010	3.5	1.5	15	12	3	250	6 Pin DIP
TIL3011	3.5	1.5	10	12	3	250	6 Pin DIP
TIL3012	3.5	1.5	5	12	3	250	6 Pin DIP
TIL3020	3.5	1.5	30	100	3	400	6 Pin DIP
TIL3021	3.5	1.5	15	100	3	400	6 Pin DIP
TIL3022	3.5	1.5	10	100	3	400	6 Pin DIP
TIL3023	3.5	1.5	5	100	3	400	6 Pin DIP

SERIES REGULATORS

Bias Current

The operating current of the device; the difference between input and output current. This current is usually the current that flows in the ground or reference terminal of the regulator and may be load dependent. Also referred to as quiescent current.

Current-Limit Sense Voltage

A voltage proportional to the load current that controls the current-limit circuitry.

Dropout Voltage

The input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage

A voltage proportional to the output voltage that controls the regulator.

Input Regulation (Line Regulation)

The change in output voltage due to a change in input voltage, often expressed as a percentage of the output voltage.

Low Dropout Regulator (LDO)

A voltage regulator that can operate with an input-to-output differential voltage that is lower than the typical series regulator (approximately 2 V). Operation at lower differential voltages allows for the use of lower voltage inputs and better efficiency.

Output Noise Voltage

The RMS output voltage with constant output current and constant input voltage, often expressed as a percentage of the output voltage. Output noise voltage is always specified over a given range of frequencies.

Output Impedance

The ratio of the change in output voltage to the change in output current during normal operation. A lower value indicates better regulation of the output voltage. Output impedance is a function of frequency; at f=0, this becomes output resistance.

Output Regulation (Load Regulation)

The change in output voltage due to a change in load current, often expressed as a percentage of the output voltage.

Output Voltage Change With Temperature

The change in the output voltage due to a change in temperature, often expressed in parts per million per °C.

Output Voltage Long-Time Drift

The change in output voltage over a given long period of time, such as 100 hours or one year.

Peak Output Current

The maximum output current that can be obtained from the regulator due to the limits of the circuitry within the regulator.

Reference Voltage

The voltage (usually fixed) that is compared with the feedback voltage to control the regulator. The output tolerance of the regulator is determined primarily by the tolerance of this voltage.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage, usually expressed in dB. This is the reciprocal of ripple sensitivity. Ripple rejection is a function of frequency and typically decreases as frequency increases.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage to the peak-to-peak input ripple voltage usually expressed in dB. This is the reciprocal of ripple rejection.

Series Regulator

A circuit that regulates the output voltage by controlling the impedance of an active device, operating in a linear mode, in series with the output.

Short-Circuit Output Current

The output current of the regulator with the output shorted to ground.

Standby Current

The input current drawn by a regulator, with a shutdown or enable terminal, when the output voltage is disabled and with no reference voltage load.

Temperature Coefficient of Output Voltage ($\propto V_{IO}$)

The average value of the ratio of the change in output voltage to the change in temperature over the total temperature range, often expressed as parts per million per °C.

SHUNT REGULATORS

Anode

The terminal of the regulator from which load current flows when the regulator is biased for regulation.

Cathode

The terminal of the regulator that sinks external load current when the regulator is biased for regulation.

Dynamic Impedance (Z_{KA})

The ratio of a change in voltage across the regulator to the corresponding change in current through the regulator when biased for regulation. This is a function of frequency; at f=0, this becomes dynamic resistance.

Noise Voltage (V_n)

The RMS output voltage with constant output current and constant input voltage, often expressed as a percentage of the output voltage. Output noise voltage is always specified over a given range of frequencies.

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)

The voltage at the reference input terminal with respect to the anode terminal.

Regulator Current (I_Z)

The allowable range of dc current through the regulator when it is biased for regulation.

Regulator Voltage (V_Z)

The dc voltage from cathode to anode of the regulator.

Shunt Regulator

A device that has a voltage-current characteristic similar to that of a voltage-regulator diode. The device controls the output voltage by sinking excess current, flowing through a series resistance, away from the load. It is normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) that varies so as to control the voltage across the device to a constant value.

Temperature Coefficient of Reference Voltage ($\propto V_{ref}$)

The ratio of the average change in reference voltage to the change in temperature over the total temperature range. This value can be stated in parts per million per °C (ppm/°C) or as a percentage of the reference voltage.

SWITCHING REGULATORS

Bode Plot

A design aid used to visualize a transfer function consisting of a logarithmic horizontal scale for frequency and a linear vertical scale for gain in dB or phase in degrees.

Charge Pump

A converter topology that uses the transfer of charge through one or more capacitors to generate an output voltage that is higher than the input voltage.

CSA

Canadian Standards Association, an independent organization that establishes and tests safety standards for electronic systems and components in Canada.

Compensation Network

The components connected around the error amplifier of a switching regulator which tailor the frequency response of the control loop. The compensation network reduces phase shift around the control loop so as to achieve sufficient phase margin for stability.

Conditionally Stable

Description of a control loop that has a phase shift of 360° at some frequency less than the unity-gain frequency, but has a phase shift of less than 360° at unity gain. This loop oscillates when the gain is reduced to unity at the frequency where the phase shift is 360°. A reduction in gain is possible at startup, under abnormal load conditions, or as the components age.

Continuous Mode

A conduction mode in which current in the inductor or transformer of the converter flows during the entire cycle.

Converter (dc-dc)

A network of reactive components and switching elements that transforms power from one dc voltage level to another. The circuit may or may not provide isolation from the input to the output.

Crossover Frequency

The frequency at which the loop response of the regulator drops to unity gain (0 dB). Also known as the unity-gain bandwidth of the converter or unity-gain frequency. This frequency determines the response time for transient recovery.

Cross Regulation

The change in output voltage of one output of a multiple output power supply caused by a load change on another output; usually expressed in percent.

Crow Bar Circuit

A protection circuit the prevents excessive output voltage from reaching the load by shorting the output to ground. Typically, a crow bar circuit employs an semiconductor-controller rectifier (SCR) to short the output to ground and a series fuse to break the circuit before the regulator is damaged.

Current-Mode PWM Control

A PWM control technique consisting of two feedback loops; an inner loop that senses the inductor current and an outer loop that senses the output voltage and is used as a reference for the inner loop control. Current-mode control improves the stability of the control loop of many converter topologies, and provides various other benefits such as pulse-by-pulse current limiting.

Dead Time

A fixed, load-independent off-time between output pulses of a switching regulator, sometimes referred to as blanking time. Dead time control is employed to limit the maximum duty cycle of a converter to prevent damage caused by such occurrences as crossover conduction.

Discontinuous Mode

A conduction mode in which current in the inductor or transformer of the converter drops to zero and remains at zero for a finite period of time during each cycle.

Duty Cycle

The ratio of on-time of the switching element to the operating period of this element.

Dynamic Response (Transient Response)

Output voltage change that occurs in response to a step change in load current or line voltage.

Efficiency

Ratio of the total output power divided by the total input power of a power supply, usually expressed as a percentage and measured at full-rated load current and at nominal input voltage.

ESL

Equivalent Series Inductance, the parasitic inductance in series with the ideal capacitance within a real capacitor.

ESR

Equivalent Series Resistance, the parasitic resistance in series with the ideal capacitance within a real capacitor, originating from the lead resistance, terminal losses, etc.

Faraday Shield

An electrostatic shield within transformers that reduces both coupling capacitance between windings and output common-mode noise. This shield is placed between the primary and secondary windings.

(Input Voltage) Feedforward Compensation

A technique to increase the loop response to supply voltage changes by controlling the ramp level as a function of the input voltage.

Gain Margin

The amount that loop gain is reduced below zero dB at the frequency where there is exactly 360° of phase shift around the control loop. This is the amount of gain that would need to be added to the loop in order for it to oscillate.

Holdup Time

The period of time that a power supply output voltage remains within its specified operating conditions after loss of input power.

Input Transient (Line Transient)

A voltage spike or step change in the input of a power supply.

Inverter

A type of switching converter that accepts dc input power and changes it to ac power.

Line Transient

See input transient.

Load Regulation

The dc change in output voltage caused by a change in output load, often express as a percentage of the nominal output voltage.

Loop Response

The frequency response of the regulator, often expressed as a Bode plot. The total loop response is the small-signal, open-loop transfer function around the control loop and is determined by the total gain and the phase shift of the output filter, output sensing network, error amplifier (with its compensation network), and the power modulator stage.

Off-Line Power Supply

A power supply that operates directly from the ac mains. The input voltage is rectified and filtered to a high dc voltage before any isolation transformer.

Output Regulation

See load regulation.

Overcurrent Protection

A protection circuit that prevents damage to the regulator by sensing an overcurrent condition and limiting excessive current flow or shutting down the regulator.

Overvoltage

A condition in which the output voltage magnitude is greater than the maximum specified limit. For both positive and negative regulators, the voltage is farther away from zero.

Output Impedance

The ratio of the change in output voltage to the change in output current during normal operation. A lower value indicates better regulation of the output voltage. Output impedance is a function of frequency; at f=0, this becomes output resistance.

Parallel Operation

A multiple output switching configuration in which two or more output stages supply power to the same load simultaneously. This configuration is used when one supply cannot meet the power demands of the load or for redundancy in case of failure of one supply.

Phase Margin

The difference between the phase shift around the control loop at the unity gain frequency and 360°. When the phase shift is less than 360°, the phase margin is positive. Generally, at least 45° of phase margin is needed to ensure stability over manufacturing variations and to reduce overshoot.

Pole

A point where the open-loop transfer function of the control loop asymptotically approaches infinity as a result of a term in the denominator approaching zero. A frequency breakpoint of the loop response that causes 20 dB per decade reduction in gain and a shift of 90° in phase margin.

Post Regulator

A circuit on the output of the power supply that improves the output regulation and/or reduces ripple or noise.

Power Factor Correction (PFC)

A design technique the changes the input current waveform of a power supply from a pulsed waveform (the result of charging the input capacitor) to a sinusoidal waveform that reduces EMI injected into the source. Power factor is proportional to the percentage of time during the cycle that current flows in the input. A power factor of 1 indicates a sine wave input, while a value less than 1 indicates the presence of harmonic current in the input circuit.

Power Good Signal

A signal generated within a power supply to indicate that the output of the supply is operating within its specified tolerances.

Power Modulator Stage

The section of the regulator that processes the power from one dc level to another dc level. This includes the comparator that converts the error signal to pulse width information, the power switch, and the transformer/inductor.

Power Modulator Gain

The small-signal gain of the power modulator stage. Because the modulator is a switched circuit, state-space averaging techniques are required to derive its gain, but the gain can be approximated as the maximum change in output voltage divided by the maximum change in ramp voltage, usually expressed in dB.

Pulse-Width-Modulation (PWM) Control

A switching regulator technique in which regulation is accomplished by changing the duty cycle of the power switch.

Push-Pull Operation

A dual output switching configuration in which two power switches conduct alternately.

Ramp

The output voltage of the oscillator stage of a voltage-mode controller that is compared to the error signal in the comparator to generate the duty cycle control signal. The peak-to-peak level of the ramp determines the gain of the modulator stage.

Remote Sensing

A design technique to reduce output-voltage error induced by the impedance of the output-load cables by including the load cables within the feedback loop. This is done by connecting separate voltage sensing cables at the load that do not carry any load current.

Resonant Mode

A control technique that regulates the output by controlling the operating frequency while turning off the power switch when the current through it (ZCS) or the voltage across it (ZVS) is zero.

Right-Half-Plane Zero

A frequency breakpoint of the loop response that causes the gain to rise 20 dB per decade but causes the phase to fall 90°. This phenomenon is present in continuous-mode boost and flyback converters and is extremely difficult to compensate for.

Single-Ended Operation

A single output switching configuration.

Soft Start

A protection circuit that prevents current surges during power up and protects against false signals that might be generated by the control circuit when power is applied.

SMPS

Switch-mode power supply. Any of a class of power converters that control the output voltage by switching the input voltage.

Synchronous Rectification

A design technique to increase converter efficiency by reducing the conduction losses in the commutation rectifier of a converter. This is typically done by replacing the diode with a transistor that is turned on when the rectifier would be expected to conduct.

Temperature Coefficient

The average change in a parameter, such as output voltage, per degree of temperature change, usually expressed as a percentage over the specified temperature range or ppm/°C.

Transient Recovery Time

The time required for the output of a power supply to settle back into its specified tolerance range after a step change in load current or line voltage. This is also called settling time.

Transient Response

The response of the converter to step changes in load or line variations.

TUV

Technischer Uberwachungs-Verin, a German organization approved for testing products to VDE standards.

UL

Underwriters Laboratories, the U.S. independent organization that conducts safety testing of products to established standards.

Unconditionally Stable

Description of a control loop that generally does not oscillate under any line/load conditions or when the loop gain is reduced. An unconditionally stable loop has less than 360° of phase shift for all frequencies less than or equal to unity-gain frequency.

Undervoltage

A condition in which the output voltage magnitude is less than the minimum specified limit. For both positive and negative regulators, the voltage is closer to zero.

Undervoltage Lockout (UVLO)

A protection circuit that prevents switching outputs from turning on until a certain supply voltage threshold is reached so as to prevent excessive dissipation on the switches and possible damage to the circuit.

Variable Frequency Control

A switching regulation technique in which a fixed output on-time or off-time is maintained. Regulation is accomplished by changing the output frequency to vary the duty cycle.

VDE

Verband Deutscher Elektrotechniker, the German organization that sets standards for product safety and noise emissions and also tests and certifies products to those standards.

Voltage-Mode Control

A PWM control technique consisting of a single feedback loop that controls the output voltage by comparing it to a fixed reference voltage.

Zero

A point where the open-loop transfer function of the control loop approaches zero as a result of a term in the numerator approaching zero. A frequency breakpoint of the loop response where the gain rises 20 dB per decade and a 90° rise in the phase margin.

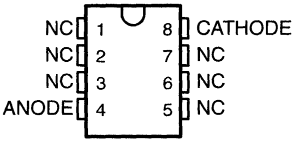
Contents

LM185-1.2, LM285-1.2, LM385-1.2, LM385B-1.2, LM385Y-1.2
MICROPOWER VOLTAGE REFERENCES

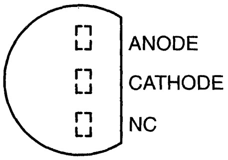
SLVS075B – APRIL 1989 – REVISED AUGUST 1995

- **Operating Current Range**
  - **LM185 . . . 10 µA to 20 mA**
  - **LM285 . . . 10 µA to 20 mA**
  - **LM385 . . . 15 µA to 20 mA**
  - **LM385B . . . 15 µA to 20 mA**
- **1% and 2% Initial Voltage Tolerance**
- **Reference Impedance**
  - **LM185 . . . 0.6 Ω Max at 25°C**
  - **LM385 . . . 1 Ω Max at 25°C**
  - **All Devices . . . 1.5 Ω Max Over Full**
  - **Temperature Range**
- **Very Low Power Consumption**
- **Applications:**
  - **Portable Meter References**
  - **Portable Test Instruments**
  - **Battery-Operated Systems**
  - **Current-Loop Instrumentation**
  - **Panel Meters**
- **Designed to be Interchangeable With National LM185-1.2, LM285-1.2, and LM385-1.2**

D PACKAGE
(TOP VIEW)

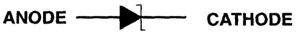


LP PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



description

These micropower two-terminal band-gap voltage references operate over a 10-µA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The LM185-1.2 series band-gap reference has low noise and long-term stability.

The LM185-1.2 series design makes the devices exceptionally tolerant of capacitive loading and thus easier to use in most reference applications. The wide dynamic operating temperature range accommodates varying current supplies with excellent regulation.

The extremely low-power drain of the LM185-1.2 series makes them useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry with battery life approaching shelf life. The wide operating current range allows them to replace older references with tighter-tolerance parts.

The LM185-1.2 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM285-1.2 is characterized for operation from −40°C to 85°C. The LM385-1.2 and LM385B-1.2 are characterized for operation from 0°C to 70°C.

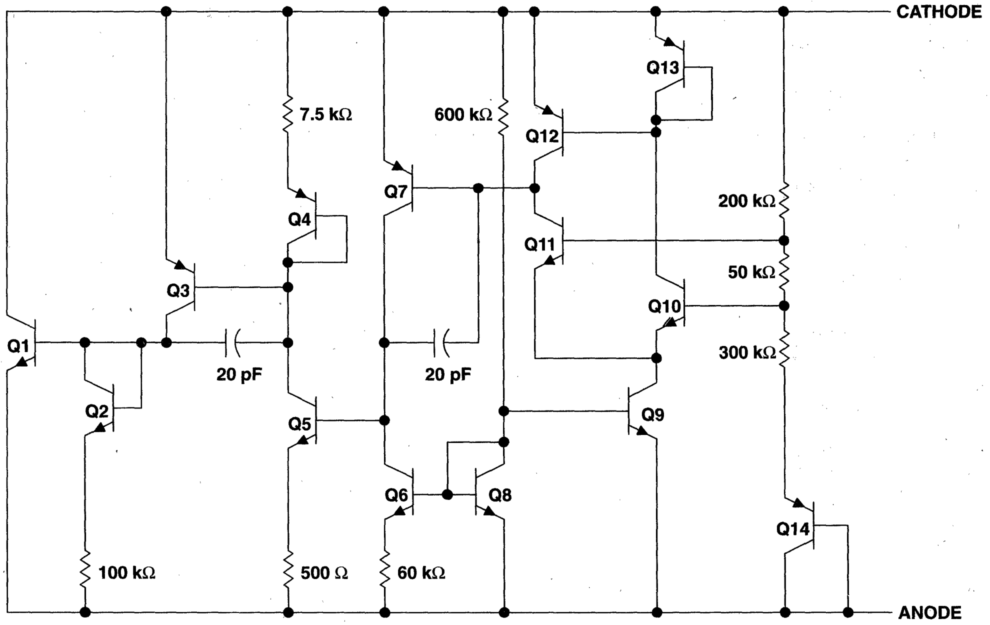
AVAILABLE OPTIONS

T_A	V_Z TOLERANCE	PACKAGED DEVICES†		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 70°C	2%	LM385D-1.2	LM385LP-1.2	LM385Y-1.2
	1%	LM385BD-1.2	LM385BLP-1.2	
−40°C to 85°C	1%	LM285D-1.2	LM285LP-1.2	
−55°C to 125°C	1%	LM185D-1.2	LM185LP-1.2	

† For ordering purposes, the decimal point in the part number must be replaced with a hyphen (i.e., show the -1.2 suffix as "-1-2").
The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM385DR-1-2).
The chip form is tested at T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic



NOTE A: Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range†

Reverse current, I_R .... 30 mA
Forward current, I_F .... 10 mA
Operating free-air temperature range, T_A: LM185-1.2 .... −55°C to 125°C
LM285-1.2 .... −40°C to 85°C
LM385-1.2, LM385B-1.2 .... 0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

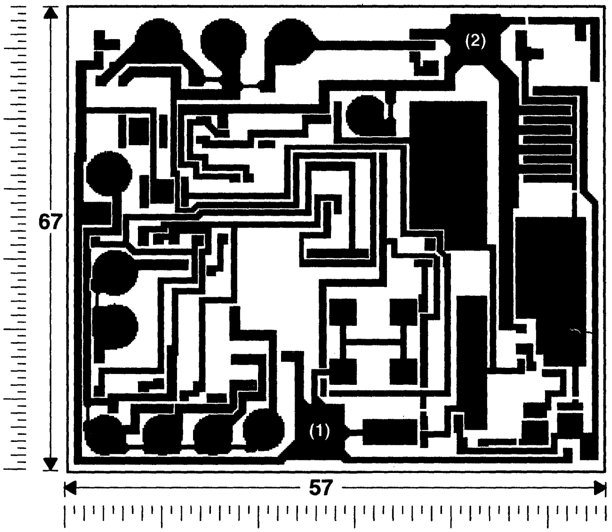
recommended operating conditions

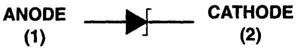
		MIN	MAX	UNIT
Reference current, I_Z		0.01	20	mA
Operating free-air temperature range, T_A	LM185-1.2	−55	125	°C
	LM285-1.2	−40	85	
	LM385-1.2, LM385B-1.2	0	70	

LM385Y-1.2 chip information

This chip, when properly assembled, displays characteristics similar to the LM385-1.2 (see electrical tables). Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL NUMBERS APPLY TO LP PACKAGE ONLY

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LM185-1.2 LM285-1.2			LM385-1.2			LM385B-1.2			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = I min to 20 mA‡	25°C	1.223	1.235	1.247	1.21	1.235	1.26	1.223	1.235	1.247	V
α_{VZ}	Average temperature coefficient of reference voltage§	I_Z = I min to 20 mA‡	25°C		±20			±20			±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = I min to 1 mA‡	25°C			1			1			1	mV
			Full range			1.5			1.5			1.5	
		I_Z = 1 mA to 20 mA	25°C			12			20			20	
			Full range			30			30			30	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA	25°C		±20			±20			±20		ppm/khr
I_{Z}min	Minimum reference current		Full range		8	10		8	15		8	15	µA
z_Z	Reference impedance	I_Z = 100 µA, f = 25 Hz	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C		60			60			60		µV

† Full range is −55°C to 125°C for the LM185-1.2, −40°C to 85°C for the LM285-1.2, and 0°C to 70°C for the LM385-1.2 and LM385B-1.2.

‡ I min = 10 µA for the LM185-1.2 and LM285-1.2. I_{min} = 15 µA for the LM385-1.2 and LM385B-1.2.

§ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	LM385Y-1.2			UNIT
			MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 15 µA to 20 mA	1.21	1.235	1.26	V
α_{VZ}	Average temperature coefficient of reference voltage†	I_Z = 15 µA to 20 mA		±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 15 µA to 1 mA			1	mV
		I_Z = 1 mA to 20 mA			20	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA		±20		ppm/khr
$I_Z$min	Minimum reference current			8	15	µA
z_Z	Reference impedance	I_Z = 100 µA		0.4	1	Ω
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz		60		µV

† The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REVERSE CURRENT vs REVERSE VOLTAGE

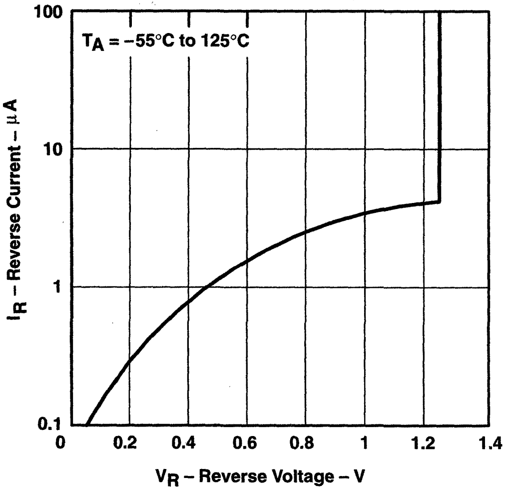


Figure 1

REFERENCE VOLTAGE CHANGE vs REVERSE CURRENT

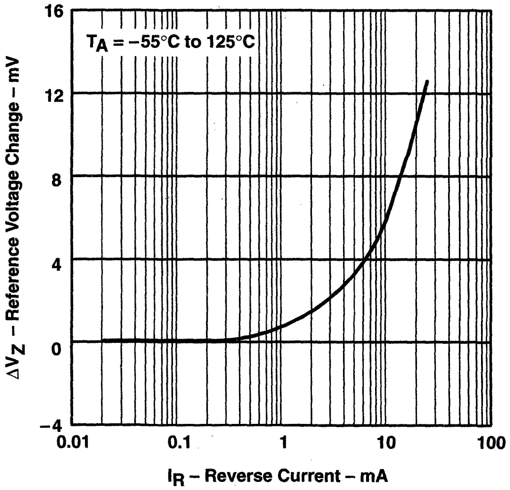


Figure 2

FORWARD VOLTAGE vs FORWARD CURRENT

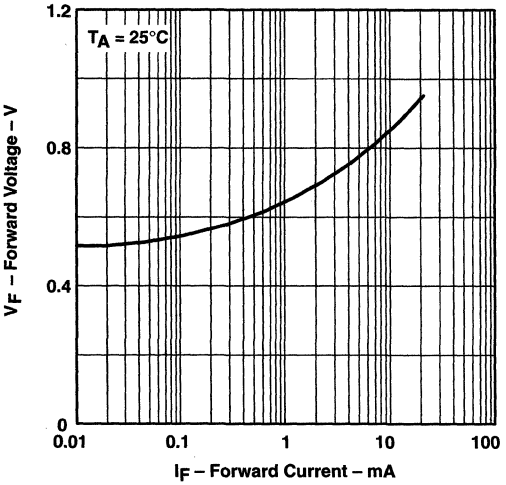


Figure 3

REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

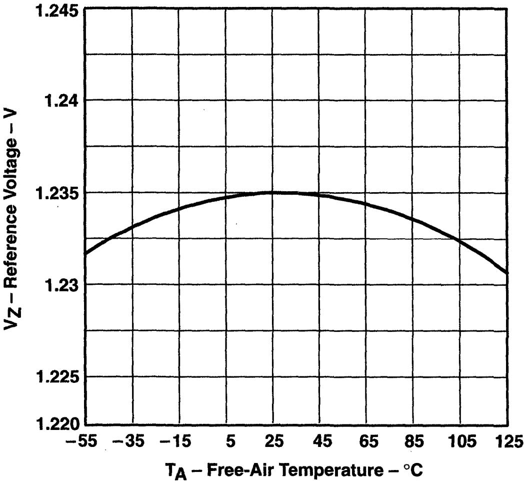


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

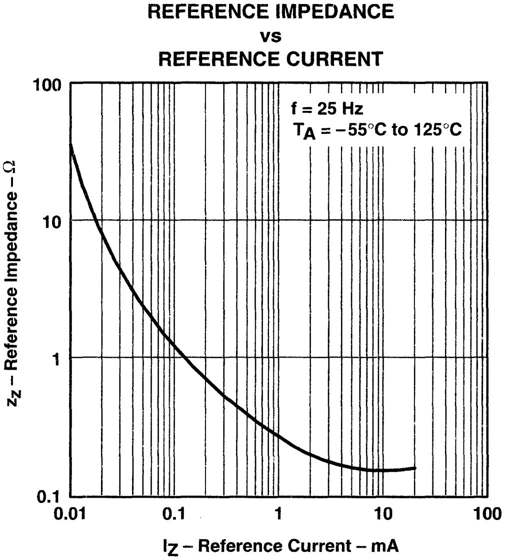

Figure 5

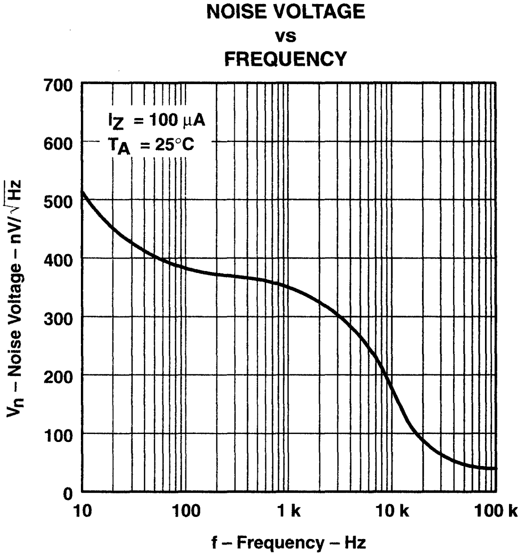

Figure 6

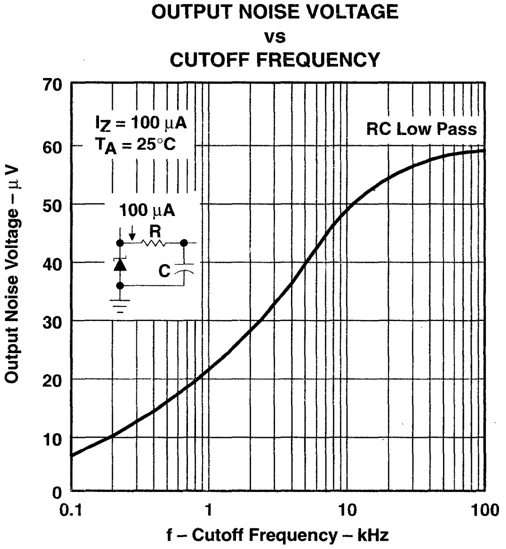

Figure 7

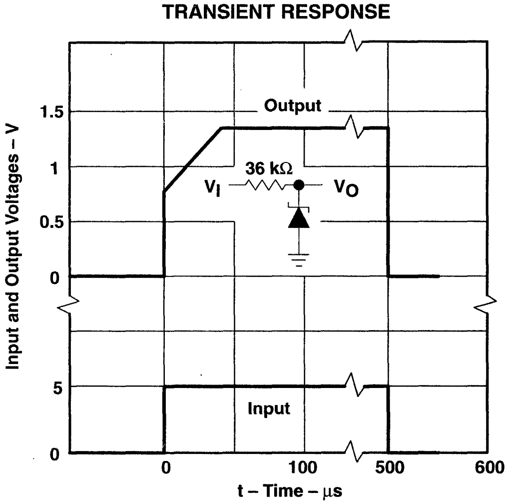

Figure 8

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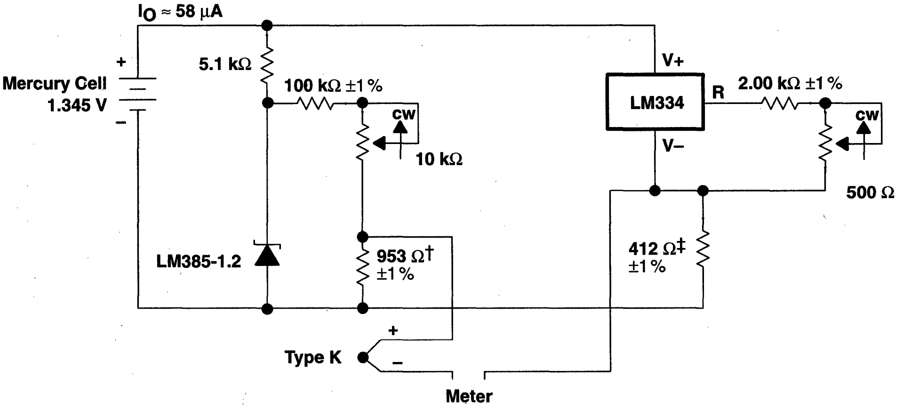
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



† Adjust for 11.15 mV at 25°C across 953 Ω
‡ Adjust for 12.17 mV at 25°C across 412 Ω

Figure 9. Thermocouple Cold-Junction Compensator

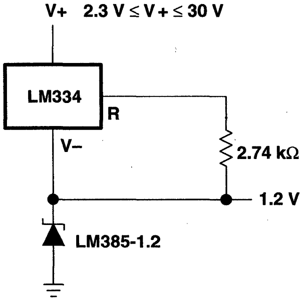


Figure 10. Operation Over a Wide Supply Range

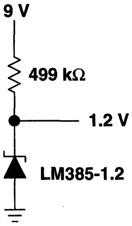


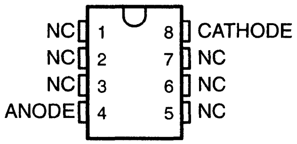
Figure 11. Reference From a 9-V Battery

LM185-2.5, LM285-2.5, LM385-2.5, LM385B-2.5, LM385Y-2.5
MICROPOWER VOLTAGE REFERENCES

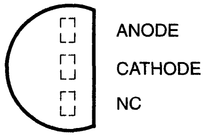
SLVS023D – JANUARY 1989 – REVISED AUGUST 1995

- **Operating Current Range . . . 20 μA to 20 mA**
- **1.5% and 3% Initial Voltage Tolerance**
- **Reference Impedance**
  - **LM185 . . . 0.6 Ω Max at 25°C**
  - **LM385 . . . 1 Ω Max at 25°C**
  - **All Devices . . . 1.5 Ω Max Over Full**
  - **Temperature Range**
- **Very Low Power Consumption**
- **Applications:**
  - **Portable Meter References**
  - **Portable Test Instruments**
  - **Battery-Operated Systems**
  - **Current-Loop Instrumentation**
  - **Panel Meters**
- **Designed to be Interchangeable With National LM185-2.5, LM285-2.5, and LM385-2.5**

D PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)



NC – No internal connection

symbol

description

These micropower two-terminal band-gap voltage references operate over a 20-μA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The LM185-2.5 series band-gap reference has low noise and long-term stability.

The LM185-2.5 series design makes these devices exceptionally tolerant of capacitive loading and thus easier to use in most reference applications. The wide dynamic operating temperature range accommodates varying current supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 series makes them useful for micropower circuitry. These voltage references can make portable meters, regulators, or general-purpose analog circuitry with battery life approaching shelf life. The wide operating current range allows them to replace older references with tighter tolerance parts.

The LM385-2.5 and LM385B-2.5 are characterized for operation from 0°C to 70°C. The LM285-2.5 is characterized for operation from −40°C to 85°C. The LM185-2.5 is characterized for operation over the full military temperature range of −55°C to 125°C.

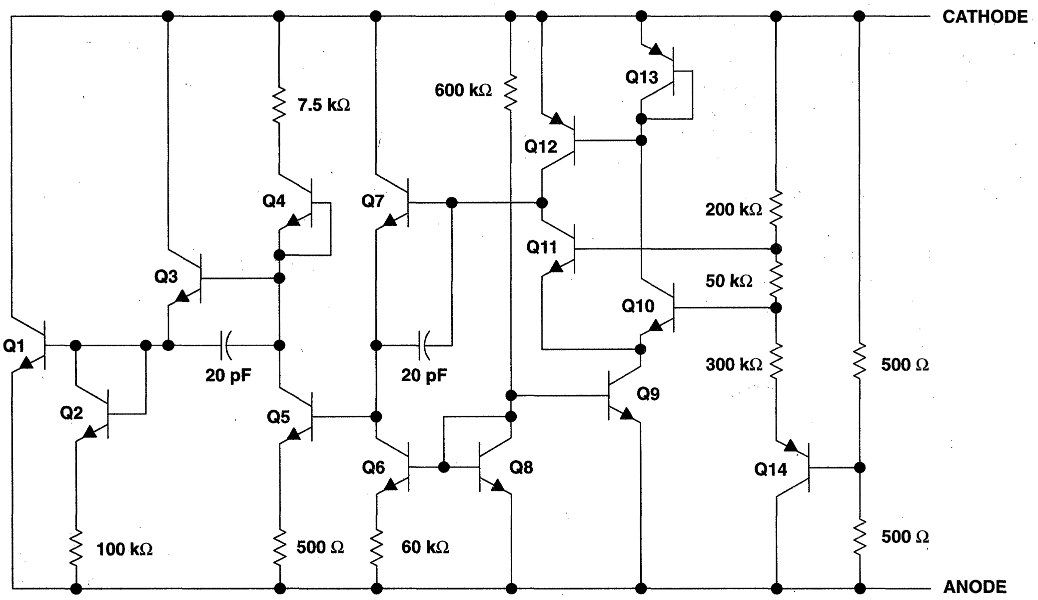
AVAILABLE OPTIONS

T_A	V_Z TOLERANCE	PACKAGED DEVICES†		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 70°C	3%	LM385D-2.5	LM385LP-2.5	LM385Y-2.5
	1.5%	LM385BD-2.5	LM385BLP-2.5	
−40°C to 85°C	1.5%	LM285D-2.5	LM285LP-2.5	
−55°C to 125°C	1.5%	LM185D-2.5	LM185LP-2.5	

† For ordering purposes, the decimal point in the part number must be replaced with a hyphen (i.e., show the -2.5 suffix as "-2-5").

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM385DR-2-5).

schematic



NOTE A: All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range†

Reverse current, I_R	30 mA
Forward current, I_F	10 mA
Operating free-air temperature range, T_A: LM185-2.5	−55°C to 125°C
LM285-2.5	−40°C to 85°C
LM385-2.5, LM385B-2.5	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

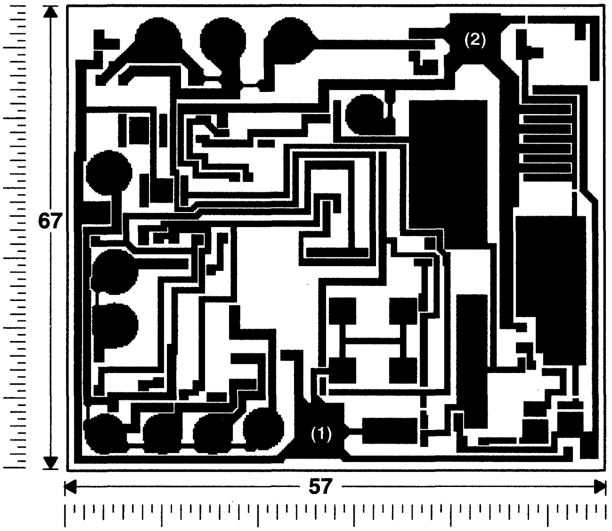
recommended operating conditions

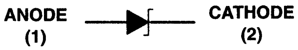
		MIN	MAX	UNIT
Reference current, I_Z		0.02	20	mA
Operating free-air temperature range, T_A	LM185-2.5	−55	125	°C
	LM285-2.5	−40	85	
	LM385-2.5, LM385B-2.5	0	70	

LM385Y-2.5 chip information

This chip, when properly assembled, displays characteristics similar to the LM385-2.5 (see electrical tables). Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL NUMBERS APPLY
TO LP PACKAGE ONLY

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LM185-2.5 LM285-2.5			LM385-2.5			LM385B-2.5			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 20 µA to 20 mA	25°C	2.462	2.5	2.538	2.425	2.5	2.575	2.462	2.5	2.538	V
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 20 µA to 20 mA	25°C		±20			±20			±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 20 µA to 1 mA	25°C			1			2			2	mV
			Full range			1.5			2			2	
		I_Z = 1 µA to 20 mA	25°C			10			20			20	
			Full range			30			30			30	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA	25°C		±20			±20			±20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range		8	20		8	20		8	20	µA
z_Z	Reference impedance	I_Z = 100 µA	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C		120			120			120		µV

† Full range is 0°C to 70°C for the LM385-2.5 and LM385B-2.5, –40°C to 85°C for the LM285-2.5, and –55°C to 125°C for the LM185-2.5.

‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

electrical characteristics at $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LM385Y-2.5			UNIT
			MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 20 µA to 20 mA	2.462	2.5	2.575	V
α_{VZ}	Average temperature coefficient of reference voltage†	I_Z = 20 µA to 20 mA		±20		ppm/°C
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA		±20		ppm/khr
z_Z	Reference impedance	I_Z = 100 µA		0.4	1	Ω
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz		120		µV

† The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

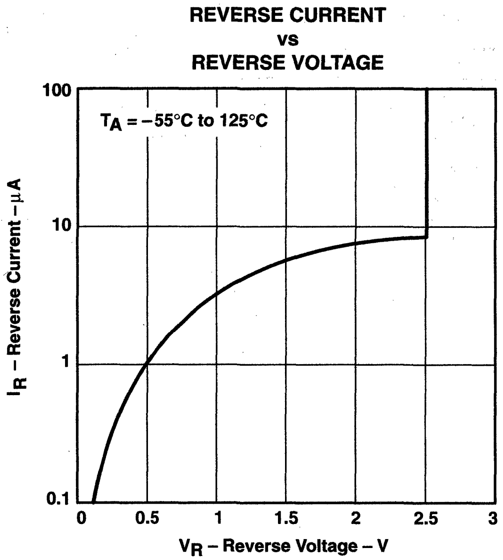

REVERSE CURRENT
vs
REVERSE VOLTAGE

Figure 1

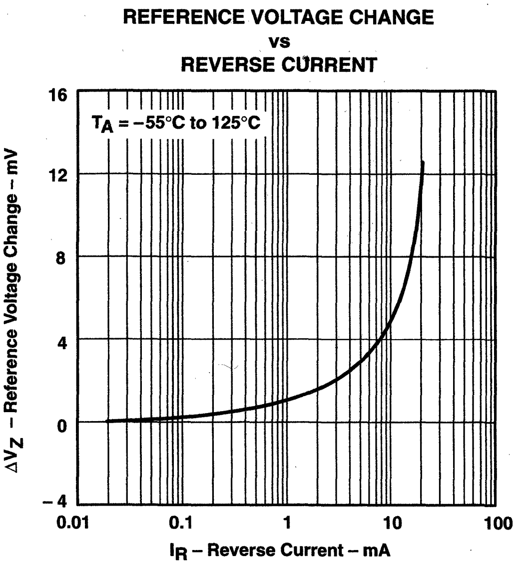

REFERENCE VOLTAGE CHANGE
vs
REVERSE CURRENT

Figure 2

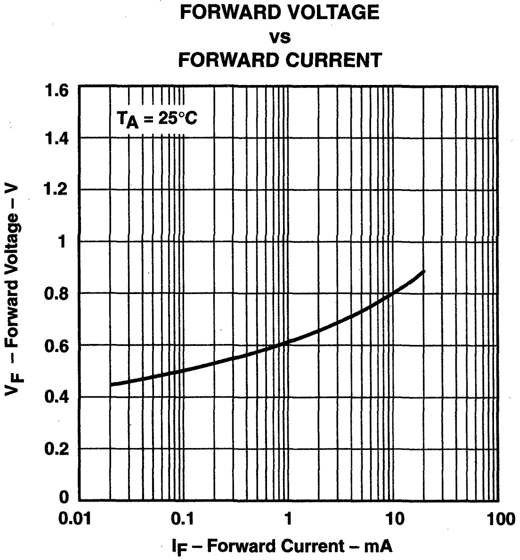

FORWARD VOLTAGE
vs
FORWARD CURRENT

Figure 3

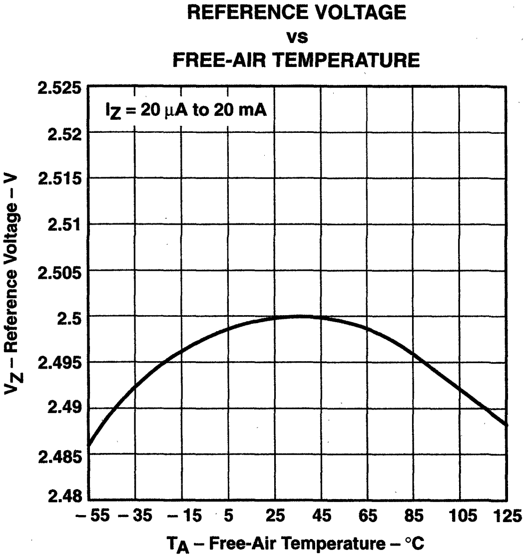

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REFERENCE IMPEDANCE vs REFERENCE CURRENT

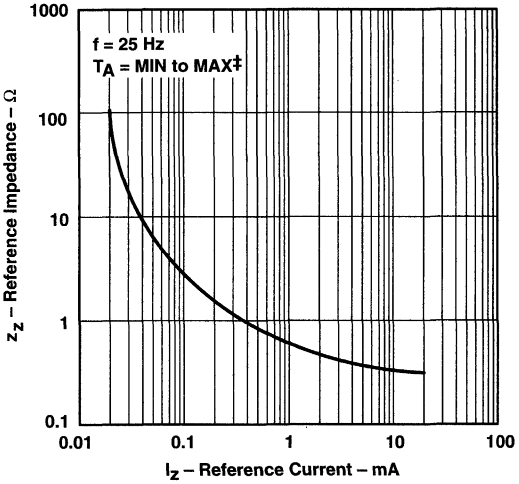

Figure 5

REFERENCE IMPEDANCE vs FREQUENCY

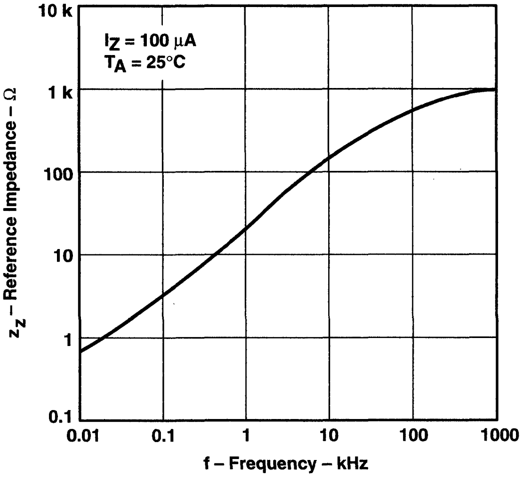

Figure 6

NOISE VOLTAGE vs FREQUENCY

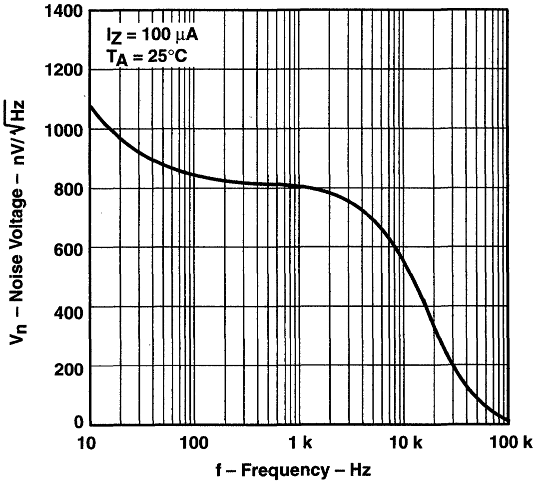

Figure 7

FILTERED RMS OUTPUT NOISE VOLTAGE vs FREQUENCY

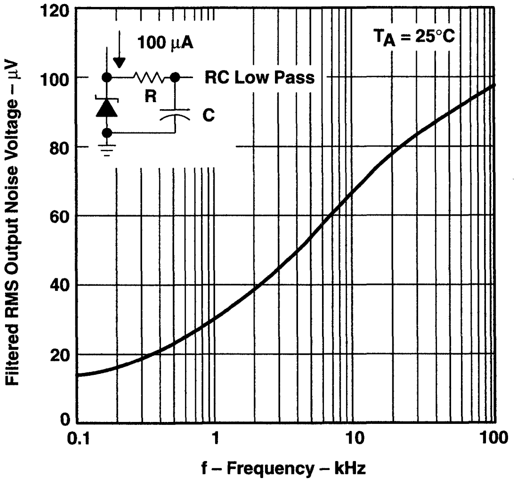

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TYPICAL CHARACTERISTICS†

TRANSIENT RESPONSE

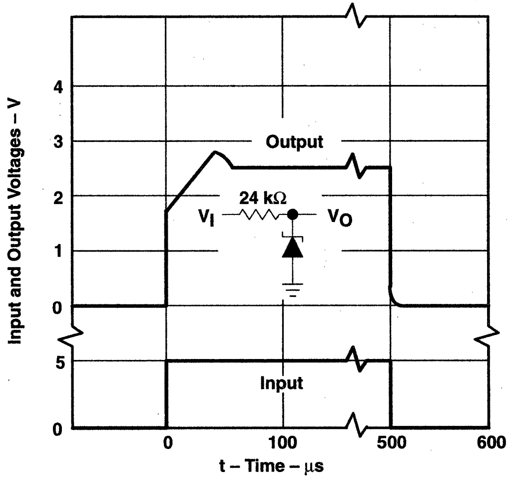

Figure 9

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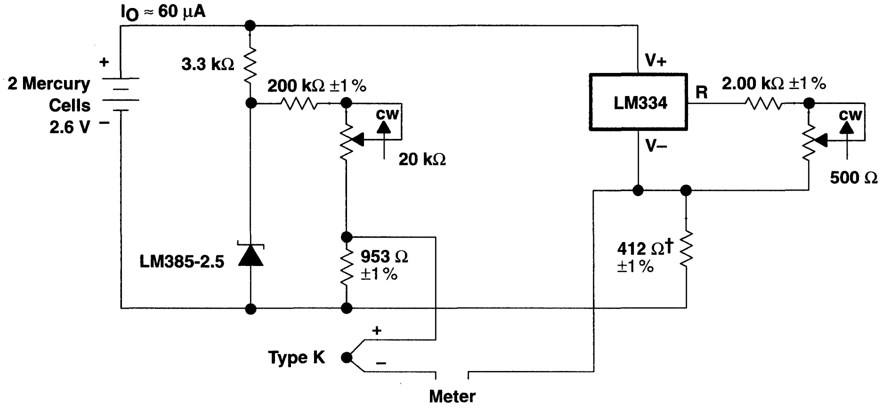
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



†Adjust for 12.17 mV at 25°C across 412 Ω

Figure 10. Thermocouple Cold-Junction Compensator

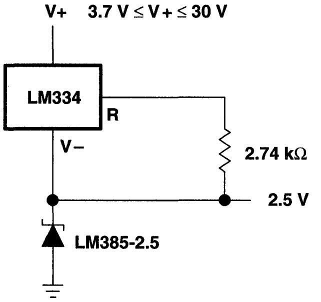


Figure 11. Operation Over a Wide Supply Range

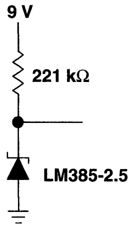


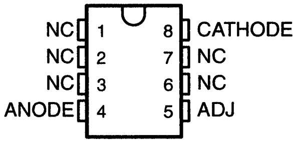
Figure 12. Reference From a 9-V Battery

LM236-2.5, LM336-2.5, LM336Y-2.5
2.5-V INTEGRATED REFERENCE CIRCUITS

SLVS063A – NOVEMBER 1988 – REVISED AUGUST 1995

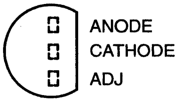
- **Low Temperature Coefficient**
- **Wide Operating Current . . . 400 μA to 10 mA**
- **0.27-Ω Dynamic Impedance**
- **±1% Tolerance Available**
- **Specified Temperature Stability**
- **Easily Trimmed for Minimum Temperature Drift**
- **Fast Turn-On**
- **Three-Lead Transistor Package**

D PACKAGE
(TOP VIEW)



NC-No internal connection

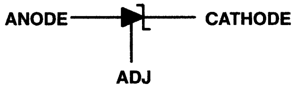
LP PACKAGE
(TOP VIEW)



description

The LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5-V shunt regulator diodes. These monolithic references operate as low temperature coefficient 2.5-V zeners with a 0.2-Ω dynamic impedance. A third terminal provided on the circuit allows the reference voltage and temperature coefficient to be easily trimmed.

symbol



The series are useful as precision 2.5-V low-voltage references (V_Z) for digital voltmeters, power supplies, or operational amplifier circuitry. The 2.5-V voltage reference makes it convenient to obtain a stable reference from 5-V logic supplies. Since the series operate as shunt regulators, they can be used as either positive or negative voltage references.

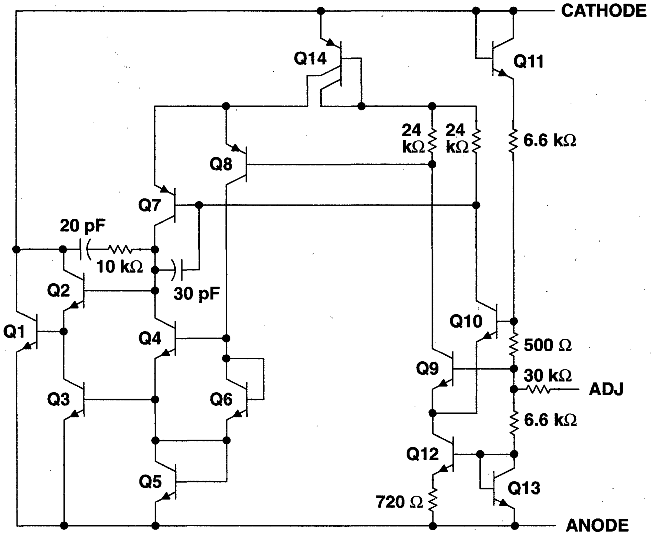
The LM236-2.5 is characterized for operation from –25°C to 85°C. The LM336-2.5 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 70°C	LM336D-2.5	LM336LP-2.5	LM336Y-2.5
–25°C to 85°C	LM236D-2.5	LM236LP-2.5	—

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LM336DR-2.5).

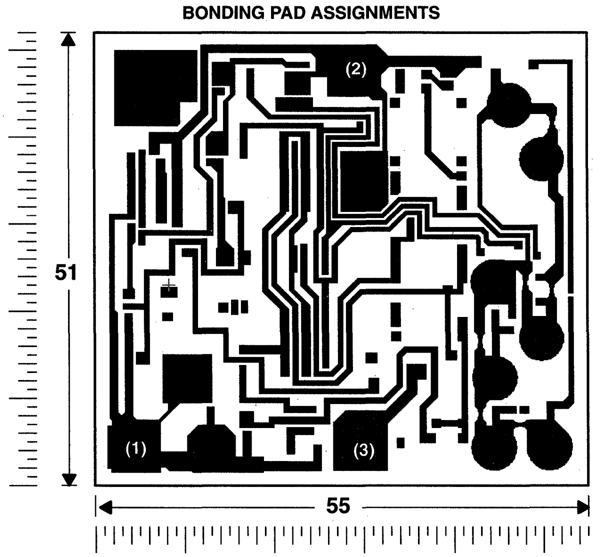
schematic diagram

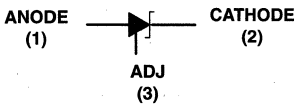


All component values are nominal

LM336Y-2.5 chip information

This chip, when properly assembled, displays characteristics similar to the LM336-2.5 (see electrical tables). Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_Jmax = 150°C$

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Reverse current, I_R		20 mA
Forward current, I_F		10 mA
Operating free-air temperature range, T_A:	LM236-2.5	–25°C to 85°C
	LM336-2.5	0°C to 70°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A‡	LM236-2.5			LM336-2.5			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	LM236, LM336	25°C	2.44	2.49	2.54	2.39	2.49	2.59	V
			LM236A, LM336B		2.465	2.49	2.515	2.44	2.49	2.54	
$\Delta V_{Z(\Delta T)}$	Change in reference voltage with temperature§	V_Z adjusted to 2.490 V, I_Z = 1 mA		Full range		3.5	9		1.8	6	mV
$\Delta V_{Z(\Delta I)}$	Change in reference voltage with current	I_Z = 400 μA to 10 mA		25°C		2.6	6		2.6	10	mV
				Full range		3	10		3	12	
$\Delta V_{Z(\Delta t)}$	Long-term change in reference voltage	I_Z = 1 mA		25°C		20			20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA, f = 1 kHz		25°C		0.2	0.6		0.2	1	Ω
				Full range		0.4	1		0.4	1.4	

‡ Full range is –25°C to 85°C for the LM236-2.5 and 0°C to 70°C for the LM336-2.5.

§ Temperature stability (change in reference voltage with temperature) for these devices is ensured by design. Design limits are specified over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	LM336Y-2.5			UNIT
			MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	2.39	2.49	2.59	V
$\Delta V_{Z(\Delta I)}$	Change in reference voltage with current	I_Z = 400 μA to 10 mA		2.6	10	mV
$\Delta V_{Z(\Delta t)}$	Long-term change in reference voltage	I_Z = 1 mA		20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA, f = 1 kHz		0.2	1	Ω

TYPICAL CHARACTERISTICS

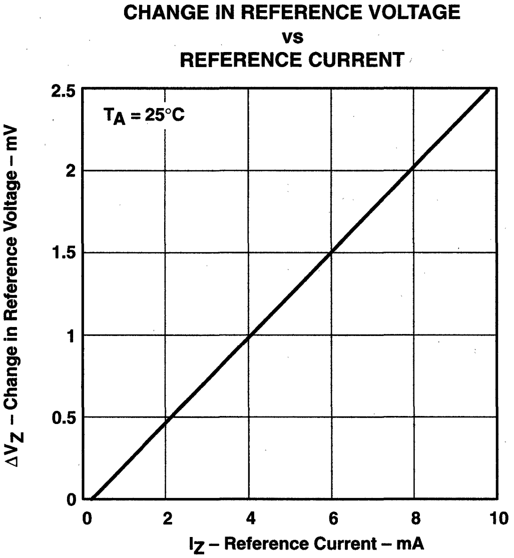


Figure 1

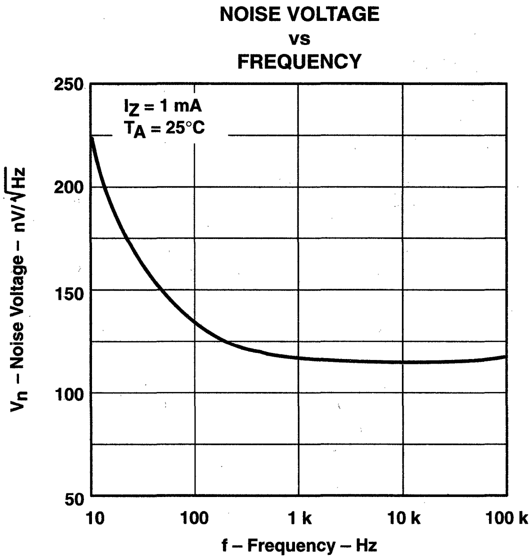


Figure 2

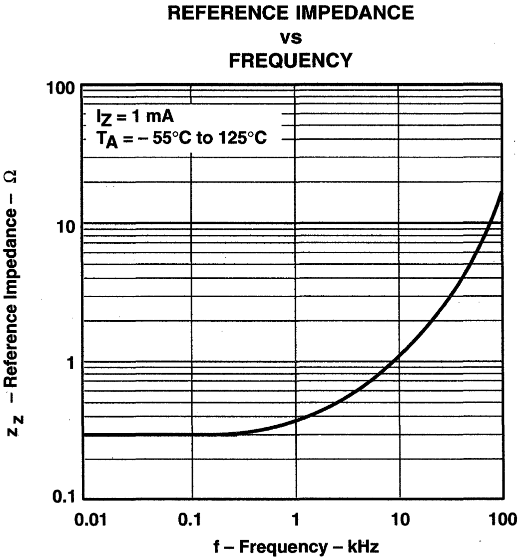


Figure 3

APPLICATION INFORMATION

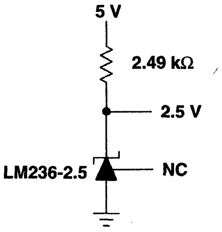
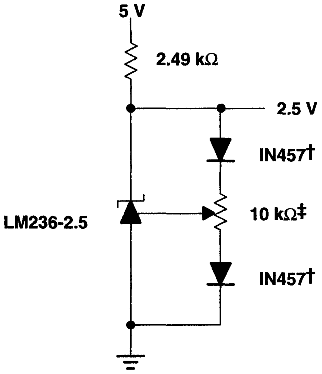


Figure 3. 2.5-V Reference



† Any silicon signal diode
‡ Adjust to 2.49 V

Figure 4. 2.5-V Reference With Minimum Temperature Coefficient

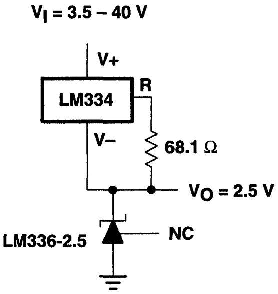


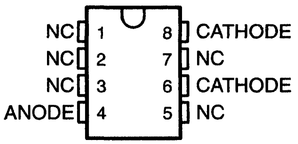
Figure 5. Wide Input Range Reference

LT1004C-1.2, LT1004C-2.5, LT1004M-1.2
LT1004M-2.5, LT1004Y-1.2, LT1004Y-2.5
MICROPOWER INTEGRATED VOLTAGE REFERENCES

SLVS022D – JANUARY 1989 – REVISED AUGUST 1995

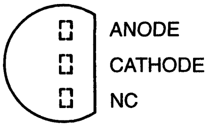
- **Initial Accuracy**
  ±4 mV for LT1004-1.2
  ±20 mV for LT1004-2.5
- **Micropower Operation**
- **Operates up to 20 mA**
- **Very Low Reference Impedance**
- **Applications:**
  - **Portable Meter Reference**
  - **Portable Test Instruments**
  - **Battery-Operated Systems**
  - **Current-Loop Instrumentation**

D PACKAGE
(TOP VIEW)



Terminals 6 and 8 are internally connected.

LP PACKAGE
(TOP VIEW)

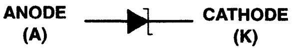


NC – No internal connection

description

The LT1004 micropower voltage reference is a two-terminal band-gap reference diode designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimizing the key parameters in the design, processing, and testing of the device results in specifications previously attainable only with selected units.

symbol



The LT1004 is a terminal-for-terminal replacement for the LM185 series of references with improved specifications. The LT1004 is an excellent device for use in systems in which accuracy was previously attained at the expense of power consumption and trimming.

The LT1004C is characterized for operation from 0°C to 70°C. The LT1004M is characterized for operation over the full military temperature range of –55°C to 125°C.

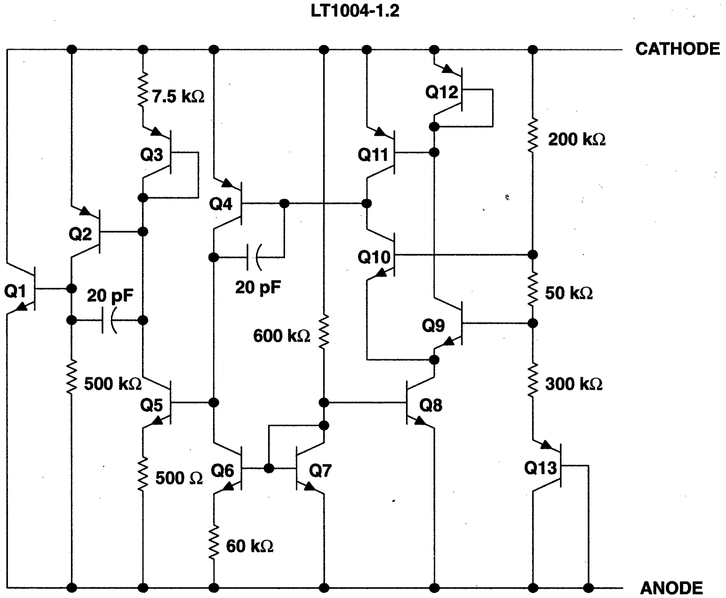
AVAILABLE OPTIONS†

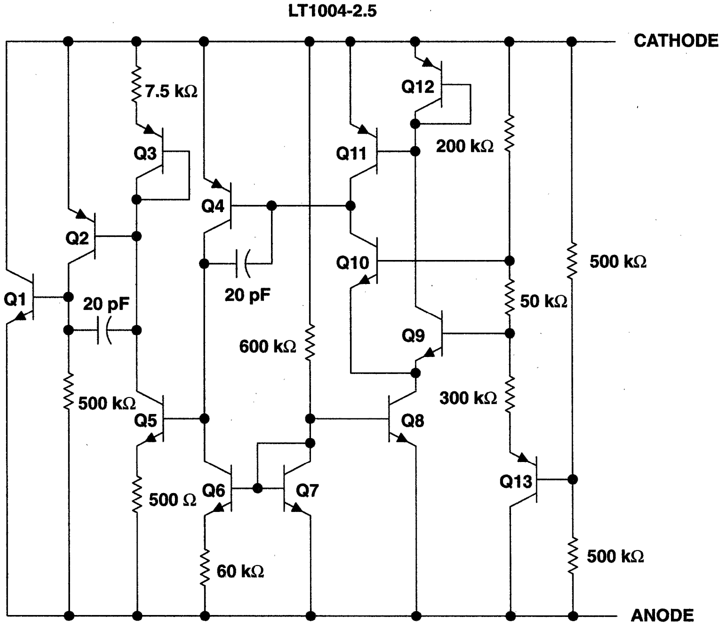
T_A	PACKAGED DEVICES‡			CHIP FORM (Y)
	V_Z TYP	SMALL-OUTLINE (D)	PLASTIC (LP)	
0°C to 70°C	1.2 V	LT1004CD-1.2	LT1004CLP-1.2	LT1004Y-1.2
	2.5 V	LT1004CD-2.5	LT1004CLP-2.5	LT1004Y-2.5
–55°C to 125°C	1.2 V	LT1004MD-1.2	LT1004MLP-1.2	—
	2.5 V	LT1004MD-2.5	LT1004MLP-2.5	

† For ordering purposes, the decimal point in the part number must be replaced with a hyphen (i.e., show the -1.2 suffix as -1-2 and the -2.5 suffix as -2-5).

‡ The packages are available taped and reeled. Add the R suffix to the device type (i.e., LT1004CDR).

schematic



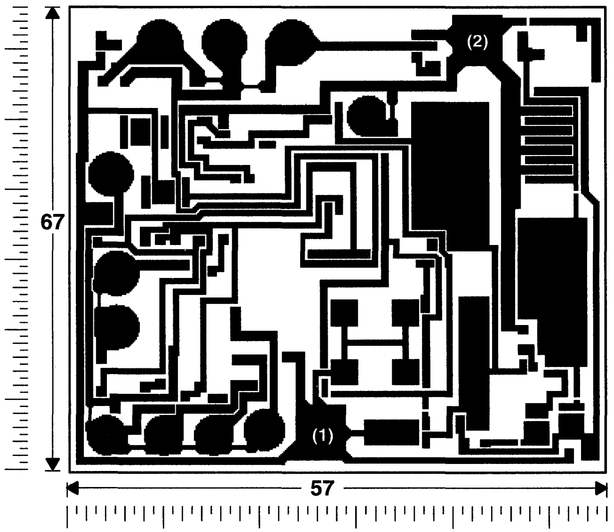


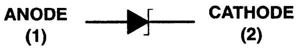
NOTE A: All component values shown are nominal.

LT1004Y-1.2 and LT1004Y-2.5 chip information

This chip, when properly assembled, displays characteristics similar to the LT1004C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

T$_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL NUMBERS APPLY
TO LP PACKAGE ONLY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Reverse current, I_R	30 mA
Forward current, I_F	10 mA
Operating free-air temperature range, T_A: LT1004C	0°C to 70°C
LT1004M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A‡		LT1004-1.2			LT1004-2.5			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 100 µA	25°C		1.231	1.235	1.239	2.48	2.5	2.52	V
			Full range	LT1004C	1.225		1.245	2.47		2.53	
				LT1004M	1.22		1.245	2.46		2.535	
α_{VZ}	Average temperature coefficient of reference voltage§	I_Z = 10 µA	25°C			20					ppm/°C
		I_Z = 20 µA							20		
ΔV_Z	Change in reference voltage with current	I_Z = $I_Z$min to 1 mA	25°C				1			1	mV
			Full range				1.5			1.5	
		I_Z = 1 mA to 20 mA	25°C				10			10	
			Full range				20			20	
$\Delta V_Z/\Delta t$	Long term change in reference voltage	I_Z = 100 µA	25°C			20			20		ppm/khr
$I_Z$min	Minimum reference current		Full range			8	10		12	20	µA
z_Z	Reference impedance	I_Z = 100 µA	25°C			0.2	0.6		0.2	0.6	Ω
			Full range				1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C			60			120		µV

‡ Full range is 0°C to 70°C for the LT1004C and –55°C to 125°C for the LT1004M.

§ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	LT1004Y-1.2			LT1004Y-2.5			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 100 µA	1.231	1.235	1.239	2.48	2.5	2.52	V
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 10 µA		20					ppm/°C
		I_Z = 20 µA					20		
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA		20			20		ppm/khr
$I_Z$min	Minimum reference current			8			12		µA
z_Z	Reference impedance	I_Z = 100 µA		0.2	0.6		0.2	0.6	Ω
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz		60			120		µV

§ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

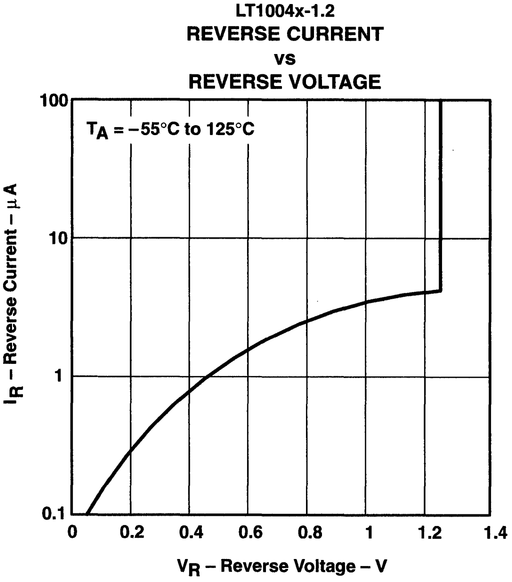


Figure 1

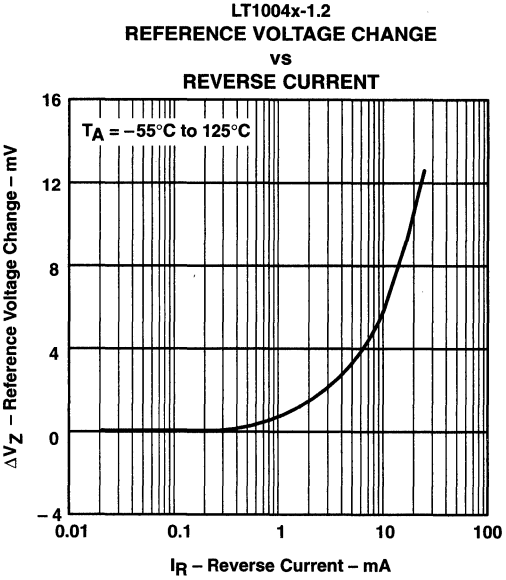


Figure 2

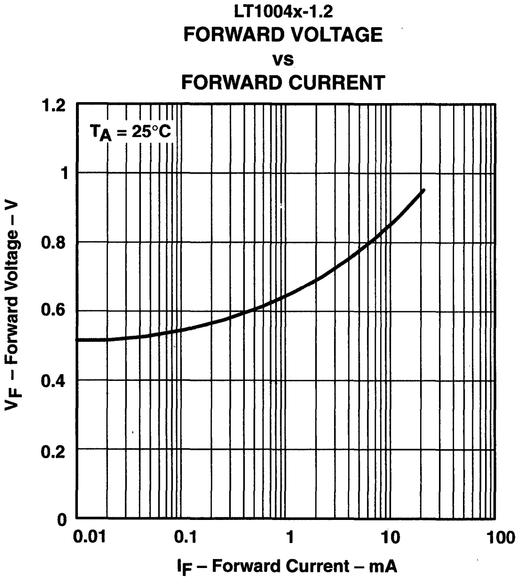


Figure 3

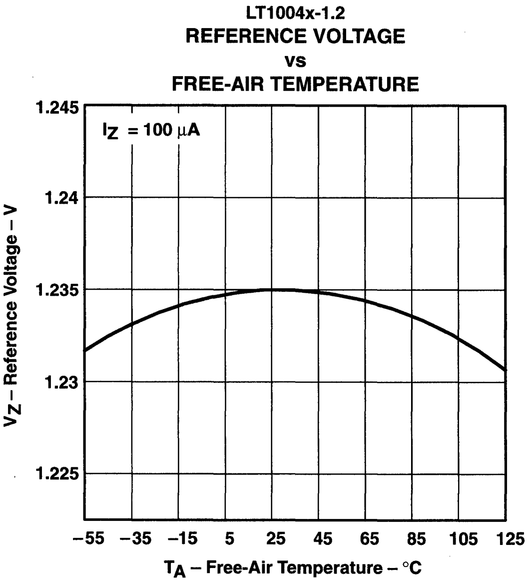


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LT1004x-1.2
REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

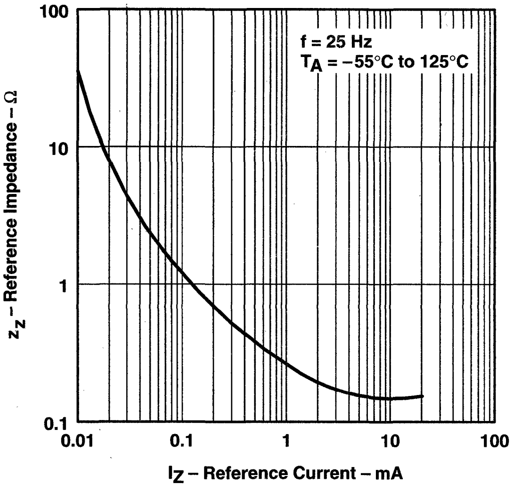

Figure 5

LT1004x-1.2
NOISE VOLTAGE
vs
FREQUENCY

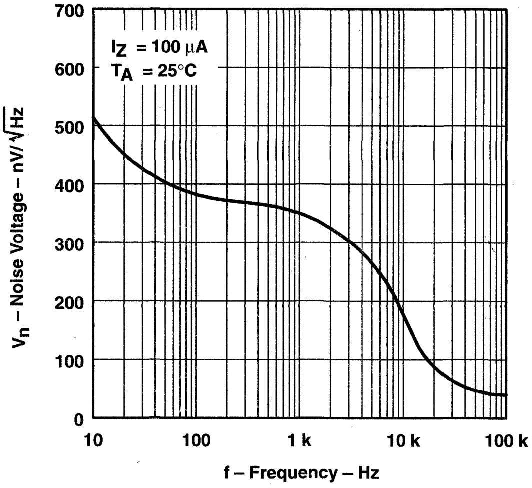

Figure 6

TL1004x-1.2
FILTERED OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

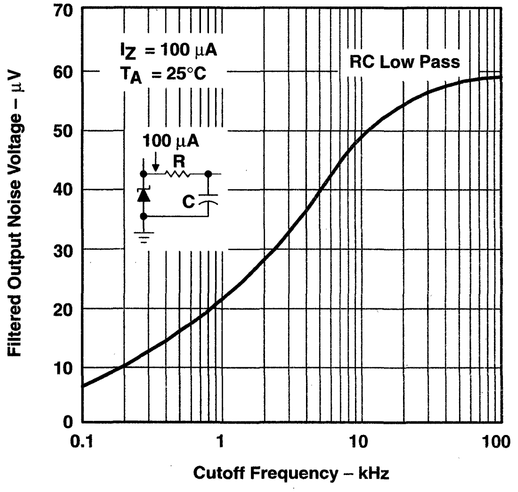

Figure 7

LT1004x-2.5
TRANSIENT RESPONSE

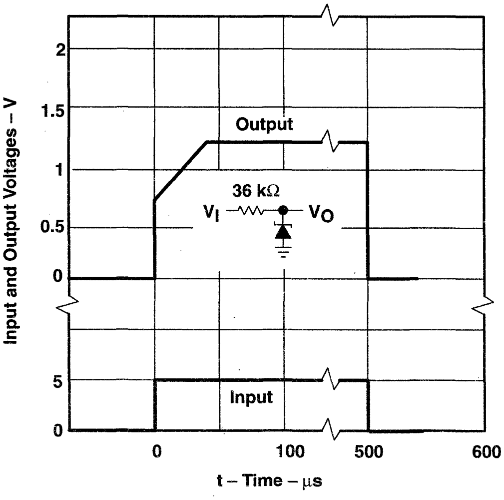

Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LT1004x-2.5
REVERSE CURRENT
vs
REVERSE VOLTAGE

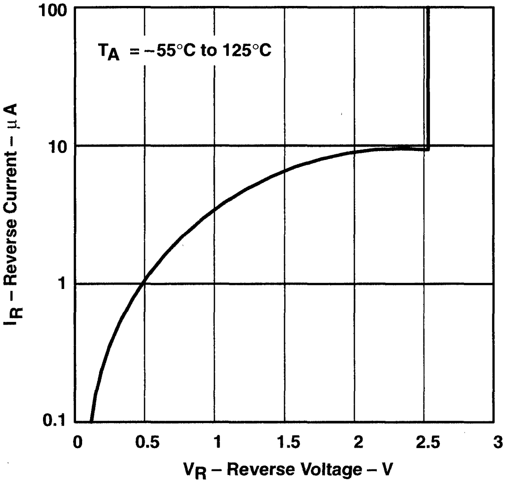

Figure 9

LT1004x-2.5
FORWARD VOLTAGE
vs
FORWARD CURRENT

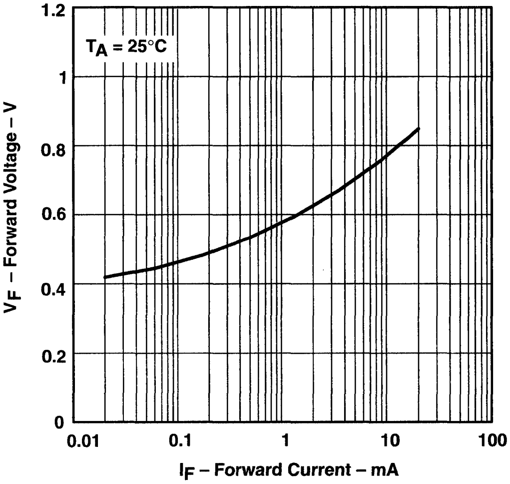

Figure 10

LT1004x-2.5
REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

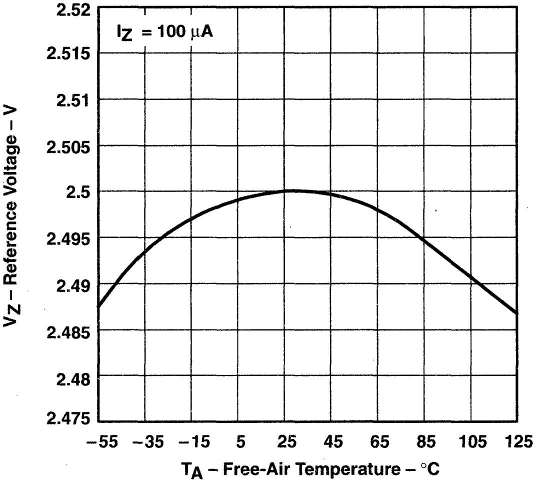

Figure 11

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LT1004x-2.5
REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

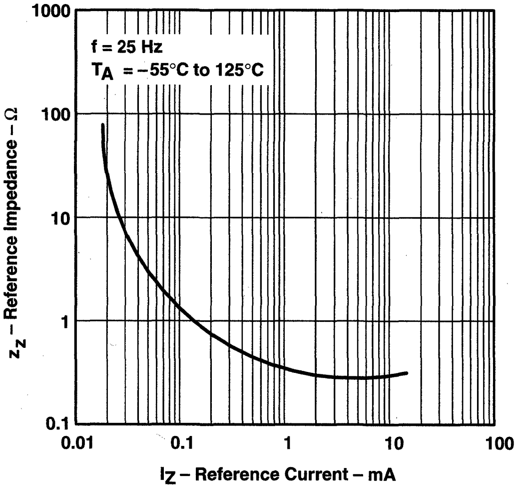

Figure 12

LT1004x-2.5
NOISE VOLTAGE
vs
FREQUENCY

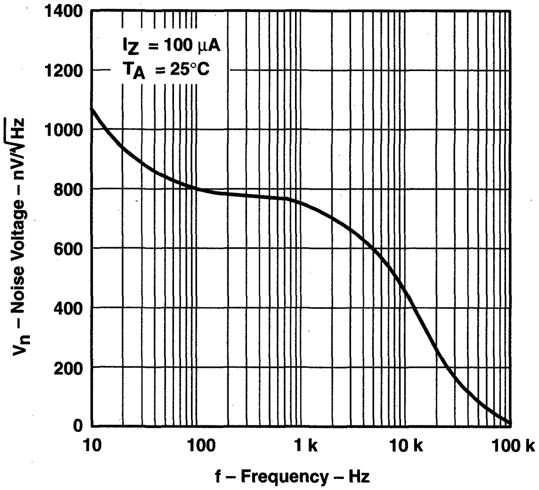

Figure 13

TL1004x-2.5
FILTERED OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

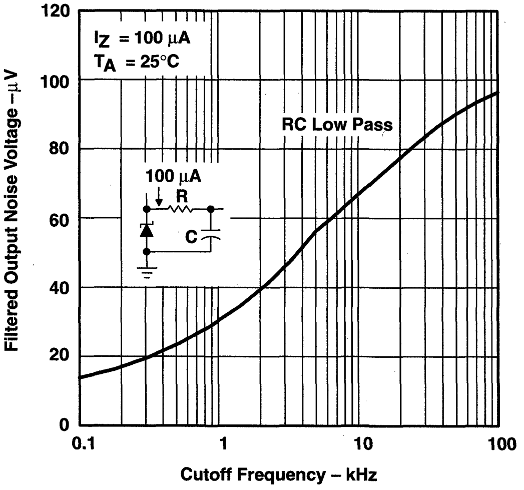

Figure 14

LT1004x-2.5
TRANSIENT RESPONSE

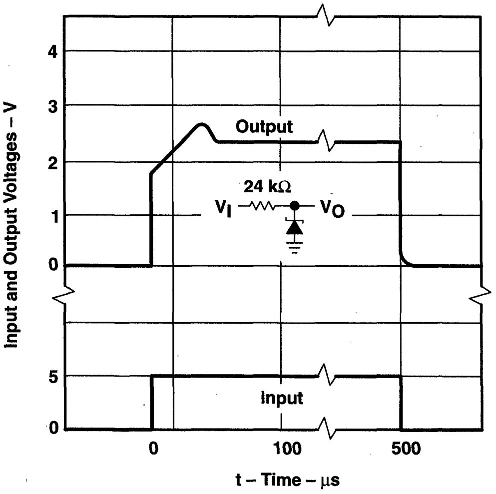

Figure 15

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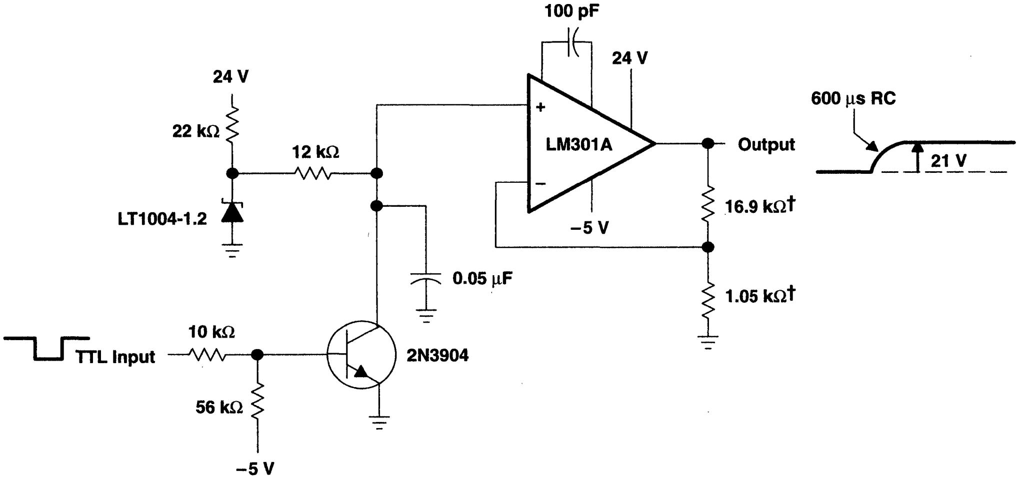
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



† 1% metal-film resistors

Figure 16. $V_{I(PP)}$ Generator for EPROMs (No Trim Required)

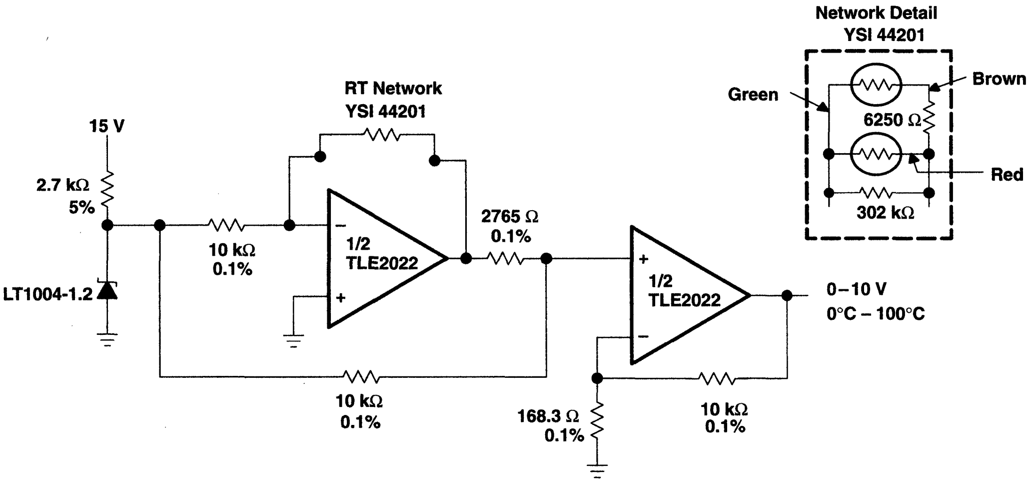


Figure 17. 0°C to 100°C Linear Output Thermometer

APPLICATION INFORMATION

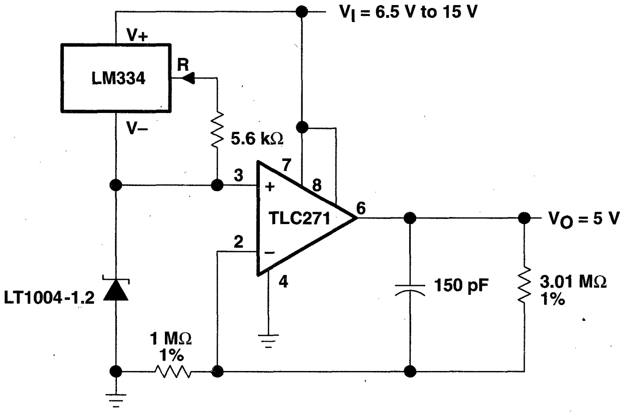


Figure 18. Micropower 5-V Reference

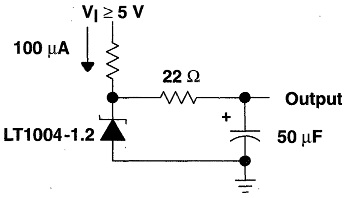


Figure 19. Low-Noise Reference

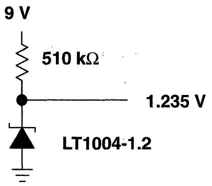
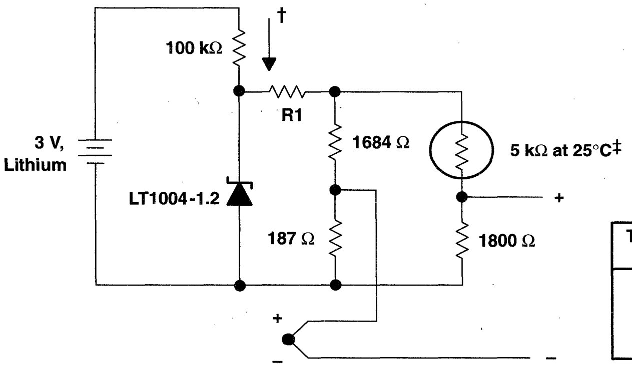


Figure 20. Micropower Reference From 9-V Battery



Thermocouple Type	R1
J	232 kΩ
K	298 kΩ
T	301 kΩ
S	2.1 MΩ

† Quiescent current ≅ 15 μA
‡ Yellow Springs Inst. Co., Part #44007
NOTE A: This application compensates within ±1°C from 0°C to 60°C.

Figure 21. Micropower Cold-Junction Compensation for Thermocouples

APPLICATION INFORMATION

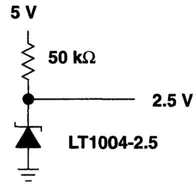


Figure 22. 2.5-V Reference

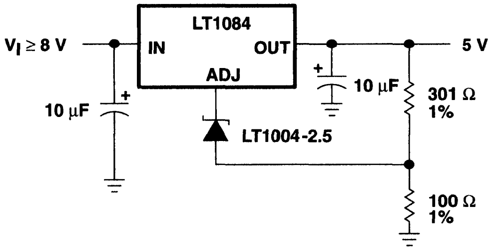
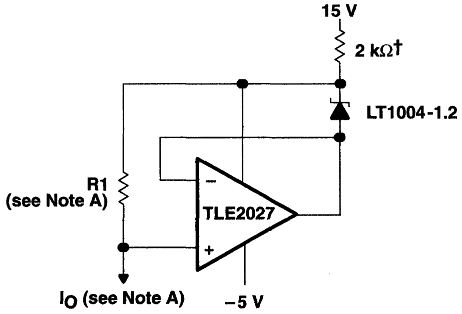


Figure 23. High-Stability 5-V Regulator



† May be increased for small output currents

NOTE A: $R1 \approx \frac{2\ \text{V}}{I_O + 10\ \mu\text{A}}$, $I_O = \frac{1.235\ \text{V}}{R1}$

Figure 24. Ground-Referenced Current Source

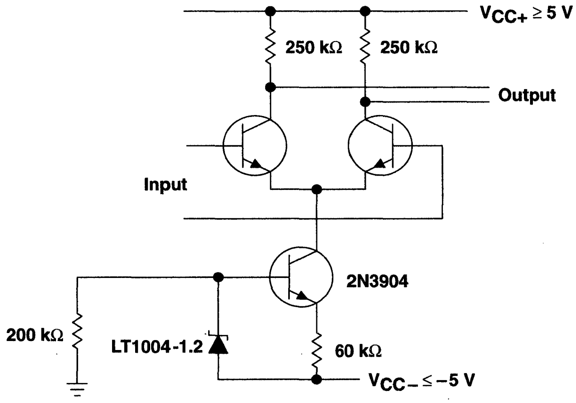
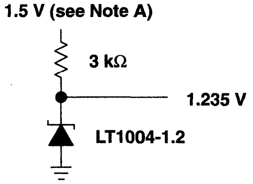


Figure 25. Amplifier With Constant Gain Over Temperature



NOTE A: Output regulates down to 1.285 V for $I_O = 0$.

Figure 26. 1.2-V Reference From 1.5-V Battery

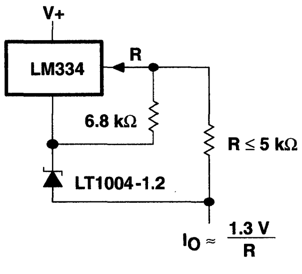
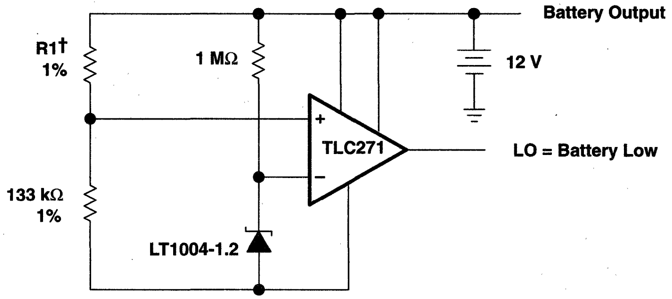


Figure 27. Terminal Current Source With Low Temperature Coefficient

APPLICATION INFORMATION



†R1 sets trip point, 60.4 kΩ per cell for 1.8 V per cell

Figure 28. Lead-Acid Low-Battery Voltage Detector

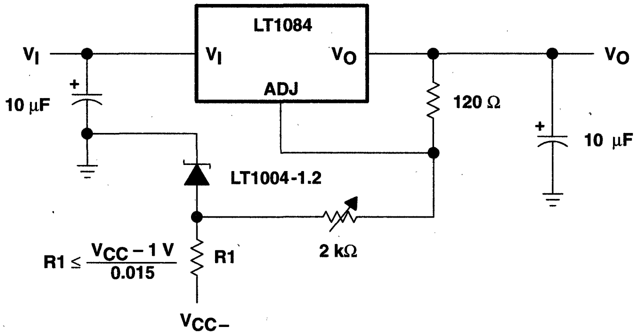


Figure 29. Variable Voltage Supply

LT1009, LT1009Y
2.5-V INTEGRATED REFERENCE CIRCUITS

SLVS013E – MAY 1987 – REVISED AUGUST 1995

- **Excellent Temperature Stability**
- **Initial Tolerance . . . 0.2% Max**
- **Dynamic Impedance . . . 0.6 Ω Max**
- **Wide Operating Current Range**
- **Directly Interchangeable With LM136**
- **Needs No Adjustment for Minimum Temperature Coefficient**
- **Surface-Mount 3-Lead Package**

description

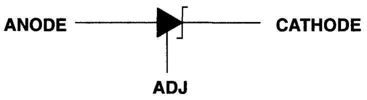
The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. A maximum initial tolerance of ±5 mV is available in the FK, JG, or LP package and ±10 mV in the D or PK package. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient α_{VZ}.

Even though the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted ±5% to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

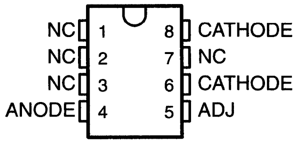
The uses of the LT1009 include a 5-V system reference, an 8-bit ADC and DAC reference, and a power supply monitor. The LT1009 can also be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from −40°C to 85°C. The LT1009M is characterized for operation over the full military temperature range of −55°C to 125°C.

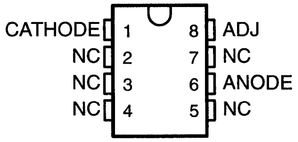
logic symbol



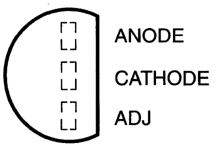
D PACKAGE
(TOP VIEW)



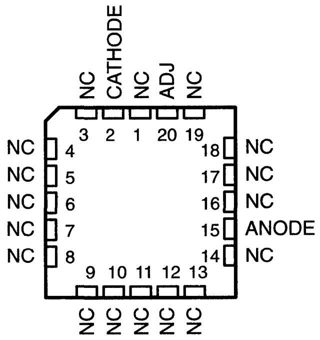
JG PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)

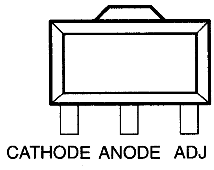


FK PACKAGE
(TOP VIEW)

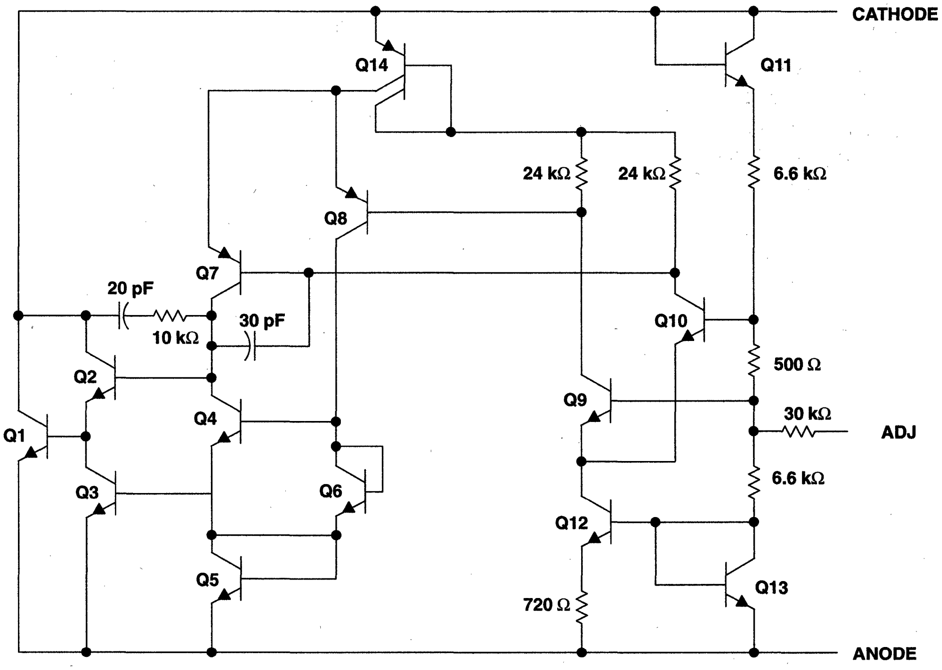


NC – No internal connection

PK PACKAGE
(TOP VIEW)



schematic



All component values shown are nominal.

AVAILABLE OPTIONS

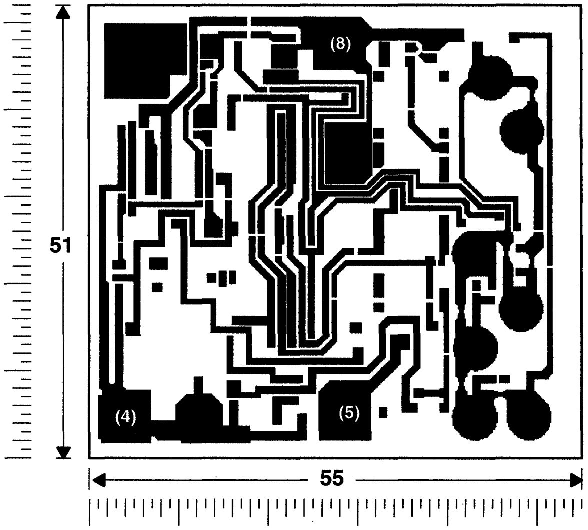
T_A	PACKAGED DEVICES					CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC CYLINDRICAL (LP)	PLASTIC LEAD-MOUNT (PK)	
0°C to 70°C	LT1009CD	—	—	LT1009CLP	LT1009CPK	LT1009Y
−40°C to 85°C	LT1009ID	—	—	LT1009ILP	—	
−55°C to 125°C	—	LT1009MFK	LT1009MJG	—	—	

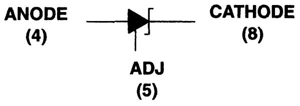
The D and LP packages are available taped and reeled. Add R suffix to device type (e.g., LT1009CDR). PK device is only available taped and reeled. No R suffix is required.

LT1009Y chip information

This chip, when properly assembled, displays characteristics similar to the LT1009C (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range†

Reverse current, I_R	20 mA
Forward current, I_F	10 mA
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating free-air temperature range, T_A: LT1009C	0°C to 70°C
LT1009I	−40°C to 85°C
LT1009M	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, LP, and PK packages	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	—
PK	500 mW	4.0 mW/°C	320 mW	—	—

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING
PK	3125 mW	25 mW/°C	2000 mW

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	LT1009C			LT1009I			LT1009M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	$I_Z = 1$ mA	FK, JG, LP package	25°C	2.495	2.5	2.505	2.495	2.5	2.505	2.495	2.5	2.505	V
			D, PK package		2.49	2.5	2.51	2.49	2.5	2.51				
			FK, JG, LP package	Full range	2.491		2.509	2.48		2.52	2.46		2.535	
			D, PK package		2.485		2.515	2.475		2.525				
V_F	Forward voltage	$I_F = 2$ mA		25°C	0.4		1	0.4		1	0.4		1	V
	Adjustment range	$I_Z = 1$ mA, V_{ADJ} = GND to V_Z		25°C	125			125						mV
		$I_Z = 1$ mA, $V_{ADJ} = 0.6$ V to $V_Z - 0.6$ V			45			45			15			
$\Delta V_{Z(temp)}$	Change in reference voltage with temperature		FK, JG, LP package	Full range			4			15			15*	mV
			D, PK package				5			15				
α_{VZ}	Average temperature coefficient of reference voltage‡			0°C to 70°C		15	25							ppm/°C
				−40°C to 85°C					20					
				−55°C to 125°C								25	35	
ΔV_Z	Change in reference voltage with current	$I_Z = 400$ µA to 10 mA		25°C		2.6	10		2.6	6		2.6	6	mV
				Full range			12			10			10	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	$I_Z = 1$ mA		25°C		20			20			20		ppm/khr
z_Z	Reference impedance	$I_Z = 1$ mA		25°C		0.3	1		0.3	1		0.3	0.6*	Ω
				Full range			1.4			1.4			1*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full range is 0°C to 70°C for the LT1009C, −40°C to 85°C for the LT1009I, and −55°C to 125°C for the LT1009M.

‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

electrical characteristics at T_A = 25°C

PARAMETER		TEST CONDITIONS	LT1009Y			UNIT
			MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	2.49	2.5	2.51	V
V_F	Forward voltage	I_F = 2 mA	0.4		1	V
	Adjustment range	I_Z = 1 mA, V_{ADJ} = GND to V_Z	125			mV
		I_Z = 1 mA, V_{ADJ} = 0.6 V to V_Z –0.6 V	45			
$\Delta V_{Z(temp)}$	Change in reference voltage with temperature			2.5		mV
α_{VZ}	Average temperature coefficient of reference voltage†			15		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 400 µA to 10 mA		2.6		mV
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 1 mA		20		ppm/khr
z_Z	Reference impedance	I_Z = 1 mA		0.3	1	Ω

† The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

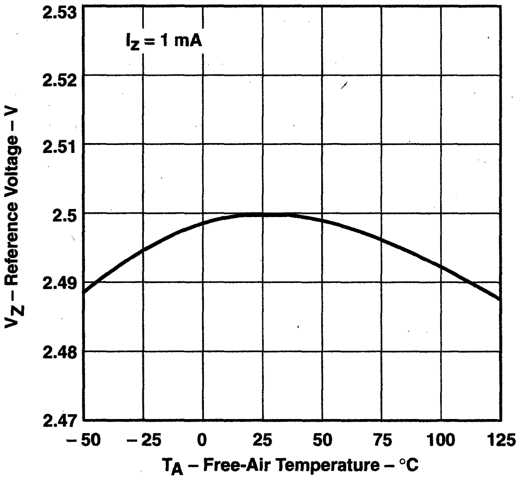

Figure 1

CHANGE IN REFERENCE VOLTAGE
vs
REFERENCE CURRENT

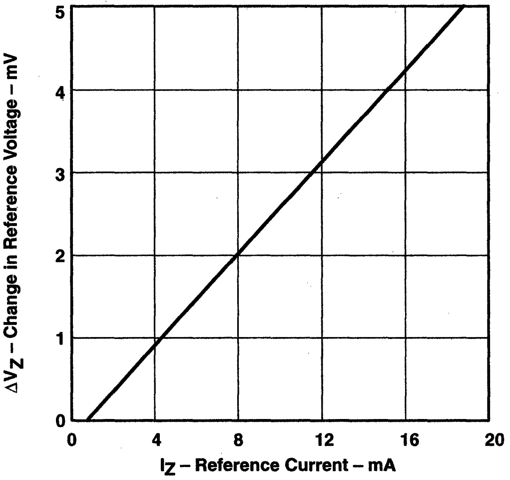

Figure 2

REVERSE CURRENT
vs
REVERSE VOLTAGE

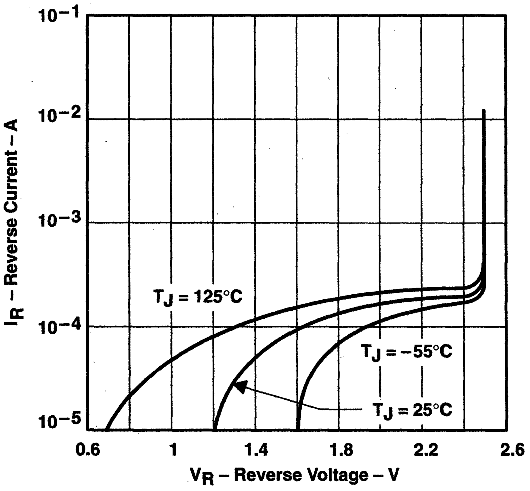

Figure 3

FORWARD VOLTAGE
vs
FORWARD CURRENT

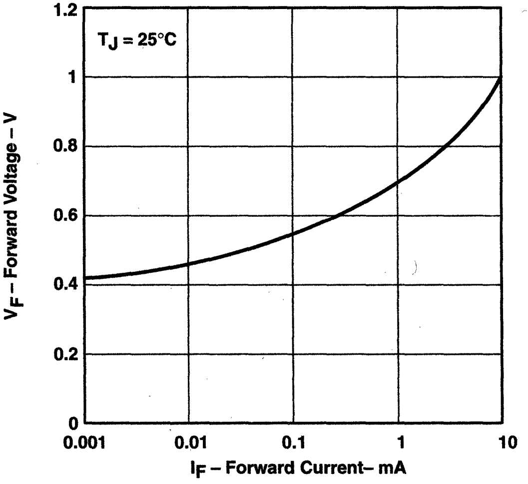

Figure 4

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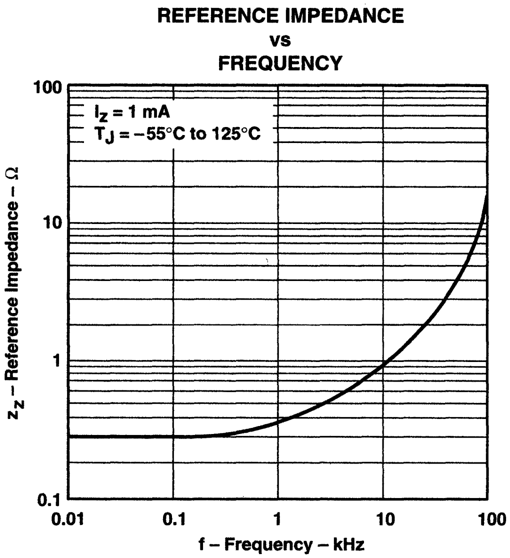
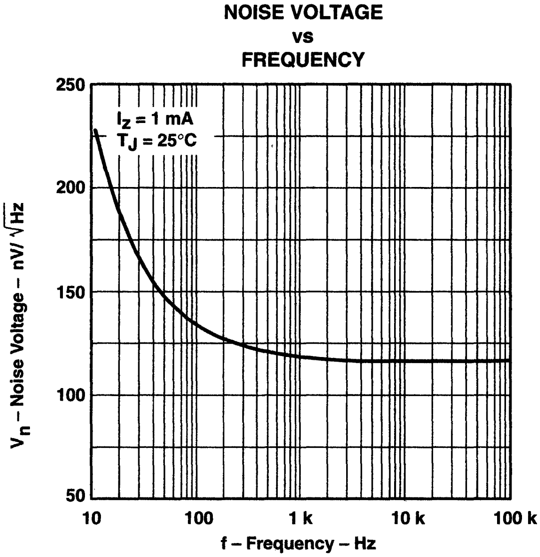
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



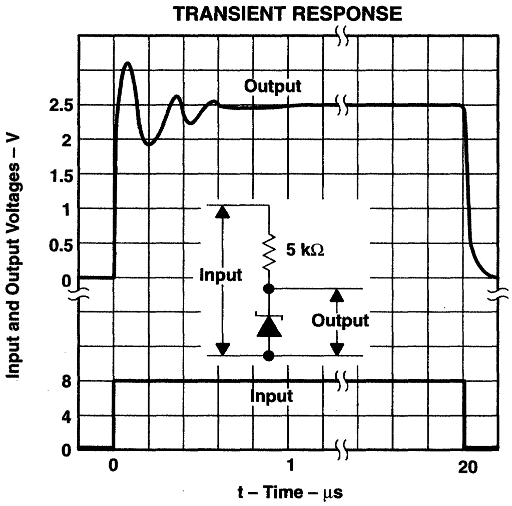
REFERENCE IMPEDANCE
vs
FREQUENCY

Figure 5



NOISE VOLTAGE
vs
FREQUENCY

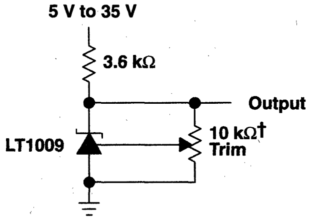
Figure 6



TRANSIENT RESPONSE

Figure 7

APPLICATION INFORMATION



†This does not affect temperature coefficient. It provides ±5% trim range.

Figure 8. 2.5-V Reference

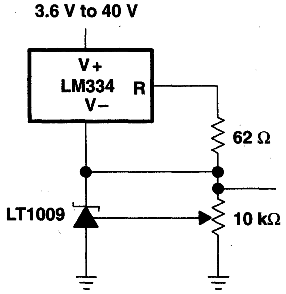


Figure 9. Adjustable Reference With Wide Supply Range

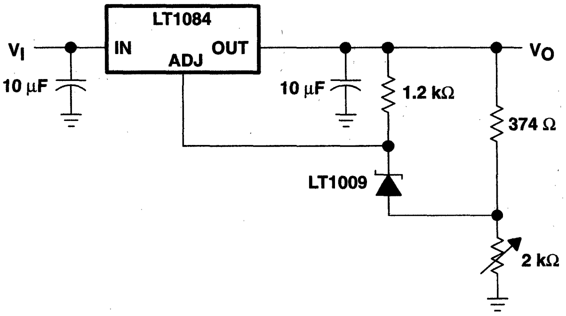


Figure 10. Power Regulator With Low Temperature Coefficient

APPLICATION INFORMATION

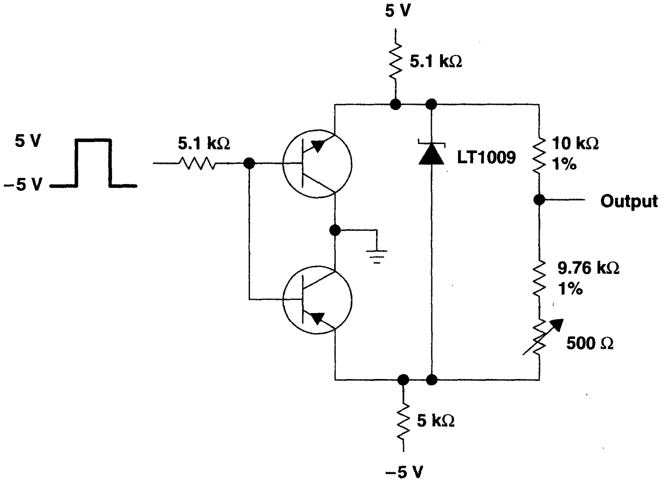


Figure 11. Switchable ±1.25-V Bipolar Reference

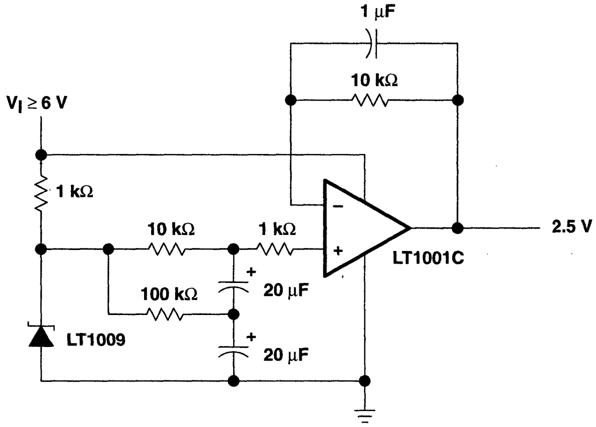


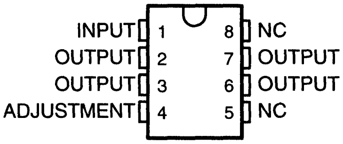
Figure 12. Low-Noise 2.5-V Buffered Reference

Contents

TL317, TL317Y
3-TERMINAL ADJUSTABLE REGULATORS

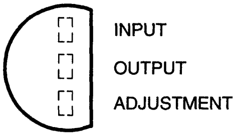
- **Output Voltage Range Adjustable From 1.2 V to 32 V When Used With an External Resistor Divider**
- **Output Current Capability of 100 mA**
- **Input Regulation Typically 0.01% Per Input-Voltage Change**
- **Output Regulation Typically 0.5%**
- **Ripple Rejection Typically 80 dB**

D PACKAGE
(TOP VIEW)



NOTE: OUTPUT terminals are all internally connected.

LP PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL317C is an adjustable 3-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

In addition to replacing fixed regulators, the TL317C regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.2 V where most loads draw little current.

The TL317C is characterized for operation from 0°C to 125°C. The TL317Q is characterized for operation from –40°C to 125°C.

AVAILABLE OPTIONS

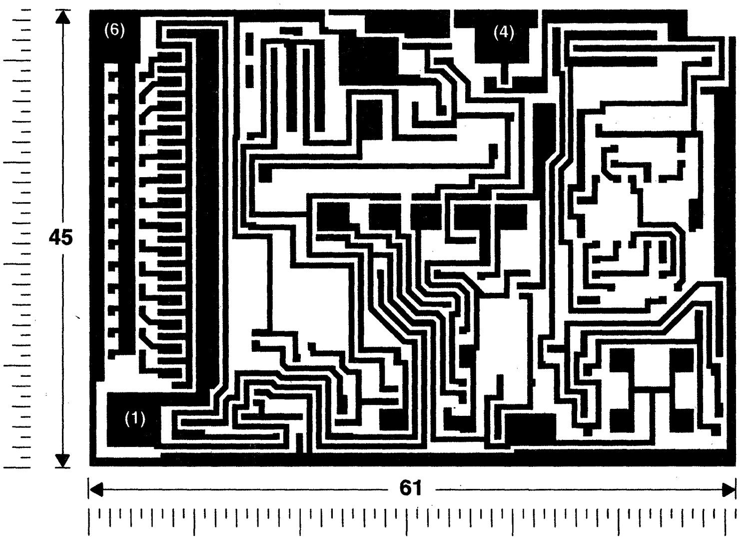
T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 125°C	TL317CD	TL317CLP	TL317Y
–40°C to 125°C	TL317QD	TL317QLP	—

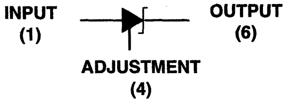
The D and LP packages are available taped and reeled. Add R suffix to device type (e.g., TL317DR).

TL317Y chip information

This chip, when properly assembled, displays characteristics similar to the TL317C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

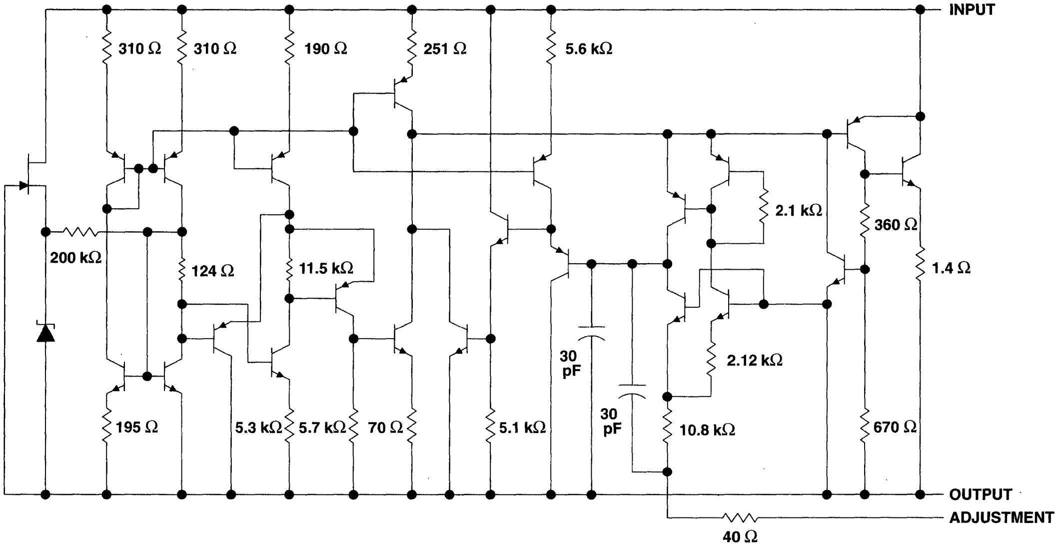
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 2,3,6, AND 7 ARE CONNECTED TOGETHER

schematic



NOTE A. All component values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$ .... 35 V
Continuous total power dissipation .... See Dissipation Rating Tables 1 and 2
Operating free-air, case, T_A, or virtual-junction temperature range, T_J: C Version .... 0°C to 150°C
Q Version .... −40°C to 150°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	145 mW
LP†	775 mW	6.2 mW/°C	155 mW

† The LP package dissipation rating is based on thermal resistance measured in still air with the device mounted in an Augat socket. The bottom of the package is 10 mm (0.375 in.) above the socket.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.6 mW/°C	96°C	742 mW
LP	1600 mW	28.6 mW/°C	94°C	713 mW

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		35	V
Output current, I_O	2.5	100	mA
Operating virtual-junction temperature, T_J	0	125	°C

electrical characteristics over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317C, TL317Q			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 1)	$V_I - V_O$ = 5 V to 35 V	T_J = 25°C		0.01	0.02	%V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-µF capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA, T_J = 25°C	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
	V_I = 5 V to 35 V, I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		50		mV
		$V_O \ge 5$ V		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C			10		mV/V
Output voltage long-term drift (see Note 2)	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			3	10	mV/V
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		30		µV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	µA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	µA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output.

NOTES: 1. Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input

2. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

electrical characteristics over recommended operating conditions, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317Y			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 1)	$V_I - V_O$ = 5 V to 35 V			0.01		%V
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-µF capacitor between ADJUSTMENT and ground			80		
Output voltage regulation	I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		5		mV/V
Output noise voltage	f = 10 Hz to 10 kHz,			30		µV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5		mA
Peak output current	$V_I - V_O \le 35$ V			200		mA
ADJUSTMENT current				50		µA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2		µA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,		1.25		V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output.

NOTE 1: Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input

APPLICATION INFORMATION

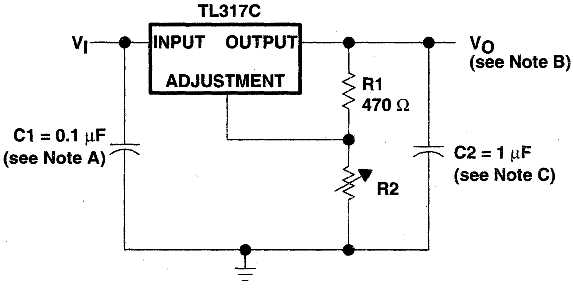


Figure 1. Adjustable Voltage Regulator

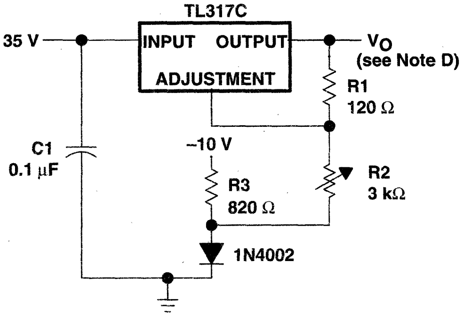
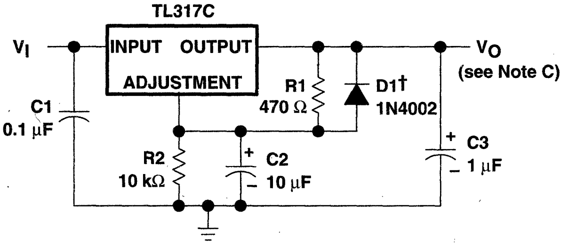


Figure 2. 0-V to 30-V Regulator Circuit



† D1 discharges C2 if output is shorted to ground.

Figure 3. Regulator Circuit With Improved Ripple Rejection

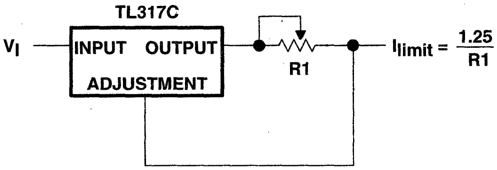


Figure 4. Precision Current-Limiter Circuit

NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors

B. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈ 1.25 V).

C. Use of an output capacitor improves transient response but is optional.

D. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2 + R3}{R1}\right) - 10\ V$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈ 1.25 V).

APPLICATION INFORMATION

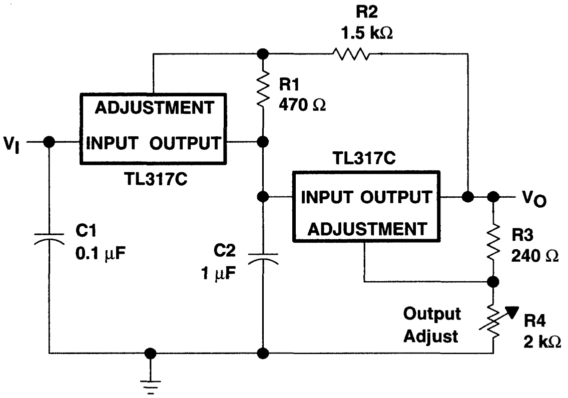


Figure 5. Tracking Preregulator Circuit

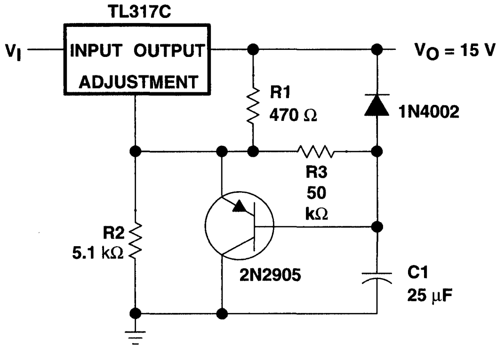


Figure 6. Slow-Turn-On 15-V Regulator Circuit

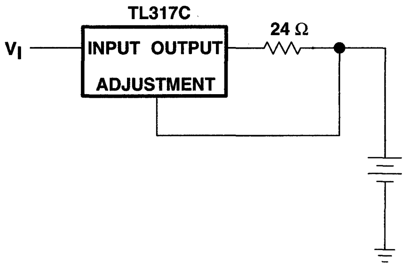


Figure 7. 50-mA Constant-Current Battery Charger Circuit

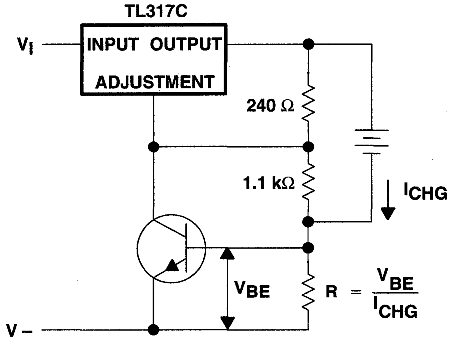
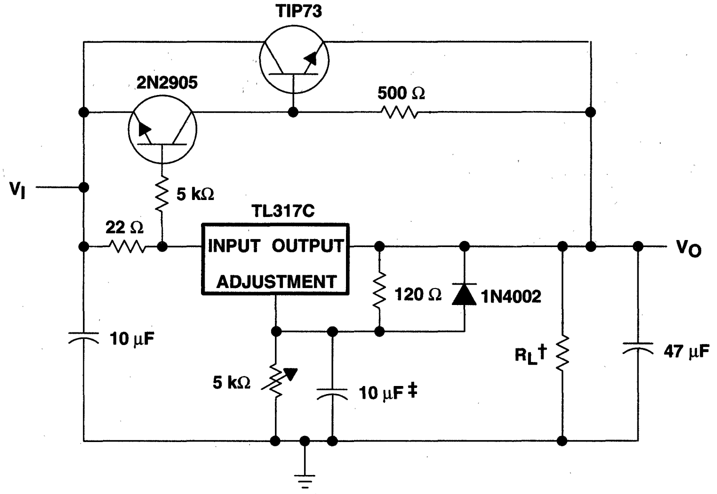


Figure 8. Current-Limited 6-V Charger

APPLICATION INFORMATION



† Minimum load current is 30 mA.
‡ Optional capacitor improves ripple rejection

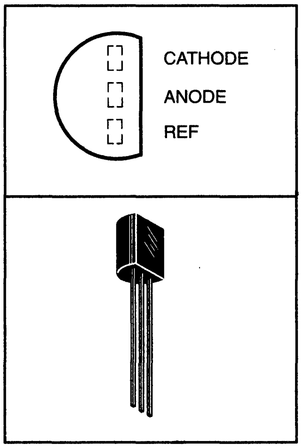
Figure 9. High-Current Adjustable Regulator

TL430C, TL430I, TL430Y
ADJUSTABLE SHUNT REGULATORS

SLVS050A – JUNE 1976 – REVISED AUGUST 1995

- **Temperature Compensated**
- **Programmable Output Voltage**
- **Low Output Resistance**
- **Low Output Noise**
- **Sink Capability to 100 mA**

LP PACKAGE
(TOP VIEW)

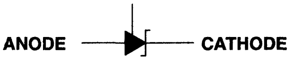


description

The TL430 is a 3-terminal adjustable shunt regulator featuring excellent temperature stability, wide operating current range, and low output noise. The output voltage may be set by two external resistors to any desired value between 3 V and 30 V. The TL430 can replace zener diodes in many applications providing improved performance

The TL430C is characterized for operation from 0°C to 70°C. The TL430I is characterized for operation from −40°C to 85°C.

symbol

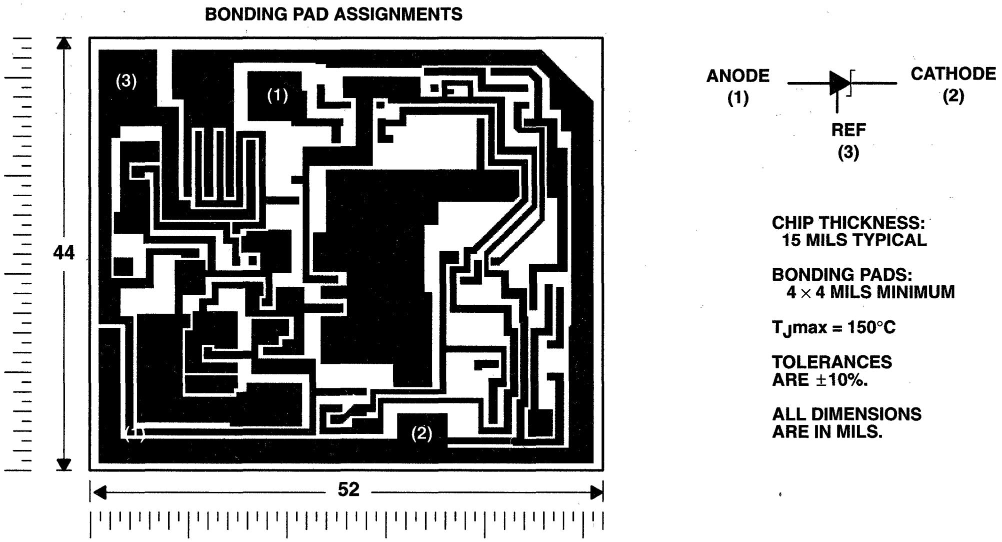


AVAILABLE OPTIONS

T_A	PACKAGED DEVICES†	CHIP FORM (Y)
	PLASTIC (LP)	
0°C to 70°C	TL430CLP	TL430Y
−40°C to 85°C	TL430ILP	—

TL430Y chip information

This chip, when properly assembled, displays characteristics similar to the TL430C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.


BONDING PAD ASSIGNMENTS

CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Regulator voltage (see Note 1)	30 V
Continuous regulator current	150 mA
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2)	775 mW
Operating free-air temperature range, T_A: TL430C	0°C to 70°C
TL430I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the anode terminal.
2. For operation above 25°C free-air temperature, derate at 6.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Regulator voltage, V_Z		V_{ref}	30	V
Regulator current, I_Z		2	100	mA
Operating free-air temperature range, T_A	TL430C	0	70	°C
	TL430I	−40	85	

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		TL430C			TL430I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	1	$V_Z = V_{I(ref)}$,	I_Z = 10 mA	2.5	2.75	3	2.6	2.75	2.9	V
$\alpha V_{I(ref)}$	Temperature coefficient of reference input voltage	1	$V_Z = V_{I(ref)}$, T_A = full range†	I_Z = 10 mA,		120			120	200	ppm/°C
$I_{I(ref)}$	Reference input current	2	I_Z = 10 mA, R2 = ∞	R1 = 10 kΩ,		3	10		3	10	μA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{I(ref)}$			0.5	2		0.5	2	mA
I_{ZK}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{I(ref)}$		50			50			mA
		2	V_Z = 5 V to 30 V,	See Note 3	100			100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{I(ref)}$, ΔI_Z = (52 – 2) mA			1.5	3		1.5	3	Ω
V_n	Noise voltage	2	f = 0.1 Hz to 10 Hz	V_Z = 3 V		50			50		μV
				V_Z = 12 V		200			200		
				V_Z = 30 V		650			650		

† Full temperature range is 0°C to 70°C for the TL430C and –40°C to 85°C for the TL430I.

NOTES: 3. The average power dissipation, $V_Z \bullet I_Z \bullet$ duty cycle, must not exceed the maximum continuous rating in any 10-ms interval.

4. The regulator resistance for $V_Z > V_{I(ref)}$, r_z, is given by:

$$r_z' = r_z\left(1 + \frac{R1}{R2}\right)$$

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		TL430Y			UNIT
					MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	1	$V_Z = V_{I(ref)}$,	I_Z = 10 mA	2.5	2.75	3	V
$I_{I(ref)}$	Reference input current	2	I_Z = 10 mA, R2 = ∞	R1 = 10 kΩ,		3	10	μA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{I(ref)}$			0.5	2	mA
I_{ZK}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{I(ref)}$		50			mA
		2	V_Z = 5 V to 30 V,	See Note 3	100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{I(ref)}$, ……. ΔI_Z = (52 – 2) mA			1.5	3	Ω
V_n	Noise voltage	2	f = 0.1 Hz to 10 Hz	V_Z = 3 V		50		μV
				V_Z = 12 V		200		
				V_Z = 30 V		650		

NOTES: 3. The average power dissipation, $V_Z \bullet I_Z \bullet$ duty cycle, must not exceed the maximum continuous rating in any 10-ms interval.

4. The regulator resistance for $V_Z > V_{I(ref)}$, r_z, is given by:

$$r_z' = r_z\left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

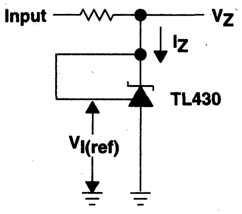
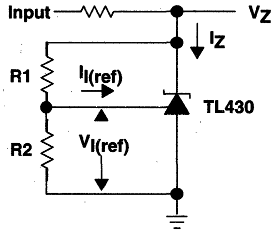


Figure 1. Test Circuit for $V_Z = V_{I(ref)}$



$$V_Z = V_{I(ref)}\left(1 + \frac{R1}{R2}\right) + I_{I(ref)} \times R1$$

Figure 2. Test Circuit for $V_Z > V_{I(ref)}$

TYPICAL CHARACTERISTICS

SMALL-SIGNAL REGULATOR IMPEDANCE
vs
FREQUENCY

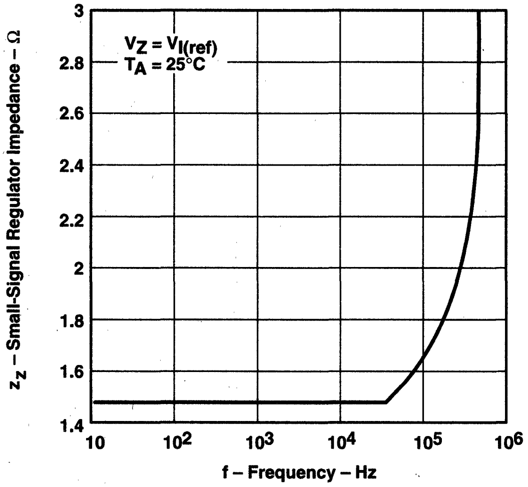


Figure 3

CATHODE CURRENT
vs
CATHODE VOLTAGE

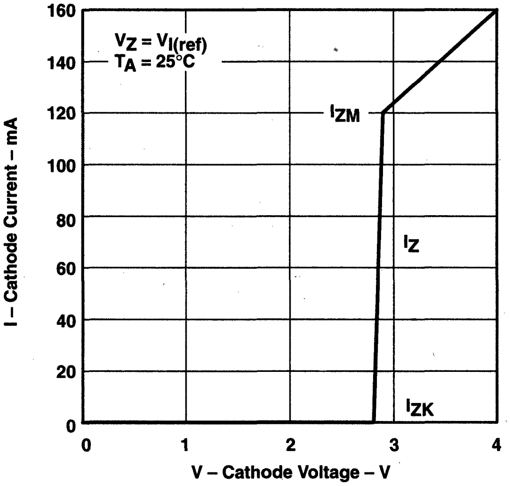
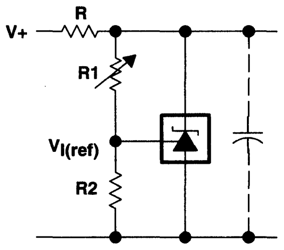


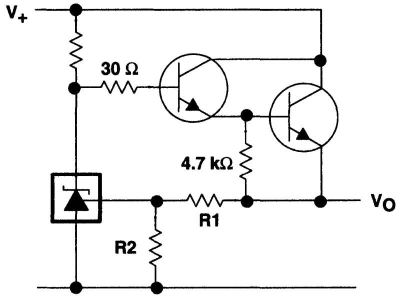
Figure 4

APPLICATION INFORMATION



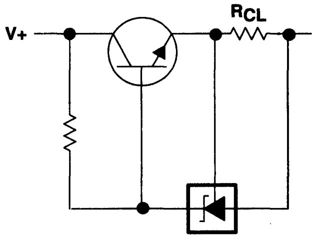
$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

Figure 5. Shunt Regulator



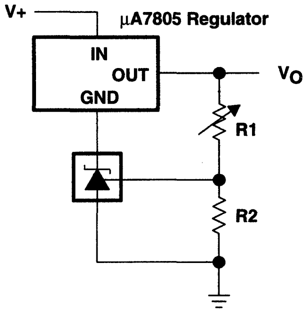
$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

Figure 6. Series Regulator



$$I_O \approx \frac{V_{I(ref)}}{R_{CL}}$$

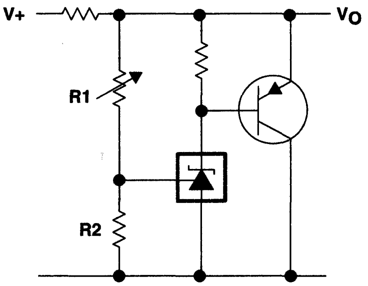
Figure 7. Current Limiter



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

$$\text{Min } V_O = V_{I(ref)} + 5\text{V}$$

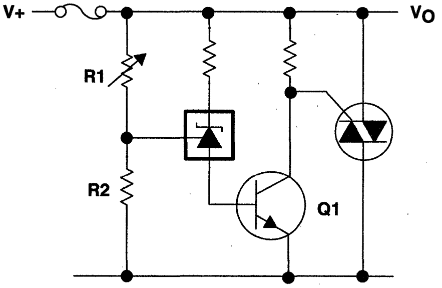
Figure 8. Output Control of a 3-Terminal Fixed Regulator



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

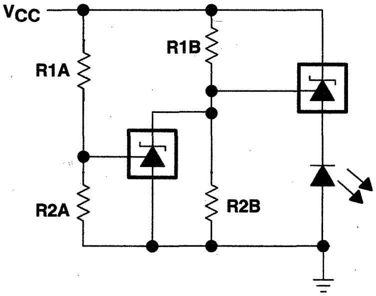
Figure 9. Higher-Current Applications

APPLICATION INFORMATION



$$V_{limit} \approx \left(1 + \frac{R1}{R2}\right)\left(V_{I(ref)} + V_{BE(Q1)}\right)$$

Figure 10. Crowbar



$$\text{Low limit} \approx V_{I(ref)}\left(1 + \frac{R1B}{R2B}\right) + V_D$$

$$\text{High limit} \approx V_{I(ref)}\left(1 + \frac{R1A}{R2A}\right)$$

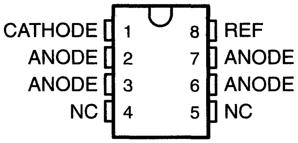
Figure 11. V_{CC} Monitor

TL431C, TL431AC, TL431I, TL431AI, TL431M, TL431Y
ADJUSTABLE PRECISION SHUNT REGULATORS

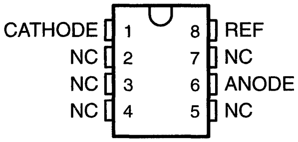
SLVS005E – JULY 1978 – REVISED AUGUST 1995

- **Equivalent Full-Range Temperature Coefficient . . . 30 ppm/°C**
- **0.2-Ω Typical Output Impedance**
- **Sink-Current Capability . . . 1 mA to 100 mA**
- **Low Output Noise**
- **Adjustable Output Voltage . . . $V_{I(ref)}$ to 36 V**
- **Available in a Wide Range of High-Density Packaging Options:**
  - **Small Outline (D)**
  - **TO-226AA (LP)**
  - **SOT-89 (PK)**

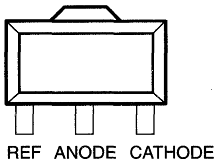
D OR PW PACKAGE
(TOP VIEW)



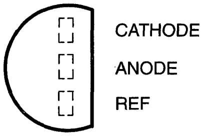
JG OR P PACKAGE
(TOP VIEW)



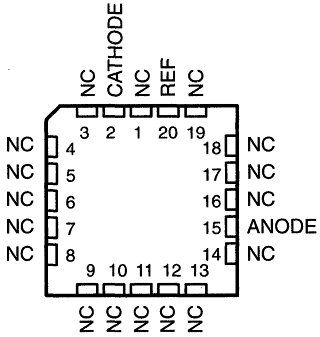
PK PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL431 and TL431A are 3-terminal adjustable shunt regulators with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between $V_{I(ref)}$ (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes in many applications, such as on-board regulation, adjustable power supplies, and switching power supplies.

The TL431 is offered in a wide variety of high-density packaging options that includes an SOT-89-type package (suffix PK).

The TL431C and TL431AC are characterized for operation from 0°C to 70°C, and the TL431I and TL431AI are characterized for operation from −40°C to 85°C. The TL431M is characterized for operation over the full military temperature range of −55°C to 125°C.

On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TL431C, TL431AC, TL431I, TL431AI, TL431M, TL431Y
ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS005E – JULY 1978 – REVISED AUGUST 1995

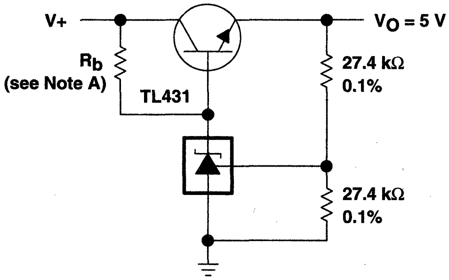
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES							CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TO-226AA (LP)	PLASTIC DIP (P)	SOT-89 (PK)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL431CD TL431ACD			TL431CLP TL431ACLP	TL431CP TL431ACP	TL431CPK	TL431CPW	TL431Y
−40°C to 85°C	TL431ID TL431AID			TL431ILP TL431AILP	TL431IP TL431AIP	TL431IPK		
−55°C to 125°C		TL431MFK	TL431MJG					

The D and LP packages are available taped and reeled. Add R suffix to device type (e.g., TL431CDR). The PK package is only available taped and reeled (no R suffix required). Chip forms are tested at $T_A = 25°C$.

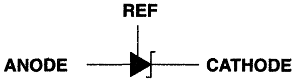
application schematic

5-V Precision Regulator

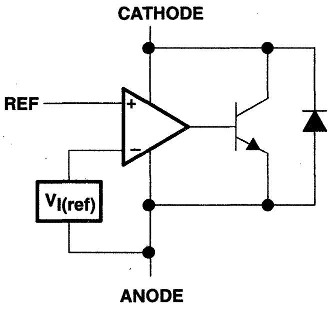


NOTE A: R_b should provide cathode current ≥ 1-mA to the TL431.

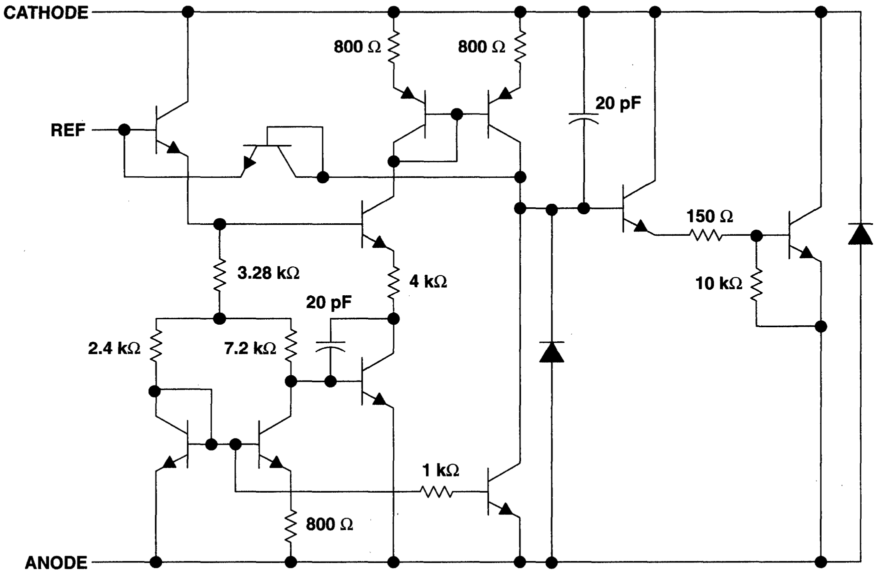
symbol



functional block diagram



equivalent schematic

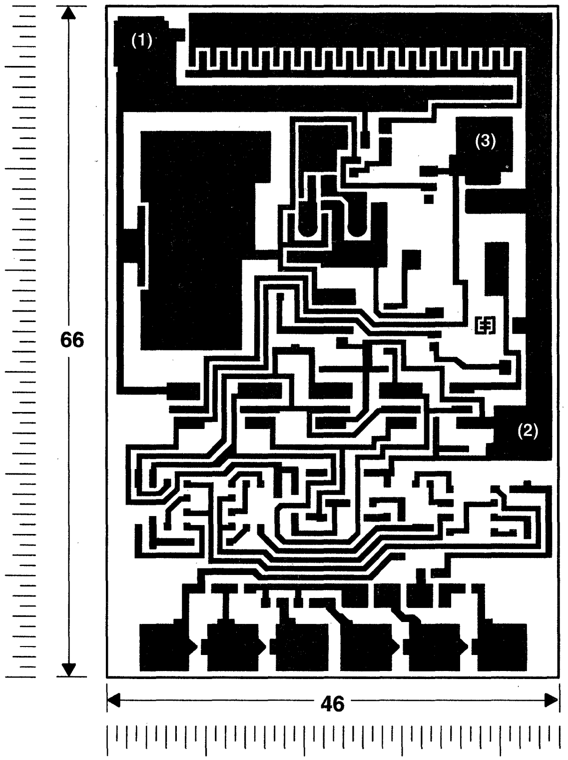


NOTE A: All component values are nominal.

TL431Y chip information

This chip, when properly assembled, displays characteristics similar to the TL431C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Pins 2,3,6, and 7 are connected together

Pins 4 and 5 are not connected

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cathode voltage, V_{KA} (see Note 1) . . . . 37 V
Continuous cathode current range, I_{KA} . . . . –100 mA to 150 mA
Reference input current range . . . . –50 μA to 10 mA
Continuous total power dissipation . . . . See Dissipation Rating Tables 1 and 2
Operating free-air temperature range, T_A: C-suffix . . . . 0°C to 70°C
I-suffix . . . . –40°C to 85°C
M-suffix . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG, LP, or PK package . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the anode terminal unless otherwise noted.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PK	500 mW	4.0 mW/°C	320 mW	260 mW	—
PW	525 mW	4.2 mW/°C	336 mW	—	—

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	T_C = 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 70°C POWER RATING	T_C = 85°C POWER RATING
PK	3125 mW	25 mW/°C	2000 mW	1625 mW

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	$V_{I(ref)}$	36	V
Cathode current, I_{KA}	1	100	mA

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

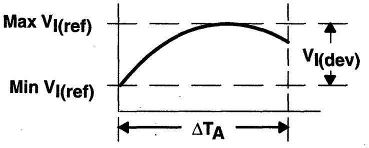
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431C			TL431I			TL431M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 10 mA		2440	2495	2550	2440	2495	2550	2400	2495	2600	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 10 mA, T_A = Full range†			4	17		5	30		22		mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_{KA} = 10 mA	ΔV_{KA} = 10 V − $V_{I(ref)}$		−1.4	−2.7		−1.4	−2.7		−1.4	−3	$\frac{mV}{V}$
				ΔV_{KA} = 36 V − 10 V		−1	−2		−1	−2		−1	−2.3	
$I_{I(ref)}$	Reference input current	2	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4		2	4		2	8*	μA
$I_{I(dev)}$	Deviation of reference input current over full temperature range‡	2	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = Full range†			0.4	1.2		0.8	2.5		1		μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{I(ref)}$			0.4	1		0.4	1		0.4	1.5	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, $V_{I(ref)}$ = 0			0.1	1		0.1	1		0.1	3	μA
$\lvert z_{KA} \rvert$	Dynamic impedance§	1	I_{KA} = 1 mA to 100 mA, $V_{KA} = V_{I(ref)}$, f ≤ 1 kHz			0.2	0.5		0.2	0.5		0.2	0.9*	Ω

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full temperature range is 0°C to 70°C for the TL431C, −40°C to 85°C for the TL431I, and −55°C to 125°C for the TL431M.

‡ The deviation parameters $V_{refI(dev)}$ and $I_{refI(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, $\alpha_{VI(ref)}$, is defined as:

$$\lvert \alpha_{VI(ref)} \rvert \left(\frac{ppm}{°C}\right) = \frac{\left(\dfrac{V_{I(dev)}}{V_{I(ref)} \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

$\alpha_{VI(ref)}$ can be positive or negative depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

Example: Max $V_{I(ref)}$ = 2496 mV at 30°C, Min $V_{I(ref)}$ = 2492 mV at 0°C, $V_{I(ref)}$ = 2495 mV at 25°C, ΔT_A = 70°C for TL431C

$$\lvert \alpha_{VI(ref)} \rvert = \frac{\left(\dfrac{4\ mV}{2495\ mV}\right) \times 10^6}{70°C} \approx 23\ ppm/°C$$

Because minimum $V_{I(ref)}$ occurs at the lower temperature, the coefficient is positive.

§ The dynamic impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I} \approx \lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$

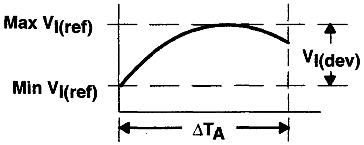
electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS	TL431AC			TL431AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 10 mA	2470	2495	2520	2470	2495	2520	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 10 mA, T_A = Full range†		4	15		5	25	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_{KA} = 10 mA, ΔV_{KA} = 10 V − $V_{I(ref)}$		−1.4	−2.7		−1.4	−2.7	$\frac{mV}{V}$
			I_{KA} = 10 mA, ΔV_{KA} = 36 V − 10 V		−1	−2		−1	−2	
$I_{I(ref)}$	Reference input current	2	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞		2	4		2	4	μA
$I_{I(dev)}$	Deviation of reference input current over full temperature range‡	2	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = Full range†		0.8	1.2		0.8	2.5	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{I(ref)}$		0.4	0.6		0.4	0.7	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, $V_{I(ref)}$ = 0		0.1	0.5		0.1	0.5	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 1 mA to 100 mA, f ≤ 1 kHz		0.2	0.5		0.2	0.5	Ω

† Full temperature range is 0°C to 70°C for the TL431AC and −40°C to 85°C for the TL431AI.

‡ The deviation parameters $V_{refI(dev)}$ and $I_{refI(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, $\alpha_{VI(ref)}$, is defined as:

$$\left|\alpha_{VI(ref)}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)} \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

$\alpha_{VI(ref)}$ can be positive or negative depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

Example: Max $V_{I(ref)}$ = 2496 mV at 30°C, Min $V_{I(ref)}$ = 2492 mV at 0°C, $V_{I(ref)}$ = 2495 mV at 25°C, ΔT_A = 70°C for TL431AC

$$\left|\alpha_{VI(ref)}\right| = \frac{\left(\frac{4\text{ mV}}{2495\text{ mV}}\right) \times 10^6}{70°C} \approx 23\text{ ppm/°C}$$

Because minimum $V_{I(ref)}$ occurs at the lower temperature, the coefficient is positive.

§ The dynamic impedance is defined as: $\left|z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $\left|z'\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{KA}\right| \left(1 + \frac{R1}{R2}\right)$

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431Y MIN	TL431Y TYP	TL431Y MAX	UNIT
$V_{I(ref)}$	Reference input voltage	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 10 mA			2495		mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_{KA} = 10 mA	ΔV_{KA} = 10 V – $V_{I(ref)}$		−1.4		$\frac{mV}{V}$
				ΔV_{KA} = 36 V – 10 V		−1		
$I_{I(ref)}$	Reference input current	2	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2		µA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{I(ref)}$			0.4		mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, $V_{I(ref)}$ = 0			0.1		µA
$\lvert z_{KA}\rvert$	Dynamic impedance†	1	$V_{KA} = V_{I(ref)}$, I_{KA} = 1 mA to 100 mA, f ≤ 1 kHz			0.2		Ω

† The dynamic impedance is defined as: $\lvert z_{ka}\rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\lvert z'\rvert = \frac{\Delta V}{\Delta I} \approx \lvert z_{KA}\rvert \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

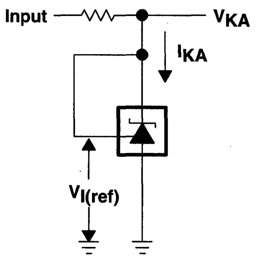
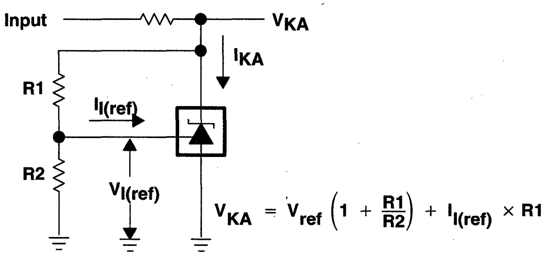


Figure 1. Test Circuit for $V_{KA} = V_{I(ref)}$



$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{I(ref)} \times R1$$

Figure 2. Test Circuit for $V_{KA} > V_{I(ref)}$

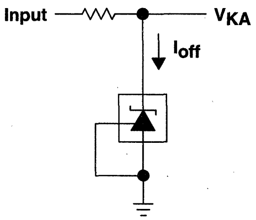


Figure 3. Test Circuit for I_{off}

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{I(ref)}$	Reference input voltage	vs Free-air temperature	4
$I_{I(ref)}$	Reference input current	vs Free-air temperature	5
I_{KA}	Cathode current	vs Cathode voltage	6, 7
I_{off}	Off-state cathode current	vs Free-air temperature	8
$\Delta V_{I(ref)}$	Change in reference voltage to change in cathode voltage	vs Free-air temperature	9
V_n	Equivalent input noise voltage	vs Frequency over a 10-second time-period	10, 11
A_V	Small-signal voltage amplification	vs Frequency	12
$\|z_{KA}\|$	Reference impedance	vs Frequency	13
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Table of Application Circuits

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TYPICAL CHARACTERISTICS†

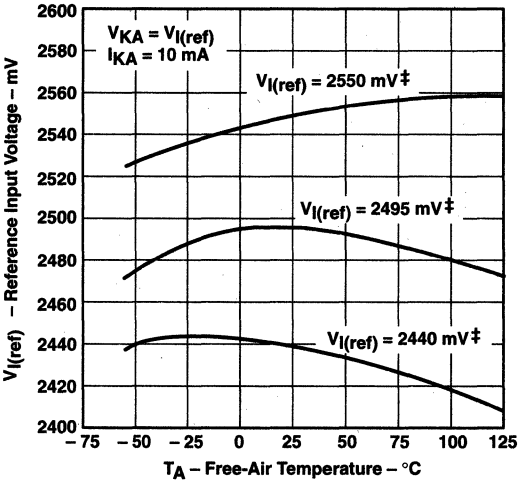

REFERENCE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

Figure 4

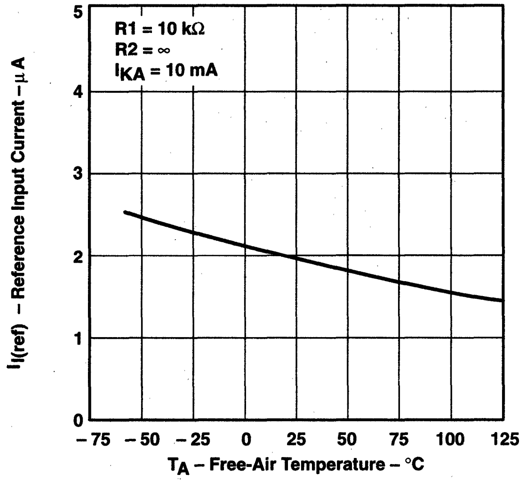

REFERENCE INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

Figure 5

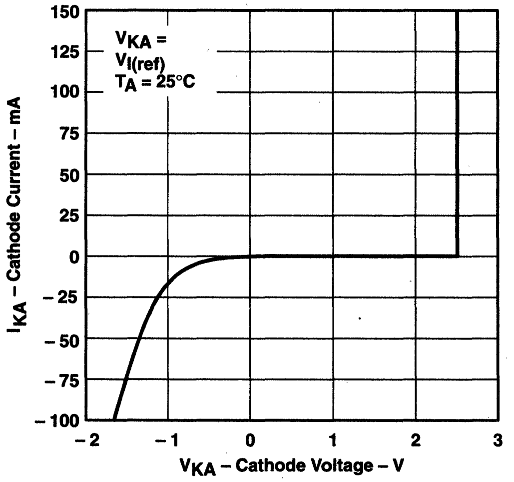

CATHODE CURRENT
vs
CATHODE VOLTAGE

Figure 6

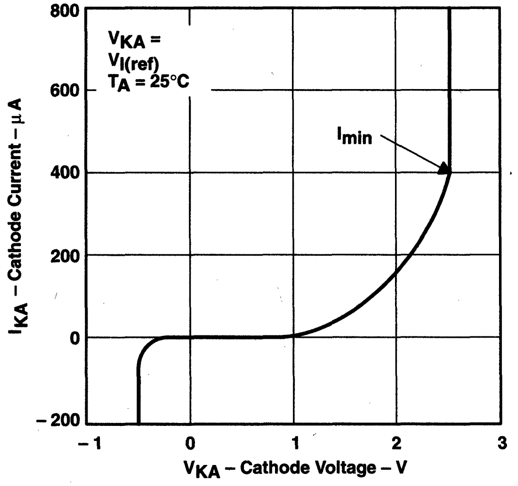

CATHODE CURRENT
vs
CATHODE VOLTAGE

Figure 7

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ Data is for devices having the indicated value of $V_{I(ref)}$ at I_{KA} = 10 mA, T_A = 25°C.

TYPICAL CHARACTERISTICS†

OFF-STATE CATHODE CURRENT vs FREE-AIR TEMPERATURE

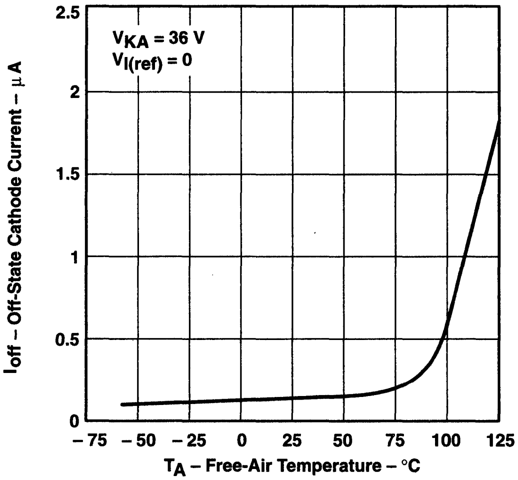


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE TO DELTA CATHODE VOLTAGE vs FREE-AIR TEMPERATURE

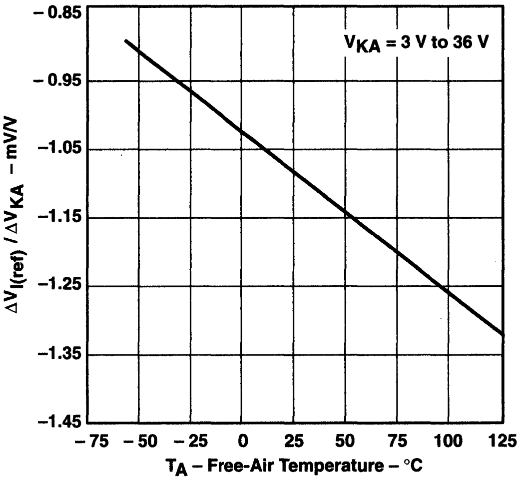


Figure 9

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

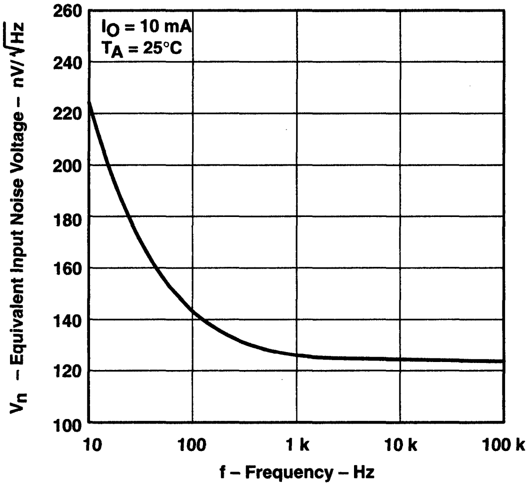


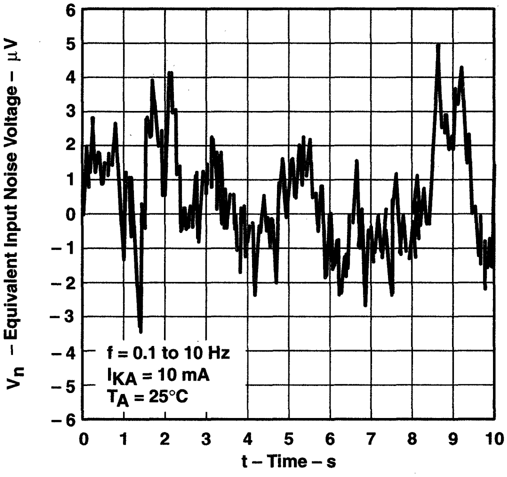
Figure 10

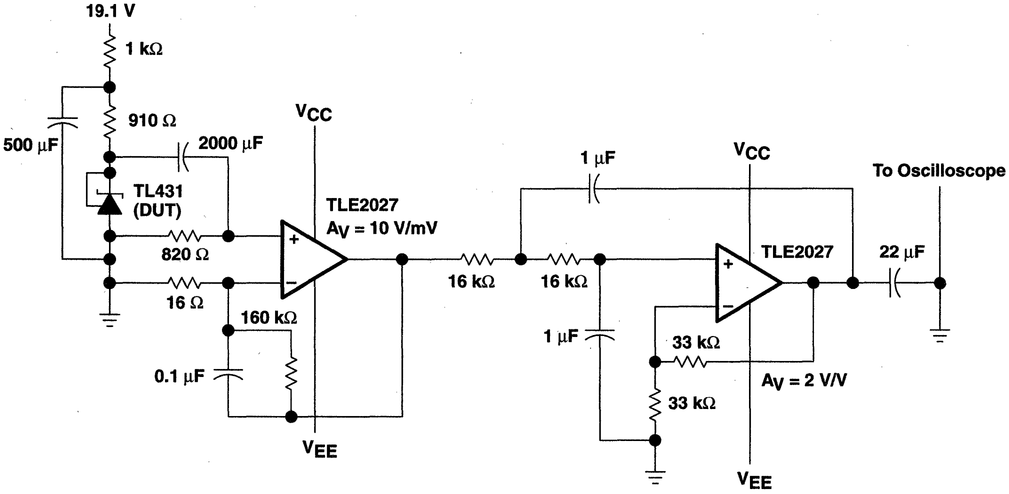
---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD



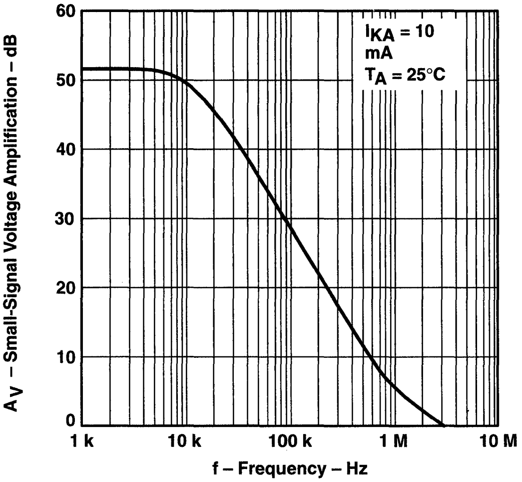


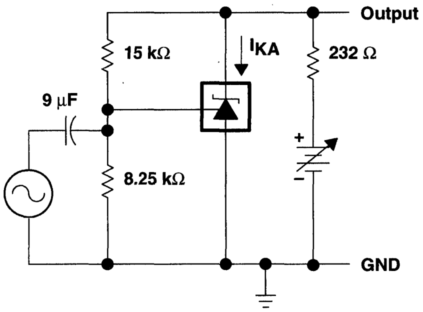
TEST CIRCUIT FOR EQUIVALENT INPUT NOISE VOLTAGE

Figure 11

TYPICAL CHARACTERISTICS

SMALL-SIGNAL VOLTAGE AMPLIFICATION vs FREQUENCY

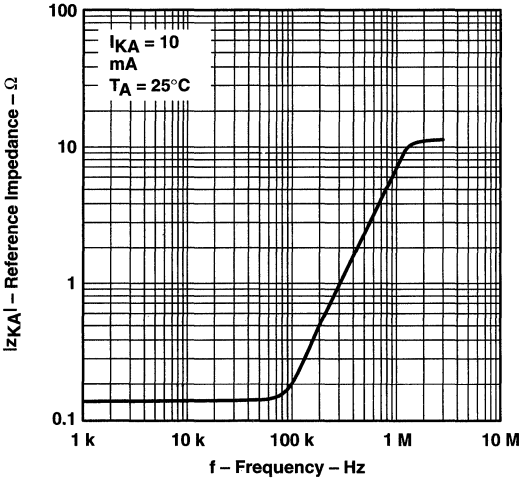


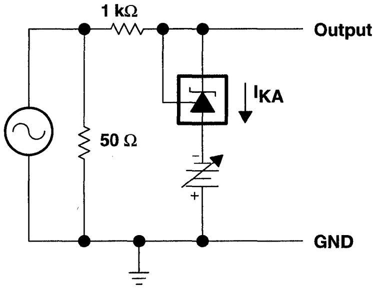


TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

Figure 12

REFERENCE IMPEDANCE vs FREQUENCY

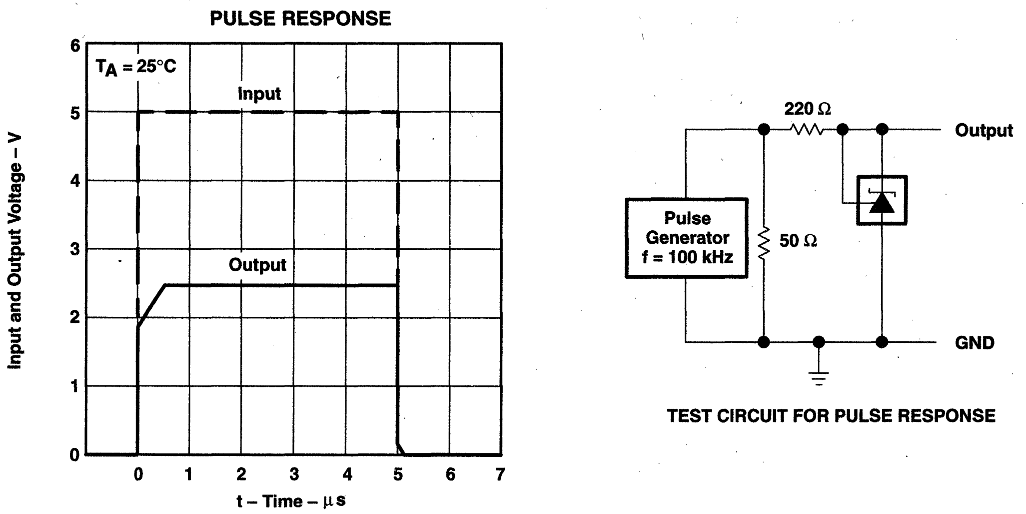




TEST CIRCUIT FOR REFERENCE IMPEDANCE

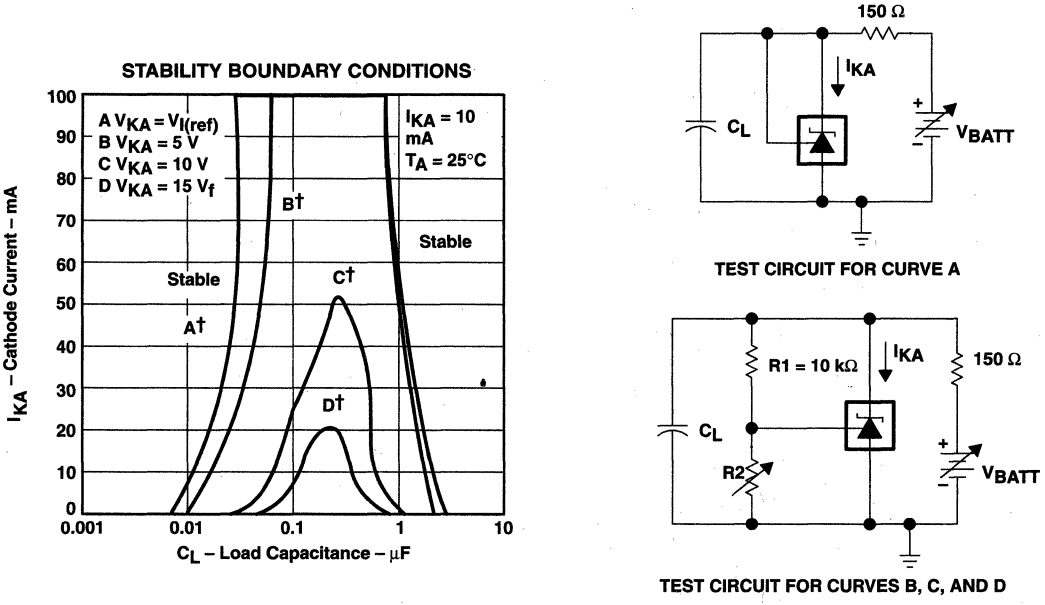
Figure 13

TYPICAL CHARACTERISTICS


PULSE RESPONSE

TEST CIRCUIT FOR PULSE RESPONSE

Figure 14


STABILITY BOUNDARY CONDITIONS

TEST CIRCUIT FOR CURVE A

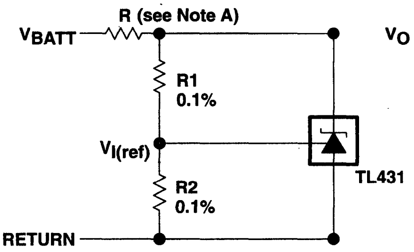
TEST CIRCUIT FOR CURVES B, C, AND D

Figure 15

---

† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_{KA} conditions with C_L = 0. V_{BATT} and C_L were then adjusted to determine the ranges of stability.

APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

NOTE A: R should provide cathode current ≥ 1-mA to the TL431 at minimum V_{BATT}.

Figure 16. Shunt Regulator

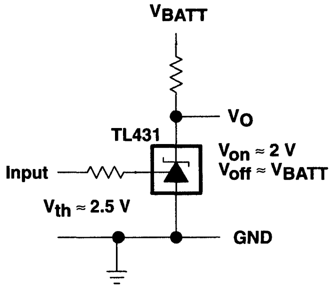
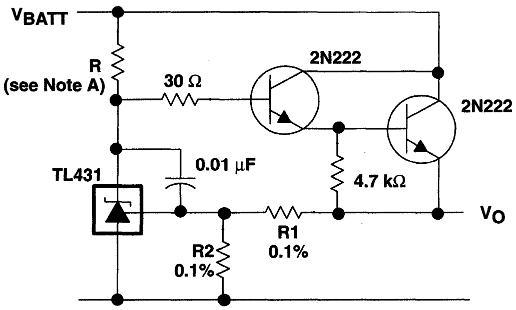


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold

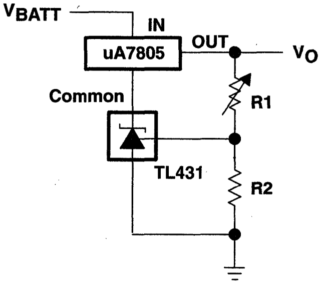


$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

NOTE A: R should provide cathode current ≥ 1-mA to the TL431 at minimum V_{BATT}.

Figure 18. Precision High-Current Series Regulator

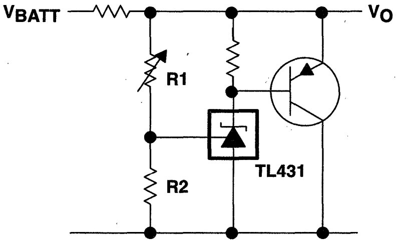
APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

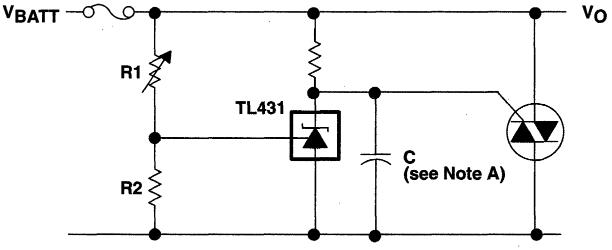
$$\text{Min } V_O = V_{I(ref)} + 5\text{ V}$$

Figure 19. Output Control of a Three-Terminal Fixed Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 20. High-Current Shunt Regulator



NOTE A: Refer to the stability boundary conditions in Figure 15 to determine allowable values for C.

Figure 21. Crowbar Circuit

APPLICATION INFORMATION

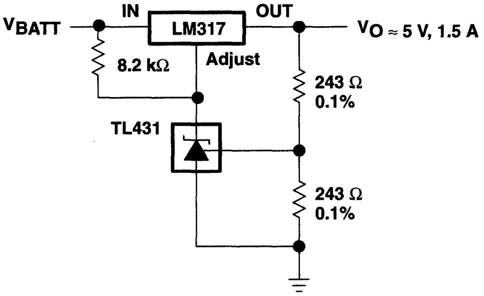
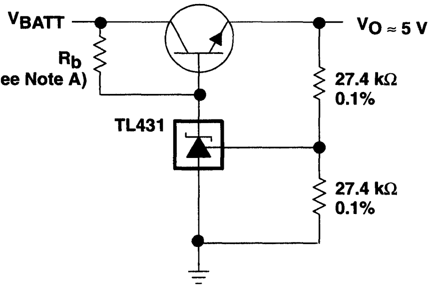


Figure 22. Precision 5-V, 1.5-A Regulator



NOTE A. R_b should provide cathode current ≥ 1-mA to the TL431.

Figure 23. Efficient 5-V Precision Regulator

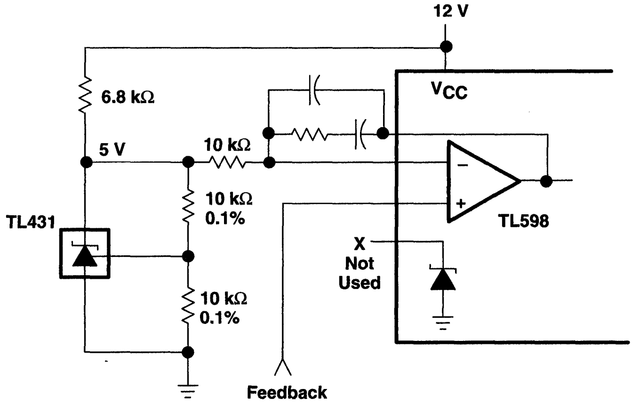
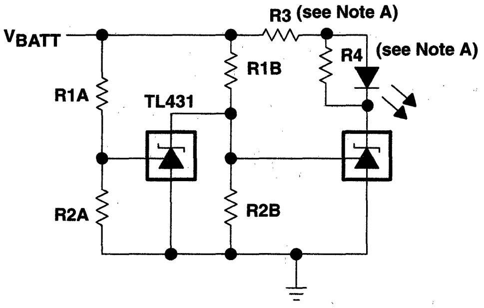


Figure 24. PWM Converter With Reference

APPLICATION INFORMATION



$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{I(ref)}$$

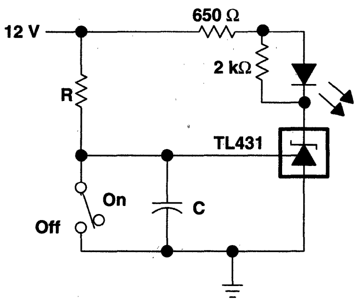
$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right) V_{I(ref)}$$

LED on when

Low Limit < V_{BATT} < High Limit

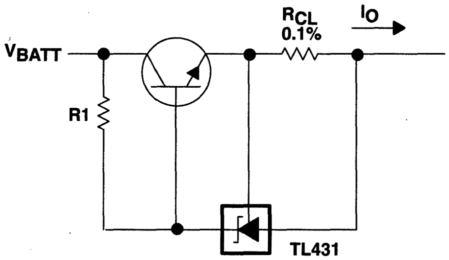
NOTE A: R3 and R4 are selected to provide the desired LED intensity and cathode current ≥ 1 mA to the TL431 at the available V_{BATT}.

Figure 25. Voltage Monitor



$$\text{Delay} = R \times C \times l_n\left(\frac{12\ V}{12\ V - V_{I(ref)}}\right)$$

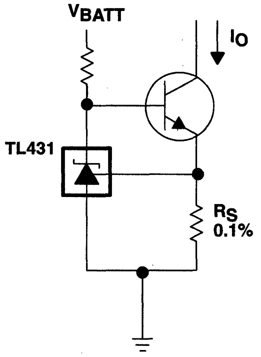
Figure 26. Delay Timer



$$I_{out} = \frac{V_{I(ref)}}{R_{CL}} + I_{KA}$$

$$R1 = \frac{V_{BATT}}{\frac{I_O}{h_{FE}} + I_{KA}}$$

Figure 27. Precision Current Limiter

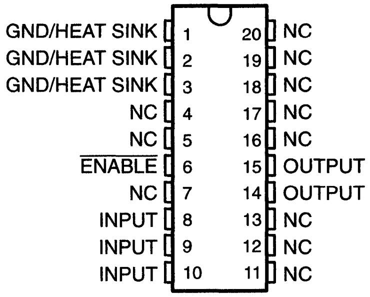


$$I_O = \frac{V_{I(ref)}}{R_S}$$

Figure 28. Precision Constant-Current Sink

- **Very Low-Dropout Voltage . . . Less Than 400 mV at 300 mA**
- **Standby Mode Reduces Current to a Maximum of 150 μA**
- **Output Regulated to Within ±2% Over Full Temperature Range**
- **Packaged in Thin Shrink Small-Outline Package**
- **Only 10-μF Load Capacitor Required to Maintain Regulation at I_O = 300 mA**

PW PACKAGE
(TOP VIEW)



GND/HEAT SINK – These terminals have an internal connection to ground and must be grounded.
NC – No internal connection
† The PW package is only available in left-end taped and reeled (order device TL75LPxxQPWLE).

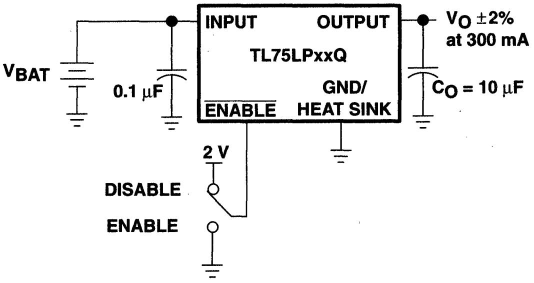
description

The TL75LPxxQ devices are low-dropout voltage regulators specifically targeted for use in portable applications. These devices generate fixed output voltages at loads of up to 300 mA with only 400-mV dropout over the full temperature range.

Low-dropout voltage regulators are commonly used in battery-powered systems such as analog and digital cellular phones. The TL75LPxx family of regulators feature a TTL/CMOS-compatible enable terminal, which can be used to switch the device into standby mode. This feature reduces power consumption when the instrument is not active. Less that 150 μA is required when the unit is disabled.

A concern in many new designs is conservation of board space and overall reduction in equipment size. The thin shrink small-outline package (TSSOP) minimizes board area and reduces component height. This package has a maximum height of less than 1.1 mm (compared to the 1.75 mm of a standard 8-pin SO package) and dimensions of only 6.5 mm by 4.4 mm.

typical application schematic



All low-dropout regulators require an external capacitor at the output to maintain regulation and stability. To further reduce board area and cost, the TL75LPxx devices are designed to require a minimum capacitor of only 10 μF. This is 1/10 the typical value used by many other low-dropout regulators. To simplify the task of choosing a suitable capacitor, TI has included in this datasheet a list of recommended capacitors for use with these devices.

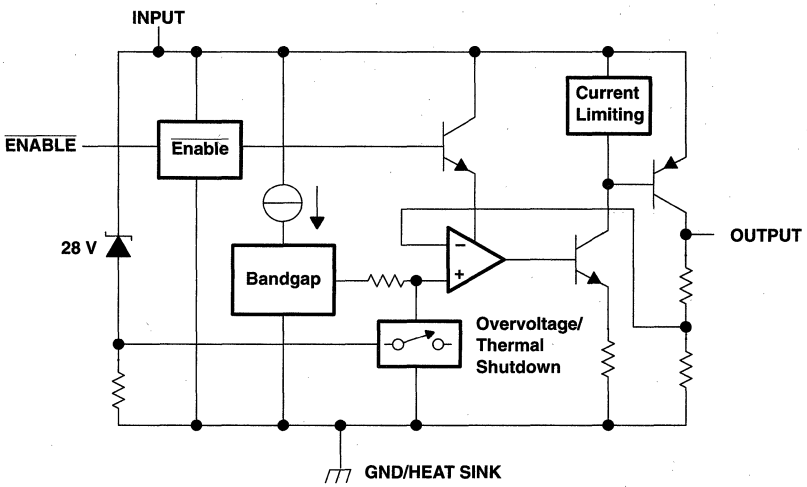
The TL75LPxxQ devices are characterized for operation over T_J = –40°C to 125°C.

AVAILABLE OPTIONS

T_J	V_O			PACKAGED DEVICES	CHIP FORM (Y)
	MIN	TYP	MAX	TSSOP (PW)	
–40°C to 125°C	4.75	4.85	4.95	TL75LP48QPWLE	TL75LP48Y
	4.9	5	5.1	TL75LP05QPWLE	TL75LP05Y
	7.84	8	8.16	TL75LP08QPWLE	TL75LP08Y
	9.8	10	10.2	TL75LP10QPWLE	TL75LP10Y
	11.76	12	12.24	TL75LP12QPWLE	TL75LP12Y

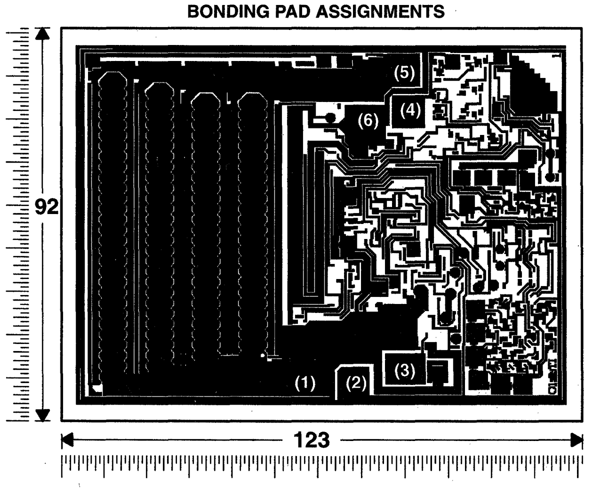
The PW package is available only in tape and reel. Chip forms are tested at 25°C.

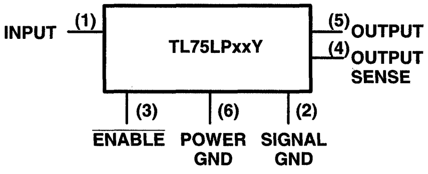
functional block diagram



TL75LPxxY chip information

This chip, when properly assembled, displays characteristics similar to the TL75LPxx. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 7 X 7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NOTE A. NOTE: SIGNAL GND and POWER GND must be tied together as close to device as possible. OUTPUT and OUTPUT SENSE should be tied together.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}, (See Note 1)	25 V
Output current, I_O	400 mA
Operating virtual junction temperature range, T_J	–55°C to 150°C
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network terminal ground.

2. Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	431 mW	166 mW
	T_C	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	T_P‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JP}$ is the thermal resistance between the junction and the device pin. To determine the virtual junction temperature (T_J) relative to the device pin temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JP} + T_P$, where P_D is the internal power dissipation of the device and T_P is the device pin temperature at the point of contact to the printed wiring board. The $R_{\theta JP}$ for the TL75LPxx series is 50.5°C/W.

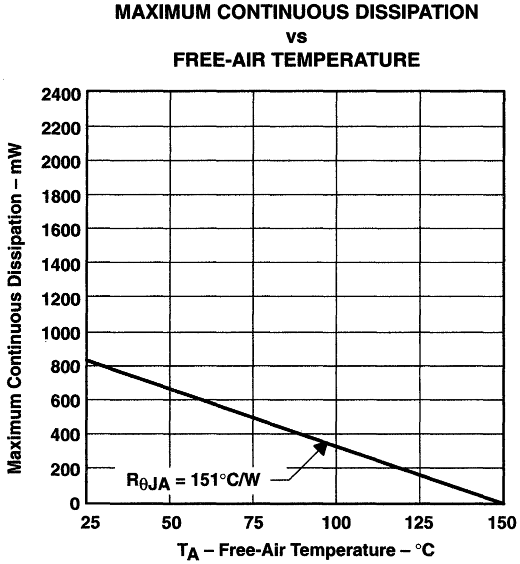


Figure 1

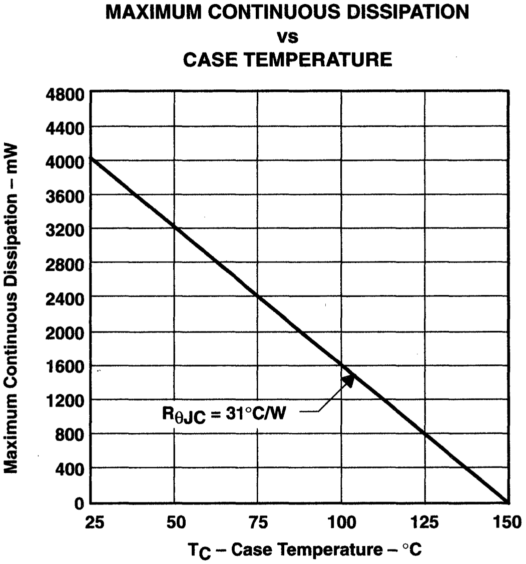


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL75LP48	5.15	23.0	V
	TL75LP05	5.3	23.0	
	TL75LP08	8.4	23.0	
	TL75LP10	10.4	23.0	
	TL75LP12	12.5	23.0	
High-level input voltage, $\overline{\text{ENABLE}}$, V_{IH}		2.0	15.0	V
Low-level input voltage, $\overline{\text{ENABLE}}$, V_{IL}		0	0.8	V
Output current range, I_O		5	300	mA
Operating virtual junction temperature range, T_J		–40	125	°C

electrical characteristics over operating virtual junction temperature range, V_I = 10 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP48Q			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 5.35 V to 10 V	4.75	4.85	4.95	V
Input voltage regulation	V_I = 5.35 V to 10 V, T_J = 25°C		10	25	mV
Ripple rejection	V_I = 5.6 V to 15.6 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output voltage regulation	I_O = 5 mA to 300 mA, T_J = 25°C		12	30	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		500		µV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics over operating virtual junction temperature range, $V_I = 10$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP05Q MIN	TL75LP05Q TYP	TL75LP05Q MAX	UNIT
Output voltage	$V_I = 5.5$ V to 10 V	4.9	5	5.1	V
Input voltage regulation	$V_I = 5.5$ V to 10 V, $T_J = 25°C$		10	25	mV
Ripple rejection	$V_I = 6$ V to 16 V, f = 120 Hz, $T_J = 25°C$	50	55		dB
Output voltage regulation	$I_O = 5$ mA to 300 mA, $T_J = 25°C$		12	30	mV
Dropout voltage	$I_O = 100$ mA		0.12	0.2	V
	$I_O = 200$ mA		0.17	0.3	
	$I_O = 300$ mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, $T_J = 25°C$		500		μV
Bias current	$I_O = 10$ mA		2.5	4	mA
	$I_O = 100$ mA		4	10	
	$I_O = 200$ mA		6	20	
	$I_O = 300$ mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}} = 0.8$ V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}} = 2$ V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}} = 2$ V		100	150	μA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics over operating virtual junction temperature range, $V_I = 10$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP08Q MIN	TL75LP08Q TYP	TL75LP08Q MAX	UNIT
Output voltage	$V_I = 8.6$ V to 15 V	7.84	8	8.16	V
Input voltage regulation	$V_I = 8.6$ V to 15 V, $T_J = 25°C$		12	40	mV
Ripple rejection	$V_I = 9$ V to 19 V, f = 120 Hz, $T_J = 25°C$	50	55		dB
Output voltage regulation	$I_O = 5$ mA to 300 mA, $T_J = 25°C$		12	40	mV
Dropout voltage	$I_O = 100$ mA		0.12	0.2	V
	$I_O = 200$ mA		0.17	0.3	
	$I_O = 300$ mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, $T_J = 25°C$		500		μV
Bias current	$I_O = 10$ mA		2.5	4	mA
	$I_O = 100$ mA		4	10	
	$I_O = 200$ mA		6	20	
	$I_O = 300$ mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}} = 0.8$ V		7	25	μA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}} = 2$ V		0.05	6	μA
Standby current	$\overline{\text{ENABLE}} = 2$ V		100	150	μA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics over operating virtual junction temperature range, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP10Q			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 10.6 V to 17 V	9.8	10	10.2	V
Input voltage regulation	V_I = 10.6 V to 17 V, T_J = 25°C		15	43	mV
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output voltage regulation	I_O = 5 mA to 300 mA, T_J = 25°C		15	50	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		1000		µV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics over operating virtual junction temperature range, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP12Q			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 12.7 V to 18 V	11.76	12	12.24	V
Input voltage regulation	V_I = 12.7 V to 18 V, T_J = 25°C		15	43	mV
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz, T_J = 25°C	50	55		dB
Output voltage regulation	I_O = 5 mA to 300 mA, T_J = 25°C		15	60	mV
Dropout voltage	I_O = 100 mA		0.12	0.2	V
	I_O = 200 mA		0.17	0.3	
	I_O = 300 mA		0.22	0.4	
Output noise voltage	f = 10 Hz to 100 kHz, T_J = 25°C		1000		µV
Bias current	I_O = 10 mA		2.5	4	mA
	I_O = 100 mA		4	10	
	I_O = 200 mA		6	20	
	I_O = 300 mA		9	30	
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics at $V_I = 10$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V, $T_J = 25$°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP48Y			UNIT
		MIN	TYP	MAX	
Output voltage			4.85		V
Input voltage regulation			10		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current			9		mA
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7		µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05		µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100		µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics at $V_I = 10$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V, $T_J = 25$°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP05Y			UNIT
		MIN	TYP	MAX	
Output voltage			5		V
Input voltage regulation			10		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current			9		mA
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7		µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05		µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100		µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics at $V_I = 10$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP08Y			UNIT
		MIN	TYP	MAX	
Output voltage			8		V
Input voltage regulation			12		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current			9		mA
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7		µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05		µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100		µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics at $V_I = 14$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}} = 0$ V, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP10Y			UNIT
		MIN	TYP	MAX	
Output voltage			10		V
Input voltage regulation			15		mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			15		mV
Dropout voltage			0.22		V
Output noise voltage	f = 10 Hz to 100 kHz		1000		µV
Bias current			9		mA
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7		µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05		µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100		µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

electrical characteristics at V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ = 0 V, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL75LP12Y			UNIT
		MIN	TYP	MAX	
Output voltage		11.76	12	12.24	V
Input voltage regulation			15	43	mV
Ripple rejection	f = 120 Hz		55		dB
Output voltage regulation			12	60	mV
Dropout voltage			0.22	0.4	V
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current			9	30	mA
High-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 0.8 V		7	25	µA
Low-level input current, $\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ = 2 V		0.05	6	µA
Standby current	$\overline{\text{ENABLE}}$ = 2 V		100	150	µA

† Pulse-testing techniques maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor with equivalent series resistance within the guidelines shown in Figures 3 and 4 on the output. All measurements are taken with a tantalum electrolytic capacitor. Although not normally recommended, an aluminum electrolytic capacitor can be used. Attention must be given its ESR value, particularly at low temperatures.

PARAMETER MEASUREMENT INFORMATION

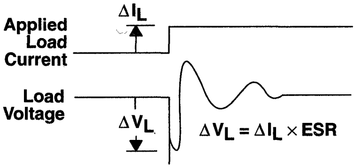
The TL75LPxx series are low-dropout voltage regulators. This means that the capacitance is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can establish the capacitance value and ESR range for optimum regulator performance.

Figure 3 shows the recommended range of ESR, measured at 120 Hz, for a given load with a 10-µF capacitor on the output. In addition, it shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 4 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 µF and a maximum ESR limit of 2 Ω. Figure 4 establishes the amount that the minimum ESR limit of Figure 3 can be adjusted for different capacitor values. For example, when the minimum load needed is 200 mA, Figure 3 suggests an ESR range of 0.8 Ω to 2 Ω for 10 µF. Figure 4 shows that changing the capacitor from 10 µF to 400 µF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω. This expanded ESR range is achieved by using a larger capacitor at the output. For better stability in low-current applications, it is recommended that a small resistance be placed in series with the capacitor (see Table 1) so that the ESR better approximates those in Figures 3 and 4.

Table 1. Compensations for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 µF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 µF	0.6 Ω	T491D336M010AS	0.5 Ω



OUTPUT CAPACITOR
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT

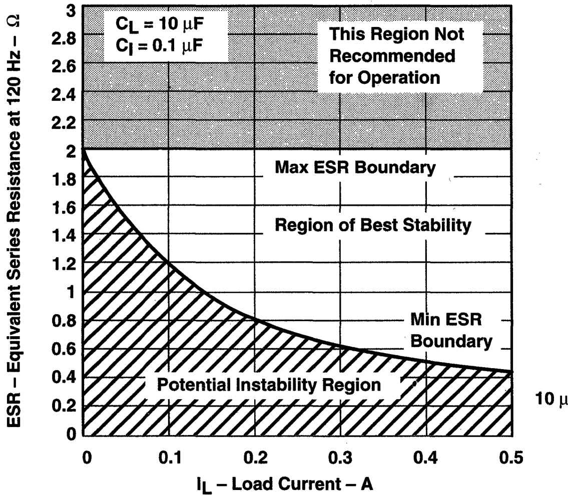


Figure 3

OUTPUT CAPACITOR
STABILITY
vs
EQUIVALENT SERIES RESISTANCE

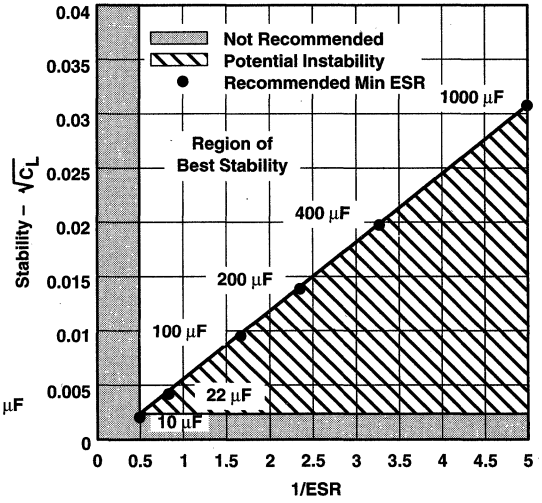


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
Output voltage		vs Input voltage	5
Input current	I_O = 10 mA	vs Input voltage	6
	I_O = 100 mA	vs Input voltage	7
Dropout voltage		vs Output current	8
Quiescent current		vs Output current	9
Short-circuit protection conditions output voltage		vs Output current	10
Load transient response			11
Line transient response			12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE

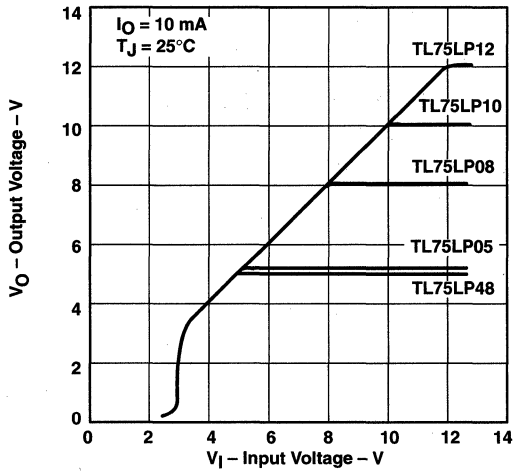


Figure 5

INPUT CURRENT vs INPUT VOLTAGE

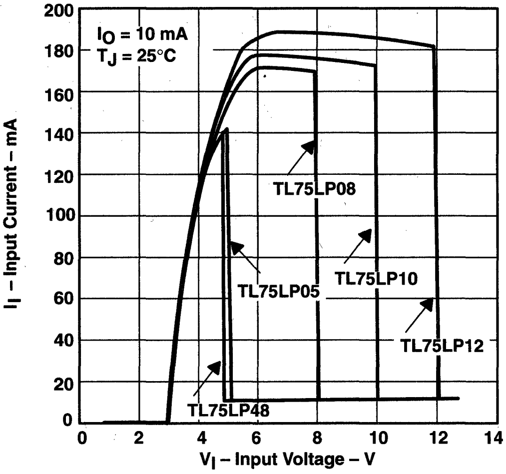


Figure 6

INPUT CURRENT vs INPUT VOLTAGE

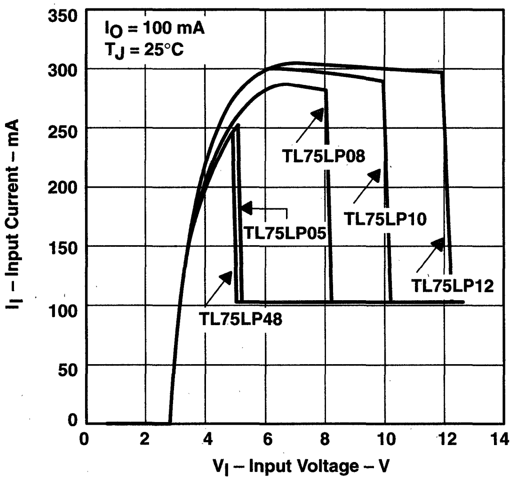


Figure 7

DROPOUT VOLTAGE vs OUTPUT CURRENT

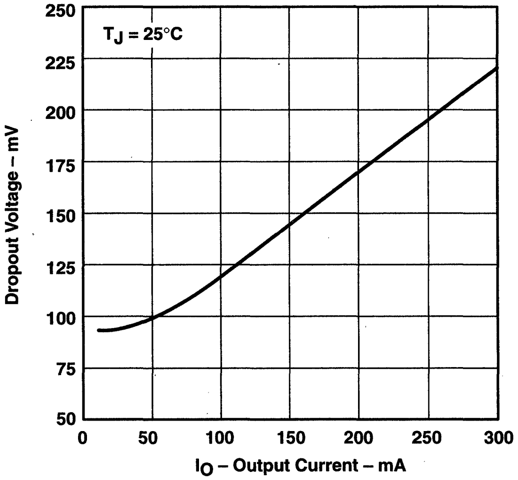


Figure 8

TYPICAL CHARACTERISTICS

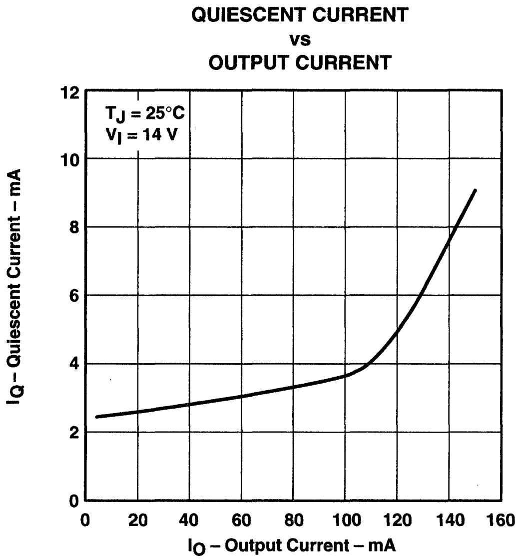

QUIESCENT CURRENT
vs
OUTPUT CURRENT

Figure 9

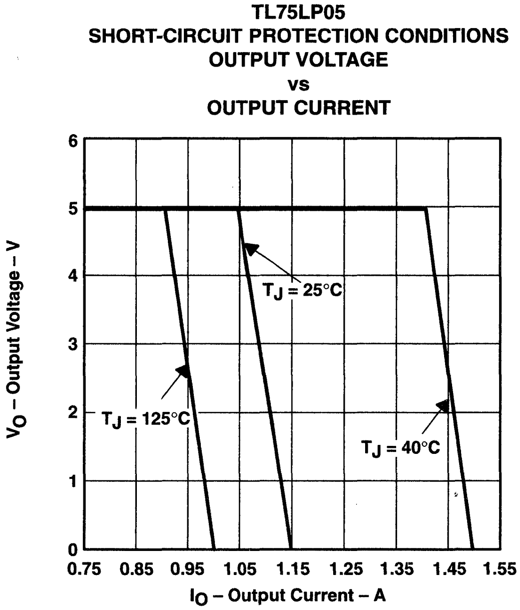

TL75LP05
SHORT-CIRCUIT PROTECTION CONDITIONS
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 10

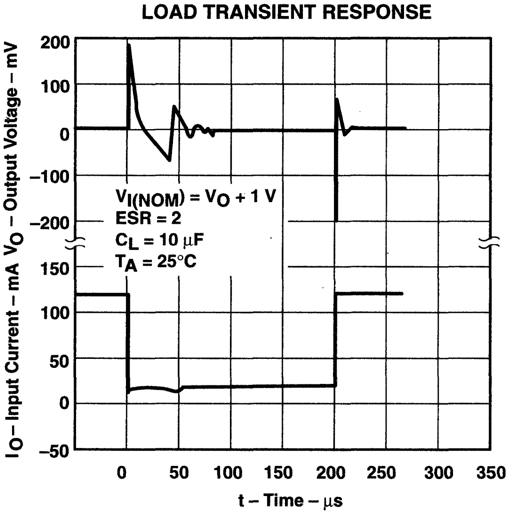

LOAD TRANSIENT RESPONSE

Figure 11

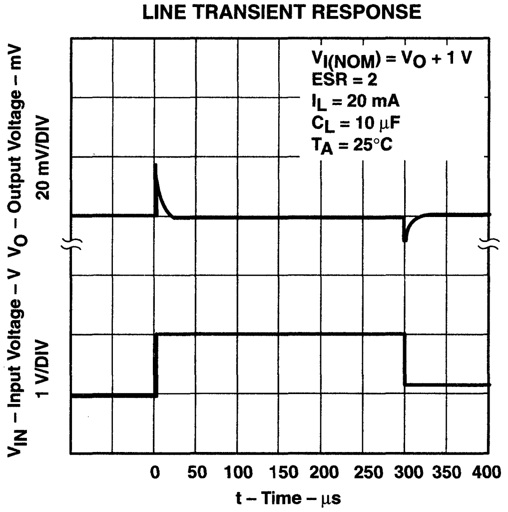

LINE TRANSIENT RESPONSE

Figure 12

TL750L, TL751L SERIES
TL751L05M, TL751L12M, TL750LxxY
LOW-DROPOUT VOLTAGE REGULATORS

SLVS017B – SEPTEMBER 1987 – REVISED AUGUST 1995

- **Very Low Dropout Voltage, Less Than 0.6 V at 150 mA**
- **Very Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751L Series, TL751L05M, and TL751L12M**
- **60-V Load-Dump Protection**
- **Reverse Transient Protection to −50 V**
- **Internal Thermal Overload Protection**
- **Overvoltage Protection**
- **Internal Overcurrent Limiting Circuitry**
- **Less Than 500-µA Disable (TL751L Series, TL75L05M, and TL75L12M)**

description

The TL750L and TL751L series and the TL751L05M and TL751L12M are low-dropout positive voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry along with internal reverse-battery protection circuitry to protect both itself and the regulated system. Both the series and the TL751L05M and TL751L12M are fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

The TL750L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. They are available in TO-226AA (formerly TO-92) (LP) packages, TO-220AB (KC) packages, 8-pin small-outline plastic packages (D), and 8-pin plastic dual-in-line packages (P).

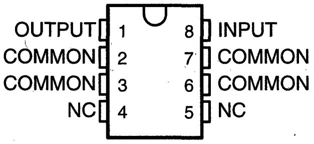
The TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. This series is offered in the 8-pin small-outline plastic package and the 8-pin plastic dual-in-line package.

The TL751L05M and TL751L12M fixed-output voltage regulators also offer 5-V and 12-V options with an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. The TL751LxM is offered in the FK and JG package.

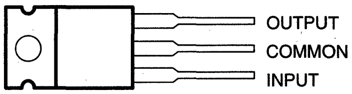
AVAILABLE OPTIONS

T_A	$V_O$typ AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TO-220AB (KC)	TO-226AA (LP)	CERAMIC FLATPACK (P)	
0°C to 125°C	5V	TL750L05CD TL751L05CD	—	—	TL750L05CKC	TL750L05CLP	TL750L05CP TL751L05CP	TL750L05Y
	8V	TL750L08CD TL751L08CD	—	—	TL750L08CKC	TL750L08CLP	TL750L08CP TL751L08CP	TL750L08Y
	10V	TL750L10CD TL751L10CD	—	—	TL750L10CKC	TL750L10CLP	TL750L10CP TL751L10CP	TL750L10Y
	12V	TL750L12CD TL751L12CD	—	—	TL750L12CKC	TL750L12CLP	TL750L12CP TL751L12CP	TL750L12Y
−40°C to 125°C	5V	TL750L05QD TL751L05QD	—	—	TL750L05QKC	TL750L05QLP	TL750L05QP TL751L05QP	—
	8V	TL750L08QD TL751L08QD	—	—	TL750L08QKC	TL750L08QLP	TL750L08QP TL751L08QP	—
	10V	TL750L10QD TL751L10QD	—	—	TL750L10QKC	TL750L10QLP	TL750L10QP TL751L10QP	—
	12V	TL750L12QD TL751L12QD	—	—	TL750L12QKC	TL750L12QLP	TL750L12QP TL751L12QP	—
−55°C to 125°C	5V	—	TL751L05MFK	TL751L05MJG	—	—	—	—
	12V	—	TL751L12MFK	TL751L12MJG	—	—	—	—

TL750L . . . D
SMALL-OUTLINE PACKAGE
(TOP VIEW)



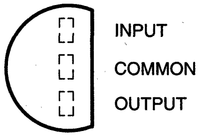
TL750L . . . KC
HEAT-SINK-MOUNTED PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

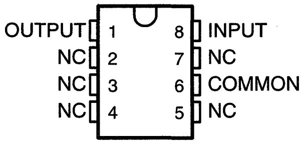
TO-220AB

TL750L . . . LP
SILECT™ PACKAGE
(TOP VIEW)

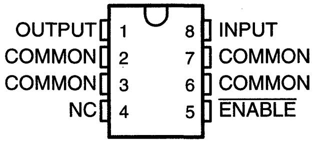


TO-226AA

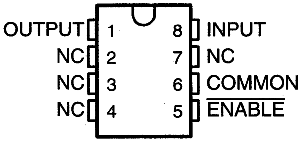
TL750L . . . P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



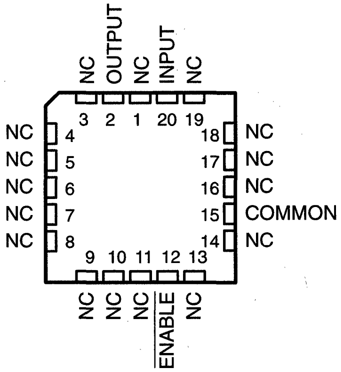
TL751L . . . D
SMALL-OUTLINE PACKAGE
(TOP VIEW)



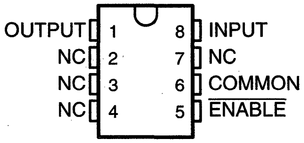
TL751L . . . P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL751L05M, TL751L12M . . . FK PACKAGE
(TOP VIEW)



TL751L05M, TL751L12M . . . JG PACKAGE
(TOP VIEW)



NC–No internal connection

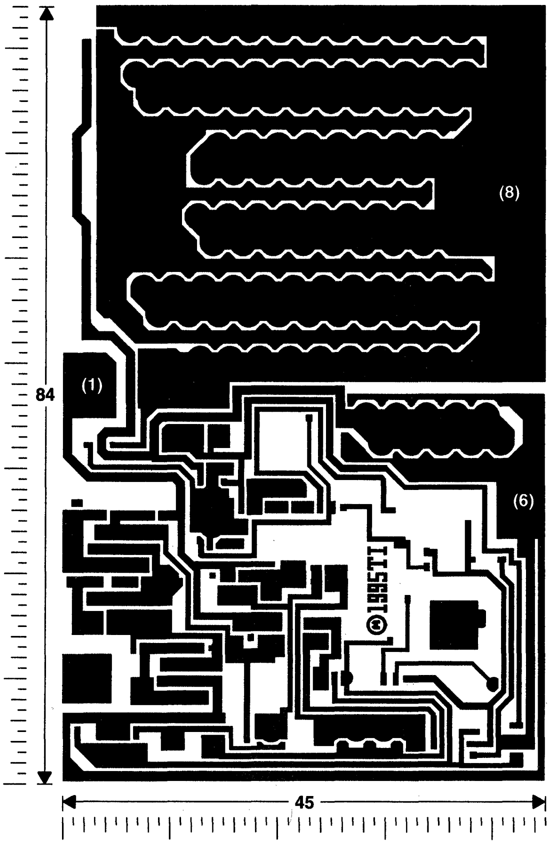
ACTUAL DEVICE COMPONENT COUNT	
Transistors	20
JFET	2
Diodes	5
Resistors	16

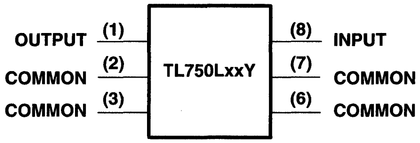
SILECT is a trademark of Texas Instruments Incorporated.

TL750LxxY chip information

These chips, when properly assembled, display characteristics similar to the TL750LxxC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max= 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

TERMINAL NUMBERS ARE FOR THE TL750 D AND P PACKAGES

TERMINALS 2, 3, 6, AND 7 ARE CONNECTED TOGETHER

TERMINALS 4 AND 5 ARE NOT CONNECTED

absolute maximum ratings over operating junction temperature range (unless otherwise noted)

	TL750L	TL751L TL751L_M	UNIT
Continuous input voltage	26	26	V
Transient input voltage, $T_A = 25°C$ (see Note 1)	60	60	V
Continuous reverse input voltage	−15	−15	V
Transient reverse input voltage: $t \leq 100$ ms	−50	−50	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating virtual junction temperature range, T_J	−40 to 150	−40 to 150	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds	260	260	°C

NOTE 1: The transient input voltage rating applies for the waveform described in Figure 1.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	825 mW	6.6 mW/°C	528 mW	429 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW
KC	2000 mW	15.2 mW/°C	1316 mW	1088 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNITS
Input voltage, V_I		TL75_L05 and TL751L05M	6	26	V
		TL75_L08	9	26	
		TL75_L10	11	26	
		TL75_L12 and TL751L12M	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}		TL751L and TL751L_M	2	15	V
Low-level ENABLE input voltage, V_{IL}†	$T_A = 25°C$	TL751L and TL751L_M	−0.3	0.8	V
	T_A = Full range	TL751L and TL751L_M	−0.15	0.8	
Output current range, I_O		TL75_L and TL751L_M	0	150	mA
Operating virtual junction temperature, T_J		TL75_L_C	0	125	°C
		TL75_L_Q	−40	125	
		TL751L_M	−55	125	

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			TL750L05, TL751L05 TL751L05M			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V	I_O = 0 to 150 mA	T_J = 25°C	4.80	5	5.2	V
			T_J = $T_J$min to 125°C	4.75		5.25	
Input regulation voltage	V_I = 9 V to 16 V				5	10	mV
	V_I = 6 V to 26 V				6	30	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		60*	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				20	50	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		µV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 6 V to 26 V,	I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

‡ Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			TL750L08, TL751L08			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V	I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
			T_J = $T_J$min to 125°C	7.6		8.4	
Input regulation voltage	V_I = 10 V to 17 V				10	20	mV
	V_I = 9 V to 26 V				25	50	
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		60*	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				40	80	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		µV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 9 V to 26 V,	I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

‡ Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TL750L10, TL751L10			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = $T_J$min to 125°C	9.5		10.5	
Input regulation voltage	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Input bias current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V				0.5	

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TL750L12, TL751L12 TL751L12M			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = $T_J$min to 125°C	11.4		12.6	
Input regulation voltage	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50*	55		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Input bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V				0.5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristicsV_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL750L05Y MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V I_O = 0 to 150 mA		5		V
Input regulation voltage	V_I = 9 V to 16 V		5		mV
	V_I = 6 V to 26 V		6		
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		65		dB
Output regulation voltage	I_O = 5 mA to 150 mA		20		mV
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Input bias current	I_O = 150 mA		10		mA
	V_I = 6 V to 26 V, I_O = 10 mA		1		

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL750L08Y MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V I_O = 0 to 150 mA		8		V
Input regulation voltage	V_I = 10 V to 17 V		10		mV
	V_I = 9 V to 26 V		25		
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		65		dB
Output regulation voltage	I_O = 5 mA to 150 mA		40		mV
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Input bias current	I_O = 150 mA		10		mA
	V_I = 9 V to 26 V, I_O = 10 mA		1		

‡ Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL750L10Y			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA		10		V
Input regulation voltage	V_I = 12 V to 19 V		10		mV
	V_I = 11 V to 26 V		30		
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		65		dB
Output regulation voltage	I_O = 5 mA to 150 mA		50		mV
Output noise voltage	f = 10 Hz to 100 kHz		700		µV
Input bias current	I_O = 150 mA		10		mA
	V_I = 11 V to 26 V, I_O = 10 mA		1		

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL750L12Y			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA		12		V
Input regulation voltage	V_I = 14 V to 19 V		15		mV
	V_I = 13 V to 26 V		20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55		dB
Output regulation voltage	I_O = 5 mA to 150 mA		50		mV
Output noise voltage	f = 10 Hz to 100 kHz		700		µV
Input bias current	I_O = 150 mA		10		mA
	V_I = 13 V to 26 V, I_O = 10 mA		1		

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 1 Ω across the output.

TYPICAL CHARACTERISTICS

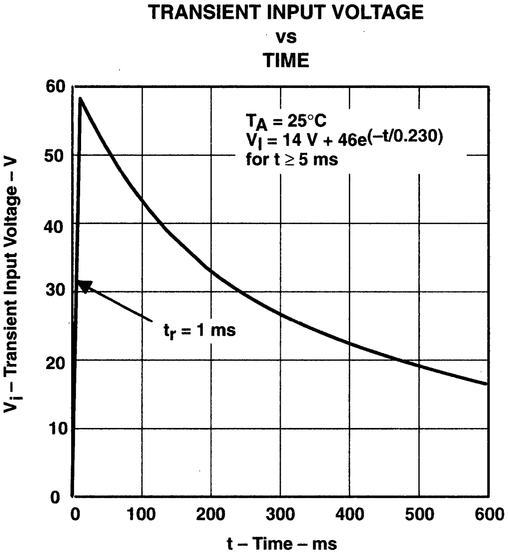


Figure 1

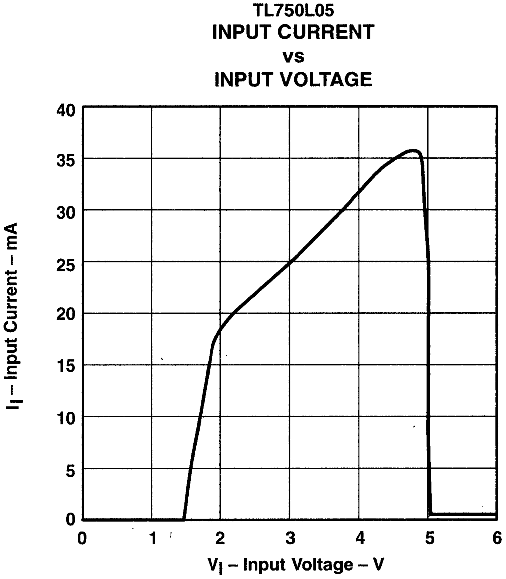


Figure 2

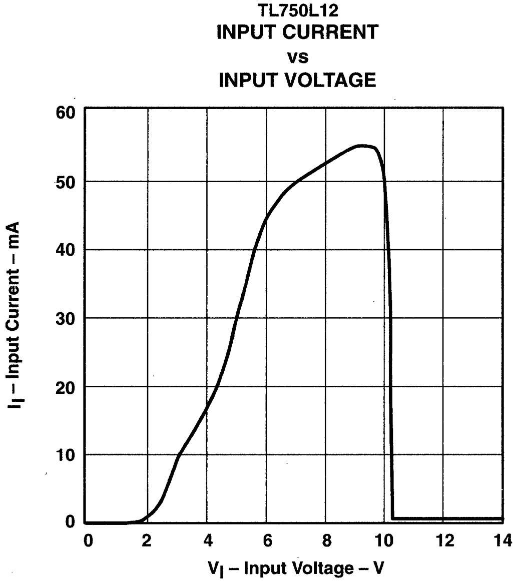


Figure 3

TL750M, TL751M SERIES
LOW-DROPOUT VOLTAGE REGULATORS

SLVS021D – JANUARY 1988 – REVISED AUGUST 1995

- **Very Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **60-V Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Overcurrent Limiting Circuitry**

description

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M incorporate on-board overvoltage and current-limit protection circuitry to protect both themselves and the regulated system. Both series are fully protected against 60-V load-dump and reverse battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options available in 3-lead KC (TO-220AB) and KTE plastic packages.

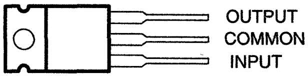
The TL751M series of fixed-output voltage regulators also offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input gives the designer complete control over power up, allowing sequential power up or emergency shutdown. When taken high, the enable input places the regulator output in a high-impedance state. It is completely TTL- and CMOS-compatible. The TL751M series is offered in 5-lead KC and KTG plastic packages.

The TL750MxxC and TL751MxxC are characterized for operation from 0°C to 125°C virtual junction temperature, and the TL750MxxQ and TL751MxxQ series are characterized for operation from –40°C to 125°C virtual junction temperature.

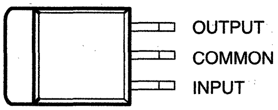
AVAILABLE OPTIONS

T_J	V_OTYP (V)	PACKAGED DEVICES				CHIP FORM (Y)
		HEAT-SINK MOUNTED (3-PIN) (KC)	HEAT-SINK MOUNTED (5-PIN) (KC)	PLASTIC FLANGE-MOUNT (KTE)	PLASTIC FLANGE-MOUNT (KTG)	
0°C to 125°C	5	TL750M05CKC	TL751M05CKC	TL750M05CKTG	TL751M05CKTG	TL750M05Y
	8	TL750M08CKC	TL751M08CKC	TL750M08CKTG	TL751M08CKTG	TL750M08Y
	10	TL750M10CKC	TL751M10CKC	TL750M10CKTG	TL751M10CKTG	TL750M10Y
	12	TL750M12CKC	TL751M12CKC	TL750M12CKTG	TL751M12CKTG	TL750M12Y
–40°C to 125°C	5	TL750M05QKC	TL751M05QKC	TL750M05QKTG	TL751M05QKTG	—
	8	TL750M08QKC	TL751M08QKC	TL750M08QKTG	TL751M08QKTG	—
	10	TL750M10QKC	TL751M10QKC	TL750M10QKTG	TL751M10QKTG	—
	12	TL750M12QKC	TL751M12QKC	TL750M12QKTG	TL751M12QKTG	—

TL750M . . . 3-LEAD KC PACKAGE
(TOP VIEW)

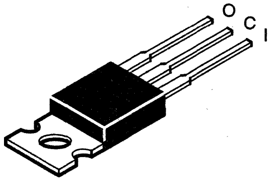


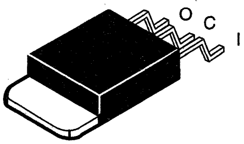
TL750M . . . 3-LEAD KTE PACKAGE
(TOP VIEW)



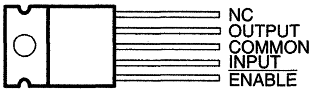
NOTE A: The common terminal is in electrical contact with the mounting base.

TO-200AB

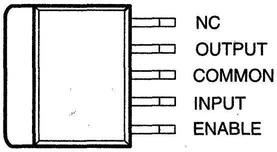




TL751M . . . 5-LEAD KC PACKAGE
(TOP VIEW)

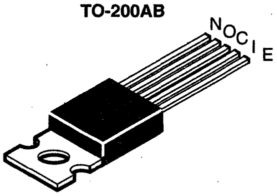


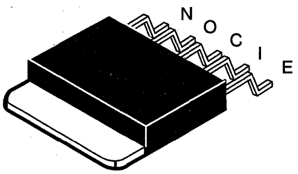
TL750M . . . 5-LEAD KTG PACKAGE
(TOP VIEW)



NOTE A: The common terminal is in electrical contact with the mounting base.

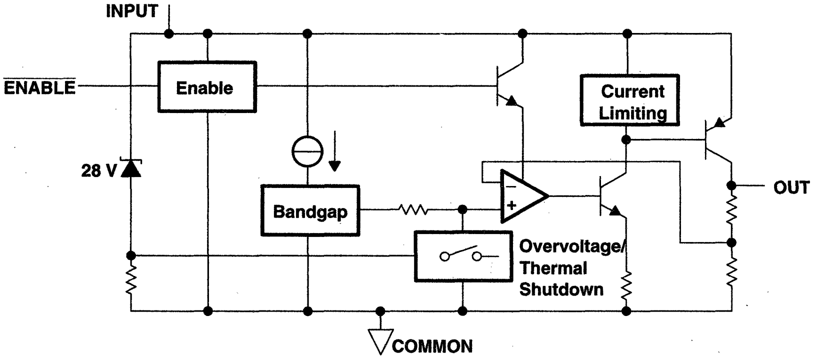
TO-200AB





NC – No internal connection

TL751Mxx functional block diagram

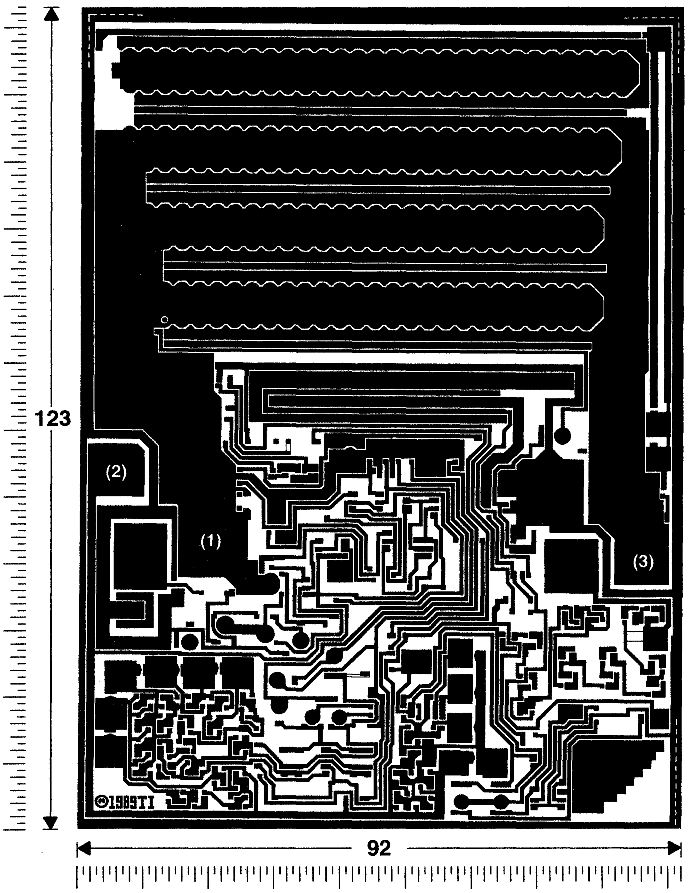


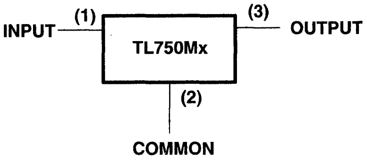
ACTUAL DEVICE COMPONENT COUNT	
Transistors	46
Diodes	14
Resistors	44
Capacitors	4
JFET	1
Tunnels (emitter R)	2

TL750MxxY chip information

This chip, when properly assembled, displays characteristics similar to the TL750MxxC. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL
BONDING PADS: 7 X 7 MILS MINIMUM
$T_J$max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over virtual junction temperature range (unless otherwise noted)†

Continuous input voltage	26 V
Transient input voltage (see Figure 5)	60 V
Continuous reverse input voltage	–15 V
Transient reverse input voltage: t = 100 ms	–50 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2 W
Continuous total power dissipation at (or below) 40°C case temperature (see Note 1)	20 W
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above T_A = 25°C and T_C = 40°C, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

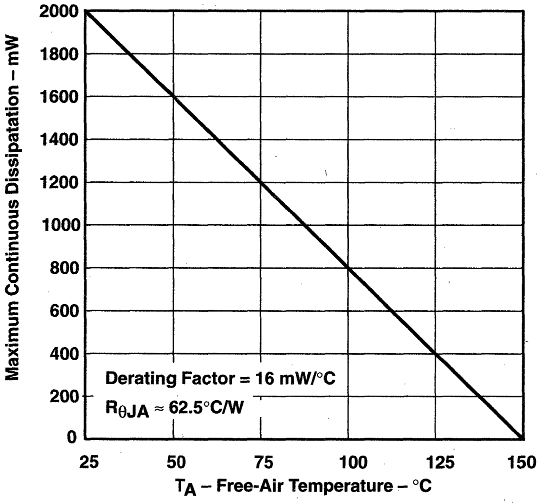


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

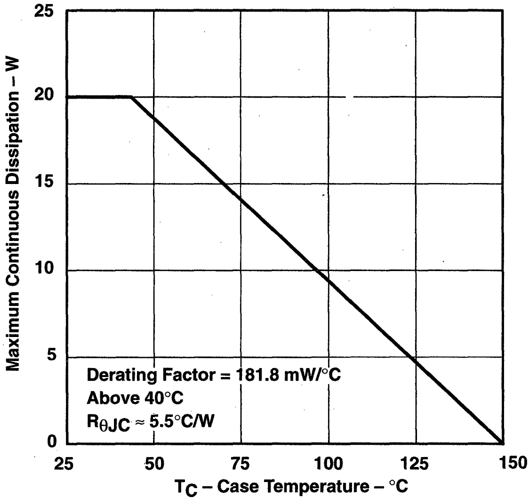


Figure 2

recommended operating conditions over recommended virtual junction temperature range

		MIN	MAX	UNIT
Input voltage range, V_I	TL75xM05	6	26	V
	TL75xM08	9	26	
	TL75xM10	11	26	
	TL75xM12	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}	TL751Mxx	2	15	V
Low-level $\overline{\text{ENABLE}}$ input voltage, V_{IL}	TL751Mxx	0	0.8	
Output current range, I_O			750	mA
Operating virtual junction temperature range, T_J	TL75xMxxC	0	125	°C
	TL75xMxxQ	–40	125	

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M05, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS			TL750M05, TL751M05			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V,	I_O = 0 mA to 750 mA	T_J = 25°C	4.9	5	5.1	V
			T_J = MIN to MAX†	4.9		5.1	
Input voltage regulation	V_I = 9 V to 16 V,	I_O = 250 mA			10	25	mV
	V_I = 6 V to 26 V,	I_O = 250 mA			12	50	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA				20	50	mV
Dropout voltage	I_O = 500 mA					0.5	V
	I_O = 750 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Bias current	I_O = 750 mA				60	75	mA
	I_O = 10 mA					5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V					200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M08, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS			TL750M08, TL751M08			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V,	I_O = 0 mA to 750 mA	T_J = 25°C	7.84	8	8.16	V
			T_J = MIN to MAX†	7.84		8.16	
Input voltage regulation	V_I = 10 V to 17 V,	I_O = 250 mA			12	40	mV
	V_I = 9 V to 26 V,	I_O = 250 mA			15	68	
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA				24	80	mV
Dropout voltage	I_O = 500 mA					0.5	V
	I_O = 750 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Bias current	I_O = 750 mA				60	75	mA
	I_O = 10 mA					5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V					200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M10, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M10, TL751M10			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V, I_O = 0 mA to 750 mA	T_J = 25°C	9.8	10	10.2	V
		T_J = MIN to MAX†	9.8		10.2	
Input voltage regulation	V_I = 12 V to 18 V, I_O = 250 mA			15	43	mV
	V_I = 11 V to 26 V, I_O = 250 mA			20	75	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			30	100	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		µV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2$ V				200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M12, TL751M12			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 mA to 750 mA	T_J = 25°C	11.76	12	12.24	V
		T_J = MIN to MAX†	11.76		12.24	
Input voltage regulation	V_I = 14 V to 19 V, I_O = 250 mA			15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA			20	78	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			30	120	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		µV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2$ V				200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, T_J = 25°C

PARAMETER	TL751Mxx			UNIT
	MIN	TYP	MAX	
Response time, $\overline{\text{ENABLE}}$ to output		50		µs

electrical characteristics, $V_I = 14$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}}$ at 0 V, $T_J = 25°C$ (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M05Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V,	I_O = 0 mA to 750 mA,		5		V
Input voltage regulation	V_I = 9 V to 16 V,	I_O = 250 mA		10		mV
	V_I = 6 V to 26 V,	I_O = 250 mA		12		
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			20		mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}}$ at 0 V, $T_J = 25°C$ (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M08Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V,	I_O = 0 mA to 750 mA,		8		V
Input voltage regulation	V_I = 10 V to 17 V,	I_O = 250 mA		12		mV
	V_I = 9 V to 26 V,	I_O = 250 mA		15		
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			24		mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14$ V, $I_O = 300$ mA, $\overline{\text{ENABLE}}$ at 0 V, $T_J = 25°C$ (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M10Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V,	I_O = 0 mA to 750 mA,		10		V
Input voltage regulation	V_I = 12 V to 18 V,	I_O = 250 mA		15		mV
	V_I = 11 V to 26 V,	I_O = 250 mA		20		
Ripple rejection	V_I = 13 V to 23 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			30		mV
Output noise voltage	f = 10 Hz to 100 kHz			1000		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

TL751M12Y electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M12Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V,	I_O = 0 mA to 750 mA,		12		V
Input voltage regulation	V_I = 14 V to 19 V,	I_O = 250 mA		15		mV
	V_I = 13 V to 26 V,	I_O = 250 mA		20		
Ripple rejection	V_I = 13 V to 23 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			30		mV
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

PARAMETER MEASUREMENT INFORMATION

The TL751Mxx is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can establish the capacitance value and ESR range for best regulator performance.

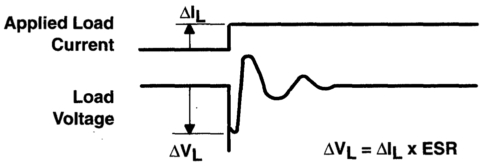
Figure 3 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output. This figure also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 4 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω. This figure establishes the amount that the minimum ESR limit shown in Figure 3 can be adjusted for different capacitor values. For example, if the minimum load needed is 200 mA, Figure 4 suggests an ESR range of 0.8 Ω to 2 Ω for 10 μF. Figure 4 shows that changing the capacitor from 10 μF to 400 μF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω , achieving an expanded ESR range by using a larger capacitor at the output. [For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figures 3 and 4.]

PARAMETER MEASUREMENT INFORMATION

Table 1. Compensations for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 μF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 μF	0.6 Ω	T491D336M010AS	0.5 Ω



OUTPUT CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR) vs LOAD CURRENT RANGE

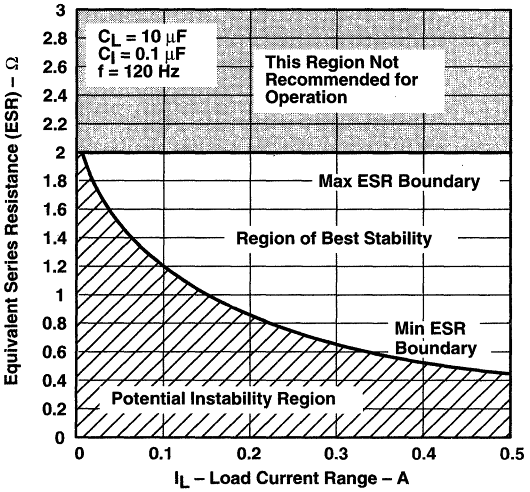


Figure 3

STABILITY vs EQUIVALENT SERIES RESISTANCE (ESR)

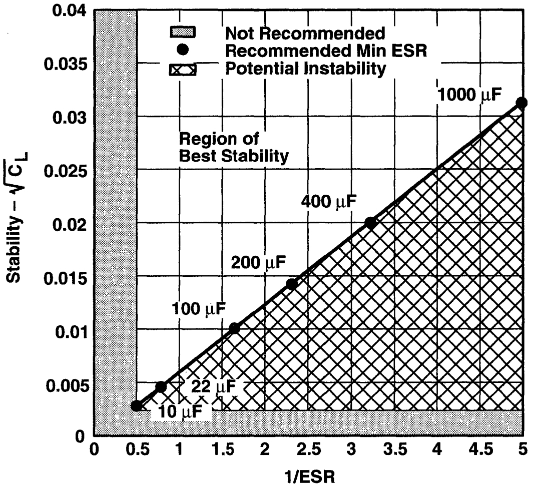


Figure 4

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
Transient input voltage		vs Time	5
Output voltage		vs Input voltage	6
Input current	I_O = 10 mA	vs Input voltage	7
	I_O = 100 mA	vs Input voltage	8
Dropout voltage		vs Output current	9
Quiescent current		vs Output current	10
Load transient response			11
Line transient response			12

TRANSIENT INPUT VOLTAGE
vs
TIME

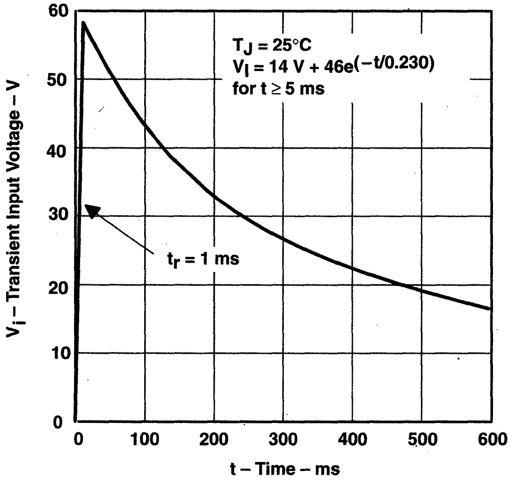


Figure 5

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

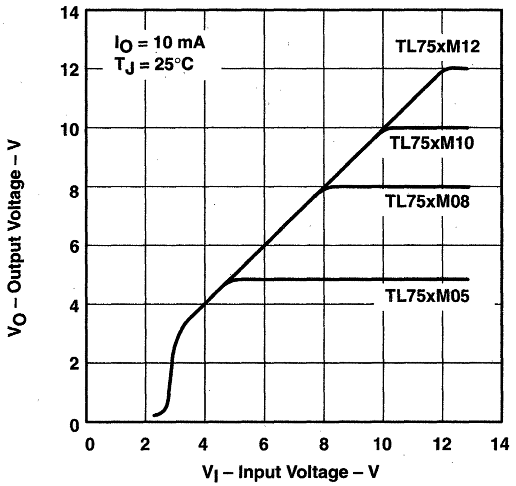


Figure 6

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

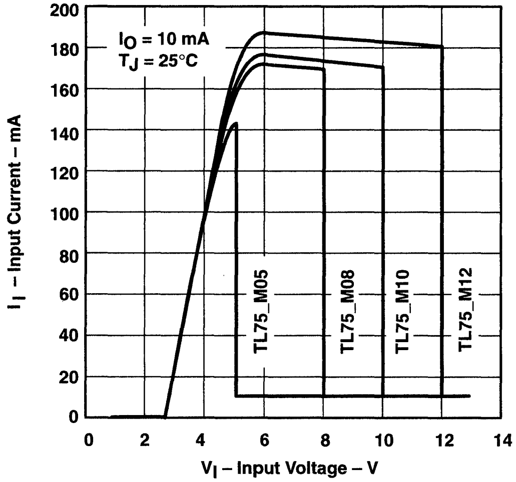


Figure 7

INPUT CURRENT vs INPUT VOLTAGE

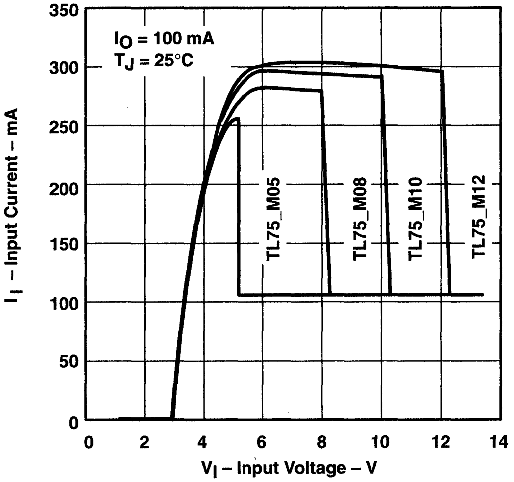


Figure 8

DROPOUT VOLTAGE vs OUTPUT CURRENT

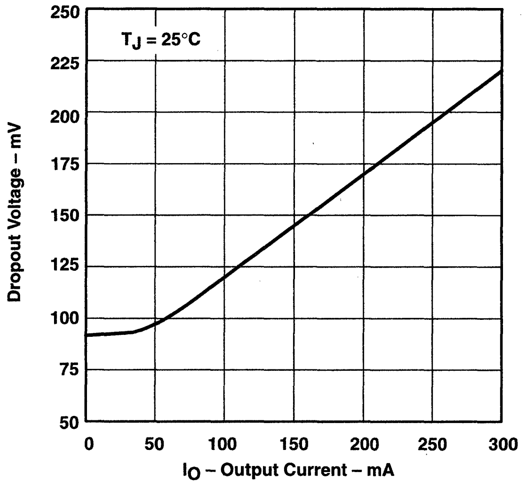


Figure 9

QUIESCENT CURRENT vs OUTPUT CURRENT

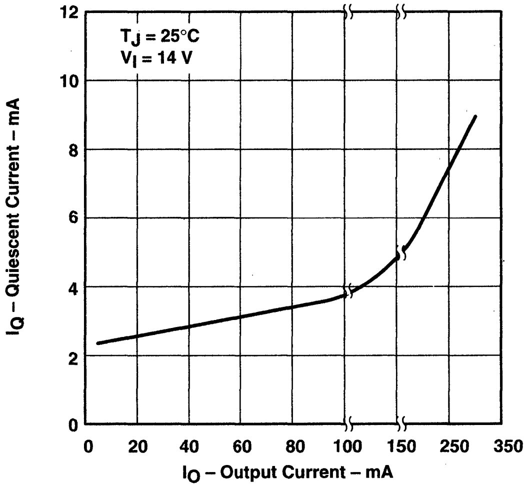


Figure 10

TYPICAL CHARACTERISTICS

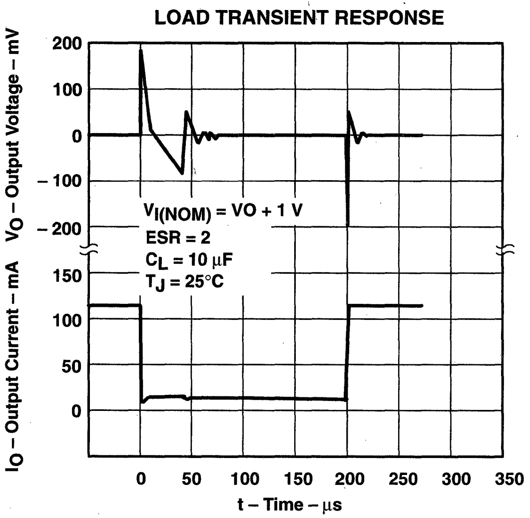


Figure 11

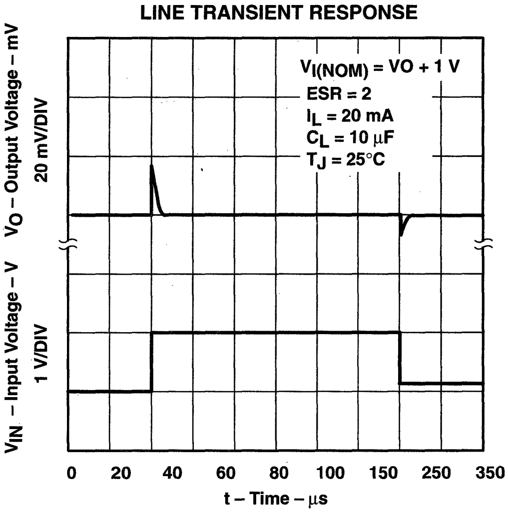


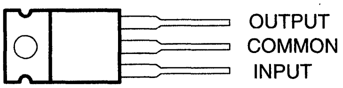
Figure 12

TL780 SERIES
POSITIVE VOLTAGE REGULATORS

SLVS055B – APRIL 1981 – REVISED AUGUST 1995

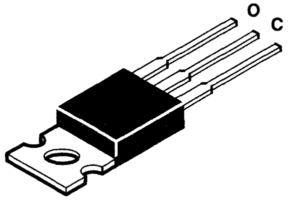
- **±1% Output Tolerance at 25°C**
- **±2% Output Tolerance Over Full Operating Range**
- **Thermal Shutdown**
- **Internal Short-Circuit Current Limiting**
- **Pinout Identical to μA7800 Series**
- **Improved Version of μA7800 Series**

KC PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

TO-200AB



description

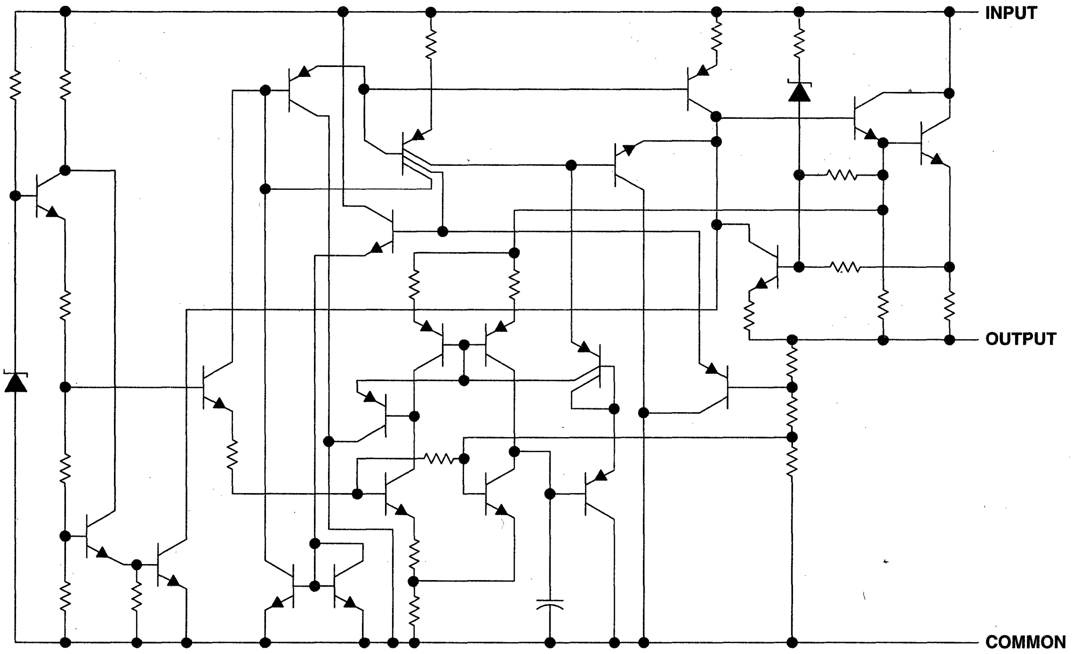
Each fixed-voltage precision regulator in this series is capable of supplying 1.5 A of load current. A unique temperature-compensation technique coupled with an internally trimmed band-gap reference has resulted in improved accuracy when compared to other 3-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current limiting and thermal shutdown features make the devices essentially immune to overload.

AVAILABLE OPTIONS

T_J	V_OTYP (V)	PACKAGED DEVICES	CHIP FORM (Y)
		HEAT-SINK MOUNTED (3-PIN) (KC)	
0°C to 125°C	5	TL78005CKC	TL78005Y
	12	TL78012CKC	TL78012Y
	15	TL78015CKC	TL78015Y

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

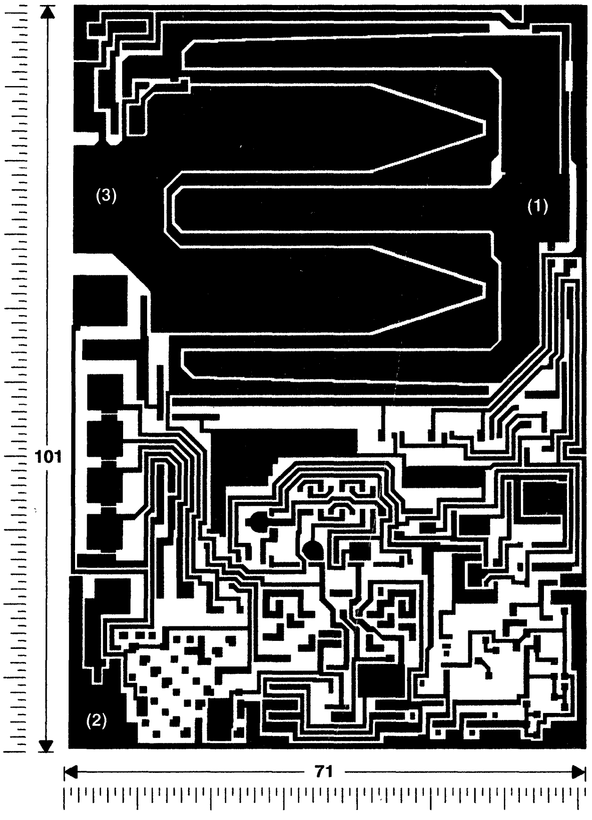
schematic

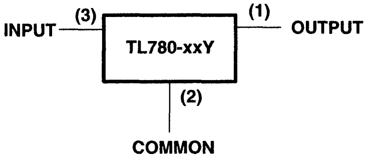


TL780-05Y, TL780-12Y, and TL780-15Y chip information

These chips, when properly assembled, display characteristics similar to the TL780-xxC Series. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input voltage, V_I .... 35 V
Continuous total dissipation at $T_A = 25°C$ (see Note 1) .... 2 W
Continuous total power dissipation at (or below) $T_C = 25°C$ (see Note 1) .... 15 W
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range .... 0°C to 150°C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above $T_A = 25°C$ or $T_C = 25°C$, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

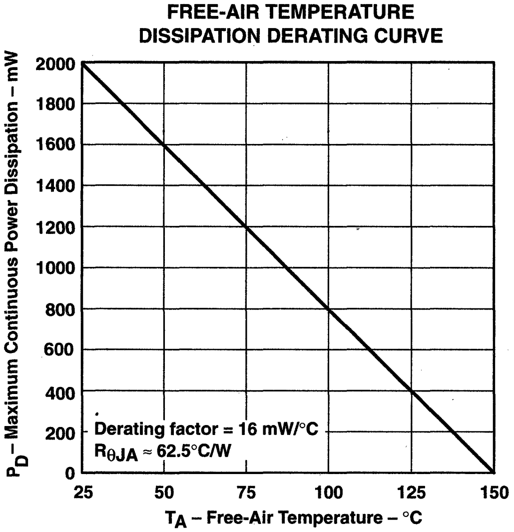


Figure 1

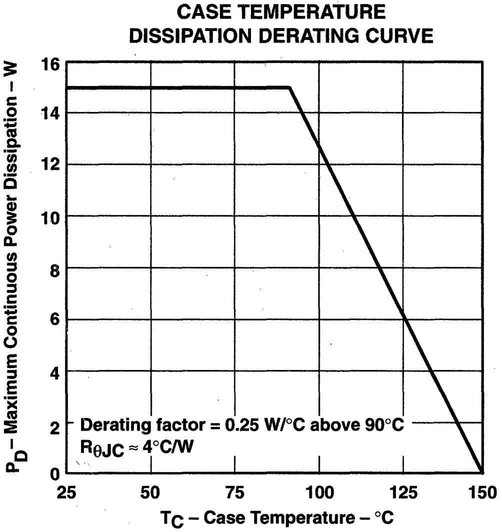


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL780-05C	7	25	V
	TL780-12C	14.5	30	
	TL780-15C	17.5	30	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	TL780-05C MIN	TL780-05C TYP	TL780-05C MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 7 V to 20 V	25°C	4.95	5	5.05	V
		0°C to 125°C	4.9		5.1	
Input voltage regulation	V_I = 7 V to 25 V	25°C		0.5	5	mV
	V_I = 8 V to 12 V			0.5	5	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	70	85		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		4	25	mV
	I_O = 250 mA to 750 mA			1.5	15	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5	8	mA
Input bias current change	V_I = 7 V to 25 V	0°C to 125°C		0.7	1.3	mA
	I_O = 5 mA to 1 A			0.003	0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.22-µF capacitor across the output.

electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	TL780-12C MIN	TL780-12C TYP	TL780-12C MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 14.5 V to 27 V	25°C	11.88	12	12.12	V
		0°C to 125°C	11.76		12.24	
Input voltage regulation	V_I = 14.5 V to 30 V	25°C		1.2	12	mV
	V_I = 16 V to 22 V			1.2	12	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	65	80		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		6.5	60	mV
	I_O = 250 mA to 750 mA			2.5	36	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		180		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5.5	8	mA
Input bias current change	V_I = 14.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.22-µF capacitor across the output.

electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	TL780-15C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 17.5 V to 30 V	25°C	14.85	15	15.15	V
		0°C to 125°C	14.7		15.3	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		1.5	15	mV
	V_I = 20 V to 26 V			1.5	15	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	60	75		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		7	75	mV
	I_O = 250 mA to 750 mA			2.5	45	
Output resistance	f = 1 kHz			0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		225		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5.5	8	mA
Input bias current change	V_I = 17.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.02	0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

electrical characteristics, V_I = 10 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL780-05Y			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,		5		V
Input voltage regulation	V_I = 7 V to 25 V		0.5		mV
	V_I = 8 V to 12 V		0.5		
Output voltage regulation	I_O = 5 mA to 1.5 A		4		mV
	I_O = 250 mA to 750 mA		1.5		
Output noise voltage	f = 10 Hz to 100 kHz		75		μV
Dropout voltage	I_O = 1 A		2		V
Input bias current			5		mA
Short-circuit output current			750		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

electrical characteristics, V_I = 19 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL780-12Y			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,		12		V
Input voltage regulation	V_I = 14.5 V to 30 V		1.2		mV
	V_I = 16 V to 22 V		1.2		
Output voltage regulation	I_O = 5 mA to 1.5 A		6.5		mV
	I_O = 250 mA to 750 mA		2.5		
Output noise voltage	f = 10 Hz to 100 kHz		180		μV
Dropout voltage	I_O = 1 A		2		V
Input bias current			5.5		mA
Short-circuit output current			350		mA
Peak output current			2.2		A

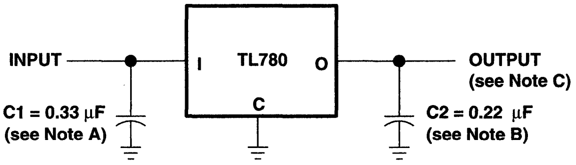
† Pulse-testing techniques the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

electrical characteristics, V_I = 23 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL780-15Y			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,		15		V
Input voltage regulation	V_I = 17.5 V to 30 V		1.5		mV
	V_I = 20 V to 26 V		1.5		
Output voltage regulation	I_O = 5 mA to 1.5 A		7		mV
	I_O = 250 mA to 750 mA		2.5		
Output resistance	f = 1 kHz		0.0035		Ω
Output noise voltage	f = 10 Hz to 100 kHz		225		μV
Dropout voltage	I_O = 1 A		2		V
Input bias current			5.5		mA
Short-circuit output current			230		mA
Peak output current			2.2		A

† Pulse-testing techniques the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C1 is required when the regulator is far from the power supply filter.
B. C2 is not required for stability; however, transient response is improved.
C. Permanent damage can occur when output is pulled below ground.

Figure 3. Test Circuit

APPLICATION INFORMATION

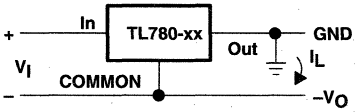
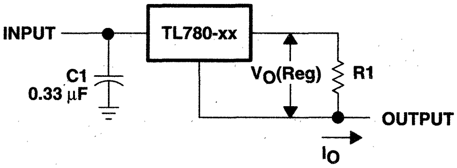


Figure 4. Positive Regulator in Negative Configuration (V_I Must Float)



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 5. Current Regulator

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

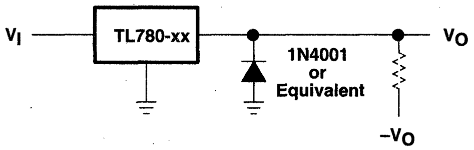


Figure 6. Output Polarity Reversal Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This, for example, could occur when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 7.

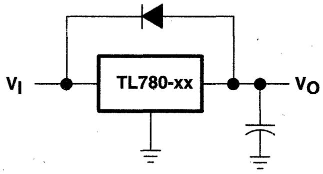


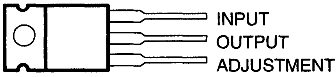
Figure 7. Reverse-Bias Protection Circuit

TL783C, TL783Y
HIGH-VOLTAGE ADJUSTABLE REGULATORS

SLVS036B – SEPTEMBER 1981 – REVISED AUGUST 1995

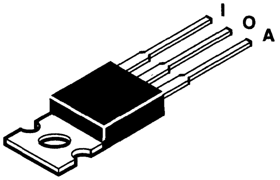
- **Output Adjustable From 1.25 V to 125 V When Used With an External Resistor Divider**
- **700-mA Output Current**
- **Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection**
- **0.001%/V Typical Input Voltage Regulation**
- **0.15% Typical Output Voltage Regulation**
- **76-dB Typical Ripple Rejection**
- **Standard TO-220AB Package**

KC PACKAGE
(TOP VIEW)



The output terminal is in electrical contact with the mounting base.

TO-220AB



description

The TL783C is an adjustable 3-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783C combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs, the TL783C maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if the adjustment terminal is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

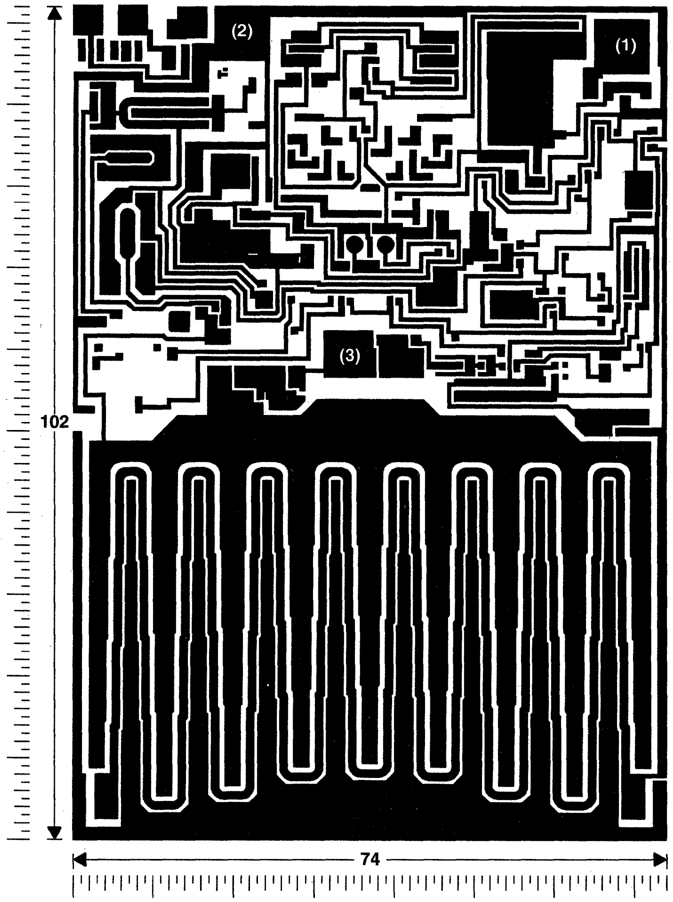
AVAILABLE OPTIONS

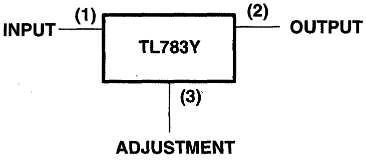
T_J	PACKAGED DEVICE	CHIP FORM (Y)
	HEAT-SINK MOUNTED (3-PIN) (KC)	
0°C to 125°C	TL783CKC	TL783Y

TL783Y chip information

This chip, when properly assembled, displays characteristics similar to the TL783C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

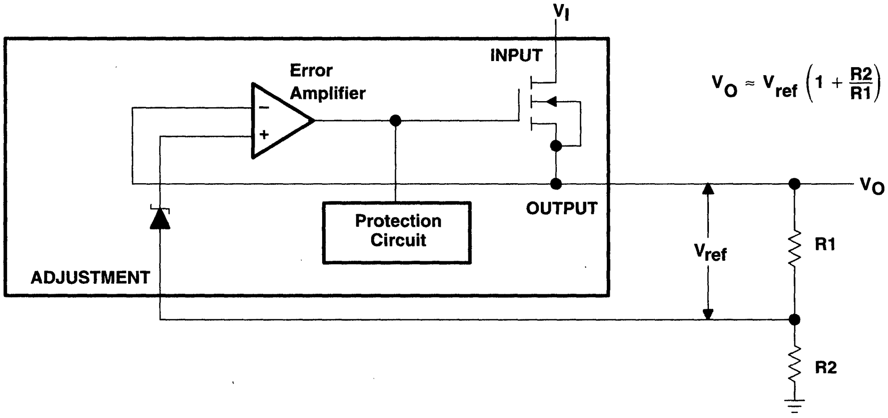
BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$	125 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1)	2 W
Continuous total power dissipation at (or below) T_C = 70°C (see Note 1)	20 W
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range	0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above T_A = 25°C or T_C = 70°C, refer to Figures 1 and 2, respectively. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

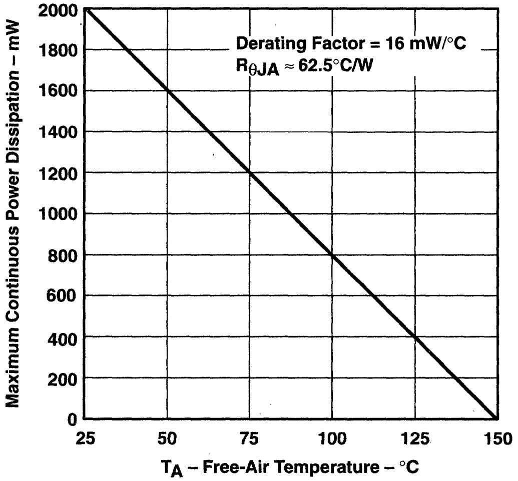


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

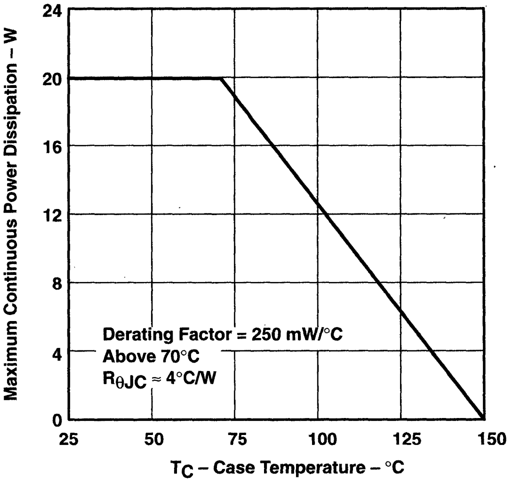


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 0°C$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL783C			UNIT
			MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O = 20$ V to 125 V, P ≤ rated dissipation	$T_J = 25°C$		0.001	0.01	%/V
		$T_J = 0°C$ to 125°C		0.004	0.02	
Ripple rejection	$\Delta V_{I(PP)} = 10$ V, $V_O = 10$ V, f = 120 Hz		66	76		dB
Output voltage regulation	$I_O = 15$ mA to 700 mA, $T_J = 25°C$	$V_O \le 5$ V		7.5	25	mV
		$V_O \ge 5$ V		0.15%	0.5%	
	$I_O = 15$ mA to 700 mA, P ≤ rated dissipation	$V_O \le 5$ V		20	70	mV
		$V_O \ge 5$ V		0.3%	1.5%	
Output voltage change with temperature				0.4%		
Output voltage long-term drift	1000 hours at $T_J = 125°C$, $V_I - V_O = 125$ V, See Note 2			0.2%		
Output noise voltage	f = 10 Hz to 10 kHz, $T_J = 25°C$			0.003%		
Minimum output current to maintain regulation	$V_I - V_O = 125$ V				15	mA
Peak output current	$V_I - V_O = 25$ V, t = 1 ms			1100		mA
	$V_I - V_O = 15$ V, t = 30 ms			715		
	$V_I - V_O = 25$ V, t = 30 ms		700	900		
	$V_I - V_O = 125$ V, t = 30 ms		100	250		
Adjustment-terminal current				83	110	µA
Change in adjustment-terminal current	$V_I - V_O = 15$ V to 125 V, $I_O = 15$ mA to 700 mA, P ≤ rated dissipation			0.5	5	µA
Reference voltage (OUTPUT to ADJUSTMENT)	$V_I - V_O = 10$ V to 125 V, $I_O = 15$ mA to 700 mA, P ≤ rated dissipation, See Note 3		1.2	1.27	1.3	V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTES: 2. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

3. Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL783Y			UNIT
			MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O = 20$ V to 125 V, $P \le$ rated dissipation			0.001		%/V
Ripple rejection	$\Delta V_{I(PP)} = 10$ V, $V_O = 10$ V, f = 120 Hz			76		dB
Output voltage regulation	$I_O = 15$ mA to 700 mA	$V_O \le 5$ V		7.5		mV
		$V_O \ge 5$ V		0.15%		
	$I_O = 15$ mA to 700 mA, $P \le$ rated dissipation	$V_O \le 5$ V		20		mV
		$V_O \ge 5$ V		0.3%		
Output voltage change with temperature				0.4%		
Output noise voltage	f = 10 Hz to 10 kHz			0.003%		
Peak output current	$V_I - V_O = 25$ V, t = 1 ms			1100		mA
	$V_I - V_O = 15$ V, t = 30 ms			715		
	$V_I - V_O = 25$ V, t = 30 ms			900		
	$V_I - V_O = 125$ V, t = 30 ms			250		
Adjustment-terminal current				83		µA
Change in adjustment-terminal current	$V_I - V_O = 15$ V to 125 V, $I_O = 15$ mA to 700 mA, $P \le$ rated dissipation			0.5		µA
Reference voltage (OUTPUT to ADJUSTMENT)	$V_I - V_O = 10$ V to 125 V, $I_O = 15$ mA to 700 mA, $P \le$ rated dissipation, See Note 3			1.27		V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTES: 2 Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

3 Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

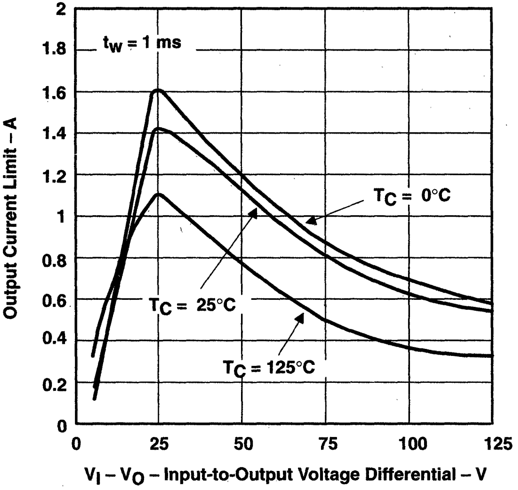


Figure 3

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

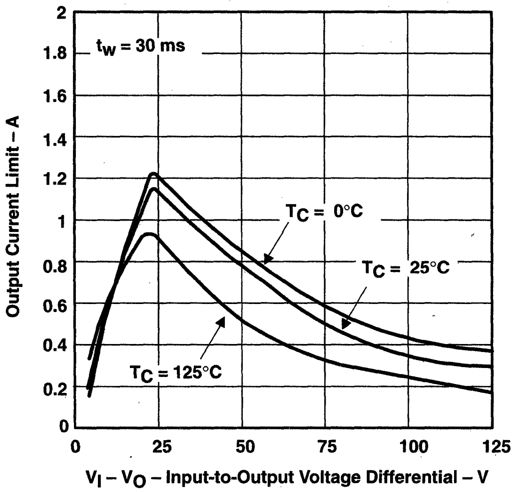


Figure 4

OUTPUT CURRENT LIMIT
vs
TIME

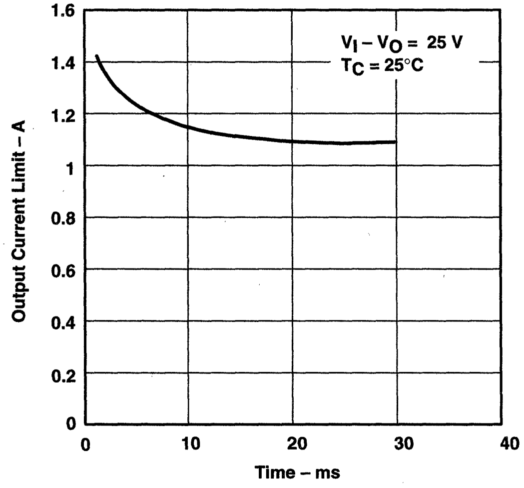


Figure 5

RIPPLE REJECTION
vs
OUTPUT VOLTAGE

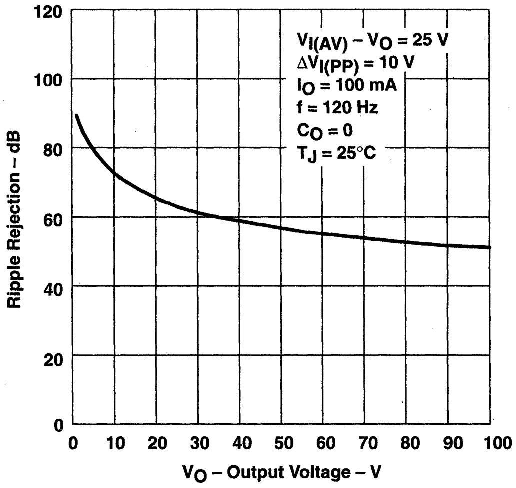


Figure 6

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
OUTPUT CURRENT

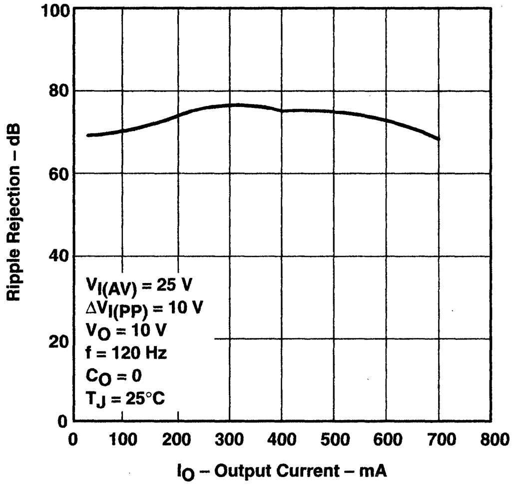


Figure 7

RIPPLE REJECTION
vs
FREQUENCY

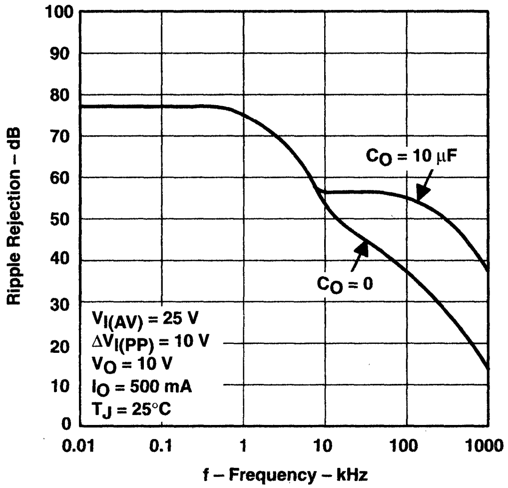


Figure 8

OUTPUT IMPEDANCE
vs
FREQUENCY

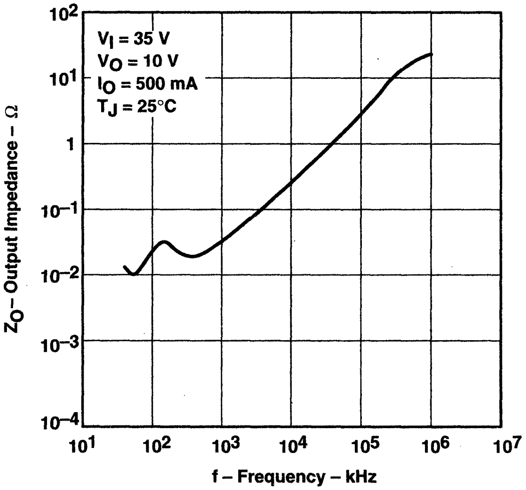


Figure 9

REFERENCE VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

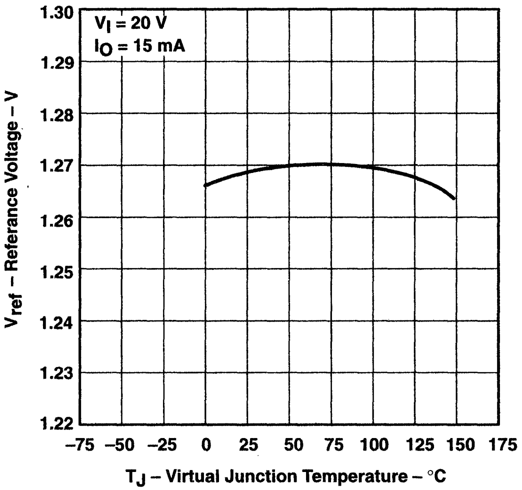


Figure 10

TYPICAL CHARACTERISTICS

ADJUSTMENT-TERMINAL CURRENT vs VIRTUAL JUNCTION TEMPERATURE

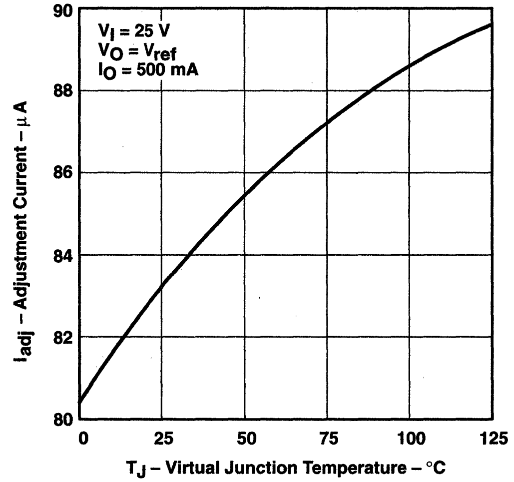


Figure 11

DROPOUT VOLTAGE vs VIRTUAL JUNCTION TEMPERATURE

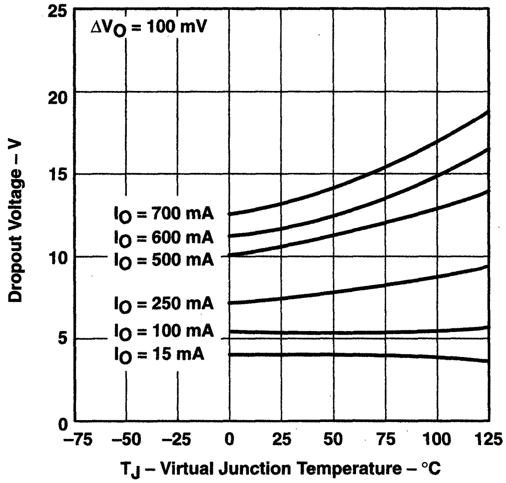


Figure 12

OUTPUT VOLTAGE DEVIATION vs VIRTUAL JUNCTION TEMPERATURE

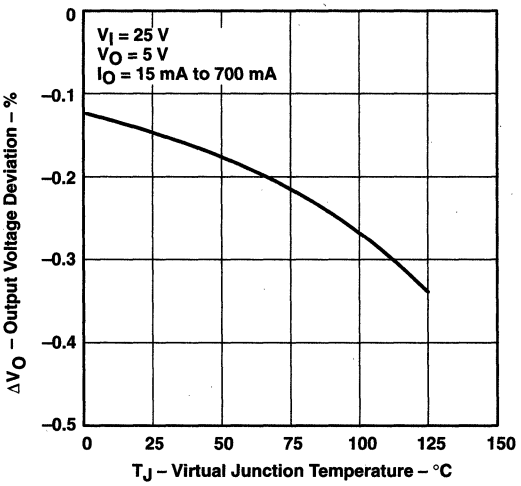
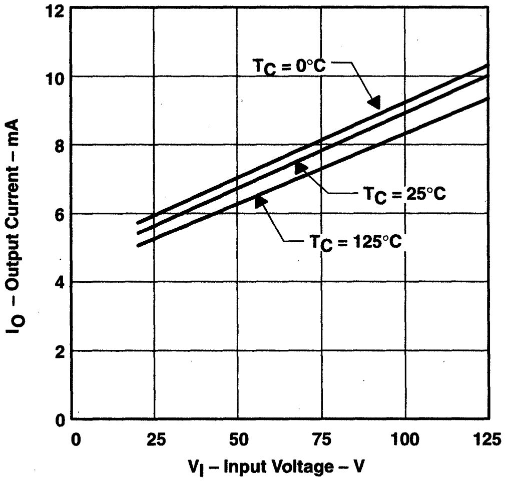


Figure 13

OUTPUT CURRENT† vs INPUT VOLTAGE



† This is the minimum current required to maintain voltage regulation.

Figure 14

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

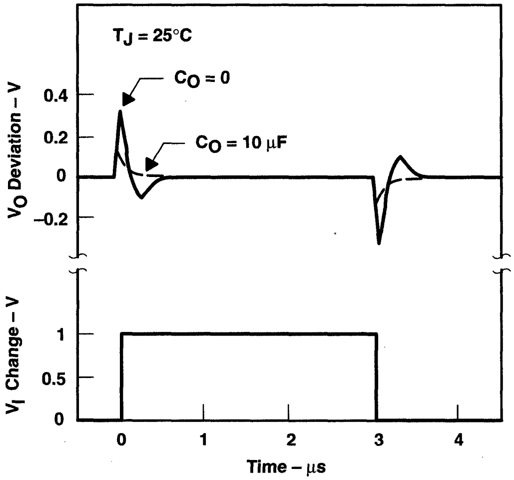


Figure 15

LOAD TRANSIENT RESPONSE

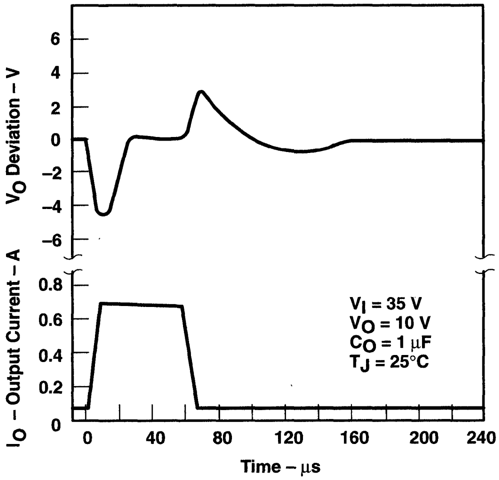


Figure 16

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) generates 1.25 V nominal (V_{ref}) between the output and adjustment terminals. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R2/R1) + I_{adj} (R2)$$

or

$$V_O \sim V_{ref} (1 + R2/R1).$$

The TL783C was designed to minimize I_{adj} and maintain consistency over line and load variations, thereby minimizing the I_{adj} (R2) error term.

To maintain I_{adj} at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω provides a minimum load current of 15 mA. Larger values can be used when the input-to-output differential voltage is less than 125 V (see output current curve) or when the load sinks some portion of the minimum current.

bypass capacitors

The TL783C regulator is stable without bypass capacitors; however, any regulator becomes unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-µF tantalum or aluminum electrolytic capacitor is usually sufficient.

DESIGN CONSIDERATIONS

bypass capacitors (continued)

Adjustment-terminal capacitors are not recommended for use on the TL783C because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large load transient conditions. The addition of an output bypass capacitor greatly enhances load transient response as well as prevent dropout. For most applications, it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_O\ (\mu F) = 15/V_O$$

Larger values provide proportionally better transient response characteristics.

protection circuitry

The TL783C regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits are meant to protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783C protect the device up to maximum-rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, when rise times in excess of 10 V/ns are applied to the input, a parasitic npn transistor in parallel with the DMOS output can be turned on causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as tantalum or aluminum electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater usually provides adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, when an instantaneous short circuit is applied to the outputs, both ringing and excessive fall times can result. A tantalum or aluminum electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I. A protective diode (see Figure 17) is required only for capacitance values greater than:

$$C_O\ (\mu F) = 3 \times 10^4/(V_O)^2.$$

Care should always be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

DESIGN CONSIDERATIONS

protection circuitry (continued)

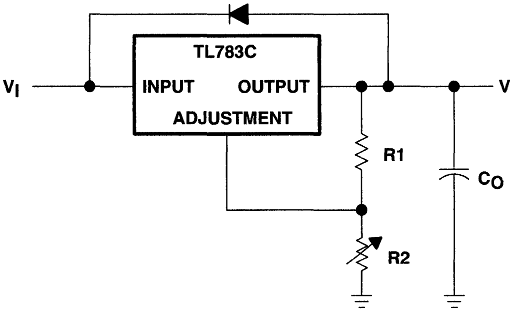


Figure 17. Regulator With Protective Diode

load regulation

The current set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R1 and R2 to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

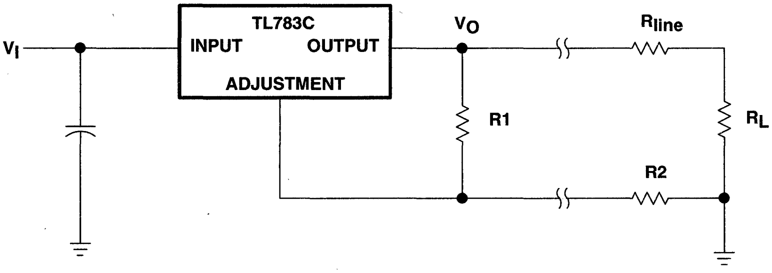
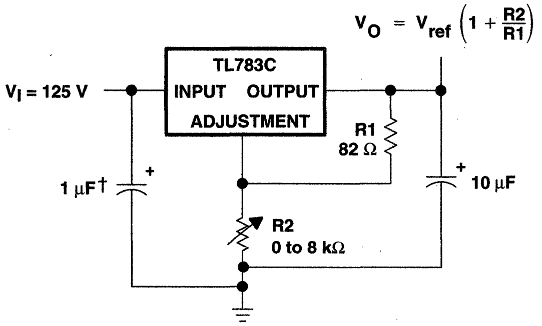


Figure 18. Regulator With Current-Set Resistor

APPLICATION INFORMATION



† Needed if device is more than 4 inches from filter capacitor

Figure 19. 1.25-V to 115-V Adjustable Regulator

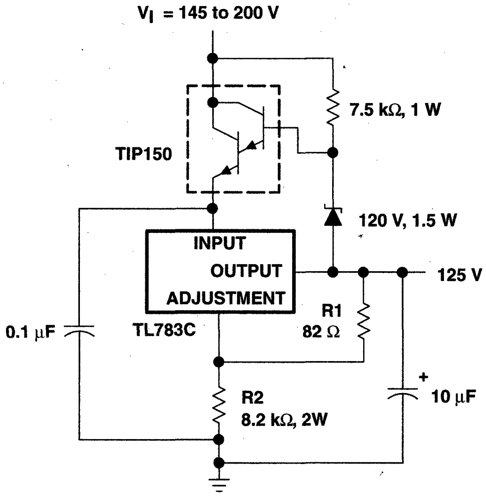


Figure 20. 125-V Short-Circuit-Protected Off-Line Regulator

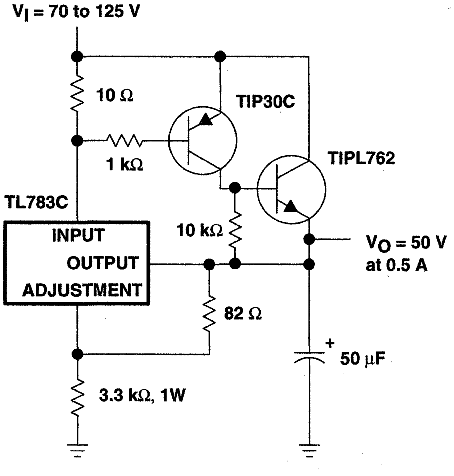


Figure 21. 50-V Regulator With Current Boost

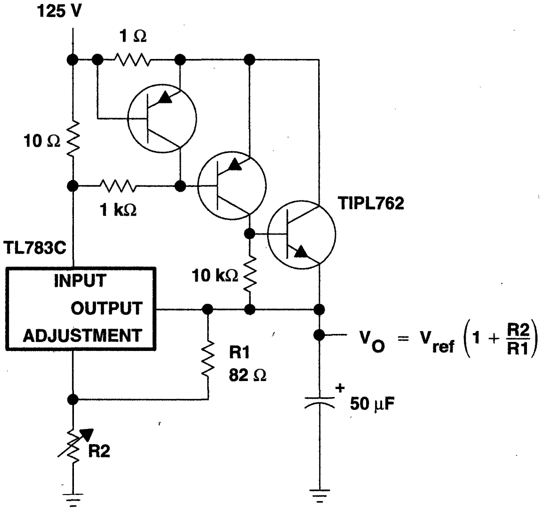


Figure 22. Adjustable Regulator With Current Boost and Current Limit

APPLICATION INFORMATION

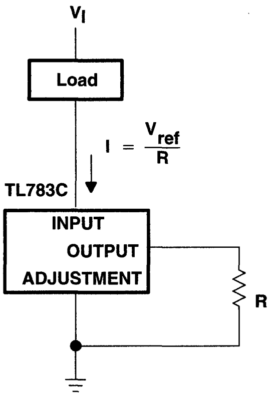


Figure 23. Current-Sinking Regulator

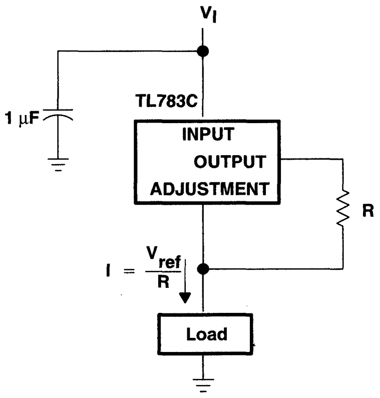


Figure 24. Current-Sourcing Regulator

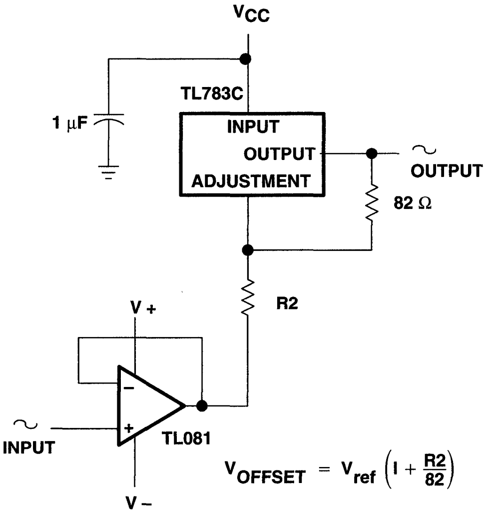


Figure 25. High-Voltage Unity-Gain Offset Amplifier

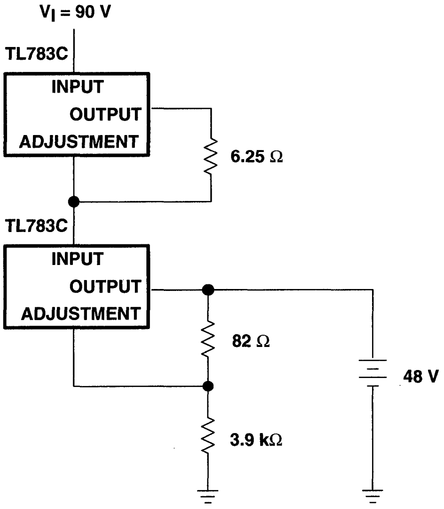


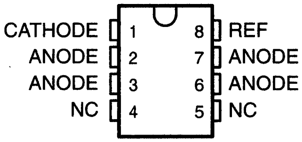
Figure 26. 48-V, 200-mA Float Charger

TL1431C, TL1431Q, TL1431Y
PRECISION PROGRAMMABLE REFERENCES

SLVS062B – DECEMBER 1991 – REVISED AUGUST 1995

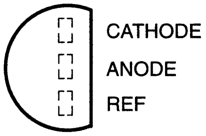
- **0.4% Initial Voltage Tolerance**
- **0.1-Ω Typical Output Impedance**
- **Fast Turn On . . . 500 ns**
- **Sink Current Capability . . . 1 mA to 100 mA**
- **Low REF Current**
- **Adjustable Output Voltage . . . V_{ref} to 36 V**
- **Available In Two High-Density Packaging Options:**
  - **Small Outline (D)**
  - **TO-226AA (LP)**

D PACKAGE
(TOP VIEW)



NC – No internal connection
ANODE terminals are internally connected.

LP PACKAGE
(TOP VIEW)



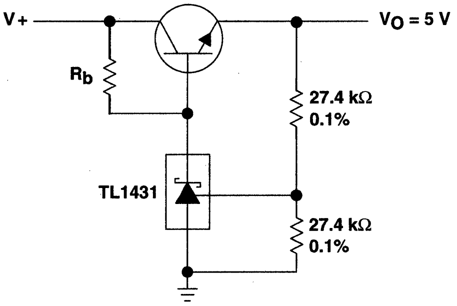
description

The TL1431 is a precision programmable reference with specified thermal stability over applicable automotive and commercial temperature ranges. The output voltage may be set to any value between $V_{I(ref)}$ (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.1 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes and other types of references in applications such as on-board regulation, adjustable power supplies, and switching power supplies.

The TL1431 is offered in a wide variety of high-density packaging options. It is also available in both the automotive temperature range and the commercial temperature range. The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TL1431Q is characterized for operation over the automotive temperature range of −40°C to 125°C.

application schematic

5-V Precision Regulator



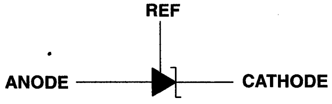
NOTE A: R_b should provide cathode current ≥ 1-mA to the TL1431.

AVAILABLE OPTIONS

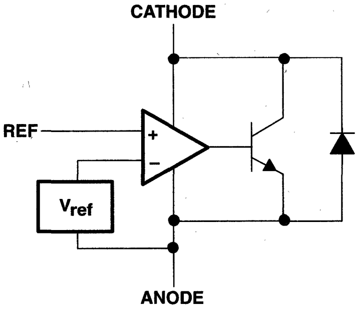
PACKAGED DEVICES			CHIP FORM (Y)
T_A	SMALL OUTLINE (D)	TO-226AA (LP)	
0°C to 70°C	TL1431CD	TL1431CLP	TL1431Y
−40°C to 125°C	TL1431QD	TL1431QLP	

The D and LP packages are available taped and reeled. Add R suffix to device type (e.g., TL1431CDR). Chip forms are tested at 25°C.

symbol



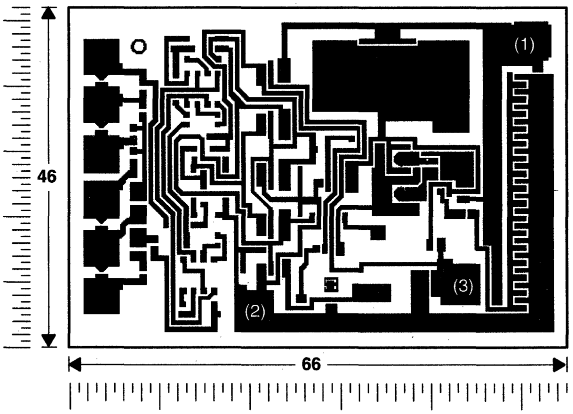
functional block diagram

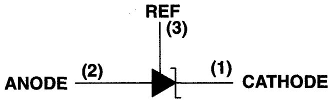


TL1431Y chip information

This chip, when properly assembled, displays characteristics similar to the TL1431. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

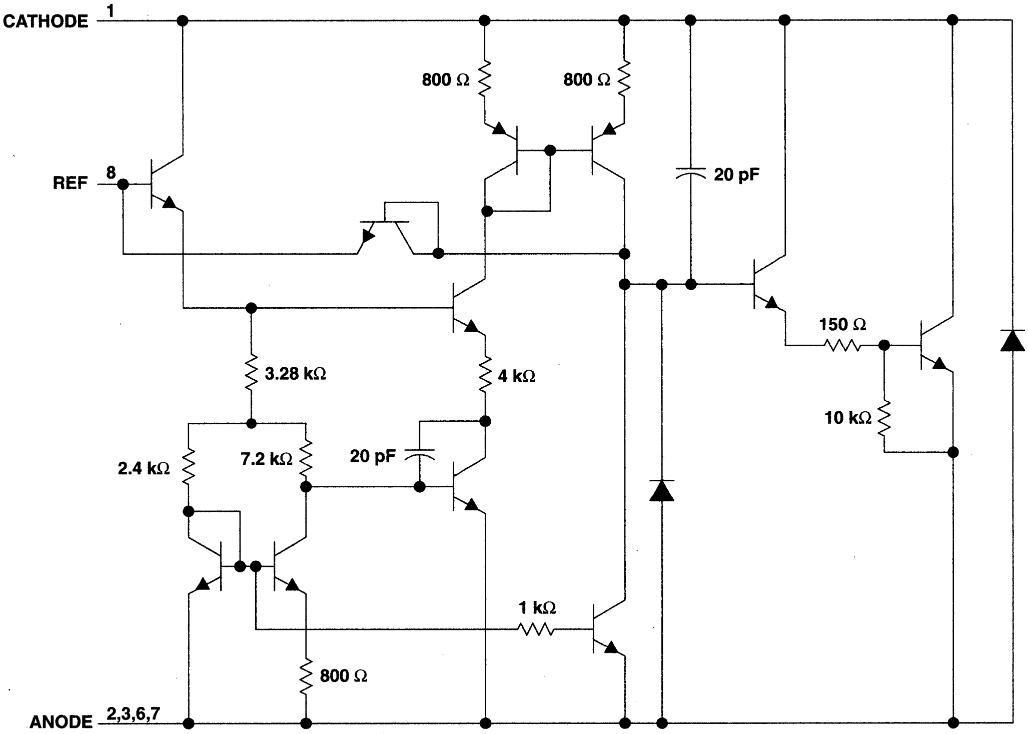
BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic



NOTE A: All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

cathode voltage, V_{KA} (see Note 1)		37 V
Continuous cathode current range, I_{KA}		−100 mA to 150 mA
Reference input current range, $I_{I(REF)}$		−50 μA to 10 mA
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A:	C suffix	0°C to 70°C
	Q suffix	−40°C to 125°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ANODE unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
LP	775 mW	6.2 mW/°C	496 mW	279 mW	155 mW

recommended operating conditions

	C SUFFIX		Q SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
cathode voltage, V_{KA}	$V_{I(ref)}$	36	$V_{I(ref)}$	36	V
cathode current, I_{KA}	1	100	1	100	mA
Operating free-air temperature, T_A	0	70	−40	125	°C

electrical characteristics at specified free-air temperature, I_{KA} = 10 mA (unless otherwise noted)

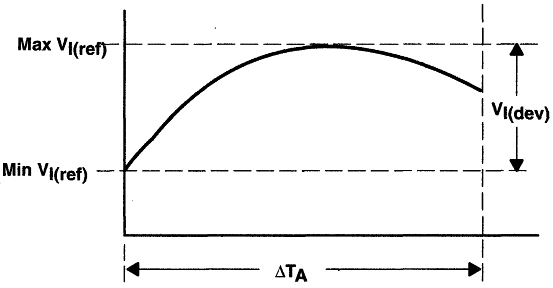
PARAMETER		TEST CONDITIONS	T_A†	TEST CIRCUIT	TL1431C			TL1431Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$	25°C	1	2490	2500	2510	2490	2500	2510	mV
			Full range		2480		2520	2470		2530	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range‡	$V_{KA} = V_{I(ref)}$	Full range	1		4	20		17	55	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	Full range	2		−1.1	−2		−1.1	−2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞	25°C	2		1.5	2.5		1.5	2.5	µA
			Full range				3			3	
$I_{I(dev)}$	Deviation of reference input current over full temperature range‡	R1 = 10 kΩ, R2 = ∞	Full range	2		0.2	1.2		0.5	1.2	µA
	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$ to 36 V	25°C	1		0.45	1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0	25°C	3		0.18	0.5		0.18	0.5	µA
			Full range				2			2	
$\lvert z_{KA} \rvert$	Output impedance§	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA	25°C	1		0.1	0.2		0.1	0.2	Ω

† Full range is 0°C to 70°C for C-suffix devices and −40°C to 125°C for Q-suffix devices.

‡ The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\dfrac{V_{I(dev)}}{V_{I(ref)} \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

§ The output impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$.

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$\lvert z' \rvert = \frac{\Delta V}{\Delta I}$, which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

electrical characteristics at I_{KA} = 10 mA, T_A = 25°C

PARAMETER		TEST CONDITIONS	TEST CIRCUIT	TL1431Y			UNIT
				MIN	TYP	MAX	
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$	1	2490	2500	2510	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	2		−1.1	−2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞	2		1.44	2.5	µA
I_{KAmin}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$ to 36 V	1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, V_{ref} = 0	3		0.18	0.5	µA
$\lvert z_{KA}\rvert$	Output impedance†	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA	1		0.1	0.2	Ω

† The output impedance is defined as: $|z'| = \frac{\Delta V}{\Delta I}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by

$|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$, which is approximately equal to $|z_{KA}| \left(1 + \frac{R1}{R2}\right)$.

PARAMETER MEASUREMENT INFORMATION

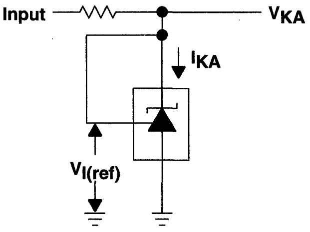


Figure 1. Test Circuit for $V_{(KA)} = V_{ref}$

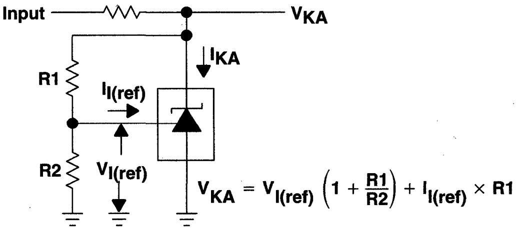


Figure 2. Test Circuit for $V_{(KA)} > V_{ref}$

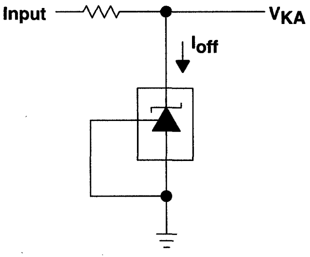


Figure 3. Test Circuit for I_{off}

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{I(ref)}$	Reference voltage	vs Free-air temperature	4
$I_{I(ref)}$	Reference current	vs Free-air temperature	5
I_{KA}	Cathode current	vs Cathode voltage	6, 7
$I_{KA(off)}$	Off-state cathode current	vs Free-air temperature	8
$\Delta V_{I(ref)}$	Ratio of delta reference voltage to delta cathode voltage	vs Free-air temperature	9
V_n	Equivalent input noise voltage	vs Frequency	10
		Over a 10-second time period	11
A_V	Small-signal voltage amplification	vs Frequency	12
$\lvert z_{KA} \rvert$	Reference impedance	vs Frequency	13
	Pulse response		14
	Stability boundary conditions		15

TYPICAL CHARACTERISTICS†

REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

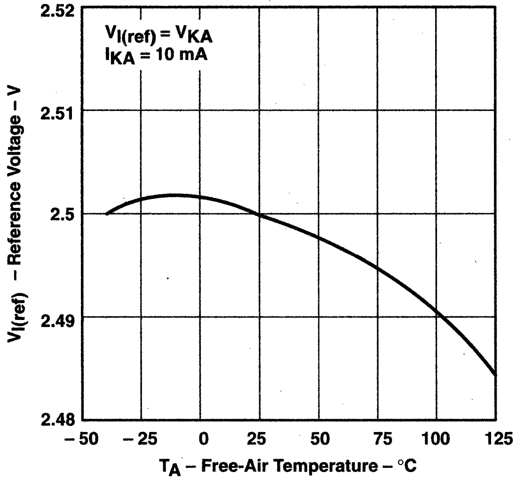


Figure 4

REFERENCE CURRENT vs FREE-AIR TEMPERATURE

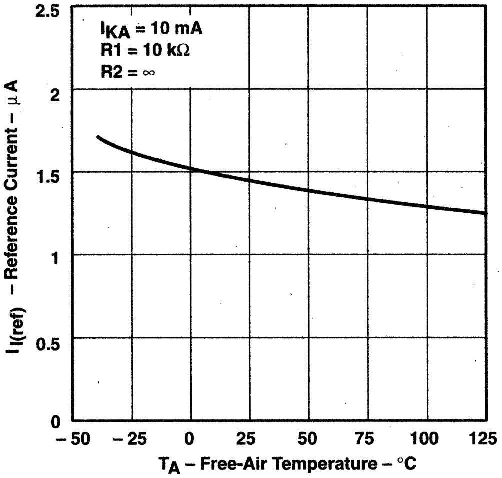


Figure 5

CATHODE CURRENT vs CATHODE VOLTAGE

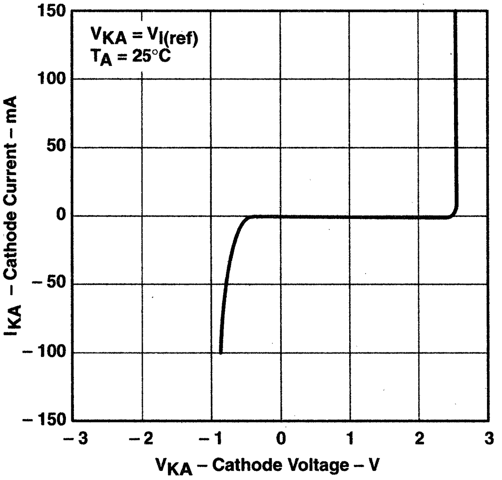


Figure 6

CATHODE CURRENT vs CATHODE VOLTAGE

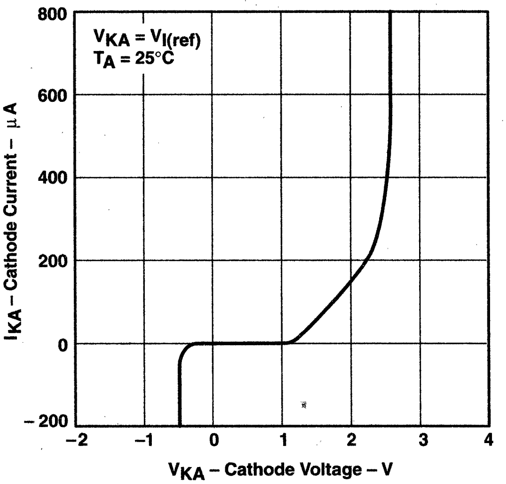


Figure 7

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OFF-STATE CATHODE CURRENT vs FREE-AIR TEMPERATURE

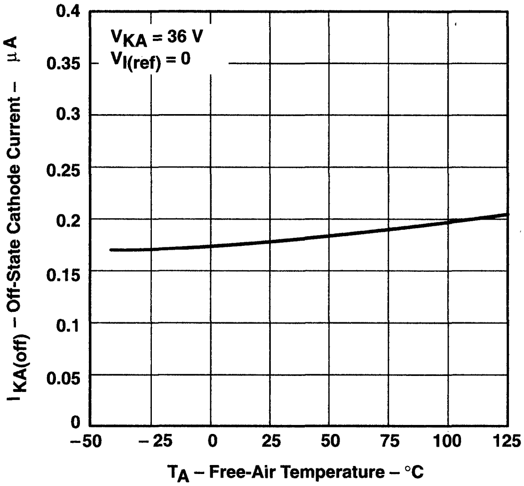


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE TO DELTA CATHODE VOLTAGE vs FREE-AIR TEMPERATURE

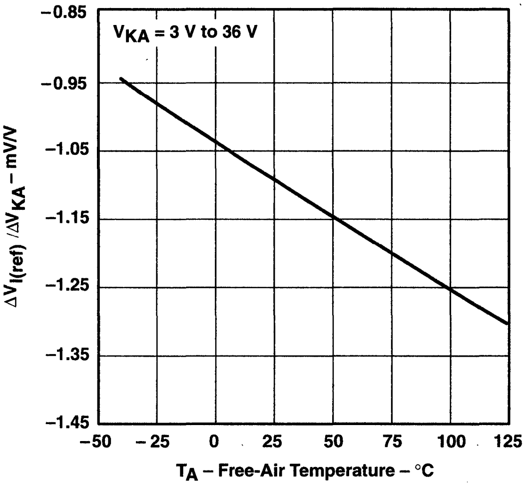


Figure 9

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

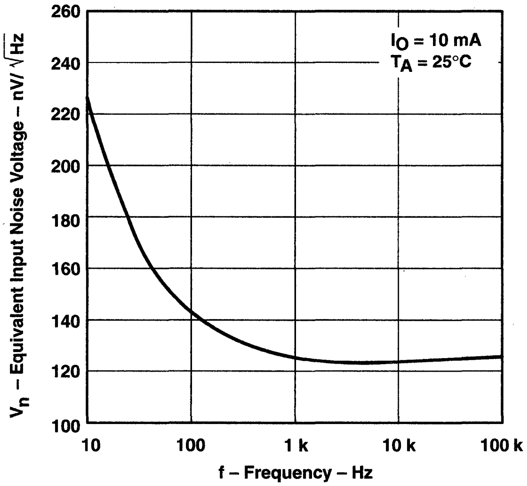


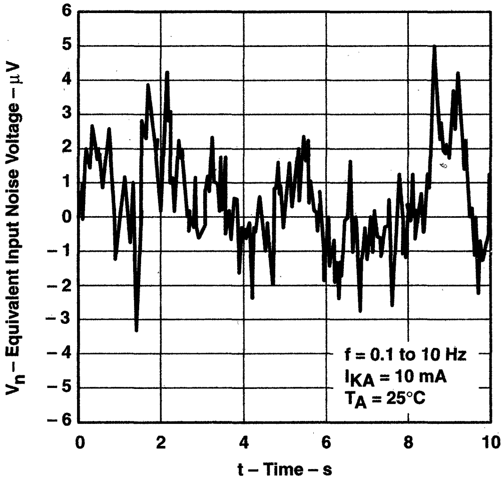
Figure 10

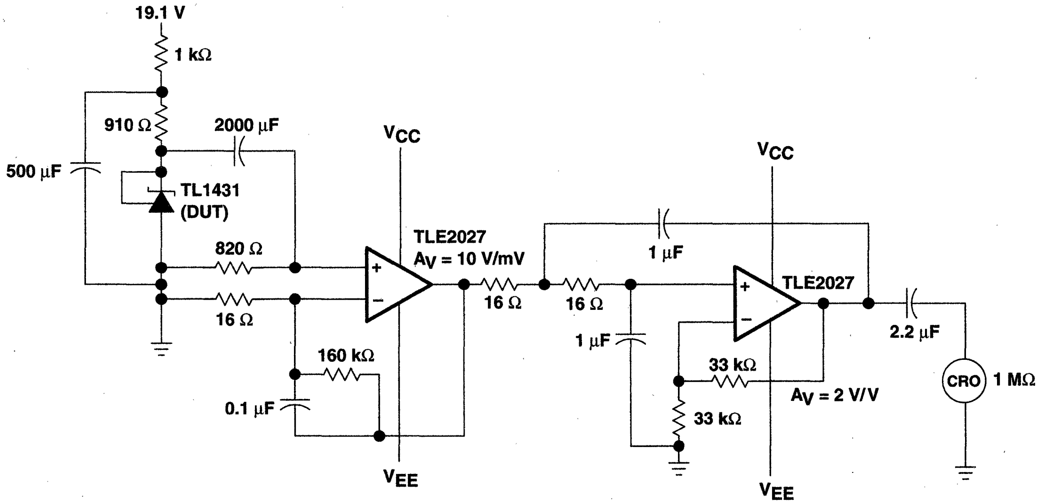
---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD



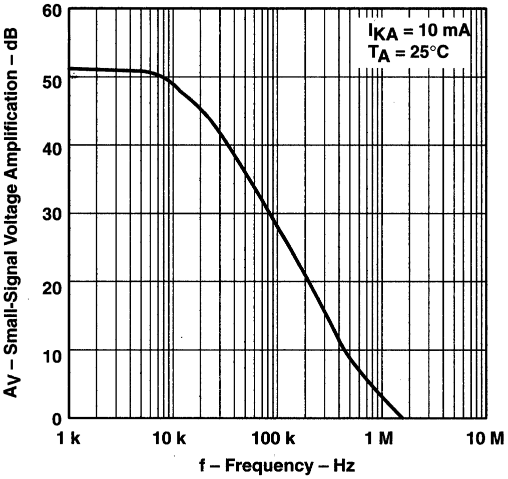


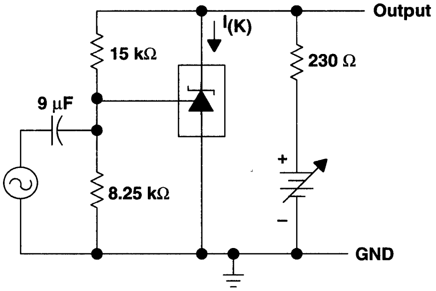
TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT INPUT NOISE VOLTAGE

Figure 11

TYPICAL CHARACTERISTICS

SMALL-SIGNAL VOLTAGE AMPLIFICATION vs FREQUENCY

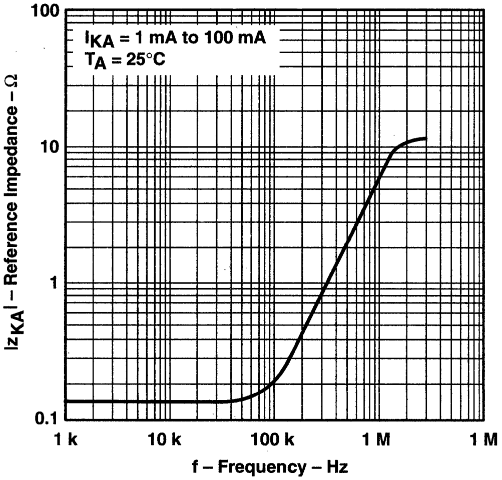


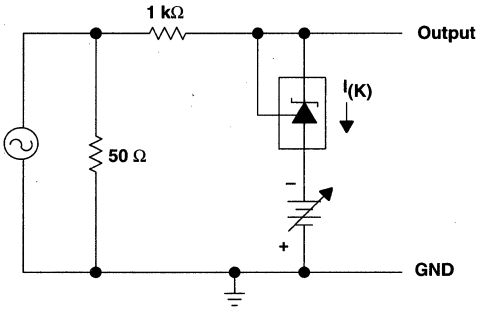


TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

Figure 12

REFERENCE IMPEDANCE vs FREQUENCY



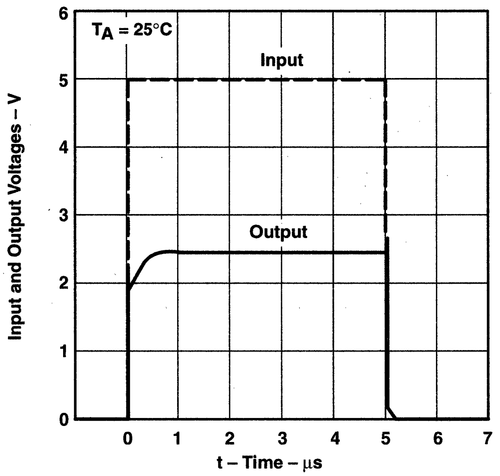


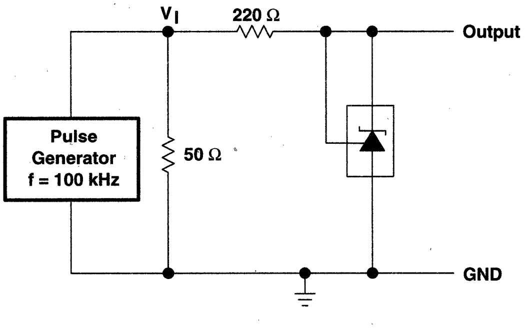
TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 13

TYPICAL CHARACTERISTICS

PULSE RESPONSE

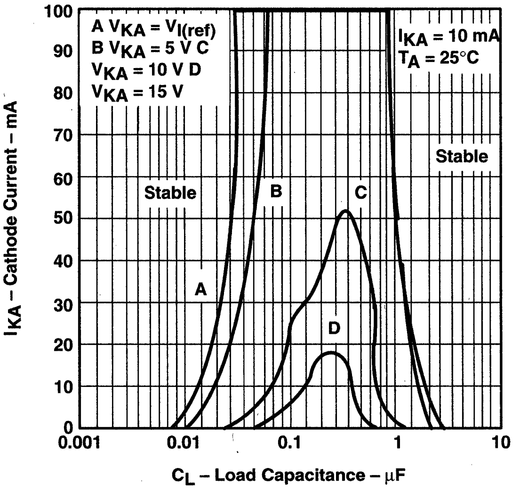




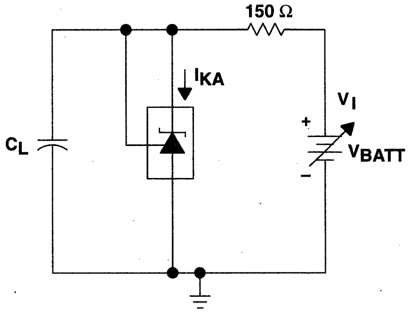
TEST CIRCUIT FOR PULSE RESPONSE

Figure 14

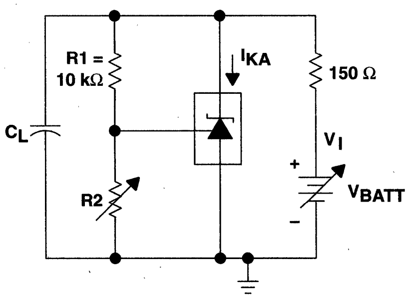
STABILITY BOUNDARY CONDITIONS†



† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions with $C_L = 0$. V_{BATT} and C_L are then adjusted to determine the ranges of stability.



TEST CIRCUIT FOR CURVE A



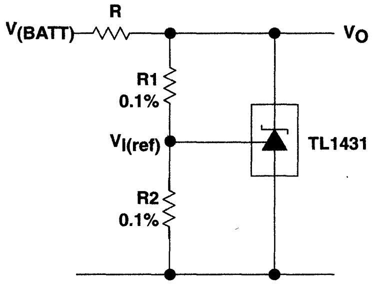
TEST CIRCUIT FOR CURVES B, C, AND D

Figure 15

APPLICATION INFORMATION

Table of Application Circuits

APPLICATION	FIGURE
Shunt regulator	16
Single-supply comparator with temperature-compensated threshold	17
Precision high-current series regulator	18
Output control of a 3-terminal fixed regulator	19
Higher-current shunt regulator	20
Crowbar	21
Precision 5-V, 1.5-A, 0.5% regulator	22
Efficient 5-V precision regulator	23
PWM down converter with 0.5% reference	24
Voltage monitor	25
Delay timer	26
Precision current limiter	27
Precision constant-current sink	28



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{I(ref)}$$

NOTE A: R should provide cathode current ≥ 1-mA to the TL1431 at minimum $V_{(BATT.)}$

Figure 16. Shunt Regulator

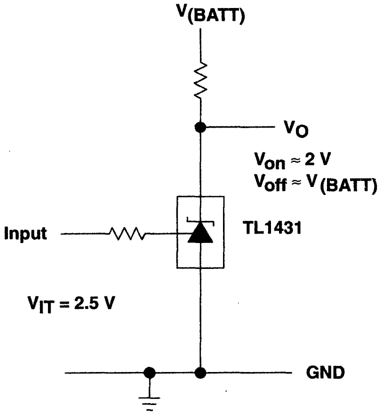
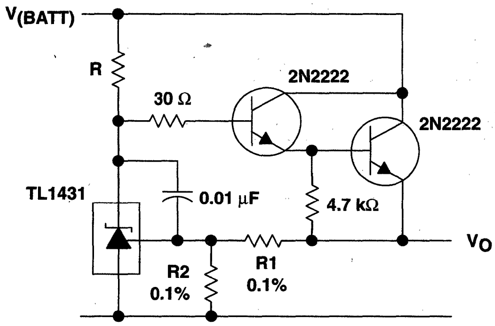


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold

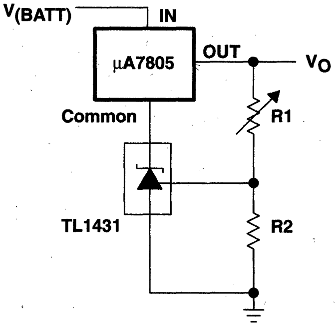
APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{I(ref)}$$

NOTE A: R should provide cathode current ≥ 1-mA to the TL1431 at minimum $V_{(BATT)}$.

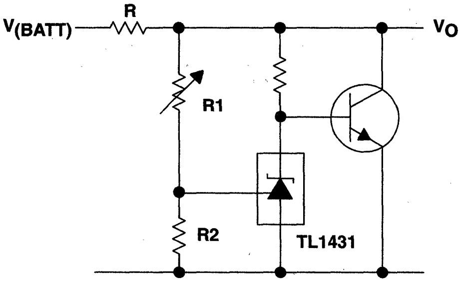
Figure 18. Precision High-Current Series Regulator



$$V = \left(1 + \frac{R1}{R2}\right)V_{I(ref)}$$

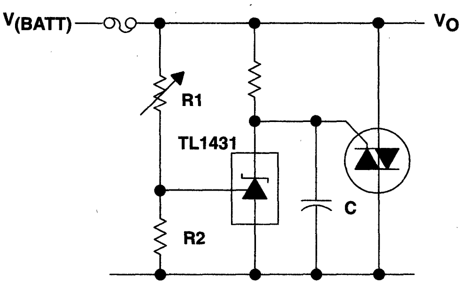
Min V = $V_{I(ref)}$ + 5 V

Figure 19. Output Control of a 3-Terminal Fixed Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{I(ref)}$$

Figure 20. Higher-Current Shunt Regulator



$$V_{trip} = \left(1 + \frac{R1}{R2}\right)V_{I(ref)}$$

NOTE A: Refer to the stability boundary conditions on Figure 15 to determine allowable values for the capacitor.

Figure 21. Crowbar

APPLICATION INFORMATION

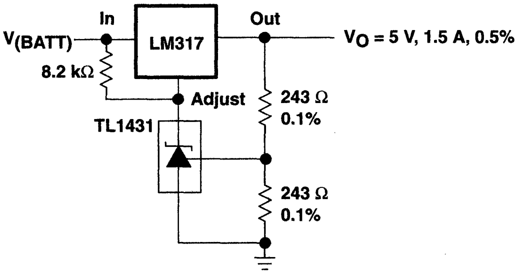
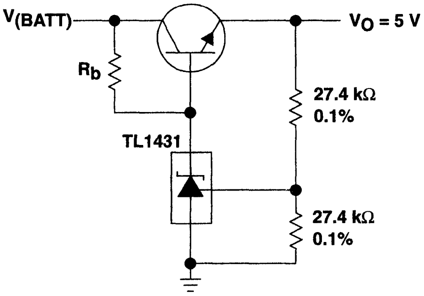


Figure 22. Precision 5-V, 1.5-A, 0.5% Regulator



NOTE A: R_b should provide cathode current ≥ 1-mA to the TL1431.

Figure 23. 5-V Precision Regulator

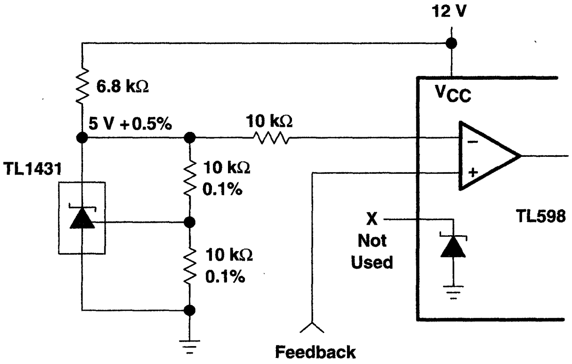
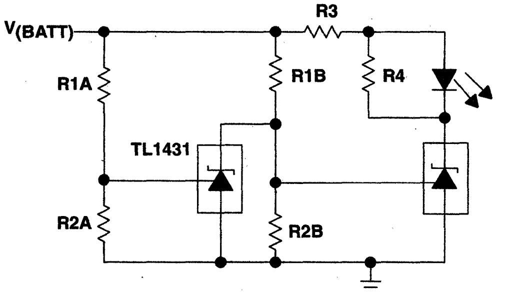


Figure 24. PWM Converter With 0.5% Reference

APPLICATION INFORMATION



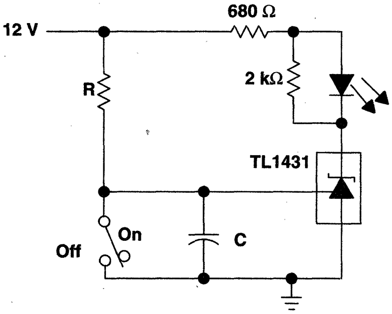
$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right)V_{I(ref)}$$

$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right)V_{I(ref)}$$

LED on When
Low Limit < $V_{(BATT)}$ < High Limit

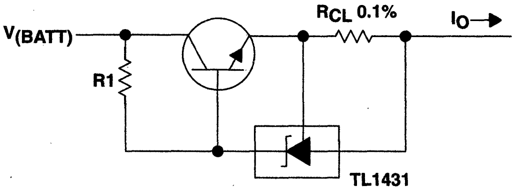
NOTE A: R3 & R4 are selected to provide the desired LED intensity and cathode current ≥ 1 mA to the TL1431.

Figure 25. Voltage Monitor



$$\text{Delay} = R \times C \times \mathrm{I_I}\frac{12\ V}{(12\ V) - V_{I(ref)}}$$

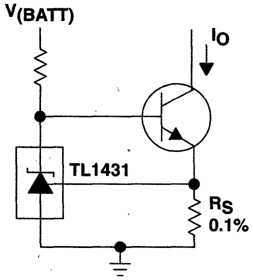
Figure 26. Delay Timer



$$I_O = \frac{V_{I(ref)}}{R_{CL}} + I_{KA}$$

$$R1 = \frac{V_{(BATT)}}{\left(\frac{I_O}{h_{FE}}\right) + I_{KA}}$$

Figure 27. Precision Current Limiter



$$I_O = \frac{V_{I(ref)}}{R_S}$$

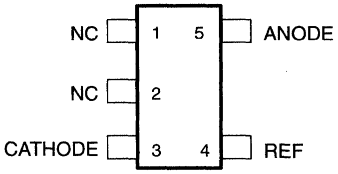
Figure 28. Precision Constant-Current Sink

TLV431A
LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS130 – OCTOBER 1995

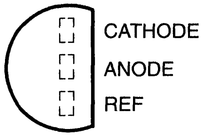
- **Low-Voltage Operation . . . to 1.24 V**
- **1% Reference Voltage Tolerance**
- **Adjustable Output Voltage, $V_O = V_{ref}$ to 6 V**
- **Low Operational Cathode Current . . . 80 μA**
- **0.25 Ω Typical Output Impedance**
- **SOT-23 Package**

DBV5 PACKAGE
(TOP VIEW)



NC - No internal connection

LP PACKAGE
(TOP VIEW)



description

The TLV431A is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage may be set to any value between V_{ref} (1.24 V) and 6 V with two external resistors (see Figure 2). The TLV431A operates from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt regulator references.

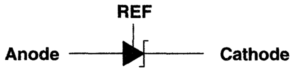
When used with an optocoupler, the TLV431A is an ideal voltage reference in an isolated feedback circuit for 3-V to 3.3-V switching-mode power supplies. This device has a typical output impedance of 0.25 Ω. Active output circuitry provides a very sharp turn-on characteristic, making the TLV431A an excellent replacement for low-voltage zener diodes in many applications, including on-board regulation and adjustable power supplies.

AVAILABLE OPTIONS

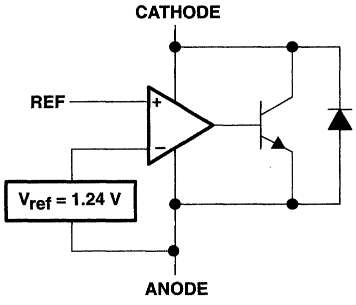
T_A	PACKAGED DEVICES		CHIP FORM (Y)
	TO-92 (LP)	SOT-23 (DBV5)	
0°C to 70°C	TLV431ACLP	TLV431ACDBV5	TLV431AY
−40°C to 85°C	TLV431AILP	TLV431AIDBV5	

The LP package is available taped and reeled. Add R suffix to device type (e.g., TLV431ACLPR).
The DBV5 is only available taped and reeled (no R suffix is required).

symbol

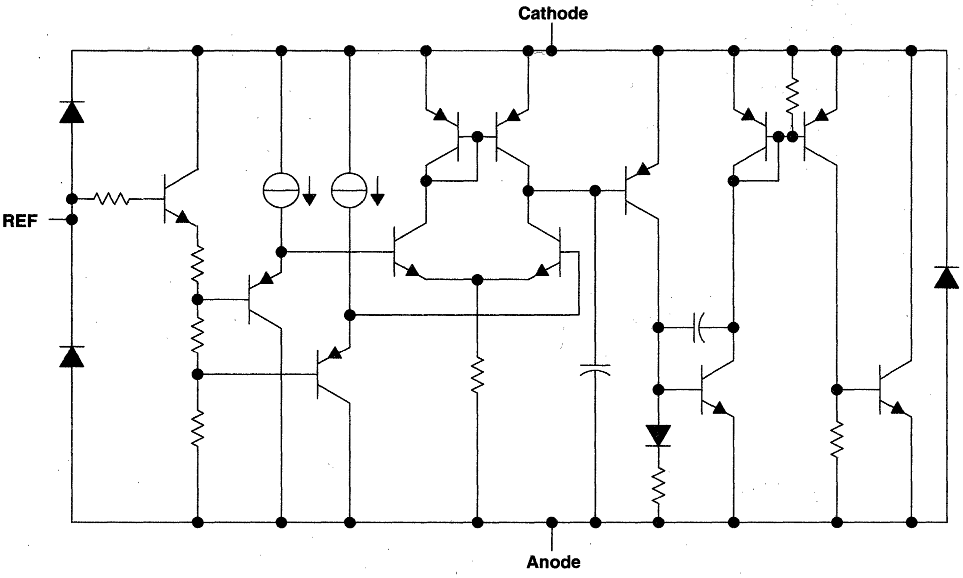


functional block diagram



TEXAS INSTRUMENTS

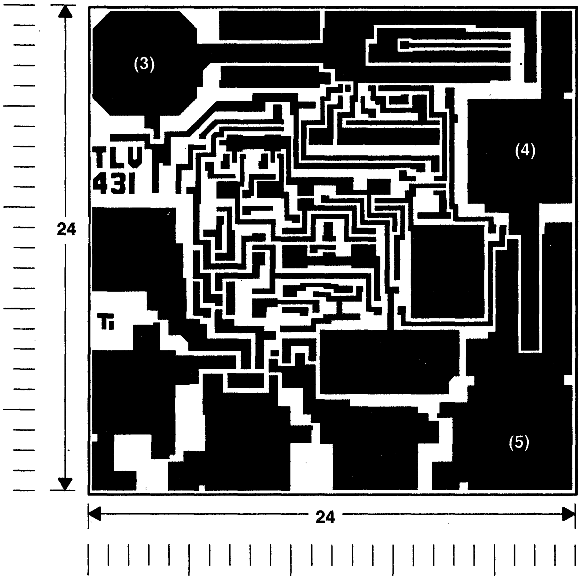
equivalent schematic



TLV431AY chip information

This chip, when properly assembled, displays characteristics similar to the TLV431A. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 10 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cathode voltage, V_{KA} (see Note 1)	7 V
Continuous cathode current range, I_K	−20 mA to 20 mA
Reference current range, I_{ref}	−0.05 mA to 3 mA
Power dissipation, P_D	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the anode terminal, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
LP	775 mW	6.2 mW/°C	496 mW	403 mW
DBV5	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

		MIN	MAX	UNIT
Cathode voltage, V_{KA}		V_{ref}	6	V
Cathode current, I_K		0.1	15	mA
Operating free-air temperature range, T_A	TLV431AC	0	70	°C
	TLV431AI	−40	85	

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV431AC			TLV431AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference voltage	$V_{KA} = V_{ref}$, I_K = 10 mA, See Figure 1	T_A = 25°C	1.228	1.240	1.252	1.228	1.240	1.252	V
			T_A = full range	1.221		1.259	1.215		1.265	
$V_{ref(dev)}$	V_{ref} deviation over full temperature range (see Note 3)	$V_{KA} = V_{ref}$, I_K = 10 mA, See Note 2 and Figure 1			4	12		6	20	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of V_{ref} change in cathode voltage change	I_K = 10 mA, $\Delta V_{KA} = V_{ref}$ to 6 V, See Figure 2			−1.5	−2.7		−1.5	−2.7	$\frac{mV}{V}$
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Figure 2			0.15	0.5		0.15	0.5	µA
$I_{ref(dev)}$	$I_{I(ref)}$ deviation over full temperature range (see Note 3)	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Note 2 and Figure 2			0.05	0.3		0.1	0.4	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{ref}$, See Figure 1			55	80		55	80	µA
I_{off}	Off-state cathode current	V_{KA} = 6 V, V_{ref} = 0, See Figure 3			0.001	0.1		0.001	0.1	µA
$\lvert z_{ka} \rvert$	Dynamic impedance (see Note 4)	$V_{KA} = V_{ref}$, f ≤ 1 kHz, I_K = 0.1 mA to 15 mA See Figure 1			0.25	0.4		0.25	0.4	Ω

NOTES: 2. Full temperature range is −40°C to 85°C for TLV431AI, and 0°C to 70°C for the TLV431AC.

3. The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\left|\alpha V_{ref}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref}\,(T_A = 25°C)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

4. The dynamic impedance is defined as: $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\left|z_{ka}\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

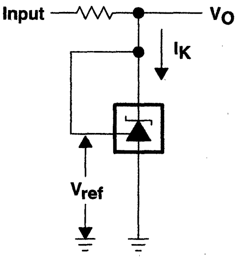


Figure 1. Test Circuit for $V_{KA} = V_{ref}$
$V_O = V_{KA} = V_{ref}$

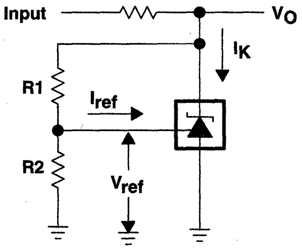


Figure 2. Test Circuit for $V_{KA} > V_{ref}$
$V_O = V_{KA} = V_{ref} \times (1 + R1/R2) + I_{ref} \times R1$

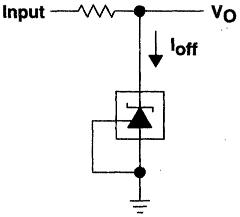


Figure 3. Test Circuit for I_{off}

PARAMETER MEASUREMENT INFORMATION

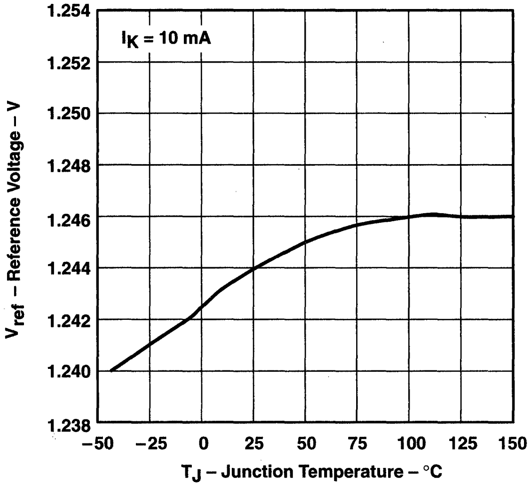

REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 4

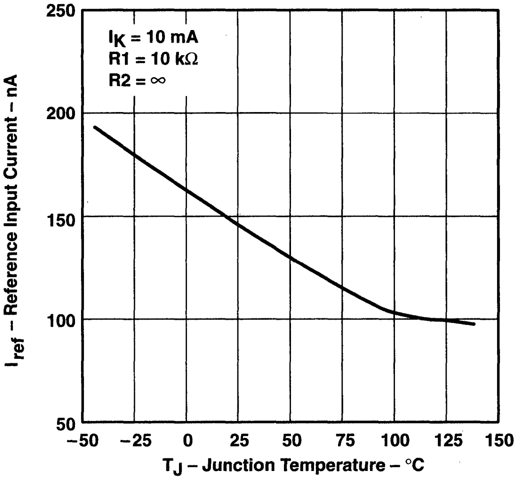

REFERENCE INPUT CURRENT
vs
JUNCTION TEMPERATURE

Figure 5

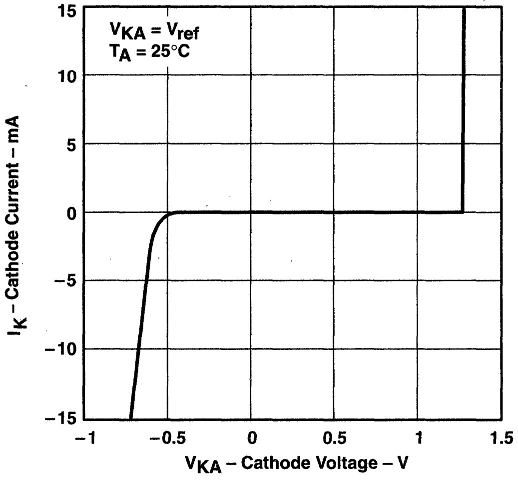

CATHODE CURRENT
vs
CATHODE VOLTAGE

Figure 6

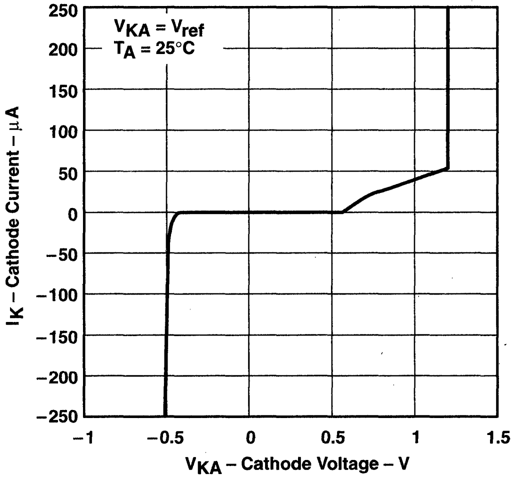

CATHODE CURRENT
vs
CATHODE VOLTAGE

Figure 7

PARAMETER MEASUREMENT INFORMATION

OFF-STATE CATHODE CURRENT vs JUNCTION TEMPERATURE

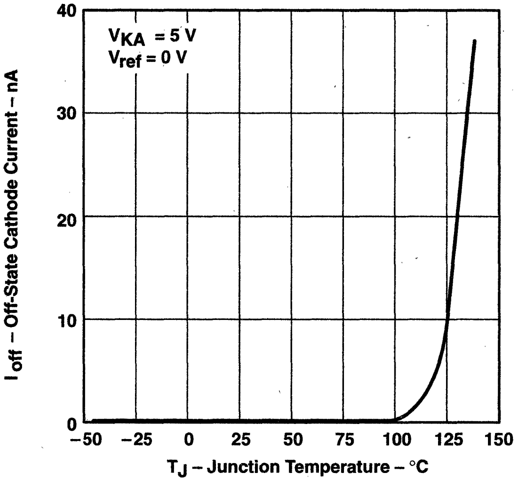


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE TO DELTA CATHODE VOLTAGE vs JUNCTION TEMPERATURE

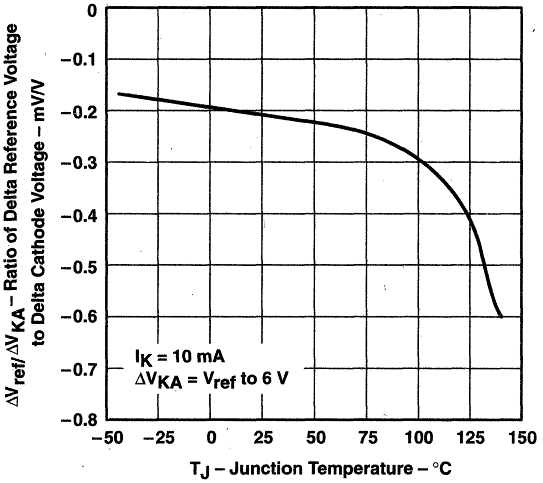
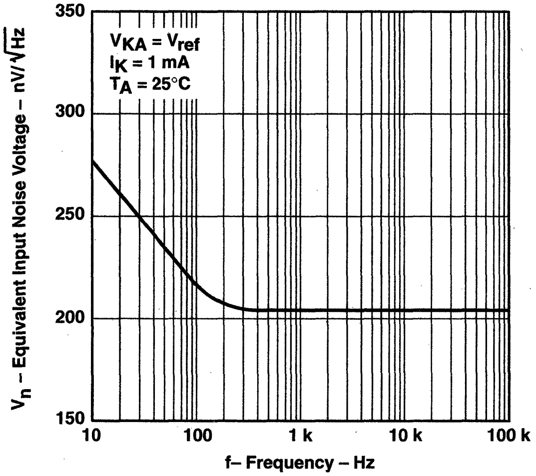
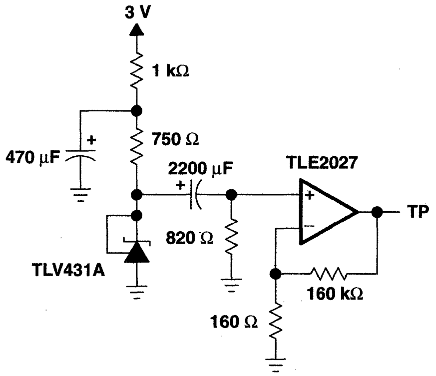


Figure 9

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



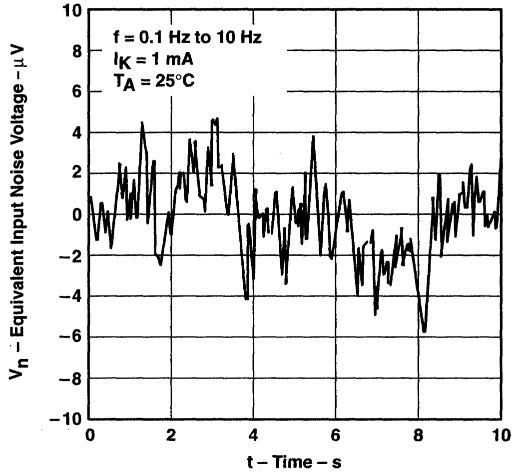


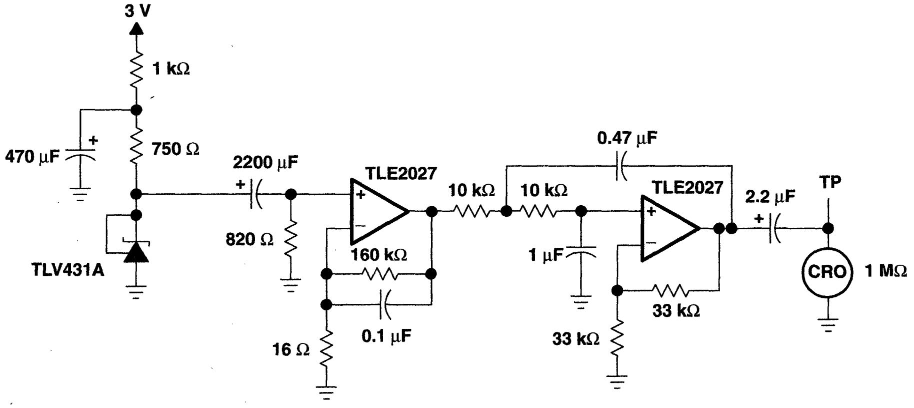
Test circuit for equivalent noise voltage

Figure 10

PARAMETER MEASUREMENT INFORMATION

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD



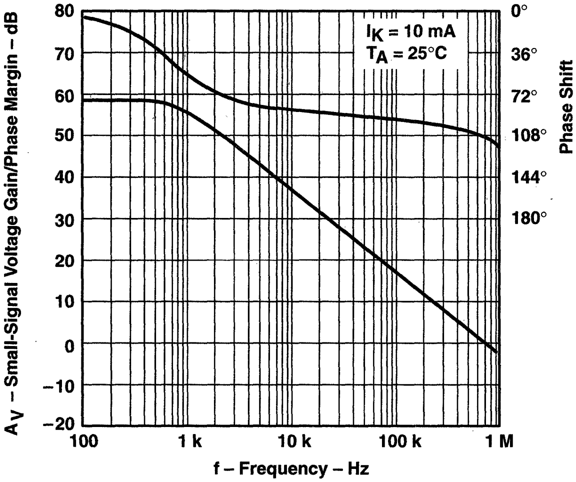


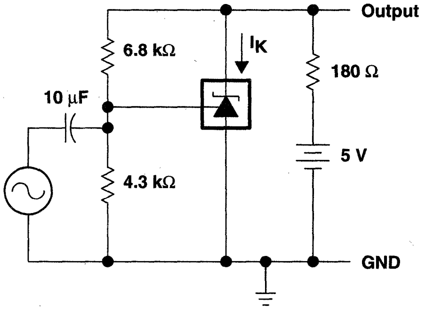
Test circuit for 0.1-Hz to 10-Hz equivalent noise voltage

Figure 11

PARAMETER MEASUREMENT INFORMATION

SMALL-SIGNAL VOLTAGE GAIN /PHASE MARGIN vs FREQUENCY

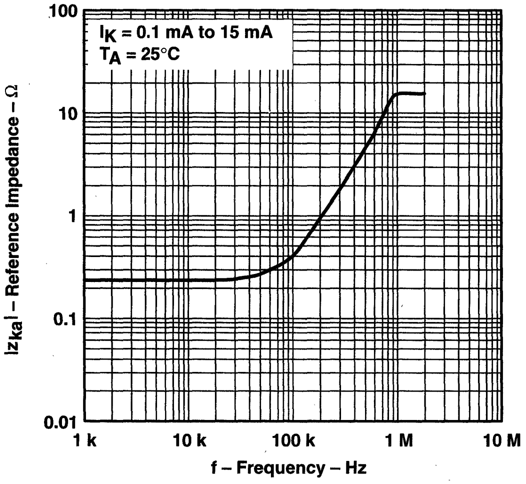


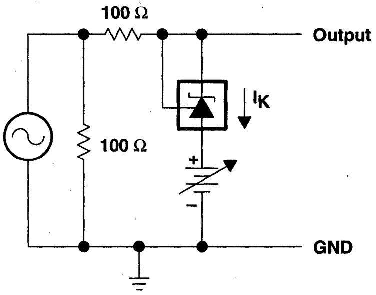


TEST CIRCUIT FOR VOLTAGE GAIN AND PHASE MARGIN

Figure 12

REFERENCE IMPEDANCE vs FREQUENCY



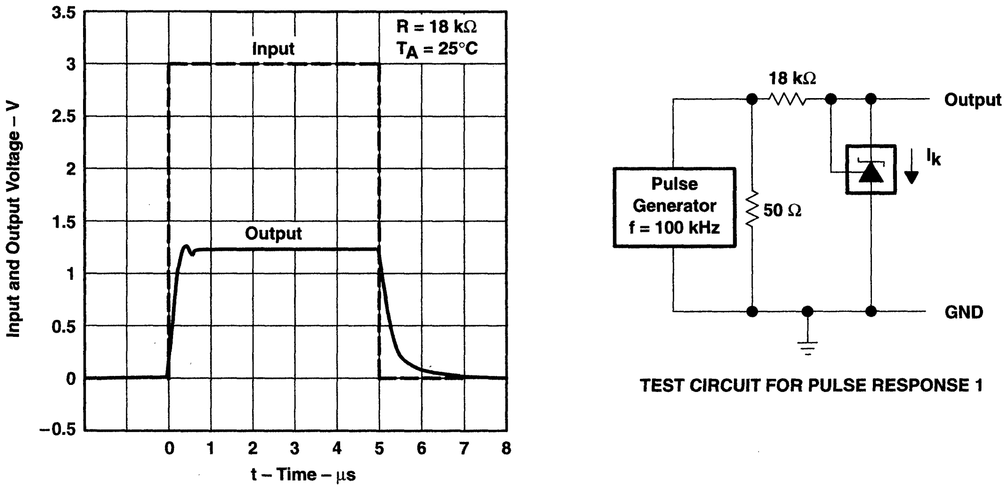


TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 13

PARAMETER MEASUREMENT INFORMATION

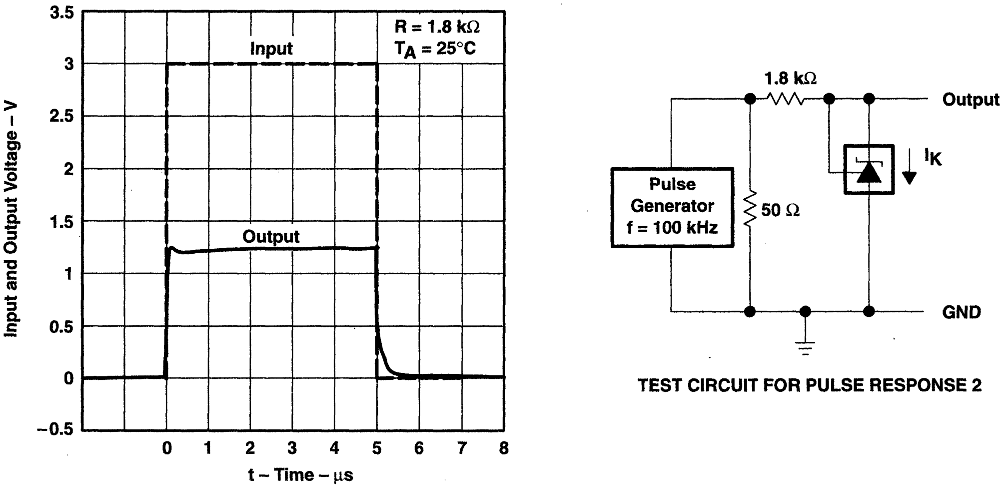
PULSE RESPONSE 1



TEST CIRCUIT FOR PULSE RESPONSE 1

Figure 14

PULSE RESPONSE 2

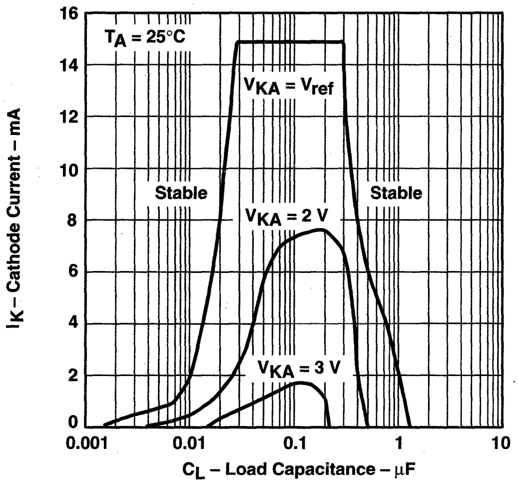


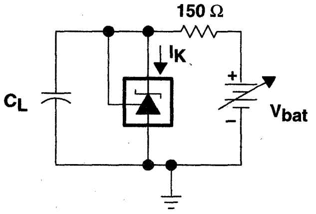
TEST CIRCUIT FOR PULSE RESPONSE 2

Figure 15

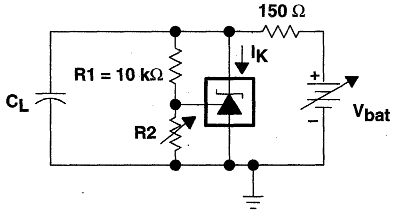
PARAMETER MEASUREMENT INFORMATION

STABILITY BOUNDARY CONDITION†





TEST CIRCUIT FOR $V_{KA} = V_{ref}$



TEST CIRCUIT FOR V_{KA} = 2 V, 3 V

† The areas under the curves represent conditions that may cause the device to oscillate. For V_{KA} = 2 V and 3 V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L were then adjusted to determine the ranges of stability.

Figure 16

APPLICATION INFORMATION

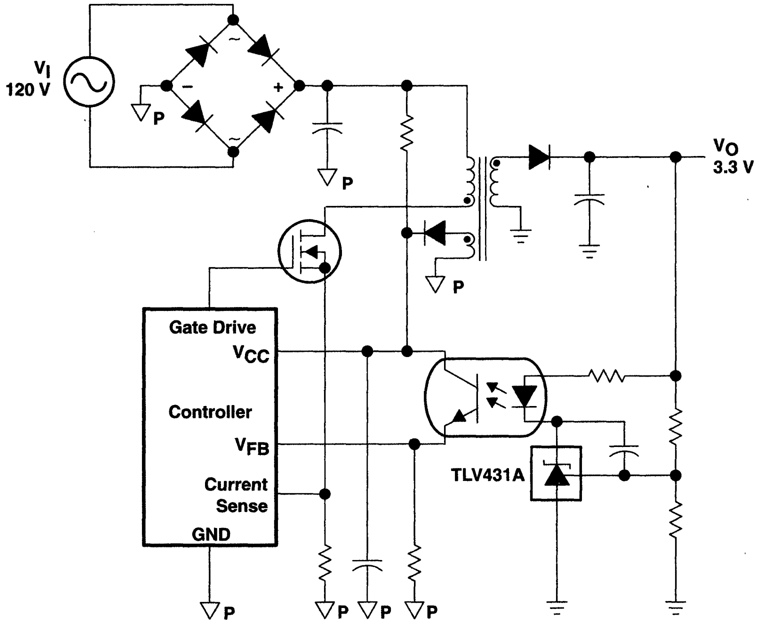


Figure 17. Flyback with Isolation using TLV431A as Voltage Reference and Error Amplifier.

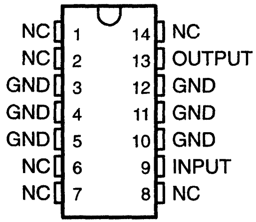
Figure 17 shows the TLV431A used in a 3.3-V isolated flyback supply. V_O of the TLV431A can be as low as V_{ref} (1.244 V ± 1%). The output of the regulator plus the forward voltage drop of the optocoupler LED (1.244 + 1.4 = 2.644 V) determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the above topology.

TLV2217-33, TLV2217-33Y
LOW-DROPOUT 3.3-V FIXED VOLTAGE REGULATORS

SLVS067B – MARCH 1992 – REVISED OCTOBER 1995

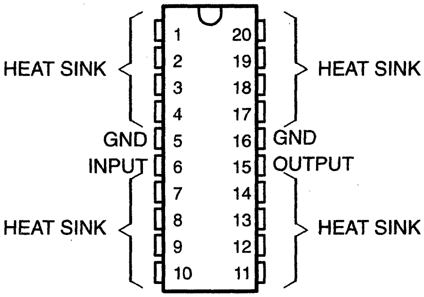
- **Fixed 3.3-V Output**
- **±1% Maximum Output Voltage Tolerance at $T_J = 25°C$**
- **500-mV Maximum Dropout Voltage at 500-mA**
- **500-mA Dropout Current**
- **±2% Absolute Output Voltage Variation**
- **Internal Overcurrent Limiting**
- **Internal Thermal Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



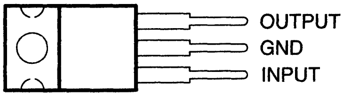
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded.

KC PACKAGE
(TOP VIEW)



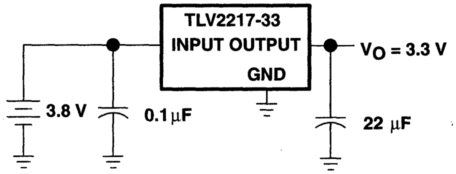
description

The TLV2217-33 is a low-dropout 3.3-V fixed voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV 2217-33 provides internal overcurrent limiting, thermal overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator may drop as low as 3.8 V, and the TLV2217-33 will continue to regulate the system. For higher voltage systems, the TLV2217-33 may be operated with a continuous input voltage of 12 V.

The TLV2217-33N and TLV2217-33KC cannot be harmed by temporary mirror-image insertion. This regulator is characterized for operation from 0°C to 125°C virtual junction temperature.

application schematic



AVAILABLE OPTIONS

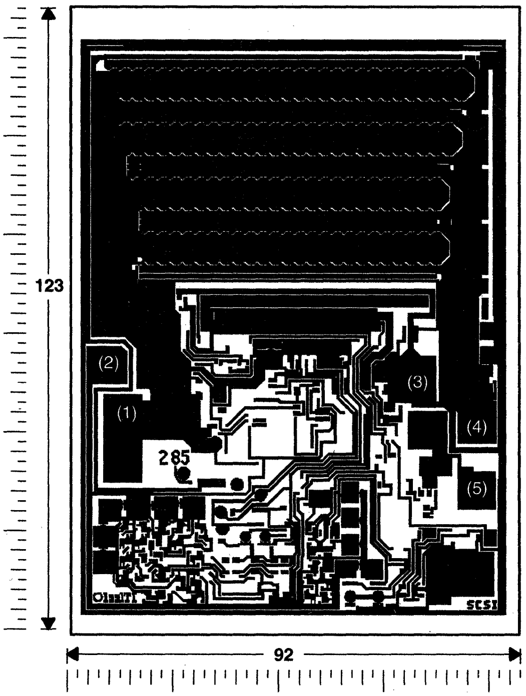
T_J	PACKAGE			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†	
0°C to 125°C	TLV2217-33KC	TLV2217-33N	TLV2217-33PWLE	TLV2217-33Y

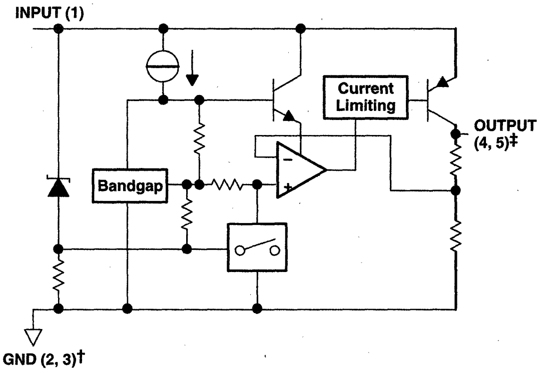
† The PW package is only available left-end taped and reeled.

TLV2217-33Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2217-33 (see electrical Tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 TYPICAL

BONDING PADS: 7 × 7 MINIMUM

T_{JMmax}= 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

† Must connect pads 2 and 3 together

‡ Must connect pads 2 and 3 together

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I .... 16 V
Continuous total power dissipation (see Note 1) .... See Dissipation Rating Table
Operating virtual junction temperature range, ,T_A .... −55°C to 150°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	T_C†	20000 mW	182.0 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

† Derate above 40°C

MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE

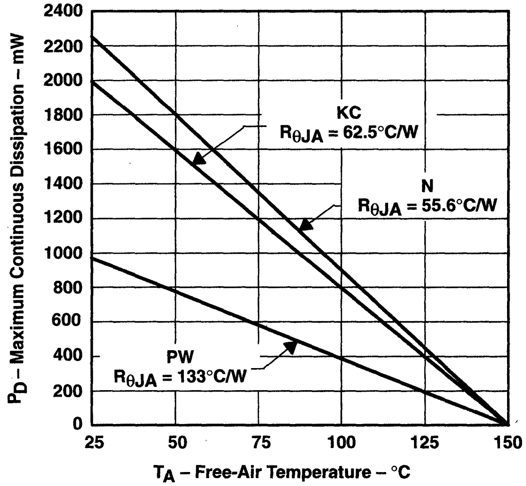


Figure 1

MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE

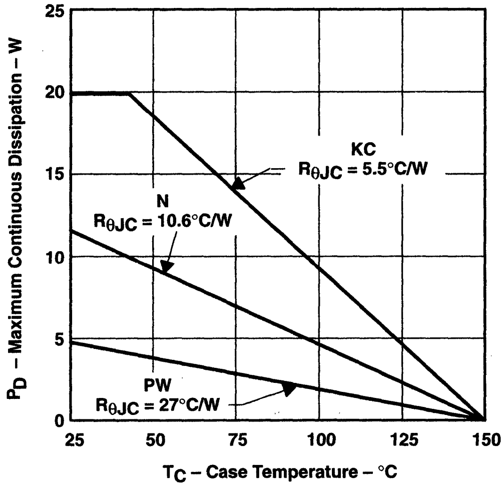


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.8	12	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}			−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33Y			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA,	V_I = 3.8 V to 5.5 V	3.267	3.30	3.333	V
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}			−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

ESR OF OUTPUT CAPACITOR
vs
LOAD CURRENT

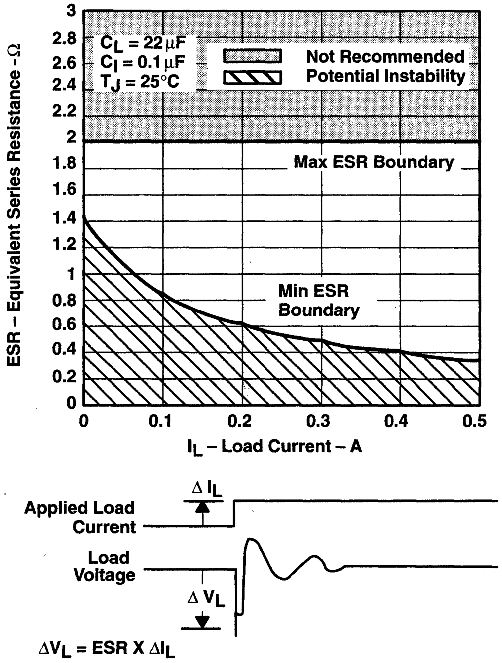


Figure 3

STABILITY
vs
ESR

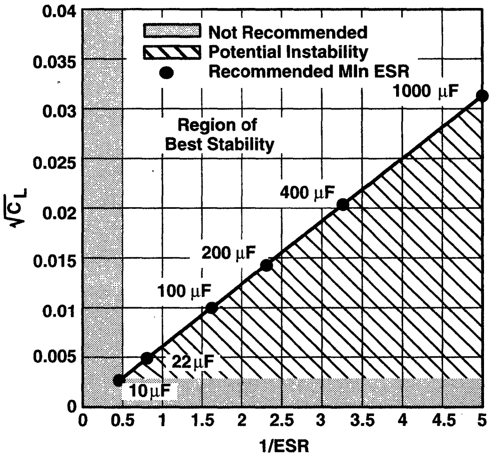


Figure 4

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
LOW-DROPOUT VOLTAGE REGULATORS

SLVS092C – NOVEMBER 1994 – REVISED AUGUST 1995

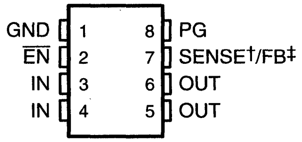
- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Very Low-Dropout Voltage . . . Maximum of 32 mV at I_O = 100 mA (TPS7150)**
- **Very Low Quiescent Current – Independent of Load . . . 285 μA Typ**
- **Extremely Low Sleep-State Current 0.5 μA Max**
- **2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions**
- **Output Current Range of 0 mA to 500 mA**
- **TSSOP Package Option Offers Reduced Component Height for Critical Applications**
- **Power Good (PG) Status Output**

description

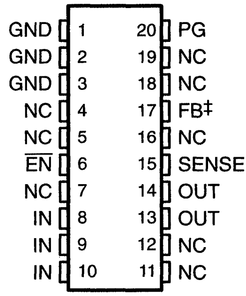
The TPS71xx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS7150) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection
† SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
‡ FB – Adjustable version only (TPS7101)

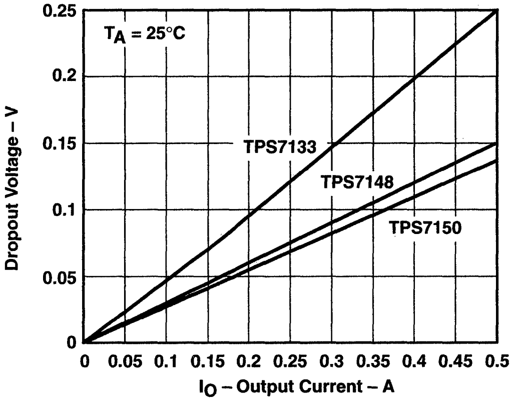


Figure 1. Dropout Voltage Versus Output Current

Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

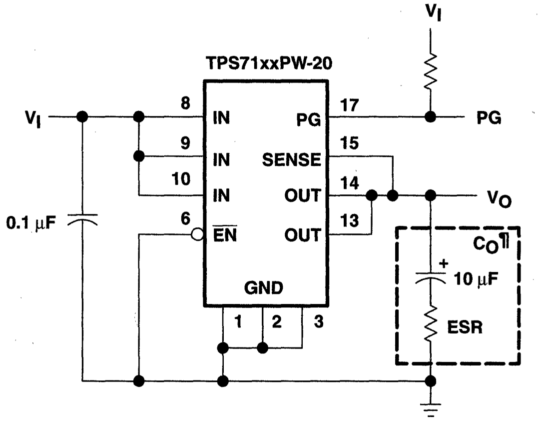
The TPS71xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71xx family is available in PDIP (8 pin), SO (8 pin), and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

TEXAS INSTRUMENTS

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−55°C to 150°C	4.9	5	5.1	TPS7150QD	TPS7150QP	TPS7150QPWLE	TPS7150Y
	4.75	4.85	4.95	TPS7148QD	TPS7148QP	TPS7148QPWLE	TPS7148Y
	3.23	3.3	3.37	TPS7133QD	TPS7133QP	TPS7133QPWLE	TPS7133Y
	Adjustable§ 1.2 V to 9.75 V			TPS7101QD	TPS7101QP	TPS7101QPWLE	TPS7101Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7150QDR). The PW package is only available left-end taped and reeled and is indicated by the LE suffix on the device type (i.e., TPS7150QPWLE). The TPS7101Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.



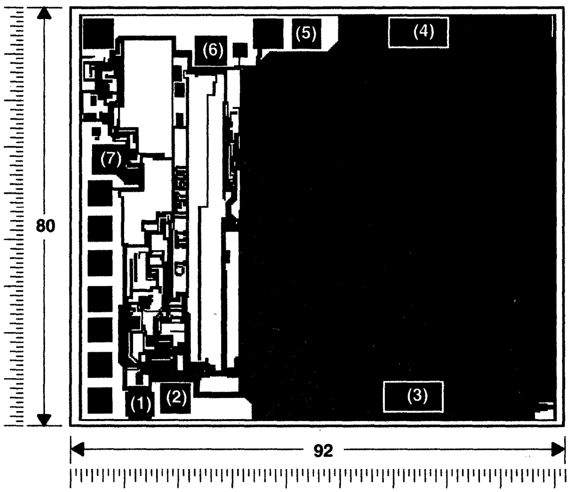
¶ Capacitor selection is nontrivial. See application information section for details.

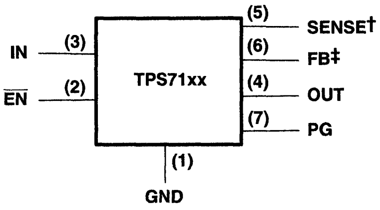
Figure 2. Typical Application Configuration

TPS71xx chip information

These chips, when properly assembled, display characteristics similar to the TPS71xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

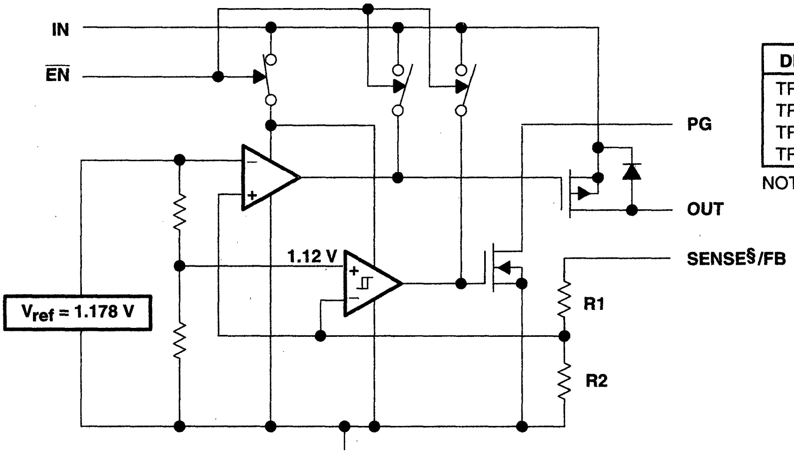
ALL DIMENSIONS ARE IN MILS.

† SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)

‡ FB – Adjustable version only (TPS7101)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the applications information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7101	0	∞	Ω
TPS7133	420	233	kΩ
TPS7148	726	233	kΩ
TPS7150	756	233	kΩ

NOTE: Resistors are nominal values only.

---

§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I, PG, SENSE, $\overline{EN}$	−0.3 to 10 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	−55°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW§	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW§	4025 mW	32.2 mW/°C	2576 mW	805 mW

§ Refer to thermal information section for detailed power dissipation considerations when using the TSSOP package.

DISSIPATION DERATING CURVE
vs
FREE-AIR TEMPERATURE

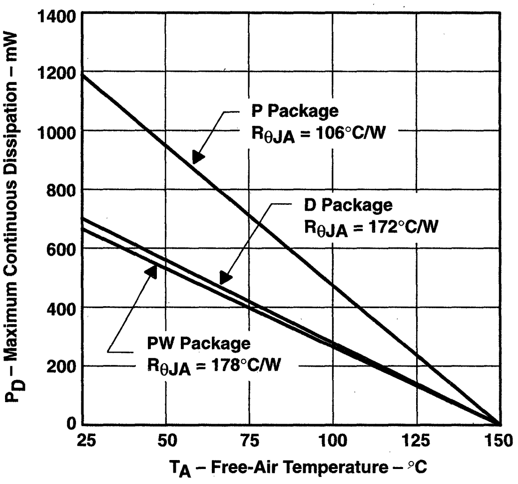


Figure 3

DISSIPATION DERATING CURVE
vs
CASE TEMPERATURE

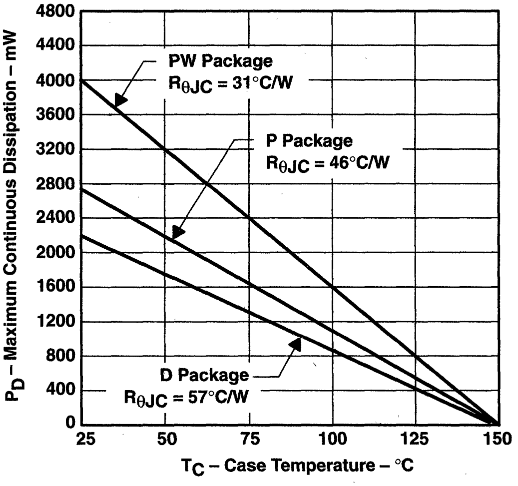


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7101Q	2.5	10	V
	TPS7133Q	3.77	10	
	TPS7148Q	5.2	10	
	TPS7150Q	5.33	10	
High-level input voltage at $\overline{\text{EN}}$, V_{IH}		2		V
Low-level input voltage at $\overline{\text{EN}}$, V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7101 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7101.

electrical characteristics at I_O = 10 mA, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	TPS7101Q, TPS7133Q TPS7148Q, TPS7150Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{\text{EN}} \le 0.5$ V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 500 mA	25°C		285	350	μA
		−40°C to 125°C			460	
Input current (standby mode)	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			2	
Output current limit	V_O = 0 V, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
PG leakage current	Normal operation, V_{PG} = 10 V	25°C		0.02	0.5	μA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{\text{EN}}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{\text{EN}}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{\text{EN}}$ hysteresis voltage		25°C		50		mV
$\overline{\text{EN}}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	μA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 μA	25°C		1.06	1.5	V
		−40°C to 125°C			1.9	

† ESR refers to the equivalent resistance, including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7101Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V, I_O = 10 mA		25°C		1.178		V
	2.5 V ≤ V_I ≤ 10 V, 5 mA ≤ I_O ≤ 500 mA, See Note 1		−40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V, 50 μA ≤ I_O ≤ 150 mA		25°C		0.7	1	Ω
			−40°C to 125°C			1	
	V_I = 2.4 V, 150 mA ≤ I_O ≤ 500 mA		25°C		0.83	1.3	
			−40°C to 125°C			1.3	
	V_I = 2.9 V, 50 μA ≤ I_O ≤ 500 mA		25°C		0.52	0.85	
			−40°C to 125°C			0.85	
	V_I = 3.9 V, 50 μA ≤ I_O ≤ 500 mA		25°C		0.32		
	V_I = 5.9 V, 50 μA ≤ I_O ≤ 500 mA		25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, 50 μA ≤ I_O ≤ 500 mA, See Note 1		25°C			18	mV
			−40°C to 125°C			25	
Output regulation	I_O = 5 mA to 500 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 1		25°C			14	mV
			−40°C to 125°C			25	
	I_O = 50 μA to 500 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 1		25°C			22	mV
			−40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	48	59		dB
			−40°C to 125°C	44			
		I_O = 500 mA, See Note 1	25°C	45	54		
			−40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 μF	25°C		95		μVrms
		C_O = 10 μF	25°C		89		
		C_O = 100 μF	25°C		74		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{FB(nom)}$		0.98 × $V_{FB(nom)}$	V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 μA, V_I = 2.13 V		25°C		0.1	0.4	V
			−40°C to 125°C			0.4	
FB input current			25°C	−10	0.1	10	nA
			−40°C to 125°C	−20		20	

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 31) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 30.

electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7133Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		0.02	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		47	60	
			–40°C to 125°C			80	
	I_O = 500 mA,	V_I = 3.23 V	25°C		235	300	
			–40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,	25°C		0.47	0.6	Ω
			–40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			20	mV
			–40°C to 125°C			27	
Output regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			–40°C to 125°C			75	
	I_O = 50 μA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			–40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	43	54		dB
			–40°C to 125°C	40			
		I_O = 500 mA	25°C	39	49		
			–40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 μF	25°C		274		μVrms
		C_O = 10 μF	25°C		228		
		C_O = 100 μF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			–40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at $I_O = 10$ mA, $V_I = 5.85$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7148Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 5.85$ V,	$I_O = 10$ mA	25°C		4.85		V
	$5.85\ V \le V_I \le 10$ V,	$5\ mA \le I_O \le 500$ mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.75$ V	25°C		0.08	6	mV
			–40°C to 125°C			8	
	$I_O = 100$ mA,	$V_I = 4.75$ V	25°C		30	37	
			–40°C to 125°C			54	
	$I_O = 500$ mA,	$V_I = 4.75$ V	25°C		150	180	
			–40°C to 125°C			250	
Pass-element series resistance	$(4.75\ V - V_O)/I_O$, $I_O = 500$ mA	$V_I = 4.75$ V,	25°C		0.32	0.35	Ω
			–40°C to 125°C			0.52	
Input regulation	$V_I = 5.85$ V to 10 V,	$50\ µA \le I_O \le 500$ mA	25°C			27	mV
			–40°C to 125°C			37	
Output regulation	$I_O = 5$ mA to 500 mA,	$5.85\ V \le V_I \le 10$ V	25°C		12	42	mV
			–40°C to 125°C			80	
	$I_O = 50$ µA to 500 mA,	$5.85\ V \le V_I \le 10$ V	25°C		42	60	mV
			–40°C to 125°C			130	
Ripple rejection	f = 120 Hz	$I_O = 50$ µA	25°C	42	53		dB
			–40°C to 125°C	39			
		$I_O = 500$ mA	25°C	39	50		
			–40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	$C_O = 4.7$ µF	25°C		410		µVrms
		$C_O = 10$ µF	25°C		328		
		$C_O = 100$ µF	25°C		212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	$I_{PG} = 1.2$ mA,	$V_I = 4.12$ V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7150Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		0.13	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	32	
			−40°C to 125°C			47	
	I_O = 500 mA,	V_I = 4.88 V	25°C		146	170	
			−40°C to 125°C			230	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 500 mA	V_I = 4.88 V.	25°C		0.29	0.32	Ω
			−40°C to 125°C			0.47	
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			25	mV
			−40°C to 125°C			32	
Output regulation	I_O = 5 mA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		30	45	mV
			−40°C to 125°C			86	
	I_O = 50 µA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		45	65	mV
			−40°C to 125°C			140	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	45	55		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	42	52		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		430		µVrms
		C_O = 10 µF	25°C		345		
		C_O = 100 µF	25°C		220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		53		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7101Y, TPS7133Y TPS7148Y, TPS7150Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 500 mA		285		μA
Output current limit	V_O = 0 V, V_I = 10 V		1.2		A
PG leakage current	Normal operation, V_{PG} = 10 V		0.02		μA
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ hysteresis voltage			50		mV
Minimum V_I for active pass element			2.05		V
Minimum V_I for valid PG	I_{PG} = 300 μA		1.06		V

† ESR refers to the equivalent resistance, including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡	TPS7101Y			UNIT
		MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V, I_O = 10 mA		1.178		V
Pass-element series resistance (see Note 2)	V_I = 2.4 V, 50 μA ≤ I_O ≤ 150 mA		0.7		Ω
	V_I = 2.4 V, 150 mA ≤ I_O ≤ 500 mA		0.83		
	V_I = 2.9 V, 50 μA ≤ I_O ≤ 500 mA		0.52		
	V_I = 3.9 V, 50 μA ≤ I_O ≤ 500 mA		0.32		
	V_I = 5.9 V, 50 μA ≤ I_O ≤ 500 mA		0.23		
Input regulation	V_I = 2.5 V to 10 V, 50 μA ≤ I_O ≤ 500 mA, See Note 1			18	mV
Output regulation	2.5 V ≤ V_I ≤ 10 V, I_O = 5 mA to 500 mA, See Note 1			14	mV
	2.5 V ≤ V_I ≤ 10 V, I_O = 50 μA to 500 mA, See Note 1			22	mV
Ripple rejection	V_I = 3.5 V, f = 120 Hz, I_O = 50 μA		59		dB
Output noise-spectral density	V_I = 3.5 V, f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω, C_O = 4.7 μF		95		μVrms
	C_O = 10 μF		89		
	C_O = 100 μF		74		
PG hysteresis voltage§	V_I = 3.5 V, Measured at V_{FB}		12		mV
PG output low voltage§	V_I = 2.13 V, I_{PG} = 400 μA		0.1		V
FB input current	V_I = 3.5 V		0.1		nA

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1 When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 31) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2 To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 30.

electrical characteristics at $I_O = 10$ mA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF/ESR† = 1 Ω, $T_J = 25°C$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7133Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	V_I = 3.23 V,	I_O = 10 mA		0.02		mV
	V_I = 3.23 V,	I_O = 100 mA		47		
	V_I = 3.23 V,	I_O = 500 mA		235		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,		0.47		Ω
Output regulation	4.3 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		21		mV
	4.3 V ≤ V_I ≤ 10 V,	I_O = 50 µA to 500 mA		30		mV
Ripple rejection	V_I = 4.3 V, f = 120 Hz	I_O = 50 µA		54		dB
		I_O = 500 mA		49		
Output noise-spectral density	V_I = 4.3 V,	f = 120 Hz		2		µV/√Hz
Output noise voltage	V_I = 4.3 V, 10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF		274		µVrms
		C_O = 10 µF		228		
		C_O = 100 µF		159		
PG hysteresis voltage	V_I = 4.3 V			35		mV
PG output low voltage	V_I = 2.8 V,	I_{PG} = 1 mA		0.22		V

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7148Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	V_I = 4.75 V,	I_O = 10 mA		0.08		mV
	V_I = 4.75 V,	I_O = 100 mA		30		
	V_I = 4.75 V,	I_O = 500 mA		150		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 500 mA	V_I = 4.75 V,		0.32		Ω
Output regulation	5.85 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		12		mV
	5.85 V ≤ V_I ≤ 10 V,	I_O = 50 µA to 500 mA		42		mV
Ripple rejection	V_I = 5.85 V, f = 120 Hz	I_O = 50 µA		53		dB
		I_O = 500 mA		50		
Output noise-spectral density	V_I = 5.85 V,	f = 120 Hz		2		µV/√Hz
Output noise voltage	V_I = 5.85 V, 10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF		410		µVrms
		C_O = 10 µF		328		
		C_O = 100 µF		212		
PG hysteresis voltage	V_I = 5.85 V			50		mV
PG output low voltage	V_I = 4.12 V,	I_{PG} = 1.2 mA		0.2	0.4	V

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7150Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA		5		V
Dropout voltage	V_I = 4.88 V,	I_O = 10 mA		0.13		mV
	V_I = 4.88 V,	I_O = 100 mA		27		
	V_I = 4.88 V,	I_O = 500 μA		146		
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 500 mA	V_I = 4.88 V.		0.29		Ω
Output regulation	6 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 500 mA		30		mV
	6 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 500 mA		45		mV
Ripple rejection	V_I = 6 V, f = 120 Hz	I_O = 50 μA		55		dB
		I_O = 500 mA		52		
Output noise-spectral density	V_I = 6 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 6 V, 10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 μF		430		μVrms
		C_O = 10 μF		345		
		C_O = 100 μF		220		
PG hysteresis voltage	V_I = 6 V			53		mV
PG output low voltage	V_I = 4.25 V,	I_{PG} = 1.2 mA		0.2		V

† ESR refers to the equivalent resistance including internal resistance and series resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
OUTPUT CURRENT

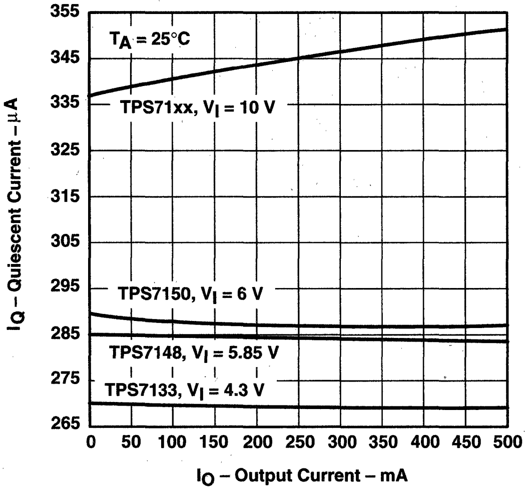

Figure 5

QUIESCENT CURRENT
vs
INPUT VOLTAGE

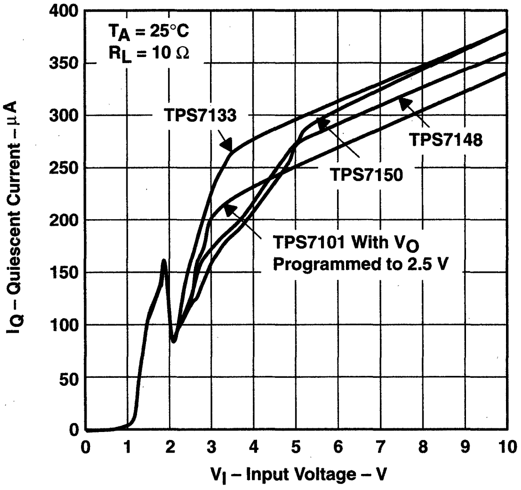

Figure 6

TPS7148Q
QUIESCENT CURRENT
vs
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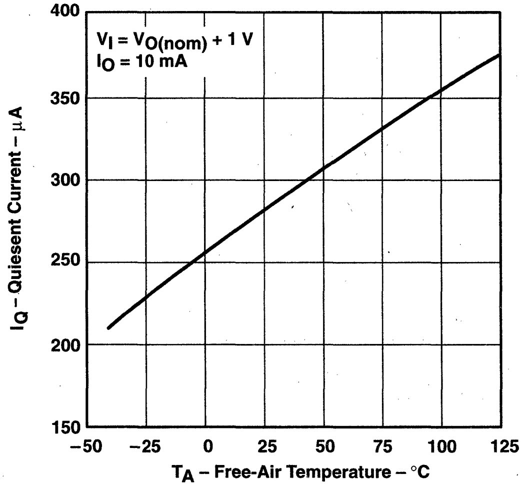

Figure 7

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

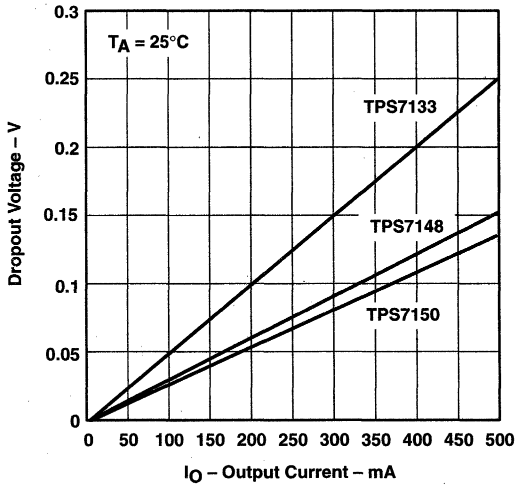

Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

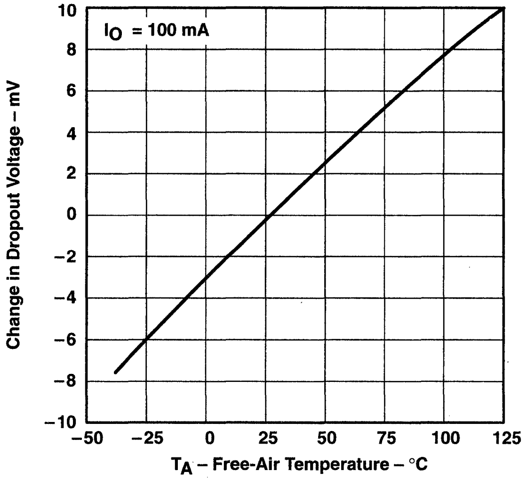

Figure 9

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

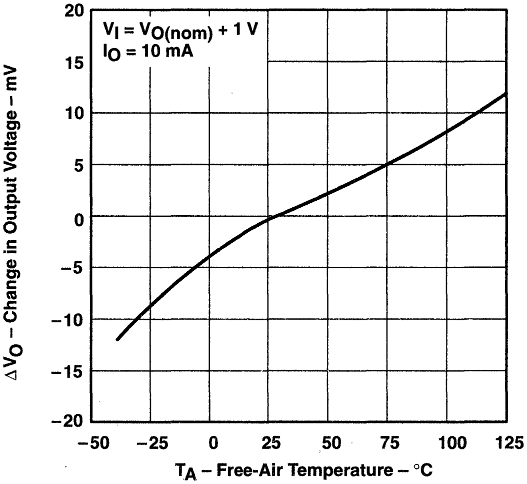

Figure 10

OUTPUT VOLTAGE vs INPUT VOLTAGE

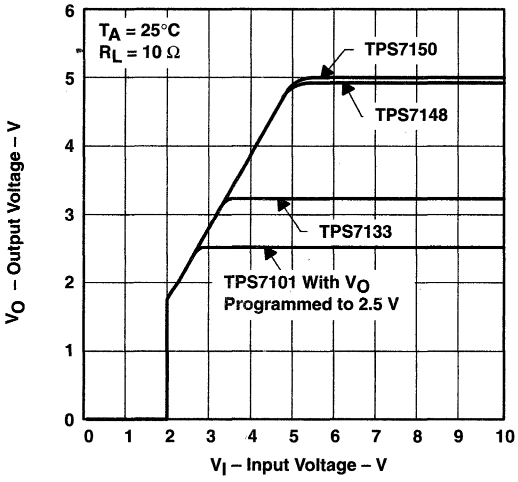

Figure 11

CHANGE IN OUTPUT VOLTAGE vs INPUT VOLTAGE

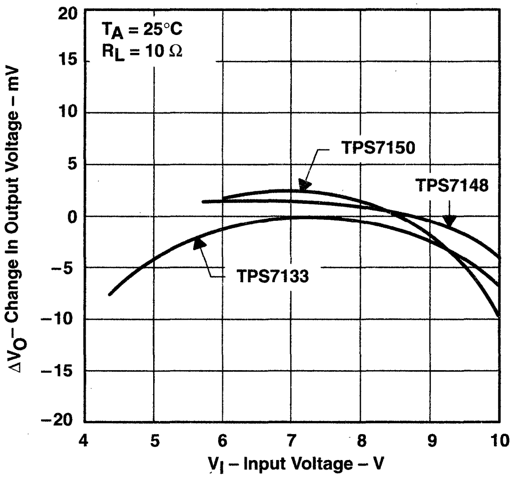

Figure 12

TYPICAL CHARACTERISTICS

TPS7101Q OUTPUT VOLTAGE vs OUTPUT CURRENT

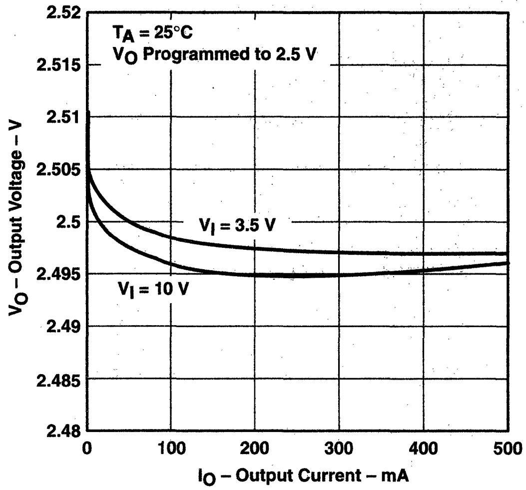

Figure 13

TPS7133Q OUTPUT VOLTAGE vs OUTPUT CURRENT

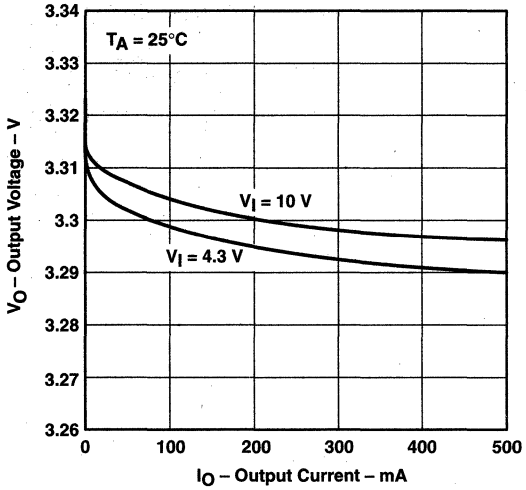

Figure 14

TPS7148Q OUTPUT VOLTAGE vs OUTPUT CURRENT

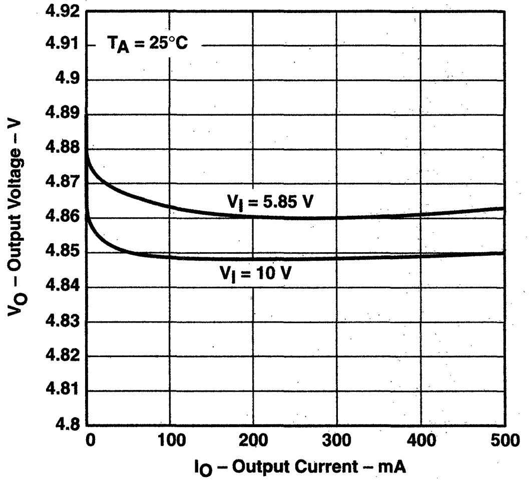

Figure 15

TPS7150Q OUTPUT VOLTAGE vs OUTPUT CURRENT

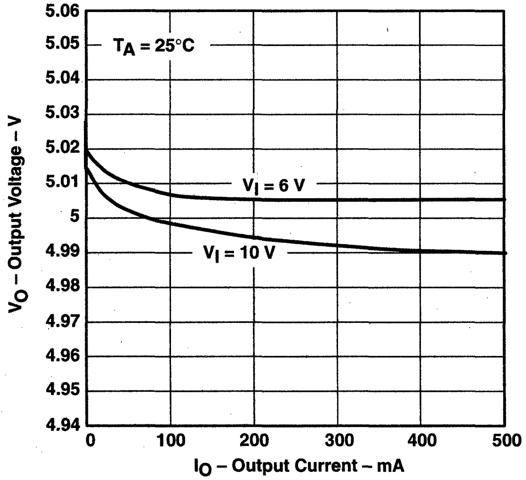

Figure 16

TYPICAL CHARACTERISTICS

**TPS7101Q
RIPPLE REJECTION
vs
FREQUENCY**

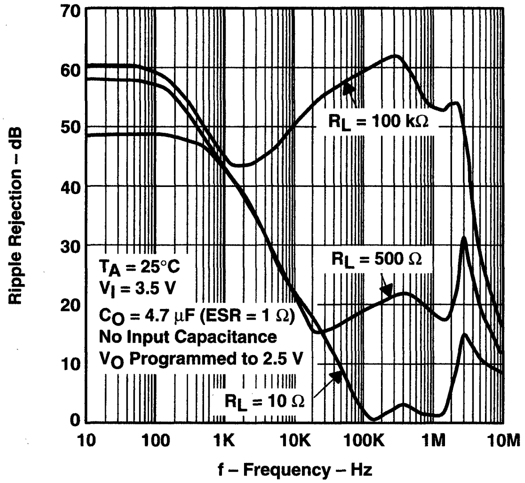

Figure 17

**TPS7133Q
RIPPLE REJECTION
vs
FREQUENCY**

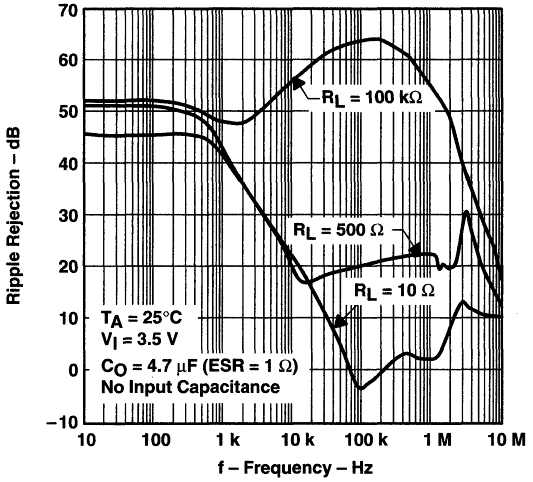

Figure 18

**TPS7148Q
RIPPLE REJECTION
vs
FREQUENCY**

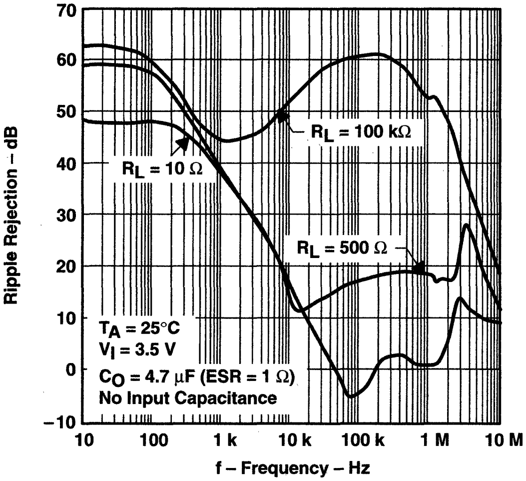

Figure 19

**TPS7150Q
RIPPLE REJECTION
vs
FREQUENCY**

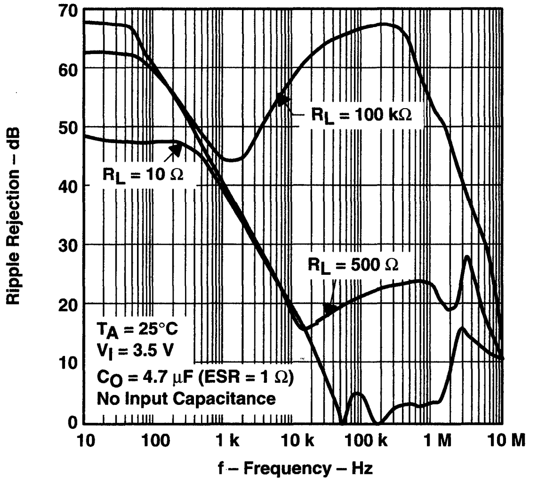

Figure 20

TYPICAL CHARACTERISTICS

TPS7101Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

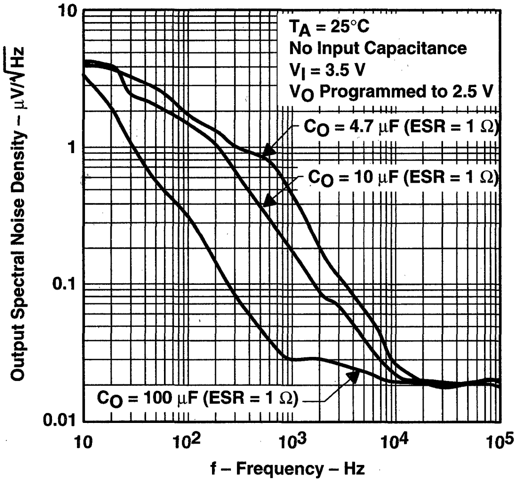

Figure 21

TPS7133Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

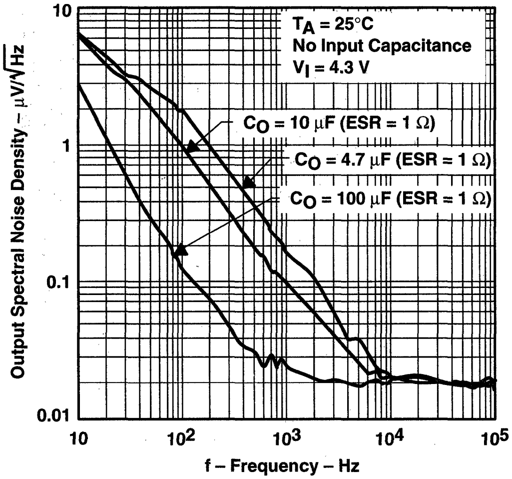

Figure 22

TPS7148Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

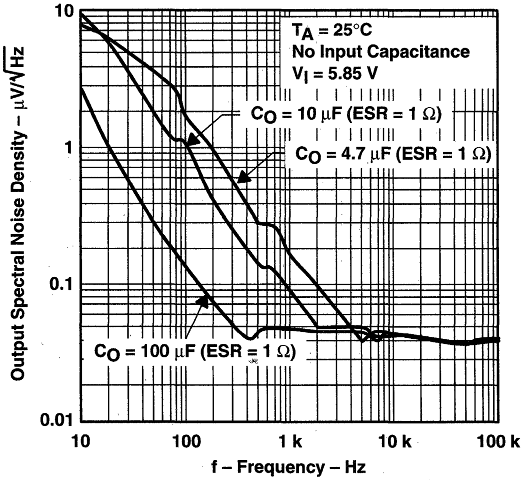

Figure 23

TPS7150Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

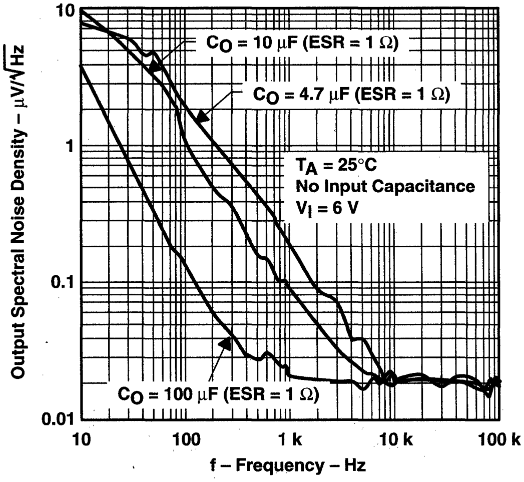

Figure 24

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

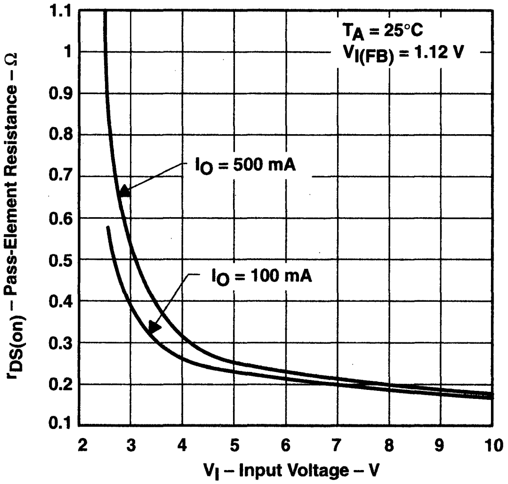

Figure 25

DIVIDER RESISTANCE vs FREE-AIR TEMPERATURE

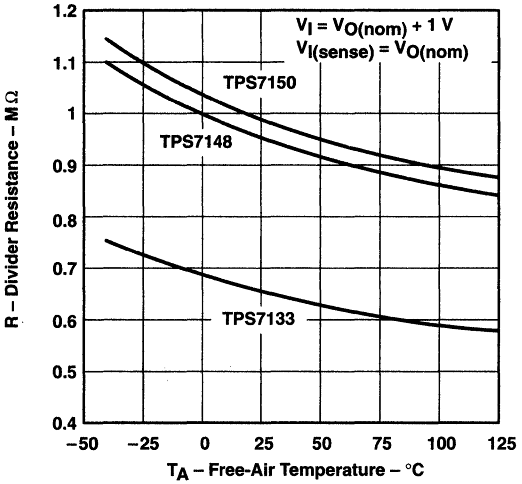

Figure 26

FIXED-OUTPUT VERSIONS SENSE PIN CURRENT vs FREE-AIR TEMPERATURE

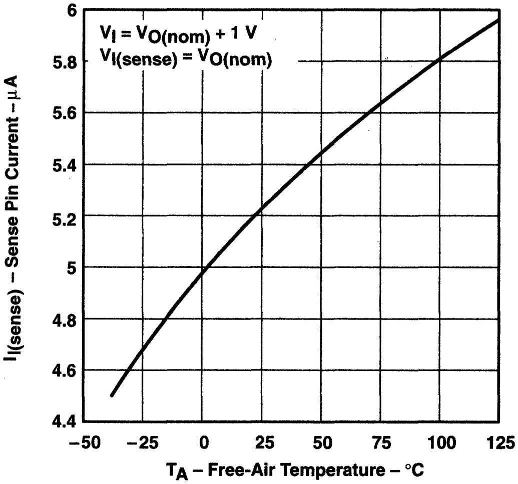

Figure 27

ADJUSTABLE VERSION FB LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

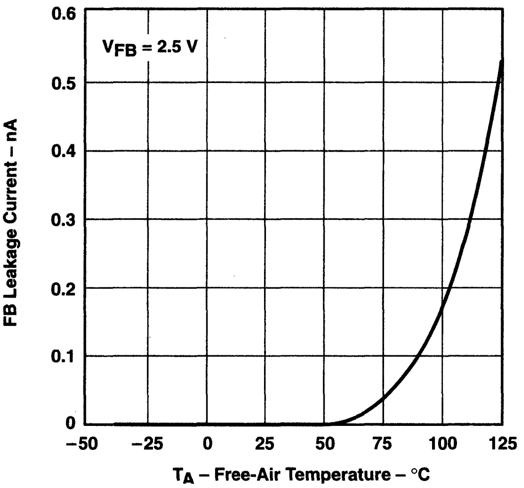

Figure 28

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE PASS ELEMENT vs FREE-AIR TEMPERATURE

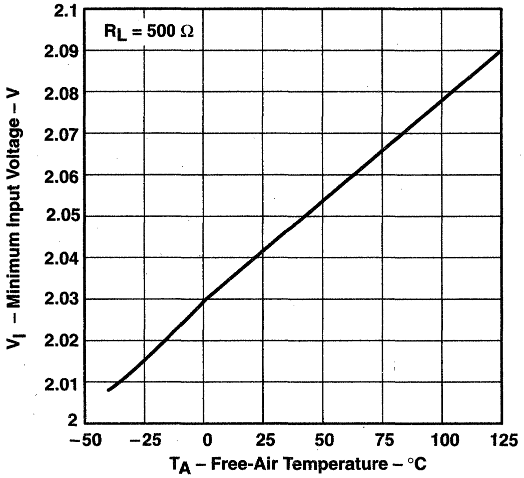

Figure 29

MINIMUM INPUT VOLTAGE FOR VALID POWER GOOD (PG) vs FREE-AIR TEMPERATURE

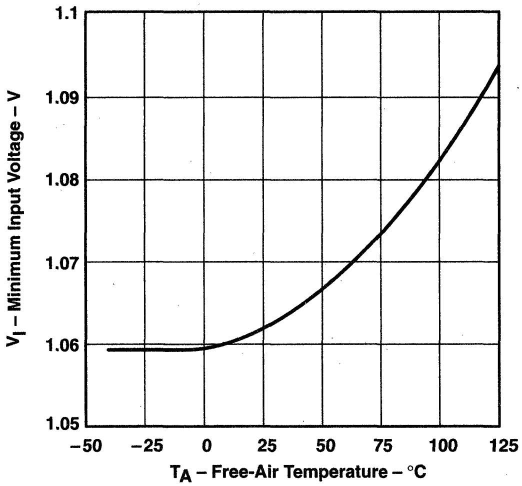

Figure 30

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

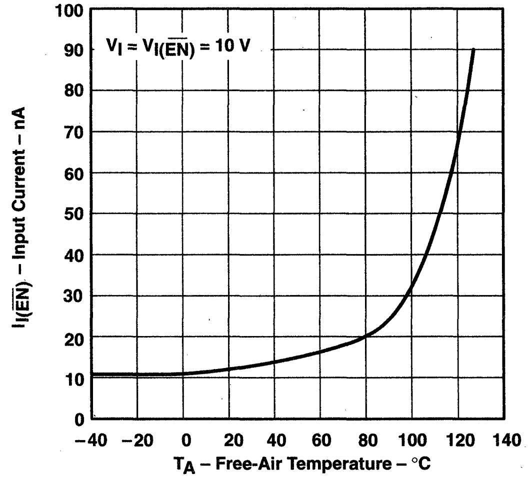

Figure 31

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE ($\overline{EN}$)

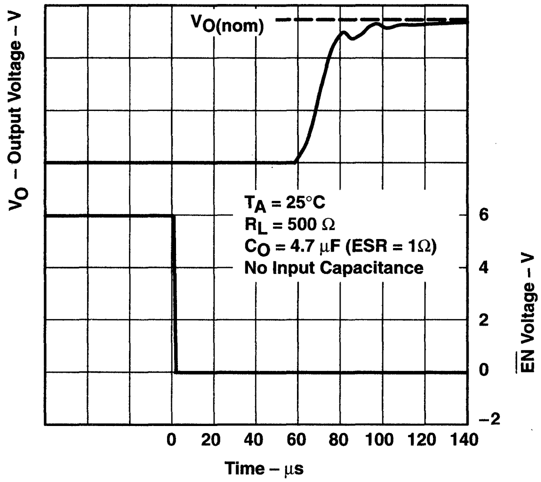

Figure 32

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

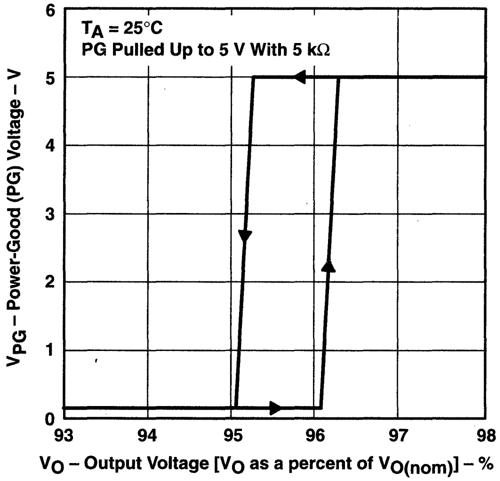

Figure 33

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY TOTAL ESR vs OUTPUT CURRENT

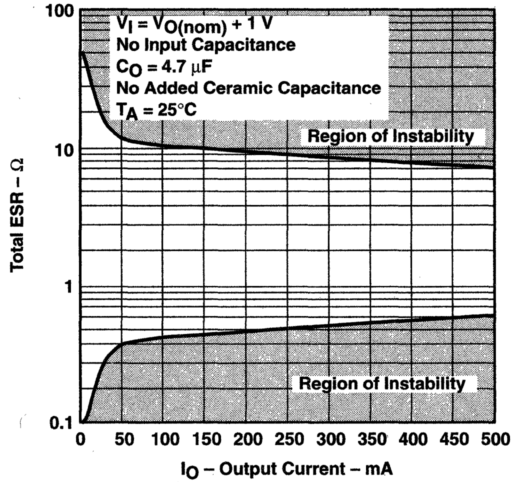

Figure 34

TYPICAL REGIONS OF STABILITY TOTAL ESR vs OUTPUT CURRENT

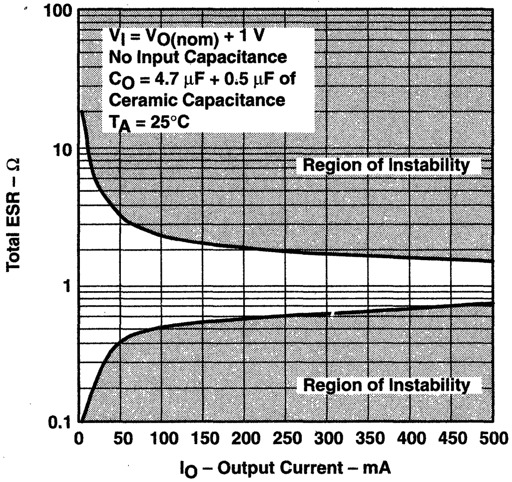

Figure 35

TYPICAL REGIONS OF STABILITY TOTAL ESR vs ADDED CERAMIC CAPACITANCE

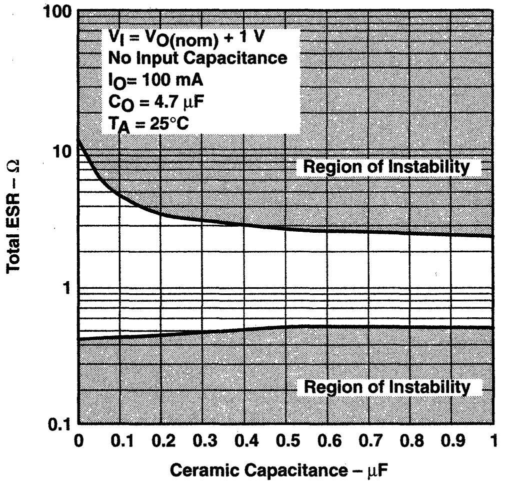

Figure 36

TYPICAL REGIONS OF STABILITY TOTAL ESR vs ADDED CERAMIC CAPACITANCE

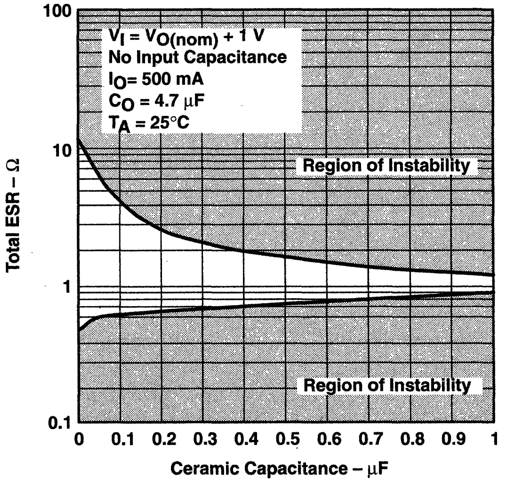

Figure 37

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

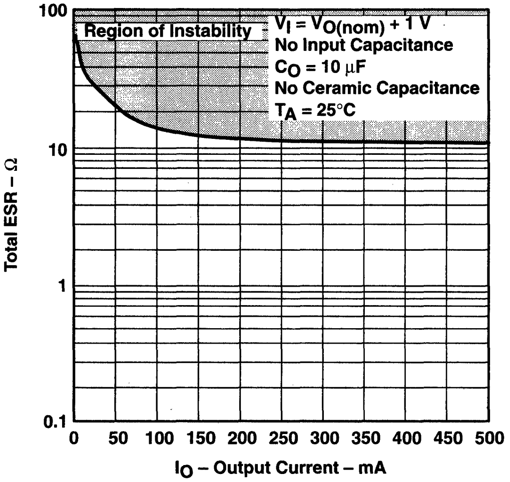

Figure 38

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

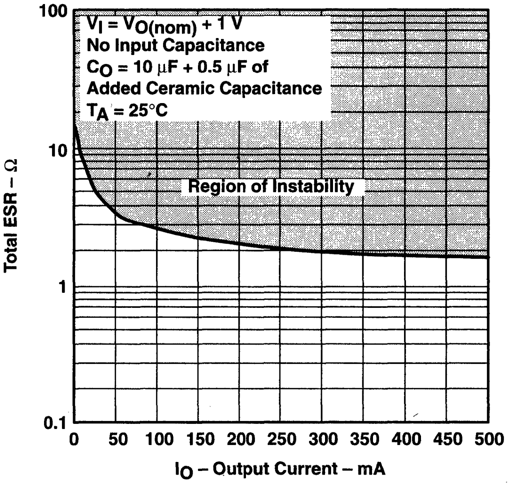

Figure 39

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

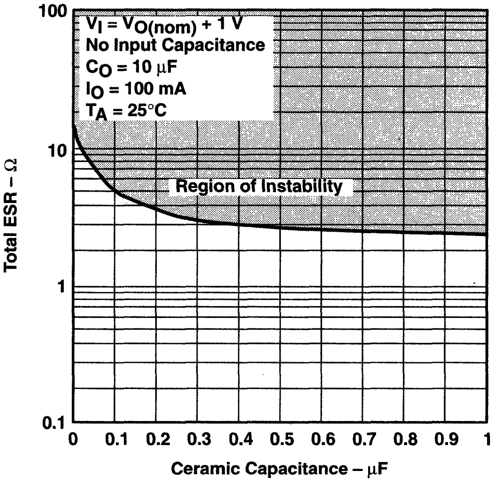

Figure 40

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

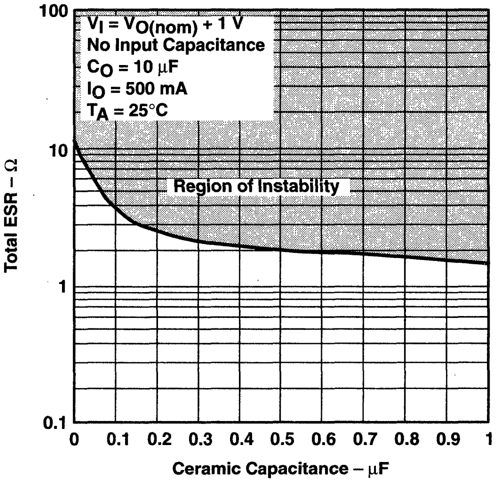

Figure 41

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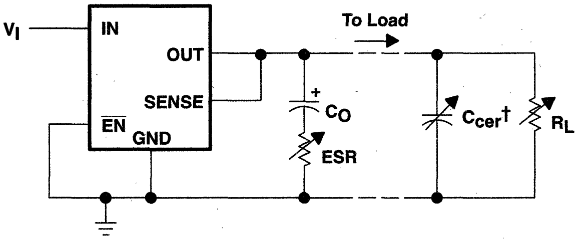
† ESR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS



† Ceramic capacitor

Figure 42. Test Circuit for Typical Regions of Stability (Figures 39 through 46)

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 43 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 44. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 45 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m · °C.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature, (i.e., 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation).

This limit should then be applied to the internal power dissipated by the TPS71xx regulator. The equation for calculating total internal power dissipation of the TPS71xx is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS71xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55°C$, airflow = 100 ft/min, copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 45, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS7148 regulator where $V_I = 6$ V and $I_O = 385$ mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

THERMAL INFORMATION

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

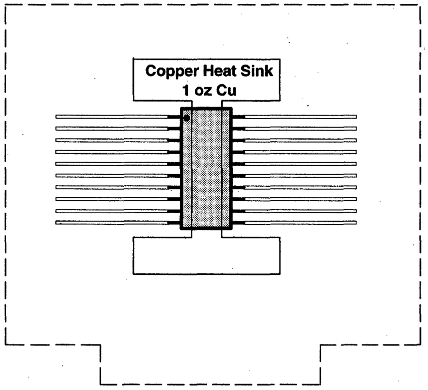


Figure 43. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

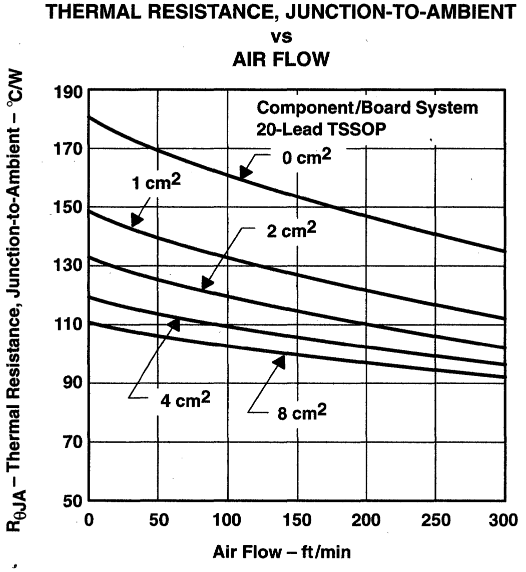

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
vs
AIR FLOW

Figure 44

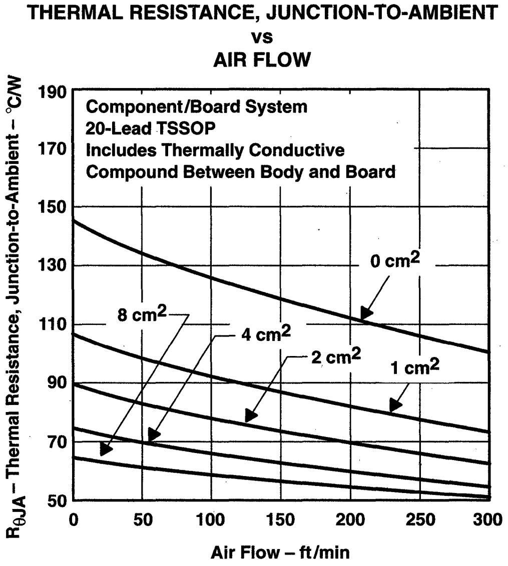

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
vs
AIR FLOW

Figure 45

APPLICATION INFORMATION

The TPS71xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71xx family includes three fixed-output voltage regulators: the TPS7133 (3.3 V), the TPS7148 (4.85 V), and the TPS7150 (5 V). The family also offers an adjustable device, the TPS7101 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71xx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71xx family is a 4.85-V regulator, the TPS7148. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS71xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection if the TPS71xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS71xx family requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 46). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figures 34 through 41 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 34 through 41), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71xx family. This information (along with the ESR graphs, Figures 34 through 41) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

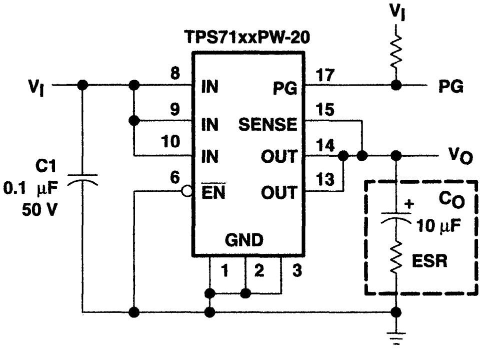


Figure 46. Typical Application Circuit

programming the TPS7101 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 9. The equation governing the output voltage is:

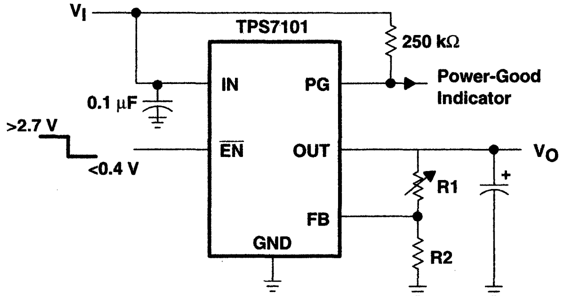
$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

V_{ref} = reference voltage, 1.178 V typ

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 47. TPS7101 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power-good indicator

The TPS71xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS71xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting may be appropriate.

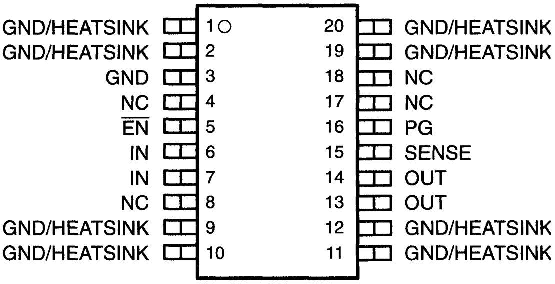
The TPS71xx also features internal current limiting and thermal protection. During normal operation, the TPS71xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TPS7133QPWP, TPS7133Y
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS101A – FEBRUARY 1995 – REVISED AUGUST 1995

- **Thermally Enhanced Surface-Mount Package (PWP)**
- **High-Current (500-mA) LDO Regulator**
- **Very Low-Dropout Voltage . . . Maximum of 60 mV at I_O = 100 mA**
- **Extremely Low Sleep-State Current 0.5 µA Max**
- **2% Output-Voltage Tolerance Over Full Range of Load, Line, and Temperature**
- **Output Current Range of 0 mA to 500 mA**
- **Power Good (PG) Status Output**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS7133QPWP is a micropower low-dropout (LDO) voltage regulator with a fixed 3.3-V output voltage, rated for loads up to 500 mA. The device is ideal for applications that require 3.3 V from a 5-V supply, or a constant output from a battery, such as alkaline or lithium ion, that drops off considerably in voltage as it discharges.

To maximize the advantage of its high-output-current capability, the TPS7133QPWP is now offered in a new thermally enhanced surface-mount power package. Designed to the same dimensions as the 20-pin TSSOP (just 1.2 mm high), the part has an innovative thermal pad, which, when soldered to the printed-wiring board (PWB), enables the device to dissipate several watts of power (see Figure 1 and Thermal Information section).

Using a PMOS transistor as the pass element keeps the quiescent current very low and constant, independent of output loading (typically 270 µA over the full range of output current, 0 mA to 500 mA). Because the PMOS device also behaves as a low-value resistor, the dropout is very low – maximum of 60 mV at 100 mA. These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO also features a sleep mode; applying a TTL high signal to $\overline{EN}$ shuts down the regulator, reducing the quiescent current to 0.5 µA.

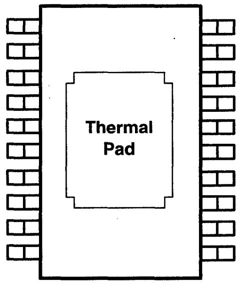


Figure 1. Bottom View of PWP Package, Showing the Thermal Pad

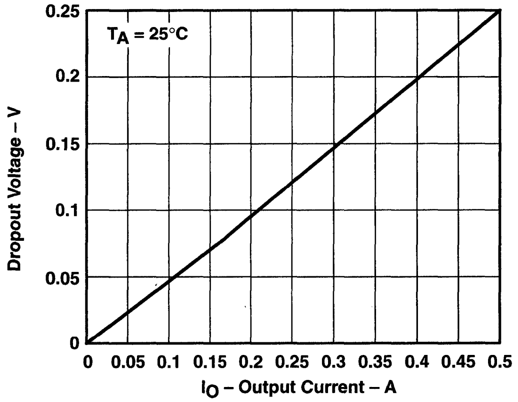
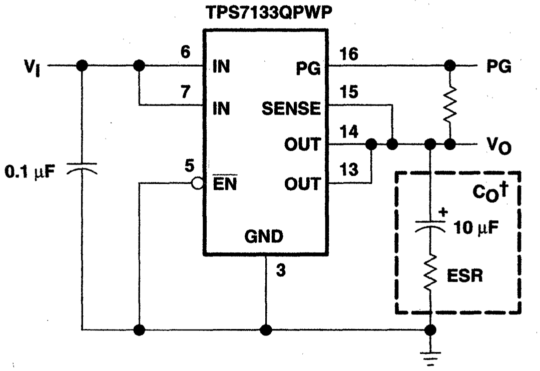


Figure 2. Typical Dropout Voltage Versus Output Current

AVAILABLE OPTIONS†

T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES	CHIP FORM (Y)
	MIN	TYP	MAX	THERMALLY-ENHANCED TSSOP (PWP)	
–55°C to 150°C	3.23	3.3	3.37	TPS7133QPWPPWPLE	TPS7133Y

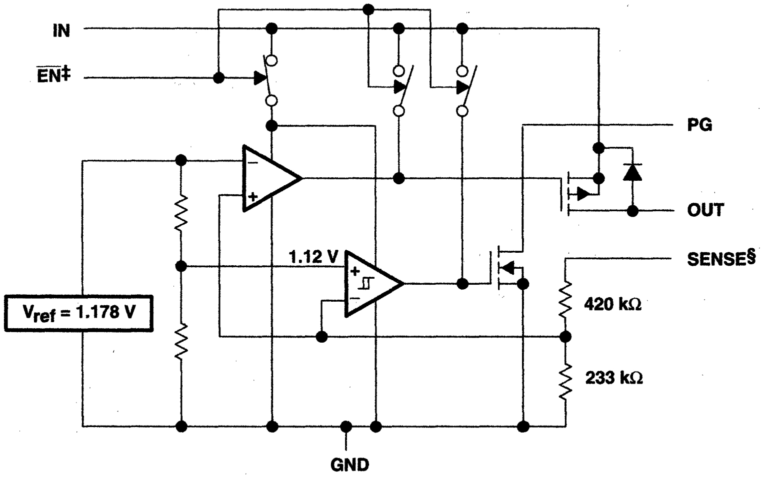
† The PWP package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS7133QPWPLE). The chip form is tested at 25°C.



† Capacitor selection is nontrivial. See application information section for details.

Figure 3. Typical Application Configuration

functional block diagram



Resistors are nominal values only.

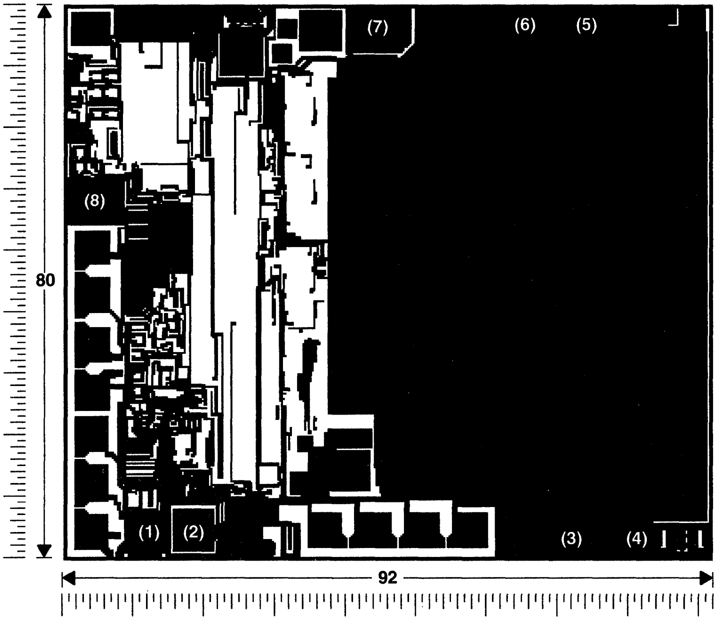
‡ Switch positions shown with EN active low.

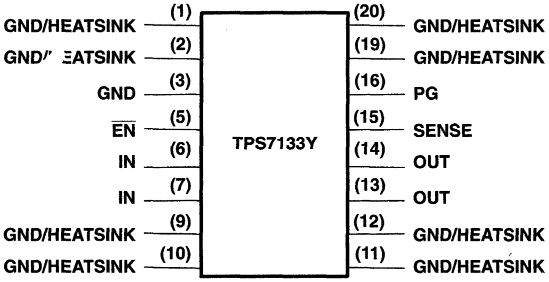
§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

TPS7133Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS7133QPWP. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

TERMINALS 4, 8, 17, AND 18 ARE NOT CONNECTED

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I, PG, SENSE, $\overline{EN}$	−0.3 to 10 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	−55°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 4)§

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 5)§

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	7.1 W

MAXIMUM CONTINUOUS DISSIPATION§
vs
FREE-AIR TEMPERATURE

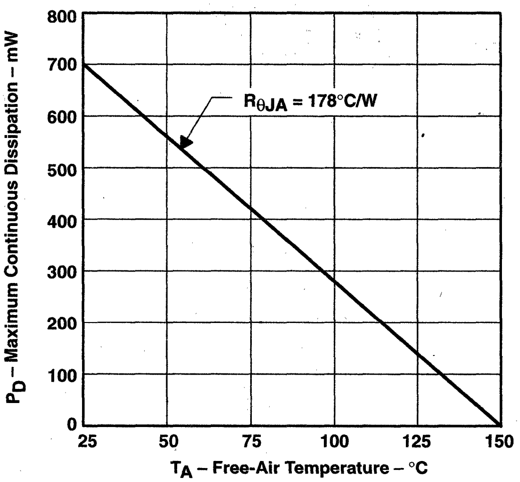
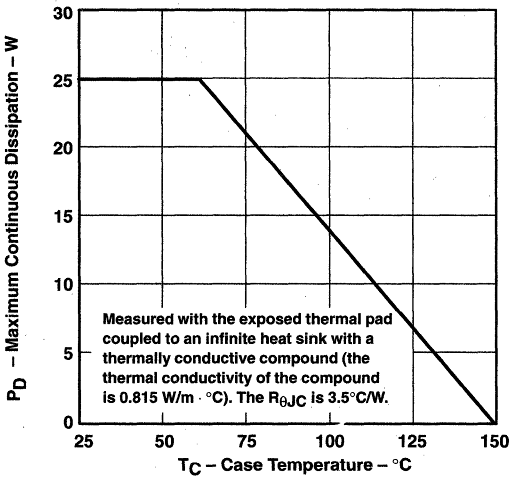


Figure 4

MAXIMUM CONTINUOUS DISSIPATION§
vs
CASE TEMPERATURE



Measured with the exposed thermal pad coupled to an infinite heat sink with a thermally conductive compound (the thermal conductivity of the compound is 0.815 W/m · °C). The $R_{\theta JC}$ is 3.5°C/W.

Figure 5

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I[†]	3.77	10	V
High-level input voltage at $\overline{EN}$, V_{IH}	2		V
Low-level input voltage at $\overline{EN}$, V_{IL}		0.5	V
Output current range, I_O	0	500	mA
Operating virtual junction temperature range, T_J	−40	125	°C

[†] Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage V_{DO}[‡] at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

[‡] This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

electrical characteristics at $I_O = 10$ mA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF/ESR[‡] = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS[§]	T_J	TPS7133QPWP			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 ≤ I_O ≤ 500 mA	25°C		285	350	µA
		−40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			2	
Output current limit	$V_O = 0$, $V_I = 10$ V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			1	
PG leakage current	Normal operation, $V_{PG} = 10$ V	25°C		0.02	0.5	µA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 ≤ V_I ≤ 10 V	25°C	−0.5		0.5	µA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	$I_{PG} = 300$ µA	25°C		1.06	1.5	V
		−40°C to 125°C			1.9	

[§] ESR refers to the equivalent series resistance, including internal and external resistance.

[¶] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at $I_O = 10$ mA, $V_I = 4.3$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ μF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7133QPWP			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4.3$ V,	$I_O = 10$ mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	$I_O = 10$ mA,	$V_I = 3.23$ V	25°C		0.02	6	mV
			−40°C to 125°C			8	
	$I_O = 100$ mA,	$V_I = 3.23$ V	25°C		47	60	
			−40°C to 125°C			80	
	$I_O = 500$ mA,	$V_I = 3.23$ V	25°C		235	300	
			−40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V_O)/I_O, $I_O = 500$ mA	$V_I = 3.23$ V,	25°C		0.47	0.6	Ω
			−40°C to 125°C			0.8	
Input voltage regulation	$V_I = 4.3$ V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			20	mV
			−40°C to 125°C			27	
Output voltage regulation	$I_O = 5$ mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			−40°C to 125°C			75	
	$I_O = 50$ μA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	$I_O = 50$ μA	25°C	43	54		dB
			−40°C to 125°C	40			
		$I_O = 500$ mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	$C_O = 4.7$ μF	25°C		274		μVrms
		$C_O = 10$ μF	25°C		228		
		$C_O = 100$ μF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	$I_{PG} = 1$ mA,	$V_I = 2.8$ V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

† ESR refers to the equivalent series resistance, including internal and external resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR‡ = 1 Ω, T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	TPS7133Y MIN	TPS7133Y TYP	TPS7133Y MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, $0 \le I_O \le 500$ mA		285		μA
Output current limit	V_O = 0, V_I = 10 V		1.2		A
PG leakage current	Normal operation, V_{PG} = 10 V		0.02		μA
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ hysteresis voltage			50		mV
Minimum V_I for active pass element			2.05		V
Minimum V_I for valid PG	I_{PG} = 300 μA		1.06		V

§ ESR refers to the equivalent series resistance, including internal and external resistance.

¶ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7133Y MIN	TPS7133Y TYP	TPS7133Y MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V		0.02		mV
	I_O = 100 mA,	V_I = 3.23 V		47		
	I_O = 500 mA,	V_I = 3.23 V		235		
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, I_O = 500 mA	V_I = 3.23 V,		0.47		Ω
Output voltage regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V		21		mV
	I_O = 50 μA to 500 mA,	4.3 V ≤ V_I ≤ 10 V		30		mV
Ripple rejection	f = 120 Hz	I_O = 50 μA		54		dB
		I_O = 500 mA		49		
Output noise-spectral density	f = 120 Hz			2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 μF		274		μVrms
		C_O = 10 μF		228		
		C_O = 100 μF		159		
PG hysteresis voltage				35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V		0.22		V

† ESR refers to the equivalent series resistance, including internal and external resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	6
		vs Input voltage	7
		vs Free-air temperature	8
V_{DO}	Typical dropout voltage	vs Output current	9
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	10
ΔV_O	Change in output voltage	vs Free-air temperature	11
V_O	Output voltage	vs Input voltage	12
ΔV_O	Change in output voltage	vs Input voltage	13
V_O	Output voltage	vs Output current	14
	Ripple rejection	vs Frequency	15
	Output special noise density	vs Frequency	16
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	17
R	Divider resistance	vs Free-air temperature	18
$I_{I(SENSE)}$	SENSE pin current	vs Free-air temperature	19
V_I	Minimum input voltage (active-pass element)	vs Free-air temperature	20
	Minimum input voltage (valid PG)	vs Free-air temperature	21
$I_{I(EN)}$	$\overline{EN}$ Input current	vs Free-air temperature	22
	Output voltage response from Enable ($\overline{EN}$)		23
V_{PG}	Power-good (PG) voltage	vs Output voltage	24
	Total ESR	vs Output current	25
			26
	Total ESR	vs Added ceramic capacitance	27
			28
	Total ESR	vs Output current	29
			30
	Total ESR	vs Added ceramic capacitance	31
			32

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs OUTPUT CURRENT

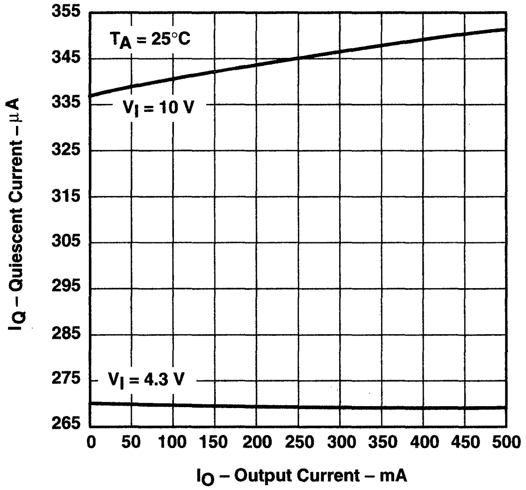


Figure 6

QUIESCENT CURRENT vs INPUT VOLTAGE

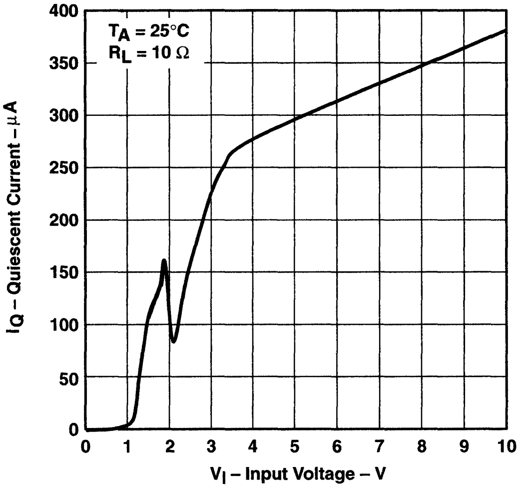


Figure 7

QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

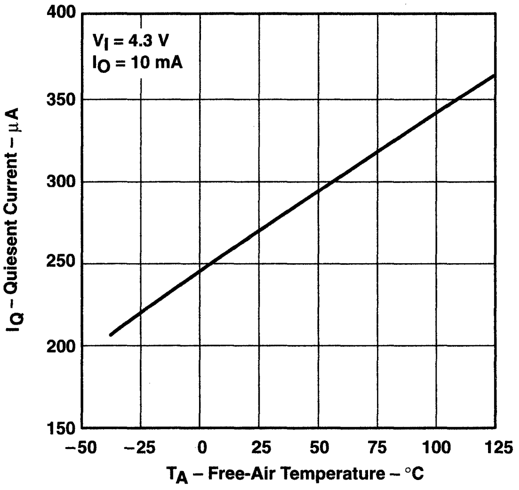


Figure 8

DROPOUT VOLTAGE vs OUTPUT CURRENT

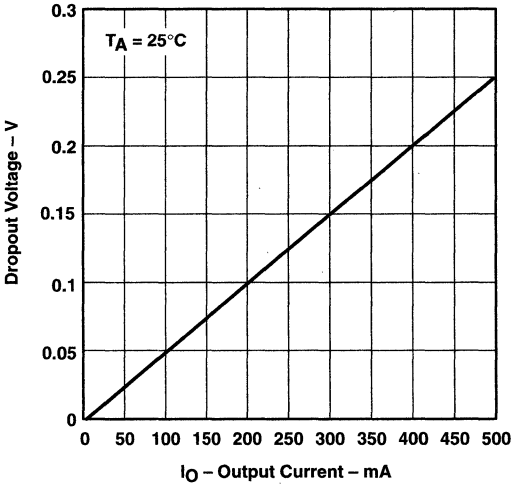


Figure 9

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

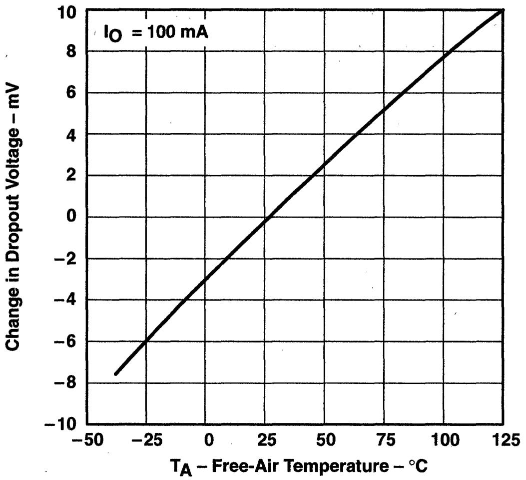


Figure 10

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

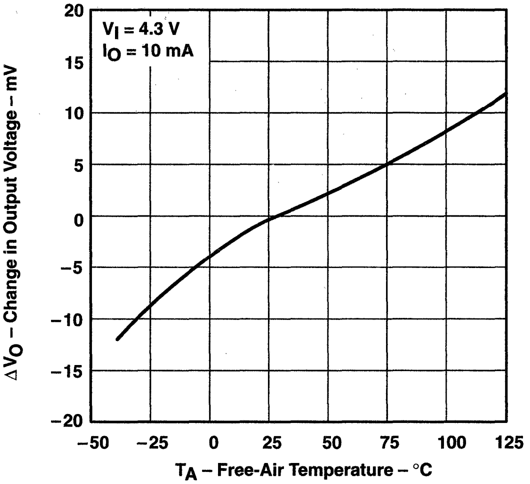


Figure 11

OUTPUT VOLTAGE vs INPUT VOLTAGE

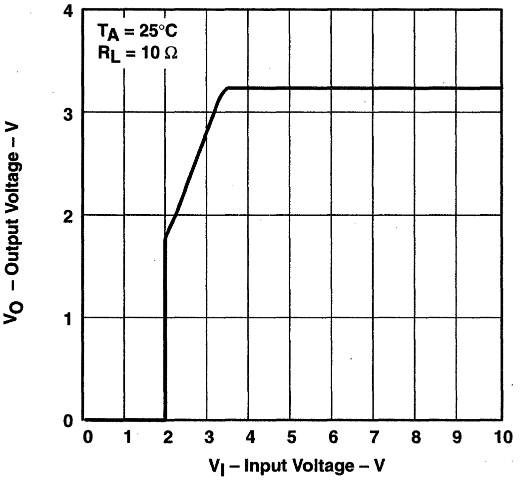


Figure 12

CHANGE IN OUTPUT VOLTAGE vs INPUT VOLTAGE

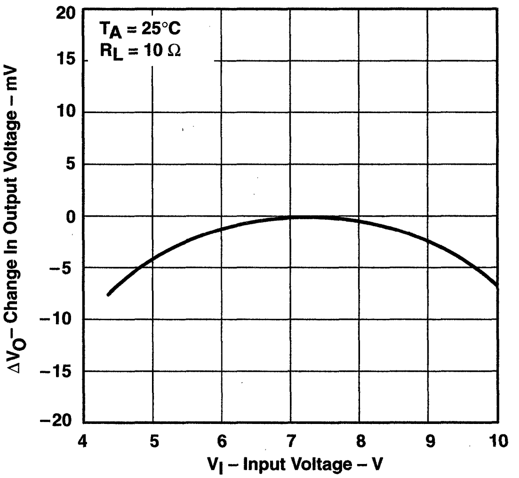


Figure 13

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

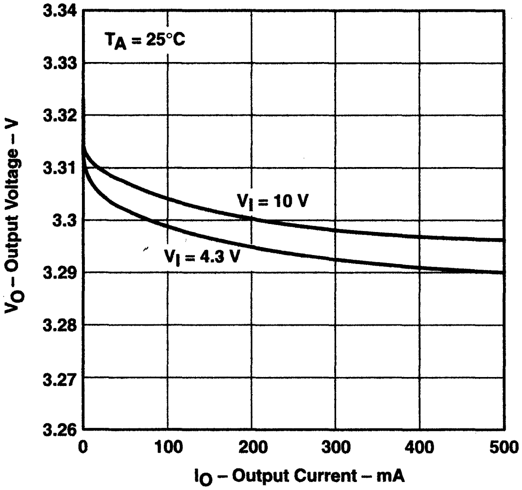


Figure 14

RIPPLE REJECTION vs FREQUENCY

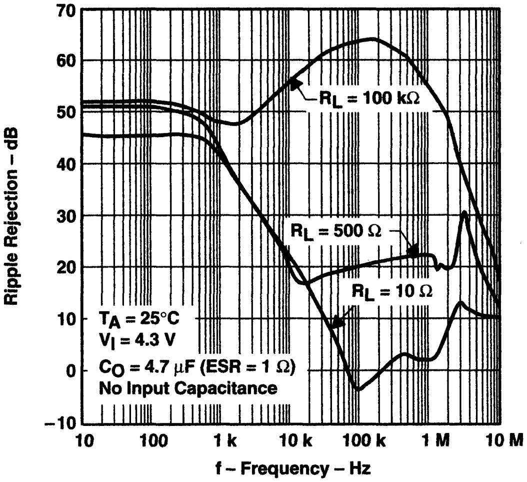


Figure 15

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

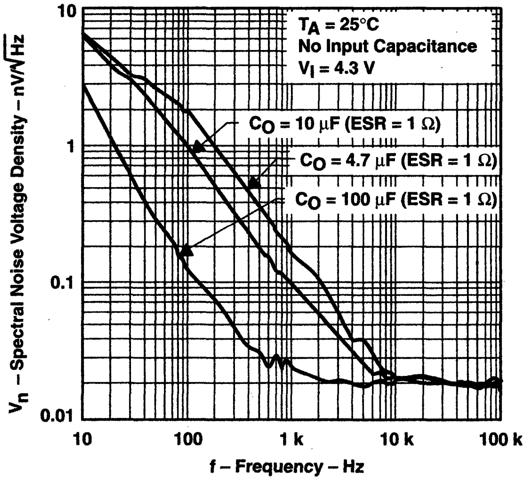


Figure 16

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

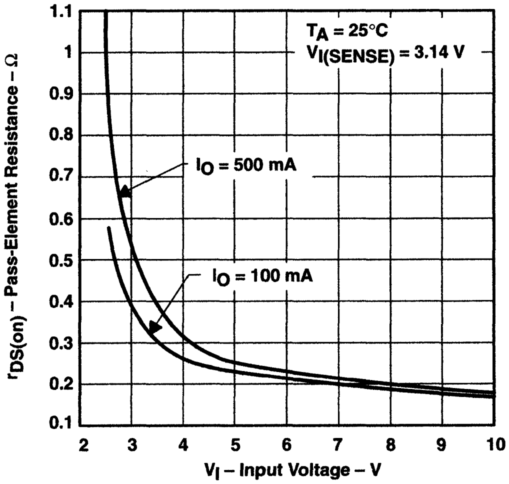


Figure 17

TYPICAL CHARACTERISTICS

DIVIDER RESISTANCE
vs
FREE-AIR TEMPERATURE

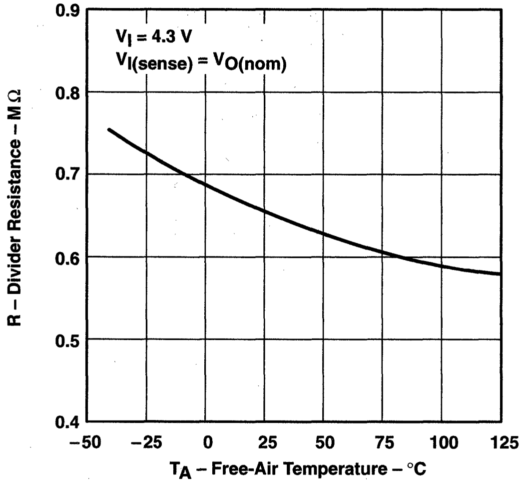


Figure 18

SENSE PIN CURRENT
vs
FREE-AIR TEMPERATURE

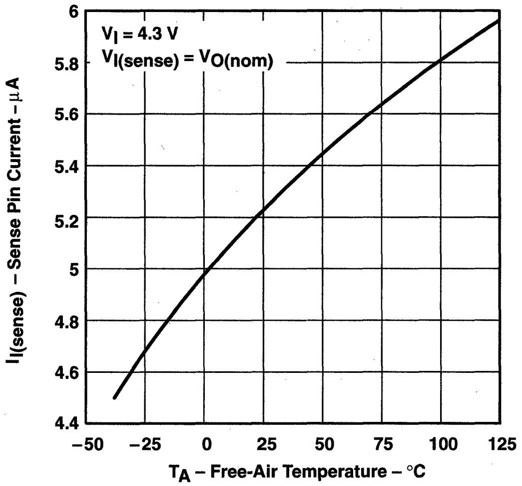


Figure 19

MINIMUM INPUT VOLTAGE
(ACTIVE PASS ELEMENT)
vs
FREE-AIR TEMPERATURE

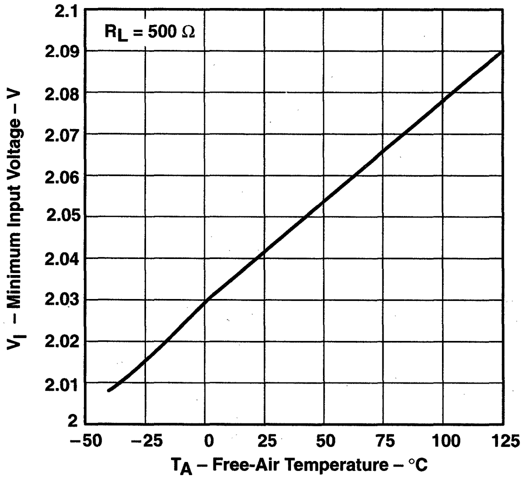


Figure 20

MINIMUM INPUT VOLTAGE
(VALID PG)
vs
FREE-AIR TEMPERATURE

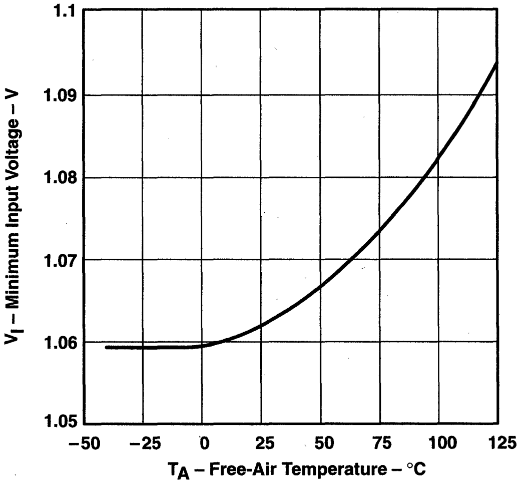


Figure 21

TYPICAL CHARACTERISTICS

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

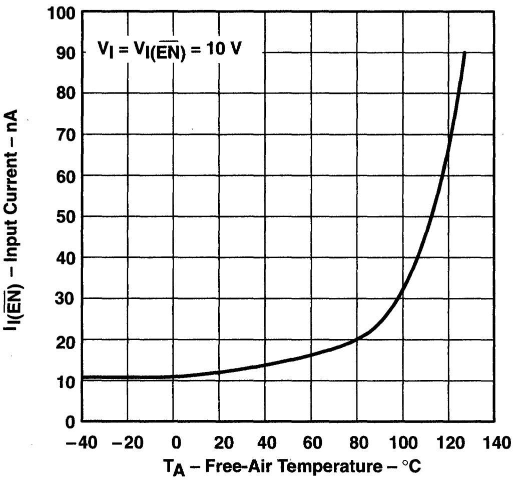


Figure 22

OUTPUT VOLTAGE RESPONSE FROM ENABLE ($\overline{EN}$)

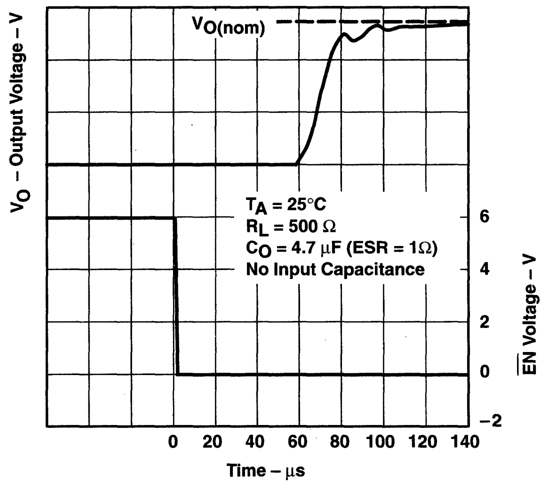


Figure 23

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

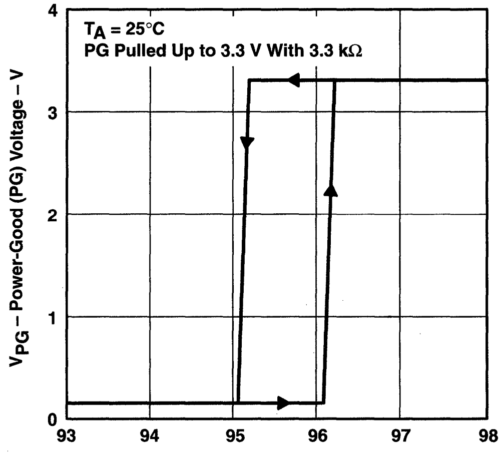


Figure 24

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT

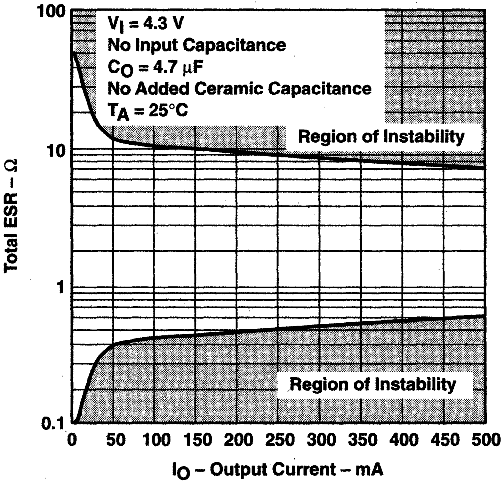


Figure 25

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT

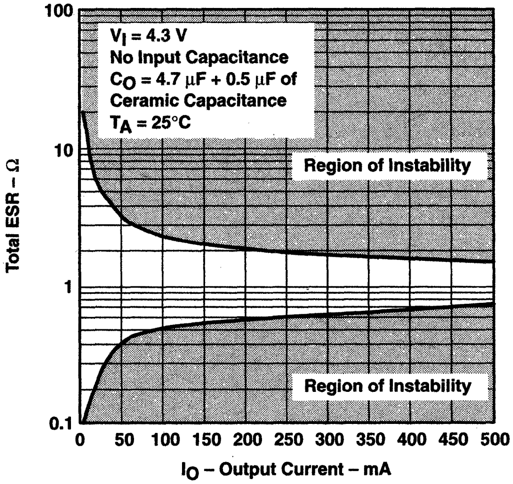


Figure 26

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

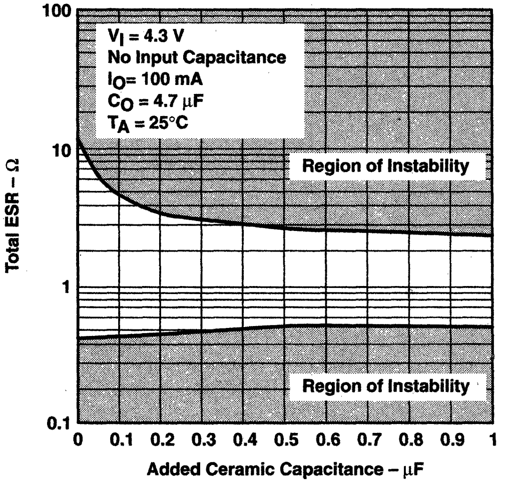


Figure 27

TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

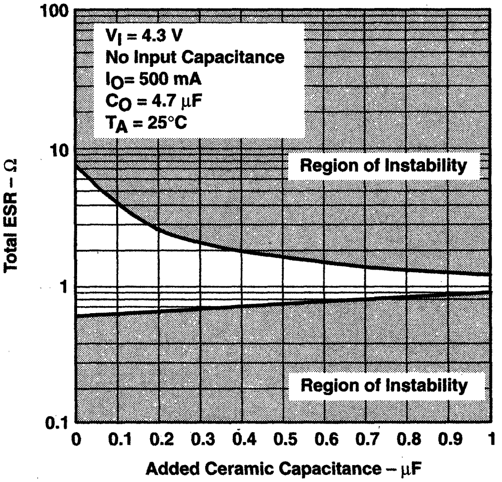


Figure 28

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

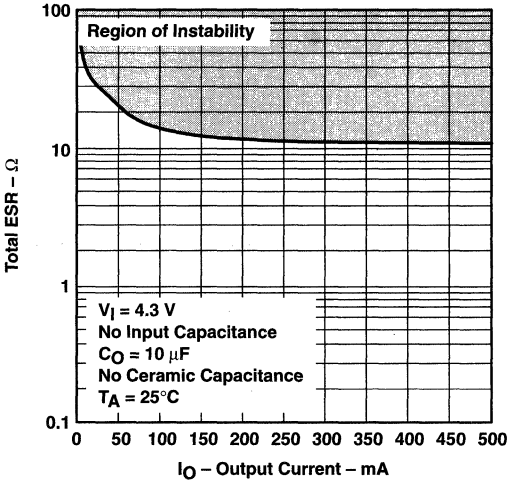


Figure 29

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

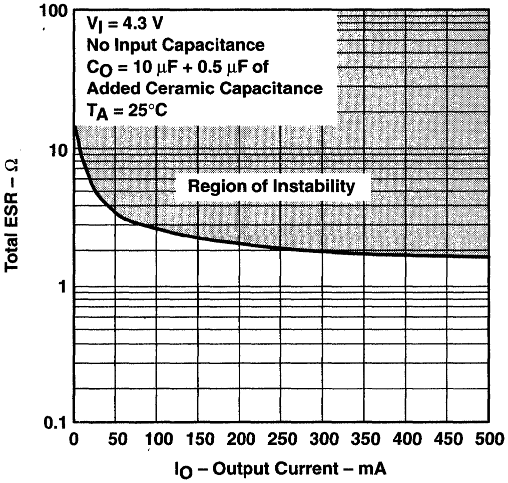


Figure 30

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

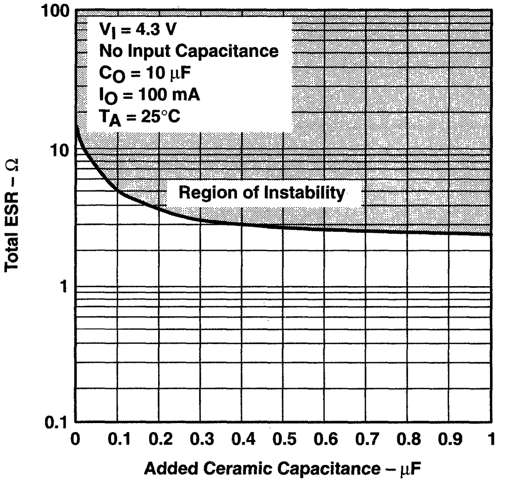


Figure 31

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

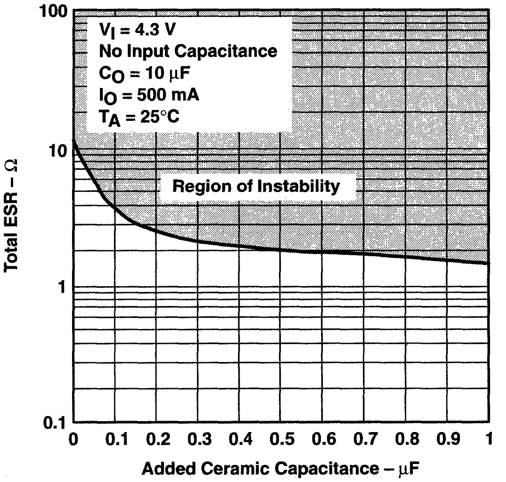


Figure 32

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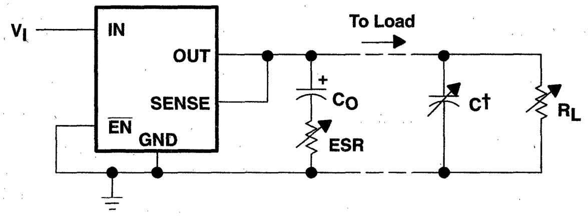
† ESR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS



† Ceramic capacitor

Figure 33. Test Circuit for Typical Regions of Stability (Figures 25 through 32)

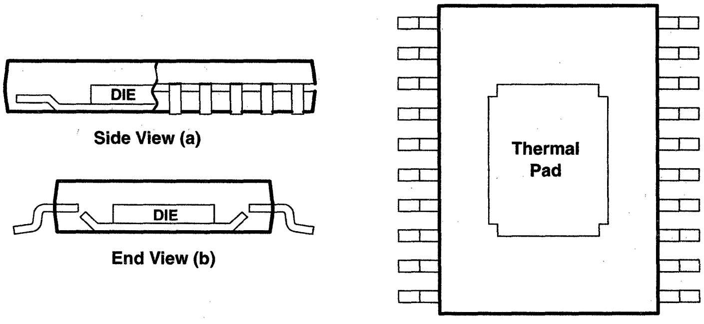
THERMAL INFORMATION

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 34(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.



Side View (a)

End View (b)

Bottom View (c)

Figure 34. Views of Thermally Enhanced PWP Package

THERMAL INFORMATION

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 36(a), 8 cm^2 of Cu heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 35 and 36). The line drawn at 0.3 cm^2 in Figures 35 and 36 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 38.

The thermal pad is directly connected to the substrate of the IC, which for the TPS7133QPWP is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWB can be a ground plane or left electrically isolated. In other TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 12 independent leads that can be used as inputs and outputs (Note: leads 1, 2, 9, 10, 11, 12, 19, and 20 are internally connected to the thermal pad and the IC substrate).

THERMAL RESISTANCE
vs
COPPER HEAT-SINK AREA

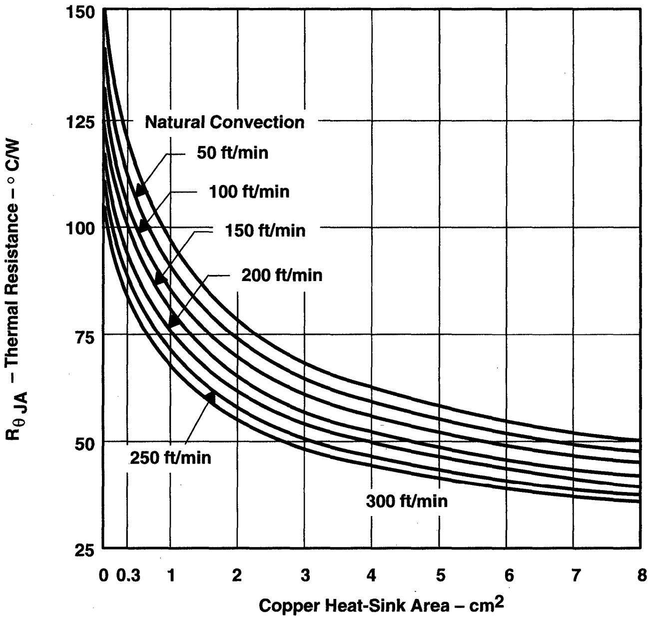
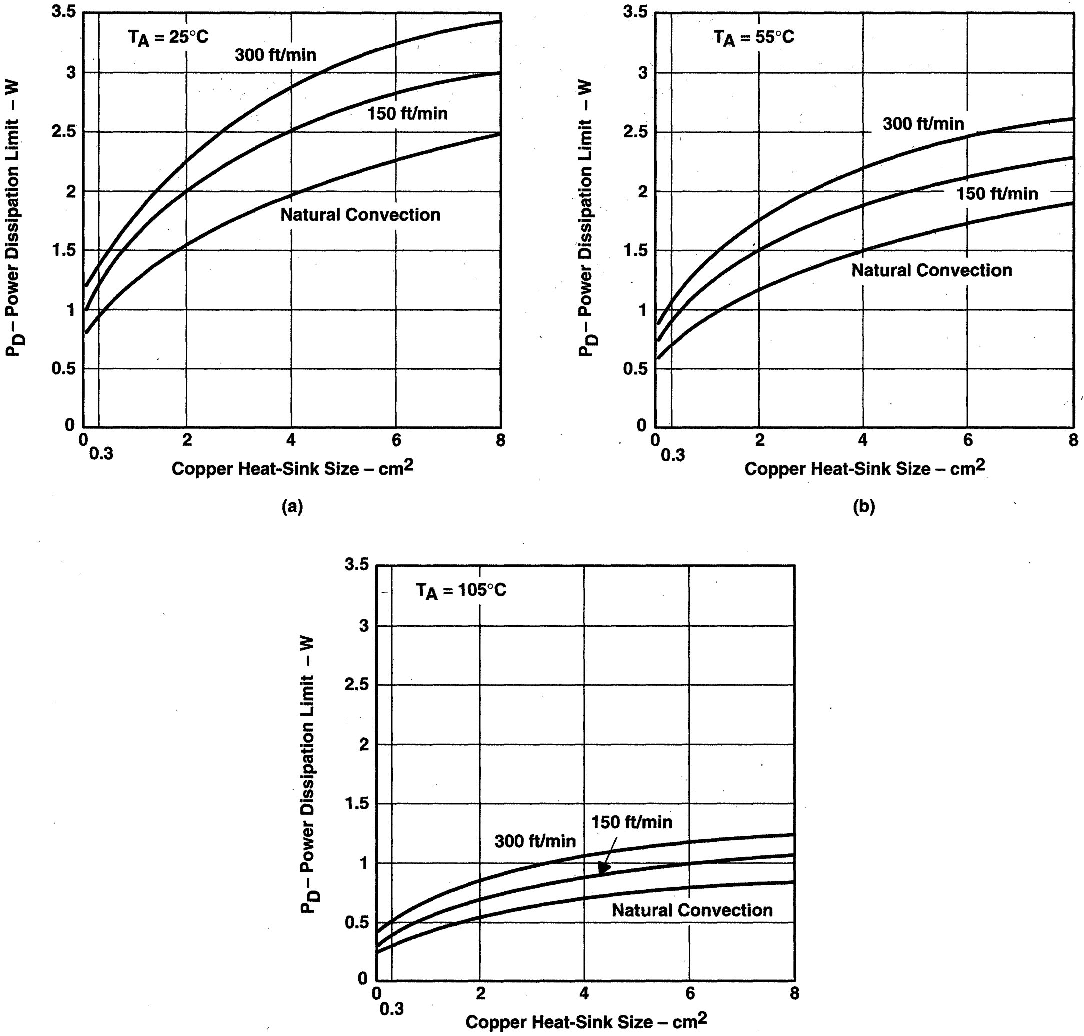


Figure 35

THERMAL INFORMATION



(a)

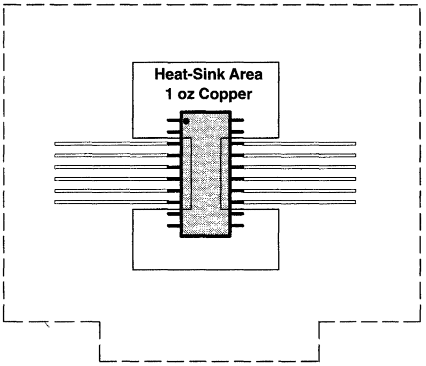
(b)

(c)

Figure 36. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

THERMAL INFORMATION

Figure 37 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figures 35 and 36. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 35 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils
Board size	3.2 in. × 3.2 in.
Board material	FR4
Cu trace/heat sink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 37. PWB Layout (Including Cu Heatsink Area) for Thermally Enhanced PWP Package

From Figure 35, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}}$$

Where

$T_J$max is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS7133QPWP regulator. The equation for calculating total internal power dissipation of the TPS7133QPWP is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Since the quiescent current of the TPS7133QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

For the case where T_A = 55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 35, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{50°C/W} = 1.4\ W$$

If the system implements a TPS7133QPWP regulator, where $V_I = 6$ V and $I_O = 500$ mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 3.3) \cdot 0.5 = 1.35\ \text{W}$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

Since the thermal pad is not a primary connection for an electrical signal, the importance of the electrical connection is not significant. The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 35 and 36 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 38 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 2, 9, 10, 11, 12, 19, and 20.

reliability information

This section includes demonstrated reliability test results obtained from the qualification program. Accelerated tests are performed at high-stress conditions so that product reliability can be established during a relatively short test duration. Specific stress conditions are chosen to represent accelerated versions of various device-application environments and allow meaningful extrapolation to normal operating conditions.

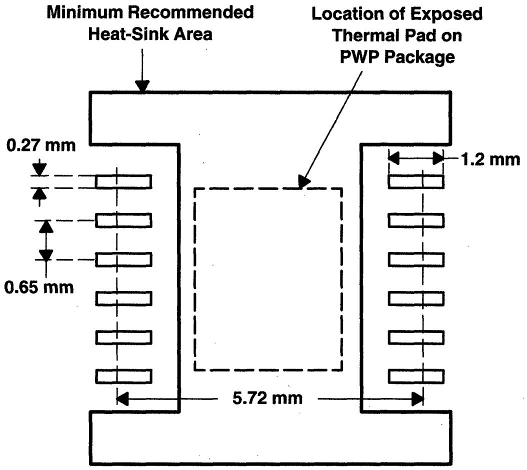


Figure 38. PWP Package Land Pattern

THERMAL INFORMATION

component level reliability test results

preconditioning

Preconditioning of components prior to reliability testing is employed to simulate the actual board assembly process used by the customer. This ensures that reliability test results are more representative of those that would be seen in the final application. The general form of the preconditioning sequence includes a moisture soak followed by multiple vapor-phase-reflow or infrared-reflow solder exposures. All components used in the following reliability tests were preconditioned in accordance with JEDEC Test Method A113 for Level 1 (not moisture-sensitive) products.

high-temperature life test

High-temperature life testing is used to demonstrate long-term reliability of the product under bias. The potential failure mechanisms evaluated with this stress are those associated with dielectric integrity and design or process sensitivity to mobile-ion phenomena. Components are tested at an elevated ambient temperature of 155°C for an extended period. Results are derated using the Arrhenius equation to an equivalent number of unit hours at a representative application temperature. The corresponding predicted failure rate is expressed in FITs, or failures per billion device-hours. The failure rate shown in this case is data-limited since no actual failures were experienced during qualification testing.

PREDICTED LONG-TERM FAILURE RATE		
Number of Units	Equivalent Unit Hours at 55°C and 0.7 eV	FITs at 50% CL
325	24,468,090	36.2

biased humidity test

Biased humidity testing is used to evaluate the effects of moisture penetration on plastic-encapsulated devices under bias. This stress verifies the integrity of the package construction and the die passivation system. The primary potential failure mechanism is electrolytic corrosion. Components are biased in a low power state to reduce heat dissipation and are subjected to a 120°C, 85%-relative-humidity environment for 100 hours.

BIASED HUMIDITY TEST RESULTS	
Equivalent Unit Hours at 85°C and 85% RH	Failures
357,000	0

autoclave test

The autoclave stress is used to assess the capabilities of the die and package construction materials with respect to moisture ingress and extended exposure. Predominant failure mechanisms include leakage currents that result from internal moisture accumulation and galvanic corrosion resulting from reactions with any present ionic contaminants. Components are subjected to a 121°C, 15 PSIG, 100%-relative-humidity environment for 240 hours.

AUTOCLAVE TEST RESULTS	
Total Unit Hours	Failures
54,720	0

THERMAL INFORMATION

thermal shock test

Thermal shock testing is used to evaluate the capability of the component to withstand mechanical stress resulting from differences in thermal coefficients of expansion among the die and package construction materials. Failure mechanisms are typically related to physical damage at interface locations between different materials. Components are cycled between –65°C and 150°C in liquid mediums for a total duration of 1000 cycles.

THERMAL SHOCK TEST RESULTS	
Total Unit Cycles	Failures
345,000	0

PWB assembly level reliability results

temperature cycle test

Temperature cycle testing of the PWB assembly is used to evaluate the capability of the assembly to withstand mechanical stress resulting from the differences in thermal coefficients of expansion among die, package, and PWB board materials. This testing is also used to sufficiently age the soldered thermal connection between the thermal pad and the Cu trace on the FR4 board and evaluate the degradation of the thermal resistance for a board-mounted test unit. The assemblies were cycled between temperature extremes of –40°C and 125°C for a total duration of 730 cycles.

TEMPERATURE CYCLE TEST RESULTS		
Total Unit Cycles	Failures	Average Change in $R_{\theta JA(system)}$
36,500	0	–0.41%

solderability test

Solderability testing is used to simulate actual board-mount performance in a reflow process.

Solderability testing is conducted as follows: The test devices are first steam-aged for 8 hours. A stencil is used to apply a solder-paste terminal pattern on a ceramic substrate (nominal stencil thickness is 0.005 inch). The test units are manually placed on the solder-paste footprint with proper implements to avoid contamination. The ceramic substrate and components are subjected to the IR reflow process as follows:

IR REFLOW PROCESS

	PREHEAT SOAK	REFLOW
Temperature	150°C to 170°C	215°C to 230°C
Time	60 sec	60 sec

After cooling to room temperature, the component is removed from the ceramic substrate and the component terminals are subjected to visual inspection at 10X magnification.

Test results are acceptable if all terminations exhibit a continuous solder coating free of defects for a minimum 95% of the critical surface area of any individual termination. Causes for rejection include: dewetting, nonwetting, and pin holes. The component leads and the exposed thermal pad were evaluated against this criteria.

SOLDERABILITY TEST RESULTS	
Number of Test Units	Failures
22	0

X-ray test

X-ray testing is used to examine and quantify the voiding of the soldered attachment between the thermal pad and the PWB copper trace. Voiding between 20% and 50% was observed on a 49-piece sample.

APPLICATION INFORMATION

The TPS7133QPWP low-dropout (LDO) regulator is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator.

device operation

The TPS7133QPWP, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent-current versus load-current curves. The TPS7133QPWP uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS7133QPWP specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS7133QPWP quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS7133QPWP also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA. $\overline{\text{EN}}$ is pulled down internally, requiring no external connection for continuous operation. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS7133QPWP is stable even at zero load; no minimum load is required for operation.

sense-pin connection

The SENSE pin must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047-pF to 0.1-μF) improves load transient response and noise rejection if the TPS7133QPWP is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS7133QPWP requires an output capacitor for stability. A low-ESR 10-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 39). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the

APPLICATION INFORMATION

AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 25 through 32 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μF), the output capacitance can be reduced to 4.7 μF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the ESR graphs (Figures 25 through 32), minimum ESR is not a problem when using 10-μF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS7133QPWP. This information (along with the ESR graphs, Figures 25 through 32) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

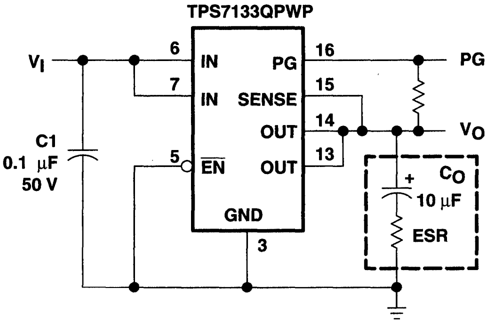


Figure 39. Typical Application Circuit

power-good indicator

The TPS7133QPWP features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS7133QPWP PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting may be appropriate.

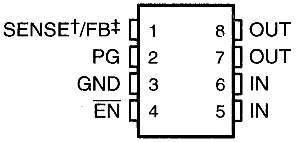
The TPS7133QPWP also features internal current limiting and thermal protection. During normal operation, the TPS7133QPWP limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TPS7201Q, TPS7233Q, TPS7248Q, TPS7250Q
TPS7201Y, TPS7233Y, TPS7248Y, TPS7250Y
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

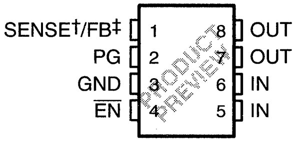
SLVS102C – MARCH 1995 – REVISED AUGUST 1995

- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Dropout Voltage <85 mV Max at I_O = 100 mA (TPS7250)**
- **Low Quiescent Current, Independent of Load, 155 μA Typ**
- **8-Pin SOIC and 8-Pin TSSOP Package (Product Preview)**
- **Output Regulated to ±2% Over Full Operating Range for Fixed-Output Versions**
- **Extremely Low Sleep-State Current, 0.5 μA Max**
- **Power-Good (PG) Status Output**

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



† SENSE – Fixed voltage options only (TPS7233, TPS7248, and TPS7250)
‡ FB – Adjustable version only (TPS7201)

description

The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and (product preview only) 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low – maximum of 85 mV at 100 mA of load current (TPS7250) – and is directly proportional to the load current (see Figure 1). Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 μA maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and micropower operation result in a significant increase in system battery operating life.

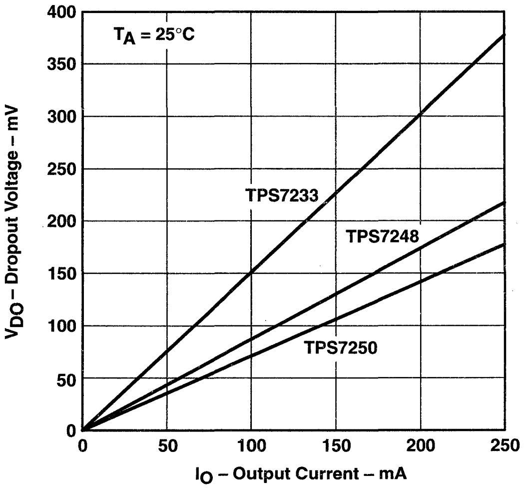


Figure 1. Typical Dropout Voltage Versus Output Current

AVAILABLE OPTIONS

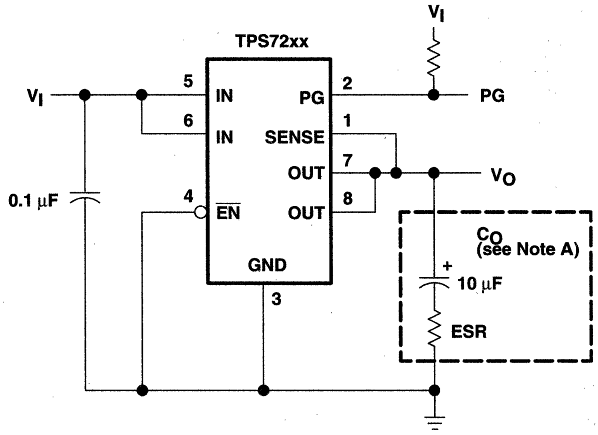
T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES		CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	TSSOP (PW)	
−55°C to 150°C	4.9	5	5.1	TPS7250QD	TPS7250QPWLE	TPS7250Y
	4.75	4.85	4.95	TPS7248QD	TPS7248QPWLE	TPS7248Y
	3.23	3.3	3.37	TPS7233QD	TPS7233QPWLE	TPS7233Y
	Adjustable§ 1.2 V to 9.75 V			TPS7201QD	TPS7201QPWLE	TPS7201Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7250QDR). The PW package is only available left-end taped and reeled. The TPS7201Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

description (continued)

The TPS72xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 0.5 μA maximum at $T_J = 25°C$. Other features include a power-good function that reports low output voltage and may be used to implement a power-on reset or a low-battery indicator.

The TPS72xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version).



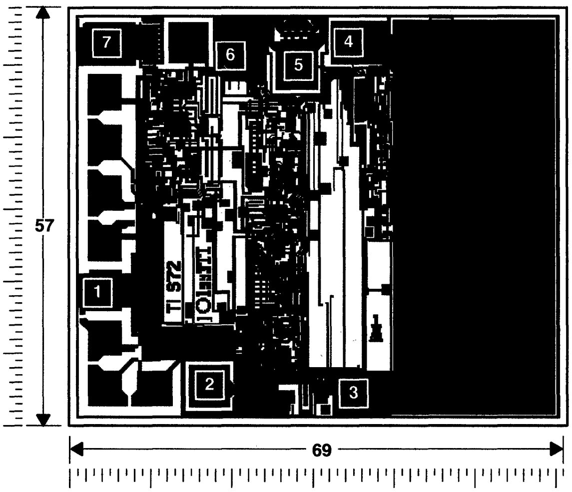
NOTE A. Capacitor selection is nontrivial. See application information section for details.

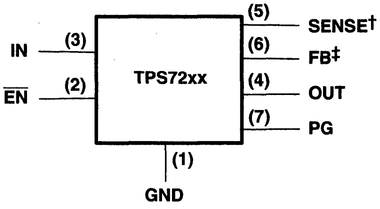
Figure 2. Typical Application Configuration

TPS72xx chip information

These chips, when properly assembled, display characteristics similar to the TPS72xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

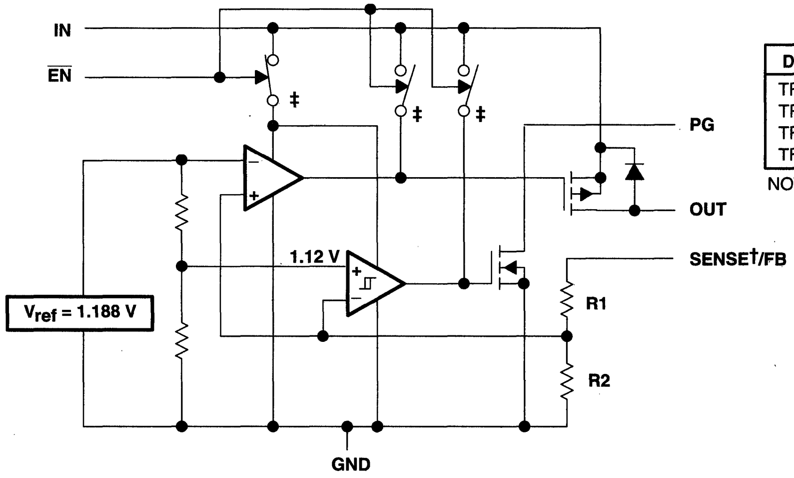
ALL DIMENSIONS ARE IN MILS.

† Fixed-voltage options only (TPS7233, TPS7248, and TPS7250)

‡ Adjustable version only (TPS7201)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the application information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7201	0	∞	Ω
TPS7233	420	233	kΩ
TPS7248	726	233	kΩ
TPS7250	756	233	kΩ

NOTE : Resistors are nominal values only.

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† For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to the SENSE-pin connection discussion in application information section.

‡ Switch positions are shown with EN low (active).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range[‡], V_I, PG, SENSE, $\overline{EN}$ . . . . –0.3 to 10 V
Output current, I_O . . . . 1.5 A
Continuous total power dissipation . . . . See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Note 1 and Figure 3)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
PW[§]	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Note 1 and Figure 4)

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2063 mW	16.5 mW/°C	1320 mW	1073 mW	413 mW
PW[§]	2900 mW	23.2 mW/°C	1856 mW	1508 mW	580 mW

[§] The PW package information is product preview only and is not yet available.

NOTE 1: Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum of 150°C. For guidelines on maintaining junction temperature within the recommended operating range, see application information section.

MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE

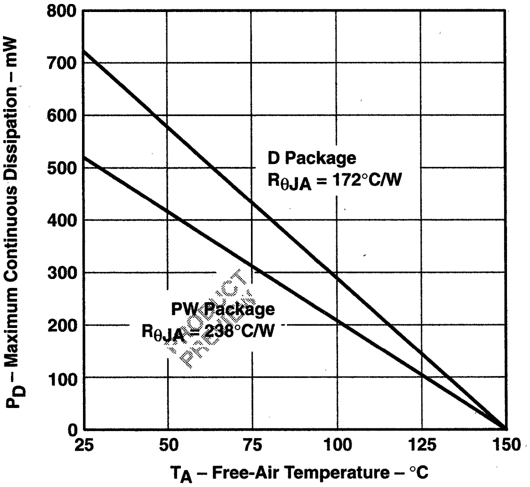

Figure 3

MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE

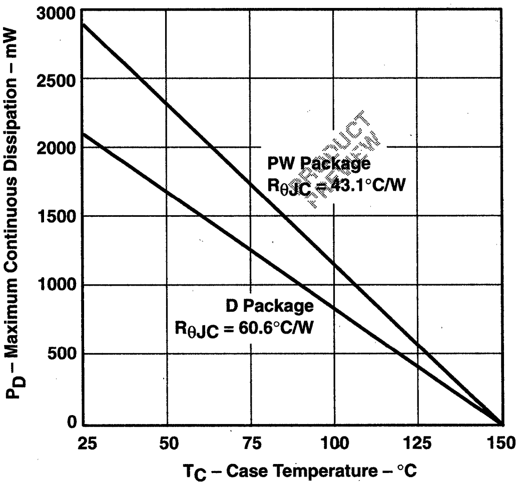

Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7201Q	2.5	10	V
	TPS7233Q	3.98	10	
	TPS7248Q	5.24	10	
	TPS7250Q	5.41	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current, I_O		0	250	mA
Operating virtual junction temperature, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7201 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 under the TPS7201 electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input-voltage range for the TPS7201.

electrical characteristics, $I_O = 10$ mA, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu F$ (CSR† = 1 Ω), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	TPS7201Q, TPS7233Q TPS7248Q, TPS7250Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \le 0.5$ V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA	25°C		180	225	μA
		−40°C to 125°C			325	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
Output current limit threshold	$V_O = 0$ V, $V_I = 10$ V	25°C		0.6	1	A
		−40°C to 125°C			1.5	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
PG leakage current	$V_{PG} = 10$ V, Normal operation	25°C			0.5	μA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		31	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	μA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		1.9	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	$I_{PG} = 300\ \mu A$	25°C		0.95	1.5	V
		−40°C to 125°C			1.9	

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q electrical characteristics, I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7201Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V, I_O = 10 mA		25°C		1.188		V
	2.5 V ≤ V_I ≤ 10 V, 5 mA ≤ I_O ≤ 250 mA, See Note 2		–40°C to 125°C	1.152		1.224	V
Reference voltage temperature coefficient			–40°C to 125°C		31	75	ppm/°C
Pass-element series resistance (see Note 3)	V_I = 2.4 V, 50 μA ≤ I_O ≤ 100 mA		25°C		2.1	4.2	Ω
			–40°C to 125°C			4.8	
	V_I = 2.4 V, 100 mA ≤ I_O ≤ 200 mA		25°C		2.9	4.4	
			–40°C to 125°C			4.6	
	V_I = 2.9 V, 50 μA ≤ I_O ≤ 250 mA		25°C		1.6	2.7	
			–40°C to 125°C			4.5	
	V_I = 3.9 V, 50 μA ≤ I_O ≤ 250 mA		25°C		1		
	V_I = 5.9 V, 50 μA ≤ I_O ≤ 250 mA		25°C		0.8		
Input regulation	V_I = 2.5 V to 10 V, 50 μA ≤ I_O ≤ 250 mA, See Note 2		25°C			23	mV
			–40°C to 125°C			36	
Output regulation	I_O = 5 mA to 250 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 2		25°C		15	25	mV
			–40°C to 125°C			36	
	I_O = 50 μA to 250 mA, 2.5 V ≤ V_I ≤ 10 V, See Note 2		25°C		17	27	
			–40°C to 125°C			43	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	49	60		dB
			–40°C to 125°C	32			
		I_O = 250 mA, See Note 2	25°C	45	50		
			–40°C to 125°C	30			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		235		μVrms
		C_O = 10 μF	25°C		190		
		C_O = 100 μF	25°C		125		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{FB(nom)}$		V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 μA, V_I = 2.13 V		25°C		0.1	0.4	V
			–40°C to 125°C			0.4	
FB input current			25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2. When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

TPS7233Q electrical characteristics, $I_O = 10$ mA, $V_I = 4.3$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ µF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7233Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		14	20	mV
			−40°C to 125°C			30	
	I_O = 100 mA,	V_I = 3.23 V	25°C		140	180	
			−40°C to 125°C			232	
	I_O = 250 mA,	V_I = 3.23 V	25°C		360	460	
			−40°C to 125°C			610	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,	25°C		1.5	1.84	Ω
			−40°C to 125°C			2.5	
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 250 mA	25°C		8	25	mV
			−40°C to 125°C			33	
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		32	42	mV
			−40°C to 125°C			71	
	I_O = 50 µA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		41	55	
			−40°C to 125°C			98	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	40	52		dB
			−40°C to 125°C	38			
		I_O = 250 mA	25°C	35	44		
			−40°C to 125°C	33			
Output noise spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		265		µVrms
		C_O = 10 µF	25°C		212		
		C_O = 100 µF	25°C		135		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		32		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

---

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7248Q electrical characteristics, $I_O = 10$ mA, $V_I = 5.85$ V, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu$F (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7248Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 5.85$ V,	$I_O = 10$ mA	25°C		4.85		V
	$5.85\ V \le V_I \le 10$ V,	$5\ mA \le I_O \le 250$ mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.75$ V	25°C		10	19	mV
			–40°C to 125°C			30	
	$I_O = 100$ mA,	$V_I = 4.75$ V	25°C		90	100	
			–40°C to 125°C			150	
	$I_O = 250$ mA,	$V_I = 4.75$ V	25°C		216	250	
			–40°C to 125°C			285	
Pass-element series resistance	$(4.75\ V - V_O)/I_O$, $I_O = 250$ mA	$V_I = 4.75$ V,	25°C		0.8	1	Ω
			–40°C to 125°C			1.4	
Input regulation	$V_I = 5.85$ V to 10 V,	$50\ \mu A \le I_O \le 250$ mA	25°C			34	mV
			–40°C to 125°C			50	
Output regulation	$I_O = 5$ mA to 250 mA,	$5.85\ V \le V_I \le 10$ V	25°C		43	55	mV
			–40°C to 125°C			95	
	$I_O = 50\ \mu$A to 250 mA,	$5.85\ V \le V_I \le 10$ V	25°C		55	75	
			–40°C to 125°C			135	
Ripple rejection	f = 120 Hz	$I_O = 50\ \mu$A	25°C	42	53		dB
			–40°C to 125°C	36			
		$I_O = 250$ mA	25°C	36	46		
			–40°C to 125°C	34			
Output noise spectral density	f = 120 Hz		25°C		2		$\mu V/\sqrt{Hz}$
Output noise voltage	$10\ Hz \le f \le 100$ kHz, CSR† = 1 Ω	$C_O = 4.7\ \mu$F	25°C		370		μVrms
		$C_O = 10\ \mu$F	25°C		290		
		$C_O = 100\ \mu$F	25°C		168		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		$0.95 \times V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	$I_{PG} = 1.2$ mA,	$V_I = 4.12$ V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7250Q electrical characteristics, I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7250Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		8	12	mV
			–40°C to 125°C			30	
	I_O = 100 mA,	V_I = 4.88 V	25°C		76	85	
			–40°C to 125°C			136	
	I_O = 250 µA,	V_I = 4.88 V	25°C		190	206	
			–40°C to 125°C			312	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,	25°C		0.76	0.825	Ω
			–40°C to 125°C			1.25	
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 250 mA	25°C			28	mV
			–40°C to 125°C			35	
Output regulation	I_O = 5 mA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		46	61	mV
			–40°C to 125°C			100	
	I_O = 50 µA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		59	79	
			–40°C to 125°C			150	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	41	52		dB
			–40°C to 125°C	37			
		I_O = 250 mA	25°C	36	46		
			–40°C to 125°C	32			
Output noise spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		390		µVrms
		C_O = 10 µF	25°C		300		
		C_O = 100 µF	25°C		175		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.19	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7201Y, TPS7233Y TPS7248Y, TPS7250Y MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA		180		μA
Output current limit threshold	V_O = 0 V, V_I = 10 V		0.6		A
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ hysteresis voltage			50		mV
Minimum V_I for active pass element			1.9		V
Minimum V_I for valid PG	I_{PG} = 300 μA		0.95		V

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7201Y			UNIT
			MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA		1.188		V
Pass-element series resistance (see Note 3)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 100 mA		2.1		Ω
	V_I = 2.4 V,	100 mA ≤ I_O ≤ 200 mA		2.9		
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA		1.6		
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA		1		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA		0.8		
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 2	I_O = 5 mA to 250 mA,		15		mV
	2.5 V ≤ V_I ≤ 10 V, See Note 2	I_O = 50 μA to 250 mA,		17		
Ripple rejection	V_I = 3.5 V, f = 120 Hz	I_O = 50 μA		60		dB
		I_O = 250 mA, See Note 2		50		
Output noise spectral density	V_I = 3.5 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		235		μVrms
		C_O = 10 μF		190		
		C_O = 100 μF		125		
PG hysteresis voltage§	V_I = 3.5 V,	Measured at V_{FB}		12		mV
PG output low voltage§	V_I = 2.13 V,	I_{PG} = 400 μA		0.1		V
FB input current	V_I = 3.5 V			0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2 When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3 To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7233Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	V_I = 3.23 V,	I_O = 10 mA		14		mV
	V_I = 3.23 V,	I_O = 100 mA		140		
	V_I = 3.23 V,	I_O = 250 mA		360		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,		1.5		Ω
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		8		mV
Output regulation	4.3 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		32		mV
	4.3 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 250 mA		41		
Ripple rejection	V_I = 4.3 V, f = 120 Hz	I_O = 50 μA		52		dB
		I_O = 250 mA		44		
Output noise spectral density	V_I = 4.3 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 4.3 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		265		μVrms
		C_O = 10 μF		212		
		C_O = 100 μF		135		
PG hysteresis voltage	V_I = 4.3 V			32		mV
PG output low voltage	V_I = 2.8 V,	I_{PG} = 1 mA		0.22		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7248Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	V_I = 4.75 V,	I_O = 10 mA		10		mV
	V_I = 4.75 V,	I_O = 100 mA		90		
	V_I = 4.75 V,	I_O = 250 mA		216		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,		0.8		Ω
Output regulation	5.85 V ≤ V_I ≤ 10 V	I_O = 5 mA to 250 mA		43		mV
	5.85 V ≤ V_I ≤ 10 V	I_O = 50 μA to 250 mA		55		
Ripple rejection	V_I = 5.85 V, f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 5.85 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 5.85 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		370		μVrms
		C_O = 10 μF		290		
		C_O = 100 μF		168		
PG hysteresis voltage	V_I = 5.85 V			50		mV
PG output low voltage	V_I = 4.12 V,	I_{PG} = 1.2 mA		0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7250Q			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA		5		V
Dropout voltage	V_I = 4.88 V,	I_O = 10 mA		8		mV
	V_I = 4.88 V,	I_O = 100 mA		76		
	V_I = 4.88 V,	I_O = 250 μA		190		
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,		0.76		Ω
Input regulation	V_I = 6 V to 10 V,	50 μA ≤ I_O ≤ 250 mA				mV
Output regulation	6 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		46		mV
	6 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 250 mA		59		
Ripple rejection	V_I = 6 V, f = 120 Hz	I_O = 50 μA		52		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 6 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 6 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		390		μVrms
		C_O = 10 μF		300		
		C_O = 100 μF		175		
PG hysteresis voltage	V_I = 6 V			50		mV
PG output low voltage	V_I = 4.25 V,	I_{PG} = 1.2 mA		0.19		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{DO}	Dropout voltage	vs Output current	8
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		vs Output current (C_O = 10 μF)	31
		vs Added ceramic capacitance (C_O = 10 μF)	32

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
OUTPUT CURRENT

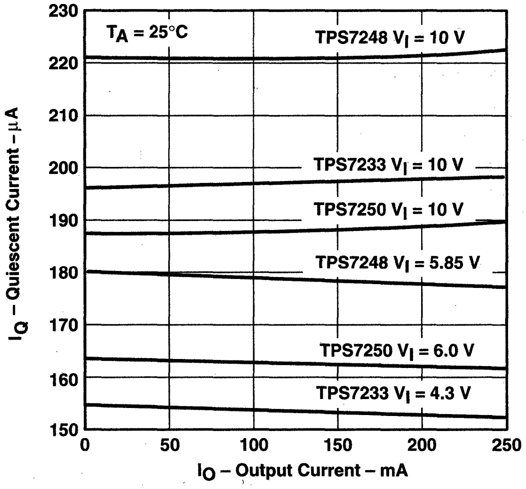


Figure 5

QUIESCENT CURRENT
vs
INPUT VOLTAGE

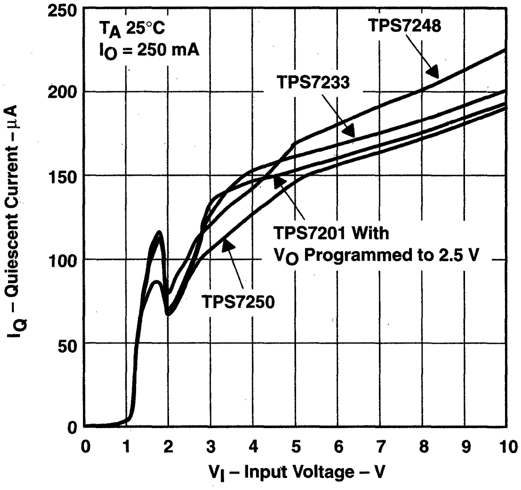


Figure 6

CHANGE IN QUIESCENT CURRENT
vs
FREE-AIR TEMPERATURE

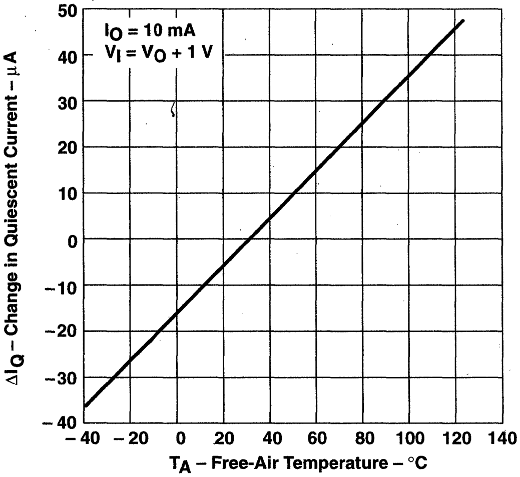


Figure 7

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

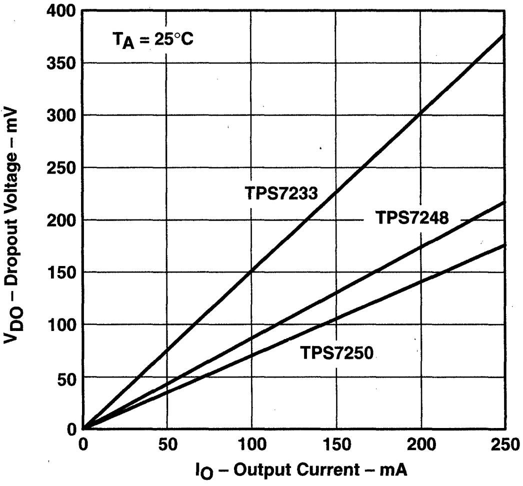


Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

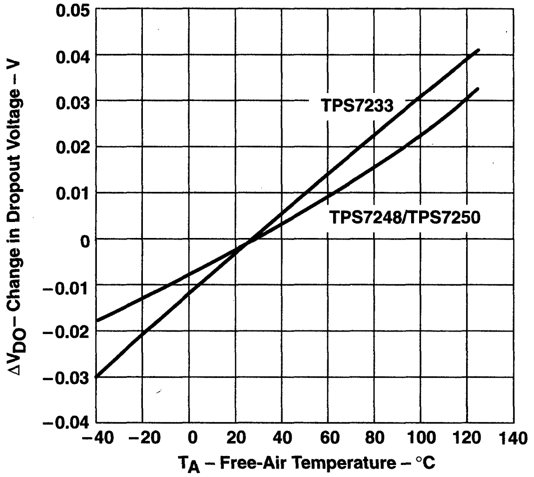


Figure 9

TPS7201
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

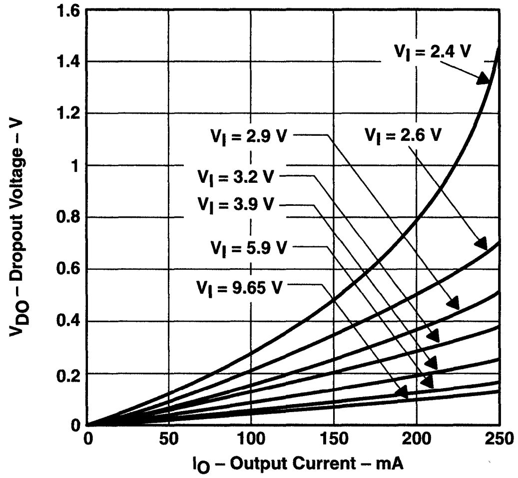


Figure 10

PASS ELEMENT SERIES RESISTANCE
vs
INPUT VOLTAGE

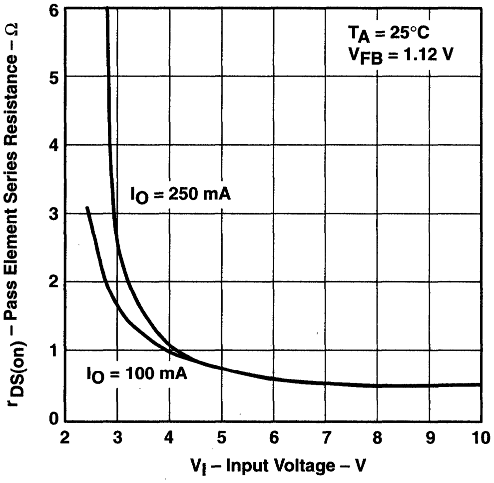


Figure 11

CHANGE IN OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

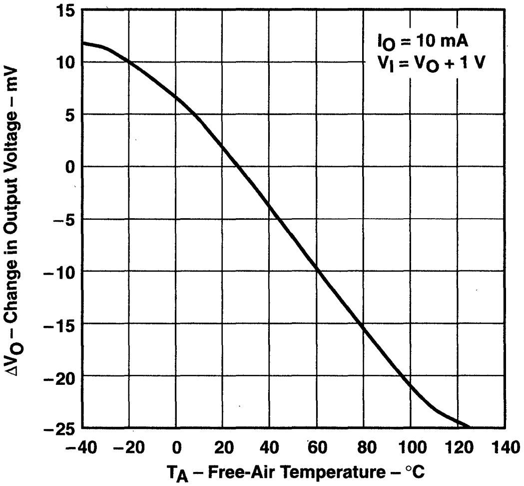


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

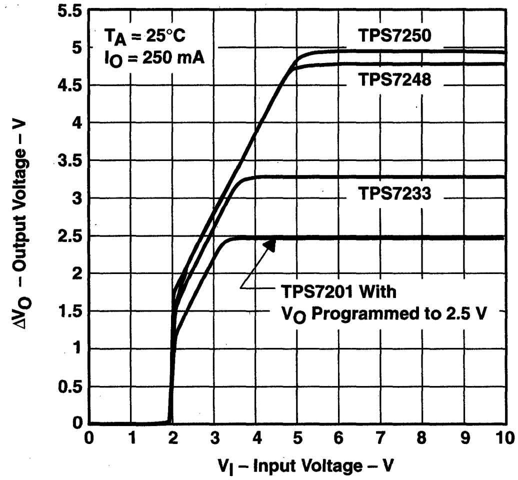


Figure 13

LINE REGULATION

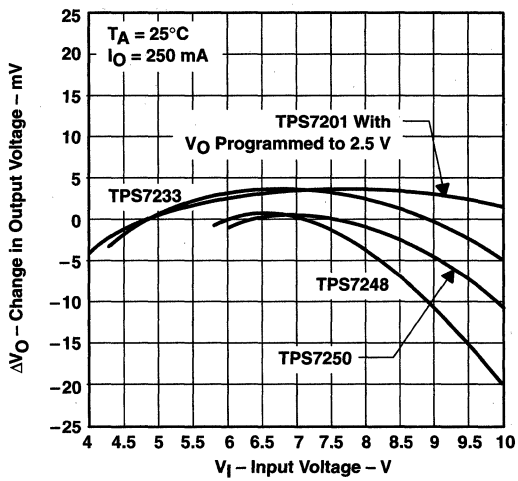


Figure 14

TPS7233

LOAD REGULATION

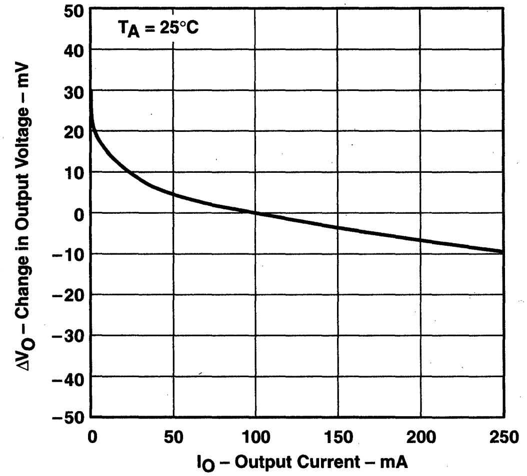


Figure 15

TPS7248

LOAD REGULATION

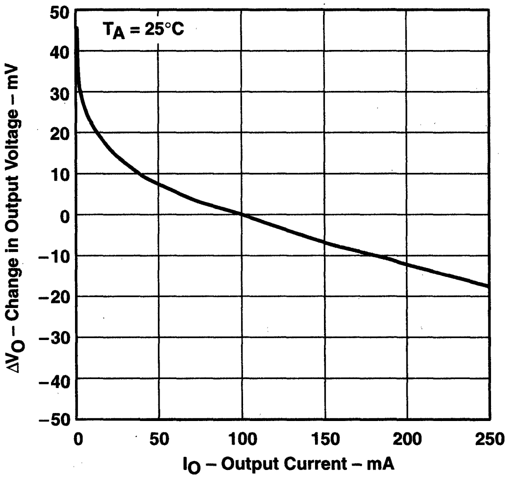


Figure 16

TYPICAL CHARACTERISTICS

TPS7250
LOAD REGULATION

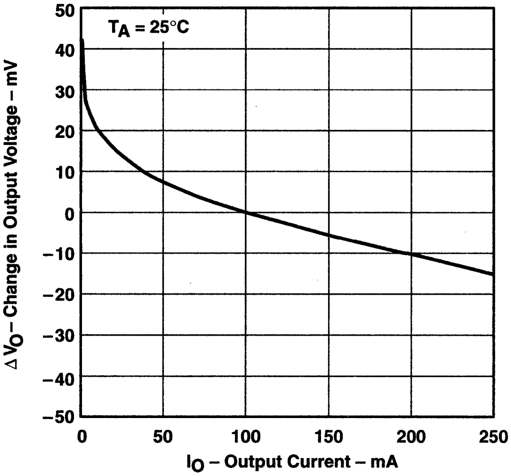
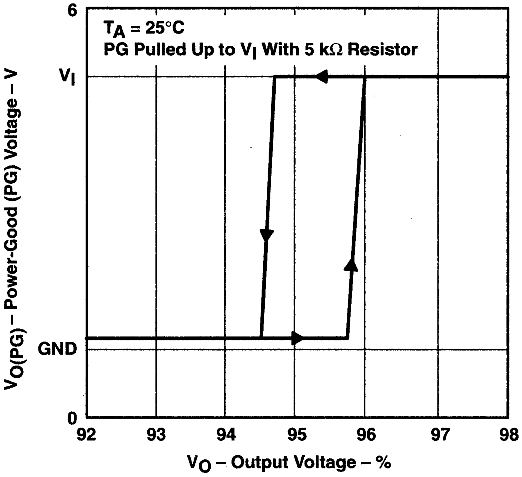


Figure 17

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE†



† VO as a percent of VOnom.

Figure 18

POWER-GOOD (PG) ON-RESISTANCE vs INPUT VOLTAGE

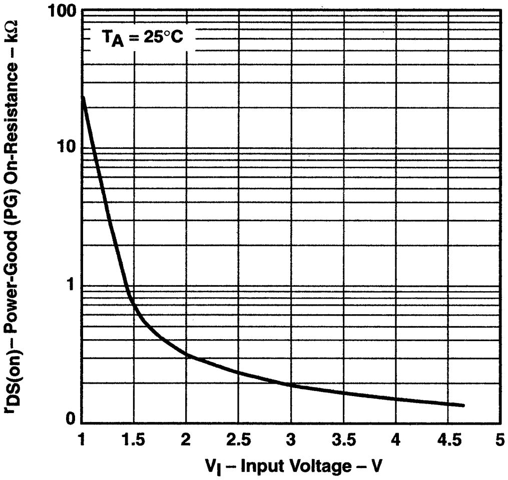


Figure 19

MINIMUM INPUT VOLTAGE FOR VALID PG vs FREE-AIR TEMPERATURE

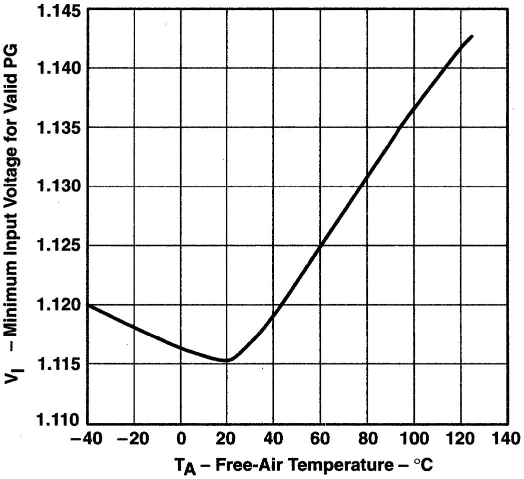


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM $\overline{\text{ENABLE}}$ ($\overline{\text{EN}}$)

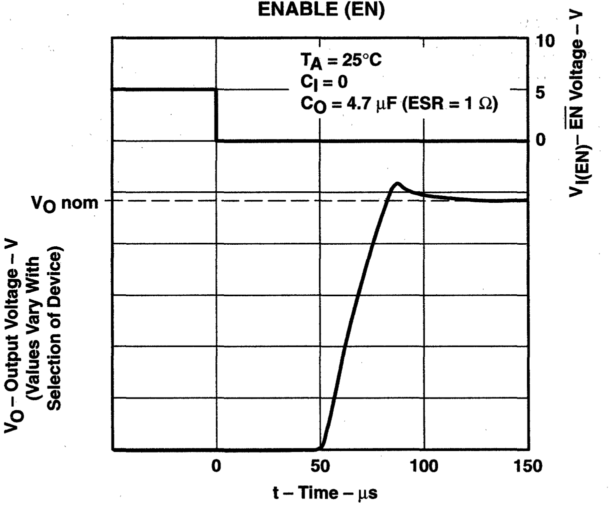


Figure 21

TPS7201 (WITH V_O PROGRAMMED TO 2.5 V), TPS7233 LOAD TRANSIENT RESPONSE

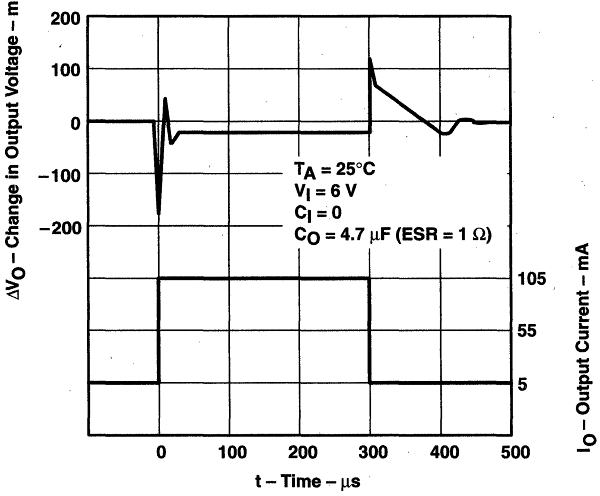


Figure 22

TYPICAL CHARACTERISTICS

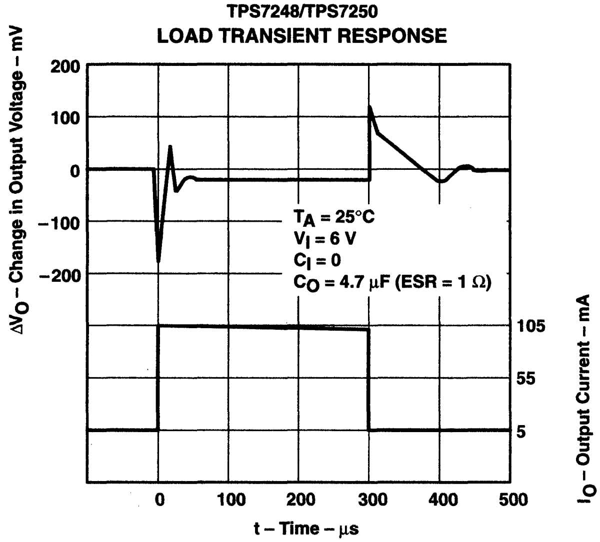


Figure 23

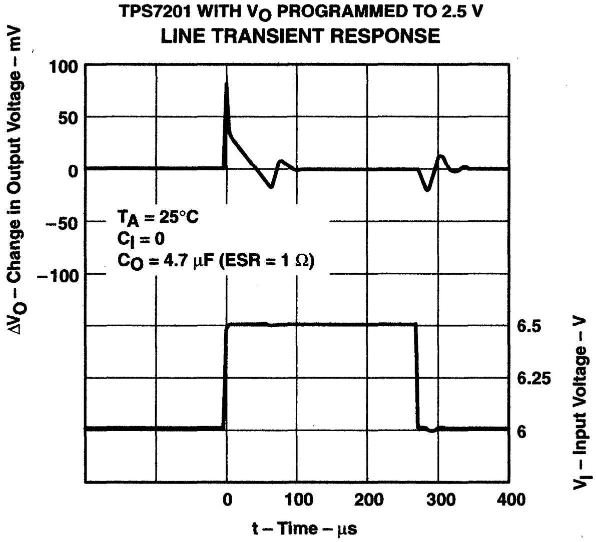


Figure 24

TYPICAL CHARACTERISTICS

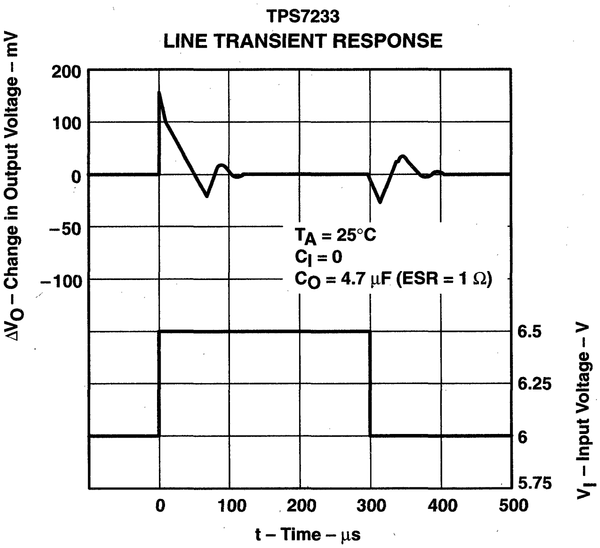


Figure 25

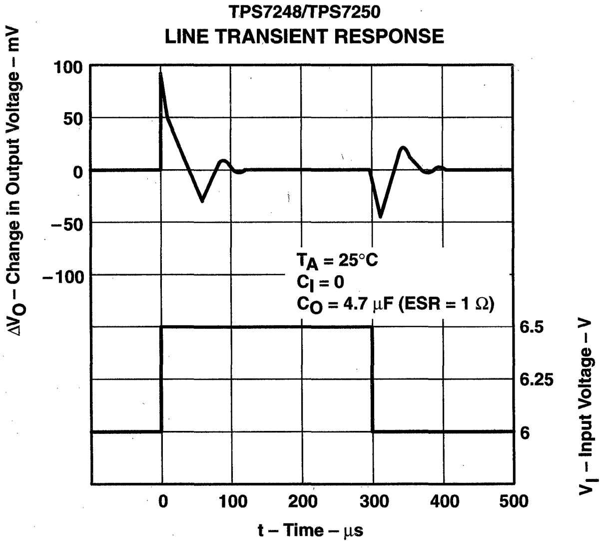


Figure 26

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

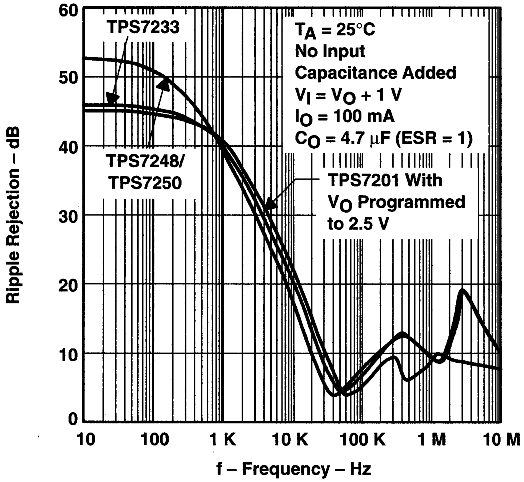


Figure 27

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

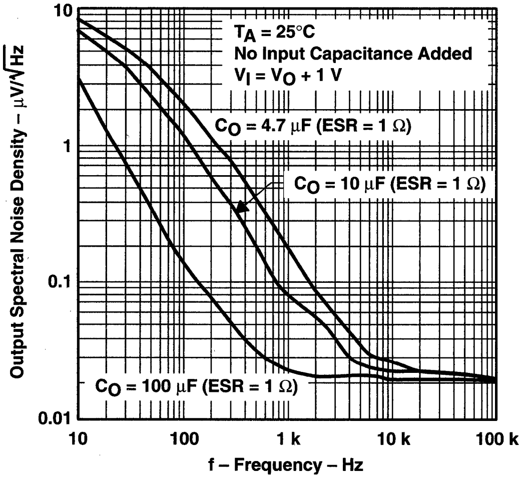


Figure 28

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

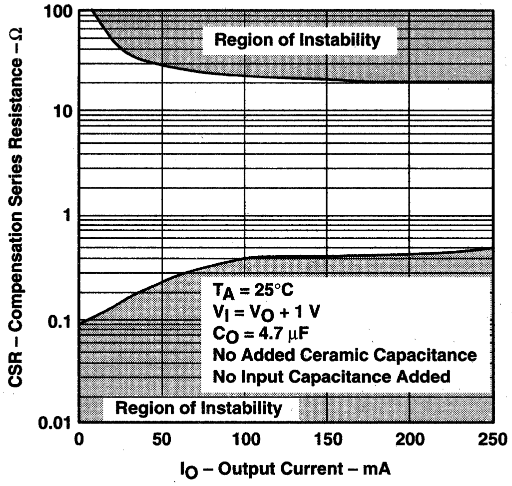


Figure 29

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

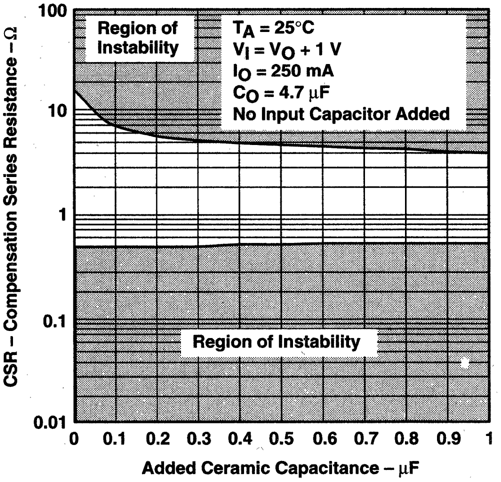


Figure 30

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

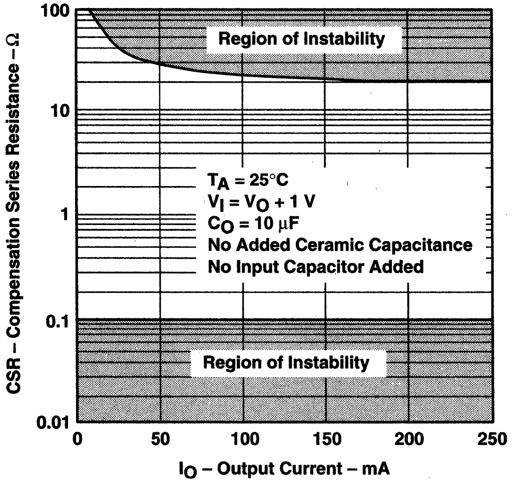


Figure 31

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

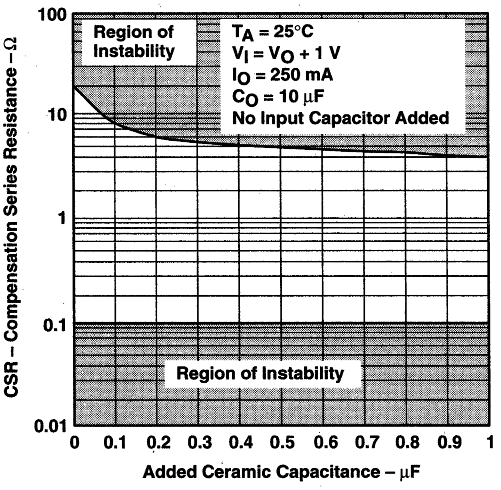


Figure 32

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† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The design of the TPS72xx family of low-dropout (LDO) regulators is based on the higher-current TPS71xx family. These new families of regulators have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low supply currents that remain constant over the full-output-current range of the device, and an enable input to reduce supply currents to less than 0.5 µA when the regulator is turned off.

device operation

The TPS72xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS transistor is a voltage-controlled device and, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS72xx is essentially constant from no-load to maximum.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load increases reduce the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 5°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic high on the enable input, $\overline{\text{EN}}$, shuts off the output and reduces the supply current to less than 0.5 µA. $\overline{\text{EN}}$ should be grounded in applications where the shutdown feature is not used.

Power good (PG) is an open-drain output signal used to indicate output-voltage status. A comparator circuit continuously monitors the output voltage. When the output drops to approximately 95% of its nominal regulated value, the comparator turns on and pulls PG low.

A typical application circuit is shown in Figure 33.

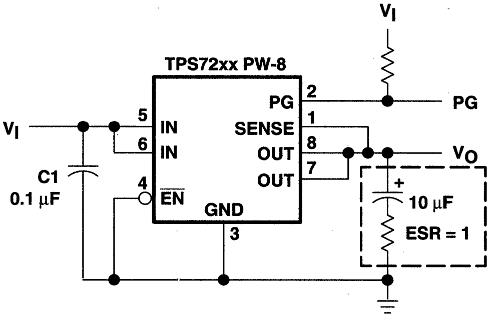


Figure 33. Typical Application Circuit

APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047-µF to 0.1-µF ceramic bypass input capacitor, connected between IN and GND and located close to the TPS72xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

An output capacitor is required to stabilize the internal feedback loop. For most applications, a 10-µF to 15-µF solid-tantalum capacitor with a 0.5-Ω resistor (see capacitor selection table) in series is sufficient. The maximum capacitor ESR should be limited to 1.3 Ω to allow for ESR doubling at cold temperatures. Figure 34 shows the transient response of a 5-mA to 85-mA load using a 10-µF output capacitor with a total ESR of 1.7 Ω.

A 4.7-µF solid-tantalum capacitor in series with a 1-Ω resistor may also be used (see Figures 29 and 30) provided the ESR of the capacitor does not exceed 1 Ω at room temperature and 2 Ω over the full operating temperature range.

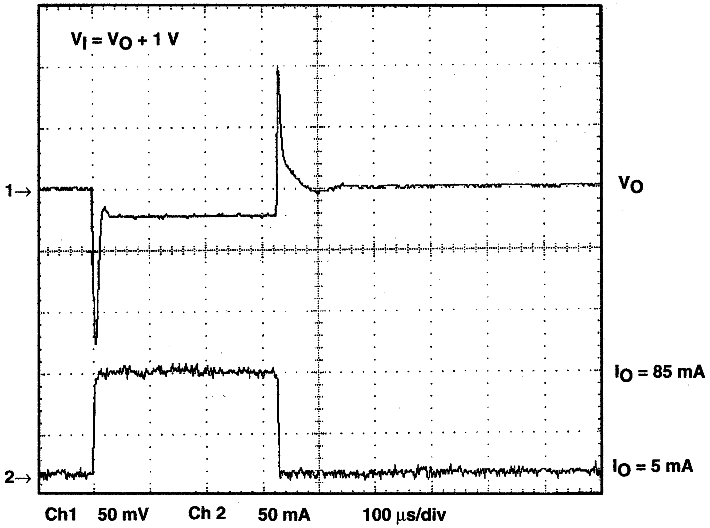


Figure 34. Load Transient Response (ESR total = 1.7 Ω), TPS7248Q

A partial listing of surface-mount capacitors usable with the TPS72xx family is provided below. This information (along with the stability graphs, Figures 29 through 32) is included to assist the designer in selecting suitable capacitors.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

sense-pin connection

SENSE must be connected to OUT for proper operation of the regulator. Normally this connection should be as short as possible; however, remote sense may be implemented in critical applications when proper care of the circuit path is exercised. SENSE internally connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and any noise pickup on the PCB trace will feed through to the regulator output. SENSE must be routed to minimize noise pickup. Filtering SENSE using an RC network is not recommended because of the possibility of inducing regulator instability.

output voltage programming

The output voltage of the TPS7201 adjustable regulator is programmed using an external resistor divider as shown in Figure 35. The output voltage is calculated using:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

V_{ref} = 1.188 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)†	
	R1	R2
2.5	191	169
3.3	309	169
3.6	348	169
4	402	169
5	549	169
6.4	750	169

† 1% values shown.

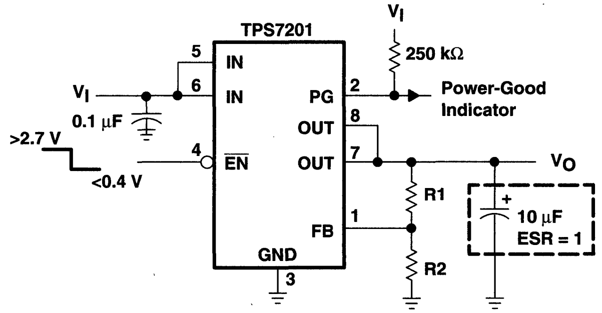


Figure 35. TPS7201 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. These restrictions limit the power dissipation that the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature, i.e.,150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \cdot I_O$$

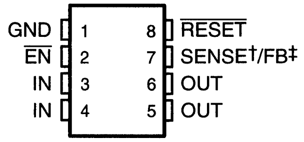
Power dissipation resulting from quiescent current is negligible.

TPS7301Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

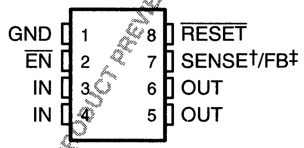
SLVS124A – JUNE 1995 – REVISED SEPTEMBER 1995

- **Available in 3.3-V, 4.85-V, and 5-V Fixed-Output and Adjustable Versions**
- **Integrated Precision Supply-Voltage Supervisor Monitoring Regulator Output Voltage**
- **Active-Low Reset Signal with 200-ms Pulse Width**
- **Very Low Dropout Voltage . . . Maximum of 35 mV at I_O = 100 mA (TPS7350)**
- **Low Quiescent Current – Independent of Load . . . 340 µA Typ**
- **Extremely Low Sleep-State Current, 0.5 µA Max**
- **2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions**
- **Output Current Range of 0 mA to 250 mA**
- **TSSOP Package Option Offers Reduced Component Height For Critical Applications**

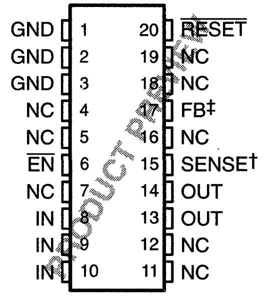
D PACKAGE
(TOP VIEW)



P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection

† SENSE – Fixed voltage options only (TPS7333, TPS7348, and TPS7350)

‡ FB – Adjustable version only (TPS7301)

description

The TPS73xx devices are members of a family of micropower low-dropout (LDO) voltage regulators. They are differentiated from the TPS71xx and TPS72xx LDOs by their integrated delayed microprocessor-reset function. If the precision delayed reset is not required, the designer should consider the TPS71xx and TPS72xx.†

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			NEGATIVE-GOING RESET THRESHOLD VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	MIN	TYP	MAX	SMALL OUT-LINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 125°C	4.9	5	5.1	4.55	4.65	4.75	TPS7350QD	TPS7350QP	TPS7350QPWLE	TPS7350Y
	4.75	4.85	4.95	4.5	4.6	4.7	TPS7348QD	TPS7348QP	TPS7348QPWLE	TPS7348Y
	3.23	3.3	3.37	2.868	2.934	3	TPS7333QD	TPS7333QP	TPS7333QPWLE	TPS7333Y
	Adjustable 1.2 V to 9.75 V			1.101	1.123	1.145	TPS7301QD	TPS7301QP	TPS7301QPWLE	TPS7301Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7350QDR). The PW package is only available left-end taped and reeled. The TPS7301Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

---

† The TPS71xx and the TPS72xx are 500-mA and 250-mA output regulators respectively, offering performance similar to that of the TPS73xx but without the delayed-reset function. The TPS72xx devices are further differentiated by availability in 8-pin thin shrink small-outline packages (TSSOP) for applications requiring minimum package size.

TEXAS INSTRUMENTS

description (continued)

The $\overline{\text{RESET}}$ output of the TPS73xx is designed to initiate a reset in microcomputer and micro-processor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

If that occurs, the $\overline{\text{RESET}}$ output (open-drain NMOS) turns on, taking the $\overline{\text{RESET}}$ signal low. $\overline{\text{RESET}}$ stays low for the duration of the undervoltage condition. Once the undervoltage condition ceases, a 200-ms (typ) time-out begins. At the completion of the 200-ms delay, $\overline{\text{RESET}}$ goes high.

An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 35 mV at an output current of 100 mA for the TPS7350) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and remains constant, independent of output loading (typically 340 μA over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The LDO family also features a sleep mode; applying a logic high signal to $\overline{\text{EN}}$ ($\overline{\text{enable}}$) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at $T_J = 25°C$.

The TPS73xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS73xx family is available in PDIP (8 pin), SO (8 pin) and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

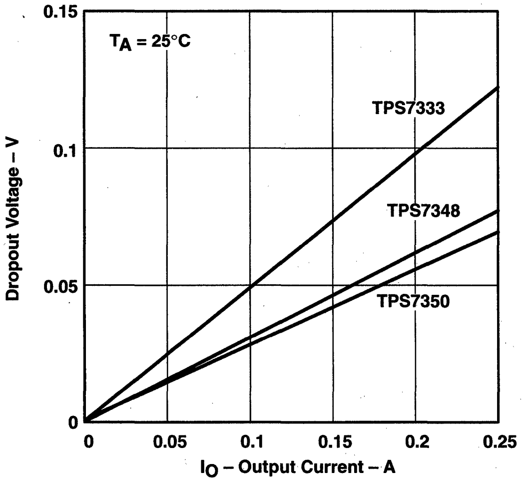
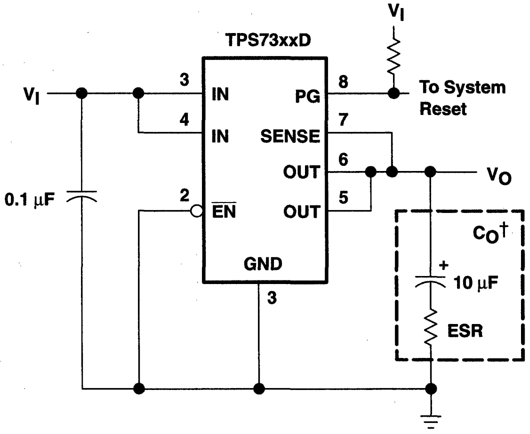


Figure 1. Dropout Voltage Versus Output Current



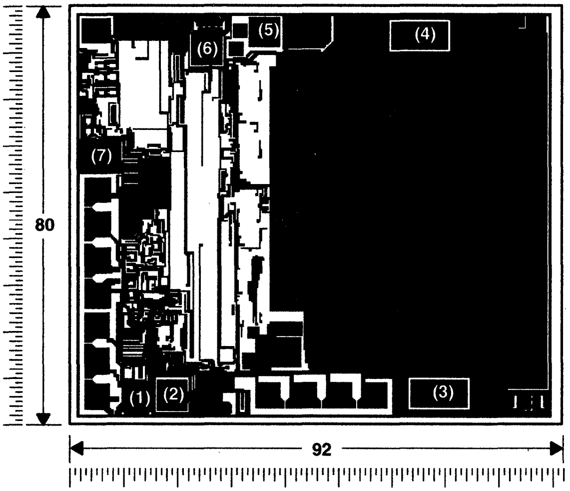
† Capacitor selection is nontrivial. See application information section for details.

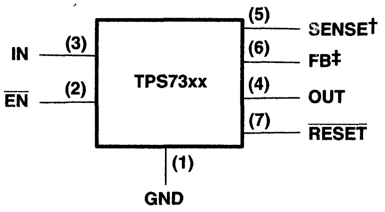
Figure 2. Typical Application Configuration

TPS73xxY chip information

These chips, when properly assembled, display characteristics similar to the TPS73xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

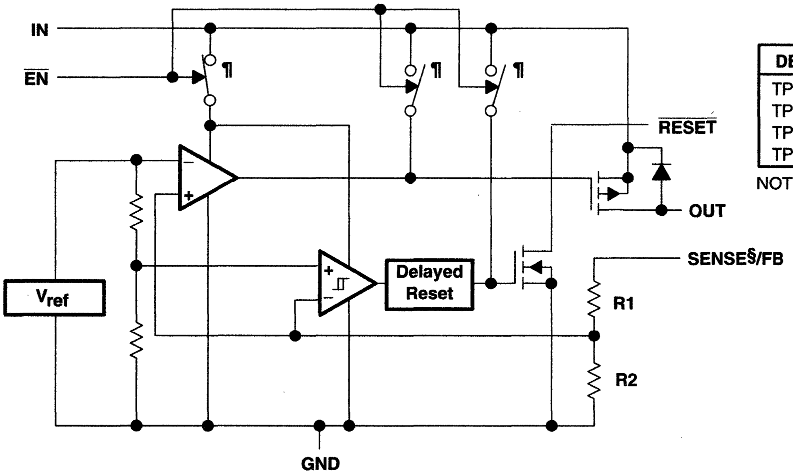
ALL DIMENSIONS ARE IN MILS.

† SENSE – Fixed voltage options only (TPS7333, TPS7348, and TPS7350)

‡ FB – Adjustable version only (TPS7301)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the applications information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

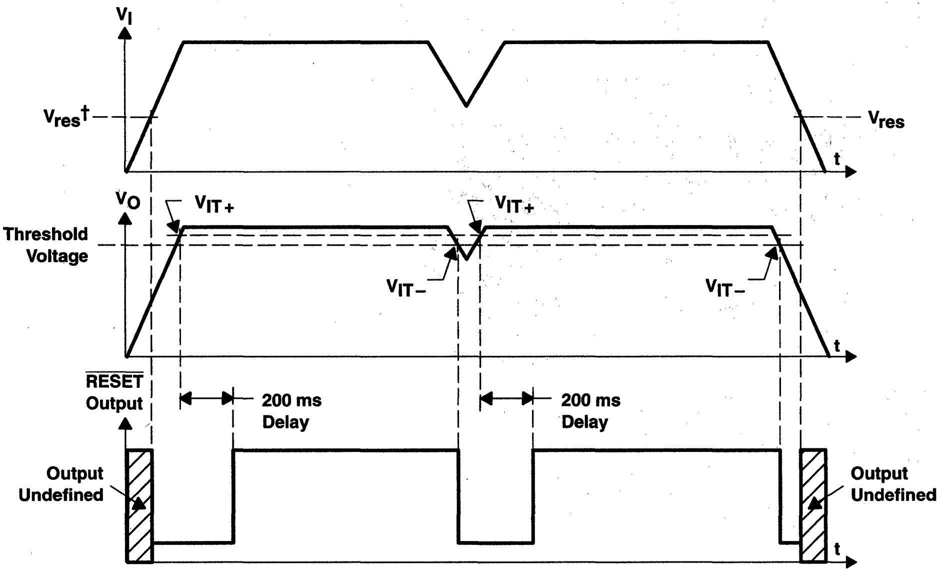
DEVICE	R1	R2	UNIT
TPS7301	0	∞	Ω
TPS7333	420	233	kΩ
TPS7348	726	233	kΩ
TPS7350	756	233	kΩ

NOTE A. Resistors are nominal values only.

§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

¶ Switch positions are shown with $\overline{\text{EN}}$ low (active).

timing diagram



† V_{res} is the minimum input voltage for a valid $\overline{RESET}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range§, V_I, $\overline{RESET}$, SENSE, $\overline{EN}$	–0.3 to 10 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

§ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P†	1175 mW	9.4 mW/°C	752 mW	235 mW
PW†‡	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	9.4 mW/°C	1765 mW	1248 mW
P†	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW†‡	4025 mW	32.2 mW/°C	2576 mW	805 mW

† The P and PW packages are product preview only and are not yet available.
‡ Refer to thermal information section for detailed power dissipation considerations when using the TSSOP package.

**MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE**

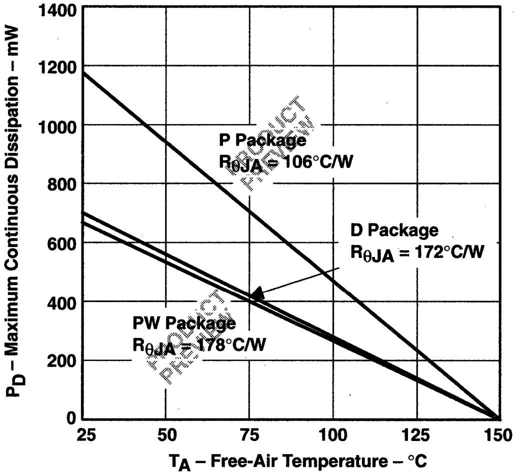


Figure 3

**MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE**

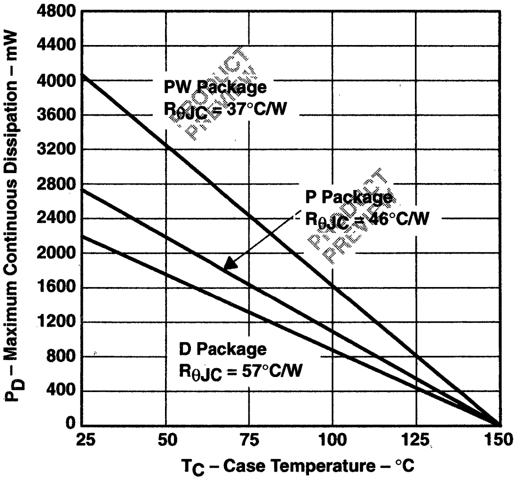


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I[†]	TPS7301Q	2.5	10	V
	TPS7333Q	3.77	10	
	TPS7348Q	5.2	10	
	TPS7350Q	5.33	10	
High-level input voltage at $\overline{\text{EN}}$, V_{IH}		2		V
Low-level input voltage at $\overline{\text{EN}}$, V_{IL}			0.5	V
Output current range, I_O		0	250	mA
Operating virtual junction temperature range, T_J		−40	125	°C

[†] Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO}, at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7301.

electrical characteristics at I_O = 10 mA, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 μF(CSR[‡] = 1 Ω), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS[§]	T_J	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{\text{EN}} \le 0.5$ V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA	25°C		340	400	μA
		−40°C to 125°C			550	
Input current (standby mode)	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	μA
		−40°C to 125°C			2	
Output current limit	V_O = 0 V, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	μA
		−40°C to 125°C			1	
$\overline{\text{RESET}}$ leakage current	Normal operation, V at $\overline{\text{RESET}}$ = 10 V	25°C		0.02	0.5	μA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{\text{EN}}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{\text{EN}}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{\text{EN}}$ hysteresis voltage		25°C		50		mV
$\overline{\text{EN}}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5	0.001	0.5	μA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid $\overline{\text{RESET}}$	$I_{O(\overline{RESET})}$ = −300 μA	25°C		1	1.5	V
		−40°C to 125°C			1.9	

[‡] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

[§] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Q electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7301Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.182		V
	2.5 V ≤ V_I ≤ 10 V, See Note 1	5 mA ≤ I_O ≤ 250 mA,	−40°C to 125°C	1.147		1.217	V
Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 µA ≤ I_O ≤ 150 mA	25°C		0.7	1	Ω
			−40°C to 125°C			1	
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 250 mA	25°C		0.83	1.3	
			−40°C to 125°C			1.3	
	V_I = 2.9 V,	50 µA ≤ I_O ≤ 250 mA	25°C		0.52	0.85	
			−40°C to 125°C			0.85	
	V_I = 3.9 V,	50 µA ≤ I_O ≤ 250 mA	25°C		0.32		
	V_I = 5.9 V,	50 µA ≤ I_O ≤ 250 mA	25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 µA ≤ I_O ≤ 250 mA,	25°C		3	18	mV
			−40°C to 125°C			25	
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 5 mA to 250 mA,	25°C		5	14	mV
			−40°C to 125°C			25	
	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 50 µA to 250 mA,	25°C		7	22	mV
			−40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	48	59		dB
			−40°C to 125°C	44			
		I_O = 250 mA, See Note 1	25°C	45	54		
			−40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		95		µVrms
		C_O = 10 µF	25°C		89		
		C_O = 100 µF	25°C		74		
$\overline{\text{RESET}}$ trip-threshold voltage§	$V_{O(FB)}$ decreasing		−40°C to 125°C	1.101		1.145	V
$\overline{\text{RESET}}$ hysteresis voltage§	Measured at $V_{O(FB)}$		25°C		12		mV
$\overline{\text{RESET}}$ output low voltage§	V_I = 2.13 V,	$I_{O(RESET)}$ = 400 µA	25°C		0.1	0.4	V
			−40°C to 125°C			0.4	
FB input current			25°C	−10	0.1	10	nA
			−40°C to 125°C	−20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 32) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation: $V_{DO} = I_O \cdot r_{DS(on)}$
$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 32.

TPS7333Q electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7333Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	7	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		44	60	
			−40°C to 125°C			80	
	I_O = 250 mA,	V_I = 3.23 V	25°C		108	150	
			−40°C to 125°C			200	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,	25°C		0.44	0.6	Ω
			−40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 250 mA	25°C		6	23	mV
			−40°C to 125°C			29	
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	32	mV
			−40°C to 125°C			60	
	I_O = 50 µA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		31	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	46	51		dB
			−40°C to 125°C	44			
		I_O = 250 mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		274		µVrms
		C_O = 10 µF	25°C		228		
		C_O = 100 µF	25°C		159		
$\overline{\text{RESET}}$ trip-threshold voltage	V_O decreasing		−40°C to 125°C	2.868			V
$\overline{\text{RESET}}$ trip-threshold voltage	V_O increasing		−40°C to 125°C				V
$\overline{\text{RESET}}$ hysteresis voltage			25°C		18		mV
$\overline{\text{RESET}}$ output low voltage	V_I = 2.8 V,	$I_{O(RESET)}$ = −1 mA	25°C		0.17	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7348Q electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7348Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	−40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		2.9	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.75 V	25°C		28	37	
			−40°C to 125°C			52	
	I_O = 250 mA,	V_I = 4.75 V	25°C		70	91	
			−40°C to 125°C			130	
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,	25°C		0.28	0.37	Ω
			−40°C to 125°C			0.52	
Input regulation	V_I = 5.85 V to 10 V,	50 µA ≤ I_O ≤ 250 mA	25°C		9	35	mV
			−40°C to 125°C			37	
Output regulation	I_O = 5 mA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		28	40	mV
			−40°C to 125°C			75	
	I_O = 50 µA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	65	mV
			−40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	45	53		dB
			−40°C to 125°C	39			
		I_O = 250 mA	25°C	39	50		
			−40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		410		µVrms
		C_O = 10 µF	25°C		328		
		C_O = 100 µF	25°C		212		
$\overline{\text{RESET}}$ trip-threshold voltage	V_O decreasing		−40°C to 125°C	4.5		4.7	V
$\overline{\text{RESET}}$ trip-threshold voltage	V_O increasing		−40°C to 125°C				V
$\overline{\text{RESET}}$ hysteresis voltage			25°C		26		mV
$\overline{\text{RESET}}$ output low voltage	$I_{O(RESET)}$ = −1.2 mA, V_I = 4.12 V		25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7350Q electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7350Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		2.9	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	35	
			–40°C to 125°C			50	
	I_O = 250 mA,	V_I = 4.88 V	25°C		68	88	
			–40°C to 125°C			125	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,	25°C		0.27	0.35	Ω
			–40°C to 125°C			0.5	
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 250 mA	25°C		4	20	mV
			–40°C to 125°C			45	
Output regulation	I_O = 5 mA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		28	40	mV
			–40°C to 125°C			75	
	I_O = 50 µA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		41	65	mV
			–40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	43	53		dB
			–40°C to 125°C	38			
		I_O = 250 mA	25°C	41	51		
			–40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF	25°C		430		µVrms
		C_O = 10 µF	25°C		345		
		C_O = 100 µF	25°C		220		
$\overline{RESET}$ trip-threshold voltage	V_O decreasing		–40°C to 125°C	4.55		4.75	V
$\overline{RESET}$ trip-threshold voltage	V_O increasing		–40°C to 125°C				V
$\overline{RESET}$ hysteresis voltage			25°C		28		mV
$\overline{RESET}$ output low voltage	$I_{O(RESET)}$ = –1.2 mA, V_I = 4.25 V		25°C		0.15	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

switching characteristics

PARAMETER	TEST CONDITIONS	T_J	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q			UNIT
			MIN	TYP	MAX	
$\overline{\text{RESET}}$ time-out delay	See Figure 5	25°C	140	200	260	ms
		–40°C to 125°C	100		300	

electrical characteristics at I_O = 10 mA, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7301Y, TPS7333Y TPS7348Y, TPS7350Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{\text{EN}} \le 0.5$ V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA		340		µA
Input current (standby mode)	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V		0.01		µA
Output current limit	V_O = 0 V, V_I = 10 V		1.2		A
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V_I ≤ 10 V		0.01		µA
$\overline{\text{RESET}}$ leakage current	Normal operation, V at $\overline{\text{RESET}}$ = 10 V		0.02		µA
Thermal shutdown junction temperature			165		°C
$\overline{\text{EN}}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V				V
$\overline{\text{EN}}$ hysteresis voltage			50		mV
$\overline{\text{EN}}$ input current	0 V ≤ V_I ≤ 10 V		0.001		µA
Minimum V_I for active pass element			2.05		V
Minimum V_I for valid $\overline{\text{RESET}}$	$I_{O(\overline{\text{RESET}})}$ = –300 µA		1		V

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Y electrical characteristics at $I_O = 10$ mA, $V_I = 3.5$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ µF(CSR† = 1 Ω), $T_J = 25$°C, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7301Y			UNIT
			MIN	TYP	MAX	
Reference voltage (measured at FB)	$V_I = 3.5$ V,	$I_O = 10$ mA		1.182		V
Pass-element series resistance (see Note 2)	$V_I = 2.4$ V,	50 µA ≤ I_O ≤ 150 mA		0.7		Ω
	$V_I = 2.4$ V,	150 mA ≤ I_O ≤ 250 mA		0.83		
	$V_I = 2.9$ V,	50 µA ≤ I_O ≤ 250 mA		0.52		
	$V_I = 3.9$ V,	50 µA ≤ I_O ≤ 250 mA		0.32		
	$V_I = 5.9$ V,	50 µA ≤ I_O ≤ 250 mA		0.23		
Input regulation	$V_I = 2.5$ V to 10 V, See Note 1	50 µA ≤ I_O ≤ 250 mA,		3		mV
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 1	$I_O = 5$ mA to 250 mA,		5		mV
	2.5 V ≤ V_I ≤ 10 V, See Note 1	$I_O = 50$ µA to 250 mA,		7		mV
Ripple rejection	f = 120 Hz	$I_O = 50$ µA		59		dB
		$I_O = 250$ mA, See Note 1		54		
Output noise-spectral density	f = 120 Hz			2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	$C_O = 4.7$ µF		95		µVrms
		$C_O = 10$ µF		89		
		$C_O = 100$ µF		74		
$\overline{\text{RESET}}$ hysteresis voltage§	Measured at $V_{O(FB)}$			12		mV
$\overline{\text{RESET}}$ output low voltage§	$V_I = 2.13$ V,	$I_{O(RESET)} = 400$ µA		0.1		V
FB input current				0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9$ V and $I_O > 150$ mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 32) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation: $V_{DO} = I_O \cdot r_{DS(on)}$
$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for $V_I = 2.4$ V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 32.

TPS7333Y electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7333Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V		4.5		mV
	I_O = 100 mA,	V_I = 3.23 V		44		
	I_O = 250 mA,	V_I = 3.23 V		108		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,		0.44		Ω
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 250 mA		6		mV
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V		21		mV
	I_O = 50 µA to 250 mA,	4.3 V ≤ V_I ≤ 10 V		31		mV
Ripple rejection	f = 120 Hz	I_O = 50 µA		51		dB
		I_O = 250 mA		49		
Output noise-spectral density	f = 120 Hz			2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF		274		µVrms
		C_O = 10 µF		228		
		C_O = 100 µF		159		
$\overline{RESET}$ hysteresis voltage				18		mV
$\overline{RESET}$ output low voltage	V_I = 2.8 V,	$I_{O(RESET)}$ = –1 mA		0.17		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

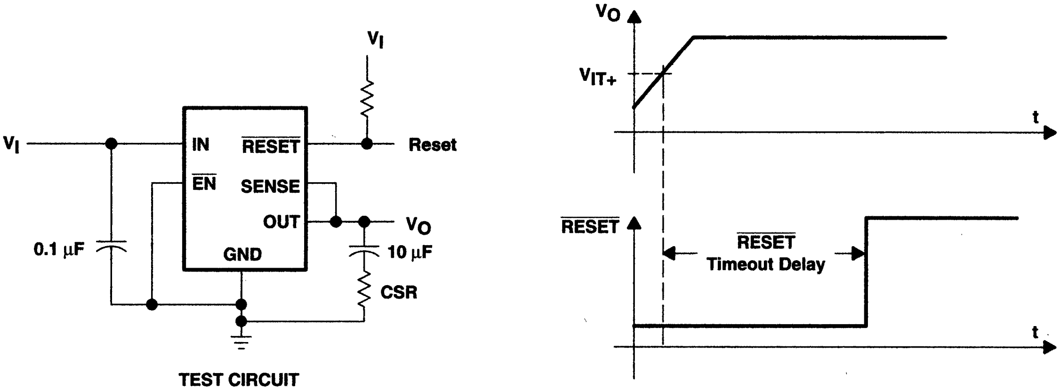
TPS7348Y electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7348Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V		2.9		mV
	I_O = 100 mA,	V_I = 4.75 V		28		
	I_O = 250 mA,	V_I = 4.75 V		70		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,		0.28		Ω
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		9		mV
Output regulation	I_O = 5 mA to 250 mA,	5.85 V ≤ V_I ≤ 10 V		28		mV
	I_O = 50 μA to 250 mA,	5.85 V ≤ V_I ≤ 10 V		42		mV
Ripple rejection	f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 250 mA		50		
Output noise-spectral density	f = 120 Hz			2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		410		μVrms
		C_O = 10 μF		328		
		C_O = 100 μF		212		
$\overline{\text{RESET}}$ hysteresis voltage				26		mV
$\overline{\text{RESET}}$ output low voltage	$I_{O(RESET)}$ = –1.2 mA, V_I = 4.12 V			0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

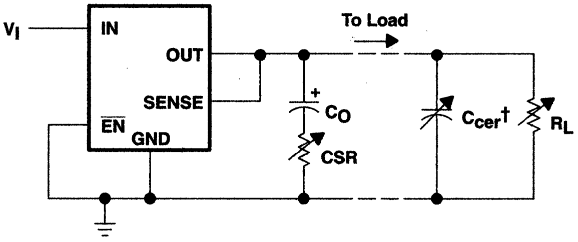
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 5. Test Circuit and Voltage Waveforms



† Ceramic capacitor

Figure 6. Test Circuit for Typical Regions of Stability (Refer to Figures 28 through 31)

TYPICAL CHARACTERISTICS

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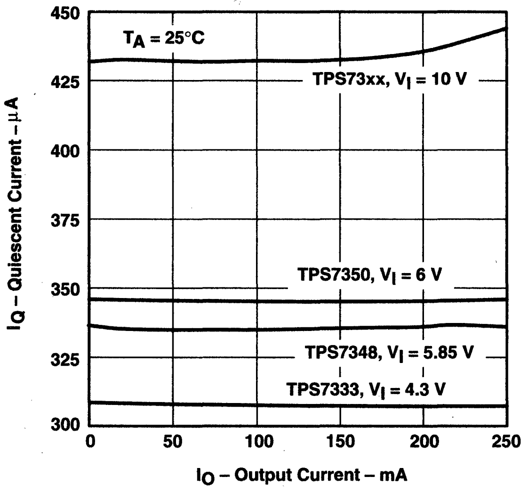
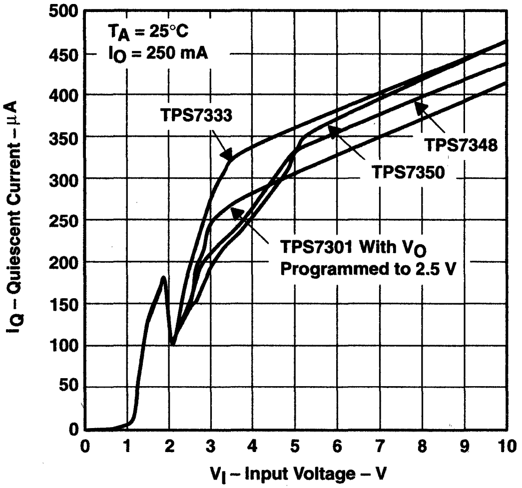
TYPICAL CHARACTERISTICS



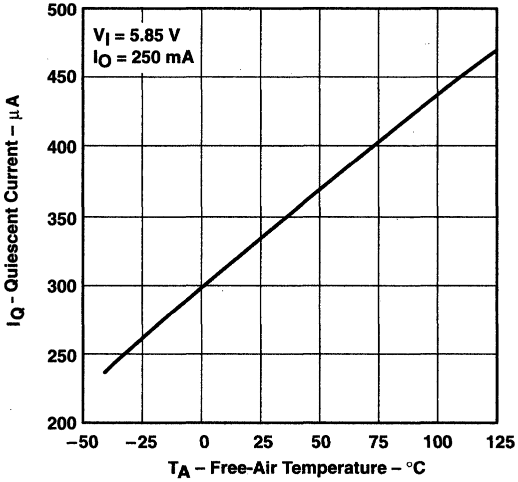
QUIESCENT CURRENT
vs
OUTPUT CURRENT

Figure 7



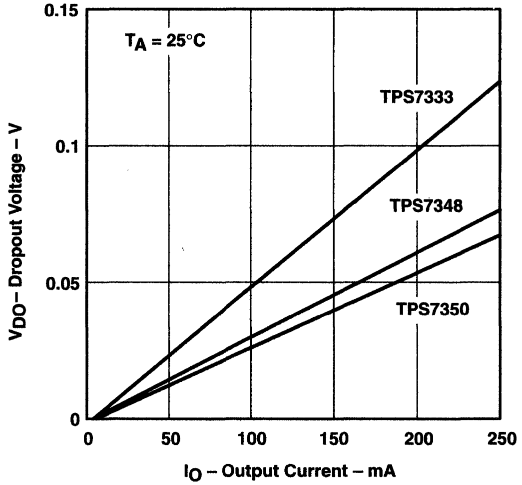
QUIESCENT CURRENT
vs
INPUT VOLTAGE

Figure 8



TPS7348Q
QUIESCENT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 9



DROPOUT VOLTAGE
vs
OUTPUT CURRENT

Figure 10

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

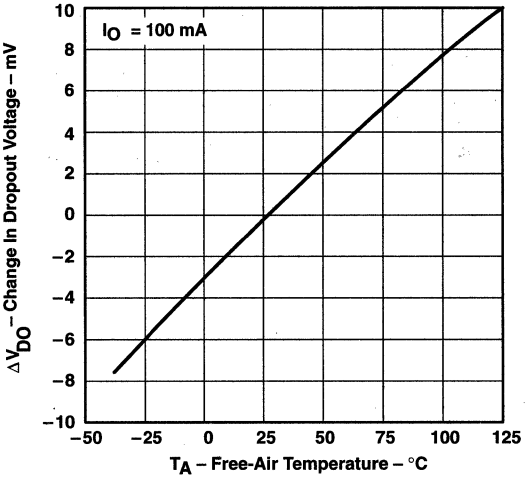


Figure 11

TPS7301 DROPOUT VOLTAGE vs OUTPUT CURRENT

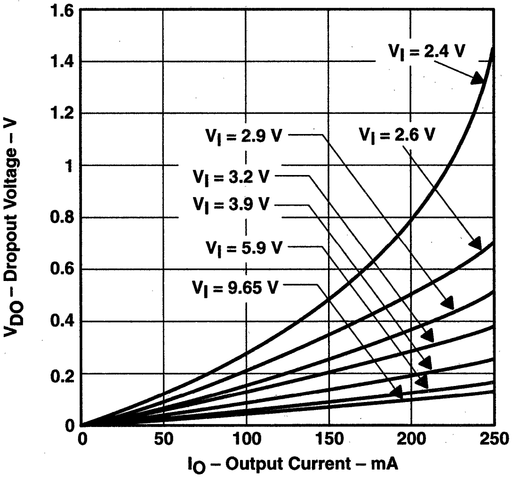


Figure 12

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

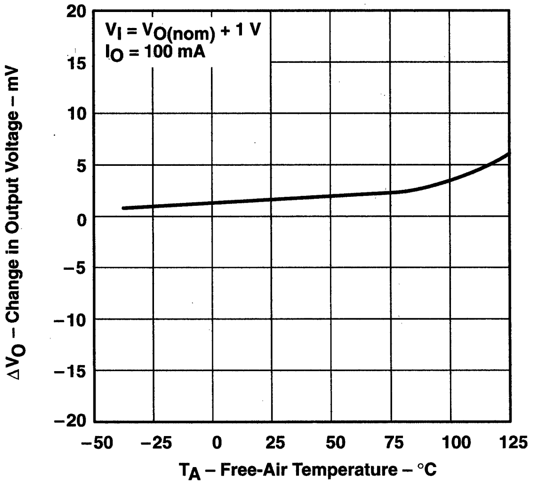


Figure 13

OUTPUT VOLTAGE vs INPUT VOLTAGE

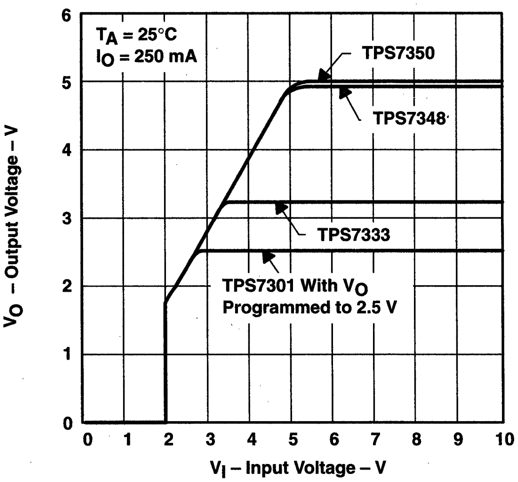


Figure 14

TYPICAL CHARACTERISTICS

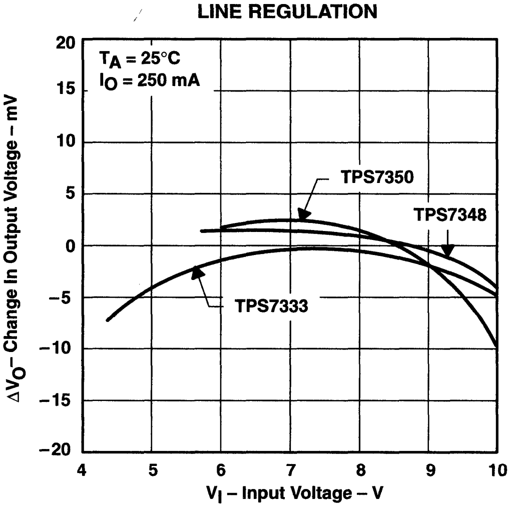


Figure 15

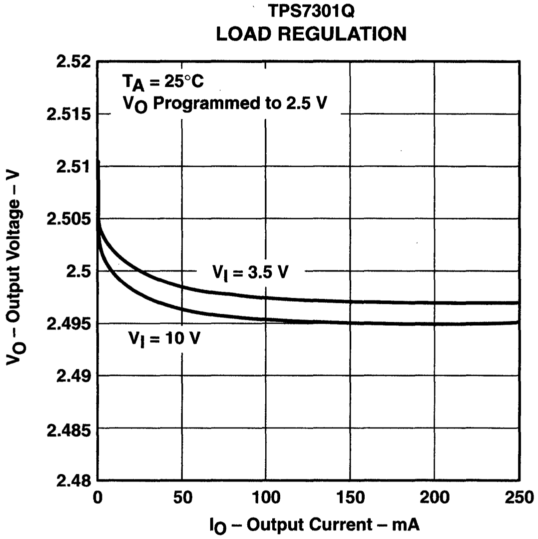


Figure 16

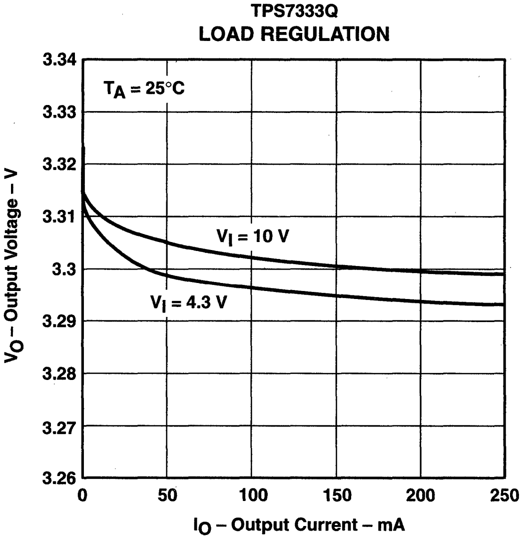


Figure 17

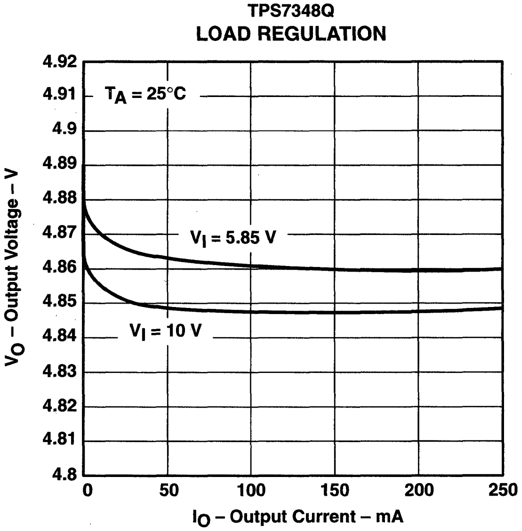


Figure 18

TYPICAL CHARACTERISTICS

TPS7350Q LOAD REGULATION

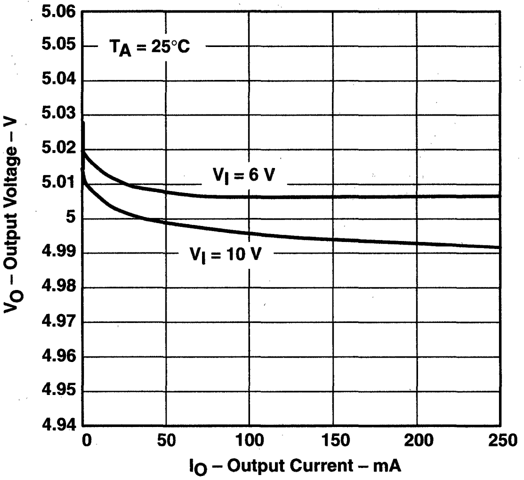


Figure 19

OUTPUT VOLTAGE RESPONSE FROM ENABLE ($\overline{EN}$)

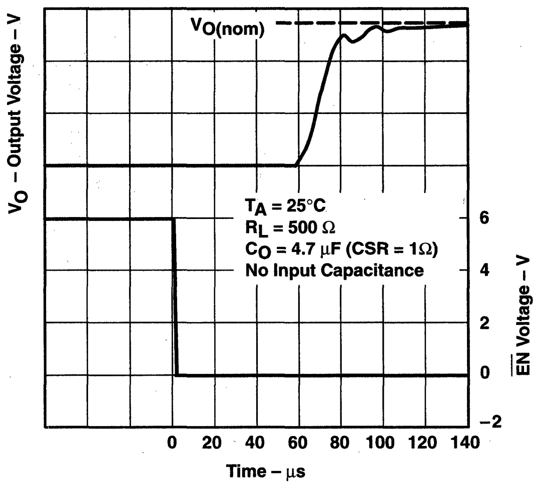


Figure 20

TPS7301 (WITH V_O PROGRAMMED TO 2.5 V) OR TPS7333 LOAD TRANSIENT RESPONSE

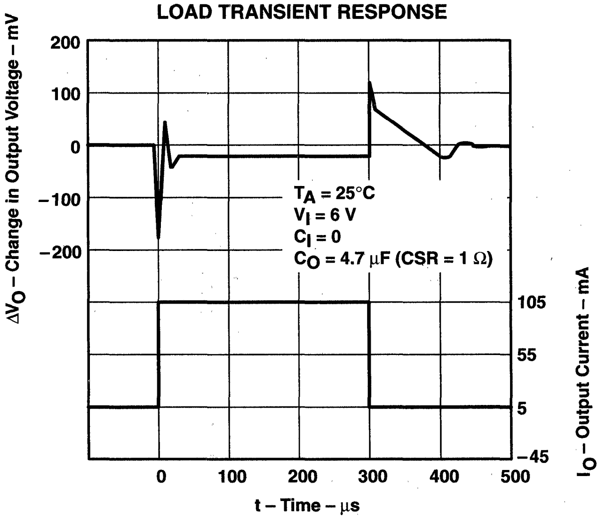


Figure 21

TYPICAL CHARACTERISTICS

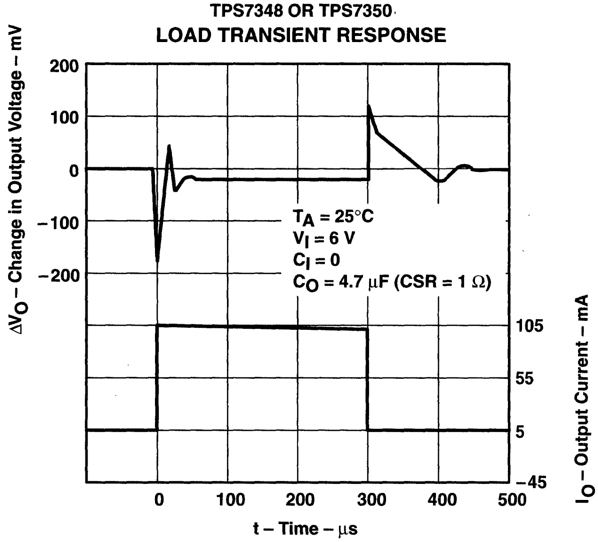


Figure 22

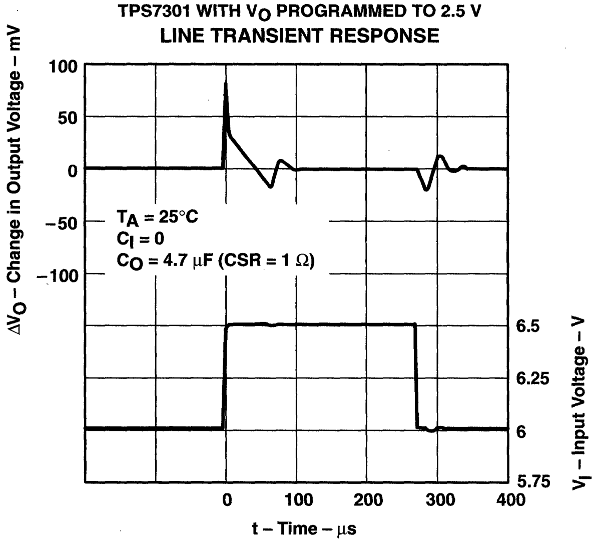


Figure 23

TYPICAL CHARACTERISTICS

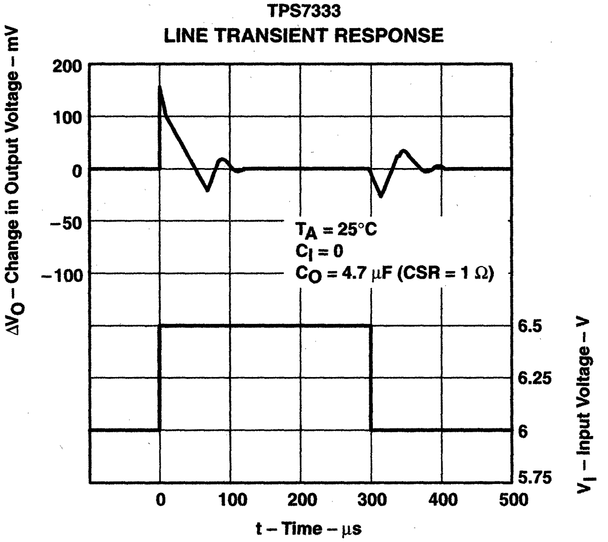


Figure 24

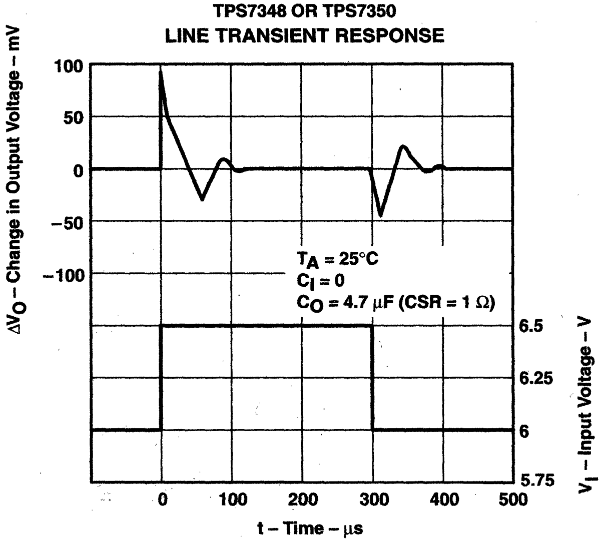


Figure 25

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

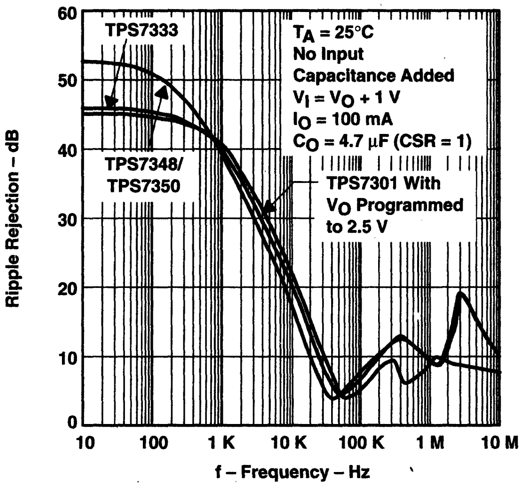


Figure 26

OUTPUT SPECTRAL-NOISE DENSITY
vs
FREQUENCY

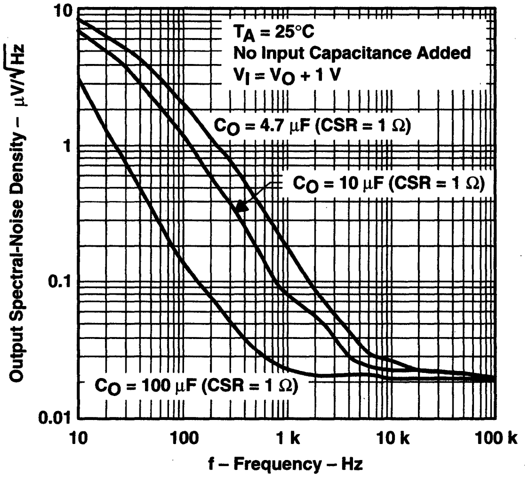


Figure 27

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY COMPENSATION SERIES RESISTANCE (CSR)† vs OUTPUT CURRENT

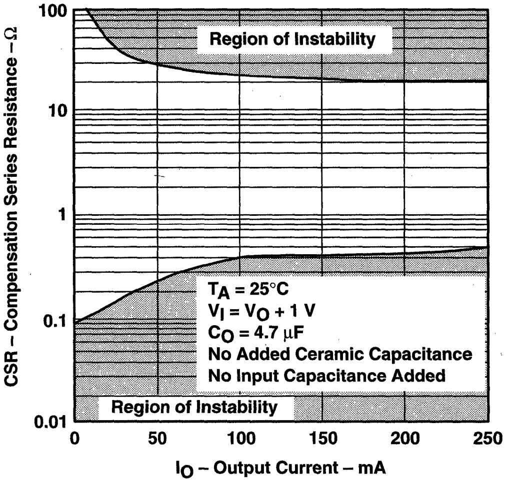


Figure 28

TYPICAL REGIONS OF STABILITY COMPENSATION SERIES RESISTANCE (CSR)† vs ADDED CERAMIC CAPACITANCE

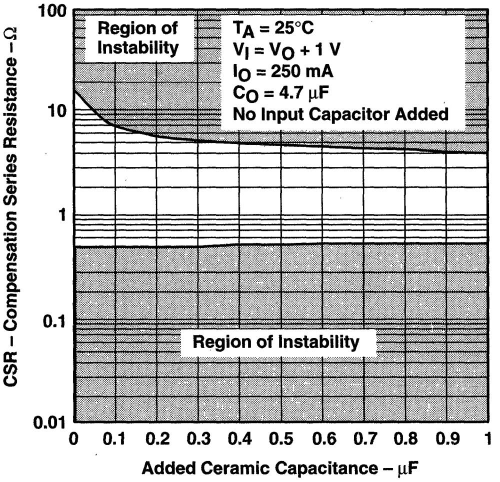


Figure 29

TYPICAL REGIONS OF STABILITY COMPENSATION SERIES RESISTANCE (CSR)† vs OUTPUT CURRENT

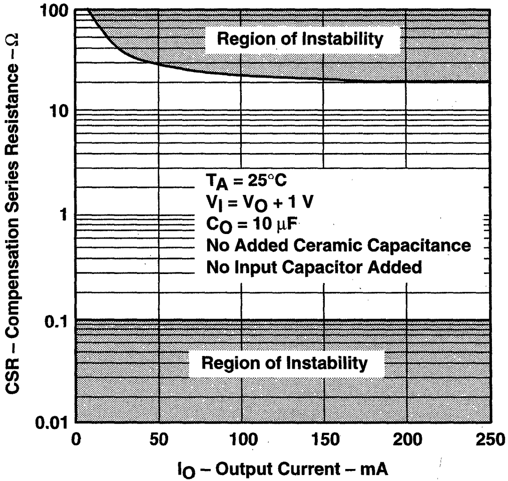


Figure 30

TYPICAL REGIONS OF STABILITY COMPENSATION SERIES RESISTANCE (CSR)† vs ADDED CERAMIC CAPACITANCE

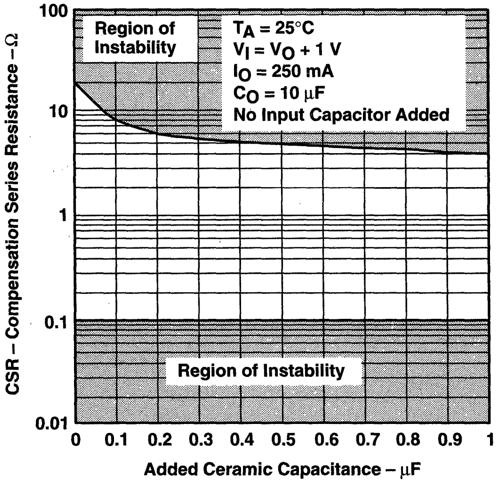


Figure 31

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† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

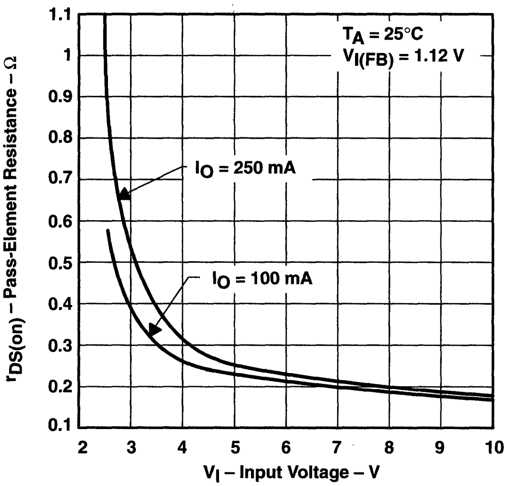


Figure 32

MINIMUM INPUT VOLTAGE FOR VALID $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

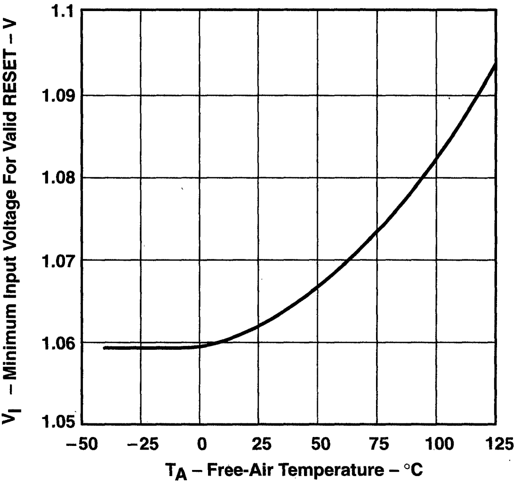


Figure 33

NEGATIVE-GOING RESET THRESHOLD vs FREE-AIR TEMPERATURE

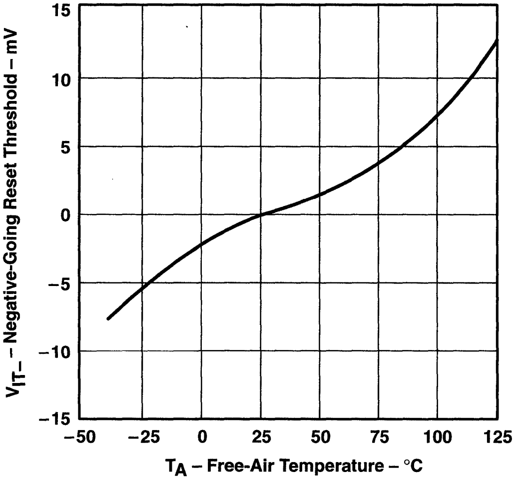


Figure 34

$\overline{\text{RESET}}$ OUTPUT CURRENT vs INPUT VOLTAGE

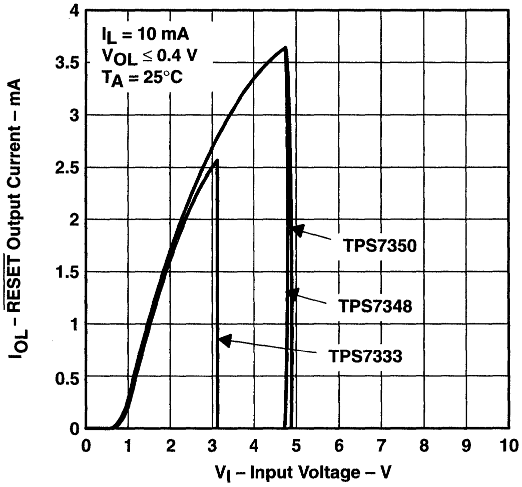


Figure 35

TYPICAL CHARACTERISTICS

RESET DELAY TIME
vs
FREE-AIR TEMPERATURE

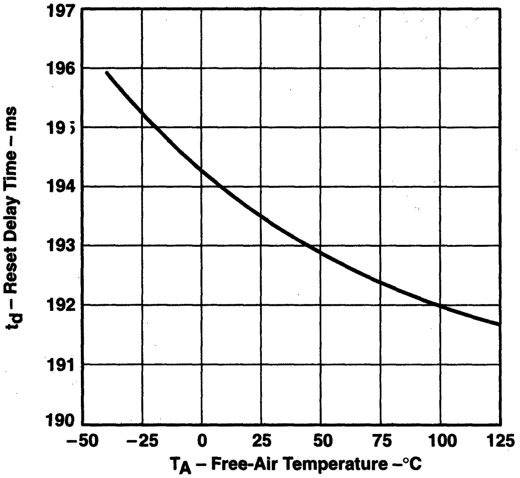


Figure 36

DISTRIBUTION FOR RESET DELAY

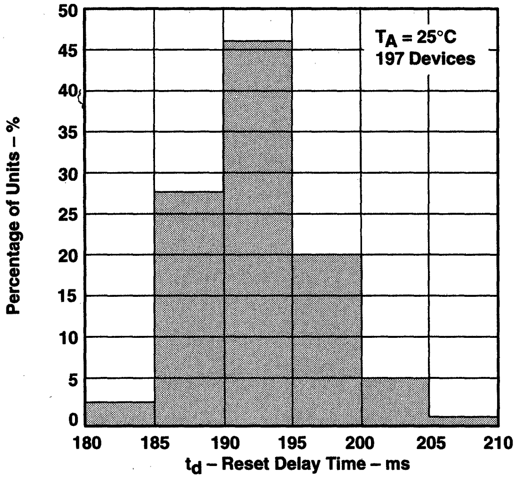


Figure 37

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 38 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 39. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 40 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m · °C.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature or 125°C i.e., 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation.

This limit should then be applied to the internal power dissipated by the TPS73xx regulator. The equation for calculating total internal power dissipation of the TPS71xx is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS73xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55°C$, airflow = 100 ft/min, and copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 40, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS7348 regulator where $V_I = 6$ V and $I_O = 385$ mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

THERMAL INFORMATION

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing either the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing either the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

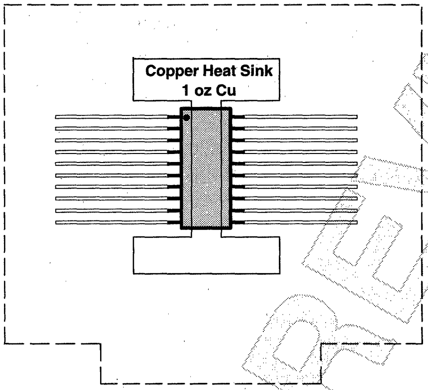


Figure 38. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

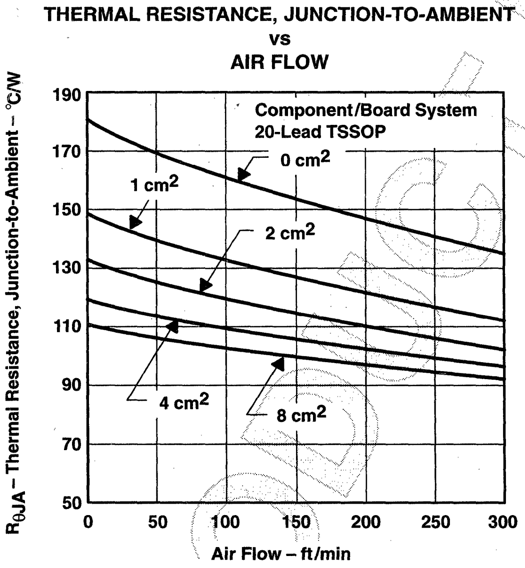


Figure 39

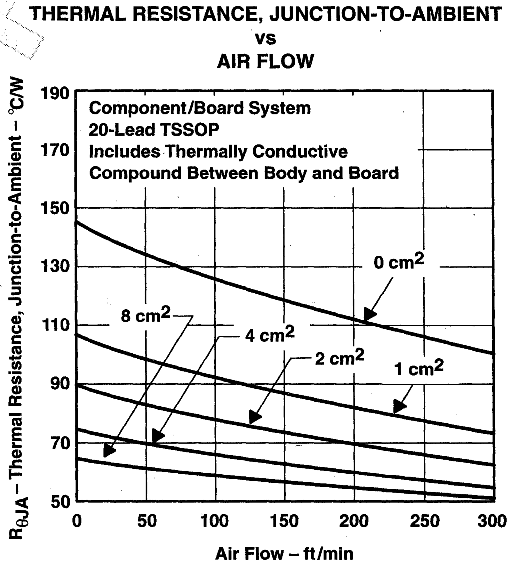


Figure 40

APPLICATION INFORMATION

The TPS73xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier generation LDOs, while adding features such as a power-saving shutdown mode and a supply-voltage supervisor. The TPS73xx family includes three fixed-output voltage regulators: the TPS7333 (3.3 V), the TPS7348 (4.85 V), and the TPS7350 (5 V). The family also offers an adjustable device, the TPS7301 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS73xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that such devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS73xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS73xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power-up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS73xx quiescent current remains low even when the regulator drops out, thus eliminating both problems.

Included in the TPS73xx family is a 4.85-V regulator, the TPS7348. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS73xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 0.5 μA. When the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS73xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS73xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS73xx family requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 41). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figures 28 through 31 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 28 through 31), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73xx family. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

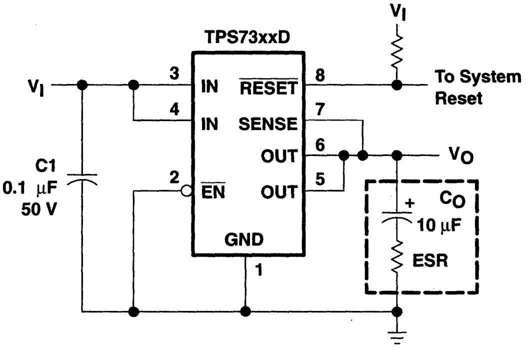


Figure 41. Typical Application Circuit

programming the TPS7301 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 42. The equation governing the output voltage is:

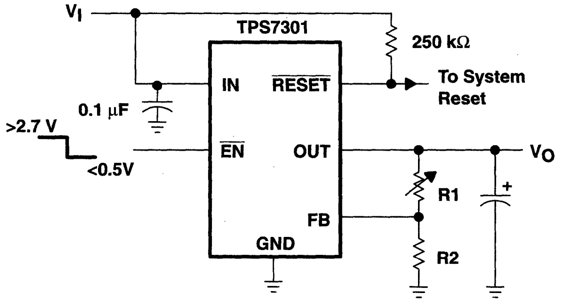
$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

V_{ref} = reference voltage, 1.182 V typ

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 42. TPS7301 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

undervoltage supervisor function

The $\overline{\text{RESET}}$ output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on taking the $\overline{\text{RESET}}$ signal low.

On power-up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typ) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output become inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pull-up resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power-down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-}. Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typ) timeout period.

NOTE:

$V_{IT+} = V_{IT-} + \text{Hysteresis}$

output noise

The TPS73xx has very low output noise, with a spectral noise density < 2 $\mu V/\sqrt{Hz}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

regulator protection

The TPS73xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS73xx also features internal current limiting and thermal protection. During normal operation, the TPS73xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

APPLICATION INFORMATION

power dissipation and junction temperature

The junction temperature must be held to 150°C or less to ensure proper regulator operation, which limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J$max is the maximum allowable junction temperature, i.e.,150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.

μA723C, μA723M, μA723Y
PRECISION VOLTAGE REGULATORS

SLVS057B – AUGUST 1972 – REVISED AUGUST 1995

- **150-mA Load Current Without External Power Transistor**
- **Typically 0.02% Input Regulation and 0.03% Load Regulation (μA723M)**
- **Adjustable Current Limiting Capability**
- **Input Voltages to 40 V**
- **Output Adjustable From 2 V to 37 V**
- **Direct Replacement for Fairchild μA723C and μA723M**

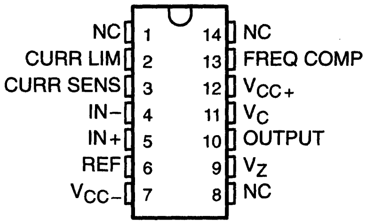
description

The μA723C and μA723M are precision monolithic integrated circuit voltage regulators featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference voltage amplifier, an error amplifier, a 150-mA output transistor, and an adjustable output current limiter.

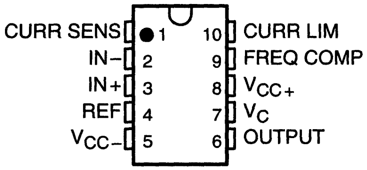
The μA723C and μA723M are designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements may be connected as shown in Figures 4 and 5.

The μA723C is characterized for operation from 0°C to 70°C. The μA723M is characterized for operation over the full military temperature range of –55°C to 125°C.

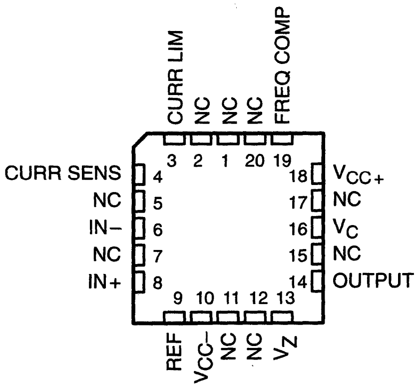
μA723C . . . D OR N PACKAGE
μA723M . . . J PACKAGE
(TOP VIEW)



μA723M . . . U PACKAGE
(TOP VIEW)

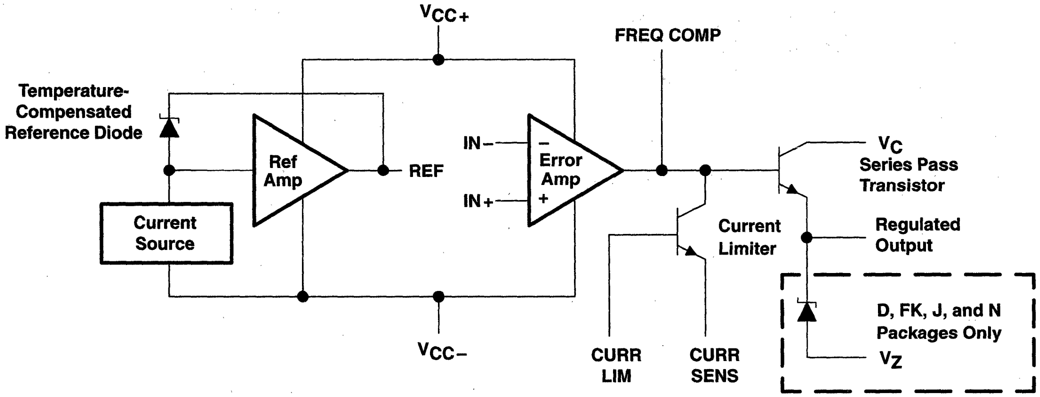


μA723M . . . FK PACKAGE
(TOP VIEW)

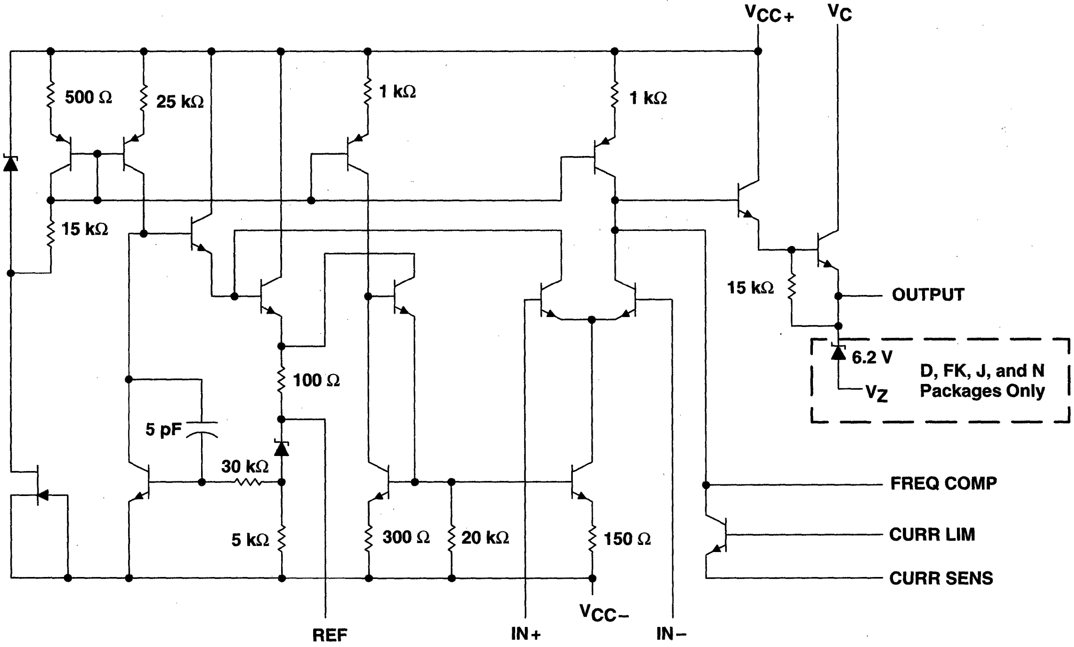


NC – No internal connection

functional block diagram



schematic

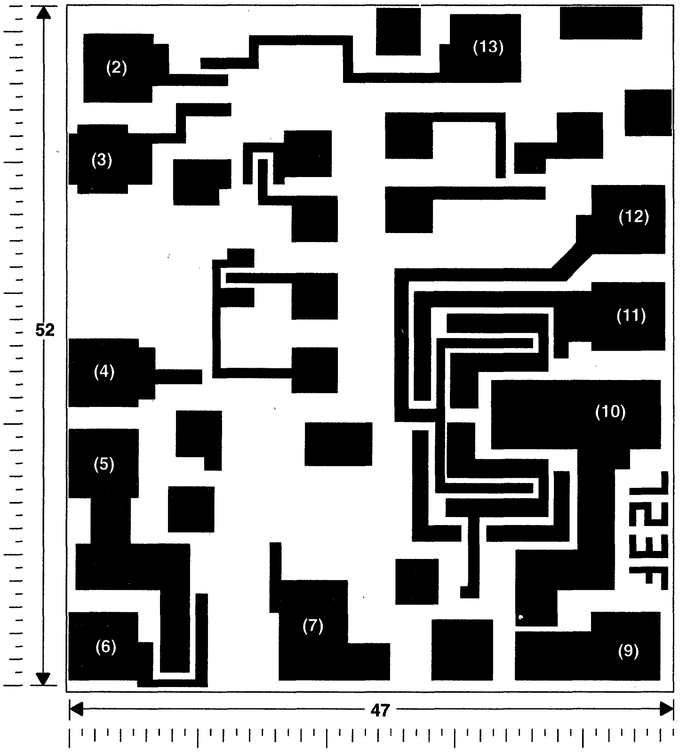


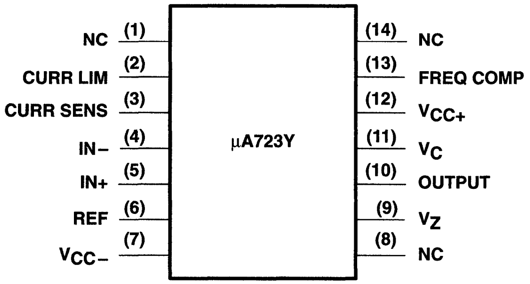
Resistor and capacitor values shown are nominal.

μA723Y chip information

This chip, when properly assembled, displays characteristics similar to the μA723C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1, 8, AND 14 ARE NOT CONNECTED

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Peak voltage from V_{CC+} to V_{CC-} ($t_w \le 50$ ms)	50 V
Continuous voltage from V_{CC+} to V_{CC-}	40 V
Input-to-output voltage differential	40 V
Differential input voltage to error amplifier	±5 V
Voltage between noninverting input and V_{CC-}	8 V
Current from V_Z	25 mA
Current from REF	15 mA
Continuous total dissipation (see Note 1)	See Dissipation Rating Table
Operating free-air temperature range, T_A: μA723C	0°C to 70°C
μA723M	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or U package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Power dissipation = $[I_{(standby)} + I_{(ref)}] V_{CC} + [V_C - V_O] I_O$.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	—
FK and J	1000 mW	11.0 mW/°C	59°C	879 mW	274 mW
N	1000 mW	9.2 mW/°C	41°C	733 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA

electrical characteristics at specified free-air temperature (see Notes 2 and 3)

PARAMETER	TEST CONDITIONS	T_A†	μA723C			μA723M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V	25°C		0.1	1		0.1	1	mV/V
	V_I = 12 V to V_I = 40 V	25°C		1	5		0.2	2	
	V_I = 12 V to V_I = 15 V	Full range			3			3	
Ripple rejection	f = 50 H_Z to 10 kHz, C_{ref} = 0	25°C		74			74		dB
	f = 50 Hz to 10 kHz, C_{ref} = 5 μF	25°C		86			86		
Output regulation		25°C		−0.3	−2		−0.3	−1.5	mV/V
		Full range			−6			−6	
Reference voltage, V_{ref}		25°C	6.8	7.15	7.5	6.95	7.15	7.35	V
Standby current	V_I = 30 V, I_O = 0	25°C		2.3	4		2.3	3.5	mA
Temperature coefficient of output voltage		Full range		0.003	0.015		0.002	0.015*	%/°C
Short-circuit output current	R_{SC} = 10 Ω, V_O = 0	25°C		65			65		mA
Output noise voltage	BW = 100 Hz to 10 kHz, C_{ref} = 0	25°C		20			20		μV
	BW = 100 Hz to 10 kHz, C_{ref} = 5 μF	25°C		2.5			2.5		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full range for μA723C is 0°C to 70°C and for μA723M is −55°C to 125°C.

NOTES: 2. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier ≤ 10 kΩ. Unless otherwise specified, $V_I = V_{CC+} = V_C$ = 12 V, V_{CC-} = 0, V_O = 5 V, I_O = 1 mA, R_{SC} = 0, and C_{ref} = 0.

3. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $T_A = 25°C$ (see Notes 2 and 3)

PARAMETER	TEST CONDITIONS	μA723Y			UNIT
		MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V		0.1		mV/V
	V_I = 12 V to V_I = 40 V		1		
Ripple rejection	f = 50 Hz to 10 kHz, C_{ref} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{ref} = 5 μF		86		
Output regulation			−0.3		mV/V
Reference voltage, V_{ref}			7.15		V
Standby current	V_I = 30 V, I_O = 0		2.3		mA
Short-circuit output current	R_{SC} = 10 Ω, V_O = 0		65		mA
Output noise voltage	BW = 100 Hz to 10 kHz, C_{ref} = 0		20		μV
	BW = 100 Hz to 10 kHz, C_{ref} = 5 μF		2.5		

NOTES: 2. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier ≤ 10 kΩ. Unless otherwise specified, $V_I = V_{CC+} = V_C$ = 12 V, V_{CC-} = 0, V_O = 5 V, I_O = 1 mA, R_{SC} = 0, and C_{ref} = 0.

3. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

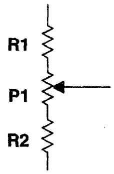
APPLICATION INFORMATION

Table 1. Resistor Values (kΩ) for Standard Output Voltages

OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 4)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 5)			OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 4)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 5)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	P2 (kΩ)			R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	R2 (kΩ)
3.0	1,5,6,9,11, 12 (4)	4.12	3.01	1.8	0.5	1.2	100	7	3.57	105	2.2	10	91
3.6	1,5,6,9,11, 12 (4)	3.57	3.65	1.5	0.5	1.5	250	7	3.57	255	2.2	10	240
5.0	1,5,6,9,11, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (Note 6)	3, 10	3.57	2.43	1.2	0.5	0.75
6.0	1,5,6,9,11, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
9.0	2,4,(5,6, 9,12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
12	2,4,(5,6, 9,12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.57	11.5	1.2	0.5	4.3
15	2,4,(5,6, 9,12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
28	2,4,(5,6, 9,12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
45	7	3.57	48.7	2.2	10	39	−100	8	3.57	95.3	2.2	10	91
75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

NOTES: 4. 4The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use the figure numbers without parentheses. If the divider is across V_O, use the figure numbers in parentheses.

5. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown below.



Adjustable Output Circuit

6. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

APPLICATION INFORMATION

Table 2. Formulas for Intermediate Output Voltages

Outputs from 2 V to 7 V See Figures 1,5,6,9, 11, 12 (4) and Note 4 $V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	Outputs from 4 V to 250 V See Figure 7 and Note 4 $V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1}$ $R3 = R4$	Current Limiting $I_{(limit)} \approx \frac{0.65\ V}{R_{SC}}$
Outputs from 7 V to 37 V See Figures 2,4,(5,6,9, 11, 12) and Note 4 $V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	Outputs from –6 V to –250 V See Figures 3, 8, 10 and Notes 4 and 6 $V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$ $R3 = R4$	Foldback Current Limiting See Figure 6 $I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\ 0.65\ V}{R_{SC} R4}$ $I_{OS} \approx \frac{0.65\ V}{R_{SC}} \times \frac{R3 + R4}{R4}$

NOTES: 4. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use figure numbers without parentheses. If the divider is across V_O, use the figure numbers in parentheses.

6. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than –9 V.

APPLICATION INFORMATION

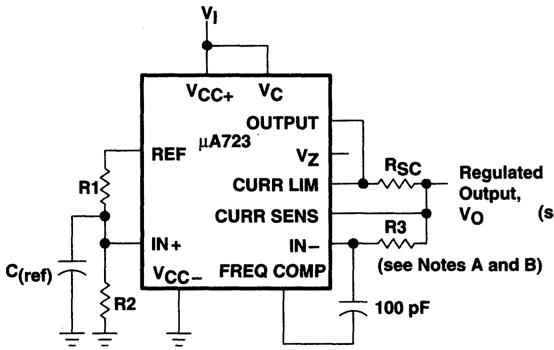


Figure 1. Basic Low-Voltage Regulator (V_O = 2 V to 7 V)

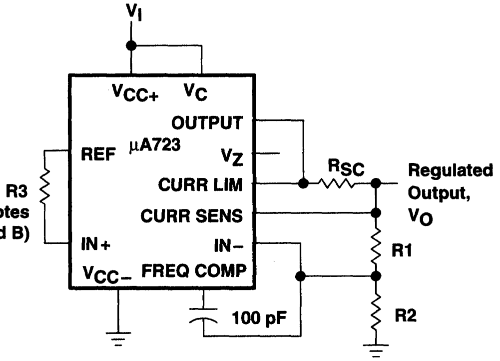


Figure 2. Basic High-Voltage Regulator (V_O = 7 V to 37 V)

NOTES: A. $R3 = \frac{R1 \times R2}{R1 + R2}$ for minimum α_{VO}

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

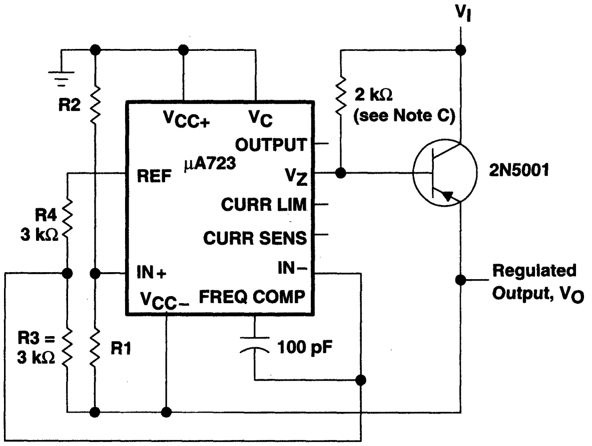


Figure 3. Negative-Voltage Regulator

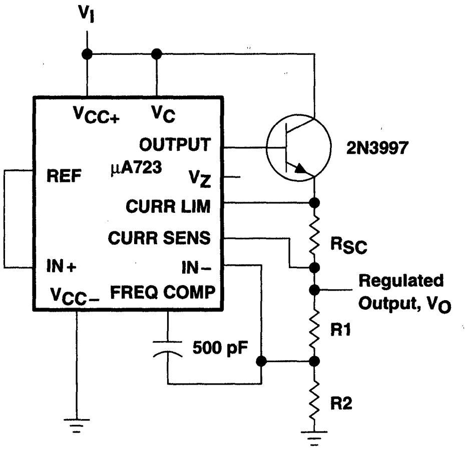


Figure 4. Positive-Voltage Regulator (External N-P-N Pass Terminator)

NOTE C: When 10-lead µA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

APPLICATION INFORMATION

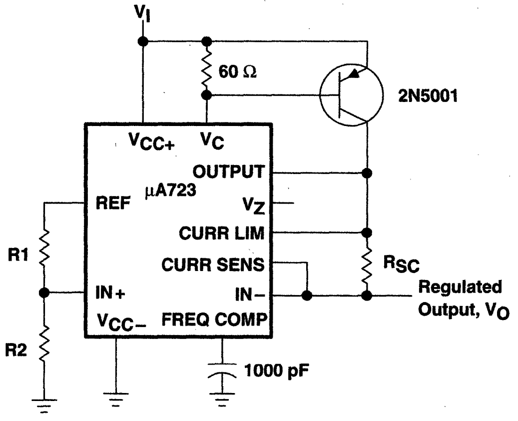


Figure 5. Positive-Voltage Regulator (External P-N-P Pass Transistor)

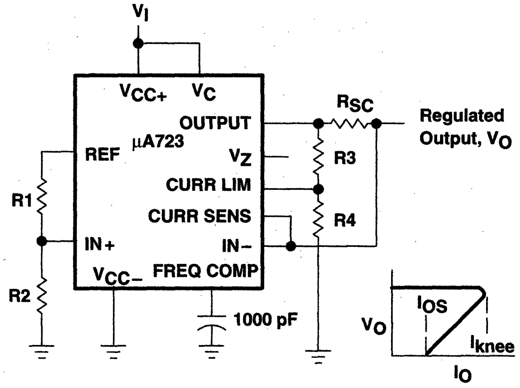


Figure 6. Foldback Current Limiting

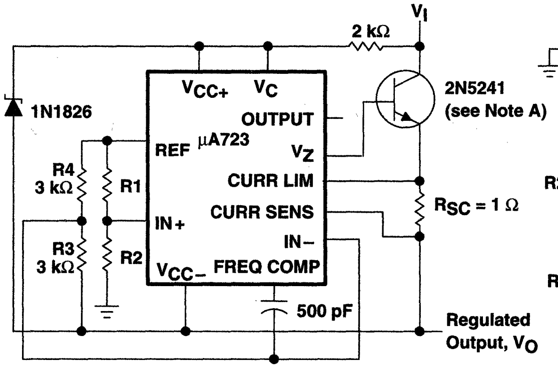


Figure 7. Positive Floating Regulator

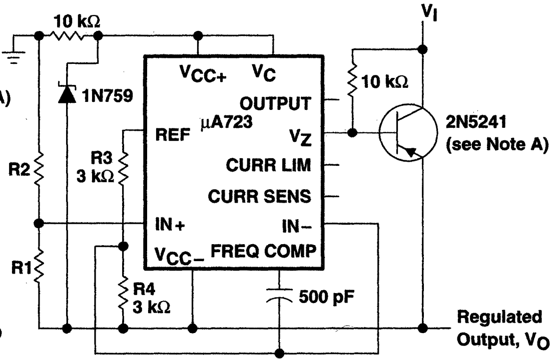


Figure 8. Negative Floating Regulator

NOTE A: When 10-lead µA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

APPLICATION INFORMATION

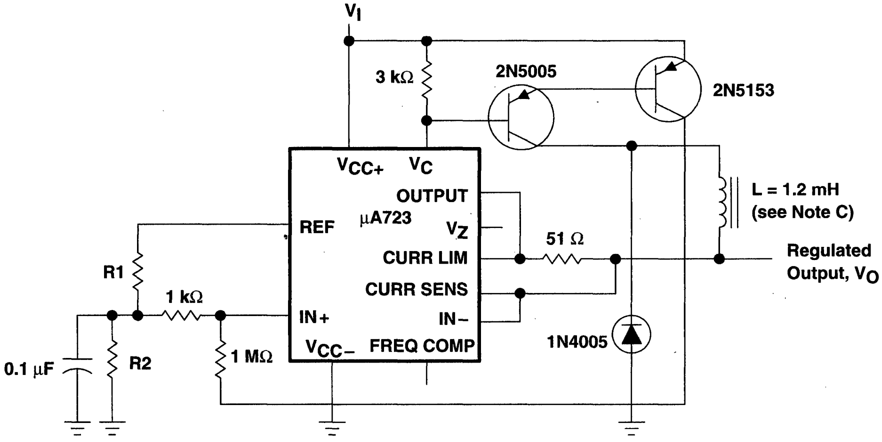


Figure 9. Positive Switching Regulator

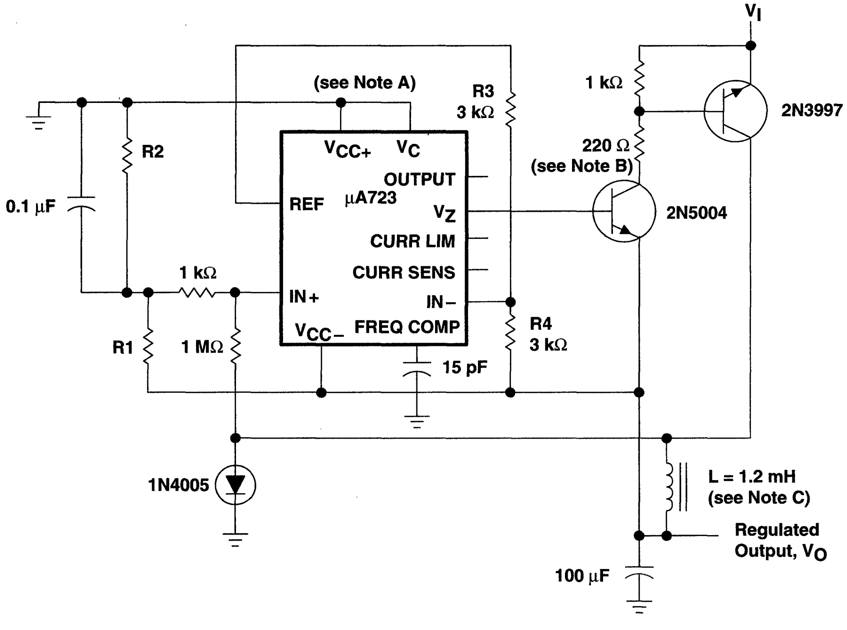
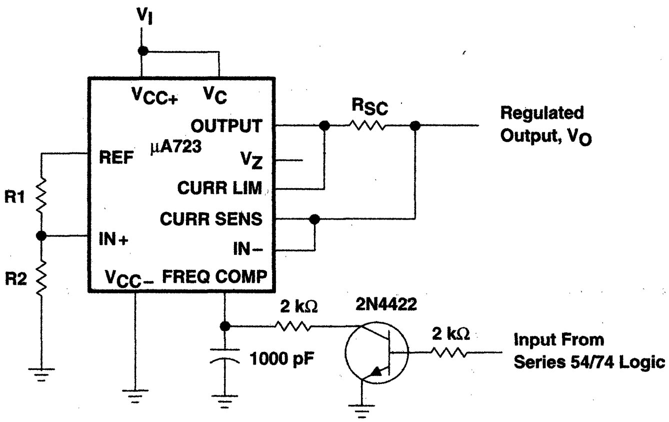


Figure 10. Negative Switching Regulator

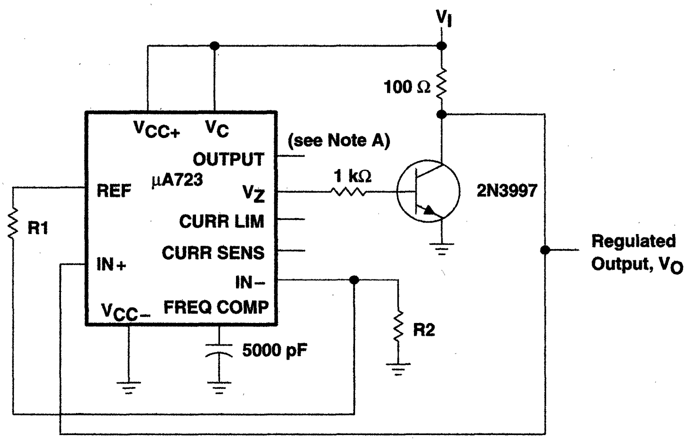
NOTES:
- A. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than –9 V.
- B. When 10-lead µA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.
- C. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core or equivalent, with a 0.009-inch air gap.

APPLICATION INFORMATION



NOTE A: A current-limit transistor may be used for shutdown if current limiting is not required.

Figure 11. Remote Shutdown Regulator With Current Limiting



NOTE A: When 10-lead µA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

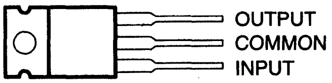
Figure 12. Shunt Regulator

μA7800 SERIES
POSITIVE-VOLTAGE REGULATORS

SLVS056A – MAY 1976 – REVISED AUGUST 1995

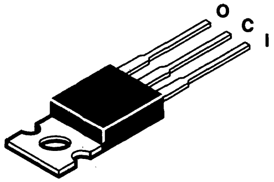
- **3-Terminal Regulators**
- **Output Current Up to 1.5 A**
- **Internal Thermal Overload Protection**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA7800 Series**

KC PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

TO–220AB



description

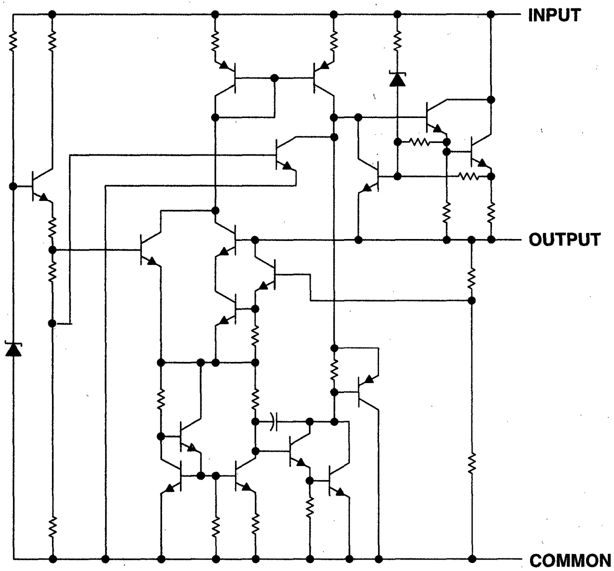
This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also used as the power-pass element in precision regulators.

The μA7800C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The μA7805Q and μA7812Q are characterized for operation over the virtual junction temperature range of −40°C to 125°C.

AVAILABLE OPTIONS

T_J	$V_{O(nom)}$ (V)	PACKAGED DEVICES	CHIP FORM (Y)
		PLASTIC FLANGE-MOUNT (KC)	
0°C to 125°C	5	μA7805CKC	μA7805Y
	6	μA7806CKC	μA7806Y
	8	μA7808CKC	μA7808Y
	8.5	μA7885CKC	μA7885Y
	10	μA7810CKC	μA7810Y
	12	μA7812CKC	μA7812Y
	15	μA7815CKC	μA7815Y
	18	μA7818CKC	μA7818Y
	24	μA7824CKC	μA7824Y
−40°C to 125°C	5	μA7805QKC	—
	12	μA7812QKC	—

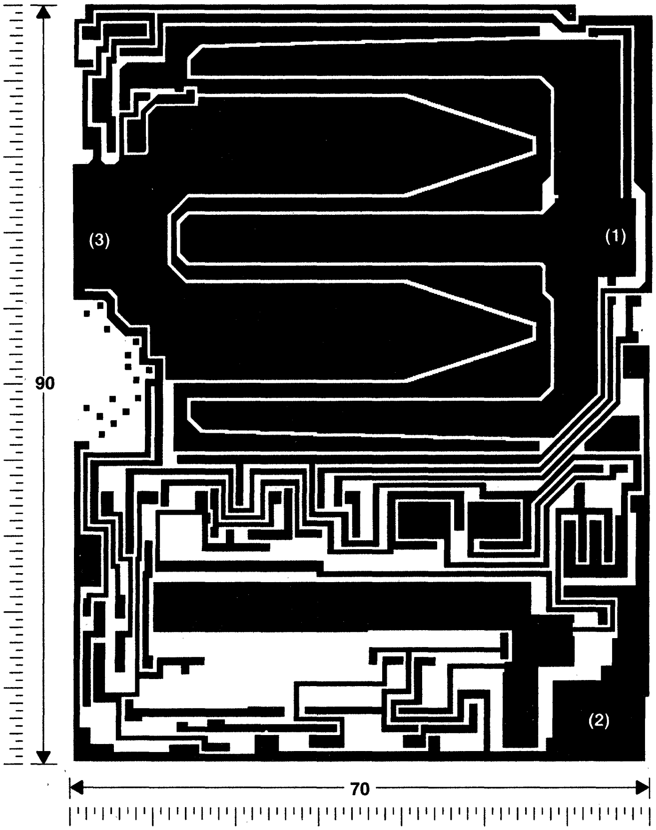
schematic

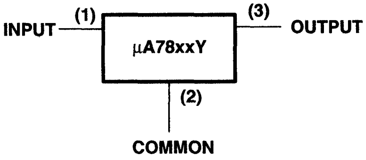


μA78xxY chip information

These chips, when properly assembled, display characteristics similar to the μA78xxC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Input voltage, V_I: µA7824C	40 V
All others	35 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2 W
Continuous total power dissipation at (or below) 90°C case temperature (see Note 1)	15 W
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range	–40 to 150°C
Storage temperature range, T_{stg}	–65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above 25°C free-air or 90°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

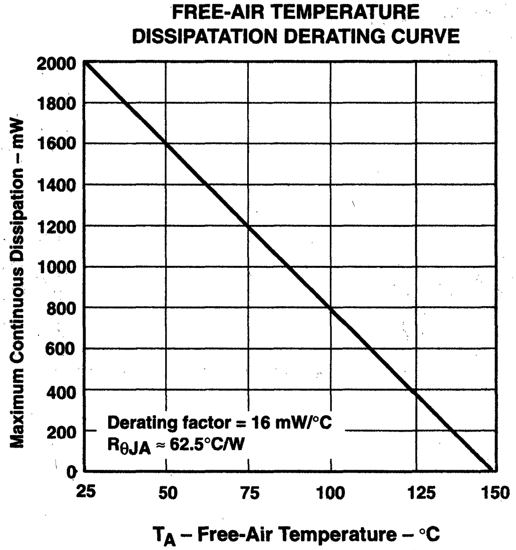

FREE-AIR TEMPERATURE DISSIPATATION DERATING CURVE

Figure 1

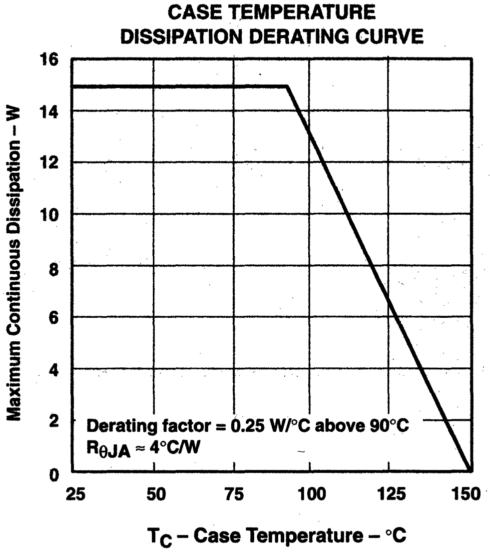

CASE TEMPERATURE DISSIPATION DERATING CURVE

Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	µA7805C	7	25	V
	µA7806C	8	25	
	µA7808C	10.5	25	
	µA7885C	10.5	25	
	µA7810C	12.5	28	
	µA7812C	14.5	30	
	µA7815C	17.5	30	
	µA7818C	21	33	
	µA7824C	27	38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J	µA7800C Series	0	125	°C
	µA7805Q, µA7812Q	−40	125	

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J[†]	µA7805C, µA7805Q			UNIT
			MIN	TYP	MAX	
Output voltage[‡]		25°C	4.8	5	5.2	V
	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, P ≤ 15 W	Full range[§]	4.75		5.25	
Input voltage regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	Full range[§]	62	78		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	Full range[§]		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	Full range[§]		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	Full range[§]			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

[†] Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

[‡] This specification applies only for dc power dissipation permitted by absolute maximum ratings.

[§] Full range virtual junction temperature is 0°C to 125°C for the µA7805C and −40°C to 125°C for the µA7805Q.

electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7806C MIN	µA7806C TYP	µA7806C MAX	UNIT
Output voltage‡		25°C	5.75	6	6.25	V
	I_O = 5 mA to 1 A, V_I = 8 V to 21 V, P ≤ 15 W	0°C to 125°C	5.7		6.3	
Input voltage regulation	V_I = 8 V to 25 V	25°C		5	120	mV
	V_I = 9 V to 13 V			1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	0°C to 125°C	59	75		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		14	120	mV
	I_O = 250 mA to 750 mA			4	60	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		45		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 8 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		550		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7808C MIN	µA7808C TYP	µA7808C MAX	UNIT
Output voltage‡		25°C	7.7	8	8.3	V
	I_O = 5 mA to 1 A, V_I = 10.5 V to 23 V, P ≤ 15 W	0°C to 125°C	7.6		8.4	
Input voltage regulation	V_I = 10.5 V to 25 V	25°C		6	160	mV
	V_I = 11 V to 17 V			2	80	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	55	72		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	160	mV
	I_O = 250 mA to 750 A			4	80	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		52		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 15 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA7885C MIN	μA7885C TYP	μA7885C MAX	UNIT
Output voltage‡		25°C	8.15	8.5	8.85	V
	I_O = 5 mA to 1 A, V_I = 11 V to 23.5 V, P ≤ 15 W	0°C to 125°C	8.1		8.9	
Input voltage regulation	V_I = 10.5 V to 25 V	25°C		6	170	mV
	V_I = 11 V to 17 V			2	85	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	170	mV
	I_O = 250 mA to 750 mA			4	85	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		55		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA7810C MIN	μA7810C TYP	μA7810C MAX	UNIT
Output voltage‡		25°C	9.6	10	10.4	V
	I_O = 5 mA to 1 A, V_I = 12.5 V to 25 V, P ≤ 15 W	0°C to 125°C	9.5	10	10.5	
Input voltage regulation	V_I = 12.5 V to 28 V	25°C		7	200	mV
	V_I = 14 V to 20 V			2	100	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	200	mV
	I_O = 250 mA to 750 mA			4	100	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 12.5 V to 28 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7812C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	11.5	12	12.5	V
	I_O = 5 mA to 1 A, V_I = 14.5 V to 27 V, P ≤ 15 W	Full range§	11.4		12.6	
Input voltage regulation	V_I = 14.5 V to 30 V	25°C		10	240	mV
	V_I = 16 V to 22 V			3	120	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	Full range§	55	71		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	240	mV
	I_O = 250 mA to 750 mA			4	120	
Output resistance	f = 1 kHz	Full range§		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	Full range§		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 14.5 V to 30 V	Full range§			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for the µA7812C and −40°C to 125°C for the µA7812Q.

electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7815C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	14.4	15	15.6	V
	I_O = 5 mA to 1 A, V_I = 17.5 V to 30 V P ≤ 15 W	0°C to 125°C	14.25		15.75	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		11	300	mV
	V_I = 20 V to 26 V			3	150	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	300	mV
	I_O = 250 mA to 750 mA			4	150	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.4	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7818C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	17.3	18	18.7	V
	I_O = 5 mA to 1 A, V_I = 21 V to 33 V, P ≤ 15 W	0°C to 125°C	17.1		18.9	
Input voltage regulation	V_I = 21 V to 33 V	25°C		15	360	mV
	V_I = 24 V to 30 V			5	180	
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz	0°C to 125°C	53	69		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	360	mV
	I_O = 250 mA to 750 mA			4	180	
Output resistance	f = 1 kHz	0°C to 125°C		0.022		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		110		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.5	8	mA
Bias current change	V_I = 21 V to 33 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		200		mA
Peak output current		25°C		2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	µA7824C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	23	24	25	V
	I_O = 5 mA to 1 A, V_I = 27 V to 38 V, P ≤ 15 W	0°C to 125°C	22.8		25.2	
Input voltage regulation	V_I = 27 V to 38 V	25°C		18	480	mV
	V_I = 30 V to 36 V			6	240	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	0°C to 125°C	50	66		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	480	mV
	I_O = 250 mA to 750 mA			4	240	
Output resistance	f = 1 kHz	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		170		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.6	8	mA
Bias current change	V_I = 27 V to 38 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 10$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	µA7805Y MIN	µA7805Y TYP	µA7805Y MAX	UNIT
Output voltage‡			5		V
Input voltage regulation	V_I = 7 V to 25 V		3		mV
	V_I = 8 V to 12 V		1		
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		78		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		15		mV
	I_O = 250 mA to 750 mA		5		
Output resistance	f = 1 kHz		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		40		µV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.2		mA
Short-circuit output current			750		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 11$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	µA7806Y MIN	µA7806Y TYP	µA7806Y MAX	UNIT
Output voltage‡			6		V
Input voltage regulation	V_I = 8 V to 25 V		5		mV
	V_I = 9 V to 13 V		1.5		
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz		75		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		14		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		45		µV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.3		mA
Short-circuit output current			550		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7808Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			8		V
Input voltage regulation	V_I = 10.5 V to 25 V		6		mV
	V_I = 11 V to 17 V		2		
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz		72		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 A		4		
Output resistance	f = 1 kHz		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		52		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.3		mA
Short-circuit output current			450		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 15$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7885Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			8.5		V
Input voltage regulation	V_I = 10.5 V to 25 V		6		mV
	V_I = 11 V to 17 V		2		
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz		70		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		55		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.3		mA
Short-circuit output current			450		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA, T_J = 25°C† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7810Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			10		V
Input voltage regulation	V_I = 12.5 V to 28 V		7		mV
	V_I = 14 V to 20 V		2		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		71		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		70		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.3		mA
Short-circuit output current			400		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA, T_J = 25°C† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7812Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			12		V
Input voltage regulation	V_I = 14.5 V to 30 V		10		mV
	V_I = 16 V to 22 V		3		
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz		71		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		75		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.3		mA
Short-circuit output current			350		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7815Y MIN	μA7815Y TYP	μA7815Y MAX	UNIT
Output voltage‡			15		V
Input voltage regulation	V_I = 17.5 V to 30 V		11		mV
	V_I = 20 V to 26 V		3		
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz		70		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		90		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.4		mA
Short-circuit output current			230		mA
Peak output current			2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 27$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7818Y MIN	μA7818Y TYP	μA7818Y MAX	UNIT
Output voltage‡			18		V
Input voltage regulation	V_I = 21 V to 33 V		15		mV
	V_I = 24 V to 30 V		5		
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz		69		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.022		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		110		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.5		mA
Short-circuit output current			200		mA
Peak output current			2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 33$ V, $I_O = 500$ mA, $T_J = 25°C$† (unless otherwise noted)

PARAMETER	TEST CONDITIONS	μA7824Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			24		V
Input voltage regulation	V_I = 27 V to 38 V		18		mV
	V_I = 30 V to 36 V		6		
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz		66		dB
Output voltage regulation	I_O = 5 mA to 1.5 A		12		mV
	I_O = 250 mA to 750 mA		4		
Output resistance	f = 1 kHz		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA		−1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		170		μV
Dropout voltage	I_O = 1 A		2		V
Bias current			4.6		mA
Short-circuit output current			150		mA
Peak output current			2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

APPLICATION INFORMATION

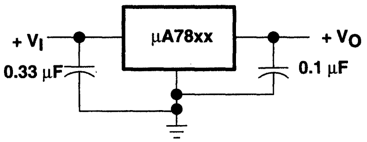


Figure 3. Fixed Output Regulator

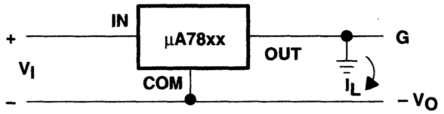
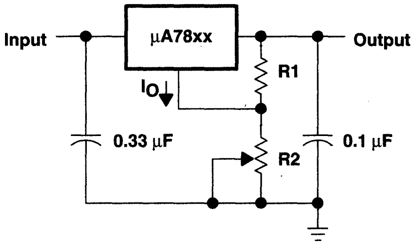


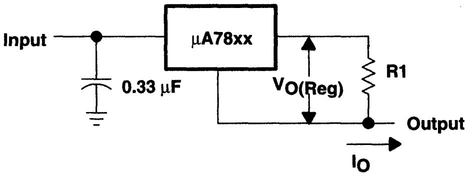
Figure 4. Positive Regulator in Negative Configuration (V_I Must Float)



NOTE A. The following formula is used when Vxx is the nominal output voltage (output to common) of the fixed regulator.

$$V_O = V_{XX} + \left(\frac{V_{XX}}{R1} + I_Q\right) R2$$

Figure 5. Adjustable Output Regulator



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 6. Current Regulator

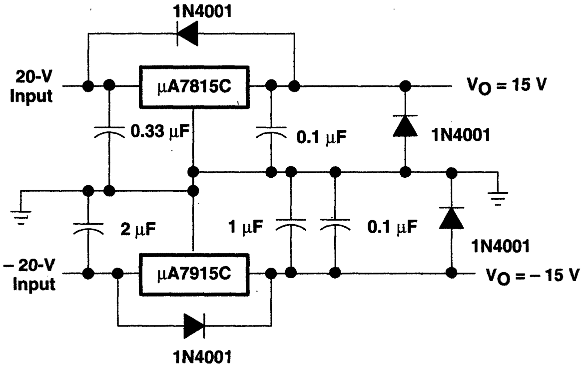


Figure 7. Regulated Dual Supply

APPLICATION INFORMATION

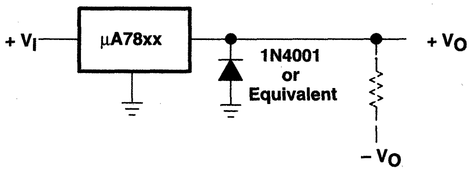


Figure 8. Output Polarity-Reversal Protection Circuit

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., op amps, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 8. This protects the regulator from output polarity reversals during startup and short-circuit operation.

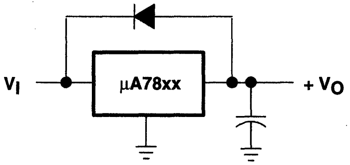


Figure 9. Reverse-Bias Protection Circuit

reverse-bias protection

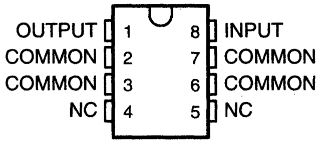
Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 9.

μA78L00 SERIES
POSITIVE-VOLTAGE REGULATORS

SLVS010D – JANUARY 1976 – REVISED OCTOBER 1995

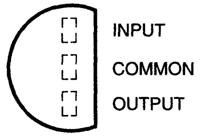
- **3-Terminal Regulators**
- **Output Current Up to 100 mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short-Circuit Current Limiting**
- **Direct Replacements for Fairchild μA78L00 Series**

D PACKAGE
(TOP VIEW)



NC–No internal connection

LP PACKAGE
(TOP VIEW)



TO-226AA

description

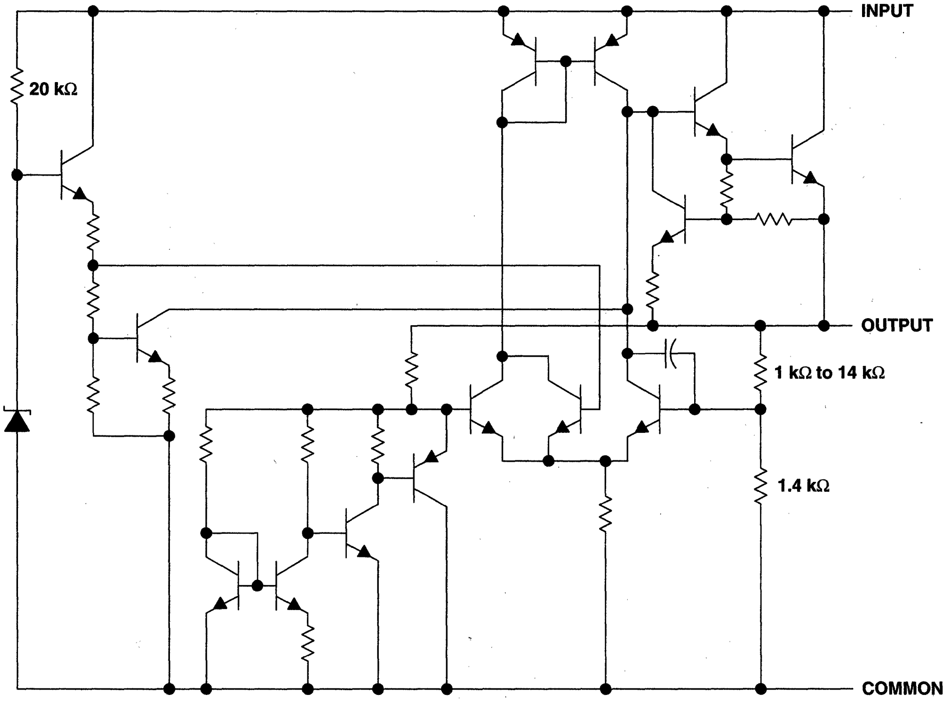
This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a zener diode-resistor combination, an effective improvement in output impedance can be obtained together with lower-bias current.

AVAILABLE OPTIONS

T_J	$V_{O(nom)}$ (V)	PACKAGED DEVICES				CHIP FORM (Y)
		PLASTIC DIP (D)		PLASTIC CYLINDRICAL (LP)		
		OUTPUT VOLTAGE TOLERANCE				
		5%	10%	5%	10%	
0°C to 125°C	2.6	μA78L02ACD	μA78L02CD	μA78L02ACLP	μA78L02CLP	μA78L02Y
	5	μA78L05ACD	μA78L05CD	μA78L05ACLP	μA78L05CLP	μA78L05Y
	6.2	μA78L06ACD	μA78L06CD	μA78L06ACLP	μA78L06CLP	μA78L06Y
	8	μA78L08ACD	μA78L08CD	μA78L08ACLP	μA78L08CLP	μA78L08Y
	9	μA78L09ACD	μA78L09CD	μA78L09ACLP	μA78L09CLP	μA78L09Y
	10	μA78L10ACD	μA78L10CD	μA78L10ACLP	μA78L10CLP	μA78L10Y
	12	μA78L12ACD	μA78L12CD	μA78L12ACLP	μA78L12CLP	μA78L12Y
	15	μA78L15ACD	μA78L15CD	μA78L15ACLP	μA78L15CLP	μA78L15Y
–40°C to 125°C	5	μA78L05AQD	μA78L05QD	μA78L05QLP	μA78L05QLP	—
	12	μA78L12AQD	μA78L12QD	μA78L12QLP	μA78L12QLP	—

D and LP packages are available taped and reeled. Add R suffix to devise type (e.g., μA78L05ACDR).

schematic

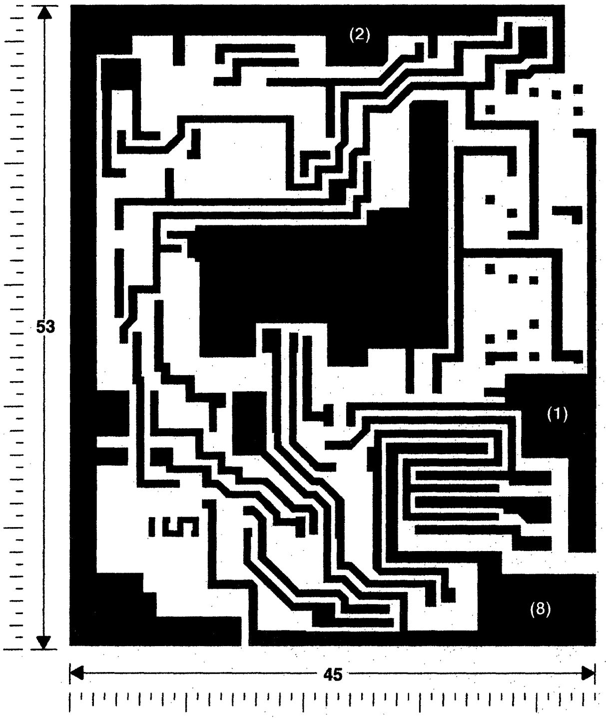


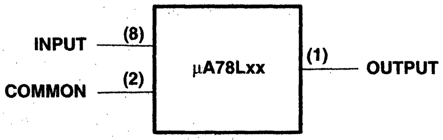
Resistor values shown are nominal.

µA78xxY chip information

These chips, when properly assembled, display characteristics similar to the µA78xxY. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 2,3,6, AND 7 ARE CONNECTED TOGETHER

TERMINALS 4 AND 5 ARE NOT CONNECTED

μA78LxxC absolute maximum ratings over operating temperature range (unless otherwise noted)

	μA78L02C, μA78L02AC THROUGH μA78L10C, μA78L10AC	μA78L12C, μA78L12AC μA78L15C, μA78L15AC	UNIT
Input voltage	30	35	V
Continuous total power dissipation (see Note 1)	See Dissipation Rating Tables 1 and 2		
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range	0 to 125	0 to 125	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

μA78LxxQ absolute maximum ratings over operating temperature range (unless otherwise noted)

	μA78L05Q, μA78L05AQ	μA78L12Q, μA78L12AQ	UNIT
Input voltage	30	35	V
Continuous total power dissipation (see Note 1)	See Dissipation Rating Tables 1 and 2		
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range	−40 to 150	−40 to 150	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW
LP†	775 mW	6.2 mW/°C	25°C	496 mW

† The LP package dissipation rating is based on thermal resistance $R_{\theta JA}$ measured in still air with the device mounted in an Augat socket. The bottom of the package is 10 mm (0.375 in) above the socket.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	19.6 mW/°C	65°C	424 mW
LP	1600 mW	28.6 mW/°C	94°C	713 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA78L02C, μA78L02AC	4.75	20	V
	μA78L05C, μA78L05AC, μA78L05Q, μA78L05AQ	7	20	
	μA78L06C, μA78L06AC	8.5	20	
	μA78L08C, μA78L08AC	10.5	23	
	μA78L09C, μA78L09AC	11.5	24	
	μA78L10C, μA78L10AC	12.5	25	
	μA78L12C, μA78L12AC, μA78L12Q, μA78L12AQ	14.5	27	
	μA78L15C, μA78L15AC	17.5	30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J	μA78LxxC thru μA78LxxAC	0	125	°C
	μA78LxxQ and μA78LxxAQ	−40	125	

electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L02C MIN	μA78L02C TYP	μA78L02C MAX	μA78L02AC MIN	μA78L02AC TYP	μA78L02AC MAX	UNIT
Output voltage‡		25°C	2.4	2.6	2.8	2.5	2.6	2.7	V
	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	Full range§	2.35		2.85	2.45		2.75	
	I_O = 1 mA to 70 mA		2.35		2.85	2.45		2.75	
Input voltage regulation	V_I = 4.75 V to 20 V	25°C		20	125		20	100	mV
	V_I = 5 V to 20 V			16	100		16	75	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz	25°C	42	51		43	51		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		12	50		12	50	mV
	I_O = 1 mA to 40 mA			6	25		6	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30			30		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.6	6		3.6	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	Full range§			2.5			2.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L02, μA78L02AC, μA78L05C, and μA78L05AC and –40°C to 125°C for μA78L05Q and μA78L05AQ.

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L05C, μA78L05Q MIN	μA78L05C, μA78L05Q TYP	μA78L05C, μA78L05Q MAX	μA78L05AC, μA78L05AQ MIN	μA78L05AC, μA78L05AQ TYP	μA78L05AC, μA78L05AQ MAX	UNIT
Output voltage‡		25°C	4.6	5	5.4	4.8	5	5.2	V
	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	Full range§	4.5		5.5	4.75		5.25	
	I_O = 1 mA to 70 mA		4.5		5.5	4.75		5.25	
Input voltage regulation	V_I = 7 V to 20 V	25°C		32	200		32	150	mV
	V_I = 8 V to 20 V			26	150		26	100	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		15	60		15	60	mV
	I_O = 1 mA to 40 mA			8	30		8	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L02, μA78L02AC, μA78L05C, and μA78L05AC and –40°C to 125°C for μA78L05Q and μA78L05AQ.

electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L06C			μA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	Full range§	5.6		6.8	5.9		6.5	
	I_O = 1 mA to 70 mA		5.6		6.8	5.9		6.5	
Input voltage regulation	V_I = 8.5 V to 20 V	25°C		35	200		35	175	mV
	V_I = 9 V to 20 V			29	150		29	125	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	39	48		40	48		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		16	80		16	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L06C, μA78L06AC, μA78L08C, and μA78L08AC.

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L08C			μA78L08AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	7.36	8	8.64	7.7	8	8.3	V
	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	Full range§	7.2		8.8	7.6		8.4	
	I_O = 1 mA to 70 mA		7.2		8.8	7.6		8.4	
Input voltage regulation	V_I = 10.5 V to 23 V	25°C		42	200		42	175	mV
	V_I = 11 V to 23 V			36	150		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	36	46		37	46		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		18	80		18	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L06C, μA78L06AC, μA78L08C, and μA78L08AC.

electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	μA78L09C			μA78L09AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	8.3	9	9.7	8.6	9	9.4	V
	V_I = 12 V to 24 V,	I_O = 1 mA to 40 mA	Full range§	8.1		9.9	8.55		9.45	
	I_O = 1 mA to 70 mA			8.1		9.9	8.55		9.45	
Input voltage regulation	V_I = 12 V to 24 V		25°C		45	225		45	175	mV
	V_I = 13 V to 24 V				40	175		40	125	
Ripple rejection	V_I = 15 V to 25 V,	f = 120 Hz	25°C	36	45		38	45		dB
Output voltage regulation	I_O = 1 mA to 100 mA		25°C		19	90		19	90	mV
	I_O = 1 mA to 40 mA				11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz		25°C		58			58		μV
Dropout voltage			25°C		1.7			1.7		V
Bias current			25°C		4.1	6		4.1	6	mA
			125°C			5.5			5.5	
Bias current change	V_I = 13 V to 24 V		Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA					0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L09C, μA78L09AC, μA78L10C, and μA78L10AC.

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	μA78L10C			μA78L10AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	9.2	10	10.8	9.6	10	10.4	V
	V_I = 13 V to 25 V,	I_O = 1 mA to 40 mA	Full range§	9		11	9.5		10.5	
	I_O = 1 mA to 70 mA			9		11	9.5		10.5	
Input voltage regulation	V_I = 13 V to 25 V		25°C		51	225		51	175	mV
	V_I = 14 V to 25 V				42	175		42	125	
Ripple rejection	V_I = 15 V to 25 V,	f = 120 Hz	25°C	36	44		37	44		dB
Output voltage regulation	I_O = 1 mA to 100 mA		25°C		20	90		20	90	mV
	I_O = 1 mA to 40 mA				11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz		25°C		62			62		μV
Dropout voltage			25°C		1.7			1.7		V
Bias current			25°C		4.2	6		4.2	6	mA
			125°C			5.5			5.5	
Bias current change	V_I = 14 V to 25 V		Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA					0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L09C, μA78L09AC, μA78L10C, and μA78L10AC.

electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L12C, μA78L12Q			μA78L12AC, μA78L12AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	11.1	12	12.9	11.5	12	12.5	V
	V_I = 14 V to 27 V, I_O = 1 mA to 40 mA	Full range§	10.8		13.2	11.4		12.6	
	I_O = 1 mA to 70 mA		10.8		13.2	11.4		12.6	
Input voltage regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			49	200		49	200	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		22	100		22	100	mV
	I_O = 1 mA to 40 mA			13	50		13	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L12C, μA78L12AC, μA78L15C, and μA78L15AC.

electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA78L15C			μA78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	13.8	15	16.2	14.4	15	15.6	V
	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	Full range§	13.5		16.5	14.25		15.75	
	I_O = 1 mA to 70 mA		13.5		16.5	14.25		15.75	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		65	300		65	300	mV
	V_I = 20 V to 30 V			58	250		58	250	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output voltage regulation	I_O = 1 mA to 100 mA	25°C		25	150		25	150	mV
	I_O = 1 mA to 40 mA			15	75		15	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	V_I = 10 V to 30 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for μA78L12C, μA78L12AC, μA78L15C, and μA78L15AC.

electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L02Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			2.6		V
Input voltage regulation	V_I = 4.75 V to 20 V		20		mV
	V_I = 5 V to 20 V		16		
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz		51		dB
Output voltage regulation	I_O = 1 mA to 100 mA		12		mV
	I_O = 1 mA to 40 mA		6		
Output noise voltage	f = 10 Hz to 100 kHz		30		μV
Dropout voltage			1.7		V
Bias current			3.6		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L05Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			5		V
Input voltage regulation	V_I = 7 V to 20 V		32		mV
	V_I = 8 V to 20 V		26		
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		49		dB
Output voltage regulation	I_O = 1 mA to 100 mA		15		mV
	I_O = 1 mA to 40 mA		8		
Output noise voltage	f = 10 Hz to 100 kHz		42		μV
Dropout voltage			1.7		V
Bias current			3.8		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L06Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			6.2		V
Input voltage regulation	V_I = 8.5 V to 20 V		35		mV
	V_I = 9 V to 20 V		29		
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz		48		dB
Output voltage regulation	I_O = 1 mA to 100 mA		16		mV
	I_O = 1 mA to 40 mA		9		
Output noise voltage	f = 10 Hz to 100 kHz		46		μV
Dropout voltage			1.7		V
Bias current			3.9		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 40$ mA, $T_A = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L08Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			8		V
Input voltage regulation	V_I = 10.5 V to 23 V		42		mV
	V_I = 11 V to 23 V		36		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		46		dB
Output voltage regulation	I_O = 1 mA to 100 mA		18		mV
	I_O = 1 mA to 40 mA		10		
Output noise voltage	f = 10 Hz to 100 kHz		54		μV
Dropout voltage			1.7		V
Bias current			4		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 16$ V, $I_O = 40$ mA, $T_A = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L09Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			9		V
Input voltage regulation	V_I = 12 V to 24 V		45		mV
	V_I = 13 V to 24 V		40		
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz		45		dB
Output voltage regulation	I_O = 1 mA to 100 mA		19		mV
	I_O = 1 mA to 40 mA		11		
Output noise voltage	f = 10 Hz to 100 kHz		58		μV
Dropout voltage			1.7		V
Bias current			4.1		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 40$ mA, $T_A = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L10Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			10		V
Input voltage regulation	V_I = 13 V to 25 V		51		mV
	V_I = 14 V to 25 V		42		
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz		44		dB
Output voltage regulation	I_O = 1 mA to 100 mA		20		mV
	I_O = 1 mA to 40 mA		11		
Output noise voltage	f = 10 Hz to 100 kHz		62		μV
Dropout voltage			1.7		V
Bias current			4.2		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 19$ V, $I_O = 40$ mA, $T_A = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	µA78L12Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			12		V
Input voltage regulation	V_I = 14.5 V to 27 V		55		mV
	V_I = 16 V to 27 V		49		
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz		42		dB
Output voltage regulation	I_O = 1 mA to 100 mA		22		mV
	I_O = 1 mA to 40 mA		13		
Output noise voltage	f = 10 Hz to 100 kHz		70		µV
Dropout voltage			1.7		V
Bias current			4.3		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 40$ mA, $T_A = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	µA78L15Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			15		V
Input voltage regulation	V_I = 17.5 V to 30 V		65		mV
	V_I = 20 V to 30 V		58		
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz		39		dB
Output voltage regulation	I_O = 1 mA to 100 mA		25		mV
	I_O = 1 mA to 40 mA		15		
Output noise voltage	f = 10 Hz to 100 kHz		82		µV
Dropout voltage			1.7		V
Bias current			4.6		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

APPLICATION INFORMATION

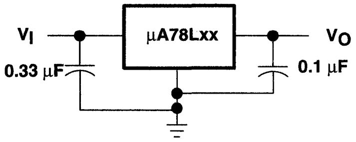


Figure 1. Fixed Output Regulator

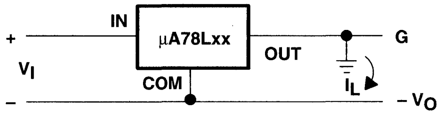


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

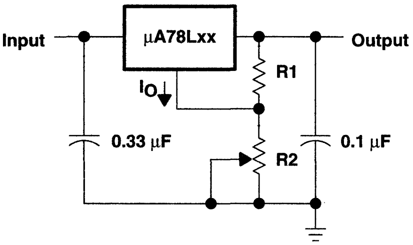
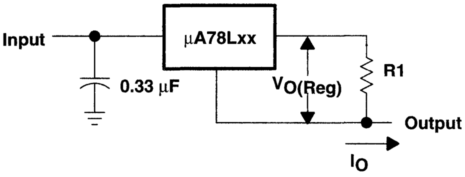


Figure 3. Adjustable Output Regulator



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 4. Current Regulator

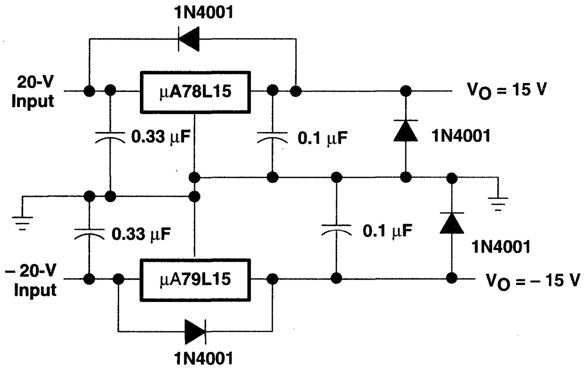


Figure 5. Regulated Dual Supply

APPLICATION INFORMATION

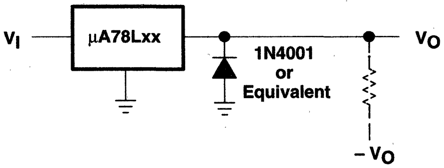


Figure 6. Output Polarity-Reversal Protection Circuit

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

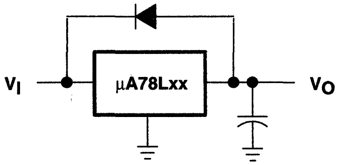


Figure 7. Reverse-Bias Protection Circuit

reverse-bias protection

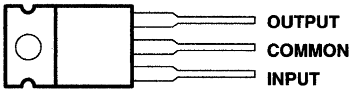
Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 7.

μA78M00 SERIES
POSITIVE-VOLTAGE REGULATORS

SLVS059A – JUNE 1976 – REVISED AUGUST 1995

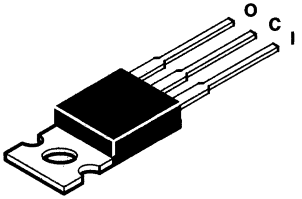
- **3-Terminal Regulators**
- **Output Current Up to 500 mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA78M00 Series**

KC PACKAGE
(TOP VIEW)

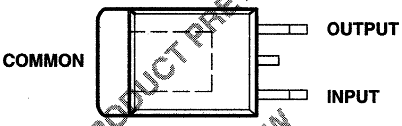


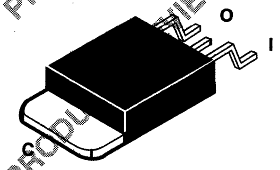
The common terminal is in electrical contact with the mounting base.

TO–220AB



KTP PACKAGE
(TOP VIEW)





description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

AVAILABLE OPTIONS

T_A	V_O(nom) (V)	PACKAGED DEVICES		CHIP FORM (Y)
		HEAT-SINK MOUNTED (KC)	HEAT-SINK MOUNTED† (KTP)	
0°C to 125°C	5	μA78M05CKC	μA78M05CKTP	μA78M05Y
	6	μA78M06CKC	μA78M06CKTP	μA78M06Y
	8	μA78M08CKC	μA78M08CKTP	μA78M08Y
	9	μA78M09CKC	μA78M09CKTP	μA78M09Y
	10	μA78M10CKC	μA78M10CKTP	μA78M10Y
	12	μA78M12CKC	μA78M12CKTP	μA78M12Y
	15	μA78M15CKC	μA78M15CKTP	μA78M15Y
	20	μA78M20CKC	μA78M20CKTP	μA78M20Y
	24	μA78M24CKC	μA78M24CKTP	μA78M24Y

† The KTP package is only available in tape and reel.

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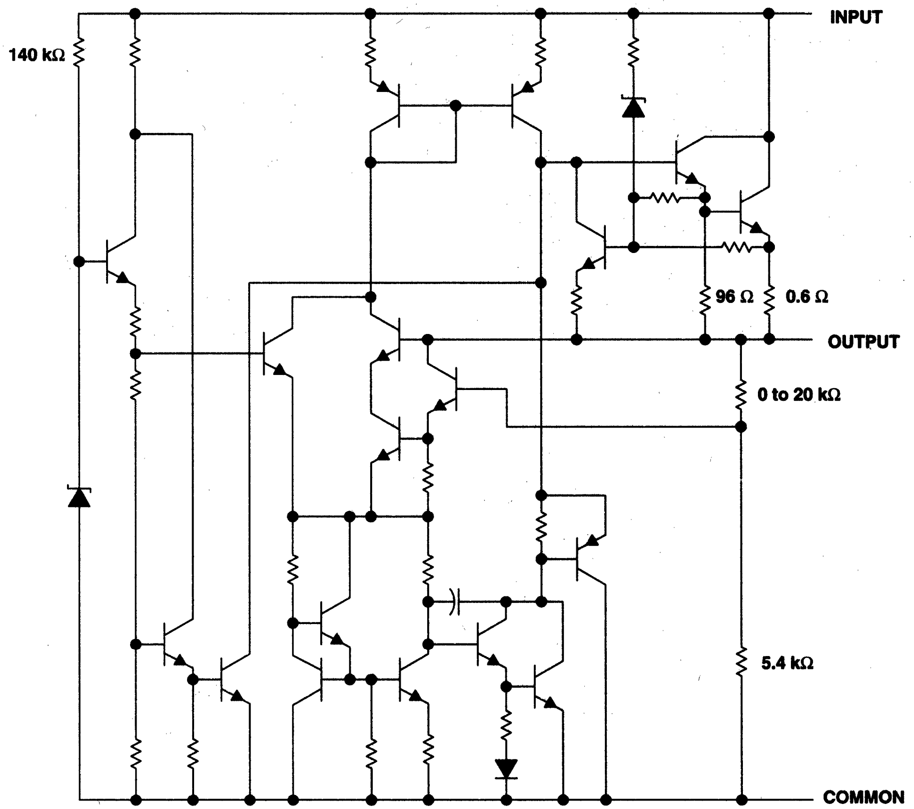
schematic

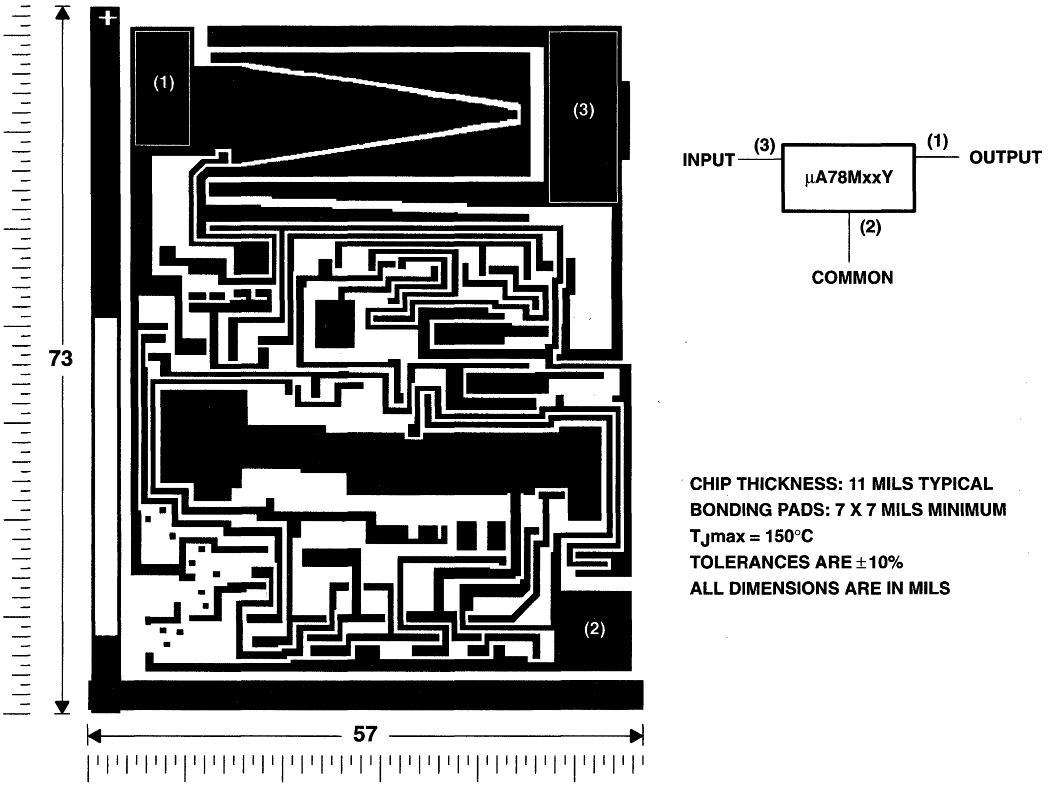


Resistor values shown are nominal.

µA78MxxY chip information

This chip, when properly assembled, displays characteristics similar to the µA78MxxC. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 11 MILS TYPICAL
BONDING PADS: 7 X 7 MILS MINIMUM
$T_J$max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating temperature range (unless otherwise noted)†

		µA78Mxx	UNIT
Input voltage, V_I	µA78M20, µA78M24	−40	V
	All others	35	
Continuous total power dissipation (see Note 1)		See Dissipation Rating Tables 1 and 2	
Operating free-air (T_A), case (T_C), or virtual junction (T_J) temperature range		0 to 150	°C
Storage temperature range, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
KC	2000 mW	16 mW/°C	1280 mW
KTP†			

† The KTP package is product preview only and derating information is not yet available.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \leq 50°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 50°C$	$T_C = 125°C$ POWER RATING
KC	20 W	200 mW/°C	5 W
KTP†			

† The KTP package is product preview only and derating information is not yet available.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	µA78M05	7	25	V
	µA78M06	8	25	
	µA78M08	10.5	25	
	µA78M09	11.5	26	
	µA78M10	12.5	28	
	µA78M12	14.5	30	
	µA78M15	17.5	30	
	µA78M20	23	35	
	µA78M24	27	38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M05C			UNIT
			MIN	TYP	MAX	
Output voltage‡			4.8	5	5.2	V
	V_I = 7 V to 20 V,	T_J = 0°C to 125°C	4.75		5.25	
Input voltage regulation	I_O = 200 mA	V_I = 7 V to 25 V		3	100	mV
		V_I = 8 V to 20 V				
		V_I = 8 V to 25 V		1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	62			dB
		I_O = 300 mA	62	80		
Output voltage regulation	I_O = 5 mA to 500 mA			20	100	mV
	I_O = 5 mA to 200 mA			10	50	
Temperature coefficient of output voltage	I_O = 5 mA	T_J = 0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			40	200	μV
Dropout voltage				2	2.5	V
Bias current				4.5	6	mA
Bias current change	I_O = 200 mA, T_J = 0°C to 125°C	V_I = 8 V to 25 V,			0.8	mA
	I_O = 5 mA to 350 mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V			300		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M06C			UNIT
			MIN	TYP	MAX	
Output voltage‡			5.75	6	6.25	V
	I_O = 5 mA to 350 mA, V_I = 8 V to 21 V, T_J = 0°C to 125°C		5.7		6.3	
Input voltage regulation	I_O = 200 mA	V_I = 8 V to 25 V		5	100	mV
		V_I = 9 V to 25 V		1.5	50	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	59			dB
		I_O = 300 mA	59	80		
Output voltage regulation	I_O = 5 mA to 500 mA			20	120	mV
	I_O = 5 mA to 200 mA			10	60	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			45		μV
Dropout voltage				2		V
Bias current				4.5	6	mA
Bias current change	V_I = 9 V to 25 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			270		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M08C			UNIT
			MIN	TYP	MAX	
Output voltage‡			7.7	8	8.3	V
	V_I = 10.5 V to 23 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		7.6		8.4	
Input voltage regulation	I_O = 200 mA	V_I = 10.5 V to 25 V		6	100	mV
		V_I = 11 V to 25 V		2	50	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	56			dB
		I_O = 300 mA	56	80		
Output voltage regulation	I_O = 5 mA to 500 mA			25	160	mV
	I_O = 5 mA to 200 mA			10	80	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			52		μV
Dropout voltage				2		V
Bias current				4.6	6	mA
Bias current change	V_I = 10.5 V to 25 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			250		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M09C			UNIT
			MIN	TYP	MAX	
Output voltage‡			8.6	9	9.4	V
	V_I = 11.5 V to 24 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		8.5		9.5	
Input voltage regulation	I_O = 200 mA	V_I = 11.5 V to 26 V		6	100	mV
		V_I = 12 V to 26 V		2	50	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	56			dB
		I_O = 300 mA	56	80		
Output voltage regulation	I_O = 5 mA to 500 mA			25	180	mV
	I_O = 5 mA to 200 mA			10	90	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			58		μV
Dropout voltage				2		V
Bias current				4.6	6	mA
Bias current change	V_I = 11.5 V to 26 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			250		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M10C			UNIT
			MIN	TYP	MAX	
Output voltage‡			9.6	10	10.4	V
	V_I = 12.5 V to 25 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		9.5		10.5	
Input voltage regulation	I_O = 200 mA	V_I = 12.5 V to 28 V		7	100	mV
		V_I = 14 V to 28 V		2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	59			dB
		I_O = 300 mA	55	80		
Output voltage regulation	I_O = 5 mA to 500 mA			25	200	mV
	I_O = 5 mA to 200 mA			10	100	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			64		μV
Dropout voltage				2		V
Bias current				4.7	6	mA
Bias current change	V_I = 12.5 V to 28 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			245		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M12C			UNIT
			MIN	TYP	MAX	
Output voltage‡			11.5	12	12.5	V
	V_I = 14.5 V to 27 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		11.4		12.6	
Input voltage regulation	I_O = 200 mA	V_I = 14.5 V to 30 V		8	100	mV
		V_I = 16 V to 30 V		2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	55			dB
		I_O = 300 mA	55	80		
Output voltage regulation	I_O = 5 mA to 500 mA			25	240	mV
	I_O = 5 mA to 200 mA			10	120	
Temperature coefficient of output voltage	I_O = 5 mA			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			75		μV
Dropout voltage				2		V
Bias current				4.8	6	mA
Bias current change	V_I = 14.5 V to 30 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M15C			UNIT
			MIN	TYP	MAX	
Output voltage‡			14.4	15	15.6	V
	V_I = 17.5 V to 30 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		14.25		15.75	
Input voltage regulation	I_O = 200 mA	V_I = 17.5 V to 30 V		10	100	mV
		V_I = 20 V to 30 V		3	50	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	54			dB
		I_O = 300 mA	54	70		
Output voltage regulation	I_O = 5 mA to 500 mA			25	300	mV
	I_O = 5 mA to 200 mA			10	150	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			90		μV
Dropout voltage				2		V
Bias current				4.8	6	mA
Bias current change	V_I = 17.5 V to 30 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 29 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M20C			UNIT
			MIN	TYP	MAX	
Output voltage‡			19.2	20	20.8	V
	V_I = 23 V to 35 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		19		21	
Input voltage regulation	I_O = 200 mA	V_I = 23 V to 35 V		10	100	mV
		V_I = 24 V to 35 V		5	50	
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	53			dB
		I_O = 300 mA	53	70		
Output voltage regulation	I_O = 5 mA to 500 mA			30	400	mV
	I_O = 5 mA to 200 mA			10	200	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			110		μV
Dropout voltage				2		V
Bias current				4.9	6	mA
Bias current change	V_I = 23 V to 35 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA78M24C			UNIT
			MIN	TYP	MAX	
Output voltage‡			23	24	25	V
	V_I = 27 V to 38 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		22.8		25.2	
Input voltage regulation	I_O = 200 mA	V_I = 27 V to 38 V		10	100	mV
		V_I = 28 V to 38 V		5	50	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	50			dB
		I_O = 300 mA	50	70		
Output voltage regulation	I_O = 5 mA to 500 mA			30	480	mV
	I_O = 5 mA to 200 mA			10	240	
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1.2		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			170		µV
Dropout voltage				2		V
Bias current				5	6	mA
Bias current change	V_I = 27 V to 38 V, I_O = 200 mA, T_J = 0°C to 125°C				0.8	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.5	
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 10$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M05Y			UNIT
			MIN	TYP	MAX	
Output voltage‡				5		V
Input voltage regulation	I_O = 200 mA	V_I = 7 V to 25 V		3		mV
		V_I = 8 V to 25 V		1		
Ripple rejection	V_I = 8 V to 18 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			20		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			40		μV
Dropout voltage				2		V
Bias current				4.5		mA
Short-circuit output current	V_I = 35 V			300		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 11$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M06Y			UNIT
			MIN	TYP	MAX	
Output voltage‡				6		V
Input voltage regulation	I_O = 200 mA	V_I = 8 V to 25 V		5		mV
		V_I = 9 V to 25 V		1.5		
Ripple rejection	V_I = 9 V to 19 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			20		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			45		μV
Dropout voltage				2		V
Bias current				4.5		mA
Short-circuit output current	V_I = 35 V			270		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M08Y			UNIT
			MIN	TYP	MAX	
Output voltage‡				8		V
Input voltage regulation	I_O = 200 mA	V_I = 10.5 V to 25 V		6		mV
		V_I = 11 V to 25 V		2		
Ripple rejection	V_I = 11.5 V to 21.5 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			25		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			52		μV
Dropout voltage				2		V
Bias current				4.6		mA
Short-circuit output current	V_I = 35 V			250		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 16$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M09Y			UNIT
			MIN	TYP	MAX	
Output voltage‡				9		V
Input voltage regulation	I_O = 200 mA	V_I = 11.5 V to 26 V		6		mV
		V_I = 12 V to 26 V		2		
Ripple rejection	V_I = 13 V to 23 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			25		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			58		μV
Dropout voltage				2		V
Bias current				4.6		mA
Short-circuit output current	V_I = 35 V			250		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 17$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]		μA78M10Y			UNIT
			MIN	TYP	MAX	
Output voltage[‡]				10		V
Input voltage regulation	I_O = 200 mA	V_I = 12.5 V to 28 V		7		mV
		V_I = 14 V to 28 V		2		
Ripple rejection	V_I = 15 V to 25 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			25		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			64		μV
Dropout voltage				2		V
Bias current				4.7		mA
Short-circuit output current	V_I = 35 V			245		mA
Peak output current				0.7		A

[†] All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

[‡] This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 9$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]		μA78M12Y			UNIT
			MIN	TYP	MAX	
Output voltage[‡]				12		V
Input voltage regulation	I_O = 200 mA	V_I = 14.5 V to 30 V		8		mV
		V_I = 16 V to 30 V		2		
Ripple rejection	V_I = 15 V to 25 V, I_O = 300 mA, f = 120 Hz			80		dB
Output voltage regulation	I_O = 5 mA to 500 mA			25		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			75		μV
Dropout voltage				2		V
Bias current				4.8		mA
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

[†] All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

[‡] This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M15C			UNIT
			MIN	TYP	MAX	
Output voltage‡				15		V
Input voltage regulation	I_O = 200 mA	V_I = 17.5 V to 30 V		10		mV
		V_I = 20 V to 30 V		3		
Ripple rejection	V_I = 18.5 V to 28.5 V, I_O = 300 mA, f = 120 Hz			70		dB
Output voltage regulation	I_O = 5 mA to 500 mA			25		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			90		μV
Dropout voltage				2		V
Bias current				4.8		mA
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = 29$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M20C			UNIT
			MIN	TYP	MAX	
Output voltage‡				20		V
Input voltage regulation	I_O = 200 mA	V_I = 23 V to 35 V		10		mV
		V_I = 24 V to 35 V		5		
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz, I_O = 300 mA			70		dB
Output voltage regulation	I_O = 5 mA to 500 mA			30		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			110		μV
Dropout voltage				2		V
Bias current				4.9		mA
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M24Y MIN	μA78M24Y TYP	μA78M24Y MAX	UNIT
Output voltage‡				24		V
Input voltage regulation	I_O = 200 mA	V_I = 27 V to 38 V		10		mV
		V_I = 28 V to 38 V		5		
Ripple rejection	V_I = 28 V to 38 V, I_O = 300 mA, f = 120 Hz			70		dB
Output voltage regulation	I_O = 5 mA to 500 mA			30		mV
	I_O = 5 mA to 200 mA			10		
Temperature coefficient of output voltage	I_O = 5 mA			−1.2		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			170		μV
Dropout voltage				2		V
Bias current				5		mA
Short-circuit output current	V_I = 35 V			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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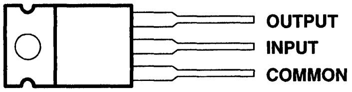
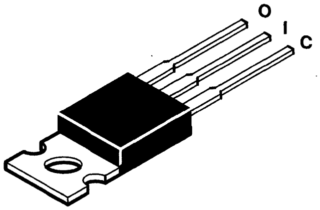
KC PACKAGE
(TOP VIEW)

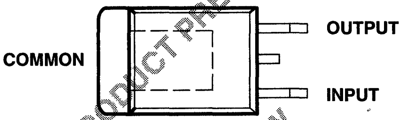


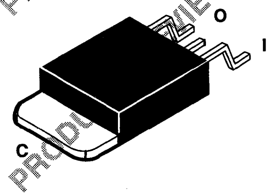
The input terminal is in electrical contact with the mounting base.

TO-220AB



KTP PACKAGE
(TOP VIEW)





description

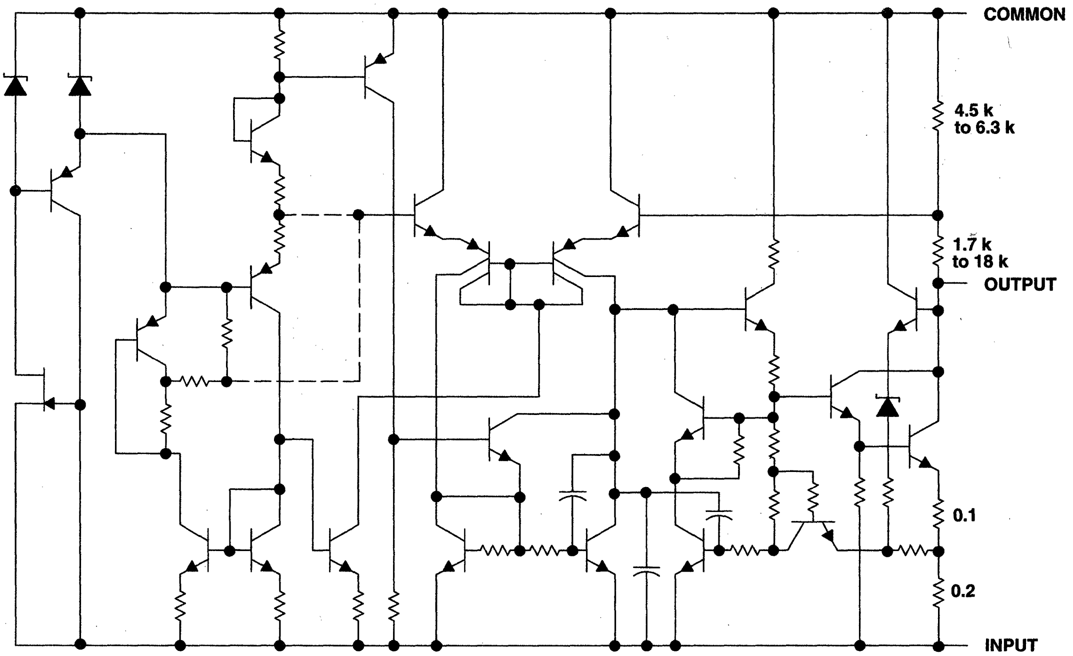
This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement the µA78M00 series in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

AVAILABLE OPTIONS

T_A	V_O(nom) (V)	PACKAGED DEVICES		CHIP FORM (Y)
		HEAT-SINK MOUNTED (KC)	HEAT-SINK MOUNTED† (KTP)	
0°C to 125°C	–5	µA79M05CKC	µA79M05CKTP	µA79M05Y
	–6	µA79M06CKC	µA79M06CKTP	µA79M06Y
	–8	µA79M08CKC	µA79M08CKTP	µA79M08Y
	–12	µA79M12CKC	µA79M12CKTP	µA79M12Y
	–15	µA79M15CKC	µA79M15CKTP	µA79M15Y
	–20	µA79M20CKC	µA79M20CKTP	µA79M20Y
	–24	µA79M24CKC	µA79M24CKTP	µA79M24Y

† The KTP package is only available in tape and reel.

schematic

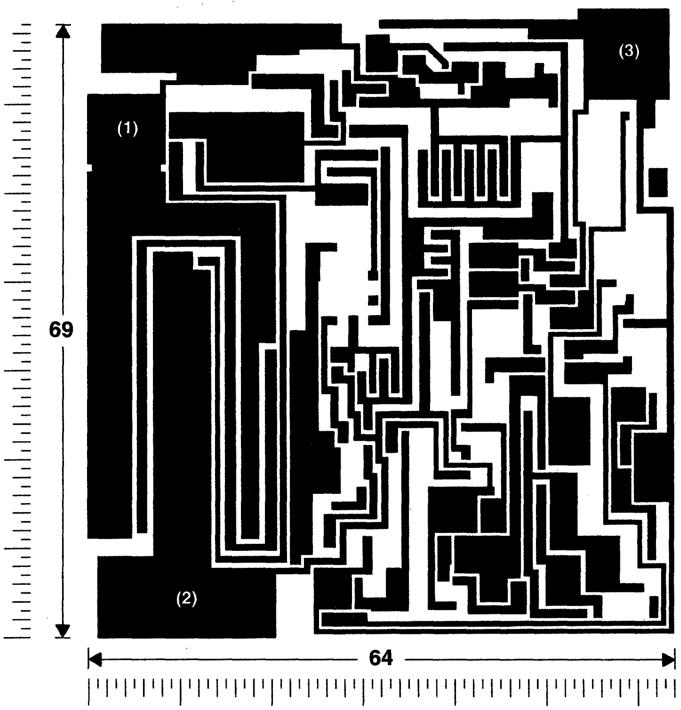


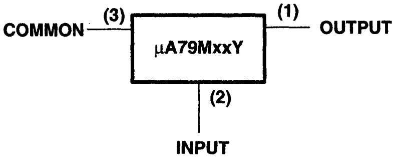
Resistor values shown are nominal and in Ω.

μA79MxxY chip information

This chip, when properly assembled, displays characteristics similar to the μA79MxxC. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL
BONDING PADS: 7 X 7 MILS MINIMUM
$T_J$max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating temperature range (unless otherwise noted)†

		μA79MxxC	UNIT
Input voltage	μA79M20, μA79M24	−40	V
	All others	−35	
Continuous total power dissipation (see Note 1)		See Dissipation Rating Tables 1 and 2	
Operating free-air, T_A, case, T_C, or virtual junction, T_J, temperature range		0 to 150	°C
Storage temperature range, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1–FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
KC	2000 mW	16 mW/°C	1280 mW	400 mW
KTP†				

† The KTP package is product preview only and derating information is not yet available.

DISSIPATION RATING TABLE 2–CASE TEMPERATURE

PACKAGE	$T_C \le 120°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 120°C$	$T_C = 125°C$ POWER RATING
KC	7.5 W	250 mW/°C	6.25 W
KTP†			

† The KTP package is product preview only and derating information is not yet available.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA79M05C	−7	−25	V
	μA79M06C	−8	−25	
	μA79M08C	−10.5	−25	
	μA79M12C	−14.5	30	
	μA79M15C	−17.5	−30	
	μA79M20C	−23	−35	
	μA79M24C	−27	−38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = –10 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA79M05C			UNIT
			MIN	TYP	MAX	
Output voltage‡			–4.8	–5	–5.2	V
	V_I = –7 V to –25 V, T_J = 0°C to 125°C	I_O = 5 mA to 350 mA,	–4.75		–5.25	
Input voltage regulation	V_I = –7 V to –25 V			7	50	mV
	V_I = –8 V to –18 V			3	30	
Ripple rejection	V_I = –8 V to –18 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	50			dB
		I_O = 300 mA	54	60		
Output voltage regulation	I_O = 5 mA to 500 mA			75	100	mV
	I_O = 5 mA to 350 mA			50		
Temperature coefficient of output voltage	I_O = 5 mA,	T_J = 0°C to 125°C		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			125		µV
Dropout voltage				1.1		V
Bias current				1	2	mA
Bias current change	V_I = –8 V to –18 V,	T_J = 0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA,	T_J = 0°C to 125°C			0.4	
Short-circuit output current	V_I = –30 V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = –11 V, I_O = 350 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA79M06C			UNIT
			MIN	TYP	MAX	
Output voltage‡			–5.75	–6	–6.25	V
	V_I = –8 V to –25 V, T_J = 0°C to 125°C	I_O = 5 mA to 350 mA,	–5.7		–6.3	
Input voltage regulation	V_I = –8 V to –25 V			7	60	mV
	V_I = –9 V to –19 V			3	40	
Ripple rejection	V_I = –9 V to –19 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	50			dB
		I_O = 300 mA	54	60		
Output voltage regulation	I_O = 5 mA to 500 mA			80	120	mV
	I_O = 5 mA to 350 mA			55		
Temperature coefficient of output voltage	I_O = 5 mA,	T_J = 0°C to 125°C		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			150		µV
Dropout voltage				1.1		V
Bias current				1	2	mA
Bias current change	V_I = –9 V to –25 V,	T_J = 0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA,	T_J = 0°C to 125°C			0.4	
Short-circuit output current	V_I = –30 V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA79M08C MIN	µA79M08C TYP	µA79M08C MAX	UNIT
Output voltage‡			−7.7	−8	−8.3	V
	$V_I = -10.5$ V to −25 V, $T_J = 0°C$ to 125°C	$I_O = 5$ mA to 350 mA	−7.6		−8.4	
Input voltage regulation	$V_I = -10.5$ V to −25 V			8	80	mV
	$V_I = -11$ V to −21 V			4	50	
Ripple rejection	$V_I = -11.5$ V to −21.5 V, f = 120 Hz	$I_O = 100$ mA, $T_J = 0°C$ to 125°C	50			dB
		$I_O = 300$ mA	54	59		
Output voltage regulation	$I_O = 5$ mA to 500 mA			90	160	mV
	$I_O = 5$ mA to 350 mA			60		
Temperature coefficient of output voltage	$I_O = 5$ mA,	$T_J = 0°C$ to 125°C		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			200		µV
Dropout voltage	$I_O = 5$ mA			1.1		V
Bias current				1	2	mA
Bias current change	$V_I = -10.5$ V to −25 V,	$T_J = 0°C$ to 125°C			0.4	mA
	$I_O = 5$ mA to 350 mA,	$T_J = 0°C$ to 125°C			0.4	
Short-circuit output current	$V_I = -30$ V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA79M12C MIN	µA79M12C TYP	µA79M12C MAX	UNIT
Output voltage‡			−11.5	−12	−12.5	V
	$V_I = -14.5$ V to −30 V, $T_J = 0°C$ to 125°C	$I_O = 5$ mA to 350 mA,	−11.4		−12.6	
Input voltage regulation	$V_I = -14.5$ V to −30 V			9	80	mV
	$V_I = -15$ V to −25 V			5	50	
Ripple rejection	$V_I = -15$V to −25 V, f = 120 Hz	$I_O = 100$ mA, $T_J = 0°C$ to 125°C	50			dB
		$I_O = 300$ mA	54	60		
Output voltage regulation	$I_O = 5$ mA to 500 mA			65	240	mV
	$I_O = 5$ mA to 350 mA			45		
Temperature coefficient of output voltage	$I_O = 5$ mA,	$T_J = 0°C$ to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			300		µV
Dropout voltage				1.1		V
Bias current				1.5	3	mA
Bias current change	$V_I = -14.5$ V to −30 V,	$T_J = 0°C$ to 125°C			0.4	mA
	$I_O = 5$ mA to 350 mA,	$T_J = 0°C$ to 125°C			0.4	
Short-circuit output current	$V_I = -30$ V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA79M15C			UNIT
			MIN	TYP	MAX	
Output voltage‡			−14.4	−15	−15.6	V
	V_I = −17.5 V to −30 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		−14.25		−15.75	
Input voltage regulation	V_I = −17.5 V to −30 V			9	80	mV
	V_I = −18 V to −28 V			7	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	50			dB
		I_O = 300 mA	54	59		
Output voltage regulation	I_O = 5 mA to 500 mA			65	240	mV
	I_O = 5 mA to 350 mA			45		
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			375		μV
Dropout voltage	I_O = 5 mA			1.1		V
Bias current				1.5	3	mA
Bias current change	V_I = −17.5 V to −30 V, T_J = 0°C to 125°C				0.4	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.4	
Short-circuit output current	V_I = −30 V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -29$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA79M20C			UNIT
			MIN	TYP	MAX	
Output voltage‡			−19.2	−20	−20.8	V
	V_I = −23 V to −35 V, I_O = 5 mA to 350 mA, T_J = 0°C to 125°C		−19		−21	
Input voltage regulation	V_I = −23 V to −35 V			12	80	mV
	V_I = −24 V to −34 V			10	70	
Ripple rejection	V_I = −24 V to −34 V, f = 120 Hz	I_O = 100 mA, T_J = 0°C to 125°C	50			dB
		I_O = 300 mA	54	58		
Output voltage regulation	I_O = 5 mA to 500 mA			75	300	mV
	I_O = 5 mA to 350 mA			50		
Temperature coefficient of output voltage	I_O = 5 mA, T_J = 0°C to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage				1.1		V
Bias current				1.5	3.5	mA
Bias current change	V_I = −23 V to −35 V, T_J = 0°C to 125°C				0.4	mA
	I_O = 5 mA to 350 mA, T_J = 0°C to 125°C				0.4	
Short-circuit output current	V_I = −30 V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		µA79M24C MIN	µA79M24C TYP	µA79M24C MAX	UNIT
Output voltage‡			−23	−24	−25	V
	$V_I = -27$ V to −38 V, $I_O = 5$ mA to 350 mA, $T_J = 0°C$ to 125°C		−22.8		−25.2	
Input voltage regulation	$V_I = -27$ V to −38 V			12	80	mV
	$V_I = -28$ V to −38 V			12	70	
Ripple rejection	$V_I = -28$ V to −38 V, f = 120 Hz	$I_O = 100$ mA, $T_J = 0°C$ to 125°C	50			dB
		$I_O = 300$ mA	54	58		
Output voltage regulation	$I_O = 5$ mA to 500 mA			75	300	mV
	$I_O = 5$ mA to 350 mA			50		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0°C$ to 125°C			−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			600		µV
Dropout voltage				1.1		V
Bias current				1.5	3.5	mA
Bias current change	$V_I = -27$ V to −38 V, $T_J = 0°C$ to 125°C				0.4	mA
	$I_O = 5$ mA to 350 mA, $T_J = 0°C$ to 125°C				0.4	
Short-circuit output current	$V_I = -30$ V			140		mA
Peak output current				0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M05Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			–5		V
Input voltage regulation	$V_I = -7$ V to –25 V		7		mV
	$V_I = -8$ V to –18 V		3		
Ripple rejection	$V_I = -8$ V to –18 V, $I_O = 300$ mA, f = 120 Hz		60		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		125		μV
Dropout voltage			1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M06Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			–6		V
Input voltage regulation	$V_I = -8$ V to –25 V		7		mV
	$V_I = -9$ V to –19 V		3		
Ripple rejection	$V_I = -9$ V to –19 V, $I_O = 300$ mA, f = 120 Hz		60		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		80		mV
	$I_O = 5$ mA to 350 mA		55		
Temperature coefficient of output voltage	$I_O = 5$ mA		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		150		μV
Dropout voltage			1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M08Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			−8		V
Input voltage regulation	$V_I = -10.5$ V to −25 V		8		mV
	$V_I = -11$ V to −21 V		4		
Ripple rejection	$V_I = -11.5$ V to −21.5 V, $I_O = 300$ mA, f = 120 Hz		59		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		90		mV
	$I_O = 5$ mA to 350 mA		60		
Temperature coefficient of output voltage	$I_O = 5$ mA		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		200		μV
Dropout voltage	$I_O = 5$ mA		1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M12Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			−12		V
Input voltage regulation	$V_I = -14.5$ V to −30 V		9		mV
	$V_I = -15$ V to −25 V		5		
Ripple rejection	$V_I = -15$V to −25 V, $I_O = 300$ mA, f = 120 Hz		60		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		65		mV
	$I_O = 5$ mA to 350 mA		45		
Temperature coefficient of output voltage	$I_O = 5$ mA		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		300		μV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	µA79M15Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			−15		V
Input voltage regulation	$V_I = -17.5$ V to −30 V		9		mV
	$V_I = -18$ V to −28 V		7		
Ripple rejection	$V_I = -18.5$ V to −28.5 V, $I_O = 300$ mA, f = 120 Hz		59		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		65		mV
	$I_O = 5$ mA to 350 mA		45		
Temperature coefficient of output voltage	$I_O = 5$ mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		375		µV
Dropout voltage	$I_O = 5$ mA		1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -29$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	µA79M20Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			−20		V
Input voltage regulation	$V_I = -23$ V to −35 V		12		mV
	$V_I = -24$ V to −34 V		10		
Ripple rejection	$V_I = -24$ V to −34 V, $I_O = 300$ mA, f = 120 Hz		58		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M24Y			UNIT
		MIN	TYP	MAX	
Output voltage‡			−24		V
Input voltage regulation	$V_I = -27$ V to −38 V		12		mV
	$V_I = -28$ V to −38 V		12		
Ripple rejection	$V_I = -28$ V to −38 V, $I_O = 300$ mA, f = 120 Hz		58		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0°C$ to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		600		μV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

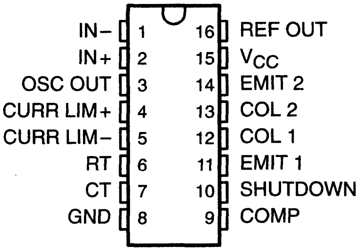
Contents

SG2524, SG3524, SG3524Y
REGULATING PULSE-WIDTH MODULATORS

SLVS077A – APRIL 1977 – REVISED AUGUST 1995

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Silicon General SG2524 and SG3524**

D OR N PACKAGE
(TOP VIEW)



description

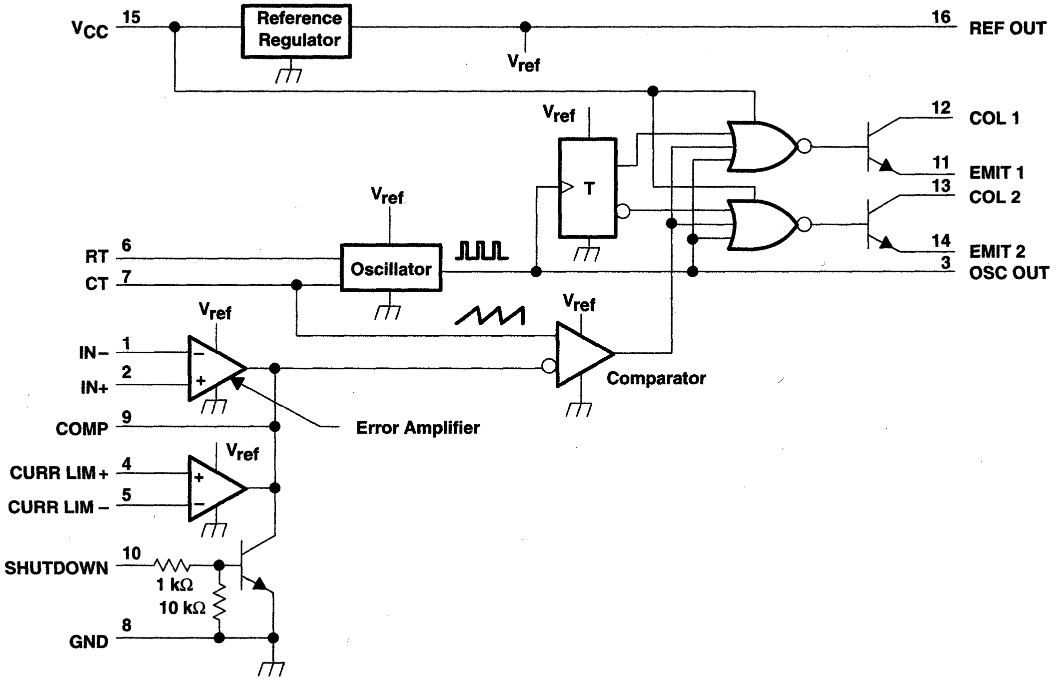
The SG2524 and SG3524 incorporate on single monolithic chips all the functions required in the construction of a regulating power supply, inverter, or switching regulator. They can also be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

The SG2524 is characterized for operation from −25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	INPUT REGULATION MAX (mV)	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	
0°C to 70°C	30	SG3524D	SG3524N	SG3524Y
−25°C to 85°C	20	SG2524D	SG2524N	—

functional block diagram

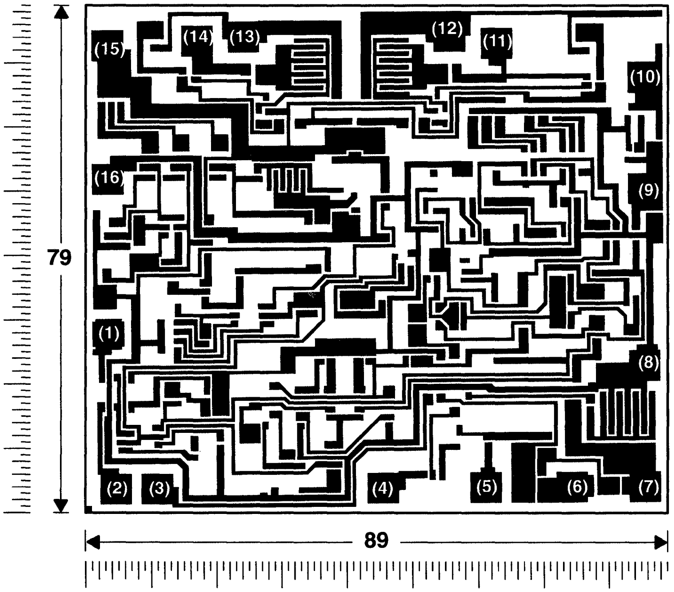


NOTE A. Resistor values shown are nominal.

SG3524Y chip information

This chip, when properly assembled, displays characteristics similar to the SG3524. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



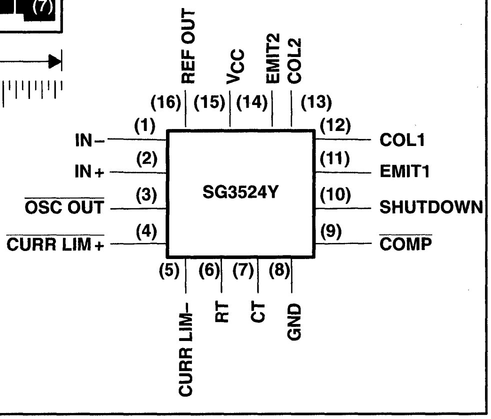
CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Notes 1 and 2) .... 40 V
Collector output current, I_{CC} .... 100 mA
Reference output current, $I_{O(ref)}$ .... 50 mA
Current through CT terminal .... −5 mA
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: SG2524 .... −25°C to 85°C
SG3524 .... 0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the V_{CC} and reference output pin both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1000 mW	9.2 mW/ °C	41°C	733 mW	595 mW
D	950 mW	7.6 mW/ °C	25°C	608 mW	494 mW

recommended operating conditions

	SG2524		SG3524		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	8	40	8	40	V
Reference output current	0	50	0	50	mA
Current through CT terminal	−0.03	−2	−0.03	−2	mA
Timing resistor, R_T	1.8	100	1.8	100	kΩ
Timing capacitor, C_T	0.001	0.1	0.001	0.1	µF
Operating free-air temperature	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG2524			SG3524			SG3524Y			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.6	5	5.4		5		V
Input regulation	V_{CC} = 8 V to 40 V		10	20		10	30		10		mV
Ripple rejection	f = 120 Hz		66			66			66		dB
Output regulation	I_O = 0 mA to 20 mA		20	50		20	50		20		mV
Output voltage change with temperature	T_A = MIN to MAX		0.3%	1%		0.3%	1%				
Short-circuit output current§	V_{ref} = 0		100			100			100		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values, except for temperature coefficients, are at T_A = 25°C

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

oscillator section

PARAMETER		TEST CONDITIONS†	SG2524, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{osc}	Oscillator frequency	C_T = 0.001 µF, R_T = 2 kΩ		450			450		kHz
	Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant		5%			5%		
Δf_{osc}	Frequency change with voltage	V_{CC} = 8 V to 40 V, T_A = 25°C			1%			1%	
	Frequency change with temperature	T_A = MIN to MAX			2%				
	Output amplitude at OSC OUT	T_A = 25°C		3.5			3.5		V
t_w	Output pulse duration (width) at OSC OUT	C_T = 0.01 µF, T_A = 25°C		0.5			0.5		µs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values, except for temperature coefficients, are at T_A = 25°C

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

error amplifier section

PARAMETER		TEST CONDITIONS†	SG2524			SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10		2		mV
I_{IB}	Input bias current	V_{IC} = 2.5 V		2	10		2	10		2		µA
	Open-loop voltage amplification		72	80		60	80			80		dB
V_{ICR}	Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4						V
CMMR	Common-mode rejection ratio			70			70			70		dB
B_1	Unity-gain bandwidth			3			3			3		MHz
	Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	0.5		3.8	V

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C

output section

PARAMETER		TEST CONDITIONS†	SG2534, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{(BR)CE}$	Collector-emitter breakdown voltage		40						V
	Collector off-state current	V_{CE} = 40 V		0.01	50		0.01		µA
V_{sat}	Collector-emitter saturation voltage	I_C = 50 mA		1	2		1		V
V_O	Emitter output voltage	V_C = 20 V, I_E = −250 µA	17	18			18		V
t_r	Turn-off voltage rise time	R_C = 2 kΩ		0.2			0.2		µs
t_f	Turn-on voltage fall time	R_C = 2 kΩ		0.1			0.1		µs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C

comparator section

PARAMETER		TEST CONDITIONS†	SG2534, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
	Maximum duty cycle, each output		45%						
V_{IT}	Input threshold voltage at COMP	Zero duty cycle		1			1		V
		Maximum duty cycle		3.5			3.5		
I_{IB}	Input bias current			−1			−1		µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 20$ V, f = 20 kHz (unless otherwise noted)

current limiting section

PARAMETER		TEST CONDITIONS	SG2524			SG3524			SG3524Y			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage range (either input)		−1 to 1			−1 to 1						V
$V_{(SENSE)}$	Sense voltage at $T_A = 25°C$	$V_{(IN+)} - V_{(IN-)} \ge 50$ mV, $V_{(COMP)} = 2$ V	175	200	225	175	200	225	175	200	225	mV
	Temperature coefficient of sense voltage			0.2			0.2			0.2		mV/°C

† All typical values, except for temperature coefficients, are at $T_A = 25°C$.

total device

PARAMETER		TEST CONDITIONS	SG2524, SG3524			SG3524Y			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{st}	Standby current	$V_{CC} = 40$ V, IN−, CURR LIM+, C_T, GND, COMP, EMIT 1, EMIT 2 grounded IN+ at 2 V, All other inputs and outputs open		8	10		8		mA

† All typical values, except for temperature coefficients, are at $T_A = 25°C$.

PARAMETER MEASUREMENT INFORMATION

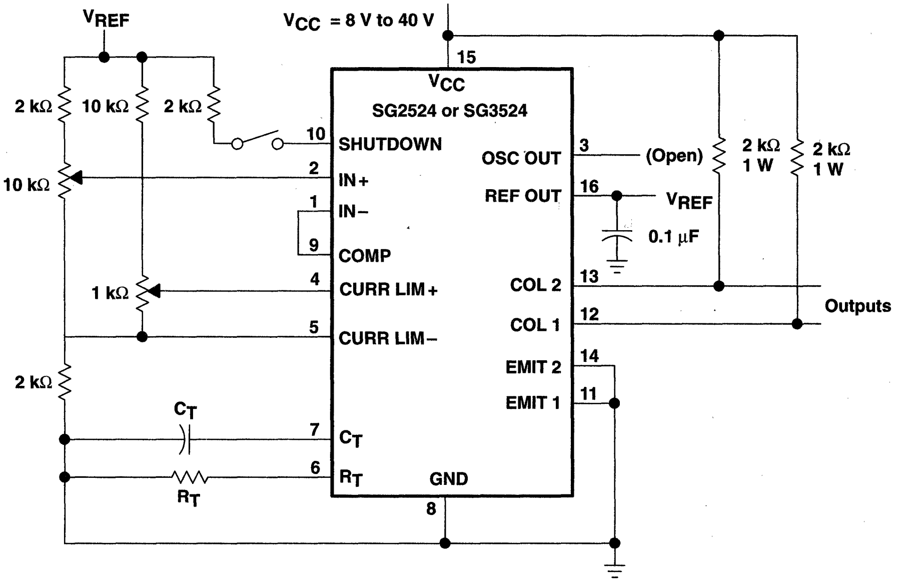
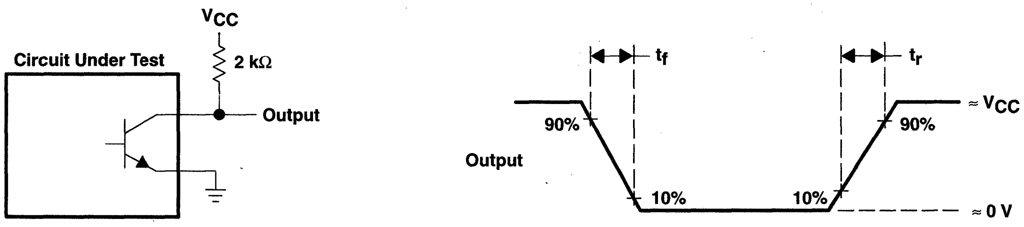


Figure 1. General Test Circuit



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 2. Switching Times

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION OF ERROR AMPLIFIER vs FREQUENCY

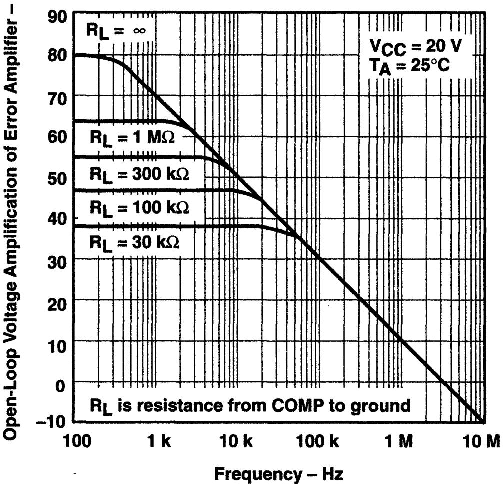


Figure 3

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

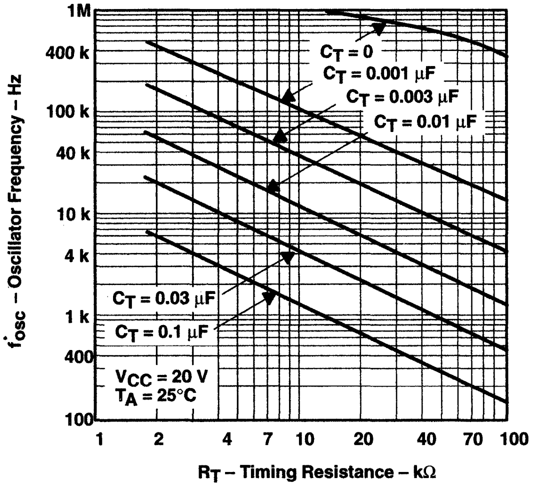


Figure 4

OUTPUT DEAD TIME vs TIMING CAPACITANCE

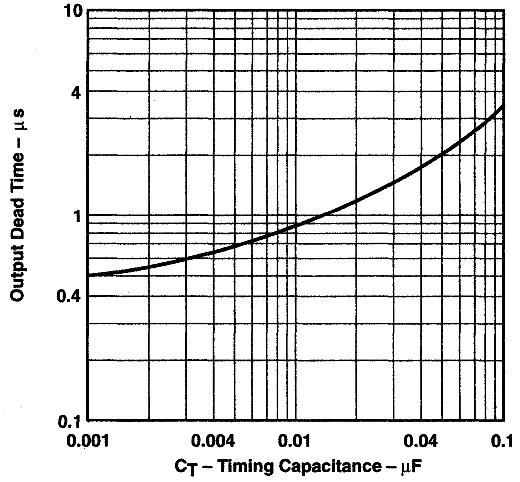


Figure 5

PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor, R_T, and one timing capacitor C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an on-board 5-V regulator that serves as a reference as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference may be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, to compensate the error amplifier, or to provide additional control to the regulator.

APPLICATION INFORMATION†

oscillator

The oscillator controls the frequency of the SG2524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.30}{R_T\ C_T}$$

where R_T is in kΩ
C_T is in µF
f is in kHz

Practical values of C_T fall between 0.001 and 0.1 µF. Practical values of R_T fall between 1.8 and 100 kΩ. This results in a frequency range typically from 130 Hz to 722 kHz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse duration may still be maintained by applying a shunt capacitance from OSC OUT to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, R_T C_T must be selected for a clock period slightly greater than that of the external clock.

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

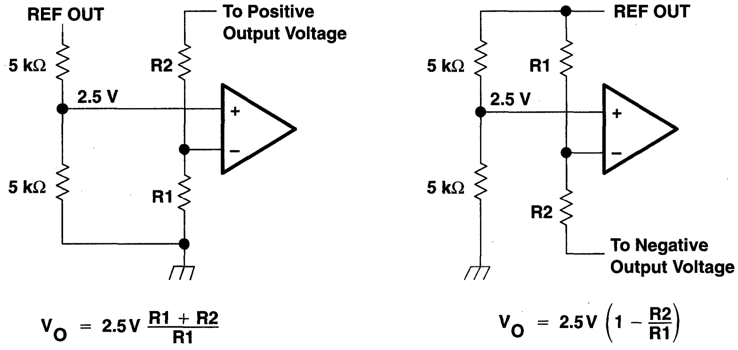
APPLICATION INFORMATION†

synchronous operation (continued)

If two or more SG2524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period is the master from which all the other SG2524s operate. In this application, the C_TR_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and subsequently resets the slave regulators.

voltage reference

The 5-V internal reference may be employed by use of an external resistor divider network to establish a reference common-mode voltage range (1.8 V to 3.4 V) within the error amplifiers as shown in Figure 6, or an external reference may be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference may be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.



$$V_O = 2.5\,V\,\frac{R1 + R2}{R1}$$

$$V_O = 2.5\,V\left(1 - \frac{R2}{R1}\right)$$

Figure 6. Error Amplifier Bias Circuits

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node (R_L = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

compensation

COMP, as discussed above, is made available for compensation. Since most output filters introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 µF. Other frequencies can be canceled by use of the formula f ≈ 1/RC.

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

shut-down circuitry

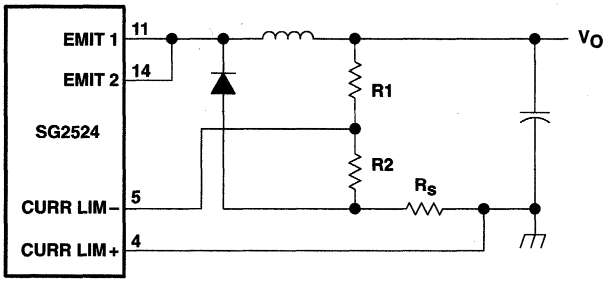
COMP can also be employed to introduce external control of the SG2524. Any circuit that can sink 200 µA can pull the compensation terminal to ground and thus disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM– may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM– may also be grounded to convert CURR LIM+ into an additional shut-down terminal.

current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV ±25 mV and must be applied in the ground line since the voltage range of the inputs is limited to 1 V to –1 V. Caution should be taken to ensure the –1 V limit is not exceeded by either input, otherwise damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.



$$I_{O(max)} = \frac{1}{R_S}\left(200\text{ mV} + \frac{V_O\,R2}{R1 + R2}\right)$$

$$I_{OS} = \frac{200\text{ mV}}{R_S}$$

Figure 7. Foldback Current Limiting for Shorted Output Conditions

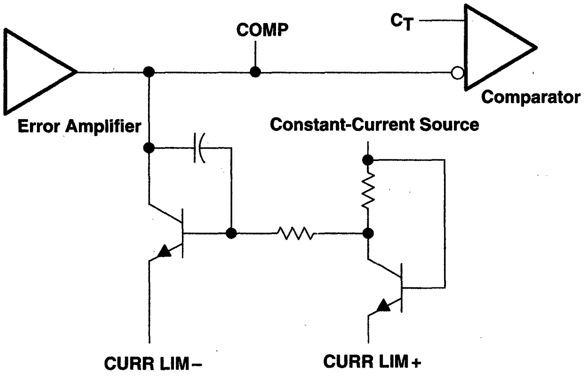


Figure 8. Current-Limit Schematic

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

output circuitry

The SG2524 contains two identical npn transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11 respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

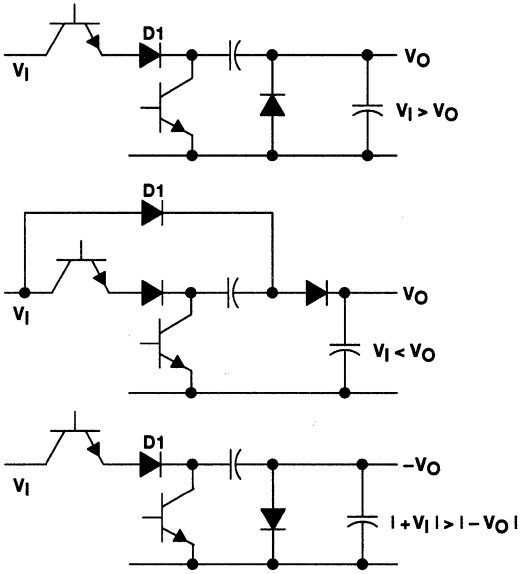

Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

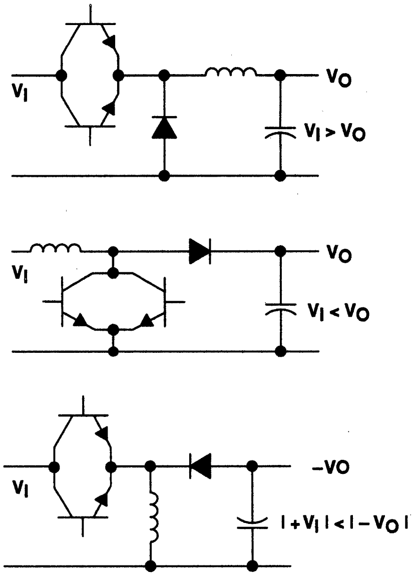

Figure 10. Single-Ended Inductor Circuit

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

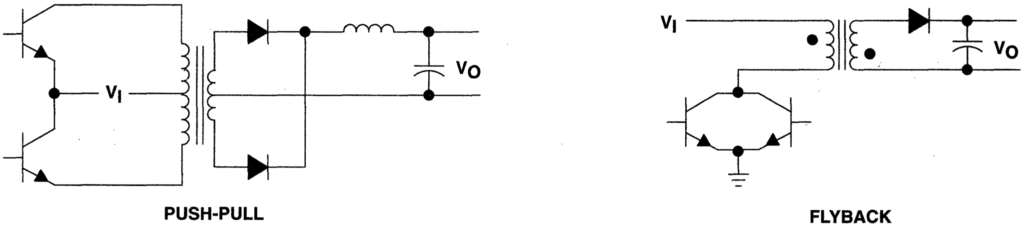

Figure 11. Transformer-Coupled Outputs

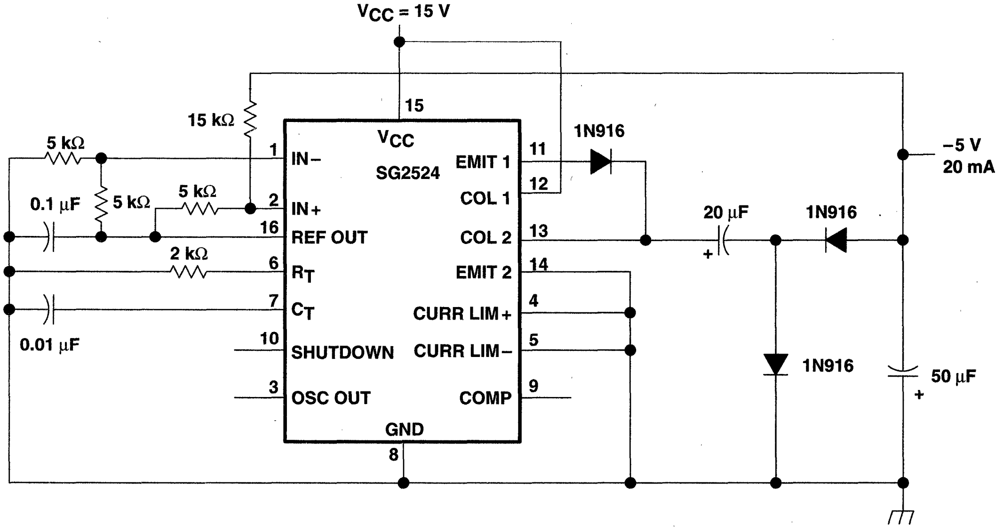

Figure 12. Capacitor-Diode Output Circuit

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

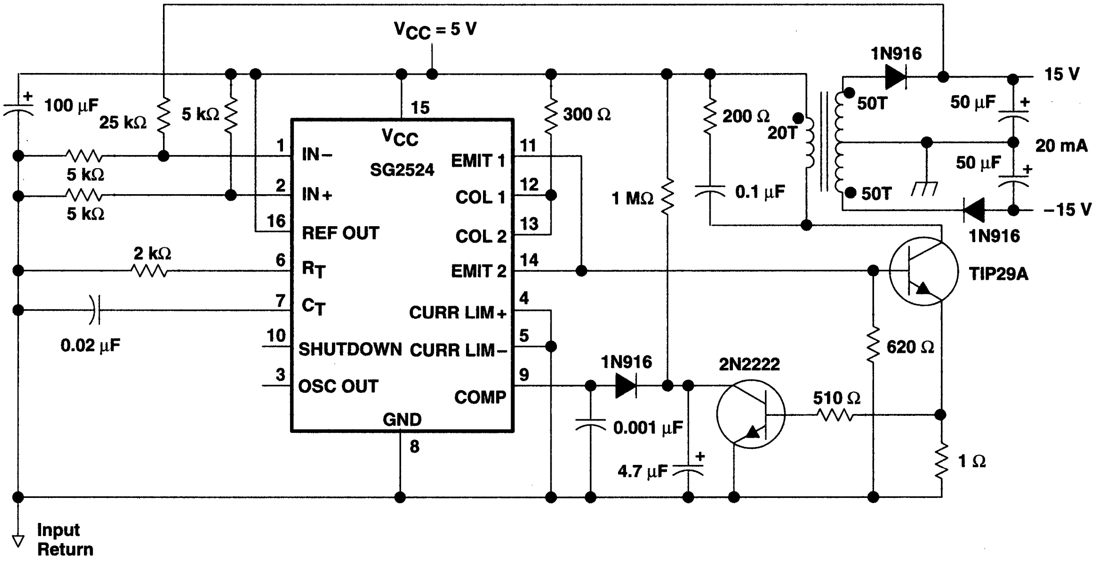

Figure 13. Flyback Converter Circuit

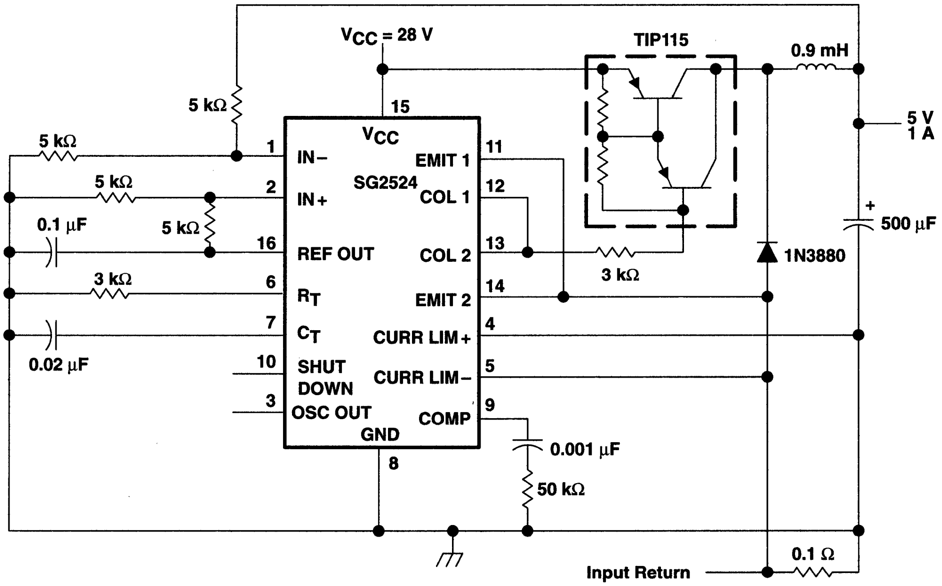

Figure 14. Single-Ended LC Circuit

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

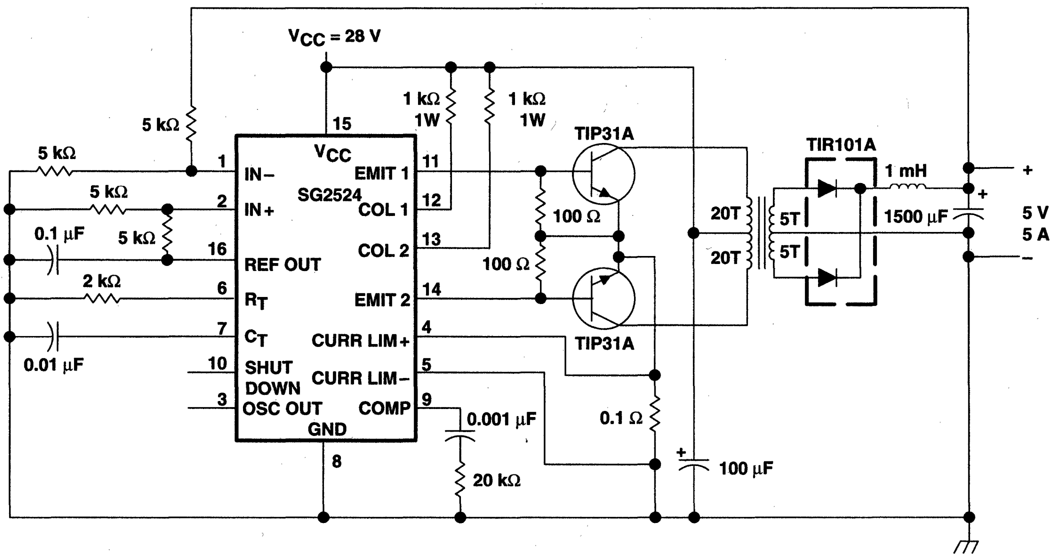

Figure 15. Push-Pull Transformer-Coupled Circuit

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

TL494C, TL494I, TL494M, TL494Y
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS074A – JANUARY 1983 – REVISED AUGUST 1995

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

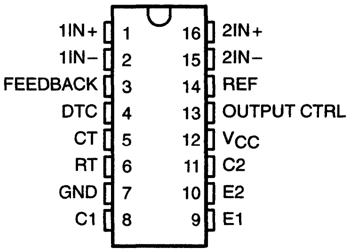
description

The TL494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, this device offers the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

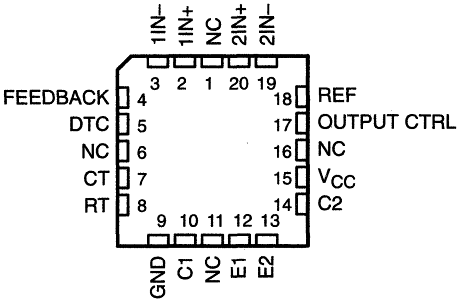
The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator may be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it may drive the common circuits in synchronous multiple-rail power supplies.

TL494C, TL494I . . . D, N, OR PW PACKAGE
TL494M . . . J PACKAGE
(TOP VIEW)



TL494M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES					CHIP FORM (Y)
	SURFACE MOUNT (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	SHRINK SMALL OUTLINE (PW)‡	
0°C to 70°C	TL494CD	—	—	TL494CN	TL494CPW	TL494Y
−40°C to 85°C	TL494ID	—	—	TL494IN	—	—
−55°C to 125°C	—	TL494MFK	TL494MJ	—	—	—

† The D package is available taped and reeled. Add R suffix to device type (e.g., TL494CDR).
‡ The PW package is only available left-end taped and reeled.

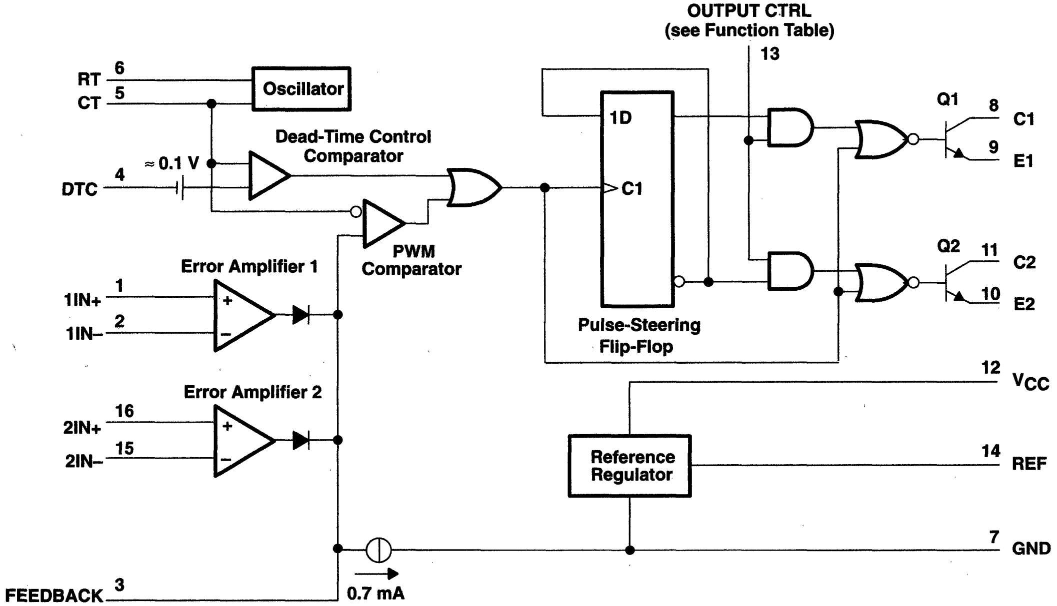
TEXAS INSTRUMENTS

description (continued)

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from −40°C to 85°C. The TL494M is characterized for operation from −55°C to 125°C.

functional block diagram

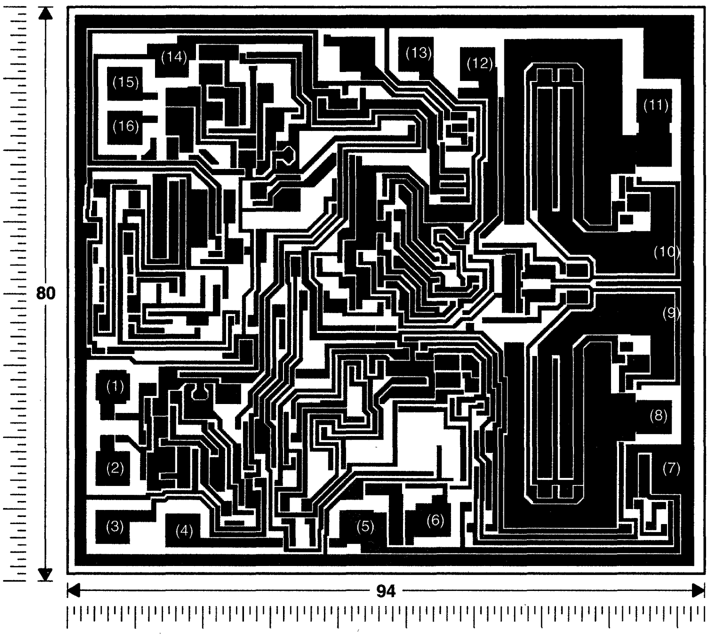


NOTE A. The terminal numbers indicated apply only to the D, J, N, and PW packages.

TL494Y chip information

This chip, when properly assembled, display characteristics similar to the TL494C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



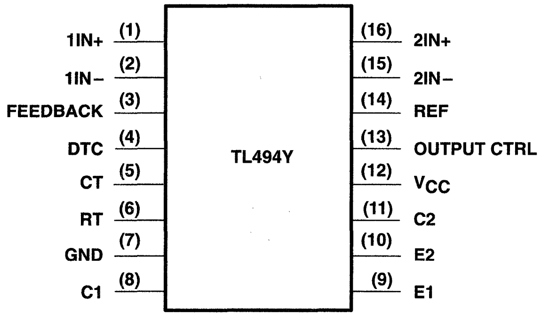
CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	TL494C	TL494I	TL494M	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	41	V
Amplifier input voltage, V_I	$V_{CC} + 0.3$	$V_{CC} + 0.3$	$V_{CC} + 0.3$	V
Collector output voltage, V_O	41	41	41	V
Collector output current, I_O	250	250	250	mA
Continuous total power dissipation	See Dissipation Rating Table			
Operating free-air temperature range, T_A	0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds, T_C: FK package	—	—	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260	260	—	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package	—	—	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	25°C	558 mW	444 mW	—
FK	1375 mW	11.0 mW/°C	25°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	25°C	880 mW	715 mW	275 mW
N	1000 mW	9.2 mW/°C	41°C	733 mW	595 mW	—
PW	700 mW	5.6 mW/°C	25°C	448 mW	—	—

recommended operating conditions

	TL494C		TL494I		TL494M		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	7	40	V
Amplifier input voltage, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40		40	V
Collector output current (each transistor)		200		200		200	mA
Current into feedback terminal		0.3		0.3		0.3	mA
Oscillator frequency, f_{osc}	1	300	1	300	1	300	kHz
Timing capacitor, C_T	0.47	10000	0.47	10000	0.47	10000	nF
Timing resistor, R_T	1.8	500	1.8	500	1.8	500	kΩ
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			TL494M			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25		2	25	mV
Output regulation	I_O = 1 mA to 10 mA		1	15		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2	10		2	30*	mV/V
Short-circuit output current§	REF = 0 V		25			–25		mA

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			TL494M			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Frequency			10			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, CT, RT, and T_A constant		100			100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1			1		Hz/kHz
Frequency change with temperature#	ΔT_A = MIN to MAX			10			10*	Hz/kHz

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:
# Temperature coefficient of timing capacitor and timing resistor not taken into account.

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

error amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL494C, TL494I TL494M			UNIT
		MIN	TYP‡	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5 V		2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5 V		25	250	nA
Input bias current	V_O (FEEDBACK) = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	–0.3 to V_{CC}–2			V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V, V (FEEDBACK) = 0.7 V	0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID} = 15 mV to 5 V, V (FEEDBACK) = 3.5 V	–2			mA

‡ All typical values except for parameter changes with temperature are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz, T_A = 25°C (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	TL494Y MIN	TL494Y TYP†	TL494Y MAX	UNIT
Output voltage (REF)	I_O = 1 mA		5		V
Input regulation	V_{CC} = 7 V to 40 V		2		mV
Output regulation	I_O = 1 mA to 10 mA		1		mV
Short-circuit output current‡	REF = 0 V		25		mA

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS	TL494Y MIN	TL494Y TYP†	TL494Y MAX	UNIT
Frequency			10		kHz
Standard deviation of frequency§	All values of V_{CC}, CT, RT, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz

error amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL494Y MIN	TL494Y TYP†	TL494Y MAX	UNIT
Input offset voltage	V_O (FEEDBACK) = 2.5 V		2		mV
Input offset current	V_O (FEEDBACK) = 2.5 V		25		nA
Input bias current	V_O (FEEDBACK) = 2.5 V		0.2		μA
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C		80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V, V (FEEDBACK) = 0.7 V		0.7		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS		TL494C, TL494I TL494M, TL494Y			UNIT
				MIN	TYP†	MAX	
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		$V_{CC} = V_C$ = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	$V_{O(C1\ or\ C2)}$ = 15 V,	I_E = −200 mA		1.5	2.5	
Output control input current		$V_I = V_{ref}$				3.5	mA

† All typical values except for temperature coefficient are at T_A = 25°C.

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL494C, TL494I TL494Y			TL494M			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input bias current (DEAD-TIME CTRL)	V_I = 0 to 5.25 V		−2	−10		−2	−10	μA
Maximum duty cycle, each output	V_I (DEAD-TIME CTRL) = 0, C_T = 0.1 μF, R_T = 12 kΩ		45%			45%	50%*	
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle		3	3.3		3	3.3	V
	Maximum duty cycle	0			0*			

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† All typical values except for temperature coefficient are at T_A = 25°C.

PWM comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL494C, TL494I TL494M, TL494Y			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (FEEDBACK)	Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)	V (FEEDBACK) = 0.7 V	0.3	0.7		mA

† All typical values except for temperature coefficient are at T_A = 25°C.

total device

PARAMETER	TEST CONDITIONS		TL494C, TL494I TL494Y			TL494M			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10		6	21	mA
		V_{CC} = 40 V		9	15		9	26	
Average supply current	V_I (DEAD-TIME CTRL) = 2 V,	See Figure 1		7.5			7.5		mA

† All typical values except for temperature coefficient are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted) (continued)

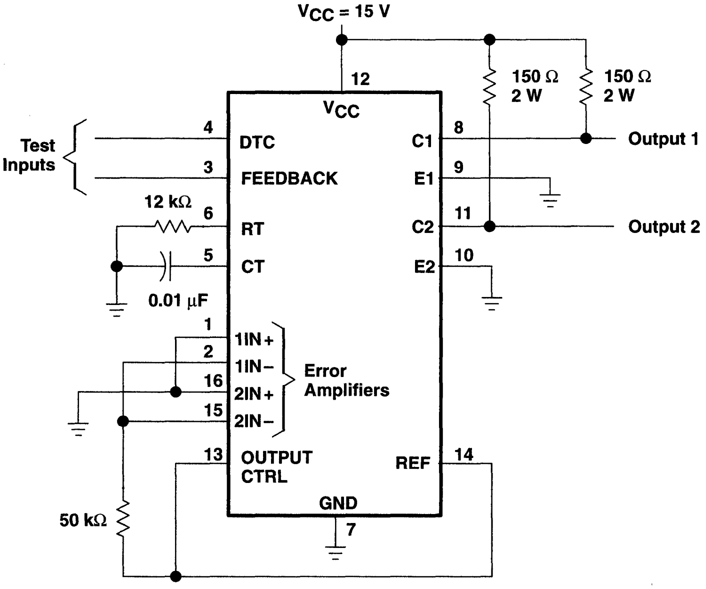
switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL494C, TL494I TL494Y			TL494M			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Rise time	Common-emitter configuration, See Figure 3		100	200		100	200*	ns
Fall time			25	100		25	100*	ns
Rise time	Emitter-follower configuration, See Figure 4		100	200		100	200*	ns
Fall time			40	100		40	100*	ns

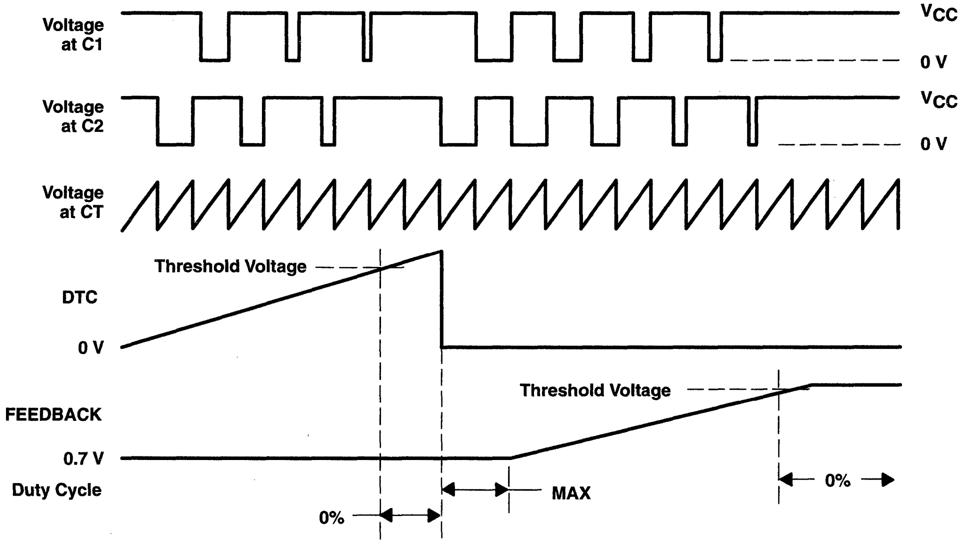
* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

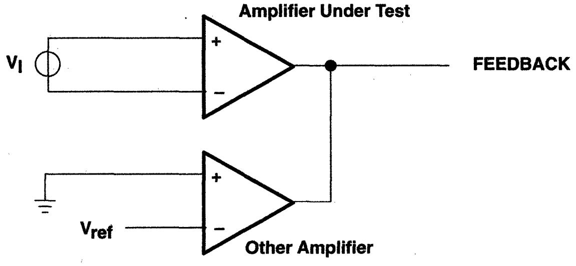
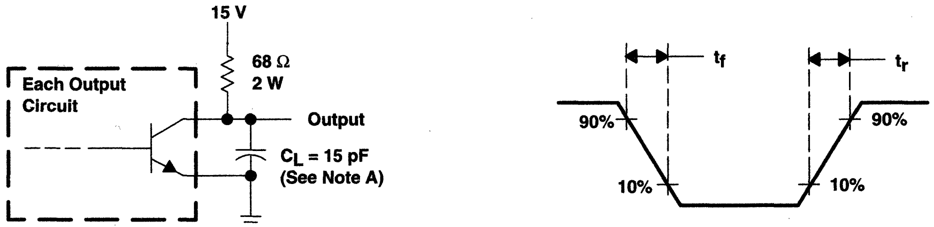


Figure 2. Amplifier Characteristics

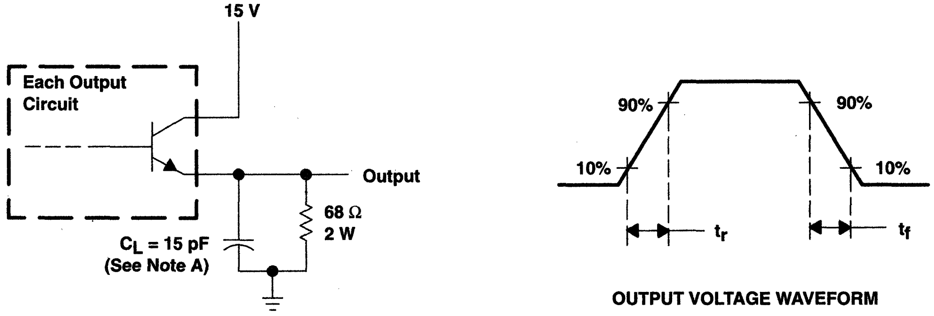


TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

NOTE A. C_L includes probe and jig capacitance.

Figure 3. Common-Emitter Configuration



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

NOTE A. C_L includes probe and jig capacitance.

Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE

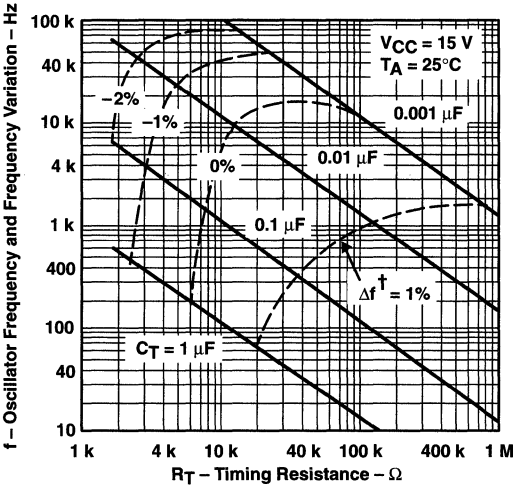


Figure 5

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

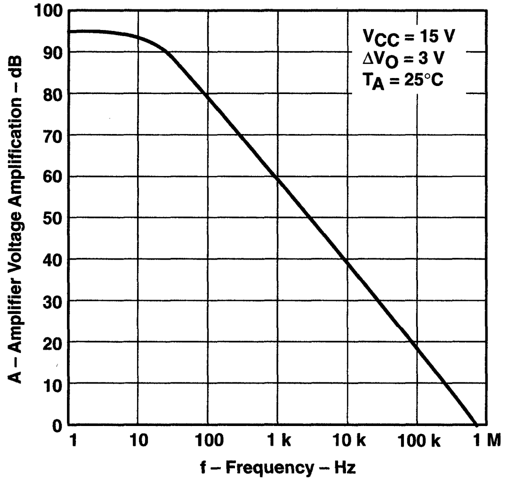


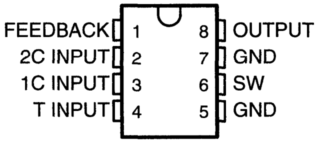
Figure 6

TL496C, TL496Y
9-V POWER-SUPPLY CONTROLLERS

SLVS012B – AUGUST 1978 – REVISED AUGUST 1995

- **Internal Step-Up Switching Regulator**
- **Fixed 9-V Output**
- **Charges Battery Source During Transformer-Coupled-Input Operation**
- **Minimum External Components Required (1 Inductor, 1 Capacitor, 1 Diode)**
- **1- or 2-Cell-Input Operation**

D OR P PACKAGE
(TOP VIEW)



Terminals 5 and 7 are connected together internally.

description

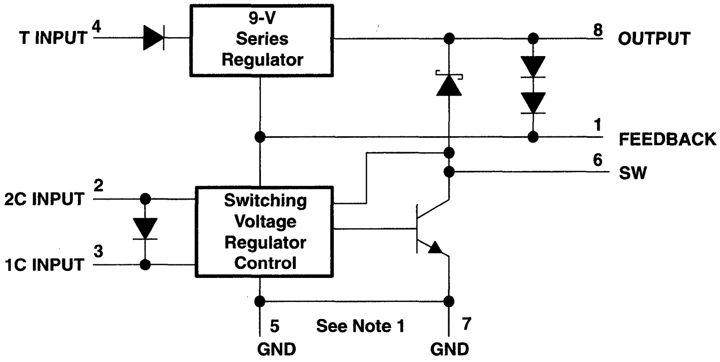
The TL496C power-supply control circuit is designed to provide a 9-V regulated supply from a variety of input sources. Operable from a 1- or 2-cell battery input, the TL496C performs as a switching regulator with the addition of a single inductor and filter capacitor. When ac coupled with a step-down transformer, the TL496C operates as a series regulator to maintain the regulated output voltage and, with the addition of a single catch diode, time shares to recharge the input batteries.

The design of the TL496C allows minimal supply current drain during standby operation (125 μA typical). With most battery sources, this allows a constant bias to be maintained on the power supply. This makes power instantly available to the system, thus eliminating power-up sequencing problems.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SURFACE MOUNT (D)	PLASTIC DIP (P)	
0°C to 70°C	TL496CD	TL496CP	TL496Y

functional block diagram

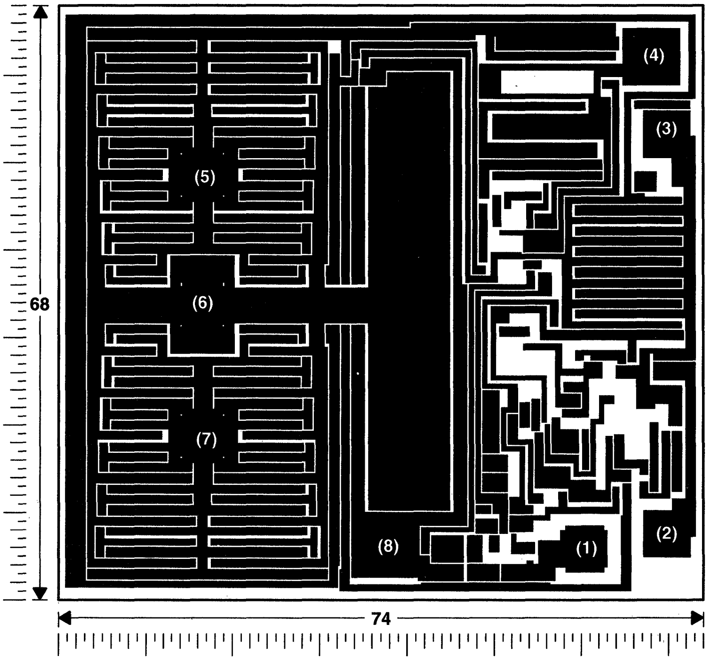


NOTE 1: Terminals 5 and 7, though connected together internally, must both be terminated to ground to ensure proper circuit operation.

TL496Y chip information

This chip, when properly assembled, displays characteristics similar to the TL496C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



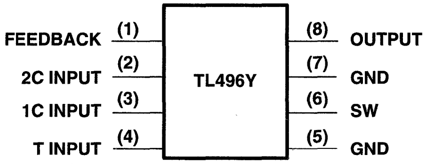
CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max= 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage, V_I: 2C INPUT	3.5 V
1C INPUT	2.5 V
T INPUT	20 V
Output voltage, V_O (SW)	12 V
Diode reverse voltage (OUTPUT)	12 V
Switch current (SW)	1.2 A
Diode current (OUTPUT)	1.2 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, one-cell operation (2C and 1C INPUTS to ground)	1.1	1.5	V
Input voltage, two-cell operation (2C INPUT to ground)	2.3	3	V
Input voltage, one-cell or two-cell operation (T INPUT to ground)	$V_O + 2$	20	V

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

series regulator section (T INPUT)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage	V_I = 5 V,	I_O = −50 mA		1.5	2	V
Regulated output voltage	V_I = 20 V,	I_O = −50 μA	9.5	10.1	11.2	V
		I_O = −80 mA	9	10	11	
	V_I = 20 V, FEEDBACK shorted to OUTPUT	I_O = −50 μA	8.5	9	9.7	
		I_O = −80 mA	6.7	8.6	9.5	
Standby current, T INPUT	V_I = 20 V,	OUTPUT = 12 V			400	μA
Reverse current through T INPUT	V_I = −1.5 V,	1 mA into OUTPUT			−25	μA

output switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CE(sat)}$	Collector-emitter saturation voltage	800 mA into SW, 2C INPUT = 2.25 V		0.35	0.6	V

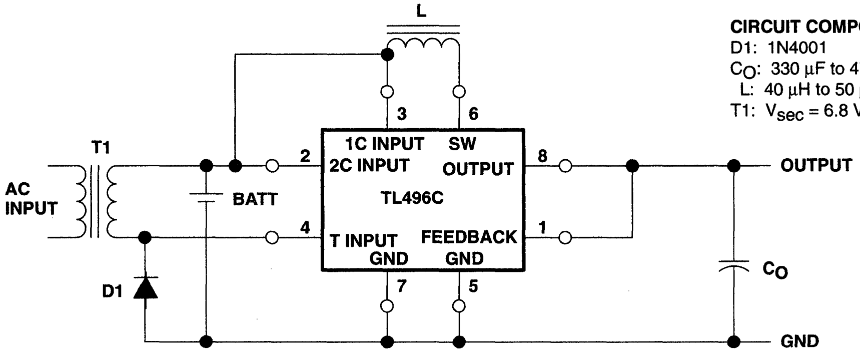
diode (SW to OUTPUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward voltage	I_F = 1.5 A		1.6	2.5	V
I_R	Reverse current through SW	SW at 0 V, 1 mA into OUTPUT			−20	μA

control section

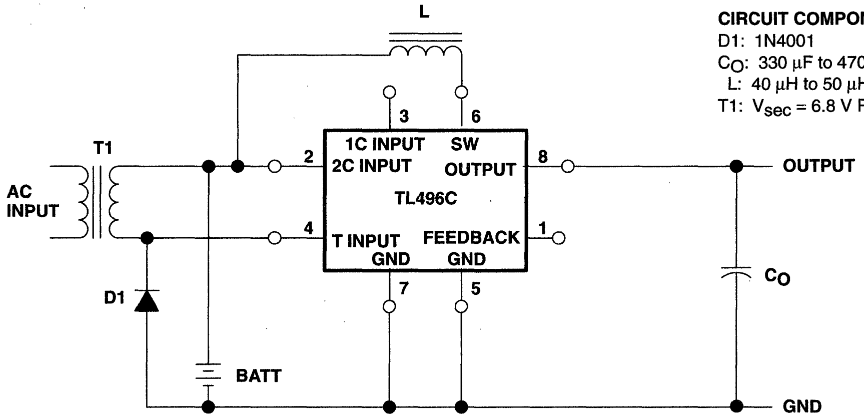
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On-state current (2C INPUT)	FEEDBACK and OUTPUT = 0 V, 2C INPUT = 3 V		60	100	mA
Standby current (FEEDBACK)	FEEDBACK = 8.65 V, 2C INPUT and SW = 3 V			40	μA
Standby current (2C INPUT and SW)	FEEDBACK = 8.65 V, 2C INPUT and SW = 3 V			400	μA
Start-up current (current into SW to initiate cycle)	FEEDBACK, 2C INPUT, SW, and OUTPUT = 2.25 V	16			mA

APPLICATION INFORMATION



CIRCUIT COMPONENT INFORMATION
D1: 1N4001
C_O: 330 µF to 470 µF, 10 V, electrolytic
L: 40 µH to 50 µH, Q ≈ 3, R < 0.15 Ω
T1: V_{sec} = 6.8 V RMS typ, R_{sec} = 11 Ω typ

Figure 1. One-Cell Operation



CIRCUIT COMPONENT INFORMATION
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L: 40 µH to 50 µH, Q ≈ 3, R < 0.15 Ω
T1: V_{sec} = 6.8 V RMS typ, R_{sec} = 11 Ω typ

Figure 2. Two-Cell Operation

electrical characteristics for one- and two-cell input operations

PARAMETER		ONE-CELL OPERATION (see Figure 1)	TWO-CELL OPERATION (see Figure 2)
Input current	No load	125 µA	125 µA
	R_L = 120 Ω	525 mA	405 mA
Output voltage	No ac input	7.2 V	8.6 V
	With ac input	8.6 V	10 V
Output current capability		40 mA	80 mA
Efficiency		66%	66%
Battery life (AA NiCad) no load		60 days	166 days

functional description

The TL496C is designed to operate from either a single-cell or two-cell battery source. To operate the device from a single cell (1.1 V to 1.5 V), the source must be connected to both inputs 1C INPUT and 2C INPUT as shown in Figure 1. For a two-cell operation (2.3 V to 3 V), the input is applied to 2C INPUT only and 1C INPUT is left open (see Figure 2).

battery operation

The TL496C operates as a switching regulator from a battery input. The cycle is initiated when a low-voltage condition is sensed by the internal feedback (the thresholds at terminals 1 and 8 are approximately 7.2 and 8.6 V respectively). An internal latch is set and the output transistor is turned on. This causes the current in the external inductor (L) to increase linearly until it reaches a peak value of approximately 1 A. When the peak current is sensed, the internal latch is reset and the output transistor is turned off. The energy developed in the inductor is then delivered to the output storage capacitor through the blocking diode. The latch remains in the off state until the feedback signal indicates the output voltage is again deficient.

transformer-coupled operation

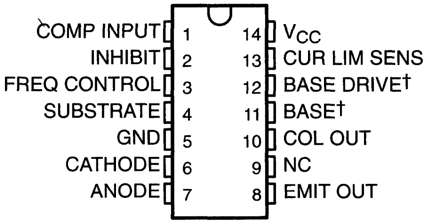
The TL496C operates on alternate half cycles of the ac input during transformer-coupled operation to first sustain the output voltage and second to recharge the batteries. The TL496C performs like a series regulator to supply charge to the output filter/storage capacitor during the first half cycle. The output voltage of the series regulator is slightly higher than that created by the switching circuit. This maintains the feedback voltage above the switching regulator control circuit threshold, effectively inhibiting the switching control circuitry. During the second half cycle, an external diode (1N4001) is used to clamp the negative-going end of the transformer secondary to ground, thus allowing the positive-going end (end connected to V+ side of battery) to pump a charge into the standby batteries.

TL497AC, TL497AI, TL497AY
SWITCHING VOLTAGE REGULATORS

SLVS009C – JUNE 1976 – REVISED AUGUST 1995

- **High Efficiency . . . 60% or Greater**
- **Output Current . . . 500 mA**
- **Input Current Limit Protection**
- **TTL-Compatible Inhibit**
- **Adjustable Output Voltage**
- **Input Regulation . . . 0.2% Typ**
- **Output Regulation . . . 0.4% Typ**
- **Soft Start-Up Capability**

TL497AC, TL497AI . . . D, N, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

† BASE (11) and BASE DRIVE (12) are used for device testing only. They are not normally used in circuit applications of the device.

description

The TL497AC and TL497AI incorporate on a single monolithic chip all the active functions required in the construction of switching voltage regulators. They can also be used as the control element to drive external components for high-power-output applications. The TL497AC and TL497AI were designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

The TL497AC and TL497AI are fixed-on-time variable-frequency switching-voltage-regulator control circuits. The switch-on time is programmed by a single external capacitor connected between FREQ CONTROL and GND. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC}. Thus, the switch-on time remains constant over the specified range of input voltage (4.5 V to 12 V). Typical on times for various values of C_T are as follows:

TIMING CAPACITOR, C_T (pF)	200	250	350	400	500	750	1000	1500	2000
ON TIME (μs)	19	22	26	32	44	56	80	120	180

The output voltage is controlled by an external resistor ladder network (R1 and R2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 V (relative to SUBSTRATE) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T. The internal transistor may be used directly for switching currents up to 500 mA. Its collector and emitter are uncommitted, and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor is also available for blocking or commutating purposes. The TL497AC and TL497AI also have on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL}, connected between V_{CC} and CUR LIM SENS. The current-limit circuitry is activated when 0.7 V is developed across R_{CL}. External gating is provided by the INHIBIT input. When the INHIBIT input is high, the output is turned off.

AVAILABLE OPTIONS

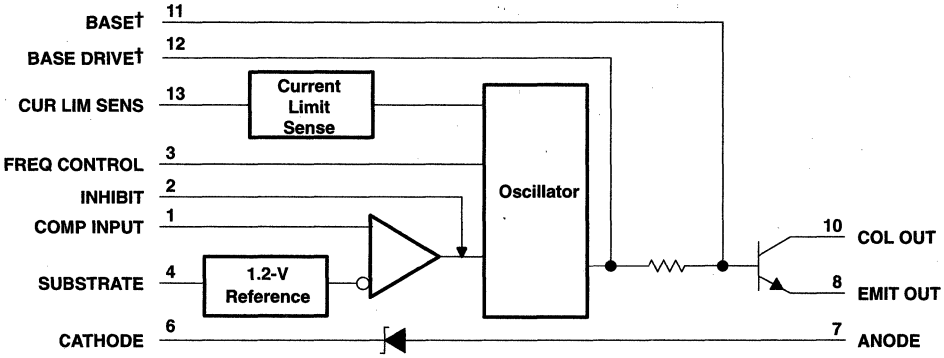
T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SURFACE MOUNT (D)	PLASTIC DIP (N)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL497ACD	TL497ACN	TL497ACPW	TL497AY
–40°C to 85°C	TL497AID	TL497AIN	—	—

description (continued)

Simplicity of design is a primary feature of the TL497AC and TL497AI. With only six external components (three resistors, two capacitors, and one inductor), the TL497AC and TL497AI operates in numerous voltage conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497AC and TL497AI replace the TL497 in all applications.

The TL497AC is characterized for operation from 0°C to 70°C, and the TL497AI is characterized for operation from −40°C to 85°C.

functional block diagram

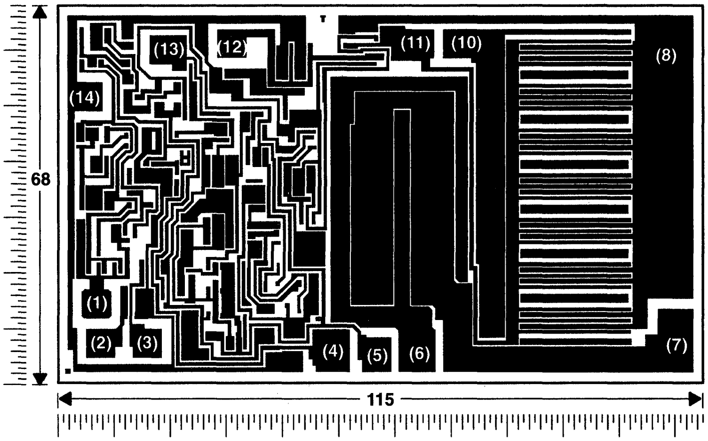


† BASE and BASE DRIVE are used for device testing only. They are not normally used in circuit applications of the device.

TL497AY chip information

This chip, when properly assembled, displays characteristics similar to the TL497AC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



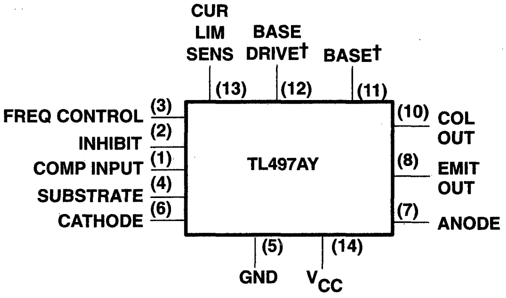
CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max= 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS



† BASE (11) and BASE DRIVE (12) are used for device testing only. They are not normally used in circuit applications of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		15 V
Output voltage, V_O		35 V
Input voltage, V_I(COMP INPUT)		5 V
Input voltage, V_I (INHIBIT)		5 V
Diode reverse voltage		35 V
Power switch current		750 mA
Diode forward current		750 mA
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A:	TL497AC	0°C to 70°C
	TL497AI	−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except diode voltages are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW
N	1000 mW	9.2 mW/°C	41°C	733 mW	595 mW
PW	700 mW	5.6 mW/°C	25°C	448 mW	—

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	12	V
High-level input voltage, V_{IH}, INHIBIT		2.5		V
Low-level input voltage, V_{IL}, INHIBIT			0.8	V
Output voltage	Step-up configuration (see Figure 1)	$V_I + 2$	30	V
	Step-down configuration (see Figure 2)	V_{ref}	$V_I - 1$	
	Inverting regulator (see Figure 3)	$-V_{ref}$	−25	
Power switch current			500	mA
Diode forward current			500	mA
Operating free-air temperature, T_A	TL497AC	0	70	°C
	TL497AI	−40	85	

electrical characteristics over recommended operating conditions, V_{CC} = 6 V (unless otherwise noted)

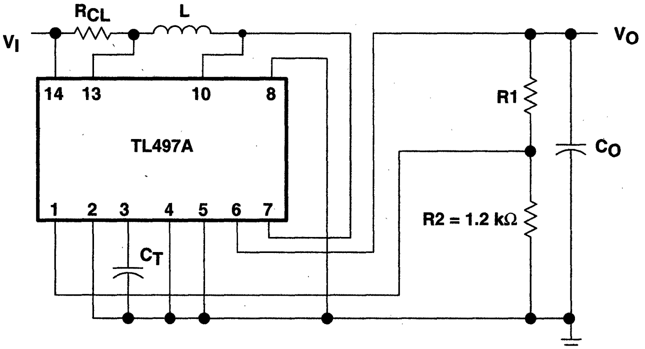
PARAMETER	TEST CONDITIONS	T_A†	TL497AC			TL497AI			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level input current, INHIBIT	$V_{I(I)}$ = 5 V	Full range		0.8	1.5		0.8	1.5	mA
Low-level input current, INHIBIT	$V_{I(I)}$ = 0 V	Full range		5	10		5	20	µA
Comparator reference voltage	V_I = 4.5 V to 6 V	Full range	1.08	1.2	1.32	1.14	1.2	1.26	V
Comparator input bias current	V_I = 6 V	Full range		40	100		40	100	µA
Switch on-state voltage	V_I = 4.5 V, I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
	I_O = 500 mA	Full range			0.85			1	
Switch off-state current	V_I = 4.5 V, V_O = 30 V	25°C		10	50		10	50	µA
		Full range			200			500	
Sense voltage, CUR LIM SENS	V_I = 6 V	25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA	Full range		0.75	0.85		0.75	0.95	V
	I_O = 100 mA	Full range		0.9	1		0.9	1.1	
	I_O = 500 mA	Full range		1.33	1.55		1.33	1.75	
Diode reverse voltage	I_O = 500 µA	Full range				30			V
	I_O = 200 µA	Full range	30						
On-state supply current		25°C		11	14		11	14	mA
		Full range			15			16	
Off-state supply current		25°C		6	9		6	9	mA
		Full range			10			11	

† Full range for the TL497AC is 0°C to 70°C and full range for the TL497AI is −40°C to 85°C.
‡ All typical values are at T_A = 25°C.

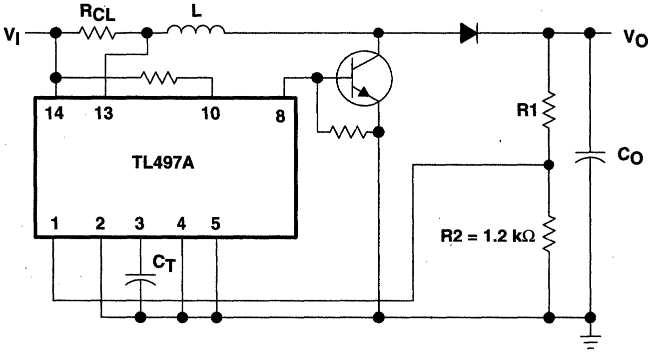
electrical characteristics over recommended operating conditions, V_{CC} = 6 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL497AY			UNIT
		MIN	TYP	MAX	
High-level input current, INHIBIT	$V_{I(I)}$ = 5 V		0.8		mA
Low-level input current, INHIBIT	$V_{I(I)}$ = 0 V		5		µA
Comparator reference voltage	V_I = 4.5 V to 6 V		1.2		V
Comparator input bias current	V_I = 6 V		40		µA
Switch on-state voltage	V_I = 4.5 V, I_O = 100 mA		0.13		V
Switch off-state current	V_I = 4.5 V, V_O = 30 V		10		µA
Diode forward voltage	I_O = 10 mA		0.75		V
	I_O = 100 mA		0.9		
	I_O = 500 mA		1.33		
On-state supply current			11		mA
Off-state supply current			6		mA

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)} < 500$ mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

Figure 1. Positive Regulator, Step-Up Configurations

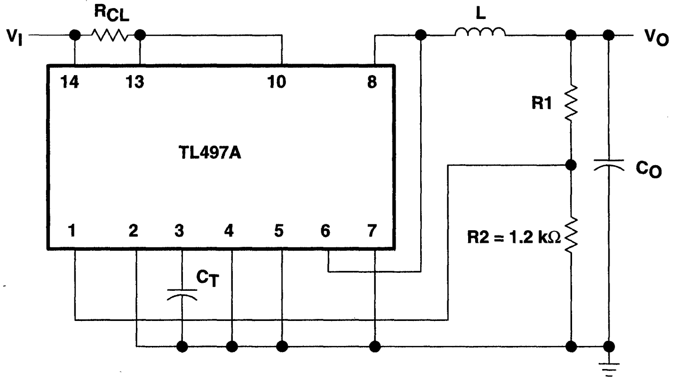
DESIGN EQUATIONS

- $I_{(PK)} = 2\ I_O \max \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{(PK)}} t_{on}\ (\mu s)$

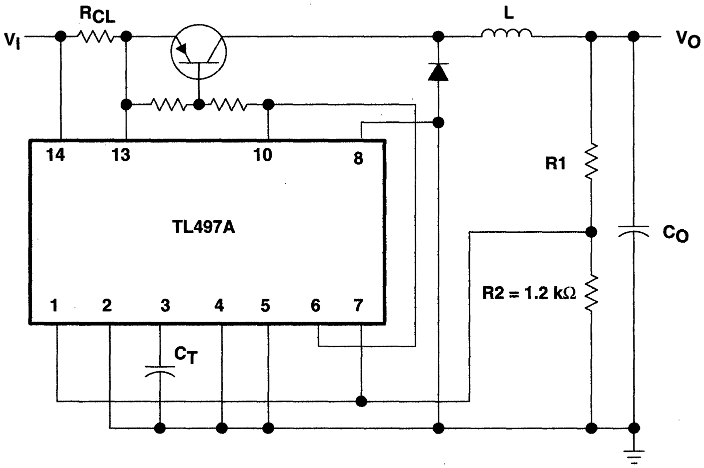
Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{(PK)}}$
- $C_O\ (\mu F) \approx t_{on} (\mu s) \frac{\left[\frac{V_I}{V_O} I_{(PK)} + I_O\right]}{V_{ripple}\ (PK)}$

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)}$ < 500 mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

Figure 2. Positive Regulator, Step-Down Configurations

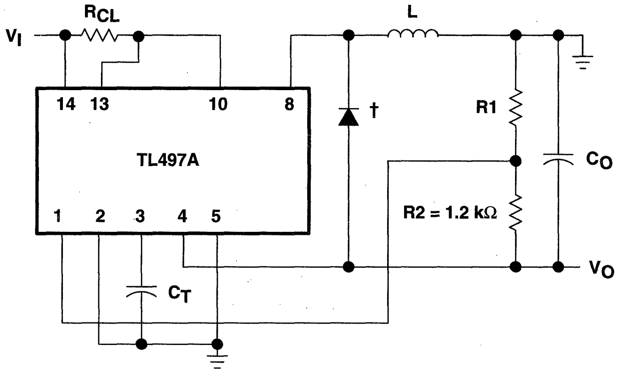
DESIGN EQUATIONS

- $I_{(PK)} = 2\ I_O \text{max}$
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{(PK)}} t_{on}(\mu s)$

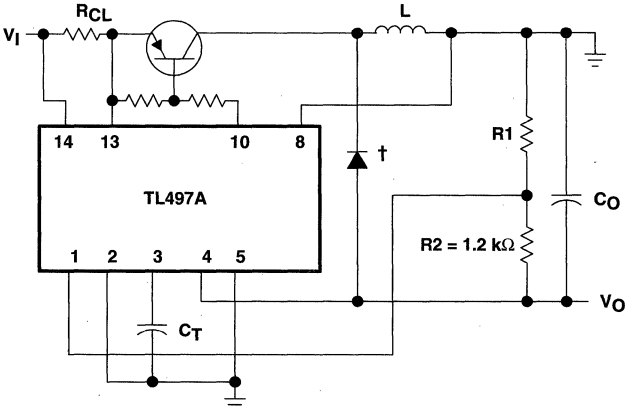
Choose L (50 to 500 µH), calculate t_{on} (10 to 150 µs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \dfrac{0.5\ V}{I_{(PK)}}$
- $C_O\ (\mu F) \approx t_{on}(\mu s) \dfrac{\left[\dfrac{V_I - V_O}{V_O} I_{(PK)} + I_O\right]}{V_{ripple}\ (PK)}$

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)} < 500$ mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

† Use external catch-diode, e.g., 1N4001, when building an inverting supply with the TL497A.

Figure 3. Inverting Applications

DESIGN EQUATIONS

- $I_{(PK)} = 2\ I_O\max\left[1 + \frac{|V_O|}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{(PK)}} t_{on}(\mu s)$

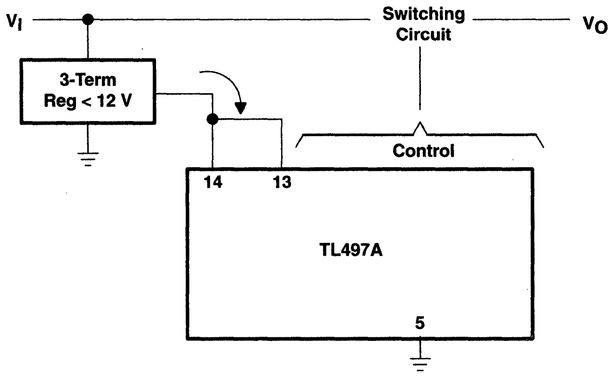
Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = \left(|V_O| - 1.2\right)\ k\Omega$

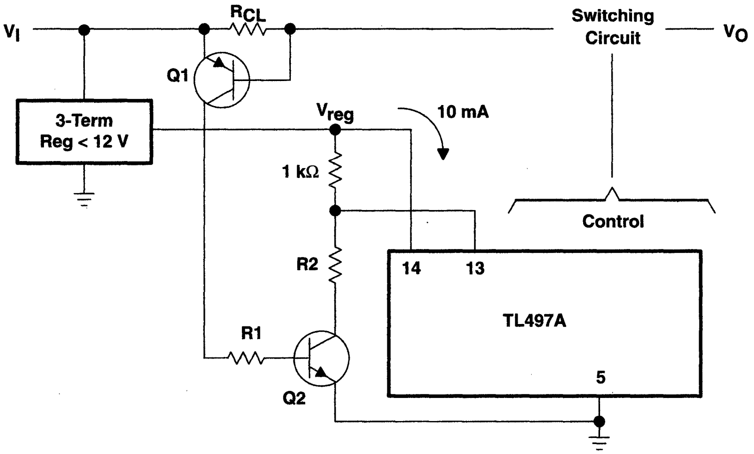
$R_{CL} = \frac{0.5\ V}{I_{(PK)}}$

- $C_O\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{|V_O|} I_{(PK)} + I_O\right]}{V_{ripple}\ (PK)}$

APPLICATION INFORMATION



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



DESIGN EQUATIONS

- $R_{CL} = \dfrac{V_{BE(Q1)}}{I_{limit\ (PK)}}$
- $R1 + \dfrac{V_I}{I_{B(Q2)}}$
- $R2 = \left(V_{reg} - 1\right) 10\ k\Omega$

CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

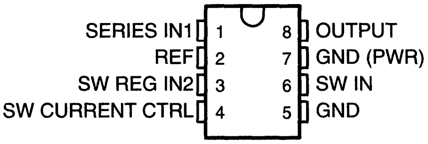
Figure 4. Extended Input Voltage Range (V_I > 12 V)

TL499AC, TL499AY
WIDE-RANGE POWER SUPPLY CONTROLLERS

SLVS029B – JANUARY 1984 – REVISED AUGUST 1995

- **Internal Series-Pass and Step-Up Switching Regulator**
- **Output Adjustable From 2.9 V to 30 V**
- **1-V to 10-V Input for Switching Regulator**
- **4.5-V to 32-V Input for Series Regulator**
- **Externally-Controlled Switching Current**
- **No External Rectifier Required**

D OR P PACKAGE
(TOP VIEW)



description

The TL499AC is a monolithic integrated circuit designed to provide a wide range of adjustable regulated supply voltages. The regulated output voltage is adjustable from 2.9 V to 30 V by adjusting two external resistors. When the TL499AC is ac-coupled to line power through a step-down transformer, it operates as a series dc voltage regulator to maintain the regulated output voltage. With the addition of a battery from 1.1 V to 10 V, an inductor, a filter capacitor, and two resistors, the TL499AC operates as a step-up switching regulator during an ac-line failure.

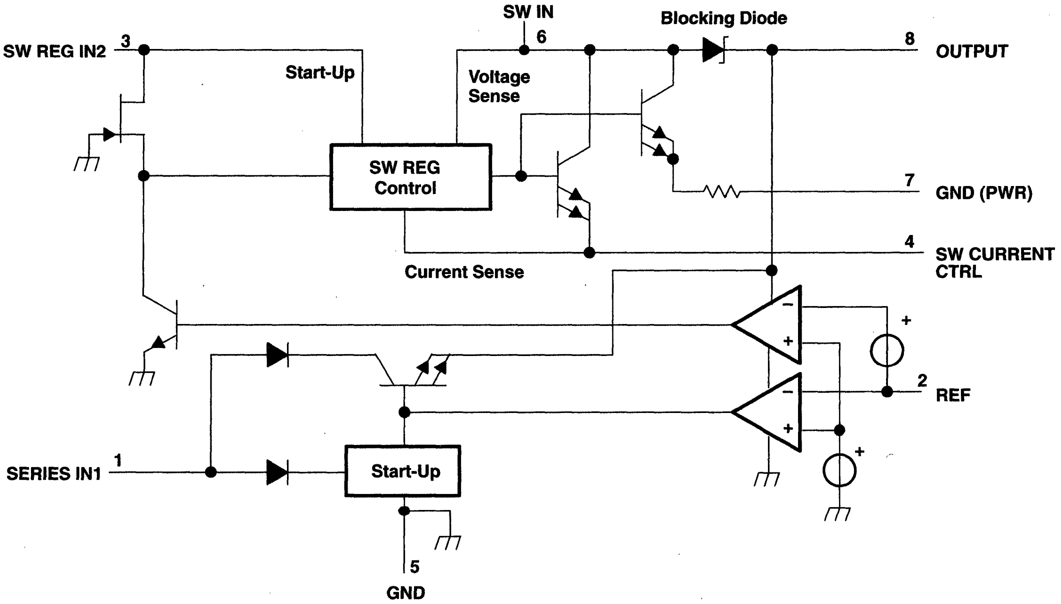
The adjustable regulated output voltage makes the TL499AC useful for a wide range of applications. Providing backup power during an ac-line failure makes the TL499AC extremely useful in microprocessor memory applications.

The TL499AC is designed for operation from –20°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SURFACE MOUNT (D)	PLASTIC DIP (P)	
–20°C to 85°C	TL499ACD	TL499ACP	TL499AY

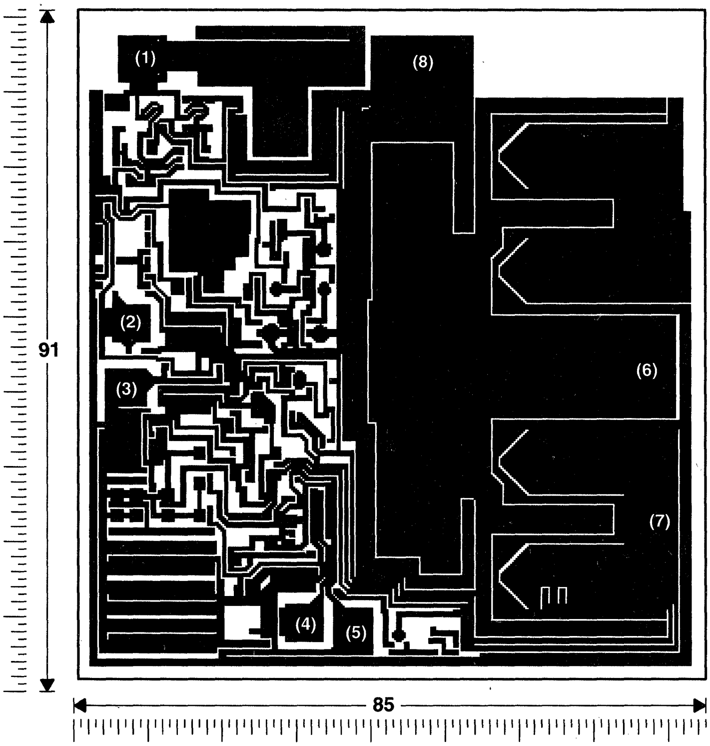
functional block diagram



TL499AY chip information

This chip, when properly assembled, displays characteristics similar to the TL499AC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



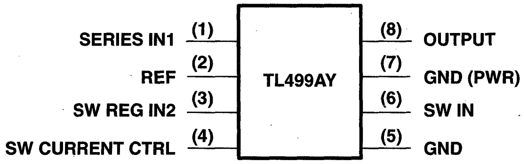
CHIP THICKNESS:
11 MILS TYPICAL

BONDING PADS:
7 X 7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS
ARE IN MILS.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output voltage, V_O (see Note 1)	35 V
Input voltage, series regulator, V_I1	35 V
Input voltage, switching regulator, V_I2	10 V
Blocking diode reverse voltage	35 V
Blocking diode forward current	1 A
Power switch current (SW IN)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–20°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	825 mW	6.6 mW/°C	429 mW
P	1000 mW	8 mW/°C	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Output voltage, V_O	2.9		30	V
Input voltage, V_I1 (SERIES IN1)	4.5		32	V
Input voltage, V_I2 (SW REG IN2)	1.1		10	V
Output-to-input differential voltage, switching regulator, $V_O - V_I2$ (see Note 2)	1.2		28.9	V
Continuous output current, I_O			100	mA
Power switch current (at SW IN)			500	mA
Current-limiting resistor, R_{CL}	150		1000	Ω
Filter capacitor	100		470	μF
Pass capacitor		0.1		μF
Inductor, L (dcr ≤ 0.1 Ω)	50		150	μH
Operating free-air temperature, T_A	–20		85	°C

NOTE 2: When operating temperature range is $T_A \leq 70°C$, minimum $V_O - V_I2$ is ≥ 1.2 V. When operating temperature range is $T_A \leq 85°C$, minimum $V_O - V_I2$ is ≥ 1.9 V.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL499AC			UNIT
			MIN	TYP	MAX	
Voltage deviation (see Note 3)				20	30	mV/V
Dropout voltage	Switching regulator	T_A = −20°C to 70°C			1.2	V
		T_A = −20°C to 85°C			1.9	V
	Series regulator	$V_{I}1$ = 15 V, I_O = 50 mA			1.8	V
Reference voltage (internal)		$V_{I}2$ = 5 V, V_O = 3 V, I_O = 1 mA	1.2	1.26	1.32	V
Reference voltage change with temperature		T_A = −20°C to 85°C		5	10	mV/V
Output regulation (of reference voltage)		I_O = 1 mA to 50 mA		10	30	mV/V
Output current (see Figure 1)	Switching regulator	$V_{I}2$ = 1.1 V, V_O = 12 V, R_{CL} = 150 Ω, T_A = 25°C	10			mA
		$V_{I}2$ = 1.5 V, V_O = 15 V, R_{CL} = 150 Ω, T_A = 25°C	15			
		$V_{I}2$ = 6 V, V_O = 30 V, R_{CL} = 150 Ω, T_A = 25°C	65			
	Series regulator				100	
Standby current	Switching regulator	$V_{I}2$ = 3 V, V_O = 9 V, T_A = 25°C		15	80	µA
	Series regulator	$V_{I}1$ = 15 V, V_O = 9 V, $R_{E}2$ = 4.7 kΩ		0.8	1.2	mA

NOTE 3: Voltage deviation is the output voltage differences that occurs in a change from series regulation to switching regulation.

voltage deviation = V_O (series reg) – (switching reg)

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL499AY			UNIT
			MIN	TYP	MAX	
Voltage deviation (see Note 3)				20	30	mV/V
Dropout voltage	Switching regulator				1.2	V
					1.9	V
	Series regulator	$V_{I}1$ = 15 V, I_O = 50 mA			1.8	V
Reference voltage (internal)		$V_{I}2$ = 5 V, V_O = 3 V, I_O = 1 mA	1.2	1.26	1.32	V
Reference voltage change with temperature				5	10	mV/V
Output regulation (of reference voltage)		I_O = 1 mA to 50 mA		10	30	mV/V
Output current (see Figure 1)	Switching regulator	$V_{I}2$ = 1.1 V, V_O = 12 V, R_{CL} = 150 Ω	10			mA
		$V_{I}2$ = 1.5 V, V_O = 15 V, R_{CL} = 150 Ω	15			
		$V_{I}2$ = 6 V, V_O = 30 V, R_{CL} = 150 Ω	65			
	Series regulator				100	
Standby current	Switching regulator	$V_{I}2$ = 3 V, V_O = 9 V		15	80	µA
	Series regulator	$V_{I}1$ = 15 V, V_O = 9 V, $R_{E}2$ = 4.7 kΩ		0.8	1.2	mA

NOTE 3: Voltage deviation is the output voltage differences that occurs in a change from series regulation to switching regulation.

voltage deviation = V_O (series reg) – (switching reg)

APPLICATION INFORMATION

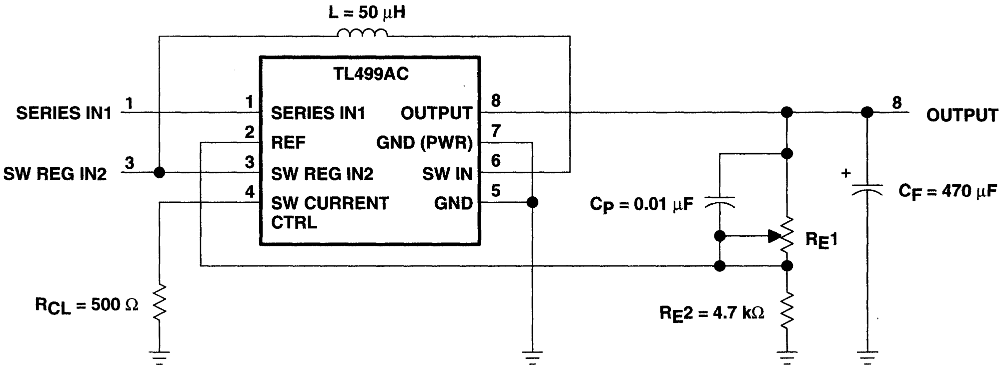


Figure 1. TL499AC Basic Configuration

Table 1. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 150 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										65	90
25									50	80	100
20						20	25	30	80	100	100
15				15	20	30	45	55	100	100	100
12	10	15	20	25	30	40	55	70	100	100	100
10	15	20	25	30	35	45	65	80	100	100	
9	20	25	25	35	40	50	70	90	100	100	
6	30	35	40	45	55	75	95	100			
5	35	40	45	55	70	85	100	100	Circuit of Figure 1 except:		
4.5	35	45	50	60	75	95	100	100†	R_{CL} = 150 Ω		
3	55	65†	75†	95†	100†				C_F = 330 μF		
2.9	60†	70†	75†	100†	100†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

APPLICATION INFORMATION

Table 2. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 200 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										50	100
25									50	70	100
20						15	25	30	70	90	100
15				10	15	25	35	45	90	100	100
12	10	10	15	20	25	35	45	60	100	100	100
10	15	20	20	25	30	40	55	70	100	100	
9	20	20	25	30	35	45	60	80	100		
6	25	30	35	45	50	65	90	100			
5	30	35	40	55	60	75	100	100	Circuit of Figure 1 except:		
4.5	35	40	45	55	65	85	100	100[†]	R_{CL} = 200 Ω		
3	50	55[†]	65[†]	80[†]	90[†]				C_F = 330 µF		
2.9	50[†]	60[†]	65[†]	85[†]	100[†]				C_P = 0.1 µF		

[†] The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 3. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 300 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										40	70
25									40	55	100
20						10	15	20	55	70	100
15				10	10	20	30	35	75	95	100
12	10	10	10	15	20	25	35	45	95	100	100
10	15	15	15	20	25	30	45	55	100	100	
9	15	15	20	25	30	35	50	60	100	100	
6	25	25	30	35	45	55	70	90			
5	30	30	35	45	50	65	85	100	Circuit of Figure 1 except:		
4.5	30	35	40	45	55	70	95	100[†]	R_{CL} = 300 Ω		
3	45	50[†]	55[†]	70[†]	90[†]				C_F = 330 µF		
2.9	45[†]	50[†]	60[†]	75[†]	95[†]				C_P = 0.1 µF		

[†] The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

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Table 4. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 510 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										30	50
25									25	40	75
20									40	55	90
15							15	20	55	70	100
12					10	15	25	35	65	80	100
10				10	20	25	30	40	70	85	
9	10	10	10	15	20	25	35	45	75	100	
6	15	20	20	25	30	35	50	60			
5	20	20	25	30	35	45	55	70	Circuit of Figure 1 except:		
4.5	20	25	30	35	40	50	65	90†	R_{CL} = 510 Ω		
3	35	35†	40†	50†	75†				C_F = 330 µF		
2.9	35†	35†	40†	55†	80†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 5. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 1 kΩ

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30											35
25										35	50
20										35	60
15								10	30	45	65
12								20	40	45	85
10							15	25	40	55	
9				10	10	15	25	30	45	60	
6	10	10	10	15	20	20	30	35			
5	10	10	15	20	20	25	35	40	Circuit of Figure 1 except:		
4.5	15	15	15	20	25	30	40	45†	R_{CL} = 1 kΩ		
3	20	25†	25†	30†	35†				C_F = 330 µF		
2.9	20†	25†	25†	30†	45†				C_P = 0.1 µF		

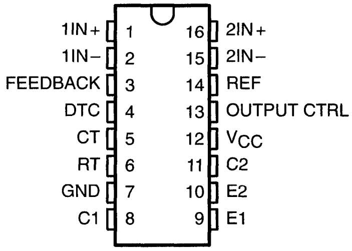
† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

TL594C, TL594I, TL594Y
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS052B – APRIL 1988 – REVISED AUGUST 1995

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **Undervoltage Lockout for Low V_{CC} Conditions**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
$V_I = 0$	Single-ended or parallel output
$V_I = V_{ref}$	Normal push-pull operation

description

The TL594 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

The TL594 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V regulator with a precision of 1%, an undervoltage lockout control circuit, and output control circuitry.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The DTC comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator may be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it may be used to drive the common circuitry in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

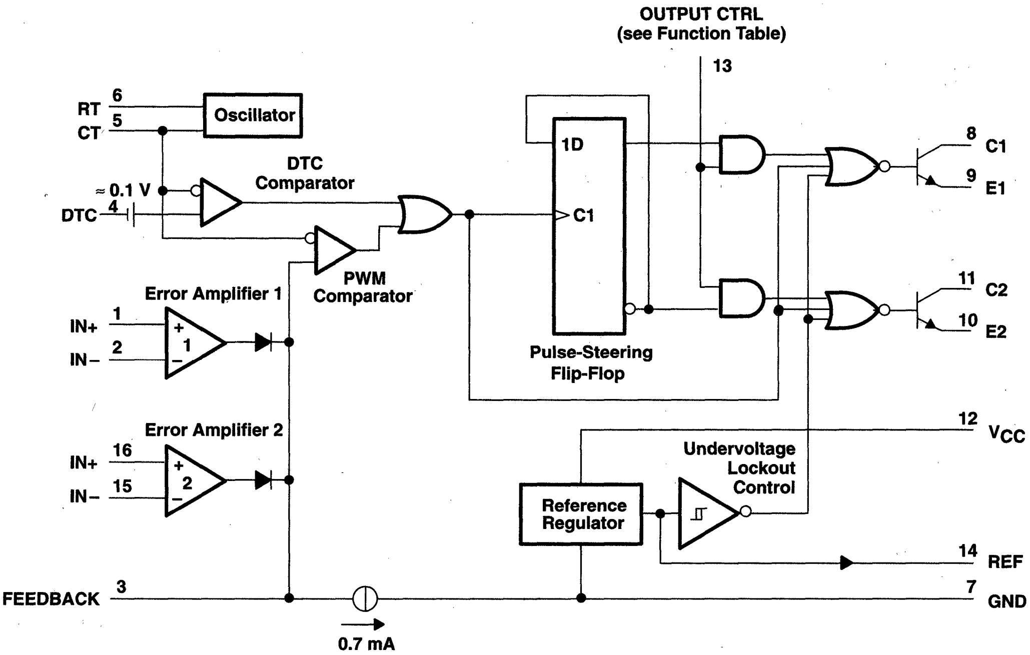
The TL594C is characterized for operation from 0°C to 70°C. The TL594I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE† (D)	PLASTIC DIP (N)	
0°C to 70°C	TL594CD	TL594CN	TL594Y
−40°C to 85°C	TL594ID	TL594IN	

† The D package is available taped and reeled. Add “R” suffix to device type (e.g., TL594CDR).

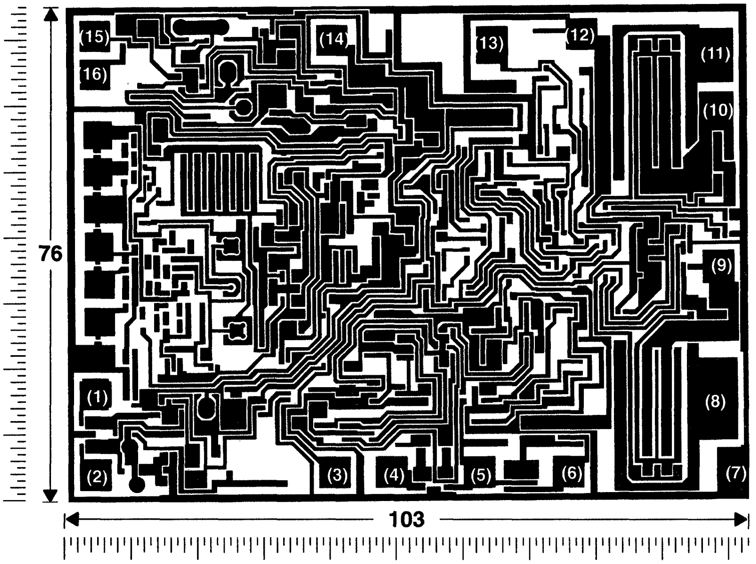
functional block diagram



TL594Y chip information

This chip, when properly assembled, displays characteristics similar to the TL594C (see electrical tables). Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



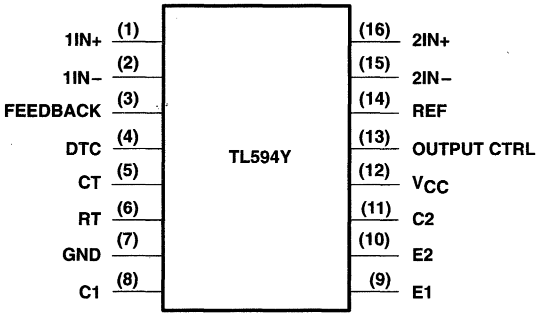
CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	TL594C	TL594I	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	V
Amplifier input voltage	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	41	41	V
Collector output current	250	250	mA
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	0 to 70	−40 to 85	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW
N	1000 mW	9.2 mW/°C	41°C	733 mW	595 mW

recommended operating conditions

	TL594C		TL594I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltage, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10000	0.47	10000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency, f_{osc}	1	300	1	300	kHz
Operating free-air temperature, T_A	0	70	−40	85	°C

electrical characteristics over recommended operating conditions, V_{CC} = 15 V, (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL594C, TL594I			UNIT
		MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA, T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25	mV
Output regulation	I_O = 1 to 10 mA, T_A = 25°C		14	35	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current§	V_{ref} = 0	10	35	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

amplifier section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Input offset voltage, error amplifier	FEEDBACK = 2.5 V		2	10	mV
Input offset current	FEEDBACK = 2.5 V		25	250	nA
Input bias current	FEEDBACK = 2.5 V		0.2	1	µA
Common-mode input voltage range, error amplifier	V_{CC} = 7 V to 40 V	0.3 to $V_{CC}-2$			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V, T_A = 25°C	65	80		dB
Output sink current, FEEDBACK	V_{ID} = –15 mV to –5 V, FEEDBACK = 0.5 V	0.3	0.7		mA
Output source current, FEEDBACK	V_{ID} = 15 mV to 5 V, FEEDBACK = 3.5 V	–2			mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

oscillator section, C_T = 0.01 µF, R_T = 12 kΩ (see Figure 2)

PARAMETER	TEST CONDITIONS†	TL594C, TL594I			UNIT
		MIN	TYP‡	MAX	
Frequency			10		kHz
Standard deviation of frequency§	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature¶	ΔT_A = MIN to MAX			50	Hz/kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:
¶ Temperature coefficient of timing capacitor and timing resistor not taken into account.

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Input bias current	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	DTC = 0 V	0.45			
Input threshold voltage	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

† All typical values except for parameter changes with temperature are at T_A = 25°C.

output section

PARAMETER		TEST CONDITIONS	TL594C, TL594I			UNIT
			MIN	TYP†	MAX	
Collector off-state current		V_C = 40 V, V_E = 0 V, V_{CC} = 40 V		2	100	μA
		DTC and OUTPUT CTRL = 0 V, V_C = 15 V, V_E = 0 V, V_{CC} = 1 to 3 V		4	200	
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V, I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5	mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Input threshold voltage, FEEDBACK	Zero duty cycle		4	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V	0.3	0.7		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

undervoltage lockout section (see Figure 2)

PARAMETER	TEST CONDITIONS†	TL594C, TL594I		UNIT
		MIN	MAX	
Threshold voltage	T_A = 25°C		6	V
	ΔT_A = MIN to MAX	3.5	6.9	
Hysteresis‡		100		mV

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

total device (see Figure 2)

PARAMETER	TEST CONDITIONS		TL594C, TL594I			UNIT
			MIN	TYP†	MAX	
Standby supply current	RT at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	DTC = 2 V,	See Figure 2		12.4		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted) (continued)

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP[†]	MAX	
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			30	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		200	400	ns
Output voltage fall time			45	100	ns

[†] All typical values except for parameter changes with temperature are at T_A = 25°C.

electrical characteristics over recommended operating conditions, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Output voltage (REF)	I_O = 1 mA,		5		V
Input regulation	V_{CC} = 7 V to 40 V,		2		mV
Output regulation	I_O = 1 to 10 mA,		14		mV
Short-circuit output current[†]	V_{ref} = 0		35		mA

[†] Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Frequency			10		kHz
Standard deviation of frequency[†]	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V,		1		Hz/kHz

[†] Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

amplifier section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Input offset voltage, error amplifier	FEEDBACK = 2.5 V		2		mV
Input offset current	FEEDBACK = 2.5 V		25		nA
Input bias current	FEEDBACK = 2.5 V		0.2		µA
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V, T_A = 25°C		80		dB
Output sink current, FEEDBACK	V_{ID} = –15 mV to –5 V, FEEDBACK = 0.5 V		0.7		mA

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Input bias current	V_I = 0 to 5.25 V		−2		μA
Input threshold voltage	Zero duty cycle		3		V

output section

PARAMETER		TEST CONDITIONS	TL594Y			UNIT
			MIN	TYP†	MAX	
Collector off-state current		V_C = 40 V, V_E = 0 V, V_{CC} = 40 V		2		μA
		DTC and OUTPUT CTRL = 0 V, V_C = 15 V, V_E = 0 V, V_{CC} = 1 to 3 V		4		
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0				μA
Collector-emitter saturation voltage	Common emitter	V_E = 0, I_C = 200 mA		1.1		V
	Emitter follower	V_C = 15 V, I_E = −200 mA		1.5		

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage, FEEDBACK	Zero duty cycle		4		V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V		0.7		mA

total device (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Standby supply current	All other inputs and outputs open R_T at V_{ref},		9		mA
Average supply current	DTC = 2 V, See Figure 2		12.4		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Output voltage rise time	Common-emitter configuration, See Figure 3		100		ns
Output voltage fall time			30		ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		200		ns
Output voltage fall time			45		ns

PARAMETER MEASUREMENT INFORMATION

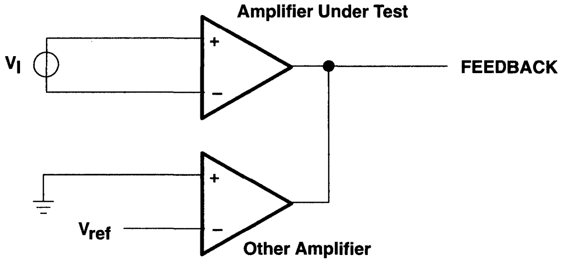
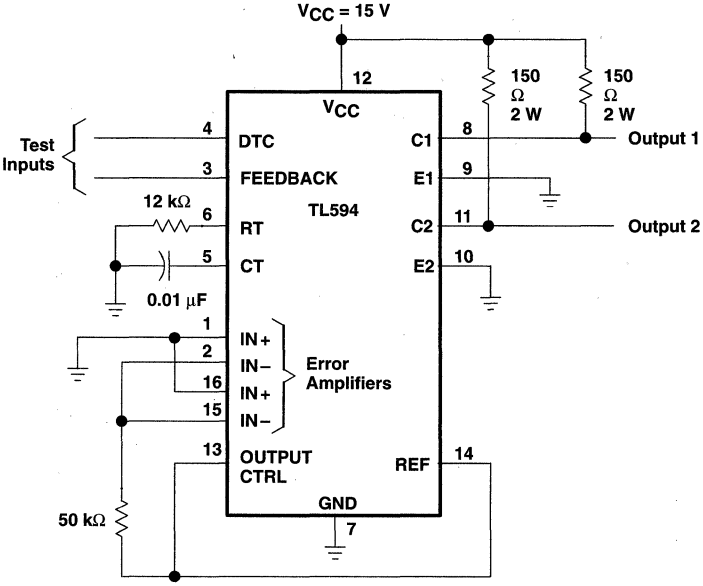
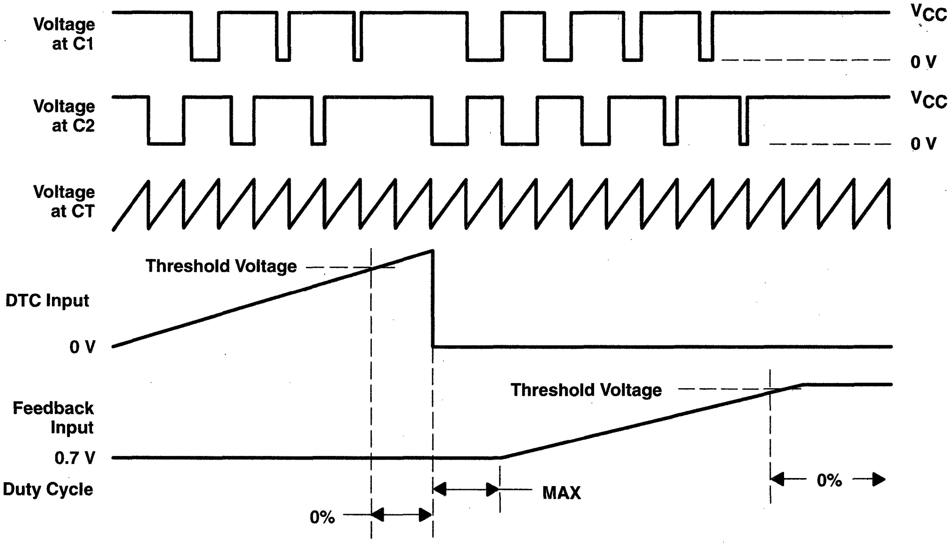


Figure 1. Amplifier Characteristics Test Circuit

PARAMETER MEASUREMENT INFORMATION



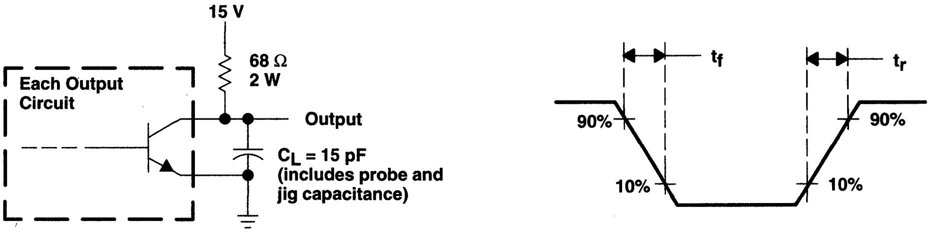
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Operational Test Circuit and Waveforms

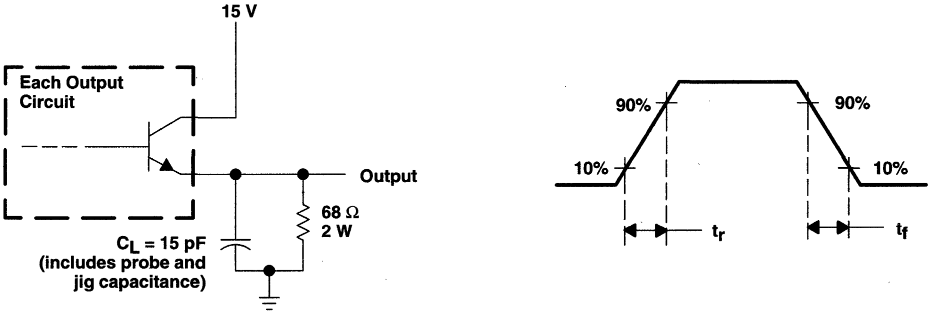
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

Figure 3. Common-Emitter Configuration



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE

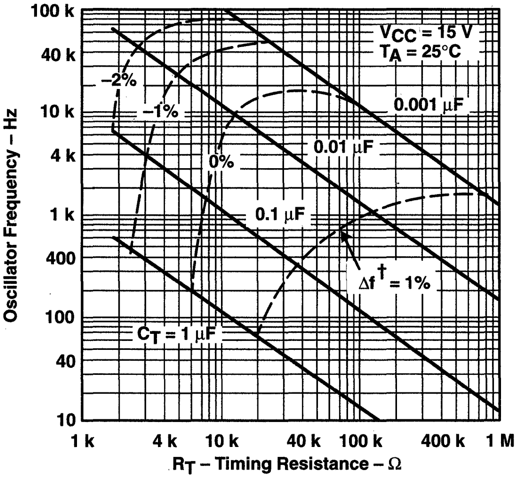


Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

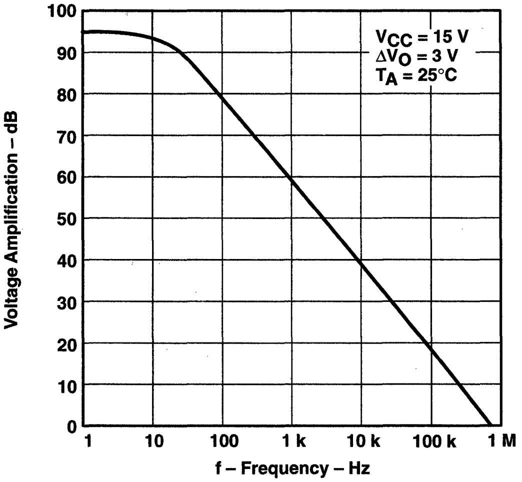


Figure 6

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

TL598C, TL598Q, TL598M, TL598Y
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS053B – FEBRUARY 1988 – REVISED OCTOBER 1995

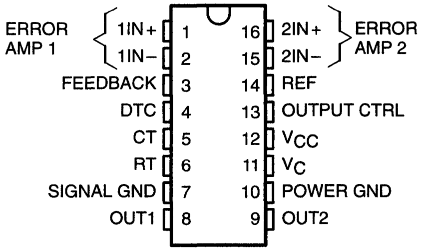
- **Complete PWM Power Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Undervoltage Lockout for Low V_{CC} Conditions**
- **Separate Power and Signal Grounds**
- **TL598Q Has Extended Temperature Range . . . −40°C to 125°C**

description

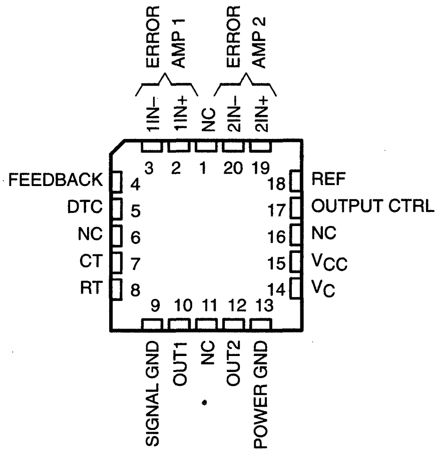
The TL598 incorporates all the functions required in the construction of pulse-width-modulated (PWM) controlled systems on a single monolithic chip. Designed primarily for power supply control, the TL598 provides the systems engineer with the flexibility to tailor the power supply control circuits to a specific application.

The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control (DTC) comparator, a pulse-steering flip-flop, a 5-V precision reference, undervoltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise and fall time performance for power FET control. The outputs share a common source supply and common power ground terminals, which allow system designers to eliminate errors caused by high current-induced voltage drops and common-mode noise.

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = REF	Normal push-pull operation

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	TL598CD	—	—	TL598CN	TL598Y
−40°C to 125°C	TL598QD	—	—	TL598QN	
−55°C to 125°C	—	TL598MFK	TL598MJ	—	

Chip forms are tested at 25°C.

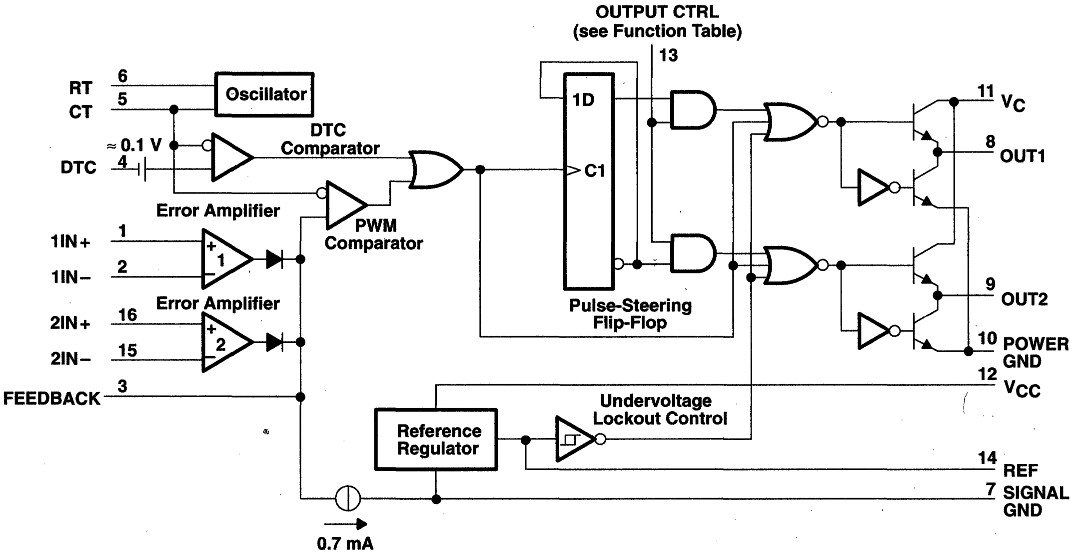
On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

The error amplifier has a common-mode voltage range from 0 V to V_{CC} −2 V. The DTC comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. A synchronous multiple supply operation may be achieved by connecting RT to the reference output and providing a sawtooth input to CT.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation. The output frequency for push-pull applications is one-half the oscillator frequency $\left(f_O = \frac{1}{2\ RT\ CT}\right)$. For single-ended applications: $f_O = \frac{1}{RT\ CT}$

The TL598C is characterized for operation from 0°C to 70°C. The TL598Q is characterized for operation from −40°C to 125°C. The TL598M is characterized for operation from −55°C to 125°C.

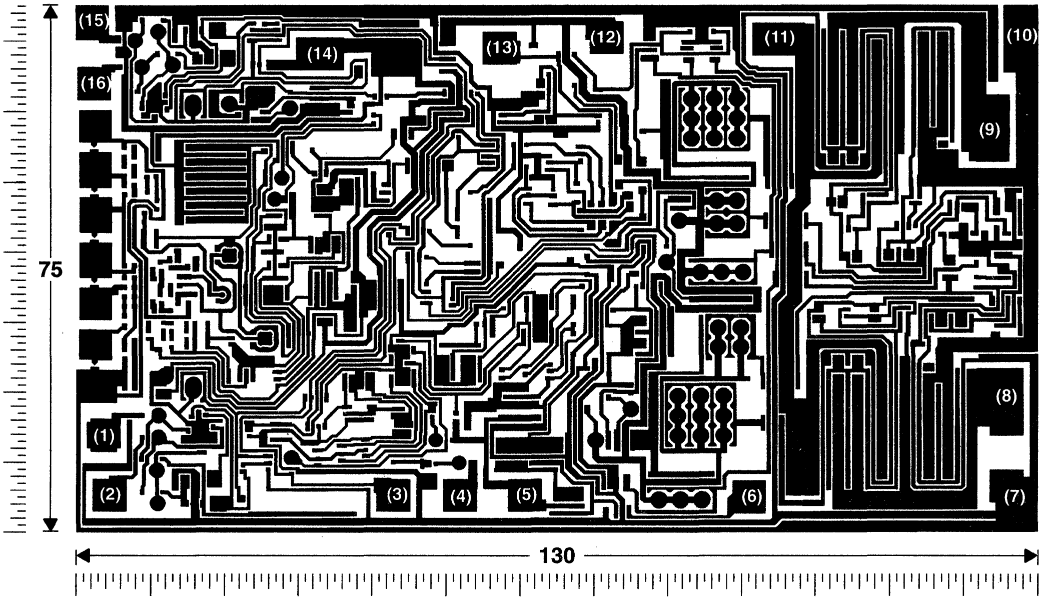
functional block diagram

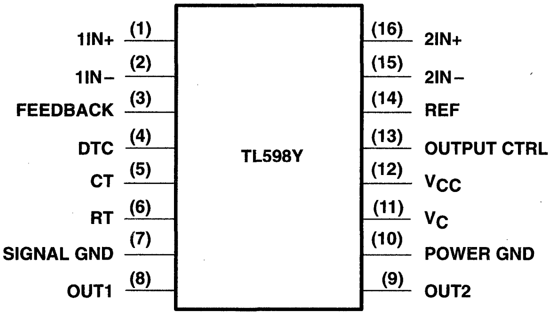


TL598Y chip information

This chip, when properly assembled, displays characteristics similar to the TL598C. Thermal compression or ultrasonic bonding can be used on the doped aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		41 V
Amplifier input voltage, V_I		V_{CC} + 0.3 V
Collector voltage		41 V
Output current (each output), sink or source, I_O		250 mA
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J:	TL598C	0°C to 150°C
	TL598Q	−40°C to 150°C
	TL598M	−55°C to 150°C
Storage temperature range, T_{stg}		−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N packages		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300°C

---

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to the signal ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	800 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	230 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		0	$V_{CC}-2$	V
Collector voltage			40	V
Output current (each output), sink or source, I_O			200	mA
Current into feedback terminal, I_{IL}			0.3	mA
Timing capacitor, C_T		0.00047	10	µF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Operating free-air temperature, T_A	TL598C	0	70	°C
	TL598Q	−40	125	
	TL598M	−55	125	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

reference section (see Note 2)

PARAMETER	TEST CONDITIONS†		TL598C			TL598Q			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	25		2	22	mV
Output regulation	I_O = 1 mA to 10 mA	T_A = 25°C		1	15		1	15	mV
		T_A = MIN to MAX			50			80	
Output voltage change with temperature	ΔT_A = MIN to MAX			2	10		2	10	mV/V
Short-circuit output current§	REF = 0 V		−10	−48		−10	−48		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 2: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

oscillator section, C_T = 0.001 μF, R_T = 12 kΩ (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS†	TL598C, TL598Q			UNIT
		MIN	TYP‡	MAX	
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1	10	Hz/kHz
Frequency change with temperature#	ΔT_A = MIN to MAX		70	120	Hz/kHz
	ΔT_A = MIN to MAX, C_T = 0.01 μF		50	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

Effects of temperature on external R_T and C_T are not taken into account.
NOTE 2: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

error amplifier section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP‡	MAX	
Input offset voltage	FEEDBACK = 2.5 V		2	10	mV
Input offset current	FEEDBACK = 2.5 V		25	250	nA
Input bias current	FEEDBACK = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	FEEDBACK = 0.5 V	0.3	0.7		mA
Output source current (FEEDBACK)	FEEDBACK = 3.5 V	−2			mA
Phase margin at unity gain	FEEDBACK = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply voltage rejection ratio	FEEDBACK = 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 2: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

undervoltage lockout section (see Note 2)

PARAMETER	TEST CONDITIONS†	TL598C		TL598Q		UNIT
		MIN	MAX	MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	4	6	V
	ΔT_A = MIN to MAX	3.5	6.9	3	6.9	
Hysteresis‡	T_A = 25°C	100		100		mV
	T_A = MIN to MAX	50		30		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

output section (see Note 2)

PARAMETER	TEST CONDITIONS		TL598C, TL598Q		UNIT
			MIN	MAX	
High-level output voltage	V_{CC} = 15 V,	I_O = −200 mA	12		V
	V_C = 15 V	I_O = −20 mA	13		
Low-level output voltage	V_{CC} = 15 V,	I_O = 200 mA		2	V
	V_C = 15 V	I_O = 20 mA		0.4	
Output control input current	$V_I = V_{ref}$			3.5	mA
	V_I = 0.4 V			100	μA

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

dead-time control section (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS	TL598C			TL598Q			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
Input bias current (DTC)	V_I = 0 to 5.25 V		−2	−10		−2	−25	μA
Maximum duty cycle, each output	DTC = 0 V	0.45			0.45			
Input threshold voltage (DTC)	Zero duty cycle		3	3.3		3	3.2	V
	Maximum duty cycle	0			0			

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

pwm comparator section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP§	MAX	
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75	4.5	V
Input sink current (FEEDBACK)	$V_{(FEEDBACK)}$ = 0.5 V	0.3	0.7		mA

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

total device (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS		TL598C, TL598Q			UNIT
			MIN	TYP§	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15	21	mA
		V_{CC} = 40 V		20	26	
Average supply current	DTC = 2 V			15		mA

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

switching characteristics, T_A = 25°C (see Note 2)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP	MAX	
Output voltage rise time	CL = 1500 pF, VC = 15 V, VCC = 15 V, See Figure 2		60	150	ns
Output voltage fall time			35	75	

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

reference section (see Note 2)

PARAMETER	TEST CONDITIONS[†]		TL598M			UNIT
			MIN	TYP[‡]	MAX	
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	22	mV
Output regulation	I_O = 1 mA to 10 mA	T_A = 25°C		1	15	mV
		T_A = MIN to MAX			80	
Output voltage change with temperature	ΔT_A = MIN to MAX			0.5%		
Short-circuit output current[§]	REF = 0		−10	−48		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values except for parameter changes with temperature are at T_A = 25°C.

[§] Duration of the short circuit should not exceed one second.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

oscillator section, C_T = 0.001 μF, R_T = 12 kΩ (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS[†]	TL598M			UNIT
		MIN	TYP[‡]	MAX	
Frequency			100		kHz
Standard deviation of frequency[¶]	All values of V_{CC}, C_T, R_T, T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%	1%	
Frequency change with temperature[#]	ΔT_A = MIN to MAX		7%	15%[*]	

[*] On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values except for parameter changes with temperature are at T_A = 25°C.

[¶] Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N}(x_n - X)^2}{N - 1}}$$

[#] Effects of temperature on external R_T and C_T are not taken into account.

NOTE 2: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

error amplifier section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598M			UNIT
		MIN	TYP†	MAX	
Input offset voltage	FEEDBACK at 2.5 V		2	10	mV
Input offset current	FEEDBACK at 2.5 V		25	250	nA
Input bias current	FEEDBACK at 2.5 V		0.2	1	µA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	FEEDBACK at 0.5 V	0.3	0.7		mA
Output source current (FEEDBACK)	FEEDBACK at 3.5 V	−2			mA
Phase margin at unity gain	FEEDBACK at 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply voltage rejection ratio	FEEDBACK at 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

† All typical values except for parameter changes with temperature are at T_A = 25°C.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

undervoltage lockout section (see Note 2)

PARAMETER	TEST CONDITIONS‡	TL598M		UNIT
		MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	V
	ΔT_A = MIN to MAX	3	6.9	
Hysteresis§	T_A = 25°C	100		mV
	T_A = MIN to MAX	30		

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

output section (see Note 2)

PARAMETER	TEST CONDITIONS		TL598M			UNIT
			MIN	TYP	MAX	
Collector off-state current	V_{CE} = 40 V, V_{CC} = 40 V, DTC connected to 0 V			2	100	µA
High-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = −200 mA	12			V
		I_O = −20 mA	13			
Low-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = 200 mA			2	V
		I_O = 20 mA			0.4	
Output control input current	V_I = REF				3.5	mA
	V_I = 0.4 V				100	µA

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 15$ V (unless otherwise noted)

dead-time control section (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS	TL598M			UNIT
		MIN	TYP†	MAX	
Input bias current (DTC)	$V_I = 0$ to 5.25 V		−2	−25	μA
Maximum duty cycle, each output	DTC at 0 V	45%*			
Input threshold voltage (DTC)	Zero duty cycle		3	3.2	V
	Maximum duty cycle	0*			

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All typical values except for parameter changes with temperature are at $T_A = 25°C$.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

pwm comparator section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598M			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75	4.5	V
Input sink current (FEEDBACK)	$V_{(FEEDBACK)} = 0.5$ V	0.3	0.7		mA

† All typical values except for parameter changes with temperature are at $T_A = 25°C$.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

total device (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS		TL598M			UNIT
			MIN	TYP†	MAX	
Standby supply current	RT at REF, All other inputs and outputs open	$V_{CC} = 15$ V		15	21	mA
		$V_{CC} = 40$ V		20	26	
Average supply current	DTC at 2 V			15		mA

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

switching characteristics, $T_A = 25°C$ (see Note 2)

PARAMETER	TEST CONDITIONS	TL598M			UNIT
		MIN	TYP	MAX	
Output voltage rise time	CL = 1500 pF, VC = 15 V, VCC = 15 V, See Figure 2			150*	ns
Output voltage fall time				75*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

NOTE 2: Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C

reference section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP†	MAX	
Output voltage (REF)	I_O = 1 mA		5		V
Input regulation	V_{CC} = 7 V to 40 V		2		mV
Output regulation	I_O = 1 mA to 10 mA		1		mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2		mV/V
Short-circuit output current‡	REF = 0 V		−48		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

‡ Duration of the short circuit should not exceed one second.

NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

oscillator section, C_T = 0.001 µF, R_T = 12 kΩ (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Frequency			100		kHz
Standard deviation of frequency§	All values of V_{CC}, C_T, R_T, T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V,		1		Hz/kHz

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N}(x_n - X)^2}{N - 1}}$$

NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

error amplifier section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input offset voltage	Feedback = 2.5 V		2		mV
Input offset current	Feedback = 2.5 V		25		nA
Input bias current	Feedback = 2.5 V		0.2		µA
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V,		80		dB
Output sink current (FEEDBACK)	FEEDBACK = 0.5 V		0.7		mA
Phase margin at unity gain	FEEDBACK = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply voltage rejection ratio	FEEDBACK = 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C

dead-time control section (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input bias current (DTC)	V_I = 0 to 5.25 V		−2		µA
Input threshold voltage (DTC)	Zero duty cycle		3		V

NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

pwm comparator section (see Note 2)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75		V
Input sink current (FEEDBACK)	FEEDBACK = 0.5 V		0.7		mA

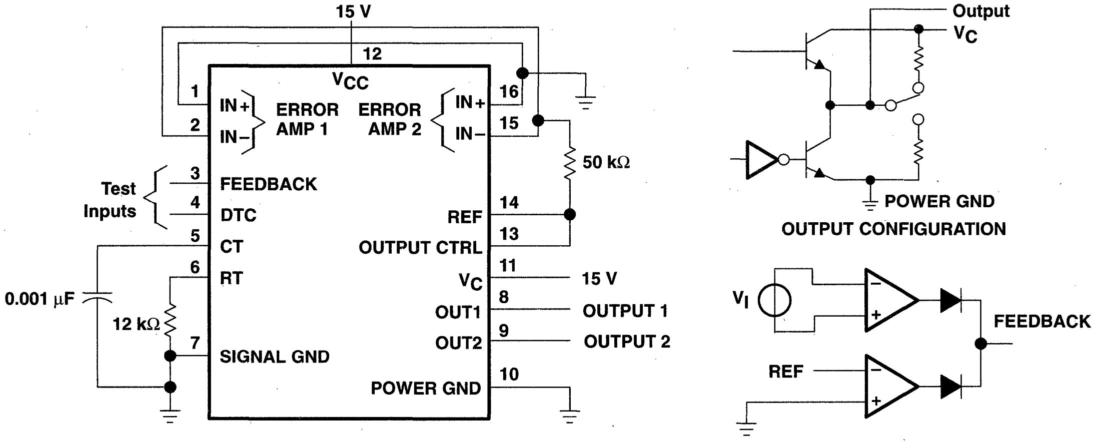
NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

total device (see Figure 1) (see Note 2)

PARAMETER	TEST CONDITIONS		TL598Y			UNIT
			MIN	TYP	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15		mA
		V_{CC} = 40 V		20		
Average supply current	DTC = 2 V			15		mA

NOTE 2 Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

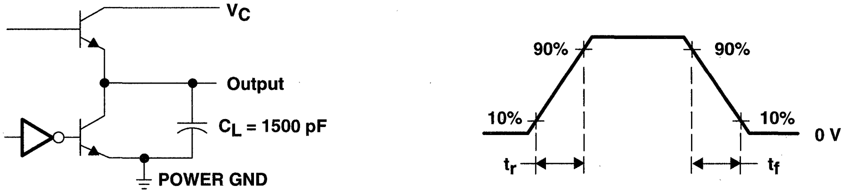
PARAMETER MEASUREMENT INFORMATION



MAIN DEVICE TEST CIRCUIT

ERROR AMPLIFIER TEST CIRCUIT

Figure 1. Test Circuits



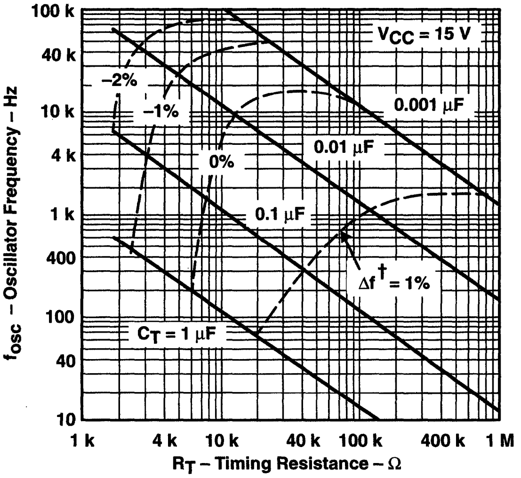
OUTPUT CONFIGURATION

OUTPUT VOLTAGE WAVEFORM

Figure 2. Switching Output Configuration and Voltage Waveform

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE



† Frequency variation (Δf) is the change in predicted oscillator frequency that occurs over the full temperature range.

Figure 3

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

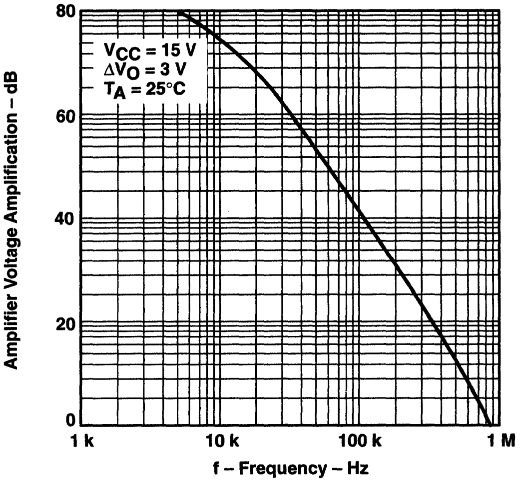


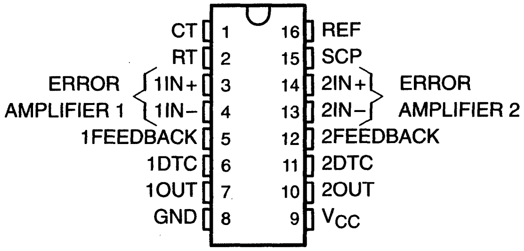
Figure 4

TL1451AC, TL1451AY
DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024C – FEBRUARY 1983 – REVISED OCTOBER 1995

- **Complete PWM Power Control Circuitry**
- **Completely Synchronized Operation**
- **Internal Undervoltage Lockout Protection**
- **Wide Supply Voltage Range**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 500 kHz Max**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 2.5-V Reference Supply**

DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description

The TL1451AC incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation (PWM) control circuits. Designed primarily for power supply control, the TL1451AC contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control (DTC) comparator has no offset unless externally altered and can provide 0% to 100% dead time. The on-chip oscillator can be operated by terminating RT and CT. During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

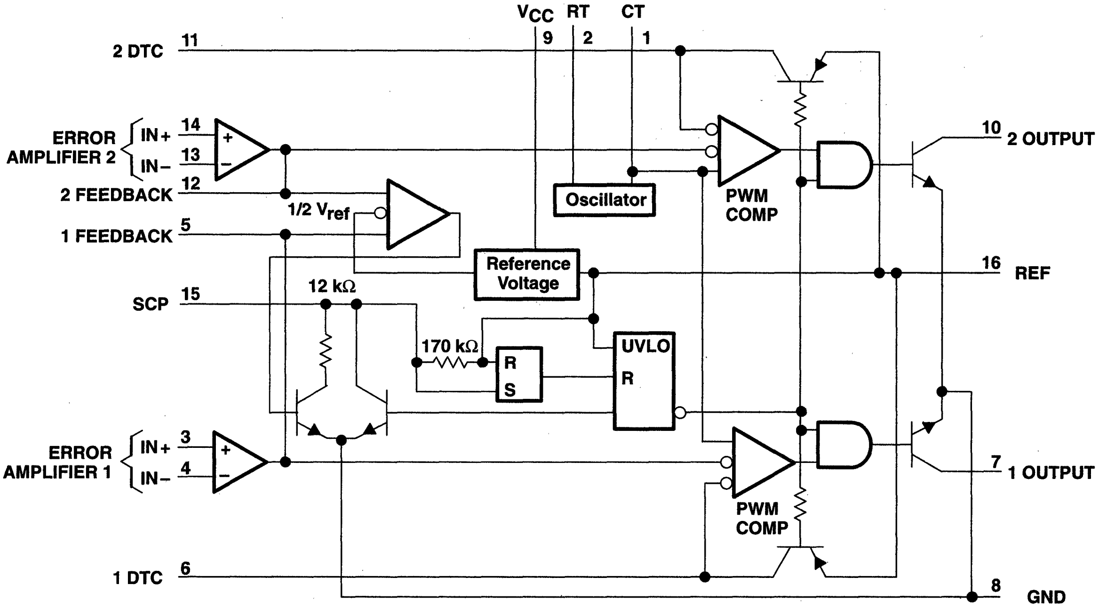
The TL1451AC is characterized for operation from −20°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (DB)†	PLASTIC DIP (N)	SMALL OUTLINE (NS)	TSSOP (PW)†	
−20°C to 85°C	TL1451ACDB	TL1451ACN	TL1451ACNS	TL1451ACPW	TL1451AY

† The DB and PW packages are only available left-end taped and reeled (add LE suffix, i.e., TL1451ACPWLE).

functional block diagram



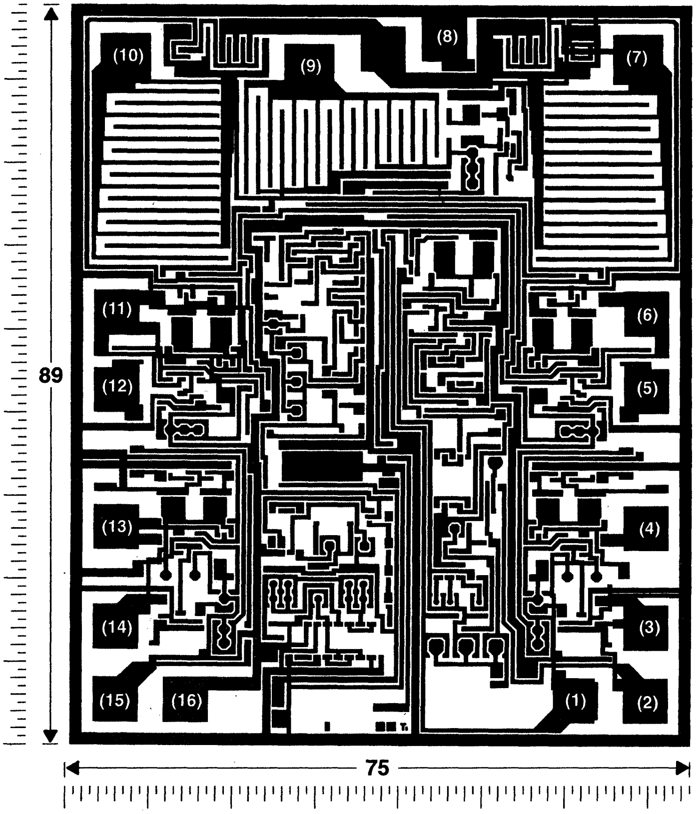
COMPONENT COUNT

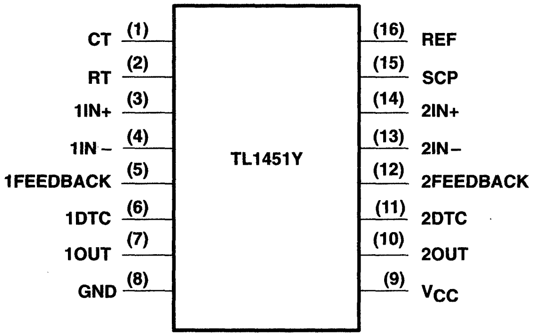
Resistors	65
Capacitors	8
Transistors	105
JFETs	18

TL1451AY chip information

This chip, when properly assembled, displays characteristics similar to the TL1451AC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES
ARE ±10%.

ALL DIMENSIONS
ARE IN MILS.

absolute maximum ratings over operating free-air temperature range[†]

Supply voltage, V_{CC}	51 V
Amplifier input voltage, V_I	20 V
Collector output voltage, V_O	51 V
Collector output current, I_O	21 mA
Continuous power total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−20°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	775 mW	6.2 mW/°C	496 mW	403 mW
N	1000 mW	8.0 mW/°C	640 mW	520 mW
NS	500 mW	4.0 mW/°C	320 mW	260 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	50	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		50	V
Collector output current, I_O		20	mA
Current into feedback terminal		45	μA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451Y			UNIT
		MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
Output voltage (pin 16)	I_O = 1 mA	2.4	2.5	2.6		2.5		V
Output voltage change with temperature	T_A = −20°C to 25°C		−0.1%	±1%		−0.1%		
	T_A = 25°C to 85°C		−0.2%	±1%		−0.2%		
Input voltage regulation	V_{CC} = 3.6 V to 40 V		2	12.5		2		mV
Output voltage regulation	I_O = 0.1 mA to 1 mA		1	7.5		1		mV
Short-circuit output current	V_O = 0	3	10	30		10		mA

[†] All typical values are at T_A = 25°C.

undervoltage lockout section

PARAMETER	TEST CONDITIONS	TL1451AC, TL1451AY			UNIT
		MIN	TYP†	MAX	
Upper threshold voltage (V_{CC})	$I_{O(ref)} = 0.1$ mA, $T_A = 25°C$		2.72		V
Lower threshold voltage (V_{CC})			2.6		V
Hysteresis (V_{CC})		80	120		mV
Reset threshold voltage (V_{CC})		1.5	1.9		V

† All typical values are at $T_A = 25°C$.

short-circuit protection control section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input threshold voltage (SCP)	$T_A = 25°C$	0.65	0.7	0.75	0.65	0.7	0.75	V
Standby voltage (SCP)	No pullup	140	185	230		185		mV
Latched input voltage (SCP)	No pullup		60	120		60		mV
Input (source) current	$V_I = 0.7$ V, $T_A = 25°C$	−10	−15	−20	−10	−15	−20	μA
Comparator threshold voltage (FEEDBACK)			1.18			1.18		V

† All typical values are at $T_A = 25°C$.

oscillator section

PARAMETER	TEST CONDITIONS	TL1451C			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$C_T = 330$ pF, $R_T = 10$ kΩ		200			200		kHz
Standard deviation of frequency	$C_T = 330$ pF, $R_T = 10$ kΩ		10%			10%		
Frequency change with voltage	$V_{CC} = 3.6$ V to 40 V		1%			1%		
Frequency change with temperature	$T_A = -20°C$ to 25°C		−0.4%	±2%		−0.4%		
	$T_A = 25°C$ to 85°C		−0.2%	±2%		−0.2%		

† All typical values are at $T_A = 25°C$.

dead-time control section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input bias current (DTC)				1				μA
Latch mode (source) current (DTC)	$T_A = 25°C$	−80	−145		−80	−145		μA
Latched input voltage (DTC)	$I_O = 40$ μA	2.3						V
Input threshold voltage at f = 10 kHz (DTC)	Zero duty cycle		2.05	2.25		2.05		V
	Maximum duty cycle	1.2	1.45			1.45		

† All typical values are at $T_A = 25°C$.

error-amplifier section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input offset voltage	V_O (FEEDBACK) = 1.25 V			±6				mV
Input offset current	V_O (FEEDBACK) = 1.25 V			±100				nA
Input bias current	V_O (FEEDBACK) = 1.25 V		160	500		160		nA
Common-mode input voltage range	V_{CC} = 3.6 V to 40 V	1.05 to 1.45						V
Open-loop voltage amplification	R_F = 200 kΩ	70	80			80		dB
Unity-gain bandwidth			1.5			1.5		MHz
Common-mode rejection ratio		60	80			80		dB
Positive output voltage swing		$V_{ref}-0.1$						V
Negative output voltage swing				1				V
Output (sink) current (FEEDBACK)	V_{ID} = −0.1 V, V_O = 1.25 V	0.5	1.6			1.6		mA
Output (source) current (FEEDBACK)	V_{ID} = 0.1 V, V_O = 1.25 V	−45	−70			−70		μA

† All typical values are at T_A = 25°C.

output section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Collector off-state current	V_O = 50 V			10				μA
Output saturation voltage	I_O = 10 mA		1.2	2		1.2		V
Short-circuit output current	V_O = 6 V		90			90		mA

† All typical values are at T_A = 25°C.

pwm comparator section

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input threshold voltage at f = 10 kHz (FEEDBACK)	Zero duty cycle		2.05	2.25		2.05		V
	Maximum duty cycle	1.2	1.45			1.45		

† All typical values are at T_A = 25°C.

total device

PARAMETER	TEST CONDITIONS	TL1451AC			TL1451AY			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	Off-state		1.3	1.8		1.3		mA
Average supply current	R_T = 10 kΩ		1.7	2.4		1.7		mA

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

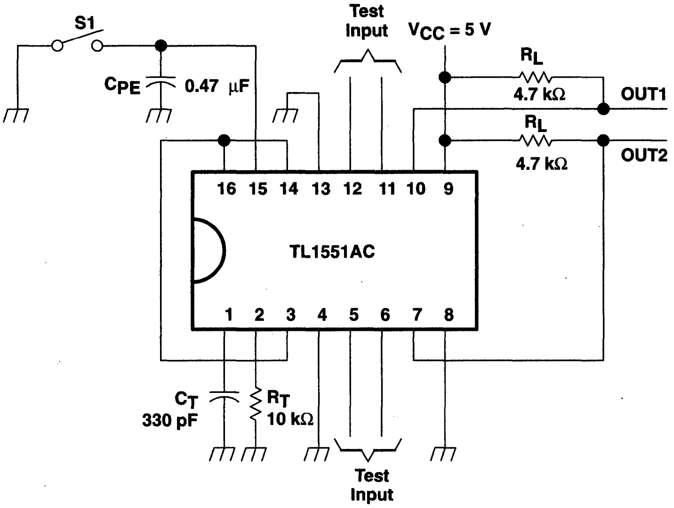
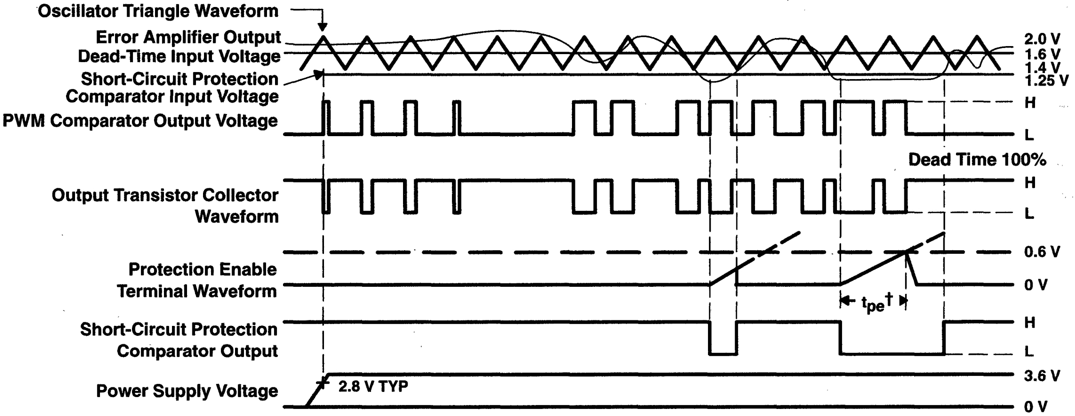


Figure 1. Test Circuit



† Protection Enable Time, $t_{pe} = (0.051 \times 10^6 \times C_{pe})$ in seconds

Figure 2. TL1451AC Timing Diagram

TYPICAL CHARACTERISTICS

TRIANGLE OSCILLATOR FREQUENCY vs TIMING RESISTANCE

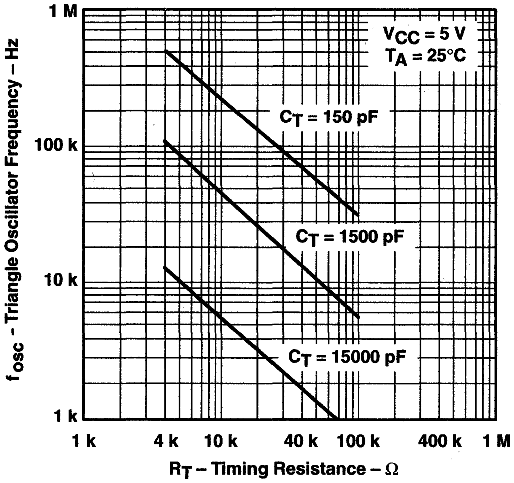


Figure 3

OSCILLATOR FREQUENCY VARIATION vs FREE-AIR TEMPERATURE

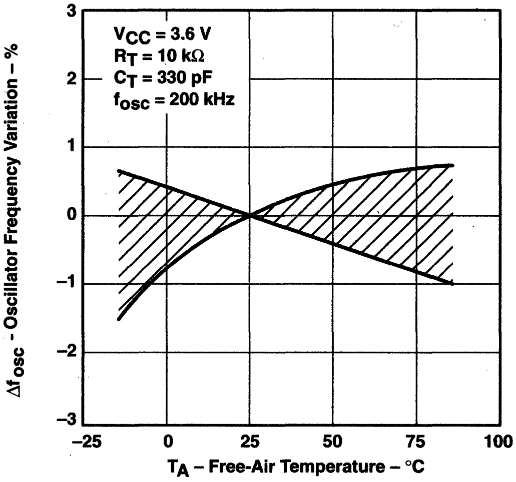


Figure 4

TRIANGLE WAVEFORM SWING VOLTAGE vs TIMING CAPACITANCE

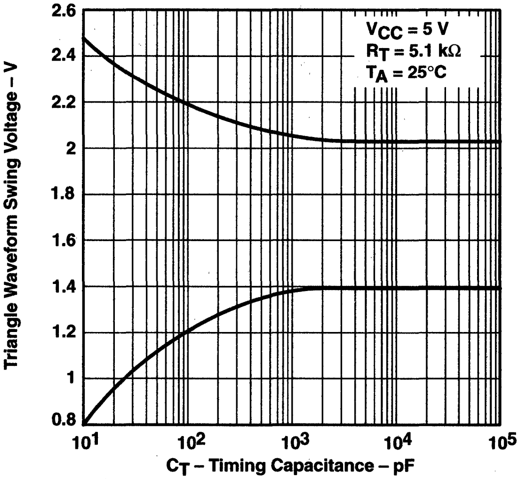


Figure 5

TRIANGLE WAVEFORM PERIOD vs TIMING CAPACITANCE

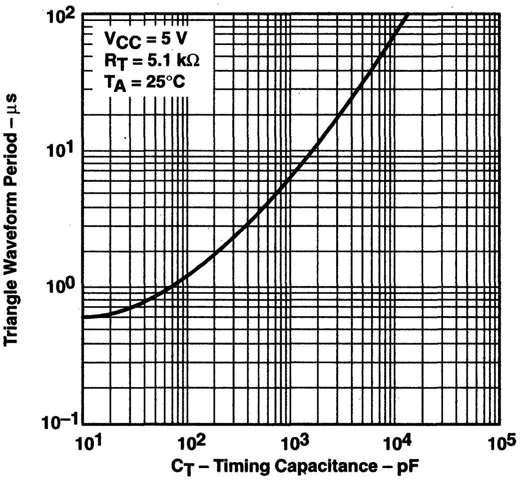


Figure 6

TYPICAL CHARACTERISTICS

REFERENCE OUTPUT VOLTAGE VARIATION vs FREE-AIR TEMPERATURE

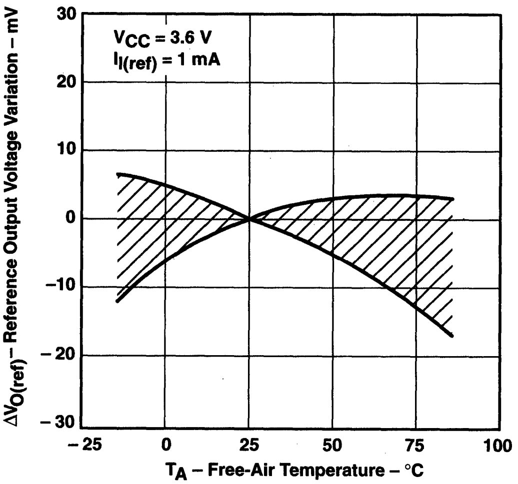


Figure 7

REFERENCE OUTPUT VOLTAGE VARIATION vs FREE-AIR TEMPERATURE

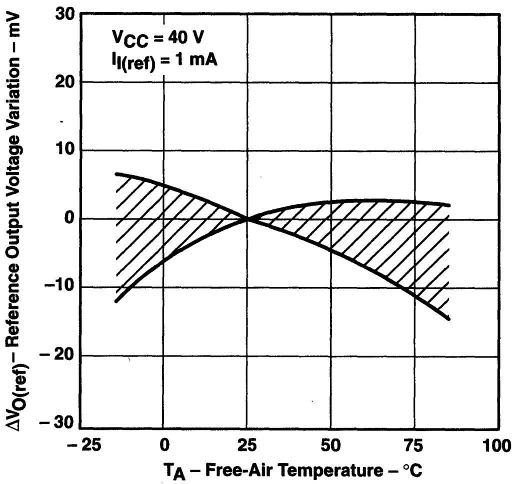


Figure 8

REFERENCE OUTPUT VOLTAGE vs SUPPLY VOLTAGE

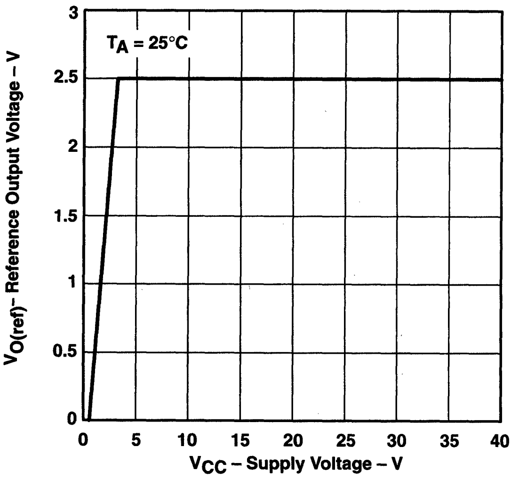


Figure 9

DROPOUT VOLTAGE VARIATION vs FREE-TEMPERATURE

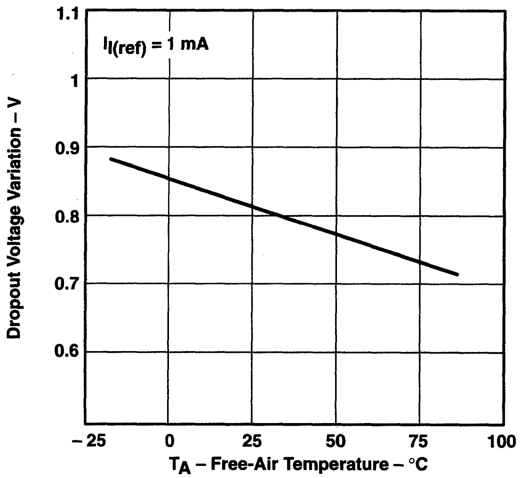


Figure 10

TYPICAL CHARACTERISTICS

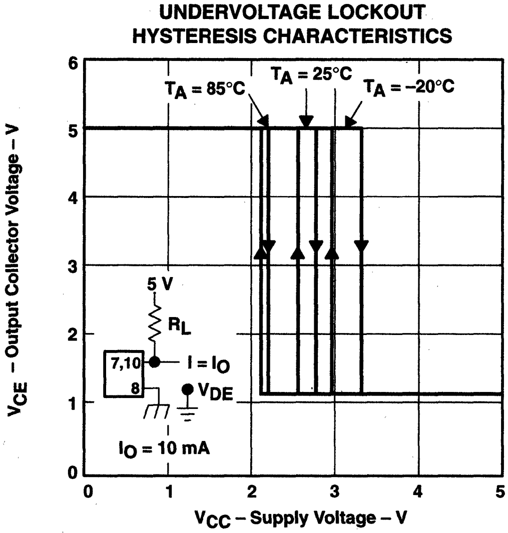


Figure 11

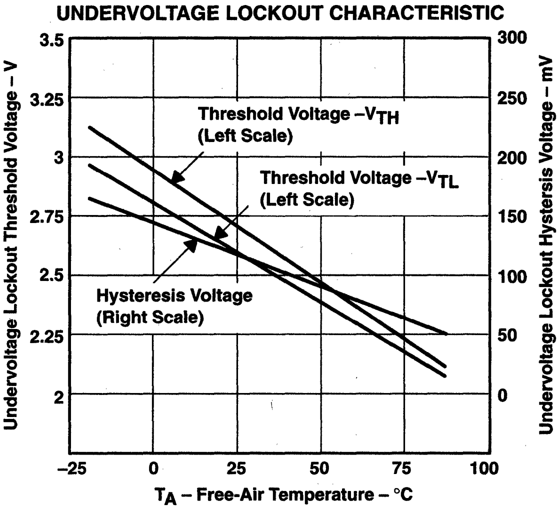


Figure 12

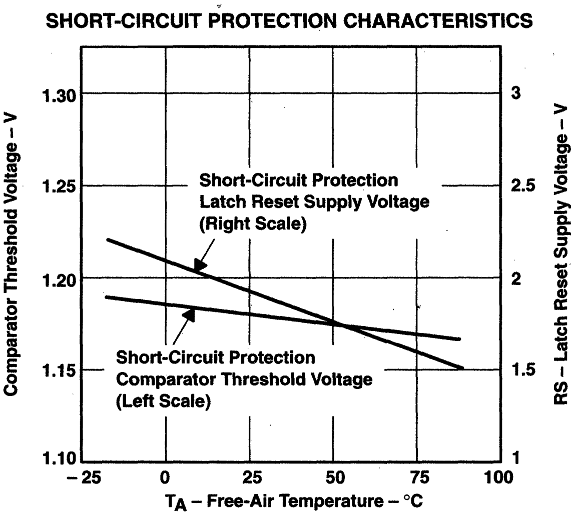
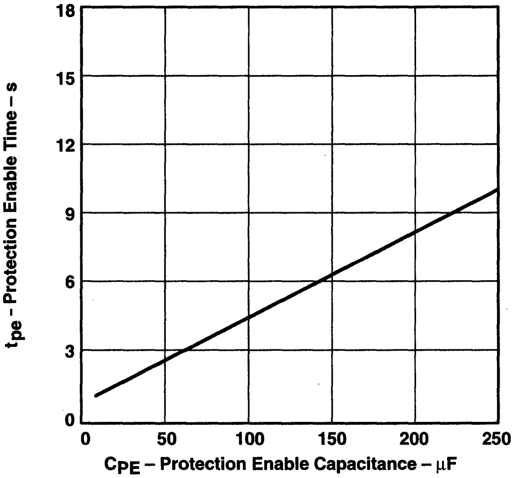


Figure 13

TYPICAL CHARACTERISTICS

PROTECTION ENABLE TIME
vs
PROTECTION ENABLE CAPACITANCE



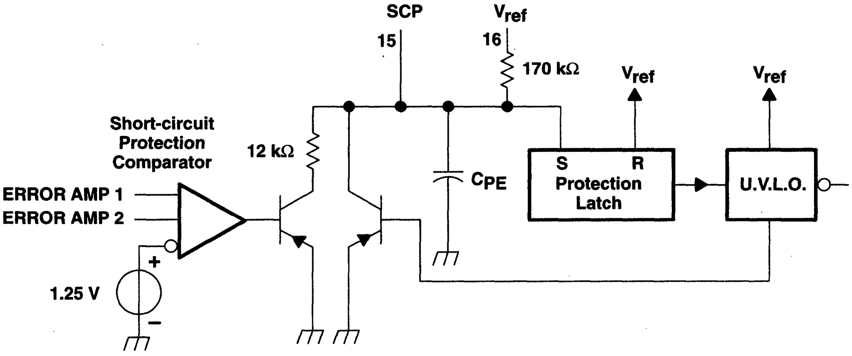


Figure 14

TYPICAL CHARACTERISTICS

ERROR AMP MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

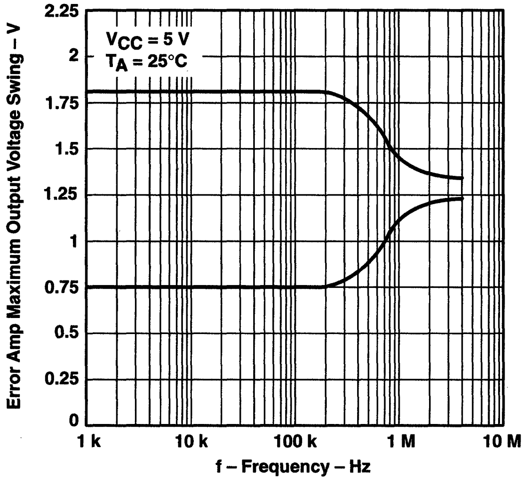


Figure 15

OPEN-LOOP VOLTAGE AMPLIFICATION vs FREQUENCY

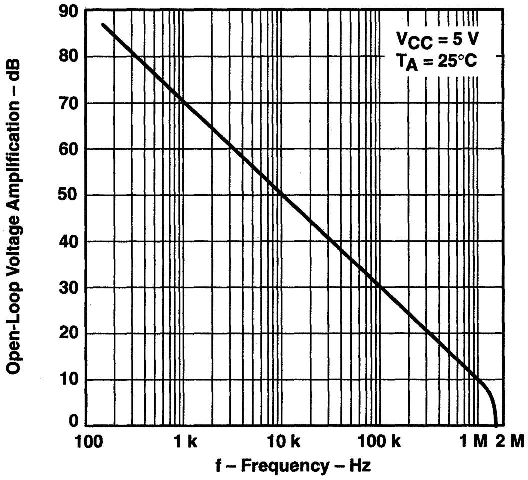


Figure 16

GAIN (AMPLIFIER IN UNITY-GAIN CONFIGURATION) vs FREQUENCY

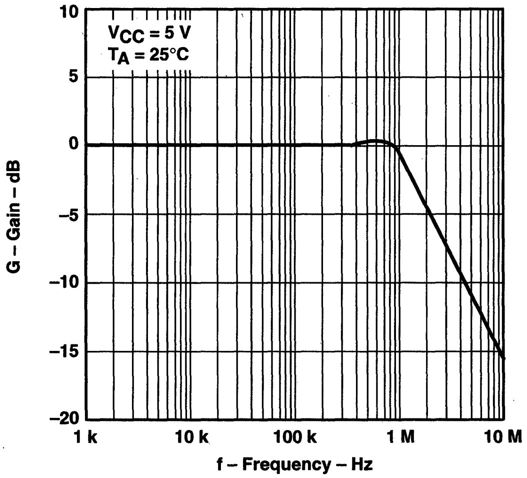
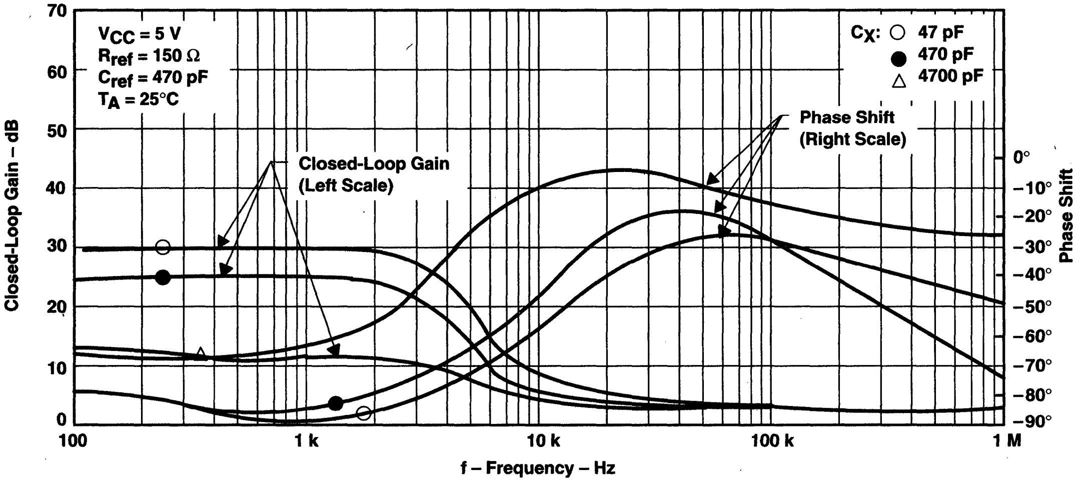
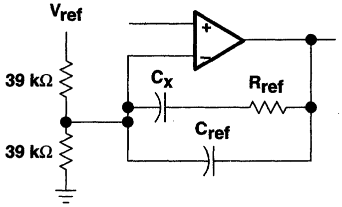


Figure 17

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



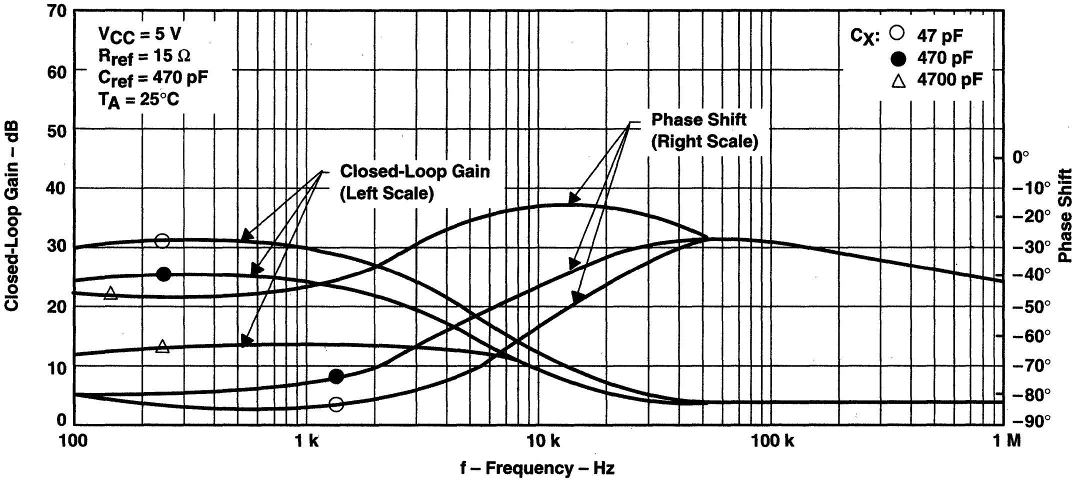


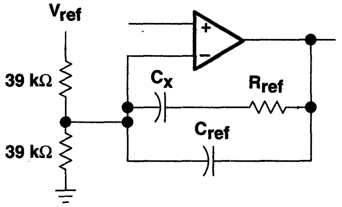
Test Circuit

Figure 18

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



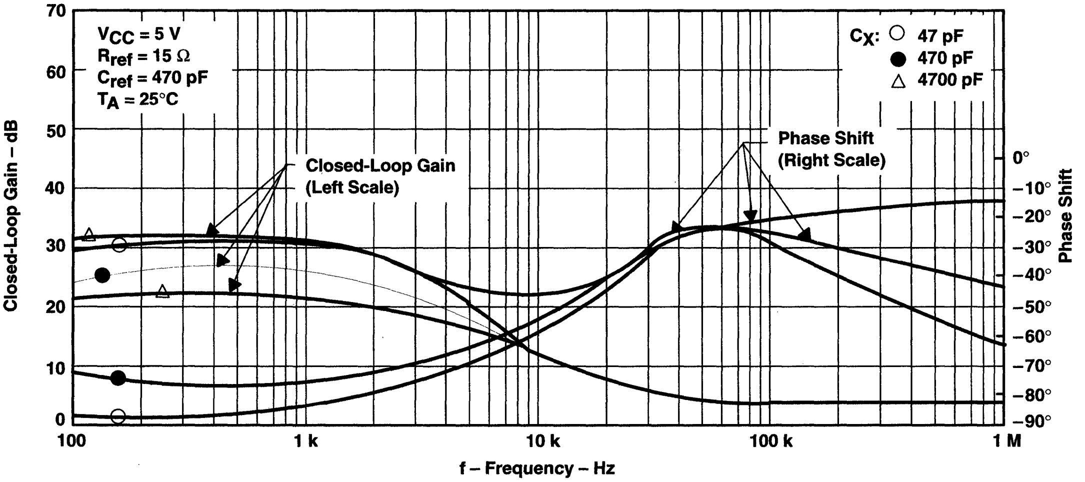


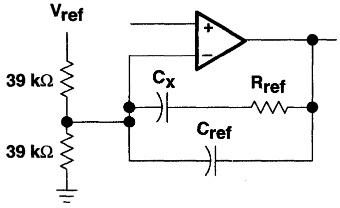
Test Circuit

Figure 19

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



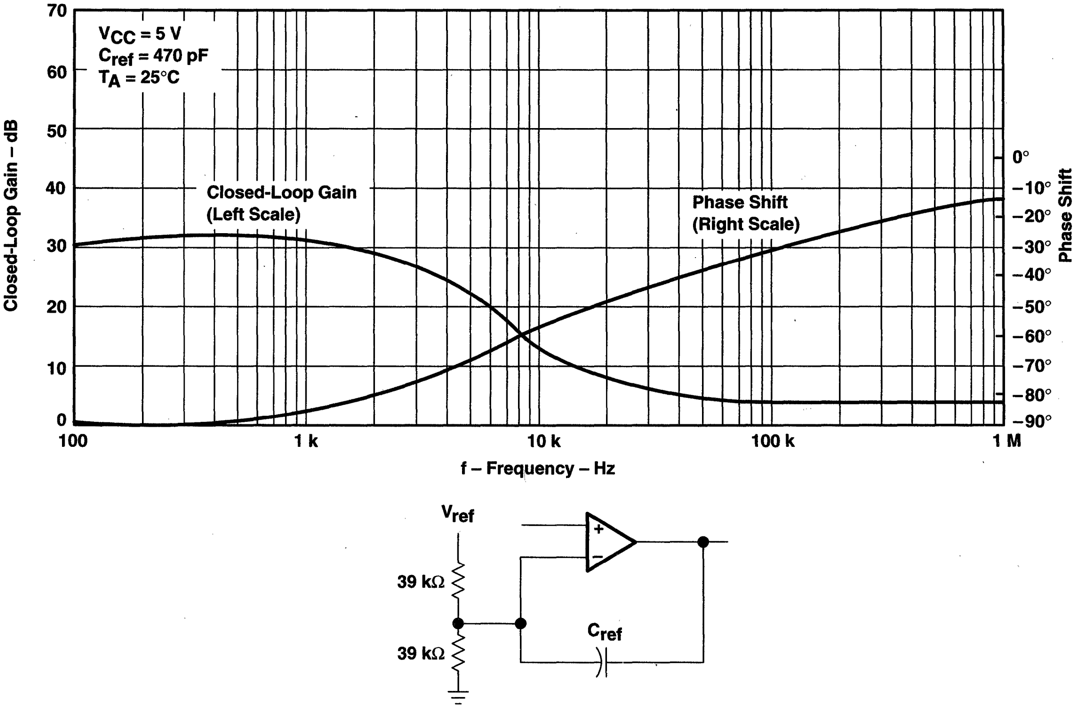


Test Circuit

Figure 20

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



Test Circuit

Figure 21

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT vs COLLECTOR OUTPUT SATURATION VOLTAGE

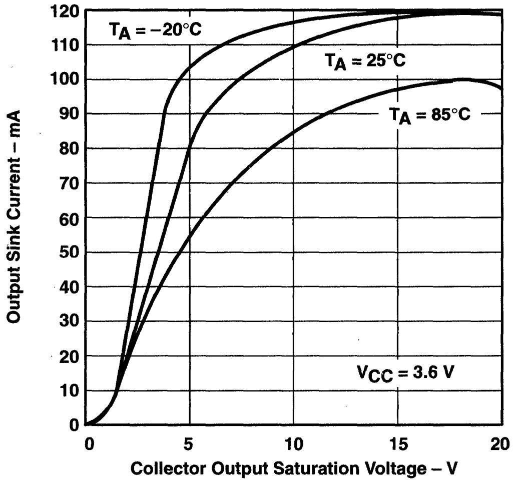
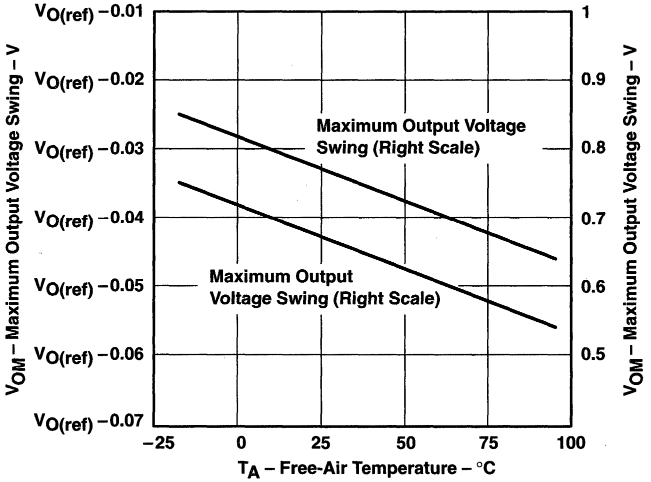
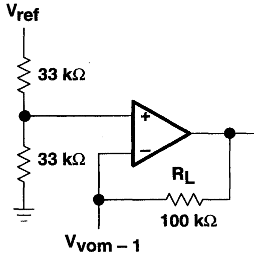


Figure 22

MAXIMUM OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE





$V_{CC} = 3.6$ V
$R_L = 100$ kΩ
$V_{OM+1} = 1.25$ V
$V_{OM-1} = 1.15$ V (Right Scale)
$V_{OM-1} = 1.35$ V (Left Scale)

TEST CIRCUIT

Figure 23

TYPICAL CHARACTERISTICS

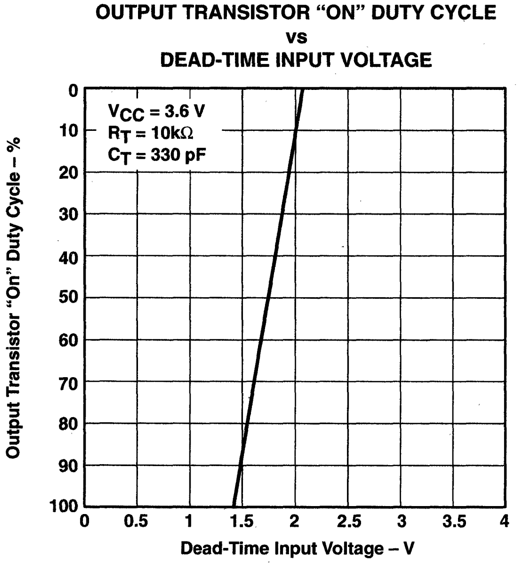


Figure 24

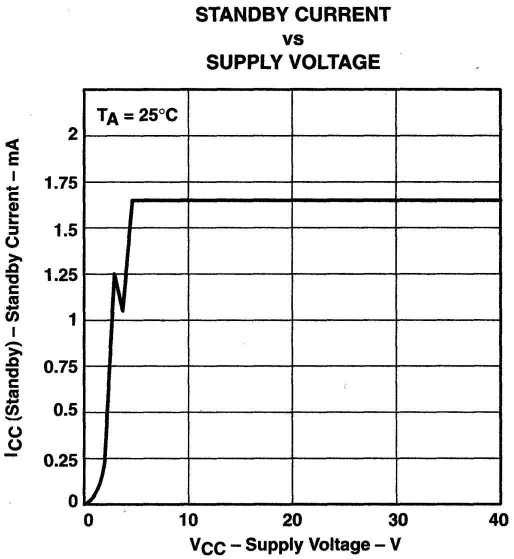


Figure 25

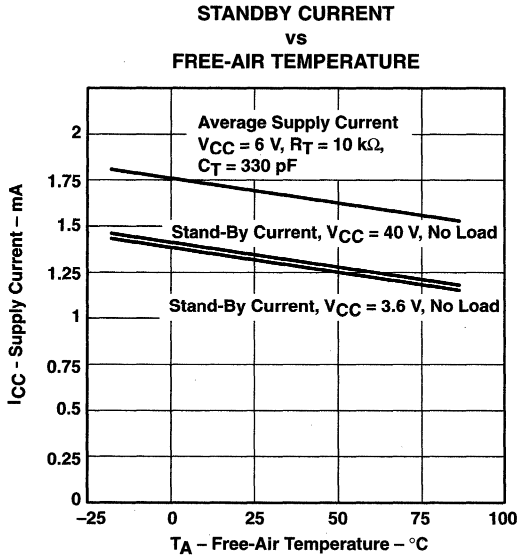


Figure 26

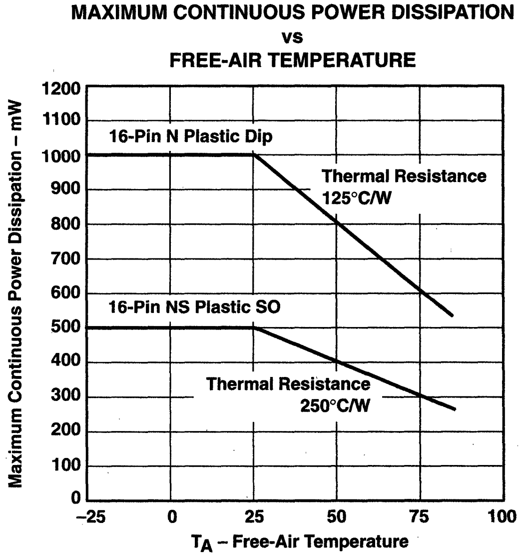
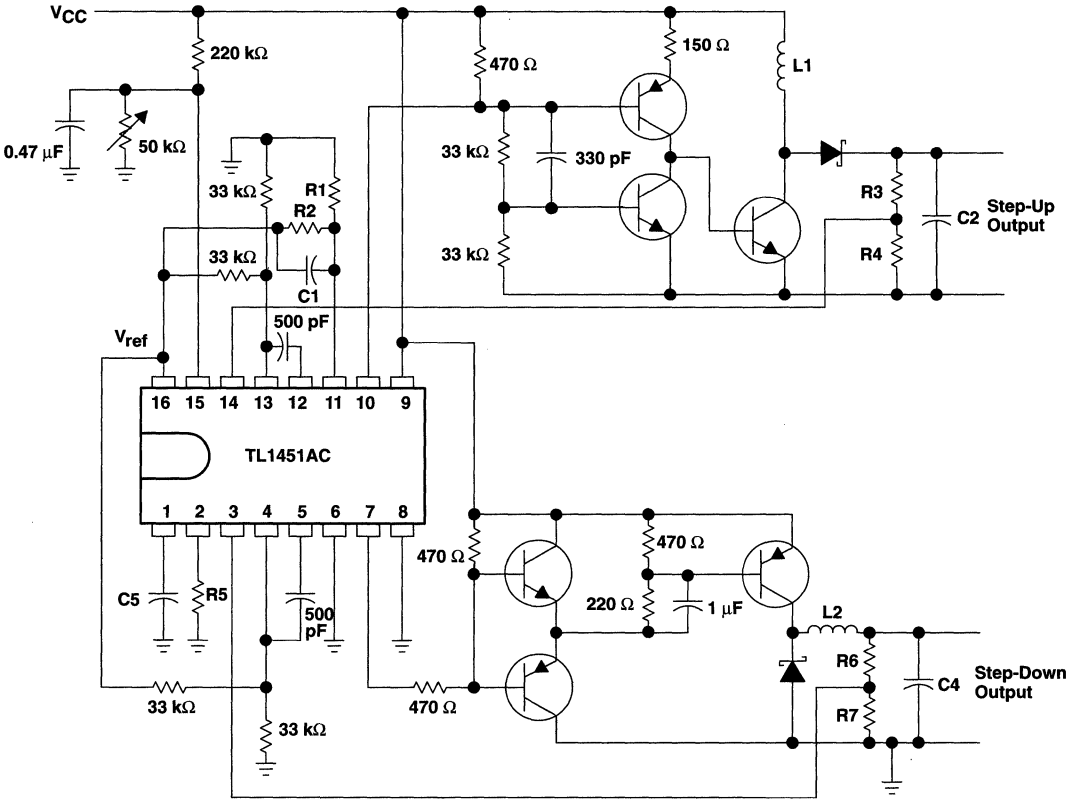


Figure 27

APPLICATION INFORMATION



NOTE A. Values for R1 through R7, C1 through C4, and L1 and L2 depend upon individual application.

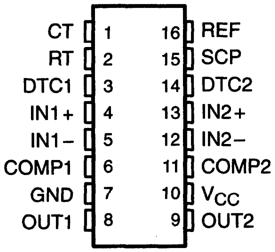
Figure 28. High-Speed Dual Switching Regulator

TL1454, TL1454Y
DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUITS

SLVS086A – APRIL 1995 – REVISED OCTOBER 1995

- **Two Complete PWM Control Circuits**
- **Outputs Drive MOSFETs Directly**
- **Oscillator Frequency . . . 50 kHz to 2 MHz**
- **3.6-V to 20-V Supply-Voltage Range**
- **Low Supply Current . . . 3.5 mA Typ**
- **Adjustable Dead-Time Control, 0% to 100%**
- **1.25-V Reference**

D, N OR PW PACKAGE
(TOP VIEW)



description

The TL1454 is a dual-channel pulse-width-modulation (PWM) control circuit, primarily intended for low-power, dc/dc converters. Applications include LCD displays, backlight inverters, notebook computers, and other products requiring small, high-frequency, dc/dc converters. Each PWM channel has its own error amplifier, PWM comparator, dead-time control comparator, and MOSFET driver. The voltage reference, oscillator, undervoltage lockout, and short-circuit protection are common to both channels.

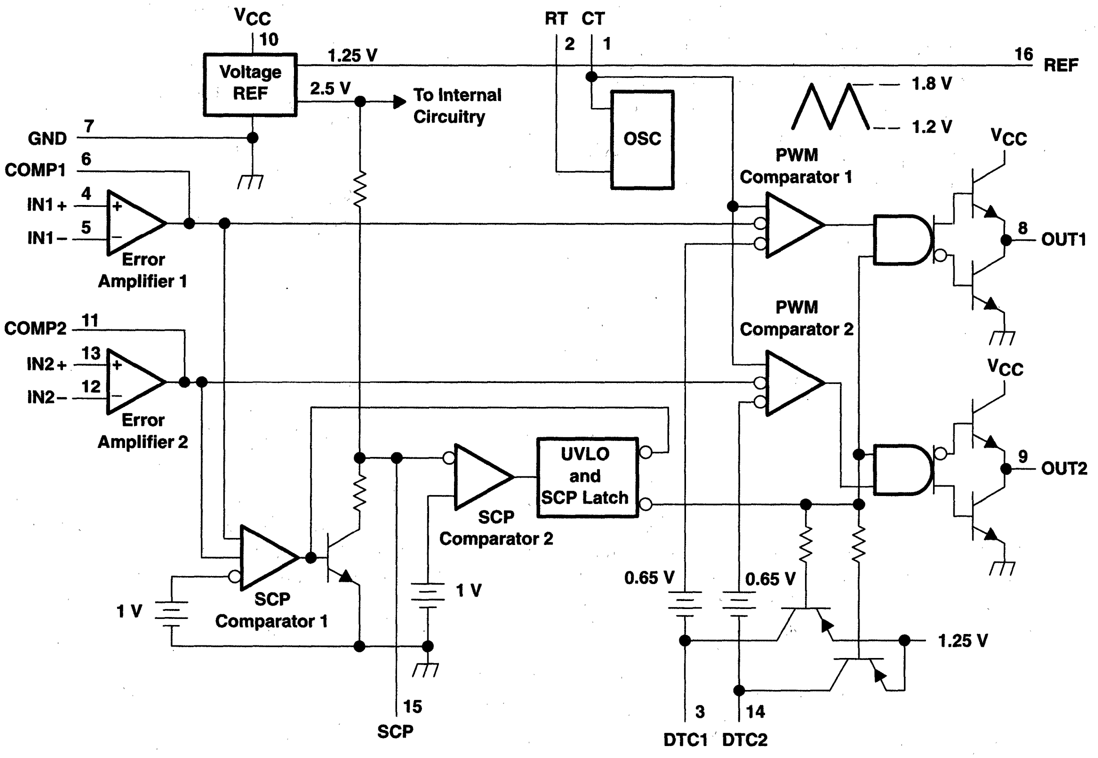
Channel 1 is configured to drive n-channel MOSFETs in step-up or flyback converters, and channel 2 is configured to drive p-channel MOSFETs in step-down or inverting converters. The operating frequency is set with an external resistor and an external capacitor, and dead time is continuously adjustable from 0 to 100% duty cycle with a resistive divider network. Soft start can be implemented by adding a capacitor to the dead-time control (DTC) network. The error-amplifier common-mode input range includes ground, which allows the TL1454 to be used in ground-sensing battery chargers as well as voltage converters.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES†			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
−20°C to 85°C	TL1454CD	TL1454CN	TL1454CPWLE	TL1454Y
−40°C to 85°C	TL1454ID	TL1454IN	—	—

† The D package is available taped and reeled. Add the suffix R to the device name (e.g., TL1454CDR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TL1454CPWLE).

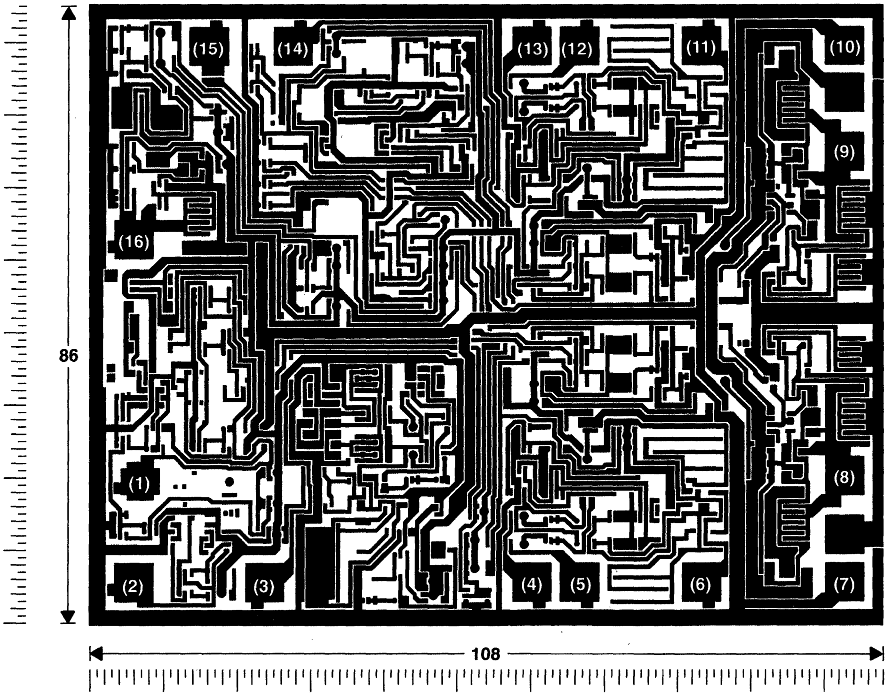
functional block diagram

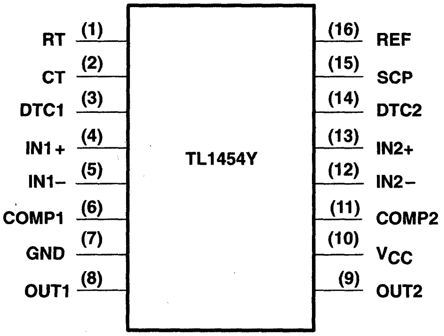


TL1454Y chip information

This chip, when properly assembled, displays characteristics similar to the TL1454C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

theory of operation

reference voltage

A linear regulator operating from V_{CC} generates a 2.5-V supply for the internal circuits and the 1.25-V reference, which can source a maximum of 1 mA for external loads. A small ceramic capacitor (0.047 µF to 0.1 µF) between REF and ground is recommended to minimize noise pickup.

error amplifier

The error amplifier generates the error signal used by the PWM to adjust the power-switch duty cycle for the desired converter output voltage. The signal is generated by comparing a sample of the output voltage to the voltage reference and amplifying the difference. An external resistive divider connected between the converter output and ground, as shown in Figure 1, is generally required to obtain the output voltage sample.

The amplifier output is brought out on COMP to allow the frequency response of the amplifier to be shaped with an external RC network to stabilize the feedback loop of the converter. DC loading on the COMP output is limited to 45 µA (the maximum amplifier source current capability).

Figure 1 illustrates the sense-divider network and error-amplifier connections for converters with positive output voltages. The divider network is connected to the noninverting amplifier input because the PWM has a phase inversion; the duty cycle decreases as the error-amplifier output increases.

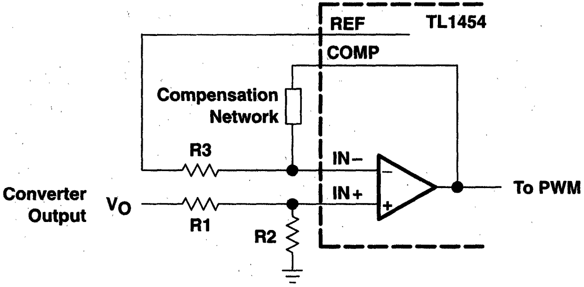


Figure 1. Sense Divider/Error Amplifier Configuration for Converters with Positive Outputs

The output voltage is given by:

$$V_O = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

where $V_{ref} = 1.25$ V.

The dc source resistance of the error-amplifier inputs should be 10 kΩ or less and approximately matched to minimize output voltage errors caused by the input-bias current. A simple procedure for determining appropriate values for the resistors is to choose a convenient value for R3 (10 kΩ or less) and calculate R1 and R2 using:

$$R_1 = \frac{R_3 V_O}{V_O - V_{ref}}$$

$$R_2 = \frac{R_3 V_O}{V_{ref}}$$

error amplifier

R1 and R2 should be tight-tolerance (±1% or better) devices with low and/or matched temperature coefficients to minimize output voltage errors. A device with a ±5% tolerance is suitable for R3.

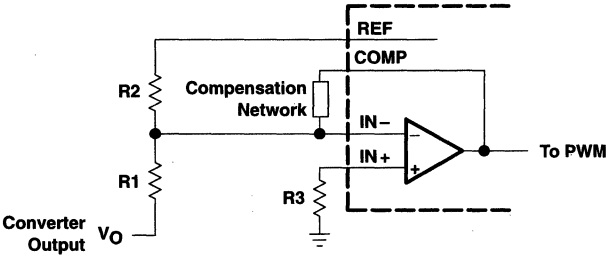


Figure 2. Sense Divider/Error Amplifier Configuration for Converters with Negative Outputs

Figure 2 shows the divider network and error-amplifier configuration for negative output voltages. In general, the comments for positive output voltages also apply for negative outputs. The output voltage is given by:

$$V_O = -\frac{R_1 V_{ref}}{R_2}$$

The design procedure for choosing the resistor value is to select a convenient value for R2 (instead of R3 in the procedure for positive outputs) and calculate R1 and R3 using:

$$R_1 = -\frac{R_2 V_O}{V_{ref}}$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

Values in the 10-kΩ to 20-kΩ range work well for R2. R3 can be omitted and the noninverting amplifier connected to ground in applications where the output voltage tolerance is not critical.

oscillator

The oscillator frequency can be set between 50 kHz and 2 MHz with a resistor connected between RT and GND and a capacitor between CT and GND (see Figure 3). Figure 6 is used to determine R_T and C_T for the desired operating frequency. Both components should be tight-tolerance, temperature-stable devices to minimize frequency deviation. A 1% metal-film resistor is recommended for R_T, and a 10%, or better, NPO ceramic capacitor is recommended for C_T.

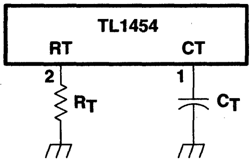


Figure 3. Oscillator Timing

dead-time control (DTC) and soft start

The two PWM channels have independent dead-time control inputs so that the maximum power-switch duty cycles can be limited to less then 100%. The dead-time is set with a voltage applied to DTC; the voltage is typically obtained from a resistive divider connected between the reference and ground as shown in Figure 4. Soft start is implemented by adding a capacitor between REF and DTC.

The voltage, V_{DT}, required to limit the duty cycle to a maximum value is given by

$$V_{DT} = V_{O(max)} - D\left(V_{O(max)} - V_{O(min)}\right) - 0.65$$

where $V_{O(max)}$ and $V_{O(min)}$ are obtained from Figure 9, and D is the maximum duty cycle.

Predicting the regulator startup or rise time is complicated because it depends on many variables, including: input voltage, output voltage, filter values, converter topology, and operating frequency. In general, the output will be in regulation within two time constants of the soft-start circuit. A five-to-ten millisecond time constant usually works well for low-power converters.

The DTC input can be grounded in applications where achieving a 100% duty cycle is desirable, such as a buck converter with a very low input-to-output differential voltge. However, grounding DTC prevents the inplementation of soft start, and the output voltage overshoot at power-on is likely to be very large. A better arrangement is to omit R_{DT1} (see Figure 4) and choose R_{DT2} = 47 kΩ. This configuration ensures that the duty cycle can reach 100% and still allows the designer to implement soft start using C_{SS}.

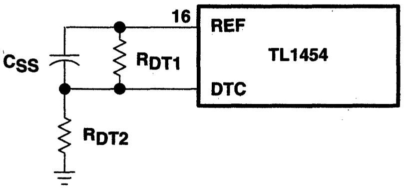


Figure 4. Dead-Time Control and Soft Start

PWM comparator

Each of the PWM comparators has dual inverting inputs. One inverting input is connected to the output of the error amplifier; the other inverting input is connected to the DTC terminal. Under normal operating conditions, when either the error-amplifier output or the dead-time control voltage is higher than that for the PWM triangle wave, the output stage is set inactive (OUT1 low and OUT2 high), turning the external power stage off.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output circuit off and resets the SCP latch whenever the supply voltage drops too low (to approximately 2.9 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL1454 SCP function prevents damage to the power switches when the converter output is shorted to ground. In normal operation, SCP comparator 1 clamps SCP to approximately 185 mV. When one of the converter outputs is shorted, the error amplifier output (COMP) will be driven below 1 V to maximize duty cycle and force the converter output back up. When the error amplifier output drops below 1 V, SCP comparator 1 releases SCP, and capacitor, C_{SCP}, which is connected between SCP and GND, begins charging. If the error-amplifier output rises above 1 V before C_{SCP} is charged to 1 V, SCP comparator 1 discharges C_{SCP} and normal operation resumes. If C_{SCP} reaches 1 V, SCP comparator 2 turns on and sets the SCP latch, which turns off the output drives and resets the soft-start circuit. The latch remains set until the supply voltage is lowered to 2 V or less, or C_{SCP} is discharged externally.

short-circuit protection (SCP) (continued)

The SCP time-out period must be greater than the converter start-up time or the converter will not start. Because high-value capacitor tolerances tend to be ±20% or more and IC resistor tolerances are loose as well, it is best to choose an SCP time-out period ten-to-fifteen times greater than the converter startup time. The value of C_{SCP} may be determined using Figure 6, or it can be calculated using:

$$C_{SCP} = \frac{T_{SCP}}{80.3}$$

where C_{SCP} is in µF and T_{SCP} is the time-out period in ms.

output stage

The output stage of the TL1454 is a totem-pole output with a maximum source/sink current rating of 40 mA and a voltage rating of 20 V. The output is controlled by a complementary output AND gate and is turned on (sourcing current for OUT1, sinking current for OUT2) when all the following conditions are met: 1) the oscillator triangle wave voltage is higher than both the DTC voltage and the error-amplifier output voltage, 2) the undervoltage-lockout circuit is inactive, and 3) the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	23 V
Error amplifier input voltage: IN1+, IN1–, IN2+, IN2–	23 V
Output voltage: OUT1, OUT2	20 V
Continuous output current: OUT1, OUT2	±200 mA
Peak output current: OUT1, OUT2	1 A
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	–20°C to 85°C
I suffix	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW
PW	500 mW	4.0 mW/°C	320 mW	260 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	20	V
Error amplifier common-mode input voltage		–0.2	1.45	V
Output voltage, V_O			20	V
Output current, I_O			±40	mA
COMP source current			–45	µA
COMP sink current			100	µA
Reference output current			1	mA
COMP dc load resistance		100		kΩ
Timing capacitor, C_T		10	4000	pF
Timing resistor, R_T		5.1	100	kΩ
Oscillator frequency		50	2000	kHz
Operating free-air temperature, T_A	TL1454C	–20	85	°C
	TL1454I	–40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 500 kHz (unless otherwise noted)

reference

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{ref}	Output voltage, REF	I_O = 1 mA, T_A = 25°C	1.23	1.25	1.28	V
		I_O = 1 mA	1.2		1.31	
	Input regulation	V_{OC} = 3.6 V to 20 V, I_O = 1 mA		2	6	mV
	Output regulation	I_O = 0.1 mA to 1 mA		1	7.5	mV
	Output voltage change with temperature	$T_A = T_{A(min)}$ to 25°C, I_O = 1 mA	–12.5	–1.25	12.5	mV
		T_A = 25°C to 85°C, I_O = 1 mA	–12.5	–2.5	12.5	
I_{OS}	Short-circuit output current	V_{ref} = 0 V		30		mA

undervoltage lockout (UVLO)

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{IT+}	Positive-going threshold voltage	T_A = 25°C		2.9		V
V_{IT-}	Negative-going threshold voltage			2.7		V
V_{hys}	Hysteresis, $V_{IT+} - V_{IT-}$		100	200		mV

short-circuit protection (SCP)

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{IT}	Input threshold voltage	T_A = 25°C	0.95	1	1.05	V
V_{stby}†	Standby voltage	No pullup	140	185	230	mV
$V_{I(latched)}$	Latched-mode input voltage			60	120	mV
$V_{IT(COMP)}$	Comparator threshold voltage	COMP1, COMP2		1		V
	Input source current	T_A = 25°C, $V_{O(SCP)}$ = 0	–5	–15	–20	μA

† This symbol is not presently listed within EIA/JEDEC standards for semiconductor symbology.

oscillator

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
f_{osc}	Frequency	C_T = 120 pF, R_T = 10 kΩ		500		kHz
	Standard deviation of frequency			50		kHz
	Frequency change with voltage	V_{CC} = 3.6 V to 20 V, T_A = 25°C		5		kHz
	Frequency change with temperature	$T_A = T_{A(min)}$ to 25°C		–2	±20	kHz
		T_A = 25°C to 85°C		–10	±20	
	Maximum ramp voltage			1.8		V
	Minimum ramp voltage			1.1		V

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 500 kHz (unless otherwise noted) (continued)

dead-time control (DTC)

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{IT}	Input threshold voltage	Duty cycle = 0%	1	1.1	1.2	V
		Duty cycle = 100%	0.4	0.5	0.6	
$V_{I(latched)}$	Latched-mode input voltage			1.2		V
I_{IB}	Common-mode input bias current	DTC1, IN1+ ≈ 1.2 V			4	µA
	Latched-mode (source) current	T_A = 25°C		−100		µA

error-amplifier

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.25 V, V_{IC} = 1.25 V			6	mV
I_{IO}	Input offset current				100	nA
I_{IB}	Input bias current			−160	−500	nA
V_{ICR}	Input voltage range	V_{CC} = 3.6 V to 20 V	−0.2 to 1.45			V
A_V	Open-loop voltage gain	R_{FB} = 200 kΩ	70	80		dB
	Unity-gain bandwidth			3		MHz
CMRR	Common-mode rejection ratio		60	80		dB
$V_{OM(max)}$	Positive output voltage swing		2.3	2.43		V
$V_{OM(min)}$	Negative output voltage swing			0.63	0.8	
I_{O+}	Output sink current	V_{ID} = −0.1 V, V_O = 1.20 V	0.1	0.5		mA
I_{O-}	Output source current	V_{ID} = 0.1 V, V_O = 1.80 V	−45	−70		µA

output

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_O = −8 mA	V_{CC}–2	4.5		V
		I_O = −40 mA	V_{CC}–2	4.4		
V_{OL}	Low-level output voltage	I_O = 8 mA		0.1	0.4	V
		I_O = 40 mA		1.8	2.5	
t_{rv}	Output voltage rise time	C_L = 2000 pF, T_A = 25°C		220		ns
t_{fv}	Output voltage fall time			220		

supply current

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$I_{CC(stdby)}$	Standby supply current	RT open, CT = 1.5 V, V_O (COMP1, COMP2) = 1.25 V, No load		3.1	6	mA
$I_{CC(average)}$	Average supply current	R_T = 10 kΩ, C_T = 120 pF, 50% duty cycle, Outputs open		3.5	7	mA

electrical characteristics, V_{CC} = 6 V, f_{osc} = 500 kHz, T_A = 25°C (unless otherwise noted)

reference

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
V_{ref}	Output voltage, REF	I_O = 1 mA,		1.25		V
	Input regulation	V_{OC} = 3.6 V to 20 V, I_O = 1 mA		2		mV
	Output regulation	I_O = 0.1 mA to 1 mA		1		mV
	Output voltage change with temperature	I_O = 1 mA		−1.25		mV
		I_O = 1 mA		−2.5		
I_{OS}	Short-circuit output current	V_{ref} = 0 V		30		mA

undervoltage lockout (UVLO)

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
V_{IT+}	Positive-going threshold voltage			2.9		V
V_{IT-}	Negative-going threshold voltage			2.7		V
V_{hys}	Hysteresis, $V_{IT+} - V_{IT-}$			200		mV

short-circuit protection (SCP)

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
V_{IT}	Input threshold voltage			1		V
V_{stby}†	Standby voltage	No pullup		185		mV
$V_{I(latched)}$	Latched-mode input voltage			60		mV
$V_{IT(COMP)}$	Comparator threshold voltage	COMP1, COMP2		1		V
	Input source current	$V_{O(SCP)}$ = 0		−15		μA

† This symbol is not presently listed within EIA/JEDEC standards for semiconductor symbology.

oscillator

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
f_{osc}	Frequency	C_T = 120 pF, R_T = 10 kΩ		500		kHz
	Standard deviation of frequency			50		kHz
	Frequency change with voltage	V_{CC} = 3.6 V to 20 V		5		kHz
	Frequency change with temperature			−2		kHz
				−10		
	Maximum ramp voltage			1.8		V
	Minimum ramp voltage			1.1		V

electrical characteristics, V_{CC} = 6 V, f_{osc} = 500 kHz, T_A = 25°C (unless otherwise noted) (continued)

dead-time control (DTC)

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
V_{IT}	Input threshold voltage	Duty cycle = 0%		1.1		V
		Duty cycle = 100%		0.5		
$V_{I(latched)}$	Latched-mode input voltage			1.2		V
	Latched-mode (source) current			−100		µA

error-amplifier

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
I_{IB}	Input bias current	V_O = 1.25 V, V_{IC} = 1.25 V		−160		nA
A_V	Open-loop voltage gain	R_{FB} = 200 kΩ		80		dB
	Unity-gain bandwidth			3		MHz
CMRR	Common-mode rejection ratio			80		dB
$V_{OM(max)}$	Positive output voltage swing			2.43		V
$V_{OM(min)}$	Negative output voltage swing			0.63		
I_{O+}	Output sink current	V_{ID} = −0.1 V, V_O = 1.20 V		0.5		mA
I_{O-}	Output source current	V_{ID} = 0.1 V, V_O = 1.80 V		−70		µA

output

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_O = −8 mA		4.5		V
		I_O = −40 mA		4.4		
V_{OL}	Low-level output voltage	I_O = 8 mA		0.1		V
		I_O = 40 mA		1.8		
t_{rv}	Output voltage rise time	C_L = 2000 pF		220		ns
t_{fv}	Output voltage fall time			220		

supply current

PARAMETER		TEST CONDITIONS	TL1454Y			UNIT
			MIN	TYP	MAX	
$I_{CC(stdby)}$	Standby supply current	RT open, CT = 1.5 V, V_O (COMP1, COMP2) = 1.25 V, No load		3.1		mA
$I_{CC(average)}$	Average supply current	R_T = 10 kΩ, C_T = 120 pF, 50% duty cycle, Outputs open		3.5		mA

PARAMETER MEASUREMENT INFORMATION

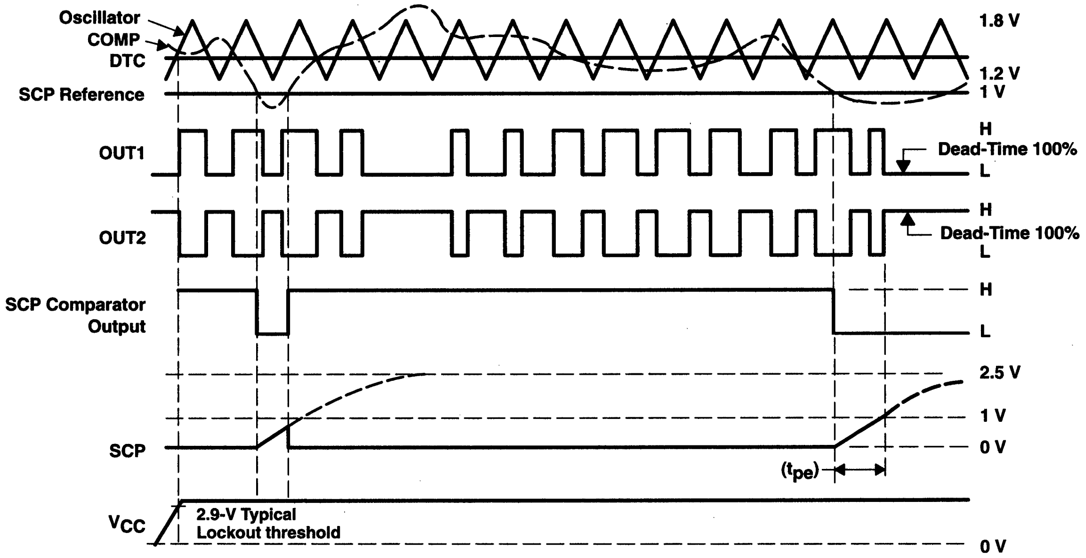


Figure 5. Timing Diagram

TYPICAL CHARACTERISTICS

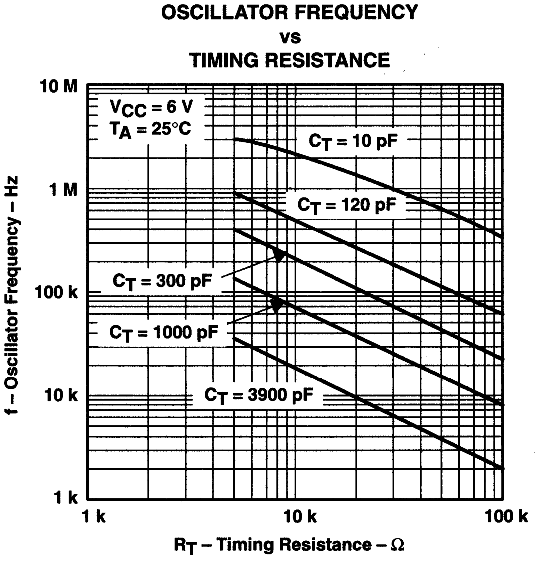


Figure 6

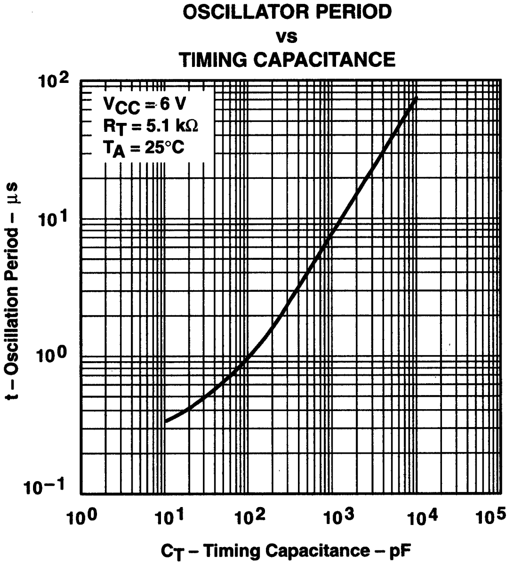


Figure 7

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

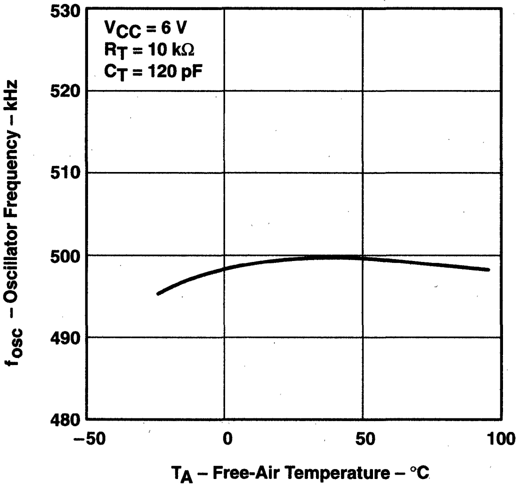


Figure 8

PWM TRIANGLE WAVEFORM AMPLITUDE
vs
TIMING CAPACITANCE

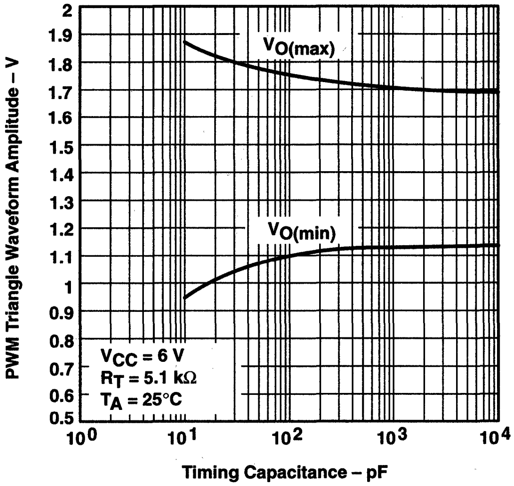


Figure 9

DTC INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

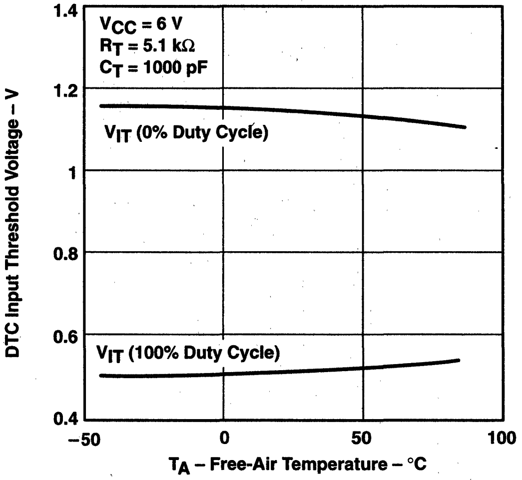


Figure 10

SCP TIME-OUT PERIOD
vs
SCP CAPACITANCE

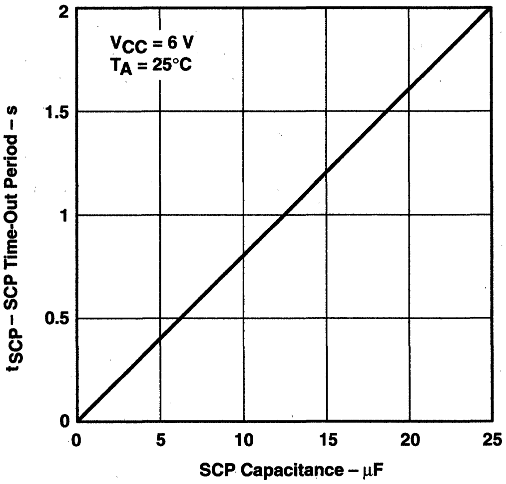


Figure 11

TYPICAL CHARACTERISTICS

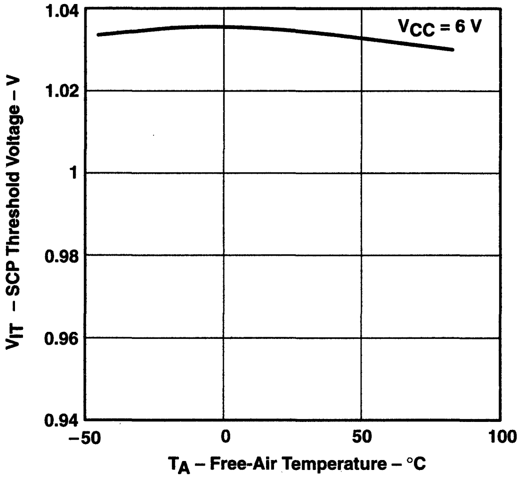

SCP THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 12

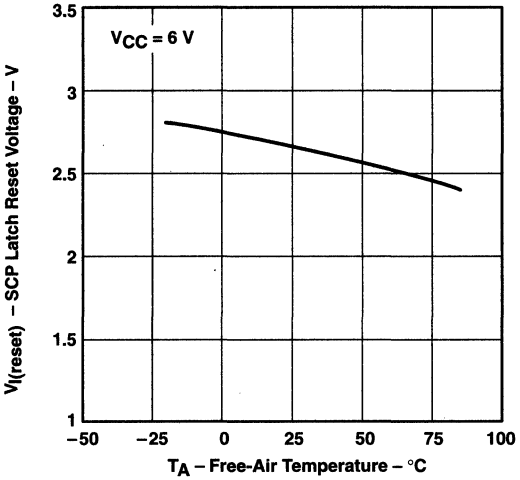

SCP LATCH RESET VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 13

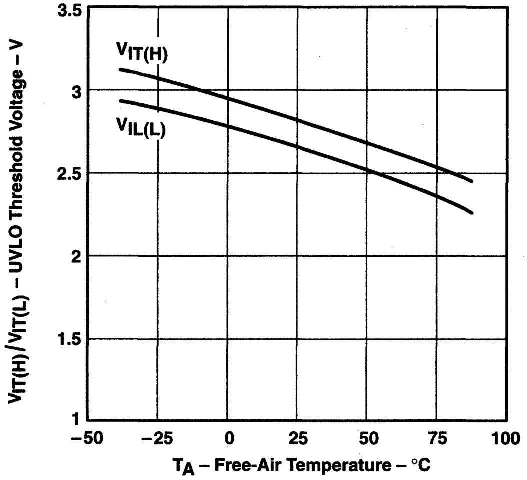

UVLO THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 14

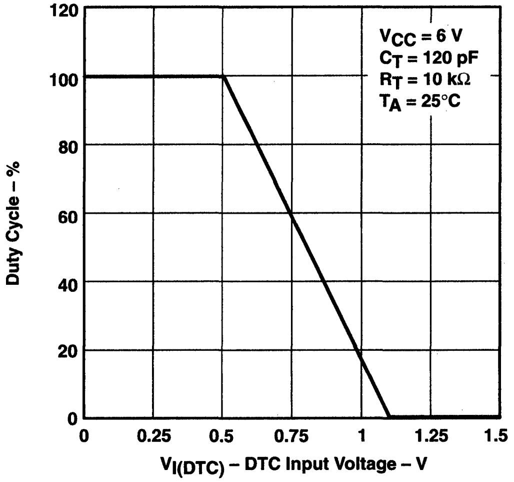

DUTY CYCLE
vs
DTC INPUT VOLTAGE

Figure 15

TYPICAL CHARACTERISTICS

ERROR-AMPLIFIER MAXIMUM OUTPUT VOLTAGE vs SOURCE CURRENT

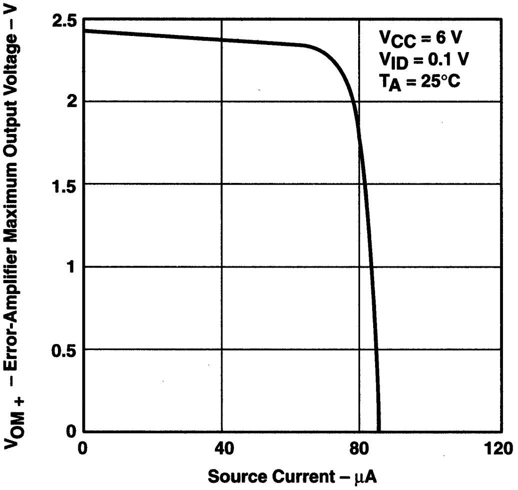


Figure 16

ERROR-AMPLIFIER MINIMUM OUTPUT VOLTAGE vs SINK CURRENT

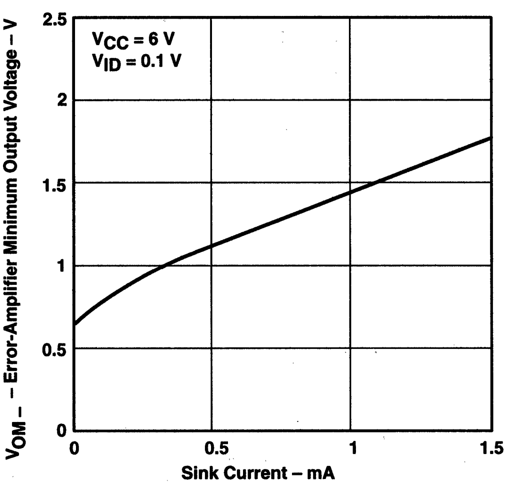


Figure 17

ERROR AMPLIFIER MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREQUENCY

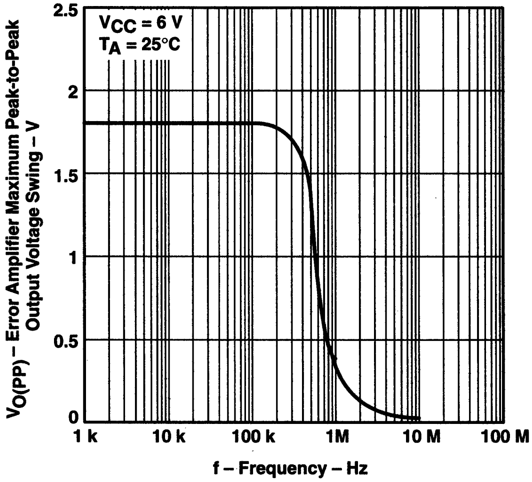


Figure 18

ERROR-AMPLIFIER MINIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

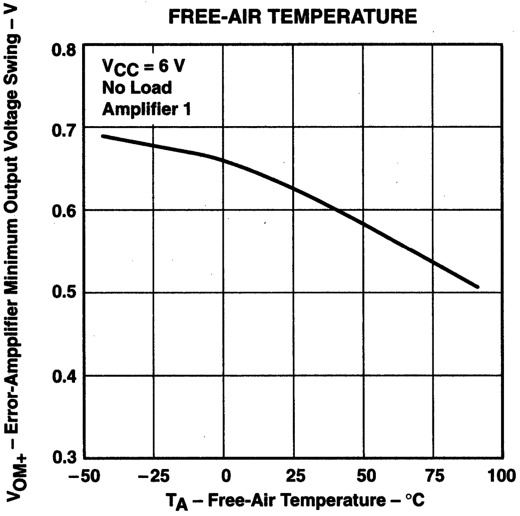


Figure 19

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY

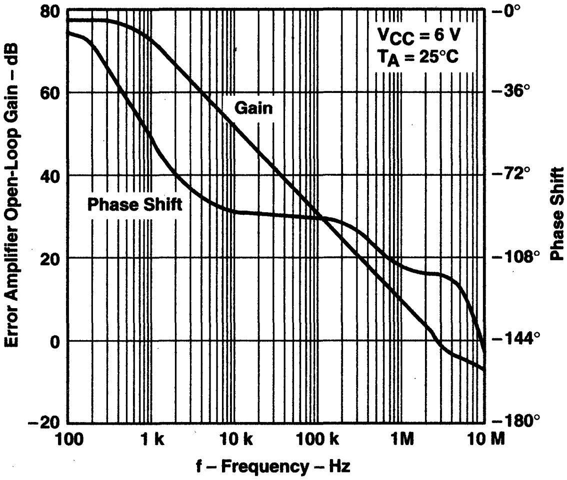


Figure 20

ERROR-AMPLIFIER POSITIVE OUTPUT VOLTAGE SWING vs FREQUENCY FREE-AIR TEMPERATURE

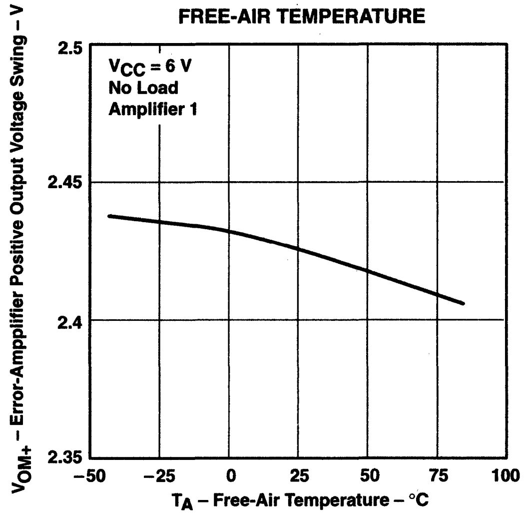


Figure 21

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

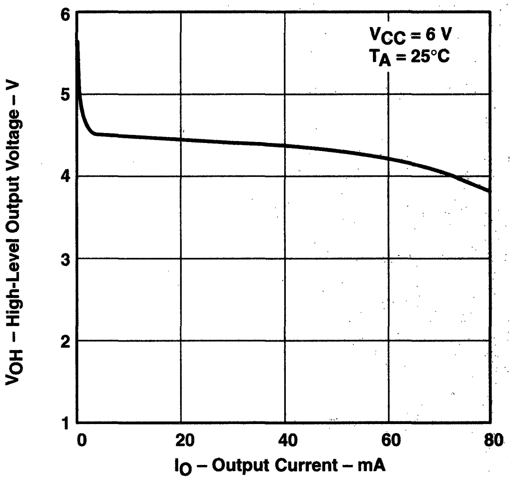


Figure 22

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

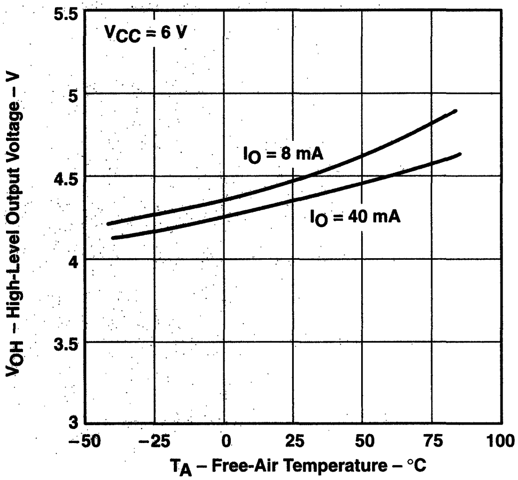


Figure 23

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

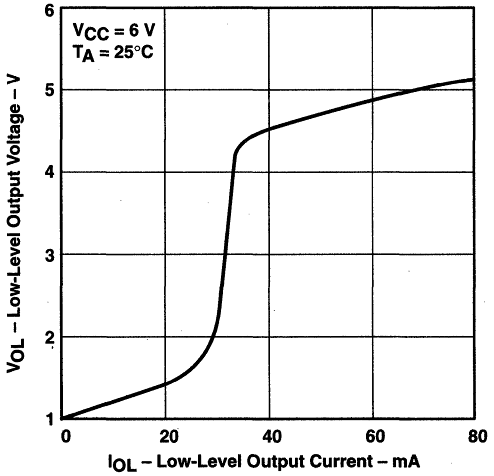


Figure 24

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

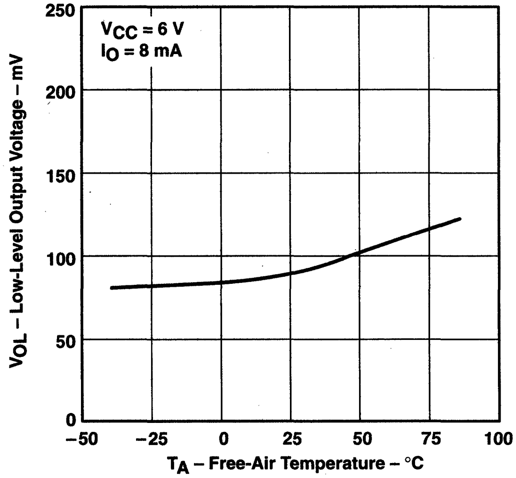


Figure 25

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

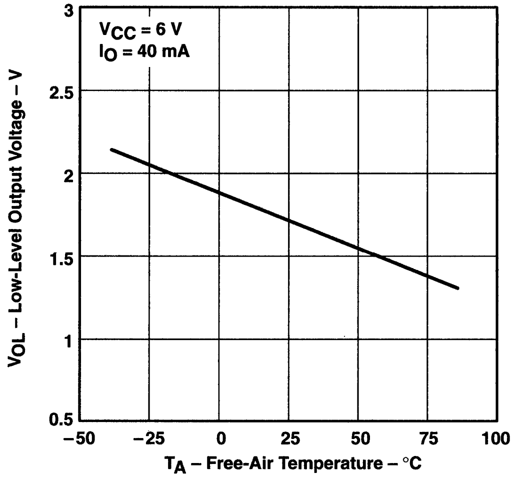


Figure 26

AVERAGE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

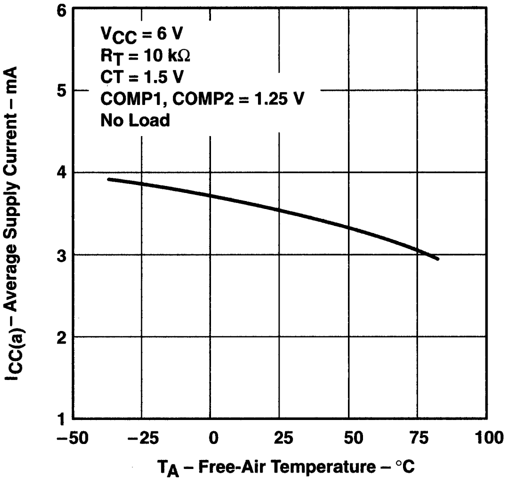


Figure 27

STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE

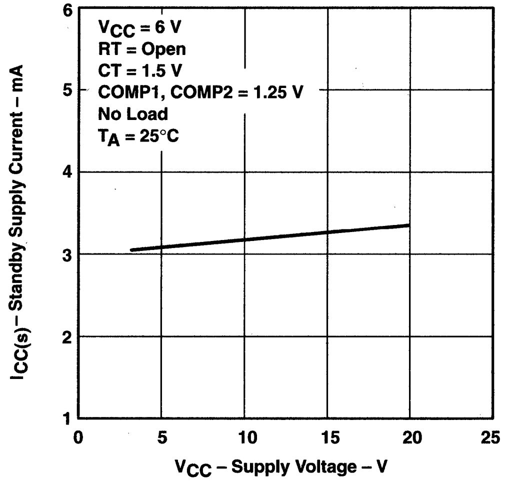


Figure 28

STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE

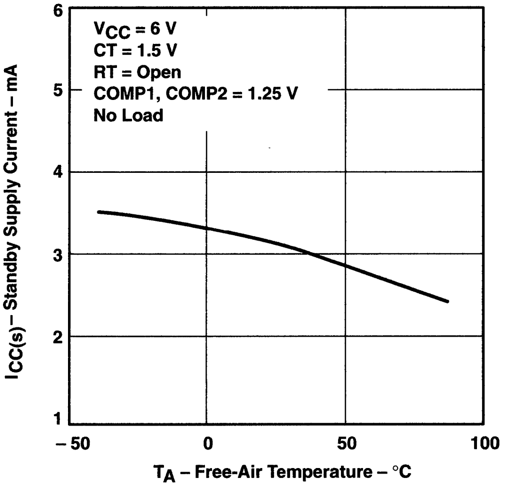


Figure 29

TYPICAL CHARACTERISTICS

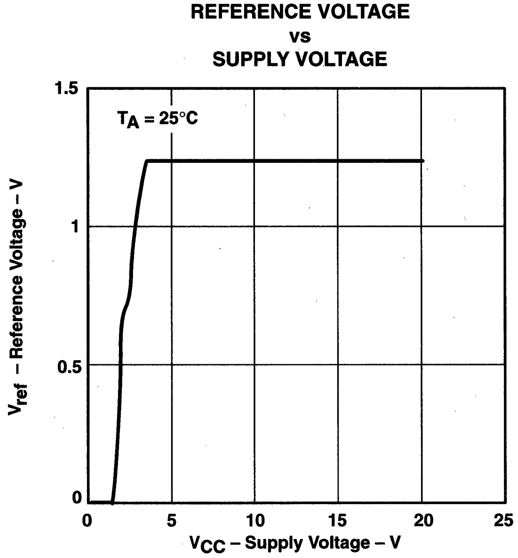


Figure 30

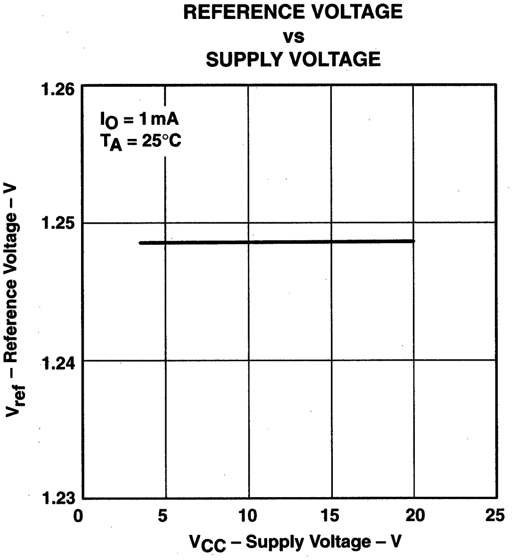


Figure 31

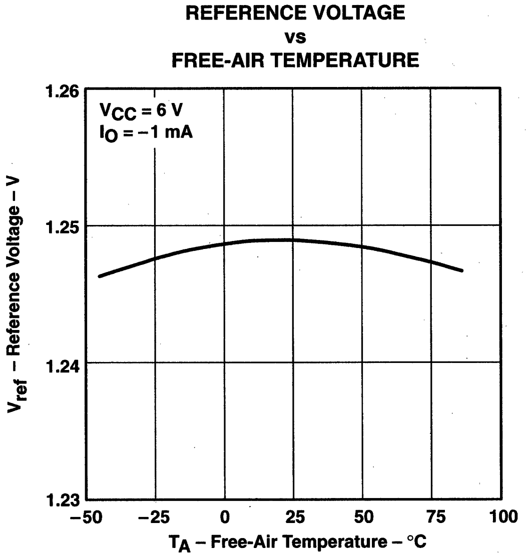


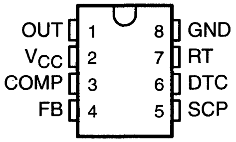
Figure 32

TL5001, TL5001Y
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS084C – APRIL 1994 – REVISED SEPTEMBER 1995

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 40 kHz to 400 kHz**
- **Variable Dead Time Provides Control Over Total Range**

D OR P PACKAGE
(TOP VIEW)



description

The TL5001 incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001 contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

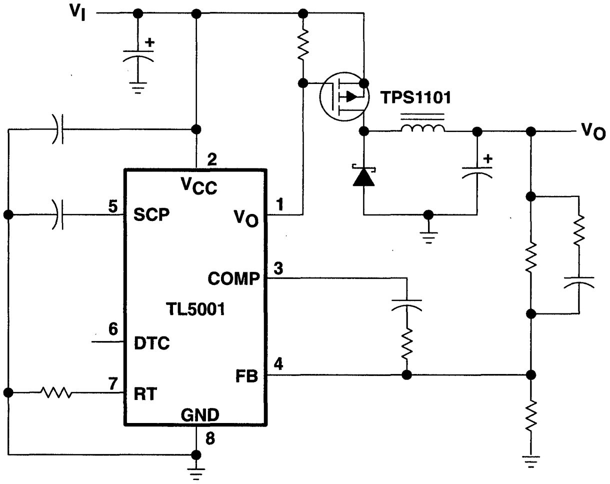
The TL5001C is characterized for operation from −20°C to 85°C. The TL5001I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)	PLASTIC DIP (P)	CHIP FORM (Y)
−20°C to 85°C	TL5001CD	TL5001CP	TL5001Y
−40°C to 85°C	TL5001ID	TL5001IP	—

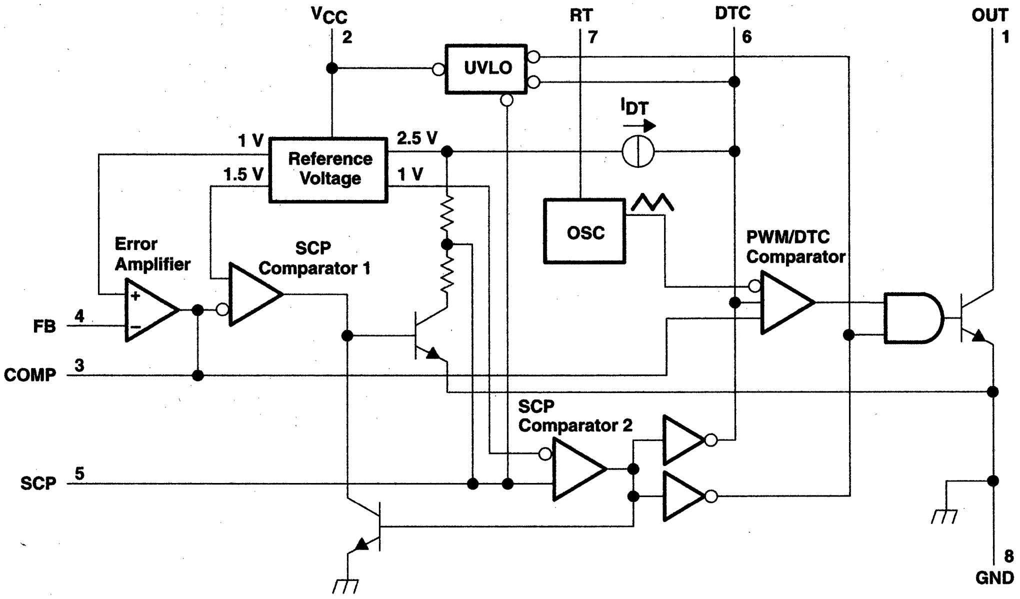
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR). Chip forms are tested at T_A = 25°C.

schematic for typical application



TEXAS INSTRUMENTS

functional block diagram

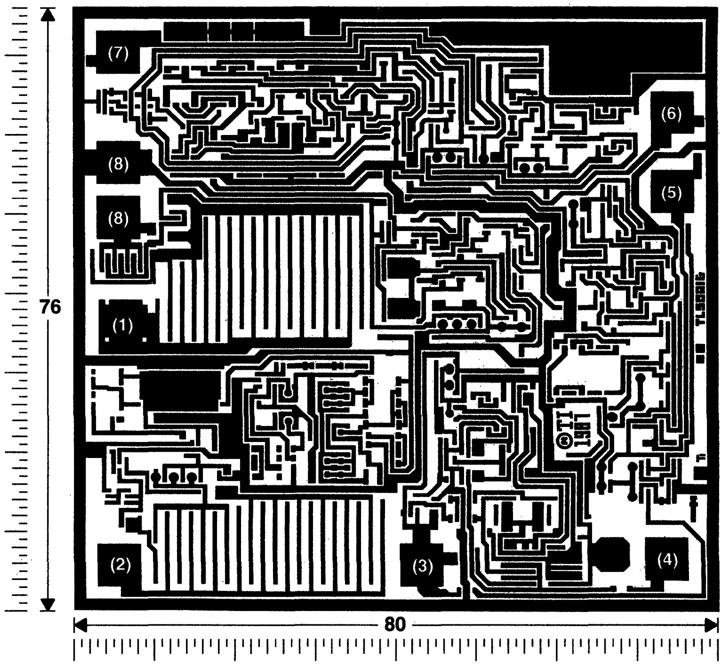


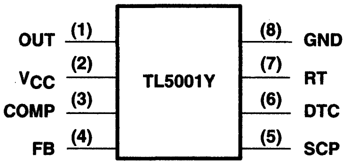
]

TL5001Y chip information

This chip, when properly assembled, displays characteristics similar to the TL5001C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
11 MILS TYPICAL

BONDING PADS:
7X7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001 and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input. The 1-V reference remains within 5% of nominal over the operating temperature range.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2)\ (1\ V)$$

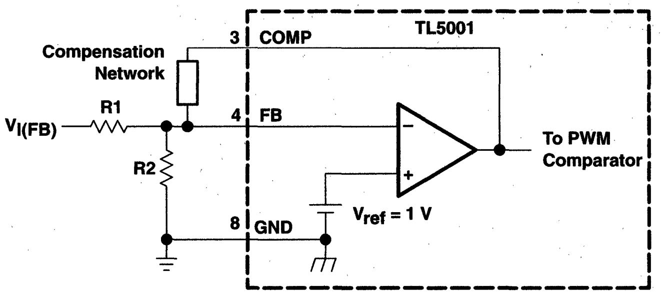


Figure 1. Error-Amplifier Gain Setting

error amplifier (continued)

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 μA, the total dc load resistance should be 100 kΩ or more.

oscillator/PWM

The oscillator frequency (f_{osc}) can be set between 40 kHz and 400 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

$$R_{DT} = \left(R_t + 1250\right)\left[D\left(V_{osc}max - V_{osc}min\right) + V_{osc}min\right]$$

where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1-e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

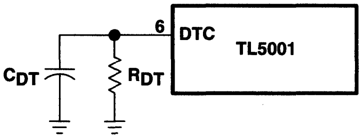


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001 remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001 includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001 output transistor.

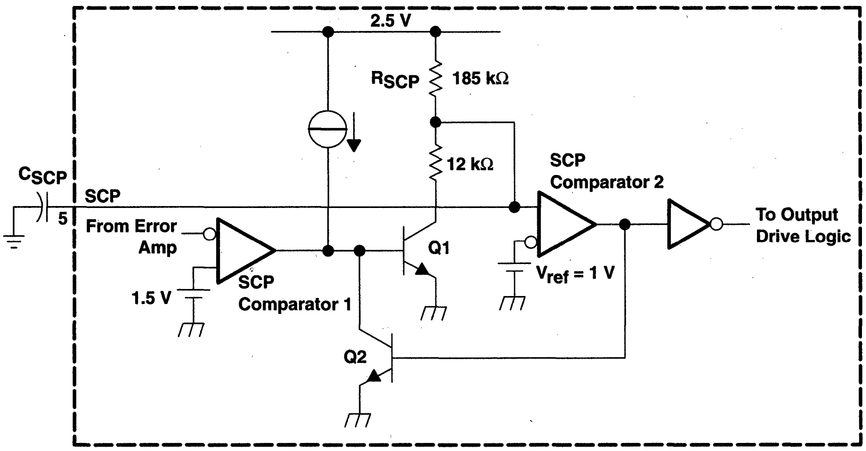


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}), connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)\left(1 - e^{-t/\tau}\right) + 0.185$$

where

$$\tau = R_{SCP} C_{SCP}$$

The end of the time-out period, t_{SCP}, occurs when $V_{SCP} = 1$ V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

where

t is in seconds, C in μF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001 is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	41 V
Amplifier input voltage, $V_{I(FB)}$	20 V
Output voltage, V_O, OUT	51 V
Output current, I_O, OUT	21 mA
Output peak current, $I_{O(peak)}$, OUT	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating ambient temperature range, T_A: TL5001C	−20°C to 85°C
TL5001I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	40	V
Amplifier input voltage, $V_{I(FB)}$		0	1.5	V
Output voltage, V_O, OUT			50	V
Output current, I_O, OUT			20	mA
COMP source current			45	µA
COMP dc load resistance		100		kΩ
Oscillator timing resistor, R_t		15	250	kΩ
Oscillator frequency, f_{osc}		40	400	kHz
Operating ambient temperature, T_A	TL5001C	−20	85	°C
	TL5001I	−40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Output voltage	COMP connected to FB	0.95	1	1.05	V
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	T_A = −20°C to 25°C (TL5001C)	−10	−1	10	mV/V
	T_A = −40°C to 25°C (TL5001I)	−10	−1	10	
	T_A = 25°C to 85°C	−10	−2	10	

† All typical values are at T_A = 25°C.

undervoltage lockout

PARAMETER	TL5001C, TL5001I			UNIT
	MIN	TYP†	MAX	
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis	100	200		mV

† All typical values are at T_A = 25°C.

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
SCP threshold voltage	T_A = 25°C	0.95	1.00	1.05	V
SCP voltage, latched	No pullup	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120	mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

† All typical values are at T_A = 25°C.

oscillator

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature	T_A = −20°C to 25°C	−4	−0.4	4	kHz
	T_A = 25°C to 85°C	−4	−0.2	4	
Voltage at RT			1		V

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

dead-time control

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I MIN	TYP†	MAX	UNIT
Output (source) current		0.9 × I_{RT}‡		1.1 × I_{RT}	µA
Input threshold voltage	Duty cycle = 0%	0.5	0.7		V
	Duty cycle = 100%		1.3	1.5	

† All typical values are at T_A = 25°C.
‡ Output source current at RT

error amplifier

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I MIN	TYP†	MAX	UNIT
Input voltage		V_{CC} = 3.6 V to 40 V	0		1.5	V
Input bias current				−160	−500	nA
Output voltage swing	Positive		1.5	2.3		V
	Negative			0.3	0.4	V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	−45	−90		µA

† All typical values are at T_A = 25°C.

output

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I MIN	TYP†	MAX	UNIT
Output saturation voltage	I_O = 10 mA		1.5	2	V
Off-state current	V_O = 50 V, V_{CC} = 0			10	µA
	V_O = 50 V			10	
Short-circuit output current	V_O = 6 V		40		mA

† All typical values are at T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I MIN	TYP†	MAX	UNIT
Standby supply current	Off state			1	1.5	mA
Average supply current		R_t = 100 kΩ		1.1	2.1	mA

† All typical values are at T_A = 25°C.

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Output voltage	COMP connected to FB		1		V
Input regulation	V_{CC} = 3.6 V to 40 V		2		mV
Output voltage change with temperature			−2		mV/V

undervoltage lockout

PARAMETER	TL5001Y			UNIT
	MIN	TYP	MAX	
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis		200		mV

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
SCP threshold voltage			1		V
SCP voltage, latched	No pullup		185		mV
SCP voltage, UVLO standby	No pullup		60		mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

oscillator

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature			−0.4		kHz
			−0.2		
Voltage at RT			1		V

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted) (continued)

dead-time control

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage	Duty cycle = 0%		0.7		V
	Duty cycle = 100%		1.3		

error amplifier

PARAMETER		TEST CONDITIONS	TL5001Y			UNIT
			MIN	TYP	MAX	
Input bias current				–160		nA
Output voltage swing	Positive			2.3		V
	Negative			0.3		V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V		600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V		–90		µA

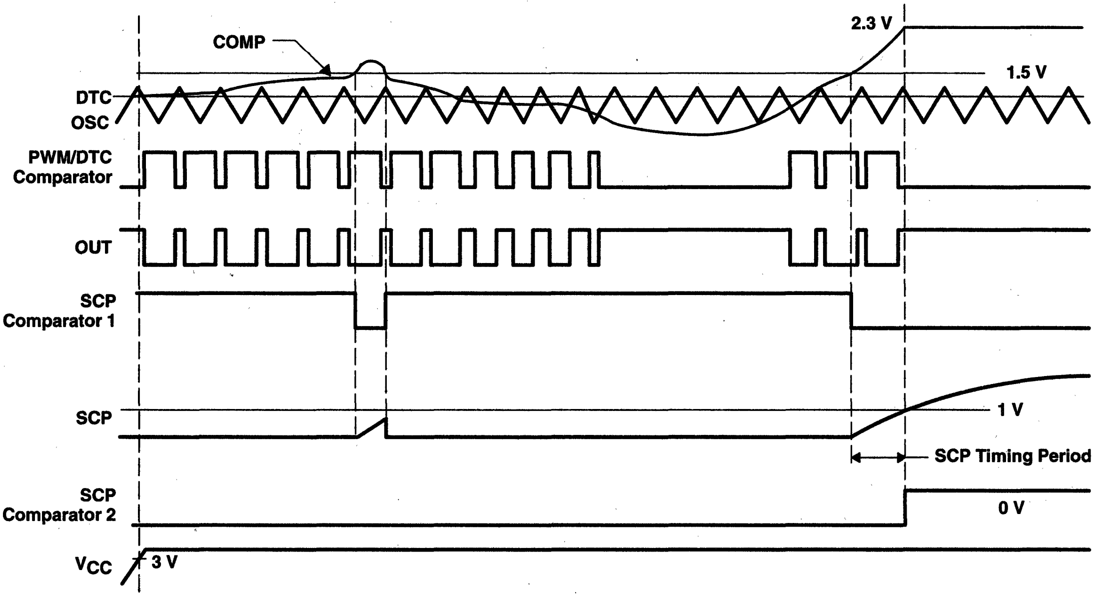
output

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Output saturation voltage	I_O = 10 mA		1.5	2	V
Short-circuit output current	V_O = 6 V		40		mA

total device

PARAMETER		TEST CONDITIONS	TL5001Y			UNIT
			MIN	TYP	MAX	
Standby supply current	Off state			1		mA
Average supply current		R_t = 100 kΩ		1.1		mA

PARAMETER MEASUREMENT INFORMATION



NOTE A. The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

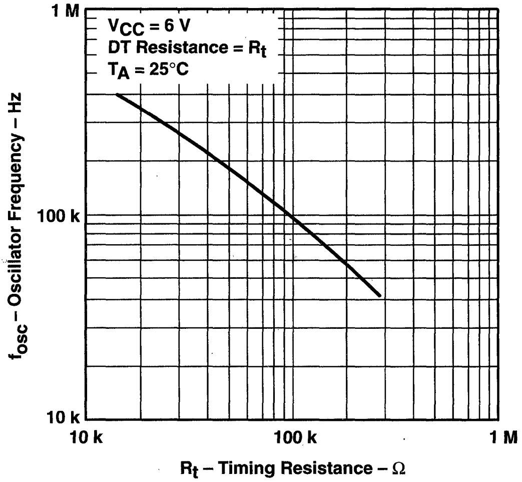


Figure 5

OSCILLATION FREQUENCY vs AMBIENT TEMPERATURE

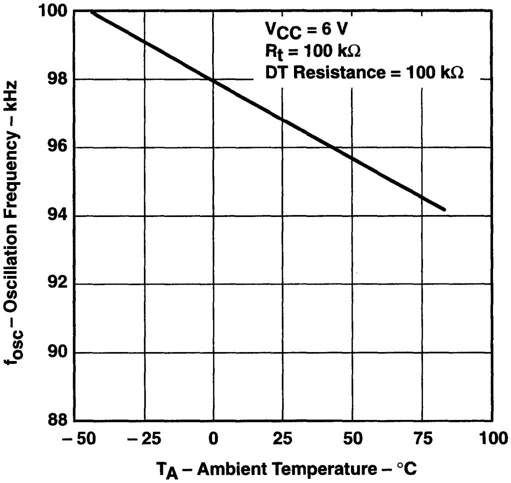


Figure 6

REFERENCE OUTPUT VOLTAGE vs POWER-SUPPLY VOLTAGE

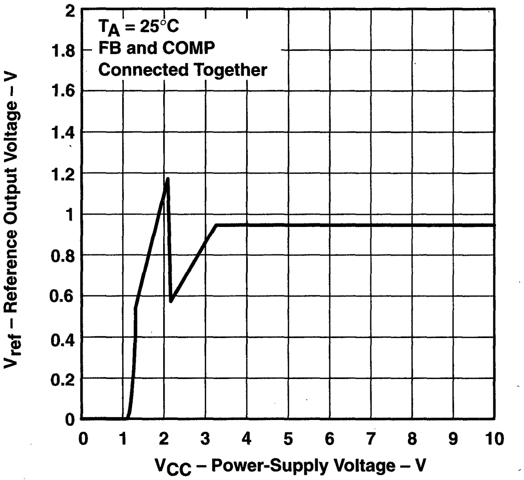


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION vs AMBIENT TEMPERATURE

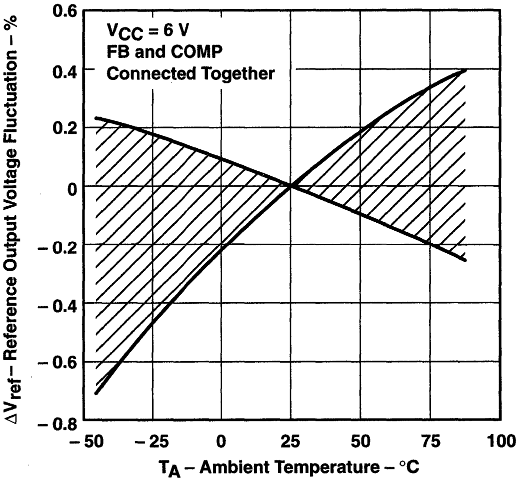
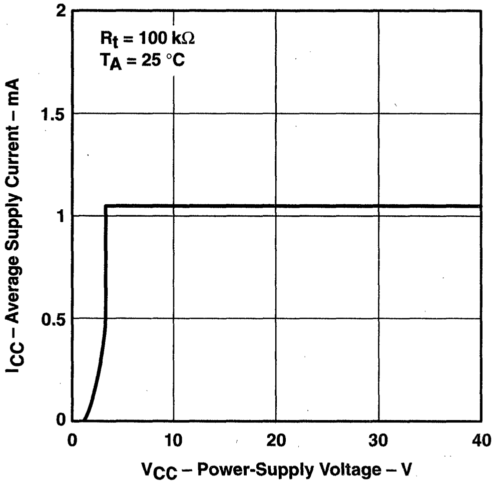


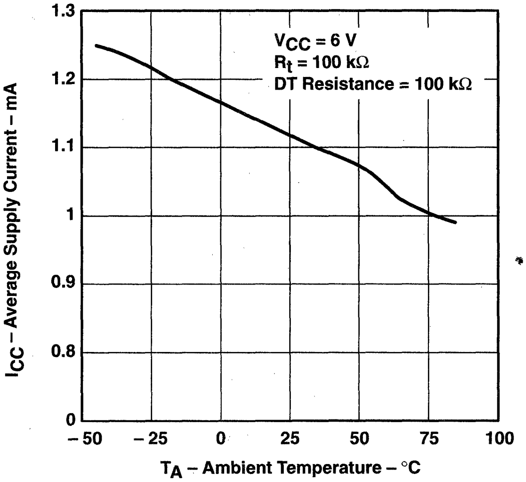
Figure 8

TYPICAL CHARACTERISTICS



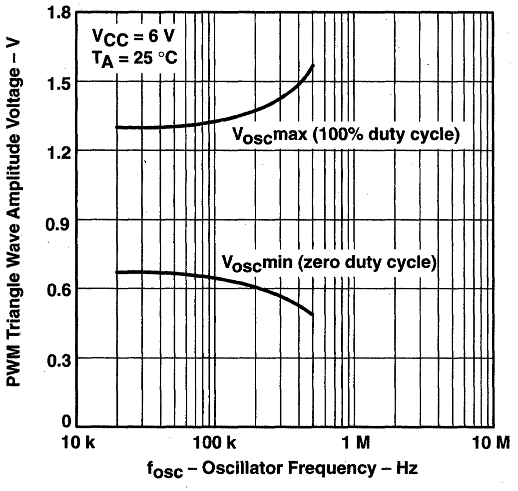
AVERAGE SUPPLY CURRENT
vs
POWER-SUPPLY VOLTAGE

Figure 9



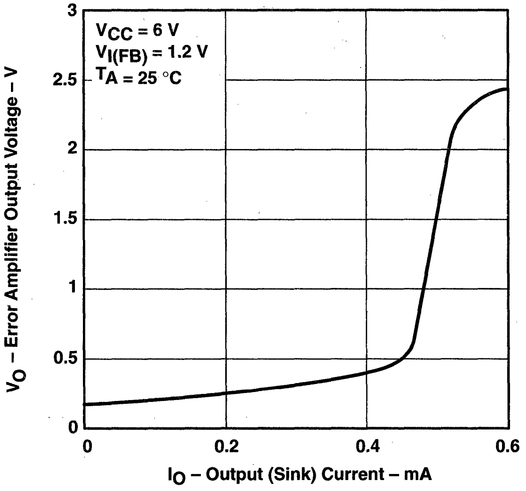
AVERAGE SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

Figure 10



PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
vs
OSCILLATOR FREQUENCY

Figure 11



ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT (SINK) CURRENT

Figure 12

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE vs OUTPUT (SOURCE) CURRENT

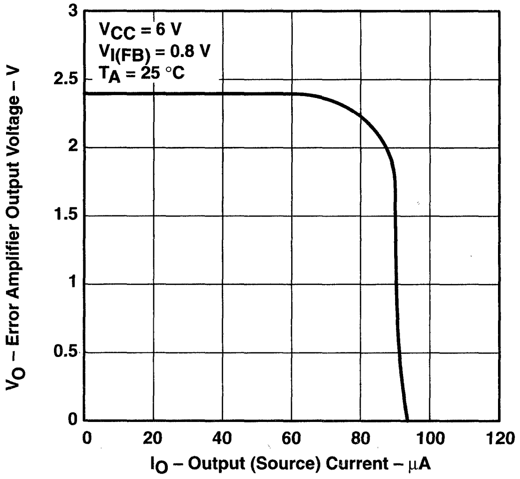


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

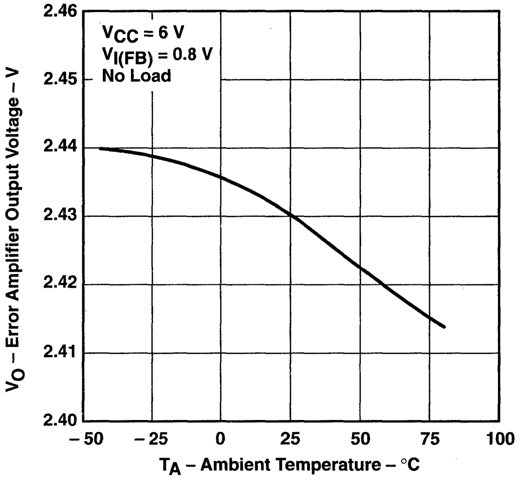


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

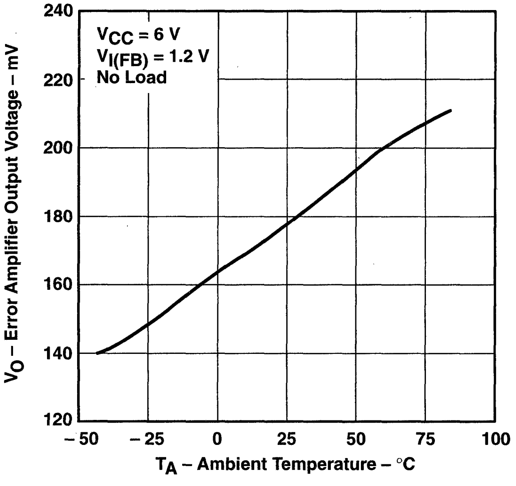


Figure 15

ERROR AMPLIFIER CLOSED-LOOP GAIN AND PHASE SHIFT vs OSCILLATOR FREQUENCY

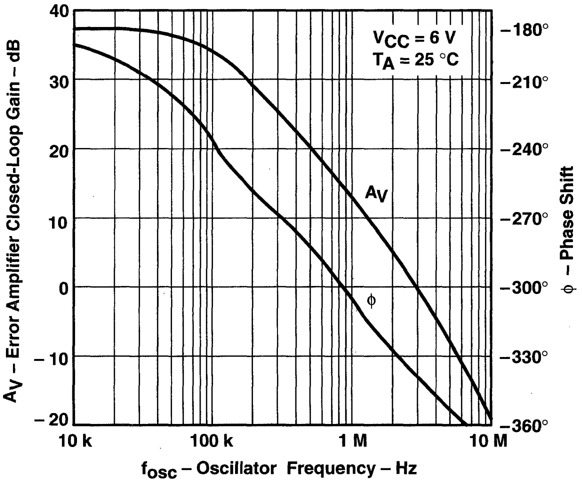


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT DUTY CYCLE vs DTC VOLTAGE

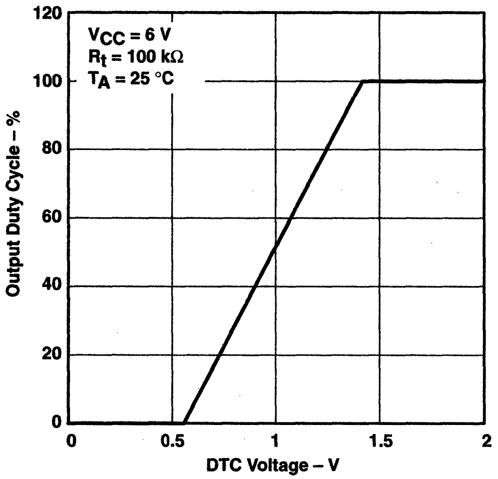


Figure 17

SCP TIME-OUT PERIOD vs SCP CAPACITANCE

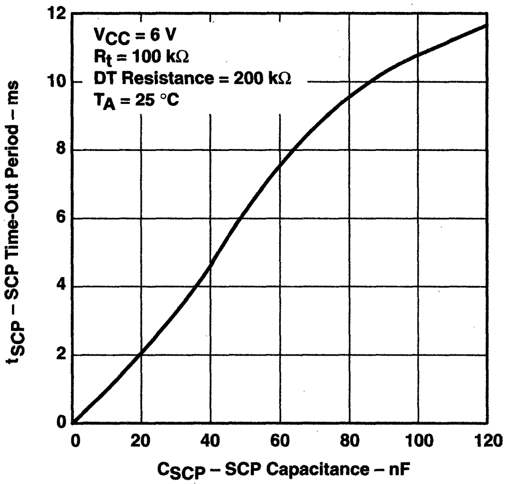


Figure 18

DTC OUTPUT CURRENT vs RT OUTPUT CURRENT

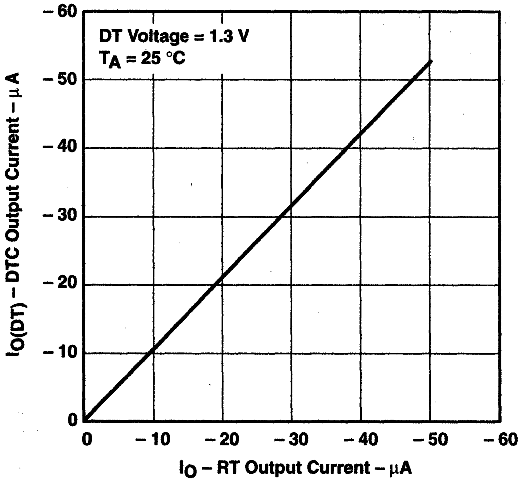


Figure 19

OUTPUT SATURATION VOLTAGE vs OUTPUT (SINK) CURRENT

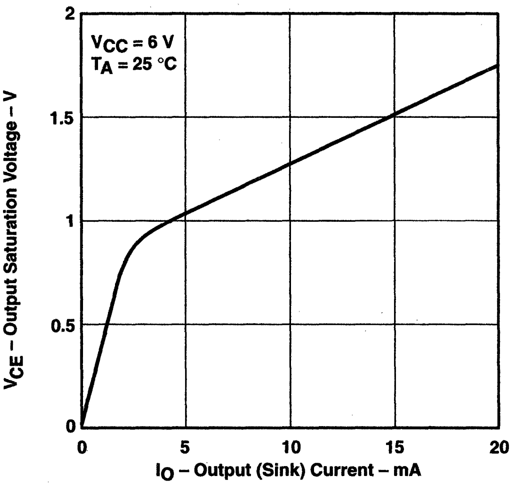
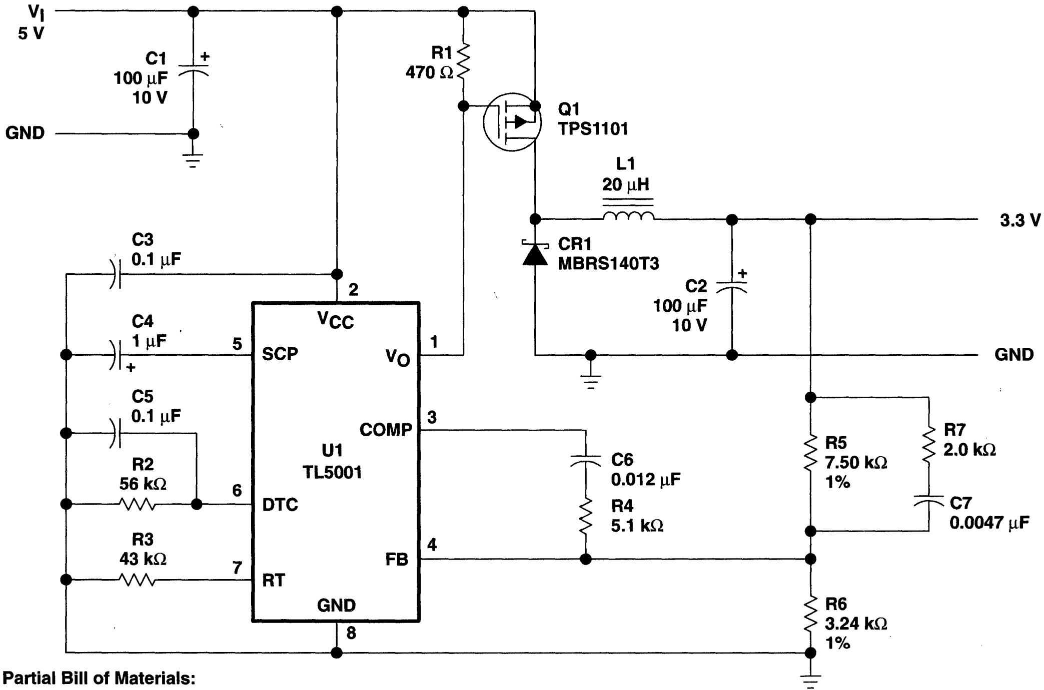


Figure 20

APPLICATION INFORMATION



Partial Bill of Materials:

U1	TL5001	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

NOTES:
A. Frequency = 200 kHz
B. Duty cycle = 90% max
C. Soft-start time constant (TC) = 5.6 ms
D. SCP TC = 70 msA

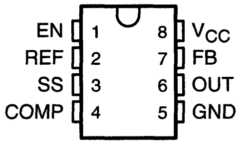
Figure 21. Step-Down Converter

TPS6734I
FIXED 12-V 120-mA BOOST-CONVERTER SUPPLY

SLVS127 – AUGUST 1995

- **Pin-for-Pin Compatible With MAX734**
- **Programming Voltage for Flash Memory**
- **2.7-V to 11-V Input Operating Range**
- **Output Current of 120 mA or Greater From 3.75-V or Higher Input**
- **3-μA Maximum Supply Current in Shutdown**
- **Only 5 External Components Required**
- **High Efficiency . . . 85% Typical (5-V Input, 120-mA Output)**
- **8-Pin SOIC and DIP Packages**
- **–40°C to 85°C Free-Air Operating Temperature Range**

D OR P PACKAGE
(TOP VIEW)



description

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 3.75 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use.

High efficiency at low supply voltages and low supply current in shutdown make the TPS6734 particularly attractive for flash memory programming supplies, PCMCIA cards, and operational amplifiers in battery-powered equipment. The TPS6734 is available in 8-pin DIP and SOIC packages and operates over a free-air temperature range of –40°C to 85°C.

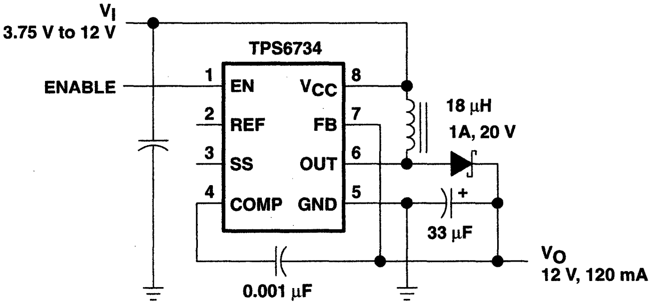


Figure 1. Typical Operating Circuit

AVAILABLE OPTIONS

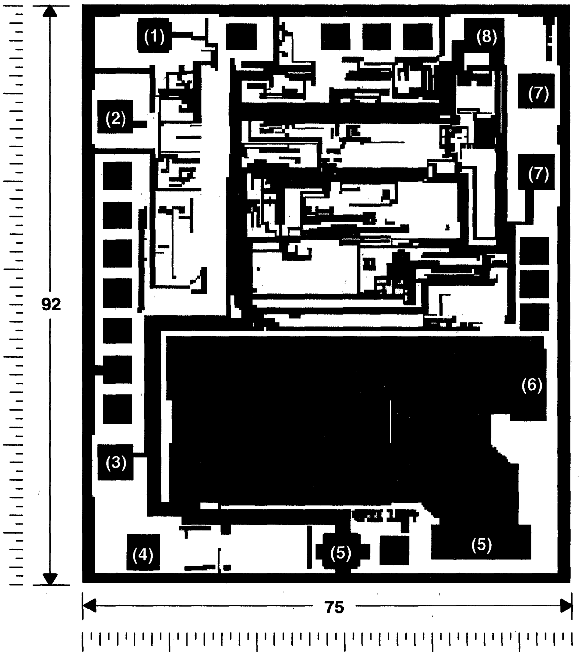
T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
−40°C to 85°C	TPS6734ID	TPS6734IP

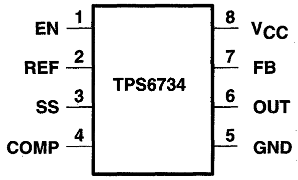
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TPS6734IDR).

TPS6734 chip information

Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pad. Chips can be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

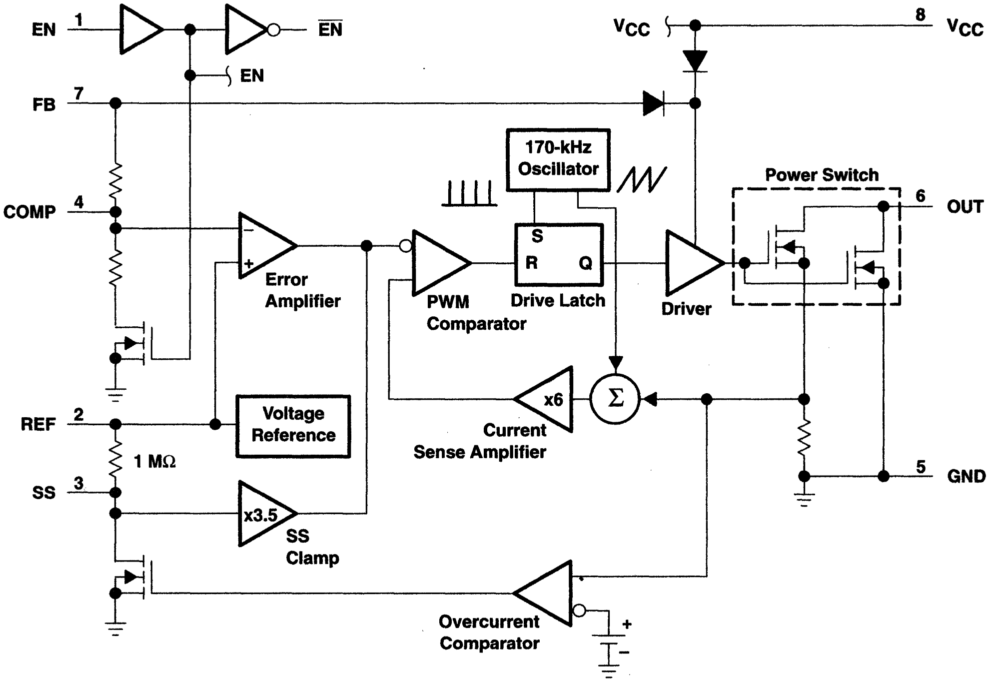
BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL
BONDING PADS: 4X4 MILS MINIMUM
$T_J$max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
EN	1	Enable. EN ≥ 2 V turns on the TPS6734. EN ≤ 0.4 V turns it off and reduces the supply current to 3 µA max.
REF	2	1.22-V reference voltage output. REF can source 100 µA for external loads.
SS	3	Soft Start. A capacitor between SS and GND brings the output voltage up slowly at power-up.
COMP	4	Compensation connection. A 0.001-µF capacitor between COMP and FB stabilizes the feedback loop.
GND	5	Ground
OUT	6	N-channel MOSFET drain connection
FB	7	Feedback voltage. FB is connected to the converter output for the feedback loop.
V_{CC}	8	Supply voltage input

detailed description

The following descriptions refer to the functional block diagram.

reference

The internal 1.22-V reference is brought out on REF and can source 100 μA maximum to external loads. A 0.01-μF to 0.1-μF decoupling capacitor connected between REF and GND is recommended to minimize noise pickup.

oscillator and ramp generator

The oscillator circuit provides a 170-kHz clock, to set the converter operating frequency, and a timing ramp for slope compensation. The clock waveform is a pulse, a few hundred nanoseconds in duration, that is used to limit the maximum power-switch duty cycle to 95%. The timing ramp is summed with the current-sense signal at the input to the current-sense amplifier.

driver latch

The latch, which consists of a set/reset flip-flop and associated logic, is used to control the state of the power switch by turning the driver on and off. A high output from the latch turns the switch on; a low output from the latch turns it off. In normal operation, the flip-flop is set high during the clock pulse, but gating keeps the latch output low until the clock pulse is over. The latch is reset when the PWM comparator output goes high.

current-sense amplifier

The current-sense amplifier has a fixed gain of 6. It amplifies the slope-compensated current-sense voltage (a summation of the voltage on the current-sense resistor and the oscillator ramp) and feeds it to the PWM comparator.

error amplifier

The error amplifier is a high-gain differential amplifier used to regulate the converter output voltage. The amplifier generates an error signal, which is fed to the PWM comparator. The error signal is generated when a sample of the output voltage is compared to the internal reference and the difference is amplified. The output sample is obtained from a resistive divider connected between FB and GND. FB is externally connected to the converter output, and the divider output is connected to both the error amplifier input and COMP. A 0.001-μF capacitor connected between FB and COMP stabilizes the voltage control loop.

PWM comparator

The PWM comparator resets the drive latch and turns off the power switch whenever the slope-compensated current-sense signal from the current-sense amplifier exceeds the error signal.

power switch

The power switch is a 0.7-Ω n-channel MOSFET with current-sensing. The drain is connected to OUT and the current sense is connected to a resistor. The voltage across the resistor is proportional to the current in the power switch and is tied to the overcurrent comparator and the current-sense amplifier. In normal operation, the power switch is turned on at the start of each clock cycle and turned off when the PWM comparator resets the drive latch.

SS clamp

The SS (soft-start) clamp circuit limits the signal level on error-amplifier output during start-up. The voltage on SS is amplified and used to momentarily override the error-amplifier output until it rises above that output, at which point the error-amplifier takes over. This prevents the input to the PWM comparator from exceeding its common-mode range (the error-amplifier output too high to be reached by the current ramp) by limiting the maximum voltage on the error-amplifier output during start-up.

soft start

Soft start causes the output voltage to increase to the regulation point at a controlled rate of rise. The voltage on the charging soft-start capacitor gradually raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by increasing the current-limit threshold on a cycle-by-cycle basis. Even if SS has no capacitor installed, some distributed capacitance will always be present. A soft-start cycle is initiated when either the enable signal (EN) is switched high, or an overcurrent fault condition triggers the discharge of the soft-start capacitor.

overcurrent comparator

The overcurrent comparator monitors the current in the power switch. The comparator trips and initiates a soft-start cycle if the power-switch current exceeds 1.5-A peak. On each clock cycle, the power switch turns on and attempts to deliver current until the overcurrent limits are exceeded.

enable (EN)

A logic low on EN puts the TPS6734 in shutdown mode. In shutdown, the output power switch, voltage reference, and other functions are shut off, the supply current is reduced to 3 µA maximum, and the soft-start capacitor is discharged through a 1-MΩ resistance. The output voltage falls to a diode drop below the input voltage because of the current path from input to output through the inductor and diode.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Pin voltages: V_{CC}, OUT (see Note 1) . . . . −0.3 V to 15 V
SS, COMP, EN (see Note 1) . . . . −0.3 V to V_{CC}+ 0.3 V
Peak switch current . . . . 1.5 A
Reference current . . . . 2.5 mA
Continuous power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 s . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to network terminal ground.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage	2.7	5	12	V
Compensation capacitor		0.001		µF
Output current at REF	0		100	µA
Reference capacitor		0.01		µF
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, $I_{O(LOAD)}$ = 0 mA, EN = 5 V, typical values are at T_A = 25°C (unless otherwise noted) (refer to circuit shown in Figure 13)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current	Operating	Entire circuit		1.2	2.5	mA
	Standby	EN = 0.4 V, entire circuit			3	µA
		EN = 0.4 V, into V_{CC}			3	µA
High-level input threshold voltage at EN			2			V
Low-level input threshold voltage at EN					0.4	V
Shutdown input leakage current at EN			−1		1	µA
On resistance at OUT		Current at OUT = 500 mA		0.7		Ω
Leakage current at OUT		V_{DS} = 12 V		1		µA
Reference voltage				1.22		V
Reference drift		T_A = −40°C to 85°C		6.7		ppm/°C
Oscillator frequency				170		kHz
Compensation pin impedance				7500		Ω

performance characteristics over recommended operating free-air temperature range, typical circuit connected as shown in Figure 13, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output voltage	V_{CC} = 4.75 V,	0 mA < $I_{O(LOAD)}$ < 120 mA	11.64	12.12	12.6	V
Load current	V_{CC} = 3.75 V		120	150		mA
	V_{CC} = 3.0 V,	Figure 11		150		
Line regulation	V_{CC} = 5 V to 12 V,	$I_{O(LOAD)}$ = 50 mA		0.20%		
Load regulation	$I_{O(LOAD)}$ = 0 mA to 120 mA			0.0042%		
Efficiency	V_{CC} = 5 V,	$I_{O(LOAD)}$ = 120 mA		86%		

TYPICAL CHARACTERISTICS

LOAD TRANSIENT RESPONSE

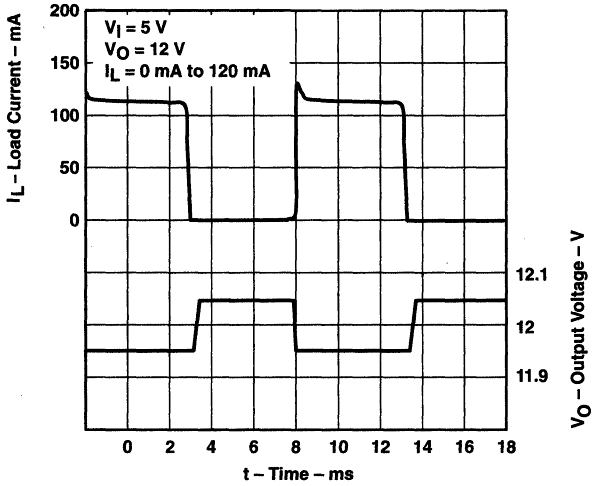


Figure 2

LINE TRANSIENT RESPONSE

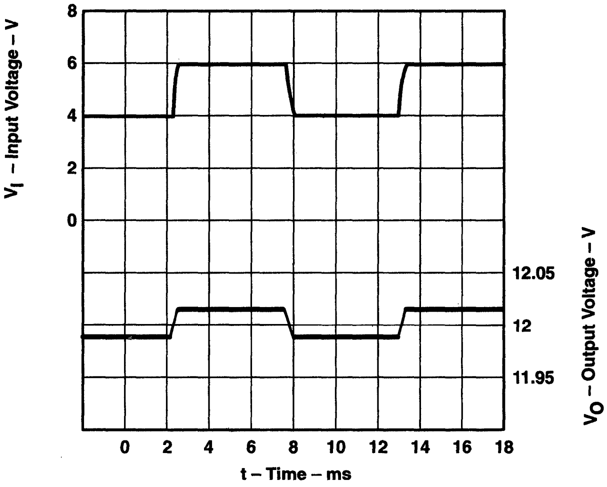


Figure 3

TYPICAL CHARACTERISTICS

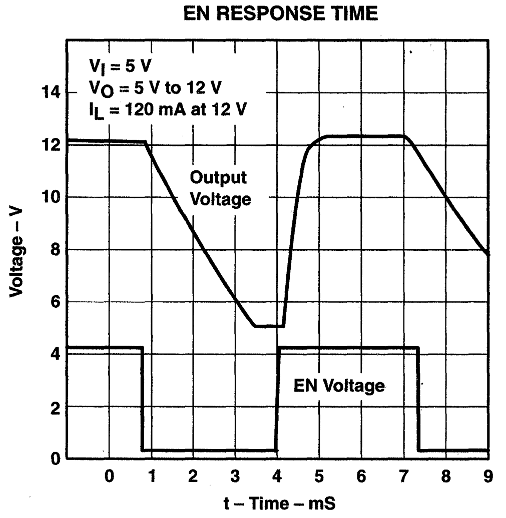

EN RESPONSE TIME

Figure 4

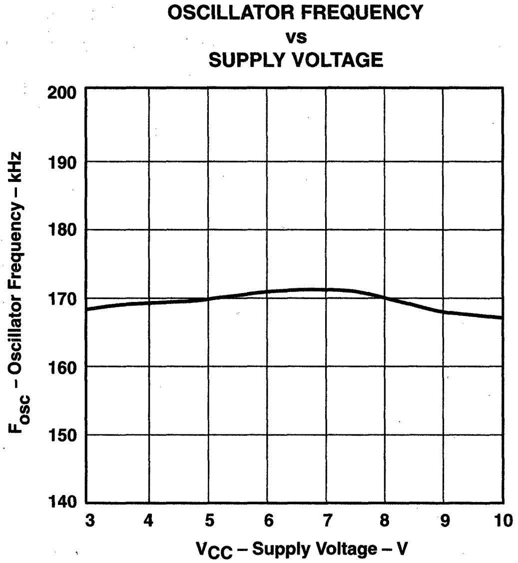

OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

Figure 5

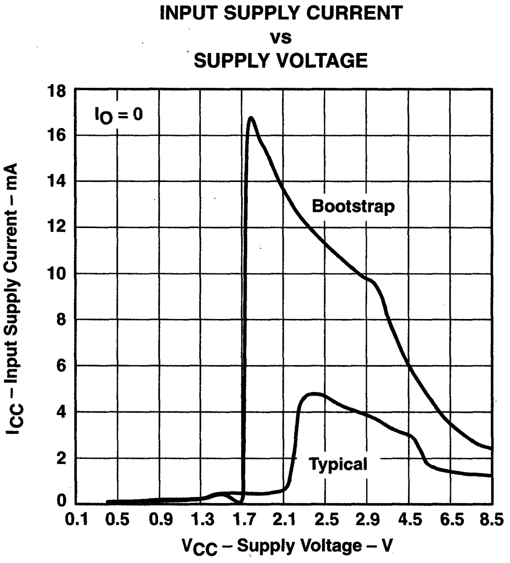

INPUT SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 6

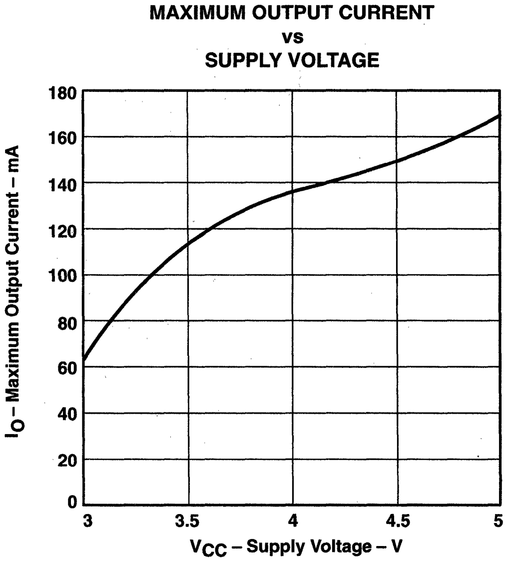

MAXIMUM OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 7

APPLICATION INFORMATION

The TPS6734 operates in a boost circuit as shown in Figures 1 and 11. Figure 1 shows the typical application circuit, which generates 12 V from a nominal 5-V source. The circuit is ideal for processor interface for energy management, because EN can be controlled by logic signals to place the 12-V source into the shutdown mode (3-μA current drain) when 12 V is not needed. An example of such an application is a flash memory device that requires 12 V for the erase cycle.

discontinuous mode

The circuit shown in Figure 1 operates in discontinuous mode over most of the range of input voltage and output current. In discontinuous mode, current through the inductor begins at zero, rises to a peak value, then ramps down to zero each cycle as shown by the voltage and current waveforms in Figure 8. The ringing in the voltage waveform on OUT results from a resonance between the inductor and the power switch capacitance and is normal for discontinuous operation.

DISCONTINUOUS MODE

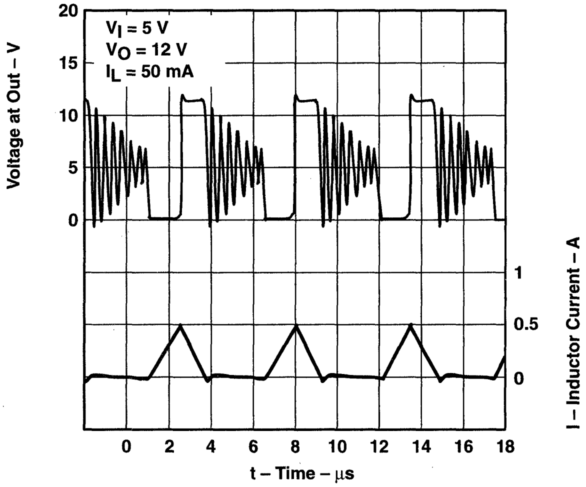


Figure 8

APPLICATION INFORMATION

continuous mode

When the converter is delivering heavy loads from low voltage sources, it operates in continuous mode. As shown in Figure 9, the inductor current does not drop to zero and the ringing is gone from the OUT voltage waveform.

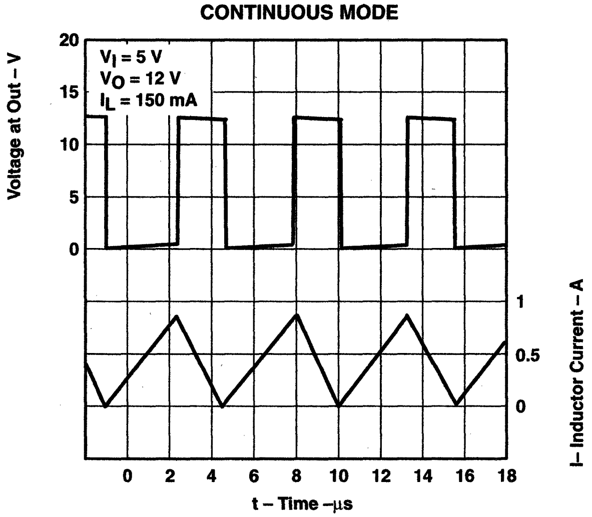


Figure 9

pulse-skipping mode

At very light load currents, the TPS6734 cannot generate drive pulses sufficiently narrow to maintain regulation and operate at 170 kHz. Under these circumstances, the converter operates in a pulse-skipping mode, in which cycles are skipped. In pulse-skipping mode, the waveforms are irregular and the output ripple contains a low-frequency component that may exceed 50 mV peak-to-peak.

APPLICATION INFORMATION

efficiency

Typical efficiency for the converter circuit shown in Figure 13 is plotted in Figure 10. The efficiency falls off rapidly at very light currents because the supply current is a significant percentage of the load.

EFFICIENCY
vs
OUTPUT CURRENT

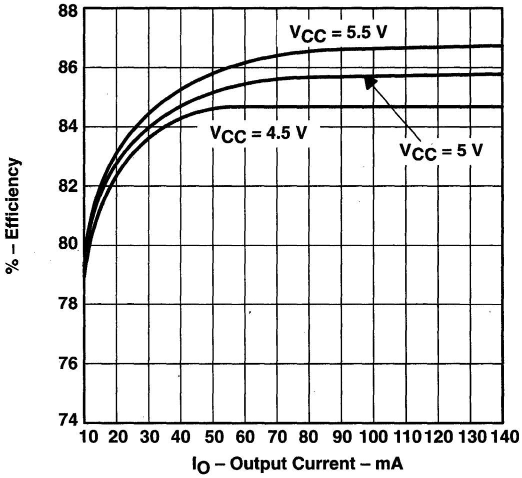


Figure 10

inductor selection

Inductance value is directly proportional to the input voltage and inversely proportional to the output power. The 18 µH shown in the typical circuit is the proper value for operation from 5-V sources up to 2-W loads. A lower inductance value should be used when operating from 3-V sources. Operation from 7 V and higher sources may require inductance values greater than 18 µH. The inductor's saturation current rating should be greater than three times the dc load current for 5-V inputs and five times the dc load for 3-V inputs.

output filter capacitor selection

The output filter capacitor should be selected for minimum ESR (equivalent series resistance). Capacitor ESR × ΔI_L (change in inductor current) determines the amplitude of the high-frequency ripple on the output voltage. The ESR of the capacitor should be less than 0.25 Ω to keep the output ripple less than 50 mV peak-to-peak over the entire current range (using 18-µH inductor).

diode

A Schottky diode or a high-speed silicon rectifier should be used. The continuous current rating of the diode should be at least 300 mA for full load (120 mA) operation.

APPLICATION INFORMATION

soft-start capacitor

Soft-start timing is controlled by the value of the SS capacitor. Table 1 lists soft-start time intervals for selected capacitor values and circuit conditions. If the circuit starts up with no load (e.g. in flash-memory programming supplies), no soft start is needed. Omitting the soft-start capacitor provides a minimum output-voltage rise time from the shutdown state, improving the output start-up time.

Table 1. Typical Soft-Start Times

SUPPLY VOLTAGE (V)	SOFT-START TIME† (ms) VERSUS CAPACITANCE (μF)				
	NO. CAP	0.047	0.1	0.47	1.0
5	0.70	22	42	220	400
7	0.46	15	37	185	225
9	0.38	10	17	88	155

† Soft-start times are ±35%

printed-circuit layout

Printed-circuit-board (PCB) layout is critical to quiet operation. A ground plane is recommended. Special attention should be given to minimizing the lengths of the switching loops. The first loop is formed by OUT, the diode, the output capacitor, and GND, the length of which can be minimized by connecting the anode of the diode close to OUT. The output capacitor should be connected, directly between the diode cathode and GND with the shortest possible path. The second loop is formed by OUT, the inductor, the input capacitor, and GND. This loop is less critical than the first; however, the connection of OUT, the inductor and the anode of the diode must be minimized. Bypass capacitors should be located as close to the device as possible to prevent instability and noise pickup. If a large V_{CC}-to-GND bypass capacitor cannot be placed adjacent to the IC pins, the pins should be bypassed directly with a small ceramic capacitor (e.g., 0.1 μF). The recommended layout shown in Figures 14 through 17 can provide guidance for PCB configuration (the ground plane beneath the TPS6734 and the short loops should be noted).

Plastic plug-in-type proto boards, or any construction scheme that allows long leads and the possibility of noise pickup, should not be used when assembling a breadboard or prototype application circuit implementing the TPS6734.

APPLICATION INFORMATION

bootstrapped output circuit

For operation below 2.7 V, the TPS6734 may be connected in a bootstrap configuration as shown in Figure 11. The bootstrap configuration is less efficient (requires more supply current and suffers a loss in efficiency at voltages below 5 V; see Figure 12) and is not recommended except for very low voltage operating conditions. Because the output-driver stage, which benefits most from higher voltages, is diode-coupled to the output voltage (see Figure 2), the bootstrapped configuration provides no benefit except at very low voltages. In the shutdown mode (EN = low), no-load quiescent current is unchanged (3 μA max) whether in the bootstrap or the typical configuration.

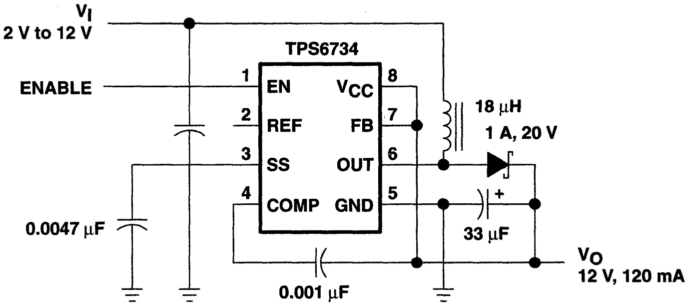


Figure 11. TPS6734 Bootstrap Configuration

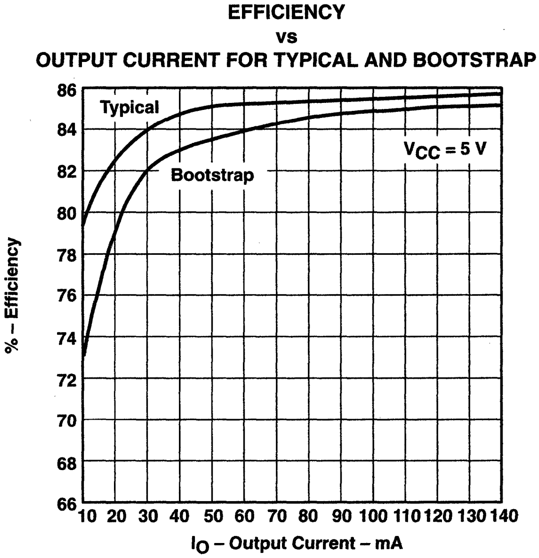
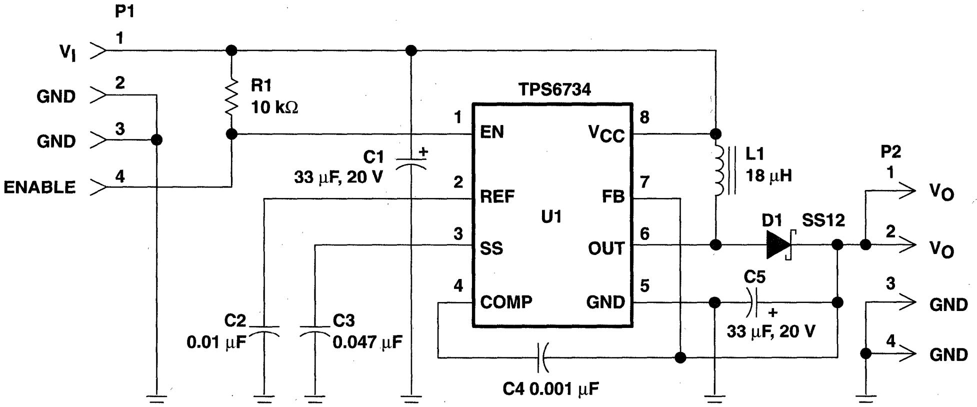


Figure 12

APPLICATION INFORMATION

TPS6734 converter design with recommended layout

The following schematic (Figure 13) and a required-components table are provided for a 12-V-output boost converter. The converter is capable of delivering 120 mA of output current over an input voltage range of 3.75 V to 12 V. Recommended layout and detailed artwork for a PCB are provided in Figures 14 through 17.



NOTE A: A jumper between pins P1-3 and P1-4 shuts off the TPS7634. Remove the jumper to resume normal operation.

Figure 13. Schematic for Printed Circuit Board (shown in Figures 14 through 17)

Required Components

QTY.	DESCRIPTION	REF DES	MANUFACTURER'S PART NO.	MANUFACTURER
1	IC, power supply, 12 V for flash memory	U1	TPS6734ID	Texas Instruments
1	Diode, Schottky	D1	SS12	General Instruments
1	Inductor, 18 µH, 150 mΩ, 1.23 A(DC)	L1	CD54180MC	Sumida
2	Capacitor, 33 µF, 20 V, tantalum	C1,5	TAPSD336M020R0200	AVX
1	Capacitor, 0.01 µF, 50 V, ceramic, 0805	C2		
1	Capacitor, 0.047 µF, 50 V, ceramic, 1206	C3		
1	Capacitor, 0.001 µF, 50 V, ceramic, 0805	C4		
2	Connector, header, 4-pin	P1,2		Molex
1	PCB, TPS6734			

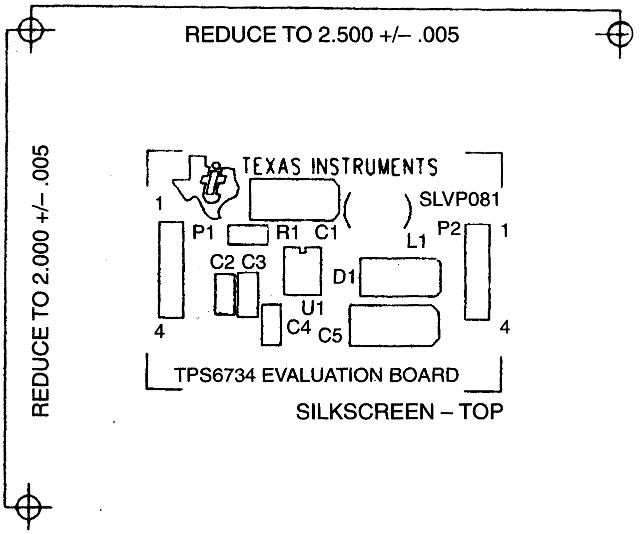


Figure 14. Component Placement

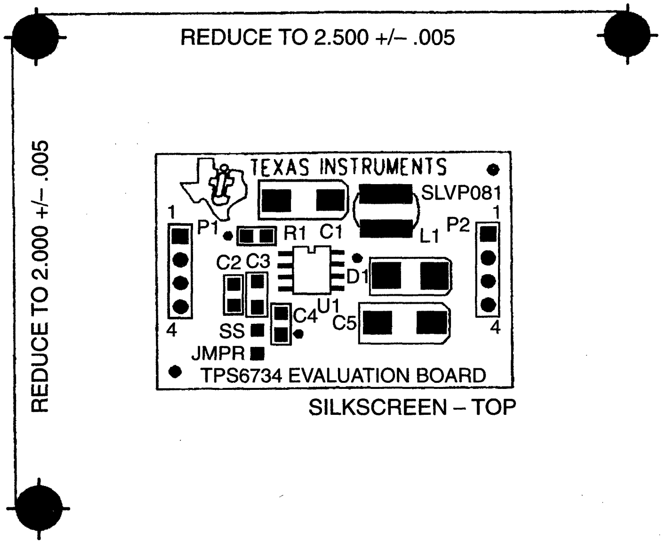


Figure 15. Solder Paste Mask

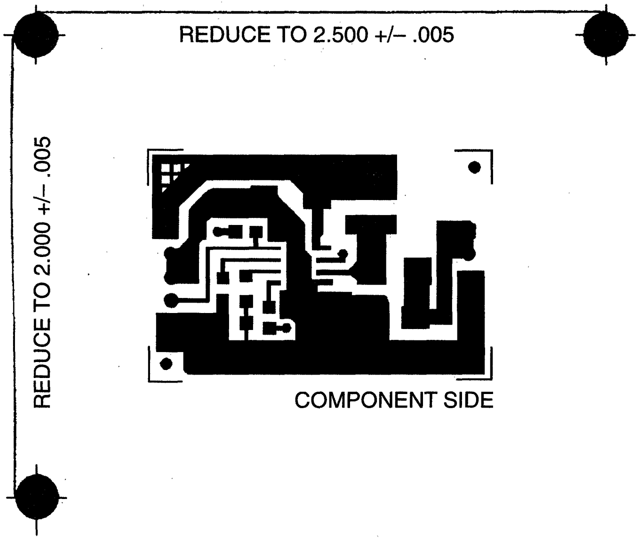


Figure 16. Printed Circuit, Component Side

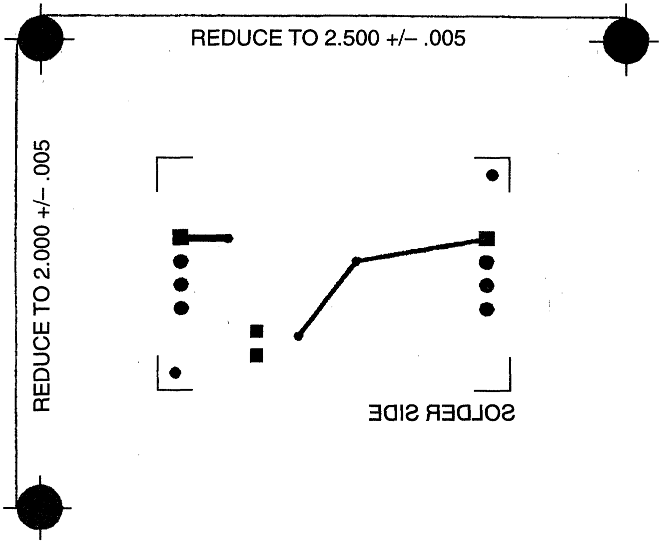
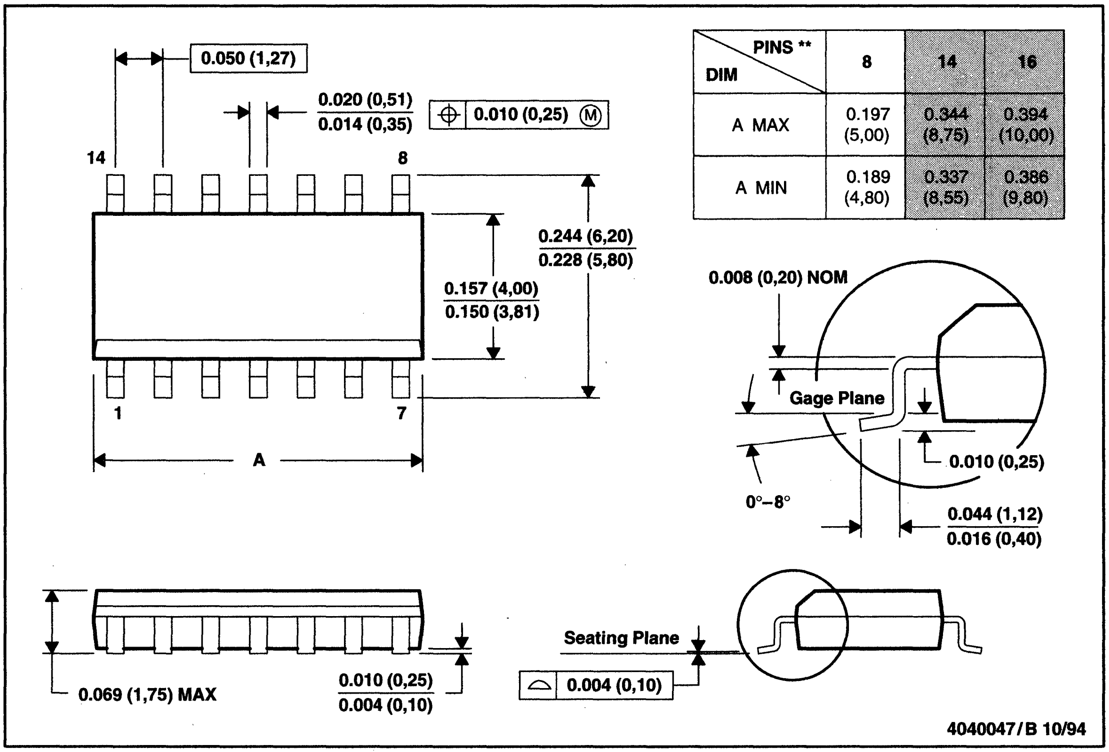


Figure 17. Printed Circuit, Wiring Side (Viewed from Component Side)

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

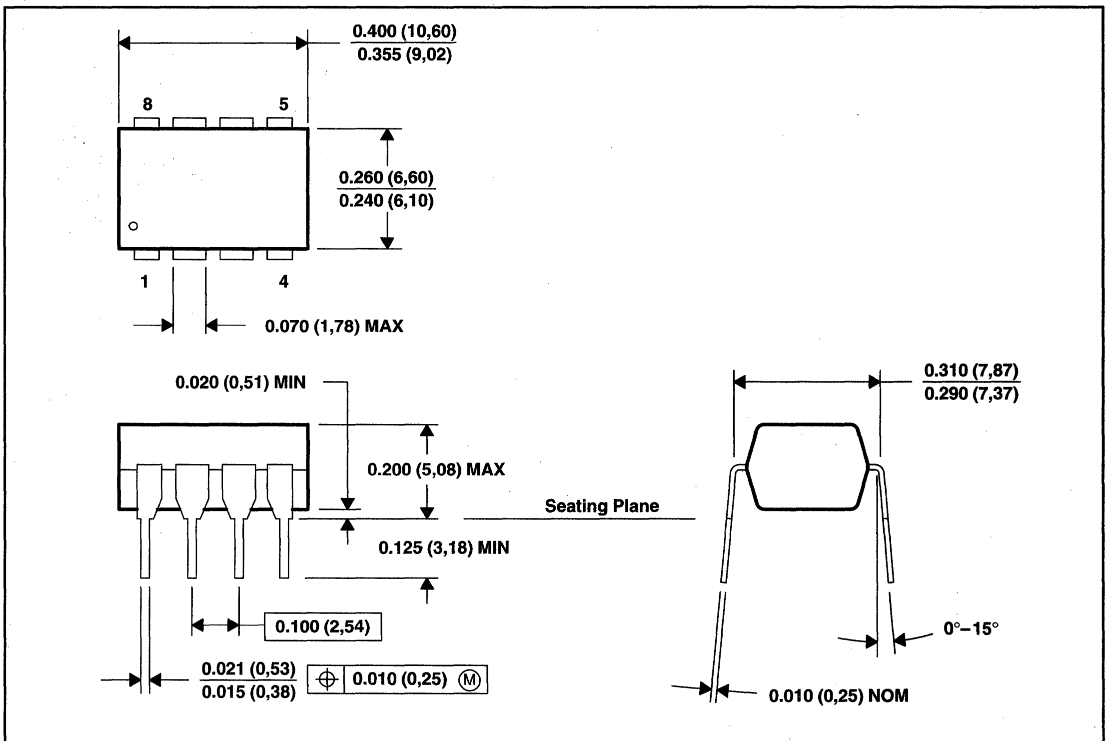


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad
- E. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



4040082/B 10/94

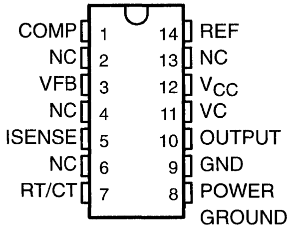
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

UC284x, UC384x, UC384xY
CURRENT-MODE PWM CONTROLLERS

SLVS038B – JANUARY 1989 – REVISED AUGUST 1995

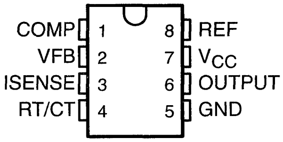
- **Optimized for Off-Line and dc-to-dc Converters**
- **Low Start-Up Current (<1 mA)**
- **Automatic Feed-Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load-Response Characteristics**
- **Undervoltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High-Current Totem-Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Error Amplifier With Low Output Resistance**
- **Designed to Be Interchangable With Unitrode UC2842 and UC3842 Series**

D PACKAGE
(TOP VIEW)



NC – No internal connection

P PACKAGE
(TOP VIEW)



description

The UC2842 and UC3842 series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO) featuring a start-up current of less than 1 mA and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (which also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

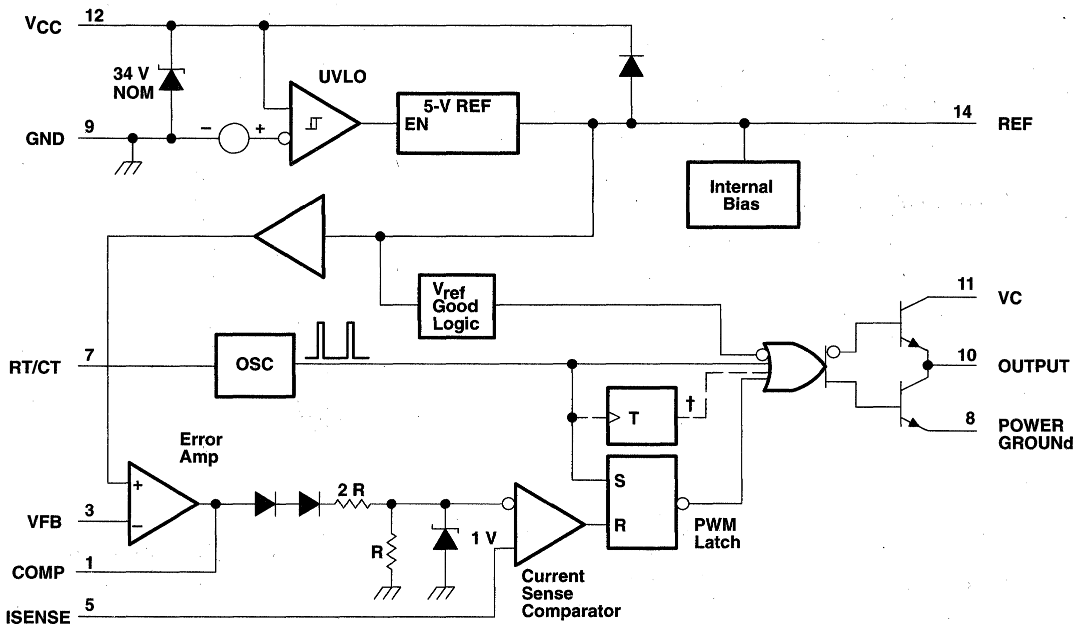
The primary difference between the UC2842-series devices and the UC3842-series devices is the ambient operating temperature range. The UC2842-series devices operate between −40°C and 85°C; the UC3842-series devices operate between 0°C and 70°C. Major differences between members of these series are the UVLO thresholds and maximum duty cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the UCx842 and UCx844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the UCx843 and UCx845 devices are 8.4 V (on) and 7.6 V (off). The UCx842 and UCx843 devices can operate to duty cycles approaching 100%. A duty cycle range of 0 to 50% is obtained by the UCx844 and UCx845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	UC3842D UC3843D UC3844D UC3845D	UC3842P UC3843P UC3844P UC3845P	UC3842Y UC3843Y UC3844Y UC3845Y
−40°C to 85°C	UC2842D UC2843D UC2844D UC2845D	UC2842P UC2843P UC2844P UC2845P	— — — —

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., LT1054CDWR).

functional block diagram

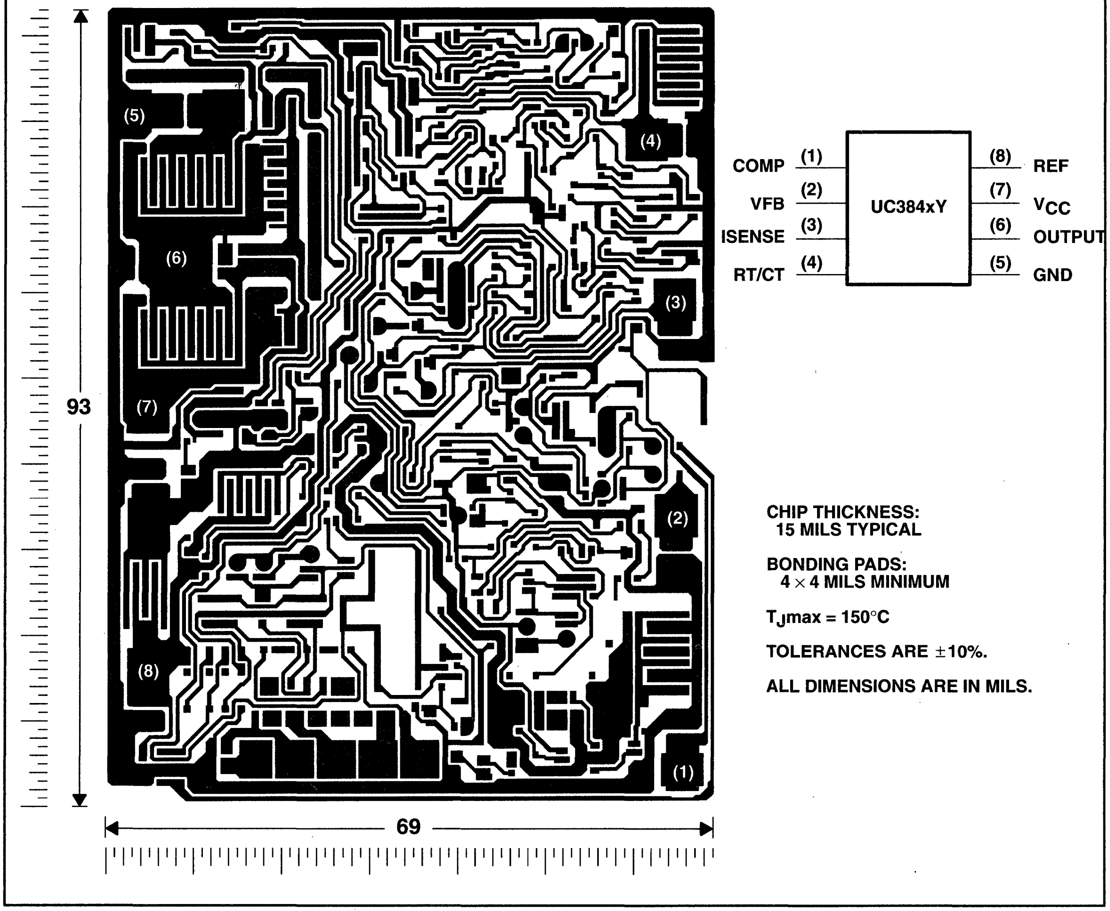


† The toggle flip-flop is present only in UC2844, UC2845, UC3844, and UC3845.
NOTE A: Terminal numbers apply to the D package only.

UC384xY chip information

This chip, when properly assembled, displays characteristics similar to the UC384x. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1) (I_{CC} < 30 mA)	Self Limiting
Analog input voltage range, V_I (VFB and ISENSE terminals)	– 0.3 V to 6.3 V
Output voltage, V_O (OUTPUT terminal)	35 V
Input voltage, V_I, (VC terminal, D package only)	35 V
Supply current, I_{CC}	30 mA
Output current, I_O	±1 A
Error amplifier output sink current	10 mA
Continuous total power dissipation	See Dissipation Rating Table
Output energy (capacitive load)	5 μJ
Operating free-air temperature range, T_A: UC284x	– 40°C to 85°C
UC384x	0°C to 70°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the device GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATE ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	UC284x			UC384x			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} and V_C†			30			30	V
Input voltage, V_I, RT/CT	0		5.5	0		5.5	V
Input voltage, V_I, VFB and ISENSE	0		5.5	0		5.5	V
Output voltage, V_O, OUTPUT	0		30	0		30	V
Output voltage, V_O, POWER GROUND†	–0.1		1	–0.1		1	V
Supply current, externally limited, I_{CC}			25			25	mA
Average output current, I_O			200			200	mA
Reference output current, $I_{O(ref)}$			–20			–20	mA
Timing capacitance, C_T				1			nF
Oscillator frequency, f_{osc}		100	500		100	500	kHz
Operating free-air temperature, T_A	–40		85	0		70	°C

† These recommended voltages for V_C and POWER GROUND apply only to the D package.

electrical characteristics, V_{CC} = 15 V (see Note 2), R_T = 10 kΩ, C_T = 3.3 nF, T_A = full range (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	I_O = 1 mA, T_J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25		6	25	mV
Temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage with worst-case variation	V_{CC} = 12 V to 25 V, I_O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C		50			50		µV
Output voltage long-term drift	After 1000 h at T_A = 25°C		5	25		5	25	mV
Short-circuit output current		–30	–100	–180	–30	–100	–180	mA

† All typical values are at T_J = 25°C.

NOTE 2: Adjust V_{CC} above the start threshold before setting it to 15 V.

oscillator section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Oscillator frequency (see Note 3)	T_J = 25°C	47	52	57	47	52	57	kHz
Frequency change with supply voltage	V_{CC} = 12 V to 25 V		2	10		2	10	Hz/kHz
Frequency change with temperature	T_A = T_{MIN} to T_{MAX}		50			50		Hz/kHz
Peak-to-peak amplitude at RT/CT			1.7			1.7		V

† All typical values are at T_J = 25°C.

NOTES: 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

3. Output frequency equals oscillator frequency for the UCx842 and UCx843. Output frequency is one-half oscillator frequency for the UCx844 and UCx845.

error amplifier section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Feedback input voltage	COMP at 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input bias current			–0.3	–1		–0.3	–2	µA
Open-loop voltage amplification	V_O = 2 V to 4 V	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply voltage rejection ratio	V_{CC} = 12 V to 25 V	60	70		60	70		dB
Output sink current	VFB at 2.7 V, COMP at 1.1 V	2	6		2	6		mA
Output source current	VFB at 2.3 V, COMP at 5 V	–0.5	–0.8		–0.5	–0.8		mA
High-level output voltage	VFB at 2.3 V, R_L = 15 kΩ to GND	5	6		5	6		V
Low-level output voltage	VFB at 2.7 V, R_L = 15 kΩ to GND		0.7	1.1		0.7	1.1	V

† All typical values are at T_J = 25°C.

NOTE 2: Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics, V_{CC} = 15 V (see Note 2), R_T = 10 kΩ, C_T = 3.3 nF, T_A = full range (unless otherwise specified) (continued)

current sense section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Voltage amplification	See Notes 4 and 5	2.85	3	3.13	2.85	3	3.15	V/V
Current sense comparator threshold	COMP at 5 V, See Note 4	0.9	1	1.1	0.9	1	1.1	V
Supply voltage rejection ratio	V_{CC} = 12 V to 25 V, See Note 4		70			70		dB
Input bias current			−2	−10		−2	−10	µA
Delay time to output			150	300		150	300	ns

† All typical values are at T_J = 25°C.

NOTES: 2. Adjust V_{CC} above the start threshold before setting it to 15 V.
4. These parameters are measured at the trip point of the latch with VFB at 0 V.
5. Voltage amplification is measured between ISENSE and COMP with the input changing from 0 V to 0.8 V.

output section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
High-level output voltage	I_{OH} = −20 mA	13	13.5		13	13.5		V
	I_{OH} = −200 mA	12	13.5		12	13.5		
Low-level output voltage	I_{OL} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{OL} = 200 mA		1.5	2.2		1.5	2.2	
Rise time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns

† All typical values are at T_J = 25°C.

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

undervoltage lockout section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start threshold voltage	UCx842, UCx844	15	16	17	14.5	16	17.5	V
	UCx843, UCx845	7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after start-up	UCx842, UCx844	9	10	11	8.5	10	11.5	V
	UCx843, UCx845	7	7.6	8.2	7	7.6	8.2	

† All typical values are at T_J = 25°C.

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

pulse-width-modulator section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum duty cycle	UCx842, UCx843	95%	97%	100%	95%	97%	100%	
	UCx844, UCx845	46%	48%	50%	46%	48%	50%	
Minimum duty cycle				0			0	

† All typical values are at T_J = 25°C.

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

supply voltage

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start-up current			0.5	1		0.5	1	mA
Operating supply current	VFB and ISENSE at 0 V		11	17		11	17	mA
Limiting voltage	I_{CC} = 25 mA		34			34		V

† All typical values are at T_J = 25°C.

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics, $V_{CC} = 15$ V (see Note 2), $R_T = 10$ kΩ, $C_T = 3.3$ nF, $T_J = 25°C$ (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 1$ mA		5		V
Line regulation	$V_{CC} = 12$ V to 25 V		6		mV
Load regulation	$I_O = 1$ mA to 20 mA		6		mV
Temperature coefficient of output voltage			0.2		mV√°C
Output noise voltage	f = 10 Hz to 10 kHz		50		µV
Output voltage long-term drift	After 1000 h at $T_A = 25°C$		5		mV
Short-circuit output current			–100		mA

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

oscillator section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Oscillator frequency (see Note 3)			52		kHz
Frequency change with supply voltage	$V_{CC} = 12$ V to 25 V		2		Hz/kHz
Frequency change with temperature			5		Hz/kHz
Peak-to-peak amplitude at RT/CT			1.7		V

NOTES: 2. Adjust V_{CC} above the start threshold before setting it to 15 V.
3. Output frequency equals oscillator frequency for the UCx842 and UCx843. Output frequency is one-half oscillator frequency for the UCx844 and UCx845.

error amplifier section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Feedback input voltage	COMP at 2.5 V		2.50		V
Input bias current			–0.3		µA
Open-loop voltage amplification	$V_O = 2$ V to 4 V		90		dB
Gain-bandwidth product			1		MHz
Supply voltage rejection ratio	$V_{CC} = 12$ V to 25 V		70		dB
Output sink current	VFB at 2.7 V, COMP at 1.1 V		6		mA
Output source current	VFB at 2.3 V, COMP at 5 V		–0.8		mA
High-level output voltage	VFB at 2.3 V, $R_L = 15$ kΩ to GND		6		V
Low-level output voltage	VFB at 2.7 V, $R_L = 15$ kΩ to GND		0.7		V

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

current sense section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Voltage amplification	See Notes 4 and 5		3		V/V
Current sense comparator threshold	COMP at 5 V, See Note 4		1		V
Supply voltage rejection ratio	$V_{CC} = 12$ V to 25 V, See Note 4		70		dB
Input bias current			–2		µA
Delay time to output			150		ns

NOTES: 2. Adjust V_{CC} above the start threshold before setting it to 15 V.
4. These parameters are measured at the trip point of the latch with VFB at 0 V.
5. Voltage amplification is measured between ISENSE and COMP with the input changing from 0 V to 0.8 V.

electrical characteristics, V_{CC} = 15 V (see Note 2), R_T = 10 kΩ, C_T = 3.3 nF, T_J = 25°C (unless otherwise specified) (continued)

output section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
High-level output voltage	I_{OH} = −20 mA		13.5		V
	I_{OH} = −200 mA		13.5		
Low-level output voltage	I_{OL} = 20 mA		0.1		V
	I_{OL} = 200 mA		1.5		
Rise time	C_L = 1 nF		50		ns
Fall time	C_L = 1 nF		50		ns

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

undervoltage lockout section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Start threshold voltage	UC3842Y, UC3844Y		16		V
	UC3843Y, UC3845Y		8.4		
Minimum operating voltage after start-up	UC3842Y, UC3844Y		10		V
	UC3843Y, UC3845Y		7.6		

NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

pulse-width-modulator section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Maximum duty cycle	UC3842Y, UC3843Y		97%		
	UC3844Y, UC3845Y		48%		

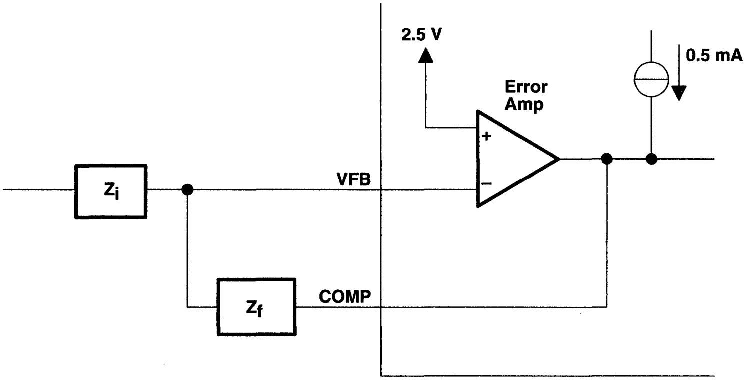
NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

supply voltage

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Start-up current			0.5	1	mA
Operating supply current	VFB and ISENSE at 0 V		11	17	mA
Limiting voltage	I_{CC} = 25 mA		34		V

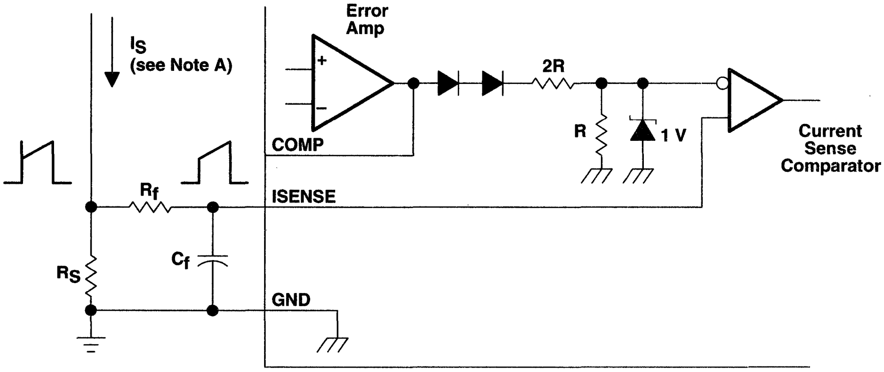
NOTE 2. Adjust V_{CC} above the start threshold before setting it to 15 V.

APPLICATION INFORMATION



NOTE A. Error amplifier can source or sink up to 0.5 mA.

Figure 1. Error Amplifier Configuration



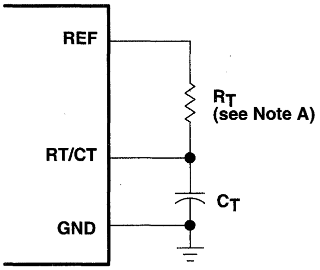
NOTE A: Peak current (I_S) is determined by the formula:

$$I_{S(max)} = \frac{1\ V}{R_S}$$

A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current Sense Circuit

APPLICATION INFORMATION



NOTE A: For $R_T > 5\ \text{K}\Omega$ $f \approx \frac{1.72}{R_T C_T}$

Figure 3. Oscillator Section

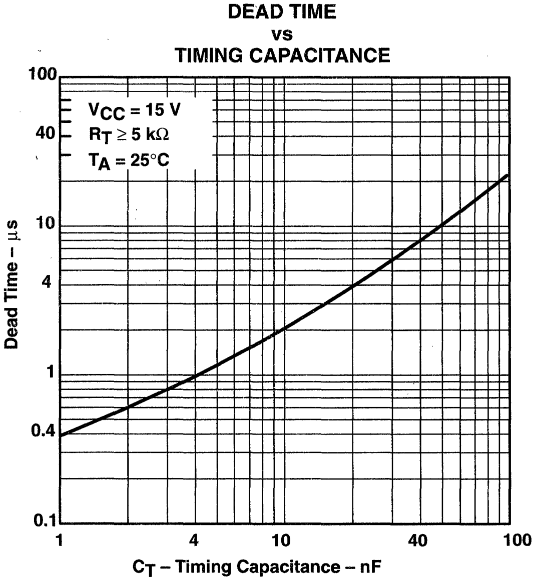


Figure 4

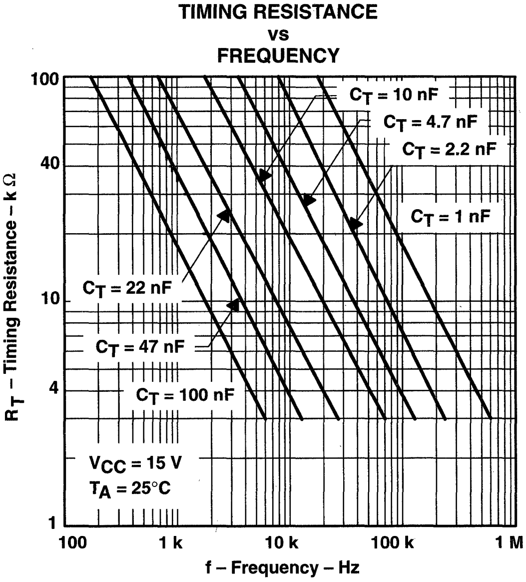


Figure 5

APPLICATION INFORMATION

open-loop laboratory test fixture

In the open-loop laboratory test fixture shown in Figure 6, high-peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

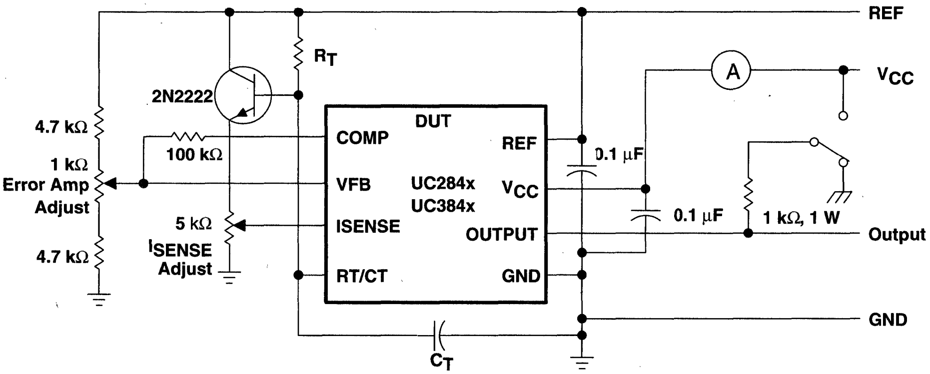


Figure 6. Open-Loop Laboratory Test Fixture

shutdown technique

Shutdown of the PWM controller (see Figure 7) can be accomplished by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

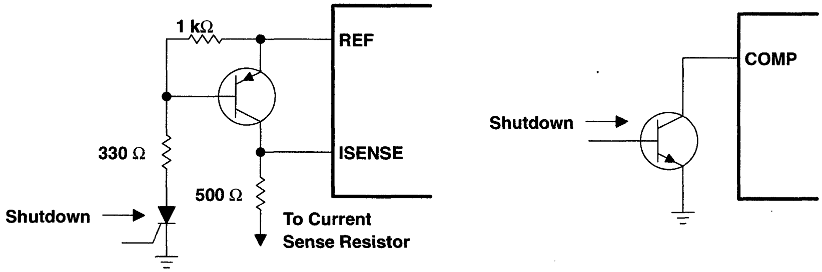


Figure 7. Shutdown Techniques

APPLICATION INFORMATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 8). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

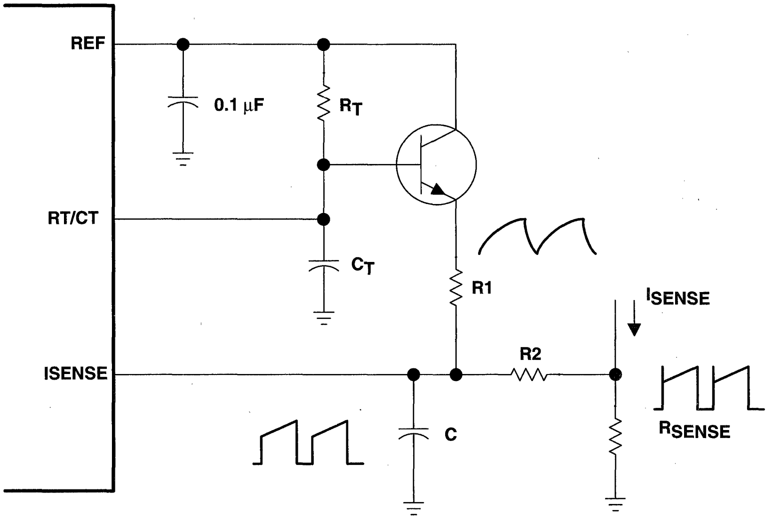


Figure 8. Slope Compensation

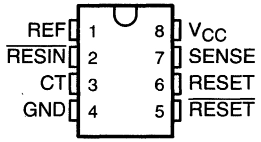
Contents

TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
TL7702AY, TL7705AY, TL7709AY, TL7712AY, TL7715AY
SUPPLY VOLTAGE SUPERVISORS

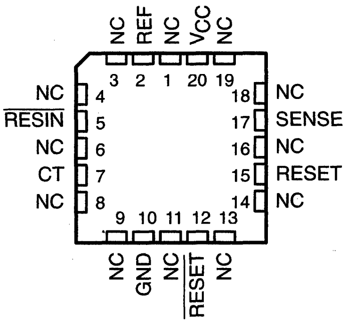
SLVS028C – APRIL 1983 – REVISED AUGUST 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL77xxA family of monolithic integrated circuit supply voltage supervisors are specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down (assuming that SENSE is below V_{IT-}), the outputs remain active until the V_{CC} falls below a maximum of 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1μF for the TL77xxAC and TL77xxAI and typically 0.02μF for the TL77xxAM) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series are characterized for operation from 0°C to 70°C. The TL77xxAI series are characterized for operation from −40°C to 85°C. The TL7702AM and TL7705AM are characterized for operation over the full military range of −55°C to 125°C.

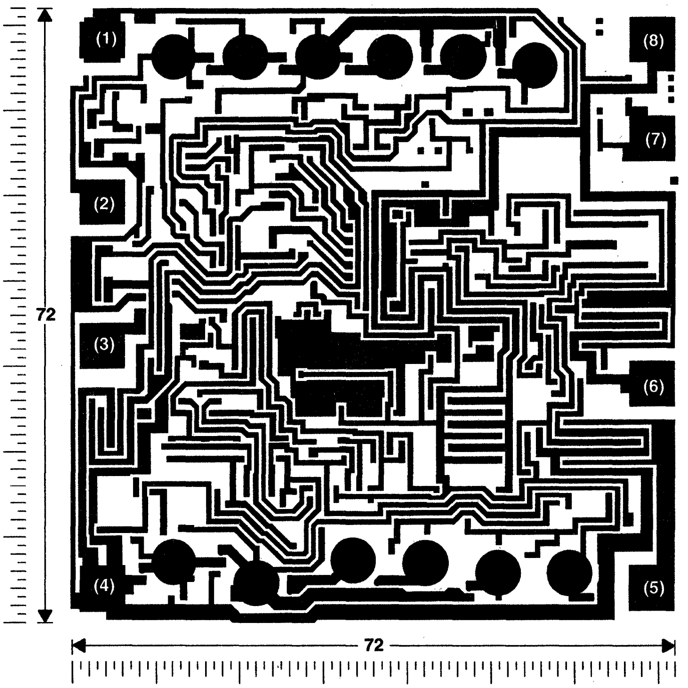
AVAILABLE OPTIONS

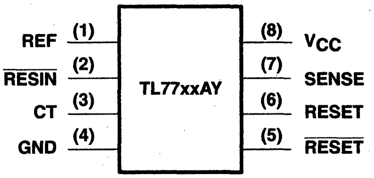
T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	TL7702ACD – TL7715ACD			TL7702ACP – TL7715ACP	TL7702ACY – TL7715ACY
−40°C to 85°C	TL7702AID – TL7715AID			TL7702AIP – TL7715AIP	
−55°C to 125°C		TL7702AMFK TL7705AMFK	TL7702AMJG TL7705AMJG		

TL77xxAY chip information

This chip, when properly assembled, displays characteristics similar to the TL77xxAC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

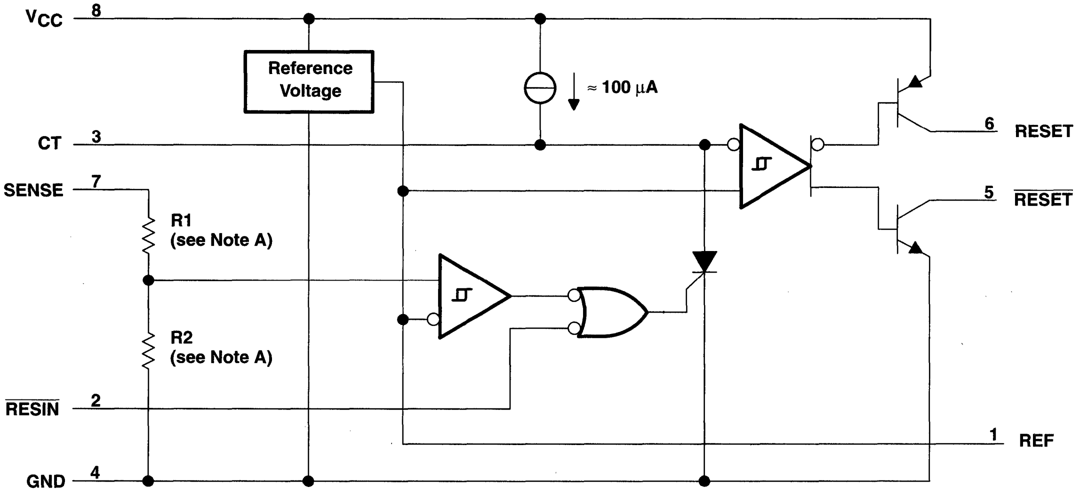
$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

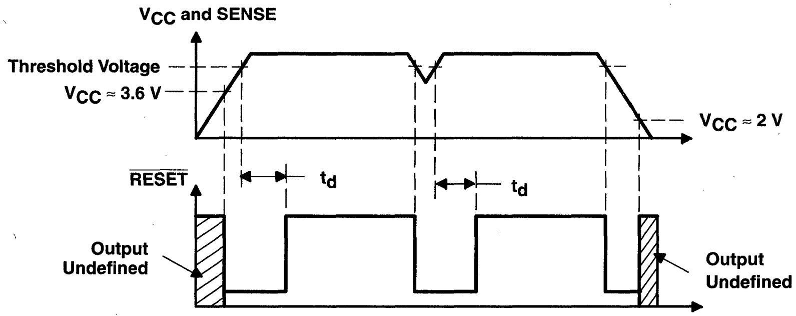
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense comparator trip point.



NOTES: A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
B. Terminal numbers shown are for the D, JG, or P package.
C. Resistor values shown are nominal.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I, $\overline{\text{RESIN}}$	−0.3 V to 20 V
Input voltage range, V_I, SENSE: TL7702A (see Note 2)	−0.3 V to 6 V
TL7705A	−0.3 V to 20 V
TL7709A	−0.3 V to 20 V
TL7712A, TL7715A	−0.3 V to 20 V
High-level output current, I_{OH}, RESET	−30 mA
Low-level output current, I_{OL}, $\overline{\text{RESET}}$	30 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxAC	0°C to 70°C
TL77xxAI	−40°C to 85°C
TL7702AM, TL7705AM	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		TL77xxAC, TL77xxAI		TL77xxAM		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		3.5	18	3.6	10	V
High-level input voltage at $\overline{\text{RESIN}}$, V_{IH}		2		2		V
Low-level input voltage at $\overline{\text{RESIN}}$, V_{IL}			0.6		0.6	V
Input voltage, SENSE, V_I	TL7702A	0	See Note 2	0	See Note 2	V
	TL7705A	0	10	0	10	
	TL7709A	0	15			
	TL7712A	0	20			
	TL7715A	0	20			
High-level output current, RESET, I_{OH}			−16		−16	mA
Low-level output current, $\overline{\text{RESET}}$, I_{OL}			16		16	mA
Timing capacitor, C_T			10		10	µF
Operating free-air temperature range, T_A	TL77xxAC	0	70			°C
	TL77xxAI	−40	85			
	TL7702AM, TL7705AM			−55	125	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC}−1 V or 6 V, whichever is less.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC, TL77xxAI			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		$I_{OH} = -16$ mA	$V_{CC}-1.5$			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		$I_{OL} = 16$ mA			0.4	V
V_{ref}	Reference voltage		$T_A = 25°C$	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A	$T_A = 25°C$	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A	$T_A = 25°C$		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current, $\overline{\text{RESIN}}$		$V_I = 2.4$ V to V_{CC}			20	µA
			$V_I = 0.4$ V			–100	
I_I	Input current, SENSE	TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5	2	µA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		$V_O = 18$ V			50	µA
I_{OL}	Low-level output current, RESET		$V_O = 0$			–50	µA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	TL77xxAC, TL77xxAI			UNIT
			MIN	TYP	MAX	
	Output pulse duration	$C_T = 0.1$ µF	0.65	1.2	2.6	µs
	Input pulse duration at $\overline{\text{RESIN}}$		0.4			µs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs	$V_{IH} = V_{IT-} + 200$ mV, $V_{IL} = V_{IT-} - 200$ mV	2			µs
t_{pd}	Propagation delay time from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	$V_{CC} = 5$ V			1	µs
t_r	RESET	$V_{CC} = 5$ V, See Note 3			0.2	µs
	$\overline{\text{RESET}}$				3.5	
t_f	RESET				3.5	µs
	$\overline{\text{RESET}}$				0.2	

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.

NOTE 3: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL7702AM, TL7705AM			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		$I_{OH} = -16$ mA	$V_{CC}-1.5$			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		$I_{OL} = 16$ mA			0.4	V
V_{ref}	Reference voltage			2.38	2.53	2.63	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702AM	$V_{CC} = 3.6$ V to 10 V	2.38	2.53	2.63	V
		TL7705AM		4.25	4.55	4.7	
V_{hys}	Hysteresis SENSE ($V_{IT+} - V_{IT-}$)	TL7702AM	$V_{CC} = 3.6$ V to 10 V		10		mV
		TL7705AM			15		
I_I	Input current, $\overline{\text{RESIN}}$		$V_I = 2.4$ V to V_{CC}			20	µA
			$V_I = 0.4$ V			−100	
I_I	Input current, SENSE	TL7702AM	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5	2	µA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		$V_O = 10$ V			50	µA
I_{OL}	Low-level output current, RESET		$V_O = 0$			−50	µA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.02-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	TL7702AM, TL7705AM			UNIT
			MIN	TYP	MAX	
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs	$V_{IH} = V_{IT-} + 200$ mV, $V_{IL} = V_{IT-} - 200$ mV	2*			µs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	$V_{CC} = 5$ V		1.5		µs
t_r	RESET	$V_{CC} = 5$ V, See Note 3			0.2*	µs
	$\overline{\text{RESET}}$				3.5*	
t_f	RESET				3.5*	µs
	$\overline{\text{RESET}}$				0.2*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

‡ All switching characteristics are measured with 0.02-µF capacitors connected at REF and V_{CC} to GND.

NOTE 3: The rise and fall times are measured with a 4.7-kΩ load resistor at $\overline{\text{RESET}}$ and RESET.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAY			UNIT
				MIN	TYP	MAX	
V_{ref}	Reference voltage				2.53		V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A			2.53		V
		TL7705A			4.55		
		TL7709A			7.6		
		TL7712A			10.8		
		TL7715A			13.5		
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A			10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current, SENSE	TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5		µA
I_{CC}	Supply current		All inputs and outputs open		1.8		mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL77xxAY			UNIT
		MIN	TYP	MAX	
Output pulse duration	C_T = 0.1 µF		1.2		µs

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.

PARAMETER MEASUREMENT INFORMATION

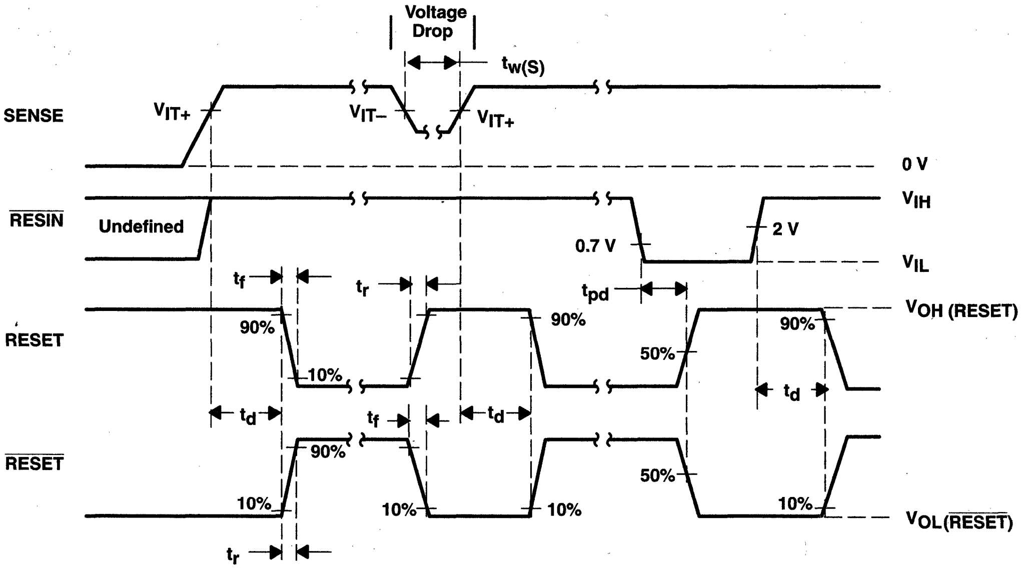


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS†

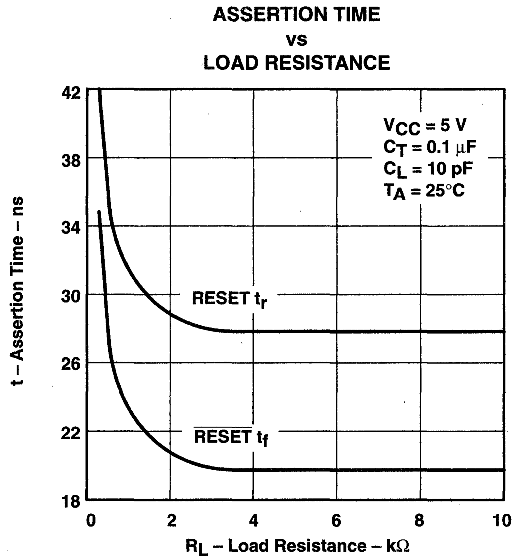


Figure 2

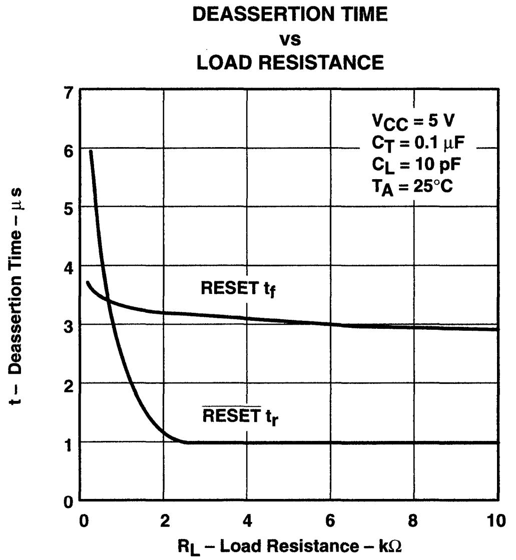


Figure 3

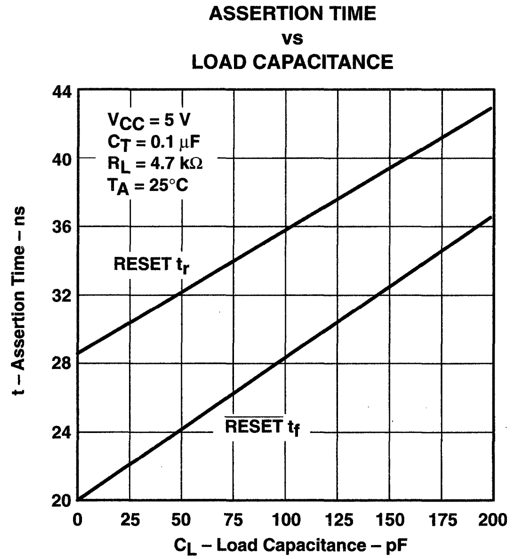


Figure 4

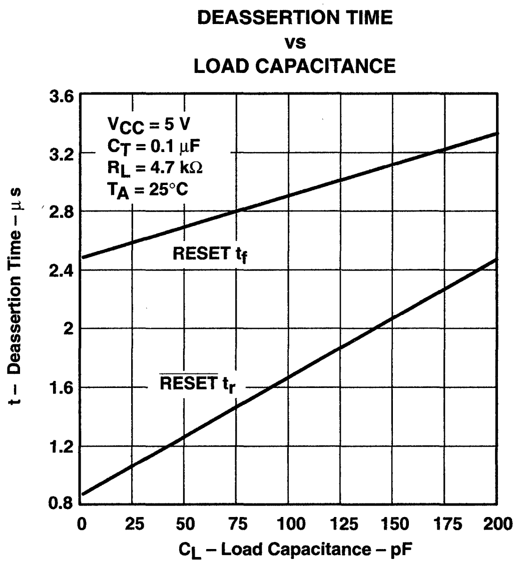


Figure 5

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† For proper operation both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

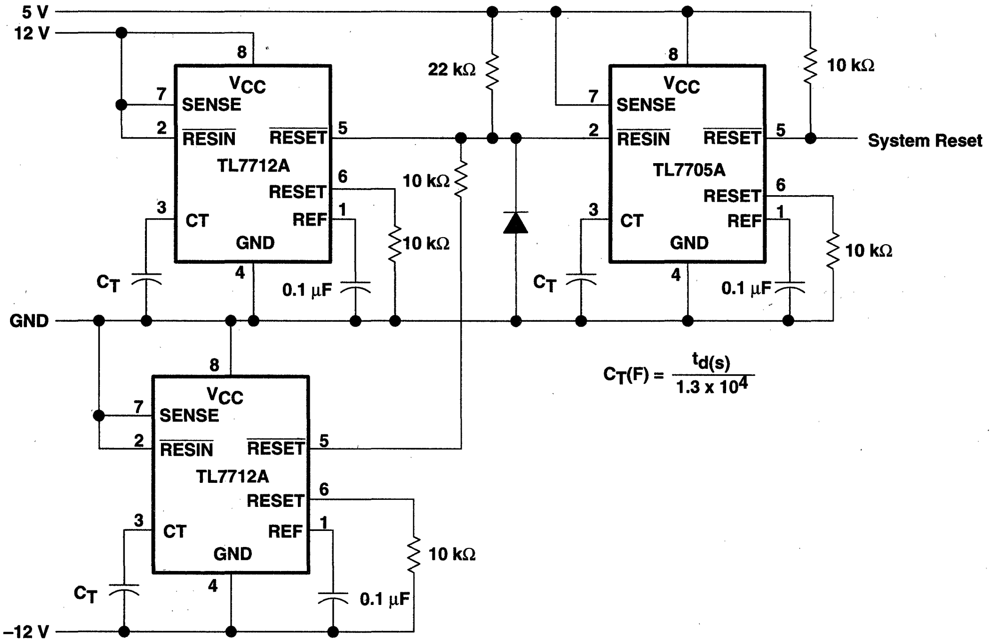


Figure 6. Multiple Power Supply System Reset Generation

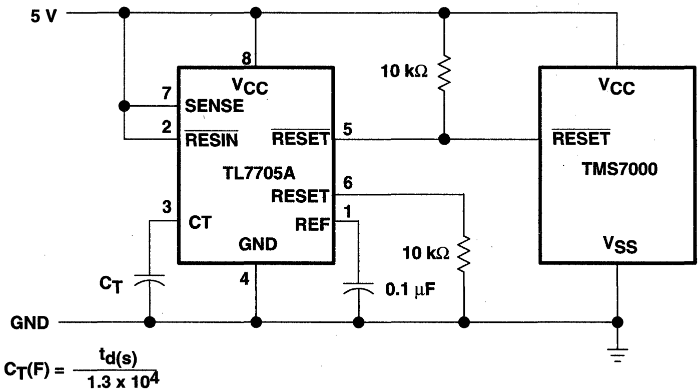


Figure 7. Reset Controller for TMS7000 System

Terminal numbers shown are for the D, JG, and P packages.

APPLICATION INFORMATION

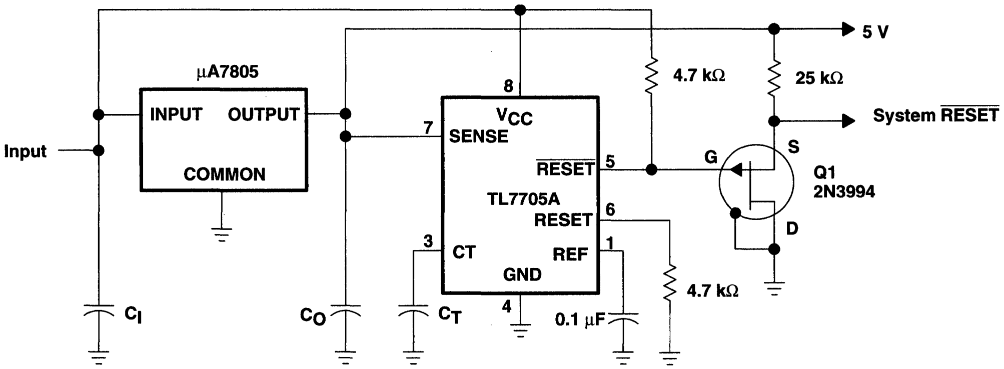


Figure 8. Eliminating Undefined States Using a P-Channel JFET

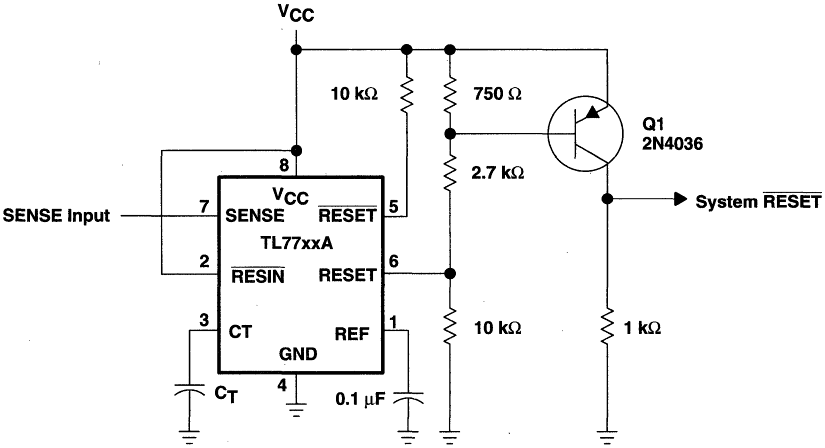


Figure 9. Eliminating Undefined States Using a pnp Transistor

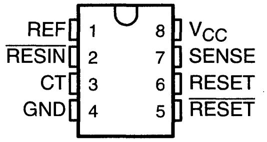
Terminal numbers shown are for the D, JG, and P packages.

TL7702B, TL7705B, TL7702BY, TL7705BY
SUPPLY VOLTAGE SUPERVISORS

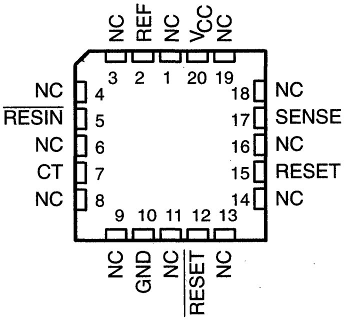
SLVS037D – SEPTEMBER 1989 – REVISED AUGUST 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1$ V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

TL77xxBC . . . P OR D PACKAGE
TL77xxBM . . . JG PACKAGE
(TOP VIEW)



TL77xxBM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7702B and TL7705B are monolithic integrated circuit voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d \approx 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 µF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC and TL7705BC are characterized from 0°C to 70°C. The TL7702BI and TL7705BI are characterized for operation from −40°C to 85°C. The TL7702BQ and TL7705BQ are characterized for operation from −40°C to 125°C. The TL7702BM and TL7705BM are characterized for operation from −55°C to 125°C.

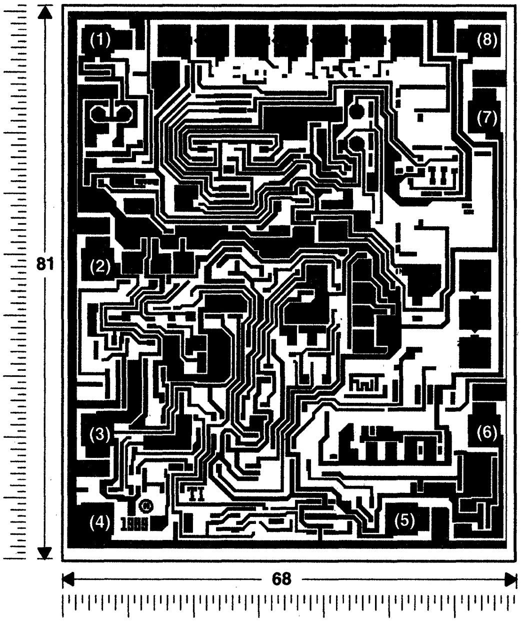
AVAILABLE OPTIONS

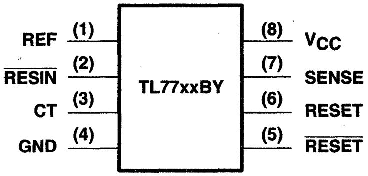
T_A	PACKAGE				CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	TL7702BCD, TL7705BCD	—	—	TL7702BCP, TL7705BCP	TL7702BY TL7705BY
−40°C to 85°C	TL7702BID, TL7705BID	—	—	TL7702BIP, TL7705BIP	
−40°C to 125°C	TL7702BQD, TL7705BQD	—	—	TL7702BQP, TL7705BQP	
−55°C to 125°C	—	TL7702BMFK TL7705BMFK	TL7702BMJG TL7705BMJG	—	

TL7702BY and TL7705BY chip information

These chips, when properly assembled, display characteristics similar to the TL7702BC and the TL7705BC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

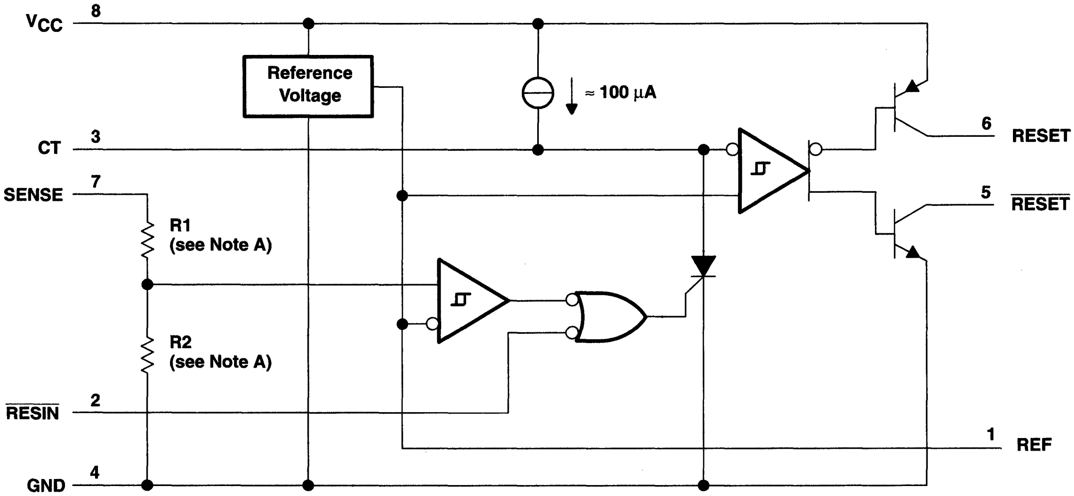
$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

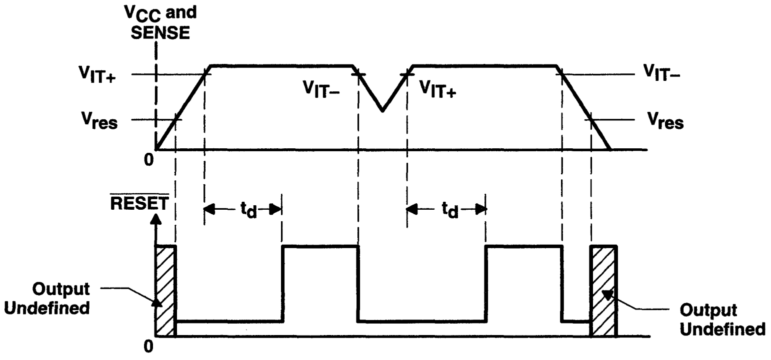
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense comparator trip point.



NOTE A: TL7702B: R1 = 0 Ω, R2 = open
TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I ($\overline{\text{RESIN}}$)	−0.3 V to 20 V
Input voltage range, V_I (SENSE)	−0.3 V to 20 V
High-level output current, I_{OH} ($\overline{\text{RESET}}$)	−30 mA
Low-level output current, I_{OL} ($\overline{\text{RESET}}$)	30 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TL770xBC	0°C to 70°C
TL770xBI	−40°C to 85°C
TL770xBQ	−40°C to 125°C
TL770xBM	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	18	V
High-level input voltage, V_{IH}	$\overline{\text{RESIN}}$	2	18	V
Low-level input voltage, V_{IL}	$\overline{\text{RESIN}}$	0	0.8	V
Input voltage, V_I	SENSE	0	18	V
High-level output current, I_{OH}	RESET		−16	mA
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		16	mA
Timing capacitor, C_T			10	μF
Operating free-air temperature range, T_A	TL770xBC	0	70	°C
	TL770xBI	−40	85	
	TL770xBQ	−40	125	
	TL770xBM	−55	125	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxBC, TL77xxBI TL77xxBQ			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		I_{ref} = 500 μA, T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702B	T_A = 25°C	2.505	2.53	2.555	
		TL7705B		4.5	4.55	4.6	
		TL7702B	T_A = Full range‡	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
V_{hys}	Hysteresis, SENSE (V_{IT+} – V_{IT-})	TL7702B	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
		TL7705B			30		
V_{res}§	Power-up reset voltage		I_{OL} at $\overline{\text{RESET}}$ = 2 mA, T_A = 25°C			1	V
I_I	Input current, $\overline{\text{RESIN}}$		V_I = 0.4 V to V_{CC}			−10	μA
I_I	Input current, SENSE	TL7702B	V_I = V_{ref} to 18 V		−0.1	−2	μA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V, See Figure 1			50	μA
I_{OL}	Low-level output current, RESET		V_O = 0 V, See Figure 1			−50	μA
I_{CC}	Supply current		V_{SENSE} = 15 V, $\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA
			V_{CC} = 18 V T_A = Full range‡			3.5	

† All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V_{CC} to GND.

‡ Full range for the C-suffix device is 0°C to 70°C, full range for the I-suffix is −40°C to 85°C, and full range for the Q-suffix device is −40°C to 125°C.

§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC, TL77xxBI TL77xxBQ			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2		150		ns
		SENSE		See Figure 2		100		
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		RESET			75	150	ns
t_f	Fall time						50	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL7702BM, TL7705BM			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		$I_{OH} = -16$ mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		$I_{OL} = 16$ mA			0.4	V
V_{ref}	Reference voltage		$I_{ref} = 500$ µA, $T_A = 25°C$	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	$T_A = 25°C$	2.505	2.53	2.555	
		TL7705B		4.5	4.55	4.6	
		TL7702B	T_A = Full range‡	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702B	$V_{CC} = 3.6$ V to 18 V, $T_A = 25°C$		10		mV
		TL7705B			30		
V_{res}§	Power-up reset voltage		I_{OL} at $\overline{\text{RESET}}$ = 2 mA, $T_A = 25°C$			1	V
I_I	Input current, $\overline{\text{RESIN}}$		$V_I = 0.4$ V to V_{CC}			−10	µA
I_I	Input current, SENSE	TL7702B	$V_I = V_{ref}$ to $V_{CC} - 1.5$ V		−0.1	−2	µA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		$V_O = 18$ V			50	µA
I_{OL}	Low-level output current, RESET		$V_O = 0$			−50	µA
I_{CC}	Supply current		$V_{SENSE} = 15$ V, $\overline{\text{RESIN}} \geq 2$ V		1.8	3	mA
			$V_{CC} = 18$ V T_A = Full range‡			4	

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
‡ Full range for the M-suffix device is −55°C to 125°C.
§ This is the lowest value at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, $V_{CC} = 5$ V, CT open, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7702BM, TL7705BM			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500*	ns
t_{PHL}	Propagation delay time from high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500*	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2		150		ns
		SENSE		See Figure 2		100		
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3			75*	ns
t_f	Fall time					150	200*	
t_r	Rise time		RESET			75	150*	ns
t_f	Fall time						50*	

*For products compliant to MIL-STD-883, Class B, these parameters are not production tested.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

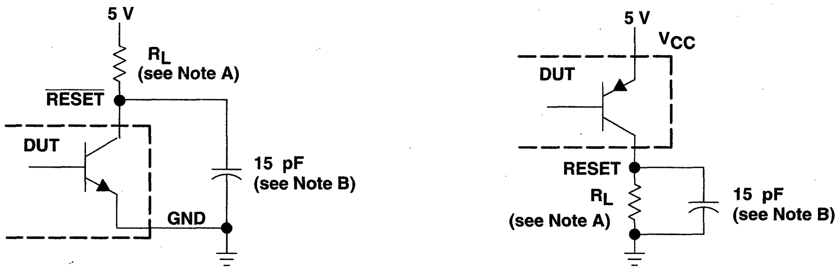
PARAMETER			TEST CONDITIONS†	TL7702Y, TL7705Y			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		I_{ref} = 500 μA	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702Y		2.505	2.53	2.555	
		TL7705Y		4.5	4.55	4.6	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702Y	V_{CC} = 3.6 V to 18 V		10		mV
		TL7705Y			30		
V_{res}‡	Power-up reset voltage		I_{OL} at $\overline{\text{RESET}}$ = 2 mA			1	V
I_I	Input current, $\overline{\text{RESIN}}$		V_I = 0.4 V to V_{CC}			−10	μA
I_I	Input current, SENSE	TL7702Y	V_I = V_{ref} to 18 V		−0.1	−2	μA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V, See Figure 1			50	μA
I_{OL}	Low-level output current, RESET		V_O = 0 V, See Figure 1			−50	μA
I_{CC}	Supply current		V_{SENSE} = 15 V, $\overline{\text{RESIN}}$ ≥ 2 V		1.8	3	mA

† All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V_{CC} to GND.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7702Y, TL7705Y			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2		150		ns
		SENSE		See Figure 2		100		
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 1 and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		RESET			75	150	ns
t_f	Fall time						50	

PARAMETER MEASUREMENT INFORMATION



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

RESET OUTPUT CONFIGURATION

NOTES: A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

WAVEFORMS

Figure 2. Input Pulse Definition

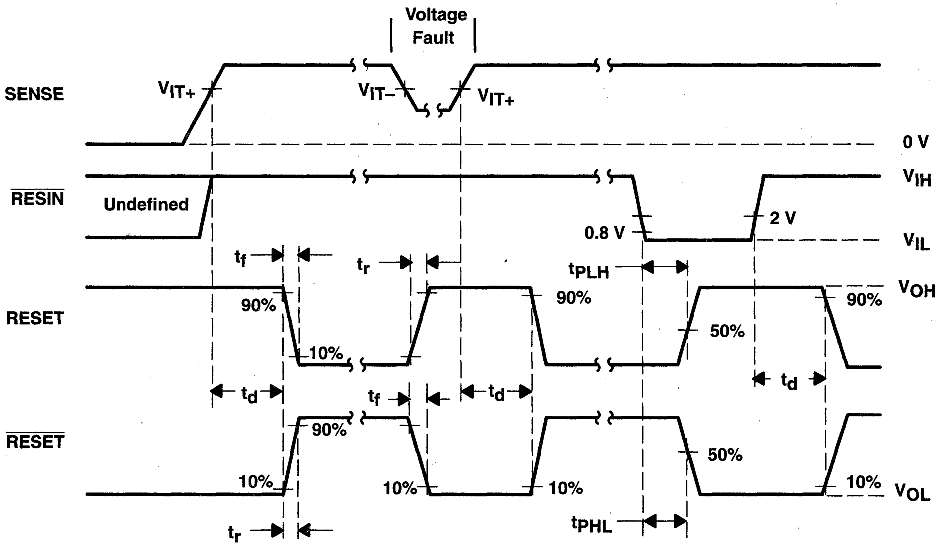


Figure 3. Voltage Waveforms

TYPICAL CHARACTERISTICS†

ASSERTION TIME
vs
LOAD RESISTANCE

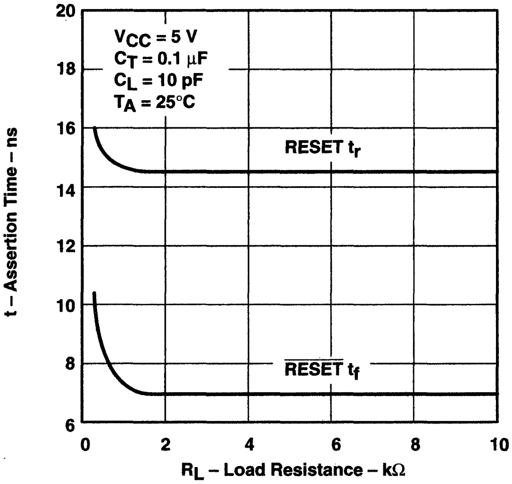


Figure 4

DEASSERTION TIME
vs
LOAD RESISTANCE

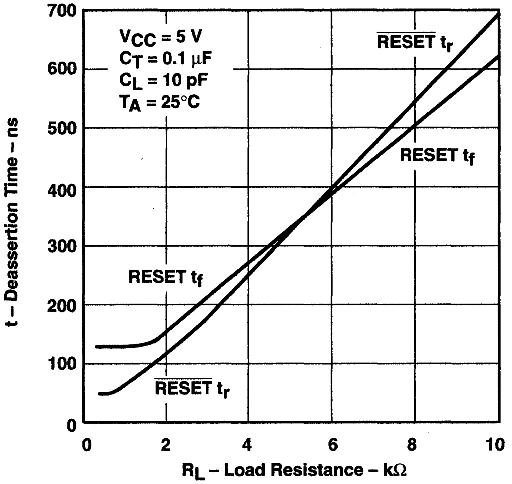


Figure 5

ASSERTION TIME
vs
LOAD CAPACITANCE

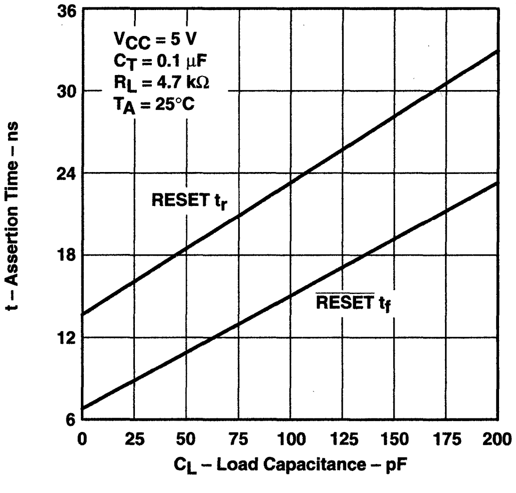


Figure 6

DEASSERTION TIME
vs
LOAD CAPACITANCE

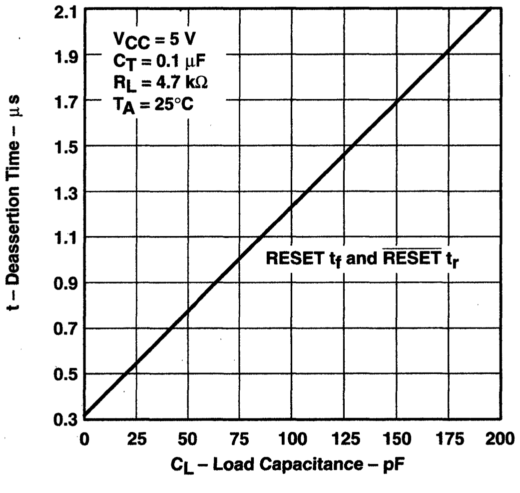


Figure 7

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† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

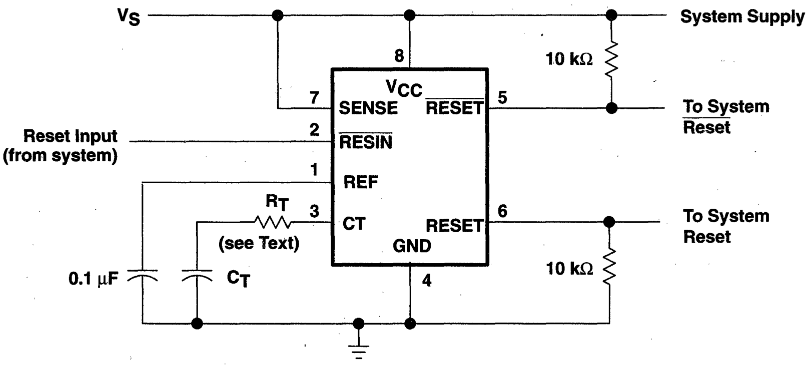


Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the on-board current source to approximately V_{CC} or an internal voltage clamp (≈7.1-V zener), whichever is less. When the circuit is then subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-}.

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T} < 1\text{ mA}$$

where:

$V_{(CT)}$ = V_{CC} or 7.1 V, whichever is less
V_{T-} = 4.55 V (nom)
R_T = value of series resistor required

for $V_{CC} = 5$ V:

$$\frac{5 - 4.55}{R_T} < 1\text{ mA}$$

Therefore,

$R_T > 450\ \Omega$

Using a 20% tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply voltage fault condition.

Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

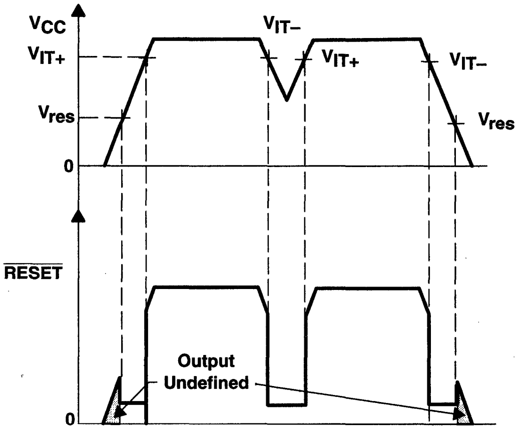
TL7757, TL7757Y
SUPPLY VOLTAGE SUPERVISOR AND PRECISION VOLTAGE DETECTOR

SLVS041D – SEPTEMBER 1991 – REVISED AUGUST 1995

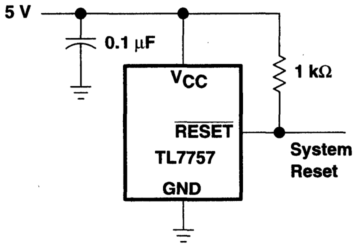
available features

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Low Standby Current . . . 20 μA
- Reset Output Defined When V_{CC} Exceeds 1 V
- Complementary Reset Output
- Precision Threshold Voltage 4.55 V ±120 mV
- High Output Sink Capability . . . 20 mA
- Comparator Hysteresis Prevents Erratic Resets

TYPICAL TIMING DIAGRAM



TYPICAL APPLICATION DIAGRAM



description

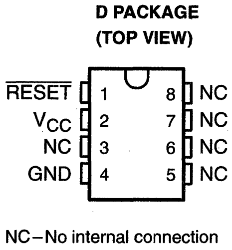
The TL7757 is a monolithic supply voltage supervisor designed for use in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the $\overline{RESET}$ output becomes active (low) to prevent undefined operation. If at any time, the supply voltage drops below threshold voltage level (V_{IT-}), the $\overline{RESET}$ output goes to the active (low) level until the supply undervoltage fault condition is eliminated.

The C-suffix device is characterized for operation from 0°C to 70°C. The I-suffix device is characterized for operation from −40°C to 85°C. The M-suffix device is characterized for operation from −55°C to 125°C.

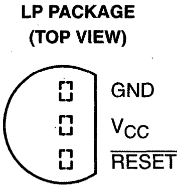
AVAILABLE OPTIONS

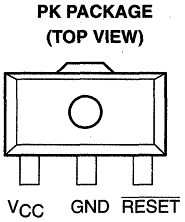
T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	TO-226AA (LP)	SOT-89 (PK)	
0°C to 70°C	TL7757CD	TL7757CLP	TL7757CPK	TL7757Y
−40°C to 85°C	TL7757ID	TL7757ILP	TL7757IPK	
−55°C to 125°C	TL7757MD	TL7757MLP	—	

D and LP packages are available taped and reeled. Add R suffix to device type (e.g., TL7757CDR). Chips are tested at 25°C.



NC–No internal connection

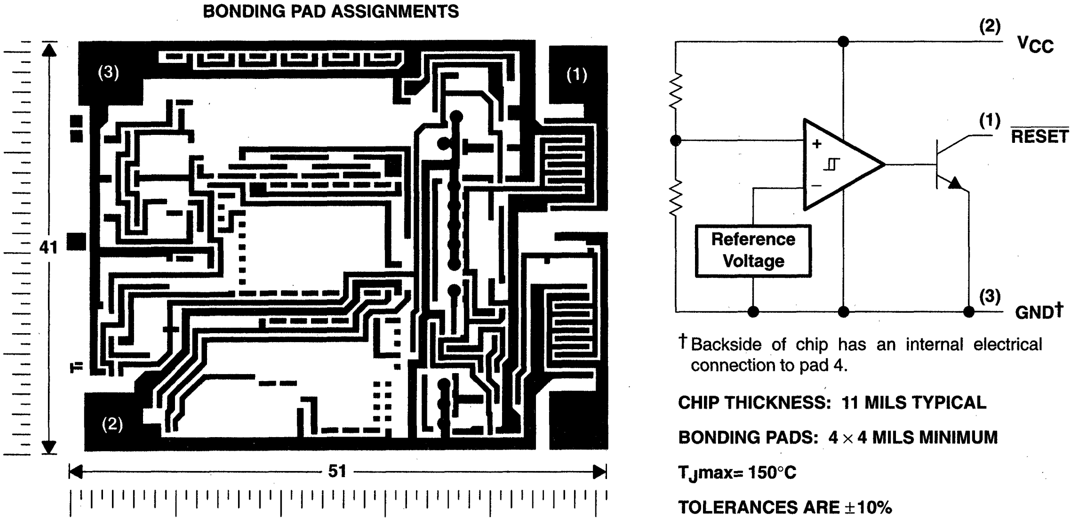




GND is in electrical contact with the tab.

TL7757Y chip information

This chip, when properly assembled, displays characteristics similar to the TL7757C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



† Backside of chip has an internal electrical connection to pad 4.

CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

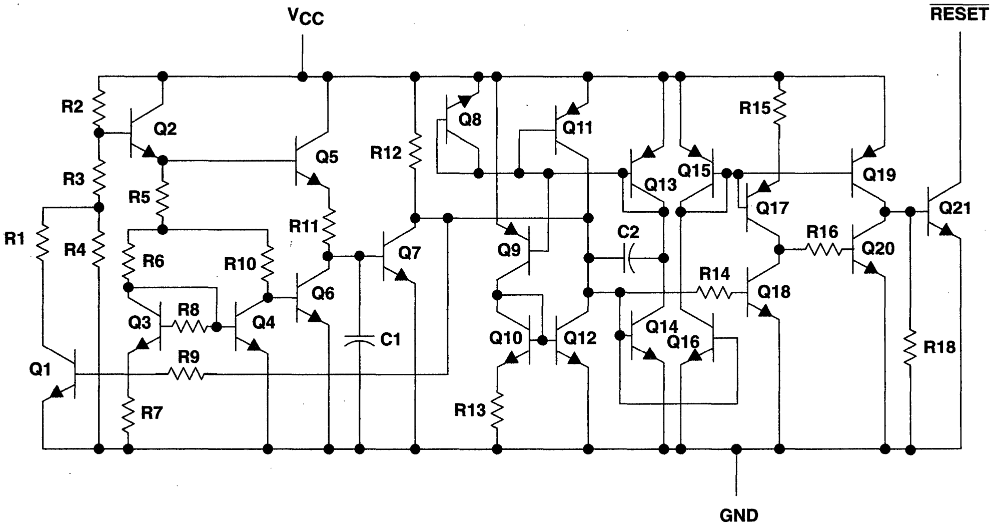
$T_J$max= 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALIZATION

equivalent schematic



ACTUAL DEVICE COMPONENT COUNT	
Transistors	27
Resistors	20
Capacitors	2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 20 V
Offstate output voltage range (see Note 1)	−0.3 V to 20 V
Output current, I_O	30 mA
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Continuous total power dissipation	See Dissipation Rating Tables
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE	$T_A = 70°C$	$T_A = 85°C$	$T_A = 125°C$
D	725 mW	5.8 mW/°C	$T_A = 25°C$	464 mW	377 mW	145 mW
LP	775 mW	6.2 mW/°C	$T_A = 25°C$	496 mW	403 mW	155 mW
PK	500 mW	4.0 mW/°C	$T_A = 25°C$	320 mW	260 mW	—

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE	$T_A = 70°C$	$T_A = 85°C$
PK	3125 mW	25 mW/°C	$T_C = 110°C$	2000 mW	1625 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	1	7	1	7	1	7	V
High-level output voltage, V_{OH}		15		15		15	V
Low-level output current, I_{OL}		20		20		20	mA
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TL7757C MIN	TL7757C TYP	TL7757C MAX	UNIT
V_{IT-}	Negative-going input threshold voltage at V_{CC}		25°C	4.43	4.55	4.67	V
			Full range	4.4		4.7	
V_{hys}‡	Hysteresis at V_{CC}		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.4	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1	25°C			1	µA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/µs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	µA
			Full range			2000	
		V_{CC} = 5.5 V	Full range			40	

† Full range is 0°C to 70°C.

‡ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL7757C MIN	TL7757C TYP	TL7757C MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		3.4	5	µs
			Full range			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	µs
			Full range			5	
t_r	Rise time	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		0.4	1	µs
			Full range			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	µs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C			5	µs
			Full range			5	

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TL7757I			UNIT
				MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}		25°C	4.43	4.55	4.67	V
			Full range	4.4		4.7	
V_{hys}‡	Hysteresis at V_{CC}		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.4	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1	25°C			1	µA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/µs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	µA
			Full range			2100	
		V_{CC} = 5.5 V	Full range			40	

† Full range is –40°C to 85°C.
‡ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL7757I			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		3.4	5	µs
			Full range			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	µs
			Full range			5	
t_r	Rise time	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		0.4	1	µs
			Full range			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	µs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C			5	µs
			Full range			5	

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TL7757M MIN	TL7757M TYP	TL7757M MAX	UNIT
V_{IT-}	Negative-going input threshold voltage at V_{CC}		25°C	4.43	4.55	4.67	V
			Full range	4.35		4.7	
V_{hys}‡	Hysteresis at V_{CC}		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.4	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1	25°C			1	μA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	μA
			Full range			2500	
		V_{CC} = 5.5 V	Full range			40	

† Full range is –55°C to 125°C.
‡ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL7757M MIN	TL7757M TYP	TL7757M MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		3.4	5*	μs
			Full range			5*	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5*	μs
			Full range			5*	
t_r	Rise time	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		0.4	1*	μs
			Full range			1*	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1*	μs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C			5*	μs
			Full range			5*	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is –55°C to 125°C.

electrical characteristics at T_A = 25°C

PARAMETER		TEST CONDITIONS	TL7757Y			UNIT
			MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}			4.55		V
V_{hys}†	Hysteresis at V_{CC}			50		mV
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V		0.4		V
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1				μA
V_{res}‡	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/μs		0.8		V
I_{CC}	Supply current	V_{CC} = 4.3 V		1400		μA
		V_{CC} = 5.5 V				

† This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at T_A = 25°C

PARAMETER		TEST CONDITIONS	TL7757Y			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3		3.4		μs
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3,		2		μs
t_r	Rise time	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3		0.4		μs
t_f	Fall time	See Figures 2 and 3		0.05		μs

PARAMETER MEASUREMENT INFORMATION

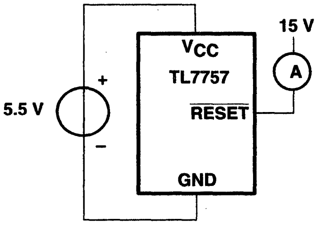
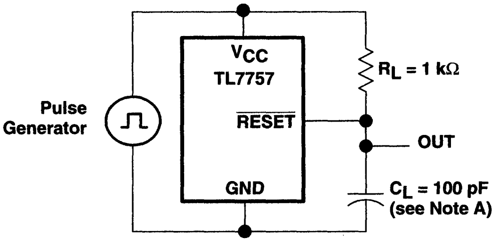
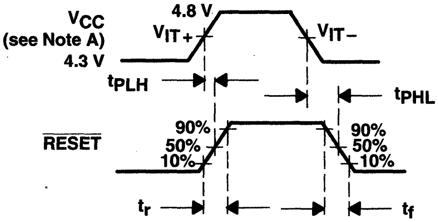


Figure 1. Test Circuit for Output Leakage Current



NOTE A: Includes jig and probe capacitance.

Figure 2. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics



NOTE A: V_{CC} slew rate ≤ 5 μs

Figure 3. Switching Diagram

TYPICAL CHARACTERISTICS†

table of graphs

			FIGURE
V_{CC}	Supply voltage	vs $\overline{RESET}$ output voltage	4
I_{CC}	Supply current	vs Supply voltage	5
		vs Free-air temperature	6
V_{OL}	Low-level output voltage	vs Low-level output current	7
		vs Free-air temperature	8
I_{OL}	Output current	vs Supply voltage	9
V_{IT-}	Input threshold voltage (negative-going V_{CC})	vs Free-air temperature	10
V_{res}	Power-up reset voltage	vs Free-air temperature	11
V_{res}	Power-up reset voltage and supply voltage	vs Time	12
	Propagation delay time		13

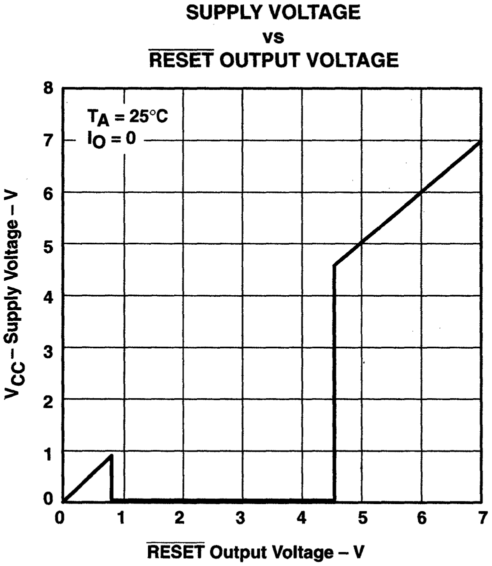


Figure 4

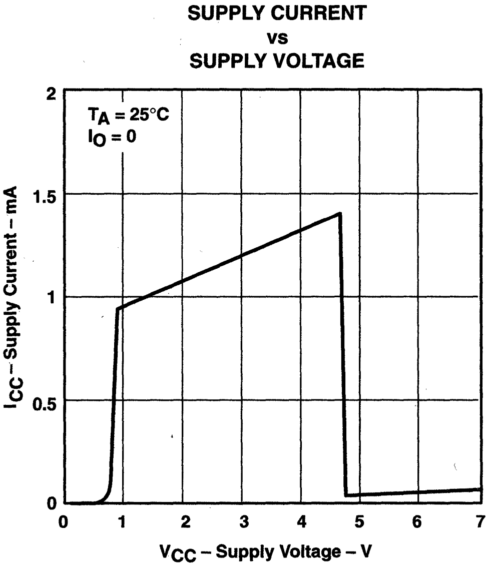


Figure 5

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

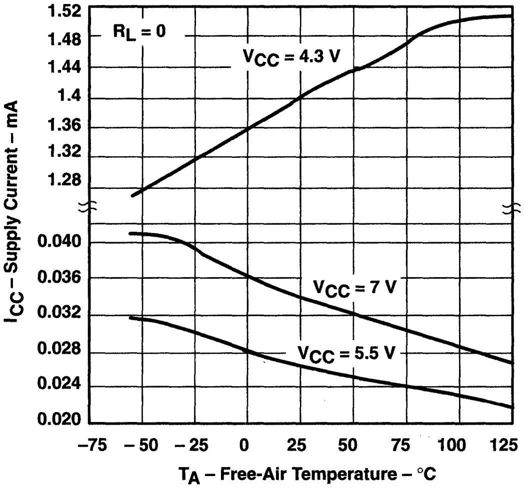

Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

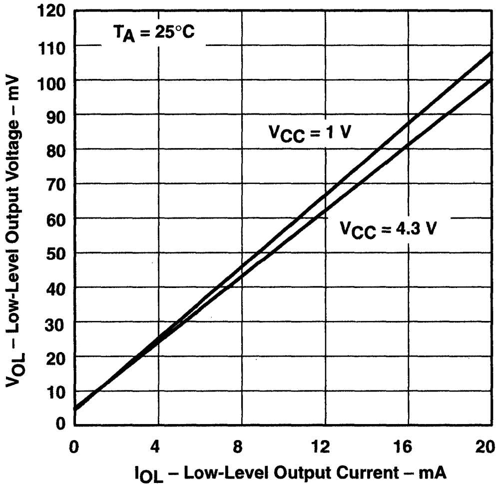

Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

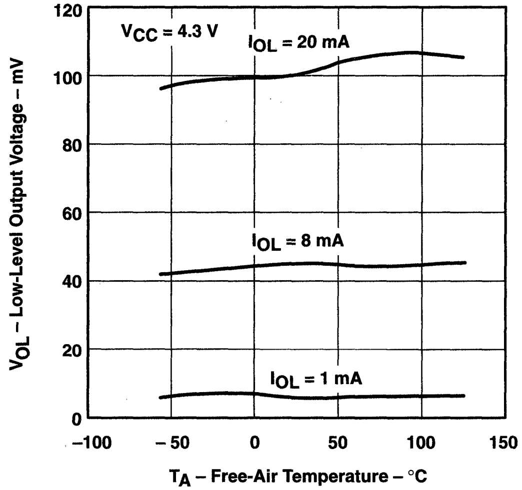

Figure 8

OUTPUT CURRENT
vs
SUPPLY VOLTAGE

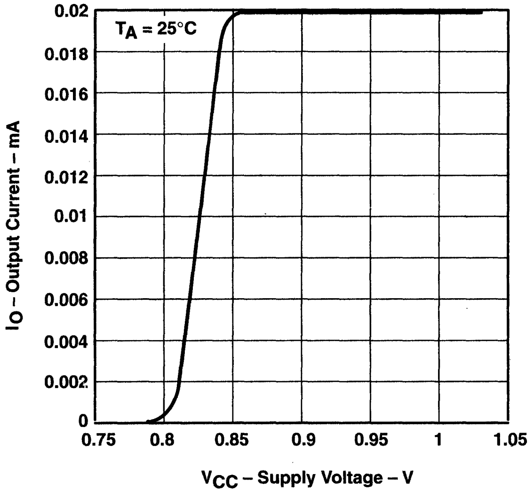

Figure 9

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE (NEGATIVE GOING V_{CC}) vs FREE-AIR TEMPERATURE

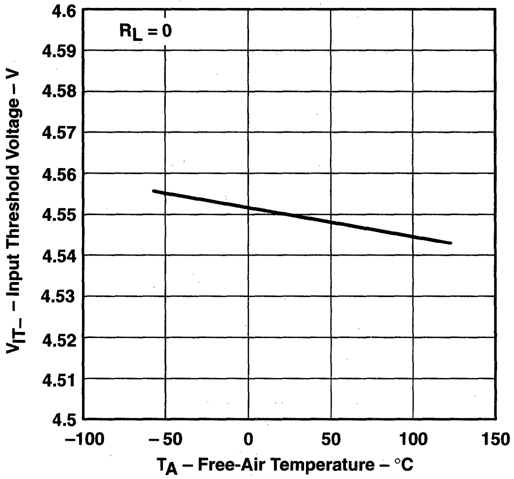

Figure 10

POWER-UP RESET VOLTAGE vs FREE-AIR TEMPERATURE

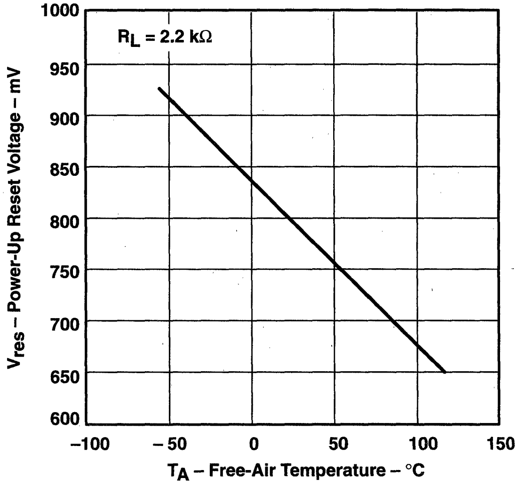

Figure 11

POWER-UP RESET VOLTAGE AND SUPPLY VOLTAGE vs TIME

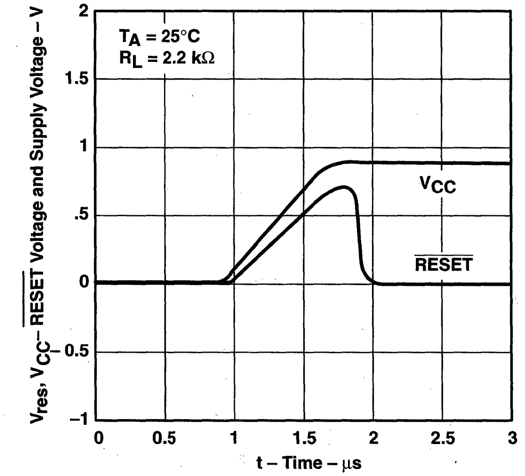

Figure 12

PROPAGATION DELAY TIME

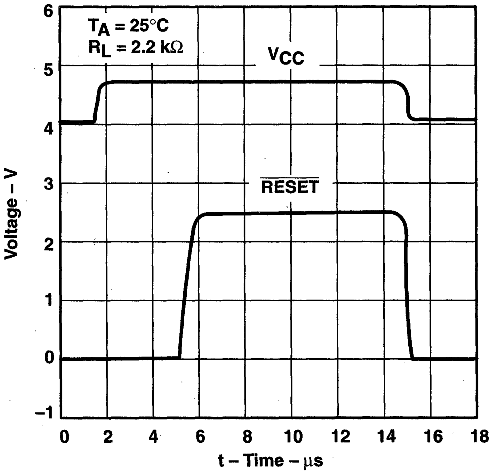

Figure 13

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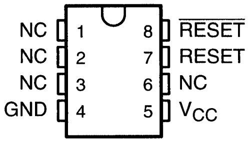
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TL7759, TL7759Y
SUPPLY VOLTAGE SUPERVISORS

SLVS042B – JANUARY 1991 – REVISED AUGUST 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Input Threshold Voltage 4.55 V ±120 mV**
- **Low Standby Current . . . 20 μA**
- **Reset Outputs Defined When V_{CC} Exceeds 1 V**
- **True and Complementary Reset Outputs**
- **Wide Operating Temperature Range 0°C to 70°C**
- **Wide Supply Voltage Range . . . 1 V to 7 V**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7759C is a monolithic supply voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power-up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. If at any time the supply voltage drops below the input threshold voltage level (V_{IT-}), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value.

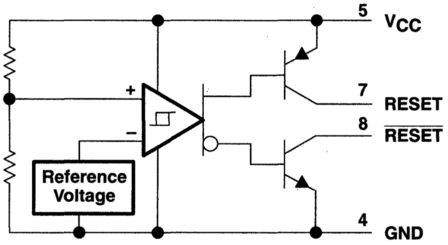
The TL7759C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

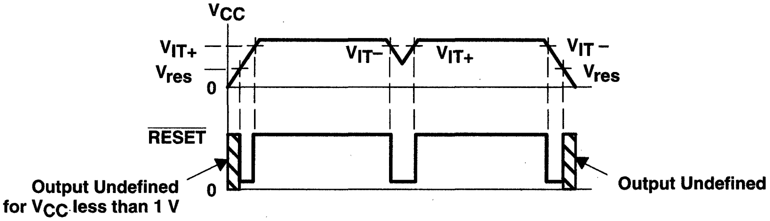
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	2.5 mV	TL7759CD	TLC7759CP	TL7759Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TL7759CDR). Chips are tested at 25°C.

functional block diagram



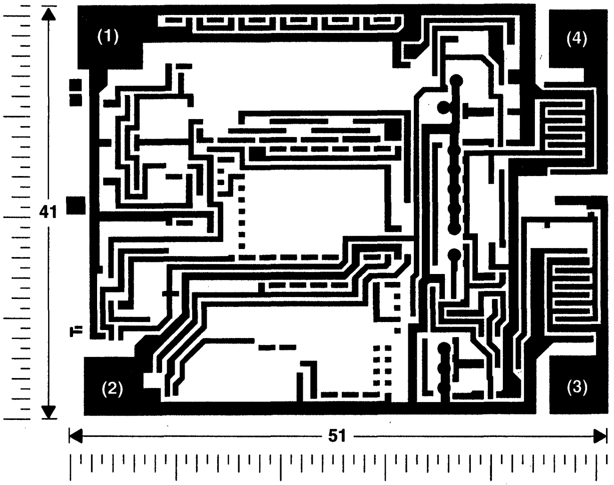
timing diagram

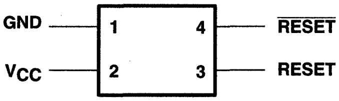


TL7759Y chip information

This chip, when properly assembled, displays characteristics similar to the TL7759C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

TERMINALS 1, 2, 3, AND 6 ARE NOT CONNECTED.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Off-state output voltage range: $\overline{\text{RESET}}$ voltage	−0.3 V to 20 V
RESET voltage	−0.3 V to 20 V
Low-level output current, I_{OL} ($\overline{\text{RESET}}$)	30 mA
High-level output current, I_{OH} (RESET)	−10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
Output voltage, V_O (see Note 2)	Transistor off $\overline{\text{RESET}}$ voltage		15	V
	Transistor off RESET voltage	0		
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		24	mA
High-level output current, I_{OH}	RESET		−8	
Operating free-air temperature, T_A		0	70	°C

NOTE 2: RESET output must not be pulled down below GND potential.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759C			UNIT
					MIN	TYP[†]	MAX	
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4	0.8	V
V_{OH}	High-level output voltage	RESET		I_{OH} = −8 mA	V_{CC}−1			
V_{IT-}	Input threshold voltage (negative-going V_{CC})		T_A = 25°C		4.43	4.55	4.67	V
			T_A = 0°C to 70°C		4.4		4.7	
V_{res}[‡]	Power-up reset voltage		R_L = 2.2 kΩ	T_A = 25°C		0.8	1	V
				T_A = 0°C to 70°C			1.2	
V_{hys}[§]	Hysteresis at V_{CC} input		T_A = 25°C		40	50	60	mV
			T_A = 0°C to 70°C		30		70	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_{CC} = 7 V, See Figure 1	V_{OH} = 15 V			1	µA
I_{OL}	Low-level output current	RESET		V_{OL} = 0 V			−1	
I_{CC}	Supply current		No load	V_{CC} = 4.3 V		1400	2000	µA
				V_{CC} = 5.5 V			40	

[†] Typical values are at T_A = 25°C.
[‡] This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≥ 5 V/µs.
[§] This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7759C		UNIT
					MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC}	RESET	See Figures 2 and 3[†]		5	µs
t_{PHL}	Propagation delay time, high-to-low-level output	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4		5	
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 2 and 4[†]		1	µs
t_f	Fall time		$\overline{\text{RESET}}$	See Figures 2 and 4		1	µs
$t_{w(min)}$	Minimum pulse duration	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4	5		µs

[†] V_{CC} slew rate > 5 V/µs.

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759Y			UNIT
					MIN	TYP	MAX	
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4		V
V_{IT-}	Input threshold voltage (negative-going V_{CC})					4.55		V
V_{res}[†]	Power-up reset voltage		R_L = 2.2 kΩ			0.8		V
V_{hys}[‡]	Hysteresis at V_{CC} input					50		mV
I_{CC}	Supply current		V_{CC} = 4.3 V,	No load		1400		µA

[†] This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≥ 5 V/µs.
[‡] This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

PARAMETER MEASUREMENT INFORMATION

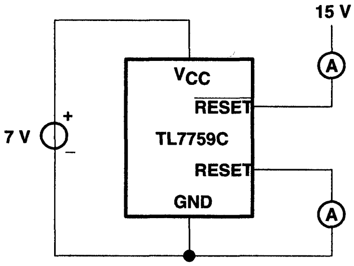
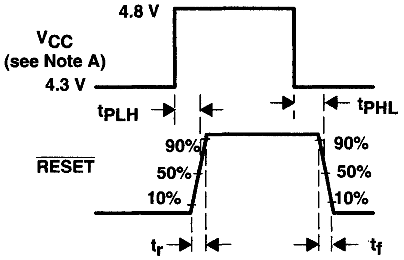
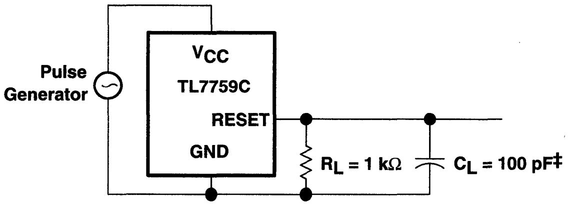


Figure 1. Test Circuit for Output Leakage Current



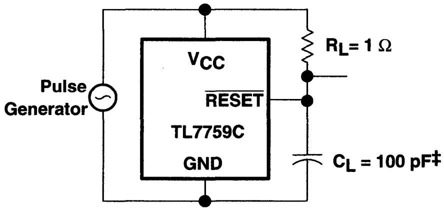
NOTE A: V_{CC} slew rate > 5 V/µs.

Figure 2. Switching Diagram



‡C_L Includes jig and probe capacitance.

Figure 3. Test Circuit for RESET Output Switching Characteristics



‡C_L Includes jig and probe capacitance.

Figure 4. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics

APPLICATION INFORMATION

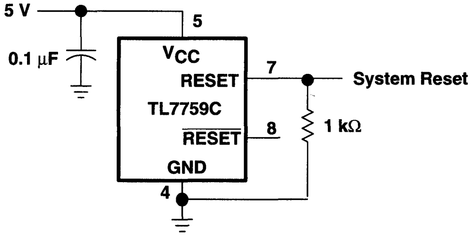


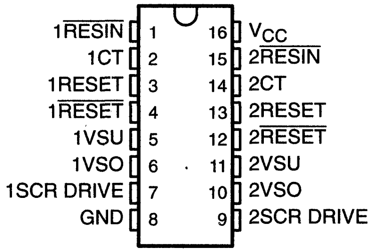
Figure 5. Power Supply System Reset Generation

TL7770-5, TL7770-12, TL7770-15
TL7770-5Y, TL7770-12Y, TL7770-15Y
DUAL POWER-SUPPLY SUPERVISORS

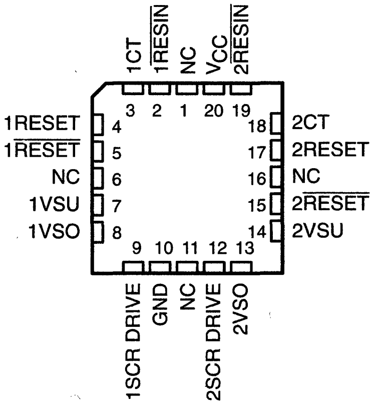
SLVS019D – OCTOBER 1987 – REVISED OCTOBER 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **Wide Supply Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL7770 is a monolithic integrated circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU terminals respectively. When V_{CC} attains the minimum voltage of 1 V during power-up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the delay timer function activates latching RESET and $\overline{\text{RESET}}$ active (high and low, respectively) for a time delay, t_d, after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low activates the time delay function, RESET and $\overline{\text{RESET}}$, during normal system voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value V_{IT+} for a time delay, t_d, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

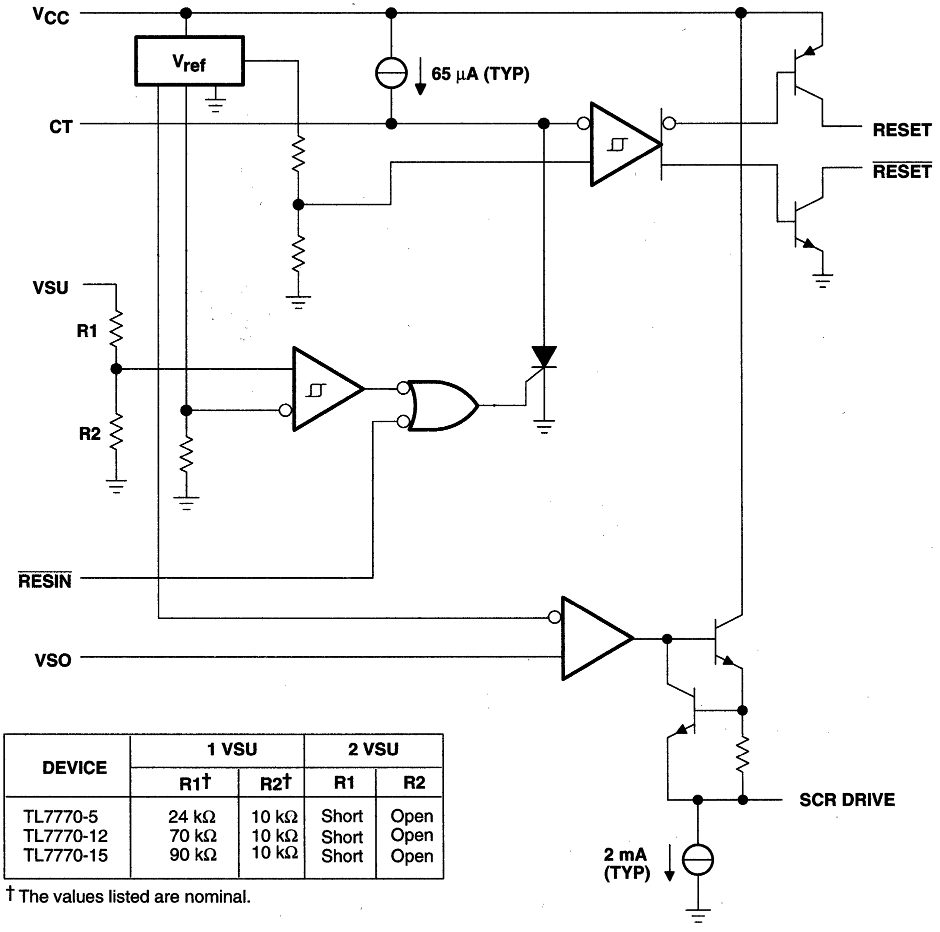
The overvoltage-detection circuit is programmable for a wide range of user designs. During an overvoltage condition, an internal silicon-controlled rectifier (SCR) is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive terminal, which can drive an external high-current SCR gate or an overvoltage warning circuit.

The TL7770C is characterized for operation from 0°C to 70°C. The TL7770M series is characterized for operation from – 55°C to 125°C. The TL7770Q series is characterized for operation from – 40°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	TL7770-5CDW	—	—	TL7770-5CN	TL7770-5Y
	TL7770-12CDW	—	—	TL7770-12CN	TL7770-12Y
	TL7770-15CDW	—	—	TL7770-15CN	TL7770-15Y
–40°C to 125°C	TL7770-5QDW	—	—	TL7770-5QN	—
	TL7770-12QDW	—	—	TL7770-12QN	—
	TL7770-15QDW	—	—	TL7770-15QN	—
–55°C to 125°C	—	TL7770-5MFK	TL7770-5MJ	—	—
	—	TL7770-12MFK	TL7770-12MJ	—	—
	—	TL7770-15MFK	TL7770-15MJ	—	—

functional block diagram (each channel)



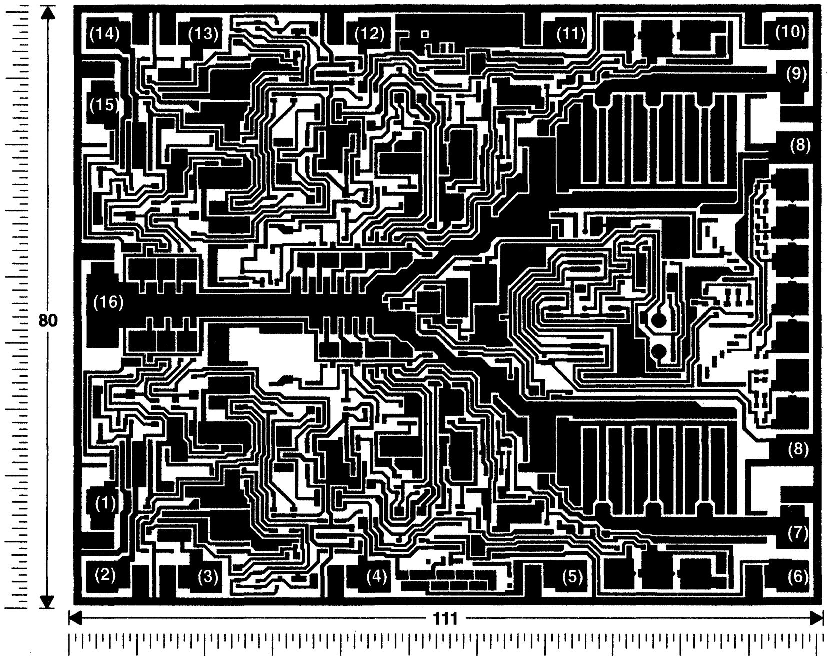
DEVICE	1 VSU		2 VSU	
	R1†	R2†	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open
TL7770-15	90 kΩ	10 kΩ	Short	Open

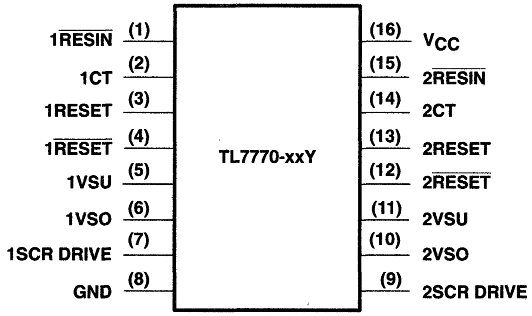
† The values listed are nominal.

TL7770-xxY chip information

These chips, when properly assembled, display characteristics similar to the TL7770-xxC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

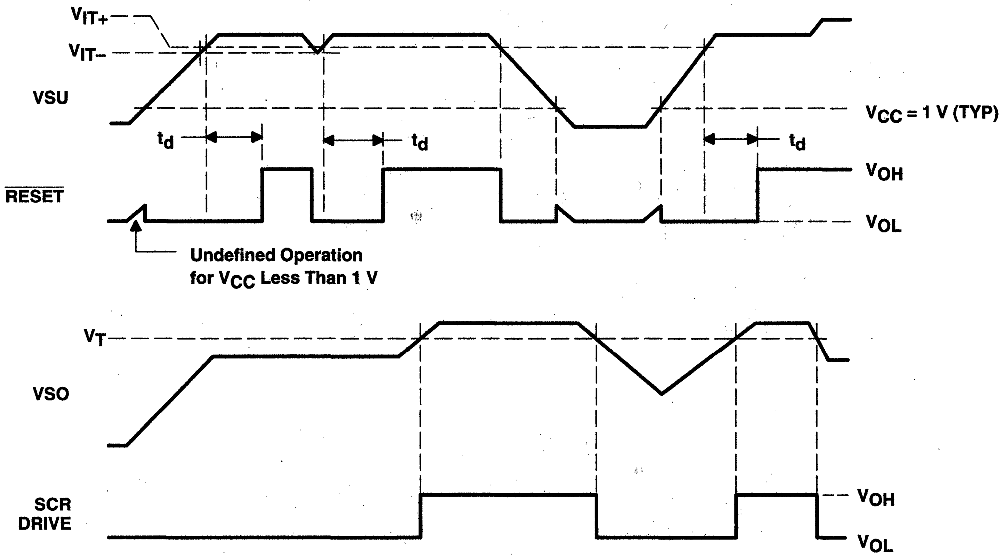
BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO (see Note 1)	–0.3 V to 18 V
Low-level output current (1$\overline{RESET}$ and 2$\overline{RESET}$), I_{OL}	20 mA
High-level output current (1RESET and 2RESET), I_{OH}	–20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TL7770_C	0°C to 70°C
TL7770_M	–55°C to 125°C
TL7770–Q	–40°C to 125°C
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package	260°C
Lead temperature 1,6 mm (1/16 in) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 2)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage (1CT and 2CT), V_O			5	V
High-level input voltage range, V_{IH}, 1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$		2	18	V
Low-level input voltage range, V_{IL}, 1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$		0	0.8	V
Output sink current (1CT and 2CT), I_O			50	μA
High-level output current (1RESET and 2RESET), I_{OH}			−16	mA
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$, I_{OL}			16	mA
Continuous output current (1SCR DRIVE and 2SCR DRIVE), I_O			25	mA
Timing Capacitor, C_T			10	μF
Operating free-air temperature, T_A	TL7770C Series	0	70	°C
	TL7770M Series	−55	125	
	TL7770Q Series	−40	125	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	TL7770-5C, TL7770-12C TL7770-15C, TL7770-5Q TL7770-12Q, TL7770-15Q			UNIT
				MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	RESET	$I_{OH} = -15$ mA	$V_{CC}-1.5$			V
		SCR DRIVE	$I_{OH} = -20$ mA	$V_{CC}-1.5$			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	$I_{OL} = 15$ mA			0.4	V
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	$T_A = 25°C$	4.5	4.55	4.6	V
		TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
		TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-15 (15-V sense, 1VSU)		13.36		13.91	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	$T_A = 25°C$		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-15 (15-V sense, 1VSU)			45		
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12, TL7770-15 (VSO)	$T_A = 25°C$	2.53	2.58	2.63	V
			T_A = MIN to MAX	2.48		2.68	
I_I	Input current	$\overline{\text{RESIN}}$	$V_I = 5.5$ V or 0.4 V			−10	μA
		VSO	$V_I = 2.4$ V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	$V_O = 18$ V			50	μA
I_{OL}	Low-level output current	RESET	$V_O = 0$			−50	μA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

total device

PARAMETER		TEST CONDITIONS†		TL7770-5C, TL7770-12C TL7770-15C, TL7770-5Q TL7770-12Q, TL7770-15Q			UNIT
				MIN	TYP‡	MAX	
V_{res}§	Power-up reset voltage	V_{CC} = VSU			0.8	1	V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	$T_A = 25°C$			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ This the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	TL7770-5M, TL7770-12M TL7770-15M			UNIT
				MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	RESET	$I_{OH} = -15$ mA	$V_{CC}-1.5$			V
		SCR DRIVE	$I_{OH} = -20$ mA	$V_{CC}-1.5$			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	$I_{OL} = 15$ mA			0.4	V
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5M (5-V sense, 1VSU)	$T_A = 25°C$	4.5	4.55	4.632	V
		TL7770-12M (12-V sense, 1VSU)		10.8	10.9	11.07	
		TL7770-15M (15-V sense, 1VSU)		13.5	13.64	13.866	
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)		1.485	1.5	1.527	
		TL7770-5M (5-V sense, 1VSU)	T_A = MIN to MAX	4.4		4.646	
		TL7770-12M (12-V sense, 1VSU)		10.62		11.12	
		TL7770-15M (15-V sense, 1VSU)		13.36		13.916	
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)		1.47		1.542	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5M (5-V sense, 1VSU)	$T_A = 25°C$		15		mV
		TL7770-12M (12-V sense, 1VSU)			36		
		TL7770-15M (15-V sense, 1VSU)			45		
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5M, TL7770-12M, TL7770-15M (VSO)	$T_A = 25°C$	2.53	2.58	2.63	V
			T_A = MIN to MAX	2.48		2.68	
I_I	Input current	$\overline{\text{RESIN}}$	$V_I = 5.5$ V or 0.4 V			−10	μA
		VSO	$V_I = 2.4$ V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	$V_O = V_{CC}$			50	μA
I_{OL}	Low-level output current	RESET	$V_O = 1$			−50	μA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

total device

PARAMETER		TEST CONDITIONS†		TL7770-5M, TL7770-12M TL7770-15M			UNIT
				MIN	TYP‡	MAX	
V_{res}§	Power-up reset voltage	V_{CC}	$V_{OL} = 0.4$ V, $I_{OL} = 1$ mA		**0.8**	1	V
I_{CC}	Supply current	1VSU 18 V, 2 VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	$T_A = 25°C$			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

electrical characteristics over recommended ranges of supply voltage, input voltage, and output current (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS	TL7770-5Y, TL7770-12Y TL7770-15Y MIN	TYP†	MAX	UNIT
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
		TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-15 (15-V sense, 1VSU)			45		
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
I_I	Input current	VSO	V_I = 2.4 V		0.5		μA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS		TL7770-5Y, TL7770-12Y TL7770-15Y MIN	TYP†	MAX	UNIT
V_{res}‡	Power-up reset voltage	V_{CC}	V_{OL} = 0.4 V, I_{OL} = 1 mA		0.8		V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA

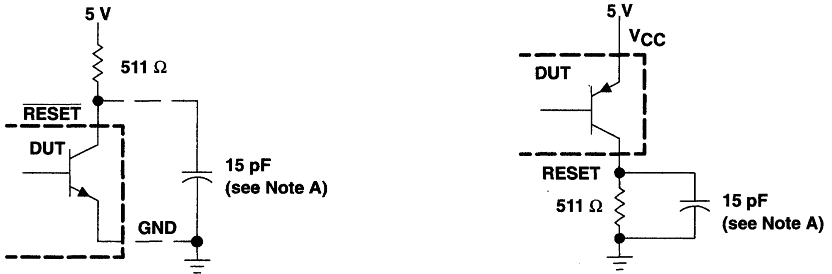
† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figure 1		270	500*	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500*	ns
t_r	Rise time		RESET				75*	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{\text{RESET}}$			75		ns
t_f	Fall time						50*	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2(a)		150		ns
		VSU		See Figure 2(b)		100		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

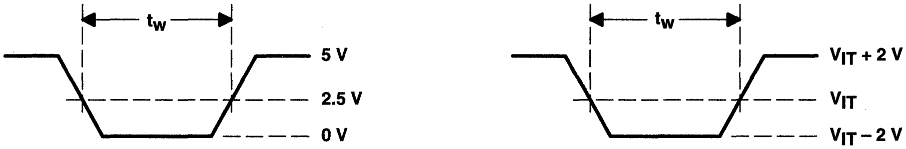


$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

RESET OUTPUT CONFIGURATION

NOTE A: This includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations



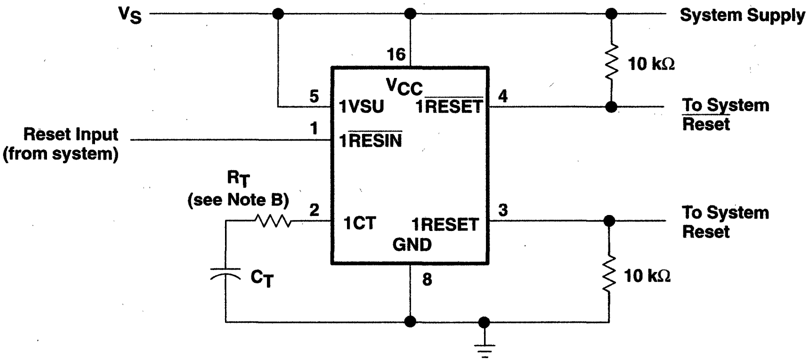
(a) $\overline{\text{RESIN}}$

(b) VSU

WAVEFORMS

Figure 2. Input Pulse Definition

APPLICATION INFORMATION



NOTES: A. Terminal numbers shown are for the DW, J, and N packages.

B. When V_{CC} and 1VSU are connected to the same point, it is recommended that series resistance (R_T) be added between the time delay programming capacitor (C_T) and the voltage supervisor device terminal (1CT).

The suggested R_T values is given by:

$$R_T > \frac{V_I - V_{IT-}}{1 \times 10^{-3}} \text{ , where } V_I = \text{(the lesser of 7.1 V or } V_S\text{)}$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - \left[\left((6.5E{-}5) \times 10^{-5}\right) \times R_T\right]}{6.5 \times 10^{-5}} \times C_T$$

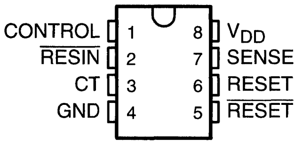
Figure 3. System Reset Controller With Undervoltage Sensing

TLC7705, TLC7705Y
MICROPOWER SUPPLY VOLTAGE SUPERVISORS

SLVS087B – DECEMBER 1994 – REVISED AUGUST 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor of 1.5% Maximum Accuracy, Compensated Over Full Temperature Range**
- **Programmable Delay Time By External Capacitor**
- **Minimum Supply Voltage of 2 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 25 μA**
- **Power Saving Totem-Pole Outputs**

D OR P PACKAGE
(TOP VIEW)



description

The TLC7705 is a micropower supply voltage supervisor designed for reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

$$t_d = 21 \times C_T$$

where

C_T is in μf
t_d is in ms

The TLC7705 has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns to above threshold voltage.

The TLC7705 is a low-power enhancement of the TL7705A. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{\text{CS}}$) of the memory circuit with the RESET output of the TLC7705 and with the CONTROL driven by the memory bank select signal ($\overline{\text{CSH1}}$) of the microprocessor (see Figure 4), the memory circuit is automatically disabled during a power loss. (In this application the TLC7705 power has to be supplied by the battery.)

The TLC7705 is characterized for operation over a temperature range of −40°C to 85°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 85°C	4.55 V	TLC7705ID	TLC7705IP	TLC7705Y

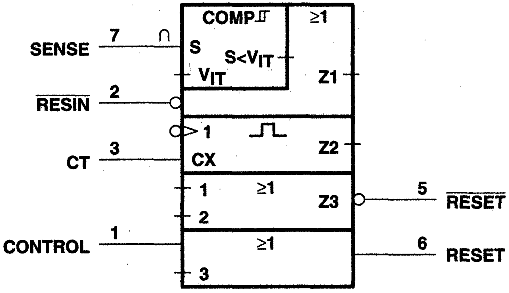
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC7705IDR).
The chip form is tested at 25°C.

FUNCTION TABLE

CONTROL	$\overline{\text{RESIN}}$	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{\text{RESET}}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L†	H†
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H†

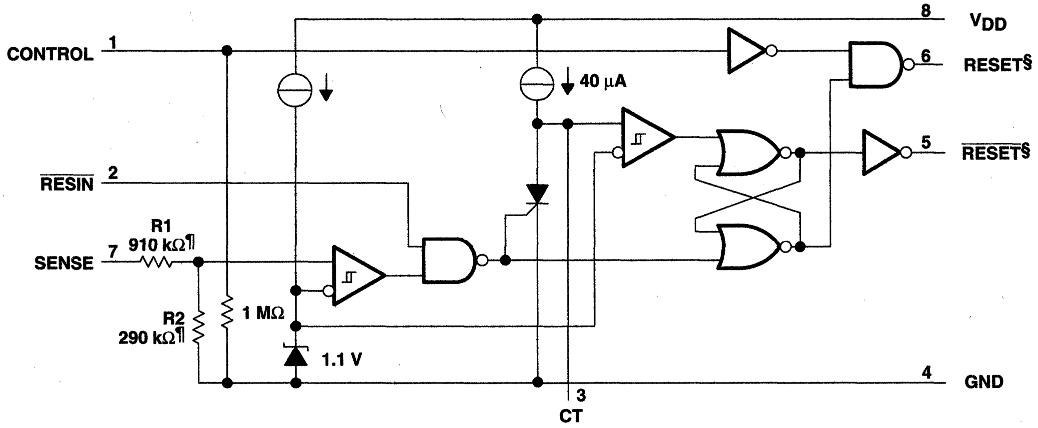
† RESET and $\overline{\text{RESET}}$ states shown are valid for $t > t_d$.

logic symbol‡



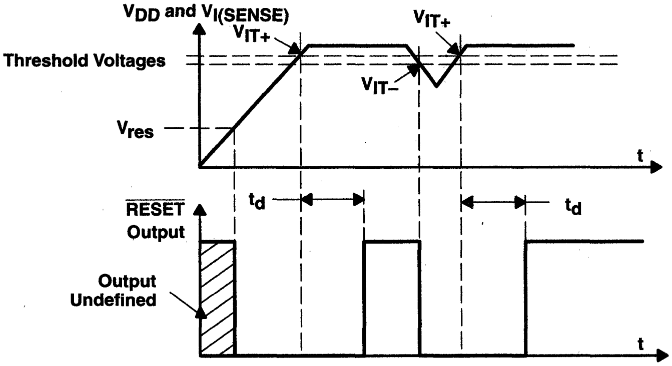
‡ This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.

functional block diagram



§ Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
¶ Nominal value

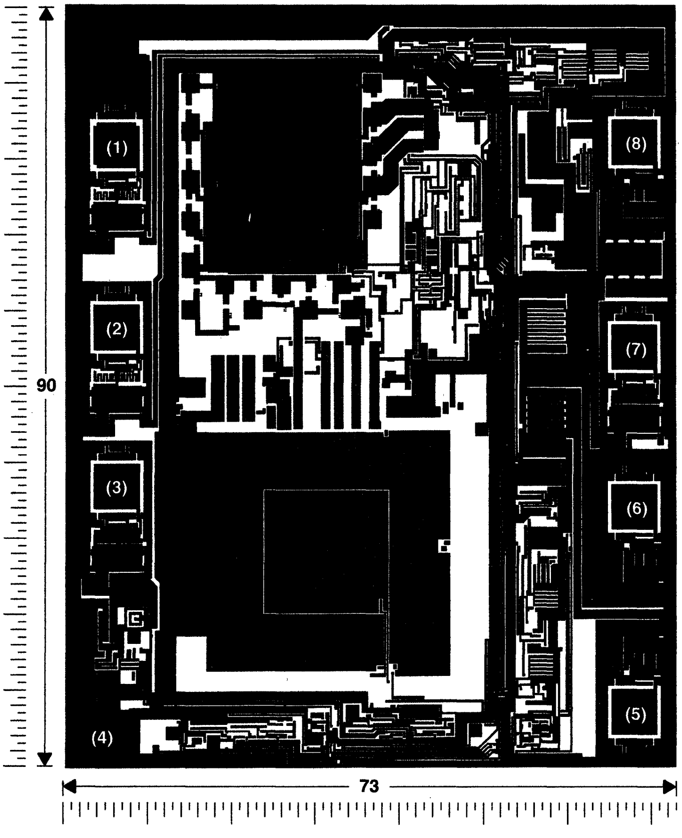
timing diagram

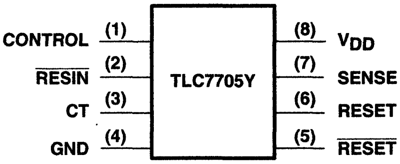


TLC7705Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC7705. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	7 V
Input voltage range (see Note 1)	−0.3 V to 7 V
Maximum low output current, I_{OL}	10 mA
Maximum high output current, I_{OH}	−10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Timing capacitor, C_t (see Note 2)			100	μF
Input voltage, V_I		0	6	V
High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IH}	$V_{DD} = 2$ V	1.7		V
	$V_{DD} = 2.7$ V	1.8		
	$V_{DD} = 4.5$ V	2		
Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IL}	$V_{DD} = 2$ V		0.3	V
	$V_{DD} = 2.7$ V		0.4	
	$V_{DD} = 4.5$ V		0.8	
High-level output current, I_{OH}	$V_{DD} = 2.7$ V		−2.5	mA
	$V_{DD} = 4.5$ V		−3	
Low-level output current, I_{OL}	$V_{DD} = 2.7$ V		2.5	mA
	$V_{DD} = 4.5$ V		3	
High-level input pulse duration at SENSE		20		μs
Low-level input pulse duration at SENSE		2		
High-level input pulse duration at $\overline{\text{RESIN}}$		20		
Low-level input pulse duration at $\overline{\text{RESIN}}$		2		
Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL, Δt/ΔV			100	ns/V
Operating free-air temperature range, T_A		−40	85	°C

‡ To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

NOTE 2: Limited by the leakage current of the capacitor

electrical characteristics over recommended operating conditions (see Note 3) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC7705I			UNIT
				MIN	TYP†	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$	$V_{DD} = 2\ V$	1.8			V
			$V_{DD} = 2.7\ V$	2.5			
			$V_{DD} = 4.5\ V$	4.3			
		$I_{OH} = -3\ mA$	$V_{DD} = 4.5\ V$	3.7			
V_{OL}	Low-level output voltage	$I_{OL} = 20\ \mu A$	$V_{DD} = 2\ V$			0.1	V
			$V_{DD} = 2.7\ V$			0.1	
			$V_{DD} = 4.5\ V$			0.1	
		$I_{OL} = 3\ mA$	$V_{DD} = 4.5\ V$			0.4	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 4)		$V_{DD} = 2\ V$ to $6\ V$	4.48	4.55	4.62	V
V_{hys}	Hysteresis, SENSE		$V_{DD} = 2\ V$ to $6\ V$		40		mV
V_{res}	Power-up reset voltage‡		$I_{OL} = 20\ \mu A$			1	V
I_I	Input current	$\overline{\text{RESIN}}$	$V_I = 0\ V$ to V_{DD}	−1		1	µA
		CONTROL	$V_I = V_{DD}$		5	10	
		SENSE	$V_I = 5\ V$		4	8	
I_{DD}	Supply current	$T_A = -40°C$ to $85°C$	$\overline{\text{RESIN}} = V_{DD}$, SENSE = $V_{DD} > V_{IT+}$§, CONTROL = 0 V, Outputs open		9	25	µA
		$T_A = 0°C$ to $70°C$			9	20	
$I_{DD(d)}$	Supply current during t_d		$V_{DD} = 5\ V$, $V_{CT} = 0\ V$, $\overline{\text{RESIN}} = V_{DD}$, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	µA
C_I	Input capacitance, SENSE		$V_I = 0\ V$ to V_{DD}		50		pF

† Typical values apply at $T_A = 25°C$.

‡ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

§ $V_{IT+} = V_{IT-} + V_{hys}$

NOTES: 3. All characteristics are measured with $C_T = 0.1\ \mu F$.

4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

electrical characteristics over recommended operating conditions, T_A = 25°C, C_T = 0.1 µF(unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC7705Y			UNIT
				MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 4)		V_{DD} = 2 V to 6 V		4.55		V
V_{hys}	Hysteresis, SENSE		V_{DD} = 2 V to 6 V		40		mV
I_I	Input current	CONTROL	$V_I = V_{DD}$		5		µA
		SENSE	V_I = 5 V		4		
I_{DD}	Supply current		$\overline{\text{RESIN}} = V_{DD}$, SENSE = $V_{DD} > V_{IT+}$†, CONTROL = 0 V, Outputs open		9		µA
$I_{DD(d)}$	Supply current during t_d		V_{DD} = 5 V, V_{CT} = 0 V, $\overline{\text{RESIN}} = V_{DD}$, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120		µA
C_I	Input capacitance, SENSE		V_I = 0 V to V_{DD}		50		pF

† $V_{IT+} = V_{IT-} + V_{hys}$

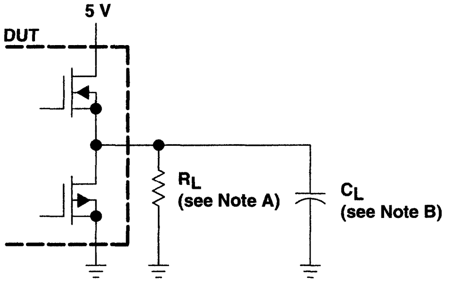
NOTE 4 To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 500 Ω, C_L = 50 pF, T_A = 25°C

PARAMETER		MEASURED		TEST CONDITIONS	TLC7705I, TLC7705Y			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \ge V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, C_T = 100 nF, See timing diagram	1.5	2.1	3.5	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}\text{max}$ + 0.2 V, $V_{IL} = V_{IT-}\text{min}$ – 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						2	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				2	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = $V_{IT+}\text{max}$ + 0.2 V, CONTROL = 0.4 V, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = $V_{IT+}\text{max}$ + 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CT = NC†			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output						35	
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

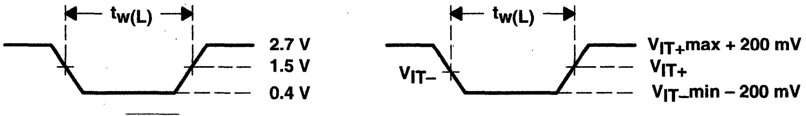
† NC equals no capacitor and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, $R_L = 500\ \Omega$.
B. $C_L = 50$ pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations



(a) $\overline{\text{RESIN}}$

(b) SENSE

WAVEFORMS

Figure 2. Input Pulse Definition

APPLICATION INFORMATION

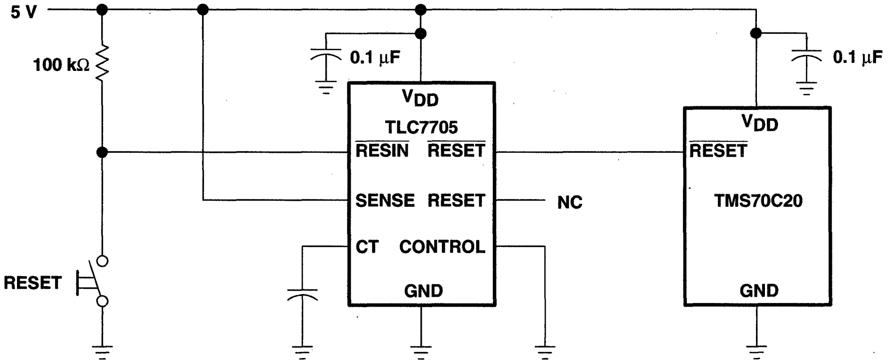


Figure 3. Reset Controller in a Microcomputer System

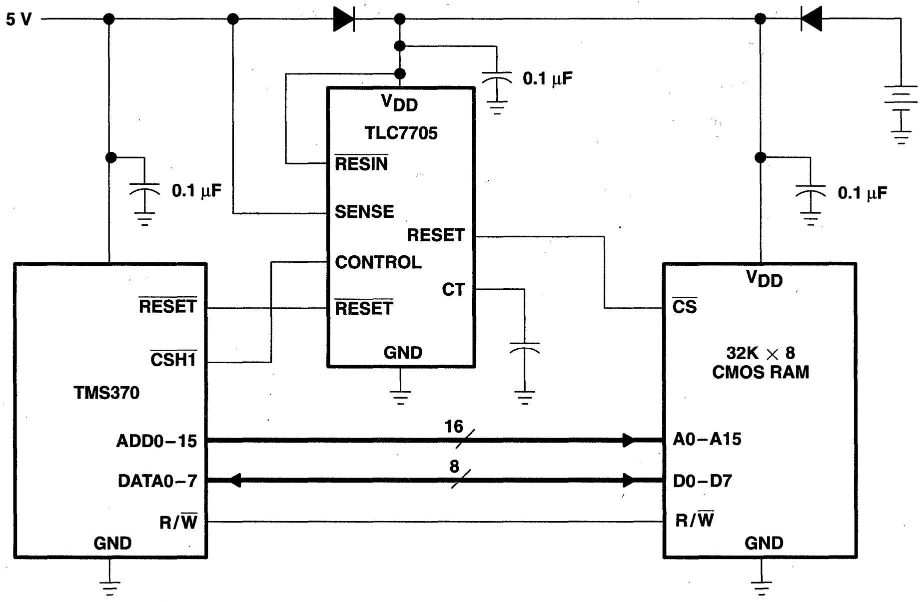


Figure 4. Data Retention During Power Down Using Static CMOS RAMs

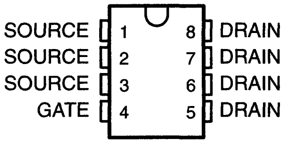
Contents

TPS1100, TPS1100Y
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

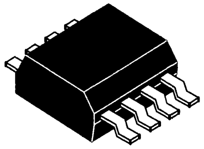
SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 0.18 Ω Typ at $V_{GS} = -10$ V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)} = -1.5$ V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015**

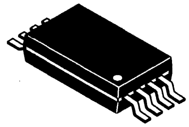
D OR PW PACKAGE
(TOP VIEW)



D PACKAGE



PW PACKAGE

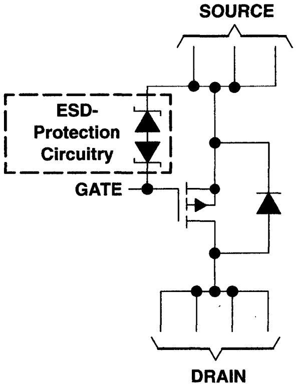


description

The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 µA, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for an small-outline integrated circuit (SOIC) package.

schematic



NOTE A. For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

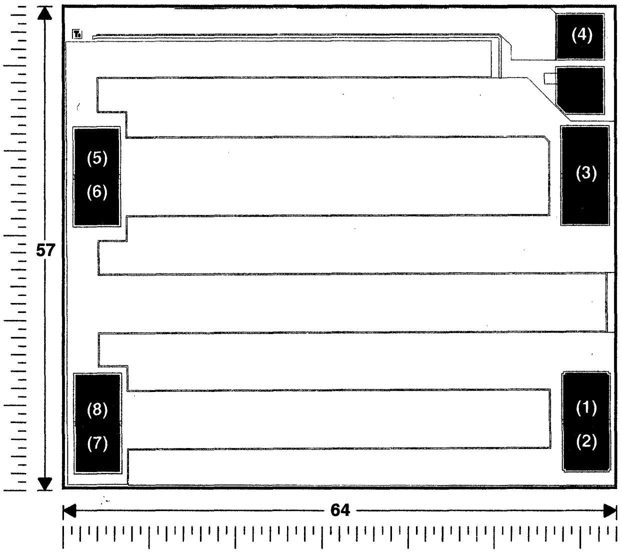
description (continued)

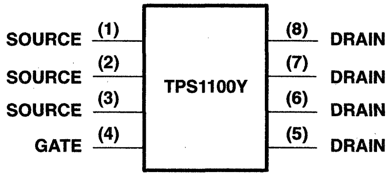
Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				–15	V
Gate-to-source voltage, V_{GS}				2 or –15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = –2.7 V	D package	T_A = 25°C	±0.41	A
			T_A = 125°C	±0.28	
		PW package	T_A = 25°C	±0.4	
			T_A = 125°C	±0.23	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.6	
			T_A = 125°C	±0.33	
		PW package	T_A = 25°C	±0.53	
			T_A = 125°C	±0.27	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.81	
			T_A = 125°C	±0.37	
	V_{GS} = –10 V	D package	T_A = 25°C	±1.6	
			T_A = 125°C	±0.72	
		PW package	T_A = 25°C	±1.27	
			T_A = 125°C	±0.58	
Pulsed drain current, I_D‡			T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S			T_A = 25°C	–1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	101 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1100			TPS1100Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$		−1	−1.25	−1.50		−1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	$I_S = -1$ A, $V_{GS} = 0$ V			−0.9			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V, $V_{GS} = -12$ V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V, $V_{GS} = 0$ V	T_J = 25°C			−0.5				µA
			T_J = 125°C			−10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A		180			180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A		291	400		291		
		$V_{GS} = -3$ V	$I_D = -0.2$ A		476	700		476		
		$V_{GS} = -2.7$ V			606	850		606		
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V, $I_D = -2$ A			2.5			2.5		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	TPS1100, TPS1100Y			UNIT
			MIN	TYP	MAX	
Q_g	Total gate charge	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -1$ A		5.45		nC
Q_{gs}	Gate-to-source charge			0.87		
Q_{gd}	Gate-to-drain charge			1.4		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D = -1$ A, $R_G = 6\ \Omega$, See Figures 1 and 2		4.5		ns
$t_{d(off)}$	Turn-off delay time			13		ns
t_r	Rise time			10		ns
t_f	Fall time			2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A, di/dt = 100 A/µs		16		

PARAMETER MEASUREMENT INFORMATION

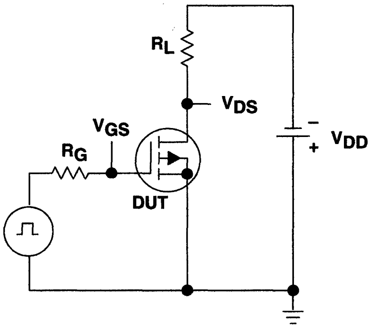


Figure 1. Switching-Time Test Circuit

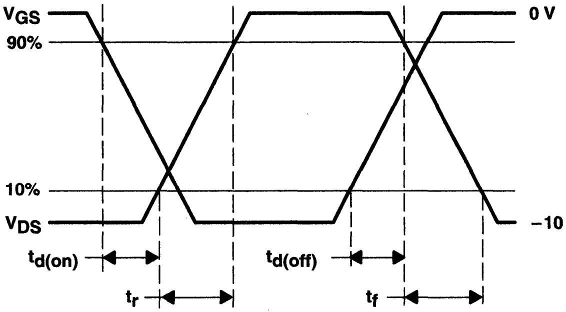


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

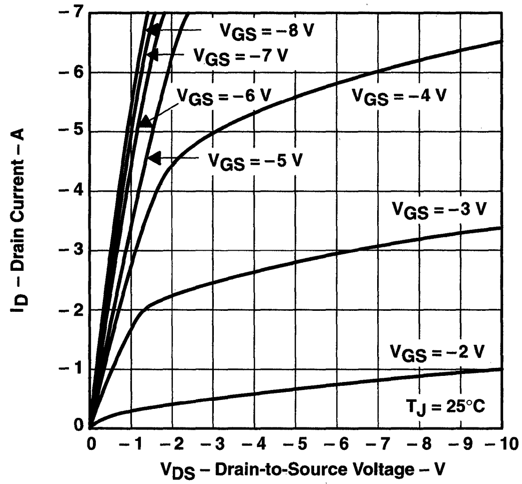


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

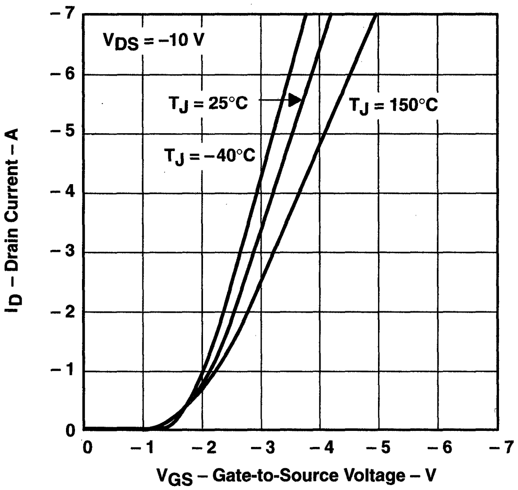


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

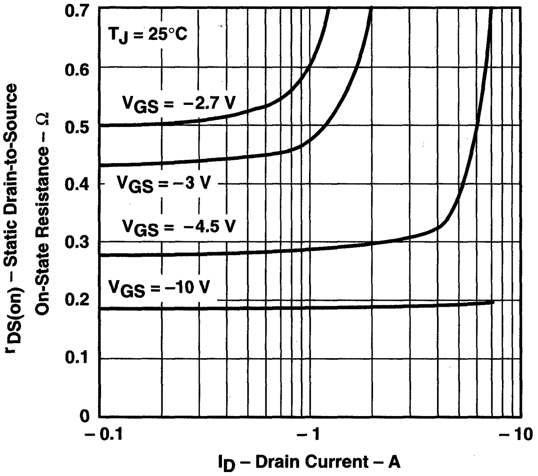
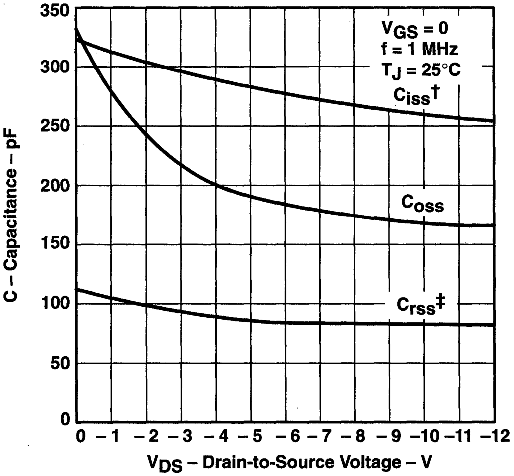


Figure 5

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}, C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

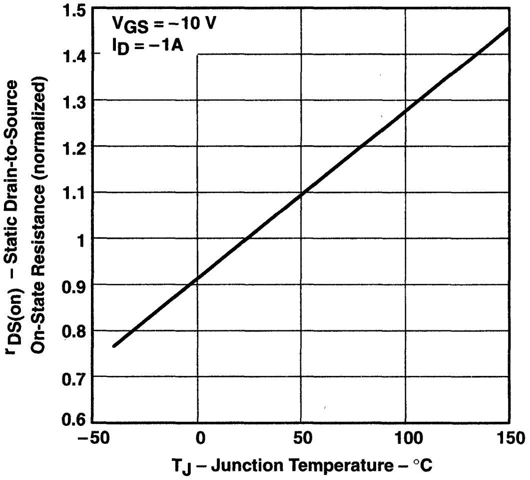


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

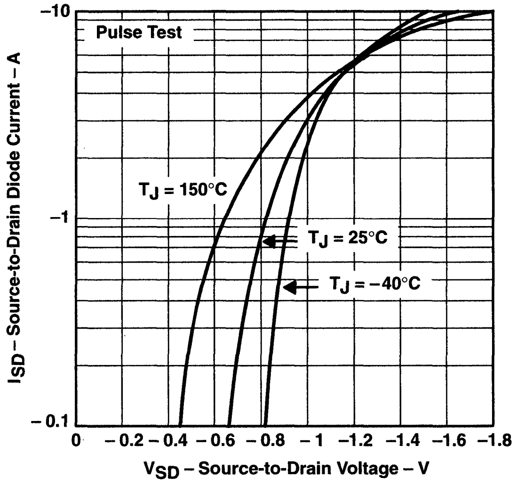


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

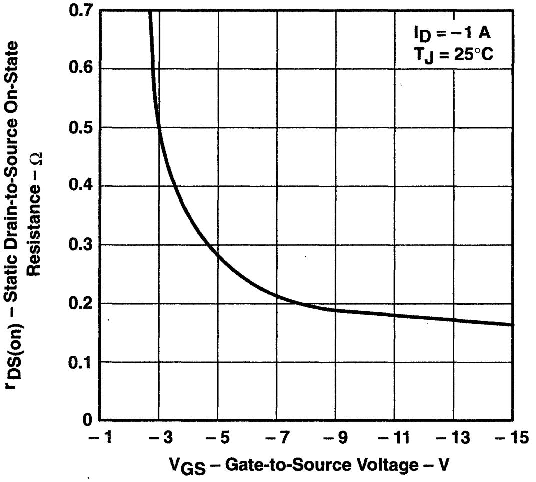


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

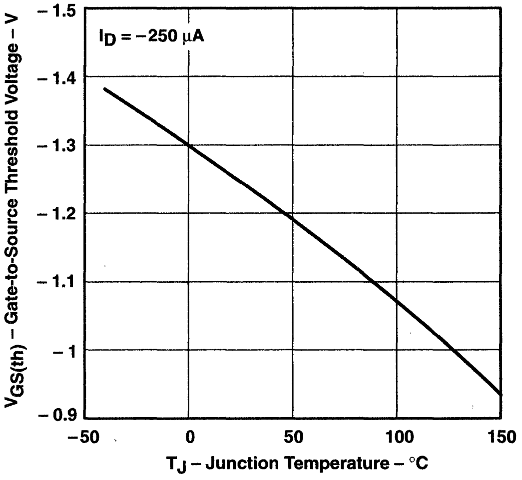


Figure 10

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

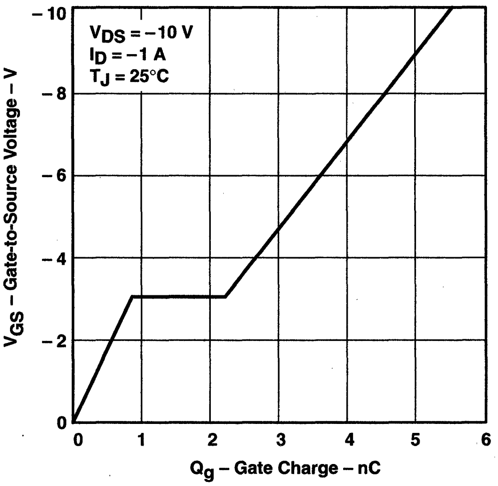


Figure 11

THERMAL INFORMATION

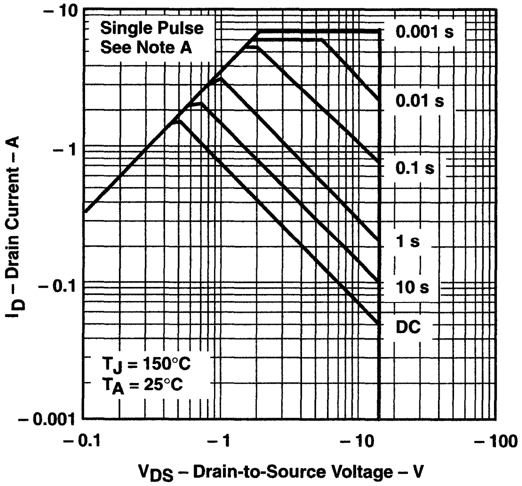

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

Figure 12

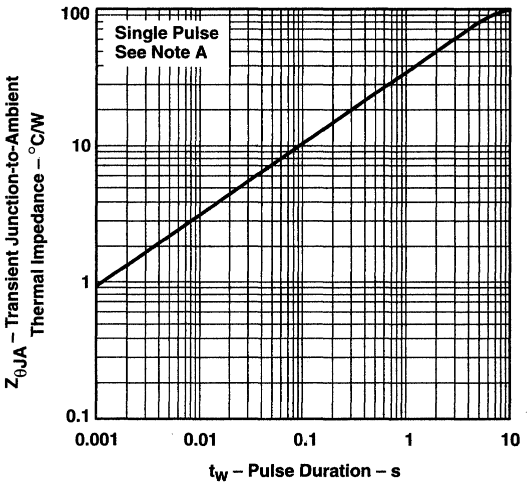

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

Figure 13

NOTE A. Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

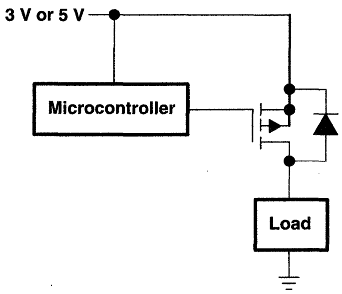


Figure 14. Notebook Load Management

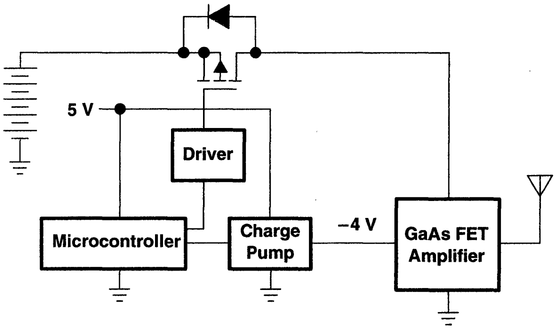


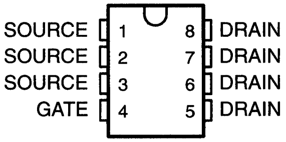
Figure 15. Cellular Phone Output Drive

TPS1101, TPS1101Y
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

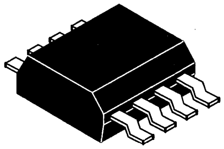
SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 0.09 Ω Typ at V_{GS} = –10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = –1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

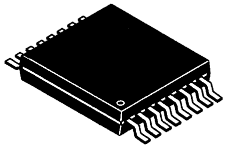
D PACKAGE
(TOP VIEW)



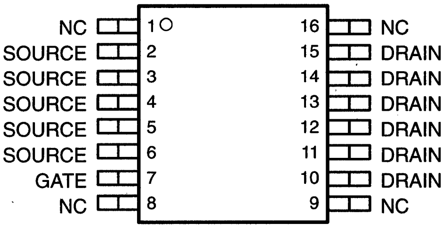
D PACKAGE



PW PACKAGE



PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS1101 is a single, low-$r_{DS(on)}$, P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of –1.5 V and an I_{DSS} of only 0.5 μA, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

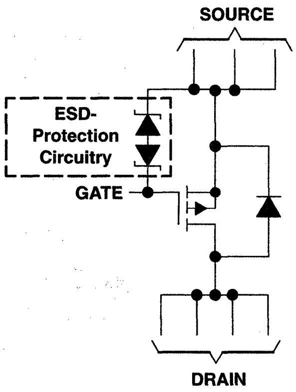
T_J	PACKAGED DEVICES†		CHIP FORM (Y)
	SMALL OUTLINE (D)	TSSOP (PW)	
–40°C to 150°C	TPS1101D	TPS1101PWLE	TPS1101Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at 25°C.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

schematic

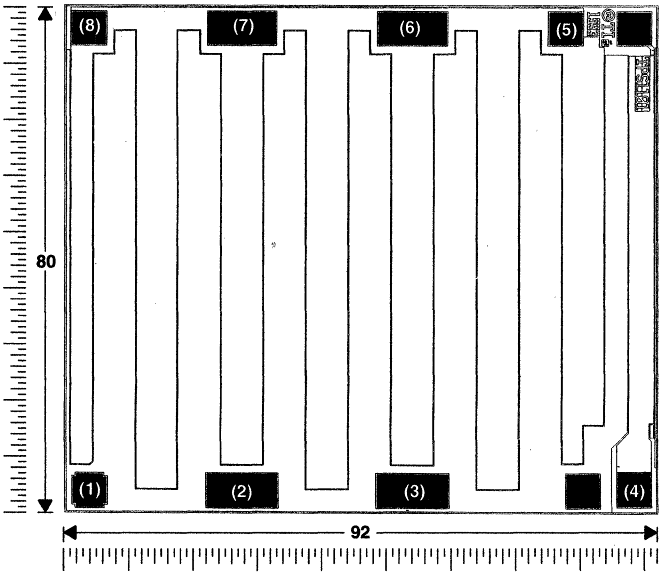


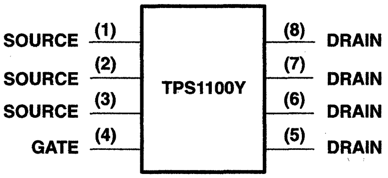
NOTE A. For all applications, all source terminals should be connected and all drain terminals should be connected.

TPS1101Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				−15	V
Gate-to-source voltage, V_{GS}				2 or −15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = −2.7 V	D package	T_A = 25°C	±0.62	A
			T_A = 125°C	±0.39	
		PW package	T_A = 25°C	±0.61	
			T_A = 125°C	±0.38	
	V_{GS} = −3 V	D package	T_A = 25°C	±0.88	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.86	
			T_A = 125°C	±0.45	
	V_{GS} = −4.5 V	D package	T_A = 25°C	±1.52	
			T_A = 125°C	±0.71	
		PW package	T_A = 25°C	±1.44	
			T_A = 125°C	±0.67	
	V_{GS} = −10 V	D package	T_A = 25°C	±2.30	
			T_A = 125°C	±1.04	
		PW package	T_A = 25°C	±2.18	
			T_A = 125°C	±0.98	
Pulsed drain current, I_D‡			T_A = 25°C	±10	A
Continuous source current (diode conduction), I_S			T_A = 25°C	−1.1	A
Storage temperature range, T_{stg}				−55 to 150	°C
Operating junction temperature range, T_J				−40 to 150	°C
Operating free-air temperature range, T_A				−40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1101			TPS1101Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$		−1	−1.25	−1.5		−1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	$I_S = -1$ A, $V_{GS} = 0$ V			−1.04			−1.04		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V, $V_{GS} = -12$ V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V, $V_{GS} = 0$ V	T_J = 25°C			−0.5				μA
			T_J = 125°C			−10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -2.5$ A		90			90		mΩ
		$V_{GS} = -4.5$ V	$I_D = -1.5$ A		134	190		134		
		$V_{GS} = -3$ V	$I_D = -0.5$ A		198	310		198		
		$V_{GS} = -2.7$ V			232	400		232		
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V, $I_D = -2$ A			4.3			4.3		S

† Pulse test: pulse duration ≤ 300 μs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	TPS1101, TPS1101Y			UNIT
			MIN	TYP	MAX	
Q_g	Total gate charge	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -1$ A		11.25		nC
Q_{gs}	Gate-to-source charge			1.5		
Q_{gd}	Gate-to-drain charge			2.6		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D = -1$ A, $R_G = 6\ \Omega$, See Figures 1 and 2		6.5		ns
$t_{d(off)}$	Turn-off delay time			19		ns
t_r	Rise time			5.5		ns
t_f	Fall time			13		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A, di/dt = 100 A/μs		16		

PARAMETER MEASUREMENT INFORMATION

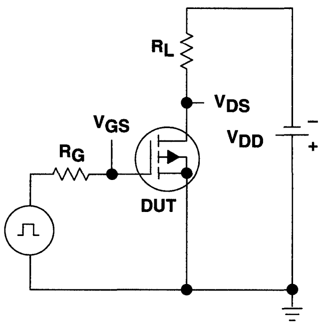


Figure 1. Switching-Time Test Circuit

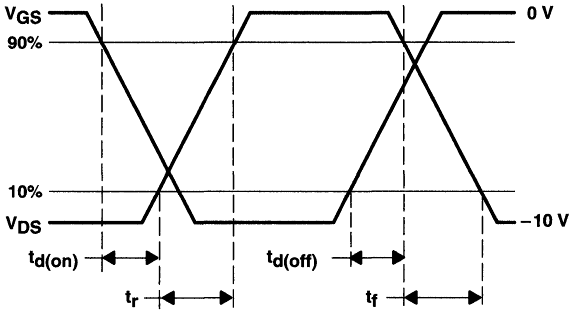


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
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Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

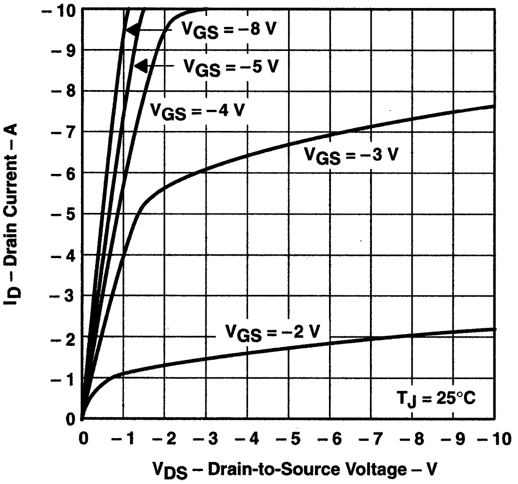


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

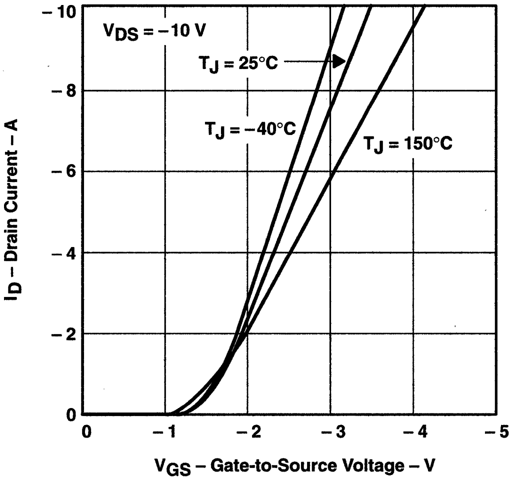


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

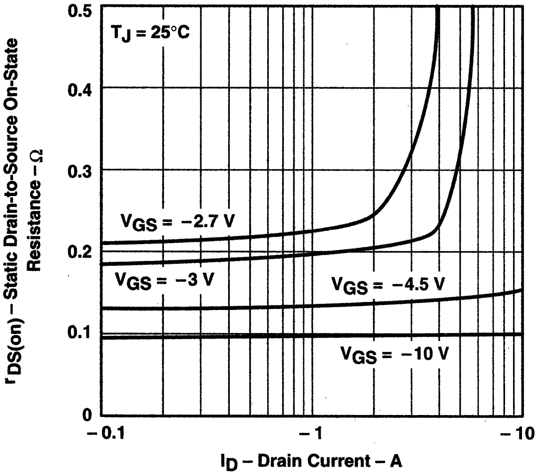
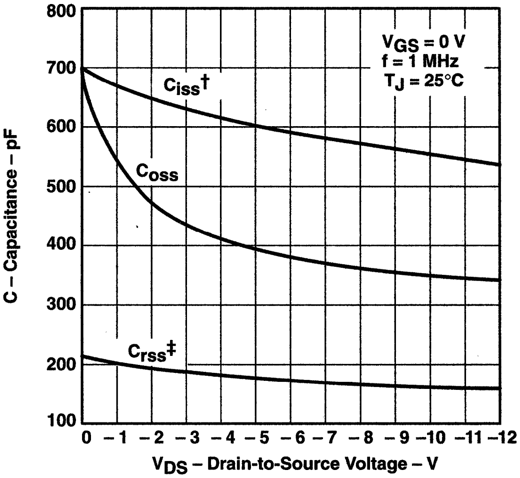


Figure 5

CAPACITANCE†
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}, C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

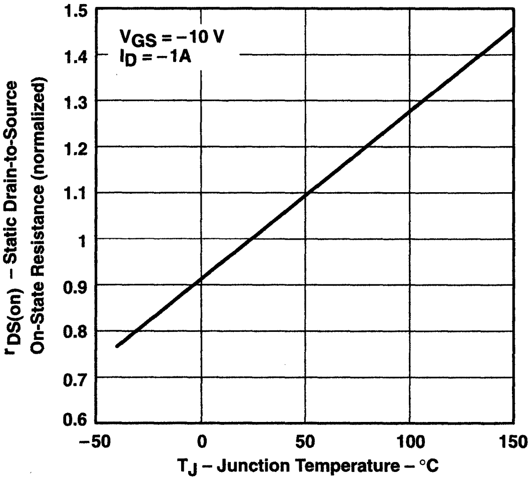

STATIC DRAIN-TO-SOURCE
ON-STATE RESISTANCE (NORMALIZED)
vs
JUNCTION TEMPERATURE

Figure 7

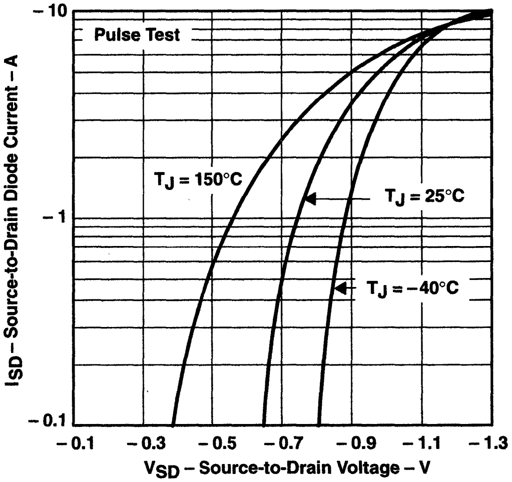

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

Figure 8

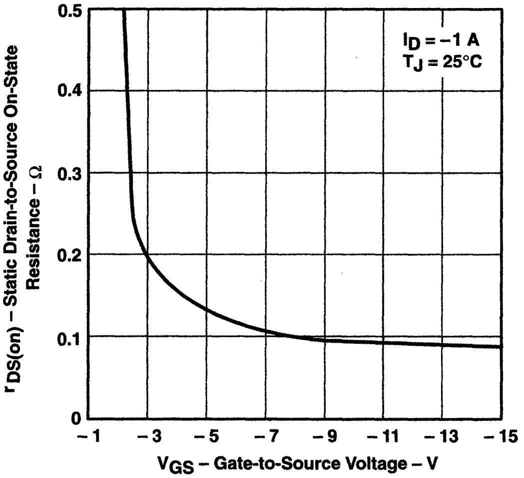

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

Figure 9

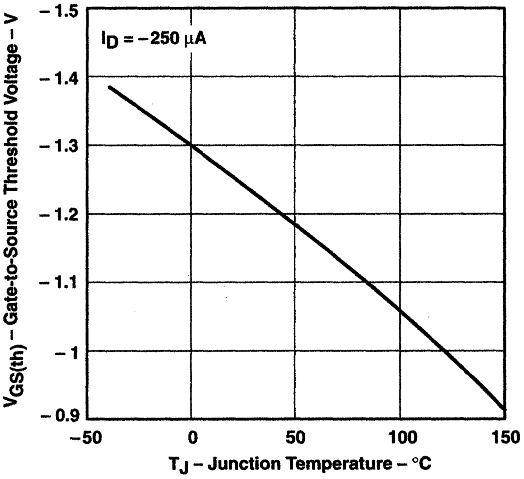

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 10

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

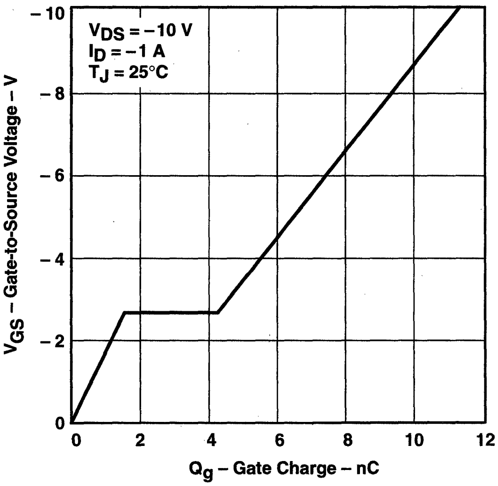


Figure 11

THERMAL INFORMATION

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

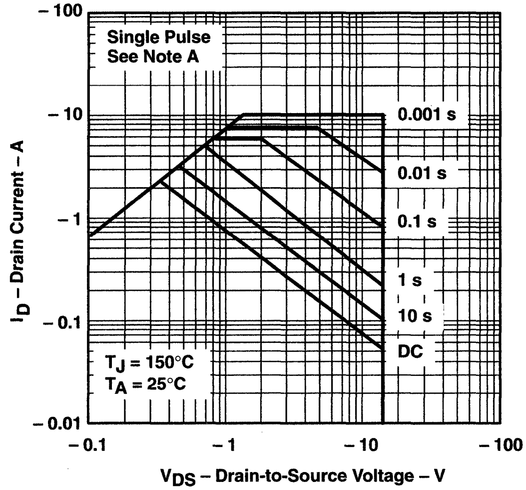


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT THERMAL IMPEDANCE vs PULSE DURATION

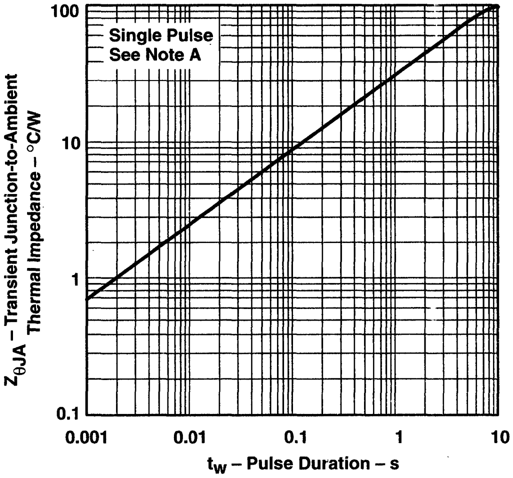


Figure 13

NOTE B. Values are for the D package and are FR4-board-mounted only.

APPLICATION INFORMATION

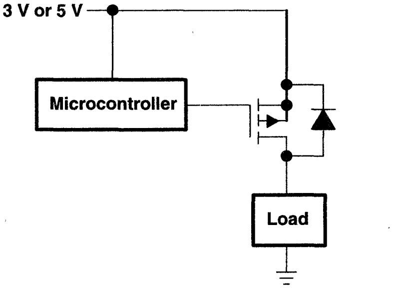


Figure 14. Notebook Load Management

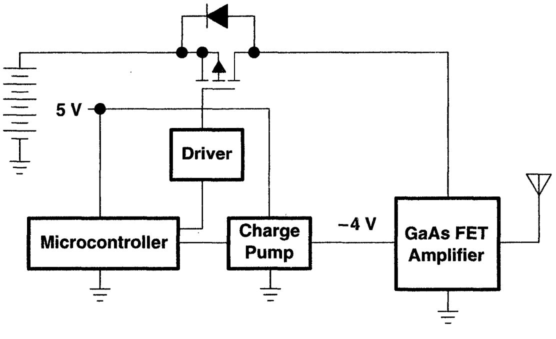


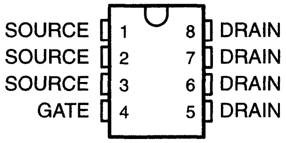
Figure 15. Cellular Phone Output Drive

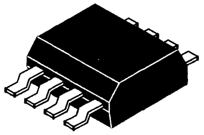
TPS1110, TPS1110Y
SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

SLVS100A – OCTOBER 1994 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 65 mΩ Typ at V_{GS} = –4.5 V**
- **High Current Capability**
  6 A at V_{GS} = –4.5 V
- **Logic-Level Gate Drive (3 V Compatible)**
  $V_{GS(th)}$ = –0.9 V Max
- **Low Drain-Source Leakage Current**
  <100 nA From 25°C to 75°C
  at V_{DS} = –6 V
- **Fast Switching . . . 5.8 ns Typ $t_{d(on)}$**
- **Small-Outline Surface-Mount Power Package**

D PACKAGE
(TOP VIEW)





description

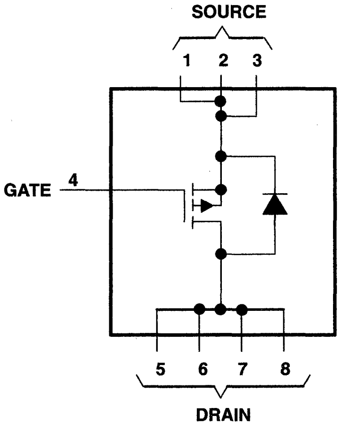
The TPS1110 is a single, low-$r_{DS(on)}$, P-channel enhancement-mode power MOS transistor. The device features extremely low-$r_{DS(on)}$ values coupled with logic-level gate-drive capability and very low drain-source leakage current. With a maximum $V_{GS(th)}$ of –0.9 V and an I_{DSS} of only –100 nA, the TPS1110 is the ideal high-side switch for low-voltage, portable battery-management power-distribution systems where maximizing battery life is an important concern. The thermal performance of the 8-pin small-outline (D) package has been greatly enhanced over the standard 8-pin SOIC, further making the TPS1110 ideally suited for many power applications. For compatibility with existing designs, the TPS1110 has a pinout common with other P-channel MOSFETs in small-outline integrated circuit (SOIC) packages. The TPS1110 is characterized for an operating junction temperature range, T_J, from –40°C to 150°C. The D package is available packaged in standard sleeves or in taped and reeled formats. When ordering the tape-and-reel format, add an R suffix to the device type number (e.g., TPS1110DR).

AVAILABLE OPTIONS

T_J	PACKAGED DEVICE†	CHIP FORM (Y)
	SMALL OUTLINE (D)	
–40°C to 150°C	TPS1110D	TPS1110Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1110DR). The chip form is tested at 25°C.

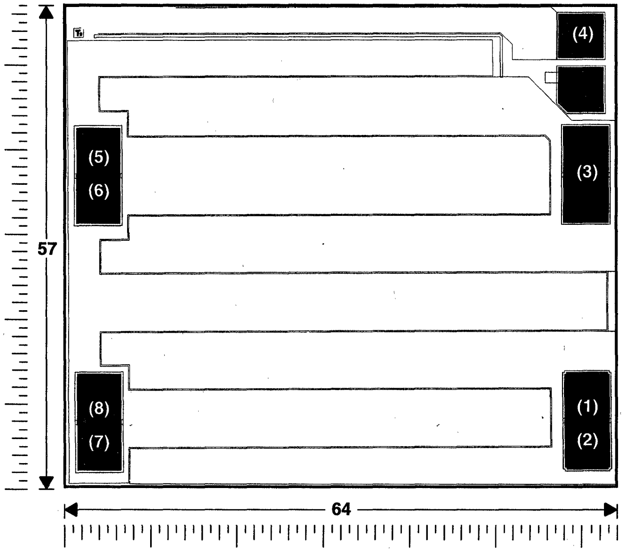
schematic

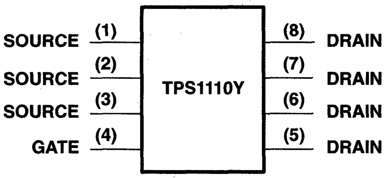


TPS1110Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1110C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			−7	V
Gate-to-source voltage, V_{GS}			±7	V
Continuous drain current, I_D	$V_{GS} = -2.7$ V	$T_P = 25°C$‡	−5	A
		$T_P = 125°C$‡	−2.3	
	$V_{GS} = -4.5$ V	$T_P = 25°C$‡	−6	
		$T_P = 125°C$‡	−2.7	
Pulse drain current, I_D		$T_A = 25°C$	−24	A
Continuous source current (diode conduction), I_S		$T_A = 25°C$	−6	A
Continuous total power dissipation		$T_P = 25°C$‡	4	W
Junction-to-pin thermal resistance (θ_{JP})			31	°C/W
Continuous total power dissipation		$T_A = 25°C$	1.25	W
Junction-to-ambient thermal resistance (θ_{JA})			100	°C/W
Storage temperature range, T_{stg}			−65 to 150	°C
Operating junction temperature range, T_J			−40 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ T_P – Temperature of drain pins measured close to the package

electrical characteristics at $T_J = 25°C$ (unless otherwise noted)

static

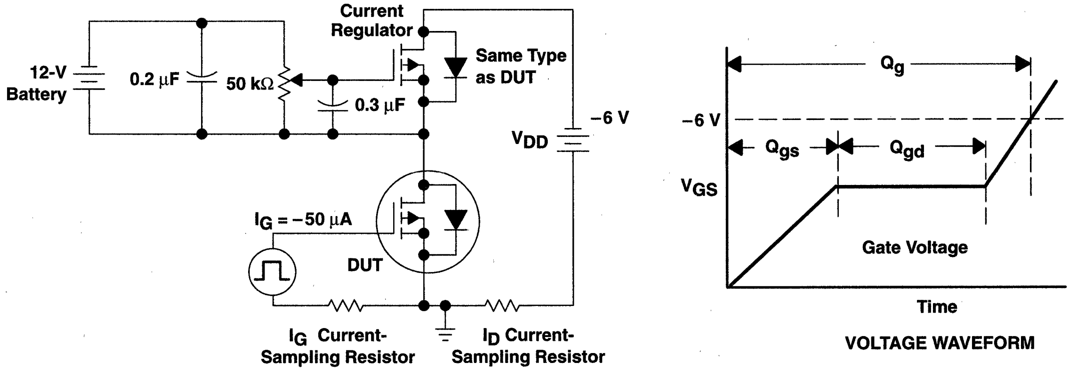
PARAMETER		TEST CONDITIONS		TPS1110			TPS1110Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, See Figure 9	$I_D = -250$ μA,	−0.5	−0.75	−0.9		−0.75		V
V_{SD}	Source-to-drain voltage (diode forward voltage)§	$I_{SD} = -3$ A, See Figure 8	$V_{GS} = 0$ V,		−0.8			−0.8		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -6$ V			±100				nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -7$ V, $V_{GS} = 0$ V	$T_J = 25°C$			−100				nA
		$V_{DS} = -6$ V, $V_{GS} = 0$ V	$T_J = 75°C$			−100				nA
			$T_J = 125°C$			−10				μA
$r_{DS(on)}$	Static drain-to-source on-state resistance§	$V_{GS} = -4.5$ V, See Figure 5	$I_D = -6$ A,		65	75		65		mΩ
		$V_{GS} = -2.7$ V, See Figure 5	$I_D = -2$ A,		100	110		100		
g_{fs}	Forward transconductance§	$V_{DS} = -5$ V,	$I_D = -6$ A		5			5		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = -6$ V, f = 1 MHz	$V_{GS} = 0$ V, See Figure 6		275			275		pF
C_{oss}	Short-circuit output capacitance, common source				415			415		
C_{rss}	Short-circuit reverse transfer capacitance, common source				73			73		

§ Pulse test: pulse duration ≤ 300 μs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	TPS1110			TPS1110Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Q_g	Total gate charge	$V_{DS} = -6$ V, $V_{GS} = -6$ V, $I_D = -3$ A See Figures 1 and 10		4.3	5.4		4.3		nC
Q_{gs}	Gate-to-source charge			0.66	0.83		0.66		
Q_{gd}	Gate-to-drain charge			0.52	0.68		0.52		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -6$ V, $R_L = 6\ \Omega$, $I_D = -1$ A, $R_G = 6\ \Omega$, See Figure 2		5.8	8		5.8		ns
$t_{d(off)}$	Turn-off delay time			22	29		22		ns
t_r	Rise time			22	29		22		ns
t_f	Fall time			4.5	7		4.5		
$t_{rr(SD)}$	Source-to-drain reverse-recovery time	$V_{DS} = -6$ V, di/dt = 100 A/µs, $I_D = -3$ A		65	98		65		
Q_{rr}	Total diode charge			71			71		nC

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

Figure 1. Gate-Charge Test Circuit and Waveform

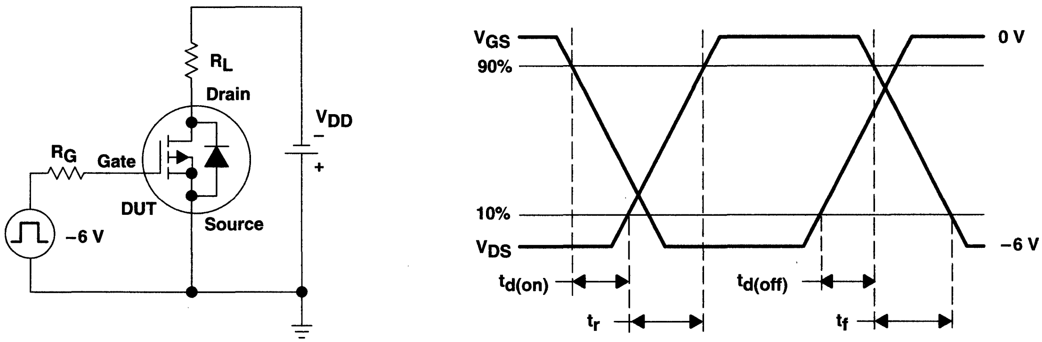


Figure 2. Resistive Switching

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Gate-to-source threshold voltage	vs Junction temperature	9
Gate-to-source voltage	vs Gate charge	10

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

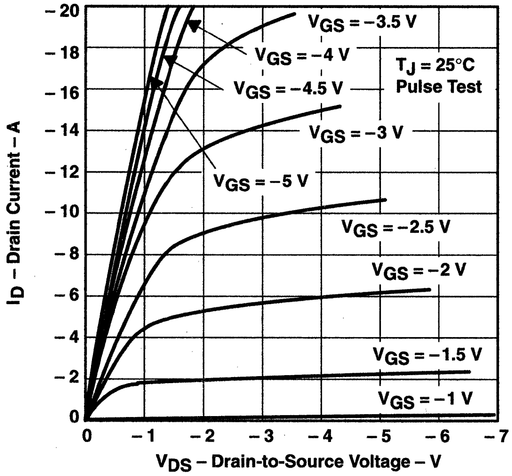


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

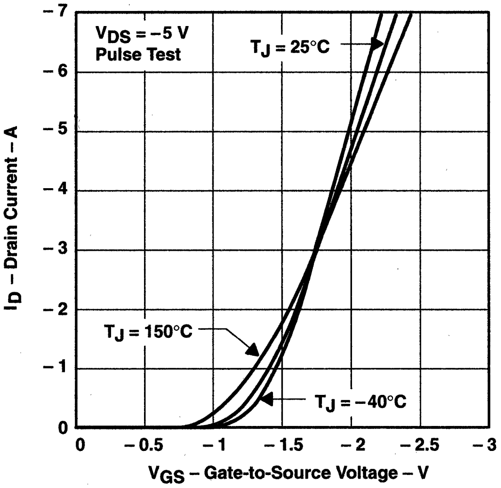


Figure 4

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

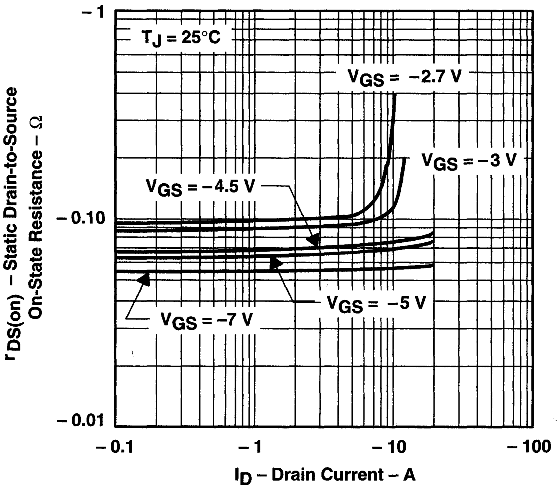
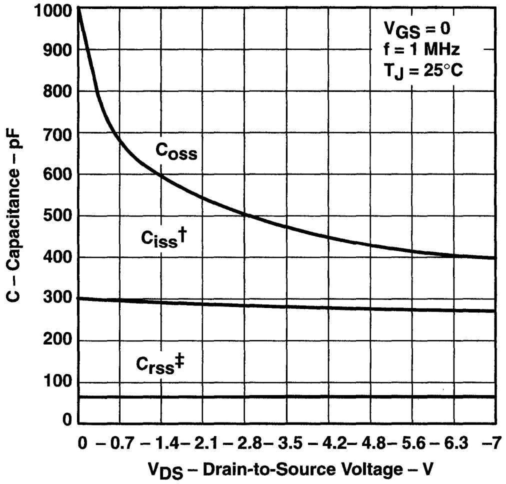


Figure 5

CAPACITANCE† vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

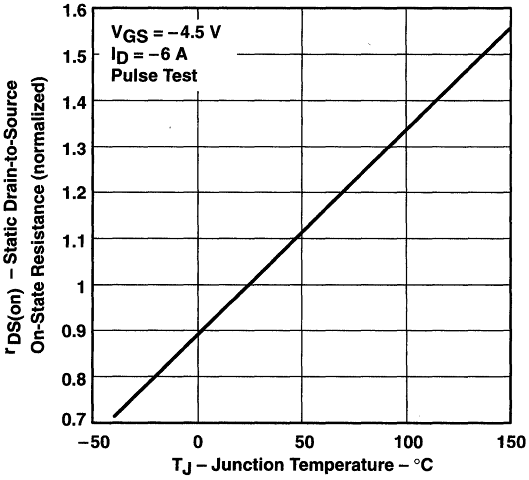


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

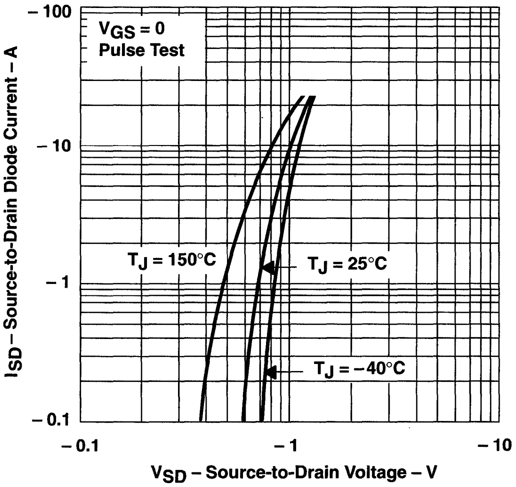


Figure 8

TYPICAL CHARACTERISTICS

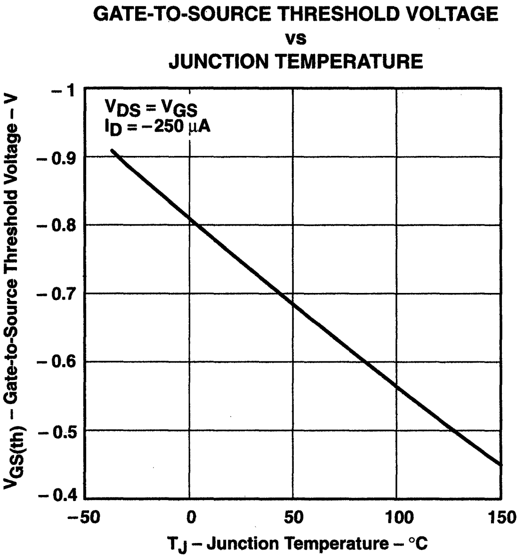


Figure 9

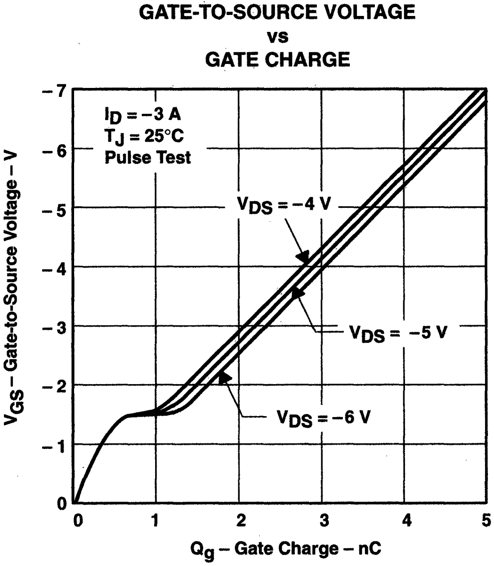


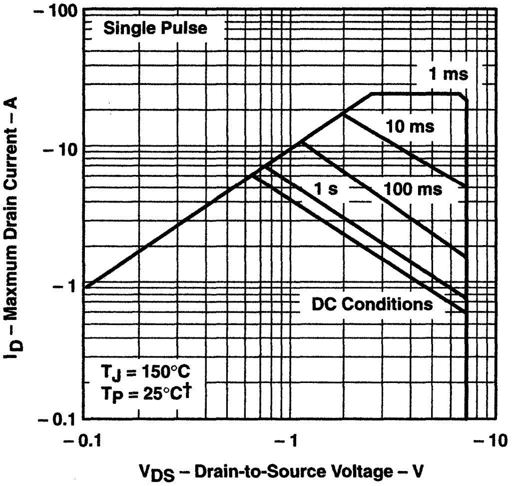
Figure 10

THERMAL INFORMATION

Table of Graphs

		FIGURE
Maximum drain current	vs Drain-to-source voltage	11
Junction-to-pin thermal resistance (normalized)	vs Pulse duration	12
Junction-to-ambient thermal resistance (normalized)	vs Pulse duration	13

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

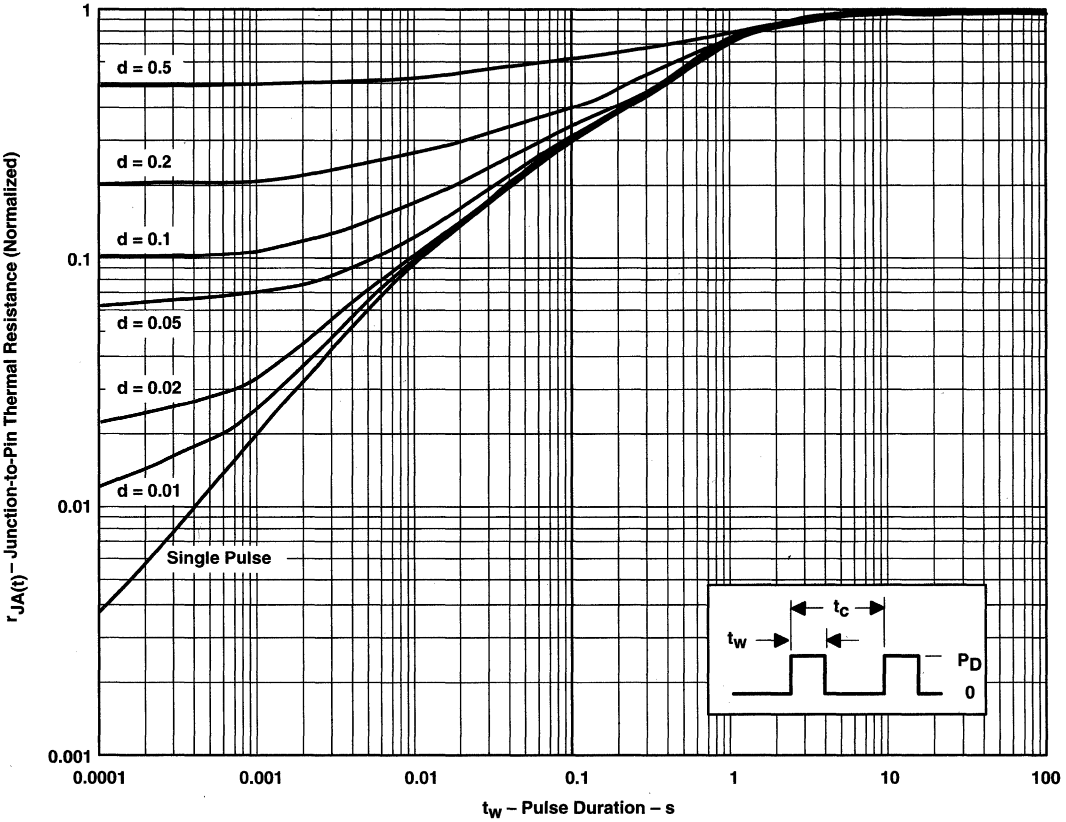


† T_P – Temperature of drain pins measured close to the package

Figure 11

THERMAL INFORMATION

JUNCTION-TO-PIN THERMAL RESISTANCE (NORMALIZED) vs PULSE DURATION

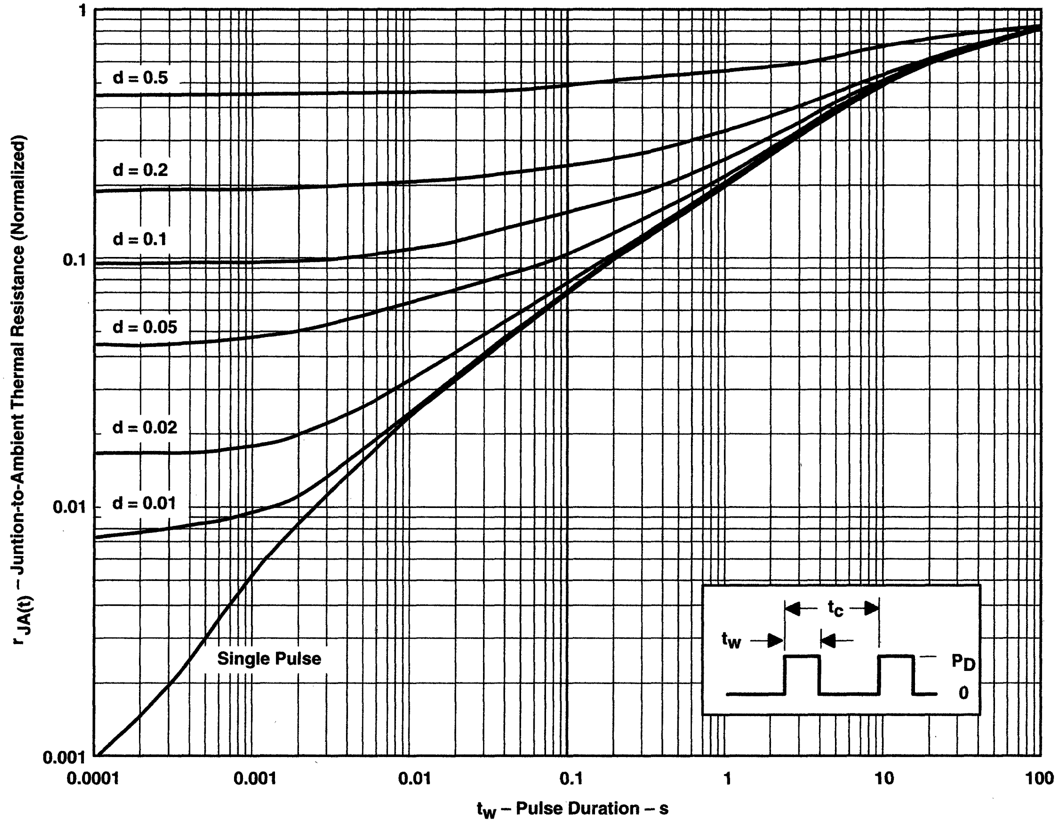


NOTE A: $Z_{\theta JP}(t) = r_{JP}(t) \cdot \theta_{JP}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c
peak $T_J = P_D \cdot Z_{\theta JP}(t) + T_P$

Figure 12

THERMAL INFORMATION

JUNCTION-TO-AMBIENT THERMAL RESISTANCE (NORMALIZED)† vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no special thermal considerations.

NOTE A: $Z_{\theta JA}(t) = r_{JA(t)} \cdot \theta_{JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C
peak $T_J = P_D \cdot Z_{\theta JA}(t) + T_A$

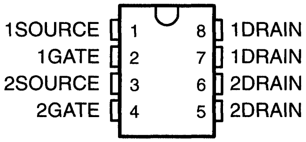
Figure 13

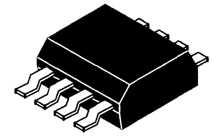
TPS1120, TPS1120Y
DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 0.18 Ω at $V_{GS} = -10$ V**
- **3-V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)} = -1.5$ V Max**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

D PACKAGE
(TOP VIEW)





description

The TPS1120 incorporates two independent p-channel enhancement-mode MOSFETs that have been optimized, by means of the Texas Instruments LinBiCMOS™ process, for 3-V or 5-V power distribution in battery-powered systems. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only 0.5 µA, the TPS1120 is the ideal high-side switch for low-voltage portable battery-management systems, where maximizing battery life is a primary concern. Because portable equipment is potentially subject to electrostatic discharge (ESD), the MOSFETs have built-in circuitry for 2-kV ESD protection. End equipment for the TPS1120 includes notebook computers, personal digital assistants (PDAs), cellular telephones, bar-code scanners, and PCMCIA cards. For existing designs, the TPS1120D has a pinout common with other p-channel MOSFETs in small-outline integrated circuit SOIC packages.

The TPS1120 is characterized for an operating junction temperature range, T_J, from −40°C to 150°C.

AVAILABLE OPTIONS

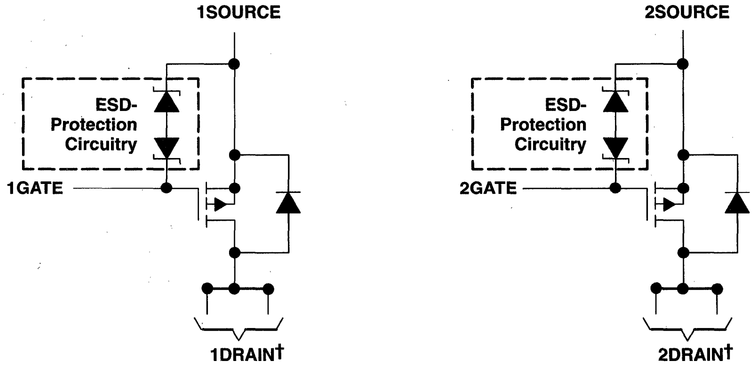
T_J	PACKAGED DEVICES† SMALL OUTLINE (D)	CHIP FORM (Y)
−40°C to 150°C	TPS1120D	TPS1120Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1120DR). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

schematic

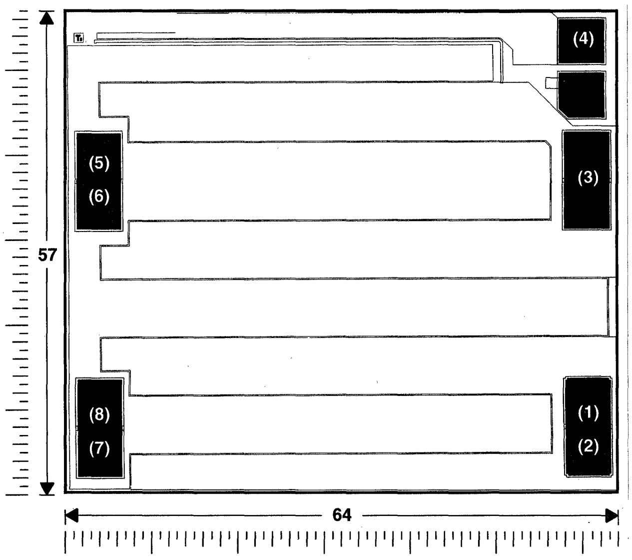


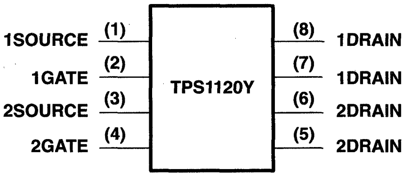
† For all applications, both drain pins for each device should be connected.

TPS1120Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1120C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			–15	V
Gate-to-source voltage, V_{GS}			2 or –15	V
Continuous drain current, each device (T_J = 150°C), I_D	V_{GS} = –2.7 V	T_A = 25°C	±0.39	A
		T_A = 125°C	±0.21	
	V_{GS} = –3 V	T_A = 25°C	±0.5	
		T_A = 125°C	±0.25	
	V_{GS} = –4.5 V	T_A = 25°C	±0.74	
		T_A = 125°C	±0.34	
	V_{GS} = –10 V	T_A = 25°C	±1.17	
		T_A = 125°C	±0.53	
Pulse drain current, I_D		T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S		T_A = 25°C	–1	A
Continuous total power dissipation		See Dissipation Rating Table		
Storage temperature range, T_{stg}			–55 to 150	°C
Operating junction temperature range, T_J			–40 to 150	°C
Operating free-air temperature range, T_A			–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	840 mW	6.71 mW/°C	538 mW	437 mW	169 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 149°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1120			UNIT
					MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250\ \mu A$		−1	−1.25	−1.50	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -12$ V				±100	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V,	$V_{GS} = 0$ V	T_J = 25°C			−0.5	µA
				T_J = 125°C			−10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A			180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A			291	400	
		$V_{GS} = -3$ V	$I_D = -0.2$ A			476	700	
		$V_{GS} = -2.7$ V				606	850	
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A			2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

static

PARAMETER		TEST CONDITIONS		TPS1120Y			UNIT
				MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250\ \mu A$		−1.25		V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V		−0.9		V
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A		180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A		291		
		$V_{GS} = -3$ V	$I_D = -0.2$ A		476		
		$V_{GS} = -2.7$ V			606		
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A		2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	TPS1120, TPS1120Y			UNIT
			MIN	TYP	MAX	
Q_g	Total gate charge	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -1$ A		5.45		nC
Q_{gs}	Gate-to-source charge			0.87		
Q_{gd}	Gate-to-drain charge			1.4		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D = -1$ A, $R_G = 6\ \Omega$, See Figures 1 and 2		4.5		ns
$t_{d(off)}$	Turn-off delay time			13		ns
t_r	Rise time			10		ns
t_f	Fall time			2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A, di/dt = 100 A/µs		16		

PARAMETER MEASUREMENT INFORMATION

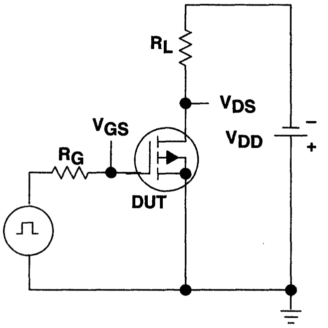


Figure 1. Switching-Time Test Circuit

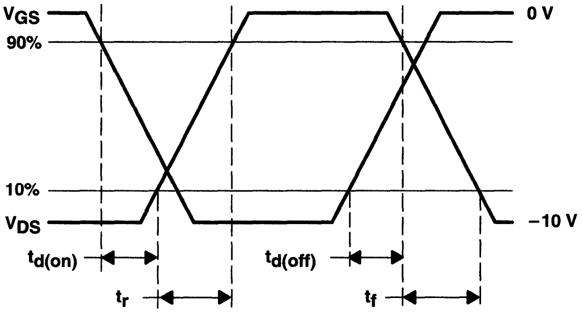


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

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Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

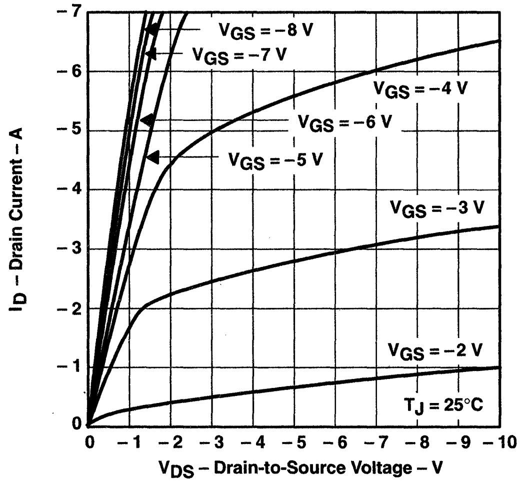

Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

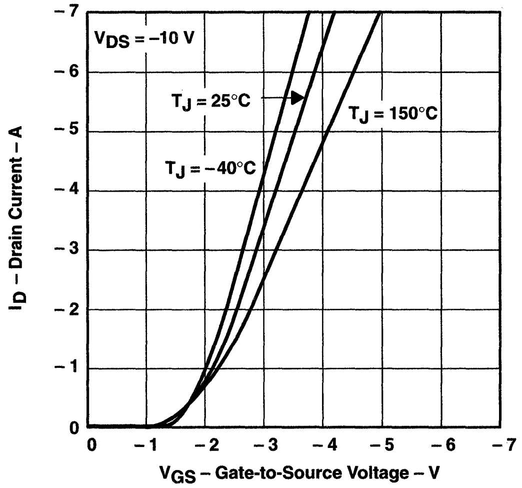

Figure 4

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† All characteristics data applies for each independent MOSFET incorporated on the TPS1120.

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

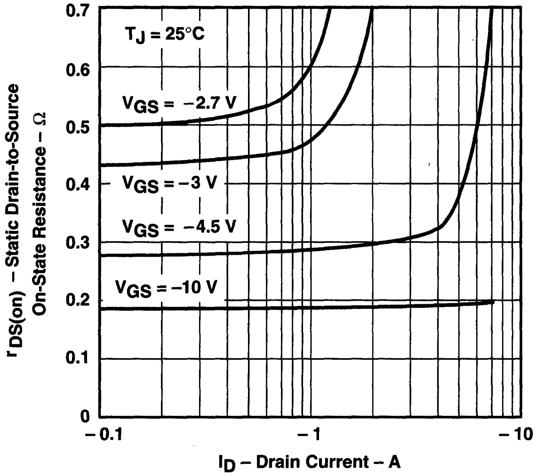
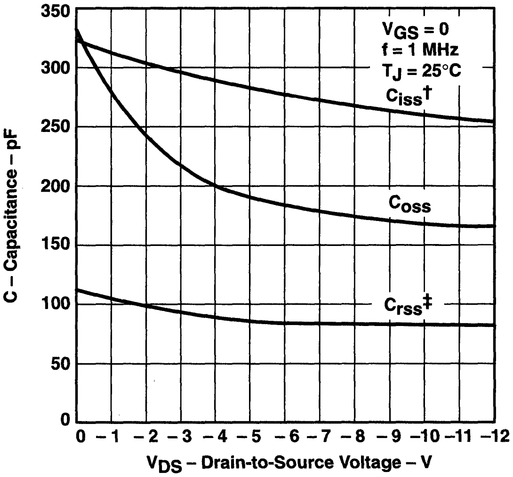


Figure 5

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd},\ C_{ds(shorted)}$

‡ $C_{rss} = C_{gd},\ C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

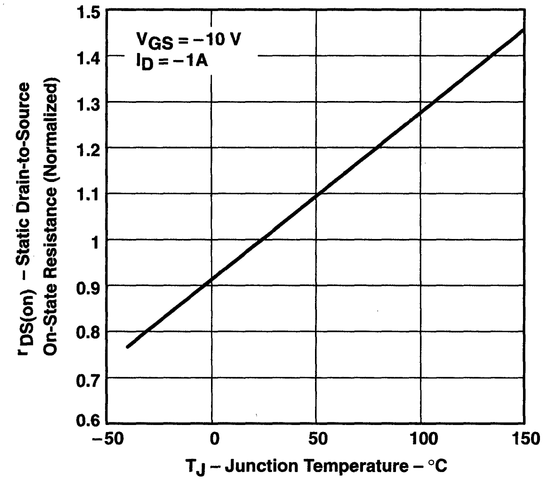


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

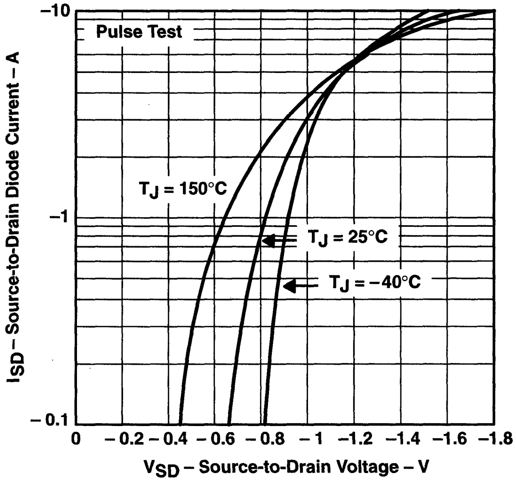


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

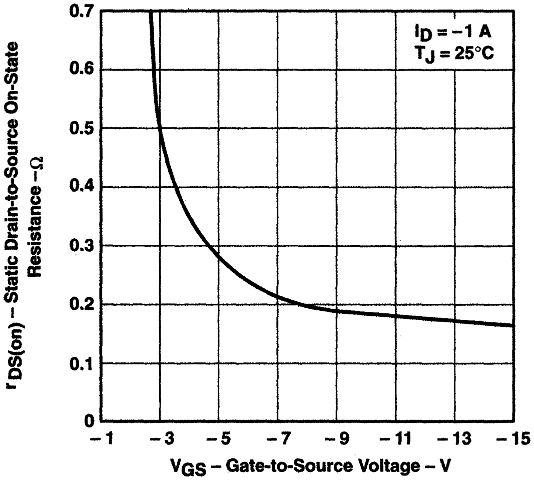


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

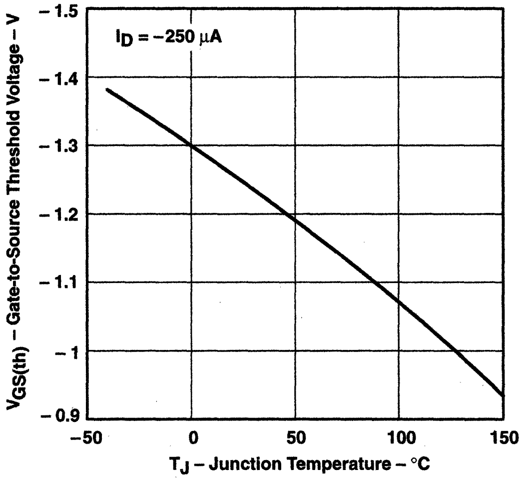


Figure 10

GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

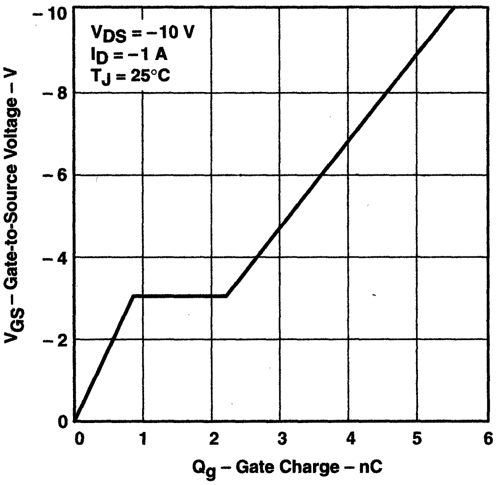


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

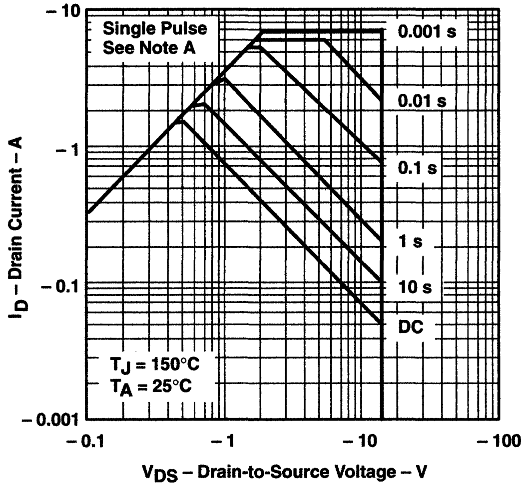


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT THERMAL IMPEDANCE
vs
PULSE DURATION

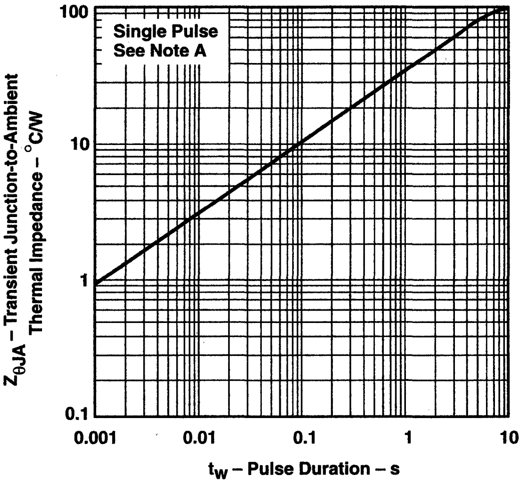


Figure 13

NOTE A: FR4-board-mounted only

THERMAL INFORMATION

The profile of the heat sinks used for thermal measurements is shown in Figure 14. Board type is FR4 with 1-oz copper and 1-oz tin/lead (63/37) plate. Use of vias or through-holes to enhance thermal conduction was avoided.

Figure 15 shows a family of $R_{\theta JA}$ curves. The $R_{\theta JA}$ was obtained for various areas of heat sinks while subject to air flow. Power remained fixed at 0.25 W per device or 0.50 W per package. This testing was done at 25°C.

As Figure 14 illustrates, there are two separated heat sinks for each package. Each heat sink is coupled to the lead that is internally tied to a single MOSFET source and is half the total area, as shown in Figure 15. For example, if the total area shown in Figure 15 is 4 cm^2, each heat sink is 2 cm^2.

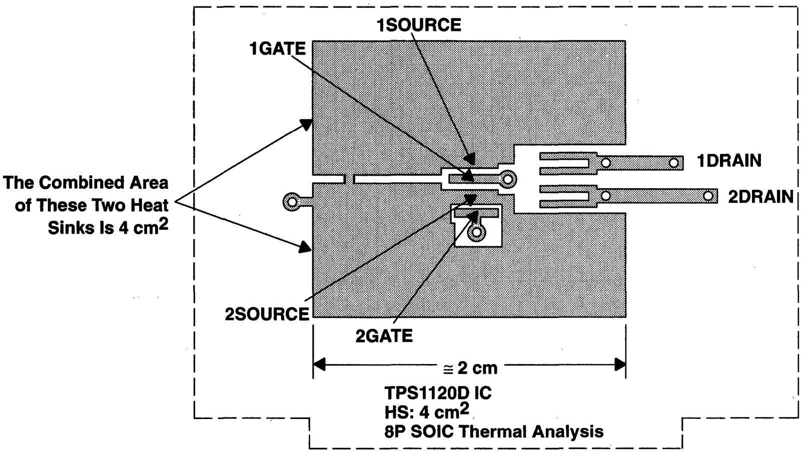


Figure 14. Profile of Heat Sinks

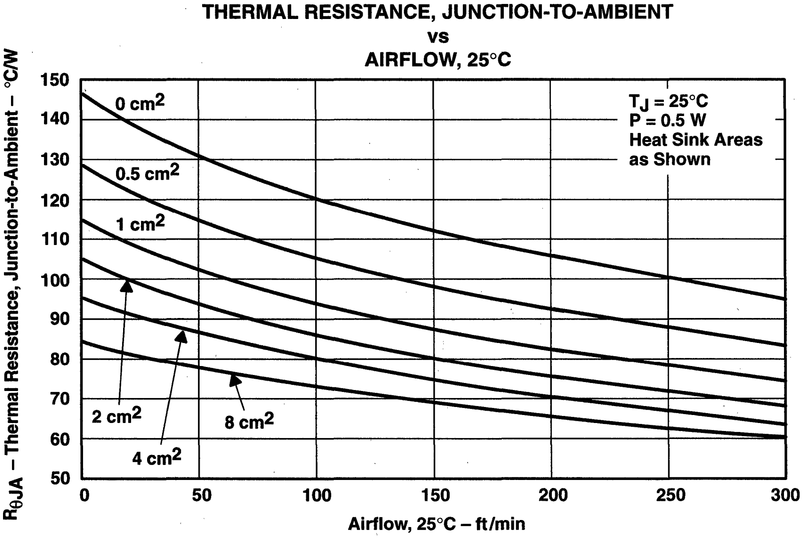


Figure 15

THERMAL INFORMATION

Figure 16 illustrates the thermally enhanced (SO) lead frame. Attaching the two MOSFET dies directly to the source terminals allows maximum heat transfer into a power plane.

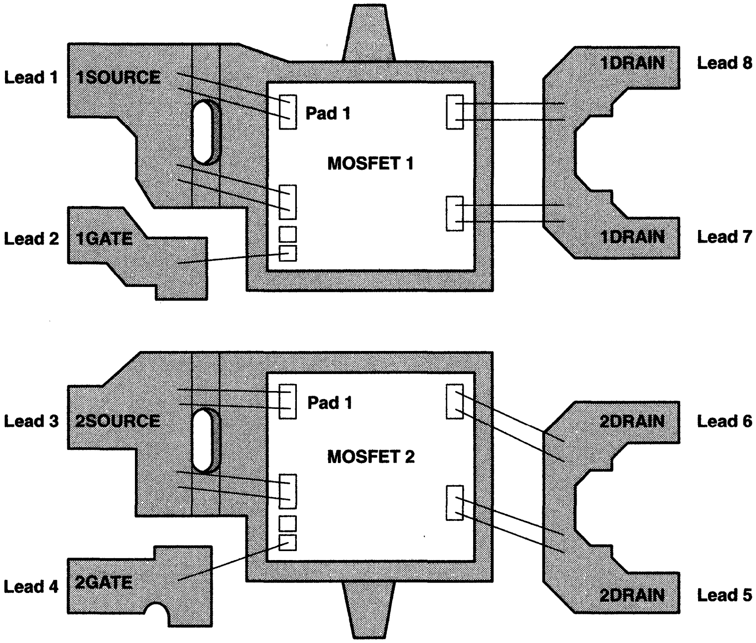


Figure 16. TPS1120 Dual MOSFET SO-8 Lead Frame

APPLICATION INFORMATION

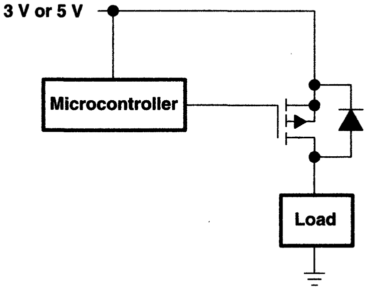


Figure 17. Notebook Load Management

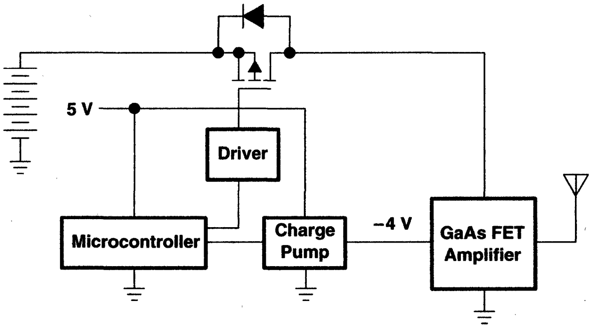


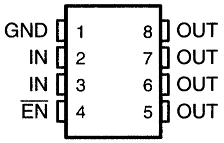
Figure 18. Cellular Phone Output Drive

TPS2010, TPS2011, TPS2012, TPS2013, TPS2010Y
POWER-DISTRIBUTION SWITCHES

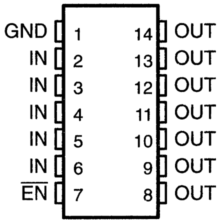
SLVS097A – DECEMBER 1994 – REVISED AUGUST 1995

- **95-mΩ Max (5.5-V Input) High-Side MOSFET Switch With Logic Compatible Enable Input**
- **Short-Circuit and Thermal Protection**
- **Typical Short-Circuit Current Limits:**
  0.4 A, TPS2010; 1.2 A, TPS2011;
  2 A, TPS2012; 2.6 A, TPS2013
- **Electrostatic-Discharge Protection, 12-kV Output, 6-kV All Other Terminals**
- **Controlled Rise and Fall Times to Limit Current Surges and Minimize EMI**
- **SOIC-8 Package Pin Compatible With the Popular Littlefoot™ Series When GND Is Connected**
- **2.7-V to 5.5-V Operating Range**
- **10-μA Maximum Standby Current**
- **Surface-Mount SOIC-8 and TSSOP-14 Packages**
- **–40°C to 125°C Operating Junction Temperature Range**

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TPS201x family of power-distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ N-channel MOSFET. Gate drive is provided by an internal driver and charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump operates at 100 kHz, requires no external components, and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short circuit is present, the TPS201x limits the output current to a safe level by switching into a constant-current mode. Continuous heavy overloads and short circuits increase power dissipation in the switch and cause the junction temperature to rise. If the junction temperature reaches approximately 180°C, a thermal protection circuit shuts the switch off to prevent damage. Recovery from thermal shutdown is automatic once the device has cooled sufficiently.

The members of the TPS201x family differ only in short-circuit current threshold. The TPS2010 is designed to limit at 0.4-A load; the other members of the family limit at 1.2 A, 2 A, and 2.6 A (see the available options table). The TPS201x family is available in 8-pin small-outline integrated circuit (SOIC) and 14-pin thin shink small-outline (TSSOP) packages and operates over a junction temperature range of –40°C to 125°C. Versions in the 8-pin SOIC package are drop-in replacements for Siliconix's Littlefoot™ power PMOS switches, except that GND must be connected.

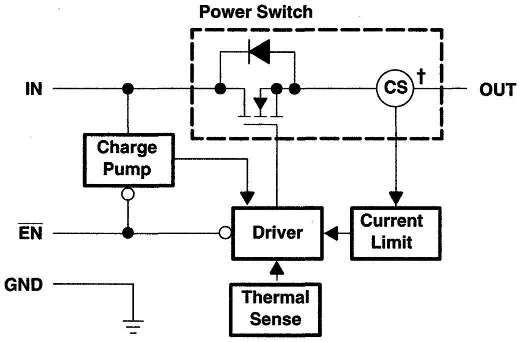
AVAILABLE OPTIONS

T_J	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT OUTPUT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES		CHIP FORM (Y)
			SOIC (D)†	TSSOP (PW)‡	
–40°C to 125°C	0.2	0.4	TPS2010D	TPS2010PWLE	TPS2010Y
	0.6	1.2	TPS2011D	TPS2011PWLE	TPS2011Y
	1	2	TPS2012D	TPS2012PWLE	TPS2012Y
	1.5	2.6	TPS2013D	TPS2013PWLE	TPS2013Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2010PWLE).

Littlefoot is a trademark of Siliconix.

functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D	PW		
$\overline{\text{EN}}$	4	7	I	Enable input. Logic low turns power switch on.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5–8	8–14	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5.5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{\text{EN}}$)

A logic high on the $\overline{\text{EN}}$ input turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET monitors the current supplied to the load. The sense FET is a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

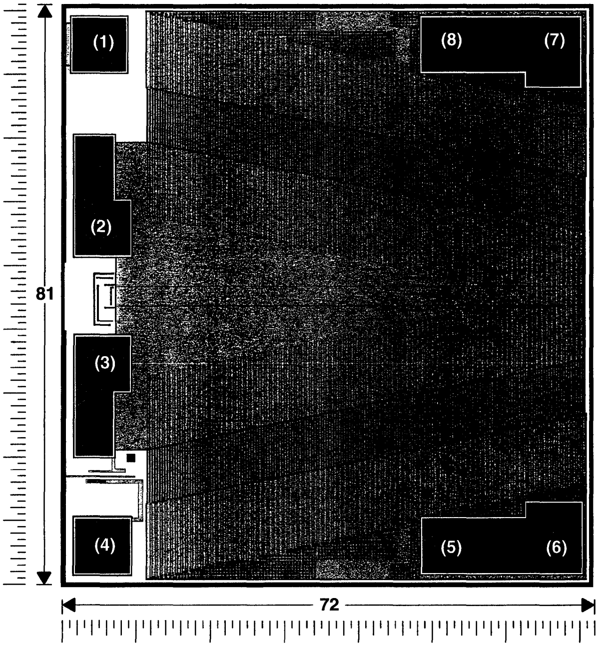
thermal sense

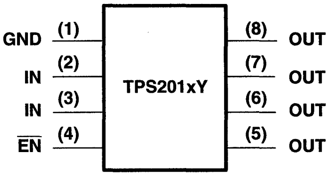
An internal thermal-sense circuit shuts the power switch off when the junction temperature rises to approximately 180°C. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

TPS201xY chip information

This chip, when properly assembled, displays characteristics similar to the TPS201xC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1)	−0.3 V to 7 V
Output voltage range, V_O (see Note 1)	−0.3 V to $V_{I(IN)}$ +0.3 V
Input voltage range, V_I at $\overline{EN}$	−0.3 V to 7 V
Continuous output current, I_O	internally limited
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$		2.7	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2010	0	0.2	A
	TPS2011	0	0.6	
	TPS2012	0	1	
	TPS2013	0	1.5	
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, I_O = rated current, $\overline{EN} = 0$ V (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
On-state resistance	$V_{I(IN)} = 5.5$ V, T_J = 25°C		75	95	mΩ
	$V_{I(IN)} = 4.5$ V, T_J = 25°C		80	110	
	$V_{I(IN)} = 3$ V, T_J = 25°C		120	175	
	$V_{I(IN)} = 2.7$ V, T_J = 25°C		140	215	
Output leakage current	$\overline{EN} = V_{I(IN)}$, T_J = 25°C		0.001	1	µA
	$\overline{EN} = V_{I(IN)}$, −40°C ≤ T_J ≤ 125°C			10	
t_r Output rise time	$V_{I(IN)} = 5.5$ V, T_J = 25°C, $C_L = 1$ µF		4		ms
	$V_{I(IN)} = 2.7$ V, T_J = 25°C, $C_L = 1$ µF		3.8		
t_f Output fall time	$V_{I(IN)} = 5.5$ V, T_J = 25°C, $C_L = 1$ µF		3.9		ms
	$V_{I(IN)} = 2.7$ V, T_J = 25°C, $C_L = 1$ µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER	TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
	2.7 V ≤ $V_{I(IN)}$ < 4.5 V			0.4	
Input current	$\overline{EN} = 0$ V or $\overline{EN} = V_{I(IN)}$	−0.5		0.5	µA
t_{PLH} Propagation (delay) time, low-to-high-level output	$C_L = 1$ µF			20	ms
t_{PHL} Propagation (delay) time, high-to-low-level output	$C_L = 1$ µF			40	

current limit

PARAMETER	TEST CONDITIONS†		TPS2010, TPS2011 TPS2012, TPS2013			UNIT
			MIN	TYP	MAX	
Short-circuit current	T_J = 25°C, $V_{I(IN)} = 5.5$ V, OUT connected to GND, device enabled into short circuit	TPS2010	0.22	0.4	0.6	A
		TPS2011	0.66	1.2	1.8	
		TPS2012	1.1	2	3	
		TPS2013	1.65	2.6	4.5	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN} = V_{I(IN)}$, T_J = 25°C		0.015	1	µA
	$\overline{EN} = V_{I(IN)}$, −40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	$\overline{EN} = 0$ V, T_J = 25°C		73	100	µA
	$\overline{EN} = 0$ V, −40°C ≤ T_J ≤ 125°C			100	

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V, T_J = 25°C (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y MIN	TYP	MAX	UNIT
On-state resistance	$V_{I(IN)}$ = 5.5 V,		75		mΩ
	$V_{I(IN)}$ = 4.5 V,		80		
	$V_{I(IN)}$ = 3 V,		120		
	$V_{I(IN)}$ = 2.7 V,		140		
Output leakage current	$\overline{EN} = V_{I(IN)}$		0.001		µA
Output rise time	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF		4		ms
	$V_{I(IN)}$ = 2.7 V, C_L = 1 µF		3.8		
Output fall time	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF		3.9		ms
	$V_{I(IN)}$ = 2.7 V, C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

current limit

PARAMETER	TEST CONDITIONS†	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y MIN	TYP	MAX	UNIT
Short-circuit current	$V_{I(IN)}$ = 5.5 V, OUT connected to GND, Device enabled into short circuit		0.4		A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y MIN	TYP	MAX	UNIT
Supply current, low-level output	$\overline{EN} = V_{I(IN)}$		0.015		µA
Supply current, high-level output	$\overline{EN}$ = 0 V		73		µA

PARAMETER MEASUREMENT INFORMATION

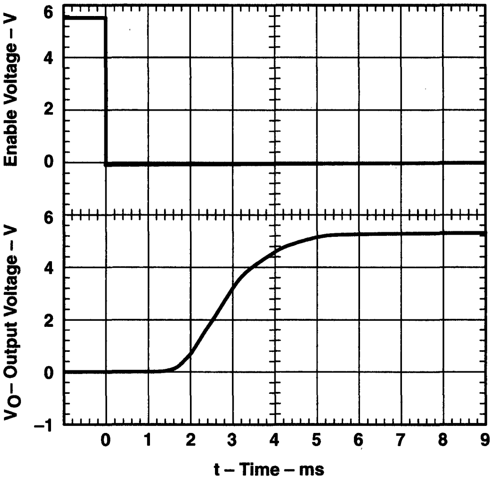


Figure 1. Propagation Delay and Rise Time With 1-µF Load, $V_{I(IN)}$ = 5.5 V

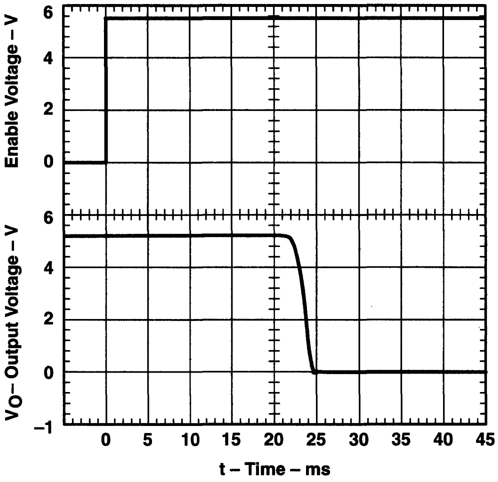


Figure 2. Propagation Delay and Fall Time With 1-µF Load, $V_{I(IN)}$ = 5.5 V

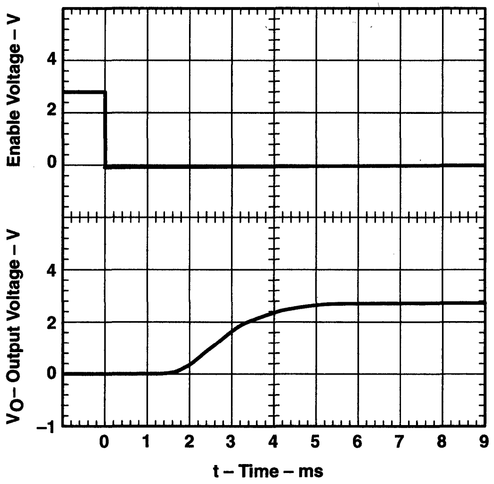


Figure 3. Propagation Delay and Rise Time With 1-µF Load, $V_{I(IN)}$ = 2.7 V

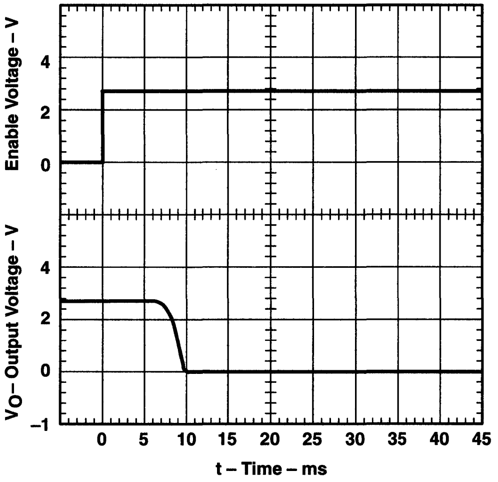


Figure 4. Propagation Delay and Fall Time With 1-µF Load, $V_{I(IN)}$ = 2.7 V

PARAMETER MEASUREMENT INFORMATION

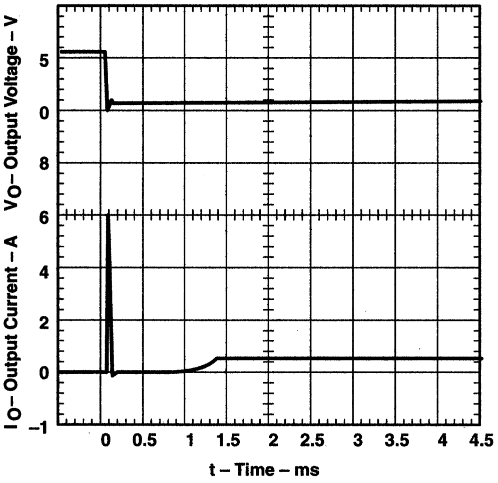


Figure 5. TPS2010, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

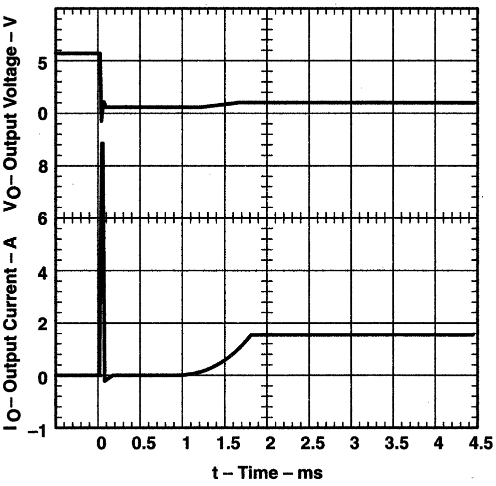


Figure 6. TPS2011, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

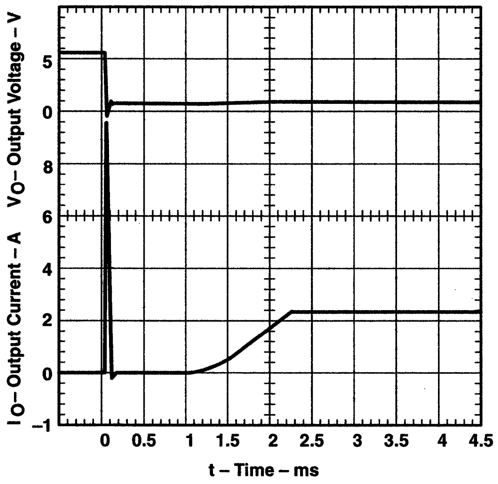


Figure 7. TPS2012, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

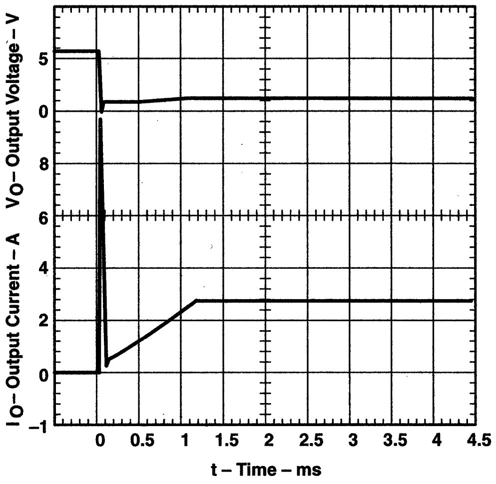


Figure 8. TPS2013 – Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

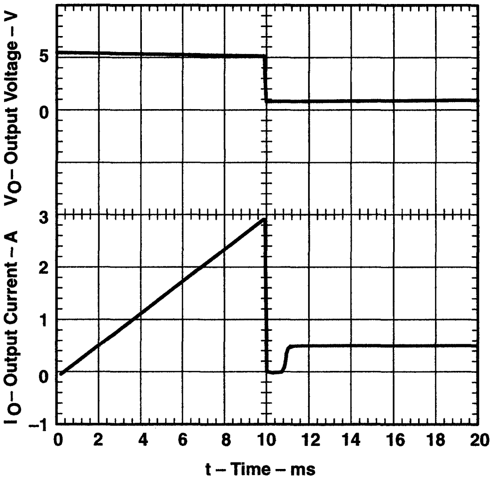


Figure 9. TPS2010 – Threshold Current, $V_{I(IN)}$ = 5.5 V

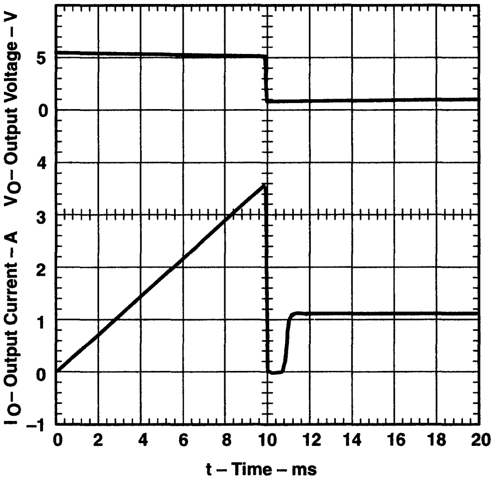


Figure 10. TPS2011 – Threshold Current, $V_{I(IN)}$ = 5.5 V

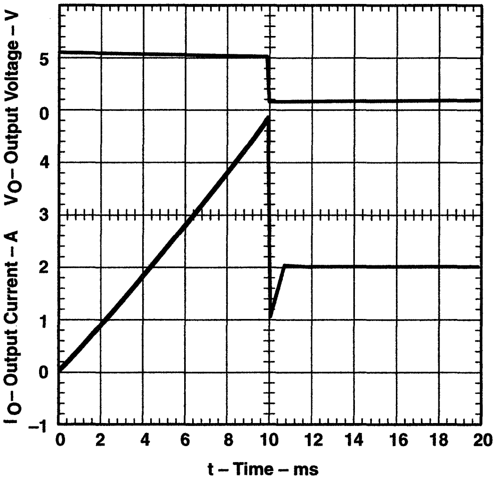


Figure 11. TPS2012 – Threshold Current, $V_{I(IN)}$ = 5.5 V

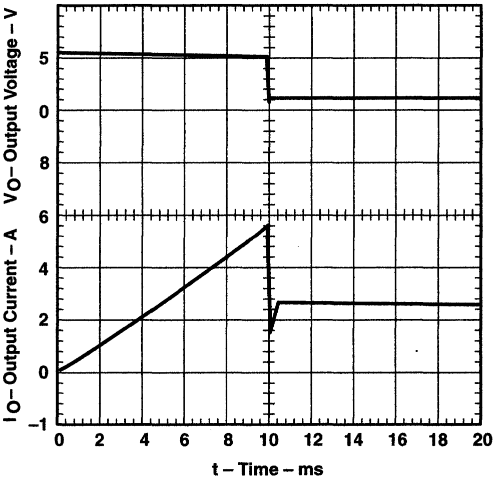


Figure 12. TPS2013 – Threshold Current, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

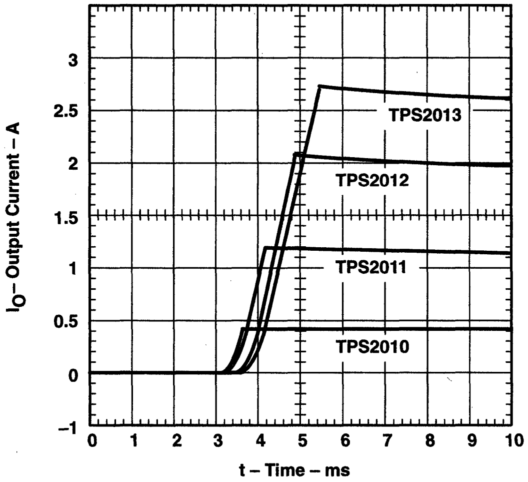
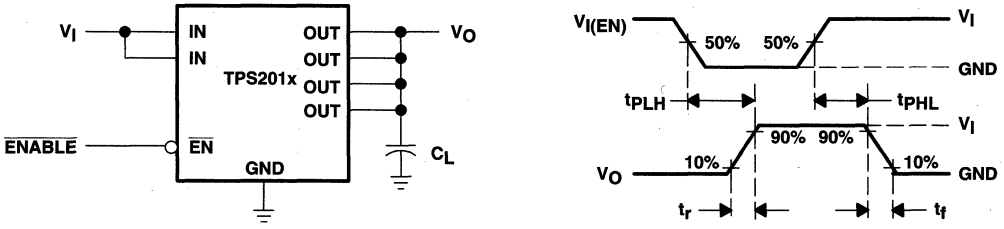


Figure 13. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 14. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME vs INPUT VOLTAGE

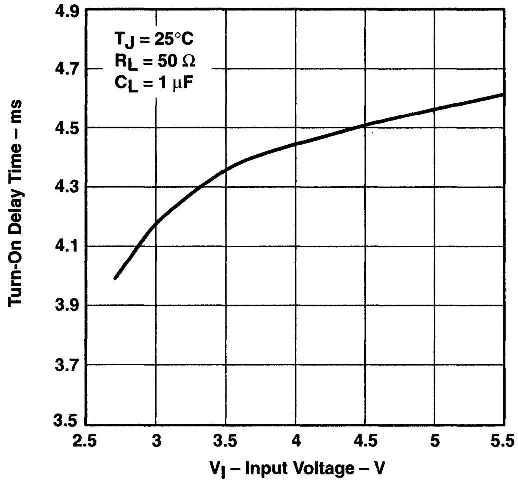


Figure 15

TURN-OFF DELAY TIME vs INPUT VOLTAGE

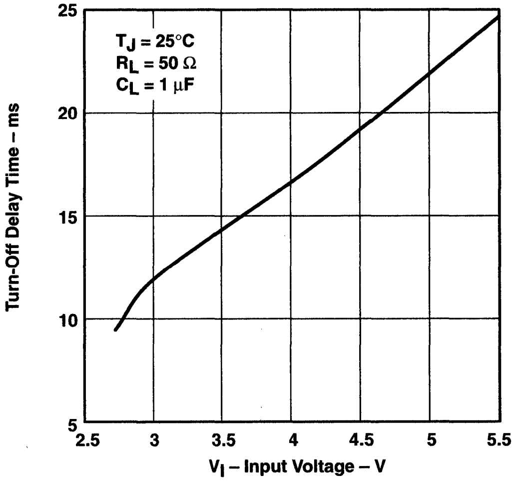


Figure 16

RISE TIME vs OUTPUT CURRENT

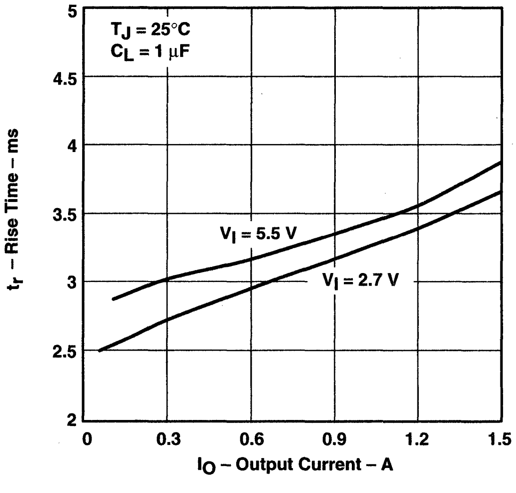


Figure 17

FALL TIME vs OUTPUT CURRENT

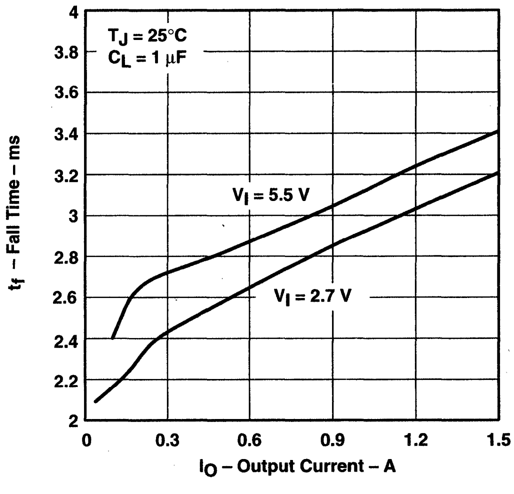


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (OUTPUT ENABLED)
vs
JUNCTION TEMPERATURE

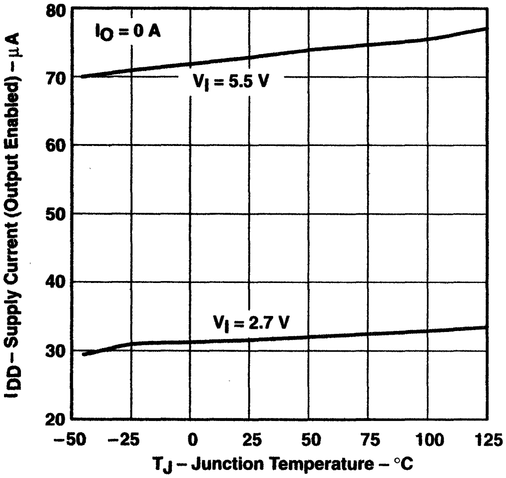


Figure 19

SUPPLY CURRENT (OUTPUT DISABLED)
vs
JUNCTION TEMPERATURE

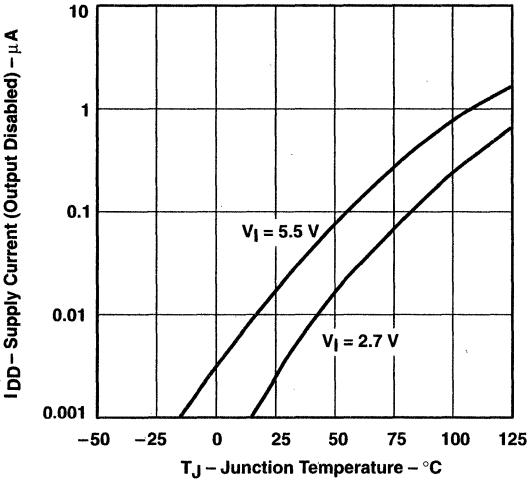


Figure 20

SUPPLY CURRENT (OUTPUT ENABLED)
vs
INPUT VOLTAGE

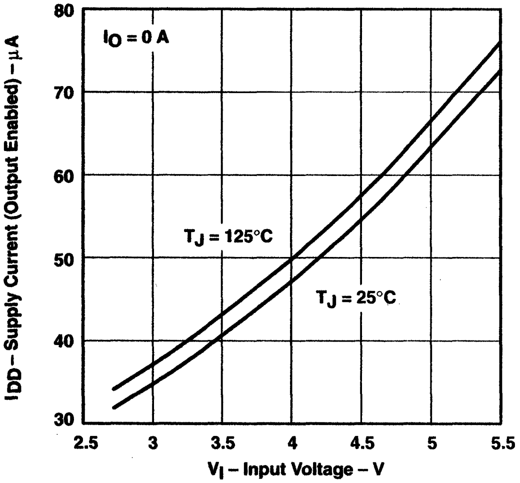


Figure 21

SUPPLY CURRENT (OUTPUT DISABLED)
vs
INPUT VOLTAGE

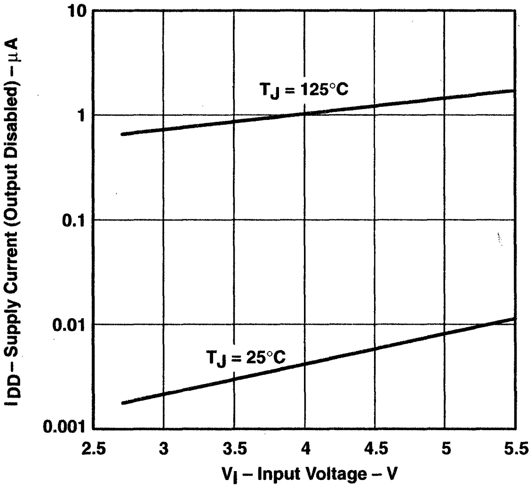


Figure 22

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

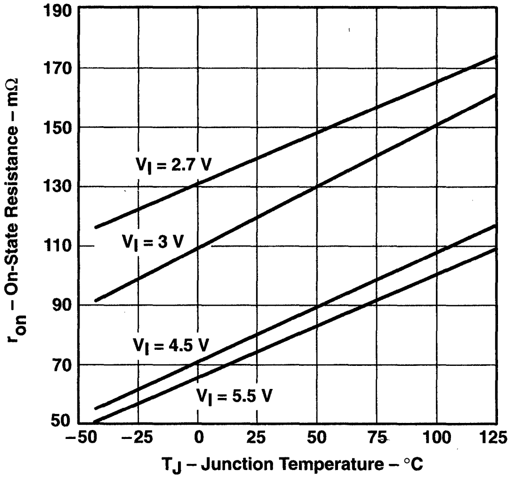


Figure 23

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

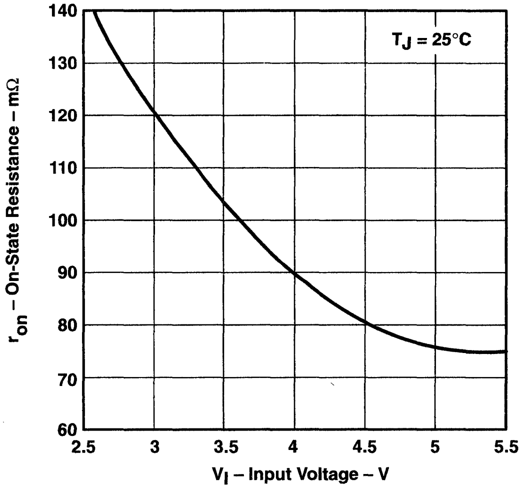


Figure 24

INPUT VOLTAGE TO OUTPUT VOLTAGE
vs
INPUT VOLTAGE

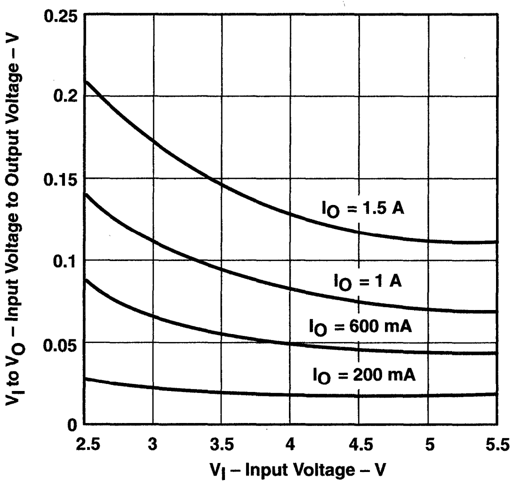


Figure 25

SHORT-CIRCUIT CURRENT
vs
INPUT VOLTAGE

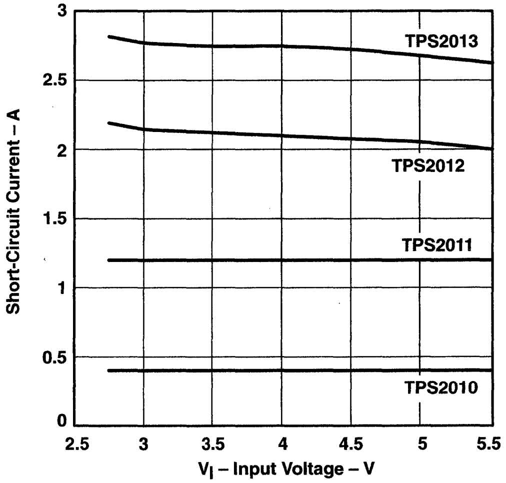


Figure 26

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

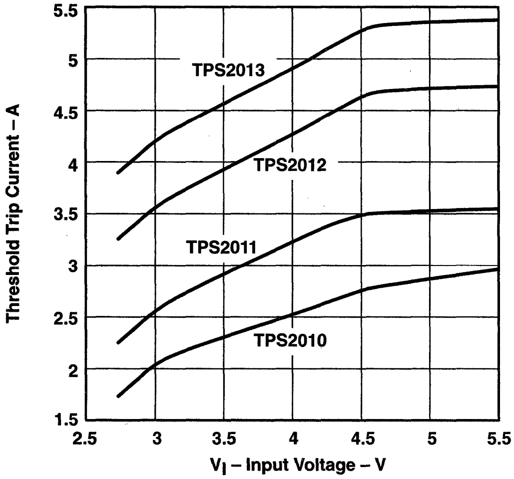


Figure 27

SHORT-CIRCUIT CURRENT vs JUNCTION TEMPERATURE

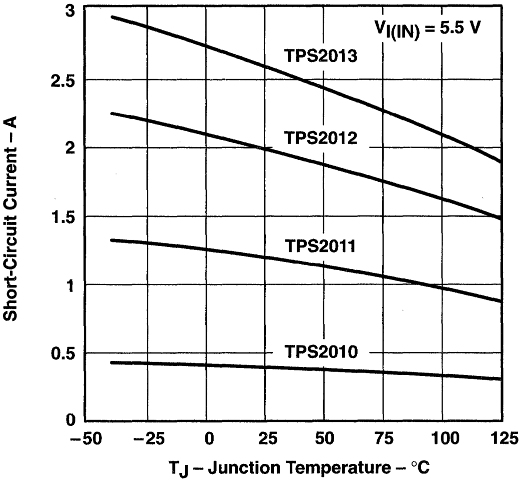


Figure 28

APPLICATION INFORMATION

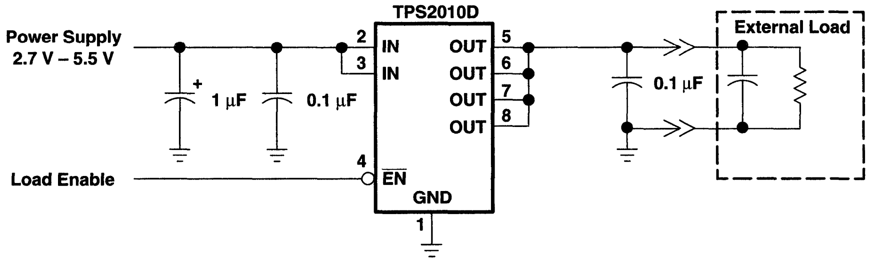


Figure 29. Typical Application

power supply considerations

The TPS201x family has multiple inputs and outputs, which must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.047-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 30). The TPS201x senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 5, 6, 7, and 8). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 9, 10, 11, and 12). The TPS201x family is capable of delivering currents up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

overcurrent (continued)

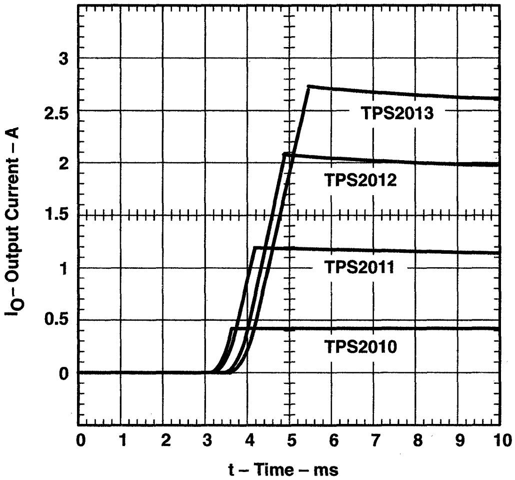


Figure 30. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V

power dissipation and junction temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages, such as SOIC or TSSOP to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, TSSOP = 179°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection is provided to prevent damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201x into its constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or input power is removed.

ESD protection

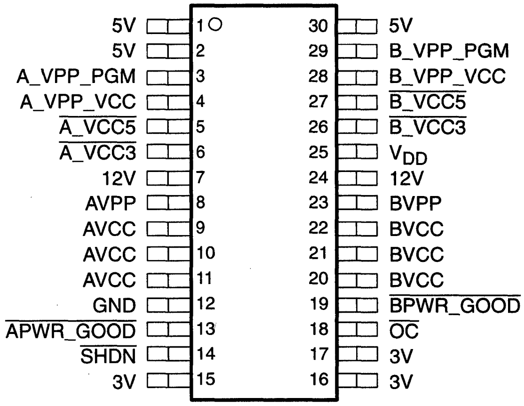
All TPS201x terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

TPS2201, TPS2201Y
DUAL-SLOT PC CARD POWER-INTERFACE SWITCHES FOR PARALLEL PCMCIA CONTROLLERS

SLVS094B – AUGUST 1994 – REVISED AUGUST 1995

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card Interface**
- **Compatible With Controllers From Cirrus, Intel, and Texas Instruments**
- **Meets PCMCIA Standards**
- **Internal Charge Pump (No External Capacitors Required) – 12-V Supply Can Be Disabled Except for Programming**
- **Short Circuit and Thermal Protection**
- **Space Saving SSOP (DB) Package**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Power Saving I_{DD} = 83 μA Typ, I_Q = 1 μA**
- **Low $r_{DS(on)}$ (160-mΩ V_{CC} Switch)**
- **Break-Before-Make Switching**

DB OR DF PACKAGE
(TOP VIEW)

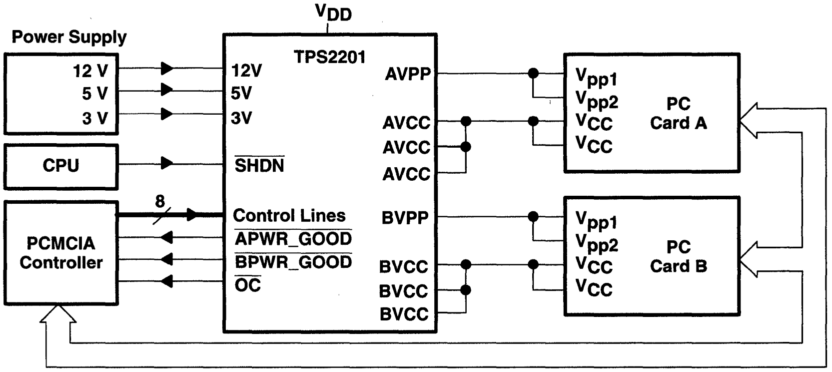


description

The TPS2201 PC Card (PCMCIA) power interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, thermal protection, and power-good reporting for PC Card control are combined on a single integrated circuit (IC), using Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3-V, 5-V and/or 12-V card power and is compatible with most PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability; current-limit reporting can help the user isolate a system fault to a bad card.

The TPS2201 maximizes battery life by generating its own switch-drive voltage using an internal charge pump. Therefore, the 12-V supply can be powered down and only brought out of standby when flash memory needs to be written to or erased. End equipment for the TPS2201 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handiterminals, and bar-code scanners.

typical PC card power distribution application



LinBiCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES		CHIP FORM (Y)
	SHINK SMALL-OUTLINE (DB)	SMALL-OUTLINE (DF)	
−40°C to 150°C	TPS2201IDB	TPS2201IDF	TPS2201Y

† The DF package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2201IDFLE).

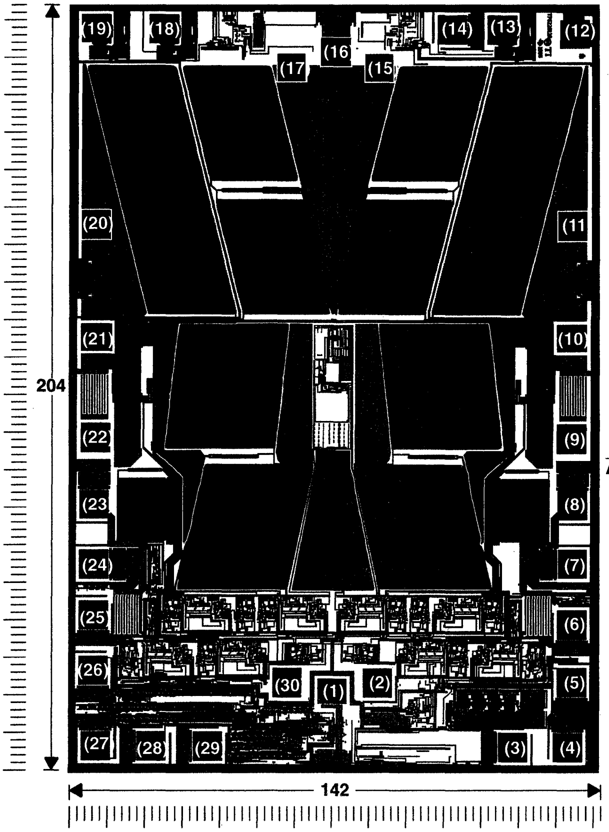
Terminal Functions

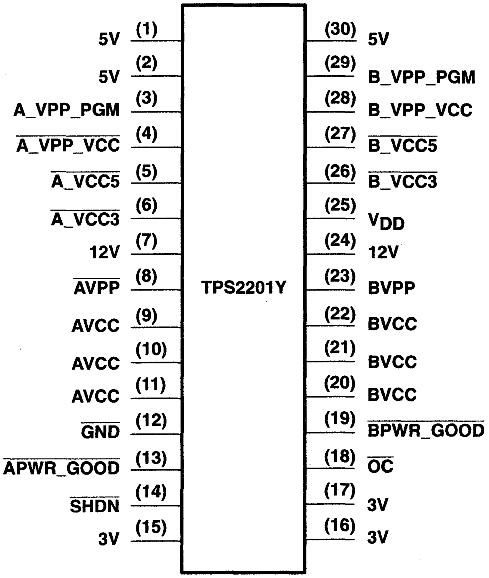
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{A\_VCC3}}$	6	I	Logic input that controls voltage on AVCC (see control-logic table)
$\overline{\text{A\_VCC5}}$	5	I	Logic input that controls voltage on AVCC (see control-logic table)
A_VPP_PGM	3	I	Logic input that controls voltage on AVPP (see control-logic table)
A_VPP_VCC	4	I	Logic input that controls voltage on AVPP (see control-logic table)
$\overline{\text{APWR\_GOOD}}$	13	O	Logic-level power-ready output that stays low as long as AVPP is within limits
AVCC	9, 10, 11	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
AVPP	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{B\_VCC3}}$	26	I	Logic input that controls voltage on BVCC (see control-logic table)
$\overline{\text{B\_VCC5}}$	27	I	Logic input that controls voltage on BVCC (see control-logic table)
B_VPP_PGM	29	I	Logic input that controls voltage on BVPP (see control-logic table)
B_VPP_VCC	28	I	Logic input that controls voltage on BVPP (see control-logic table)
$\overline{\text{BPWR\_GOOD}}$	19	O	Logic-level power-ready output that stays low as long as BVPP is within limits
BVCC	20, 21, 22	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{SHDN}}$	14	I	Logic input that shuts down the TPS2201 and set all power outputs to high-impedance state
$\overline{\text{OC}}$	18	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
V_{DD}	25		5-V power to chip
GND	12		Ground
3V	15, 16, 17	I	3-V V_{CC} input for card power
5V	1, 2, 30	I	5-V V_{CC} input for card power
12V	7, 24	I	12-V VPP input for card power

TPS2201Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS2201. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}	−0.3 V to 7 V
Input voltage range for card power: $V_{I(5V)}$	−0.3 V to 7 V
$V_{I(3V)}$	−0.3 V to $V_{I(5V)}$
$V_{I(12V)}$	−0.3 V to 14 V
Logic input voltage	−0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$	internally limited
$I_{O(xVPP)}$	internally limited
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW	532 mW
DF	1158 mW	9.26 mW/°C	741 mW	602 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 108°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.75	5.25	V
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3V)}$	0	$V_{I(5V)}$†	V
	$V_{I(12V)}$	0	13.5	V
Output current, I_O	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Operating virtual junction temperature, T_J		−40	125	°C

† $V_{I(3\,V)}$ should not be taken above $V_{I(5\,V)}$.

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

dc characteristics

PARAMETER		TEST CONDITIONS	TPS2201			UNIT
			MIN	TYP	MAX	
Switch resistances	5 V to xVCC				160	mΩ
	3 V to xVCC				225	
	5 V to xVPP				6	Ω
	3 V to xVPP				6	
	12 V to xVPP				1	
Clamp low voltage		I_{PP} at 10 mA			0.8	V
Clamp low voltage		I_{CC} at 10 mA			0.8	V
Leakage current	I_{PP} High-impedance state	T_A = 25°C		1	10	µA
		T_A = 85°C			50	
	I_{CC} High-impedance state	T_A = 25°C		1	10	
		T_A = 85°C			50	
Input current	I_{DD}	$V_{O(AVCC)} = V_{O(BVCC)} = 5$ V, $V_{O(AVPP)} = V_{O(BVPP)} = 12$ V		83	150	µA
	I_{DD} in shutdown	$V_{O(BVCC)} = V_{O(AVCC)} = V_{O(AVPP)}$ $= V_{O(BVPP)} =$ high Z			1	µA
Power-ready threshold, $\overline{\text{PWR\_GOOD}}$			10.72	11.05	11.4	V
Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$ (12-V mode)				50		mV
Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output shorted to GND	0.75	1.3	1.9	A
	$I_{O(xVPP)}$		120	200	400	mA

logic section

PARAMETER	TEST CONDITIONS	TPS2201		UNIT
		MIN	MAX	
Logic input current			1	µA
Logic input high level		2.7		V
Logic input low level			0.8	V
Logic output high level	I_O = 1 mA	$V_{DD}-0.4$		V
Logic output low level			0.4	V

switching characteristics†

PARAMETER		TEST CONDITIONS		TPS2201			UNIT
				MIN	TYP	MAX	
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		ms
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1‡)	$V_{I(x\_VPP\_PGM)}$ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		
		$V_{I(\overline{x\_VCC3})}$ to xVCC (3 V)	t_{on}		5.8		ms
			t_{off}		28		
		$V_{I(\overline{x\_VCC5})}$ to xVCC (5 V)	t_{on}		4		ms
			t_{off}		30		

† Refer to Parameter Measurement Information
‡ Rise and fall times are with C_L = 100 µF.

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted) (continued)

dc characteristics

PARAMETER		TEST CONDITIONS	TPS2201Y			UNIT
			MIN	TYP	MAX	
Leakage current	I_{PP} High-impedance state			1		µA
	I_{CC} High-impedance state			1		
Input current	I_{DD}	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V		83		µA
Power-ready threshold, $\overline{\text{PWR\_GOOD}}$				11.05		V
Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$ (12-V mode)				50		mV

switching characteristics[†]

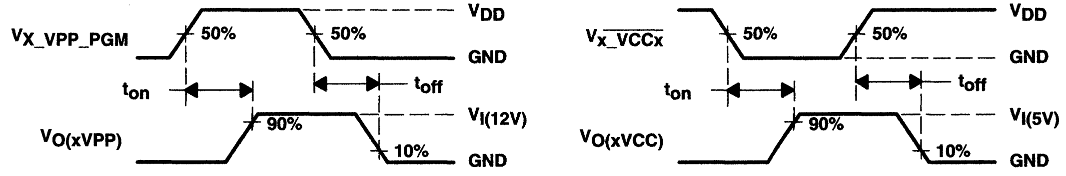
PARAMETER		TEST CONDITIONS		TPS2201Y			UNIT
				MIN	TYP	MAX	
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		ms
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1[‡])	$V_{I(x\_VPP\_PGM)}$ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		
		$V_{I(\overline{x\_VCC3})}$ to xVCC	t_{on}		5.8		ms
			t_{off}		28		
		$V_{I(\overline{x\_VCC5})}$ to xVCC	t_{on}		4		ms
			t_{off}		30		

[†] Refer to Parameter Measurement Information

[‡] Rise and fall times are with C_L = 100 µF.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT LOAD CIRCUIT



VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS

Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

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PARAMETER MEASUREMENT INFORMATION

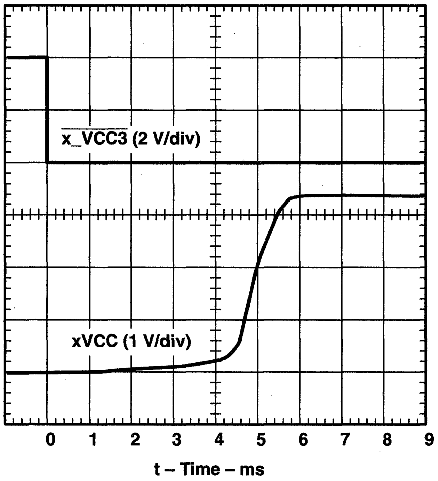

Figure 2. xVCC Propagation Delay and Rise Times With 1-µF Load, 3-V Switch

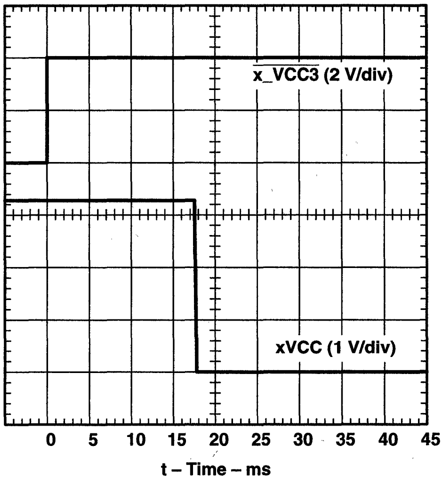

Figure 3. xVCC Propagation Delay and Fall Times With 1-µF Load, 3-V Switch

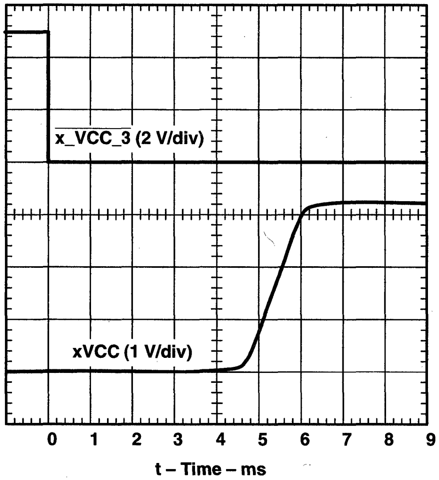

Figure 4. xVCC Propagation Delay and Rise Times With 100-µF Load, 3-V Switch

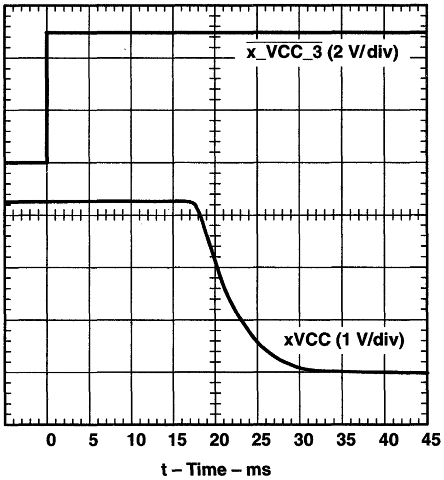

Figure 5. xVCC Propagation Delay and Fall Times With 100-µF Load, 3-V Switch

PARAMETER MEASUREMENT INFORMATION

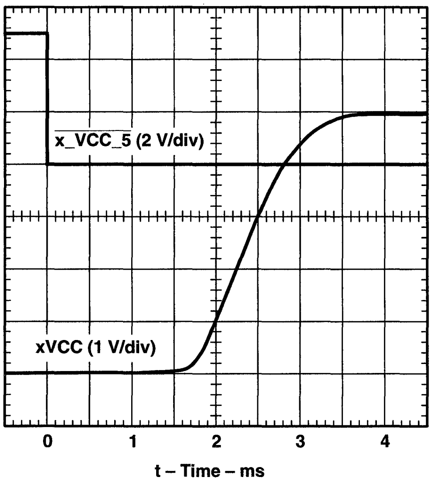

Figure 6. xVCC Propagation Delay and Rise Times With 1-µF Load, 5-V Switch

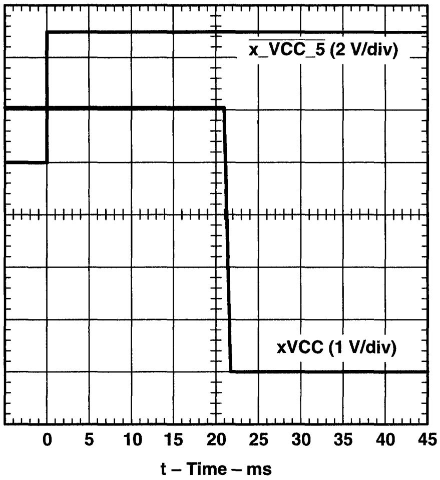

Figure 7. xVCC Propagation Delay and Fall Times With 1-µF Load, 5-V Switch

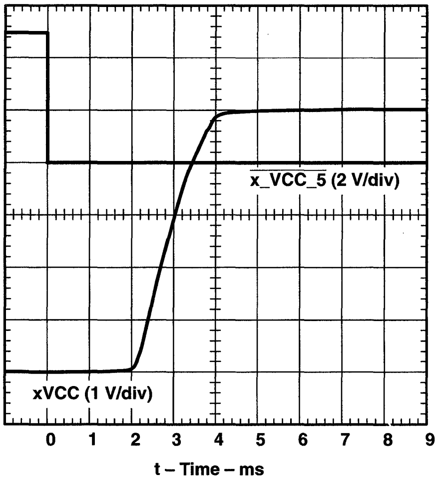

Figure 8. xVCC Propagation Delay and Rise Times With 100-µF Load, 5-V Switch

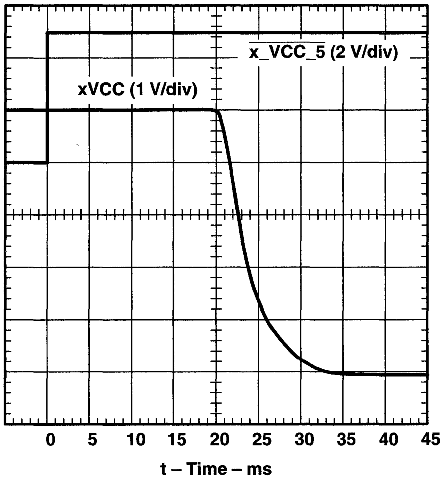

Figure 9. xVCC Propagation Delay and Fall Times With 100-µF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

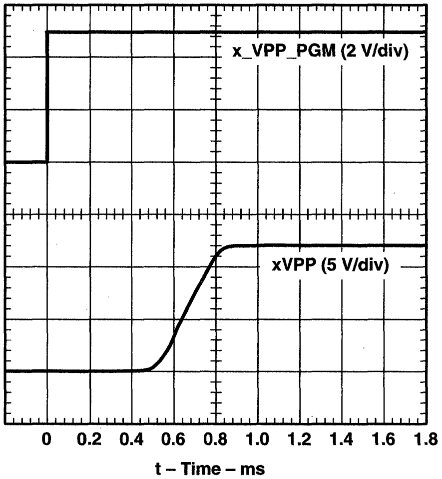

Figure 10. xVPP Propagation Delay and Rise Times With 1-µF Load, 12-V Switch

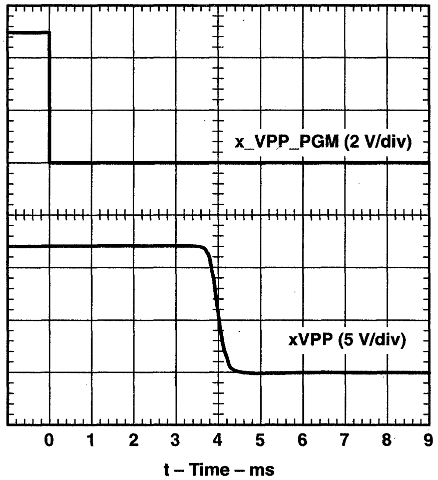

Figure 11. xVPP Propagation Delay and Fall Times With 1-µF Load, 12-V Switch

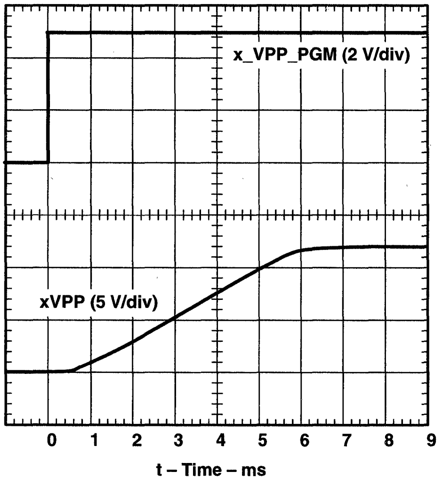

Figure 12. xVPP Propagation Delay and Rise Times With 100-µF Load, 12-V Switch

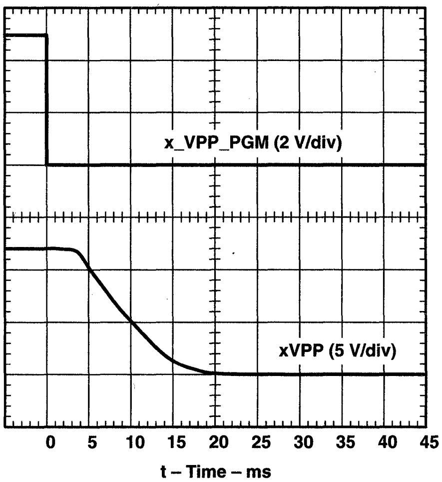

Figure 13. xVPP Propagation Delay and Fall Times With 100-µF Load, 12-V Switch

TYPICAL CHARACTERISTICS†

Table of Graphs

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$r_{DS(on)}$	Static drain-source on-state resistance, 3-V switch	vs Junction temperature	15
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V switch	vs Junction temperature	16
$r_{DS(on)}$	Static drain-source on-state resistance, 12-V switch	vs Junction temperature	17
$V_{O(xVCC)}$	Output voltage, 5-V switch	vs Output current	18
$V_{O(xVCC)}$	Output voltage, 3-V switch	vs Output current	19
xV_{pp}	Output voltage, V_{pp} switch	vs Output current	20
$I_{SC(xVCC)}$	Short-circuit current, 5-V switch	vs Junction temperature	21
$I_{SC(xVPP)}$	Short-circuit current, 12-V switch	vs Junction temperature	22

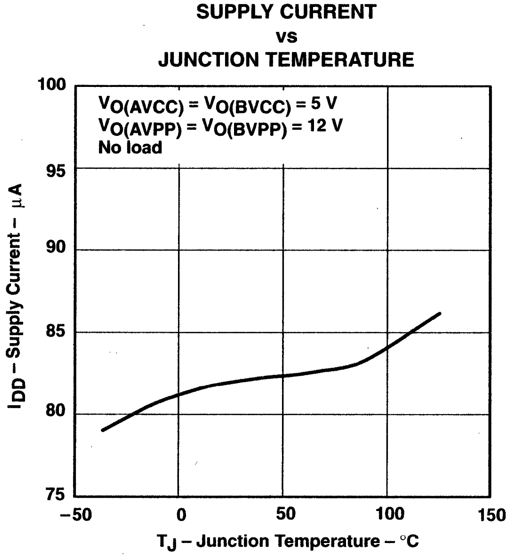

Figure 14

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† t = pulse tested

TYPICAL CHARACTERISTICS†

3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

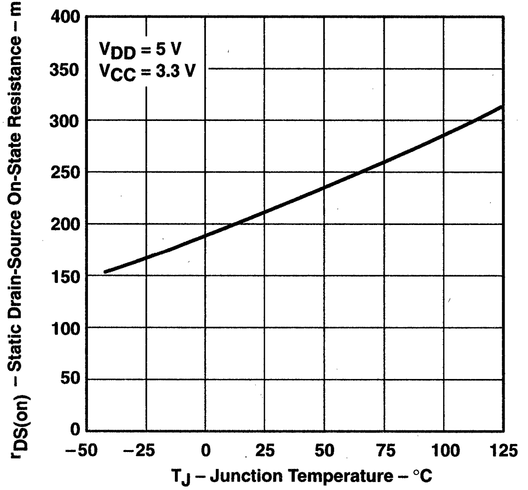

Figure 15

5-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

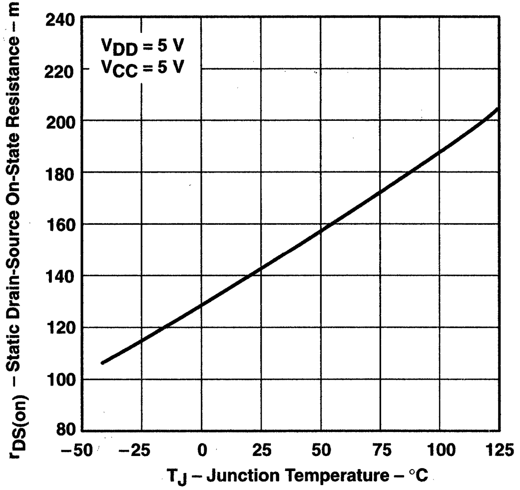

Figure 16

12-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

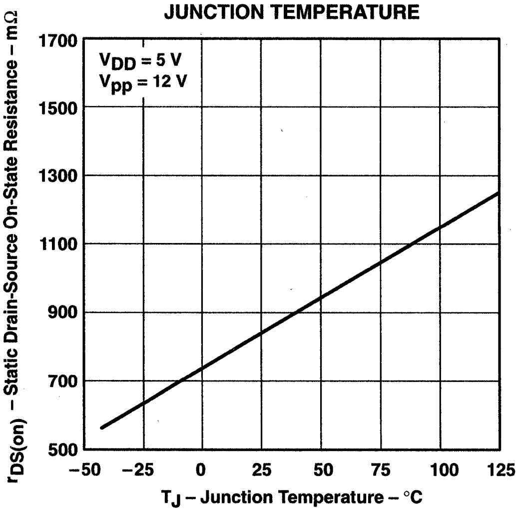

Figure 17

5-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

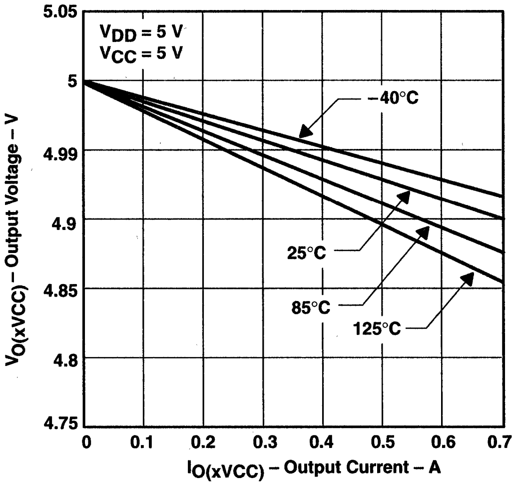

Figure 18

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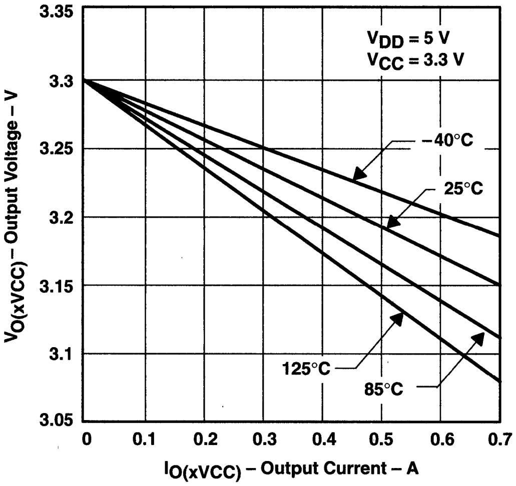
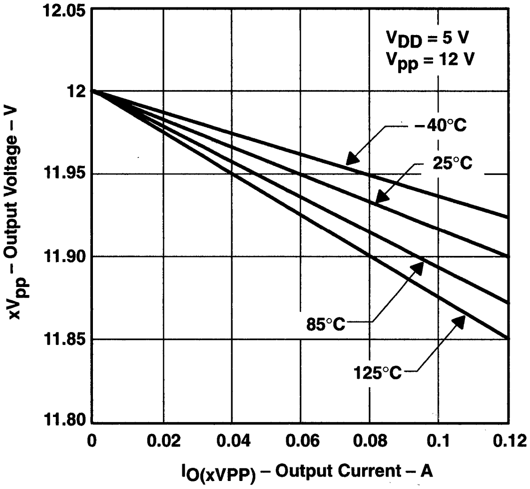
† t = pulse tested

TYPICAL CHARACTERISTICS†



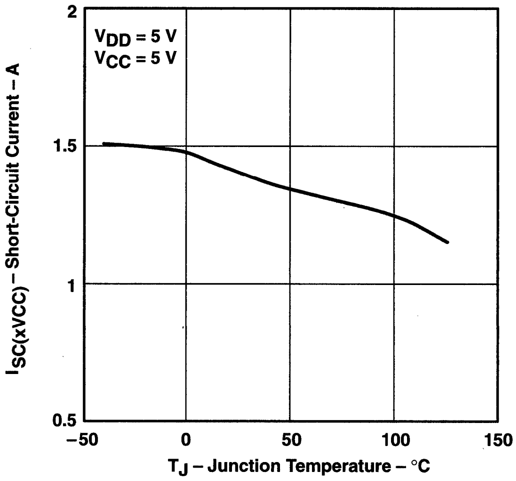
3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 19



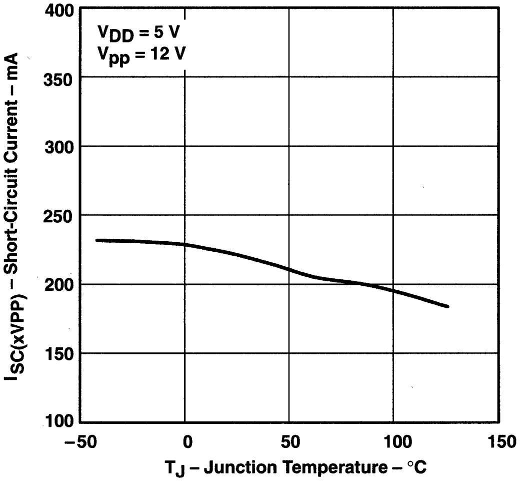
V_{pp} SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 20



5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

Figure 21



12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

Figure 22

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† t = pulse tested

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold: modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established and was comprised of members from leading computer, software, PC card, and semiconductor manufacturers. One key goal was to realize the concept of plug and play – cards and hosts from different vendors should be compatible and able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the PC Card connector's 68 pins. This power interface consists of two V_{CC}, two V_{pp}, and four ground pins. Multiple V_{CC} and ground pins are used to minimize connector-pin and line resistance. The two V_{pp} pins were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} pins; flash-memory programming and erase voltage is supplied through the V_{pp} pins. As each pin is rated to 0.5 A, V_{CC} and V_{pp} can theoretically supply up to 1 A, assuming equal pin resistance and no pin failure. A conservative design would limit current to 500 mA. Some applications, however, require higher V_{CC} currents; disk drives, for example, may need as much as 750-mA peak current to create the initial torque necessary to spin up the platter. V_{pp} currents, on the other hand, are defined by flash-memory programming requirements, typically under 120 mA.

future power trends

The 1-A physical-pin current alluded to in the PC Card specification has caused some host-system engineers to believe they are required to deliver 1 A within the voltage tolerance of the card. Future applications, such as RF cards, could use the extra power for their radio transmitters. The 5 W required for these cards will require very robust power supplies and special cooling considerations. The limited number of host sockets that will be able to support them makes the market for these high-powered PC Cards uncertain. The vast majority of the cards require less than 600 mA continuous current and the trend is towards even lower-powered PC Cards that will assure compatibility with a greater number of host systems. Recognizing the need for power derating, an adhoc committee of the PCMCIA is currently working to limit the amount of steady-state dc current to the PC Card to something less than the currently implied 1 A. If a system is designed to support 1 A, then the switch $r_{DS(on)}$, power supply requirements, and PC Card cooling need to be carefully considered.

designing around 1-A delivery

Delivering 1 A means minimizing voltage (and power) losses across the PC Card power interface, which requires that designers trade off switch resistance and the cost associated with large-die (low $r_{DS(on)}$) MOSFET transistors. The PC Card standard requires that 5 V ±5%, or 3.3 V ±0.3 V be supplied to the card. The approximate 10% tolerance for the 3.3-V supply makes the 3.3-V $r_{DS(on)}$ less critical than the 5-V switch. A conservative approach is to allow 2% for voltage-regulator tolerance and 1% for etch- and terminal-resistance drops, which leaves 2% (100 mV) voltage drop for the 5-V switch, and at least 6% (198 mV) for the 3.3-V switch.

Calculating the $r_{DS(on)}$ necessary to support a 100 mV or 198 mV switch loss, using R = E/I and setting I = 1 A, the 5-V and 3.3-V switches would need to be 100 mΩ and 198 mΩ respectively. One solution would be to pay for a more expensive switch with lower $r_{DS(on)}$. A second, less expensive approach is to increase the headroom of the power supply–for example, to increase the 5-V supply 1.5% or to 5.075 ±2%. Working through the numbers once more, the 2% for the regulator plus 1 % for etch and terminal losses leaves 97% or 4.923 V. The allowable

APPLICATION INFORMATION

designing around 1-A delivery (continued)

voltage loss across the power distribution switch is now 4.923 V minus 4.750 V or 173 mV. Therefore, a switch with 173 mΩ or less could deliver 1 A or greater. Setting the power supply high is a common practice for delivering voltages to allow for system switch, connector, and etch losses and has a minimal effect on overall battery life. In the example above, setting the power supply 1.5% high would only decrease a 3-hour battery life by approximately 2.7 minutes, trivial when compared with the decrease in battery life when running a 5-W PC Card.

heat dissipation

A greater concern in delivering 1 A or 5 W is the ability of the host to dissipate the heat generated by the PC Card. For desktop computers the solution is simpler: locate the PC Card cage such that it receives convection cooling from the forced air of the fan. Notebooks and other handheld equipment will not be able to rely on convection, but must rely on conduction of heat away from the PC Card through the rails into the card cage. This is difficult because PC Card/card cage heat transfer is very poor. A typical design scenario would require the PC Card to be held at 60°C maximum with the host platform operating as high as 50°C. Preliminary testing reveals that a PC Card can have a 20°C rise, exceeding the 10°C differential in the example, when dissipating less than 2 W of continuous power. The 60°C temperature was chosen because it is the maximum operating temperature allowable by PC Card specification. Power handling requirements and temperature rises are topics of concern and are currently being addressed by the PCMCIA committee.

overcurrent and over-temperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. This can be particularly frustrating to the consumer who has already experienced problems with shortened battery life due to improper Nicad conditioning or memory effect. Most hosts include fuses for protection. The reliability of fused systems is poor, though, as blown fuses require troubleshooting and repair, usually by the manufacturer. The TPS2201 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have the added advantage that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2201 asserts a signal at $\overline{\text{OC}}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry engages, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{PP} power for switch-gate drive and other chip functions, requiring that it be present at all times. The TPS2201 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V V_{DD} supply; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the TPS2201 during a software shutdown, in which quiescent current drops to a maximum of 1 µA.

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2201 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the

APPLICATION INFORMATION

voltage transitioning requirement (continued)

capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2201 offers a selectable V_{CC} and V_{PP} ground state, per PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100 kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis will reveal that the RC time constant delays the required discharge time to over 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2201 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial controller interface. The TPS2201 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

power supply considerations

The TPS2201 has multiple terminals for each of its 3.3 V, 5 V, and 12 V power inputs and for the switched V_{CC} outputs. Any individual terminal can conduct the rated input or output current. Unless all terminals are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12 V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power terminals be paralleled for optimum operation. The V_{DD} input lead must be connected to the 5V input leads.

Although the TPS2201 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-µF or larger capacitor; doing so improves the immunity of the TPS2201 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2201 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance.

The TPS2201, unlike other PC Card power-interface switches, does not use the 12-V power supply for switching or other chip functions. Instead, an internal charge pump generates the necessary voltage from V_{DD}, allowing the 12-V input supply to be shut down except when the V_{pp} programming or erase voltage is needed. Careful system design making use of this feature reduces power consumption and extends battery lifetime.

The 3.3-V power input should not be taken higher than the 5-V input. Doing so, though nondestructive, results in high current flow into the device, and could result in abnormal operation. In any case, this occurrence indicates a malfunction of one input voltage or both, which should be investigated.

Similarly, no terminal should be taken below −0.3 V; forward biasing the parasitic-substrate diode results in substrate currents and unpredictable performance.

APPLICATION INFORMATION

overcurrent and thermal protection

The TPS2201 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2201 controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2201 engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2201 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to engage if powered up into a short in the range of 0.75 A to 1.9 A, typically at about 1.3 A; the V_{pp} outputs limit from 120 mA to 400 mA, typically around 200 mA. The protection circuitry acts by linearly limiting the current passing through the switch, rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating when the package power-dissipation ratings are exceeded. Thermal limiting, disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16, 17, and 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \cdot I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma\, P_D \cdot R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°\mathrm{C/W}$$

Compare the calculated junction temperature with the initial temperature estimate. If they are not within a few degrees of each other, reiterate using the calculated temperature as the initial estimate.

logic input and outputs

The TPS2201 was designed to be compatible with most popular PCMCIA controllers and current PCMCIA and JEIDA standards. However, some controllers require slightly counterintuitive connections to achieve desired output states. The TPS2201 control logic inputs $\overline{\text{A\_VCC3}}$, $\overline{\text{A\_VCC5}}$, $\overline{\text{B\_VCC3}}$ and $\overline{\text{B\_VCC5}}$ are defined active low (see Figure 23 and control-logic table). As such, they are directly compatible with the Cirrus Logic CL-PD6720 controller's logic outputs (see Figure 24). The TPS2201 separate V_{pp} power good indicators can be ORed together to provide a single input to the Cirrus controller.

APPLICATION INFORMATION

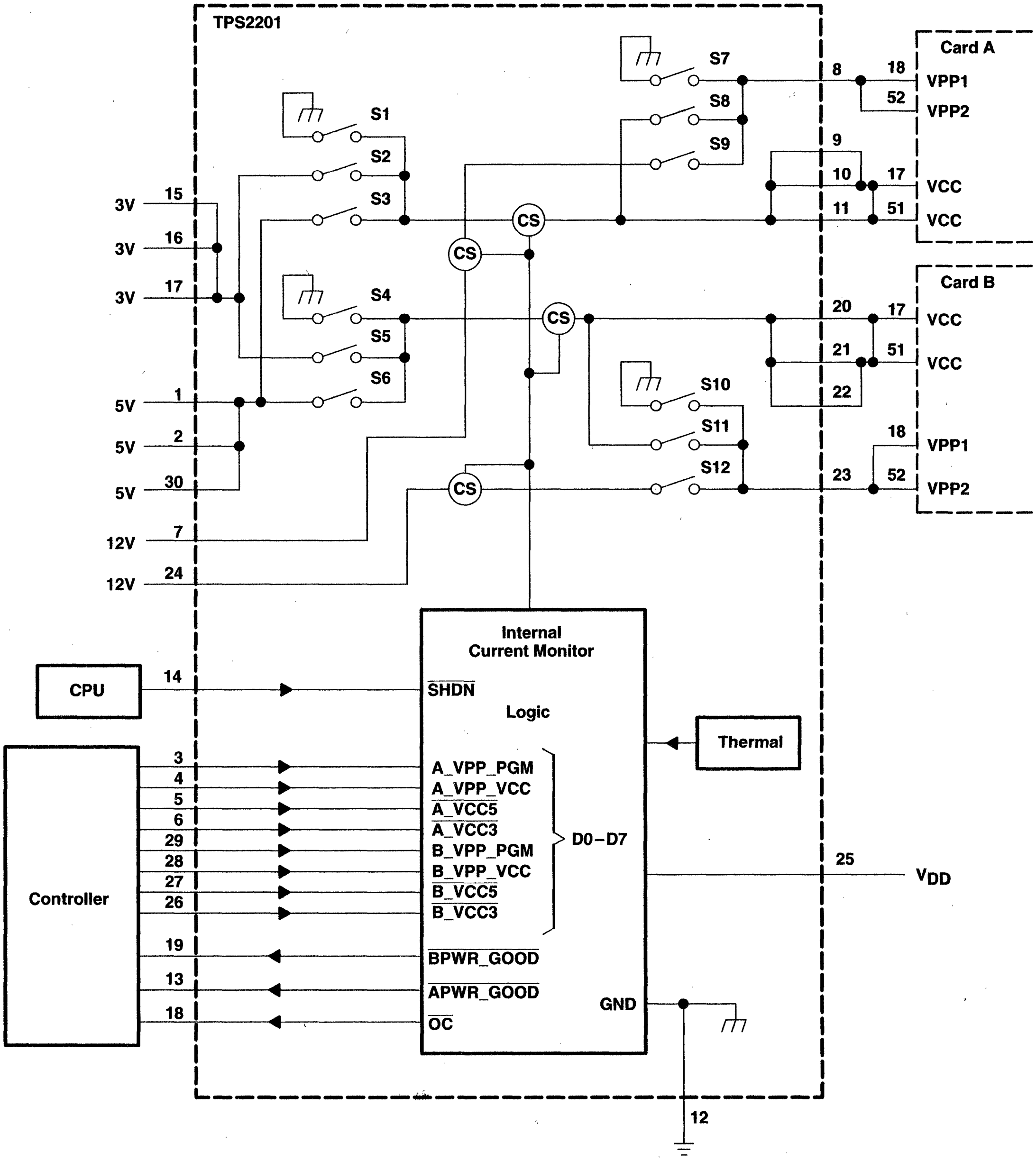


Figure 23. Internal Switching Matrix

APPLICATION INFORMATION

TPS2201 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	A_VPP_PGM	A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	B_VPP_PGM	B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC‡
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	$\overline{\text{A\_VCC3}}$	$\overline{\text{A\_VCC5}}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	$\overline{\text{B\_VCC3}}$	$\overline{\text{B\_VCC5}}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC
‡ Output depends on BVCC

APPLICATION INFORMATION

logic input and outputs (continued)

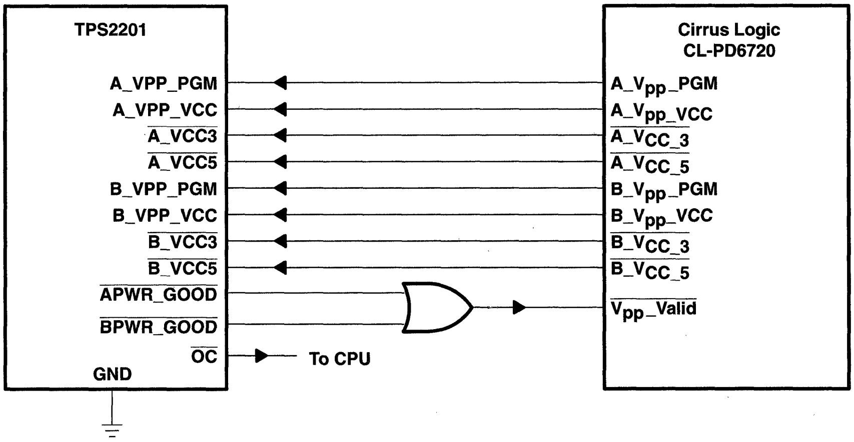


Figure 24. Logic Connections to CL-PD6720

Intel's 82365SLDF controller uses active-high control logic for V_{CC} selection, which requires connecting the 82365SLDF's 3-V control outputs (A_VCC_EN0, B_VCCEN0) to the TPS2201's 5-V control inputs ($\overline{\text{A\_VCC5}}$, $\overline{\text{B\_VCC5}}$) and the 5-V control outputs (AVCC_EN1, B_VCC_EN1) to the 3-V control inputs ($\overline{\text{A\_VCC3}}$, $\overline{\text{B\_VCC3}}$), as illustrated in Figure 25. Examination of the control logic tables on page 16 will confirm that these connections will in fact select the correct output voltage. An alternative approach would be to invert the Intel V_{CC} control logic signals before routing them to the TPS2201.

The separate V_{pp} power-good indicators of the TPS2201 can be connected directly to the Intel controller as shown in Figure 25.

Cirrus Logic defines a (1, 1) on the V_{CC} select lines to be the PC Card no connect state; Intel chose (0, 0) to select this state. As the tables show, either combination switches the V_{CC} outputs to 0 V. The decision to provide 0 V versus a high impedance for the no connect state eliminates potential charging at the switch-to-card interface. Feedback from the PC Card design community favors this approach.

V_{pp} logic allows for 0-V or high-impedance output for no connect (0, 0) or reserved (1, 1) logic inputs, respectively (refer to AVPP and BVPP control-logic tables on page 16). Both the Cirrus Logic and Intel controllers interface directly with the V_{pp} control inputs of the TPS2201.

The shutdown input of the TPS2201, $\overline{\text{SHDN}}$, when held at a logic low places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} supplies (see discussion above).

ESD protection

All TPS2201 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC card connector. Bypassing the outputs with 0.1-μF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

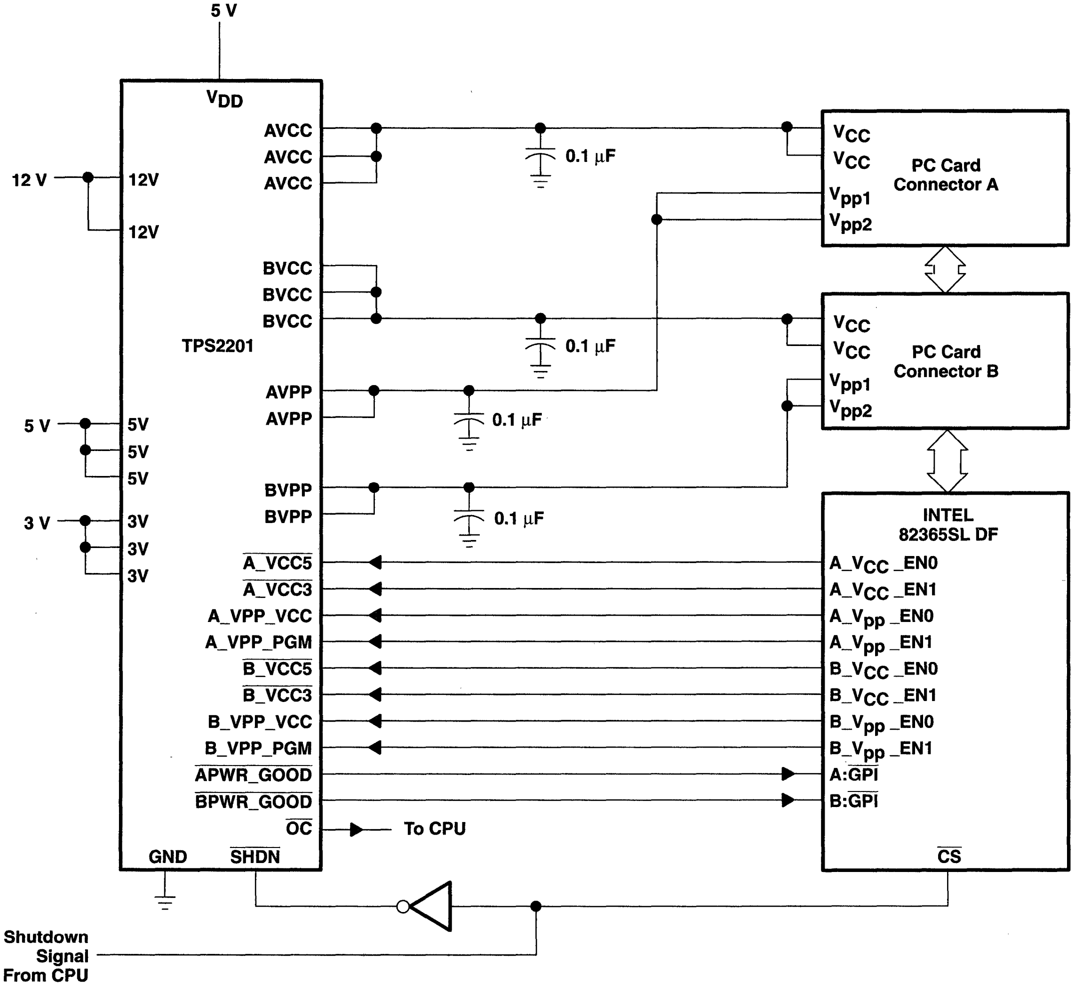


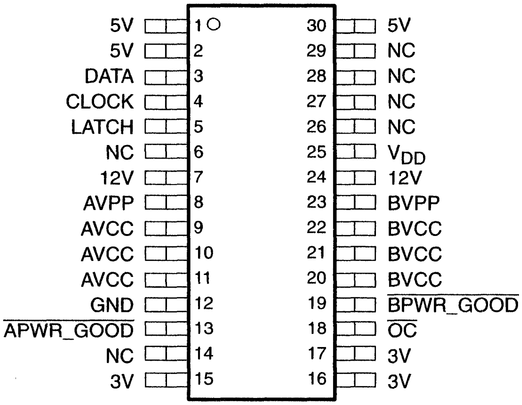
Figure 25. Detailed Operating Circuits Using Intel 82365SLDF Controller

TPS2202, TPS2202Y
DUAL-SLOT PC CARD POWER-INTERFACE SWITCHES FOR SERIAL PCMCIA CONTROLLERS

SLVS103A – DECEMBER 1994 – REVISED AUGUST 1995

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card Interface**
- **Saves PCMCIA Controller I/O Leads by Utilizing 3-Lead Serial Interface**
- **Meets PCMCIA Standards**
- **Internal Charge Pump (No External Capacitors Required) – 12-V Supply Can Be Disabled Except for Flash Programming**
- **Short Circuit and Thermal Protection**
- **Space-Saving 30-Pin SSOP(DB) Package**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Power Saving I_{DD} = 83 μA Typ, I_Q = 1 μA**
- **Low $r_{DS(on)}$ (160-mΩ V_{CC} Switch)**
- **Break-Before-Make Switching**
- **ESD Protection Up to 2 kV Per Mil-STD-883C, Method 3015**

DB OR DF PACKAGE
(TOP VIEW)



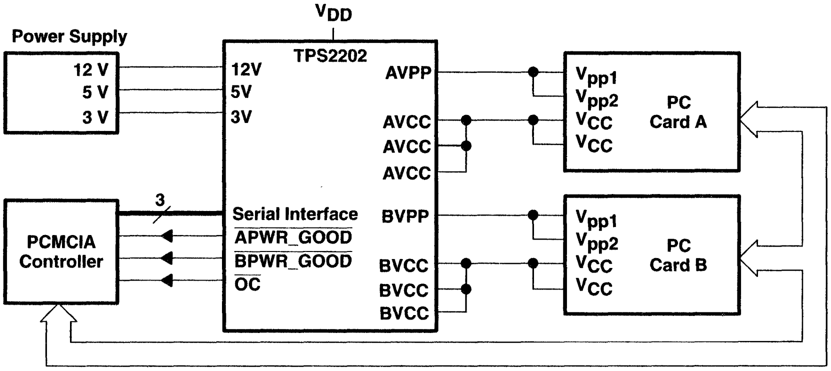
NC – No internal connection

description

The TPS2202 PC Card (PCMCIA) power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, thermal protection, and power-good reporting for PC Card control are combined on a single integrated circuit (IC), using Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3-V, 5-V, and/or 12-V card power by means of a reduced I/O serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability; current-limit reporting can help the user isolate a system fault to a bad card.

The TPS2202 maximizes battery life by using an internal charge pump to generate its own switch-drive voltage. Therefore, the 12-V supply can be powered down and only brought out of standby when flash memory needs to be written to or erased. End equipment for the TPS2202 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handiterminals, and bar-code scanners.

typical PC-card power-distribution application



LinBiCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES		CHIP FORM (Y)
	SHINK SMALL-OUTLINE (DB)	SMALL-OUTLINE (DF)	
−40°C to 150°C	TPS2202IDB	TPS2202IDF	TPS2202Y

† The DF package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2202IDFLE).

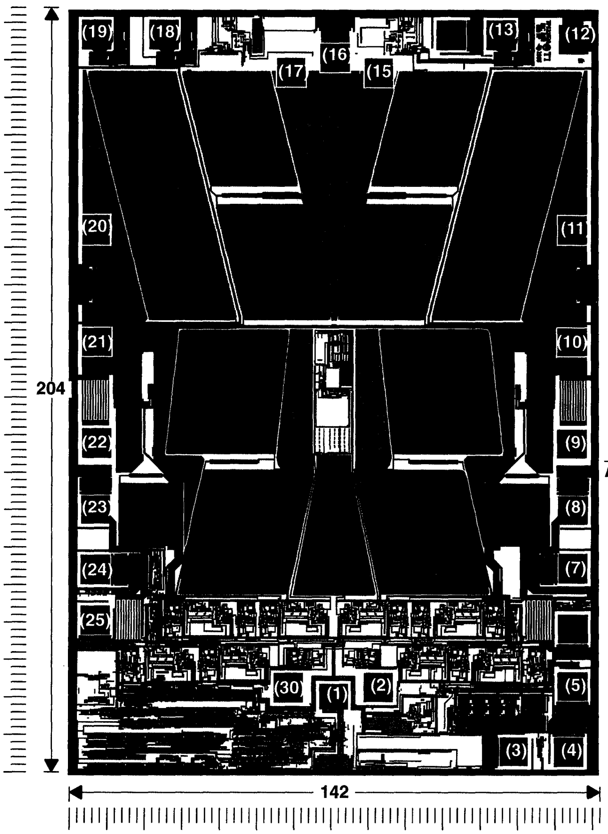
Terminal Functions

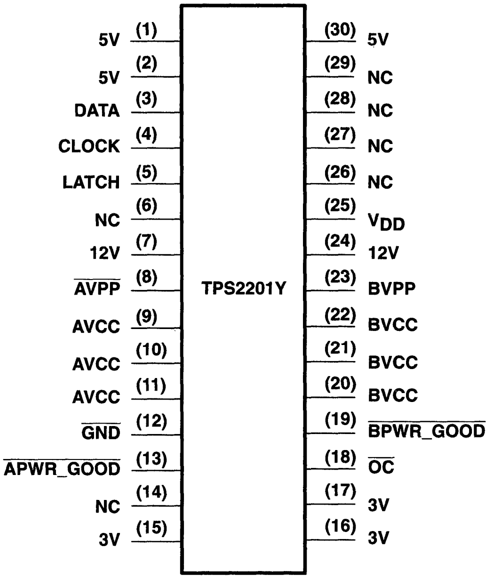
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V	15, 16, 17	I	3-V V_{CC} input for card power
5V	1, 2, 30	I	5-V V_{CC} input for card power
12V	7, 24	I	12-V VPP input for card power
AVCC	9, 10, 11	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
AVPP	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{APWR\_GOOD}}$	13	O	Logic-level power-ready output that stays low as long as AVPP is within limits.
BVCC	20, 21, 22	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{BPWR\_GOOD}}$	19	O	Logic-level power-ready output that stays low as long as BVPP is within limits.
CLOCK	4	I	Logic-level clock for serial data word
DATA	3	I	Logic-level serial data word
GND	12		Ground
LATCH	5	I	Logic-level latch for serial data word
NC	6, 14, 26, 27, 28, 29		No internal connection
$\overline{\text{OC}}$	18	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists.
V_{DD}	25		5-V power to chip

TPS2202Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS2202. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

TERMINALS 6, 14, 26, 27, 28, AND 29 ARE NOT CONNECTED

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}		−0.3 V to 7 V
Input voltage range for card power:	$V_{I(5V)}$	−0.3 V to 7 V
	$V_{I(3V)}$	−0.3 V to $V_{I(5V)}$
	$V_{I(12V)}$	−0.3 V to 14 V
Logic input voltage		−0.3 V to 7 V
Continuous total power dissipation		See Dissipation Rating Table
Output current (each card):	$I_{O(xVCC)}$	internally limited
	$I_{O(xVPP)}$	internally limited
Operating virtual junction temperature range, T_J		−40°C to 150°C
Operating free-air temperature range, T_A		−40°C to 85°C
Storage temperature range, T_{stg}		−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW	532 mW
DF	1158 mW	9.26 mW/°C	741 mW	602 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 108°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.75	5.25	V
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3V)}$	0	$V_{I(5V)}$†	V
	$V_{I(12V)}$	0	13.5	V
Output current, I_O	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Clock frequency, f_{clock}		0	2.5	MHz
Operating virtual junction temperature, T_J		−40	125	°C

† $V_{I(3V)}$ should not be taken above $V_{I(5V)}$.

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

dc characteristics

PARAMETER		TEST CONDITIONS	TPS2202			UNIT
			MIN	TYP	MAX	
Switch resistance†	5 V to xVCC				160	mΩ
	3 V to xVCC				225	
	5 V to xVPP				6	Ω
	3 V to xVPP				6	
	12 V to xVPP				1	
Clamp low voltage		I_{PP} at 10 mA			0.8	V
Clamp low voltage		I_{CC} at 10 mA			0.8	V
Leakage current	I_{PP} High-impedance state	T_A = 25°C		1	10	μA
		T_A = 85°C			50	
	I_{CC} High-impedance state	T_A = 25°C		1	10	
		T_A = 85°C			50	
Input current	I_{DD}	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V		83	150	μA
	I_{DD} in shutdown	$V_{O(BVCC)} = V_{O(AVCC)} = V_{O(AVPP)}$ $= V_{O(BVPP)}$ = high Z			1	μA
Power-ready threshold, $\overline{\text{PWR\_GOOD}}$			10.72	11.05	11.4	V
Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$ (12-V mode)				50		mV
Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output powered up into a short to GND	0.75	1.3	1.9	A
	$I_{O(xVPP)}$		120	200	400	mA

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics‡

PARAMETER		TEST CONDITIONS		TPS2202			UNIT
				MIN	TYP	MAX	
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		ms
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1§)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		
		LATCH↑ to xVCC (3 V)	t_{on}		5.8		ms
			t_{off}		28		
		LATCH↑ to xVCC (5 V)	t_{on}		4		ms
			t_{off}		30		

‡ Refer to Parameter Measurement Information

§ Propagation delays are with C_L = 100 μF.

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted) (continued)

logic section

PARAMETER	TEST CONDITIONS	TPS2202		UNIT
		MIN	MAX	
Logic input current			1	µA
Logic input high level		2.7		V
Logic input low level			0.8	V
Logic output high level	I_O = 1 mA	V_{DD}−0.4		V
Logic output low level			0.4	V

dc characteristics

PARAMETER		TEST CONDITIONS	TPS2202Y			UNIT
			MIN	TYP	MAX	
Leakage current	I_{PP} High-impedance state			1		µA
	I_{CC} High-impedance state			1		
Input current	I_{DD}	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V		83		µA
Power-ready threshold, $\overline{\text{PWR\_GOOD}}$				11.05		V
Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$ (12-V mode)				50		mV

switching characteristics†

PARAMETER		TEST CONDITIONS		TPS2202Y			UNIT
				MIN	TYP	MAX	
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		ms
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1‡)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		
		LATCH↑ to xVCC	t_{on}		5.8		ms
			t_{off}		28		
		LATCH↑ to xVCC	t_{on}		4		ms
			t_{off}		30		

† Refer to Parameter Measurement Information
‡ Propagation delays are with C_L = 100 µF.

PARAMETER MEASUREMENT INFORMATION

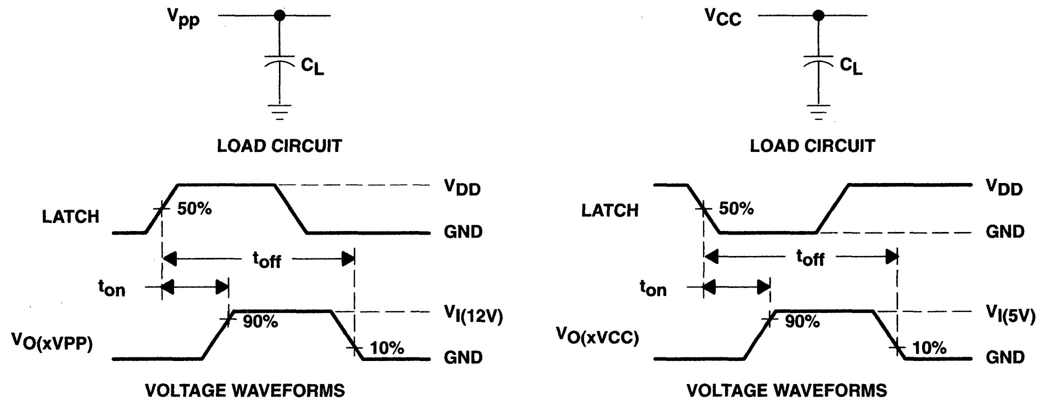
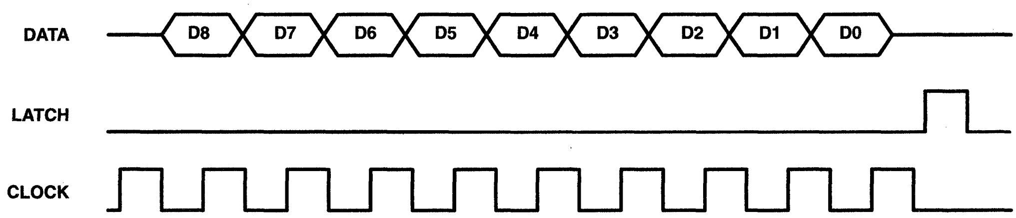


Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
Serial-Interface Timing	2
xVCC Propagation Delay and Rise Times With 1-μF Load, 3-V Switch	3
xVCC Propagation Delay and Fall Times With 1-μF Load, 3-V Switch	4
xVCC Propagation Delay and Rise Times With 100-μF Load, 3-V Switch	5
xVCC Propagation Delay and Fall Times With 100-μF Load, 3-V Switch	6
xVCC Propagation Delay and Rise Times With 1-μF Load, 5-V Switch	7
xVCC Propagation Delay and Fall Times With 1-μF Load, 5-V Switch	8
xVCC Propagation Delay and Rise Times With 100-μF Load, 5-V Switch	9
xVCC Propagation Delay and Fall Times With 100-μF Load, 5-V Switch	10
xVPP Propagation Delay and Rise Times With 1-μF Load, 12-V Switch	11
xVPP Propagation Delay and Fall Times With 1-μF Load, 12-V Switch	12
xVPP Propagation Delay and Rise Times With 100-μF Load, 12-V Switch	13
xVPP Propagation Delay and Fall Times With 100-μF Load, 12-V Switch	14



NOTE A. Data is clocked in on the a positive leading edge of the clock. The latch should occur before next positive leading edge of the clock. For definition of D0–D8, see control logic table.

Figure 2. Serial-Interface Timing

PARAMETER MEASUREMENT INFORMATION

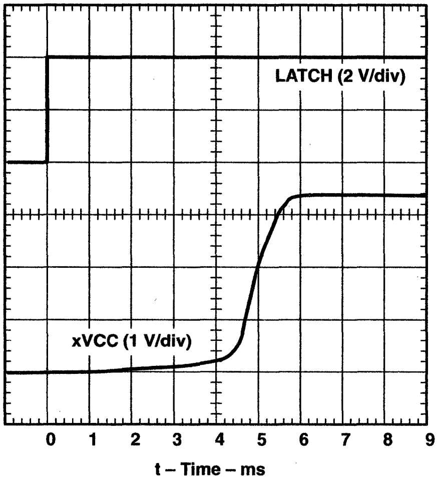


Figure 3. xVCC Propagation Delay and Rise Times With 1-µF Load, 3-V Switch

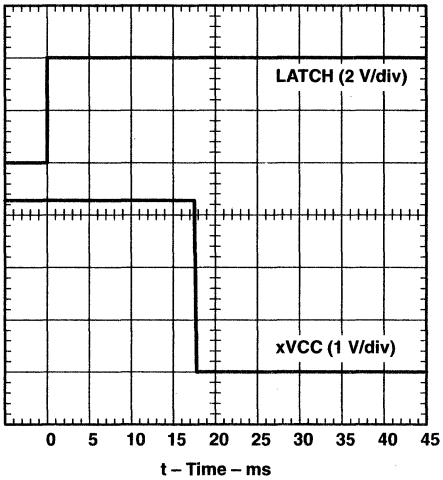


Figure 4. xVCC Propagation Delay and Fall Times With 1-µF Load, 3-V Switch

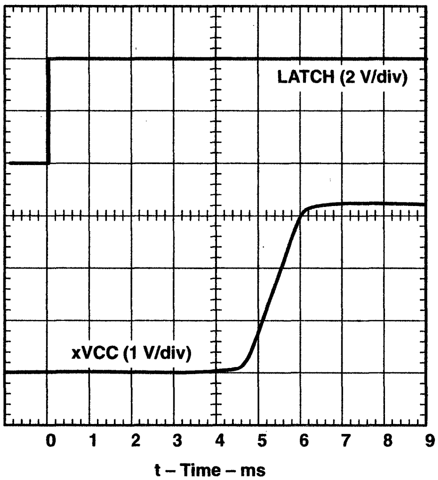


Figure 5. xVCC Propagation Delay and Rise Times With 100-µF Load, 3-V Switch

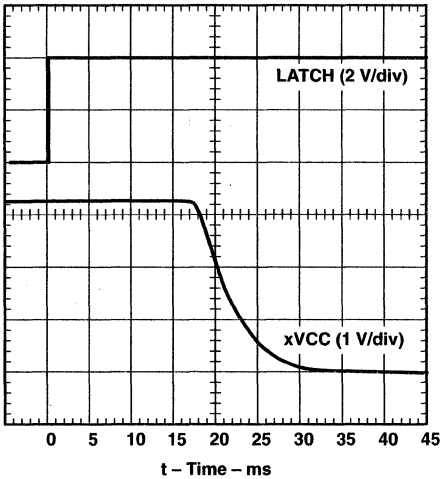


Figure 6. xVCC Propagation Delay and Fall Times With 100-µF Load, 3-V Switch

PARAMETER MEASUREMENT INFORMATION

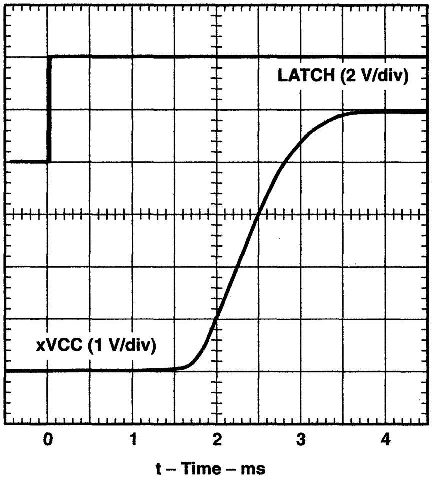


Figure 7. xVCC Propagation Delay and Rise Times With 1-µF Load, 5-V Switch

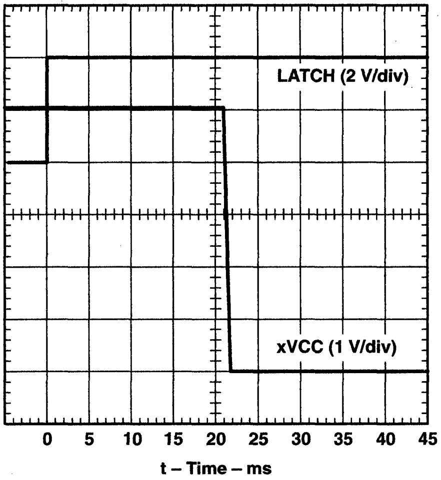


Figure 8. xVCC Propagation Delay and Fall Times With 1-µF Load, 5-V Switch

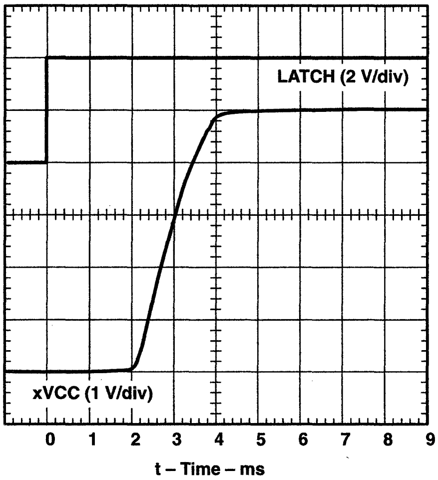


Figure 9. xVCC Propagation Delay and Rise Times With 100-µF Load, 5-V Switch

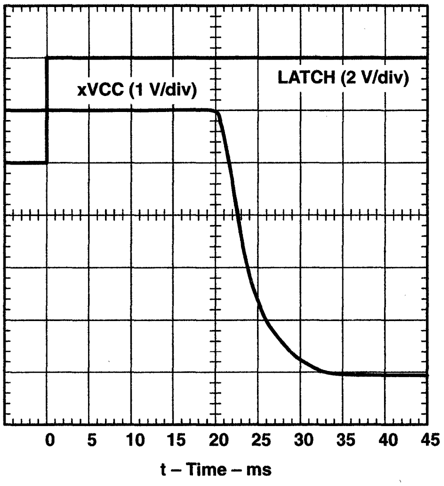


Figure 10. xVCC Propagation Delay and Fall Times With 100-µF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

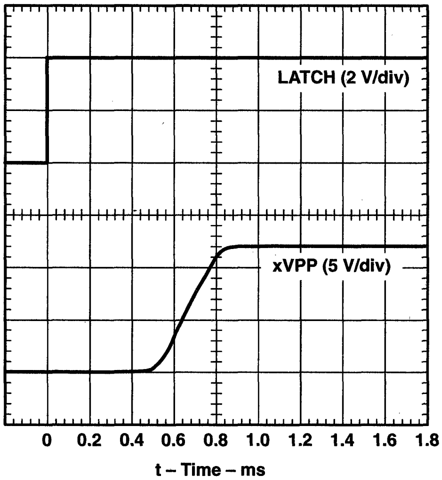


Figure 11. xVPP Propagation Delay and Rise Times With 1-μF Load, 12-V Switch

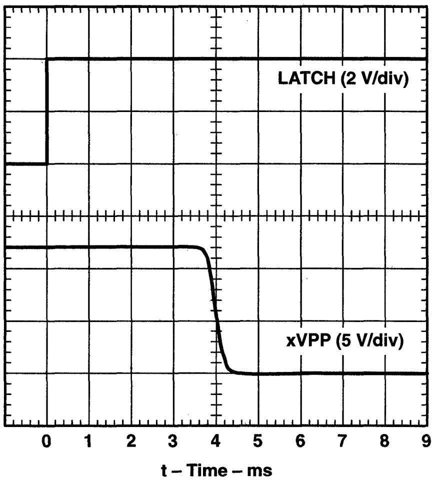


Figure 12. xVPP Propagation Delay and Fall Times With 1-μF Load, 12-V Switch

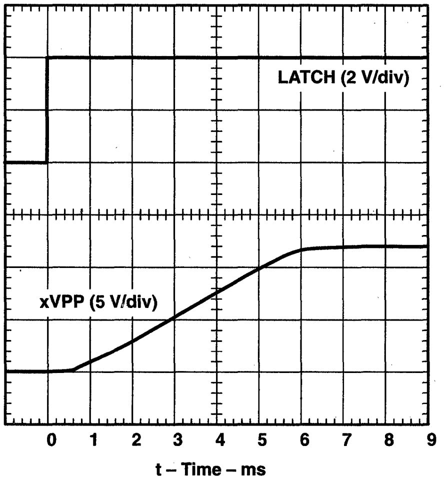


Figure 13. xVPP Propagation Delay and Rise Times With 100-μF Load, 12-V Switch

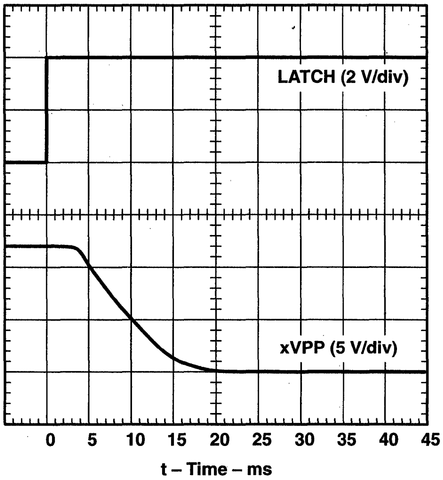


Figure 14. xVPP Propagation Delay and Fall Times With 100-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS†

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Junction temperature	15
$r_{DS(on)}$	Static drain-source on-state resistance, 3-V switch	vs Junction temperature	16
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V switch	vs Junction temperature	17
$r_{DS(on)}$	Static drain-source on-state resistance, 12-V switch	vs Junction temperature	18
$V_{O(xVCC)}$	Output voltage, 5-V switch	vs Output current	19
$V_{O(xVCC)}$	Output voltage, 3-V switch	vs Output current	20
xV_{pp}	Output voltage, V_{pp} switch	vs Output current	21
$I_{SC(xVCC)}$	Short-circuit current, 5-V switch	vs Junction temperature	22
$I_{SC(xVPP)}$	Short-circuit current, 12-V switch	vs Junction temperature	23

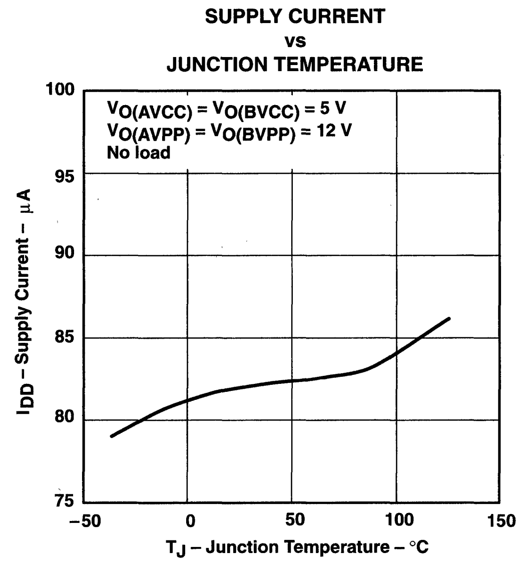


Figure 15

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† t = pulse tested

TYPICAL CHARACTERISTICS†

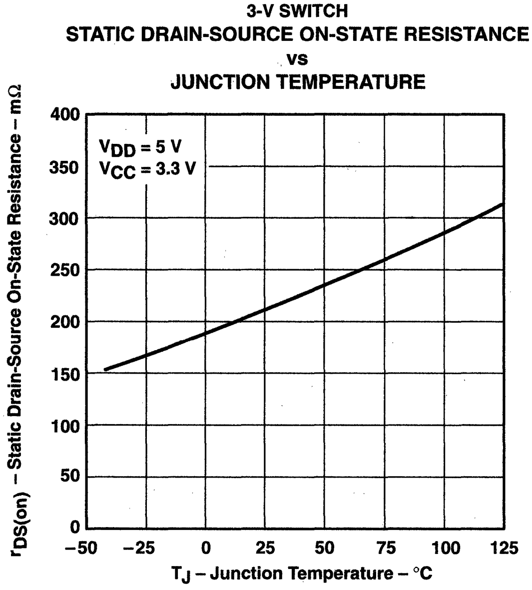

Figure 16

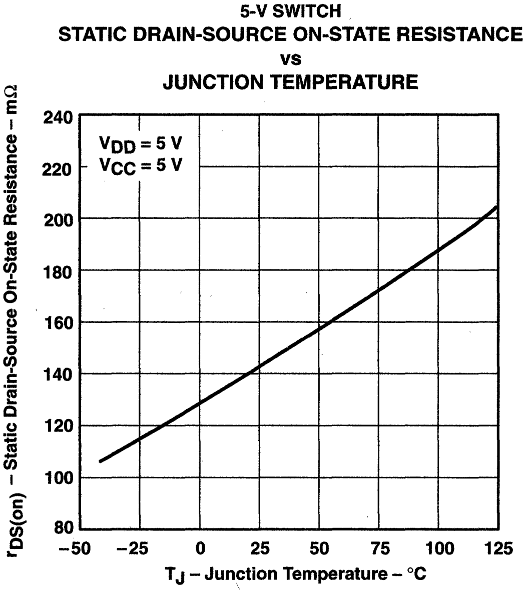

Figure 17

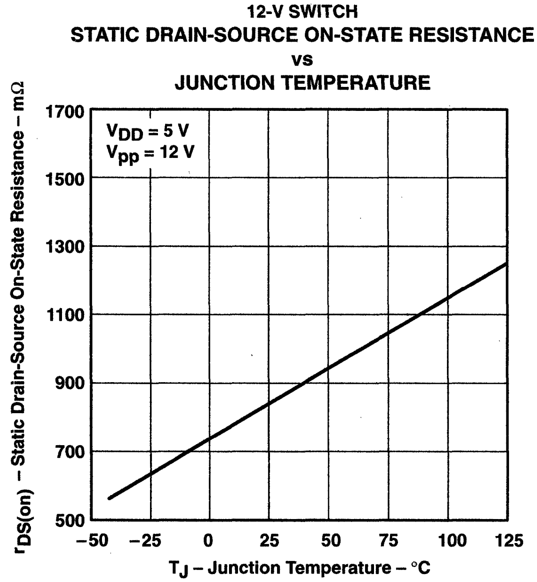

Figure 18

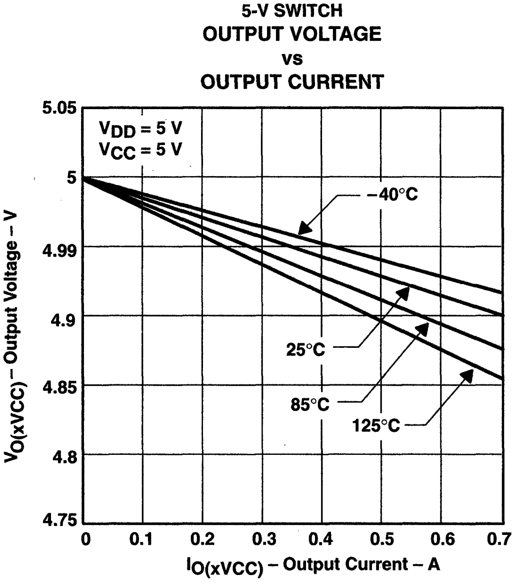

Figure 19

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† t = pulse tested

TYPICAL CHARACTERISTICS†

3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

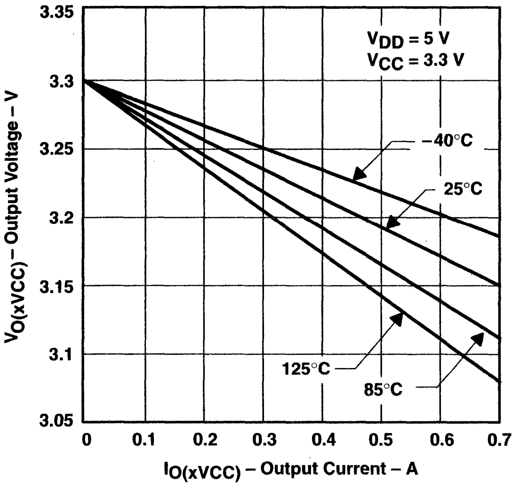

Figure 20

V_{pp} SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

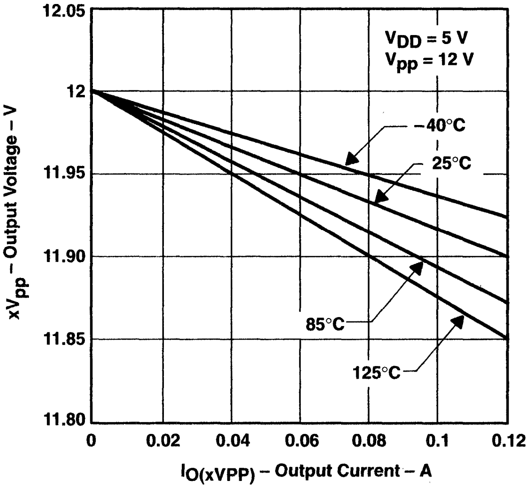

Figure 21

5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

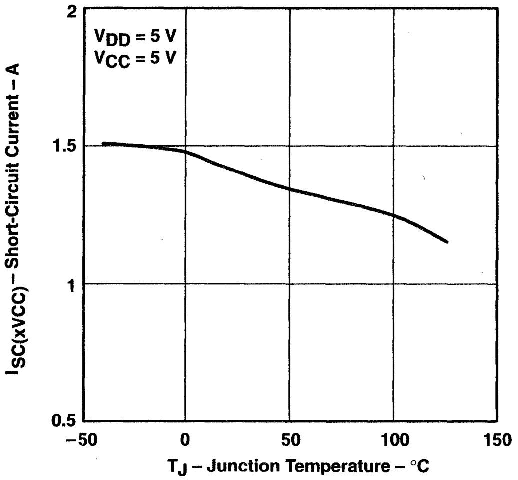

Figure 22

12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

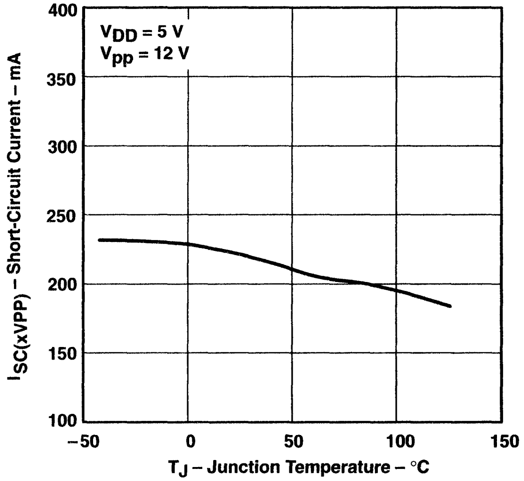

Figure 23

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† t = pulse tested

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold: modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established and was comprised of members from leading computer, software, PC card, and semiconductor manufacturers. One key goal was to realize the concept of plug and play – cards and hosts from different vendors should be compatible and able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the PC Card connector's 68 pins. This power interface consists of two V_{CC}, two V_{pp}, and four ground pins. Multiple V_{CC} and ground pins minimize connector-pin and line resistance. The two V_{pp} pins were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} pins; flash-memory programming and erase voltage is supplied through the V_{pp} pins. As each pin is rated to 0.5 A, V_{CC} and V_{pp} can theoretically supply up to 1 A, assuming equal pin resistance and no pin failure. A conservative design would limit current to 500 mA. Some applications, however, require higher V_{CC} currents; disk drives, for example, may need as much as 750-mA peak current to create the initial torque necessary to spin up the platter. V_{pp} currents, on the other hand, are defined by flash-memory programming requirements, typically under 120 mA.

future power trends

The 1-A physical-pin current alluded to in the PC Card specification has caused some host-system engineers to believe they are required to deliver 1 A within the voltage tolerance of the card. Future applications, such as RF cards, could use the extra power for their radio transmitters. The 5 W needed for these cards will require very robust power supplies and special cooling considerations. The limited number of host sockets that will be able to support them makes the market for these high-powered PC Cards uncertain. The vast majority of the cards require less than 600 mA continuous current and the trend is towards even lower-powered PC Cards that will assure compatibility with a greater number of host systems. Recognizing the need for power derating, an adhoc committee of the PCMCIA is currently working to limit the amount of steady-state dc current to the PC Card to something less than the currently implied 1 A. If a system is designed to support 1 A, then the switch $r_{DS(on)}$, power supply requirements, and PC Card cooling need to be carefully considered.

designing around 1-A delivery

Delivering 1 A means minimizing voltage (and power) losses across the PC Card power interface, which requires that designers trade off switch resistance and the cost associated with large-die (low $r_{DS(on)}$) MOSFET transistors. The PC Card standard requires that 5 V ±5%, or 3.3 V ±0.3 V be supplied to the card. The approximate 10% tolerance for the 3.3-V supply makes the 3.3-V $r_{DS(on)}$ less critical than the 5-V switch. A conservative approach is to allow 2% for voltage-regulator tolerance and 1% for etch- and terminal-resistance drops, which leaves 2% (100 mV) voltage drop for the 5-V switch, and at least 6% (198 mV) for the 3.3-V switch.

Calculating the $r_{DS(on)}$ necessary to support a 100 mV or 198 mV switch loss, using R = E/I and setting I = 1 A, the 5-V and 3.3-V switches would need to be 100 mΩ and 198 mΩ respectively. One solution would be to pay for a more expensive switch with lower $r_{DS(on)}$. A second, less expensive approach is to increase the headroom of the power supply–for example, to increase the 5-V supply 1.5% or to 5.075 ±2%. Working through the numbers once more, the 2% for the regulator plus 1 % for etch and terminal losses leaves 97% or 4.923 V.

APPLICATION INFORMATION

designing around 1-A delivery (continued)

The allowable voltage loss across the power distribution switch is now 4.923 V minus 4.750 V or 173 mV. Therefore, a switch with 173 mΩ or less could deliver 1 A or greater. Setting the power supply high is a common practice for delivering voltages to allow for system switch, connector, and etch losses and has a minimal effect on overall battery life. In the example above, setting the power supply 1.5% high would only decrease a 3-hour battery life by approximately 2.7 minutes, trivial when compared with the decrease in battery life when running a 5-W PC Card.

heat dissipation

A greater concern in delivering 1 A or 5 W is the ability of the host to dissipate the heat generated by the PC Card. For desktop computers the solution is simpler: locate the PC Card cage such that it receives convection cooling from the forced air of the fan. Notebooks and other handheld equipment are not be able to rely on convection, but must rely on conduction of heat away from the PC Card through the rails into the card cage. This is difficult because PC Card/card cage heat transfer is very poor. A typical design scenario would require the PC Card to be held at 60°C maximum with the host platform operating as high as 50°C. Preliminary testing reveals that a PC Card can have a 20°C rise, exceeding the 10°C differential in the example, when dissipating less than 2 W of continuous power. The 60°C temperature was chosen because it is the maximum operating temperature allowable by PC Card specification. Power handling requirements and temperature rises are topics of concern and are currently being addressed by the PCMCIA committee.

overcurrent and over-temperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. This can be particularly frustrating to the consumer who has already experienced problems with shortened battery life due to improper Nicad conditioning or memory effect. Most hosts include fuses for protection. The reliability of fused systems is poor, though, as blown fuses require troubleshooting and repair, usually by the manufacturer. The TPS2202 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have the added advantage that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2202 asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry engages, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{pp} power for switch-gate drive and other chip functions, requiring that it be present at all times. The TPS2202 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V V_{DD} supply; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the TPS2202 during a software shutdown, in which quiescent current drops to a maximum of 1 µA.

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2202 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the

APPLICATION INFORMATION

voltage transitioning requirement (continued)

capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2202 offers a selectable V_{CC} and V_{PP} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100 kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis will reveal that the RC time constant delays the required discharge time to over 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2202 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial controller interface. The TPS2202 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

power supply considerations

The TPS2202 has multiple terminals for each of its 3.3 V, 5 V, and 12 V power inputs and for the switched V_{CC} outputs. Any individual terminal can conduct the rated input or output current. Unless all terminals are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12 V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power terminals be paralleled for optimum operation. The V_{DD} input lead must be connected to the 5V input leads.

Although the TPS2202 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-µF or larger capacitor; doing so improves the immunity of the TPS2202 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2202 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance.

The TPS2202, unlike other PC Card power-interface switches, does not use the 12-V power supply for switching or other chip functions. Instead, an internal charge pump generates the necessary voltage from V_{DD}, allowing the 12-V input supply to be shut down except when the V_{pp} programming or erase voltage is needed. Careful system design making use of this feature reduces power consumption and extends battery lifetime.

The 3.3-V power input should not be taken higher than the 5-V input. Doing so, though nondestructive, results in high current flow into the device, and could result in abnormal operation. In any case, this occurrence indicates a malfunction of one input voltage or both, which should be investigated.

Similarly, no terminal should be taken below −0.3 V; forward biasing the parasitic-substrate diode results in substrate currents and unpredictable performance.

APPLICATION INFORMATION

overcurrent and thermal protection

The TPS2202 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2202 controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2202 engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2202 may latch nondestructively in an off state. Cycling power reestablishes normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to engage if powered up into a short in the range of 0.75 A to 1.9 A, typically at about 1.3 A; the V_{pp} outputs limit from 120 mA to 400 mA, typically around 200 mA. The protection circuitry acts by linearly limiting the current passing through the switch, rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating when the package power-dissipation ratings are exceeded. Thermal limiting, disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16, 17, and 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \cdot I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma P_D \cdot R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If they are not within a few degrees of each other, reiterate using the calculated temperature as the initial estimate.

logic input and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 9-bit (D0 through D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 µA to conserve battery power.

The TPS2202 serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and JEIDA standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} outputs, as previously discussed.

APPLICATION INFORMATION

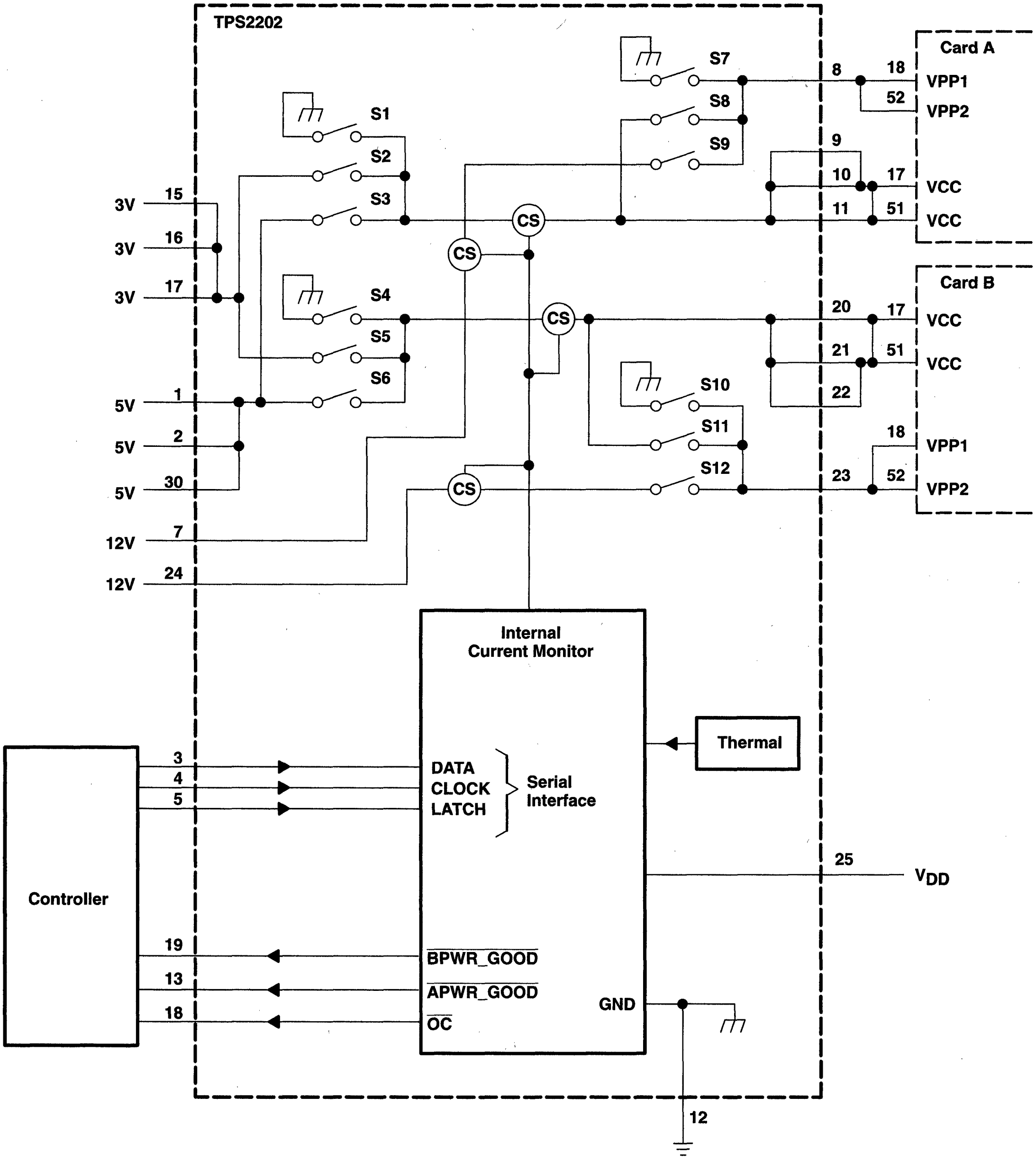


Figure 24. Internal Switching Matrix

APPLICATION INFORMATION

TPS2202 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D0 A_VPP_PGM	D1 A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[†]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D4 B_VPP_PGM	D5 B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[‡]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D3 $\overline{\text{A}}$_VCC3	D2 $\overline{\text{A}}$_VCC5	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D6 $\overline{\text{B}}$_VCC3	D7 $\overline{\text{B}}$_VCC5	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

[†] Output depends on AVCC
[‡] Output depends on BVCC

ESD protection

All TPS2202 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

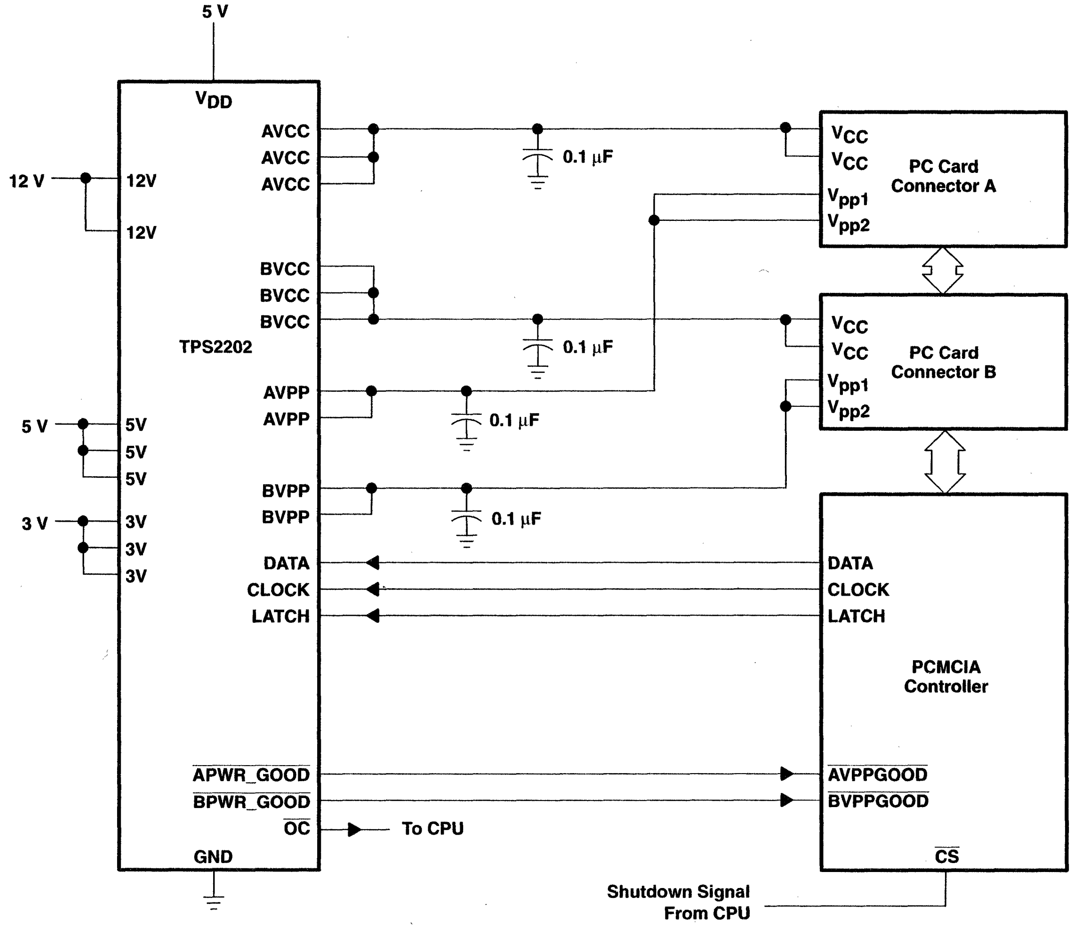


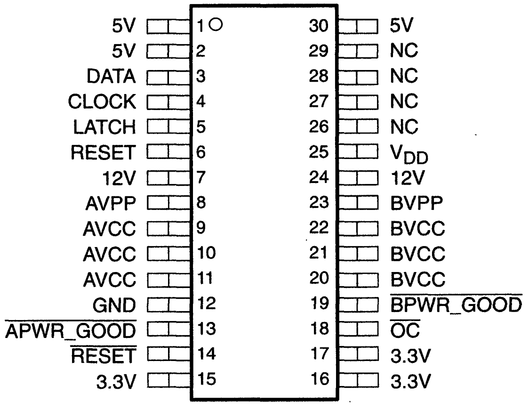
Figure 25. Detailed Interconnections and Capacitor Recommendations

TPS2202AI
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH WITH RESET FOR SERIAL PCMCIA CONTROLLER

SLVS123 – SEPTEMBER 1995

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card™ Interface**
- **P²C™ 3-Lead Serial Interface Compatible With CardBus™ Controllers**
- **Meets PC Card Standards**
- **RESET Allows System Initialization of PC Cards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short Circuit and Thermal Protection**
- **Space-Saving 30-Pin SSOP (DB) Package**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Power Saving I_{DD} = 83 μA Typ, I_Q = 1 μA**
- **Low $r_{DS(on)}$ (160-mΩ V_{CC} Switch)**
- **Break-Before-Make Switching**

DF OR DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2202AI PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, thermal protection, and power-good reporting for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power by means of the P²C (PCMCIA Peripheral-Control) Texas Instruments nonproprietary serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to a specific card.

The TPS2202AI incorporates a reset function, selectable by one of two inputs, to help alleviate system errors. The reset function enables PC Card initialization concurrent with host platform initialization, allowing a system reset. Reset is accomplished by grounding the V_{CC} and V_{pp} (flash-memory programming voltage) outputs, which discharges residual card voltage.

End equipment for the TPS2202AI includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handiterminals, and bar-code scanners. The TPS2202AI is only available taped and reeled (either TPS2202AIDFLE or TPS2202AIDBLE).

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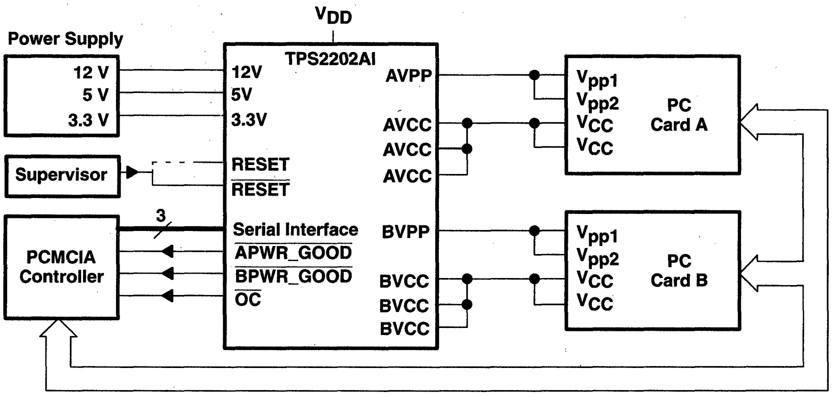
PC Card and CardBus are trademarks of PCMCIA (Personal Computer Memory Card International Association).

typical PC card power-distribution application



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3V	15, 16, 17	I	3.3-V V_{CC} input for card power
5V	1, 2, 30	I	5-V V_{CC} input for card power
12V	7, 24	I	12-V V_{pp} input for card power
AVCC	9, 10, 11	O	Switched output that delivers 3.3 V, 5 V, low or high impedance to card
AVPP	8	O	Switched output that delivers 3.3 V, 5 V, 12 V, low or high impedance to card
$\overline{\text{APWR\_GOOD}}$	13	O	Logic-level power-ready output that stays low as long as AVPP is within limits
BVCC	20, 21, 22	O	Switched output that delivers 3.3 V, 5 V, low or high impedance
BVPP	23	O	Switched output that delivers 3.3 V, 5 V, 12 V, low or high impedance
$\overline{\text{BPWR\_GOOD}}$	19	O	Logic-level power-ready output that remains low as long as BVPP is within limits
CLOCK	4	I	Logic-level clock for serial data word
DATA	3	I	Logic-level serial data word
GND	12		Ground
LATCH	5	I	Logic-level latch for serial data word
NC	26, 27, 28, 29		No internal connection
$\overline{\text{OC}}$	18	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
RESET	6	I	Logic-level RESET input active high. Do not connect if terminal 14 is used.
$\overline{\text{RESET}}$	14	I	Logic-level $\overline{\text{RESET}}$ input active low. Do not connect if terminal 6 is used.
V_{DD}	25	I	5-V power to chip

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}	−0.3 V to 7 V
Input voltage range for card power: $V_{I(5V)}$	−0.3 V to 7 V
$V_{I(3.3V)}$	−0.3 V to $V_{I(5V)}$
$V_{I(12V)}$	−0.3 V to 14 V
Logic input voltage	−0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$	internally limited
$I_{O(xVPP)}$	internally limited
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DF	1158 mW	9.26 mW/°C	741 mW	602 mW
DB	1024 mW	8.2 mW/°C	655 mW	532 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.75	5.25	V
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	$V_{I(5V)}$§	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Clock frequency		0	2.5	MHz
Operating virtual junction temperature, T_J		−40	125	°C

§ $V_{I(3.3V)}$ should not be taken above $V_{I(5V)}$.

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Switch resistances†	5 V to xVCC				160	mΩ
		3.3 V to xVCC				225	
		5 V to xVPP				6	Ω
		3.3 V to xVPP				6	
		12 V to xVPP				1	
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{pp} High-impedance state	T_A = 25°C		1	10	µA
			T_A = 85°C			50	
		I_{CC} High-impedance state	T_A = 25°C		1	10	
			T_A = 85°C			50	
I_I	Input current	I_{DD} Supply current	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V		83	150	µA
		I_{DD} Supply current in shutdown	$V_{O(BVCC)} = V_{O(AVCC)} = V_{O(AVPP)} = V_{O(BVPP)}$ = Hi-Z			1	µA
	Power-ready threshold, $\overline{\text{PWR\_GOOD}}$			10.72	11.05	11.4	V
	Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$	12-V mode			50		mV
	Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output powered up into a short to GND	0.75	1.3	1.9	A
		$I_{O(xVPP)}$		120	200	400	mA

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	I_O = 1 mA	V_{DD}−0.4		V
Logic output low level			0.4	V
Logic input minimum pulse width		1		µs

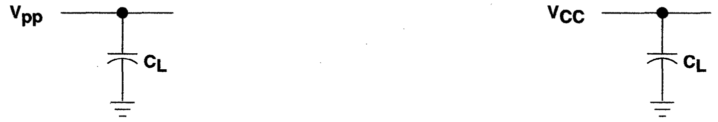
switching characteristics[†]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Output rise times	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall times	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1[‡])	LATCH↑ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		ms
		LATCH↑ to xVCC (3 V)	t_{on}		5.8		ms
			t_{off}		28		ms
		LATCH↑ to xVCC (5 V)	t_{on}		4		ms
			t_{off}		30		ms

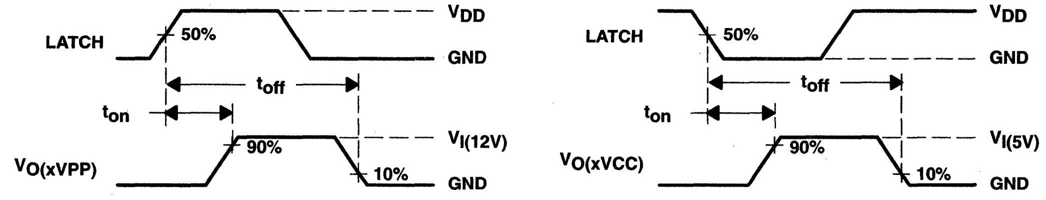
[†] Refer to Parameter Measurement Information

[‡] Propagation delays are with $C_L = 100\ \mu F$.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT LOAD CIRCUIT



VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS

Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

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xVCC Propagation Delay and Rise Time With 100-µF Load, 3.3-V Switch	5
xVCC Propagation Delay and Fall Time With 100-µF Load, 3.3-V Switch	6
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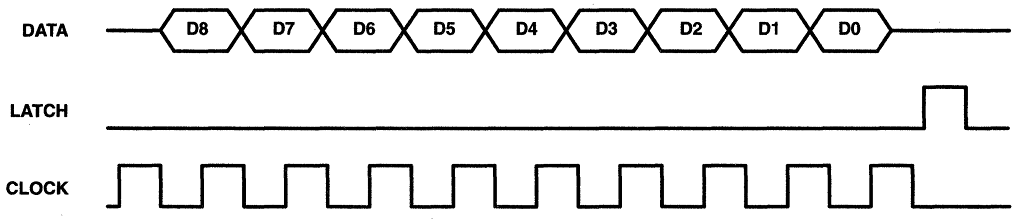

NOTE A. Data is clocked in on the positive leading edge of the clock. The latch should occur before next positive leading edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 2. Serial-Interface Timing

PARAMETER MEASUREMENT INFORMATION

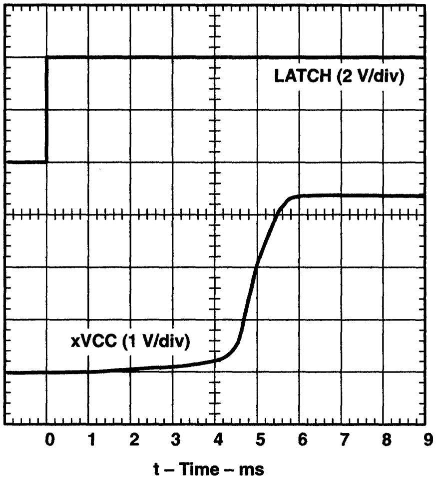

Figure 3. xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch

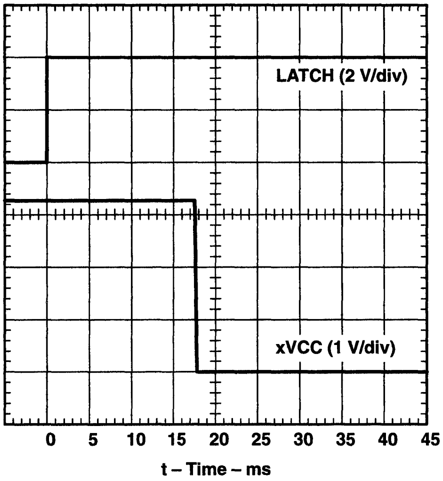

Figure 4. xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch

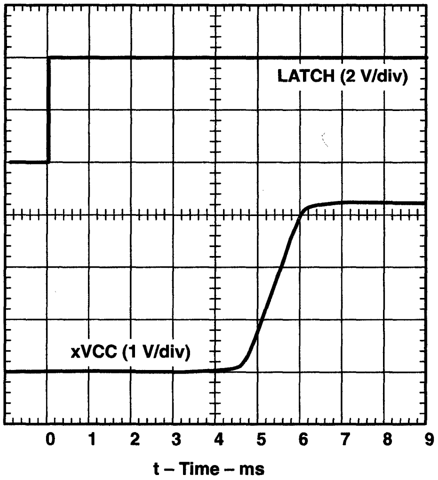

Figure 5. xVCC Propagation Delay and Rise Time With 100-µF Load, 3.3-V Switch

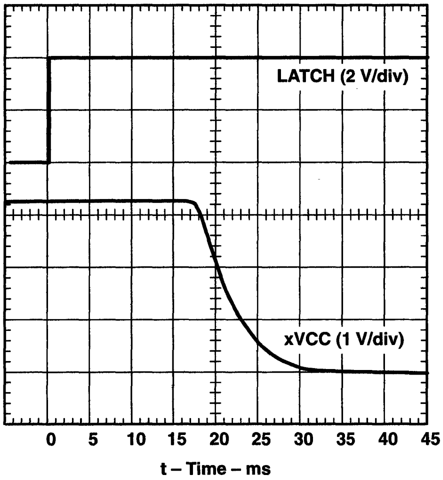

Figure 6. xVCC Propagation Delay and Fall Time With 100-µF Load, 3.3-V Switch

PARAMETER MEASUREMENT INFORMATION

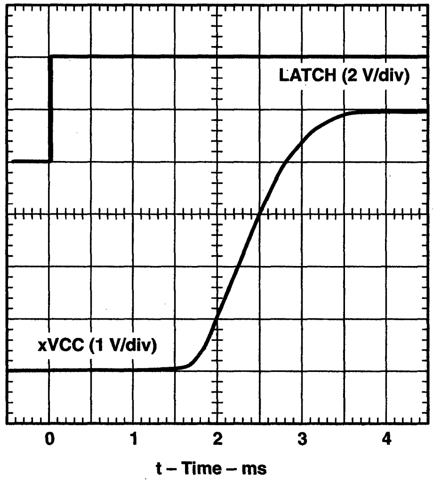

Figure 7. xVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch

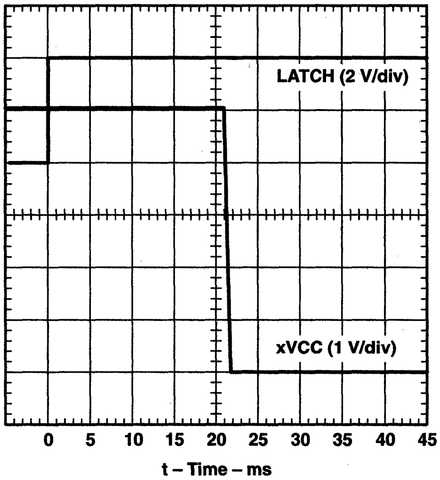

Figure 8. xVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch

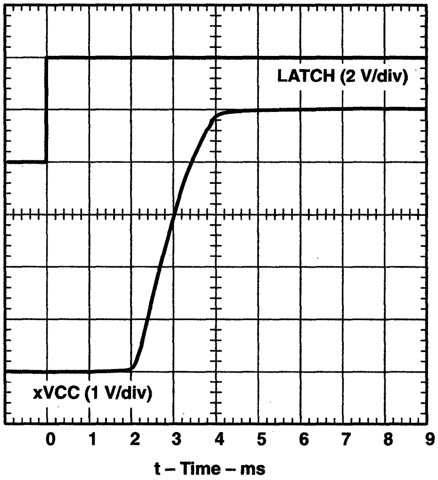

Figure 9. xVCC Propagation Delay and Rise Time With 100-µF Load, 5-V Switch

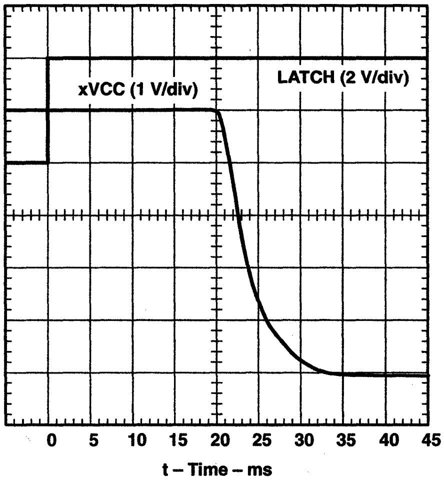

Figure 10. xVCC Propagation Delay and Fall Time With 100-µF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

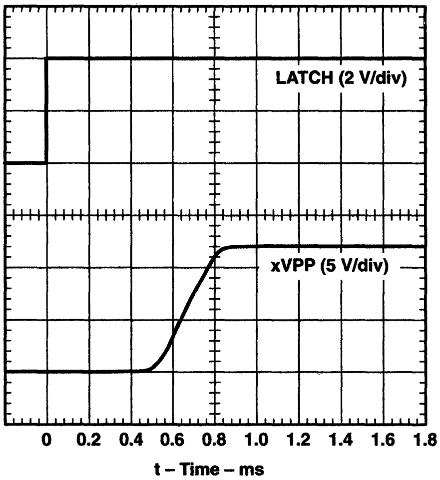

Figure 11. xVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch

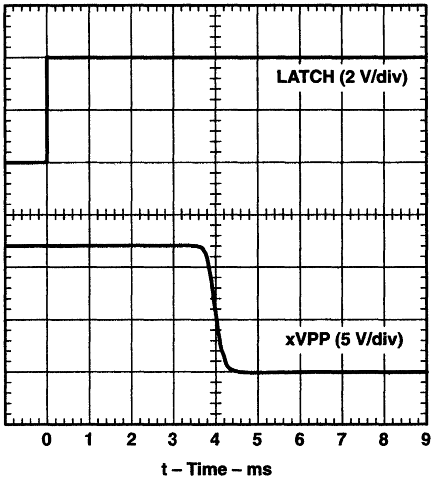

Figure 12. xVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch

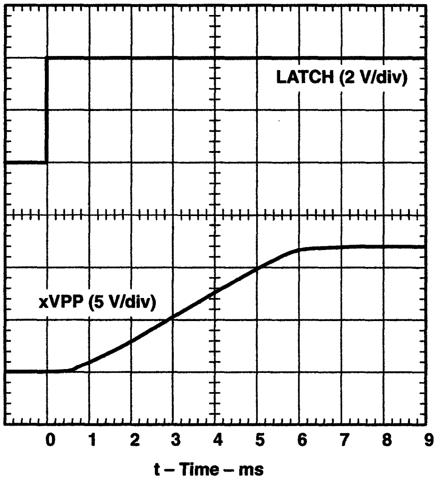

Figure 13. xVPP Propagation Delay and Rise Time With 100-µF Load, 12-V Switch

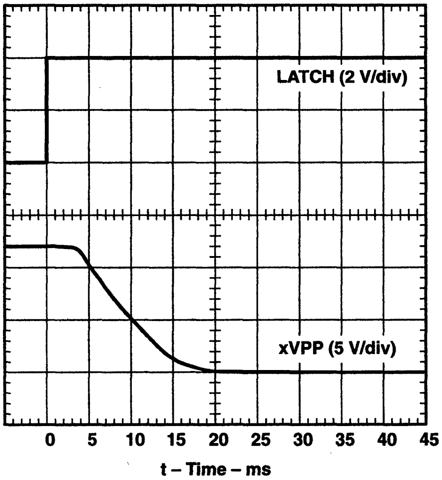

Figure 14. xVPP Propagation Delay and Fall Time With 100-µF Load, 12-V Switch

TYPICAL CHARACTERISTICS†

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$r_{DS(on)}$	Static drain-source on-state resistance, 12-V switch	vs Junction temperature	18
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$V_{O(xVCC)}$	Output voltage, 3.3-V switch	vs Output current	20
xV_{pp}	Output voltage, V_{pp} switch	vs Output current	21
$I_{SC(xVCC)}$	Short-circuit current, 5-V switch	vs Junction temperature	22
$I_{SC(xVPP)}$	Short-circuit current, 12-V switch	vs Junction temperature	23

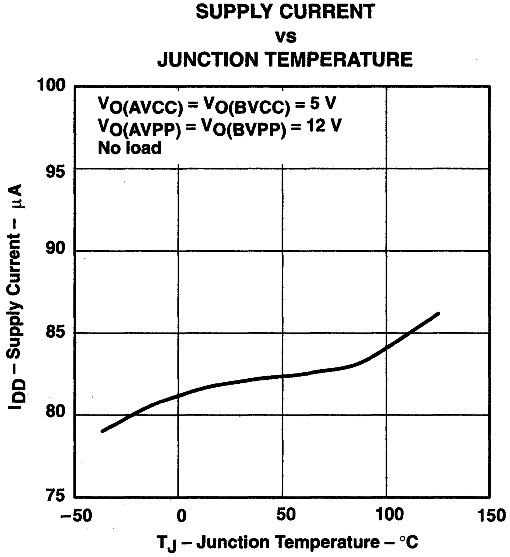

Figure 15

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† t = pulse tested

TYPICAL CHARACTERISTICS[†]

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

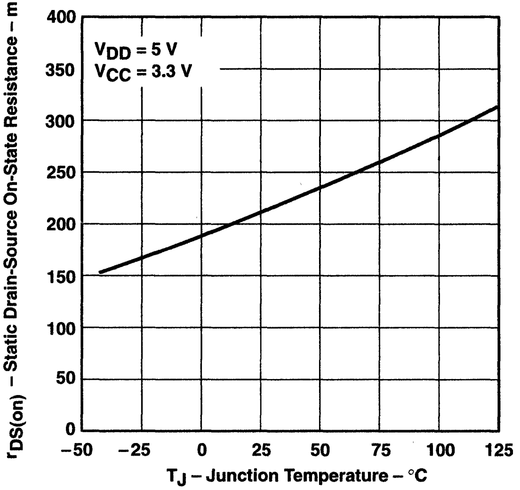

Figure 16

5-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

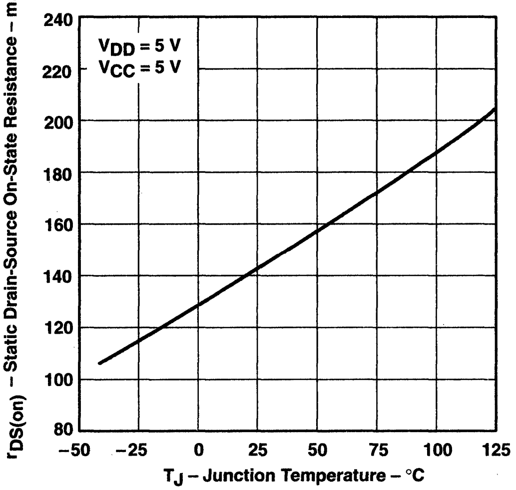

Figure 17

12-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

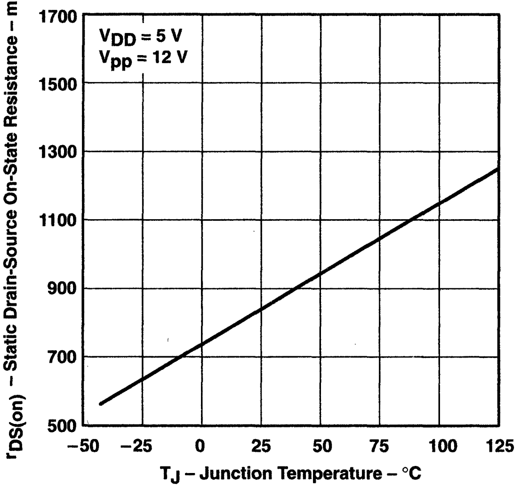

Figure 18

5-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

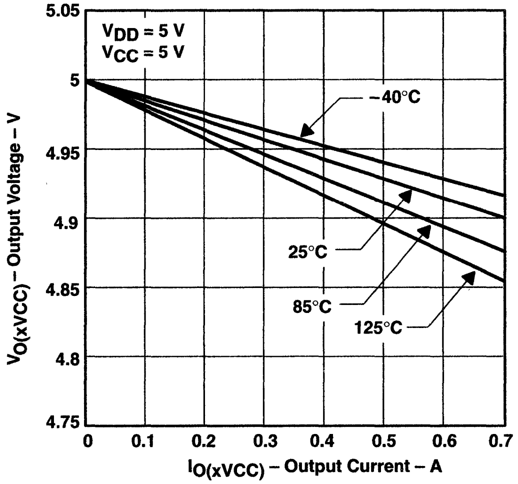

Figure 19

[†] t = pulse tested

TYPICAL CHARACTERISTICS†

3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

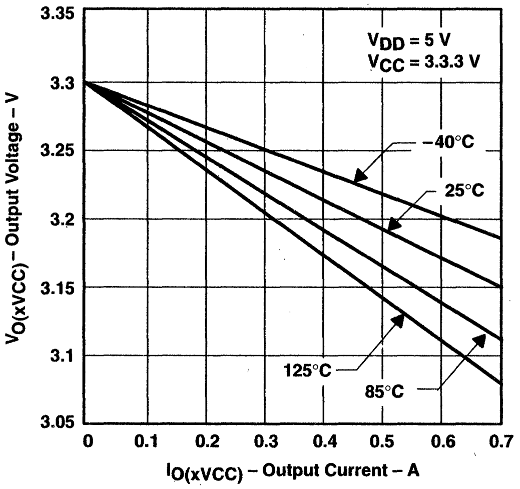

Figure 20

V_pp SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

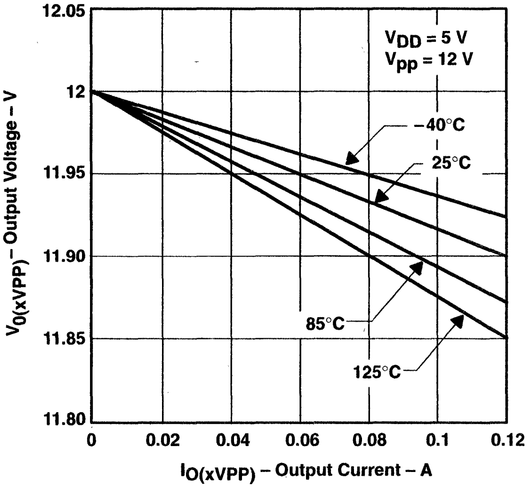

Figure 21

5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

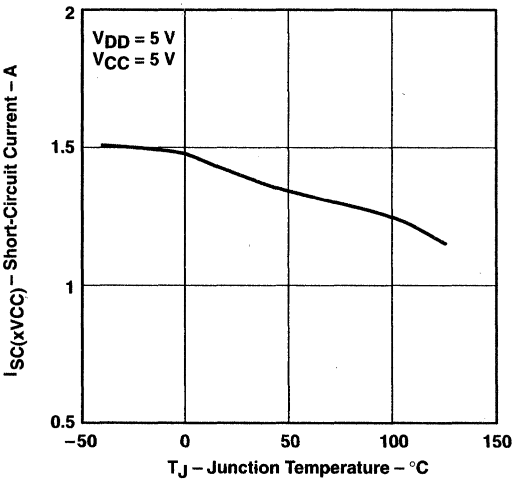

Figure 22

12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

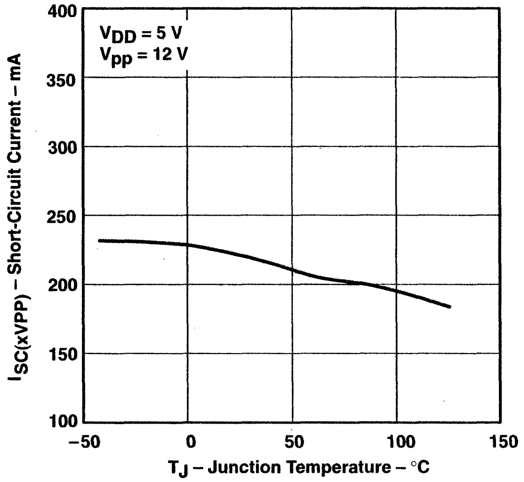

Figure 23

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† t = pulse tested

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC card, and semiconductor manufacturers. One key goal was to realize the "plug and play" concept. Cards and hosts from different vendors should be compatible – able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the PC Card connector's 68 terminals. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals. As each terminal is rated to 0.5 A, V_{CC} and V_{pp} can theoretically supply up to 1 A, assuming equal terminal resistance and no terminal failure. A conservative design would limit current to 500 mA. Some applications, however, require higher V_{CC} currents. Disk drives, for example, may need as much as 750-mA peak current to create the initial torque necessary to spin up the platter. V_{pp} currents, on the other hand, are defined by flash-memory programming requirements, typically under 120 mA.

future power trends

The 1-A physical-terminal current alluded to in the PC Card specification has caused some host-system engineers to believe they are required to deliver 1 A within the voltage tolerance of the card. Future applications, such as RF cards, could use the extra power for their radio transmitters. The 5 W required for these cards require very robust power supplies and special cooling considerations. The limited number of host sockets that are able to support cards makes the market for these high-powered PC Cards uncertain. The vast majority of the cards require less than 600 mA continuous current and the trend is towards even lower powered PC Cards that assure compatibility with a greater number of host systems. Recognizing the need for power derating, an ad hoc committee of the PCMCIA is currently working to limit the amount of steady-state dc current to the PC Card to something less than the currently implied 1 A. When a system is designed to support 1 A, the switch $r_{DS(on)}$, power-supply requirements, and PC Card cooling need to be carefully considered.

designing around 1-A delivery

Delivering 1 A means minimizing voltage and power losses across the PC Card power interface, which requires that designers trade off switch resistance and the cost associated with large-die (low $r_{DS(on)}$) MOSFET transistors. The PC Card standard requires that 5 V ±5% or 3.3 V ±0.3 V be supplied to the card. The approximate 10% tolerance for the 3.3-V supply makes the 3.3-V $r_{DS(on)}$ less critical than the 5-V switch. A conservative approach is to allow 2% for voltage-regulator tolerance and 1% for etch- and pin-resistance drops, which leaves 2% (100 mV) for voltage drop at the 5-V switch and at least 6% (198 mV) for the 3.3-V switch.

Calculating the $r_{DS(on)}$ necessary to support a 100 mV or 198 mV switch loss, using R = E/I and setting I = 1 A, the 5-V and 3.3-V switches would need to be 100 mΩ and 198 mΩ respectively. One solution would be to pay for a more expensive switch with lower $r_{DS(on)}$. A second, less expensive approach is to increase the headroom of the power supply–for example, to increase the 5 V supply 1.5% or to 5.075 ±2%. Working through the numbers once more, the 2% for the regulator plus 1 % for etch and terminal losses leaves 97% or 4.923 V. The allowable

APPLICATION INFORMATION

designing around 1-A delivery (continued)

voltage loss across the power distribution switch is now 4.923 V minus 4.750 V or 173 mV. Therefore, a switch with 173 mΩ or less could deliver 1 A or greater. Setting the power supply high is a common practice for delivering voltages to allow for system switch, connector, and etch losses. This practice has a minimal effect on overall battery life. In the example above, setting the power supply 1.5% high would only decrease a 3-hour battery life by approximately 2.7 minutes, trivial when compared with the decrease in battery life when running a 5-W PC Card.

heat dissipation

A greater concern in delivering 1 A or 5 W is the ability of the host to dissipate the heat generated by the PC Card. For desktop computers the solution is simpler: locate the PC Card cage such that it receives convection cooling from the forced air of the fan. Notebooks and other handheld equipment will not be able to rely on convection, but on conduction of heat away from the PC Card through the rails into the card cage. This is difficult because PC Card/card cage heat transfer is very poor. A typical design scenario would require the PC Card to be held at 60°C maximum with the host platform operating as high as 50°C. Preliminary testing reveals that a PC Card can have a 20°C rise, exceeding the 10°C differential in the example, when dissipating less than 2 W of continuous power. Sixty degrees centigrade was chosen because it is the maximum operating temperature allowable by PC Card specification. Power handling requirements and temperature rises are topics of concern and are currently being addressed by the PCMCIA committee.

overcurrent and over-temperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. This can be particularly frustrating to the consumer who has already experienced problems with shortened battery life due to improper Nicad conditioning or memory effect. Most hosts include fuses for protection. The reliability of fused systems is poor though, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2202AI takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an added advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2202AI asserts a signal at $\overline{\text{OC}}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{pp} power for switch-gate drive and other chip functions, which requires that power be present at all times. The TPS2202AI offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V V_{DD} supply; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the TPS2202AI during a software shutdown in which quiescent current drops to a maximum of 1 μA.

APPLICATION INFORMATION

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2202AI is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2202AI offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100 kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis will reveal that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2202AI is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial controller interface. The TPS2202AI offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

power supply considerations

The TPS2202AI has multiple pins for each of its 3.3-V, 5-V, and 12-V power inputs and for the switched V_{CC} outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12-V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power pins be paralleled for optimum operation. The V_{DD} input lead must be connected to the 5-V input leads.

Although the TPS2202AI is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-µF or larger capacitor; doing so improves the immunity of the TPS2202AI to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2202AI and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance.

The TPS2202AI, unlike other PC Card power-interface switches, does not use the 12-V power supply for switching or other chip functions. Instead, an internal charge pump generates the necessary voltage from V_{DD}, allowing the 12-V input supply to be shut down except when the V_{pp} programming or erase voltage is needed. Careful system design using this feature reduces power consumption and extends battery lifetime.

The 3.3-V power input should not be taken higher than the 5-V input. Though doing so is nondestructive, this results in high current flow into the device and could result in abnormal operation. In any case, this occurrence indicates a malfunction of one input voltage or both which should be investigated.

Similarly, no pin should be taken below –0.3 V; forward biasing the parasitic-substrate diode results in substrate currents and unpredictable performance.

APPLICATION INFORMATION

RESET or $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying a low impedance to the V_{CC} and V_{pp} terminals. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The RESET or $\overline{\text{RESET}}$ input will close internal switches S1, S4, S7, and S10 with all other switches left open (see TPS2202AI control-logic table). The TPS2202AI remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. RESET or $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The unused pin is internally pulled up or down and should be left unconnected.

overcurrent and thermal protection

The TPS2202AI uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{\text{OC}}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2202AI controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2202AI engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2202AI may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to activate if powered up, into a short in the range of 0.75 A to 1.9 A, typically at about 1.3 A. The V_{pp} outputs limit from 120 mA to 400 mA, typically around 200 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16, 17, and 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma P_D \times R_{\theta JA}\right) + T_A, \; R_{\theta JA} = 108°\text{C/W}$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

APPLICATION INFORMATION

logic input and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 9-bit (D0 through D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 µA to conserve battery power.

The TPS2202AI serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} outputs as previously discussed.

APPLICATION INFORMATION

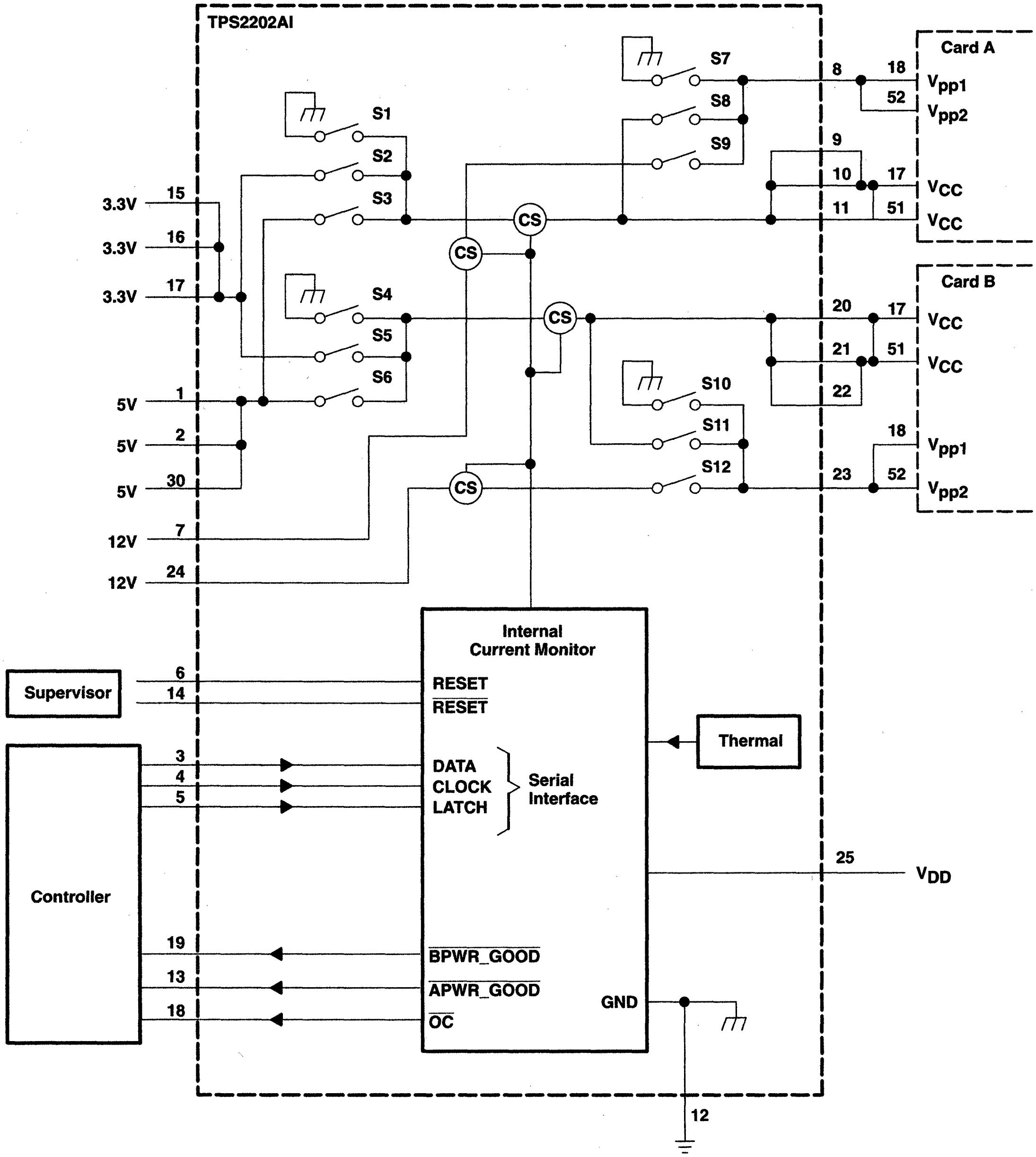


Figure 24. Internal Switching Matrix

APPLICATION INFORMATION

TPS2202AI control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D0 A_VPP_PGM	D1 A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[†]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D4 B_VPP_PGM	D5 B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[‡]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D3 $\overline{\text{A\_VCC3}}$	D2 $\overline{\text{A\_VCC5}}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D6 $\overline{\text{B\_VCC3}}$	D7 $\overline{\text{B\_VCC5}}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

[†] Output depends on AVCC
[‡] Output depends on BVCC

ESD protection

All TPS2202AI inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

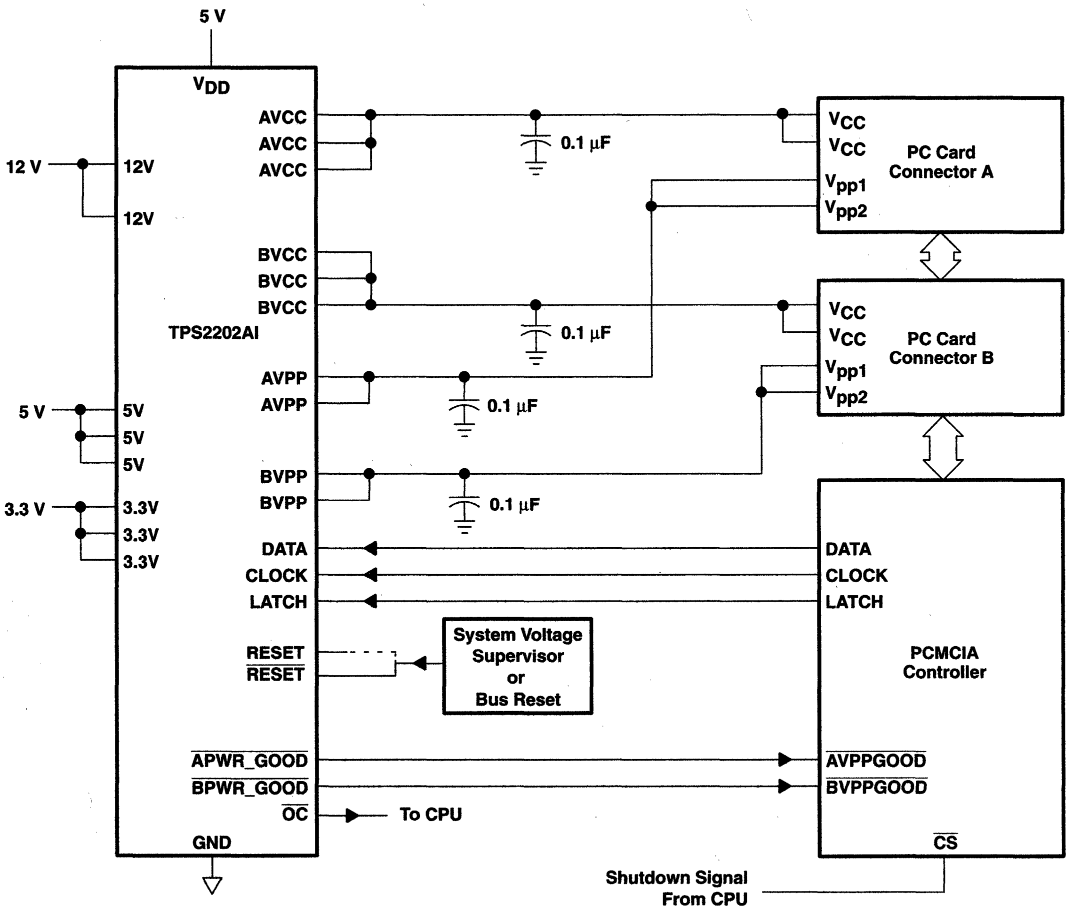


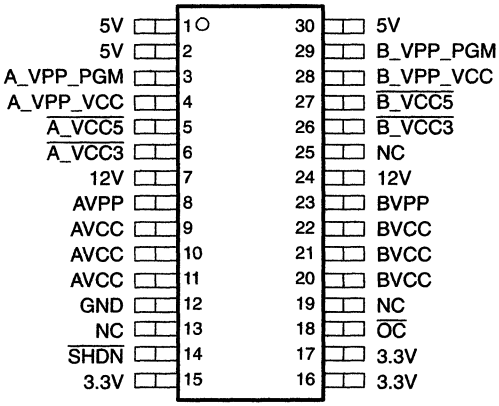
Figure 25. Detailed Interconnections and Capacitor Recommendations

TPS2205I
DUAL-SLOT PC CARD POWER-INTERFACE SWITCH WITH SUSPEND MODE FOR PARALLEL PCMCIA CONTROLLER

SLVS128 – OCTOBER 1995

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card™ Interface**
- **Suspend Mode (3.3 V only)**
- **Compatible With Controllers From Cirrus, Intel, and Texas Instruments**
- **Meets PCMCIA Standards**
- **Internal Charge Pump (No External Capacitors Required) – 12-V Supply Can Be Disabled Except for Programming**
- **Short Circuit and Thermal Protection**
- **SSOP (30) Package Less than 2 mm High**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Power Saving I_{DD} = 83 μA Typ, I_Q = 1 μA**
- **Low $r_{DS(on)}$ (150-mΩ 5-V Switch; 200-mΩ 3.3-V Switch)**
- **Break-Before-Make Switching**

DF or DB PACKAGE
(TOP VIEW)



NC - No Internal Connection

description

The TPS2205 PC Card (PCMCIA) power interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting and reporting, and thermal protection for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V and/or 12-V card power and is compatible with most PCMCIA controllers. The suspend mode allows the TPS2205 to operate off of 3.3-V input pins during modem or pager operations. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability; current-limit reporting can help the user isolate a system fault to a bad card.

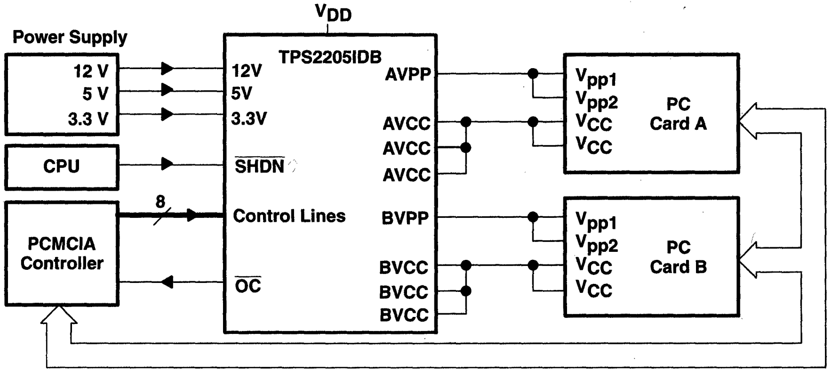
The TPS2205 maximizes battery life by generating its own switch-drive voltage using an internal charge pump. Therefore, the 12-V supply can be powered down and only brought out of standby when flash memory needs to be written to or erased. End equipment for the TPS2205 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handiterminals, and bar-code scanners.

The TPS2205I is only available in the DB package, left-end taped and reeled (indicated by the LE suffix on the device type; when ordering, specify TPS2205IDBLE).

LinBiCMOS is a trademark of Texas Instruments Incorporated.
PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

PRODUCT PREVIEW

typical PC Card power distribution application



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}	−0.3 V to 7 V
Input voltage range for card power: $V_{I(5V)}$	−0.3 V to 7 V
$V_{I(3.3V)}$	−0.3 V to $V_{I(5V)}$
$V_{I(12V)}$	−0.3 V to 14 V
Logic input voltage	−0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$	internally limited
$I_{O(xVPP)}$	internally limited
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DF	1158 mW	9.26 mW/°C	741 mW	602 mW
DB	1024 mW	8.2 mW/°C	655 mW	532 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{A\_VCC3}}$	6	I	Logic input that controls voltage on AVCC (see control-logic table)
$\overline{\text{A\_VCC5}}$	5	I	Logic input that controls voltage on AVCC (see control-logic table)
A_VPP_PGM	3	I	Logic input that controls voltage on AVPP (see control-logic table)
A_VPP_VCC	4	I	Logic input that controls voltage on AVPP (see control-logic table)
AVCC	9, 10, 11	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
AVPP	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{B\_VCC3}}$	26	I	Logic input that controls voltage on BVCC (see control-logic table)
$\overline{\text{B\_VCC5}}$	27	I	Logic input that controls voltage on BVCC (see control-logic table)
B_VPP_PGM	29	I	Logic input that controls voltage on BVPP (see control-logic table)
B_VPP_VCC	28	I	Logic input that controls voltage on BVPP (see control-logic table)
BVCC	20, 21, 22	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{SHDN}}$	14	I	Logic input that shuts down the TPS2205 and set all power outputs to high-impedance state
$\overline{\text{OC}}$	18	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
V_{DD}	25		5-V power to chip
GND	12		Ground
3.3V	15, 16, 17	I	3.3-V V_{CC} in for card power
5V	1, 2, 30	I	5-V V_{CC} in for card power
12V	7, 24	I	12-V VPP in for card power
NC	13,19		

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		TBD	TBD	V
Input voltage range, V_I	$V_{I(5\ V)}$	0	5.25	V
	$V_{I(3.3\ V)}$	0	$V_{I(5\ V)}$†	V
	$V_{I(12\ V)}$	0	13.5	V
Output current	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Operating virtual junction temperature, T_J		−40	125	°C

† $V_{I(3\ V)}$ should not be taken above $V_{I(5\ V)}$.

PRODUCT PREVIEW

electrical characteristics, T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

dc characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch resistances	5 V to xVCC			150		mΩ
	3.3 V to xVCC			200		mΩ
	3.3 V to xVCC	Suspend mode		500		mΩ
	5 V to xVPP				6	Ω
	3.3 V to xVPP				6	
	12 V to xVPP				1	
$V_{O(xVPP)}$ Clamp low voltage		I_{PP} at 10 mA			0.8	V
$V_{O(xVCC)}$ Clamp low voltage		I_{CC} at 10 mA			0.8	V
Leakage current	I_{PP} High-impedance state	T_A = 25°C		1	10	µA
		T_A = 85°C			50	
	I_{CC} High-impedance state	T_A = 25°C		1	10	
		T_A = 85°C			50	
Input current	I_{DD} Supply current	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V		83	150	µA
	I_{DD} Supply current in shutdown	$V_{O(BVCC)} = V_{O(AVCC)} = V_{O(AVPP)}$ $= V_{O(BVPP)}$ = high Z			1	µA
Power-ready threshold, $\overline{\text{PWR\_GOOD}}$			10.72	11.05	11.4	V
Power-ready hysteresis, $\overline{\text{PWR\_GOOD}}$	12-V mode			50		mV
Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output shorted to GND	1			A
	$I_{O(xVPP)}$		120	200	400	mA

electrical characteristics, $T_A = 25°C$, $V_{DD} = 5$ V (unless otherwise noted) (continued)

logic section

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$I_O = 1$ mA	$V_{DD}-0.4$		V
Logic output low level			0.4	V

switching characteristics†

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r, t_f	Output rise and fall times	$V_{O(xVCC)}$ rise time			1.2		ms
		$V_{O(xVCC)}$ fall time			10		ms
		$V_{O(xVPP)}$ rise time			5		ms
		$V_{O(xVPP)}$ fall time			14		ms
t_{pd}	Propagation delay (see Figure 1‡)	$V_{I(x\_VPP\_PGM)}$ to $V_{O(xVPP)}$	t_{on}		5.8		ms
			t_{off}		18		ms
		$V_{I(\overline{x\_VCC3})}$ to xVCC	t_{on}		5.8		ms
			t_{off}		28		ms
		$V_{I(\overline{x\_VCC5})}$ to xVCC	t_{on}		4		ms
			t_{off}		30		ms

† Refer to Parameter Measurement Information
‡ Rise and fall times are with $C_L = 100$ µF.

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

TPS2205 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	A_VPP_PGM	A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[†]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	B_VPP_PGM	B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC[‡]
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	$\overline{\text{A\_VCC3}}$	$\overline{\text{A\_VCC5}}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	$\overline{\text{B\_VCC3}}$	$\overline{\text{B\_VCC5}}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

[†] Output depends on AVCC
[‡] Output depends on BVCC

Contents

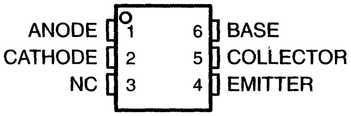
4N25, 4N26, 4N27, 4N28
OPTOCOUPLERS

SOES020 – SEPTEMBER 1978 – REVISED OCTOBER 1995

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium-Arsenide-Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation 2.5-kV, 1.5-kV, or 0.5-kV Rating**
- **Plastic Dual-Inline Package**
- **High-Speed Switching t_r = 2 µs, t_f = 2 µs Typical**

4N25, 4N26, 4N27, OR 4N28 . . . PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Peak input-to-output voltage‡: 4N25	± 2.5 kV
4N26, 4N27	± 1.5 kV
4N28	± 0.5 kV
Collector-base voltage‡	70 V
Collector-emitter voltage‡ (see Note 1)	30 V
Emitter-collector voltage‡	7 V
Emitter-base voltage	7 V
Input-diode reverse voltage‡	3 V
Input-diode continuous forward current at (or below) 25°C free-air temperature‡ (see Note 2)	80 mA
Input-diode peak forward current‡ (t_w = 300 µs, duty cycle = 2 %)	3 A
Continuous power dissipation at (or below) 25°C free-air temperature‡:	
Infrared-emitting diode (see Note 3)	150 mW
Phototransistor (see Note 3)	150 mW
Total, infrared-emitting diode plus phototransistor (see Note 4)	250 mW
Storage temperature range, T_{stg}‡	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds‡	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ JEDEC registered data. This data sheet contains all applicable JEDEC-registered data in effect at the time of publication.

NOTES:
1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100 °C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100 °C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100 °C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	4N25, 4N26			4N27, 4N28			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$†	Collector-base breakdown voltage	I_C = 100 μA, I_E = 0, I_F = 0	70			70			V
$V_{(BR)CEO}$†	Collector-emitter breakdown voltage	I_C =1 mA, I_B = 0, I_F = 0	30			30			V
$V_{(BRECO)}$†	Emitter-collector breakdown voltage	I_E = 100 μA, I_B = 0, I_F = 0	7			7			V
I_R†	Input diode static reverse current	V_R = 3 V			100			100	μA
$I_{C(on)}$†	On-state collector current (phototransistor operation)	V_{CE} = 10 V, I_B = 0, I_F = 10 mA	2	5		1	3		mA
$I_{C(on)}$	On-state collector current (phototransistor operation)	V_{CB} = 10 V, I_E = 0, I_F = 10 mA		20			20		μA
$I_{C(off)}$†	Off-state collector current (phototransistor operation)	V_{CE} = 10 V, I_B = 0, I_F = 0		1	50		1	50	nA
$I_{C(off)}$†	Off-state collector current (photodiode operation)	V_{CB} = 10 V, I_E = 0, I_F = 0		0.1	20		0.1	20	nA
V_F†	Input diode static forward voltage	I_F = 10 mA		1.25	1.5		1.25	1.5	V
$V_{CE(sat)}$†	Collector-emitter saturation voltage	I_C = 2 mA, I_B = 0, I_F = 50 mA		0.25	0.5		0.25	0.5	V
r_{IO}	Input-to-output internal resistance	V_{in-out} = ±2.5 kV for 4N25, ±1.5 kV for 4N26, 4N27, ±0.5 kV for 4N28, See Note 5	10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-output capacitance	V_{in-out} = 0, f = 1 MHz, See Note 5		1			1		pF

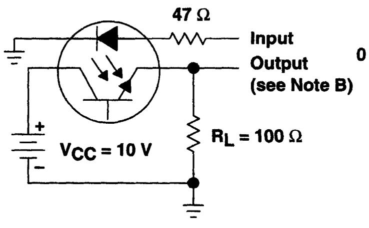
† JEDEC registered data

NOTE 5: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

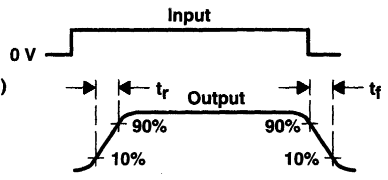
switching characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, I_B = 0, $I_{C(on)}$ 2 mA		2		μs
t_f	Fall time		R_L = 100 Ω, See Test Circuit A of Figure 1		2		
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, I_E = 0, $I_{C(on)}$ 20 μA		1		μs
t_f	Fall time		R_L = 1 kΩ, See Test Circuit B of Figure 1		1		

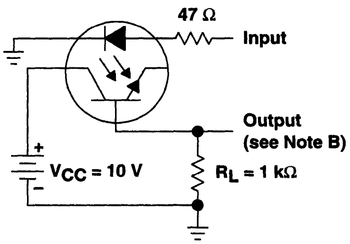
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS

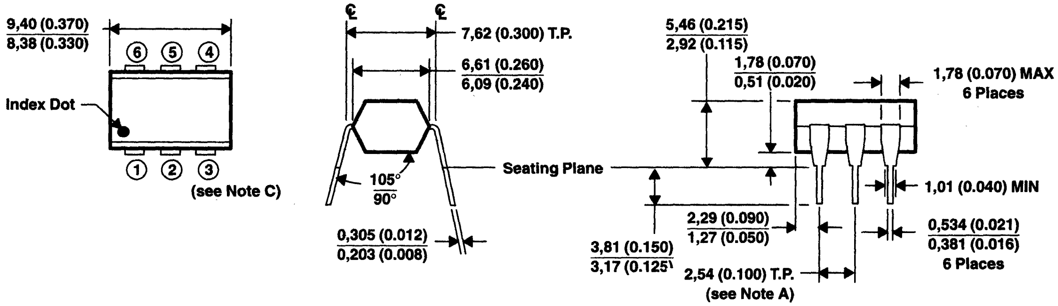


TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r \le 15$ ns, duty cycle ≈ 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \le 12$ ns, $R_{in} \ge 1$ MΩ, $C_{in} \le 20$ pF.

MECHANICAL INFORMATION

The package consists of a gallium-arsenide infrared-emitting diode and an npn silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode (part of the infrared-emitting diode)
2. Cathode (part of the infrared-emitting diode)
3. No internal connection
4. Emitter (part of the phototransistor)
5. Collector (part of the phototransistor)
6. Base (part of the phototransistor)
D. The dimensions given fall within JEDEC MO-001 AM dimensions.
E. All linear dimensions are given in millimeters and parenthetically given in inches.

Figure 1. Mechanical Information

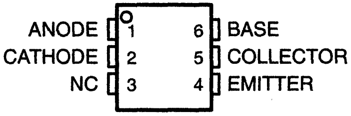
4N35, 4N36, 4N37
OPTOCOUPLERS

SOES021 – NOVEMBER 1981 – REVISED OCTOBER 1995

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium-Arsenide-Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation 1.5-kV, 2.5-kV, or 3.55-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching $t_r = 7\ \mu s$, $t_f = 7\ \mu s$ Typical**
- **Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays and Pulse Transformers**

4N35, 4N36, OR 4N37 . . . PACKAGE (TOP VIEW)



NC – No internal connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†‡

Input-to-output peak voltage (8-ms half sine wave):	4N35	3.55 kV
	4N36	2.5 kV
	4N37	1.5 kV
Input-to-output root-mean-square voltage (8-ms half sine wave):	4N35	2.5 kV
	4N36	1.75 kV
	4N37	1.05 kV
Collector-base voltage		70 V
Collector-emitter voltage (see Note 1)		30 V
Emitter-base voltage		7 V
Input-diode reverse voltage		6 V
Input-diode forward current:	Continuous	60 mA
	Peak (1 µs, 300 pps)	3 mA
Phototransistor continuous collector current		100 mA
Continuous total power dissipation at (or below) 25°C free-air temperature:		
Infrared-emitting diode (see Note 2)		100 mW
Phototransistor (see Note 3)		300 mW
Continuous power dissipation at (or below) 25°C lead temperature:		
Infrared-emitting diode (see Note 4)		100 mW
Phototransistor (see Note 5)		500 mW
Operating temperature range, T_A		–55°C to 100°C
Storage temperature range, T_{stg}		–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

NOTES:
1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100 °C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100 °C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100 °C lead temperature at the rate of 1.33 mW/°C. Lead temperature is measured on the collector lead 0.8 mm (1/32 inch) from the case.
5. Derate linearly to 100°C lead temperature at the rate of 6.7 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C = 100\ \mu A$, $I_E = 0$, $I_F = 0$	70†			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C = 10\ mA$, $I_B = 0$, $I_F = 0$	30†			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E = 100\ \mu A$, $I_C = 0$, $I_F = 0$	7†			V
I_R	Input diode static reverse current	$V_R = 6\ V$			10†	µA
I_{IO}	Input-to-output current	V_{IO} = rated peak value, t = 8 ms			100	mA
$I_{C(on)}$	On-state collector current	$V_{CE} = 10\ V$, $I_F = 10\ mA$, $I_B = 0$	10†			mA
		$V_{CE} = 10\ V$, $I_F = 10\ mA$, $I_B = 0$, $T_A = -55°C$	4†			
		$V_{CE} = 10\ V$, $I_F = 10\ mA$, $I_B = 0$, $T_A = 100°C$	4†			
$I_{C(off)}$	Off-state collector current	$V_{CE} = 10\ V$, $I_F = 0$, $I_B = 0$		1	50	nA
		$V_{CE} = 30\ V$, $I_F = 0$, $I_B = 0$, $T_A = 100°C$			500†	µA
h_{FE}	Transistor Static Forward Current Transfer Ratio	$V_{CE} = 5\ V$, $I_C = 10\ mA$, $I_F = 0$		500		
V_F	Input diode static forward voltage	$I_F = 10\ mA$	0.8†		1.5†	V
		$I_F = 10\ mA$, $T_A = -55°C$	0.9†		1.7†	
		$I_F = 10\ mA$, $T_A = 100°C$	0.7†		1.4†	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$I_C = 0.5\ mA$, $I_F = 10\ mA$, $I_B = 0\ mA$			0.3†	V
r_{IO}	Input-to-output internal resistance	$V_{IO} = 500\ V$, See Note 6	10^{11}†			Ω
C_{io}	Input-to-output capacitance	$V_{IO} = 0$, f = 1 MHz, See Note 6		1	2.5†	pF

† JEDEC registered data

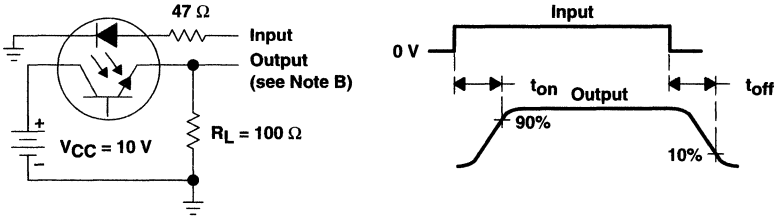
NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Time-on time	$V_{CC} = 10\ V$,	$I_{C(on)} = 2\ mA$,			10	µs
t_{off}	Turn-off time	$R_L = 100\ \Omega$,	See Figure 1			10	

† JEDEC registered data

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1% t_w = 100 μs.

B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

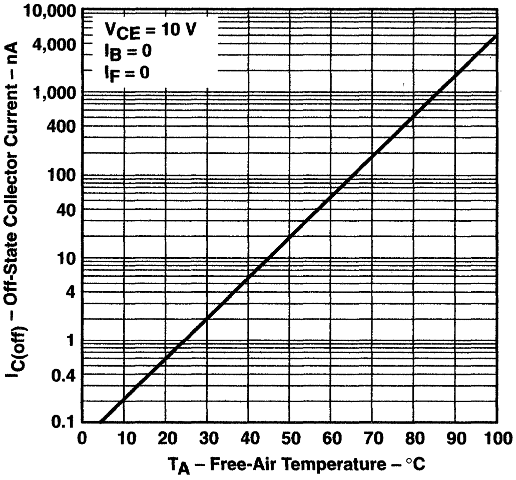


Figure 2

TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO (NORMALIZED)
vs
ON-STATE COLLECTOR CURRENT

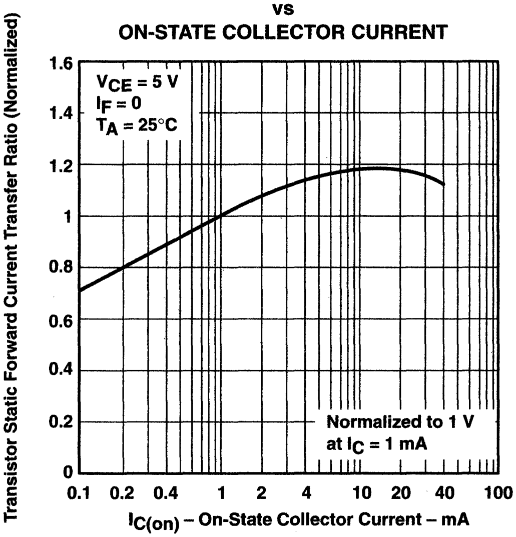


Figure 3

TYPICAL CHARACTERISTICS

**COLLECTOR CURRENT
vs
MODULATION FREQUENCY**

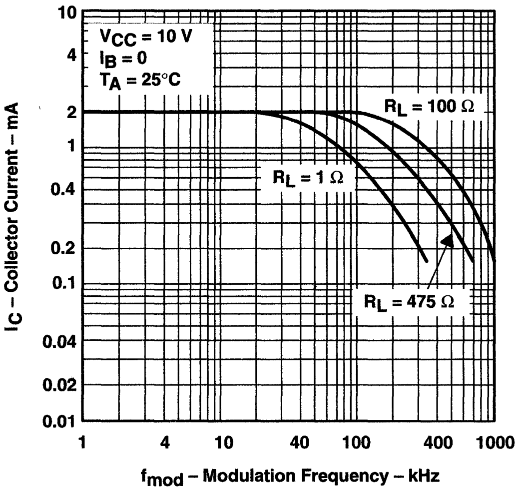


Figure 4

**INPUT-DIODE FORWARD
CONDUCTION CHARACTERISTICS**

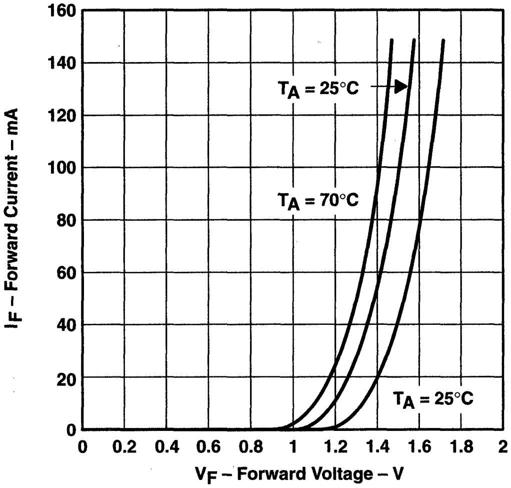


Figure 5

**COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT**

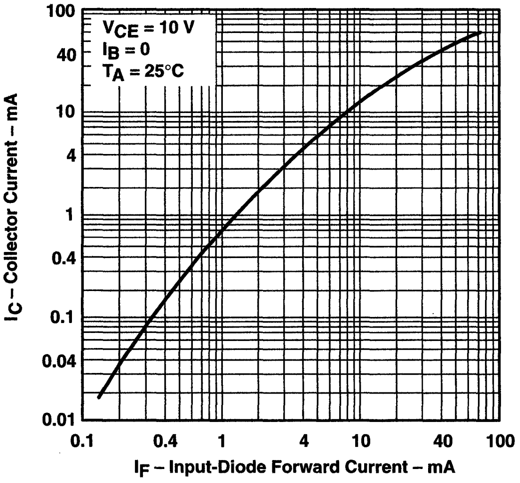
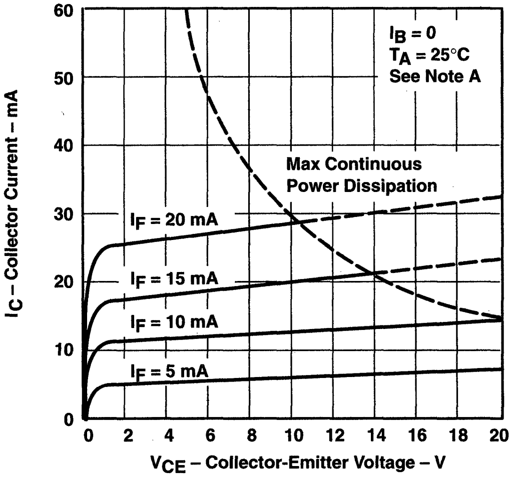


Figure 6

**COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE**

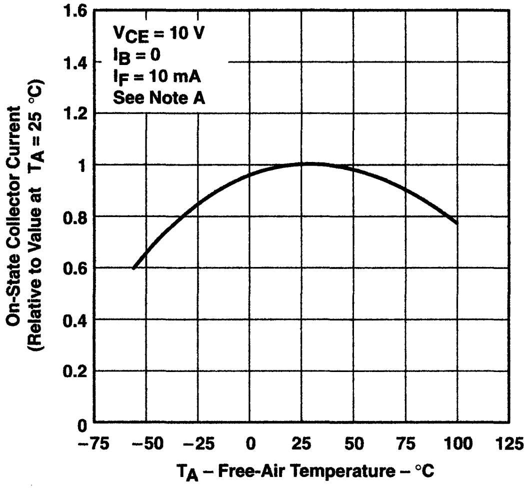


NOTE A. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.

Figure 7

TYPICAL CHARACTERISTICS

ON-STATE COLLECTOR CURRENT (RELATIVE TO VALUE AT 25°C) vs FREE-AIR TEMPERATURE

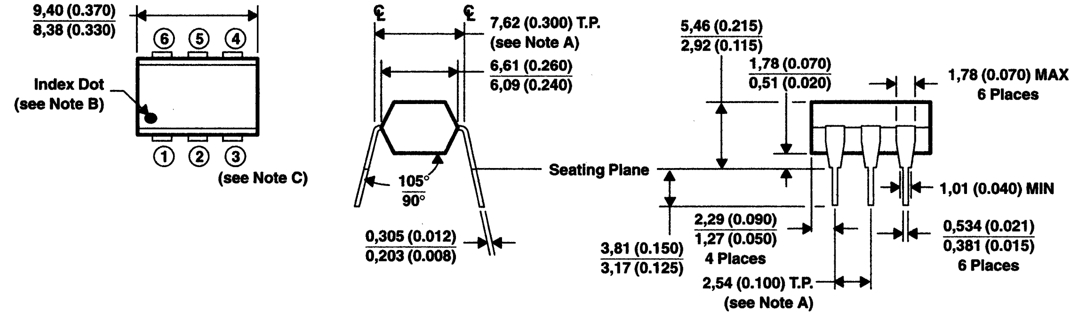


NOTE A. These parameters were measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 2 %.

Figure 8

MECHANICAL INFORMATION

The package consists of a gallium-arsenide infrared-emitting diode and an npn silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
- A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
- B. Pin 1 identified by index dot.
- C. Terminal connections:
  1. Anode (part of the infrared-emitting diode)
  2. Cathode (part of the infrared-emitting diode)
  3. No internal connection
  4. Emitter (part of the phototransistor)
  5. Collector (part of the phototransistor)
  6. Base (part of the phototransistor)
- D. The dimensions given fall within JEDEC MO-001 AM dimensions.
- E. All linear dimensions are given in millimeters and parenthetically given in inches.

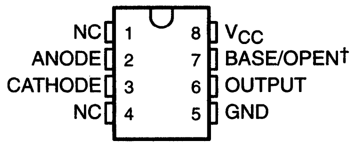
Figure 9. Mechanical Information

6N135, 6N136, HCPL4502
OPTOCOUPLERS/OPTOISOLATORS

SOES022 – JULY 1986 – REVISED OCTOBER 1995

- **Compatible with TTL Inputs**
- **High-Speed Switching . . . . 1 Mbit/s Typ**
- **Bandwidth . . . 2 MHz Typ**
- **High Common-Mode Transient Immunity . . . . 1000 V/µs Typ**
- **High-Voltage Electrical Insulation . . . 3000 VDC Min**
- **Open-Collector Output**
- **UL Recognized . . . File Number 65085**

6N135, 6N136, OR HCPL4502 PACKAGE (TOP VIEW)



† Terminal 7 is BASE on the 6N135 and 6N136 and OPEN on the HCPL4502

NC – No internal connection

description

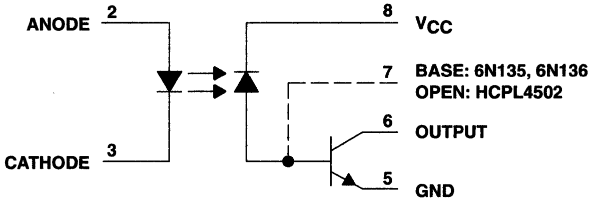
These high-speed optocouplers are designed for use in analog or digital interface applications that require high-voltage isolation between the input and output. Applications include line receivers that require high common-mode transient immunity, and analog or logic circuits that require input-to-output electrical isolation.

The 6N135, 6N136, and HCPL4502 optocouplers each consists of a light-emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor-collector output. This feature, which reduces the transistor base-to-collector capacitance, results in speeds up to one hundred times that of a conventional phototransistor optocoupler.

The 6N135 is designed for TTL/CMOS, TTL/LSTTL, and wide-band analog applications.

The 6N136 and HCPL4502 are designed for high-speed TTL/TTL applications. The HCPL4502 has no base connection.

schematic



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†‡

Supply and output voltage range, V_{CC} and V_O	−0.5 V to 15 V
Reverse input voltage	5 V
Emitter-base reverse voltage	5 V
Peak input forward current (pulse duration = 1 ms, 50% duty cycle, see Note 1)	50 mA
Peak transient input forward current (pulse duration 1 μs, 300 Hz)	1 A
Average forward input current(see Note 2)	25 mA
Peak output current	16 mA
Average output current	8 mA
Base current	5 mA
Input power dissipation at (or below) 70°C free-air temperature (see Note 3)	45 mW
Output power dissipation at (or below) 70°C free-air temperature (see Note 4)	100 mW
Storage temperature range, T_{stg}	−55°C to 125°C
Operating free-air temperature range, T_A	−55°C to 100°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ JEDEC registered data for 6N135 and 6N136

NOTES:
1. Derate linearly above 70°C free-air temperature at the rate of 1.67 mA/°C.
2. Derate linearly above 70°C free-air temperature at the rate of 0.83 mA/°C.
3. Derate linearly above 70°C free-air temperature at the rate of 1.50 mW/°C.
4. Derate linearly above 70°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics over operating free-air temperature range of 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		6N135			6N136, HCPL4502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_F‡	Input forward voltage	$I_F = 16$ mA,	$T_A = 25°C$		1.6	1.7		1.6	1.7	V
∝VF	Temperature coefficient of forward voltage	$I_F = 16$ mA			−1.8			−1.8		mV/°C
V_{BR}‡	Input breakdown voltage	$I_R = 10$ µA,	$T_A = 25°C$	5			5			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.5$ V, $I_F = 16$ mA, $I_B = 0$	$I_{OL} = 1.1$ mA		0.1	0.4				V
			$I_{OL} = 2.4$ mA					0.1	0.4	
I_{OH}‡	High-level output current	$I_F = 0$, $I_B = 0$, $T_A = 25°C$	$V_{CC} = V_O = 5.5$ V		3	500		3	500	nA
			$V_{CC} = V_O = 15$ V		0.01	1		0.01	1	µA
I_{OH}	High-level output current	$V_{CC} = 15$ V, $I_F = 0$,	$V_O = 15$ V, $I_B = 0$			50			50	µA
I_{CCH}‡	Supply current, high-level output	$V_{CC} = 15$ V, $I_F = 0$, $T_A = 25°C$	$I_O = 0$, $I_B = 0$,		0.02	1		0.02	1	µA
I_{CCH}	Supply current, high-level output	$V_{CC} = 15$ V, $I_F = 0$,	$I_O = 0$, $I_B = 0$			2			2	µA
I_{CCL}	Supply current, low-level output	$V_{CC} = 15$ V, $I_F = 16$ mA,	$I_O = 0$, $I_B = 0$		40			40		µA
h_{FE}	Transistor forward current transfer ratio	$V_O = 5$ V,	$I_O = 3$ mA		100			100 (6N136 only)		
CTR‡	Current transfer ratio	$V_{CC} = 4.5$ V, $I_F = 16$ mA, $T_A = 25°C$,	$V_O = 0.4$ V, $I_B = 0$, See Note 5	7%	18%		19%	24%		
CTR	Current transfer ratio	$V_{CC} = 4.5$ V, $I_F = 16$ mA, See Note 5	$V_O = 0.5$ V, $I_B = 0$,	5%			15%			
r_{IO}	Input-output resistance	$V_{IO} = 500$ V, See Note 6	$T_A = 25°C$,		10^{12}			10^{12}		Ω
I_{IO}‡	Input-output insulation leakage current	$V_{IO} = 3000$ V, $T_A = 25°C$, See Note 6	$t = 5$ s, RH = 45%,			1			1	µA
C_i	Input capacitance	$V_F = 0$,	$f = 1$ MHz		60			60		pF
C_{io}	Input-output capacitance	$f = 1$ MHz,	See Note 6		0.6			0.6		pF

† All typical values are at $T_A = 25°C$.
‡ JEDEC registered data for 6N135 and 6N136

NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured with terminals 2 and 3 shorted together and terminals 5, 6, 7, and 8 shorted together.

operating characteristics, V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		6N135			6N136, HCPL4502		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	

PARAMETER		TEST CONDITIONS	6N135 MIN	6N135 TYP	6N135 MAX	6N136, HCPL4502 MIN	6N136, HCPL4502 TYP	6N136, HCPL4502 MAX	UNIT
BW	Bandwidth (−3 dB)	R_L = 100 Ω, See Note 7		2			2		MHz

NOTE 7: Bandwidth is the range of frequencies within which the ac output voltage is not more than 3 dB below the low-frequency value.

switching characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C

PARAMETER		TEST CONDITIONS	6N135 MIN	6N135 TYP	6N135 MAX	6N136, HCPL4502 MIN	6N136, HCPL4502 TYP	6N136, HCPL4502 MAX	UNIT
t_{PLH}†	Propagation delay time, low-to-high-level output	R_L = 4.1 kΩ, See Note 8, See Figure 1		1	1.5				μs
		R_L = 1.9 kΩ, See Note 9, See Figure 1					0.6	0.8	
t_{PHL}†	Propagation delay time, high-to-low-level output	R_L = 4.1 kΩ, See Note 8, See Figure 1		0.7	1.5				μs
		R_L = 1.9 kΩ, See Note 9, See Figure 1					0.6	0.8	
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, I_F = 0, R_L = 4.1 kΩ, See Notes 8 and 10, See Figure 2		1000					V/μs
		ΔV_{CM} = 10 V, I_F = 0, R_L = 1.9 kΩ, See Notes 9 and 10, See Figure 2					−1000		
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = 10 V, R_L = 4.1 kΩ, See Notes 9 and 10, See Figure 2		−1000					V/μs
		ΔV_{CM} = 10 V, R_L = 1.9 kΩ, See Notes 9 and 10, See Figure 2					−1000		

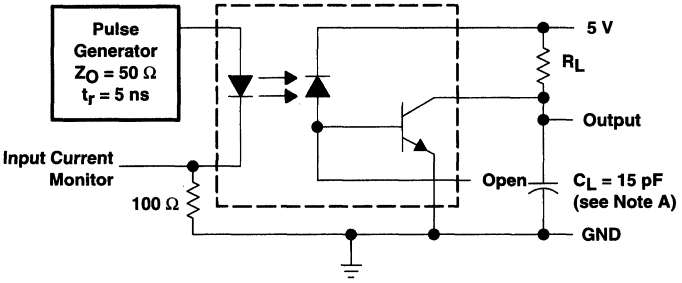
† JEDEC registered data for 6N135 and 6N136

NOTES: 8. The 4.1-kΩ load represents one LSTTL unit load of 0.36 mA and a 6.1-kΩ pullup resistor.

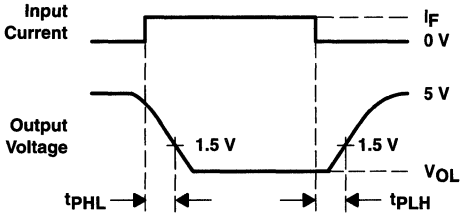
9. The 1.9-kΩ load represents one TTL unit load of 1.6 mA and a 5.6-kΩ pullup resistor.

10. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

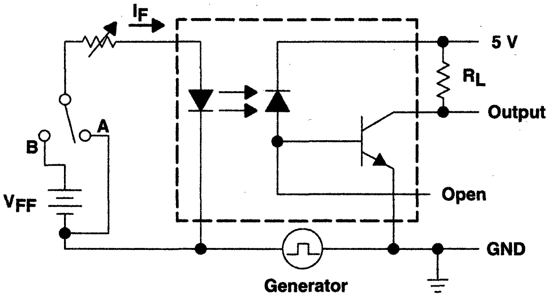


WAVEFORMS

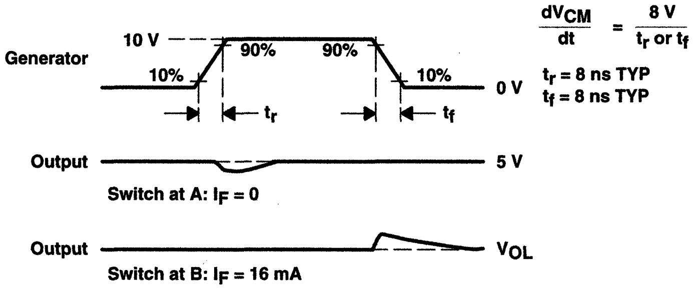
NOTE A. C_L includes probe and stray capacitance.

Figure 1. Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Transient Immunity Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

INPUT-DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

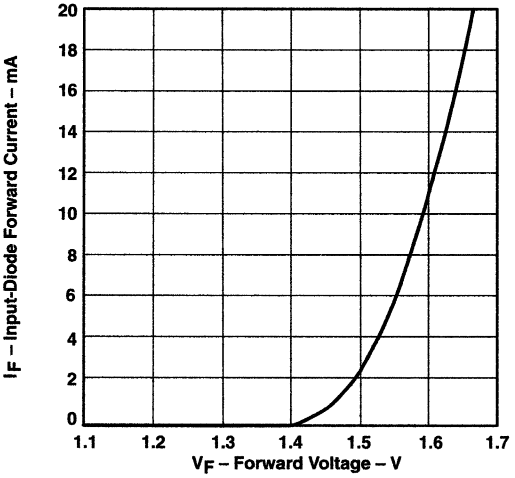


Figure 3

6N135
CURRENT TRANSFER CHARACTERISTICS

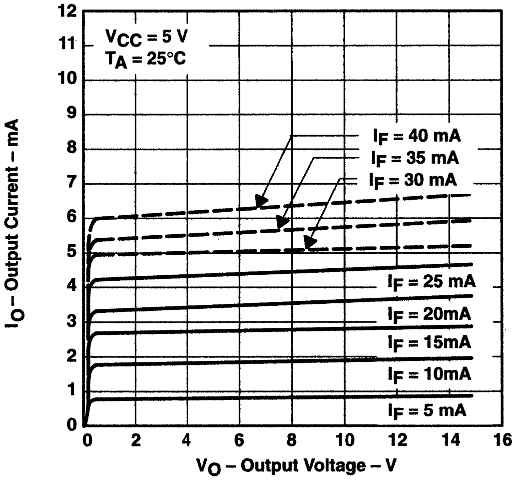


Figure 4

CURRENT TRANSFER RATIO (NORMALIZED)
vs
INPUT DIODE FORWARD CURRENT

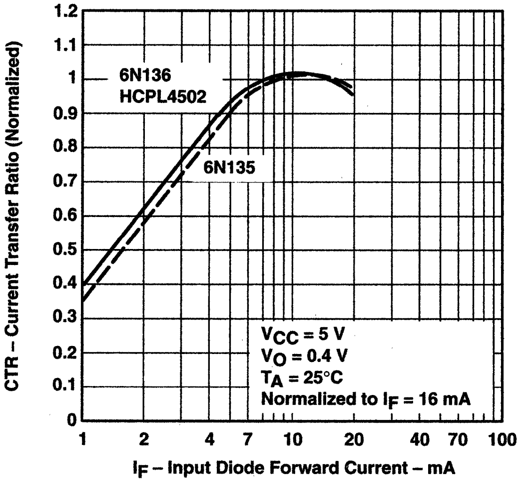


Figure 5

CURRENT TRANSFER RATIO (NORMALIZED)
vs
FREE-AIR TEMPERATURE

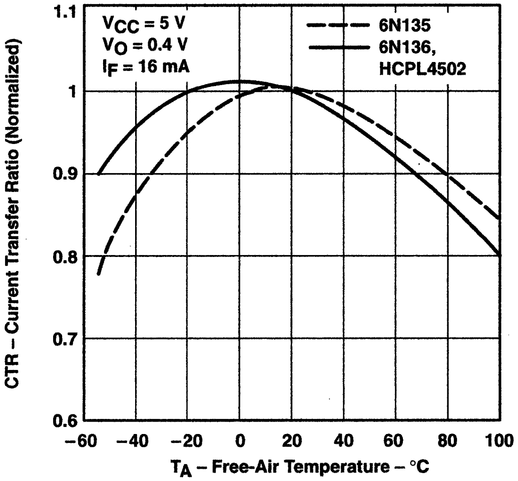


Figure 6

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

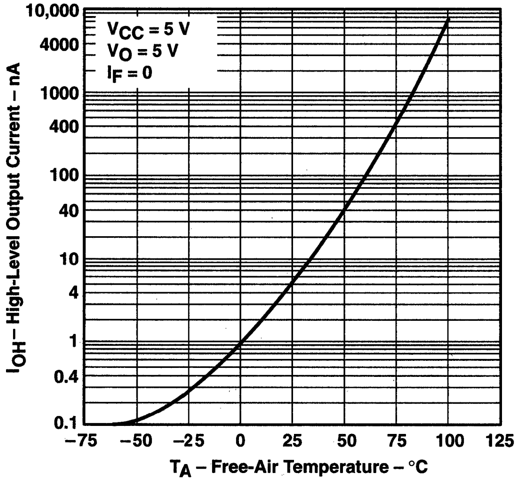


Figure 7

DIFFERENTIAL CURRENT TRANSFER RATIO vs INPUT-DIODE QUIESCENT FORWARD CURRENT

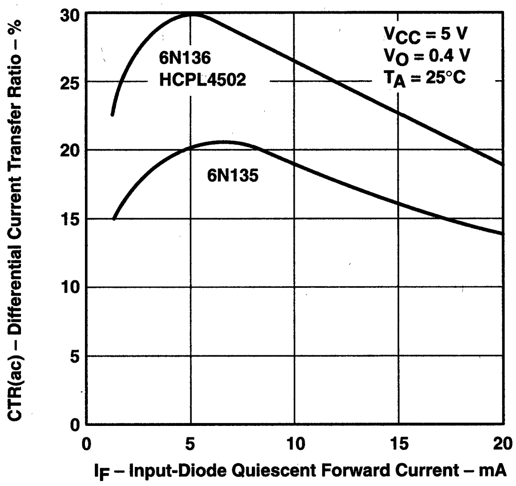


Figure 8

FREQUENCY RESPONSE (NORMALIZED) vs FREQUENCY

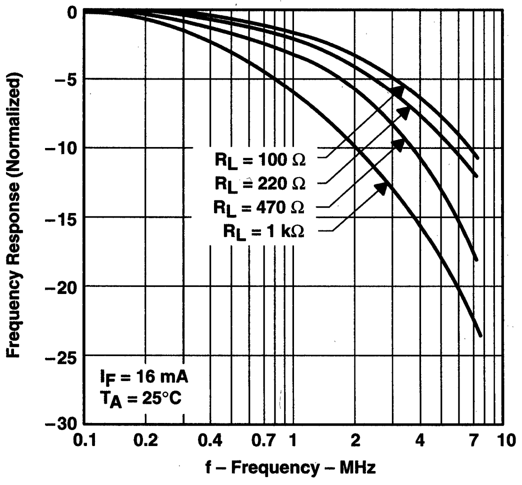


Figure 9

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

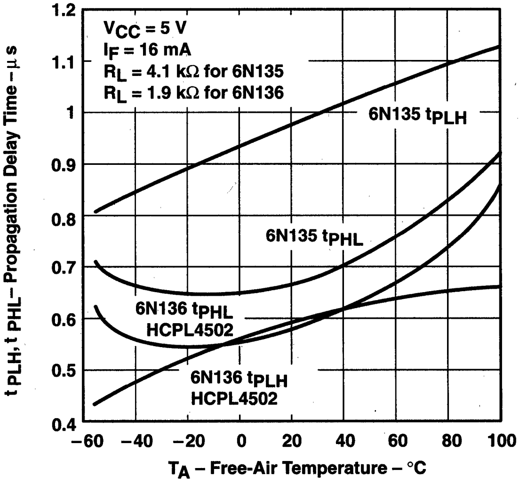
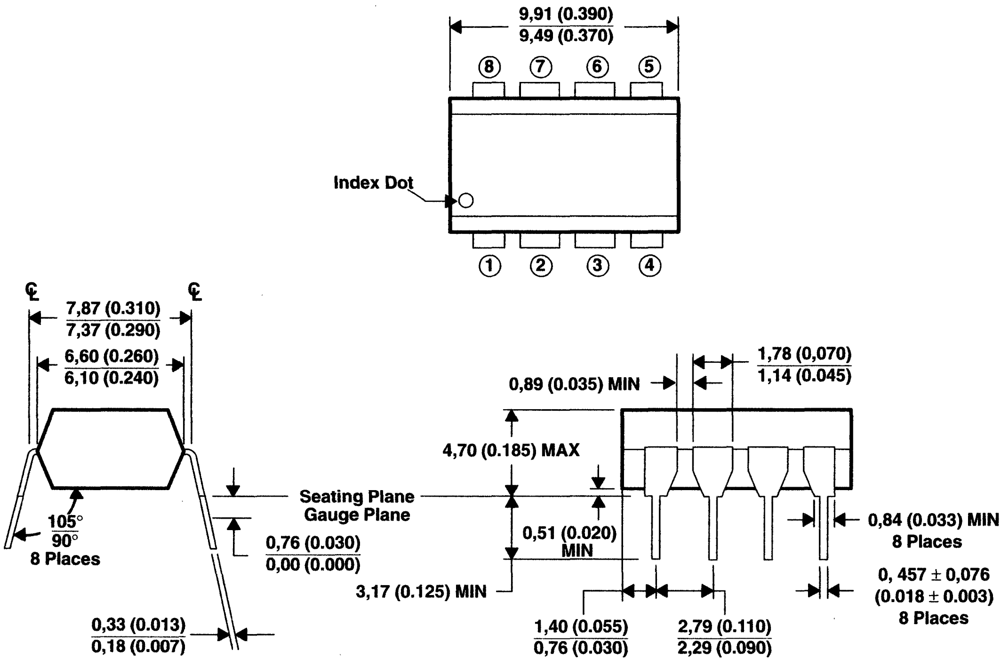


Figure 10

MECHANICAL INFORMATION



NOTES: A. JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

B. Terminal connections:
1. No internal connection (part of the light-emitting diode)
2. Anode (part of the light-emitting diode)
3. Cathode (part of the light-emitting diode)
4. No internal connection
5. GND (Emitter) (part of the light-emitting diode)
6. Output (part of the detector)
7. Base: 6N135, 6N136 (part of the detector)
Open: HCPL4502 (part of the detector)
8. V_{CC} (part of the detector)

C. All linear dimensions are given in millimeters and parenthetically given in inches.

Figure 11. Mechanical Information

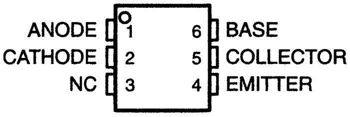
MCT2, MCT2E
OPTOCOUPLERS

SOES023 – MARCH 1983 – REVISED OCTOBER 1995

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor**
- **High Direct-Current Transfer Ratio**
- **Base Lead Provided for Conventional Transistor Biasing**
- **High-Voltage Electrical Isolation . . . 1.5-kV, or 3.55-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 5 µs, t_f = 5 µs Typical**
- **Designed to be Interchangeable with General Instruments MCT2 and MCT2E**

MCT2 OR MCT2E . . . PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input-to-output voltage: MCT2	± 1.5 kV
MCT2E	± 3.55 kV
Collector-base voltage	70 V
Collector-emitter voltage (see Note 1)	30 V
Emitter-collector voltage	7 V
Emitter-base voltage	7 V
Input-diode reverse voltage	3 V
Input-diode continuous forward current	60 mA
Input-diode peak forward current ($t_w \leq$ 1 ns, PRF $\leq$ 300 Hz)	3 A
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	200 mW
Phototransistor (see Note 2)	200 mW
Total, infrared-emitting diode plus phototransistor (see Note 3)	250 mW
Operating free-air temperature range, T_A	−55°C to 100°C
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100 °C free-air temperature at the rate of 2.67 mW/°C.
3. Derate linearly to 100 °C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

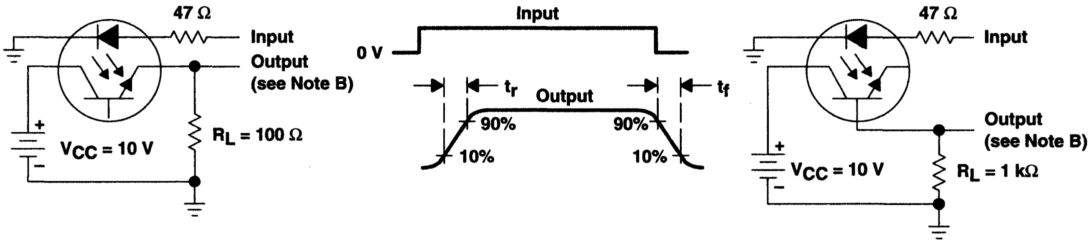
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA, I_E = 0, I_F = 0		70			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C =1 mA, I_B = 0, I_F = 0		30			V
$V_{(BRECO)}$	Emitter-collector breakdown voltage		I_E = 100 μA, I_B = 0, I_F = 0		7			V
I_R	Input diode static reverse current		V_R = 3 V				10	μA
$I_{C(on)}$	On-state collector current	Phototransistor operation	V_{CE} = 10 V, I_B = 0, I_F = 10 mA		2	5		mA
		Photodiode operation	V_{CB} = 10 V, I_E = 0, I_F = 10 mA			20		μA
$I_{C(off)}$	Off-state collector current	Phototransistor operation	V_{CE} = 10 V, I_B = 0, I_F = 0			1	50	nA
		Photodiode operation	V_{CB} = 10 V, I_E = 0, I_F = 0			0.1	20	nA
H_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V, I_C = 100 μA, I_F = 0	MCT2		250		
				MCT2E	100	300		
V_F	Input diode static forward voltage		I_F = 20 mA			1.25	1.5	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 2 mA, I_B = 0, I_F = 16 mA			0.25	4	V
r_{IO}	Input-to-output internal resistance		$V_{in\text{-}out}$ = ±1.5 kV for MCT2, ±3.55 kV for MCT2E, See Note 4		10^{11}			Ω
C_{io}	Input-to-output capacitance		$V_{in\text{-}out}$ = 0, f = 1 MHz, See Note 4			1		pF

NOTE 4: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5		μs
t_f	Fall time						
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, $I_{C(on)}$ 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall time						

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.

B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT vs INPUT-DIODE FORWARD CURRENT

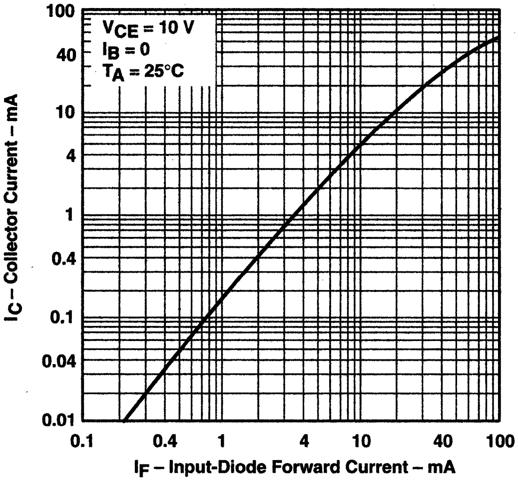
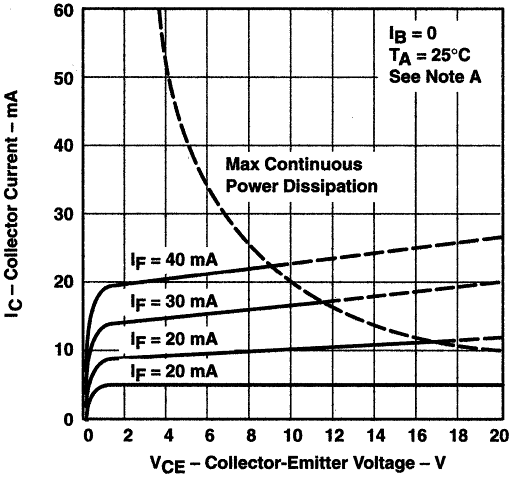


Figure 2

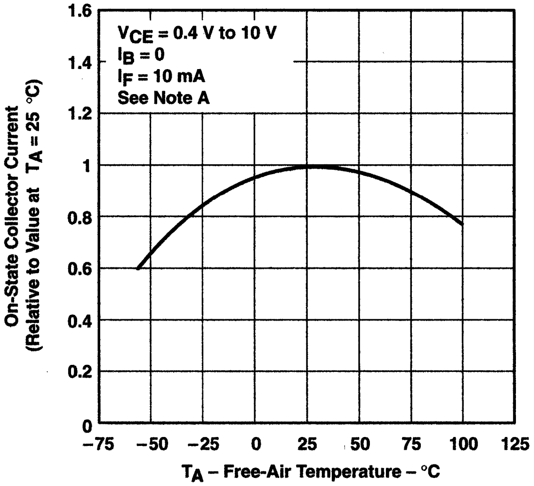
COLLECTOR CURRENT vs COLLECTOR-EMITTER VOLTAGE



NOTE A. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.

Figure 3

ON-STATE COLLECTOR CURRENT (RELATIVE TO VALUE AT 25°C) vs FREE-AIR TEMPERATURE

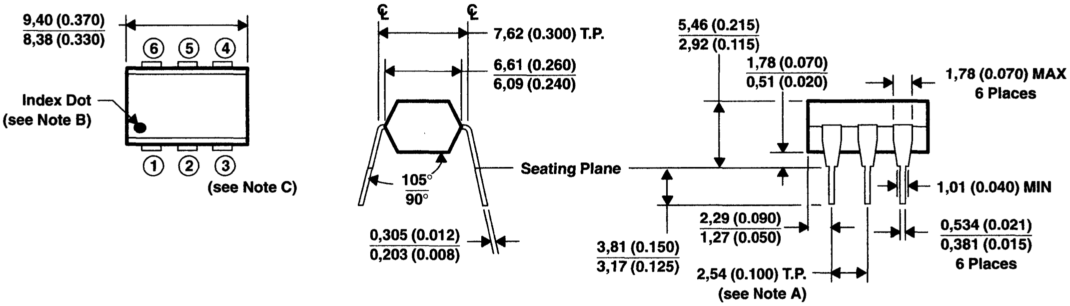


NOTE A. These parameters were measured using pulse techniques, t_W = 1 ms, duty cycle ≤ 2 %.

Figure 4

MECHANICAL INFORMATION

The package consists of a gallium-arsenide infrared-emitting diode and an npn silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
- A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
- B. Pin 1 identified by index dot.
- C. Terminal connections:
  - 1. Anode (part of the infrared-emitting diode)
  - 2. Cathode (part of the infrared-emitting diode)
  - 3. No internal connection
  - 4. Emitter (part of the phototransistor)
  - 5. Collector (part of the phototransistor)
  - 6. Base (part of the phototransistor)
- D. The dimensions given fall within JEDEC MO-001 AM dimensions.
- E. All linear dimensions are given in millimeters and parenthetically given in inches.

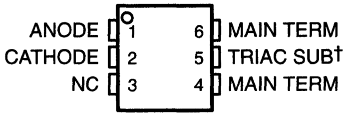
Figure 5. Mechanical Information

MOC3009 THRU MOC3012
OPTOCOUPLERS/OPTOISOLATORS

SOES024 – AUGUST 1985 – REVISED OCTOBER 1995

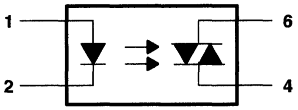
- **250 V Phototriac Driver Output**
- **Gallium-Arsenide-Diode Infrared Source and Optically Coupled Silicon Traic Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 7500 V Peak**
- **Output Driver Designed for 115 V ac**
- **Standard 6-Terminal Plastic DIP**
- **Directly Interchangeable with Motorola MOC3009, MOC3010, MOC3011, and MOC3012**
- **Direct Replacements for:**
  TRW Optron OPI3009, OPI3010, OPI3011, and OPI3012;
  General Instrument MCP3009, MCP3010, MCP3011;
  General Electric GE3009, GE3010, GE3011, and GE3012

MOC30209– MOC3012 . . . PACKAGE
(TOP VIEW)



† Do not connect this terminal
NC – No internal connection

logic diagram



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1)	7.5 kV
Input diode reverse voltage	3 V
Input diode forward current, continuous	50 mA
Output repetitive peak off-state voltage	250 V
Output on-state current, total rms value (50-60 Hz, full sine wave): $T_A = 25°C$	100 mA
$T_A = 70°C$	50 mA
Output driver nonrepetitive peak on-state current (t_w = 10 ms, duty cycle = 10%, see Figure 7)	1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototriac (see Note 3)	300 mW
Total device (see Note 4)	330 mW
Operating junction temperature range, T_J	−40°C to 100°C
Storage temperature range, T_{stg}	−40°C to 150°C
Lead temperature 1,6 (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

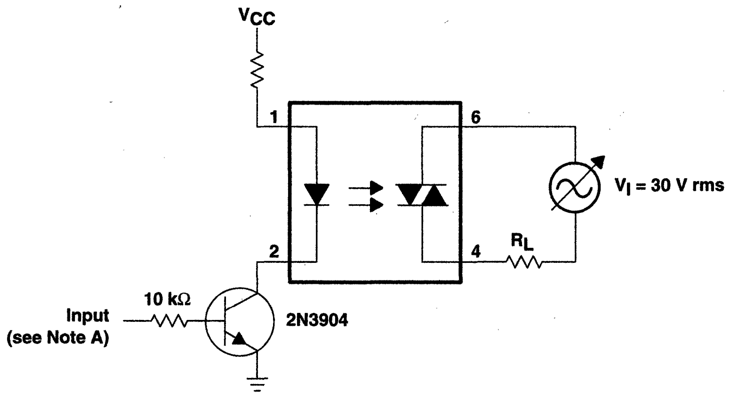
TEXAS
INSTRUMENTS

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		$V_R = 3$ V		0.05	100	µA
V_F	Static forward voltage		$I_F = 10$ mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		$V_{DRM} = 250$ V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		12		V/µs
dv/dt(c)	Critical rate of rise of commutating voltage		$I_O = 15$ mA, See Figure 1		0.15		V/µs
I_{FT}	Input trigger current, either direction	MOC3009	Output supply voltage = 3 V		15	30	mA
		MOC3010			8	15	
		MOC3011			5	10	
		MOC3012				5	
V_{TM}	Peak on-state voltage, either direction		$I_{TM} = 100$ mA		1.8	3	V
I_H	Holding current, either direction				100		µA

NOTE 5: Test voltage must be applied within dv/dt rating.

PARAMETER MEASUREMENT INFORMATION



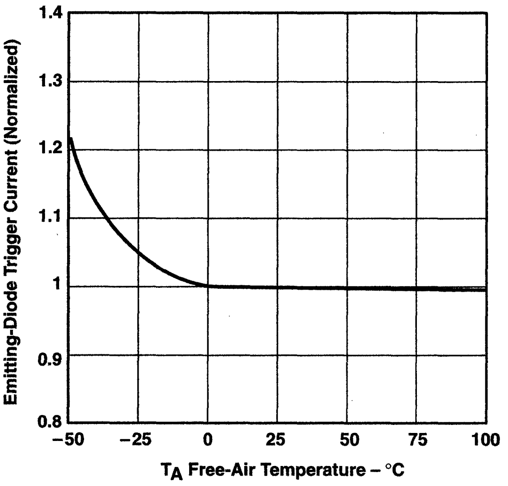
NOTE A. The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 V. The frequency of V_{in} is increased until the phototriac just turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2\pi f V_{in}}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-V pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

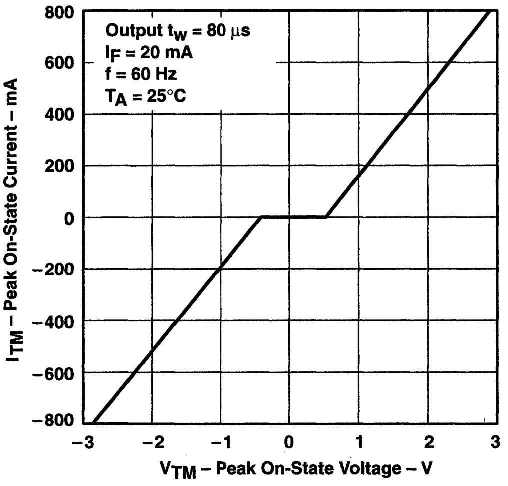
Figure 1. Critical Rate of Rise Test Circuit

TYPICAL CHARACTERISTICS



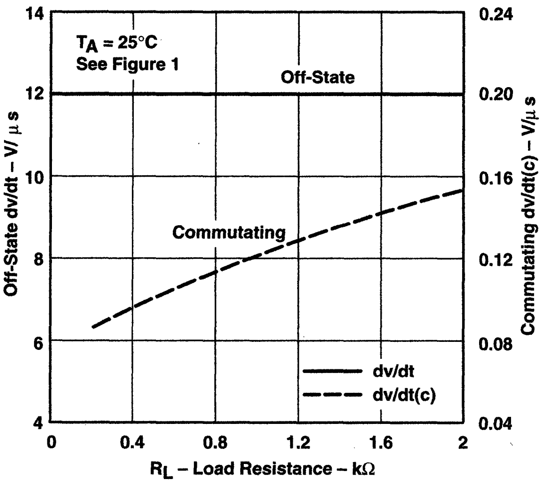
EMITTING-DIODE TRIGGER CURRENT (NORMALIZED)
vs
FREE-AIR TEMPERATURE

Figure 2



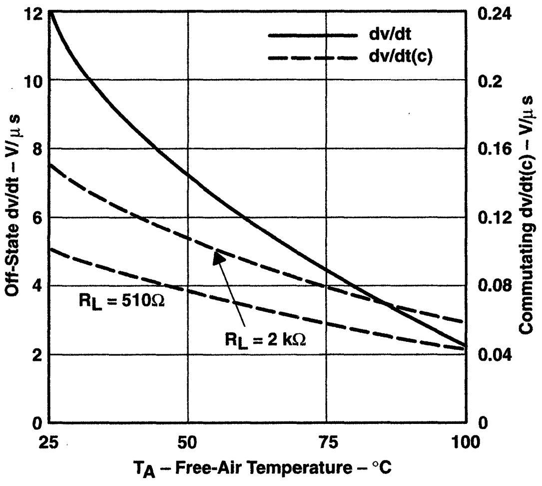
ON-STATE CHARACTERISTICS

Figure 3



CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
OFF-STATE dv/dt AND COMMUTATING dv/dt(c)
vs
LOAD RESISTANCE

Figure 4



CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
OFF-STATE dv/dt AND COMMUTATING dv/dt(c)
vs
FREE-AIR TEMPERATURE

Figure 5

TYPICAL CHARACTERISTICS

RMS APPLIED VOLTAGE (FOR dv/dt(c) = 0.15 V/μs) vs FREQUENCY

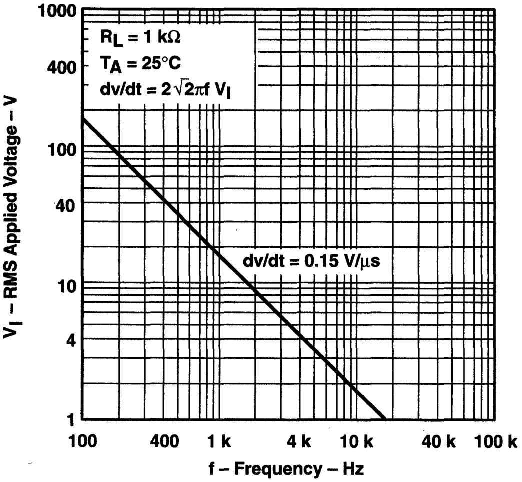


Figure 6

NONREPETITIVE PEAK ON-STATE CURRENT vs PULSE DURATION

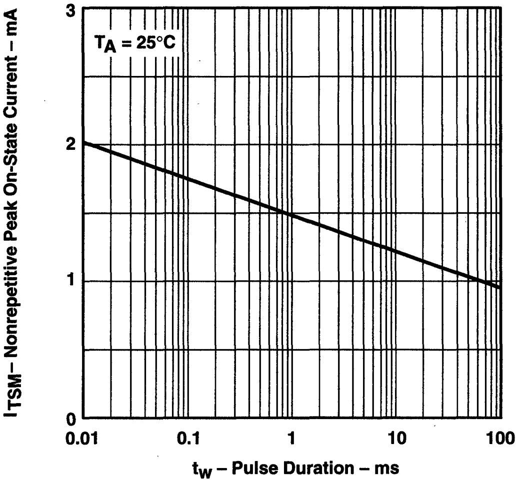


Figure 7

APPLICATIONS INFORMATION

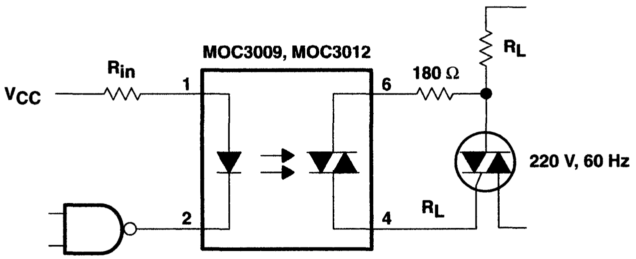
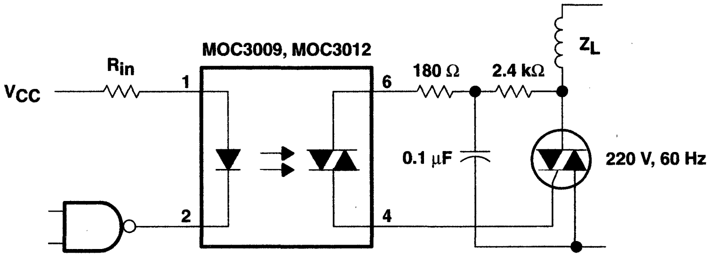
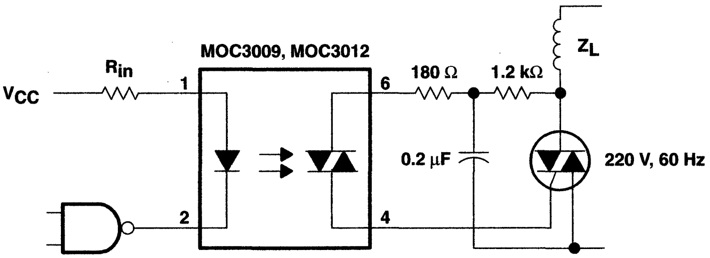


Figure 8. Resistive Load



$I_{GT} \leq 15$ mA

Figure 9. Inductive Load With Sensitive-Gate Triac

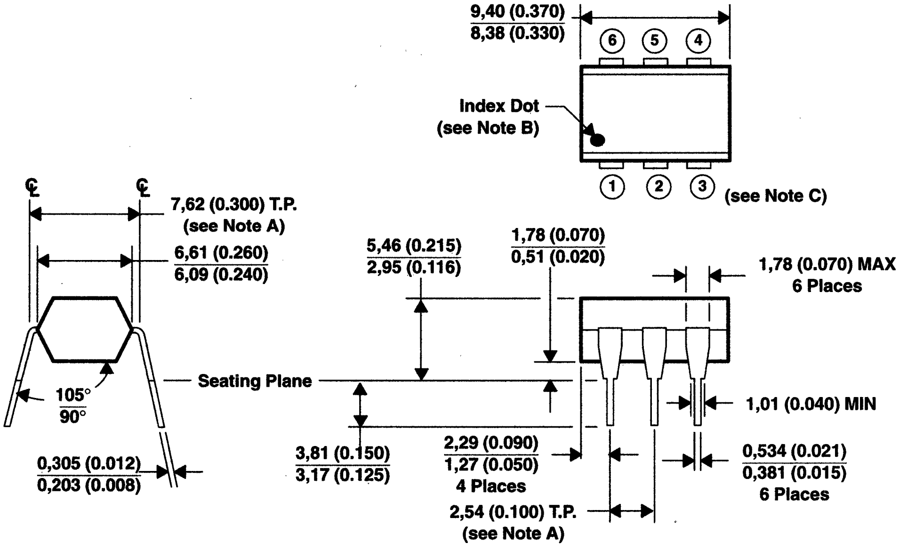


15 mA < I_{GT} < 50 mA

Figure 10. Inductive Load With Nonsensitive-Gate Triac

MECHANICAL INFORMATION

Each device consists of a gallium-arsenide infrared-emitting diode optically coupled to a silicon phototriac mounted on a 6-terminal lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable with operated in high-humidity conditions.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode (part of infrared-emitting diode)
2. Cathode (part of infrared-emitting diode)
3. No internal connection
4. Main terminal (part of phototriac)
5. Triac Substrate (DO NOT connect) (part of phototriac)
6. Main terminal (part of phototriac)
D. The dimensions given fall within JEDEC MO-001 AM dimensions.
E. All linear dimensions are given in millimeters and parenthetically given in inches.

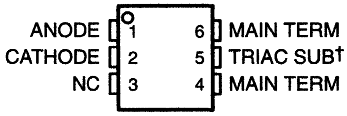
Figure 11. Mechanical Information

MOC3020 THRU MOC3023
OPTOCOUPLERS/OPTOISOLATORS

SOES025 – OCTOBER 1986 – REVISED OCTOBER 1995

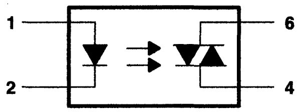
- **250 V Phototriac Driver Output**
- **Gallium-Arsenide-Diode Infrared Source and Optically-Coupled Silicon Traic Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 7500 V Peak**
- **Output Driver Designed for 220 V ac**
- **Standard 6-Terminal Plastic DIP**
- **Directly Interchangeable with Motorola MOC3020, MOC3021, MOC3022, and MOC3023**
- **Direct Replacements for:**
  - **TRW Optron OPI3020, OPI3021, OPI3022, and OPI3023;**
  - **General Instrument MCP3020, MCP3021, and MCP3022;**
  - **General Electric GE3020, GE3021, GE3022, and GE3023**

MOC3020 – MOC3023 . . . PACKAGE
(TOP VIEW)



† Do not connect this terminal
NC – No internal connection

logic diagram



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1)	7.5 kV
Input diode reverse voltage	3 V
Input diode forward current, continuous	50 mA
Output repetitive peak off-state voltage	400 V
Output on-state current, total rms value (50-60 Hz, full sine wave): $T_A = 25°C$	100 mA
$T_A = 70°C$	50 mA
Output driver nonrepetitive peak on-state current (t_w = 10 ms, duty cycle = 10%, see Figure 7)	1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototriac (see Note 3)	300 mW
Total device (see Note 4)	330 mW
Operating junction temperature range, T_J	−40°C to 100°C
Storage temperature range, T_{stg}	−40°C to 150°C
Lead temperature 1,6 (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

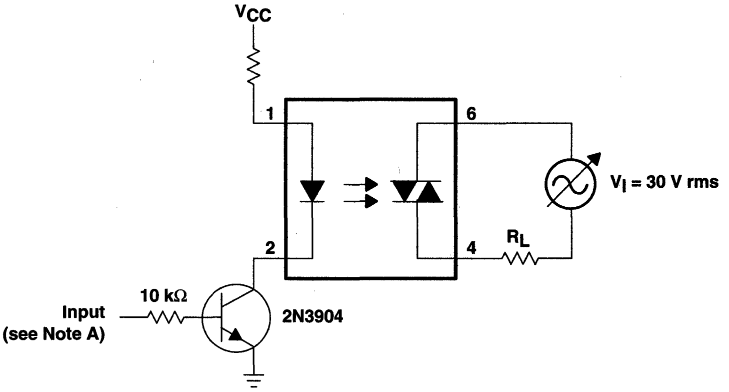
TEXAS INSTRUMENTS

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		$V_R = 3$ V		0.05	100	µA
V_F	Static forward voltage		$I_F = 10$ mA		1.2	1.5	V
$I_{(DRM)}$	Repetitive off-state current, either direction		$V_{(DRM)} = 400$ V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		100		V/µs
dv/dt(c)	Critical rate of rise of commutating voltage		$I_O = 15$ mA, See Figure 1		0.15		V/µs
I_{FT}	Input trigger current, either direction	MOC3020	Output supply voltage = 3 V		15	30	mA
		MOC3021			8	15	
		MOC3022			5	10	
		MOC3023			3	5	
V_{TM}	Peak on-state voltage, either direction		$I_{TM} = 100$ mA		1.4	3	V
I_H	Holding current, either direction				100		µA

NOTE 5: Test voltage must be applied at a rate no higher than 12 V/µs.

PARAMETER MEASUREMENT INFORMATION



NOTE A. The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 V. The frequency of V_{in} is increased until the phototriac turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2\pi f V_{in}}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-V pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

Figure 1. Critical Rate of Rise Test Circuit

TYPICAL CHARACTERISTICS

EMITTING-DIODE TRIGGER CURRENT (NORMALIZED)
vs
FREE-AIR TEMPERATURE

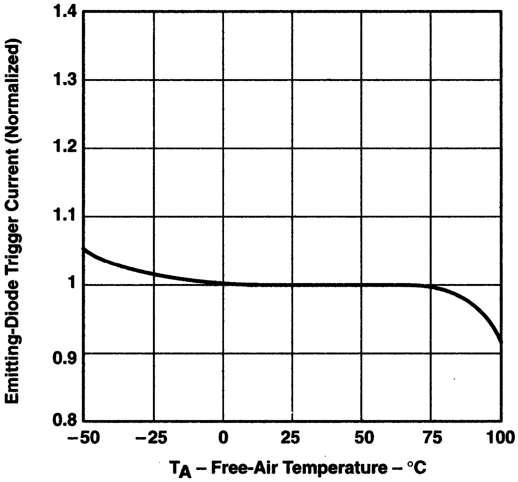


Figure 2

ON-STATE CHARACTERISTICS

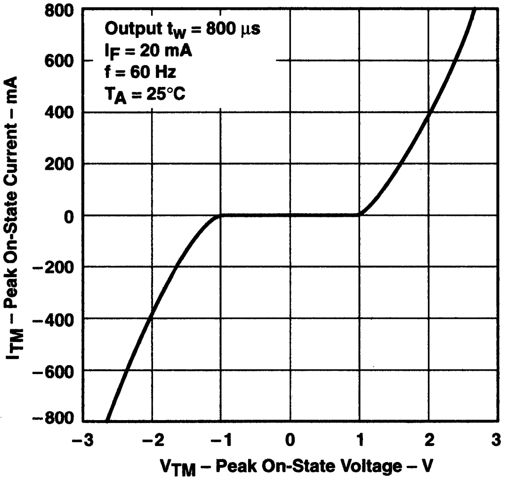


Figure 3

NONREPETITIVE PEAK ON-STATE CURRENT
vs
PULSE DURATION

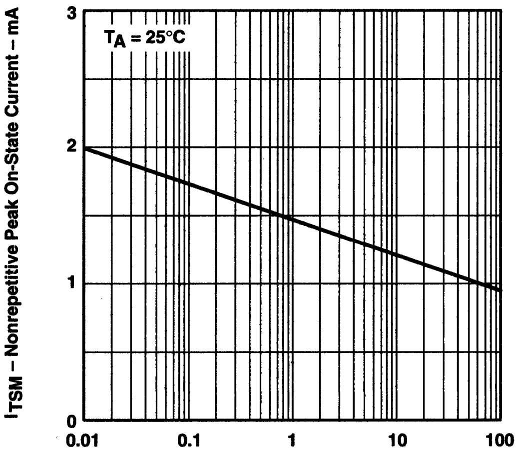


Figure 4

APPLICATIONS INFORMATION

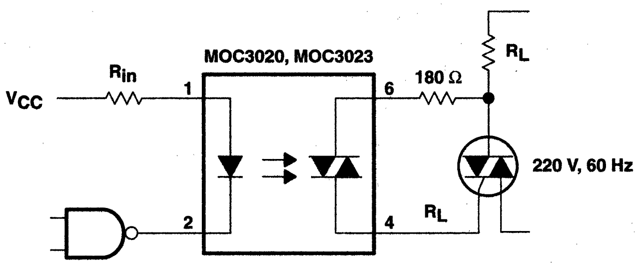
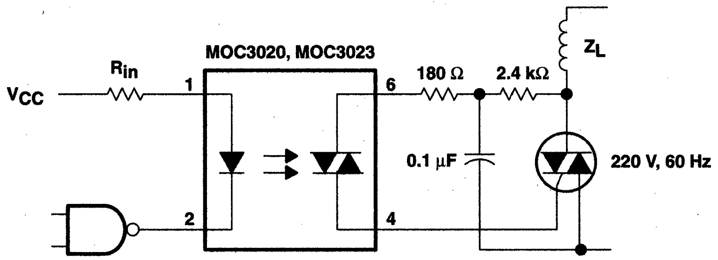
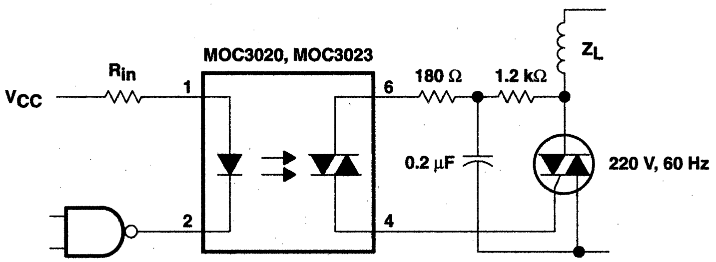


Figure 5. Resistive Load



$I_{GT} \leq 15$ mA

Figure 6. Inductive Load With Sensitive-Gate Triac

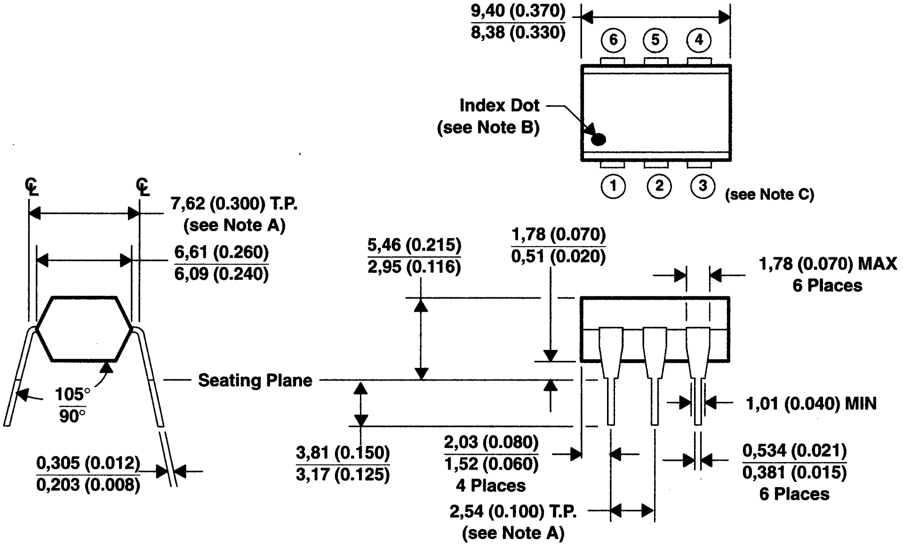


15 mA < I_{GT} < 50 mA

Figure 7. Inductive Load With Nonsensitive-Gate Triac

MECHANICAL INFORMATION

Each device consists of a gallium-arsenide infrared-emitting diode optically coupled to a silicon phototriac mounted on a 6-terminal lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.



NOTES:
- A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
- B. Pin 1 identified by index dot.
- C. Terminal connections:
  1. Anode (part of the infrared-emitting diode)
  2. Cathode (part of the infrared-emitting diode)
  3. No internal connection
  4. Main terminal (part of the phototransistor)
  5. Triac Substrate (DO NOT connect) (part of the phototransistor)
  6. Main terminal (part of the phototransistor)
- D. The dimensions given fall within JEDEC MO-001 AM dimensions.
- E. All linear dimensions are given in millimeters and parenthetically given in inches.

Figure 8. Mechanical Information

TIL191, TIL192, TIL193, TIL191A, TIL192A, TIL193A
TIL191B, TIL192B, TIL193B
OPTOCOUPLERS

SOES026 – APRIL 1989 – REVISED OCTOBER 1995

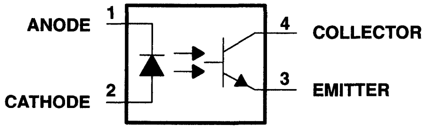
- **Gallium-Arsenide-Diode Infrared Source**
- **Source Is Optically Coupled to Silicon npn Phototransistor**
- **Choice of One, Two, or Four Channels**
- **Choice of Three Current-Transfer Ratios**
- **High-Voltage Electrical Isolation 3.535 kV Peak (2.5 kV rms)**
- **Plastic Dual-In-Line Packages**
- **UL Listed — File #E65085**

description

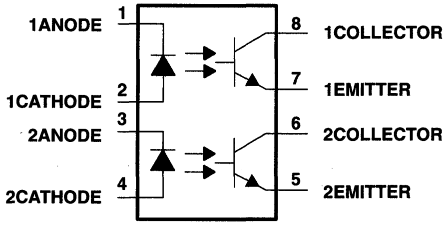
These optocouplers consist of a gallium-arsenide light-emitting diode and a silicon npn phototransistor per channel. The TIL191 has a channel in a 4-terminal package, the TIL192 has two channels in an 8-terminal package, and the TIL193 has four channels in a 16-terminal package. The standard devices, TIL191, TIL192, and TIL193, are tested for a current-transfer ratio of 20% minimum. Devices selected for a current-transfer ratio of 50% and 100% minimum are designated with the suffix A and B respectively.

schematic diagrams

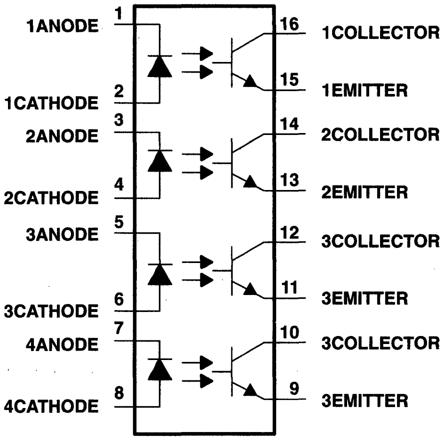
TIL191



TIL192



TIL193



absolute maximum ratings at 25°C free-air (unless otherwise noted)†

Input-to-output voltage (see Note 1)	±3.535 kV peak or dc (±2.5 kV rms)
Collector-emitter voltage (see Note 2)	35 V
Emitter-collector voltage	7 V
Input diode reverse voltage	5 V
Input diode continuous forward current at (or below) 25°C free-air temperature (see Note 3)	50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature:	
Phototransistor (see Note 4)	150 mW
Input diode plus phototransistor per channel (see Note 5)	200 mW
Storage temperature range, T_{stg}	−55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. This rating applies for sine-wave operation at 50 Hz or 60 Hz. This capability is verified by testing in accordance with UL requirements.
2. This value applies when the base-emitter diode is open circuited.
3. Derate linearly to 100°C free-air temperature at the rate of 0.67 mA/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 2.67 mW/°C.

electrical characteristics 25°C free-air temperature range (unless otherwise noted)

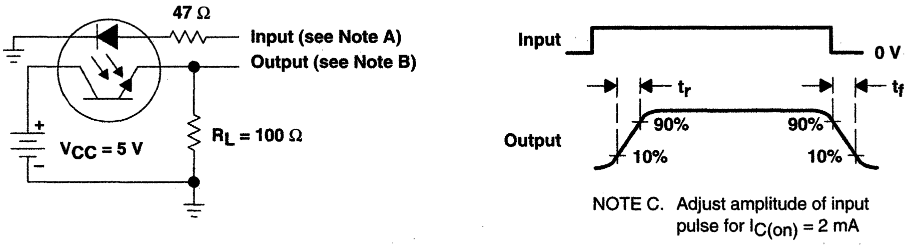
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		$I_C = 0.5$ mA,	$I_F = 0$	35			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		$I_C = 100$ µA,	$I_F = 0$	7			V
I_R	Input diode static reverse current		$V_R = 5$ V				10	µA
$I_{C(off))}$	Off-state collector current		$V_{CE} = 24$ V,	$I_F = 0$			100	nA
CTR	Current transfer ratio	TIL191, TIL192, TIL193	$I_F = 5$ mA	$V_{CE} = 5$ V	20%			
		TIL191A, TIL192A, TIL193A			50%			
		TIL191B, TIL192B, TIL193B			100%			
V_F	Input diode static forward voltage		$I_F = 20$ mA				1.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		$I_F = 5$ mA	$I_C = 1$ mA			0.4	V
C_{io}	Input-to-output capacitance		$V_{in–out} = 0$ mA	f = 1 MHz,		1		pF
r_{io}	Input-to-output internal resistance		$V_{in–out} = \pm 1$ mA	See Note 6		10^{11}		Ω

NOTE 6: These parameters are measured between all input diode leads shorted together and all phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		TYP	UNIT
t_r	Rise time	$V_{CC} = 5$ V, $R_L = 100\ \Omega$,	$I_{C(on)} = 2$ mA, See Figure 1	6	µs
t_f	Fall time			6	

PARAMETER MEASUREMENT INFORMATION



NOTE C. Adjust amplitude of input pulse for $I_{C(on)} = 2$ mA

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $Z_{OUT} = 50\ \Omega$, $t_r \le 15$ ns, t_w 100 µs.
B. The output waveform is monitored on a oscilloscope with the following characteristic: $t_r \le 12$ ns, $R_{in} \ge 1$M µs, $C_{in} \le 20$ pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

FORWARD CURRENT vs FORWARD VOLTAGE

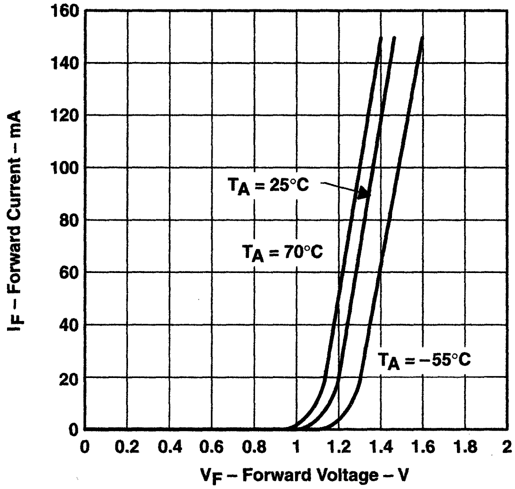


Figure 2

TIL191, TIL192, TIL193 COLLECTOR CURRENT vs COLLECTOR-EMITTER VOLTAGE

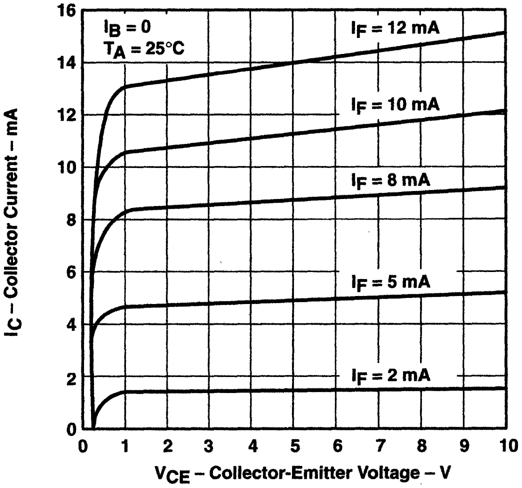


Figure 3

ON-STATE COLLECTOR CURRENT (NORMALIZED) vs INPUT DIODE FORWARD CURRENT

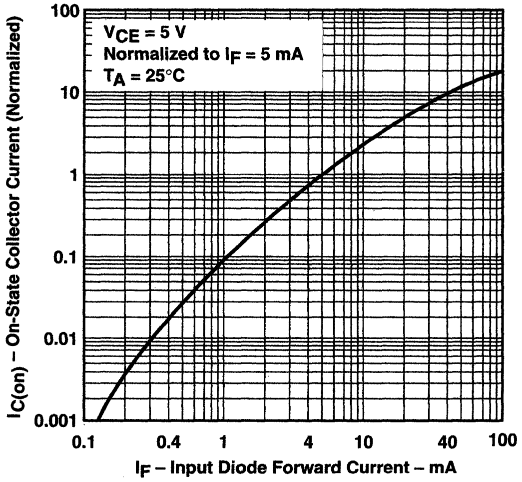


Figure 4

ON-STATE COLLECTOR CURRENT (RELATIVE TO VALUE AT 25°C) vs FREE-AIR TEMPERATURE

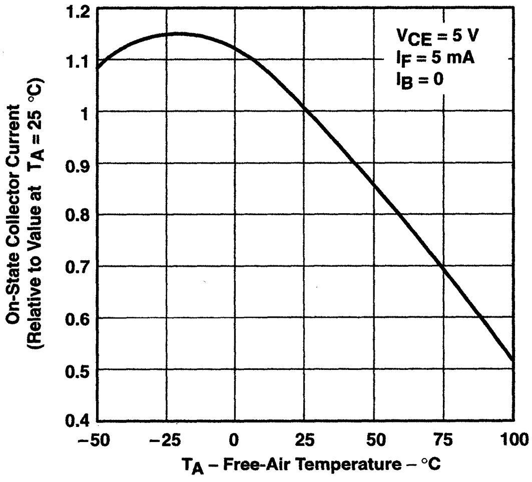


Figure 5

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

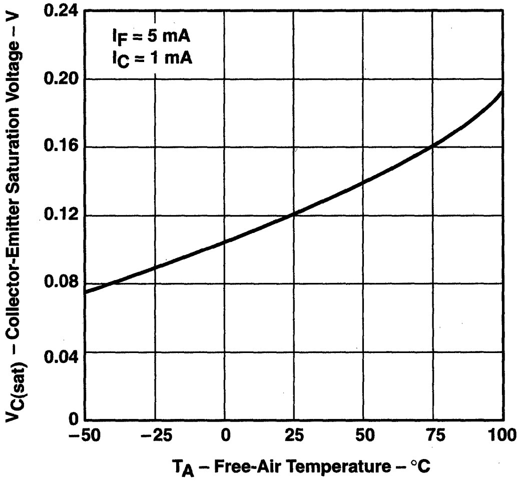


Figure 6

APPLICATION INFORMATION

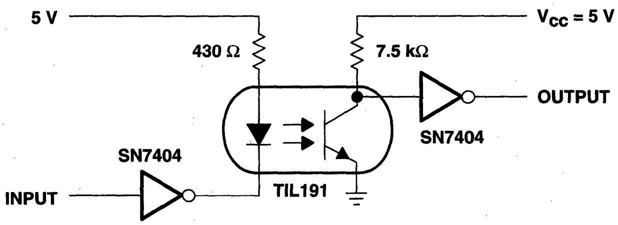
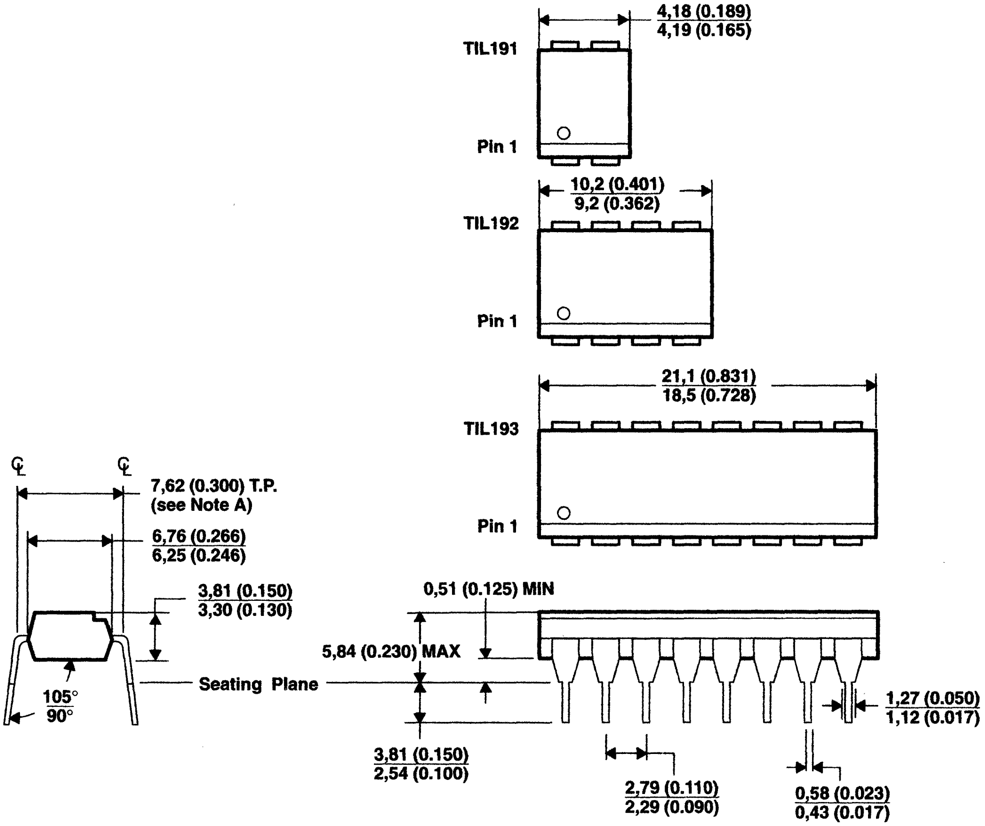


Figure 7

MECHANICAL INFORMATION



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. All linear dimensions are given in millimeters and parenthetically given in inches.

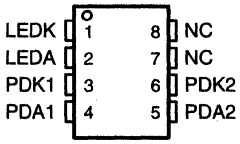
Figure 8. Mechanical Information

TIL300, TIL300A
PRECISION LINEAR OPTOCOUPLER

SOES019 – OCTOBER 1995

- **ac or dc Signal Coupling**
- **Wide Bandwidth . . . >200 kHz**
- **High Transfer-Gain Stability . . . ±0.05%/°C**
- **3500 V Peak Isolation**
- **UL Approval Pending**
- **Applications**
  - **Power-Supply Feedback**
  - **Medical-Sensor Isolation**
  - **Opto Direct-Access Arrangement (DAA)**
  - **Isolated Process-Control Transducers**

P PACKAGE
(TOP VIEW)

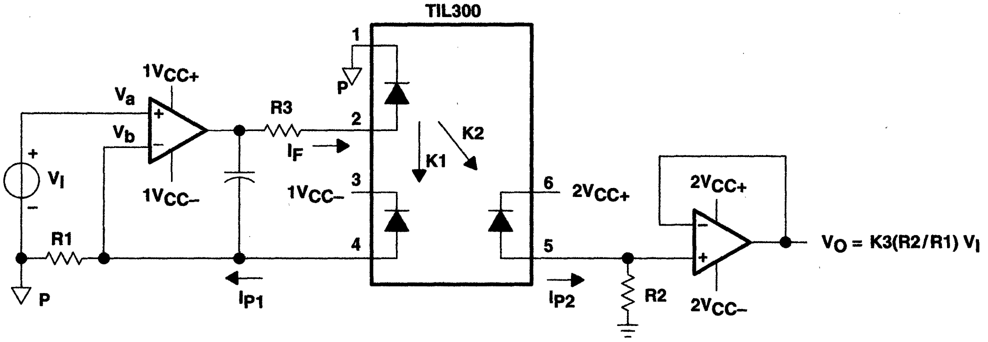


NC – No internal connection

description

The TIL300 precision linear optocoupler consists of an infrared LED irradiating an isolated feedback photodiode and an output photodiode in a bifurcated arrangement. The feedback photodiode captures a percentage of the flux of the LED and generates a control signal that can be used to regulate the LED drive current. This technique is used to compensate for the nonlinear time and temperature characteristics of the LED. The output-side photodiode produces an output signal that is linearly proportional to the servo-optical flux emitted from the LED.

A typical application circuit (shown in Figure 1) uses an operational amplifier as the input to drive the LED. The feedback photodiode sources current through R1, which is connected to the inverting input of the input operational amplifier. The photocurrent I_{P1} assumes a magnitude that satisfies the relationship $I_{P1} = V_I/R1$. The magnitude of the current is directly proportional to the LED current through the feedback transfer gain $K1 (V_I/R1 = K1 \times I_F)$. The operational amplifier supplies LED current to produce sufficient photocurrent to keep the node voltage V_b equal to node voltage V_a.



NOTES: A. K1 is servo current gain, the ratio of the feedback photodiode current (I_{P1}) to the input LED current (I_F), i.e. $k1 = I_{P1}/I_F$.
B. K2 is forward gain, the ratio of the output photodiode current (I_{P2}) to the input LED current (I_F), i.e. $K2 = I_{P2}/I_F$.
C. K3 is transfer gain, the ratio of the forward gain to the servo gain, i.e. $K3 = K2/K1$.

Figure 1. Typical Application Circuit

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LEDK	1		LED cathode
LEDA	2		LED anode
PDK1	3		Photodiode 1 cathode
PDA1	4		Photodiode 1 anode
PDA2	5		Photodiode 2 anode
PDK2	6		Photodiode 2 cathode
NC	7		No internal connection
NC	8		No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Emitter

Continuous power dissipation (see Note 1)	160 mW
Input LED forward current, I_F	60 mA
Surge current with pulse width < 10 µs	250 mA
Reverse voltage, V_R	5 V
Reverse current, I_R	10 µA

Detector

Continuous power dissipation (see Note 2)	50 mW
Reverse voltage, V_R	50 V

Coupler

Continuous power dissipation (see Note 3)	210 mW
Storage temperature, T_{stg}	–55°C to 150°C
Operating temperature, T_A	–55°C to 100°C
Input-to-output voltage	3500 Vpeak
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Derate linearly from 25°C at a rate of 2.66 mW/°C.
2. Derate linearly from 25°C at a rate of 0.66 mW/°C.
3. Derate linearly from 25°C at a rate of 3.33 mW/°C.

PRODUCT PREVIEW

electrical characteristics at T_A = 25°C

Emitter

	PARAMETER	CONDITIONS		MIN	TYP†	MAX	UNIT
V_F	Forward voltage	I_F = 10 mA			1.25	1.50	V
	V_F temperature coefficient				–2.2		mV/°C
I_R	Reverse current	V_R = 5 V				10	µA
t_r	Rise time	I_F = 10 mA,	ΔI_F = 2 mA		1		µs
t_f	Fall time	I_F = 10 mA,	ΔI_F = 2 mA		1		µs
C_j	Junction capacitance	V_F = 0,	f = 1 MHz		15		pF

Detector

	PARAMETER	CONDITIONS		MIN	TYP†	MAX	UNIT
I_{DK}†	Dark current	V_R = 15 V,	I_F = 0			25	nA
	Open circuit voltage	I_F = 10 mA			0.5		V
I_{OS}	Short circuit current limit	I_F = 10 mA			80		µA
C_j	Junction capacitance	V_F = 0,	f = 1 MHz		12		pF

Coupler

	PARAMETER		CONDITIONS		MIN	TYP†	MAX	UNIT
K1‡	Servo current gain		Detector bias voltage = –15 V	I_F = 1 mA	0.3%	0.5%	0.8%	
				I_F = 10 mA	0.5%	0.8%	1.1%	
K2§	Forward current gain			I_F = 1 mA	0.3%	0.5%	0.8%	
				I_F = 10 mA	0.5%	0.8%	1.1%	
K3¶	Transfer gain	TIL300		I_F = 1 mA	0.75	1	1.25	
				I_F = 10 mA	0.75	1	1.25	
		TIL300A		I_F = 1 mA	0.9	1	1.10	
				I_F = 10 mA	0.9	1	1.10	
	Gain temperature coefficient	K1/K2	I_F = 10 mA			–0.5		%/°C
		K3				±0.005		
ΔK3#	Transfer gain linearity		I_F = 1 to 10 mA			±0.25%		
			I_F = 1 to 10 mA,	T_A = 0 to 75°C		±0.5%		
BW	Bandwidth		I_F = 10 mA, $I_{F(MODULATION)}$	R_L = 50 Ω,		200		kHz
t_r	Rise time		I_F = 10 mA, $I_{F(MODULATION)}$	R_L = 50 Ω,		1.75		µs
t_f	Fall time		I_F = 10 mA, $I_{F(MODULATION)}$	R_L = 50 Ω,		1.75		µs
V_{iso}†	Peak Isolation voltage		I_{IO} = 10 µA,	f = 60 Hz	3500			V

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ Servo current gain (K1) is the ratio of the feedback photodiode current (I_{P1}) to the input LED current (I_F) current (I_F), i.e. K1 = I_{P1}/I_F.

§ Forward gain (K2 is the ratio of the output photodiode current (I_{P2}) to the input LED current (I_F), i.e. K2 = I_{P2}/I_F.

¶ Transfer gain (K3) is the ratio of the forward gain to the servo gain, i.e. K3 = K2/K1.

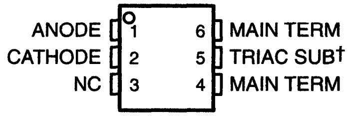
\# Transfer gain linearity (ΔK3) is the percent deviation of the transfer gain K3 as a function of LED input current (I_F) or the package temperature.

TIL3009 THRU TIL3012
OPTOCOUPLERS/OPTOISOLATORS

SOES027 – DECEMBER 1987 – REVISED OCTOBER 1995

- **250-V Phototriac Driver Output**
- **Gallium-Arsenide-Diode Infrared Source and Optically-Coupled Silicon Triac Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 3535 V peak**
- **Output Driver Designed for 115 V AC**
- **Standard 6-Pin Plastic DIP**

TIL30209– TIL3012 . . . PACKAGE
(TOP VIEW)

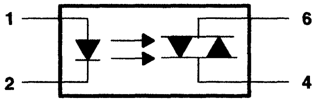


† Do not connect this terminal
NC – No internal connection

description

Each device consists of a gallium-arsenide infrared-emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case withstands soldering temperature with no deformation. Device performance characteristics remain stable when operated in high-humidity conditions.

logic diagram



absolute maximum ratings at 25°C free-air (unless otherwise noted)†

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1)	3.535 kV
Input diode reverse voltage	3 V
Input diode forward current, continuous	50 mA
Output repetitive peak off-state voltage	250 V
Output on-state current, total rms value (50-60 Hz, full sine wave):	
$T_A = 25°$	100 mA
$T_A = 70°$	50 mA
Output driver nonrepetitive peak on-state current ($t_w = 10$ ms, duty cycle = 10%, see Figure 7)	1.2 mA
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototriac (see Note 3)	300 mW
Total device (see Note 4)	330 mW
Operating junction temperature range, T_J	−40°C to 100°C
Storage temperature range, T_{stg}	−40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

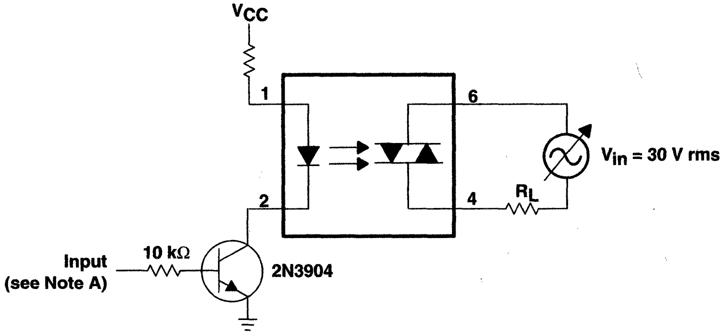
NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics 25°C free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		$V_R = 3$ V		0.05	100	μA
V_F	Static forward voltage		$I_F = 10$ mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		$V_{DRM} = 250$ V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		12		V/μs
dv/dt(c)	Critical rate of rise of communication voltage		$I_O = 15$ mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current either direction	TIL3009	Output supply voltage = 3 V		15	30	mA
		TIL3010			8	15	
		TIL3011			5	10	
		TIL3012				5	
V_{TM}	Peak on-state voltage, either direction		$I_{TM} = 100$ mA		1.8	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied within dv/dt rating.

PARAMETER MEASUREMENT INFORMATION



NOTE A. The critical rate of rise of off-state voltage, dv/dt, is measured with the input of 0 volts. The frequency of V_{in} is increased until the phototriac turns on. This frequency is then used to calculate the dv/dt according to the following formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac remains on (latches) after the input pulse has ceased. With no further input pulses., the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs can then be used to calculate the dv/dt(c) according to the formula shown above.

Figure 1. CRITICAL RATE OF RISE TEST CIRCUIT

TYPICAL CHARACTERISTICS

EMITTING DIODE TRIGGER CURRENT (NORMALIZED)
vs
FREE-AIR TEMPERATURE

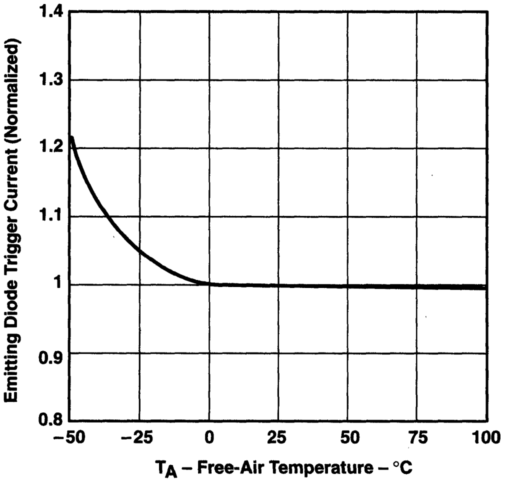


Figure 2

ON-STATE CHARACTERISTICS

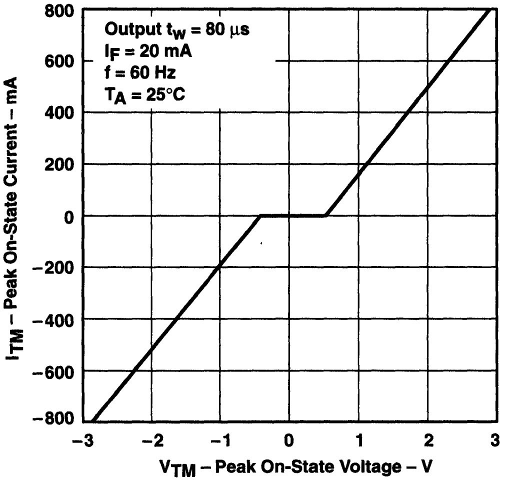


Figure 3

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
OFF-STATE dv/dt AND COMMUTATING dv/dt(c)
vs
LOAD RESISTANCE

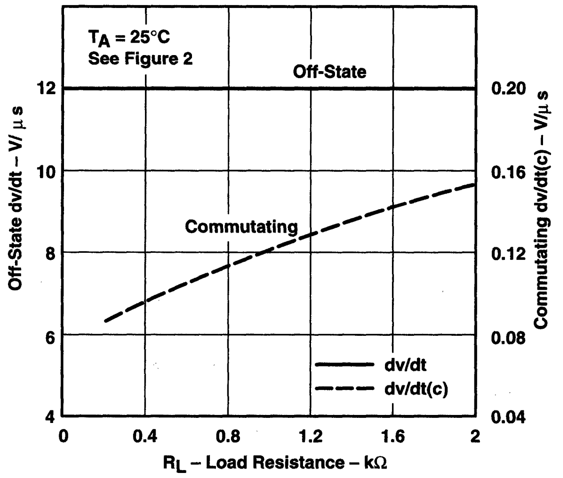


Figure 4

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
OFF-STATE dv/dt AND COMMUTATING dv/dt(c)
vs
FREE-AIR TEMPERATURE

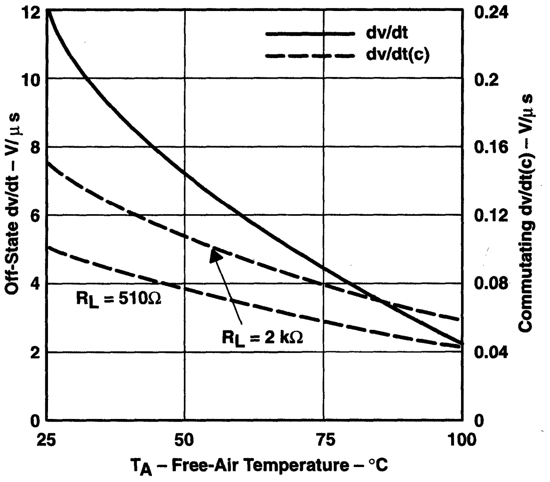


Figure 5

TYPICAL CHARACTERISTICS

RMS APPLIED VOLTAGE (FOR dv/dt(c) = 0.15 V/μs) vs FREQUENCY

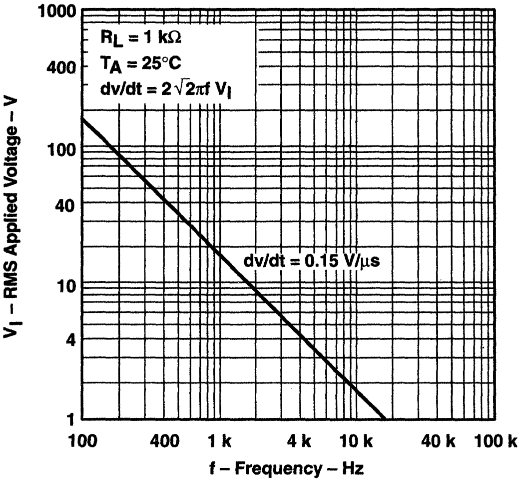


Figure 6

NONREPETITIVE PEAK ON-STATE CURRENT vs PULSE DURATION

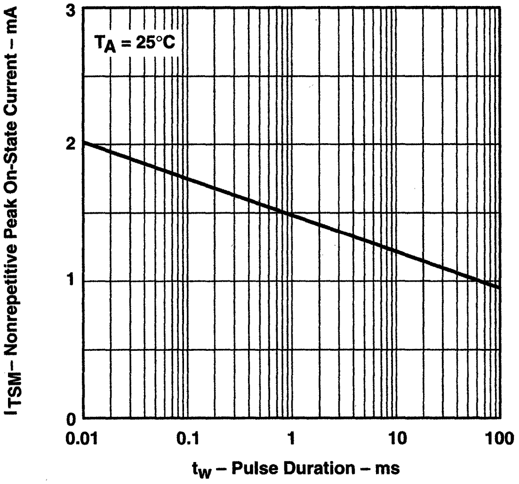


Figure 7

APPLICATION INFORMATION

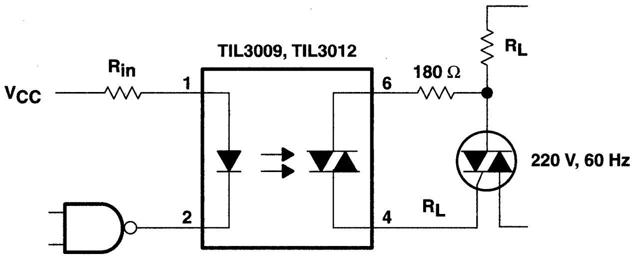


Figure 8. Resistive Load

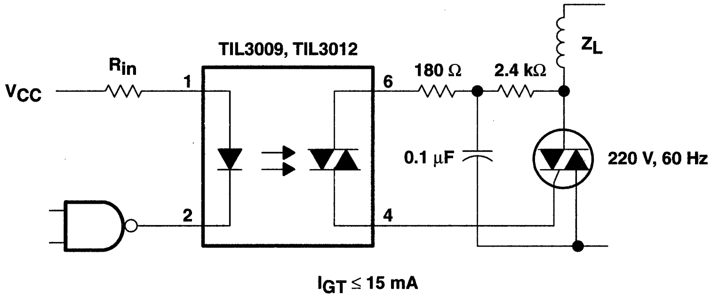


Figure 9. Inductive Load With Sensitive-Gate Traic

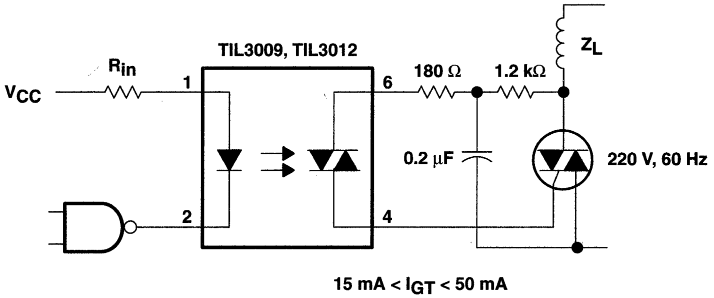
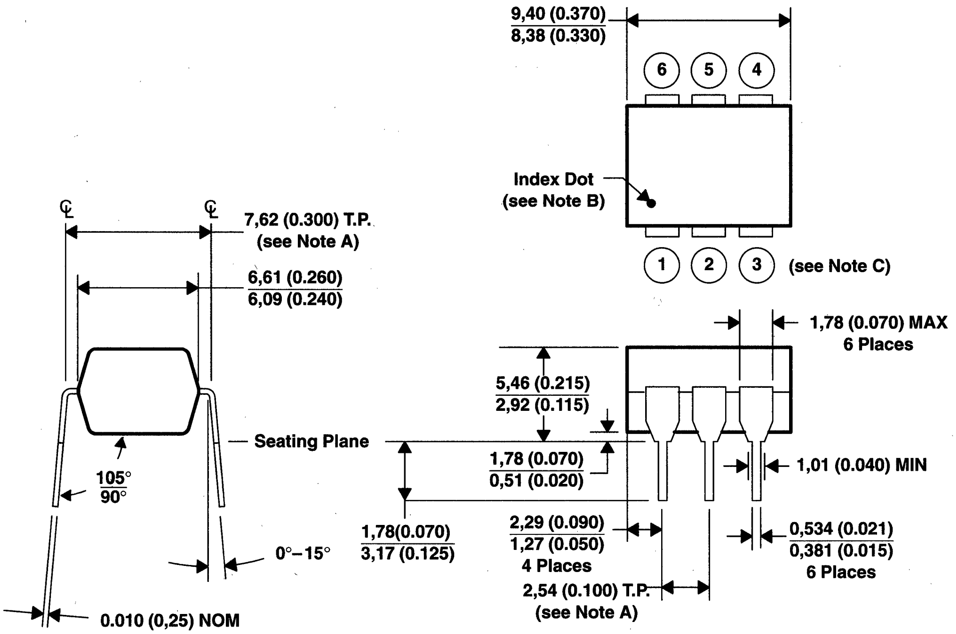


Figure 10. Inductive Load With Nonsensitive-Gate Triac

MECHANICAL INFORMATION



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

B. Pin 1 identified by index dot.

C. Terminal connections:

1. Anode (part of infrared-emitting diode)
2. Cathode (part of infrared-emitting diode)
3. No internal connection
4. Main terminal (part of phototriac)
5. Triac Substrate (DO NOT connect) (part of phototriac)
6. Main terminal (part of phototriac)

D. The dimensions given fall within JEDEC MO-001 AM dimensions.

E. All linear dimensions are given in millimeters and parenthetically given in inches.

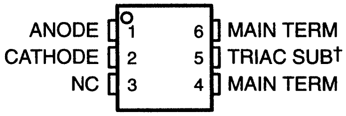
Figure 11. Mechanical Information

TIL3020 THRU TIL3023
OPTOCOUPLERS/OPTOISOLATORS

SOES028 – DECEMBER 1987 – REVISED OCTOBER 1995

- **400-V Phototriac Driver Output**
- **Gallium-Arsenide-Diode Infrared Source and Optically-Coupled Silicon Triac Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 3535 V peak**
- **Output Driver Designed for 220 V AC**
- **Standard 6-Pin Plastic DIP**

TIL3020 – TIL3023 . . . PACKAGE
(TOP VIEW)

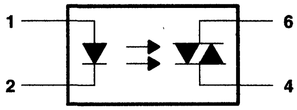


† Do not connect this terminal
NC – No internal connection

description

Each device consists of a gallium-arsenide infrared-emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case withstands soldering temperature with no deformation. Device performance characteristics remain stable when operated in high-humidity conditions.

logic diagram



absolute maximum ratings at 25°C free-air (unless otherwise noted)†

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1)	3.535 kV
Input diode reverse voltage	3 V
Input diode forward current, continuous	50 mA
Output repetitive peak off-state voltage	250 V
Output on-state current, total rms value (50-60 Hz, full sine wave):	
$T_A = 25°C$	100 mA
$T_A = 70°C$	50 mA
Output driver nonrepetitive peak on-state current (t_w = 10 ms, duty cycle = 10%, see Figure 7)	1.2 mA
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototriac (see Note 3)	300 mW
Total device (see Note 4)	330 mW
Operating junction temperature range, T_J	–40°C to 100°C
Storage temperature range, T_{stg}	–40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

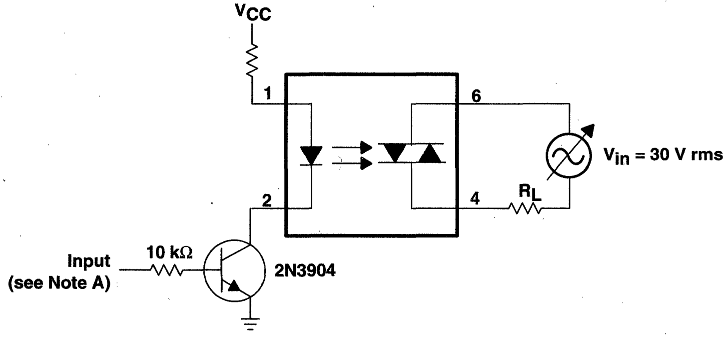
NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics 25°C free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	µA
V_F	static forward voltage		I_F = 10 mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		V_{DRM} = 250 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		100		V/µs
dv/dt(c)	Critical rate of rise of communication voltage		I_O = 15 mA, See Figure 1		0.15		V/µs
I_{FT}	Input trigger current, either direction	TIL3020	Output supply voltage = 3 V		15	30	mA
		TIL3021			8	15	
		TIL3022			5	10	
		TIL3023			3	5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.4	3	V
I_H	Holding current, either direction				100		µA

NOTE 5: Test voltage must be applied at a rate no higher than 12 V/µs.

PARAMETER MEASUREMENT INFORMATION



NOTE A. The critical rate of rise of off-state voltage, dv/dt, is measured with the input of 0 volts. The frequency of V_{in} is increased until the phototriac turns on. This frequency is then used to calculate the dv/dt according to the following formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac remains on (latches) after the input pulse has ceased. With no further input pulses., the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs can then be used to calculate the dv/dt(c) according to the formula shown above.

Figure 1. Critical Rate of Rise Test Circuit

TYPICAL CHARACTERISTICS

EMITTING DIODE TRIGGER CURRENT (NORMALIZED) vs FREE-AIR TEMPERATURE

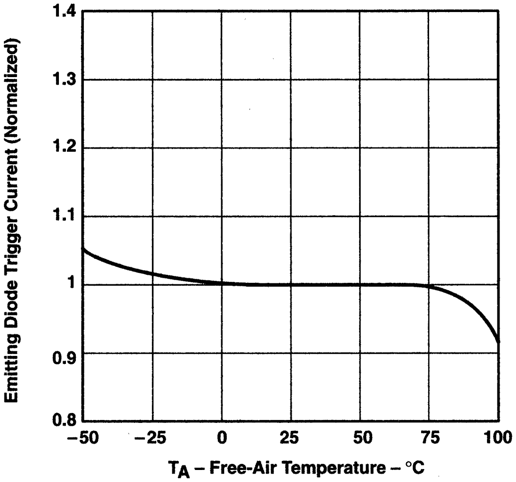


Figure 2

ON-STATE CHARACTERISTICS

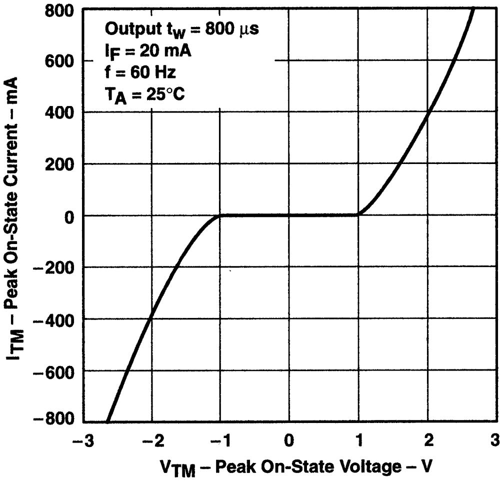


Figure 3

NONREPETITIVE PEAK ON-STATE CURRENT vs PULSE DURATION

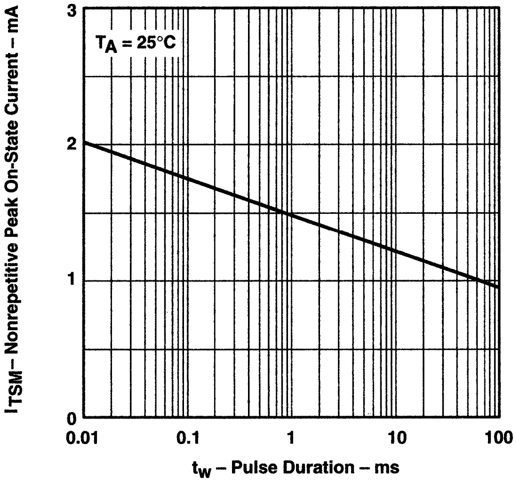


Figure 4

APPLICATION INFORMATION

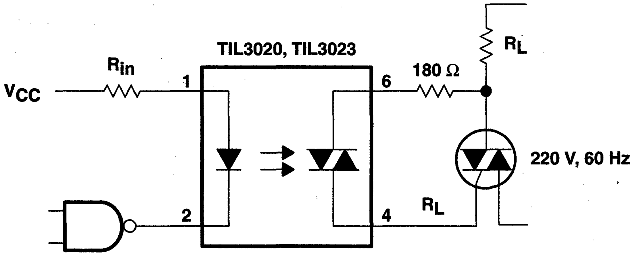
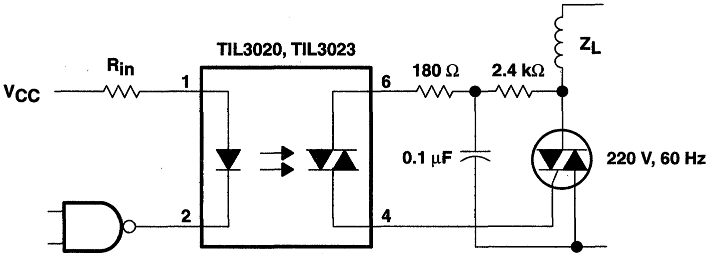
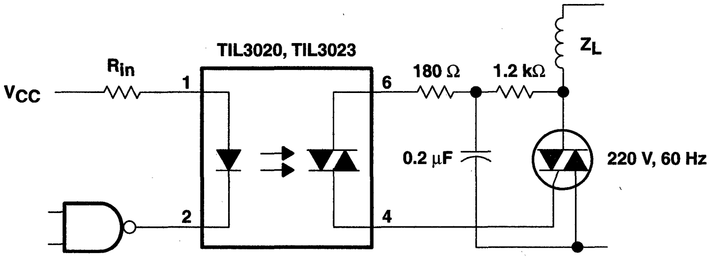


Figure 5. Resistive Load



$I_{GT} \leq 15$ mA

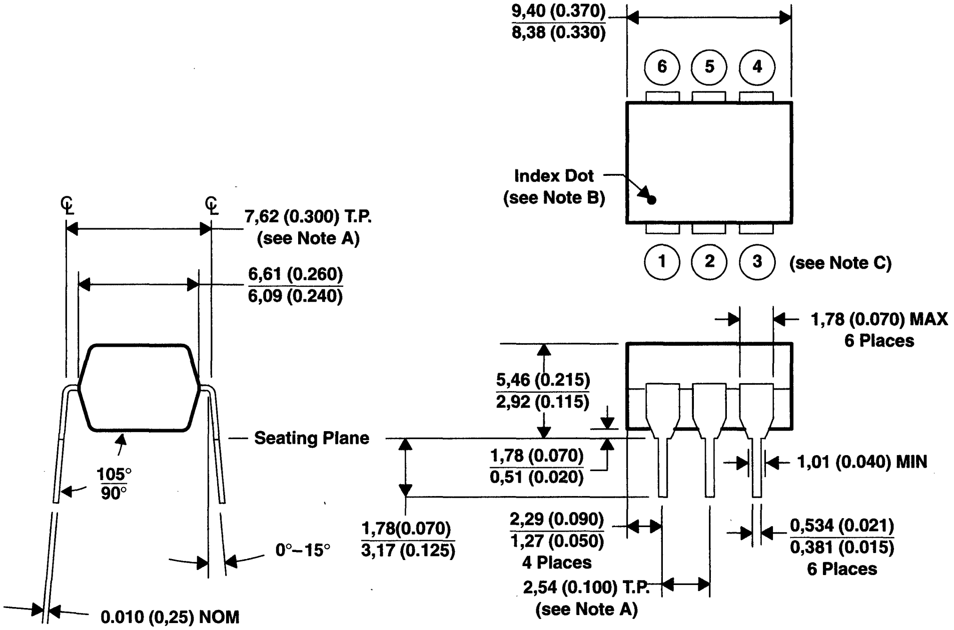
Figure 6. Inductive Load With Sensitive-Gate Traic



15 mA < I_{GT} < 50 mA

Figure 7. Inductive Load With Nonsensitive-Gate Triac

MECHANICAL INFORMATION



NOTES:
A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
   1. Anode (part of the infrared-emitting diode)
   2. Cathode (part of the infrared-emitting diode)
   3. No internal connection
   4. Main terminal (part of the phototransistor)
   5. Triac Substrate (DO NOT connect) (part of the phototransistor)
   6. Main terminal (part of the phototransistor)
D. The dimensions given fall within JEDEC MO-001 AM dimensions.
E. All linear dimensions are given in millimeters and parenthetically given in inches.

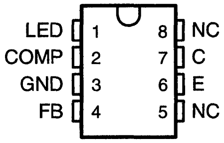
Figure 8. Mechanical Information

TPS5904, TPS5904A
OPTO-ISOLATED FEEDBACK AMPLIFIERS

SOES016A – MAY 1995 – REVISED OCTOBER 1995

- **TL431 Precision Programmable Reference and an Optocoupler in a Single Package**
- **0.4% Voltage-Reference Tolerance**
- **Controlled Optocoupler CTRs:**
  - **TPS5904 100% to 400%**
  - **TPS5904A 150% to 300%**
- **High Withstand Voltage (WTV), 7500 V Peak for 1 Minute**
- **UL Recognized – File #E65085**
- **VDE 884 Agency Approval Pending**

P PACKAGE
(TOP VIEW)



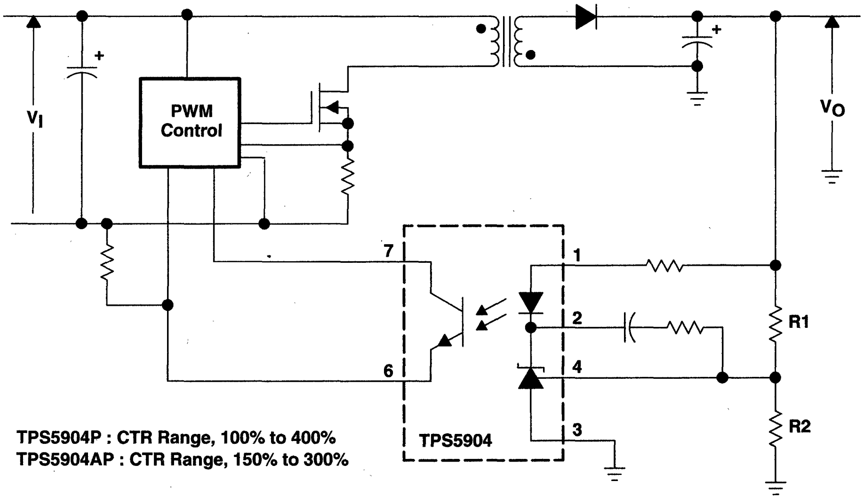
NC – No internal connection

description

The TPS5904 and TPS5904A opto-isolated feedback amplifiers consist of the industry standard TL431 precision programmable reference with a 0.4% reference voltage tolerance, and an optocoupler. The devices are primarily intended for use as the error-amplifier/reference/isolation-amplifier element in isolated ac-to-dc power supplies and dc-to-dc converters. The optocoupler is a gallium-arsenide (GaAs) light-emitting diode that emits at a wavelength of 940 nm, combined with a silicon phototransistor. The current transfer ratio (CTR) ranges from 100% to 400% in the standard version. The TPS5904A version with a 150%-to-300% CTR is available for higher-performance applications. When using the TPS5904 or TPS5904A, power-supply designers can reduce component count and save space in tightly packaged designs. The tight-tolerance reference eliminates the need for adjustments in many applications.

The TPS5904 and TPS5904A are characterized for operation from −40°C to 100°C. Each device is supplied in an 8-pin DIP package.

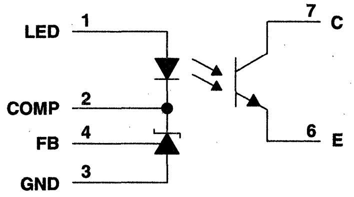
typical application



TPS5904P : CTR Range, 100% to 400%
TPS5904AP : CTR Range, 150% to 300%

TEXAS INSTRUMENTS

functional block diagram



Terminal Functions

TERMINAL NAME	 NO.	I/O	DESCRIPTION
C	7		Phototransistor collector
COMP	2	O	Light-emitting diode and TL431 cathodes
E	6		Phototransistor emitter
FB	4	I	Feedback
GND	3		Ground
LED	1	I	Light-emitting diode anode
NC	5, 8		No connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input power dissipation at (or below) T_A = 25°C (see Note 1)	250 mW
Input LED current, $I_{I(LED)}$	50 mA
Input LED voltage, $V_{I(LED)}$	37 V
Input diode reverse voltage	6 V
Output power dissipation at (or below) T_A = 25°C (see Note 2)	150 mW
Output collector-to-emitter voltage	35 V
Output emitter-to-collector voltage	7 V
Output collector current	50 mA
Total continuous power dissipation at (or below) T_A = 25°C (see Note 3)	350 mW
Operating free-air temperature range, T_A	−40°C to 100°C
Storage temperature range, T_{stg}	−55°C to 150°C
Total input-to-output voltage	7.5 kV peak or dc (5.3 kVrms)
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Flammability	(see Note 4)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Derate linearly from 25°C at a rate of 2.95 mW/°C.
2. Derate linearly from 25°C at a rate of 1.76 mW/°C.
3. Derate linearly from 25°C at a rate of 4.12 mW/°C.
4. Optocoupler total-package flame retardancy is tested to IEC695-2-2 using a flame application time of 30 seconds. Outer mold compound is verified to meet UL 94V-0.

electrical characteristics, T_A = 25°C (unless otherwise noted)

input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Light-emitting diode forward voltage	$V_{O(COMP)} = V_{I(FB)}$, $I_{I(LED)}$ = 10 mA, See Figure 1		1.2	1.4	V
I_R	Light-emitting diode reverse current	V_R = 6 V			10	µA
V_{ref}	Reference voltage	$V_{O(COMP)} = V_{I(FB)}$, $I_{I(LED)}$ = 10 mA, See Figure 1	2.49	2.5	2.51	V
$V_{ref(dev)}$	Deviation of reference voltage over temperature	$V_{O(COMP)} = V_{I(FB)}$, $I_{I(LED)}$ = 10 mA, T_A = 25°C to 100°C, See Figure 1		25		mV
$\frac{\Delta V_{ref}}{\Delta V_{I(LED)}}$	Ratio of reference voltage change-to-change in input light-emitting-diode voltage	$\Delta V_{I(LED)}$ = 4 V to 37 V, $I_{I(LED)}$ = 10 mA, See Figure 2		−1.1	−2	mV/V
$I_{I(FB)}$	Feedback input current	$I_{I(LED)}$ = 10 mA, R3 = 10 kΩ , See Figure 2		1.5	3	µA
$I_{ref(dev)}$	Deviation of reference input current over temperature	$I_{I(LED)}$ = 10 mA, R3 = 10 kΩ, T_A = 25°C to 100°C, See Figure 3		0.5		µA
$I_{DRV(min)}$	Minimum drive current	$V_{O(COMP)} = V_{I(FB)}$, See Figure 1		0.45	1	mA
$I_{I(off)}$	Off-state input light-emitting-diode current	$V_{I(LED)}$ = 37 V, $V_{I(FB)}$ = 0, See Figure 4		0.18	0.5	µA
$\lvert Z_{ka}\rvert$†	Regulator output impedance	$V_{O(COMP)} = V_{I(FB)}$, f ≤ 1 kHz, $I_{O(COMP)}$ = 1 mA to 50 mA		0.1		Ω

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CEO}	Collect dark current	V_{CE} = 35 V, See Figure 5			100	nA
$V_{(BR)ECO}$	Emitter-collector voltage breakdown	I_E = 100 µA	7			V

coupler

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTR	Current transfer ratio	TPS5904	$V_{O(COMP)} = V_{I(FB)}$, $I_{I(LED)}$ = 5 mA, V_{CE} = 5 V, See Figure 6	100%		400%	
		TPS5904A		150%		300%	
$V_{CE(sat)}$	Collector-emitter saturation voltage		$V_{O(COMP)} = V_{I(FB)}$, $I_{I(LED)}$ = 10 mA, I_C = 1 mA, See Figure 6		0.1	0.2	V
V_{iso}†	Isolation voltage		I_{IO} = 10 µA, f = 60 Hz	7500			V
C_{io}	Input to output capacitance		V_{IO} = 0, f = 1 kHz		0.6		pF

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

PARAMETER MEASUREMENT INFORMATION

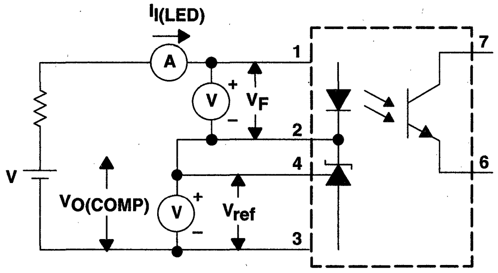


Figure 1. V_{ref}, V_F, I_{min} Test Circuit

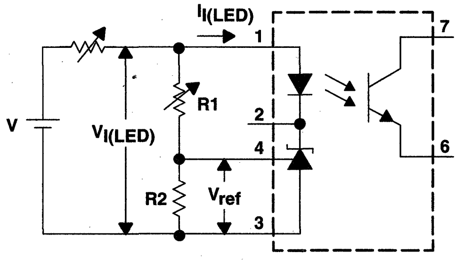


Figure 2. $\Delta V_{ref}/\Delta V_{I(LED)}$ Test Circuit

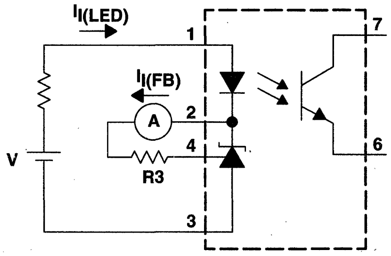


Figure 3. $I_{I(FB)}$ Test Circuit

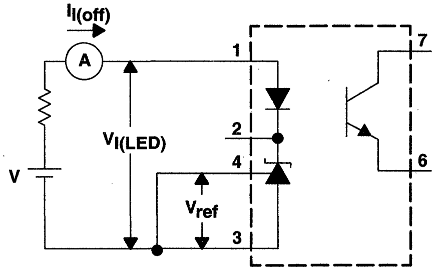


Figure 4. $I_{I(off)}$ Test Circuit

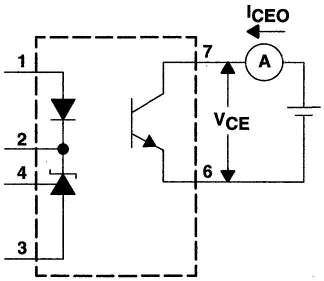


Figure 5. I_{CEO} Test Circuit

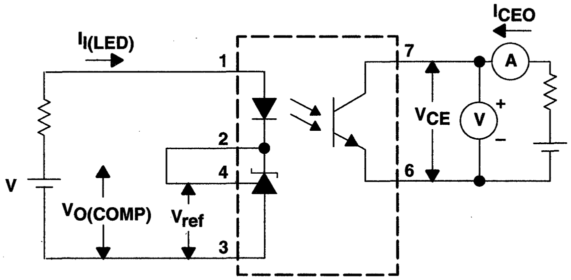


Figure 6. CTR, $V_{CE(sat)}$ Test Circuit

TYPICAL CHARACTERISTICS

INPUT LIGHT-EMITTING-DIODE CURRENT vs REFERENCE VOLTAGE

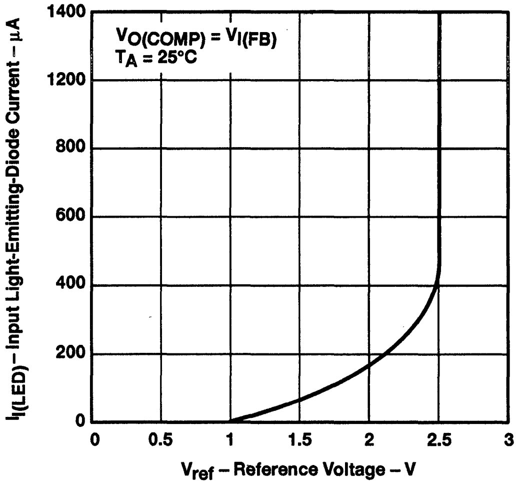


Figure 7

INPUT LIGHT-EMITTING-DIODE CURRENT vs REFERENCE VOLTAGE

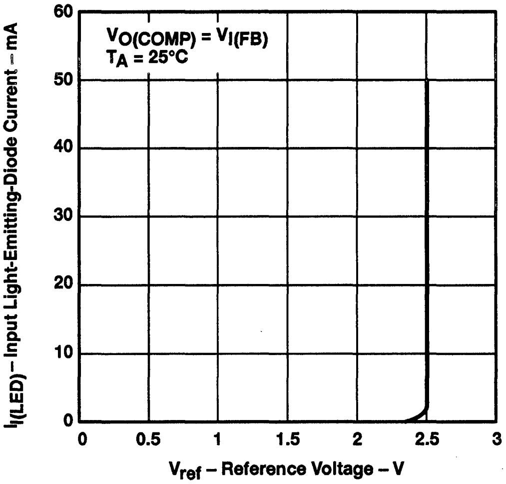


Figure 8

REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

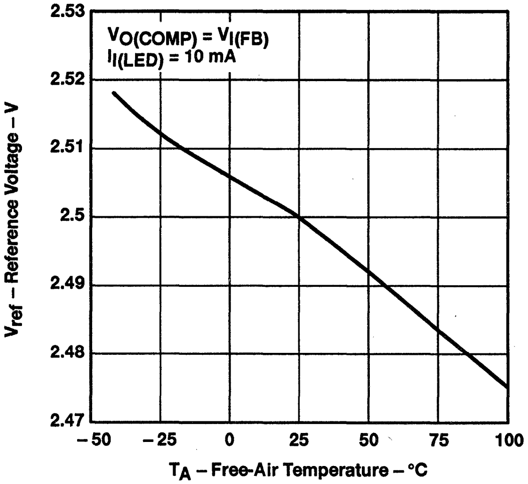


Figure 9

RATIO OF DELTA REFERENCE VOLTAGE TO DELTA LED VOLTAGE vs FREE-AIR TEMPERATURE

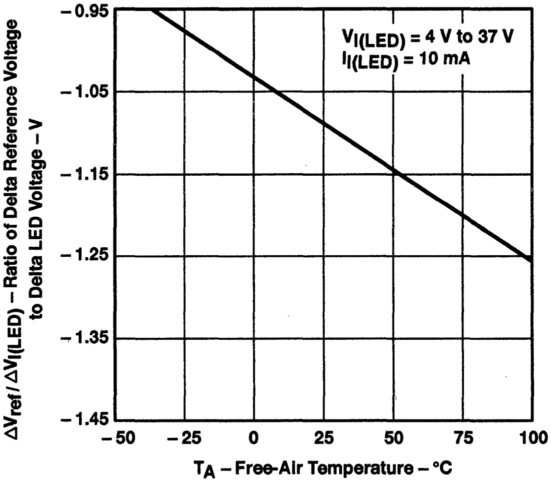


Figure 10

TYPICAL CHARACTERISTICS

**REFERENCE CURRENT
vs
FREE-AIR TEMPERATURE**

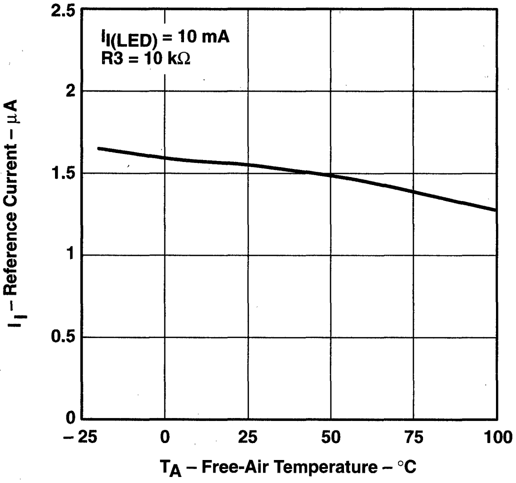


Figure 11

**OFF-STATE INPUT
LIGHT-EMITTING-DIODE CURRENT
vs
FREE-AIR TEMPERATURE**

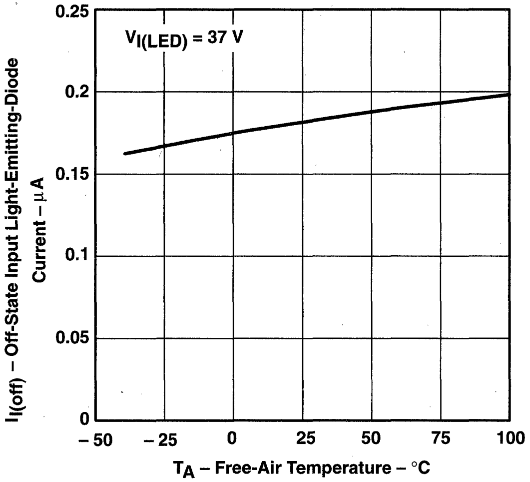


Figure 12

**COLLECTOR DARK CURRENT
vs
FREE-AIR TEMPERATURE**

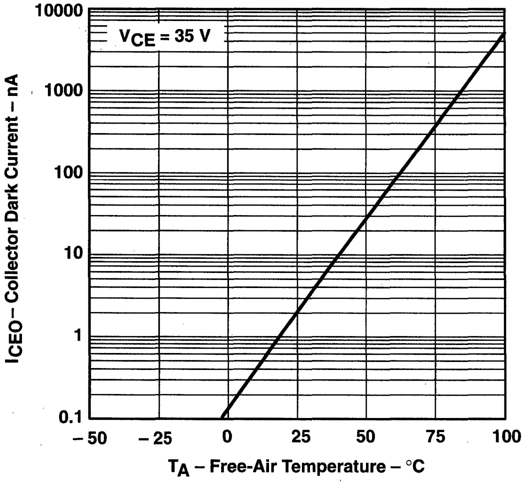


Figure 13

**NORMALIZED CURRENT TRANSFER RATIO
RELATIVE TO VALUE AT T_A = 25°C
vs
FREE-AIR TEMPERATURE**

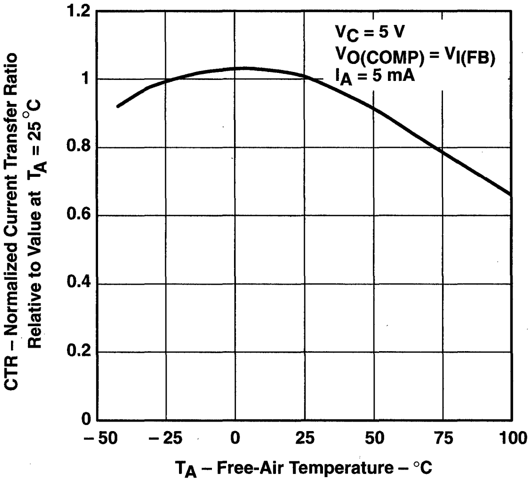


Figure 14

TYPICAL CHARACTERISTICS

CURRENT TRANSFER RATIO vs INPUT LIGHT-EMITTING-DIODE CURRENT

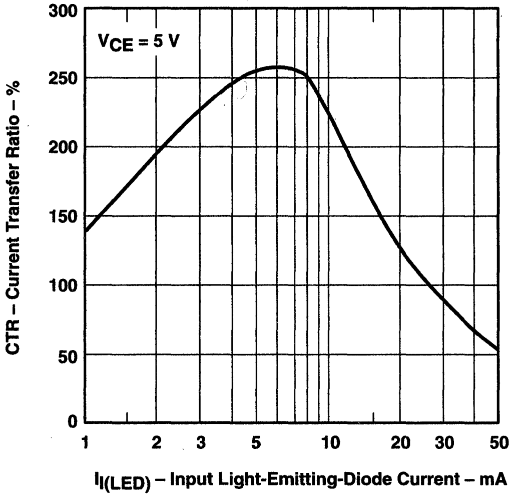


Figure 15

COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

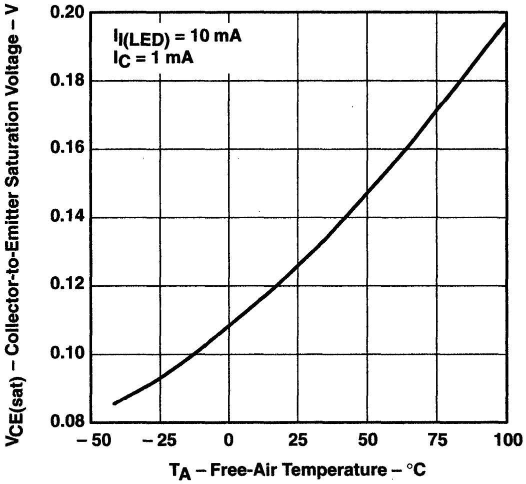


Figure 16

INPUT LIGHT-EMITTING-DIODE FORWARD CURRENT vs LIGHT-EMITTING-DIODE FORWARD VOLTAGE

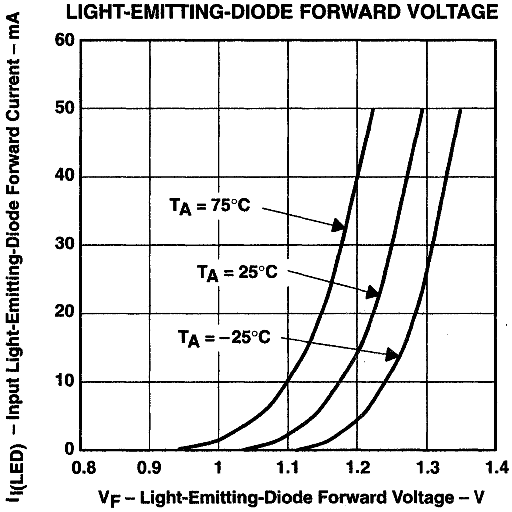


Figure 17

Contents

LT1054, LT1054Y
SWITCHED-CAPACITOR VOLTAGE CONVERTERS WITH REGULATOR

SLVS033B – FEBRUARY 1990 – REVISED AUGUST 1995

- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin Compatible With the LTC1044/7660**

description

The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current is typically 1.1 V. This holds true over the full supply voltage range of 3.5 V to 15 V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback terminal. Supply current in shut-down is typically 100 μA.

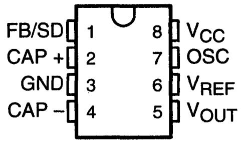
The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

AVAILABLE OPTIONS

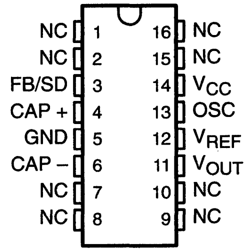
T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	LT1054CDW	LT1054CP	LT1054Y
−40°C to 85°C	LT1054IDW	LT1054IP	—

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., LT1054CDWR).

P PACKAGE
(TOP VIEW)

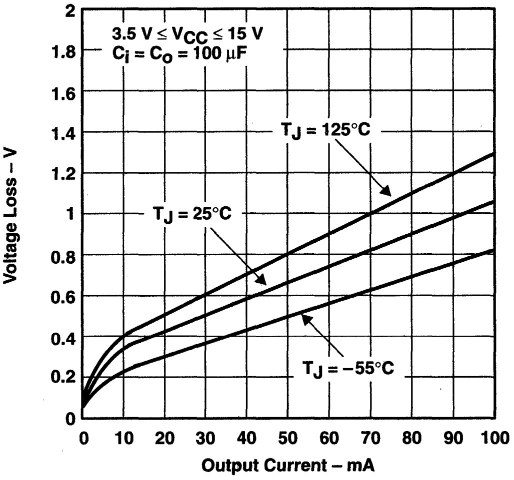


DW PACKAGE
(TOP VIEW)

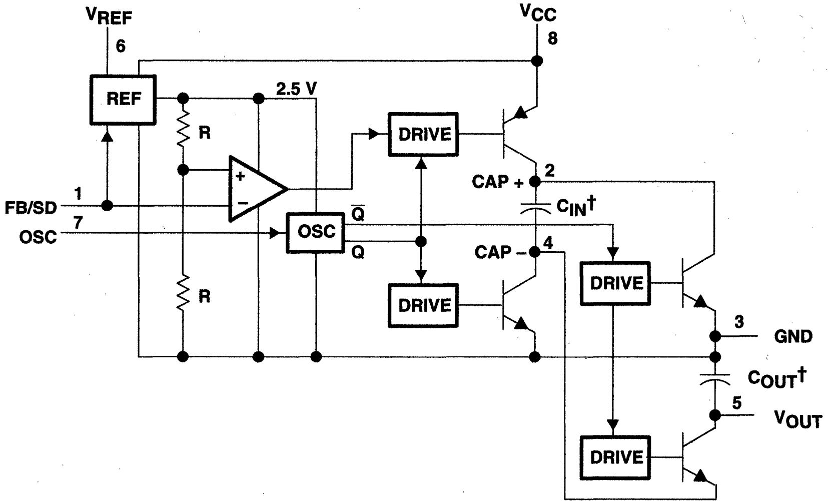


NC – No internal connection

VOLTAGE LOSS
vs
OUTPUT CURRENT



functional block diagram



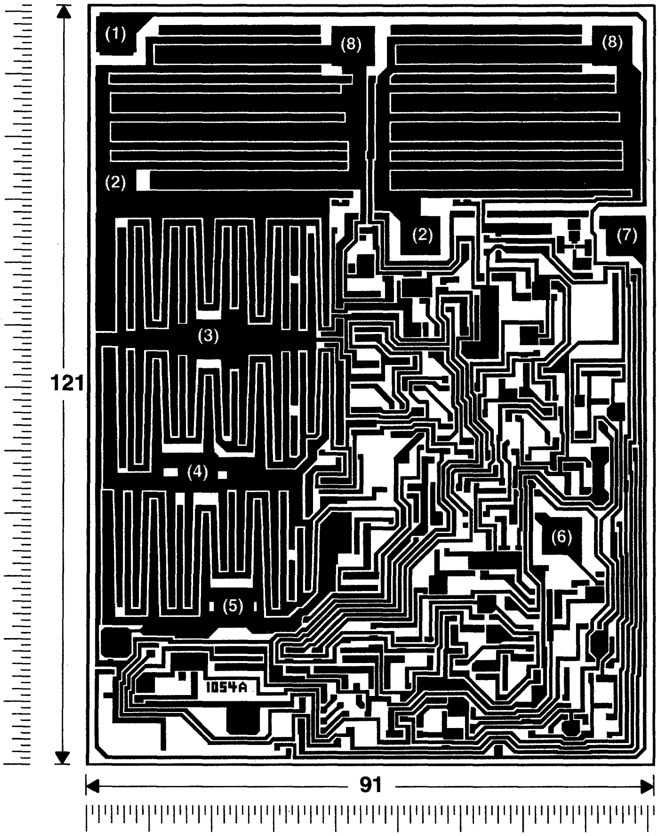
† External capacitors

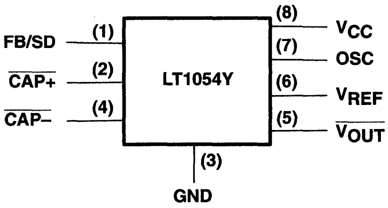
NOTE A. Terminal numbers shown are for the P package only.

LT1054Y chip information

This chip, when properly assembled, displays characteristics similar to the LT1054. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL NUMBERS SHOWN
ARE FOR THE P PACKAGE ONLY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		16 V
Input voltage range, V_I (FB/SD terminal)		0 V to V_{CC}
Input voltage range, V_I (OSC terminal)		0 V to V_{ref}
Junction temperature (see Note 2) T_J:	LT1054C	125°C
	LT1054I	135°C
Operating free-air temperature range, T_A:	LT1054C	0°C to 70°C
	LT1054I	−40°C to 85°C
Storage temperature range, T_{stg}		−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The absolute maximum supply voltage rating of 16 V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \leq 15$ V, this rating may be increased to 20 V.

2. The devices are functional up to the absolute maximum junction temperature.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	15	V
Operating free-air temperature range, T_A	LT1054C	0	70	°C
	LT1054I	−40	85	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LT1054C, LT1054I			UNIT
					MIN	TYP‡	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 3		25°C	−4.7	−5	−5.2	V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 3		Full range		5	25	mV
	Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 3		Full range		10	50	mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = 100 µF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
			I_O = 100 mA	Full range		1.1	1.6	
	Output resistance	ΔI_O = 10 mA to 100 mA See Note 5		Full range		10	15	Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA		25°C	2.35	2.5	2.65	V
				Full range	2.25		2.75	
	Maximum switch current			25°C		300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V	Full range		2.5	3.5	mA
			V_{CC} = 15 V	Full range		3	4.5	
	Supply current in shut-down	$V_{(FB/SD)}$ = 0 V		Full range		100	150	µA

† Full range is 0°C to 70°C for the LT1054C and −40°C to 85°C for the LT1054I.

‡ All typical values are at T_A = 25°C.

NOTES: 3. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).

4. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.

5. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents less than 10 mA due to the characteristics of the switch transistors.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1054Y			UNIT
				MIN	TYP	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 3			−5		V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 3			5		mV
	Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 3			10		mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = 100 µF tantalum	I_O = 10 mA		0.35		V
			I_O = 100 mA		1.1		
	Output resistance	ΔI_O = 10 mA to 100 mA See Note 5			10		Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V			25		kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA			2.5		V
	Maximum switch current				300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V		2.5		mA
			V_{CC} = 15 V		3		
	Supply current in shut-down	$V_{(FB/SD)}$ = 0 V			100		µA

NOTES: 3 All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).

4 For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.

5 Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents less than 10 mA due to the characteristics of the switch transistors.

TYPICAL CHARACTERISTICS

Table of Graphs

Table of Figures

TYPICAL CHARACTERISTICS†

SHUTDOWN THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

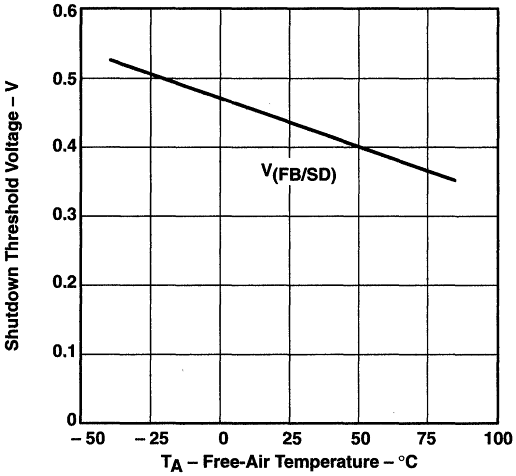


Figure 1

SUPPLY CURRENT vs INPUT VOLTAGE

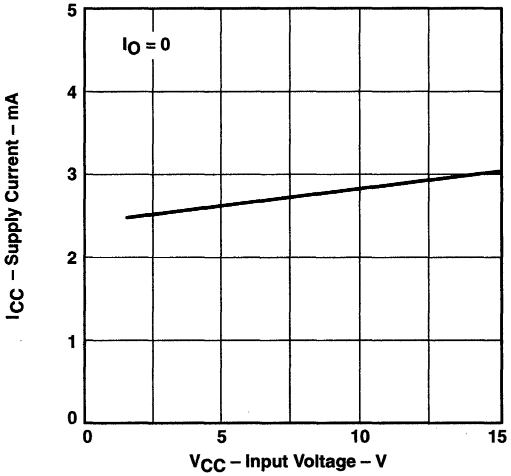


Figure 2

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

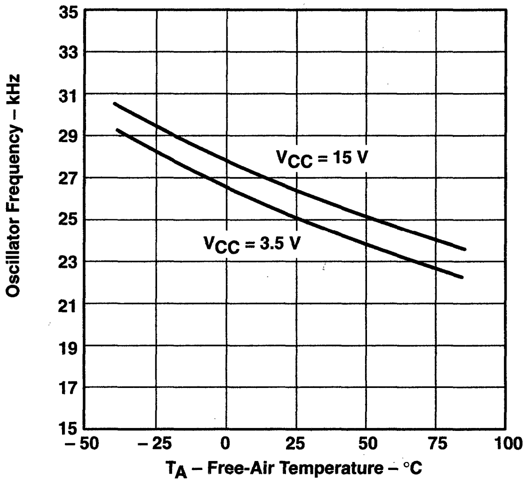


Figure 3

SUPPLY CURRENT IN SHUTDOWN vs INPUT VOLTAGE

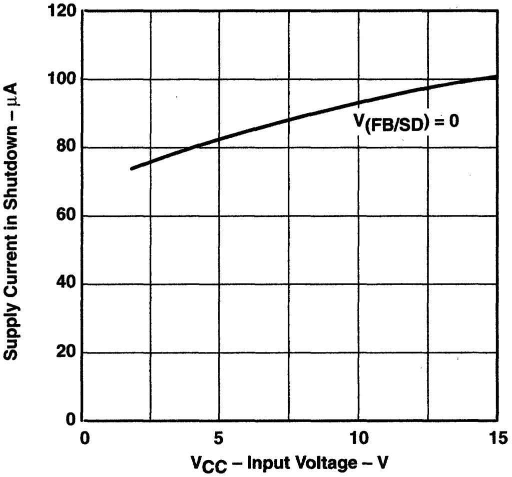


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT vs OUTPUT CURRENT

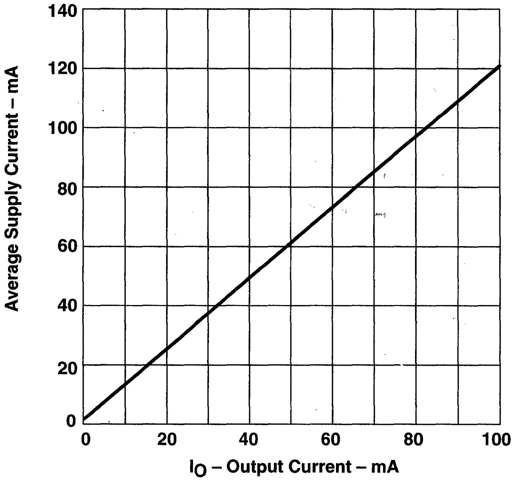


Figure 5

OUTPUT VOLTAGE LOSS vs INPUT CAPACITANCE

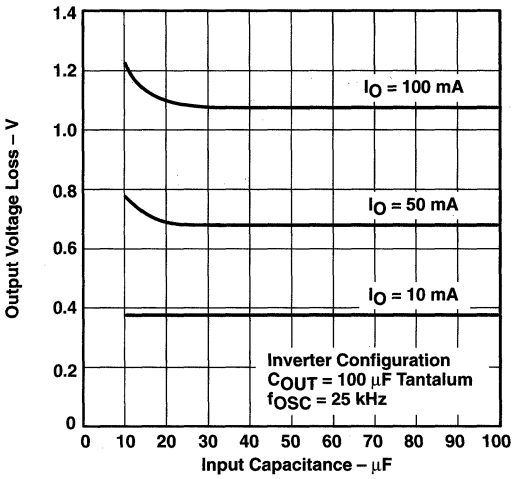


Figure 6

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

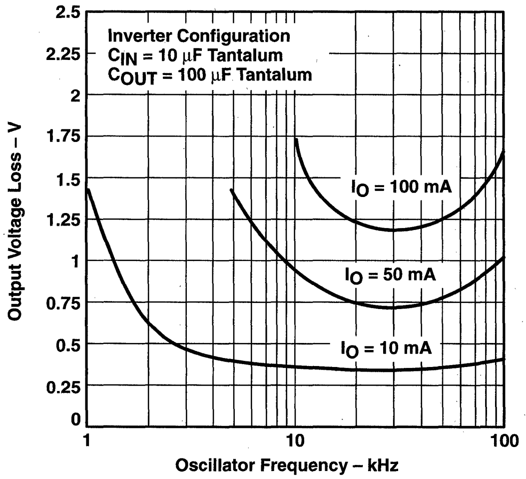


Figure 7

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

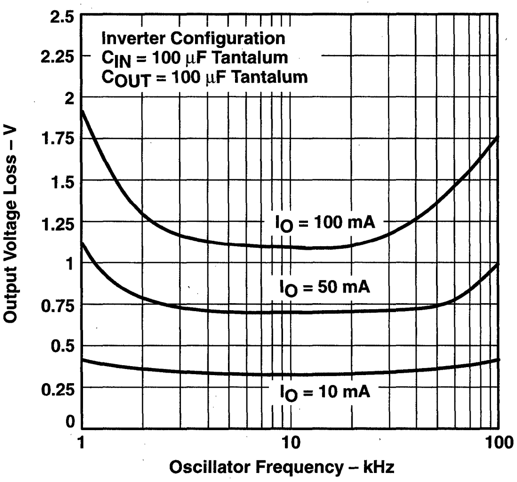


Figure 8

TYPICAL CHARACTERISTICS†

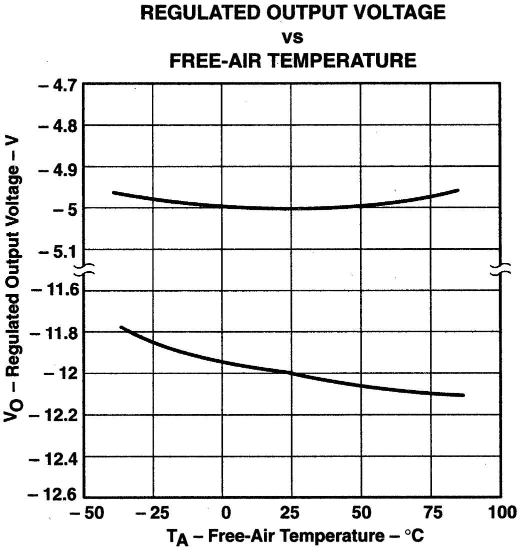


Figure 9

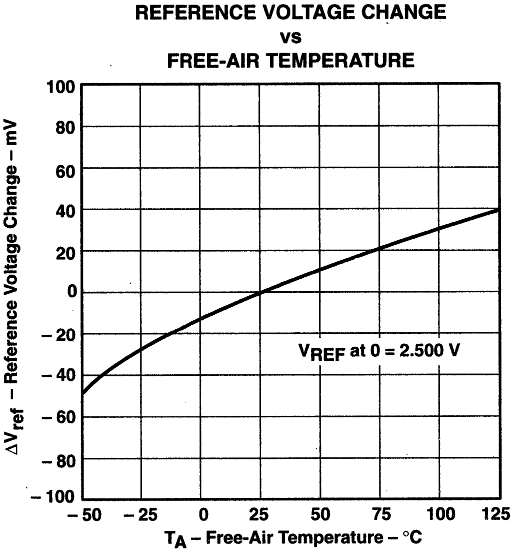


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PRINCIPLES OF OPERATION

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 11 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is as shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \tag{1}$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \tag{2}$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \tag{3}$$

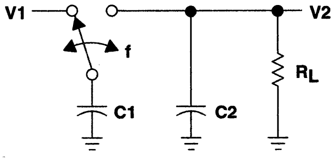


Figure 11. Switched-Capacitor Building Block

PRINCIPLES OF OPERATION

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is as shown in Figure 12. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

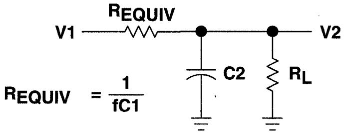


Figure 12. Switched-Capacitor Equivalent Circuit

terminal functions (see functional block diagram)

Supply voltage V_{CC} alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the LT1054, and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 µF, preferably tantalum or some other low equivalent-series-resistance (ESR) type, is recommended. A larger capacitor is desirable in some cases. An example is when the actual input supply is connected to the LT1054 through long leads or when the pulse currents drawn by the LT1054 might affect other circuits through supply coupling.

In addition to being the output terminal, V_{OUT} is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other terminals. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 13). This transistor prevents V_{OUT} from being pulled above GND during start-up. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \le \frac{\left(\left|V_{OUT}\right|\right)\beta}{I_{OUT}} \tag{4}$$

APPLICATION INFORMATION

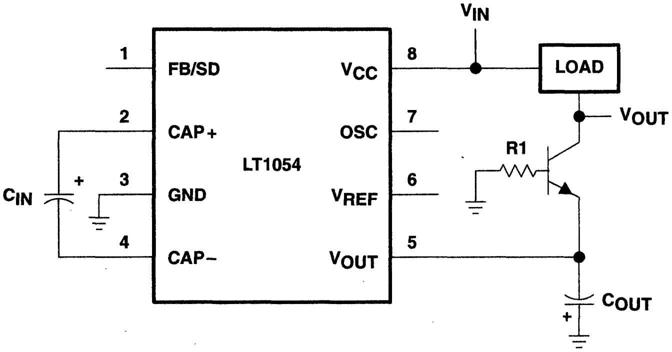


Figure 13. Circuit with Load Connected from V_{CC} to V_{OUT}

The voltage reference (V_{ref}) output provides a 2.5-V reference point for use in LT1054-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback terminal. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 µA. V_{ref} draws approximately 100 µA when shorted to ground and does not affect the internal reference/regulator. This terminal can also be used as a pullup for LT1054 circuits that require synchronization.

CAP+ is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional, as should be expected when using bipolar switches.

The OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 µA, so that the duty cycle is approximately 50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 14) in the range of 5 pF - 20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{ref}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an NPN transistor can then be used to drive OSC at the external clock frequency as shown in Figure 14.

The frequency can be lowered by adding an external capacitor (C_1 in Figure 14) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

APPLICATION INFORMATION

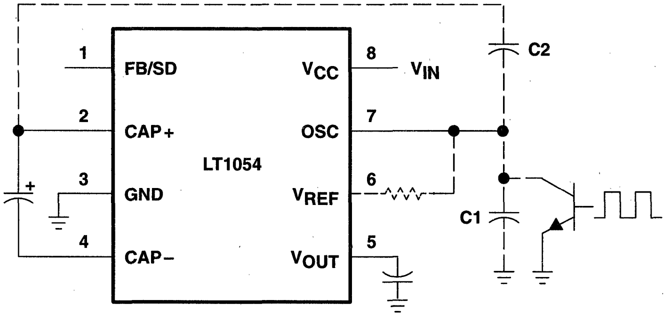
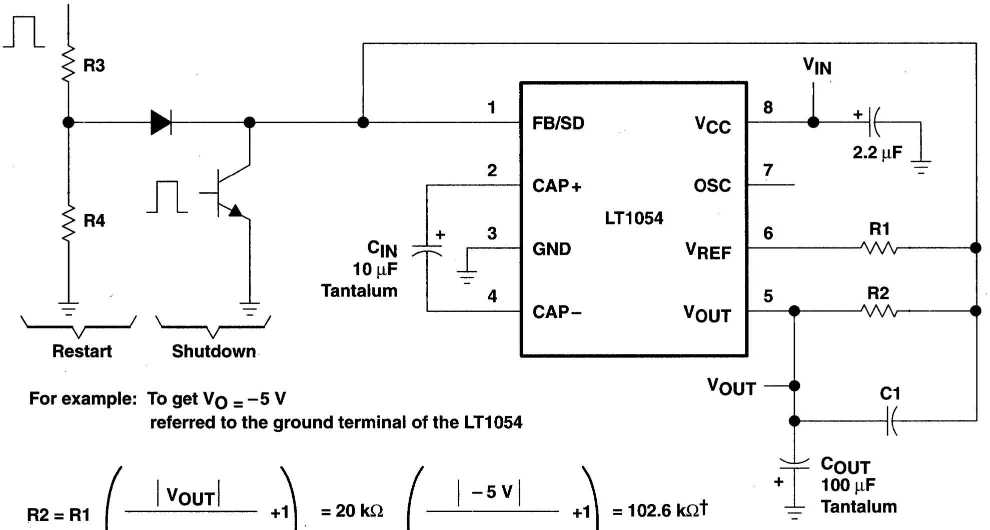


Figure 14. External Clock System

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 µA . Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 15, the restart signal can be either a pulse (t_p > 100 µs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 15 should be chosen to provide a signal level at FB/SD of 0.7 V - 1.1 V.

FB/SD is also the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.

APPLICATION INFORMATION



For example: To get $V_O = -5$ V
referred to the ground terminal of the LT1054

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|-5\text{ V}|}{\frac{2.5\text{ V}}{2} - 40\text{ mV}} + 1\right) = 102.6\text{ k}\Omega^{\dagger}$$

Where: R1 = 20 kΩ
V_{REF} = 2.5 V Nominal

† Choose the closest 1% value

Figure 15. Basic Regulation Configuration

regulation

The error amplifier of the LT1054 drives the pnp switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 15 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 µA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 µF for all output voltages.

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground terminal of the LT1054, must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler can provide higher voltages at reduced output currents.

APPLICATION INFORMATION

capacitor selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good-quality low-ESR capacitors, such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the ESR of the capacitor is multiplied by four, since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown:

$$\Delta V = \frac{I_{OUT}}{2\,fC_{OUT}} \tag{5}$$

where:

ΔV = p-p ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (\text{ESR of } C_{OUT}) \tag{6}$$

power dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 is calculated as shown.

$$P \approx (V_{CC} - |V_{OUT}|)\ I_{OUT} + (V_{CC})\ (I_{OUT})\ (0.2) \tag{7}$$

where both V_{CC} and V_{OUT} are referenced to ground. The power dissipation is equivalent to that of a linear regulator. Limited power handling capability of the LT1054 packages causes limited output current requirements or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 16. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown:

$$R_X = V_x/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - \left[(\text{LT1054 voltage loss})\ (1.3) + |V_{OUT}|\right] \tag{8}$$

and I_{OUT} = maximum required output current. The factor of 1.3 allows some operating margin for the LT1054.

APPLICATION INFORMATION

When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ \text{V} - |-5\ \text{V}|)\ (100\ \text{mA}) + (12\ \text{V})\ (100\ \text{mA})\ (0.2)$$

$$P = 700\ \text{mW} + 240\ \text{mW} = 940\ \text{mW}$$

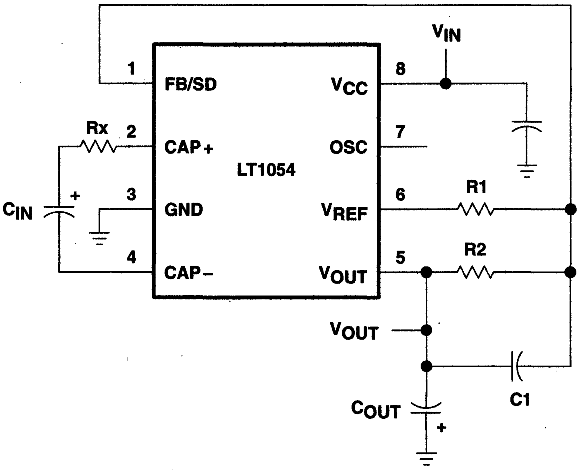


Figure 16. Power-Dissipation-Limiting Resistor in Series with C_{IN}

At $R_{\theta JA}$ of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external-resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

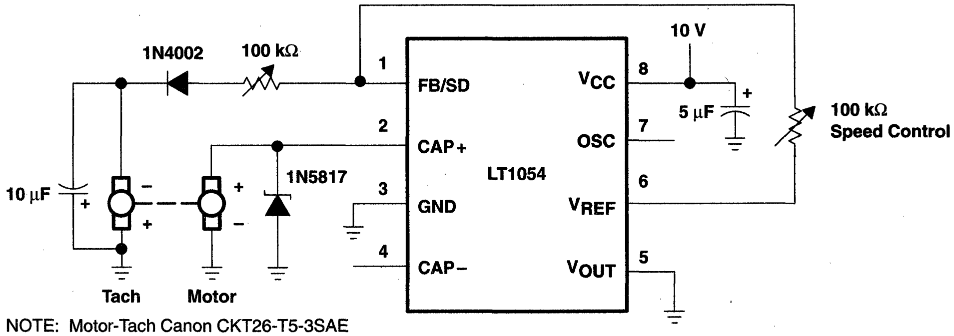
$$V_x = 12\ \text{V} - \left[(1.6\ \text{V})\ (1.3) + |-5\ \text{V}|\right] = 4.9\ \text{V}$$

and

$$R_x = 4.9\ \text{V}/(4.4)\ (100\ \text{mA}) = 11\ \Omega$$

APPLICATION INFORMATION

The resistor reduces the power dissipated by the LT1054 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the LT1054 leads help to remove heat from the device. This is especially true for plastic packages.



NOTE: Motor-Tach Canon CKT26-T5-3SAE

Figure 17. Motor Speed Servo

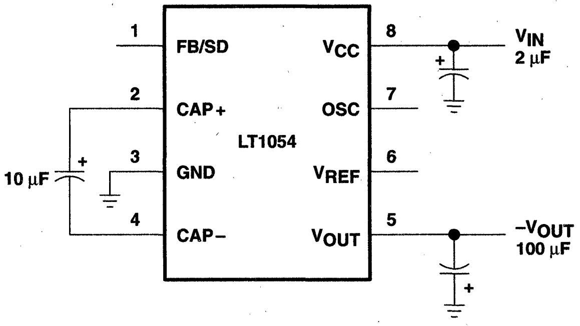
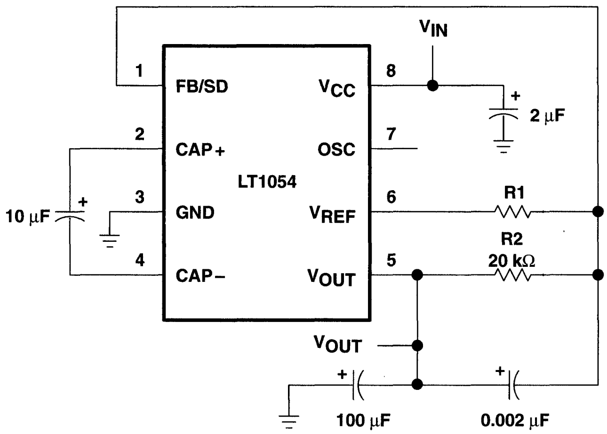


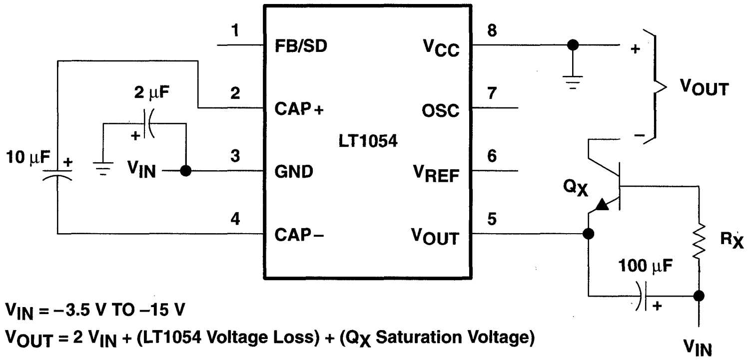
Figure 18. Basic Voltage Inverter

APPLICATION INFORMATION



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 19. Basic Voltage Inverter/Regulator



$V_{IN} = -3.5$ V TO −15 V

$V_{OUT} = 2\,V_{IN}$ + (LT1054 Voltage Loss) + (Q_X Saturation Voltage)

Figure 20. Negative Voltage Doubler

APPLICATION INFORMATION

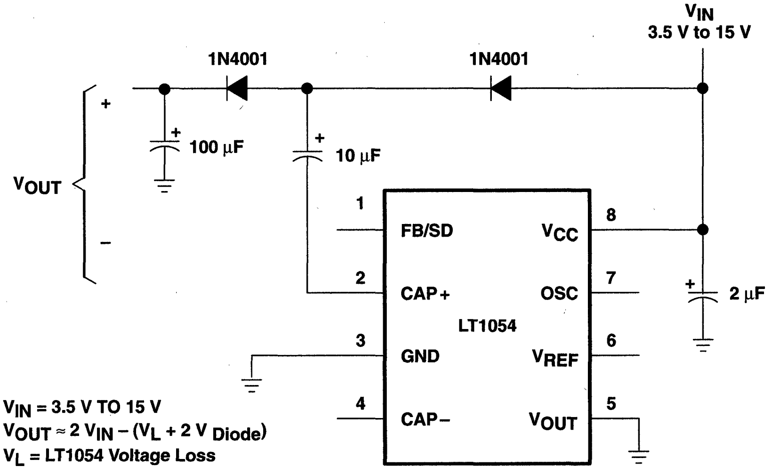
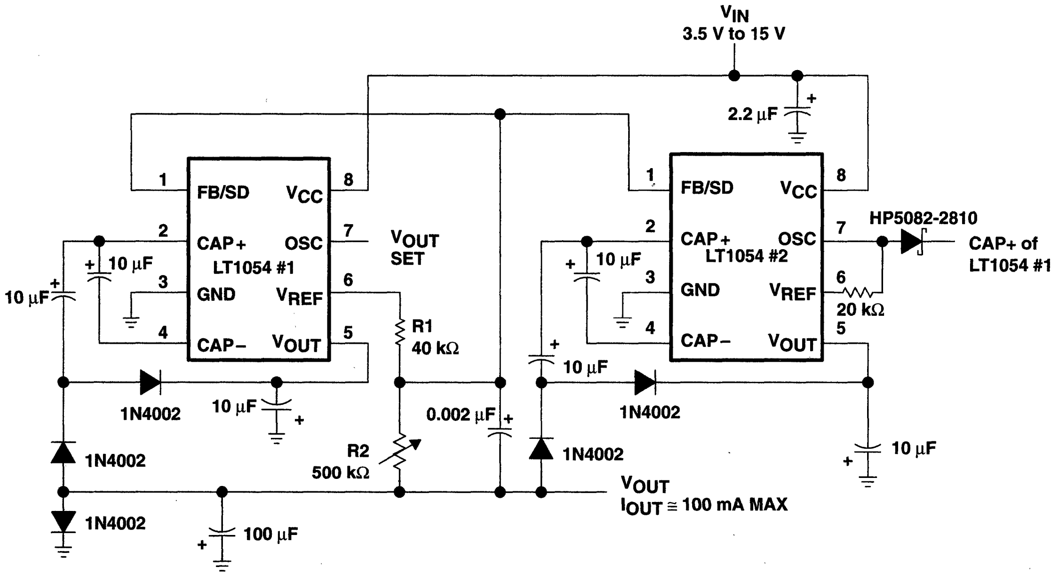


Figure 21. Positive Doubler

APPLICATION INFORMATION



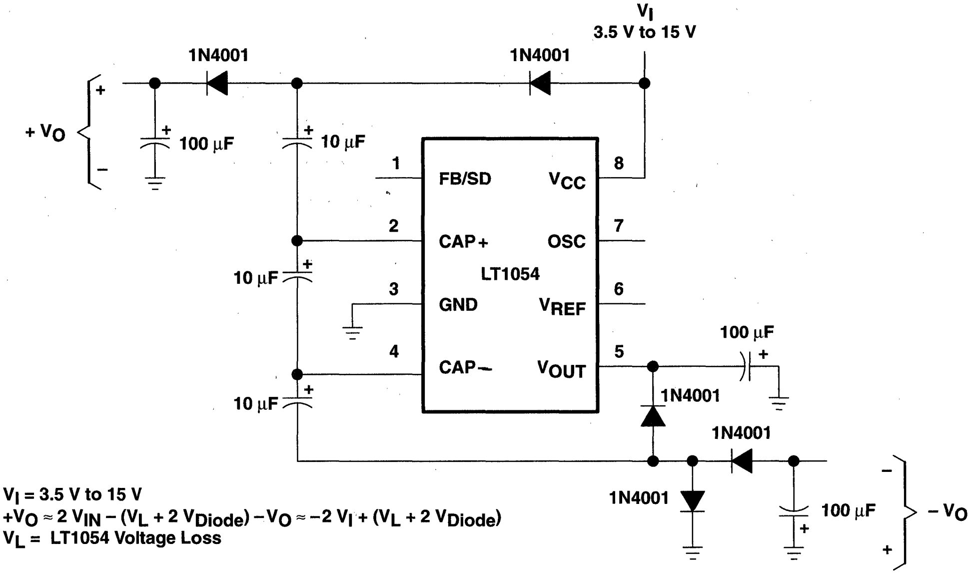
$V_{IN} = 3.5$ to 15 V

$V_{OUT}\ MAX \approx -2\ V_{IN} + [\text{LT1054 Voltage Loss} + 2\ (V_{Diode})]$

$$R2 = R1\left(\frac{\left|V_{OUT}\right|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{\left|V_{OUT}\right|}{1.21\text{ V}} + 1\right)$$

Figure 22. 100-mA Regulating Negative Doubler

APPLICATION INFORMATION



$V_I = 3.5$ V to 15 V
$+V_O \approx 2\,V_{IN} - (V_L + 2\,V_{Diode})$ $-V_O \approx -2\,V_I + (V_L + 2\,V_{Diode})$
$V_L =$ LT1054 Voltage Loss

Figure 23. Dual Output Voltage Doubler

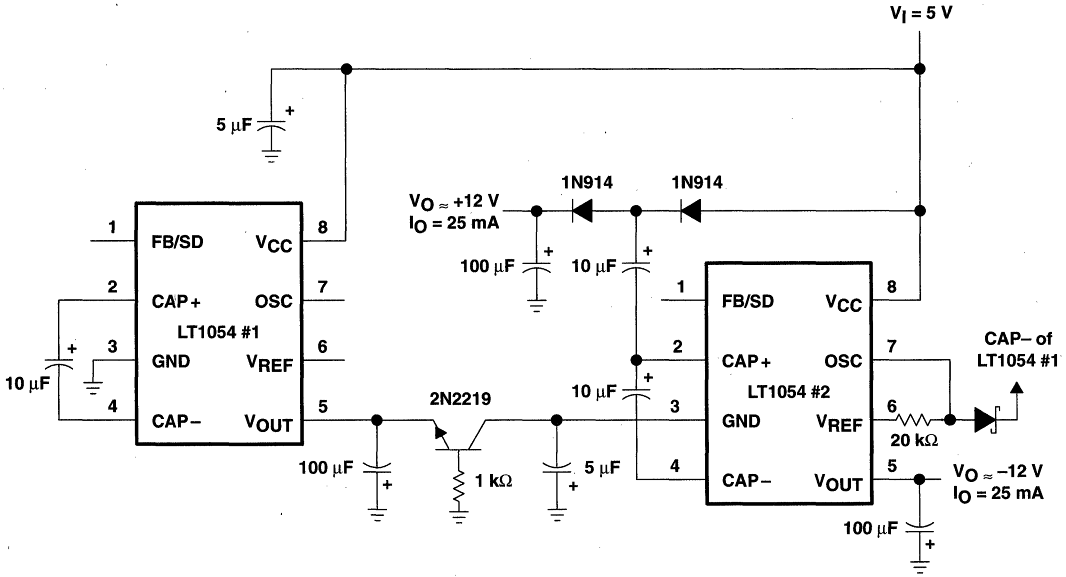
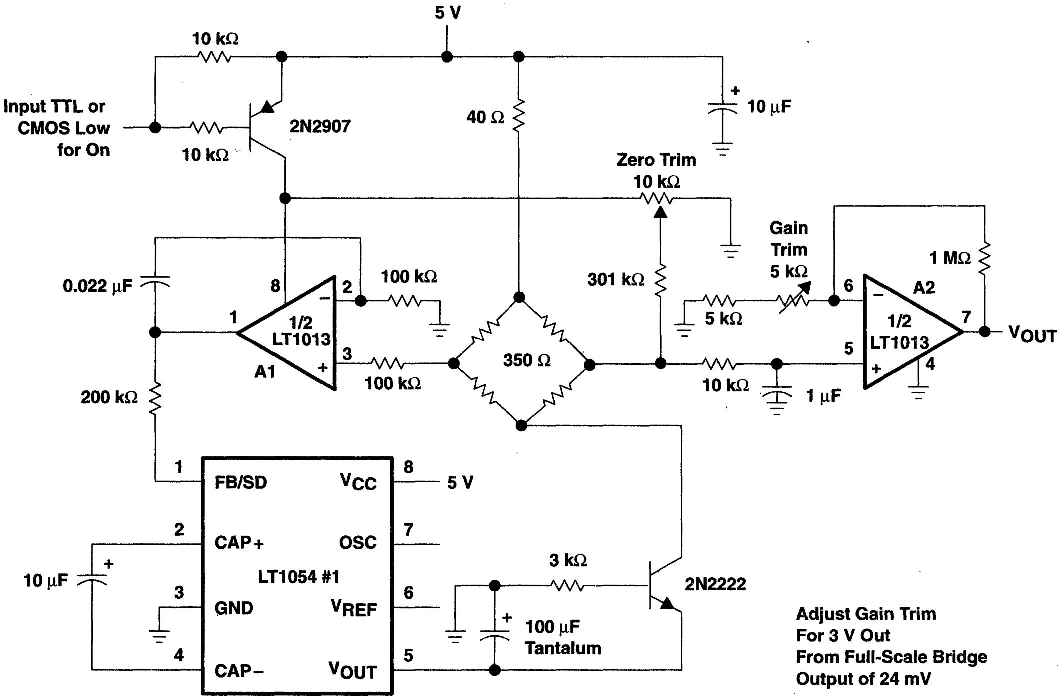


Figure 24. 5-V to ±12-V Converter

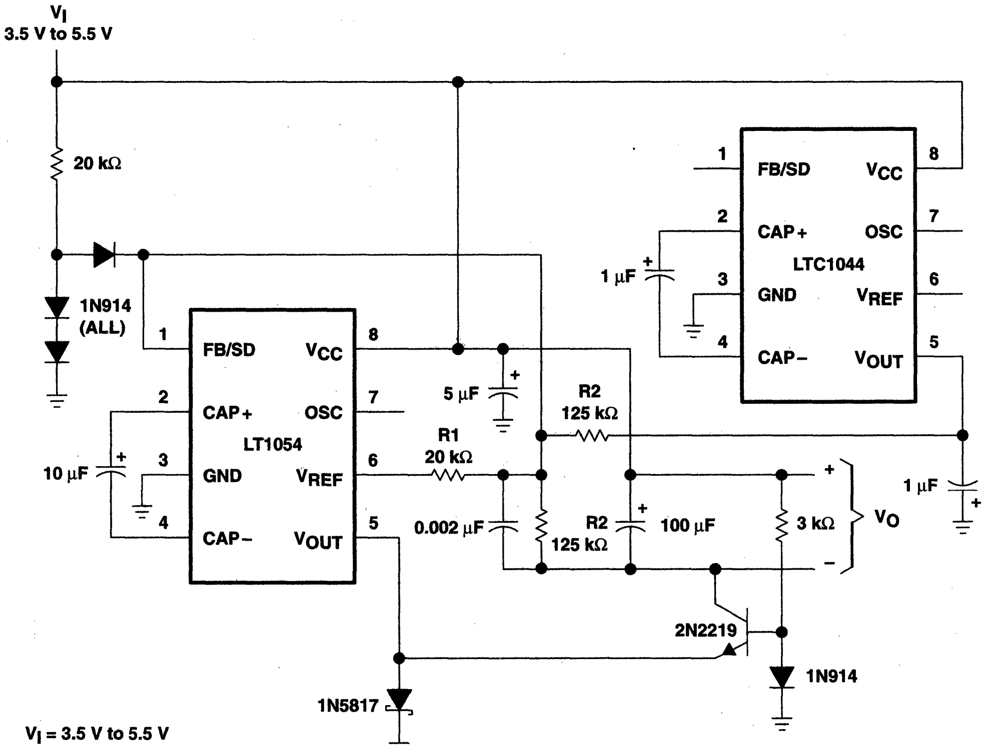
APPLICATION INFORMATION



Adjust Gain Trim
For 3 V Out
From Full-Scale Bridge
Output of 24 mV

Figure 25. Strain Gage Bridge Signal Conditioner

APPLICATION INFORMATION

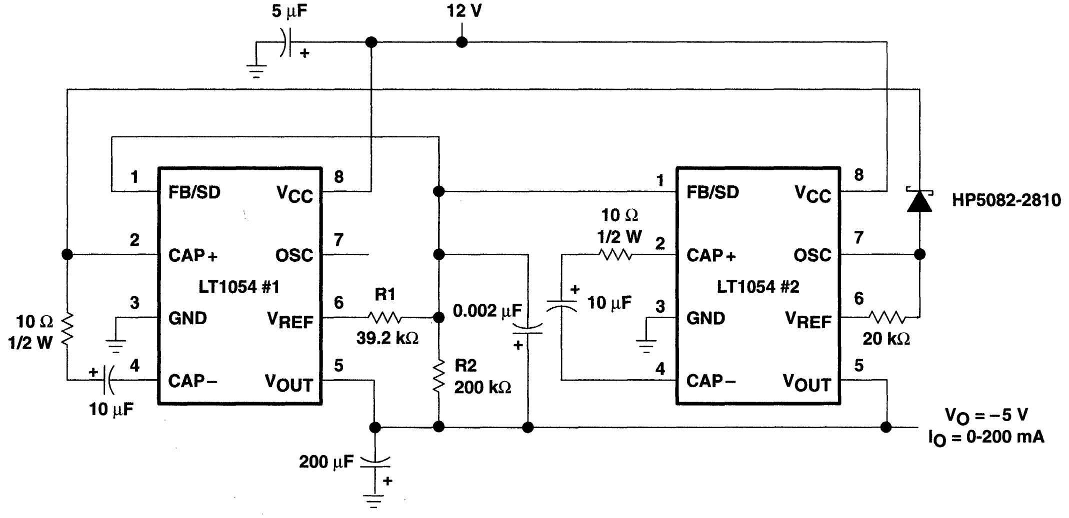


$V_I = 3.5$ V to 5.5 V
$V_O = 5$ V
I_O MAX = 50 mA

$$R2 = R1\left(\frac{\left|V_{OUT}\right|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{\left|V_{OUT}\right|}{1.21\text{ V}} + 1\right)$$

Figure 26. 3.5-V to 5-V Regulator

APPLICATION INFORMATION



$$R2 = R1\left(\frac{\left|V_{OUT}\right|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{\left|V_{OUT}\right|}{1.21\text{ V}} + 1\right)$$

Figure 27. Regulating 200-mA + 12-V to −5-V Converter

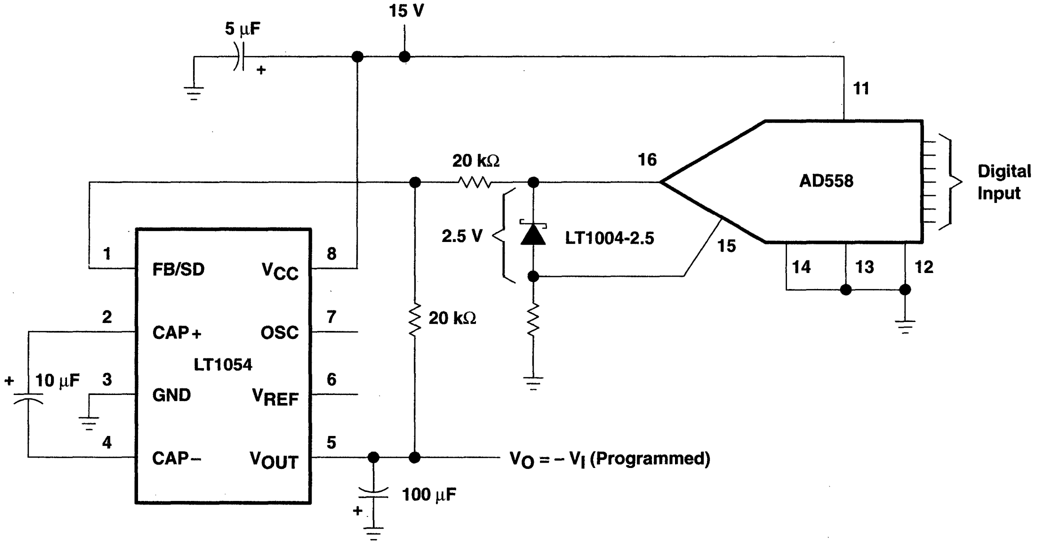


Figure 28. Digitally Programmable Negative Supply

APPLICATION INFORMATION

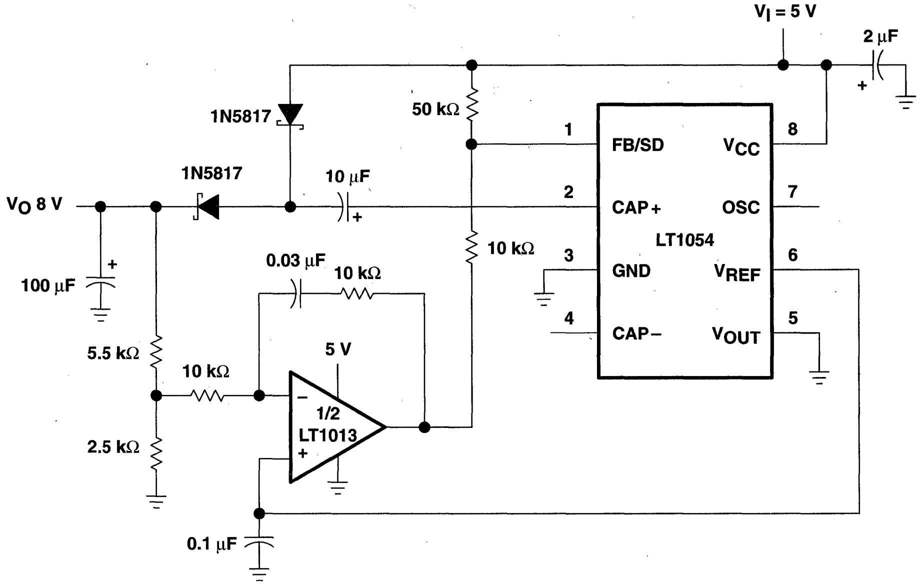
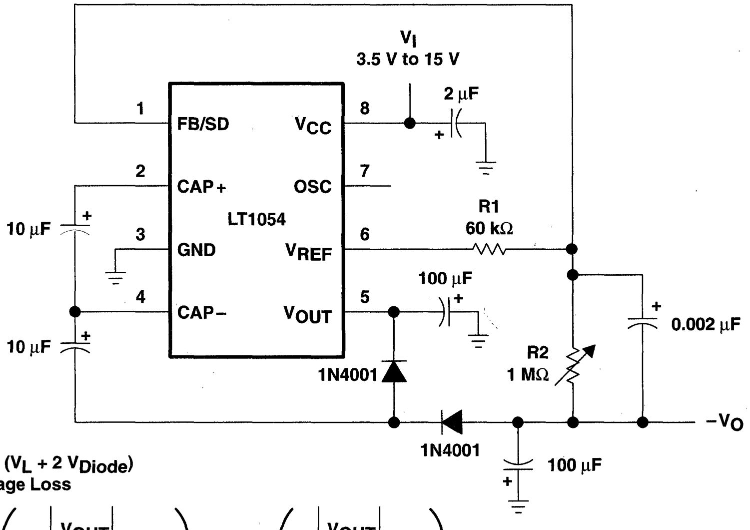


Figure 29. Positive Doubler with Regulation (5-V to 8-V Converter)



V_I = 3.5 V to 15 V
V_O MAX ≈ 2 V_{IN} + (V_L + 2 V_{Diode})
V_L = LT1054 Voltage Loss

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

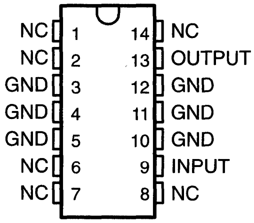
Figure 30. Negative Doubler with Regulator

TL-SCSI285, TL-SCSI285Y
FIXED-VOLTAGE REGULATORS FOR SCSI ACTIVE TERMINATION

SLVS065C – NOVEMBER 1991 – REVISED AUGUST 1995

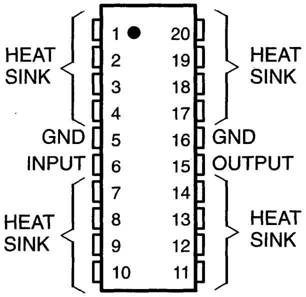
- **Fully Matches Parameters for Alternative 2 SCSI Active Termination**
- **Fixed 2.85-V Output**
- **±1% Maximum Output Tolerance at T_J = 25°C**
- **0.7-V Maximum Dropout Voltage**
- **620-mA Output Current**
- **±2% Absolute Output Variation**
- **Internal Overcurrent Limiting Circuitry**
- **Internal Thermal Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



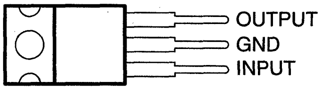
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE
(TOP VIEW)

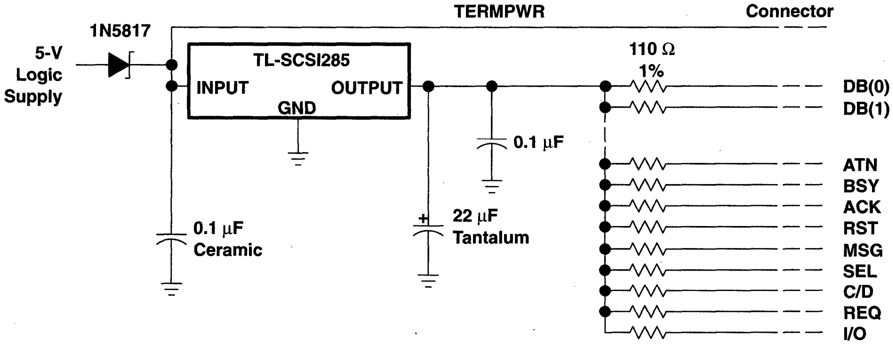


description

The TL-SCSI285 is a low-dropout (0.7-V) fixed-voltage regulator specifically designed for small computer systems interface (SCSI) alternative 2 active signal termination. The TL-SCSI285 0.7-V maximum dropout ensures compatibility with existing SCSI systems while providing a wide TERMPWR voltage range. At the same time the ±1% initial tolerance on its 2.85-V output voltage ensures a tighter line driver current tolerance, thereby increasing system noise margin.

The fixed 2.85-V output voltage of the TL-SCSI285 supports the SCSI alternative 2 termination standard while reducing system power consumption. The 0.7-V maximum dropout voltage brings increased TERMPWR

typical application schematic



AVAILABLE OPTIONS

T_J	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†	
0°C to 125°C	TL-SCSI285KC	TL-SCSI285N	TL-SCSI285PWLE	TL-SCSI285Y

† The PW package is only available left-end taped and reeled.

description (continued)

isolation, making the device ideal for battery-powered systems. The TL-SCSI285, with internal current limiting, overvoltage protection, ESD protection, and thermal protection offers designers enhanced system protection and reliability.

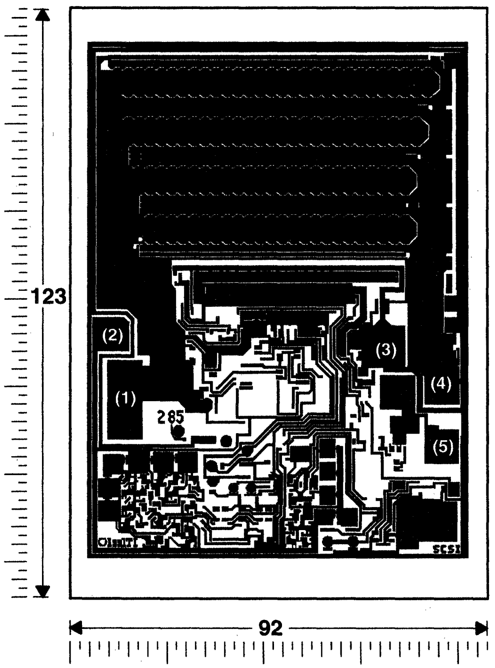
When configured as a SCSI active terminator, the TL-SCSI285 low-dropout regulator eliminates the 220-Ω and the 330-Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with 110-Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

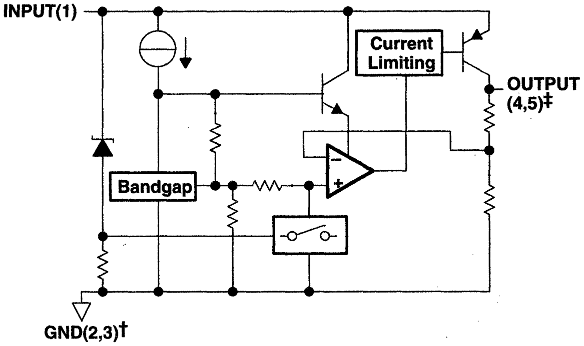
The TL-SCSI285 is characterized for operation from 0°C to 125°C virtual junction temperature.

TL-SCSI285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL-SCSI285. Thermal compression or ultrasonic bonding can be used on the doped aluminum pads. The chips can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





† Connect pads 2 and 3 together.
‡ Connect pads 4 and 5 together.

CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 7 X 7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I	7.5 V
Continuous total dissipation (see Note 1)	See Dissipation Rating Table
Operating virtual junction temperature range, T_A	−55°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	T_C	20000 mW	182.0 mW/°C†	11810 mW	9080 mW	1800 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

† Derate above 40°C

MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE

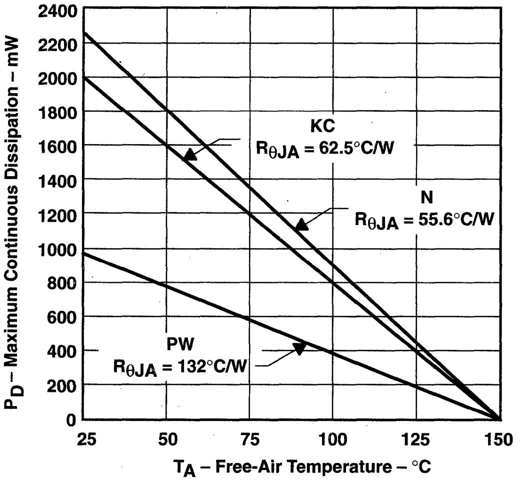


Figure 1

MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE

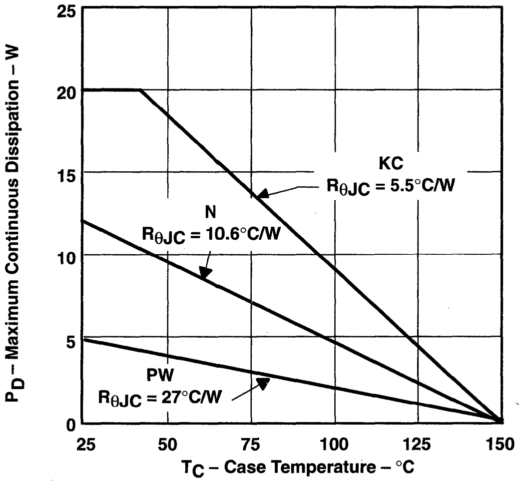


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		3.55	5.5	V
Output current, I_O	KC and N packages	0	620	mA
	PW package	0	500	
Operating virtual junction temperature range, T_J		0	125	°C

electrical characteristics, V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL-SCSI285KC TL-SCSI285N MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.55 V to 5.5 V, T_J = 25°C	2.82	2.85	2.88	V
	I_O = 500 mA to 620 mA, V_I = 3.65 V to 5.5 V, T_J = 0 to 125°C	2.79		2.91	
Input regulation	V_I = 3.55 V to 5.5 V		5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}		−62		dB
Output regulation	I_O = 20 mA to 620 mA		5	30	mV
	I_O = 20 mA to 500 mA		5	30	
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Dropout voltage	I_O = 500 mA			0.7	V
	I_O = 620 mA			0.8	
Bias current	I_O = 0		2	5	mA
	I_O = 27 mA, equivalent 1 line asserted		3	6	
	I_O = 500 mA, equivalent 18 lines asserted (8 bit)		26	49	
	I_O = 620 mA		37	62	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22.0-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

electrical characteristics, V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL-SCSI285PW MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.55 V to 5.5 V	T_J = 25°C	2.82	2.85	2.88	V
		T_J = 0 to 125°C	2.79		2.91	
Input regulation	V_I = 3.55 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}			−62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 500 mA				0.7	V
Bias current	I_O = 0			2	5	mA
	I_O = 27 mA, equivalent 1 line asserted			3	6	
	I_O = 500 mA, equivalent 18 lines asserted (8 bit)			26	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22.0-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

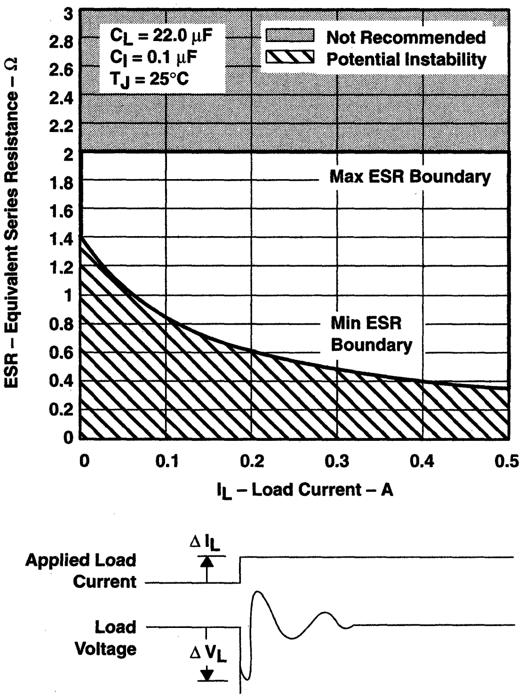
electrical characteristics, V_I = 4.5 V, I_O = 500 mA, T_J = 25°C

PARAMETER	TEST CONDITIONS†	TL-SCSI285Y MIN	TL-SCSI285Y TYP	TL-SCSI285Y MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.55 V to 5.5 V		2.85		V
Input regulation	V_I = 3.55 V to 5.5 V		5		mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}		−62		dB
Output regulation	I_O = 20 mA to 620 mA		5		mV
	I_O = 20 mA to 500 mA		5		
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 0		2		mA
	I_O = 27 mA, equivalent 1 line asserted		3		
	I_O = 500 mA, equivalent 18 lines asserted (8 bit)		26		
	I_O = 620 mA		37		

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22.0-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

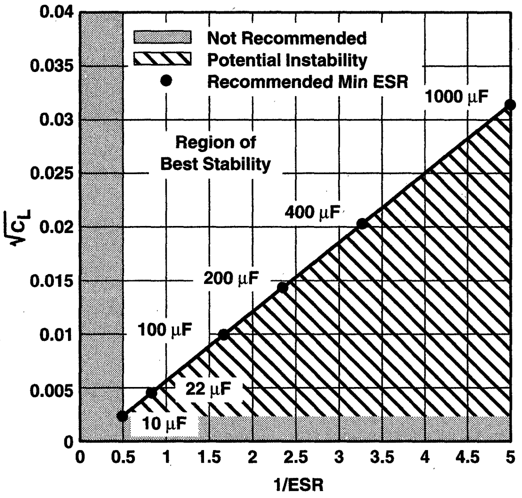
COMPENSATION CAPACITOR SELECTION INFORMATION

The TL-SCSI285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can establish the capacitance value and ESR range for best regulator performance.



ESR OF OUTPUT CAPACITOR
vs
LOAD CURRENT

Figure 3



STABILITY
vs
ESR

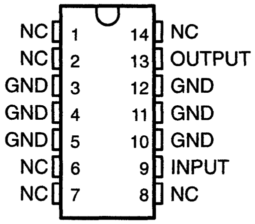
Figure 4

TL2217-285, TL2217-285Y
FIXED-VOLTAGE REGULATORS FOR SCSI ACTIVE TERMINATION

SLVS066C – NOVEMBER 1991 – REVISED AUGUST 1995

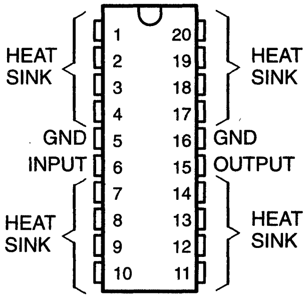
- **Fully Matches Parameters for Alternative 2 SCSI Active Termination**
- **Fixed 2.85-V Output**
- **±1.5% Maximum Output Tolerance at $T_J = 25°$**
- **1-V Maximum Dropout Voltage**
- **500-mA Output Current**
- **±3% Absolute Output Variation**
- **Internal Overcurrent Limiting**
- **Internal Thermal Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



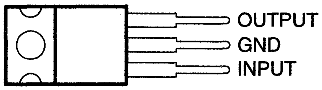
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded or electrically isolated.

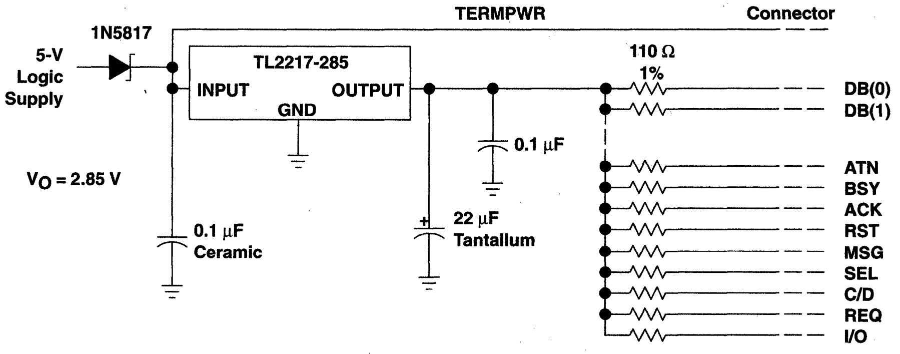
KC PACKAGE
(TOP VIEW)



description

The TL2217-285 is a low-dropout (1-V) fixed-voltage regulator specifically designed for small computer systems interface (SCSI) alternative 2 active signal termination. The TL2217-285 1-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the ±1.5% initial tolerance on its 2.85-V output voltage ensures a tighter line driver current tolerance, thereby increasing system noise margin.

typical application schematic



AVAILABLE OPTIONS

T_A	PACKAGE			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†	
0°C to 125°C	TL2217-285KC	TL2217-285N	TL2217-285PWLE	TL2217-285Y

† The PW package is only available left-end taped and reeled.

description (continued)

The fixed 2.85-V output voltage of TL2217-285 supports the SCSI alternative 2 termination standard while reducing system power consumption. The 1-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL2217-285, with internal current limiting, overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

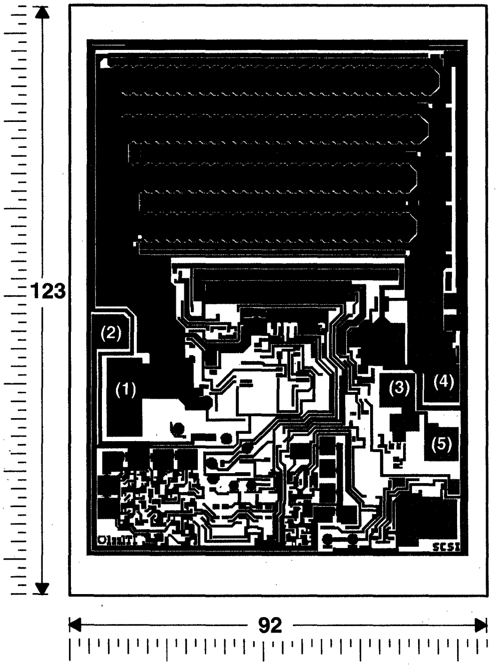
When configured as a SCSI active terminator, the TL2217-285 low-dropout regulator eliminates the 220-Ω and 330-Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with 110-Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

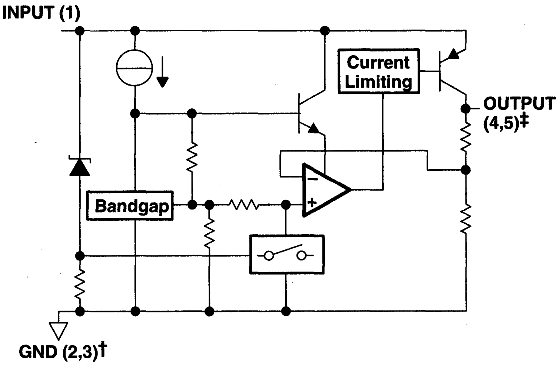
The TL2217-285 is characterized for operation from 0°C to 125°C virtual junction temperature.

TL2217-285Y chip information

These chips, properly assembled, display characteristics similar to the TL2217-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 7X7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

† Must connect pads 2 and 3 together
‡ Must connect pads 4 and 5 together

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I	7.5 V
Continuous total power dissipation (see Note 1)	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
KC	T_A	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	T_C†	20000 mW	182.0 mW/°C	14540 mW	11810 mW	4530 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

† Derate above 40°C

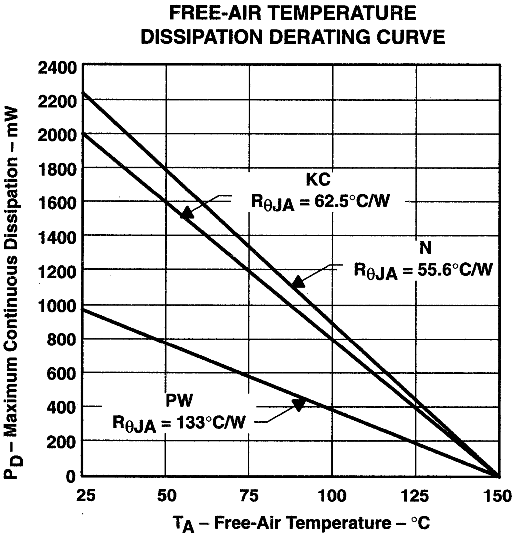

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

Figure 1

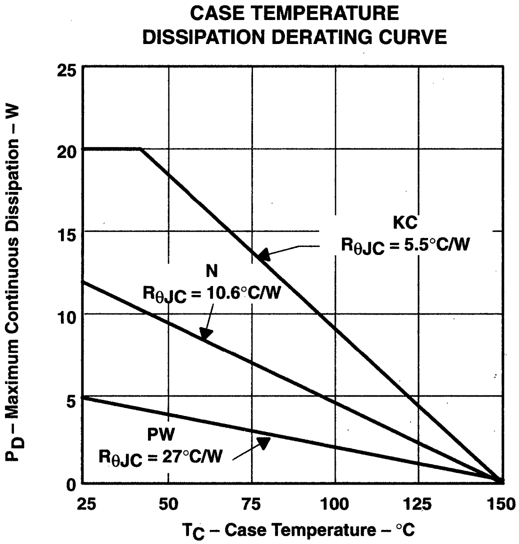

CASE TEMPERATURE
DISSIPATION DERATING CURVE

Figure 2

recommeneded operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.85	5.5	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics over recommended operating conditions, $V_I = 4.5$ V, $I_O = 500$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL2217-285			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.85 V to 5.5 V	T_J = 25°C	2.81	2.85	2.89	V
		T_J = 0°C to 125°C	2.765		2.935	
Input voltage regulation	V_I = 3.85 V to 5.5 V			5	15	mV
Ripple rejection	f = 120Hz, V_{ripple} = 1 V_{PP}			−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage					1	V
Bias current	I_O = 0			2	5	mA
	I_O = 27 mA, equivalent 1 line asserted			3	6	
	I_O = 500 mA, equivalent 18 lines asserted (8 bit)			26	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

electrical characteristics over recommended operating conditions, $V_I = 4.5$ V, $I_O = 500$ mA, $T_J = 25°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL2217-285Y			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.85 V to 5.5 V	2.81	2.85	2.89	V
Input voltage regulation	V_I = 3.85 V to 5.5 V		5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}		−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA		5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Dropout voltage	I_O = 500 mA			1	V
Bias current	I_O = 0		2	5	mA
	I_O = 27 mA, equivalent 1 line asserted		3	6	
	I_O = 500 mA, equivalent 18 lines asserted (8 bit)		26	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TL2217-285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

ESR (OUTPUT CAPACITOR)
vs
LOAD CURRENT

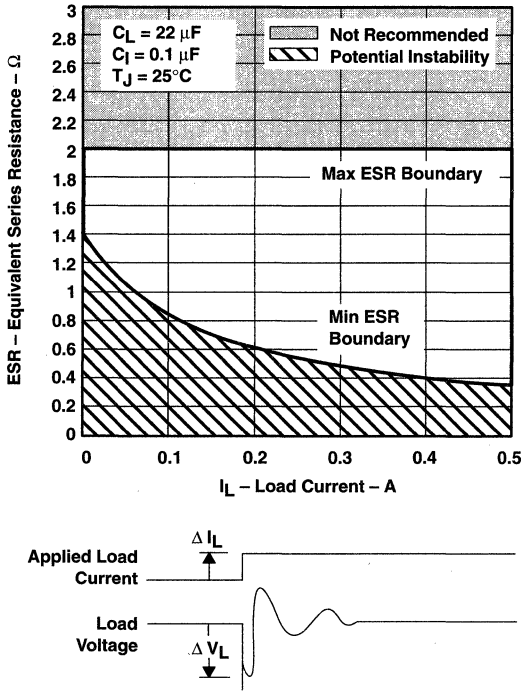


Figure 3

STABILITY
vs
ESR

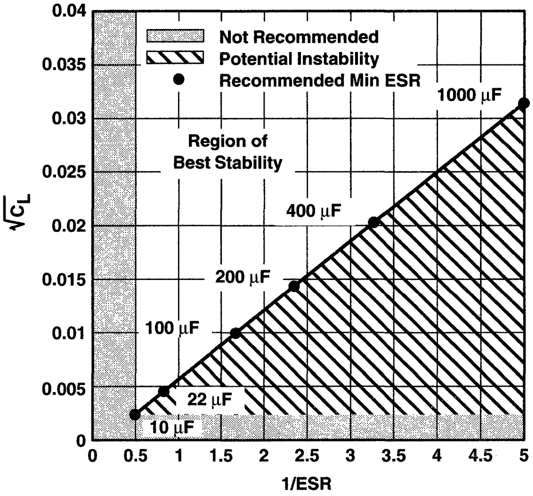


Figure 4

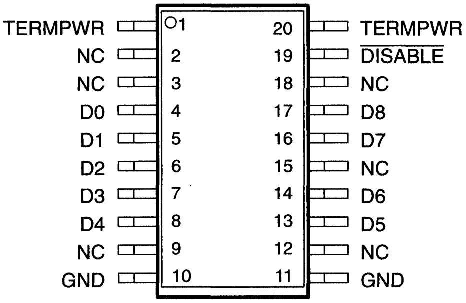
TL2218-285, TL2218-285Y
EXCALIBUR CURRENT-MODE SCSI TERMINATOR

SLVS072C – DECEMBER 1992 – REVISED OCTOBER 1995

available features

- **Fully Integrated 9-Channel SCSI Termination**
- **No External Components Required**
- **Maximum Allowed Current Applied at First High-Level Step**
- **6-pF Typical Power-Down Output Capacitance**
- **Wide V_{term}† (Termination Voltage) Operating Range, 3.5 V to 5.5 V**
- **TTL-Compatible Disable Feature**
- **Compatible With Active Negation**
- **Thermal Regulation**

PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL2218-285 is a current-mode 9-channel monolithic terminator specially designed for single-ended small-computer-systems-interface (SCSI) bus termination. A user-controlled disable function is provided to reduce standby power. No impedance-matching resistors or other external components are required for its operation as a complete terminator.

The device operates over a wide termination-voltage (V_{term}†) range of 3.5 V to 5.5 V, offering an extra 0.5 V of operating range when compared to the minimum termination voltage of 4 V required by other integrated active terminators. The TL2218-285 functions as a current-sourcing terminator and supplies a constant output current of 23 mA into each asserted line. When a line is deasserted, the device senses the rising voltage level and begins to function as a voltage source, supplying a fixed output voltage of 2.85 V. The TL2218-285 features compatibility with active negation drivers and has a typical sink current capability of 20 mA.

The TL2218-285 is able to ensure that maximum current is applied at the first high-level step. This performance means that the device should provide a first high-level step exceeding 2 V even at a 10-MHz rate. Therefore, noise margins are improved considerably above those provided by resistive terminators.

A key difference between the TL2218-285 current-mode terminator and a Boulay terminator is that the TL2218-285 does not incorporate a low dropout regulator to set the output voltage to 2.85 V. In contrast with the Boulay termination concept, the accuracy of the 2.85 V is not critical with the current-mode method used in the TL2218-285 because this voltage does not determine the driver current. Therefore, the primary device specifications are not the same as with a voltage regulator but are more concerned with output current.

The $\overline{\text{DISABLE}}$ terminal is TTL compatible and must be taken low to shut down the outputs. The device is normally active, even when $\overline{\text{DISABLE}}$ is left floating. In the disable mode, only the device startup circuits remain active, thereby reducing the supply current to just 500 μA. Output capacitance in the shutdown mode is typically 6 pF.

The TL2218-285 has on-board thermal regulation and current limiting, thus eliminating the need for external protection circuitry. A thermal regulation circuit that is designed to provide current limiting, rather than an actual thermal shutdown, is included in the individual channels of the TL2218-285. When a system fault occurs that leads to excessive power dissipation by the terminator, the thermal regulation circuit causes a reduction in the asserted-line output current sufficient to maintain operation. This feature allows the bus to remain active during a fault condition, which permits data transfer immediately upon removal of the fault. A terminator with thermal shutdown does not allow for data transfer until sufficient cooling has occurred. Another advantage offered by the TL2218-285 is a design that does not require costly laser trimming in the manufacturing process.

The TL2218-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

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† This symbol is not presently listed within EIA/JEDEC standards for letter symbols.

AVAILABLE OPTIONS

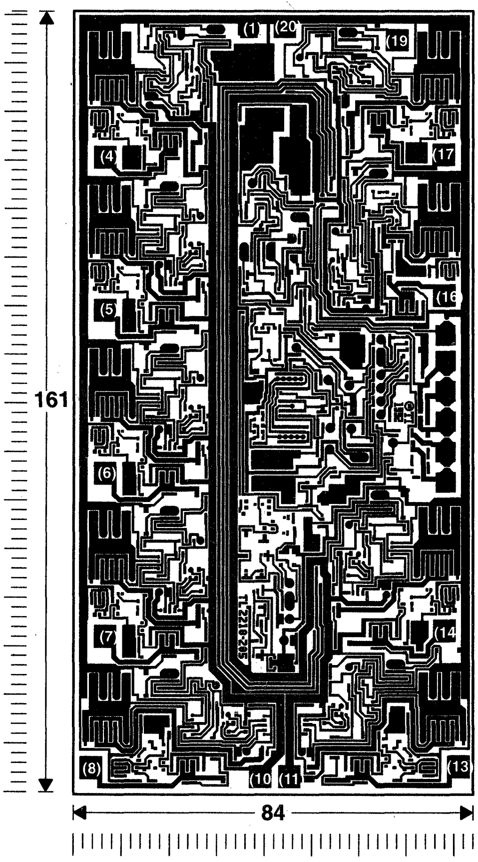
T_J	SURFACE MOUNT (PW)†	CHIP FORM (Y)
0°C to 125°C	TL2218-285PWLE	TL2218-285Y

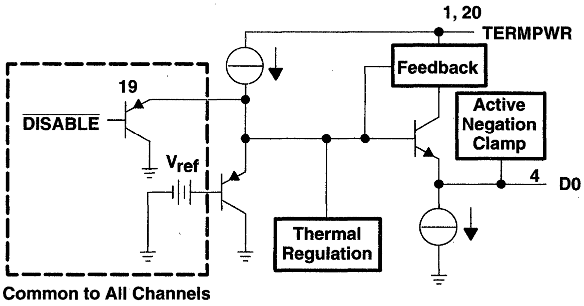
† The PW package is only available left-end taped and reeled.

TL2218-285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2218-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL

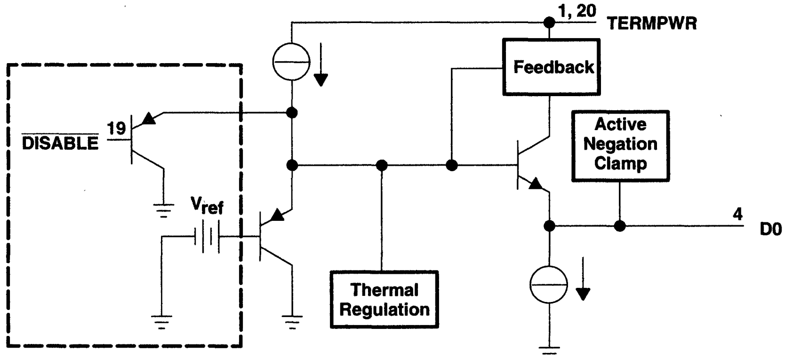
BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

functional block diagram (each channel)



Common to All Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Figures 1, 2, and 3)†

Continuous termination voltage	10 V
Continuous output voltage range	0 V to 5.5 V
Continuous disable voltage range	0 V to 5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−55°C to 150°C
Storage temperature range, T_{stg}	−60°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	166 mW
	T_C	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	T_L‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

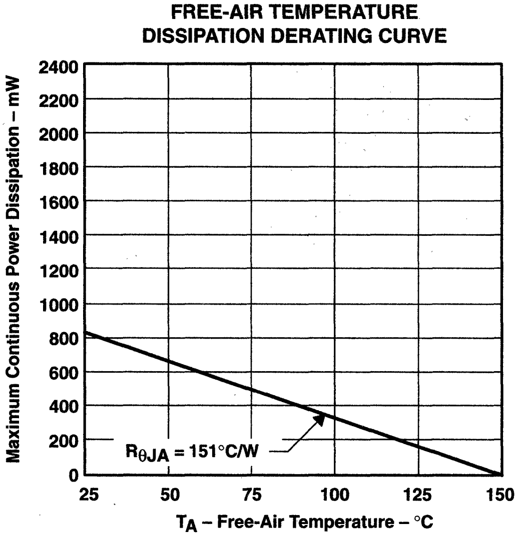


Figure 1

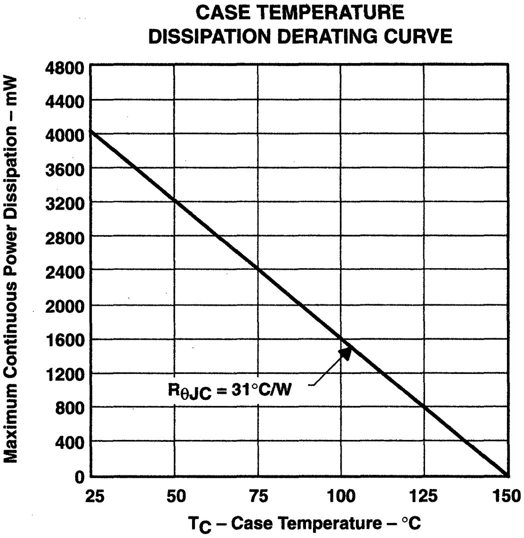


Figure 2

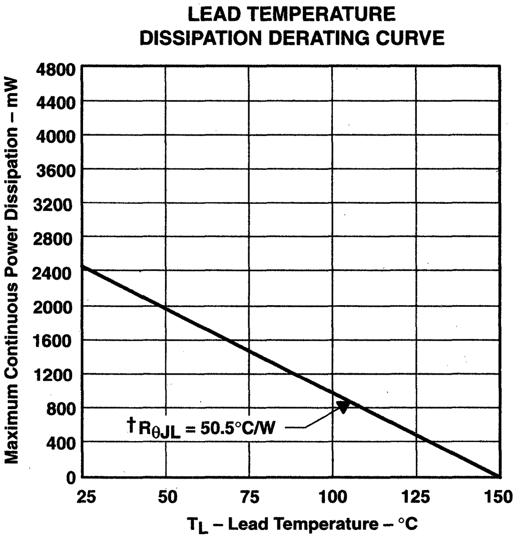


Figure 3

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† $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device, and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

recommended operating conditions

	MIN	MAX	UNIT
Termination voltage	3.5	5.5	V
High-level disable input voltage, V_{IH}	2	V_{term}	V
Low-level disable input voltage, V_{IL}	0	0.8	V
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics, V_{term} = 4.75 V, V_O = 0.5 V, T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage		2.5	2.85		V
TERMPWR supply current	All data lines open		9		mA
	All data lines = 0.5 V		228		
	$\overline{\text{DISABLE}}$ = 0 V		500		µA
Output current		−20.5	−23	−24	mA
Disable input current (see Note 1)	$\overline{\text{DISABLE}}$ = 4.75 V			1	µA
	$\overline{\text{DISABLE}}$ = 0 V			600	
Output leakage current	$\overline{\text{DISABLE}}$ = 0 V		100		nA
Output capacitance, device disabled	V_O = 0 V, 1 MHz		6		pF
Termination sink current, total	V_O = 4 V		20		mA

NOTE 1: When $\overline{\text{DISABLE}}$ is open or high, the terminator is active.

THERMAL INFORMATION

The need for smaller surface-mount packages for use on compact printed-wiring boards (PWB) causes an increasingly difficult problem in the area of thermal dissipation. In order to provide the systems designer with a better approximation of the junction temperature rise in the thin-shrink small-outline package (TSSOP), the junction-to-lead thermal resistance ($R_{\theta JL}$) is provided along with the more typical values of junction-to-ambient and junction-to-case thermal resistances, $R_{\theta JA}$ and $R_{\theta JC}$.

$R_{\theta JL}$ is used to calculate the device junction temperature rise measured from the leads of the unit. Consequently, the junction temperature is dependent upon the board temperature at the leads, $R_{\theta JL}$, and the internal power dissipation of the device. The board temperature is contingent upon several variables, including device packing density, thickness, material, area, and number of interconnects. The $R_{\theta JL}$ value depends on the number of leads connecting to the die-mount pad, the lead-frame alloy, area of the die, mount material, and mold compound. Since the power level at which the TSSOP can be used is highly dependent upon both the temperature rise of the PWB and the device itself, the systems designer can maximize this level by optimizing the circuit board. The junction temperature of the device can be calculated using the equation $T_J = (P_D \times R_{\theta JL}) + T_L$ where T_J = junction temperature, P_D = power dissipation, $R_{\theta JL}$ = junction-to-lead thermal resistance, and T_L = board temperature at the leads of the unit.

The values of thermal resistance for the TL2218-285 PW are as follows:

Thermal Resistance	Typical Junction Rise
$R_{\theta JA}$	151°C/W
$R_{\theta JC}$	31 °C/W
$R_{\theta JL}$	50.5°C/W

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_O	Output current	vs Input voltage	4
V_O	Output voltage	vs Input voltage	5
I_O	Output current	vs Junction temperature	6
V_O	Output voltage	vs Junction temperature	7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
INPUT VOLTAGE

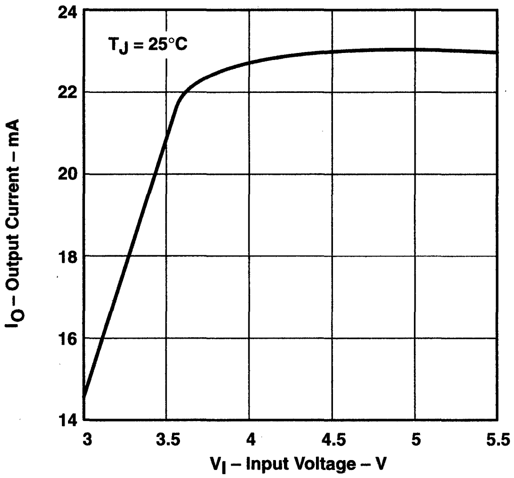


Figure 4

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

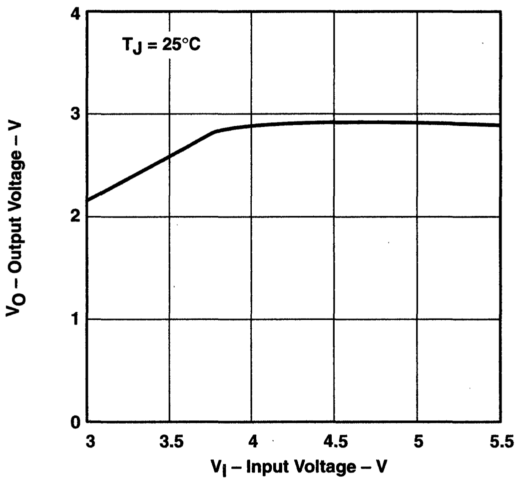


Figure 5

OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

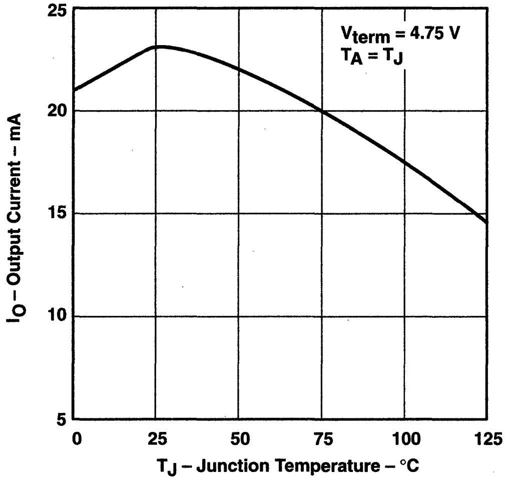


Figure 6

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

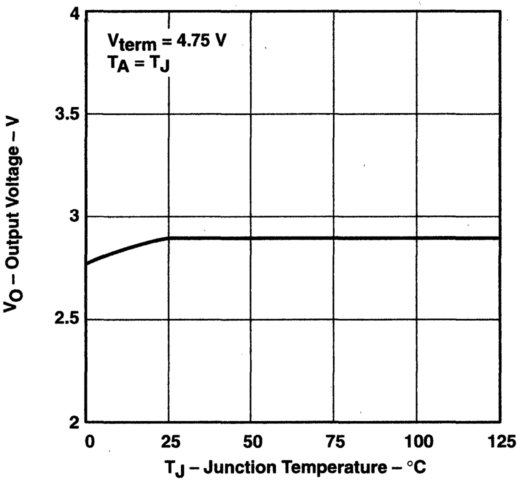


Figure 7

TLE2425, TLE2425Y
PRECISION VIRTUAL GROUNDS

SLOS065B – MARCH 1991 – REVISED AUGUST 1995

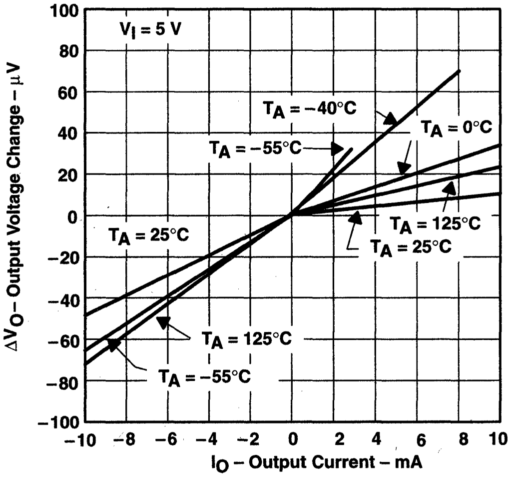
- **2.5-V Virtual Ground for 5-V/GND Analog Systems**
- **Self-Contained in Small-Outline, Dual-In-Line or 3-Terminal TO-226AA Packages**
- **High Output-Current Capability Sink or Source . . . 20 mA Typ**
- **Micropower Operation . . . 170 µA Typ,**
- **Excellent Regulation Characteristics**
  - **Output Regulation**
    −45 µV Typ at I_O = 0 to −10 mA
    +15 µV Typ at I_O = 0 to +10 mA
  - **Input Regulation = 1.5 µV/V Typ**
- **Low-Impedance Output . . . 0.0075 Ω Typ**
- **Macromodel Included**

description

In signal-conditioning applications using a single power source, a reference voltage is required for termination of all signal grounds. To accomplish this, engineers have typically used solutions consisting of resistors, capacitors, operational amplifiers, and voltage references. Texas Instruments has eliminated all of those components with one easy-to-use 3-terminal device. That device is the TLE2425 precision virtual ground.

Use of the TLE2425 over other typical circuit solutions gives the designer increased dynamic signal range, improved signal-to-noise ratio, lower distortion, improved signal accuracy, and easier interfacing to ADCs and DACs. These benefits are the result of combining a precision micropower voltage reference and a high-performance precision operational amplifier in a single silicon chip. It is the precision and performance of these two circuit functions together that yield such dramatic system-level performance.

OUTPUT REGULATION



The TLE2425 improves input regulation as well as output regulation and, in addition, reduces output impedance and power dissipation in a majority of virtual-ground-generation circuits. Both input regulation and load regulation exceed 12 bits of accuracy on a single 5-V system. Signal-conditioning front ends of data acquisition systems that push 12 bits and beyond can use the TLE2425 to eliminate a major source of system error.

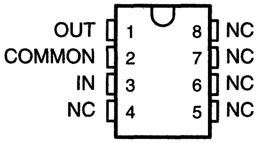
The TLE2425C is characterized for operation from 0°C to 70°C. The TLE2425I is characterized for operation from −40°C to 85°C. The TLE2425M is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC TO-226AA (LP)	
0°C to 70°C	TLE2425CD	—	TLE2425CD	TLE2425Y
−40°C to 85°C	TLE2425ID	—	TLE2425ID	—
−55°C to 125°C	TLE2425MD	TLE2425MD	TLE2425MD	—

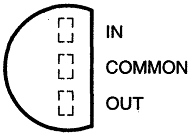
† The D and LP packages are available taped and reeled in the commercial temperature range only. Add R suffix to the device type (e.g., TLE2425CDR). The chip form is tested at 25°C.

D, OR JG PACKAGE (TOP VIEW)



NC – No internal connection

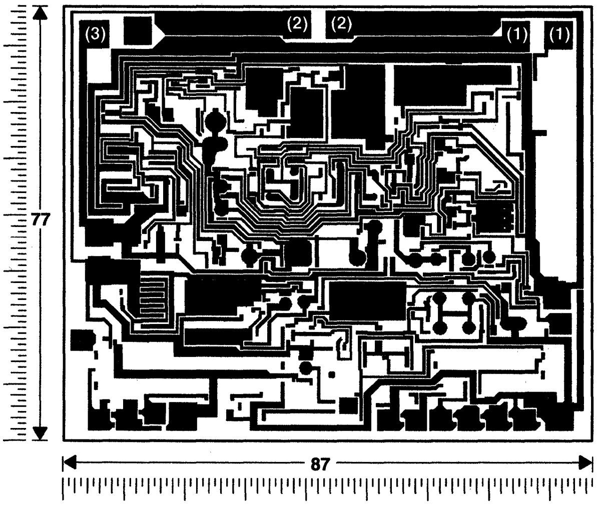
LP PACKAGE (TOP VIEW)

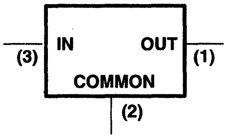


TLE2425Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2425C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_Jmax = 150°C$

TOLERANCES ARE ±10%.

ALL DIMENSIONS
ARE IN MILS.

NOTE A. NOTE: Both number 1 bonding pads and both number 2 bonding pads must be bonded out to the corresponding pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Continuous input voltage, V_I	40 V
Output current, I_O	±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mV	6.2 mW/°C	496 mW	403 mW	155 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_I = 5$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2425C			UNIT
				MIN	TYP	MAX	
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	$I_O = 0$		25°C		170	250	µA
			Full range			250	
Input voltage regulation	$V_I = 4.5$ V to 5.5 V		25°C		1.5	20	µV
			Full range			25	
	$V_I = 4$ V to 40 V		25°C		1.5	20	µV/V
			Full range			25	
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)} = 1$ V	25°C		80		dB
Output voltage regulation (source current)‡	$I_O = 0$ to −10 mA		25°C	−160	−45	160	µV
			Full range	−250		250	
	$I_O = 0$ to −20 mA		25°C	−450	−150	450	
Output voltage regulation (sink current)‡	$I_O = 0$ to 10 mA		25°C	−160	15	160	µV
			Full range	−250		250	
	$I_O = 0$ to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h,	Noncumulative	25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	$V_O = 5$ V		25°C	30	55		mA
Short-circuit output current (source current)	$V_O = 0$			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		µV
Output voltage response to output current step	V_O to 0.1%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		110		µs
		$C_L = 100$ pF			115		
	V_O to 0.01%, $I_O = \pm 10$ mA	$C_L = 0$			180		
		$C_L = 100$ pF			180		
Output voltage response to input voltage step	$V_I = 4.5$ to 5.5 V,	V_O to 0.1%	25°C		12		µs
	$V_I = 4.5$ to 5.5 V,	V_O to 0.01%			30		
Output voltage turn-on response	$V_I = 0$ to 5 V,	V_O to 0.1%	25°C		125		µs
	$V_I = 0$ to 5 V,	V_O to 0.01%			210		

† Full range is 0°C to 70°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, $V_I = 5$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2425I			UNIT
				MIN	TYP	MAX	
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	$I_O = 0$		25°C		170	250	μA
			Full range			250	
Input voltage regulation	$V_I = 4.5$ V to 5.5 V		25°C		1.5	20	μV
			Full range			75	
	$V_I = 4$ V to 40 V		25°C		1.5	20	μV/V
			Full range			75	
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)} = 1$ V	25°C		80		dB
Output voltage regulation (source current)‡	$I_O = 0$ to −10 mA		25°C	−160	−45	160	μV
			Full range	−250		250	
	$I_O = 0$ to −20 mA		25°C	−450	−150	450	
Output voltage regulation (sink current)‡	$I_O = 0$ to 8 mA		25°C	−160	15	160	μV
			Full range	−250		250	
	$I_O = 0$ to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h,	Noncumulative	25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	$V_O = 5$ V		25°C	30	55		mA
Short-circuit output current (source current)	$V_O = 0$			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		110		μs
		$C_L = 100$ pF			115		
	V_O to 0.01%, $I_O = \pm 10$ mA	$C_L = 0$			180		
		$C_L = 100$ pF			180		
Output voltage response to input voltage step	$V_I = 4.5$ to 5.5 V,	V_O to 0.1%	25°C		12		μs
	$V_I = 4.5$ to 5.5 V,	V_O to 0.01%			30		
Output voltage turn-on response	$V_I = 0$ to 5 V,	V_O to 0.1%	25°C		125		μs
	$V_I = 0$ to 5 V,	V_O to 0.01%			210		

† Full range is −40°C to 85°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A†	TLE2425M			UNIT
			MIN	TYP	MAX	
Output voltage		25°C	2.48	2.5	2.52	V
		Full range	2.47		2.53	
Temperature coefficient of output voltage		25°C		20		ppm/°C
Bias current	I_O = 0	25°C		170	250	μA
		Full range			250	
Input voltage regulation	V_I = 4.5 V to 5.5 V	25°C		1.5	20	μV
		Full range			100	
	V_I = 4.5 V to 40 V	25°C		1.5	20	μV/V
		Full range			100	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V	25°C		80		dB
Output voltage regulation (source current)‡	I_O = 0 to −10 mA	25°C	−160	−45	160	μV
		Full range	−250		250	
	I_O = 0 to −20 mA	25°C	−450	−150	450	
Output voltage regulation (sink current)‡	I_O = 0 to 3 mA	25°C	−160	15	160	μV
		Full range	−250		250	
	I_O = 0 to 20 mA	25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative	25°C		15		ppm
Output impedance		25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	V_O = 5 V	25°C	30	55		mA
Short-circuit output current (source current)	V_O = 0		−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz	25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ±10 mA, C_L = 0	25°C		110		μs
	V_O to 0.1%, I_O = ±10 mA, C_L = 100 pF			115		
	V_O to 0.01%, I_O = ±10 mA, C_L = 0			180		
	V_O to 0.01%, I_O = ±10 mA, C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%	25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%	25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%			210		

† Full range is −55°C to 125°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics V_I = 5 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLE2425Y			UNIT
			MIN	TYP	MAX	
Output voltage				2.5		V
Temperature coefficient of output voltage				20		ppm/°C
Bias current	$I_O = 0$			170		µA
Input voltage regulation	V_I = 4.5 V to 5.5 V			1.5		µV
	V_I = 4 V to 40 V			1.5		µV/V
Ripple rejection	f = 120 Hz,	$\Delta V_{I(PP)}$ = 1 V		80		dB
Output voltage regulation (source current)†	I_O = 0 to –10 mA			–45		µV
	I_O = 0 to –20 mA			–150		
Output voltage regulation (sink current)†	I_O = 0 to 10 mA			15		µV
	I_O = 0 to 20 mA			65		
Output impedance				7.5		mΩ
Short-circuit output current (sink current)	V_O = 5 V			55		mA
Short-circuit output current (source current)	$V_O = 0$			–50		
Output noise voltage, rms	f = 10 Hz to 10 kHz			100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ±10 mA	$C_L = 0$		110		µs
		C_L = 100 pF		115		
	V_O to 0.01%, I_O = ±10 mA	$C_L = 0$		180		
		C_L = 100 pF		180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V,	V_O to 0.1%		12		µs
	V_I = 4.5 to 5.5 V,	V_O to 0.01%		30		
Output voltage turn-on response	V_I = 0 to 5 V,	V_O to 0.1%		125		µs
	V_I = 0 to 5 V,	V_O to 0.01%		210		

† Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table Of Graphs

		FIGURE
Output voltage	Distribution	1
	vs Free-air temperature	2
Output voltage hysteresis	vs Free-air temperature	3
Input bias current	vs Input voltage	4
	vs Free-air temperature	5
Input voltage regulation		6
Ripple rejection	vs Frequency	7
Output voltage regulation		8
Output impedance	vs Frequency	9
Short-circuit output current	vs Free-air temperature	10
Spectral noise voltage density	vs Frequency	11
Wide-band noise voltage	vs Frequency	12
Output voltage change with current step	vs Time	13
Output voltage change with voltage step	vs Time	14
Output voltage power-up response	vs Time	15
Output current	vs Load capacitance	16

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF OUTPUT VOLTAGE

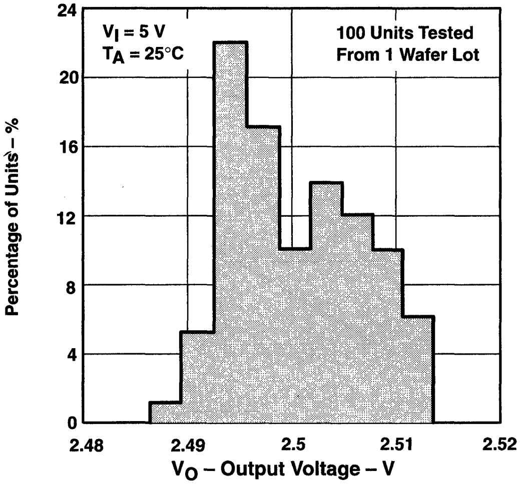


Figure 1

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

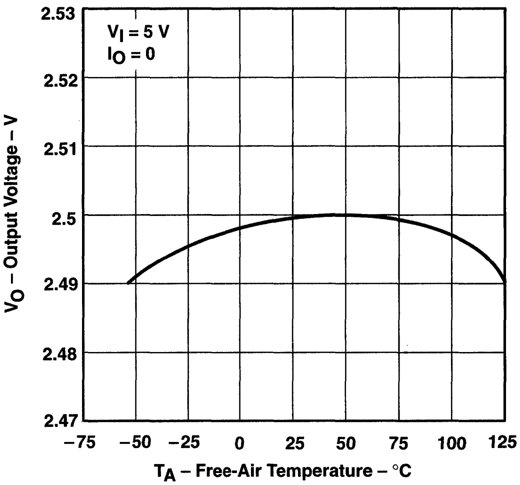


Figure 2

OUTPUT VOLTAGE HYSTERESIS vs FREE-AIR TEMPERATURE

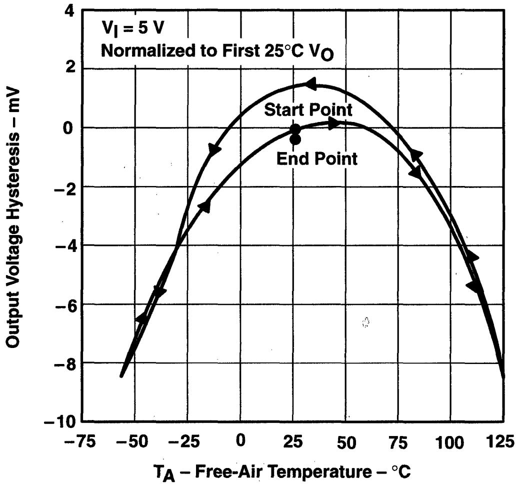


Figure 3

INPUT BIAS CURRENT vs INPUT VOLTAGE

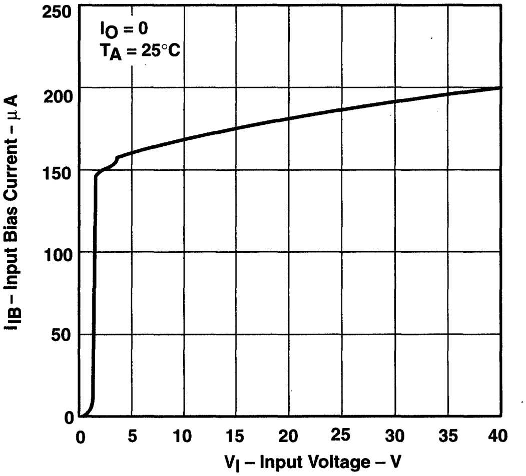


Figure 4

---

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

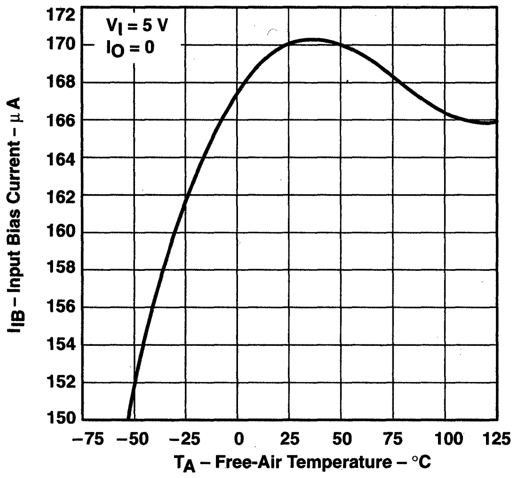


Figure 5

INPUT VOLTAGE REGULATION

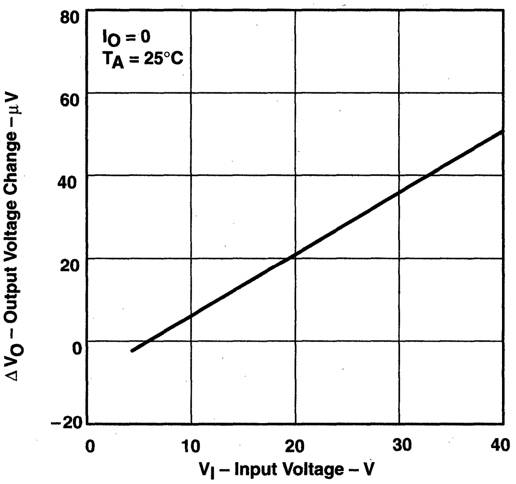


Figure 6

RIPPLE REJECTION
vs
FREQUENCY

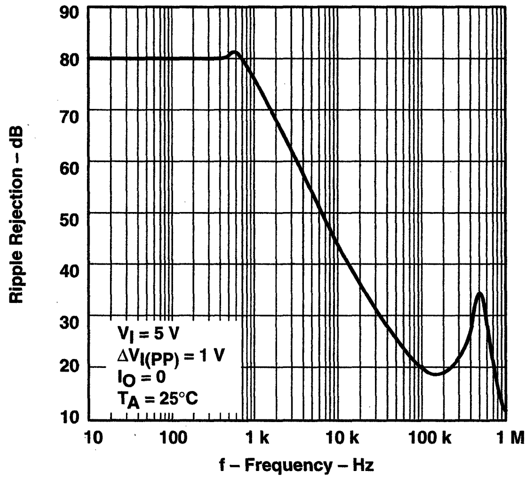


Figure 7

OUTPUT VOLTAGE REGULATION

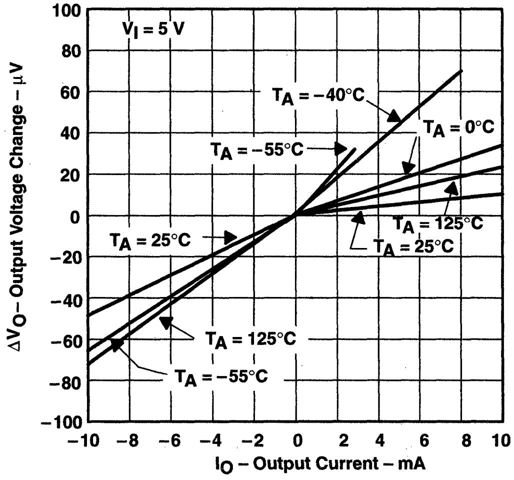


Figure 8

---

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

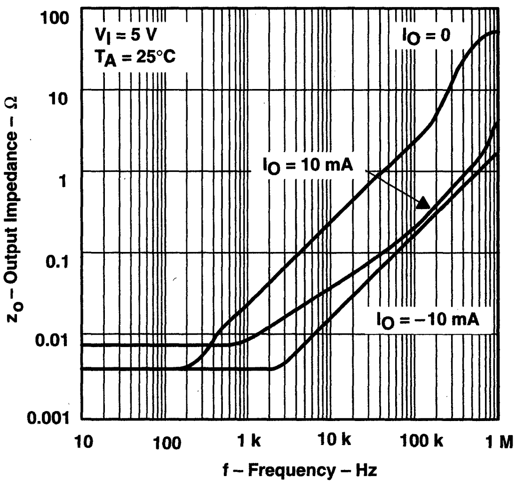


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

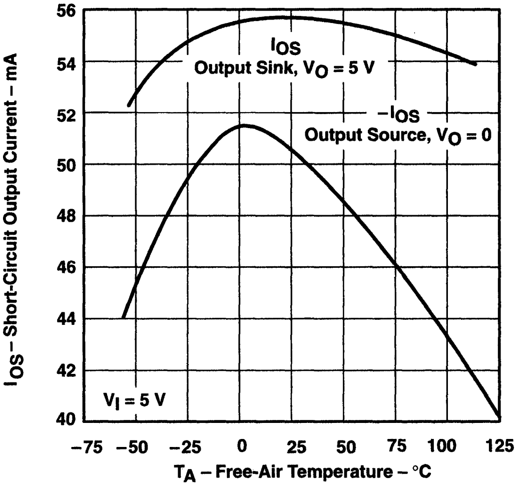


Figure 10

SPECTRAL NOISE VOLTAGE DENSITY
vs
FREQUENCY

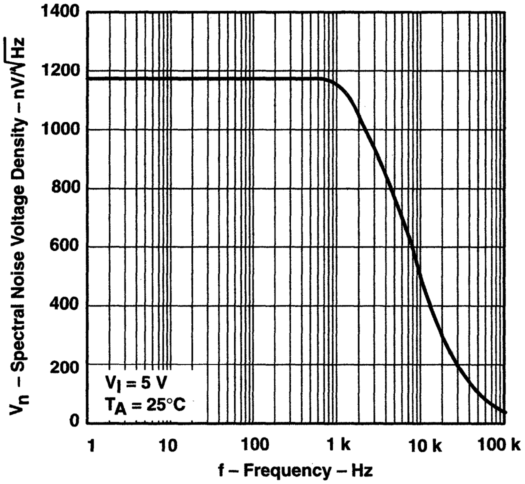


Figure 11

WIDE-BAND NOISE VOLTAGE
vs
FREQUENCY

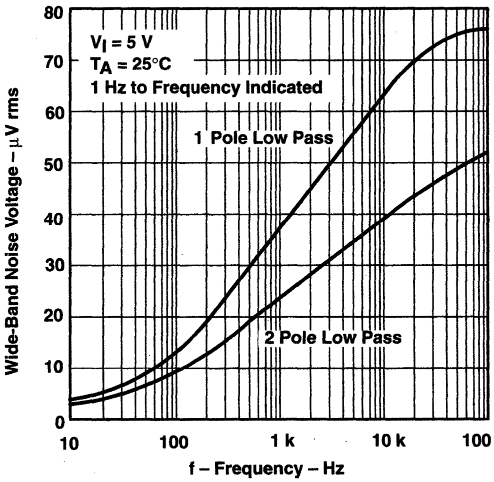


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE TO OUTPUT CURRENT STEP
vs
TIME

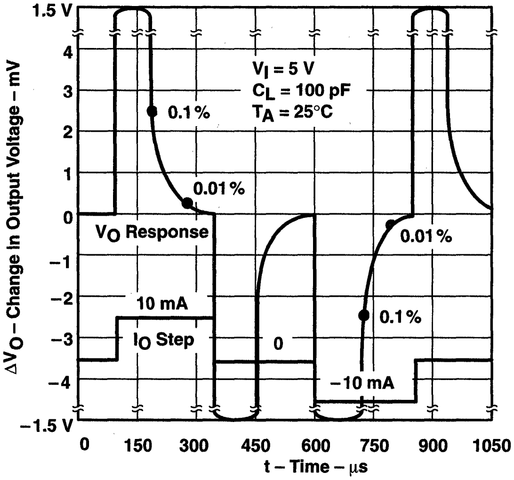


Figure 13

OUTPUT VOLTAGE RESPONSE TO INPUT VOLTAGE STEP
vs
TIME

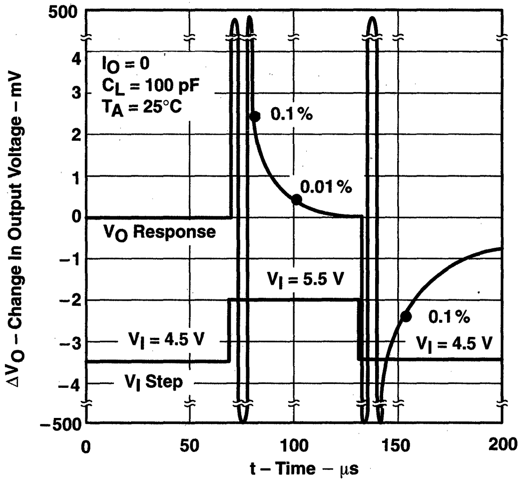


Figure 14

OUTPUT VOLTAGE POWER-UP RESPONSE
vs
TIME

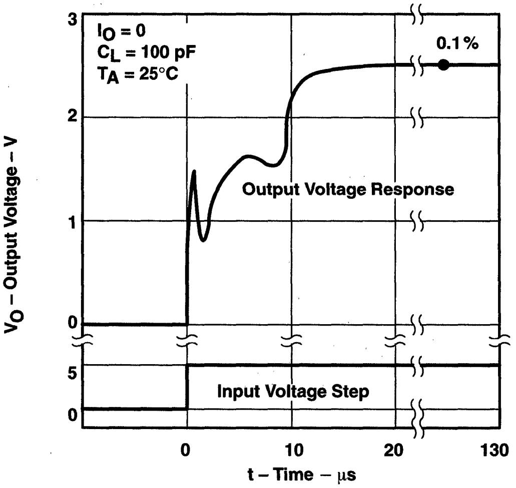


Figure 15

STABILITY RANGE
OUTPUT CURRENT
vs
LOAD CAPACITANCE

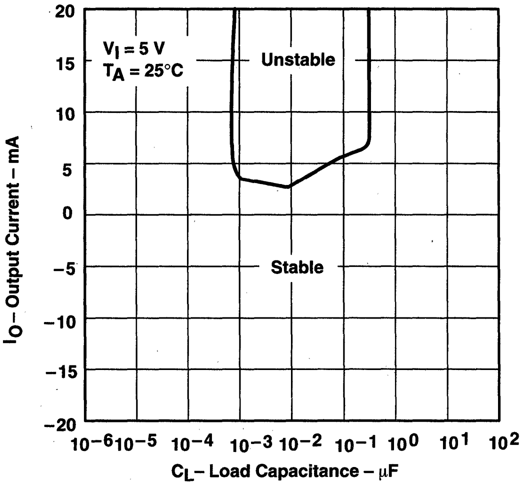


Figure 16

macromodel information

```
*   TLE2425 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
*   CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
*   REV (N/A)     SUPPLY VOLTAGE: 5 V
*   CONNECTIONS: INPUT
*                |   COMMON
*                |   |   OUTPUT
*                |   |   |
.SUBCKT TLE2425  3   4   5
*
```

```
*   OPAMP SECTION
    C1     11 12  21.66E-12
    C2      6 7   30.00E-12
    C3     87 0   10.64E-9
    CPSR   85 86  15.9E-9
    DCM+   81 82  DX
    DCM-   83 81  DX
    DC      5 53  DX
    DE     54 5   DX
    DLN    92 90  DX
    DLP    90 91  DX
    DP      4 3   DX
    ECMR   84 99  (2,99) 1
    EGND   99 0   POLY(2)    (3,0)  (4,0)  0   .5  .5
    EPSR   85 0   POLY(1)    (3,4)  -16.22E-6 3.24E-6
    ENSE   89 2   POLY(1)    (88,0) 120E-6 1
    FB      7 99  POLY(6)    VB  VC  VE  VLP VLN VPSR   0   74.8E6 -10E6  10E6   10E6
+   -10E6  74E6
    GA      6 0   11  12  320.4E-6
    GCM     0 6   10  99  1.013E-9
    GPSR   85 86  (85,86)    100E-6
    GRC1   4   11 (4,11) 3.204E-4
    GRC2   4   12 (4,12) 3.204E-4
    GRE1   13 10  (13,10)    1.038E-3
    GRE2   14 10  (14,10)    1.038E-3
    HLIM   90 0   VLIM   1K
    HCMR   80 1   POLY(2)    VCM+   VCM-   0   1E2 1E2
    IRP     3 4   146E-6
    IEE     3 10  DC  24.05E-6
    IIO     2 0   .2E-9
    I1     88 0   1E-21
    Q1     11 89  13  QX
    Q2     12 80  14  QX
    R2      6 9   100.0E3
    RCM    84 81  1K
    REE    10 99  8.316E6
    RN1    87 0   2.55E8
    RN2    87 88  11.67E3
```

macromodel information (continued)

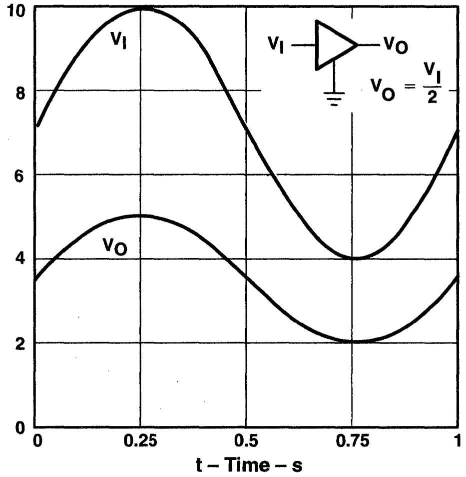
```
   RO1      8  5   63
   RO2      7  99  62
   VCM+    82  99  1.0
   VCM-    83  99  -2.3
   VB       9  0   DC  0
   VC       3  53  DC  1.400
   VE      54  4   DC  1.400
   VLIM     7  8   DC  0
   VLP     91  0   DC  30
   VLN      0  92  DC  30
   VPSR     0  86  DC  0
   RFB      5  2   1K
   RIN     30  1   1K
   RCOM    34  4   .1
*REGULATOR SECTION
   RG1     30  0   20MEG
   RG2     30  31  .2
   RG3     31  35  400K
   RG4     35  34  411K
   RG5     31  36  25MEG
   HREG    31  32  POLY(2)    VPSET  VNSET  0   1E2 1E2
   VREG    32  33  DC  0V
   EREG    33  34  POLY(1)    (36,34)    1.23 1
   VADJ    36  34  1.27V
   HPSET   37  0   VREG   1.030E3
   VPSET   38  0   DC  20V
   HNSET   39  0   VREG   6.11E5
   VNSET   40  0   DC  -20V
   DSUB     4  34  DX
   DPOS    37  38  DX
   DNNEG   40  39  DX
.MODEL DX  D(IS=800.0E-18)
.MODEL QX  PNP(IS=800.0E-18 BF=480)
.ENDS
```

TLE2426, TLE2426Y
THE “RAIL SPLITTER”
PRECISION VIRTUAL GROUND

SLOS098B – AUGUST 1991 – REVISED AUGUST 1995

- **1/2 V_I Virtual Ground for Analog Systems**
- **Self-Contained 3-terminal TO-226AA Package**
- **Micropower Operation . . . 170 μA Typ, V_I = 5 V**
- **Wide V_I Range . . . 4 V to 40 V**
- **High Output-Current Capability**
  - **Source . . . 20 mA Typ**
  - **Sink . . . 20 mA Typ**
- **Excellent Output Regulation**
  - **−45 μV Typ at I_O = 0 to −10 mA**
  - **+15 μV Typ at I_O = 0 to +10 mA**
- **Low-Impedance Output . . . 0.0075 Ω Typ**
- **Noise Reduction Pin (D, JG, and P Packages Only)**

INPUT/OUTPUT TRANSFER CHARACTERISTICS



description

In signal-conditioning applications utilizing a single power source, a reference voltage equal to one-half the supply voltage is required for termination of all analog signal grounds. Texas Instruments introduces a precision virtual ground whose output voltage is always equal to one-half the input voltage, the TLE2426 “rail splitter.”

The unique combination of a high-performance, micropower operational amplifier and a precision-trimmed divider on a single silicon chip results in a precise V_O/V_I ratio of 0.5 while sinking and sourcing current. The TLE2426 provides a low-impedance output with 20 mA of sink and source capability while drawing less than 280 μA of supply current over the full input range of 4 V to 40 V. A designer need not pay the price in terms of board space for a conventional signal ground consisting of resistors, capacitors, operational amplifiers, and voltage references. The performance and precision of the TLE2426 is available in an easy-to-use, space saving, 3-terminal LP package. For increased performance, the optional 8-pin packages provide a noise-reduction pin. Wtih the addition of an external capacitor (C_{NR}), peak-to-peak noise is reduced while line ripple rejection is improved.

Initial output tolerance for a single 5-V or 12-V system is better than 1% with 3.6% over the full 40-V input range. Ripple rejection exceeds 12 bits of accuracy. Whether the application is for a data acquisition front end, analog signal termination, or simply a precision voltage reference, the TLE2426 eliminates a major source of system error.

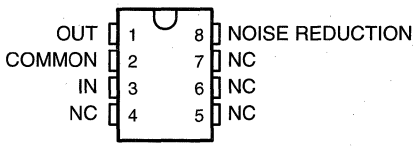
The C-suffix devices are characterized for operation from 0°C to 70°C. The I suffix devices are characterized for operation from −40°C to 85°C. The M suffix devices are characterized over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

	PACKAGED DEVICES				CHIP FORM (Y)
T_A	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC (LP)	PLASTIC DIP (P)	
0°C to 70°C	TLE2426CD	—	TLE2426CLP	TLE2426CP	TLE2426Y
−40°C to 85°C	TLE2426ID	—	TLE2426ILP	TLE2426IP	
−55°C to 125°C	TLE2426MD	TLE2426MJG	TLE2426MLP	TLE2426MP	

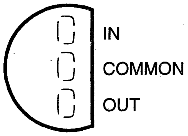
The D and LP packages are available taped and reeled in the commercial temperature range only. Add R suffix to the device type (e. g., TLC2426CDR). Chips are tested at 25°C.

D, JG, OR P PACKAGE
(TOP VIEW)



NC – No internal connection

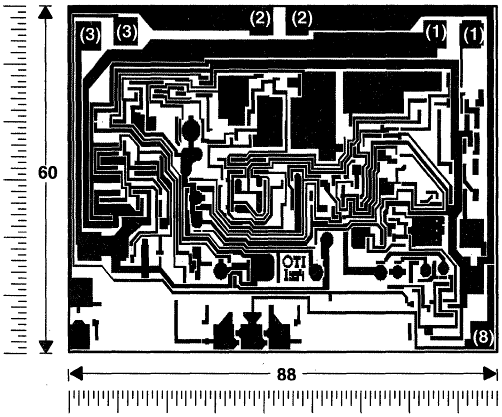
LP PACKAGE
(TOP VIEW)

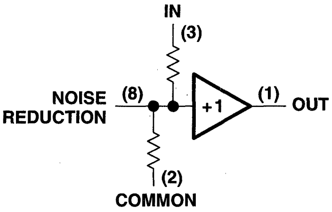


TLE2426Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2426C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NOTE A. Both bonding pads numbered 1, both numbered 2, and both numbered 3, must be bonded out to the corresponding functions pin.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Continuous input voltage, V_I	40 V
Continuous filter trap voltage	40 V
Output current, I_O	±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mV	6.2 mW/°C	496 mW	403 mW	155 mW
P	1000 mV	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_I = 5$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426C			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4$ V		25°C	1.98	2	2.02	V
	$V_I = 5$ V			2.48	2.5	2.52	
	$V_I = 40$ V			19.8	20	20.2	
	$V_I = 5$ V		Full range	2.475		2.525	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	$V_I = 5$ V	25°C		170	300	μA
		$V_I = 4$ to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	$I_O = 0$ to −10 mA		25°C		−45	±160	μV
			Full range			±250	
	$I_O = 0$ to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	$I_O = 0$ to 10 mA		25°C		15	±160	μV
			Full range			±250	
	$I_O = 0$ to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	$V_O = 5$ V	25°C	20	26		mA
	Sourcing current,	$V_O = 0$		−20	−47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	$C_{NR} = 0$	25°C		120		μV
		$C_{NR} = 1$ μF			30		
Output voltage current step response	V_O to 0.1%, $I_O = \pm10$ mA	$C_L = 0$	25°C		290		μs
		$C_L = 100$ pF			275		
	V_O to 0.01%, $I_O = \pm10$ mA	$C_L = 0$	25°C		400		
		$C_L = 100$ pF			390		
Step response	$V_I = 0$ to 5 V, V_O to 0.1%	$C_L = 100$ pF	25°C		20		μs
	$V_I = 0$ to 5 V, V_O to 0.01%				160		

† Full range is 0°C to 70°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426C MIN	TLE2426C TYP	TLE2426C MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 12 V			5.95	6	6.05	
	V_I = 40 V			19.8	20	20.2	
	V_I = 12 V		Full range	5.945		6.055	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	300	µA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to −10 mA		25°C		−45	±160	µV
			Full range			±250	
	I_O = 0 to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	µV
			Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V	25°C	20	31		mA
	Sourcing current,	V_O = 0		−20	−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		µV
		C_{NR} = 1 µF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		µs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		20		µs
	V_I = 0 to 12 V, V_O to 0.01%				120		

† Full range is 0°C to 70°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, $V_I = 5$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426I			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4$ V		25°C	1.98	2	2.02	V
	$V_I = 5$ V			2.48	2.5	2.52	
	$V_I = 40$ V			19.8	20	20.2	
	$V_I = 5$ V		Full range	2.47		2.53	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	$V_I = 5$ V	25°C		170	300	μA
		$V_I = 4$ to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	$I_O = 0$ to −10 mA		25°C		−45	±160	μV
			Full range			±250	
	$I_O = 0$ to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	$I_O = 0$ to 10 mA		25°C		15	±160	μV
	$I_O = 0$ to 8 mA		Full range			±250	
	$I_O = 0$ to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	$V_O = 5$ V	25°C	20	26		mA
	Sourcing current,	$V_O = 0$		−20	−47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	$C_{NR} = 0$	25°C		120		μV
		$C_{NR} = 1$ μF			30		
Output voltage current step response	V_O to 0.1%, $I_O = \pm10$ mA	$C_L = 0$	25°C		290		μs
		$C_L = 100$ pF			275		
	V_O to 0.01%, $I_O = \pm10$ mA	$C_L = 0$	25°C		400		
		$C_L = 100$ pF			390		
Step response	$V_I = 0$ to 5 V, V_O to 0.1%	$C_L = 100$ pF	25°C		20		μs
	$V_I = 0$ to 5 V, V_O to 0.01%				160		

† Full range is −40°C to 85°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, $V_I = 12$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426I			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4$ V		25°C	1.98	2	2.02	V
	$V_I = 12$ V			5.95	6	6.05	
	$V_I = 40$ V			19.8	20	20.2	
	$V_I = 12$ V		Full range	5.935		6.065	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	$V_I = 12$ V	25°C		195	300	µA
		$V_I = 4$ to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	$I_O = 0$ to −10 mA		25°C		−45	±160	µV
			Full range			±250	
	$I_O = 0$ to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	$I_O = 0$ to 10 mA		25°C		15	±160	µV
	$I_O = 0$ to 8 mA		Full range			±250	
	$I_O = 0$ to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	$V_O = 12$ V	25°C	20	31		mA
	Sourcing current,	$V_O = 0$		−20	−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	$C_{NR} = 0$	25°C		120		µV
		$C_{NR} = 1$ µF			30		
Output voltage current step response	V_O to 0.1%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		290		µs
		$C_L = 100$ pF			275		
	V_O to 0.01%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		400		
		$C_L = 100$ pF			390		
Step response	$V_I = 0$ to 12 V, V_O to 0.1%	$C_L = 100$ pF	25°C		20		µs
	$V_I = 0$ to 12 V, V_O to 0.01%				120		

† Full range is −40°C to 85°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, $V_I = 5$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426M			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4$ V		25°C	1.98	2	2.02	V
	$V_I = 5$ V			2.48	2.5	2.52	
	$V_I = 40$ V			19.8	20	20.2	
	$V_I = 5$ V		Full range	2.465		2.535	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	$V_I = 5$ V	25°C		170	300	µA
		$V_I = 4$ to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	$I_O = 0$ to −10 mA		25°C		−45	±160	µV
			Full range			±250	
	$I_O = 0$ to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	$I_O = 0$ to 10 mA		25°C		15	±160	µV
	$I_O = 0$ to 3 mA		Full range			±250	
	$I_O = 0$ to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	$V_O = 5$ V	25°C	20	26		mA
	Sourcing current,	$V_O = 0$		−20	−47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	$C_{NR} = 0$	25°C		120		µV
		$C_{NR} = 1$ µF			30		
Output voltage current step response	V_O to 0.1%, $I_O = \pm10$ mA	$C_L = 0$	25°C		290		µs
		$C_L = 100$ pF			275		
	V_O to 0.01%, $I_O = \pm10$ mA	$C_L = 0$	25°C		400		
		$C_L = 100$ pF			390		
Step response	$V_I = 0$ to 5 V, V_O to 0.1%	$C_L = 100$ pF	25°C		20		µs
	$V_I = 0$ to 5 V, V_O to 0.01%				120		

† Full range is −55°C to 125°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, $V_I = 12$ V, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426M			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4$ V		25°C	1.98	2	2.02	V
	$V_I = 12$ V			5.95	6	6.05	
	$V_I = 40$ V			19.8	20	20.2	
	$V_I = 12$ V		Full range	5.925		6.075	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	$V_I = 12$ V	25°C		195	250	µA
		$V_I = 4$ to 40 V	Full range			350	
Output voltage regulation (sourcing current)‡	$I_O = 0$ to −10 mA		25°C		−45	±160	µV
			Full range			±250	
	$I_O = 0$ to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	$I_O = 0$ to 10 mA		25°C		15	±160	µV
	$I_O = 0$ to 8 mA		Full range			±250	
	$I_O = 0$ to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	$V_O = 12$ V	25°C	20	31		mA
	Sourcing current,	$V_O = 0$		−20	−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	$C_{NR} = 0$	25°C		120		µV
		$C_{NR} = 1$ µF			30		
Output voltage current step response	V_O to 0.1%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		290		µs
		$C_L = 100$ pF			275		
	V_O to 0.01%, $I_O = \pm 10$ mA	$C_L = 0$	25°C		400		
		$C_L = 100$ pF			390		
Step response	$V_I = 0$ to 12 V, V_O to 0.1%	$C_L = 100$ pF	25°C		12		µs
	$V_I = 0$ to 12 V, V_O to 0.01%				120		

† Full range is −55°C to 125°C.

‡ Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLE2426Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5 V			2.5		V
Supply current	No load			170		µA
Output voltage regulation (sourcing current)†	I_O = 0 to –10 mA			–45		µV
	I_O = 0 to –20 mA			–150		
Output voltage regulation (sinking current)†	I_O = 0 to 10 mA			15		µV
	I_O = 0 to 20 mA			65		
Output impedance				7.5		mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current,	V_O = 5 V		26		mA
	Sourcing current,	V_O = 0		–47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF		20		µs
	V_I = 0 to 5 V, V_O to 0.01%			160		

† Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLE2426Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 12 V			6		V
Supply current	No load			195		µA
Output voltage regulation (sourcing current)†	I_O = 0 to –10 mA			–45		µV
	I_O = 0 to –20 mA			–150		
Output voltage regulation (sinking current)†	I_O = 0 to 3 mA			15		µV
	I_O = 0 to 20 mA			65		
Output impedance				7.5		mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V		31		mA
	Sourcing current,	V_O = 0		–70		
Output noise voltage, rms	f = 10 Hz to 10 kHZ	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current, step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF		12		µs
	V_I = 0 to 12 V, V_O to 0.01%			120		

† Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†

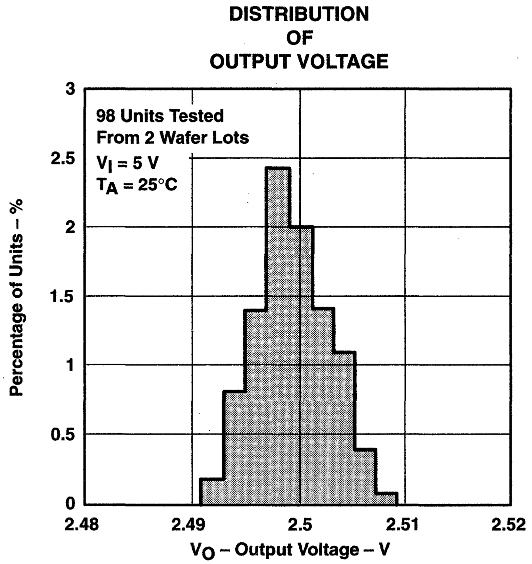

Figure 1

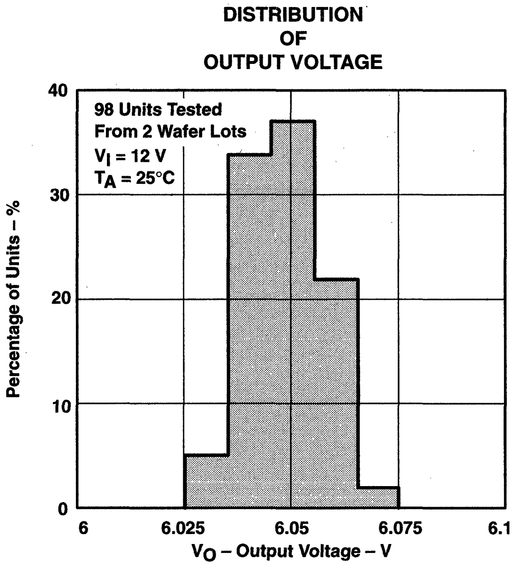

Figure 2

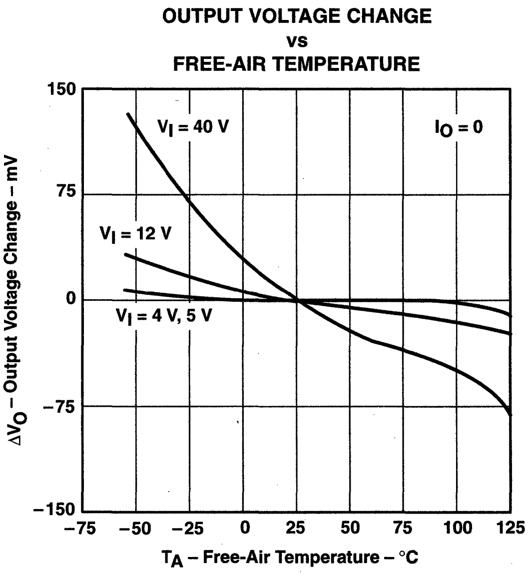

Figure 3

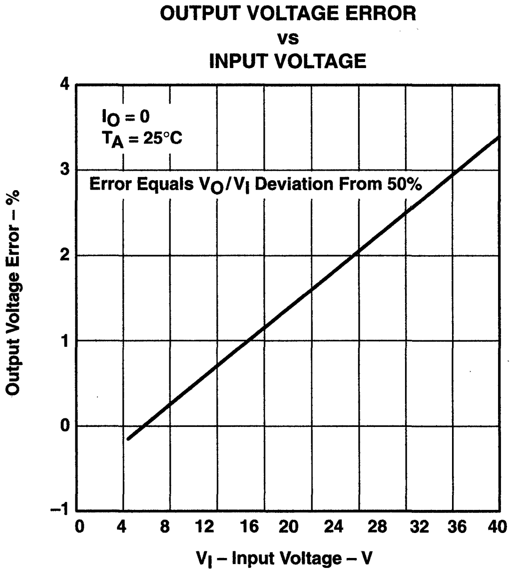

Figure 4

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† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

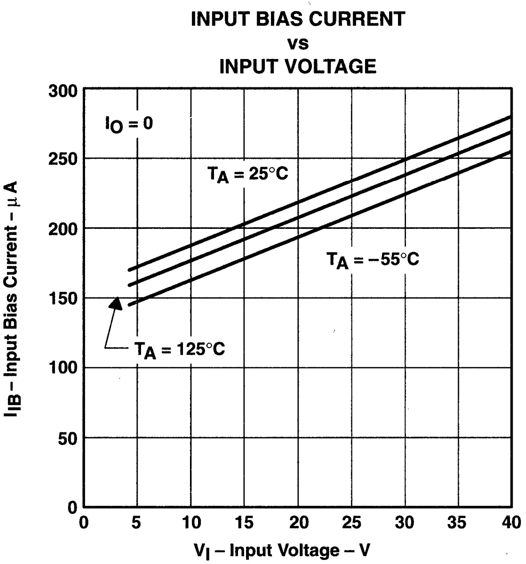

Figure 5

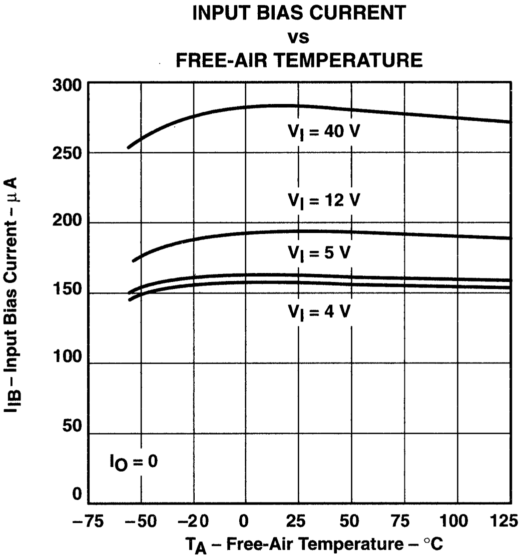

Figure 6

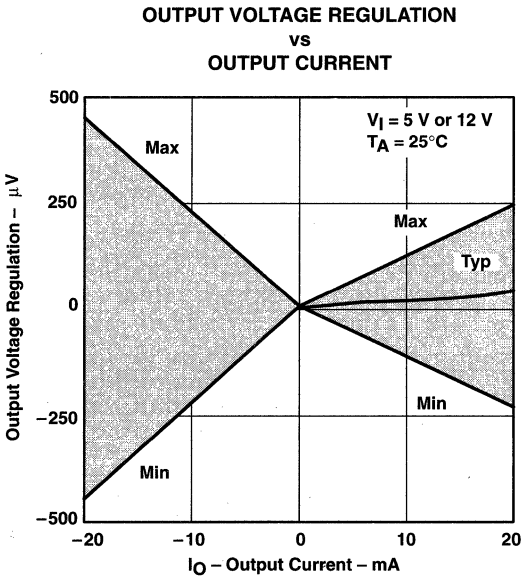

Figure 7

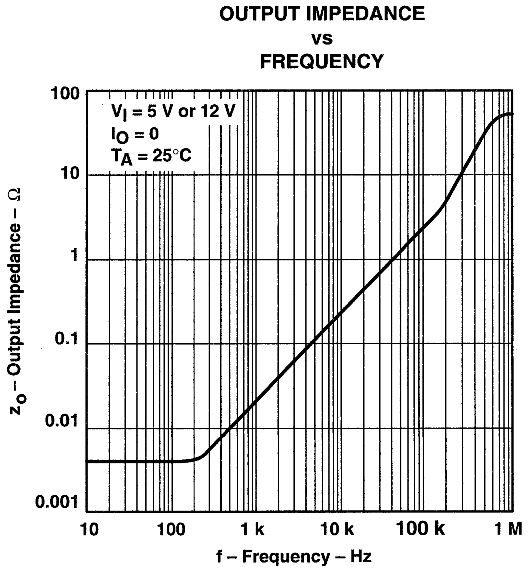

Figure 8

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† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

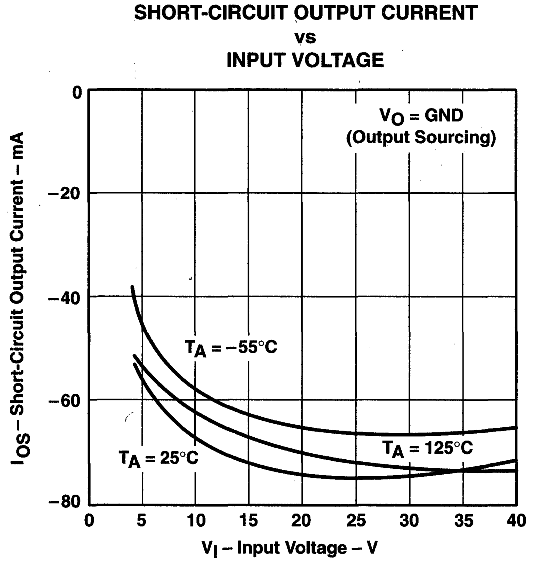

Figure 9

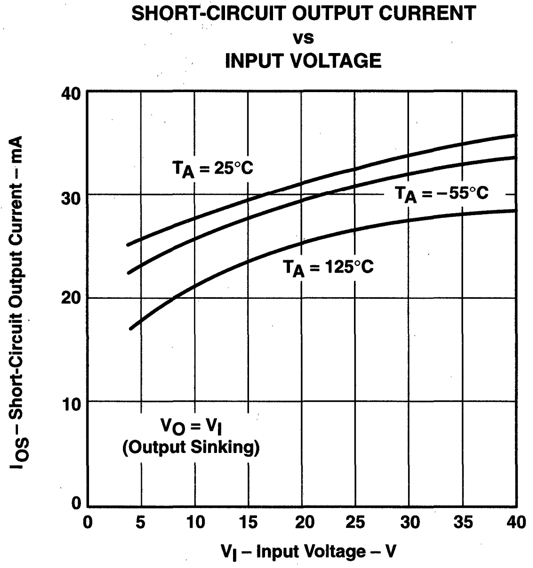

Figure 10

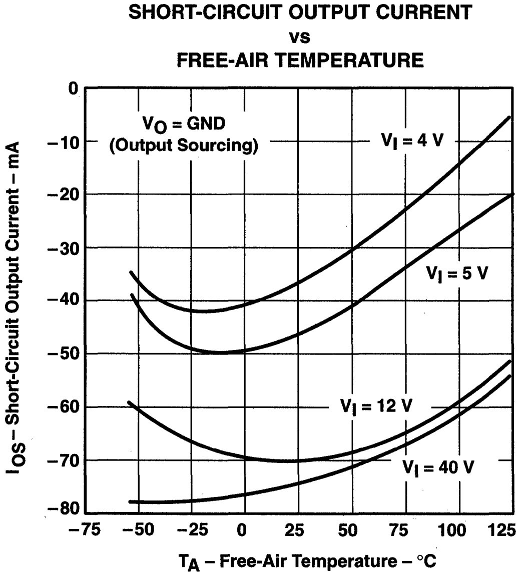

Figure 11

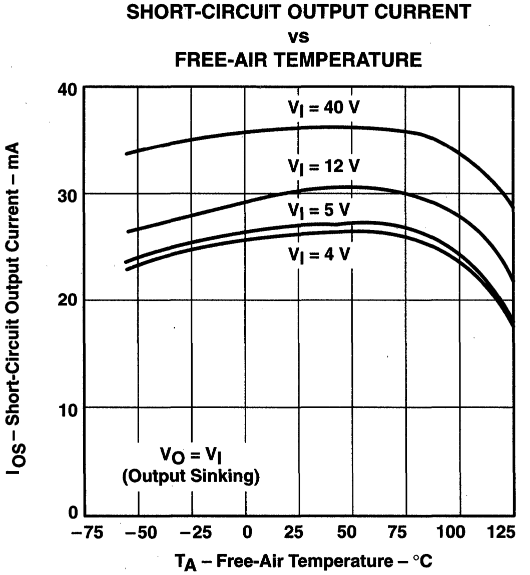

Figure 12

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† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

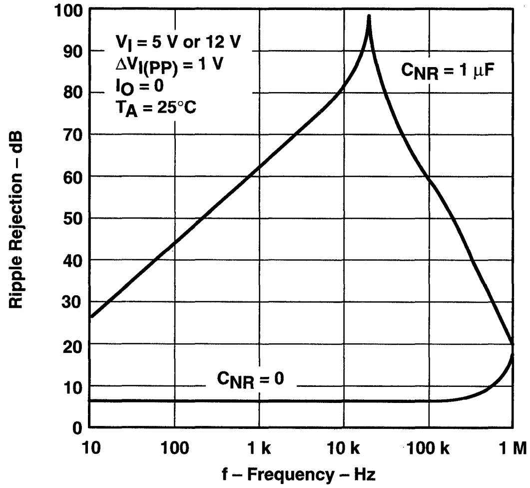


Figure 13

SPECTRAL NOISE VOLTAGE DENSITY
vs
FREQUENCY

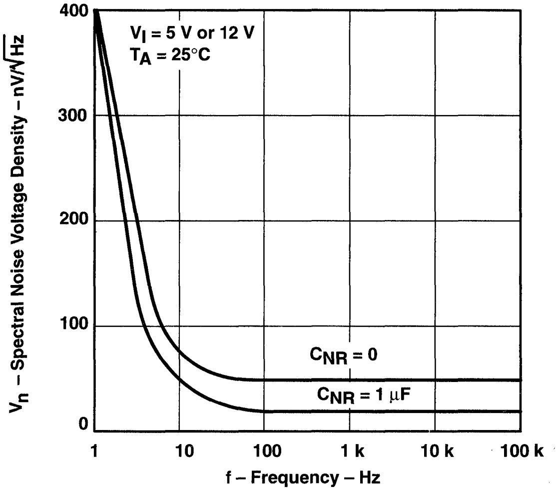


Figure 14

OUTPUT VOLTAGE RESPONSE
TO OUTPUT CURRENT STEP

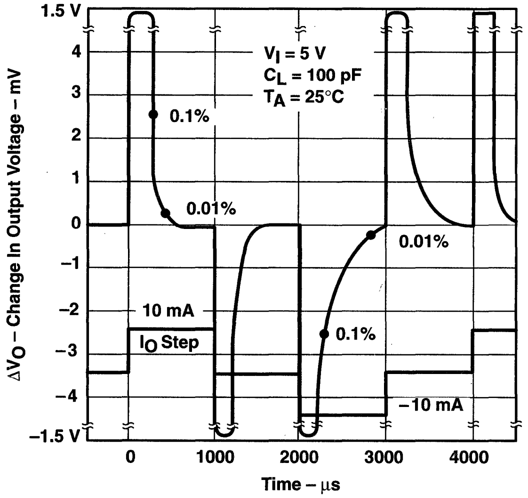


Figure 15

OUTPUT VOLTAGE POWER-UP RESPONSE

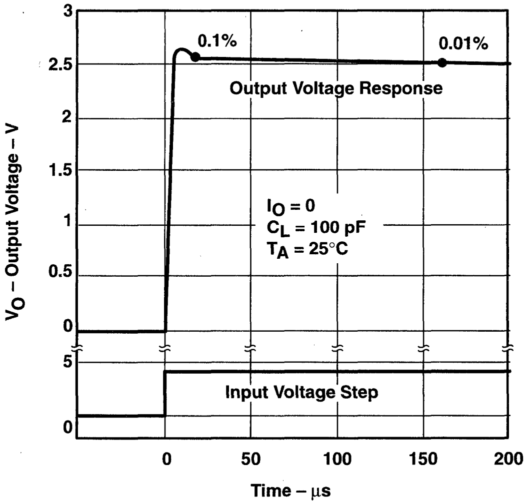


Figure 16

TYPICAL CHARACTERISTICS

STABILITY RANGE
OUTPUT CURRENT
vs
LOAD CAPACITANCE

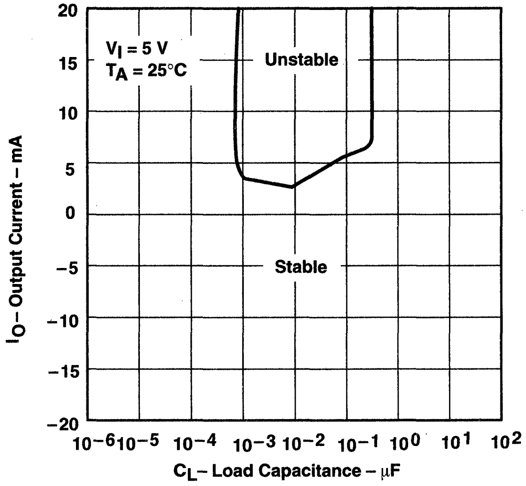


Figure 17

macromodel information

```
*   TLE2426 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
*   CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
*   REV (N/A)     SUPPLY VOLTAGE: 5 V
*   CONNECTIONS:      FILTER
                      |  INPUT
*                     |  |  COMMON
*                     |  |  |  OUTPUT
*                     |  |  |  |
.SUBCKT TLE2426       1  3  4  5
```

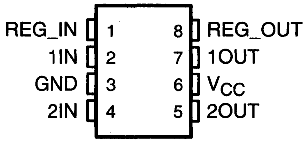
```
   C1      11  12  21.66E-12
   C2       6   7  30.00E-12
   C3      87   0  10.64E-9
   CPSR    85  86  15.9E-9
   DCM+    81  82  DX
   DCM-    83  81  DX
   DC       5  53  DX
   DE      54   5  DX
   DLP     90  91  DX
   DLN     92  90  DX
   DP       4   3  DX
   ECMR    84  99  (2,99) 1
   EGND    99   0  POLY(2)    (3,0) (4,0)   0   .5  .5
   EPSR    85   0  POLY(1)    (3,4)  -16.22E-6 3.24E-6
   ENSE    89   2  POLY(1)    (88,0) 120E-6 1
   FB       7  99  POLY(6)    VB  VC  VE  VLP VLN VPSR  0 74.8E6 -10E6  10E6    10E6    -10E6  74E6
   GA       6   0  11  12  320.4E-6
   GCM      0   6  10  99  1.013E-9
   GPSR    85  86  (85,86)    100E-6
   GRC1     4  11  (4,11) 3.204E-4
   GRC2     4  12  (4,12) 3.204E-4
   GRE1    13  10  (13,10)    1.038E-3
   GRE2    14  10  (14,10)    1.038E-3
   HLIM    90   0  VLIM   1K
   HCMR    80   1  POLY(2)    VCM+    VCM-    0   1E2     1E2
   IRP      3   4  146E-6
   IEE      3  10  DC  24.05E-6
   IIO      2   0  .2E-9
   I1      88   0  1E-21
   Q1      11  89  13  QX
   Q2      12  80  14  QX
   R2       6   9  100.0E3
   RCM     84  81  1K
   REE     10  99   8.316E6
   RN1     87   0   2.55E8
   RN2     87  88  11.67E3
   RO1      8   5  63
   RO2      7  99  62
   VCM+    82  99  1.0
   VCM-    83  99  -2.3
   VB       9   0  DC  0
   VC       3  53  DC  1.400
   VE      54   4  DC  1.400
   VLIM     7   8  DC  0
   VLP     91   0  DC  30
   VLN      0  92  DC  30
   VPSR     0  86  DC  0
   RFB      5   2  1K
   RIN1     3   1  220K
   RIN2     1   4  220K
.MODEL DX  D(IS=800.OE-18)
.MODEL QX  PNP(IS=800.OE-18 BF=480)
.ENDS
```

TPS2811, TPS2812, TPS2814, TPS2815
DUAL HIGH-SPEED MOSFET DRIVERS

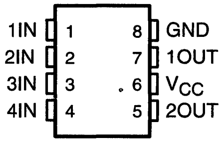
SLVS132 – OCTOBER 1995

- **Industry-Standard Driver Replacement**
- **20-ns Max Rise/Fall Times and 30 ns Max Propagation Delay – 1-nF Load**
- **2-A Peak Output Current**
- **100-µA Supply Current – Inputs High or Low**
- **4-V to 14-V Driver Supply Voltage Range; Internal Regulator Extends Range to 34 V**
- **–40°C to 150°C Junction Temperature Operating Range.**

TPS2811, TPS2812, TPS2813 . . . D, P, AND PW PACKAGES (TOP VIEW)



TPS2814, TPS2815 . . . D, P, AND PW PACKAGES (TOP VIEW)



description

The TPS2811 series of dual high-speed MOSFET drivers are capable of delivering peak currents of 2 A into highly capacitive loads. This performance is accompanied by supply currents an order of magnitude lower than those of competitive products. The design inherently minimizes shoot-through current.

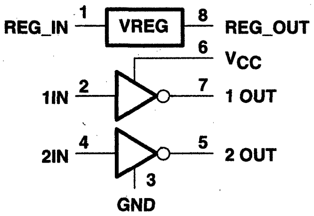
Each of the TPS2811, TPS2812, and TPS2813 drivers include a regulator to allow operation with supply inputs between 14 V and 34 V. The regulator output can be used to power other circuitry, provided power dissipation does not exceed package limitations. Supply voltages below 14 V may be connected directly to V_{CC}, REG_OUT, and REG_IN, or REG_IN can be left open.

The TPS2811 series are available in 8-pin PDIP, SOIC, and TSSOP packages and operate over a junction temperature range of –40°C to 150°C.

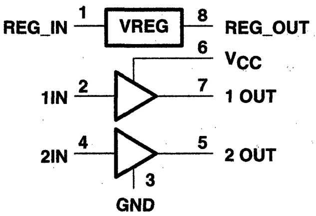
PRODUCT PREVIEW

logic diagrams (positive logic)

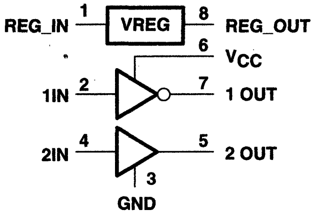
TPS2811



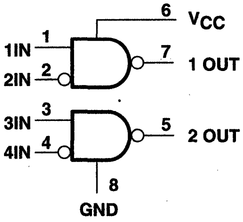
TPS2812



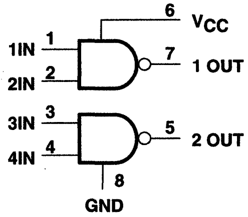
TPS2813



TPS2814



TPS2815



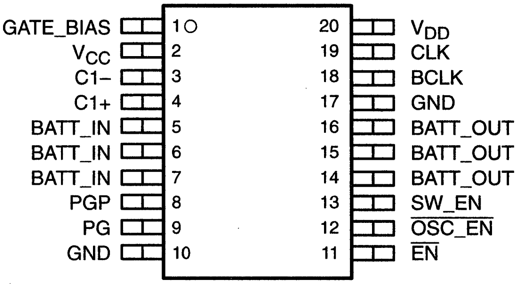
PRODUCT PREVIEW

TPS9103
POWER SUPPLY FOR GaAs POWER AMPLIFIERS

SLVS131 – OCTOBER 1995

- **On-chip Charge Pump Provides Negative Gate Bias for Depletion-Mode GaAs Power Amplifiers**
- **Buffered Clock Output to Drive Additional External Charge Pump**
- **200-mΩ High-Side Switch With Logic-Compatible Enable Input Controls Supply Voltage to the GaAs Power Amplifier**
- **Power-Good Circuitry Prevents High-Side Switch Turn-on Until Negative Gate Bias is Present**
- **Charge Pump Can Be Driven From the Internal Oscillator or An External Clock**
- **10-µA Maximum Standby Current**
- **Low-Profile (1.2-mm Max Height), 20-Pin TSSOP Package**

PW PACKAGE
(TOP VIEW)



description

The TPS9103 is a highly integrated power supply for depletion-mode GaAs power amplifiers (PA) in cellular handsets and other wireless communications equipment. Functional integration and low-profile packaging combine to minimize circuit-board area and component height requirements. The device includes: a p-channel MOSFET, configured as a high-side switch to control the application of power to the PA; a driver for the high-side switch with a logic-compatible input; a charge pump to provide negative gate-bias voltage; and logic to prevent turn-on of the high-side switch until gate bias is present. The high-side switch has a maximum on-state resistance of 200 mΩ.

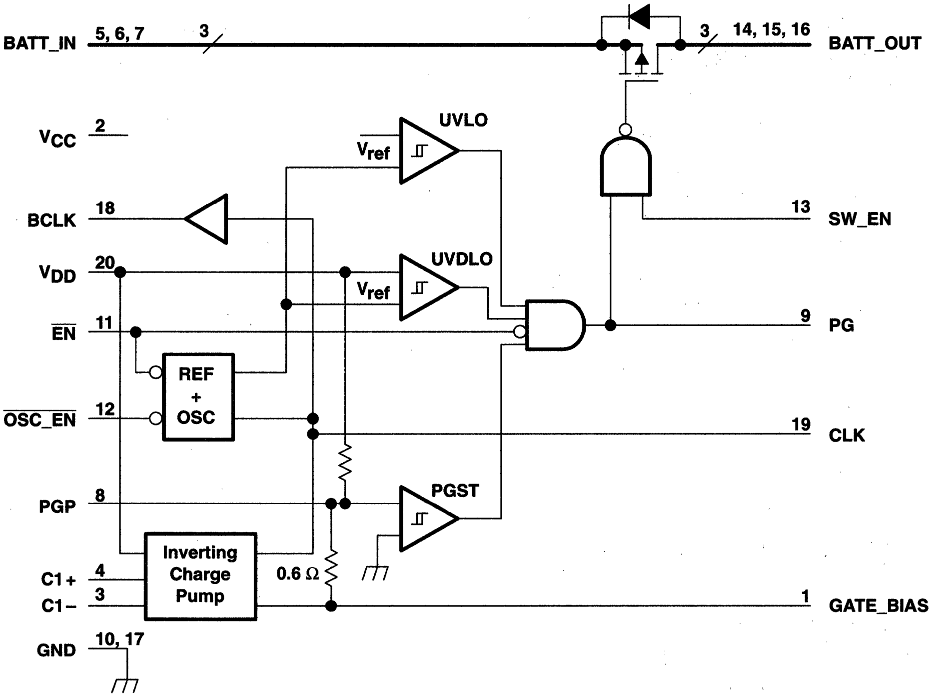
The TPS9103 is available in a 20-pin TSSOP package and operates over an ambient temperature range of −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM (Y)
	TSSOP (PW)	
−40°C to 85°C	TPS9103IPWLE	TPS9103Y

The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type).

functional block diagram



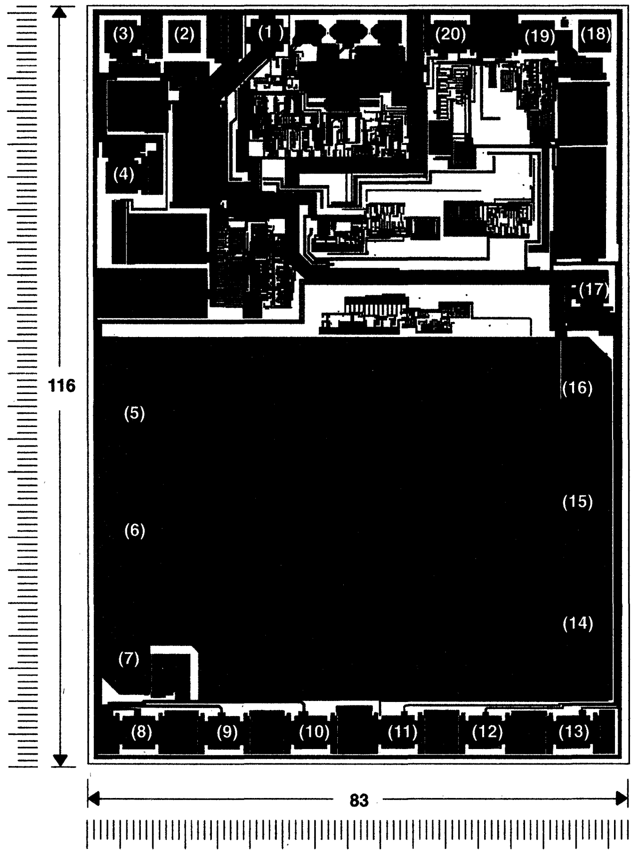
Terminal Functions

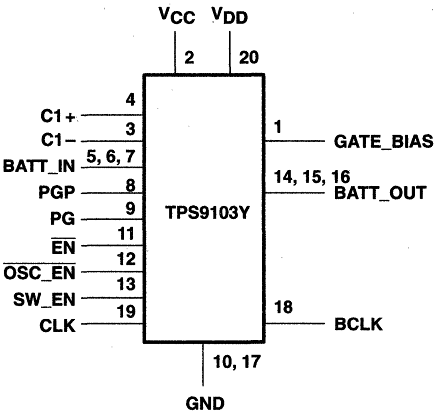
TERMINAL		DESCRIPTION
NAME	NO.	
GATE_BIAS	1	Negative gate-bias output voltage
V_{CC}	2	Logic supply voltage
C1–	3	External capacitor connection (inverting charge pump)
C1+	4	External capacitor connection (inverting charge pump)
BATT_IN	5	High-side switch input voltage
BATT_IN	6	High-side switch input voltage
BATT_IN	7	High-side switch input voltage
PGP	8	Program input for power-good threshold
PG	9	Power-good output
GND	10	Ground
$\overline{\text{EN}}$	11	Chip-enable input
$\overline{\text{OSC\_EN}}$	12	Oscillator-enable input
SW_EN	13	High-side switch enable input
BATT_OUT	14	High-side switch output voltage
BATT_OUT	15	High-side switch output voltage
BATT_OUT	16	High-side switch output voltage
GND	17	Ground
BCLK	18	Buffered clock output
CLK	19	Clock (bidirectional)
V_{DD}	20	Charge-pump supply voltage

TPS9103Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS9103. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

High-side switch input voltage, at BATT_IN (see Note 1)	−0.3 V to 15 V
Supply voltage, V_{CC}, V_{DD}	−0.3 V to 7 V
Differential input voltage, at GATE_BIAS (see Note 2)	15 V
Input voltage at SW_EN, $\overline{\mathrm{EN}}$, CLK, $\overline{\mathrm{OS\_CEN}}$, PG, GND	−0.3 V to V_{CC} + 0.3 V
Voltage at GATE_BIAS	−5.5 V
Output current at PG	
Output current at BCLK	
Continuous output current at GATE_BIAS	10 mA
Continuous output current at BATT_OUT	2 A
Peak output current at BATT_OUT	4 A
Maximum capacitor value at C1	0.4 μF
Maximum external clock frequency at CLK	100 kHz
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	−40°C to 85°C
Junction temperature range, T_J	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to device GND.
2. Differential voltage calculated: $|V_I\text{max}| + |\text{GATE\_BIAS}|$

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	645 mW	6.5 mW/°C	353 mW	255 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
High-side switch input voltage, at BATT_IN	3		9	V
Supply voltage, V_{CC}, V_{DD}	2.7		5.5	V
Output voltage, V_O, at GATE_BIAS	–2		–5	V
Continuous output current at GATE_BIAS	0		10	mA
Continuous output current at BATT_OUT	0			A
Charge-pump capacitor value at C1		0.33		μF
External clock frequency at CLK	25		75	kHz
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_I = 6 V, V_{CC} = V_{DD} = 3.3 V, I(BATT_OUT) = 0.5 A, I(GATE_BIAS) = 2 mA, $\overline{\text{EN}}$ = $\overline{\text{OSC\_EN}}$ = 0 V, SW_EN = V_{CC}, C1 = 0.33 μF (unless otherwise noted)

charge pump

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	T_A = 25°C	–3	–3.15	–3.3	V
Output Resistance	V_{CC} = 3.3 V		90		Ω

high-side switch

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On resistance	T_A = 25°C			200	mΩ
	T_A = 25°C, $V_{I(BATT\_IN)}$ = 3 V			400	mΩ
Leakage current	T_A = 25°C, $V_{I(BATT\_IN)}$ = 9 V, SW_EN = 0 V			1	μA
	T_A = 85°C, $V_{I(BATT\_IN)}$ = 9 V, SW_EN = 0 V			10	
Delay to output high	SW_EN from 0 V to V_{CC}			2	μs
Delay to output low	SW_EN from V_{CC} to 0 V			2	μs

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	T_A = 25°C	45	50	55	kHz
	V_{CC} = 2.7 V to 5.5 V	40		60	kHz
Duty cycle	V_{CC} = 2.7 V to 5.5 V	40%	50%	60%	

buffered clock output (BCLK)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Resistance				10	Ω
High-state output voltage	I(BCLK) = 30 mA	V_{CC} –0.3			V
Low-stage output voltage	I(BCLK) = 30 mA			0.4	V

digital inputs (SW_EN, $\overline{\text{EN}}$, $\overline{\text{OSC\_EN}}$, CLK)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		V_{CC} – 0.3		V_{CC} + 0.3	V
Low-level input voltage		GND – 0.3		GND + 0.3	V
Input current		–1		1	μA

power good (PG)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Threshold voltage	See Note 3		0.60 × V_{DD}		V
On-state voltage	I(PG) = 500 μA			0.3	V
Off-state voltage	I(PG) = –500 μA	V_{CC} –0.3			V
Delay GATE_BIAS to PG	See Note 4			5	μs

NOTES: 3. Threshold externally adjustable by programming PGP input.
4. Power-good output PG must be logic zero 5 μs after GATE_BIAS drops below threshold; i.e., GATE_BIAS is not negative enough.

power good (PGP)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance		100			kΩ

undervoltage lockout (UVLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage		2.4		2.7	V
Hysteresis		100			mV

undervoltage lockout (UVDLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage		2.4		2.7	V
Hysteresis			100		mV

supply current (ICC)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby			1	10	µA
UVLO	$V_{CC} < 2.4$ V		30	50	µA
Operating			350	500	µA

PRINCIPLES OF OPERATION

functional description

high-side switch and driver (BATT_IN, BATT_OUT, SW_EN)

The high-side switch is a p-channel MOSFET with a maximum on-state resistance of 200 mΩ ($V_{I(BATT\_IN)} = 6$ V and $V_{CC} = 3.3$ V). The driver pulls the gate of the high-side switch to GATE_BIAS instead of ground to reduce the size of the MOSFET. Gate breakdown considerations limit BATT_IN-to-GATE_BIAS to 15 V. Extremely fast switching times are not required in this application, and the high-side switch/driver is designed to provide 2 µs maximum switching times with minimum power consumption. The GaAs depletion-mode MOSFETs in the PA are protected from damage at power-up by internal logic that inhibits the driver until negative gate bias is available. The control input SW_EN is compatible with 3-V and 5-V CMOS logic; a logic-high input turns the high-side switch on.

oscillator ($\overline{\text{OSC\_EN}}$, CLK)

The internal oscillator drives the charge pump at 50 kHz with a nominal duty cycle of 50% when both the $\overline{\text{EN}}$ and $\overline{\text{OSC\_EN}}$ inputs are logic lows. CLK outputs the internal oscillator signal (no buffer). A logic-high input to $\overline{\text{OSC\_EN}}$ disables the internal oscillator and allows the charge pump to operate from an external clock connected to CLK.

charge pump (GATE_BIAS, C1+, C1–)

The inverting charge pump generates the negative gate-bias voltage output GATE_BIAS.

chip enable ($\overline{\text{EN}}$)

A logic high on $\overline{\text{EN}}$ shuts down the internal functions of the TPS9103 and turns the bias system off, reducing the supply current to less than 10 µA. A logic-low input causes normal operation to resume.

power good (PG, PGP)

PG output is logic low if GATE_BIAS is not in regulation. The high-side switch is disabled and PG is forced to logic low whenever the magnitude of GATE_BIAS is less than $0.6 \times V_{DD}$. A modified threshold for the power-good function can be achieved by programming PGP with an external resistor.

PRINCIPLES OF OPERATION

undervoltage lockout for V_{CC} and V_{DD} (UVLO and UVDLO)

Undervoltage lockout prevents operation at supply voltages too low for proper operation. When UVLO or UVDLO is active, all power-switch drives are forced to the off state and bias is removed from unneeded functions. A minimum 100 mV of hysteresis is built in to minimize cycling on and off because of source impedance loading when the supply voltage is close to the threshold.

buffered clock output (BCLK)

The buffered clock output is a driver of an external charge pump. For more details, please see the application section.

supply input for inverting charge pump (V_{DD})

V_{DD} is a separate supply input for the inverting charge pump. In normal operation, V_{DD} is connected to V_{CC}. If the negative gate-bias absolute value needs to be larger than V_{CC} (i.e., more negative), then a higher voltage supply needs to be connected to V_{DD}. This can be supplied from an external charge pump driven from BCLK.

Contents

Designing Switching Voltage Regulators with TL494

Application Report

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

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Abstract

In this application report, the TL494 switching power supply control is discussed in detail. A general overview of the device's architecture presents the primary functions contained in the 16-pin dual-in-line package and its features. An in-depth study of each of the device's primary building blocks highlights the versatility and limitations of the control circuit and gives a thorough understanding of their interrelationship. Applying the control circuit to several basic applications demonstrates the circuits' usefulness and outlines some still unresolved problems.

Introduction

Over the past few years, a series of monolithic integrated circuits for the control of switching power supplies have been introduced. One of these, the TL494, combines many of the features previously requiring several control circuits. The TL494 simplifies many design problems with its unique architecture. It is the purpose of this application report to give the reader a thorough understanding of the TL494, its features, its performance characteristics, and its limitations.

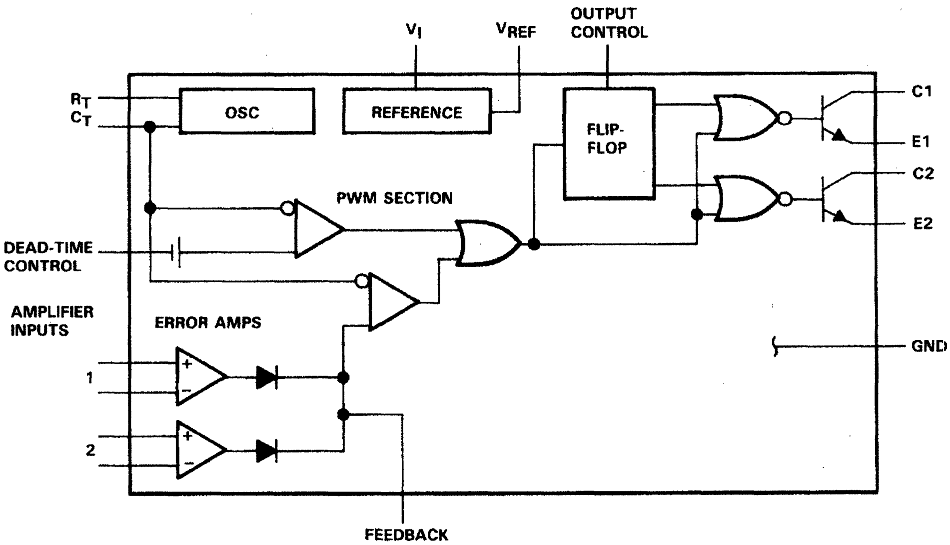


Figure 1. TL494 Block Diagram

The Basic Device

The design of the TL494 not only incorporates the primary building blocks required for the control of a switching power supply but also addresses many basic problems and reduces the amount of additional circuitry required in a total design. Figure 1 shows a block diagram of the TL494.

Principle of Operation

The TL494 is a fixed-frequency pulse-width-modulation (PWM) control circuit. Modulation of output pulses is accomplished by comparison of the sawtooth waveform, created by the internal oscillator on the timing capacitor (C_T), to either of two control signals. The output stage is enabled during that portion of time when the sawtooth voltage is greater than the control signals. As the control signals increase, the period of time the sawtooth input is greater decreases; therefore the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to each of the two output transistors. Figure 2 illustrates the relationship between the pulses and signals.

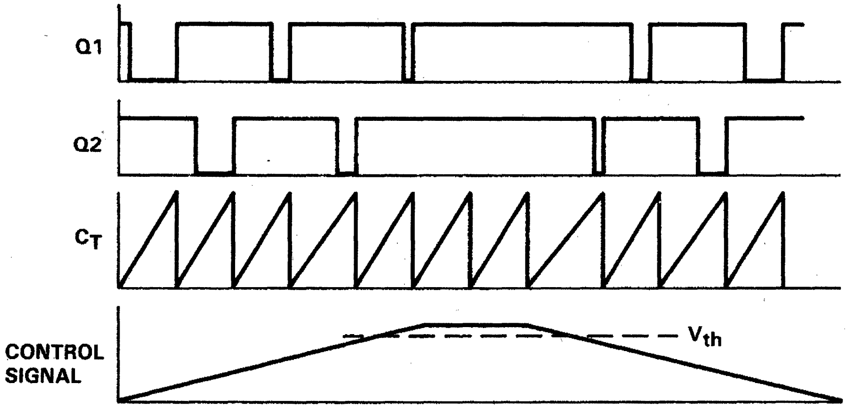


Figure 2. TL494 Modulation Technique

The control signals are derived from two sources: the dead-time (off-time) control circuit and the error amplifier circuit. The dead-time-control input is compared directly by the dead-time-control comparator. This comparator has a fixed 100-mV offset. With the control input biased to ground, the output is inhibited during the portion of time the sawtooth waveform is below 110 mV. This provides a preset dead time of approximately 3%, which is the minimum dead time that can be programmed. The PWM comparator compares the control signal created by the error amplifiers. One function of the error amplifier is to monitor the output voltage and provide sufficient gain so that millivolts of error at its input will result in a control signal of sufficient amplitude to provide 100% modulation control. The error amplifiers can also be used to monitor the output current and provide current limiting to the load.

5-V Reference Regulator

The TL494 internal 5-V reference regulator is shown in Figure 3. In addition to providing a stable reference, it acts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time-control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain a thermal stability of less than 100-mV variation over the operating free-air temperature range of 0 °C to 70 °C. Short-circuit protection is provided to protect the internal circuit from excessive load or short-circuit conditions. Designed primarily as an internal reference and preregulator, 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial accuracy of ±5% and maintains a stability of less than 25-mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input voltage and tracks it, as shown in Figure 4.

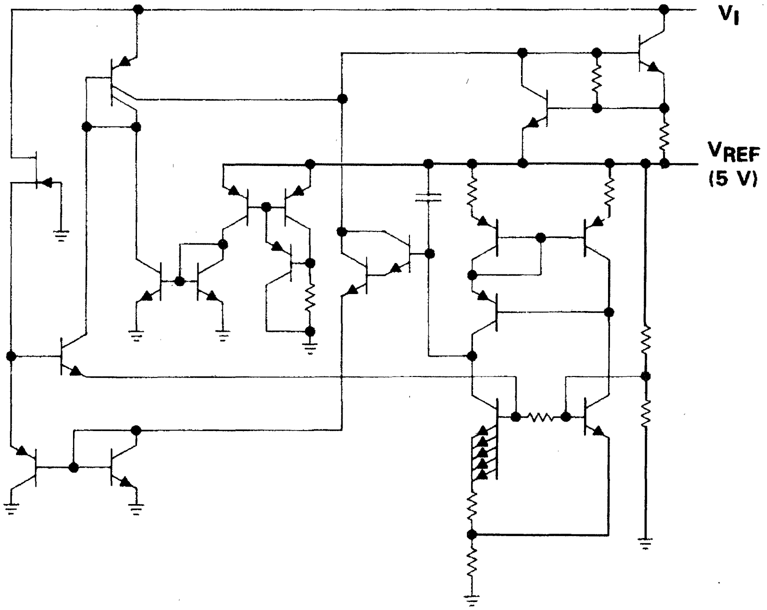


Figure 3. 5-V Reference Regulator

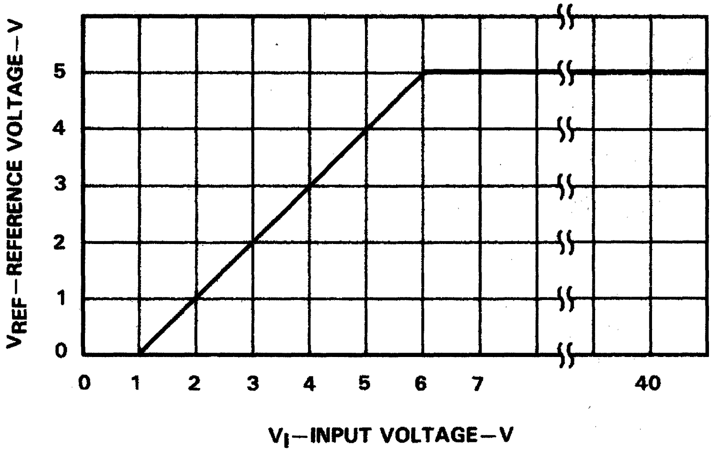


Figure 4. Reference Voltage vs Input Voltage

Oscillator

A schematic of the TL494 internal oscillator is presented in Figure 5. The oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison to the various control signals.

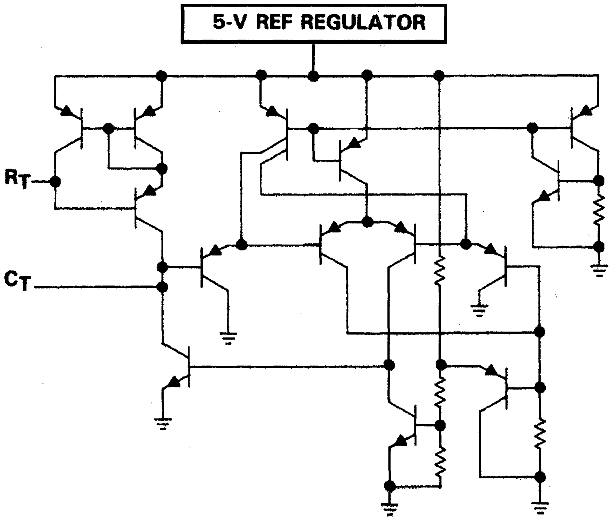


Figure 5. Internal Oscillator Schematic

Operation Frequency

The frequency of the oscillator is programmed by selection of the timing components R_T and C_T. The oscillator charges the external timing capacitor, C_T, with a constant current — the value of which is determined by the external timing resistor, R_T. This produces a linear-ramp voltage waveform. When the voltage across C_T reaches 3 V, it is discharged by the oscillator circuit and the charging cycle is reinitiated. The charging current is determined by the formula:

$$I_{CHARGE} = \frac{3\ V}{R_T}$$

The period of the sawtooth is:

$$t = \frac{3\ V \bullet C_T}{I_{CHARGE}} \qquad t = R_T \bullet C_T$$

The frequency of the oscillator then becomes:

$$f_{OSC} = \frac{1}{R_T \bullet C_T}$$

The oscillator frequency, however, is only equal to the output frequency for single-ended applications; for push-pull applications, the output frequency is one-half the oscillator frequency:

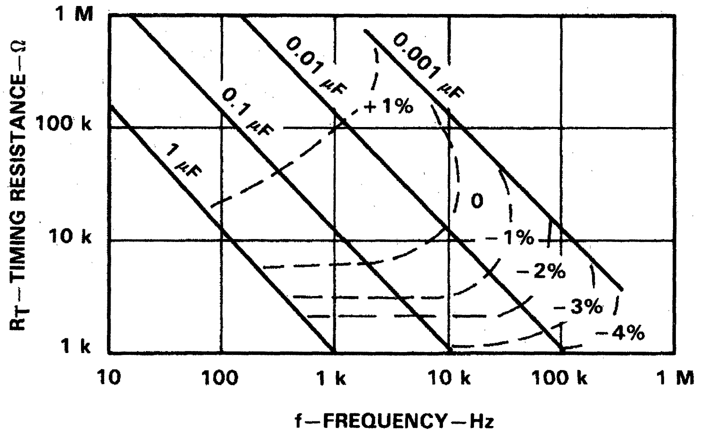
Single-ended applications: $f = \dfrac{1}{R_T \bullet C_T}$

Push-pull applications: $f = \dfrac{1}{2R_T \bullet C_T}$

The oscillator is programmable over a range from 1 kHz to 300 kHz. Practical values for R_T and C_T range from 1 kΩ to 500 kΩ and 470 pF to 10 μF, respectively. A plot of the oscillator frequency versus R_T and C_T is shown in Figure 6. The stability of the oscillator, for free-air temperature variations from 0 °C to 70 °C for various ranges of R_T and C_T, is also indicated in Figure 6.

Operation Above 150 kHz

At an operation frequency of 150 kHz, the period of the oscillator is 6.67 μs. The dead time established by the internal offset of the dead-time comparator ($\approx$3% period) yields a blanking pulse of 200 ns. This is the minimum blanking pulse acceptable to assure proper toggling of the pulse-steering flip-flop. For frequencies above 150 kHz, additional



NOTE: The percent of oscillator frequency variation over the 0 °C to 70 °C free-air temperature range is represented by dashed lines.

Figure 6. Oscillator Frequency vs R_T/C_T

dead time (above 3%) is provided internally to assure proper triggering and blanking of the internal pulse-steering flip-flop. Figure 7 shows the relationship of internal dead time (expressed in percent) provided for various values of R_T and C_T.

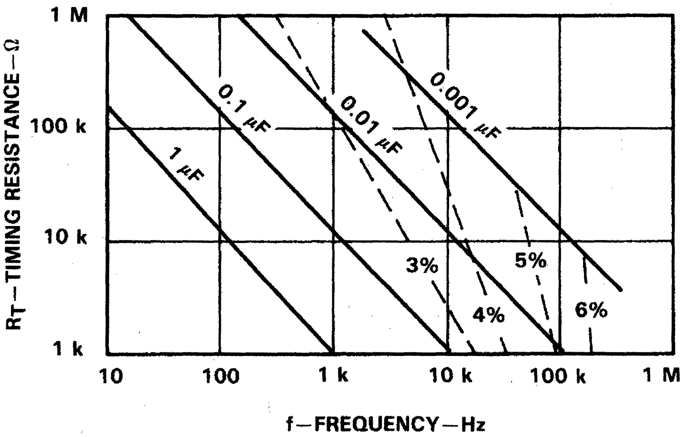


Figure 7. Variation of Dead Time vs R_T/C_T

Dead-Time-Control/PWM Comparator

The functions of the dead-time-control comparator and the PWM comparator are incorporated in a single comparator circuit, as shown in Figure 8. Since the two functions are totally independent, each function is discussed separately.

Comparator

The comparator is biased from the 5-V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit any hysteresis, so caution should be observed to protect against false triggering near the threshold. The comparator exhibits a response time of 400 ns from either of the control signal inputs to the output transistors, with only 100-mV overdrive. This assures positive control of the output, within a half cycle, for operation within the recommended 300-kHz range.

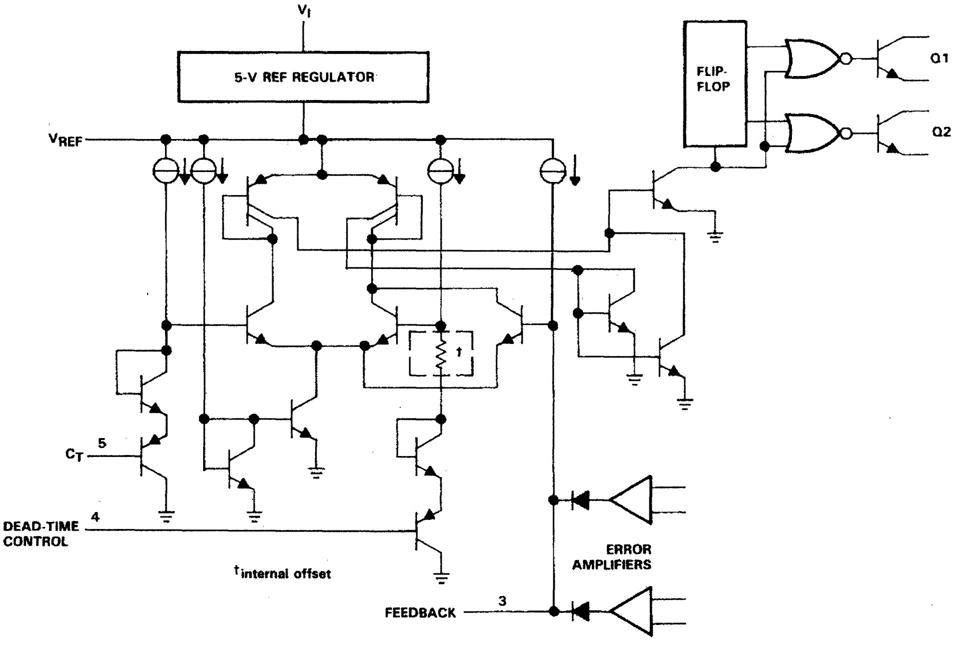


Figure 8. PWM/Dead-Time-Control Comparator

Dead-Time Control

The dead-time-control input provides control of the minimum dead time (off time). The output of the comparator inhibits switching transistors Q1 and Q2 whenever the voltage at its input is greater than the ramp voltage of the oscillator (see Figure 28). An internal offset of 110 mV assures a minimum dead time of ≈3% with the dead-time-control input grounded. Additional dead time can be imposed by applying a voltage to the dead-time-control input. This provides a linear control of the dead time from its minimum of 3% to 100% as the input voltage is varied from 0 V to 3.3 V, respectively. With full range control, it allows control of the output from external sources without disrupting the error amplifiers. The dead-time-control input is a relatively high-impedance input (I_I = $< 10\ \mu A$) and should be used where additional control of the output duty cycle is required. The input, however, must be terminated for proper control. An open circuit is an undefined condition.

Pulse-Width Modulation

The comparator also provides modulation control of the output pulse width. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode which is omitted from the control signal input. This requires the control signal (error amplifier output) to be ≈0.7 V greater than the voltage across C_T to inhibit the output logic, and assures maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse width varies from 97% of the period to 0 as the voltage present at the error amplifier output varies from 0.5 V to 3.5 V, respectively.

Error Amplifiers

A schematic of the error amplifier circuit is shown in Figure 9. Both high-gain error amplifiers receive their bias from the V_I supply rail. This permits a common-mode input voltage range from −0.3 V to 2 V less than V_I. Both amplifiers behave characteristically of a single-ended single-supply amplifier in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. The amplifier outputs are biased low by a current sink to provide maximum pulse width out when both amplifiers are biased off.

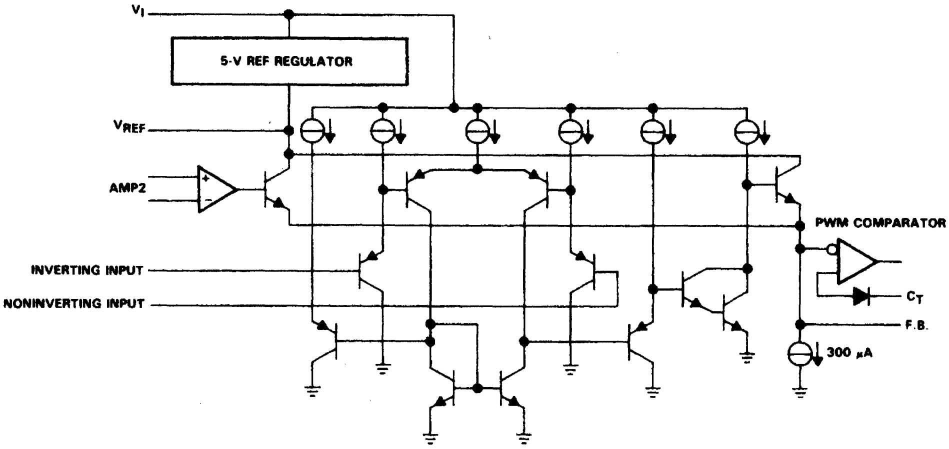


Figure 9. Error Amplifiers

Figure 10 shows the output structure of the amplifiers operating into the 300-µA current sink. Attention must be given to this node for biasing considerations in gain control and external control interface circuits. Since the amplifier output is biased low only through a current sink (I_{SINK} = 0.3 mA), bias current required by external circuitry into the feedback terminal must not exceed the capability of the current sink, otherwise, the maximum output pulse width will be limited. Figure 11 illustrates the proper biasing techniques for feedback gain control.

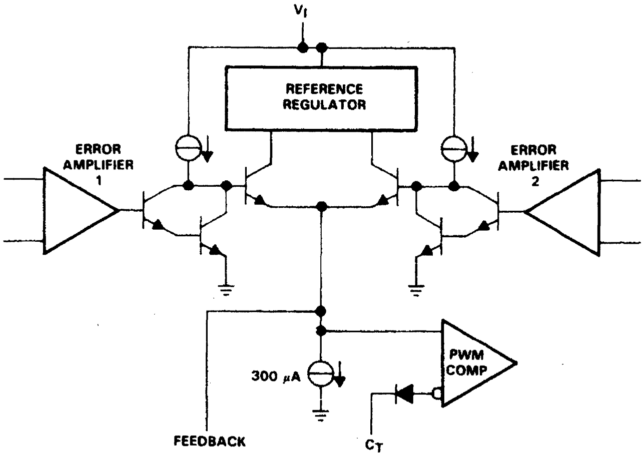
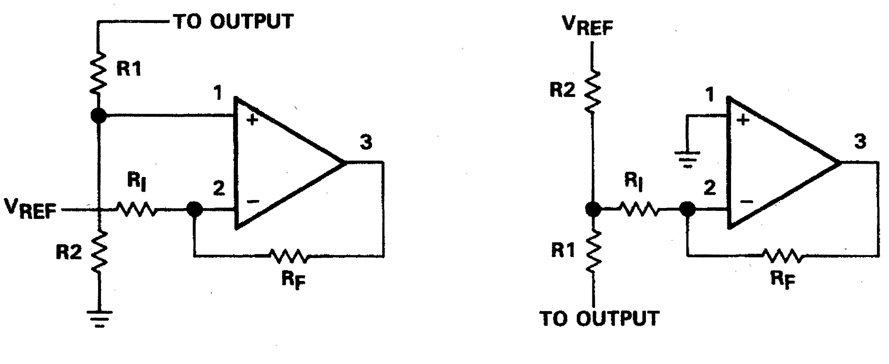


Figure 10. Multiplex Structure of Amplifiers



POSITIVE OUTPUT NEGATIVE OUTPUT

Figure 11. Error Amplifier Bias Configurations for Controlled Gain Applications

A plot of amplifier transfer characteristics is shown in Figure 12. This illustrates the linear gain characteristics of the amplifiers over the active input range of the PWM comparator (0.5 V to 3.5 V). This is important for overall circuit stability. The open-loop gain of the amplifiers, for output voltages from 0.5 V to 3.5 V, is 60 dB. A Bode plot of the amplifiers' gain characteristics is shown in Figure 13. Both amplifiers exhibit a response time of approximately 400 ns from their inputs to their outputs. Precautions should be taken to minimize capacitive loading of the amplifiers' outputs. Since they employ active pull-up only, the amplifiers' ability to respond to an increasing load demand can be severely degraded by capacitive loads.

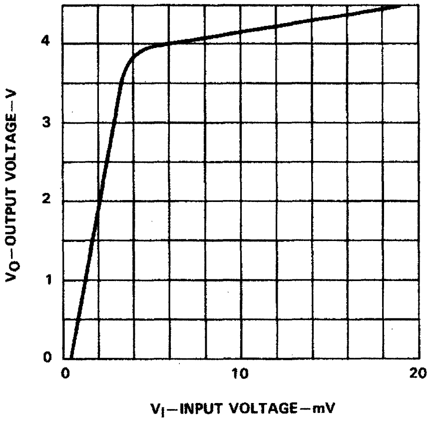


Figure 12. Amplifier Transfer Characteristics

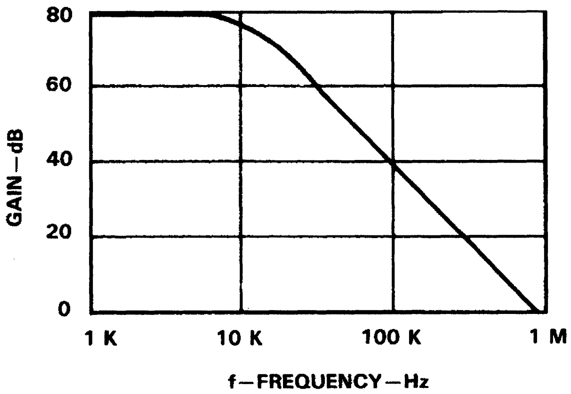


Figure 13. Amplifier Bode Plot

Output-Control Logic

The output-control logic is structured to provide added versatility through external control. Designed for either push-pull or single-ended applications, circuit performance can be optimized by selection of the proper conditions applied to the various control inputs.

Output-Control Input

The output-control input determines whether the output transistors operate in parallel or push-pull fashion. This input is the supply source for the pulse-steering flip-flop, as shown in Figure 14. The output-control input is asynchronous and has direct control over the output, independent of the oscillator or pulse-steering flip-flop. The input condition is intended to be a fixed condition that is defined by the application. For parallel operation, the output-control input must be grounded. This disables the pulse-steering flip-flop and inhibits its outputs. In this mode, the pulses seen at the output of the dead-time-control/PWM comparator are transmitted by both output transistors in parallel. For push-pull operation, the output-control input must be connected to the internal 5-V reference regulator. Under this condition, each of the output transistors is enabled, alternately, by the pulse-steering flip-flop.

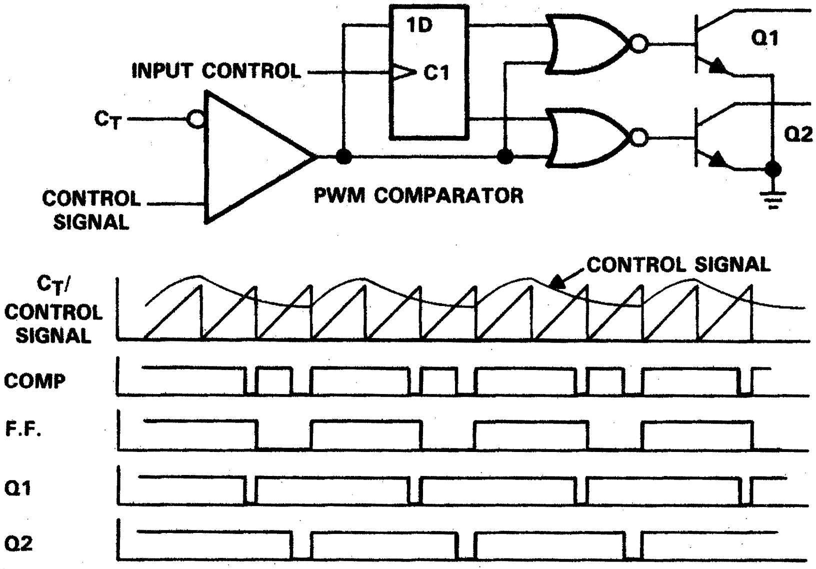


Figure 14. Output-Steering Architecture

Pulse-Steering Flip-Flop

The pulse-steering flip-flop is a positive-edge-triggered D-type flip-flop that changes state synchronously with the rising edge of the comparator output (see Figure 14). The dead time provides blanking during this period to ensure against the possibility of having both outputs on, simultaneously, during the transition of the pulse-steering flip-flop outputs. A schematic of the pulse-steering flip-flop is shown in Figure 15. Since the flip-flop receives its trigger from the output of the comparator, not the oscillator, the output always operates in a push-pull manner. The flip-flop will not change state unless an output pulse occurred in the previous period of the oscillator. This architecture prevents either output from double pulsing, but restricts the application of the control signal sources to dc feedback signals (for additional detail read 'Pulse-Current Limiting' in this application report).

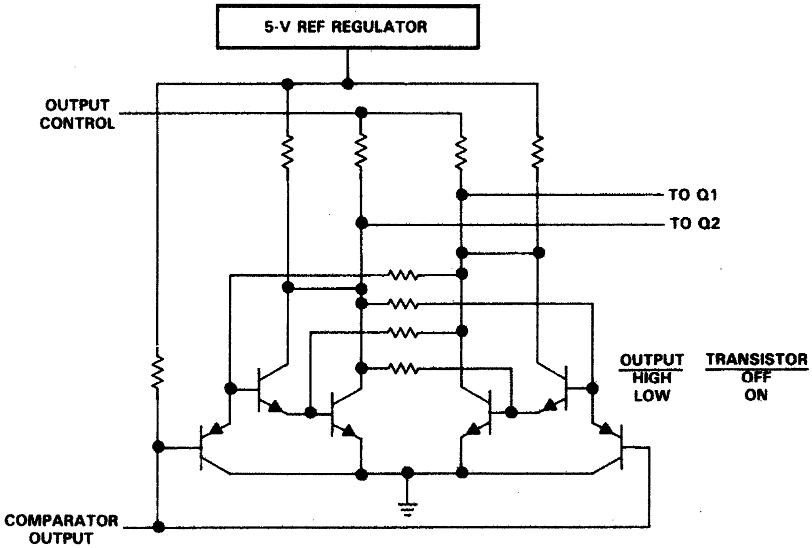


Figure 15. Pulse-Steering Flip-Flop

Output Transistors

There are two output transistors available on the TL494. The output structure is illustrated in Figure 16. Both transistors are configured open collector/open emitter and each is capable of sinking or sourcing up to 200 mA of current. The transistors exhibit a saturation voltage of less than 1.3 V in the common-emitter configuration and less than 2.5 V in the emitter-follower configuration. The outputs are protected against excessive power dissipation to prevent damage but do not employ sufficient current limiting to allow them to be operated as current-source outputs.

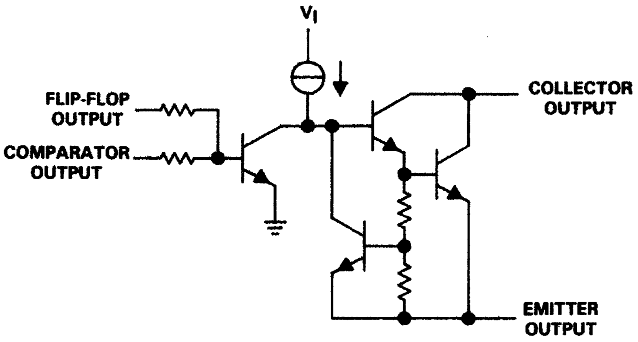


Figure 16. Output Transistor Structure

Applications

Reference Regulator

The internal 5-V reference regulator is designed primarily to provide the internal circuitry with a stable supply rail for varying input voltages. The regulator provides sufficient drive to sustain up to 10 mA of supply current to additional load circuitry. Excessive loading, however, may degrade the performance of the TL494 since the 5-V reference regulator establishes the supply voltage of much of the internal control circuitry.

Current Boosting the 5-V Regulator

Conventional bootstrap techniques for three-terminal regulators, such as the one shown in Figure 17, are *not recommended* for use on the TL494. Referring to Figure 17: Normally, the bootstrap is programmed by resistor R_B so that transistor Q1 turns on as the load current approaches the capability of the regulator. This works quite well where the current in the input (through R_B) is determined by the load current. This is not necessarily the case with the TL494. The input current not only reflects the load current but includes the current drawn by the internal control circuit, which is biased from the reference regulator as well as the input rail itself. As a result, the bias of shunt transistor Q1 is not controlled by the load current drawn by the reference regulator.

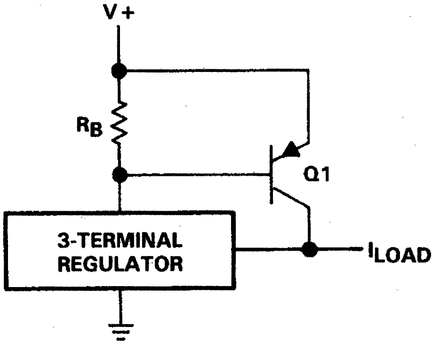


Figure 17. Conventional 3-Terminal Regulator Current-Boost Technique

Figure 18 shows the bootstrapping technique that is preferred for the TL494. This technique provides isolation between any bias-circuit load and the reference regulator output and provides a sufficient amount of supply current without affecting the stability of the internal reference regulator. This technique should be applied for bias circuit drive only since the regulation of the high-current output is solely dependent on the load.

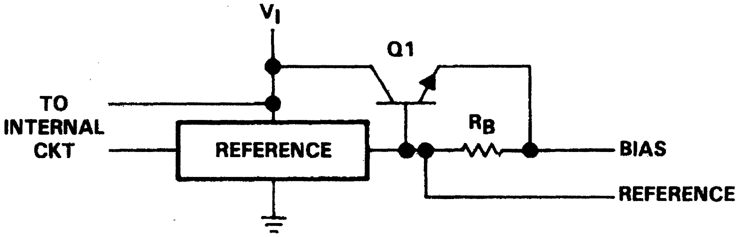


Figure 18. TL494 Reference Regulator Current-Boost Technique

Applications of the Oscillator

The design of the internal oscillator allows a great deal of flexibility in the operation of the TL494 control circuit.

Synchronizing

Synchronizing two or more oscillators in a common system is easily accomplished with the architecture of the TL494 control circuits. Since the internal oscillator is used for no other purpose than creation of the sawtooth waveform on the timing capacitor, the oscillator can be inhibited as long as a compatible sawtooth is provided externally to the timing capacitor terminal. The internal oscillator can be inhibited by terminating the R_T terminal to the reference supply output.

Master/Slave Synchronization

For synchronizing two or more TL494s, establish one device as the master and program its oscillator normally. Disable the oscillators of each slave circuit as explained above and use the sawtooth created by the master for each of the slave circuits, tying all C_T pins together as shown in Figure 19.

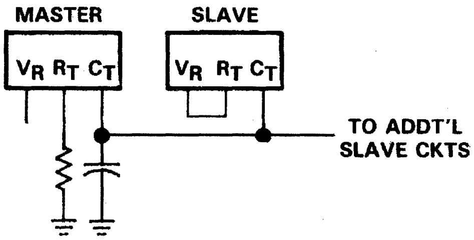


Figure 19. Master/Slave Synchronization

Master Clock Operation

To synchronize the TL494 to an external clock, the internal oscillator can be used as a sawtooth-pulse generator. Program the internal oscillator for a period that is 85% to 95% of the master clock and strobe the internal oscillator through the timing resistor, as shown in Figure 20. Q1 is turned on by a positive pulse applied to its base. This initiates the internal oscillator by grounding R_T and pulls the base of Q2 low. Q1 is latched on through the collector of Q2 and, as a result, the internal oscillator is locked on. As C_T charges, a positive voltage is developed across C1. Q1 forms a clamp on the trigger side of C1. At the completion of the period of the internal oscillator, the timing capacitor is discharged to ground and C1 drives the base of Q1 negative, causing Q1 and Q2 to turn off in turn. With the latch of Q1/Q2 turned off, R_T is open circuited and the internal oscillator is disabled until another trigger pulse is experienced.

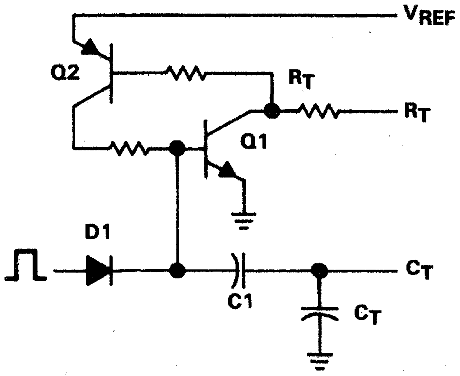


Figure 20. External Clock Synchronization

A common problem when synchronizing the power supply to a system clock occurs during start up. Normally, an additional start-up oscillator is required. Here again, the internal oscillator can be used by modifying the previous circuit slightly, as shown in Figure 21. During power up, when the output voltage is low, Q3 is biased on causing Q1 to stay on and the internal oscillator to behave normally. Once the output voltage has increased sufficiently ($V_O > V_{REF}$ for Figure 21), Q3 is no longer biased on and the Q1/Q2 latch becomes dependent of the trigger signal, as previously discussed.

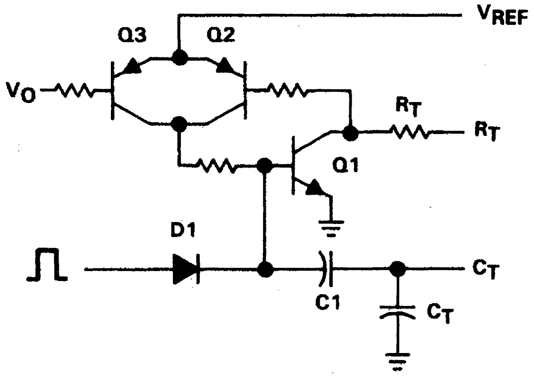


Figure 21. Oscillator Start-Up Circuit

Fail-Safe Operation

With the modulation scheme employed by the TL494 and the structure of the oscillator, the TL494 will inherently turn off if either timing component fails. If timing resistor R_T opens, no current is provided by the oscillator to charge C_T. The addition of a bleeder resistor, as shown in Figure 22, assures the discharge of C_T. With the C_T input at ground, or if C_T short circuits, both outputs are inhibited.

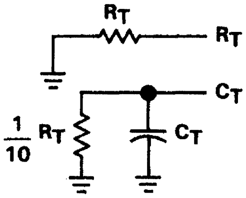
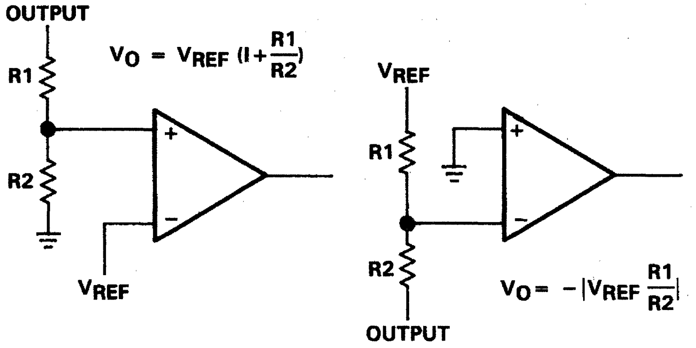


Figure 22. Fail-Safe Protection

Error-Amplifier-Bias Configuraton

The design of the TL494 is aligned to employ both amplifiers in a noninverting configuration. Figure 23 illustrates the proper bias circuits for negative and positive output voltages. The gain control circuits, shown previously in Figure 11, can be integrated into the bias circuits.



POSITIVE OUTPUT CONFIGURATION NEGATIVE OUTPUT CONFIGURATION

Figure 23. Error Amplifier Bias Configurations

Current Limiting

Either amplifier provided on the TL494 can be used for current limiting. Application of either amplifier is limited primarily to load current control. The architecture of the TL494 defines that these amplifiers be used for dc control applications. Both amplifiers have a broad common-mode voltage range which allows direct current sensing at the output voltage rails. Several techniques can be employed for current limiting.

Fold-Back Current Limiting

Figure 24 illustrates the proper bias technique for fold-back current limiting. Initial current limiting occurs when sufficient voltage is developed across R_{CL} to compensate for the base-emitter voltage of Q1 plus the voltage across R1. When current limiting occurs, the output voltage will drop. As the output decays, the voltage across R1 decreases proportionally. This results in less voltage required across R_{CL} to maintain current limiting. The resulting output characteristics are illustrated in Figure 25.

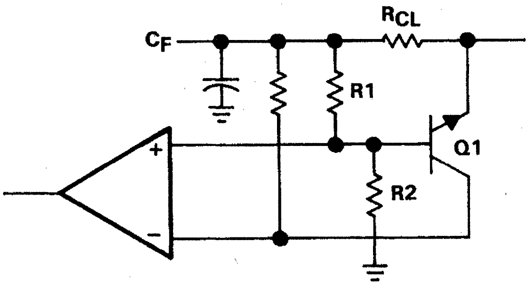
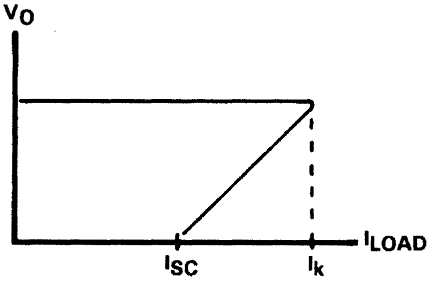


Figure 24. Fold-Back Current Limiting



$$I_K = \frac{V_O\,R1 + V_{BE(Q1)}\,(R1 + R2)}{R_{CL}\,R2}$$

$$I_{SC} = \frac{V_{BE(Q1)}\,(R1 + R2)}{R_{CL}\,R2}$$

Figure 25. Fold-Back Current Characteristics

Pulse-Current Limiting

The internal architecture of the TL494 is not aligned to accommodate direct pulse-current limiting. The problem arises from two factors: 1. The internal amplifiers do not function as a latch, they are intended for analog applications. 2. The pulse-steering flip-flop sees any positive transition of the PWM comparator as a trigger and toggles its outputs prematurely, i.e., prior to the completion of the oscillator period. As a result, a pulsed control voltage occurring during a normal on time not only causes the output transistors to turn off but also toggles the pulse-steering flip-flop. With the outputs off, the excessive current condition decays and the control voltage returns to the quiescent-error-signal level. When the pulse ends, the outputs are again enabled and the residual on-time pulse appears on the opposite output. The resulting waveforms are shown in Figure 26. The major problem here is the lack of dead-time control. A sufficiently narrow pulse may result in both outputs being on concurrently, depending on the delays of the external circuitry. A condition where insufficient dead time exists is a destructive condition. Pulse-current limiting, therefore, is best implemented externally, as shown Figure 27.

The current in the switching transistors is sensed by R_{CL}. When sufficient current is experienced, the sensing transistor Q1 is forward biased, the base of Q2 is pulled low through Q1, and the dead-time control input is pulled to the 5-V reference. Drive for the base of Q3 is provided through the collector of Q2. Q3 acts as a latch to maintain Q2 in a saturated state when Q1 turns off, as the current decays through R_{CL}. The latch will remain in this state, inhibiting the output transistors, until the oscillator completes its period and discharges C_T to 0 V. When this occurs, the Schottky diode, D1, will forward bias and turn off Q3 and Q2, allowing the dead-time control to return to its programmed voltage.

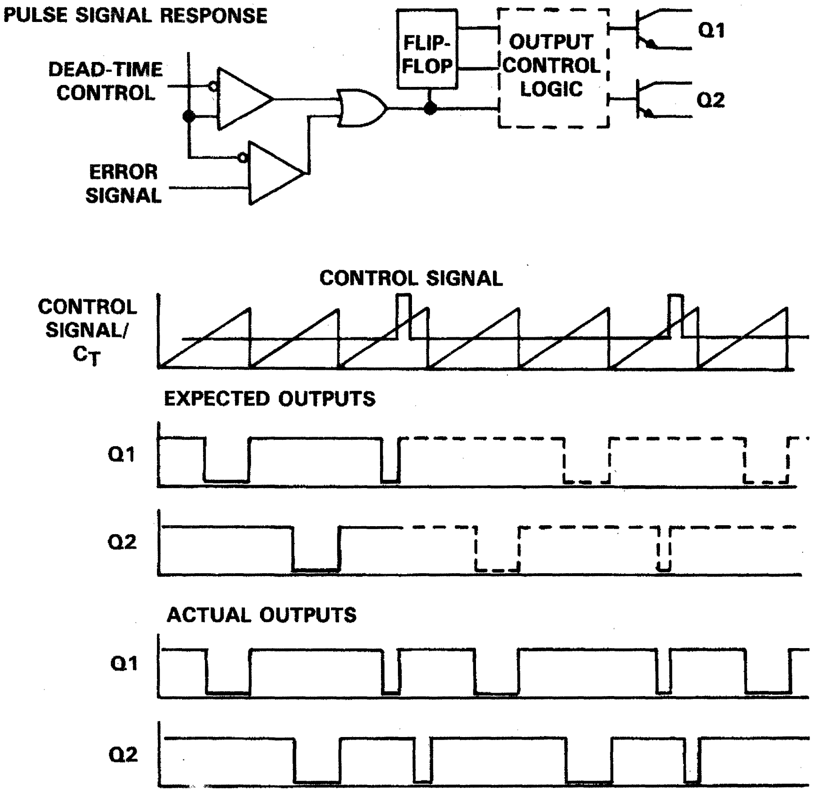


Figure 26. Error Signal Considerations

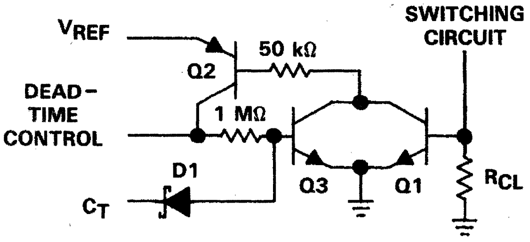


Figure 27. Peak-Current Protection

Applications of the Dead-Time Control

The primary function of the dead-time control is to control the minimum off-time exhibited by the output of the TL494. The dead-time-control input provides control from 5% to 100% dead time, as illustrated in Figure 28.

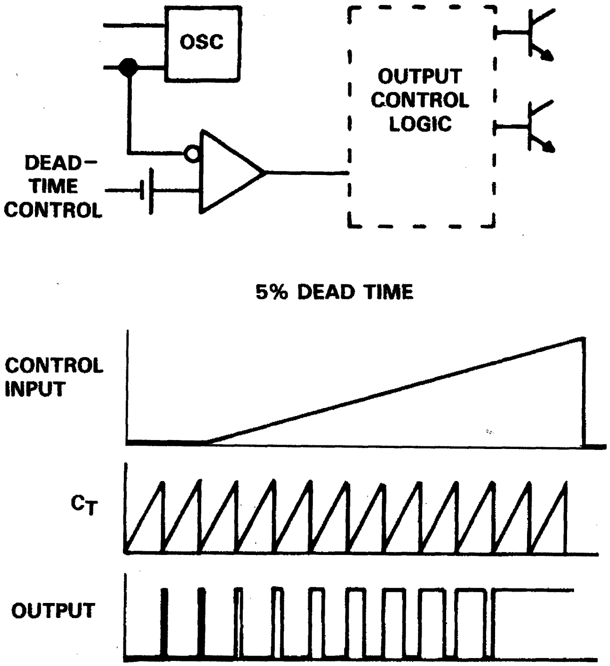


Figure 28. Dead-Time Control Characteristics

The TL494 can therefore be tailored to the specific power transistor switches that are used to assure that the output transistors never experience a common on-time. The bias circuit for the basic function is shown in Figure 29. The dead-time control can be used for many additional control signals.

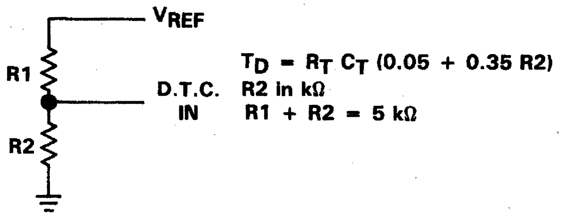


Figure 29. Tailored Dead Time

Soft Start

With the availability of the dead-time control, input implementation of a soft-start circuit is relatively simple; Figure 30 shows one example. Initially, capacitor C_S forces the dead-time-control input to follow the 5-V reference regulator which disables both outputs, i.e., 100% dead time. As the capacitor charges through R_S, the output pulse slowly increases until the control loop takes command. If additional control is to be introduced at this input, a blocking diode should be used to isolate the soft-start circuit. If soft start is desired in conjunction with a tailored dead time, the circuit in Figure 29 can be used with the addition of capacitor C_T across resistor R1.

The use of soft-start protection is recommended. Not only does such circuitry prevent large current surges during power-up, it also protects against any false signals which might be created by the control circuit as power is applied.

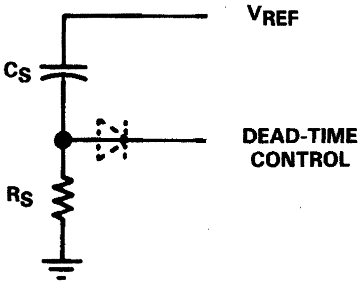


Figure 30. Soft-Start Circuit

Overvoltage Protection

The dead-time control also provides a convenient input for overvoltage protection which may be sensed as an output voltage condition or input protection. Figure 31 employs a TL430 as the sensing element. When the supply rail being monitored increases to the point that 2.7 V is developed at the driver node of R1 and R2, the TL430 goes into conduction. This forward biases Q1, causing the dead-time control to be pulled up to the reference voltage, disabling the output transistors.

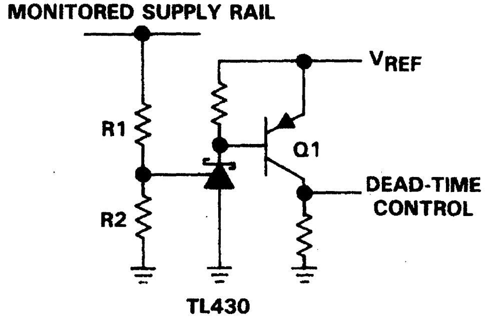


Figure 31. Overvoltage Protection Circuit

Modulation of Turn-Off Transition

Modulation of the output pulse by the TL494 is accomplished by modulating the turn-on transition of the output transistors. The turn-off transition is always concurrent with the falling edge of the oscillator waveform. Figure 32 shows the oscillator output as it is compared to a varying control signal and the resulting output waveforms. If modulation of the turn-off transition is desired, an external negative slope sawtooth, as shown in Figure 33, can be used without degrading the overall performance of the TL494.

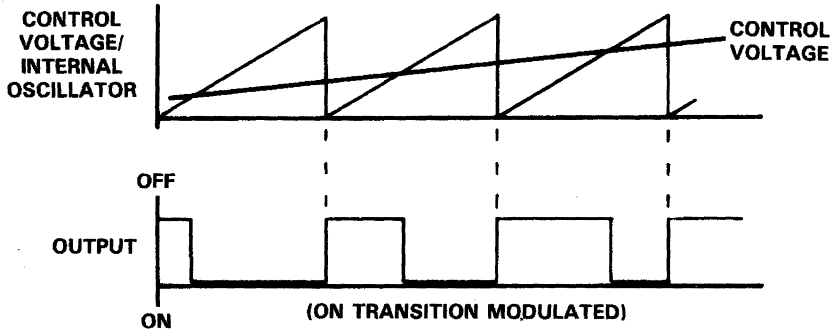


Figure 32. Turn-On Transition

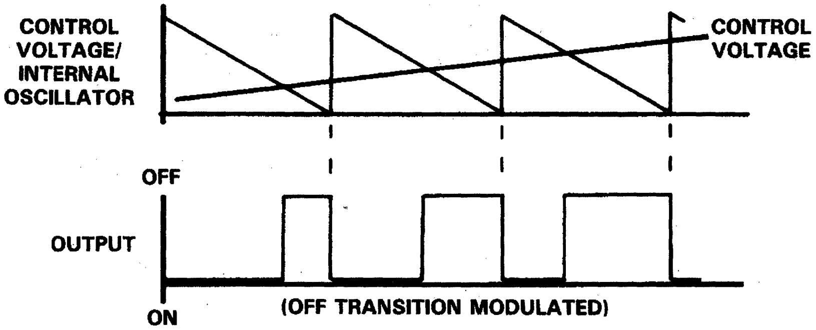


Figure 33. Turn-Off Transition

Designing Switching Voltage Regulators with TL497A

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INTRODUCTION

The TL497 represents a revolution in the implementation of a monolithic, highly efficient switching regulator.

Conventional series regulators employ an active element, usually a transistor operating in a linear mode, which functions as a variable resistor. The product of this resistance and the load current create a changing differential voltage required to step down from an unregulated input voltage to a fixed output voltage. In this type of circuit, current requirements defined by the load, must be experienced by the pass element. As the input to output voltage differential or load current requirement increases the power dissipated in the pass element increases proportionally. This power represents a loss to the system and limits the efficiency of series regulators.

The switching regulator, on the other hand, does not operate in the linear mode and is capable of achieving high efficiency power conversion even at large input/output voltage differentials. In the past the complexity of the circuitry required to construct a switching regulator negated the advantage of efficiency gained over series pass regulators. Use of the TL497A, however, eliminates the complex circuit designs previously required and offers marked performance improvements in efficiency over systems using series pass regulators.

PRINCIPLE OF OPERATION

The principle of operation and the method by which voltage conversion at high efficiencies can be achieved using switching regulators can best be demonstrated by analyzing the basic configuration of a step-down switching voltage regulator (Figure 1).

Q1 is the switch transistor which is turned on and off by the regulator's control circuitry at a frequency and duty cycle required to maintain the desired output. Because this transistor is always in the saturated state when it is conducting, or otherwise completely nonconducting, the power dissipated in the switch is much lower than that dissipated in a series regulator whose pass transistor is continuously operated in the linear region. This is the primary contributor to the increased efficiency experienced with a switching voltage regulator. The transfer of energy from the input to the output is achieved through the inductor L. During the time Q1 is on (t_{on}) the input voltage is applied to the LC filter and the current in the inductor increases. When Q1 is turned off the energy developed in the inductor during the previous half cycle, maintains the current flow to the load through the catch diode D1 and delivers that energy to the load.

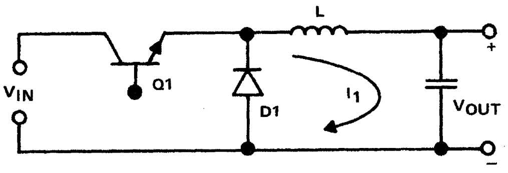


FIGURE 1. Step-Down Switching Voltage Regulator

The output voltage is determined by the input voltage (V_{IN}) and the duty cycle of the switch Q1.

$$V_{OUT} = V_{IN} \frac{t_{ON}}{T}$$

where $T = t_{ON} + t_{OFF}$

Therefore, by controlling the duty cycle (t_{on}/T), changes in the input voltage can be compensated for. If V_{IN} increases, the control circuit will cause a corresponding reduction in the duty cycle and thereby maintain a constant V_{OUT}, without increasing the amount of power dissipated internally in the regulator.

THE TL497A

General

The TL497A incorporates on a single monolithic chip all the active functions required in the construction of a Switching Voltage Regulator: a precision 1.22-volt reference, a pulse generator, a high-gain comparator, current limit sense and shut-down circuitry, a catch diode, and a series pass transistor. The TL497A was designed to offer versatility and to optimize the ease of its use in the various step-up, step-down, and voltage inversion applications requiring high efficiency.

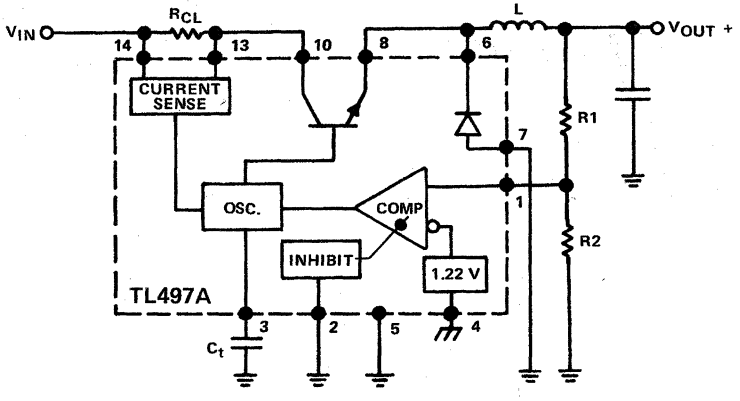


FIGURE 2. TL497A Block Diagram

Programming

A block diagram of the TL497A is shown in Figure 2. The internal 1.22-volt precision band-gap reference is internally connected between the substrate terminal and the inverting input of the high-gain comparator. The output of the circuit is sensed through a resistor ladder network (R1-R2) by the noninverting input of the comparator and is programmed by the resistors R1 and R2 such that the feedback voltage equals the 1.22 volt reference. Thus;

$$V_{OUT}\frac{R2}{R1+R2}=1.22\text{ volts}$$

To keep it simple the voltage across R2 is 1.22 volts. For 1mA programming current R2 becomes 1.22 KΩ. Therefore:

SET $R2 = 1.22\ K\Omega$

AND CALCULATE $R1 = (V_{OUT} - 1.22)\ K\Omega$

Oscillator

The oscillator is composed of a current pulse generator which charges and discharges the external timing capacitor (C_t) at fixed current rates whenever the feedback voltage is less than 1.22 v. The charging rate is 1/6 that of the discharge rate which results in the voltage waveform shown in Figure 3. The total period of the charge/discharge cycle is determined by the external timing capacitor (C_t) and is constant for all input voltages within the TL497A recommended operating ranges.

The charge/discharge period (T) varies with C_t as shown in Table I.

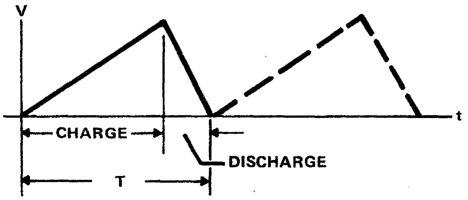


FIGURE 3. C_t Voltage Waveform

The dotted line of Figure 3 shows the timing capacitor waveform under continuous operation conditions. Only under these conditions does T determine the oscillators frequency ($F_{max} = 1/T$). These conditions exist during initial power-up of the system or whenever the comparator indicates the output voltage is less than the desired voltage-out. After the timing capacitor is discharged, the oscillator control circuit will sample the output of the comparator to determine if the output voltage is at a satisfactory level. If the comparator indicates the output is deficient, the current generator will retrigger and the oscillator will go through another C_t charge/discharge cycle; after which it will sample the comparator again and so forth. If on the other hand, the comparator indicates the output voltage is satisfactory, the current generator will be on standby until it is triggered by the comparator as illustrated in Figure 4. The pass transistor is turned "ON" during the charging portion (t_C) and turned "OFF" during the discharge portion (t_D) and any subsequent standby

Table I. Charge/Discharge Period Vs. C_t

C_t (pF)	200	250	350	400	500	750	1000	1500	2000
T (μs)	23	27	32	39	50	70	95	140	230

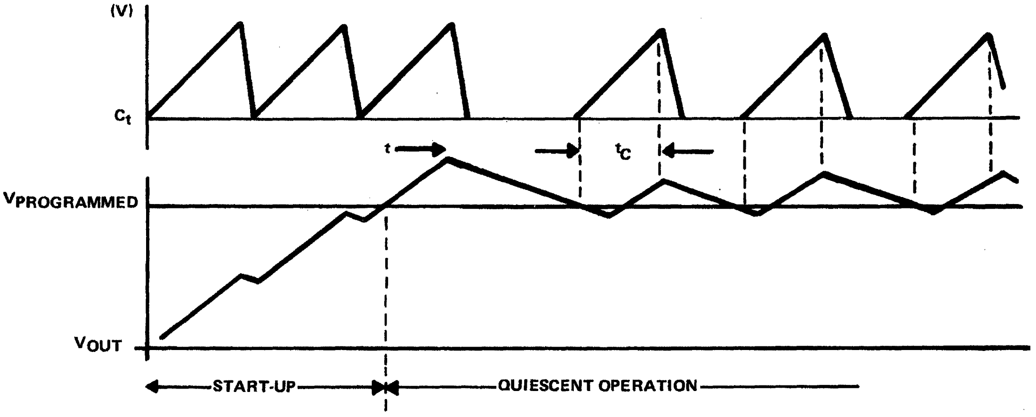


FIGURE 4. Typical C_t Voltage Waveform During Start-Up and Quiescent Operation

Table II. On-Time Vs. C_t

C_t (pF)	200	250	350	400	500	750	1000	1500	2000
t_C (µs)	19	22	26	32	44	56	80	120	180

period after the charge/discharge cycle of C_t. Under these conditions the operating frequency becomes dependent on the load requirement and C_T only determines the ON time (t_{ON}) which remains constant. Thus the duty cycle is modulated by the changing frequency. The on-time of the switching transistor coincides with t_C as shown in Table II.

Current Limiting

Current limiting is accomplished with the current-limit control provided. The voltage developed across the user selected series current limit resistor (R_{CL}) is sensed. When this voltage becomes greater than one V_{BE} drop (0.5 V typically) the current limit circuitry provides an additional current path to charge the timing capacitor. This, in effect, shortens the on-time of the switching transistor and reduces the amount of energy developed in the inductor. This can be observed as an increase in the slope of the charging portion of the charge/discharge cycle of the timing capacitor (Figure 5). With current limiting, saturation of the power inductor may be prevented and soft start-up achieved. If not used, the current limit sense should be tied to $V_{CC}+$ (pin-14).

Pass Transistor

The switching transistor provided in the TL497A is a high-gain device designed to switch up to 500 mA peak using the base drive circuitry provided by the TL497A. Access to the internal base current limiting resistor is made available, however, it is not recommended the base drive circuitry be tampered with. The emitter and collector are brought out also, for user versatility.

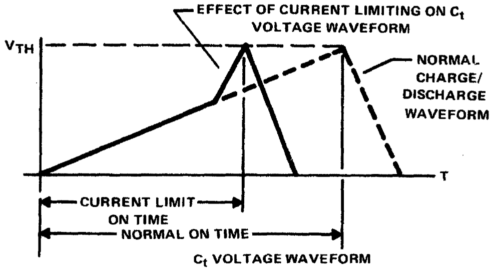


FIGURE 5. C_t Voltage Waveform

Catch Diode

An uncommitted catch diode capable of operating at peak currents to 500 mA is available for commutation and blocking purposes, however, an external diode may be desired for optimum circuit performance.

Enable Circuitry

Shutdown circuitry is provided for external control which allows the user to enable and disable the TL497A by an external TTL logic command. A logic high disables the TL497A and turns off the switching transistor. A logic low enables the TL497A and allows it to operate according to the previous discussion.

DESIGN AND OPERATION
of a
STEP-DOWN SWITCHING VOLTAGE REGULATOR

The circuit in Figure 6 shows the basic configuration for a step-down switching voltage regulator. A thorough understanding of this circuit is necessary to optimize the design of a step-down switching voltage regulator using the TL497A.

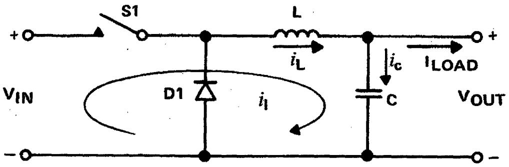


FIGURE 6. Basic Step-Down Regulator

First, define the initial conditions (prior to the closing of S1).

Initial Conditions (t = 0–):

$$V_C = V_{OUT}$$

$$i_L = 0$$

When the switch S1 is closed, the current in the inductor and the voltage across the filter capacitor (C) cannot change instantaneously.

at S1 closed (t = 0+):

$$V_C = V_{OUT}$$

$$i_L = i_1 = 0$$

Writing a loop equation around the circuit

$$V_{in} = R_s i_1 + L \frac{di_1}{dt} + V_c$$

Substituting $i_1 = 0$ and $V_c = V_{out}$ at t = 0+

$$V_{in} = L \frac{di_1}{dt} + V_{out}$$

Therefore $\frac{di_1}{dt} = \frac{V_{in} - V_{out}}{L}$

The current through the inductor (i_L) at any given time (t) is

$$I = \frac{V_{in} - V_{out}}{L} t$$

For a constant V_{IN}, V_{OUT}, and L, I varies linearly with t.

The current increases while S1 is closed according to the waveform shown in Figure 7. The peak current in the inductor, therefore, is dependent on the period of time S1 is closed, which is the on-time of the switch (t_{ON}).

$$\therefore I_{pk} = \frac{V_{in} - V_{out}}{L} t_{ON}$$

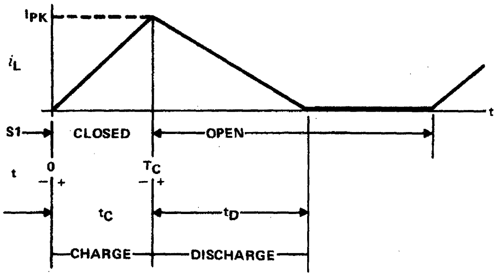


FIGURE 7. Inductor Current Waveform

When S1 opens ($t = t_{C+}$), the current through the inductor is I_{pk} since the current cannot change instantaneously, the voltage across the inductor inverts, and the blocking diode (D1) is forward biased to provide a current path for the discharge of the inductor into the load and filter capacitor. The inductor current then discharges linearly as illustrated in Figure 7.

Prior to S1 open ($t = T_{C-}$)

$$i_L = I_{pk}$$

$$V_C = V_{OUT}$$

At S1 open ($t = T_{C+}$)

$$i_L = I_{pk}$$

$$V_C = V_{OUT}$$

Writing a loop equation for i_1

$$V_f + L \frac{di_1}{dt} + V_C = 0$$

Substituting the conditions at $t = T_{C+}$ and assuming V_f of D1 is 0 V:

$$L \frac{di_1}{dt} = -V_{OUT}$$

∴ the current through the inductor for $t > T_C$

$$i_L = I_{pk} - \frac{V_{OUT}}{L}(t - T_C)$$

The discharge time of the inductor then is that time required for $i_L = 0$. Therefore

$$t_D = \frac{I_{pk}}{V_{OUT}} L$$

Analyzing for a moment the currents at the inductor/capacitor/output node.

$$i_L = i_C + I_{load}$$

if I_{load} is considered constant.

$$\Delta i_C = \Delta i_L = I_{pk}$$

when $\quad i_L = I_{load};\ i_C = 0$

when $\quad i_L = 0;\ i_C = -I_{load}$

Thus the inductor and capacitor current waveforms relate to each other as shown in Figure 8.

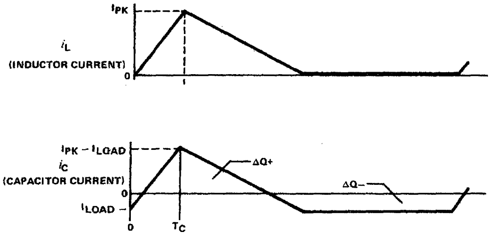


FIGURE 8. Inductor Current and Capacitor Current Waveforms

For the output voltage to remain constant, the net charge delivered to the filter capacitor must be zero. This means that the charge delivered to the capacitor from the inductor must be dissipated in the load. Since the charge developed in the inductor is fixed (constant on time), the time required for the load to dissipate that charge will vary with the load requirements. The actual operating frequency is therefore dependent on the load requirements. The actual frequency can be determined by studying the current waveform of the filter capacitor. The charge delivered to the capacitor and the charge dissipated by the load are equal to the areas under the capacitor current waveform above and below $i_C = 0$ respectively, as shown in Figures 9 and 10.

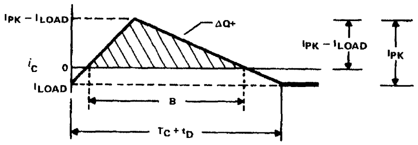


FIGURE 9. Capacitor Current Waveform (ΔQ+)

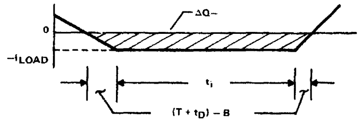


FIGURE 10. Capacitor Current Waveform (ΔQ–)

$$B = \frac{I_{pk} - I_{load}}{I_{pk}}(T_C + t_D)$$

$$\Delta Q+ = \frac{1}{2}\,\frac{(I_{pk} - I_{load})^2}{I_{pk}}(T_C + t_D)$$

$$\Delta Q- = [I_{load}\, t_i] + \frac{1}{2}\left[(T_C + t_D) - \frac{I_{pk} - I_{load}}{I_{pk}}(T_C + t_D)\right] I_{load}$$

Setting ΔQ+ equal to ΔQ– and solving for t_i

$$t_i = \frac{(I_{pk} - 2I_{load})(T_C + t_D)}{2I_{load}}$$

To determine the frequency of oscillation, total the durations of the previous portions of the regulator's cycle,

$$T = T_C + t_D + t_i$$

$$\therefore T = (T_C + t_D)\,\frac{1}{2}\,\frac{I_{pk}}{I_{load}}$$

Knowing the period

$$\text{frequency} = \frac{1}{T}$$

The ΔQ calculations also yield the voltage change experienced by the output capacitor C.

$$V_C = \frac{1}{C}\int i\,dt \text{ or } \frac{\Delta Q}{C}$$

$$\Delta V_C = \frac{1}{2C}\,\frac{(I_{pk} - I_{load})^2}{I_{pk}}\,\frac{T_C V_{IN}}{V_{OUT}}$$

Note this accounts for the ripple voltage contributed by the ripple current present in the switching regulator seen by an ideal capacitor. Realistically the capacitor will have an equivalent series resistance (ESR) which establishes the minimum ripple voltage achievable.

$$V_{RIPPLE\,(MIN)} = I_{pk}\,(ESR)$$

When the filter capacitor size has been increased such that $\Delta V_C \simeq V_{RIPPLE\ (MIN)}$ additional increases in C will net insignificant reduction in V_{RIPPLE}. It is important therefore to employ a filter capacitor with minimal ESR. Note, however, due to its architecture some ripple voltage is required for proper operation of the regulation circuit.

SUMMARY

The previous derivations have assumed that the regulator is operating in the discontinuous mode. This means the inductor current is discontinuous ($I_L = 0$). When the load is continually increased, the idle time (t_i in Figure 10) decreases to the point where the regulator initiates a charge cycle at or before the complete discharge of the inductor. This condition is called the continuous mode of operation (I_L never equals 0, $t_i = 0$). In this mode a dc idle current is passed through the inductor. The TL497A is not designed to operate in this mode without special considerations given to the circuit design. To determine the load current where the circuit transforms from the discontinuous mode to the continuous mode of operation, refer to Figure 8. The point of transition occurs, when the inductor starts charging as soon as it completes the previous discharge cycle ($t_i = 0$). Under these conditions the capacitor current waveform is as shown in Figure 11. Setting $t_i = 0$ and solving for I_{OUT};

$$I_{OUT} = \frac{I_{pk}}{2}$$

Hence $$I_X = \frac{I_{pk}}{2}$$

Where I_X is the load current at which the inductor current is continuous and the regulator enters the continuous mode.

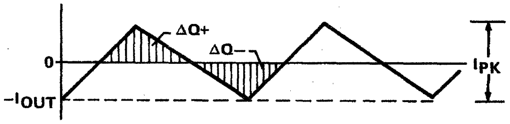


FIGURE 11. Capacitor Current Waveform (Continuous Mode)

Summarizing:

for the step-down switching regulator

$$I_{pk} \geqslant 2\,I_{load} \quad \text{(for discontinuous operation)}$$

$$L = \frac{V_{IN} - V_{OUT}}{I_{pk}}\,t_{ON}$$

$$f_0 = \frac{2\,I_{load}}{I_{pk}}\,\frac{V_{OUT}}{T_{ON}\,V_{IN}}$$

where: $$t_D = \frac{I_{pk}}{V_{OUT}}\,L$$

$$t_i = \frac{[I_{pk} - 2\,I_{load}]}{2\,I_{load}} \cdot \frac{T_{ON}\,V_{IN}}{V_{OUT}}$$

$$C = \frac{(I_{pk} - I_{load})^2}{V_{RIPPLE}\,2\,I_{pk}} \cdot \frac{T_{ON}\,V_{IN}}{V_{OUT}}$$

A STEP-DOWN SWITCHING REGULATOR DESIGN EXERCISE
with
TL497A

A schematic of the basic step-down regulator is shown in Figure 12.

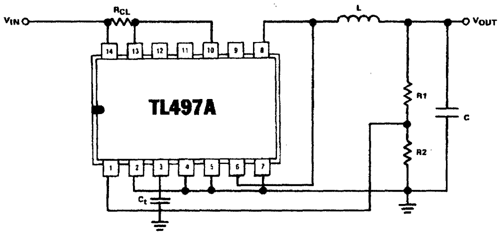


FIGURE 12. Basic Step-Down Regulator

Conditions:

$V_{IN} = 15\ V$

$V_{OUT} = 5\ V$

$I_{OUT} = 200\ mA$

$V_{ripple} < 1.0\%$

Calculations:

$$I_{pk} \geqslant 2\, I_{load} = 400\ mA$$

This is the limit condition for discontinuous operation. For design margin, I_{pk} will be designed for 500 mA which is also the limit of the internal pass transistor and catch diode.

$$\therefore I_{pk} \rightarrow 500\ mA$$

$$L = \frac{V_{IN} - V_{OUT}}{I_{pk}}\, t_{ON}$$

$$L = \frac{10\ V}{500 \times 10^{-3}}\, t_{ON}$$

Recommended on-time is; $19\ \mu s < t_{ON} < 150\ \mu s$, thus the range of acceptable inductance is, 380 µH to 3 mH.

choosing L = 390 µH

$$t_{ON} = \frac{390 \times 10^{-6} \times 500 \times 10^{-3}}{10} = 19.5 \times 10^{-6}\ sec.$$

To program TL497A for 5 V_{OUT}:

$R2 = 1.2\ k\Omega$ (fixed)

$R1 = (5 - 1.2)\ k\Omega = 3.8\ k\Omega$

To set current limiting:

$$R_{CL} = 0.5/I_{limit}$$

$$R_{CL} = \frac{0.5}{500 \times 10^{-3}} = 1\ \Omega$$

For the on-time chosen above, C_t can be approximated;

$$C_t\ (pf) \simeq 12\ t_{ON}\ (\mu s)$$

$$C_t \simeq 240\ pf$$

or it can be selected from Table II, page 5.

To determine C_{filter} for desired ripple voltage:

$$C = \frac{(I_{pk} - I_{load})^2}{V_{RIPPLE}\, 2\, I_{pk}} \cdot \frac{T_{ON}\, V_{IN}}{V_{OUT}}$$

for constant C, V_{RIPPLE} increases as I_{load} descreases.

C = 45 µF (for 200 mA/1% ripple)

The maximum operating frequency is encountered under maximum load conditions.

$$f_{max} = \frac{2\, I_{load}\,(max)}{I_{pk}} \cdot \frac{V_{OUT}}{T_{ON}\, V_{IN}}$$

The minimum operating frequency occurs under minimum load conditions.

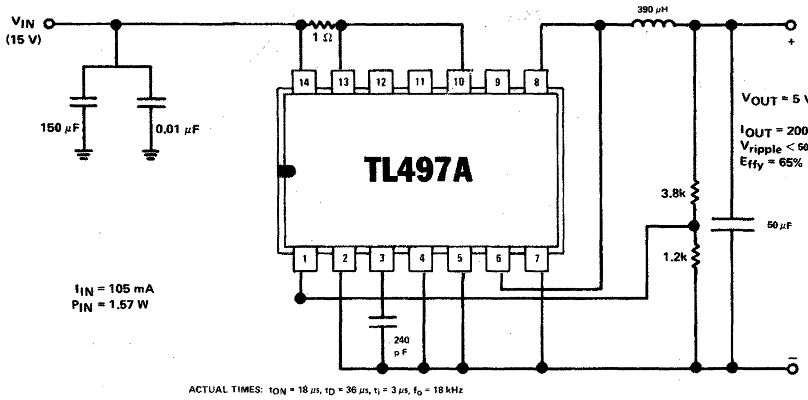
$$f_{min} = f_{max} \frac{I_{load}\,(min)}{I_{load}\,(max)}$$

Figure 13 illustrates the regulator with the above values applied to it.

Waveforms at C_t for indication of proper circuit performance are shown in Figure 14.

For peak currents greater than 500 mA, it is necessary to use an external transistor and diode. Several techniques are shown in Figure 15.

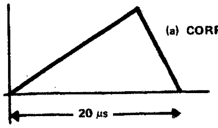
Figure 16 shows the TL497A in high-voltage—high-current applications.



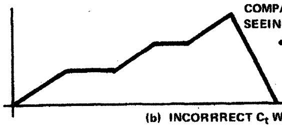
ACTUAL TIMES: t_{ON} = 18 µs, t_D = 36 µs, t_i = 3 µs, f_o = 18 kHz

NOTE: 13 µs ON-TIME RESULTS IN I_{pk} = 433 mA. RECALCULATING t_D, t_i AND f_o WILL CONCUR WITH ACTUAL TIMES OBSERVED.

FIGURE 13. 15 Volt to 5 Volt Switching Regulator for Output Currents to 200 mA



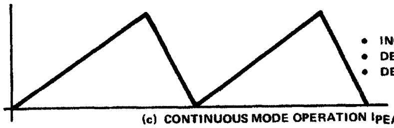
(a) CORRECT C_t WAVEFORM
$t_{on} \approx 15$ µs



COMPARATOR INPUT (PIN 1) IS SEEING NOISE SPIKES.

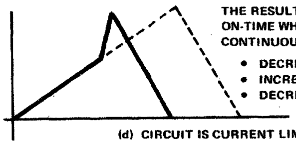
- READ SECTIONS ON VOLTAGE COMPARATOR AND DESIGN VARIATIONS FOR IMPROVED PERFORMANCE.

(b) INCORRRECT C_t WAVEFORM



- INCREASE C_t
- DECREASE LOAD
- DECREASE L

(c) CONTINUOUS MODE OPERATION I_{PEAK} WILL INCREASE.



THE RESULT WILL BE A SHORTENED ON-TIME WHICH MAY RESULT IN CONTINUOUS MODE OPERATION, ALSO

- DECREASE R_{CL}
- INCREASE L
- DECREASE C_t

(d) CIRCUIT IS CURRENT LIMITING.

FIGURE 14. Circuit Performance Waveforms

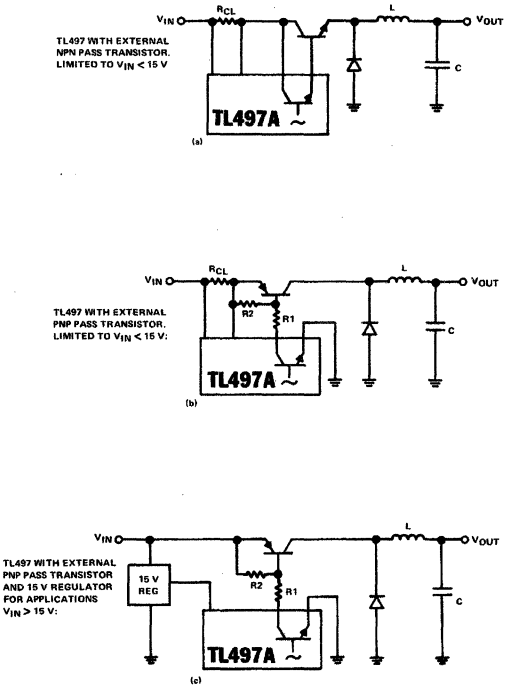
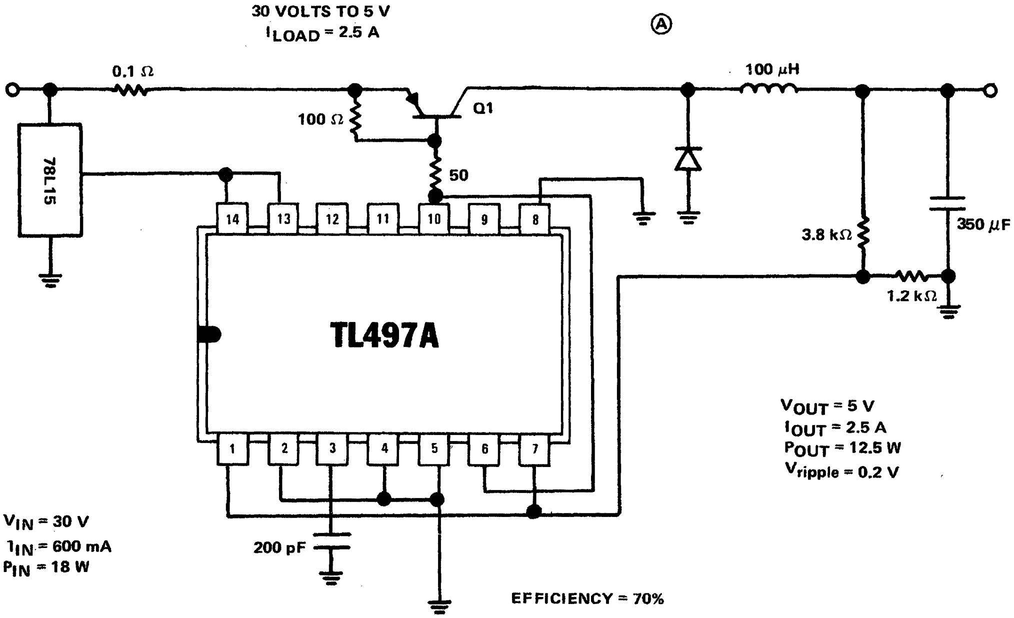


FIGURE 15. Techniques for Obtaining Peak Currents Greater Than 500 mA



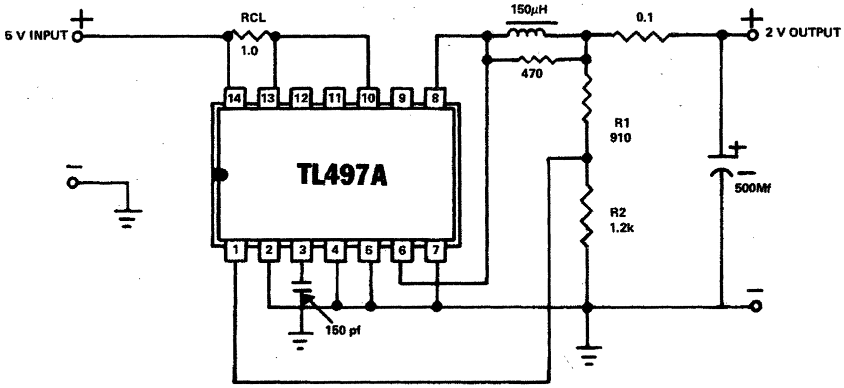
ACTUAL TIMES: $t_c = 20\ \mu s$, $t_D = 80\ \mu s$, $t_i = 10\ \mu s$, f = 9.1 kHz

Ⓐ THE USE OF THE INTERNAL DIODE (PINS 6 AND 7) TO CLAMP THE FEEDBACK AND PROTECT AGAINST NOISE IS DISCUSSED IN A LATER CHAPTER [DESIGN VARIATIONS FOR IMPROVED PERFORMANCE].

FIGURE 16. TL497A in High-Voltage–High-Current Applications

The advent of logic or gate array devices brings about the need of a good regulated low voltage power supply. These arrays may have up to 800 inverters or gates per array. Normally the power requirements are 20 volts at about 200 mA, per array. The input requirement is usually 5.0 volts. This circuits meets the above requirements at an overall efficiency of 72%.

Figure 18 is another step-down regulator. With an input of from 7V to 12V it has an output of 5 volts at 2.0 amps. The TIP34 is a plastic TO-220 PNP transistor of 10 amp capacity. The IN5187D is a 3.0 amp fast recovery diode.



NOTE – ADD .1Mf CAPACITOR AT THE INPUT AND OUTPUT FOR IMPROVED TRANSIENT RESPONSE AND BETTER RIPPLE REJECTION.

FIGURE 17. TL497A Logic Array Power Supply, Step-Down Circuit

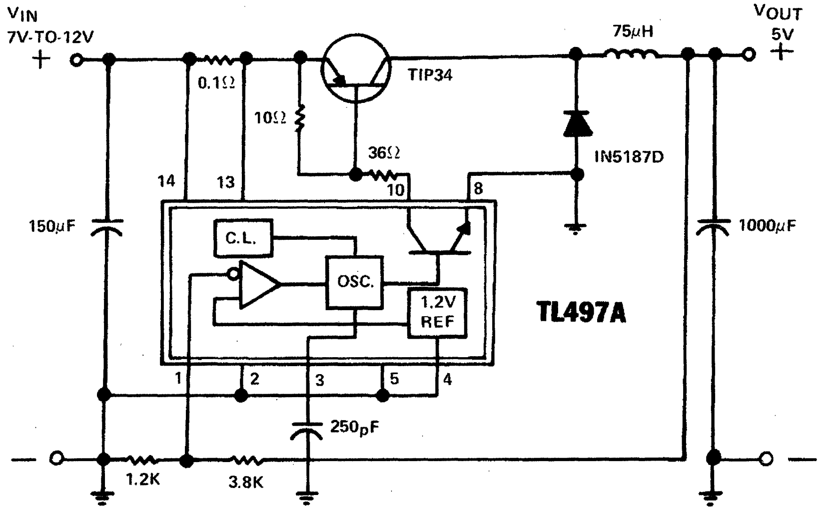


FIGURE 18. Step-Down Regulator

DESIGN AND OPERATION
of a
STEP-UP SWITCHING VOLTAGE REGULATOR

In the step-up regulator, the formulaes change slightly. Note the basic circuit configuration in Figure 19.

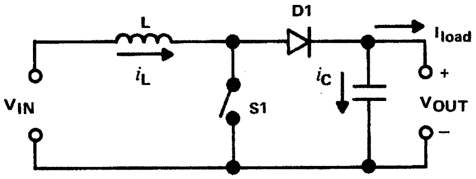


FIGURE 19. Basic Step-UP Regulator Circuit

During the charging cycle (S1 closed) the inductor (L) is charged directly by the input potential.

$$i_L = \frac{V_{IN}}{L} t_C$$

thus

$$I_{pk} = \frac{V_{IN}}{L} t_{ON}$$

In the step-up application however, the peak current is not related to the load current as in the previous application. This is attributed to the fact that during the inductor charge cycle the blocking diode D1 is reverse biased and no charge is delivered to the load. The circuit in Figure 19 delivers power to the load only during the discharge cycle of the inductor (when S1 is open). The diode D1 is forward biased and the inductor discharges into the load capacitor. The potential across the inductor during this phase of the charge/discharge cycle is $V_{OUT} - V_{IN}$. The discharge time of the inductor then becomes:

$$t_D = \frac{I_{pk}}{V_{OUT} - V_{IN}} L$$

To determine the peak current relation to the load current, review the inductor and capacitor current waveforms shown in Figure 20.

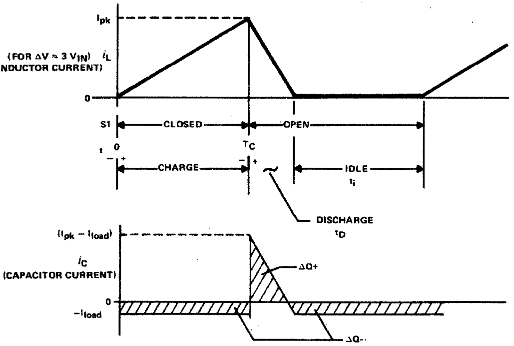


FIGURE 20. Inductor and Capacitor Current Step-Up Regulator

Studying the current waveforms (I_L and I_C) and recalling $\Delta Q+$ must equal $\Delta Q-$ for the potential across the load capacitor to remain constant, the relation of peak current to load current can be determined. Approaching it as ΔQ is the area under the respective curves, maximum load current for discontinuous operation ($t_i = 0$) relates to the peak current as:

$$I_{load} = \frac{I_{pk} t_D}{2(t_D + t_C)}$$

Peak inductor current can be related to load current by:

$$I_{pk} = \frac{2 I_{load}(t_D + t_C)}{t_D}$$

To ease calculation of I_{pk} without prior calculation of t_D, t_C and t_D may be substituted for by their voltage ratios. Equating the charge/discharge times (t_C/t_D), it will be noted that the charge to discharge ratio is proportional to the ratio of the input/output differential to input voltage ratio.

$$\frac{t_D}{t_C} = \frac{V_{IN}}{V_{OUT} - V_{IN}}$$

$$t_D = t_C \frac{V_{IN}}{V_{OUT} - V_{IN}}$$

setting $t_D = 1$

$$t_C = \frac{V_{OUT} - V_{IN}}{V_{IN}}$$

$$\therefore I_{pk} = 2 I_{load} \left[1 + \frac{V_{OUT} - V_{IN}}{V_{IN}} \right]$$

which reduces to:

$$I_{pk} = 2 I_{load} \frac{V_{OUT}}{V_{IN}}$$

From the capacitor current waveform of Figure 20, the remaining performance factors may be determined.

Setting $\Delta Q+$ equal to $\Delta Q-$ and solving for t_i where $I_{load} < I_{load(max)}$ (t_i is not 0).

$$t_i = \frac{I_{pk}\, t_D}{2\, I_{load}} - (t_D + t_C)$$

$$V_{ripple} = \frac{(I_{pk} - I_{load})^2}{2\, C\, I_{pk}}\; T_D$$

Summarizing:

For the step-up voltage regulator

$$I_{pk} = 2\, I_{load} \left[\frac{V_{OUT}}{V_{IN}}\right]$$

$$L = \frac{V_{IN}}{I_{pk}}\, t_{ON}$$

$$f_0 = \frac{2\, I_{load}}{I_{pk}\, t_D}$$

$$C = \frac{(I_{pk} - I_{load})^2}{V_{ripple}\, 2\, I_{pk}} \cdot T_D$$

$$T_D = t_{ON} \left[\frac{V_{IN}}{V_{OUT} - V_{IN}}\right]$$

A STEP-UP SWITCHING REGULATOR DESIGN EXERCISE with TL497A

Figure 21 is the basic step-up regulator using the TL497A.

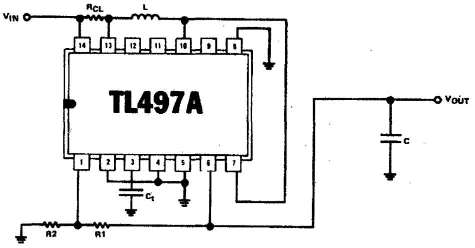


FIGURE 21. Basic Step-Up Regulator Using the TL497A

Conditions:

$$V_{IN} = 5\text{ V}$$

$$V_{OUT} = 15\text{ V}$$

$$I_{OUT} = 75\text{ mA}$$

$$V_{ripple} < 1\%$$

Calculations:

$$I_{pk} \geqslant 2\, I_{load} \left[\frac{V_{OUT}}{V_{IN}}\right]$$

$$I_{pk} \geqslant 450\text{ mA}$$

For design margin $I_{pk} \rightarrow 500$ mA

$$L = \frac{V_{IN}}{I_{pk}}\, t_{ON}$$

$$L = \frac{5}{500 \times 10^{-3}}\, t_{ON}$$

Recommended on-time is; 19 μs $< t_{ON} <$ 150 μs, thus the range of acceptable inductance is; 190 μH to 1.5 mH

choosing L = 200 μH

$t_{ON} = 20\ \mu\text{s}$

To program the TL497:

R2 = 1.2 kΩ

R1 = (15 – 1.2) kΩ = 13.8 kΩ

To set the current limiting:

$$R_{CL} = 0.5/I_{limit}$$

$$R_{CL} = \frac{0.5}{500 \times 10^{-3}} = 1\ \Omega$$

For on-time chosen above (20 μs) C_t can be estimated;

$$C_t\,(\text{pf}) \simeq 12\, t_{ON}\,(\mu\text{s})$$

$$C_t \simeq 240\text{ pF}$$

or it can be selected from Table II, page 5.

To determine C_{filter} for desired ripple voltage

$$C = \frac{(I_{pk} - I_{load})^2\ T_D}{V_{ripple}\ 2\ I_{pk}}$$

$$t_D = t_{ON}\left[\frac{V_{IN}}{V_{OUT} - V_{IN}}\right] = 10\,\mu s$$

$C = 12.0\,\mu F$

The nominal operating frequency f_0 is:

$$f_0 = \frac{1}{T} = \frac{2\ I_{load}}{I_{pk}\ T_D}$$

$f_0 = 30$ kHz

Applying these values to the TL497A results in a schematic as shown in Figure 22.

Figure 23 shows another step-up circuit which will supply 12 volts output at 80 mA with an input of 5 volts.

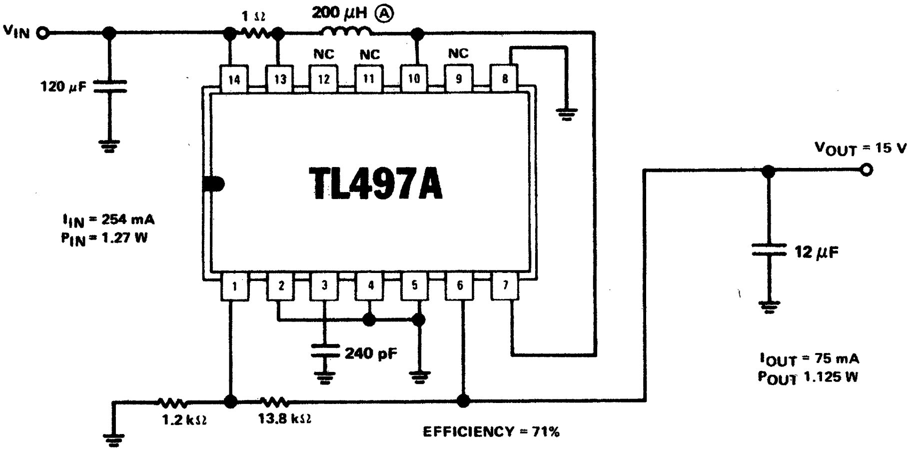


FIGURE 22. 5 Volt to 15 Volt Switching Regulator

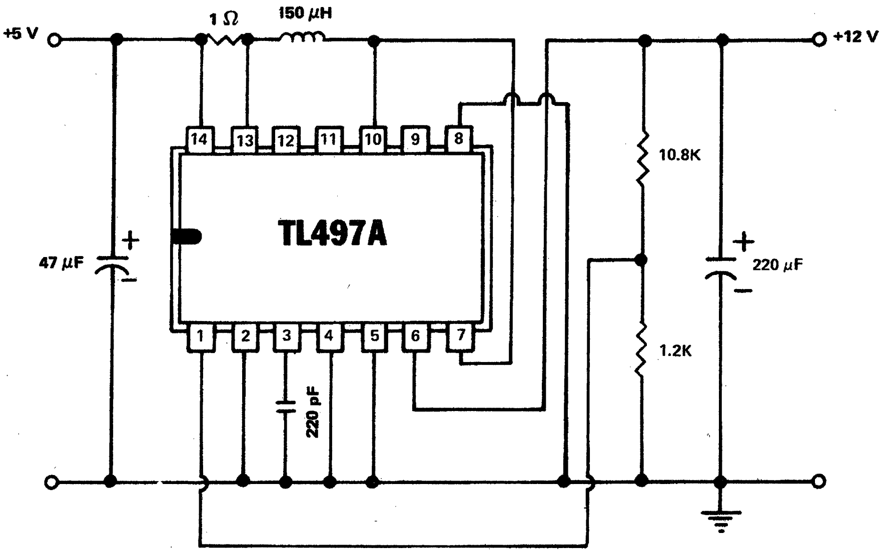


FIGURE 23. TL497A Step-Up Circuit, 5V Input to 12V @ 80mA Output

DESIGN AND OPERATION OF SWITCHING VOLTAGE REGULATOR IN INVERTING CONFIGURATION

The inverting regulator is similar to the step-up regulator in that during the charging cycle of the inductor, the load is isolated from the input. The only difference is in the potential across the inductor during its discharge. This can best be demonstrated by a review of the basic inverting regulator circuit (Figure 24).

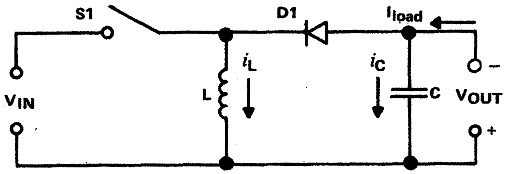


FIGURE 24. Basic Inverting Regulator Circuit

During the charging cycle (S1 closed) the inductor (L) is charged only by the input potential-similar to the step-up configuration.

$$I_{pk} = \frac{V_{IN}}{L}\, t_{ON}$$

Like the step-up configuration, in the inverting configuration (Figure 25) the input provides no contribution to the load current during the charging cycle and thus the maximum load current for discontinuous operation will be limited by the peak current, in accordance with that observed in the step-up configuration.

$$I_L \text{ max (discontinuous)} = \frac{I_{pk}\, t_D}{2\,(t_D + t_C)}$$

The discharge rate (t_D) however differs due to the difference in the potential across the inductor during its discharge which is V_{OUT}.

$$\therefore t_D = \frac{I_{pk}}{|V_{OUT}|}\, L$$

To simplify calculation of I_{pk} from I_{load};

$$I_{pk} = \frac{V_{IN}}{L}\, t_c = \frac{|V_{OUT}|}{L}\, t_D$$

$$\therefore \frac{t_D}{t_C} = \frac{V_{IN}}{V_{OUT}}$$

Substituting this into the expression for I_L max and simplifying;

$$I_{pk} = 2\, I_{load} \left(1 + \frac{|V_{OUT}|}{V_{IN}}\right)$$

The current waveforms in the inverting configuration look identical to those demonstrated in the step-up configuration. The same formulaes therefore apply for t_i, I_L max (discontinuous) and V_{ripple}.

Summarizing:

For the inverting regulator:

$$I_{pk} \geq 2\, I_{load} \left(1 + \frac{|V_{OUT}|}{V_{IN}}\right)$$

$$L = \frac{V_{IN}}{I_{pk}}\, t_{ON}$$

$$f_0 = \frac{2\, I_{load}}{I_{pk}\, t_D}$$

$$C = \frac{(I_{pk} - I_{load})^2}{V_{ripple}\, 2\, I_{pk}} \cdot T_D$$

where:

$$t_D = t_{ON} \frac{V_{IN}}{|V_{OUT}|}$$

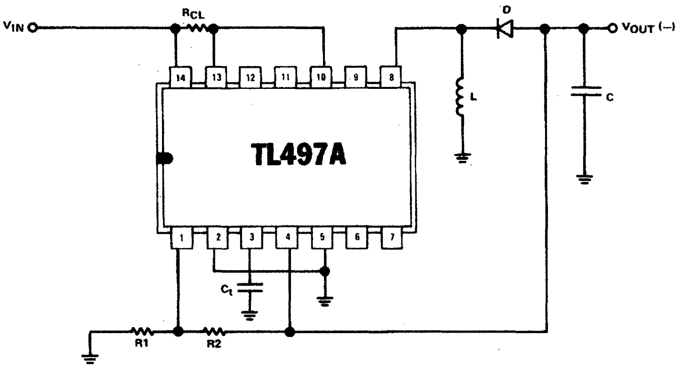


FIGURE 25. Basic Inverting Regulator

AN INVERTING REGULATOR DESIGN EXERCISE with TL497A

Conditions:

$$V_{IN} = 5\ V$$

$$V_{OUT} = -5\ V$$

$$I_{OUT} = 100\ mA$$

Calculations:

$$I_{pk} \geqslant 2\ I_{load} \left(1 + \frac{|V_{OUT}|}{V_{IN}}\right)$$

$$I_{pk} \geqslant 400\ mA$$

For design margin $I_{pk} \rightarrow 500$ mA

$$L = \frac{V_{IN}}{I_{pk}}\ t_{ON}$$

$$L = \frac{5}{500 \times 10^{-3}}\ t_{ON}$$

Recommended on-time: 19 μs $< t_{ON} <$ 150 μs, thus the range of acceptable inductance is; 190 μH to 1.5 MH

choosing L = 200 μH

$t_{ON} = 20\ \mu s$

To program the TL497:

R2 = 1.2 kΩ

R1 = (5 – 1.2) = 3.8 kΩ

To set the current limiting:

$$R_{CL} = 0.5/I_{limit}$$

$$R_{CL} = \frac{0.5}{500 \times 10^{-3}} = 1\ \Omega$$

For the t_{ON} chosen above (20 μs) C_t can be estimated;

$$C_t\ (pf) \simeq 12\ t_{ON}\ (\mu s)$$

$$\therefore C_t = 240\ pF$$

or it can be selected from Table II, page 5.

To determine C_{filter} for desired ripple voltage:

$$C = \frac{(I_{pk} - I_{load})^2}{V_{ripple}\ 2\ I_{pk}} \cdot T_D$$

$$t_D = t_{ON} \frac{V_{IN}}{V_{OUT}} = 20\ \mu s$$

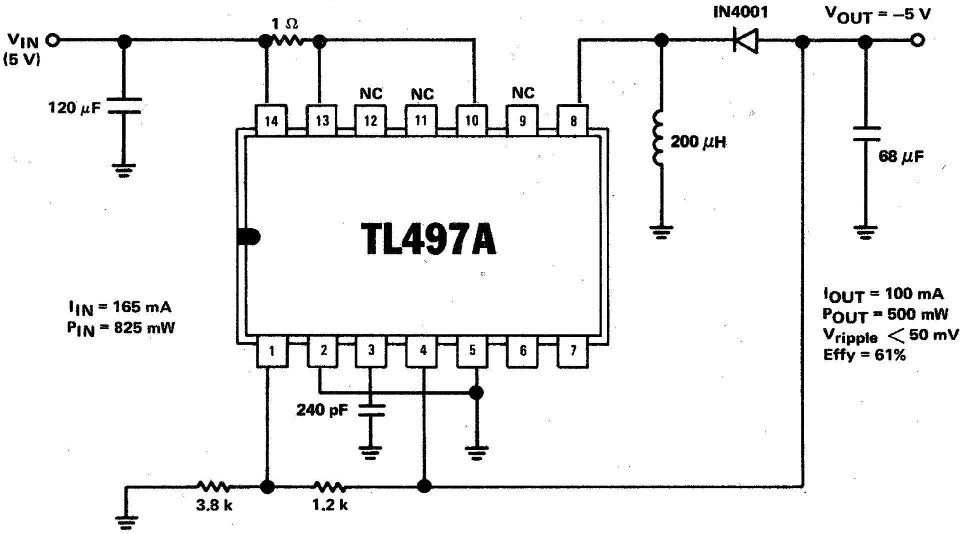
$$C_{filter} = 64\ \mu F$$

The nominal operating frequency f_0 is:

$$f_0 = \frac{2\ I_{load}}{I_{pk}\ T_D}$$

$$f_0 = 20\ kHz$$

Applying these values to the TL497A will give results as shown in Figure 26.



*NOTE – DO NOT USE INTERNAL DIODE (PINS–6, 7) FOR CATCH DIODE ON AN INVERTING CIRCUIT.

FIGURE 26. +5 Volt to –5 Volt Switching Regulator

SPECIAL TL497A CIRCUITS

The following are several TL497A circuits that do not fall strictly in a step-up or step down category but rather a combination of both types.

Figure 27 is an automotive power supply built to supply 8.5 volts regulated to power a microprocessor board. During low voltage conditions (4 volts) it acts as a step-up circuit producing about 11 volts at the positive side of the 1000 µF capacitor. When a high voltage condition exists (15 volts) it acts as a step-down circuit still giving about 11 volts to the capacitor. This 11 volts then is regulated to the desired 8.5 volts by a µA 7885 3-terminal regulator.

Figure 28 is a dual output circuit producing both a +12V and –12V from a +5 volt input to the supply. While not supplying a large amount of current it will put out about 12 mA of current of each voltage polarity.

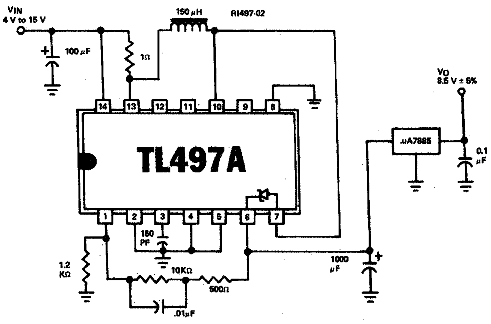


FIGURE 27. 12V To 8.5V Step-Up/Down Circuit

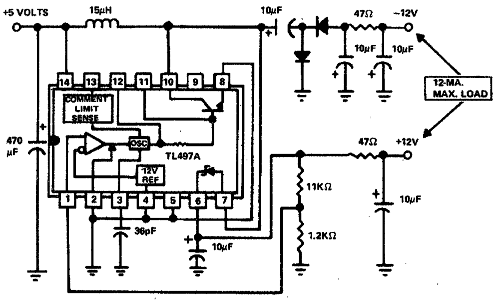
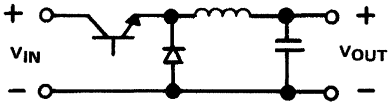


FIGURE 28. TL497A Dual Supply
+12 Volts and –12 Volts From +5 Volts

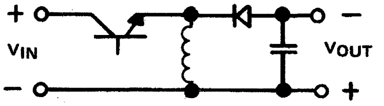
DESIGN VARIATIONS FOR IMPROVED PERFORMANCE

Improving Efficiency

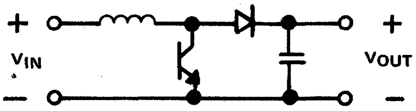
The dominant contribution by the TL497A to the overall efficiency of the switching regulator is the V_{CE} (SAT) of the transistor switch. Recall, the previous sections have considered the switch to be ideal ($V_{CE\ (SAT)} = 0$ V), this is not the case in the real world. As the V_{CE} (SAT) increases the circuit efficiency decreases. Consider for a moment the basic architecture of the three applications presented herein (see Figure 29).



STEP-DOWN REGULATOR



INVERTING REGULATOR



STEP-UP REGULATOR

FIGURE 29. Basic Regulator Architectures

Note in all but the step-up regulator the switching transistor is applied to the positive input rail. In these configurations it is impossible to drive the NPN transistor switch into saturation since its base drive circuit resides at a potential lower than its collector potential. Improved performance can be achieved by using an external PNP transistor driven by the internal NPN. (See Figure 30(a, b).)

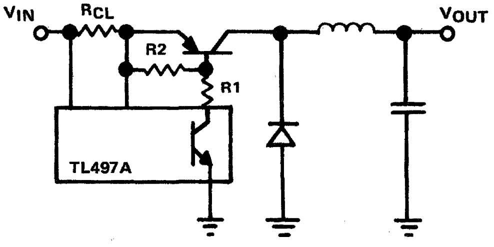
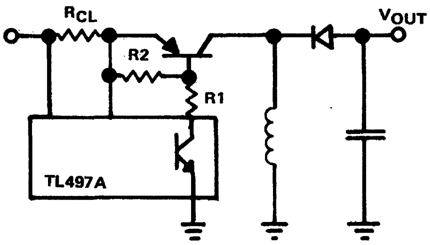


FIGURE 30(a). Step-Down Regulator



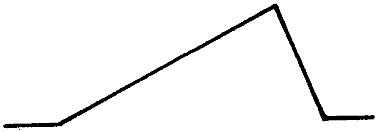
INVERTING REGULATOR

$$R1 = \frac{(V_{IN} - 1.5)\, h_{FE}}{I_{pk}} \qquad R2 = \frac{10R1}{V_{IN} - 1.5}$$

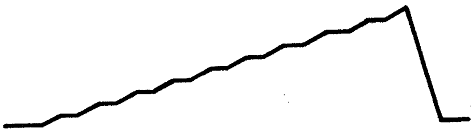
FIGURE 30(b). TL497A With External PNP Switch For Improved Performance

Improving on Time Stability

The on time is determined by the timming capacitor (C_T) and its associated circuitry. The on time cycle (charging of C_T) is initiated when the voltage at the feedback input (pin 1) is less than 1.2 volts. During the on time as the timming capacitor is being charged to its internally prescribed peak voltage, the error comparator remains active. If during this period the feedback voltage is increased above 1.2 volts, the on-time cycle will be interrupted. This condition can be the result of a noise spike fed back when the switching transistor turns on. The resulting C_T waveform is as illustrated in Figure 31.



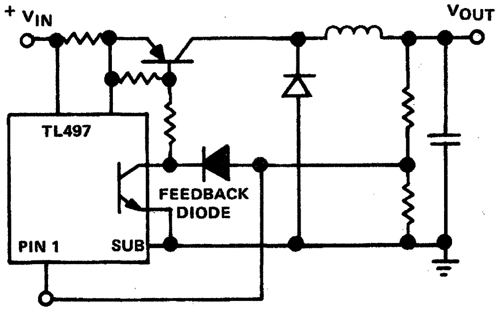
CORRECT WAVEFORM



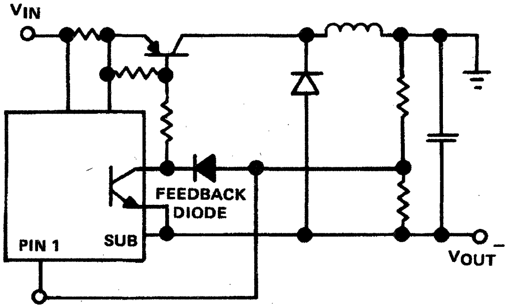
INTERRUPTED WAVEFORM

FIGURE 31. C_T Waveforms

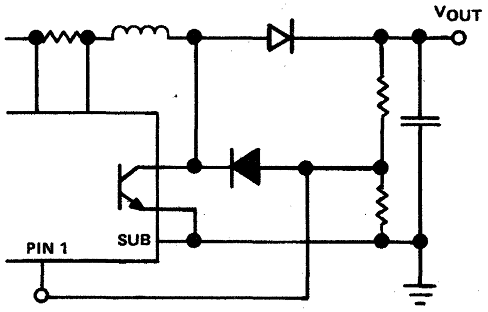
Note the appearance of the charging ramp of the C_T waveform. It can appear as a few easily defined steps or as numerous, almost undetectable, smaller steps. Another evident condition of the presence of this problem is a jittering on time. This severely degrades the efficiency of the converter circuit as power is lost during each transition of the switching transistor. Solution of this problem is quite simple, clamp the feedback node (pin 1) to less than 1.2 volts during the on-time cycle. Figure 32 shows how this can easily be accomplished with the addition of a single feedback diode.



STEP-DOWN REGULATOR



INVERTING REGULATOR



STEP-UP REGULATOR

FIGURE 32. Basic Regulator with Feedback Diodes

The function of the feedback diode is simple. When the on-time cycle is initiated, the internal switching transistor turns on. Note that in all three configurations of Figure 32 the emitter of the internal switch is tied to the substrate pin [ground or V_{OUT} (–)]. When the internal switch turns on, the feedback diode is forward biased and the feedback signal is clamped at approximately 0.8 volt ($V_{CE\ (SAT)} \sim 0.3$ V, $V_F \sim 0.5$ V), which is less than the 1.2 volts reference. Voltage spikes or noise appearing at the output will not be reflected at pin 1 as the diode clamp holds the feedback at 0.8 volt. Thus a clean on-cycle will result. At the conclusion of the on cycle, the internal switch turns off the diode reverse biases and the feedback voltage returns to its voltage prescribed by the resistor ladder and V_{OUT}. If not used as the flyback diode the internal diode is quite satisfactory for this application.

Ringing

An oscilloscope is a must when building a switching power supply with this or any other circuit. It is good to first obtain the correct waveform on the oscillator ramp (pin # 3). (See Figure 32 and Figure 14.) Next look at the switched waveform on the collector of switch (pin 10). See Figure 33. These must be correct or the circuit will not function properly. If ringing is noticed on the switched waveform (pin 10) it can be reduced by placing a 470 to 1000 ohm resistor directly across the inductor to more rapidly dump the coil current when the switch is off.

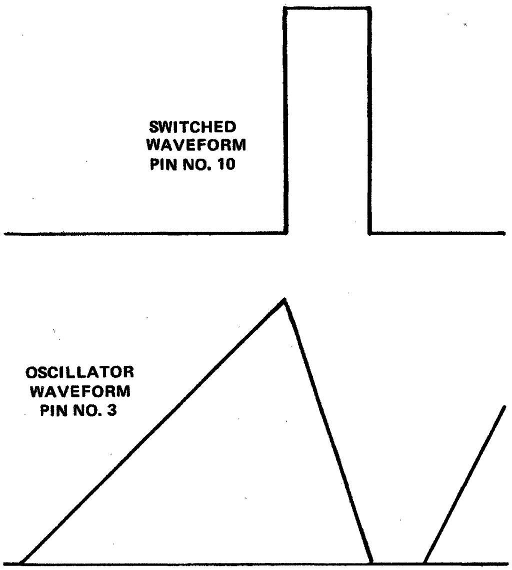


FIGURE 33.

EXTENDED VOLTAGE OPERATION

It is sometimes desirable to operate the TL497A from a voltage higher than the maximum voltage rating of 15.0 volts as per the specification. This may be accomplished with few parts, chiefly a TL783 regulator and a diode as shown in Figure 34. The TL783 output voltage chosen should be lower than the output voltage of the supply. The TL783 will provide a reference voltage to the TL497A until the V_{OUT} comes up. D_{FB} then forward biases, thus supplying the TL497A and shutting back the TL783 regulator. The residual power consumption is only about 5.0 mA in the TL783 circuit.

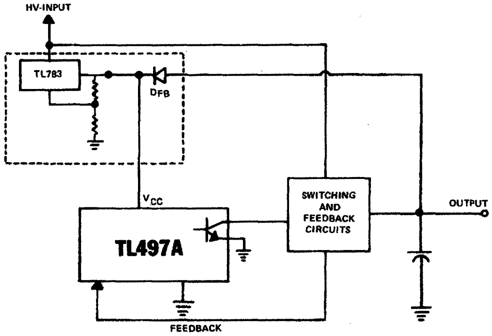
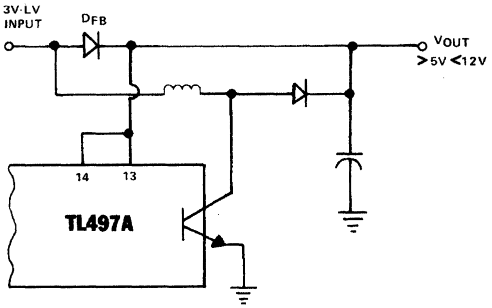


FIGURE 34.

LOW VOLTAGE OPERATION

In some occasions there is a need to operate from a voltage lower than the minimum voltage rating of the TL497A which is 4.5 volts. Since the oscillator will run with less than 3 volts V_{CC}, regulation may be accomplished with a circuit similar to Figure 35. With the application of 3 volts, the diode D_{FB} forward biases furnishing V_{CC} to the oscillator of the TL497A. This causes the switching transistor to operate and steps the voltage up to its designed output. (4.5 V – 15 V) Once V_{OUT} comes up higher than 3.0 volts, D_{FB} is reversed biased and V_{CC} to the TL497A is now furnished by its own output voltage.



NOTE-1 - SINCE ONLY THE OSCILLATOR SECTION WILL FUNCTION ON A 3.0 VOLT SUPPLY, THE REMAINDER OF THE CHIP IS INOPERATIVE. THE COMPLETE CIRCUIT WILL FUNCTION WHEN V_{OUT} REACHES ABOUT 4.5 VOLTS.

FIGURE 35.

SWITCHING REGULATOR DESIGN TIPS

The TL497A being a fixed on-time, variable frequency device does not need a "HI-Q" type of inductor.* "HI-Q" coils are not desirable due to the TL497A's broad frequency range of operation. If the "Q" is too high, excessive ringing will occur on the output pulse. If when using a coil with a typical "Q" of greater than 10 ringing does occur, a shunt resistance may be placed across the coil to dampen the waveform.

While not necessary, it is highly desirable to use a toroid inductor as opposed to a cylindrical wound coil. The toroid type of winding helps to contain the flux closer to the core and reduce the possible radiation from the supply. A typical inductor of 150 μH inductance and capable of handling 0.5 amperes of current would have a D.C. resistance of about 0.6 Ω. Below is a list of possible inductor sources.

Care should be used in placement of parts and routing of ground connections similiar to practices used in constructing R.F. circuits. These technique's will help to prevent unwanted oscillations due to positive feedback or ground loops.

*NOTE: See page 22 for possible inductor sources.

INDUCTOR SOURCES*

Reliability, Inc.
P.O. Box 218370
Houston, TX 77218
(713) 492-0550

Coil Craft
1102 Silver Lake Rd.
Cary, Ill 60013
(312) 639-2361

Mini-Magnetics
453 Ravendale Dr. Unite E
Mountain View, CA 94043
(408) 255-7160

Ferroxcube
5083 Kings Highway
Saugerties, N.Y. 12477
(914) 246-2811

Pulse Engineering, Inc.
P.O. Box 12235
San Diego, CA 92112
(714) 279-5900

TRW Inductive Products
Mr. Austin Profeta
150 Varick St.
New York, N.Y.
(212) 255-3500

West Coast Magnetics, Inc.
140 San Lazaro
Sunnyvale, CA 94086
(408) 733-9853

Microtran Company, Inc.
145 E. Mineola Avenue
P.O. Box 236
Valley Stream, N.Y. 11582
(516) 561-6050

Cambion
445 Concord Ave.
Cambridge, MA 02138
Telex: 92-1480
(617) 491-5400

South Haven Coil, Inc.
P.O. Box 409 Blue Star Highway
South Haven, Michigan 49090
AC 616 #637-5201

*Texas Instruments does not endorse or warrant the suppliers referenced.

APPENDIX

Tables 1 and 2 illustrate the operating range of the TL497A without the addition of an external power transistor. Standard inductor values have been used giving maximum operating frequencies (discontinuous mode) in the range 9 kHz – 103 kHz. Worst case figures for transistor on-state voltage, $V_{CE\ (SAT)}$, and diode forward voltage drop, V_f, have been assumed throughout giving a conservatively rated output current, I_O (max), in the majority of cases.

Input Voltage V_{in} (V)	Output Voltage V_o (V)	Output Current I_{max} (mA)	Power Transfer P_{max} (W)	Feedback Resistors R1 R2	Inductor L (μH)	Timing Capacitor Ct (pF)	Operating Frequency f_{max} (kHz)
5.0 4.75	6	152 143	0.91	4.8K 1.2K	150	220	18.9
5.0 4.75	12	79 74	0.95	10.8K 1.2K	150	220	33
5.0 4.75	15	64 60	0.96	13.8K 1.2K	150	220	35.7
5.0 4.75	18	53 50	0.95	16.8K 1.2K	150	220	38.5
5.0 4.75	24	40 38	0.96	22.8K 1.2K	150	220	40
5.0 4.75	30	32 30	0.96	28.8K 1.2K	150	220	41.7
5.0 4.75	-5	96 90	0.48	3.8K 1.2K	150	220	30
5.0 4.75	-12	57 54	0.68	10.8K 1.2K	150	220	37
5.0 4.75	-24	34 32	0.82	22.8K 1.2K	150	220	41.7

The following assumptions have been made:

1. Power switch operation at maximum peak current.
2. Worst case transistor and diode conduction losses.
3. Use of standard 150 μH inductor and 220 pF timing capacitor.

Note: The 30V and -24V supplies will not give the full output in the worst case since the ratio tc/tc + td exceeds the maximum limit of 0.85 defined by the I.C.

Table 1. TL497A Operation from a 5 V Supply

Input Voltage V_{in} (V)	Output Voltage V_o (V)	Output Current I_{max} (mA)	Power Transfer P_{max} (W)	Feedback Resistors R1 R2	Inductor L (μH)	Timing Capacitor Ct (pF)	Operating Frequency f_{max} (kHz)
12	5	250	1.2	3.8K 1.2K	256	220	22.7
12	10	250	2.5	8.8K 1.2K	73	220	45.5
12	15	180	2.7	13.8K 1.2K	439	220	9.8
12	18	151	2.7	16.8K 1.2K	439	220	16.5
12	24	114	2.7	22.8K 1.2K	439	220	24.9
12	30	91	2.7	28.8K 1.2K	439	220	29.8
12	-5	159	0.8	3.8K 1.2K	439	220	14.5
12	-12	114	1.4	10.8K 1.2K	439	220	24.9
12	-24	76	1.8	22.8K 1.2K	439	220	33.2

Note: Use a standard 220 pF timing capacitor. The assumptions of maximum peak current operation and worst case transistor and diode losses apply.

Table 2. TL497A Operation from a 12 V Supply.

Designing With the TL5001 PWM Controller

TEXAS
INSTRUMENTS

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ABSTRACT

Electrical and electronic products today are required to be lighter and smaller, use less power, and cost less. Because of these requirements, manufacturers are turning more and more to small high-frequency dc-to-dc converters for power-supply solutions. The TL5001 is a pulse-width-modulation (PWM) control integrated circuit, which with a few external components can be used to implement such converters that can operate at frequencies up to 400 kHz.

INTRODUCTION

The TL5001 integrated circuit incorporates all the PWM-control functions in a compact 8-pin package, including:

- Oscillator/triangle-wave generator
- PWM comparator with adjustable dead-time control input
- Open-collector output-drive transistor
- 1-V temperature-stable reference
- Wide-bandwidth error amplifier
- Short-circuit protection (SCP)
- Undervoltage lockout (UVLO)

In addition, the TL5001 operates over a 40-kHz to 400-kHz frequency range with supply voltages ranging from 3.6 V to 40 V and typically consumes only 1 mA of supply current.

This application report demonstrates the design of three simple step-down (buck) converters. The designs include: two converters operating from 12 V and delivering 5 V at 3 A, 3.3 V at 3 A, and one that operates from 5 V and delivers 3.3 V at 0.75 A, using the TL5001 and a few external components.

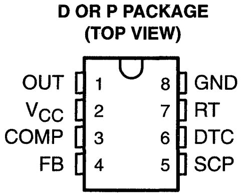
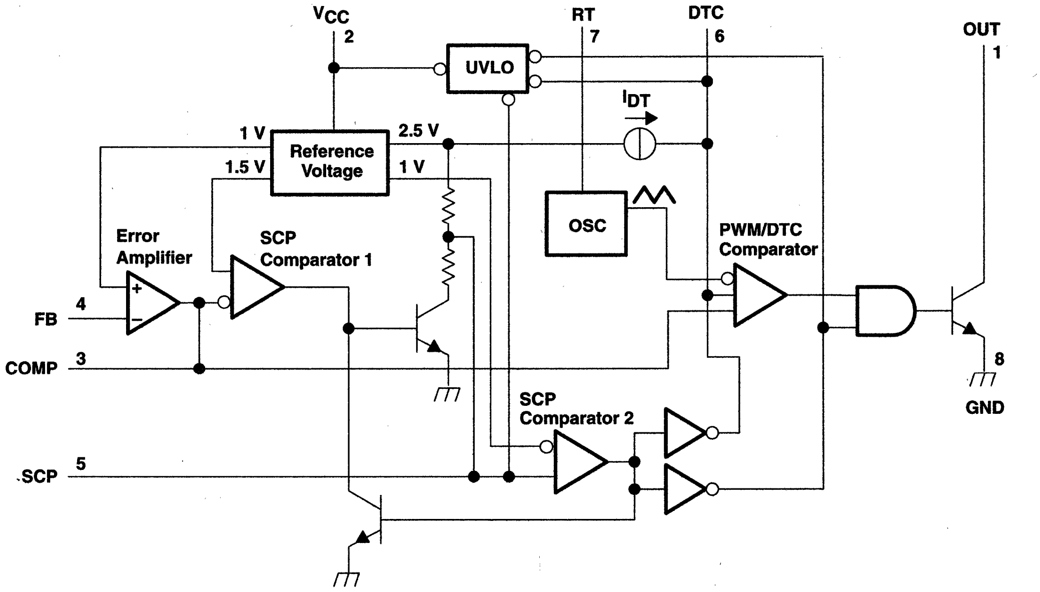


Figure 1. Package Layout



SCP = Short-circuit protection
UVLO = Undervoltage lockout protection

Figure 2. Functional Block Diagram

EXAMPLE 1: 12-V to 5-V at 3-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 8.

Specifications

Input voltage range, V_I	10 V to 15 V
Output voltage, V_O	5 V
Output current, I_O	0 A to 3 A
Output ripple voltage	≤50 mV
Regulation	1%
Efficiency	≥80%
Ambient temperature range, T_A	0°C to 55°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down converter operating at 200 kHz.

Duty-Cycle Estimates

Before starting the detailed design, it is useful to estimate the duty cycle, D (ratio of the power-switch conduction time to the period of the operating frequency), for various input voltages. The duty cycle for a step-down converter operating in continuous mode is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume $V_d = 0.6$ V)

V_{sat} = power-switch conduction voltage (assume $V_{sat} = 0.5$ V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for $V_I = 10$, 12, and 15 V is 0.59, 0.49, and 0.39, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose the inductance value to maintain continuous-mode operation down to 10% of rated output current.

$$\Delta I_O = 2 \times 0.1 \times I_{O(max)} = 2 \times 0.1 \times 3 = 0.6 \text{ A peak-to-peak}$$

The ripple current is simply the product of the inductor voltage and t_{on}, the power-switch conduction time, divided by the inductor value.

$$\Delta I_O = \frac{V_{ind} \times t_{on}}{L1} = \frac{V_{ind}\ DTs}{L1}$$

where Ts = period of the converter operating frequency.

The inductor voltage during t_{on} is the input voltage minus V_{sat}, the power-switch conduction voltage, minus the output voltage. Solving for L1,

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)(D)\ (t)}{\Delta I_O} = \frac{(15 - 0.5 - 5)\ (0.39)\ \left(5 \times 10^{-6}\right)}{0.6} = 30.87\ \mu H$$

Because the core is too large, there are not many off-the-shelf surface-mount devices for this design. A 27-µH inductor (27 turns of 22-gauge magnet wire on a Micrometals T50-26B powdered-iron toroid) was selected because it was readily available.

Output-Filter-Inductor Selection

Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficently high.

Capacitor

The output capacitor is selected to limit ripple voltage to the level required by the specification. The three elements of the capacitor that contribute to ripple are: equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance. Normally, in designs of this type, it is necessary to provide a great deal of capacitance to get ESR to acceptable levels. ESL, which can be a problem at high frequencies, can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

Assuming all the inductor ripple current flows through the filter capacitor and the ESR is zero, the capacitance needed to limit the ripple to 50 mV peak-to-peak is:

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.6}{(8)\left(200 \times 10^3\right)(0.05)} = 7.5\ \mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.6} = 83\ m\Omega$$

Capacitor ripple current is seldom a problem in low-voltage converters unless a large number of devices are paralleled. However, to be on the safe side, the rms current is established as:

$$\Delta I_{O(rms)} = 0.6 \times 0.289 = 0.17\ \text{Arms}$$

The output-filter capacitor(s) should be rated for: at least ten times the calculated minimum capacitance, an ESR 30% to 50% lower than the calculated maximum, a 0.5-Arms-or-greater ripple-current rating at 100 kHz and 85°C, and a 7.5-V or greater voltage rating.

Use one 220-µF 10-V OS-CON SA-series device, even though it is in a lead-mounted radial package. The ESR is 35 mΩ (at 100 kHz) and the 85°C ripple-current rating is 2.36 Arms. Where package height and/or surface-mount packaging is critical, two solid tantalum-chip 100-µF 10-V devices with 100-mΩ ESR and 1.1-Arms ripple-current rating from either the AVX TPS series or the Sprague 593D series connected in parallel work well.

Output-Filter-Capacitor Selection

Three capacitor technologies: low-impedance aluminum, organic semiconductor, and solid tantalum, are suitable for low-cost commercial applications such as this one. Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but ESR is higher than the other two and there are currently no surface-mount devices suitable for this application. Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds – a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

Power-Switch Design

The power-switch design includes: selecting the power switch, catch rectifier, and rectifier-snubbing network (if needed), calculating power dissipations and junction temperatures, and ensuring the semiconductors have proper heat sinking.

Power Switch

The design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. Based on the preliminary estimate, $r_{DS(on)}$ should be less than 0.5 V ÷ 3 A = 167 mΩ with a 10-V gate drive and the drain-to-source breakdown voltage appropriate for a 15-V supply. Surface-mount packaging is also desirable.

The IRF9Z34S is a 60-V p-channel MOSFET in a power surface-mount package with $r_{DS(on)}$ = 140 mΩ maximum with a 10-V gate drive.

Power dissipation, which includes both conduction and switching losses, is given by:

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

Where t_{r+f} = total MOSFET switching time (turn-on and turnoff) and $r_{DS(on)}$ is adjusted for temperature.

Assuming the drive circuit is adequate for t_{r+f} = 100 ns and the junction temperature is 125°C with a 55°C ambient, the $r_{DS(on)}$ adjustment factor is 1.6.

$$P_D = \left(3^2\right)(0.14 \times 1.6)(0.59) + (0.5)(10)(3)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)$$

$$P_D = 1.19 + 0.30 = 1.49 \text{ W}$$

Conduction losses are dominant in this application but may not be in others. It is good practice to check dissipation at the extreme limits of input voltage to find the worst case.

The thermal impedance $R_{\theta JA}$ = 40°C/W for FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (40 \times 1.49) = 115°C$$

Bipolar Versus MOSFET Power Transistors

Each of the three designs presented in this report could be implemented with bipolar or MOSFET transistors as the power switch. Bipolars are inexpensive and can perform well in low-voltage applications such as these, but designing a drive circuit to realize the performance is not a trivial effort. Furthermore, complex base-drive schemes can eliminate much, if not all, of the cost advantage. MOSFETs were selected for this application because the fast switching times required for high-frequency operation are acheived with relatively simple, low-component-count gate drive circuits, and the focus in this report is the controller design.

Catch Rectifier

The catch rectifier conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low-forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low-voltage outputs is usually a Schottky rectifier.

The breakdown voltage must be 20 V or greater to handle the 15-V input; the current rating must be at least 3 A (normally the current rating will be much higher than the output current because the power limits the number of acceptable devices); and a surface-mount package is extremely desirable.

The 50WQ03F is a 5.5-A, 30-V Schottky in a DPAK, power surface-mount package. Care must be taken to ensure that the rectifier maximum junction temperature is not exceeded. The first step in determining the rectifier junction temperature is to estimate worst-case power dissipation. Neglecting leakage current and assuming the ripple current in the inductor is much less than the output current, the catch-rectifier power dissipation is:

$$P_D = I_O \times V_d \times (1 - D)$$

where V_d is the rectifier conduction drop. Worst-case dissipation occurs at high line where D is minimum. The 50WQ03F has a maximum forward drop of 0.55 V at a forward current of 3 A and a junction temperature of 125°C.

$$P_D = 3 \times 0.55 \times (1 - 0.39) = 1 \text{ W}$$

The thermal impedance $R_{\theta JA}$ = 50°C/W when mounted on FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (50 \times 1) = 105°\text{C}$$

Catch-Rectifier Snubber Network

Step-down converters almost universally suffer from ringing on the voltage waveform at the node where the power-switch drain, output inductor, and catch-rectifier cathode connect. The ringing, which results from driving parasitic inductances and capacitances with fast rise-time waveforms, ranges in severity from objectionable to unacceptable depending on component selection and PCB layout. An RC-snubber damping network in parallel with the catch rectifier is by far the simplest way to minimize or eliminate the problem. Since deleting components from a printed-circuit layout is usually easier than adding them, the safest strategy is to include the network in the initial design and delete the components if they prove unnecessary.

The initial design is straightforward, but the PCB layout may necessitate component-value adjustments during the prototype phase. The capacitor value chosen is 4 to 10 times greater than the rectifier junction capacitance; higher values improve the snubbing but dissipate more power. The 50WQ03F has a typical junction capacitance of 180 pF, and a snubber-capacitor value should be between 750 pF and 1.8 nF. Use C8 = 1.2 nF for convenience. Rectifiers normally ring in the range from 1 to 50 MHz. Choose the snubber resistor, R10, for a 50-ns time constant:

$$R10 = \frac{50 \times 10^{-9}}{C8} = \frac{50 \times 10^{-9}}{1.2 \times 10^{-9}} = 41.7\ \Omega \Rightarrow \text{Use } 43\ \Omega$$

Because the capacitor is charged and discharged each cycle, the power dissipation in R10 is:

$$(2)(C8)\left(V_I{}^2\right)\left(\frac{f_s}{2}\right) = (2)\left(1.2 \times 10^{-9}\right)\left(15^2\right)\left(\frac{200 \times 10^3}{2}\right) = 54 \text{ mW}$$

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, the dead-time control voltage, the soft-start timing, and the short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

Resistance value R1 is selected to set the oscillation frequency to 200 kHz. Select R1 = 43 kΩ from the graph shown in Figure 3.

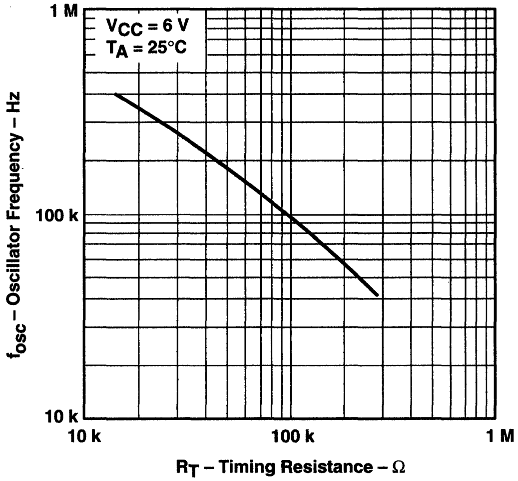


Figure 3. Oscillator Frequency Versus Timing Resistance

Dead-Time Control

Dead-time control provides a minimum period of time during each cycle when the power switch cannot be on; i.e., it limits the duty cycle to some value less than 100%. Even though dead time is not necessary in this application, a small amount is provided to minimize the surge current that would result from a short circuit while the protection circuit is timing out.

The dead time is set by connecting a resistor, R2, between DTC and GND. A constant current I_{DT} flows out of DTC generating a voltage, V_{DT}. I_{DT} is controlled by the current I_T that flows out of RT (this current is normally equal to I_T, but varies slightly with frequency and the peak amplitude of V_{DT}). The maximum duty cycle is 0.59. Typically, the actual duty cycle is set slightly higher to allow for parameter tolerances. For this design, a duty cycle of 0.70 is chosen. See Figure 4 to find the maximum and minimum ramp-voltage levels, $V_{O(100\%)}$ and $V_{O(0\%)}$; R2 is calculated from the following expression (R_{DT}, R_t in kΩ, D in decimal):

$$R2 = (R1 + 1.25)\left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right]$$

$$= (43 + 1.25)[0.7(1.4 - 0.6) + 0.6] = 51.3\ k\Omega$$

A value of 51 kΩ is used for R2.

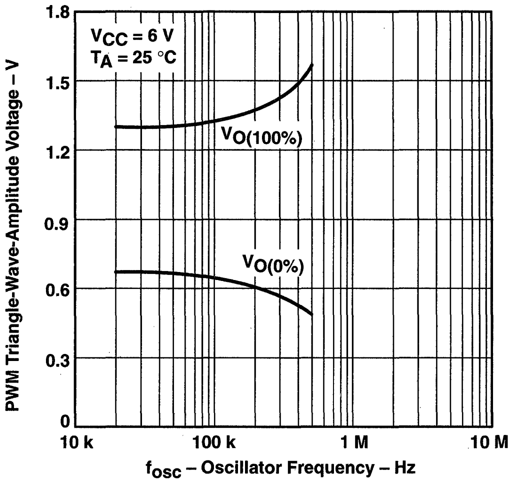


Figure 4. PWM Triangle-Wave-Amplitude Voltage Versus Oscillator Frequency

Soft-Start Timing

Soft start is implemented by adding a capacitor in parallel with the dead-time control resistor, R2. A start-up time of 5 ms is chosen.

$$C5 = \frac{t_r}{R2} = \frac{5 \times 10^{-3}}{51 \times 10^3} = 0.1 \ \mu F$$

SCP Timing

In normal operation, SCP and the timing capacitor, C4, are clamped to approximately 185 mV. Under short-circuit conditions, C4 is allowed to charge. If the voltage across C4 reaches 1 V, the SCP latch is activated and the converter is shut down. The protection-enable period, t_{pe}, must be longer than the dc/dc converter start-up time, or the converter will never come up. Because the soft start is designed to bring the converter up within 5 ms, t_{pe} = 75 ms should work well. C4 is given by (t_{pe} in s, C4 in μF);

$$C4 = 12.46 \times t_{pe} = 12.46 \times 0.075 = 0.935 \ \mu F \Rightarrow 1 \ \mu F$$

Output Sense Network

The output sense network is a resistive divider connected between the converter output and ground with the divider output connected to the TL5001 FB terminal (refer to Figure 6). The divider ratio is chosen for a 1-V output (the TL5001 reference voltage) when the converter output is at the desired value.

Establishing the proper divider ratio is critical, but selecting values for the sense network is somewhat arbitrary. Choosing the values too high can result in converter-output-voltage accuracy problems because the error-amplifier input-bias current loads the network. Values that are too low can dissipate too much power, drain too much power from limited power sources such as batteries, or lead to loop-compensation-capacitor values that are too high to be practical. As a rule, a divider current approximately 1000 times greater than the maximum error-amplifier input current is chosen. Resistors with 1% tolerances and low and/or reasonably well-matched temperature coefficients are recommended to minimize the output voltage tolerance.

Because the worst-case TL5001 input bias current is 0.5 μA, the divider current should be approximately 1000 × 0.5 μA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is $V_O - 1$ V = 4 V.

$$R6 = \frac{1 \ V}{0.5 \ mA} = 2 \ k\Omega$$

$$R5 = \frac{\left(V_O - 1 \ V\right)}{0.5 \ mA} = \frac{5 - 1}{0.5 \times 10^{-3}} = 8 \ k\Omega$$

Since they are readily available and provide the right divider ratio, R5 = 7.50 kΩ and R6 = 1.87 kΩ are used.

Loop Compensation

The loop-compensation design procedure consists of shaping the error-amplifier frequency response with external components to stabilize the dc/dc converter feedback control loop without destroying the control-loop ability to respond to line and/or load transients. A detailed treatment of dc/dc converter stability analysis and design is well beyond the scope of this report; however, several references on the subject are available. The following is a simplified approach to designing networks to stabilize continuous-mode buck converters that works well when the open-loop gain is below unity at a frequency much lower than the frequency of operation.

Ignoring the error-amplifier frequency response, the response of the pulse-width modulator and power switch operating in continuous mode can be modeled as a simple gain block. The magnitude of the gain is the change in output voltage for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). Typically, increasing the COMP voltage from 0.6 V to 1.4 V increases the duty cycle from 0 to 100% and the output voltage from 0 V to approximately 12 V at the nominal input voltage. The gain, A_{PWM}, is:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{(12 - 0)}{(1.4 - 0.6)} = 15 \Rightarrow 24 \text{ dB at nominal input}$$

Similarly, the gain is 22 dB at low line and 25 dB at high line. Converters with wider input ranges, 2:1 or more, need to check for stability at several line voltages to ensure that gain variation does not cause a problem.

The output filter is an LC filter and functions accordingly. The inductor and capacitor produce an underdamped complex-pole pair at the filter resonant frequency and the capacitor ESR (R_S) puts a zero in the response above the resonant frequency. The complex poles are located at:

$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\left(27 \times 10^{-6}\right)\left(220 \times 10^{-6}\right)}} = 2.06 \text{ kHz}$$

The zero is located at:

$$\frac{1}{2\pi R_S C} = \frac{1}{(2\pi)(0.035)\left(220 \times 10^{-6}\right)} = 20.7 \text{ kHz.}$$

Figure 5 includes gain and phase plots of the open-loop response (error amplifier not included) obtained from a simple SPICE simulation.

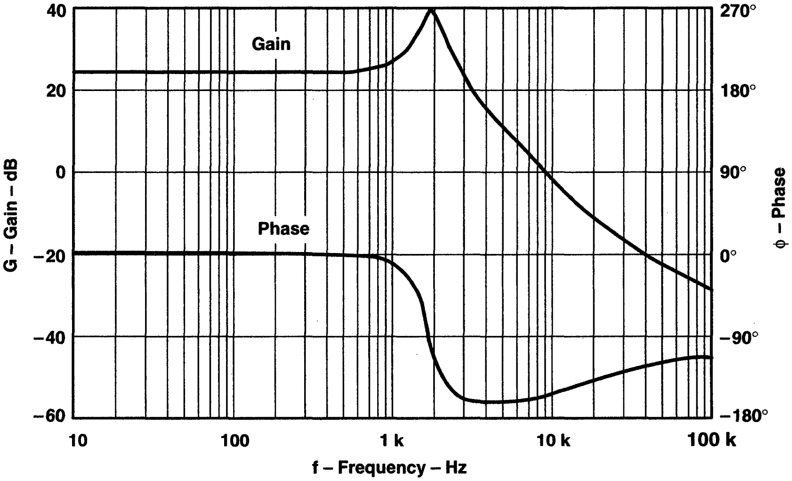


Figure 5. Uncompensated Open-Loop Response

The presence of the complex-pole pair is evident from the resonant peaking in the gain at 2 kHz and the rapid phase transition in the vicinity of 2 kHz. The zero is hard to see in the gain plot but shows up well in the phase response; the complex poles provide −180° of phase shift at 20 kHz and the zero adds 45° for a net of −135°.

Unless the designer is trying to meet an unusual requirement, such as very wide band response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage; compensation zeros are added near the filter poles to correct for the sharp change in phase encountered near the filter-resonant frequency; and an open-loop unity-gain frequency is selected well beyond the filter-resonant frequency but 10% or less than the converter operating frequency. In this instance, a unity-gain frequency (f_T) of approximately 20 kHz is chosen to provide good transient response. Figure 6 shows a standard compensation network chosen for this example.

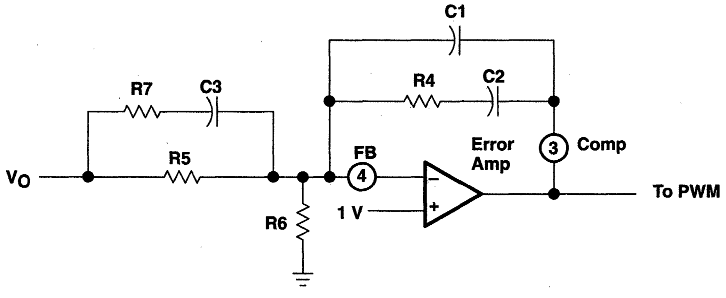


Figure 6. Compensation Network

Assuming an ideal amplifier, the transfer function is:

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C2 + C1)}\right]\left[\frac{[S(R5 + R7)\ C3 + 1]\ (S\ R4\ C2 + 1)}{(S\ R7\ C3 + 1)\left[S\ R4\ \left(C1 \parallel C2\right) + 1\right]}\right]$$

The integrator gain, 1/[R5 · (C2 + C1)], establishes the open-loop unity-gain frequency. The zeros are located at approximately the same frequency as the output-filter poles to compensate for the gain reduction and phase shift. The pole at 1/(2π · R7 · C3) is positioned at approximately the same frequency as the zero in the output filter to maintain the 20 dB-per-decade roll-off in the gain response. The final pole at 1/(2 π · R4 · C1 || C2) is placed at a frequency between half of the operating frequency and the operating frequency to minimize high-frequency noise at the pulse-width-modulator input. The last pole is not always necessary but should be included in the design until the need is established.

The sum of the gains of the modulator, the LC filter, and the error amplifier is 0 dB at the unity-gain frequency. The gain of the modulator/LC filter at 20 kHz may be calculated or obtained from a bode plot using straight-line approximations or from a simple SPICE simulation. As shown in Figure 5, the modulator/filter gain is –12 dB at 20 kHz.

The compensation network has two zeros at 2 kHz to cancel out the LC filter poles. These two zeros contribute a gain of 40 dB at 20 kHz; therefore, the gain contributed by the compensation-network integrator needs to be –28 dB [0 – (–12 +40) = –28]. The integrator gain of –28 dB translates to a voltage gain of 0.0398.

$$\frac{1}{(2\ \pi)\left(f_T\right)(R5)(C2 + C1)} = 0.0398\ \left(\text{at } f_T\ =\ 20\ \text{kHz}\right)$$

In practice, C2 >> C1,

$$C2 = \frac{1}{(2\pi)\left(f_T\right)(R5)(0.0398)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(7.5 \times 10^3\right)(0.0398)} = 0.027\ \mu F$$

R4 is chosen to position a zero at 2 kHz.

$$R4 = \frac{1}{(2\pi)(f)(C2)} = \frac{1}{(6.28)\left(2 \times 10^3\right)\left(0.027 \times 10^{-6}\right)} = 2.95\ k\Omega \Rightarrow \text{Use } 3.0\ k\Omega$$

R7 and C3 are chosen to provide a zero, f_{Z1}, at 2 kHz and a pole, f_{P1}, at 20 kHz.

$$f_{Z1} = \frac{1}{2\pi(R5 + R7)\ C3} = \frac{1}{[(2\pi)(R5)(C3)] + [(2\pi)(R7)(C3)]}$$

$$f_{P1} = \frac{1}{(2\pi)\ (R7)\ (C3)}$$

After algebraic manipulation:

$$(2\pi)(R7)(C3) = \frac{1}{f_P}$$

$$C3 = \frac{\frac{1}{f_Z} - \frac{1}{f_P}}{(2\pi)(R5)} = \frac{\left[\frac{1}{2 \times 10^3} - \frac{1}{20 \times 10^3}\right]}{(6.28)\left(7.5 \times 10^3\right)} = 0.0096\ \mu F \Rightarrow \text{Use } C3 = 0.01\ \mu F$$

$$R7 = \frac{1}{(2\pi)\left(f_P\right)(C3)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(0.01 \times 10^{-6}\right)} = 796\ \Omega \Rightarrow \text{Use } 820\ \Omega$$

C1 is chosen to provide the pole, f_{P2}, at 100 kHz. Assuming C3 >> C1.

$$C1 = \frac{1}{(2\pi)\left(f_{P2}\right)(R4)} = \frac{1}{(6.28)\left(100 \times 10^3\right)(3000)} = 531\ pF \Rightarrow \text{Use } 470\ pF$$

Results of the compensated-loop response are shown in Figure 7.

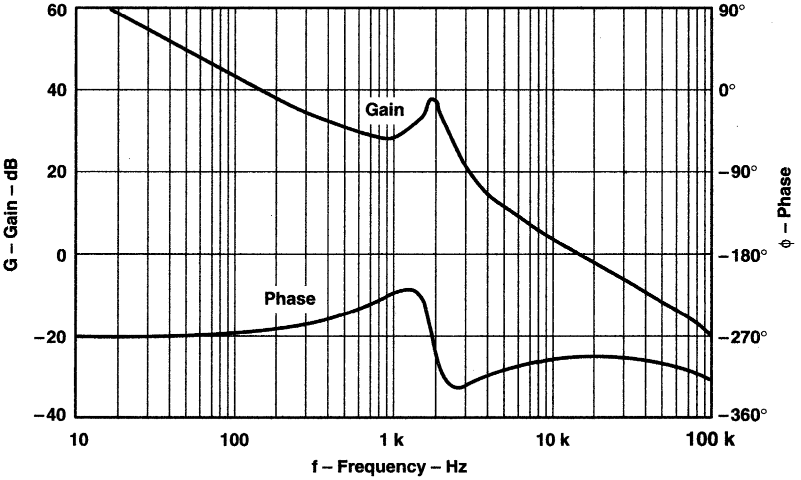
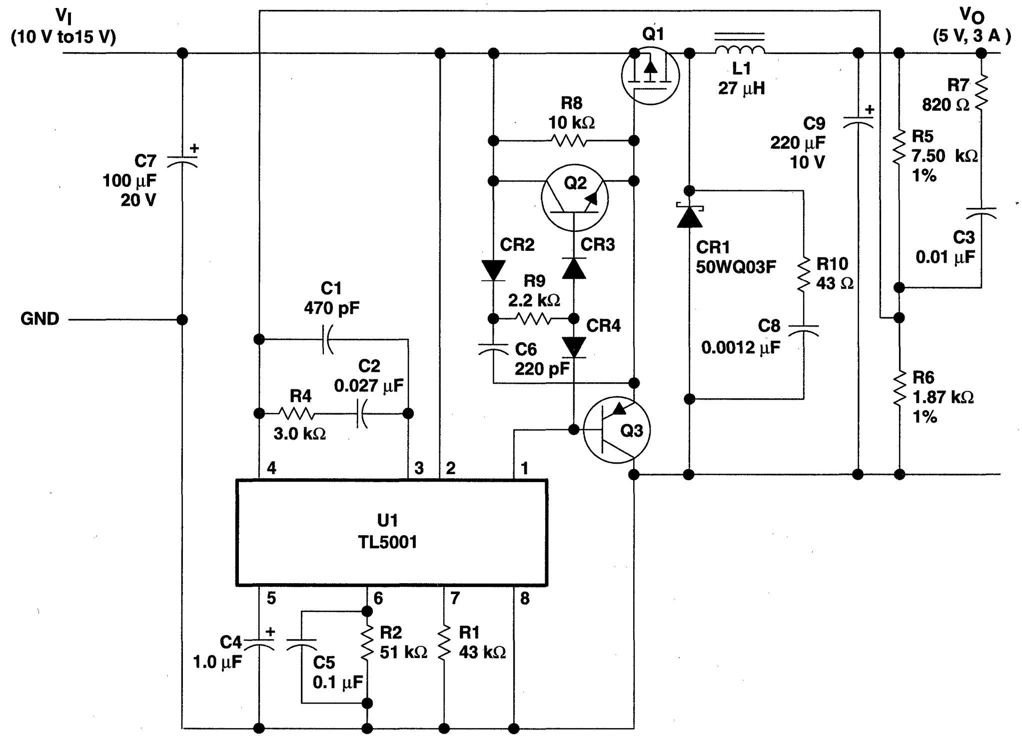


Figure 7. Compensated-Loop Response

Summary

The schematic (Figure 8), bill of materials, and test results for the completed design are provided in this summary.



Q1 – IRF9Z34S
Q2 – PMBT2222APH
Q3 – PMBT2907APH
All diodes are PMBD914PH, unless otherwise specified.
R3 – Not used

Figure 8. 12-V to 5-V at 3-A Converter

Table 1. Example 1: Bill of Materials

REF DES	PART NO.	DESCRIPTION	MFG
U1	TL5001	IC, PWM Controller	Texas Instruments
C1		Capacitor, Ceramic, 470 pF, 50 V, 10%	
C2		Capacitor, Ceramic, 0.027 µF, 50 V, 10%	
C3		Capacitor, Ceramic, 0.01 µF, 50 V, 10%	
C4		Capacitor, Tantalum, 1.0 µF, 20 V, 10%	
C5		Capacitor, Ceramic, 0.10 µF, 50 V, 10%	
C6		Capacitor, Ceramic, 220 pF, 50 V, 10%	
C7	20SA100M	Capacitor, Aluminum, 100 µF, 20 V, 20%	Sanyo
C8		Capacitor, Ceramic, 0.0012 µF, 50 V, 10%	
C9	10SA220M	Capacitor, Aluminum, 220 µF, 10 V, 20%	Sanyo
CR1	50WQ03F	Diode, Schottky, 30 V, 5.5 A	International Rectifier
CR2–4	PMBD914PH	Diode, Switching, 100 V, 200 mA	
L1	T50-26B	Core, Inductor, 27 µH, 27 Turns #22	MicroMetals
Q1	IRF9Z34S	Transistor, MOSFET, p-ch, 60 V, 18A, 0.14 Ω	International Rectifier
Q2	PMBT2222APH	Transistor, NPN, 30 V, 150 mA	
Q3	PMBT2907APH	Transistor, PNP, 40 V, 150 mA	
R1		Resistor, CF, 43 kΩ, 1/4 W, 5%	
R2		Resistor, CF, 51 kΩ, 1/4 W, 5%	
R4		Resistor, CF, 3.0 kΩ, 1/4 W, 5%	
R5		Resistor, MF, 7.50 kΩ, 1/4 W, 1%	
R6		Resistor, MF, 1.87 kΩ, 1/4 W, 1%	
R7		Resistor, CF, 820 Ω, 1/4 W, 5%	
R8		Resistor, CF, 10 kΩ, 1/4 W, 5%	
R9		Resistor, CF, 2.2 kΩ, 1/4 W, 5%	
R10		Resistor, CF, 43 Ω, 1/4 W, 5%	

Table 2. Example 1: Test Results

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	$V_I = 12$ V, $I_O = 0 \sim 3$ A	0.4%
Line regulation	$I_O = 1.5$ A, $V_I = 10 \sim 15$ V	0.4%
Output ripple (peak-to-peak)	$V_I = 12$ V, $I_O = 3$ A	10 mV
Efficiency	$V_I = 12$ V, $I_O = 3$ A	81.7%

EXAMPLE 2: 12-V to 3.3-V at 3-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 9. This design is very similar to that in Example 1 and thus much of the detail is not repeated.

Specifications

Input voltage range, V_I	10 V to 15 V
Output voltage, V_O	3.3 V
Output current, I_O	0 A to 3 A
Output ripple voltage	≤50 mV
Efficiency	>70%
Ambient temperature range, T_A	0°C to 55°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down (buck) topology operating at 200 kHz.

Duty-Cycle Estimates

Estimate the power-switch duty cycle over the range of input voltages using:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume $V_d = 0.6$ V)
V_{sat} = power-switch conduction voltage (assume $V_{sat} = 0.5$ V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for V_I = 10, 12, and 15 V is 0.41, 0.34, and 0.27, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose L1 to limit the peak-to-peak ripple current to 10% of the maximum output current.

$$\Delta I_O = 2 \times 0.1 \times I_{O(max)} = 2 \times 0.1 \times 3 = 0.6 \text{ A peak-to-peak}$$

Inductance is given by:

$$L1 = \left(V_I - V_{sat} - V_O\right) \times D \times \frac{t}{\Delta I_O}$$

Maximum ripple current occurs at the maximum input voltage. Solving for L1:

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)(D)(t)}{\Delta I_O} = \frac{(15 - 0.5 - 3.3)(0.27)\left(5 \times 10^{-6}\right)}{0.6} = 25.2\ \mu H$$

For convenience, use the same inductor as in example 1; therefore, L1 = 27 µH.

Capacitor

Assuming all the inductor ripple current flows through the capacitor and ESR is negligible, calculate the capacitance needed to limit the ripple voltage to 50 mV peak-to-peak.

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.6}{(8)\left(200 \times 10^3\right)(0.05)} = 7.5\ \mu F$$

Assuming the capacitance is at least 10 times greater than the calculated value, the ESR to limit the ripple to 50 mV peak-to-peak is:

$$\text{ESR} = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.6} = 83\ \text{m}\Omega$$

The rms capacitor-ripple current is:

$$\text{Capacitor current} = 0.289 \times \Delta I_O = 0.289 \times 0.6 = 0.17\ \text{Arms}$$

For convenience, use the same 220-µF, 10-V, 35-mΩ OS-CON SA-series device that was used in Example 1. Alternate choices include a 100-µF, 16-V, 45-mΩ device in the same family but one case-size smaller, and two of the solid tantalum 100-µF, 10-V devices described in example 1.

Power-Switch Design

The power-switch design procedure includes selecting the power switch, the catch rectifier, and the rectifier-snubbing network (if needed), calculating power dissipations and junction temperatures, and ensuring the semiconductors have proper heat sinking.

Power Switch

The surface-mount p-channel device used in Example 1 should work in this design also. The IRF9Z34S has a 60-V drain-to-source breakdown and a 140-mΩ maximum $r_{DS(on)}$ with a 10-V gate drive.

Assume that the worst-case junction temperature is 125°C in a 55°C ambient temperature and the drive circuit provides a 100-ns total switching time (turn-on and turnoff). $r_{DS(on)}$ increases by a factor of 1.6 at 125°C.

$$P_D = \left(3^2\right)(0.14 \times 1.6)(0.41) + (0.5)(10)(3)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)$$
$$P_D = 0.83 + 0.30 = 1.13\ \text{W}$$

The thermal impedance $R_{\theta JA}$ = 40°C/W for FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (40 \times 1.13) = 100°\text{C}$$

Catch Rectifier

Since the requirements are so similar, consider the same device used in Example 1, the 50WQ03F. The device is a 5.5-A, 30-V Schottky diode in a DPAK, power surface-mount package.

Worst-case dissipation occurs at high line where D is minimum. The 50WQ03F has a maximum forward drop of 0.55 V at a forward current of 3 A and a junction temperature of 125°C.

$$P_D = 3 \times 0.55 \times (1 - 0.39) = 1\ \text{W}$$

The thermal impedance $R_{\theta JA}$ = 50°C/W when mounted on FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = 55 + (50 \times 1) = 105°\text{C}$$

Catch-Rectifier Snubber Network

The capacitor value chosen is 4 to 10 times greater than the rectifier junction capacitance; higher values improve the snubbing but dissipate more power. The 50WQ03F has a typical junction capacitance of 180 pF, and the snubber-capacitor value should be between 750 pF and 1.8 nF. Use C8 = 1.2 nF for convenience. Rectifiers normally ring in the range from 1 to 50 MHz. Choose the snubber resistor, R10, for a 50-ns time constant:

$$R10 = \frac{50 \times 10^{-9}}{C8} = \frac{50 \times 10^{-9}}{1.2 \times 10^{-9}} = 41.7\ \Omega \Rightarrow \text{Use } 43\ \Omega$$

Because the capacitor is charged and discharged each cycle, the power dissipation in R10 is:

$$(2)(C8)\left(V_I^2\right)\left(\frac{f_s}{2}\right) = (2)\left(1.2 \times 10^{-9}\right)\left(15^2\right)\left(\frac{200 \times 10^3}{2}\right) = 54 \text{ mW}$$

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, dead-time control voltage, soft-start timing, and short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

Select resistor R1 = 43 kΩ using the graph in Figure 3 to set the oscillator frequency to 200 kHz.

Dead-Time Control

The dead-time-control resistor, R2, is chosen to limit the duty cycle to approximately 0.55, well above the anticipated 0.41 maximum duty cycle. See Figure 4 to find the maximum and minimum ramp-voltage levels, $V_{O(100\%)}$ and $V_{O(0\%)}$. R2 is calculated from the following expression (R_{DT}, R_t in kΩ, D in decimal):

$$R2 = (R1 + 1.25)\left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right]$$

where R1 and R2 are in kΩ.

$$R2 = (43 + 1.25)[0.55\ (1.4 - 0.6) + 0.6] = 46 \text{ k}\Omega \Rightarrow 47 \text{ k}\Omega$$

Soft-Start Timing

As in Example 1, choose C5 = 0.1 µF to bring the output voltage into regulation in approximately 5 ms.

SCP Timing

As in Example 1, choose C4 = 1.0 µF to set the protection enable period to approximately 75 ms.

Output Sense Network

The worst-case input bias current for the TL5001 is 0.5 µA; therefore, the divider current should be approximately 1000 × 0.5 µA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is $V_O - 1\text{ V} = 2.3\text{ V}$. Choose R5 = 7.50 kΩ so that the compensation values in Example 1 can be used in this design as well.

$$I_{divider} = \frac{\left(V_O - 1\text{ V}\right)}{R5} = \frac{3.3 - 1}{7.5 \times 10^3} = 0.307 \text{ mA}$$

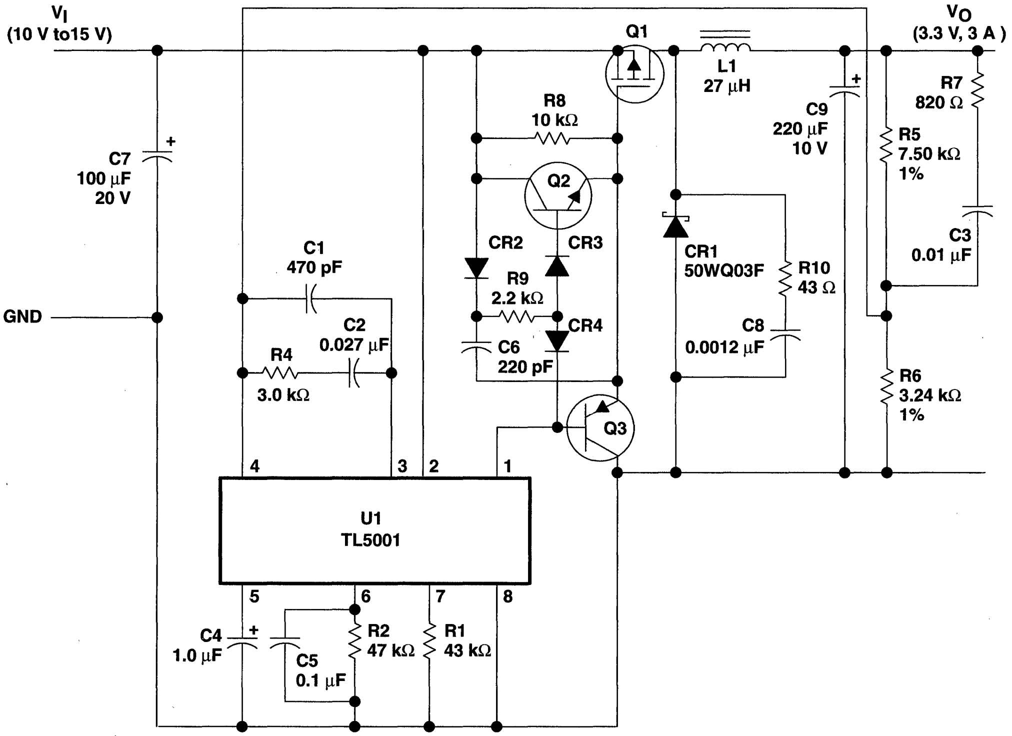
$$R6 = \frac{1\text{ V}}{0.307\text{ mA}} = 3.26 \text{ k}\Omega \Rightarrow \text{Use } 3.24 \text{ k}\Omega$$

Loop Compensation

Because the output-filter components, the PWM gain, and R5 are the same as in Example 1, the same compensation design can be used for this application (refer to Example 1 for details).

Summary

The schematic (Figure 9), bill of materials, and test results for the completed design are provided in this summary.



Q1 – IRF9Z34S
Q2 – PMBT2222APH
Q3 – PMBT2907APH
All diodes are PMBD914PH, unless otherwise specified.
R3 – Not used

Figure 9. 12-V to 3.3-V at 3-A Converter

Table 3. Example 2: Bill of Materials

REF DES	PART NO.	DESCRIPTION	MFG
U1	TL5001	IC, PWM Controller	Texas Instruments
C1		Capacitor, Ceramic, 470 pF, 50 V, 10%	
C2		Capacitor, Ceramic, 0.027 μF, 50 V, 10%	
C3		Capacitor, Ceramic, 0.01 μF, 50 V, 10%	
C4		Capacitor, Tantalum, 1.0 μF, 20 V, 10%	
C5		Capacitor, Ceramic, 0.10 μF, 50 V, 10%	
C6		Capacitor, Ceramic, 220 pF, 50 V, 10%	
C7	20SA100M	Capacitor, Aluminum, 100 μF, 20 V, 20%	Sanyo
C8		Capacitor, Ceramic, 0.0012 μF, 50 V, 10%	
C9	10SA220M	Capacitor, Aluminum, 220 μF, 10 V, 20%	Sanyo
CR1	50WQ03F	Diode, Schottky, 30 V, 5.5 A	International Rectifier
CR2–4	PMBD914PH	Diode, Switching, 100 V, 200 mA	
L1	T50-26B	Core, Inductor, 27 μH, 27 Turns #22	MicroMetals
Q1	IRF9Z34S	Transistor, MOSFET, p-ch, 60 V, 18A, 0.14 Ω	International Rectifier
Q2	PMBT2222APH	Transistor, NPN, 30 V, 150 mA	
Q3	PMBT2907APH	Transistor, PNP, 40 V, 150 mA	
R1		Resistor, CF, 43 kΩ, 1/4 W, 5%	
R2		Resistor, CF, 47 kΩ, 1/4 W, 5%	
R4		Resistor, CF, 3.0 kΩ, 1/4 W, 5%	
R5		Resistor, MF, 7.50 kΩ, 1/4 W, 1%	
R6		Resistor, MF, 3.24 kΩ, 1/4 W, 1%	
R7		Resistor, CF, 820 Ω, 1/4 W, 5%	
R8		Resistor, CF, 10 kΩ, 1/4 W, 5%	
R9		Resistor, CF, 2.2 kΩ, 1/4 W, 5%	
R10		Resistor, CF, 43 Ω, 1/4 W, 5%	

Table 4. Example 2: Test Results

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	$V_I = 12$ V, $I_O = 0 \sim 3$ A	0.7%
Line regulation	$I_O = 1.5$ A, $V_I = 10 \sim 15$ A	0.9%
Output ripple (peak-to-peak)	$V_I = 12$ V, $I_O = 3$ A	8 mV
Efficiency	$V_I = 12$ V, $I_O = 3$ A	74.7%

EXAMPLE 3: 5-V to 3.3-V at 0.75-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 13 . Example 1 gives a more detailed explanation of the same design procedure used in this section.

Specifications

Input voltage range, V_I	4.75 V to 5.25 V
Output voltage, V_O	3.3 V
Output current, I_O	0 A to 0.75 A
Output ripple voltage	≤50 mV
Regulation	1%
Efficiency	>70%
Ambient temperature range, T_A	−20°C to 65°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down (buck) converter operating at 200 kHz.

Duty-Cycle Estimates

Estimate the power-switch duty cycle over the range of input voltages using:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume $V_d = 0.5$ V)

V_{sat} = power-switch conduction voltage (assume $V_{sat} = 0.25$ V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for V_I = 4.75, 5, and 5.25 V is 0.84, 0.80, and 0.76, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose L1 to maintain continuous-mode operation to 20% of the rated output current.

$$\Delta I_O = 2 \times 0.2 \times I_{O(max)} = 2 \times 0.2 \times 0.75 = 0.3 \text{ A peak-to-peak}$$

The inductor value is calculated using

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)DTs}{\Delta I_O}$$

where Ts is the period of the converter operating frequency.

Maximum ripple current occurs at the maximum input voltage. Solving for L1:

$$L1 = \frac{(5.25 - 0.25 - 3.3)(0.76)\left(5 \times 10^{-6}\right)}{0.3} = 21.5 \ \mu H$$

Use L1 = 20 µH (Coiltronics CTX20-1, 1.15 A dc-current rating, surface-mount package). Using the new value for L1, ΔI_O is recalculated:

$$\Delta I_O = \frac{\left(V_I - V_{sat} - V_O\right)DTs}{L1} = \frac{(5.25 - 0.25 - 3.3)(0.76)\left(5 \times 10^{-6}\right)}{20 \times 10^{-6}} = 323 \text{ mA peak-to-peak}$$

Capacitor

Assuming all the inductor ripple current flows through the capacitor and ESR is zero, the capacitance needed to limit the ripple voltage to 50 mV peak-to-peak is:

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.323}{(8)\left(200 \times 10^3\right)(0.05)} = 4.04\ \mu\text{F}$$

If the capacitance is at least ten times greater than the calculated value, the ESR to limit the ripple to 50 mV peak-to-peak is:

$$\text{ESR} = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.323} = 155\ \text{m}\Omega$$

Capacitor ripple current is seldom a problem in low-voltage converters unless a large number of devices are paralleled. However, the capacitor current is calculated as follows:

$$I_{rms} = 0.289 \times \Delta I_O = 0.289 \times 0.323 = 0.093\ \text{Arms}$$

The output filter capacitor(s) should provide at least ten times the calculated minimum capacitance and an ESR 30% to 50% lower than the calculated maximum to provide some margin for ESL, PCB leads, temperature, and aging. The 200-kHz, 85°C ripple current should be 0.25 Arms or greater, and the voltage rating should be at least 6.3 V.

For this case, a 100-µF, 10-V tantalum electrolytic with an ESR of 0.100 Ω maximum was chosen.

Power-Switch Design

The power-switch design procedure includes selecting the power switch, the catch rectifier, and the rectifier-snubbing network (if needed); calculating power dissipations and junction temperatures; and ensuring the semiconductors have proper heat sinking.

Power Switch

This design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. Based on the preliminary estimate, $r_{DS(on)}$ should be less than 0.25 V ÷ 0.75 A = (333 mΩ) with a 5-V gate drive and a drain-to-source breakdown voltage appropriate for a 5-V supply. A low gate-to-source threshold voltage and surface-mount packaging are also desirable.

The TPS1101D is a 15-V p-channel MOSFET in an SO-8 package with $r_{DS(on)}$ = 0.19 mΩ maximum, with a 4.5-V gate drive.

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

Where t_{r+f} = total MOSFET switching time (turn-on and turnoff) and $r_{DS(on)}$ is adjusted for temperature. Assuming the drive circuit is adequate for t_{r+f} = 100 ns and the junction temperature is 100°C with a 65°C ambient, the adjustment factor is 1.3 and $r_{DS(on)}$ = 1.3 × 0.19 = 0.25.

$$P_D = \left[\left(0.75^2\right)(0.25)(0.80)\right] + \left[(0.5)(5)(0.75)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)\right]$$

$$P_D = 113 + 38 = 151\ \text{mW}$$

The thermal impedance $R_{\theta JA}$ = 158°C/W for FR-4 with no special heat-sinking considerations.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 65 + (158 \times 0.151) = 89°\text{C}$$

Catch Rectifier

The power dissipation in this design is very low because of a relatively low output-current requirement and the high-power-switch duty cycles. Consequently, a small surface-mount Schottky device such as the MBRS140T3 is more than adequate. The MBRS140T3 is rated for 1 A of forward current and a 40-V breakdown. The conduction drop, V_d, is 0.35-V at 1-A forward current and a 100°C junction. The power dissipation is:

$$P_D = I_O \times V_d \times (1 - D)$$

$$P_D = 0.75 \times 0.35 \times (1 - 0.76) = 63\ \text{mW}$$

In the absence of thermal-impedance data for this package with FR-4 mounting, a reasonable estimate of junction temperature is not practical. However, some assurance can be derived from considering the thermal impedance necessary to limit the junction to 100°C which is comfortably below the 125°C maximum rating. The thermal impedance, $R_{\theta JA}$, needed to raise the junction temperature from the 65°C ambient to 100°C with 63 mW of dissipation is:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} = \frac{100 - 65}{0.063} = 556^\circ\text{C/W}$$

There should be no problem since even signal diodes are in the 300°C to 400°C/W range. Some preliminary testing to establish thermal performance is highly recommended for applications where the margins are lower.

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, dead-time control voltage, soft-start timing, and short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

From the graph in Figure 3, choose R2 = 43 kΩ to set the oscillator frequency to 200 kHz.

Dead-Time Control

The maximum duty cycle in this application is 84% and because there is no benefit in limiting the duty cycle a few points below 100%, the dead-time control resistor is omitted.

Soft-Start Timing

The DTC input can be used to soft start the converter even though dead-time control is not implemented. The soft-start capacitor is charged with a constant current approximately equal to the current flowing from the RT terminal. The output voltage should be in regulation by the time C5 has charged to 1.4 V. Choose C5 such that the output voltage comes up in 6 ms.

$$\text{Charging current} = \frac{1\ \text{V}}{43\ \text{k}\Omega} = 23.3\ \mu\text{A}$$

$$C5 = \frac{\left(23.3 \times 10^{-6}\right)\left(6 \times 10^{-3}\right)}{1.4} = 0.1\ \mu\text{F}$$

SCP Timing

As in Example 1, choose C4 = 1 µF to set the protection enable period to approximately 75 ms.

Output Sense Network

The worst-case input bias current for TL5001 is 0.5 µA; therefore, the divider current should be approximately 1000 × 0.5 µA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is V_O – 1 V = 2.3 V. For this design, R5 is set at 7.50 kΩ.

$$I_{divider} = \frac{\left(V_O - 1\ \text{V}\right)}{R5} = \frac{3.3 - 1}{7.5 \times 10^3} = 0.307\ \text{mA}$$

$$R6 = \frac{1\ \text{V}}{0.307\ \text{mA}} = 3.26\ \text{k}\Omega \Rightarrow \text{Use } 3.24\ \text{k}\Omega$$

Loop Compensation

Refer to Example 1 for more detailed explanation.

The open-loop response without the error amplifier consists of the gain of the PWM/power switch, A_{PWM}, and the output filter response. The gain, A_{PWM}, is:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{(5 - 0)}{(1.4 - 0.6)} = 6.25 \Rightarrow 15.9 \text{ dB at nominal input}$$

Similarly, the gain is 15.5 dB at low line and 16.3 dB at high line.

The output filter produces an underdamped complex-pole pair at the filter's resonant frequency, and the capacitor ESR puts a zero in the response above the resonant frequency. The complex poles are located at:

$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\left(20 \times 10^{-6}\right)\left(100 \times 10^{-6}\right)}} = 3.56 \text{ kHz}$$

The zero is located at:

$$\frac{1}{2\pi R_S C} = \frac{1}{(2\pi)(0.1)\left(100 \times 10^{-6}\right)} = 15.9 \text{ kHz.}$$

Figure 10 includes gain and phase plots of the open-loop response (error amplifier not included) obtained from a simple SPICE simulation.

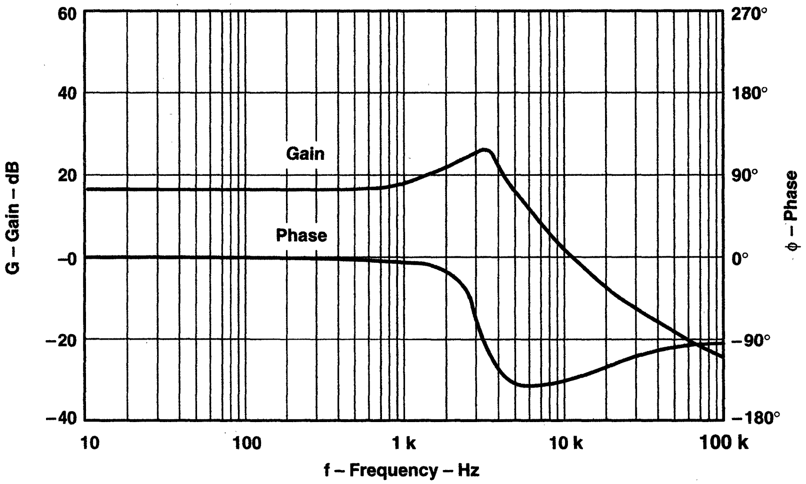


Figure 10. Uncompensated Open-Loop Response

Choose a unity-gain frequency of approximately 20 kHz to provide good transient response. Figure 11 shows a standard compensation network chosen for this example.

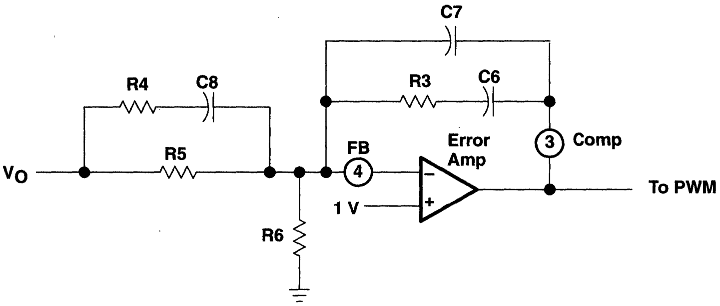


Figure 11. Compensation Network

Assuming an ideal amplifier, the transfer function is:

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C6 + C7)}\right]\left[\frac{[S(R5 + R4)\ C8 + 1]\ (S\ R3\ C6 + 1)}{(S\ R4\ C8 + 1)\left[S\ R3\left(C6 \parallel C7\right) + 1\right]}\right]$$

The integrator gain, 1/[R5 · (C6 + C7)], is used to set the open-loop unity-gain frequency. The zeros are located at approximately the same frequency as the output-filter poles to compensate for the gain reduction and phase shift. The pole at 1/(2π · R4 · C8) is positioned at approximately the same frequency as the zero in the output filter to maintain the 20 dB-per-decade roll-off in the gain response. The final pole at 1/(2π · R3 · C6 ‖ C7) is placed between half the operating frequency and the operating frequency to minimize noise at the pulse-width-modulator input.

The sum of the gains of the modulator, the LC filter, and the error amplifier is 0 dB at the unity-gain frequency. The gain of the modulator/LC filter at 20 kHz may be calculated or obtained from a bode plot using straight-line approximations or from a simple SPICE simulation. As shown in Figure 10, the modulator/LC filter gain is −8 dB at 20 kHz.

The compensation network has two zeros at 3.6 kHz to cancel out the LC filter poles. These two zeros contribute a gain of 29 dB at 20 kHz; therefore, the gain contributed by the compensation-network integrator needs to be −21 dB [0 − (−8 + 29) = −21]. The integrator gain of −21 dB translates to a voltage gain of 0.089.

$$\frac{1}{(2\pi)\left(f_T\right)(R5)(C6 + C7)} = 0.089\ \left(\text{at } f_T = 20\ \text{kHz}\right)$$

$$C6 = \frac{1}{(2\pi)\left(f_T\right)(R5)(0.089)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(7.5 \times 10^3\right)(0.089)} = 0.0119\ \mu\text{F} \Rightarrow \text{Use C6} = 0.012\ \mu\text{F.}$$

R3 is chosen to position a zero at 3.6 kHz.

$$R3 = \frac{1}{(2\pi)(f)(C6)} = \frac{1}{(6.28)\left(3.6 \times 10^3\right)\left(0.012 \times 10^{-6}\right)} = 3.69\ \text{k}\Omega \Rightarrow \text{Use } 3.6\ \text{k}\Omega$$

R4 and C8 are chosen to provide an additional zero, f_Z, at 3.6 kHz and a pole, f_P, at 15.9 kHz.

$$C8 = \frac{\frac{1}{f_Z} - \frac{1}{f_P}}{(2\pi)(R5)} = \frac{\left[\frac{1}{3.6 \times 10^3} - \frac{1}{15.9 \times 10^3}\right]}{(6.28)\left(7.5 \times 10^3\right)} = 0.0046\ \mu\text{F} \Rightarrow \text{Use C8} = 0.0047\ \mu\text{F}$$

$$R4 = \frac{1}{(2\pi)\left(f_P\right)(C8)} = \frac{1}{(6.28)\left(15.9 \times 10^3\right)\left(0.0047 \times 10^{-6}\right)} = 2.13\ \text{k}\Omega \Rightarrow \text{Use } 2.0\ \text{k}\Omega$$

C7 is chosen to provide the pole at 100 kHz. Assuming C6 >> C7,

$$C7 = \frac{1}{(2\pi)\left(f_P\right)(R3)} = \frac{1}{(6.28)\left(100 \times 10^3\right)(3600)} = 442\ \text{pF} \Rightarrow \text{Use } 470\ \text{pF}$$

Results of the compensated-system response are shown in Figure 12.

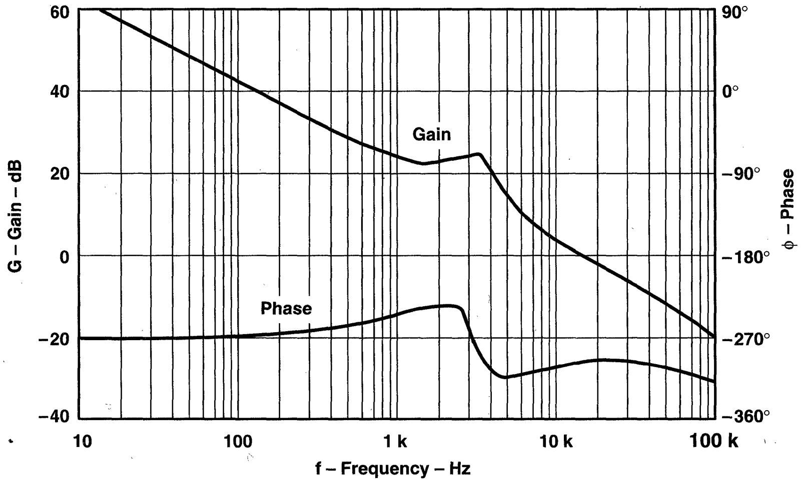
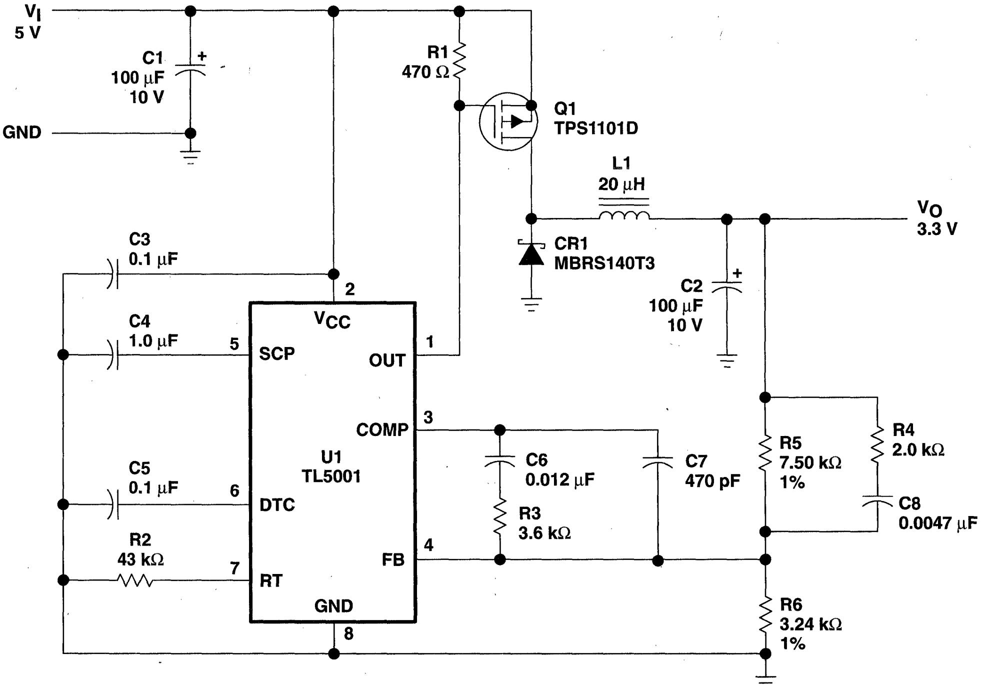


Figure 12. Compensated-Loop Response

Summary

The schematic (Figure 13), bill of materials, and test results for the completed design are provided in this summary.



NOTES:
A. Frequency = 200 kHz
B. Duty cycle = 100% MAX
C. Soft-start timing = 6 ms
D. SCP timing = 75 ms

Figure 13. 5-V to 3.3-V/0.75-A Converter

Table 5. Example 3: Bill of Materials

REF DES	PART NO.	DESCRIPTION				MFG
U1	TL5001	IC, PWM Controller				Texas Instruments
C1, C2	TPSD107M010R0100	Capacitor, Tantalum,	100 μF,	10 V,	20%	AVX
C4		Capacitor, Ceramic,	1.0 μF,	50 V,	10%	
C3, C5		Capacitor, Ceramic,	0.1 μF,	50 V,	10%	
C6		Capacitor, Ceramic,	0.012 μF,	50 V,	10%	
C7		Capacitor, Ceramic,	470 pF,	50 V,	10%	
C8		Capacitor, Ceramic,	0.0047 μF,	50 V,	10%	
CR1	MBRS140T3	Diode, Schottky,	20 V,	1 A		Motorola
L1	CTX20-1	Inductor, Toroid,	20 μH			Coiltronics
Q1	TPS1101D	Transistor, MOSFET,	p-ch,	15 V,	0.19 Ω	Texas Instruments
R1		Resistor, CF,	470 Ω,	1/4 W,	5%	
R2		Resistor, CF,	43 kΩ,	1/4 W,	5%	
R3		Resistor, CF,	3.6 kΩ,	1/4 W,	5%	
R4		Resistor, CF,	2.0 kΩ,	1/4 W,	5%	
R5		Resistor, MF,	7.50 kΩ,	1/4 W,	1%	
R6		Resistor, MF,	3.24 kΩ,	1/4 W,	1%	

Table 6. Example 3: Test Results

PARAMETER	TEST CONDITIONS			MEASUREMENT
Load regulation	$V_I = 5$ V,	$I_O = 0 \sim 750$ mA		1.4%
Output ripple (peak-to-peak)	$I_O = 750$ mA			<20 mV
Efficiency	$V_I = 5$ V,	$I_O = 750$ mA,	Q1 = SI9405	74.4%
	$V_I = 5$ V,	$I_O = 750$ mA,	Q1 = TPS1101	84.1%†

† The higher efficiency achieved with the TPS1101 is due to lower gate capacitance, which speeds up switching and reduces switching loss.

Appendix A
5-V Prototype-Board Waveforms

The following photos were taken using the 12-V to 5-V prototype breadboard that was designed and documented as presented in the first section of this application report. The results are typical of those seen on the other designs in this paper.

Minimum Dead Time (maximum duty cycle)

The dead time of the output switch was measured with the feedback resistance disconnected.

Vertical: 2 V/div
Horizontal: 1 µs/div
Coupling: dc

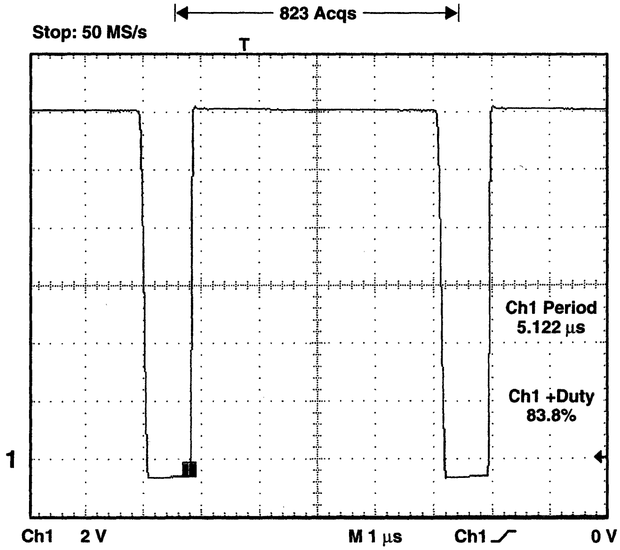


Figure A–1

Output Switch Drain to Ground Voltage

The input of the low-pass output filter is shown in Figure A–2. The high-level voltage is equal to the input voltage minus $V_{DS(on)}$. The low-level voltage is one diode drop below ground.

Vertical: 2 V/div
Horizontal: 1 µs/div
Coupling: dc

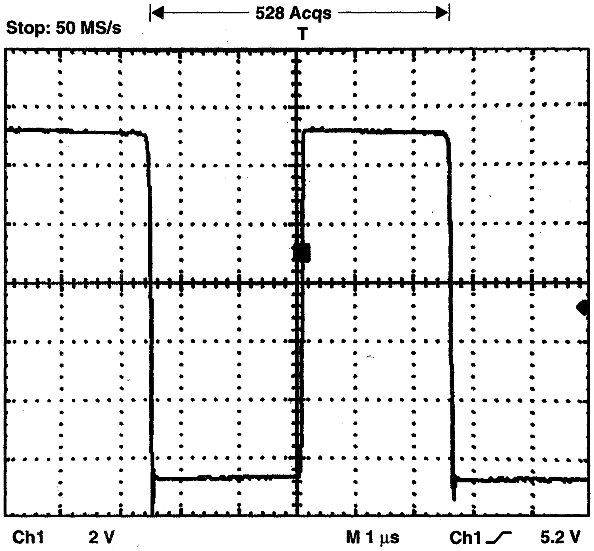


Figure A–2

Output Voltage Rise Time (electronic load)

The soft-start circuit slows the rise of the output voltage to prevent excessive overshoot.

Vertical: 1 V/div
Horizontal: 2 ms/div
Coupling: dc

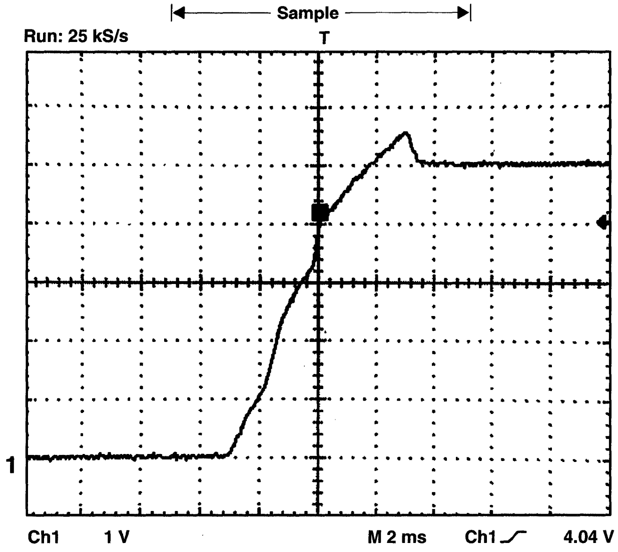


Figure A–3

Output Voltage Rise Time (resistive load)

This photo shows the response to a resistive load.

Vertical: 1 V/div
Horizontal: 2 ms/div
Coupling: dc

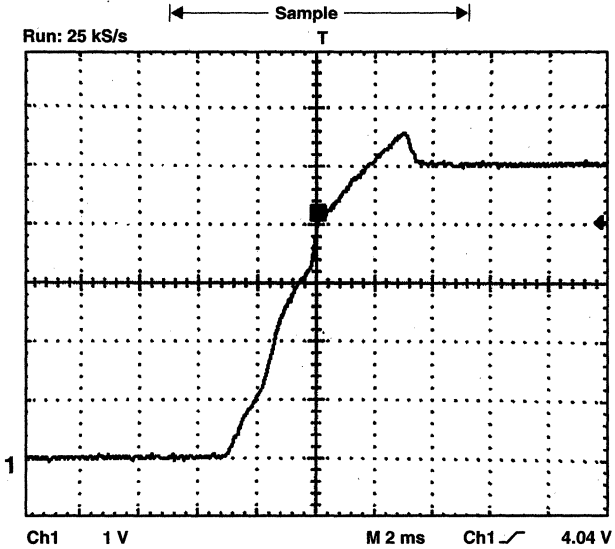


Figure A–4

Output Voltage Ripple

The output ripple is shown in Figure A–5. The triangular-shaped ripple is clearly a function of the ESR of the output capacitor.

Vertical: 2 mV/div
Horizontal: 2 µs/div
Coupling: ac

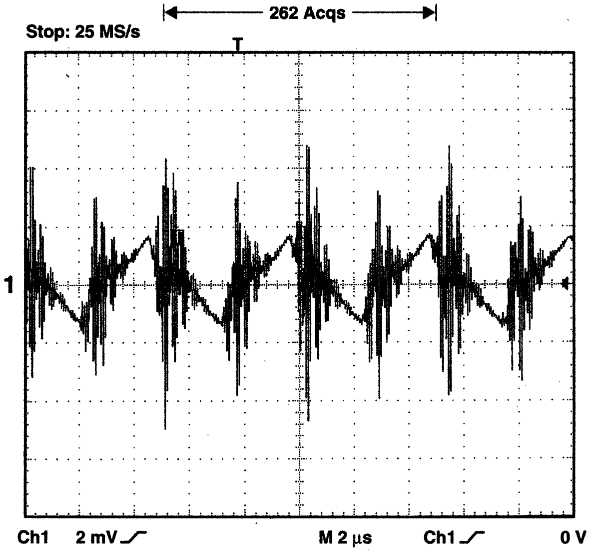


Figure A–5

Output Dynamic Response

The response of the output to step-load changes is shown in Figure A–6. The electronic load was stepped from 1.5 A to 3 A.

Top Waveform: V_O
Vertical: 100 mV/div
Horizontal: 0.5 ms/div
Coupling: ac

Bottom Waveform: I_O
Vertical: 1 A/div
Horizontal: 0.5 ms/div
Coupling: dc

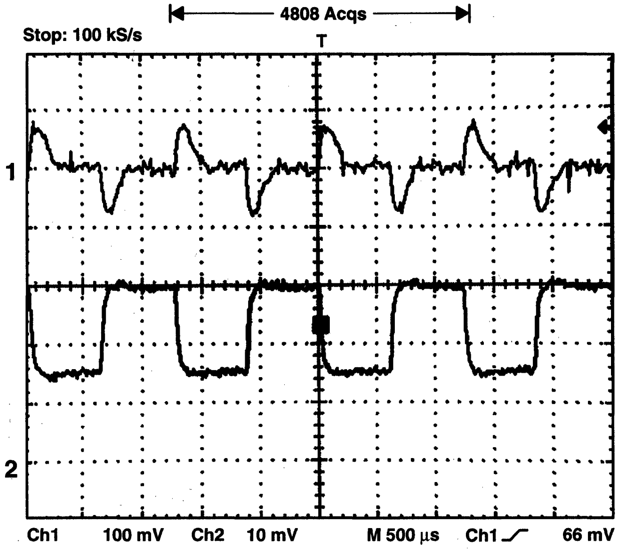


Figure A–6

Acknowledgement

This application report is the synergistic result of many individual efforts. The work involved included characterization of the controller chip; design, breadboarding, and debugging of application examples; and preparation of the report itself. Every effort has been made to provide a document that is useful and understandable to the customer/designer. The following list, though not all inclusive, represents the major contributors to this document:

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Component Selection and PCB Layout Guidelines for Low-Power DC/DC Converters

Contents

List of Illustrations

List of Tables

Component Selection Guidelines

Due to the wide variation in current levels in the typical power supply, the range of size of the components is usually extensive. Even in low-power dc-to-dc converters the power switch, rectifier, and output capacitor may range from very small surface-mounted parts to D-Pak size. The inductor is usually the largest component in low-power situations and determines the overall size of the supply.

Output-Filter Inductor

The key parameters to consider in selecting an inductor for an output filter application are inductance, continuous and peak current ratings, series resistance (DCR), and packaging. The inductance and current rating requirements are determined during the electrical design and depend heavily on:

- Input and output voltages, output current
- Converter topology
- Operating frequency
- Operating mode (continuous or discontinuous)
- Designer's preference

Inductance decreases as current increases in all inductors, but the slope and frequency onset of this decrease varies depending upon the core material, air gaps, and ac flux. Some inductors hold a relatively constant value out to a point where the inductance suddenly collapses, while others decrease slowly and continually over a wide range. Even within families of cores, the change in inductance over frequency with a change in permeability can be great. Inductance in ferrites is largely unaffected by ac flux. Some iron powder materials are strongly affected by ac flux changes that cause large inductance increases at higher flux levels. To ensure adequate performance, design the inductor for the peak current and at the lowest operating frequency. Pulse width modulator (PWM) tolerances can be 15% or more before considering the external timing component tolerances.

The series resistance (DCR) must be low enough to limit the heat rise to acceptable levels. The resistance of copper increases with temperature and can cause a degenerating condition on the output. Heat rise in inductors is hard to calculate; the easiest way to determine this is to use the manufacturers recommended current ratings at maximum temperature. The DCR may have to be lower than that necessary for heat rise in order to meet the efficiency and regulation specifications at low line.

Core losses are generally low enough that they do not cause a thermal problem in these applications except at high operating frequencies and at high ripple current.

Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficiently high.

Output-Filter Capacitor

Unless the converter is to be subjected to large load transients, the filter capacitor is chosen to limit the output ripple voltage to specification levels. Most low-power converters utilize single-stage filter designs.

The filter capacitor passes most (ideally all) the ac components of the inductor current and the impedance must be low enough to limit the ripple voltage. The impedance consists of a capacitance in series with a resistance (equivalent series resistance, ESR) and an inductance (equivalent series inductance, ESL), and depending on the capacitor technology, the overall impedance is dominated by either the capacitance or the ESR at the frequencies of interest. Besides impedance, the voltage rating must be greater than the maximum output voltage and the ripple current must be within ratings.

Four capacitor technologies, low-impedance aluminum, organic semiconductor, solid tantalum, and multilayer ceramic, are suitable for low-cost commercial applications. Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but the ESR is higher than the other three. Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds — a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but some of the size and performance advantage is sacrificed. Solid tantalum chip capacitors and ceramic capacitors are probably the best choices if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

Now, high-capacitance multilayer-ceramic capacitors are available. These have very low ESR (less than 5 mΩ), but the capacitance tolerance is very broad (typically +80% to –20% and varies with bias). In addition, the larger values (22 µF and larger) have ESL problems that must be considered in use. The ESR is so low that the resulting zero in the loop response generally can be ignored, but the capacitance is too variable to rely on for the output filter response and should be paralleled with another more stable, higher ESR capacitor. Wide variations in the output capacitance affects the open loop filter poles and makes the power supply more sensitive to external factors. When using 22-µF or greater ceramic, it is recommended that a 0.47-µF capacitor or larger be used in parallel to reduce the effects of the internal ESL.

Input-Filter Capacitor

Input filters supply the surge current needed during the power-switch on time. They must supply the current without significant voltage droop for the maximum turn-on time. In addition, the current surge when the input voltage is applied must be considered. Buck and buck-derived configurations have a step function input current waveform with large harmonic content. Boost and flyback regulators have triangular or ramp waveforms. These instantaneous step changes require large surge capability. Low ESR capacitors allow a much greater surge than high-ESR capacitors. Tantalum capacitors do not tolerate this surge and so should not be used in input filter applications. Aluminum electrolytics are excellent here due to their large capacitance-to-volume ratio and surge current capabilities. For surface mount, ceramics work well and their low ESR prevents the input voltage from having a voltage step.

Power Switches

Many converters can be implemented with bipolar or MOSFET transistors as the power switch. Bipolars are inexpensive and can perform well in low-voltage applications, but designing a drive circuit to realize the performance is not a trivial effort. Furthermore, complex base-drive schemes can eliminate much, if not all, of the cost advantage. MOSFETs offer the fast switching times required for high-frequency operation, using relatively simple, low-component-count gate-drive circuits.

Output Rectifiers

The output rectifier is critical to good converter performance. Rectifier conduction losses are generally a significant percentage of the total converter dissipation, and either high-conduction loss or poor-switching performance increases dissipation in other components. The key parameters to consider in selecting the rectifier include the:

- Current rating
- Voltage breakdown
- Forward voltage drop
- Switching speed

- Junction capacitance
- Thermal resistance
- Packaging

After voltage rating, the primary concern is usually power dissipation, either to ensure that the rectifier operates within its junction temperature rating or to optimize the overall converter efficiency. A low forward voltage drop reduces power dissipation that minimizes the use of heatsinks to maintain junction temperature to acceptable levels and optimizes power converter efficiency. Fast switching speeds are essential to minimize dissipation. Schottky rectifiers are popular choices in low-power, low-voltage applications for their characteristic low forward drop and fast switching.

Current rating is a secondary concern for most designs. Typically, the device required to limit dissipation to acceptable levels has a current rating that is a factor of two or more greater than the application requires.

The breakdown voltage rating must at least equal the maximum input voltage in buck converters and the output voltage in boost converters. Some margin for the voltage surges, spikes, and ringing typically encountered in practical applications is also advisable.

Low junction capacitance minimizes component size and power dissipation in snubbing networks.

Rectifiers are readily available in a wide range of packages for both lead and surface mount applications. The surface mount packages tend to perform better than the lead mounts due to the reduced parasitics; however, they are harder to heatsink when external heatsinking is required at higher power levels.

The output rectifier can be replaced with a low $R_{DS(on)}$ MOSFET (synchronous rectifier) in applications where efficiency overrides cost concerns.

Snubber Network

Converters almost universally suffer from ringing on the voltage waveform at the node where the power-switch, output inductor, and rectifier are connected. The ringing results from driving parasitic inductances and capacitances with fast rise-time waveforms and ranges in severity from objectionable to unacceptable depending on component selection and printed-circuit board (PCB) layout. A series RC-snubber network in parallel with the rectifier is the simplest way to minimize the problem. Since deleting components from a PCB layout is usually easier than adding them, the safest strategy is to include the network in the initial design and delete it, if it is not needed.

High frequency ceramic or film capacitors and film resistors should be selected for snubber applications; avoid wire-wound resistors because they tend to be inductive.

PCB Layout Considerations

Electrical design is only half the work in the creation of a reliable power supply. Unlike digital circuits, power circuits handle a broad range of currents — from the microampere control current to the tens (or hundreds) of amperes flowing in the power stage. The production of clean output power with minimal noise depends critically upon PCB layout. Power supply circuits also produce high-frequency signals that may cause many problems within the load or the source if not properly handled. Even though a power supply can operate at 50 kHz to 500 kHz, the switching edges can have rise and fall times in the order of 10 ns or faster, correlating to frequencies of up to 100 MHz. Without proper layout, radiation can be a major problem. Proper layout techniques generally include minimizing high-current loops within the power stage, proper grounding of the control stage, and proper sizing of the traces to adequately handle the peak currents. Ground planes are useful but cannot solve every problem. The control of current flow within the supply is more important.

Magnetic coupling between adjacent circuitry is a major source of noise pickup. The magnetic field produced by a current is proportional to the area of the loop in which it circulates. Thus, noise coupling can be greatly reduced by minimizing the loop areas.

A ground plane is extremely useful in satisfying this goal. On thru-hole boards, a top-surface ground plane with strategic cutouts to control the flow of output currents and control-section currents is ideal. Surface-mount boards usually have minimal top-surface area for a ground plane.

Other points to consider during the PCB layout process are selection of the proper components, separation of the ground plane to reduce cross-conduction, snubbers on the commutation/output rectifiers, proper placement of EMI suppressing components to reduce noise pickup/transmission, and thermal considerations.

Power Stage Considerations

The power stage includes the low-pass output filter, the power switch, and the input filter. It contains very high circulating currents and, therefore, should be given the highest priority when laying out the PCB. Figure 9–1 shows the current paths for a typical buck converter. The charging (forward) current, I_1, flows through the input capacitor, the power switch, and the inductor before splitting between the output capacitor and the load. The inductor discharge (commutating) current, I_2, flows through the commutating diode and the inductor, then to the output capacitor and the load. The peak value of these currents is the same. The paths for these currents should be as short as possible.

The input filter capacitor should be close to the power switch and the commutating rectifier. In buck regulators, the input current waveform from the input capacitor to the power switch is a step function. This contains large harmonics that are difficult to filter out. The closer that the input filter is to the power switch, the less the radiation. Flyback regulators have a ramp input waveform that has a high-frequency trailing edge.

Next in priority, due to its relatively high current level, is the drive circuit for the power stage. It should be placed as close to the power switch as possible. The power switch generally has a large input capacitance associated with its gate. High peak currents achieve the very fast rise and fall times required for high efficiency. If the gate lead trace is longer than approximately 2 inches, a small (approximately 10 Ω) resistor should be placed in the trace near the FET to damp the LC tank formed by the inductance of the trace and the gate capacitance of the FET. Current I_{D1} is the turn-on current that charges the gate capacitance and current I_{D2} is the turn-off current that discharges this capacitance. When using bipolar power switches, base capacitance is not a problem, but the average drive current is much higher, resulting in the same requirement for short current paths.

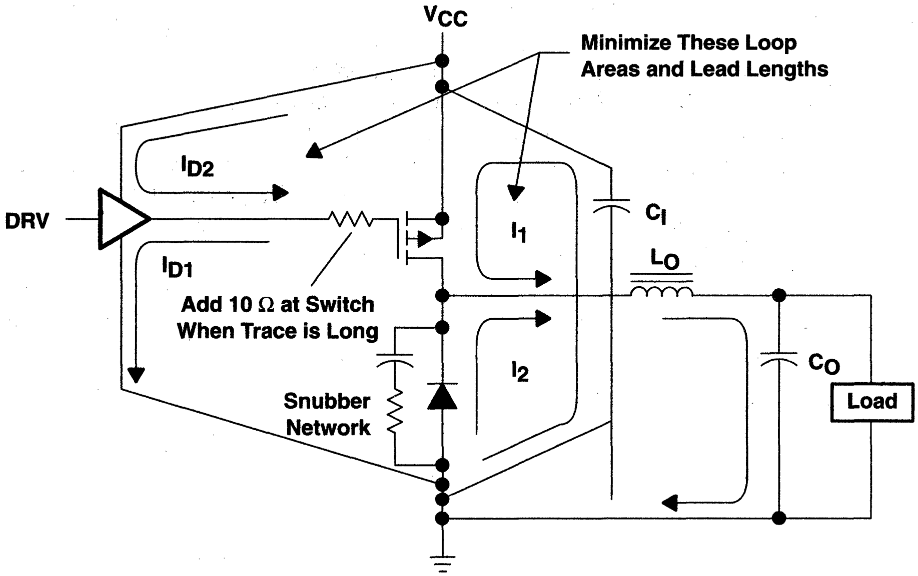


Figure 9–1. Buck Power Stage Layout Considerations

In continuous-mode boost converters, the input current is higher than the output current by the ratio of the output voltage to the input voltage divided by the efficiency. In a 5-V to 15-V, 5-ampere, 90% efficient boost converter, the current through the inductor and power switch is over 16 amps! Discontinuous-mode converters (of any type) have much higher currents than their continuous-mode counterparts.

In converters with high voltages present, such as offline switchers and in some boost or flyback converters, care must be exercised to ensure that proper isolation of the high voltage is done. Various safety standards from safety agencies (such as UL and VDE) specify the required creepage distance between high-voltage points and the user. In some cases, the effects of high-voltage transients (from startup, lightning, or static) must also be considered. Converters operating from the ac mains usually have input EMI filters. To be effective, these filters must be physically located close to the input source and laid out in a very tight configuration noting, however, that the high-voltage transients mentioned previously may be doing their best to try to bypass the filter.

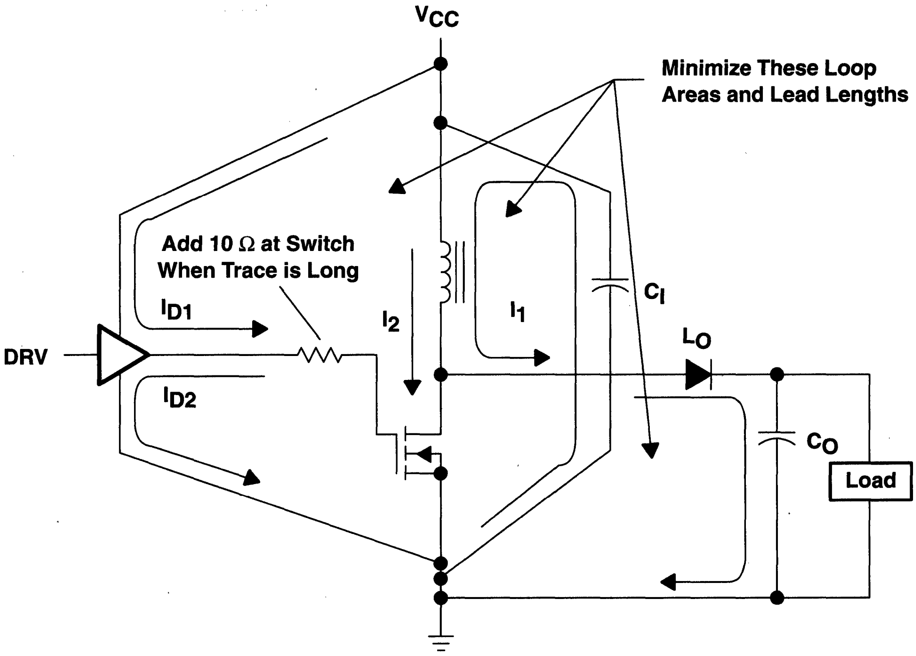


Figure 9–2. Boost Power Stage Layout Considerations

Power stage currents are dependent upon the output requirements, input voltage, and operating mode of the power supply. Figure 9–3 shows the inductor-current waveforms for a continuous-mode and a discontinuous-mode power supply with the same output current and input voltage. The peak current of the discontinuous supply is much higher and varies with duty cycle.

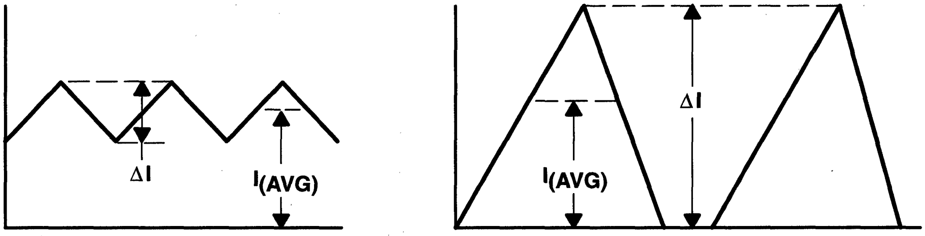


Figure 9–3. Continuous vs. Discontinuous-Mode Inductor Current

Output Stage Considerations

In a Buck regulator, the output-filter capacitor placement is not as critical as the input filter. Output current flows through the output inductor to the load. Additional trace length in this path acts as additional capacitance as long as the power and return traces are physically close to each other. The trace length from the output capacitor to the main output trace should be kept as short as possible. This minimizes the series resistance and inductance between the capacitor and the main trace. In many cases, parallel capacitors are used in the output filter to reduce the equivalent series resistance (ESR). If the capacitors are connected at equal intervals along the output path, the effective ESR of the first capacitor is much lower than the last capacitor. Care must be used in this configuration to make sure that the first capacitor in the string is not overloaded by the higher ripple current that it must conduct.

Discontinuous-mode boost regulators have large current pulses in the output capacitor. Here, the capacitor should be close to the power switch to reduce magnetic radiation.

The ideal configuration on multilayer boards is for the output and return traces to be directly over each other to minimize the enclosed loop inductance and to increase coupling capacitance. This technique can be beneficial when applied to almost any closed signal path. On single-sided boards, the optimum solution is closely-paralleled traces, see Figure 9–4.

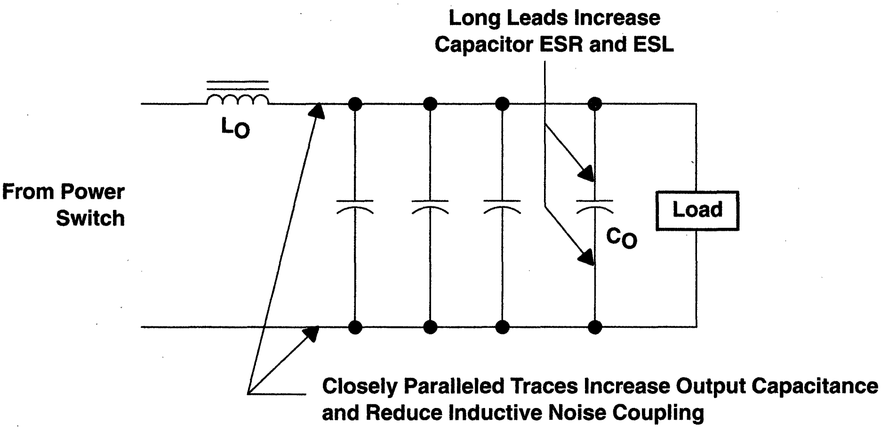


Figure 9–4. Output Layout Considerations

Controller Layout Considerations

Ground connections are very critical in the control stage of a power supply. Any voltage difference between the feedback divider ground and controller ground results in an error in the output voltage. Noise pickup in the sensing circuit is amplified and fed directly to the output. Ideally, the controller supply current should not flow through the feedback path. This is not always possible, though, and the next best choice is to have the controller referenced to the output ground as close as possible. The supply voltage should be bypassed to prevent transient currents from the controller from being propagated across the PCB. The bypass capacitor, $C_{(bp)}$, should be located as close as possible to the controller with short leads to the V_{CC} and ground terminals. Surface-mount chip capacitors mounted next to the controller give the shortest possible routing. Again, current loops should be minimized with parallel traces to reduce noise radiation and pickup.

The feedback path from the low-impedance output through the resistor divider to the high impedance operational amplifier inputs should be as short as possible and should consist of parallel paths to reduce noise pickup. The divider ground point should be close to the output ground, but more importantly, the center point of the divider should be close to the input error amplifier due to its high impedance and noise susceptibility. Sometimes breaking the ground plane into two or more sections with a single common connection point can help in keeping the high output-return current from flowing around or near the controller circuit. This technique can greatly reduce noise pickup by the sensitive controller circuitry.

Many controllers today have the driver stage built in. This compounds the problems of ground currents, especially when the driver does not have its own power ground terminal. It is even more important, in this case, to locate the controller close to the output to reduce the effects of error currents.

In both the cases discussed previously, close to the output does not imply close to the power stage. The switching elements in a modern high-frequency power supply generate large amounts of EMI that can be magnetically coupled into the high-impedance input of the controller. The further away from these elements the controller is, the harder it is for the signals to couple. In the small circuits of today, this is becoming harder to do. If at all possible keep the error amplifier and reference voltage terminals away from the power stage.

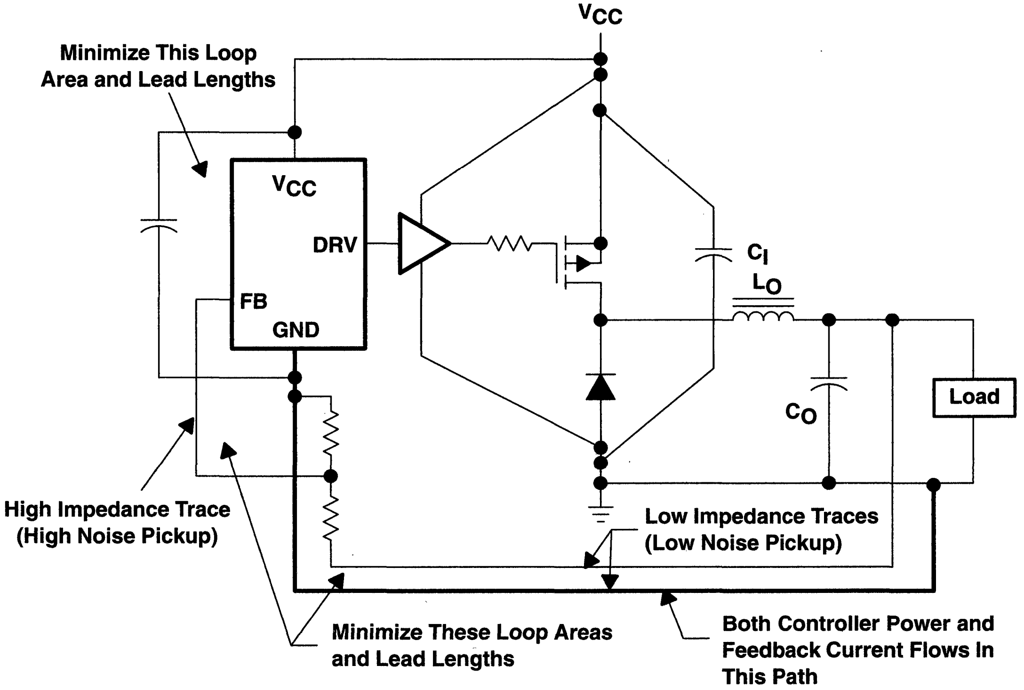


Figure 9–5. Controller Layout Considerations

Trace Width Considerations

Trace widths on a power supply board are a compromise among minimum loop area for noise reduction, maximum trace widths for low IR drops, and available board area. Outside layers of PCBs are generally available with 1-ounce and 2-ounce copper, a reference to the weight of the copper per square foot of board. Inner layers of multilayer boards can have 1/2-ounce copper. One-ounce copper is nominally 1.3435 mils or 0.0013435 inch thick. Wire is generally measured in circular mils. A circular mil is the area of a circle that is 1 mil in diameter. To convert circular mils to square mils, multiply by the factor $\pi/4$. In order to have the same current density as 20-gauge wire (1022 circular mils) using 1-ounce copper, a trace width of 597 mils is required! However, flat traces on a PCB can carry more current than the same amount on copper wire due to the greater surface area of the trace for heat radiation into the air and heat conduction onto the board itself. Good design practice limits the temperature rise on FR4 board to 20°C (MIL-STD-275C). The current flowing through the traces is derated to account for several factors. The recommended derating factors are as shown in Table 9–1.

Table 9–1. Derating Factors

Condition	Current Multiplication Factor
Tin/lead surface or auto soldering	1.42
Solder mask or insulating surface	1.18
Copper thickness ≥ 3 Oz.	1.18
Base material ≤ 0.031 in.	1.18

The information in Table 9–2, taken from MIL-STD-275C (commercial equivalent is ANSI/IPC-D-275), shows the maximum derated current to achieve a temperature rise of 20°C or less.

Table 9–2. Maximum Derating Current for $\Delta T_A \leq 20°C$

Trace Width (Inches)	Current (Amps)
0.025	2
0.075	5
0.200	10
0.440	20

The information given in Table 9–2 is the maximum recommended current. The resistance of the trace still needs to be calculated to verify that the voltage drop is satisfactory for the application.

The resistance of a 10-mil trace of one-ounce copper is 502 mΩ per inch. For any given trace width, the resistance is:

$$R = \frac{0.00502L}{WT}$$

Where:

R is the trace resistance in ohms
L is the length of the trace in mils
W is the width of the trace in mils
T is the copper weight of the board in ounces per square foot

Two useful variations of this formula are:

$$W = \frac{0.00502L}{RT}$$ gives the required width in mils for a desired trace resistance.

$$W = \frac{0.00502LI}{VT}$$ gives the required width in mils for a desired voltage drop.

Where:

W is the width of the trace in mils
L is the length of the trace in mils
I is the current in amps
V is the voltage drop in volts
T is the copper weight of the board in ounces per square foot

Example:

When a circuit with 10 amps and a 100 mV drop is desired on a 1-inch trace, the trace width is calculated as follows:

$$W = \frac{(0.00502)(1000)(10)}{(0.1)(1)} = 502 \text{ mils using 1-ounce copper}$$

$$W = \frac{(0.00502)(1000)(10)}{(0.1)(2)} = 251 \text{ mils using 2-ounce copper}$$

$$W = \frac{(0.00502)(1000)(10)}{(0.1)(3)} = 167 \text{ mils using 3-ounce copper}$$

As can be seen in the previous example, heavier-weight copper is very useful in power supply circuits. A secondary advantage to heavy copper traces is the heat-sinking ability of copper. This can come into play when calculating the junction temperature (discussed later in this chapter). Generally, the resistance of the circuit traces should be insignificant compared with the rest of the circuit. The power stage of a converter may contain a MOSFET with less than 50 mΩ of on-resistance, an inductor with less than 100 mΩ of dc resistance (DCR) and an output capacitor with 100 mΩ of ESR. The trace resistance for this circuit should be in the order of 25 mΩ (both signal and return path) to meet this requirement.

Thermal Considerations for Surface-Mount Semiconductors

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Once the power dissipated in each device is calculated, the operating junction temperature must be determined to verify a safe operating environment. Junction temperature is found using the formula:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

If the junction temperature is higher than the desired maximum, one of the three approaches listed previously can be used to reduce $R_{\theta JA}$.

Improving the power-dissipation capability generally means adding a thermal conduction plane or heatsink to the PCB. Both choices require extra board space, but can be better than adding multiple or larger devices. Heat flows from warmer surfaces to cooler surfaces. If a naturally cooler surface is available, it would be an ideal heat sink.

Increasing the thermal coupling of the component to the PCB can reduce $R_{\theta JA}$. This can be implemented by the use of thermal compound or soldering of the component to the copper.

The use of forced airflow in low-power converters is generally an undesirable solution due to the added power useage of the fan. Natural convection airflow can be enhanced by the proper placement of the components and any vents that are available. Since warm air rises, vertical surfaces tend to transmit heat to the air better than horizontal surfaces. The hottest devices should be located at the top of the board or toward the output side of the airflow so as to reduce their effect on other components.

If $R_{\theta JA}$ cannot be reduced to a satisfactory level and power dissipation cannot be reduced, the only other alternative is to select a larger device that can dissipate the power.

Figure 9–6 is an example of a thermally enhanced layout for a surface-mount power package with graphs showing the effects of airflow and thermal conduction planes of various sizes.

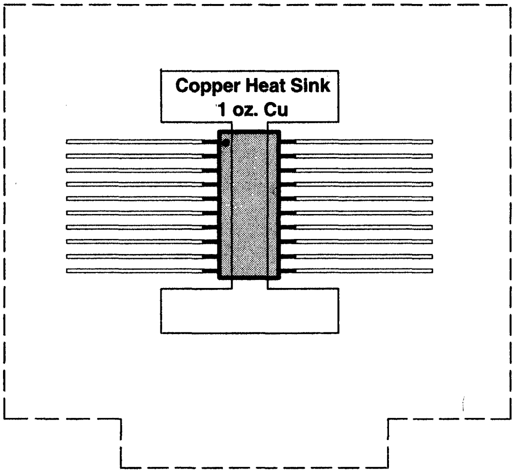


Figure 9–6. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT vs AIR FLOW

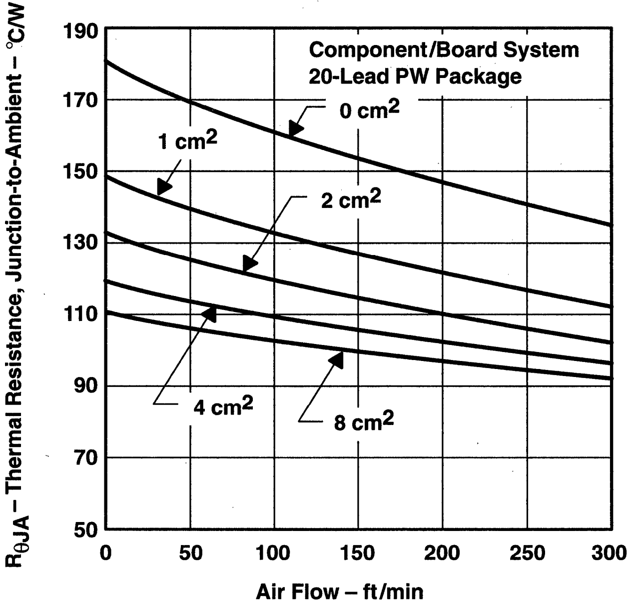


Figure 9–7

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT vs AIR FLOW

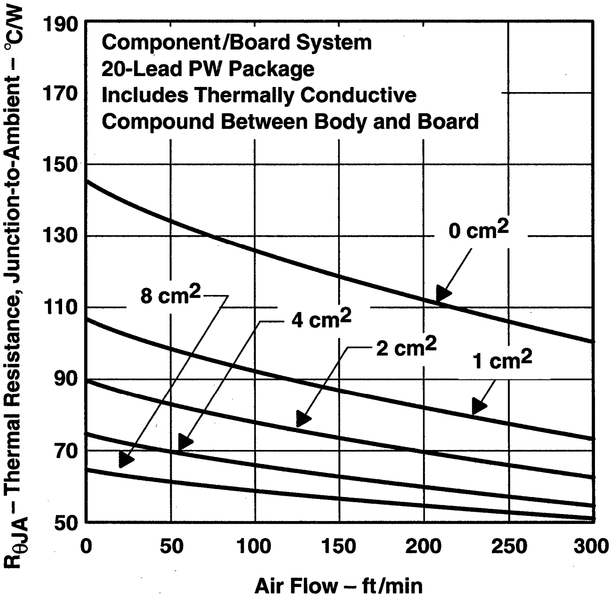


Figure 9–8

Example

Figure 9–9 is an example schematic and layout of a dual output regulator using the TL1454 controller chip. Using the techniques discussed in this document resulted in a regulator with very clean outputs that produced little noise.

Note that the top side ground plane (Figure 9–10) is cut into two sections to keep the return currents in the power section from flowing in the control section ground. The common point for the two sections of the ground plane is at the bypass capacitor for the controller chip. This was done because the outputs are located at opposite sides of the board. Usually, the common point should be located as close as possible to the output. Also note the short distance between the power switches Q1 and Q2 (Figure 9–11), the input capacitor C1, and the output capacitors C12 and C13. Heavy traces were used in the power section. The drive circuits were located so as to minimize the distance between the controller and the drive transistors and between the drive transistors and the power switches. In this layout the feedback traces are longer than is usually desired, but with the separated ground planes and low inductance path, this configuration worked very well. A better solution would have the feedback resistors closer to the controller.

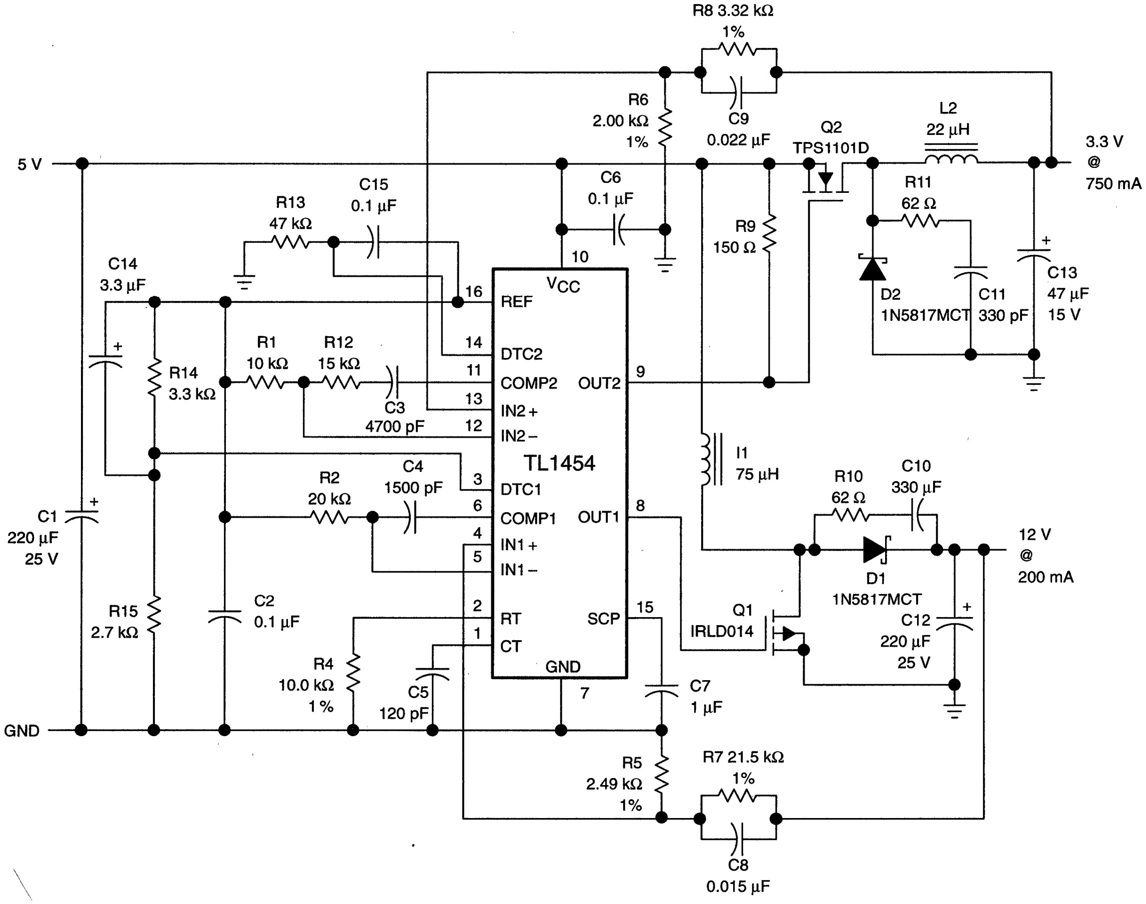
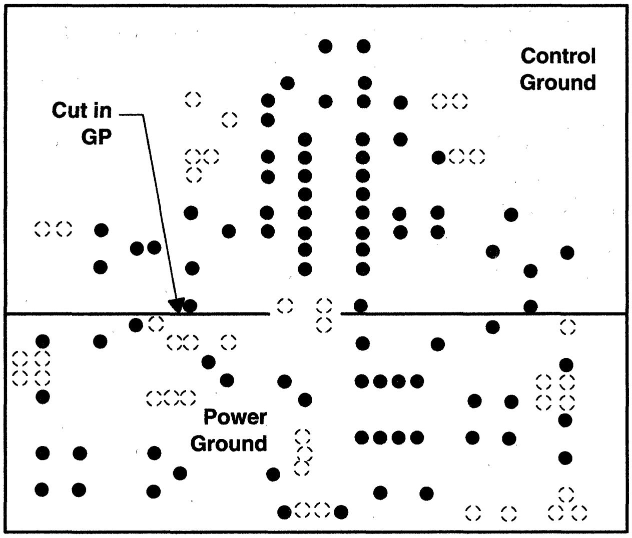
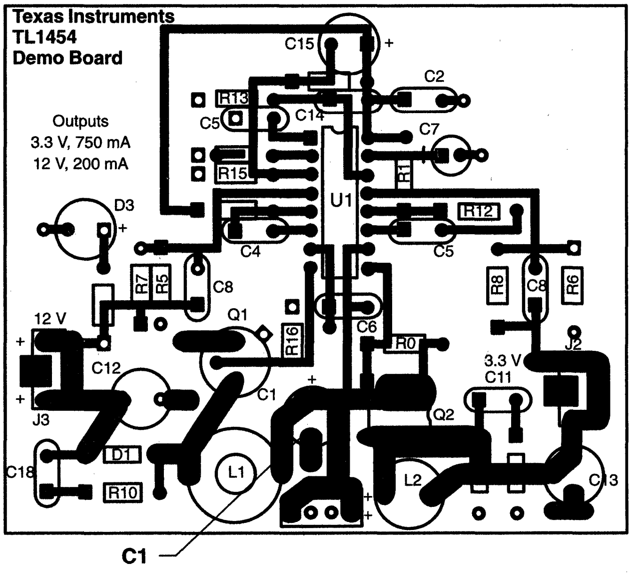


Figure 9–9. Dual Regulator Schematic



Top Side (Ground Plane)

Figure 9–10. Top Side Ground Plane

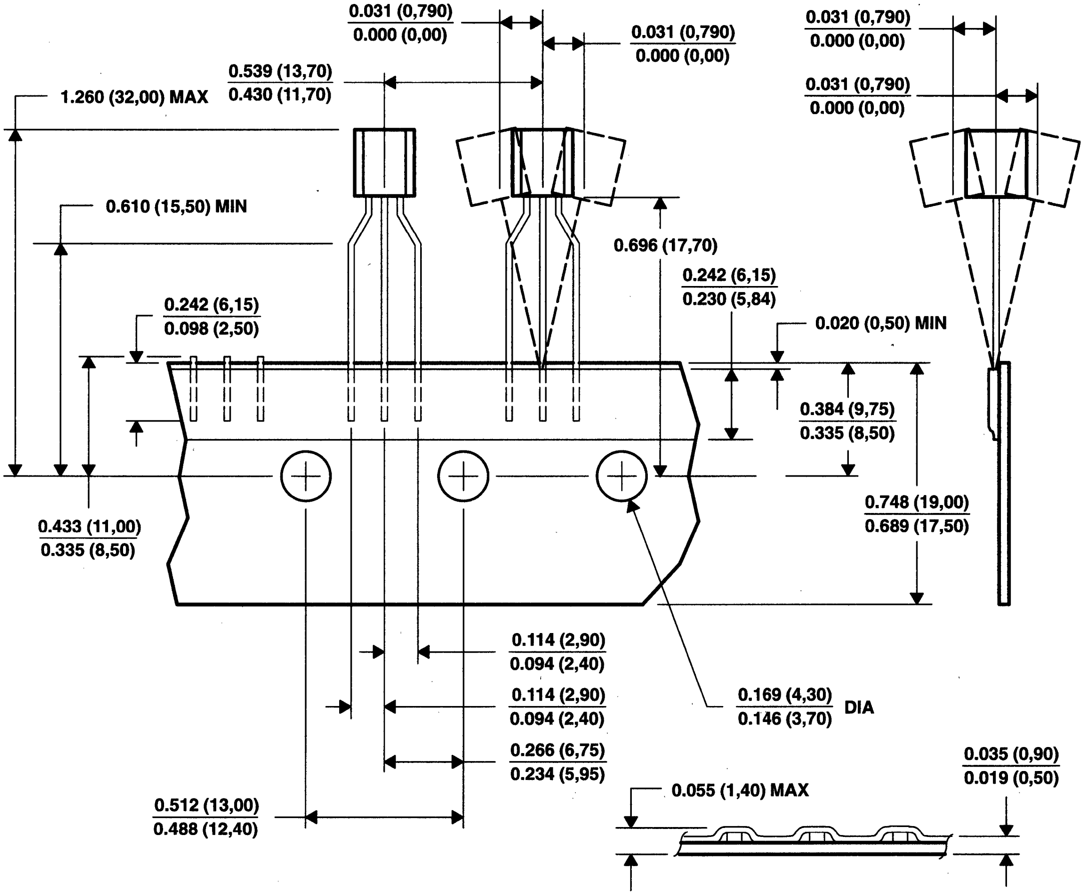


Bottom Side (Top View With Top Silk Screen)

Figure 9–11. Solder Side and Component Layout

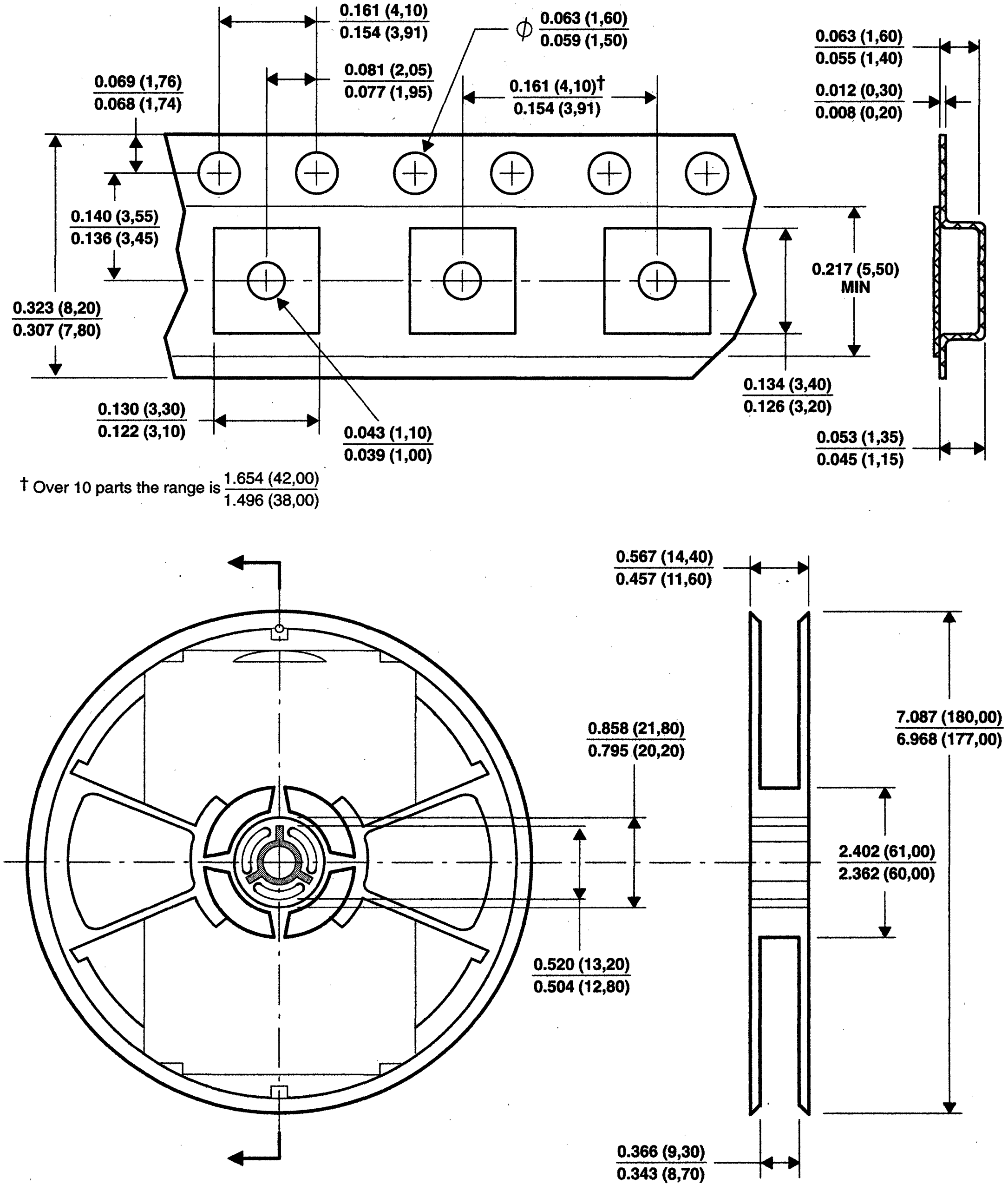
Mechanical Data 10

Contents



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Figure 10–1. Lead Taping Detail for TO-226-A (TO-92 Package)



† Over 10 parts the range is $\frac{1.654\ (42{,}00)}{1.496\ (38{,}00)}$

Figure 10–2. Tape and Reel Information For the SOT-23 (DBV Package)

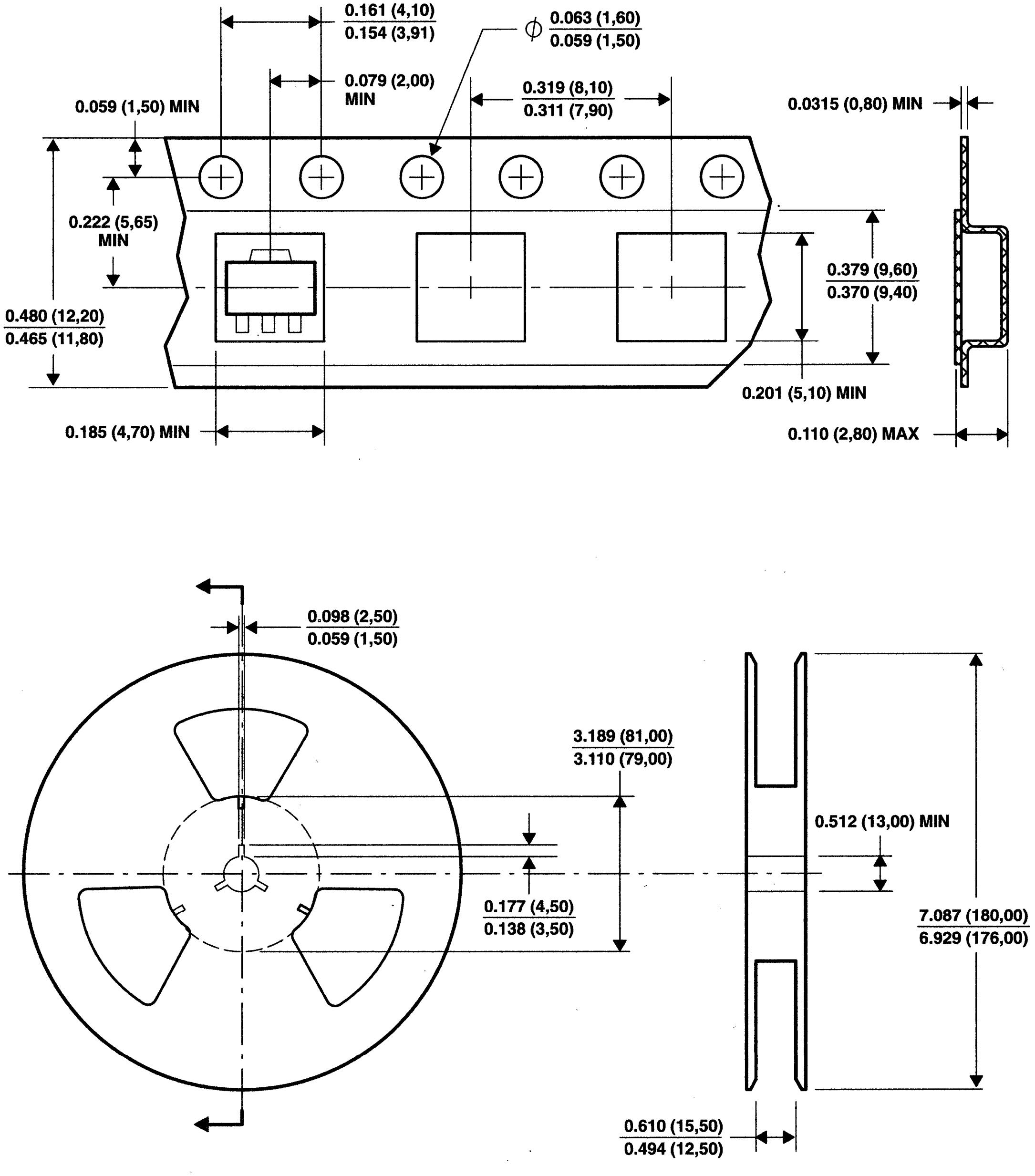
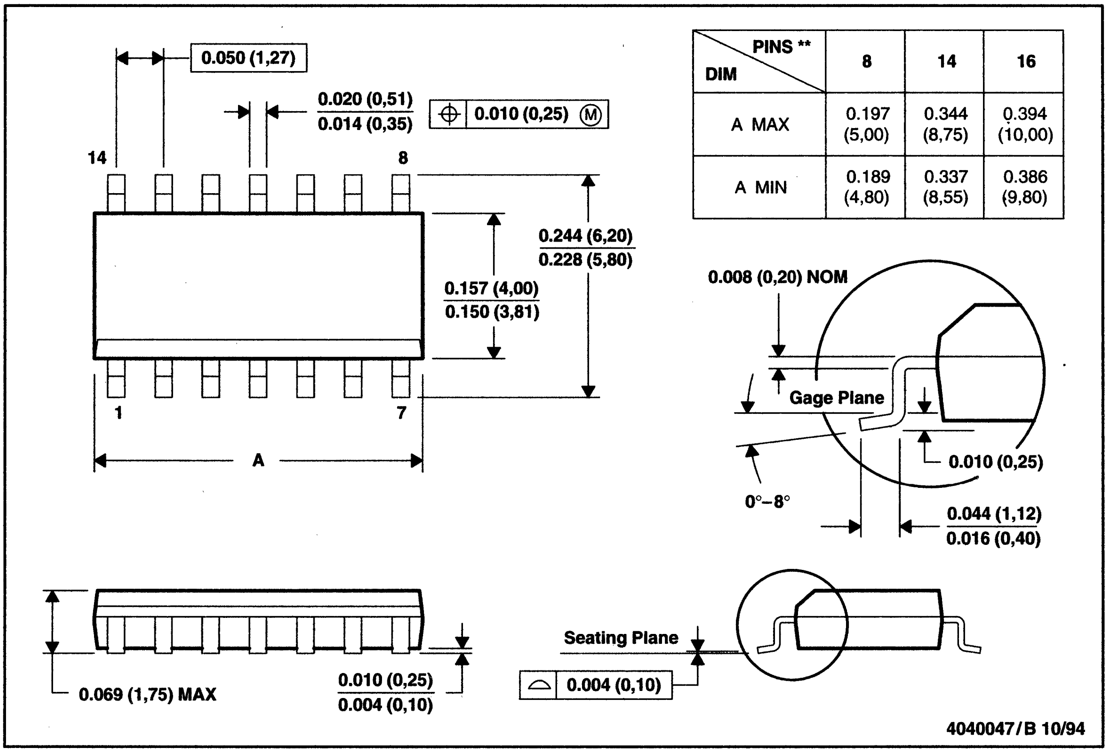


Figure 10–3. Tape and Reel Information For the SOT-89 (PK Package)

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad
- E. Falls within JEDEC MS-012

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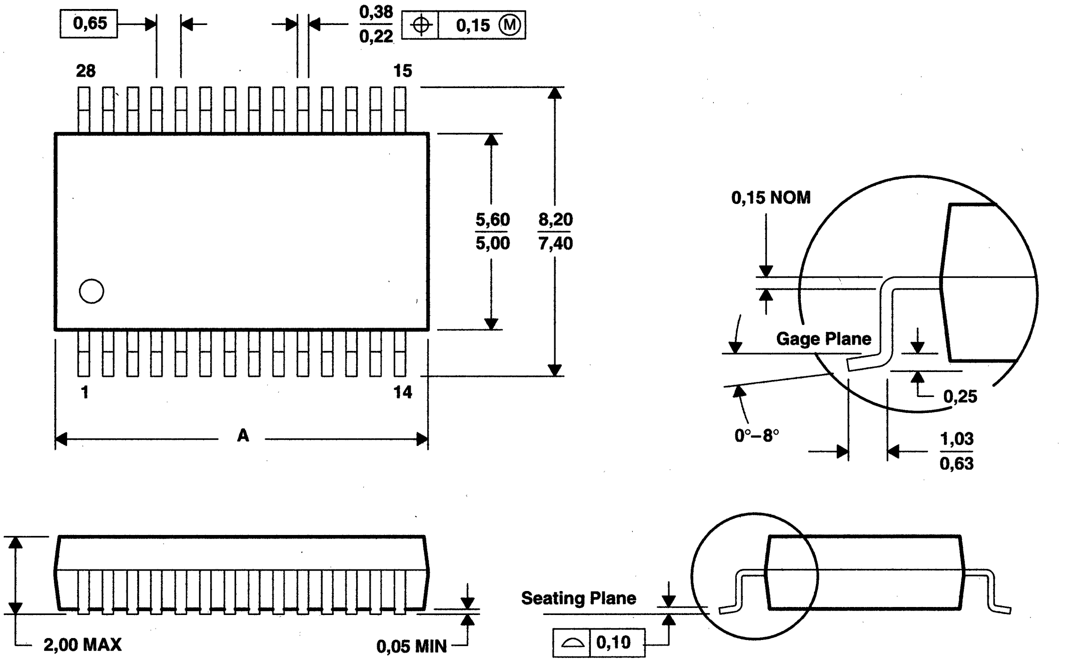
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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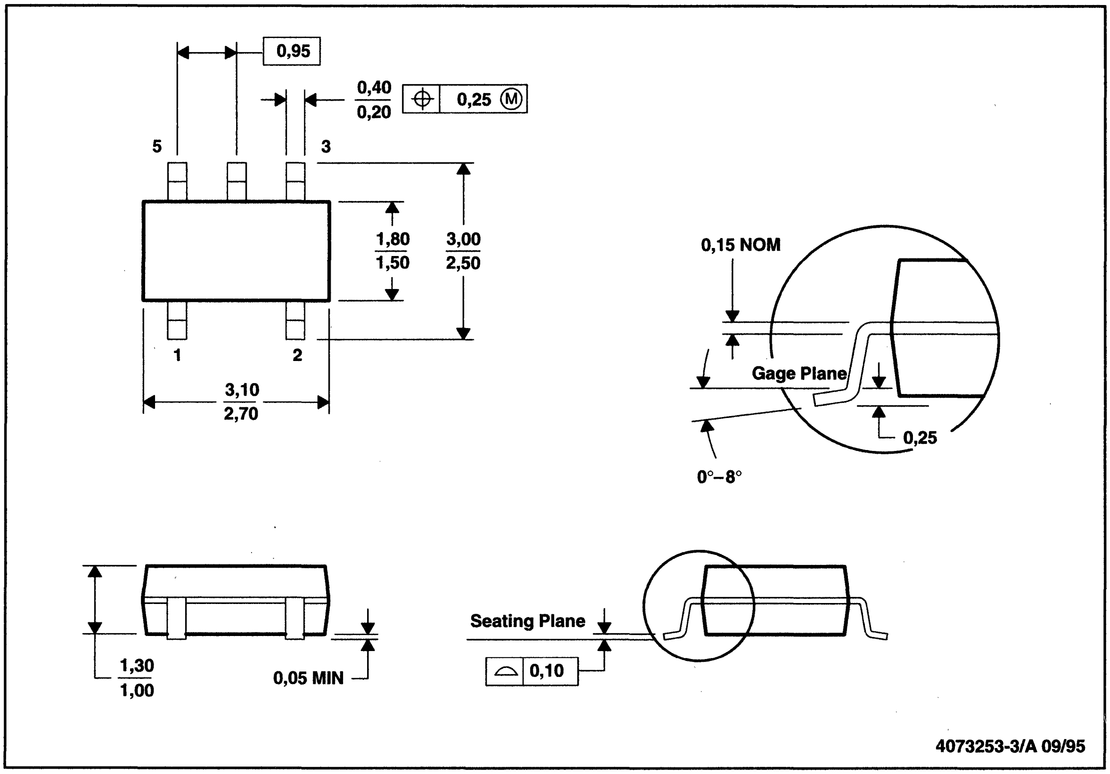
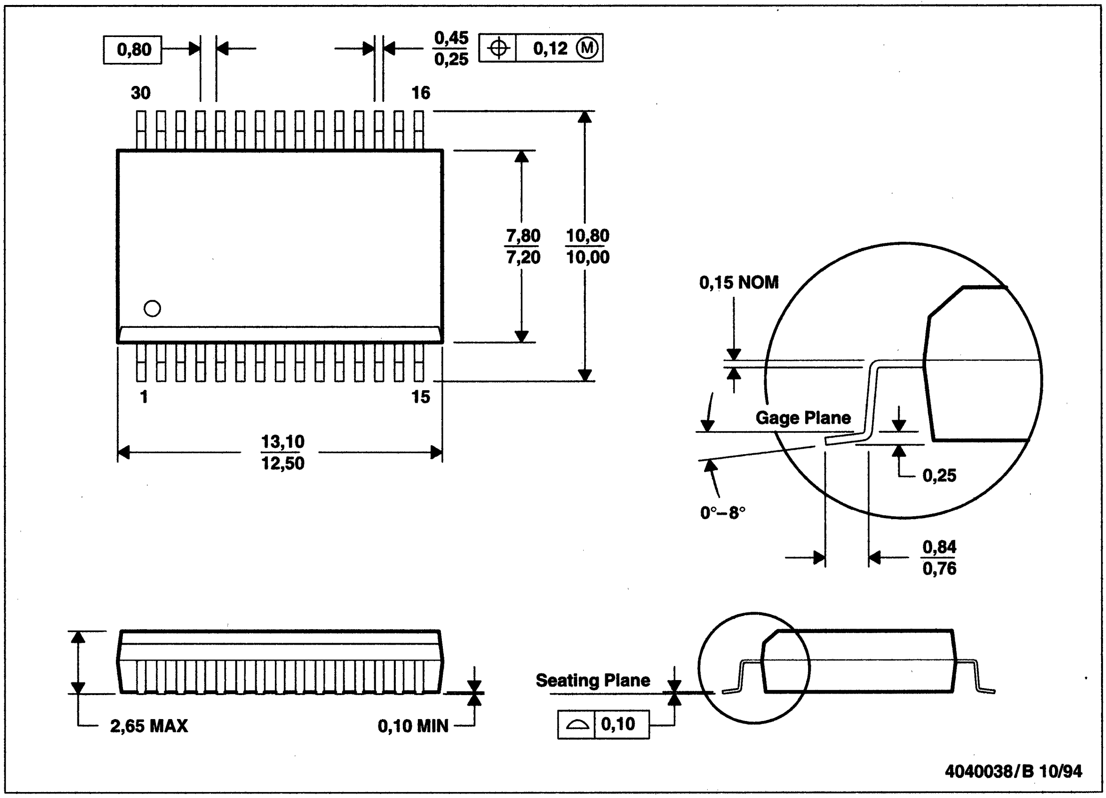
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

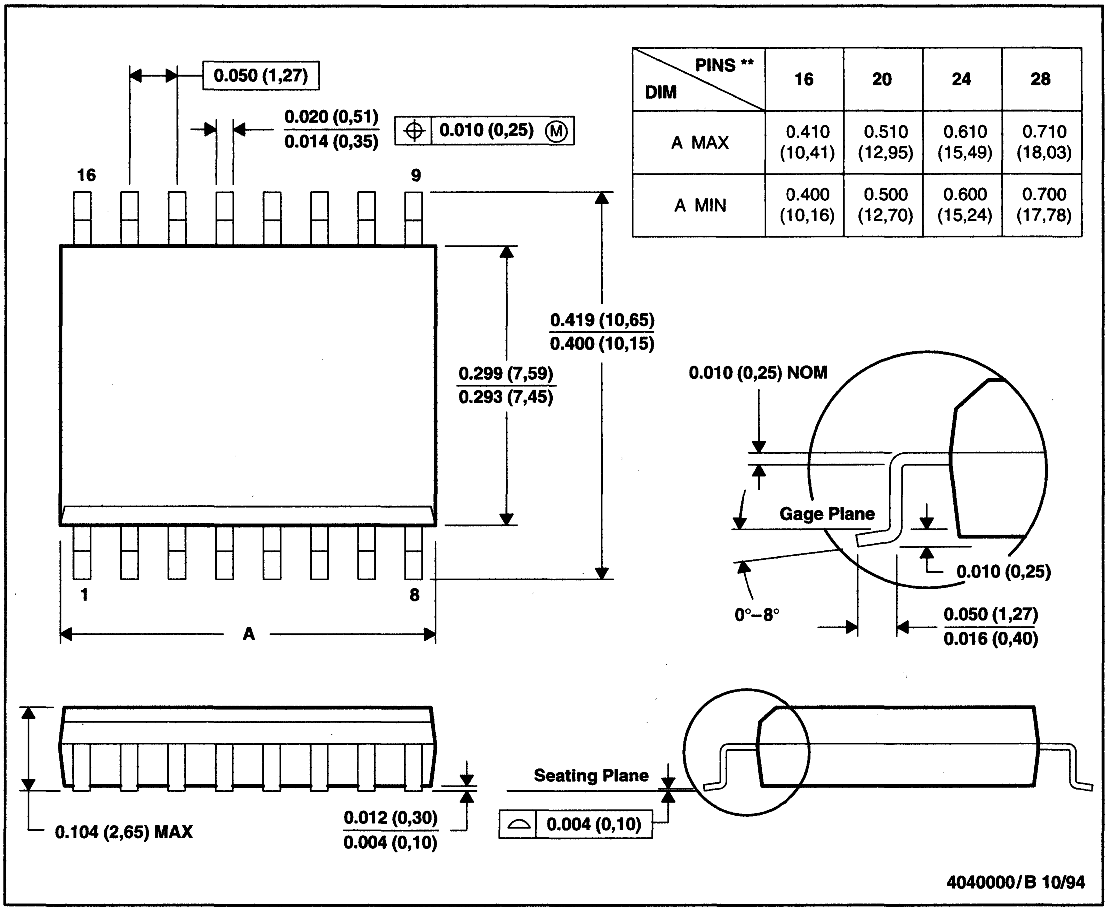
DF (R-PDSO-G30) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



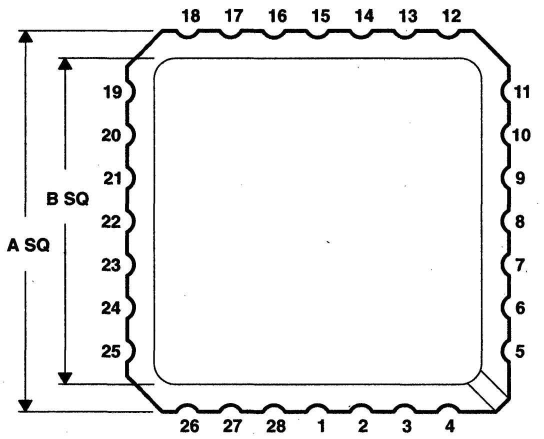
PINS ** DIM	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

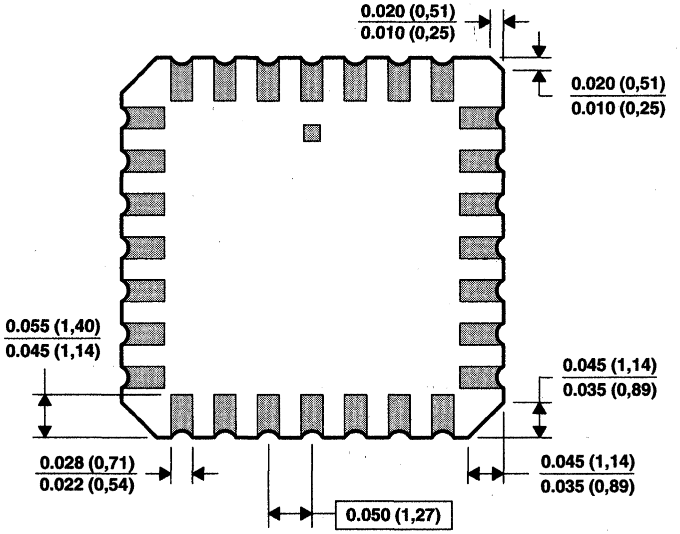
OCTOBER 1995

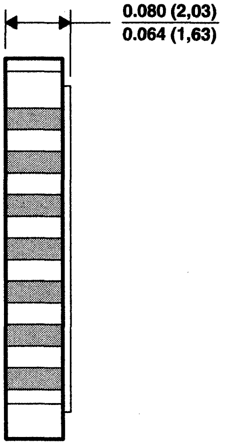
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





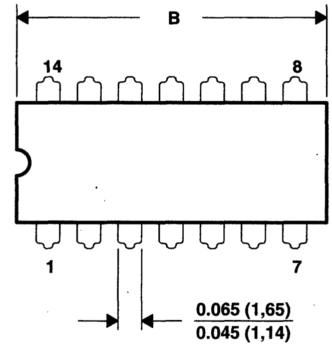
4040140/B 10/94

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

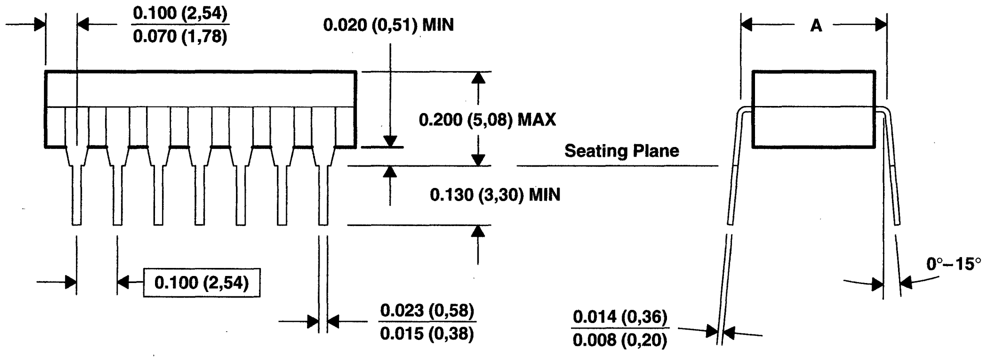
OCTOBER 1995

J (R-GDIP-T**) CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



PINS ** / DIM	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



4040083/B 10/94

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

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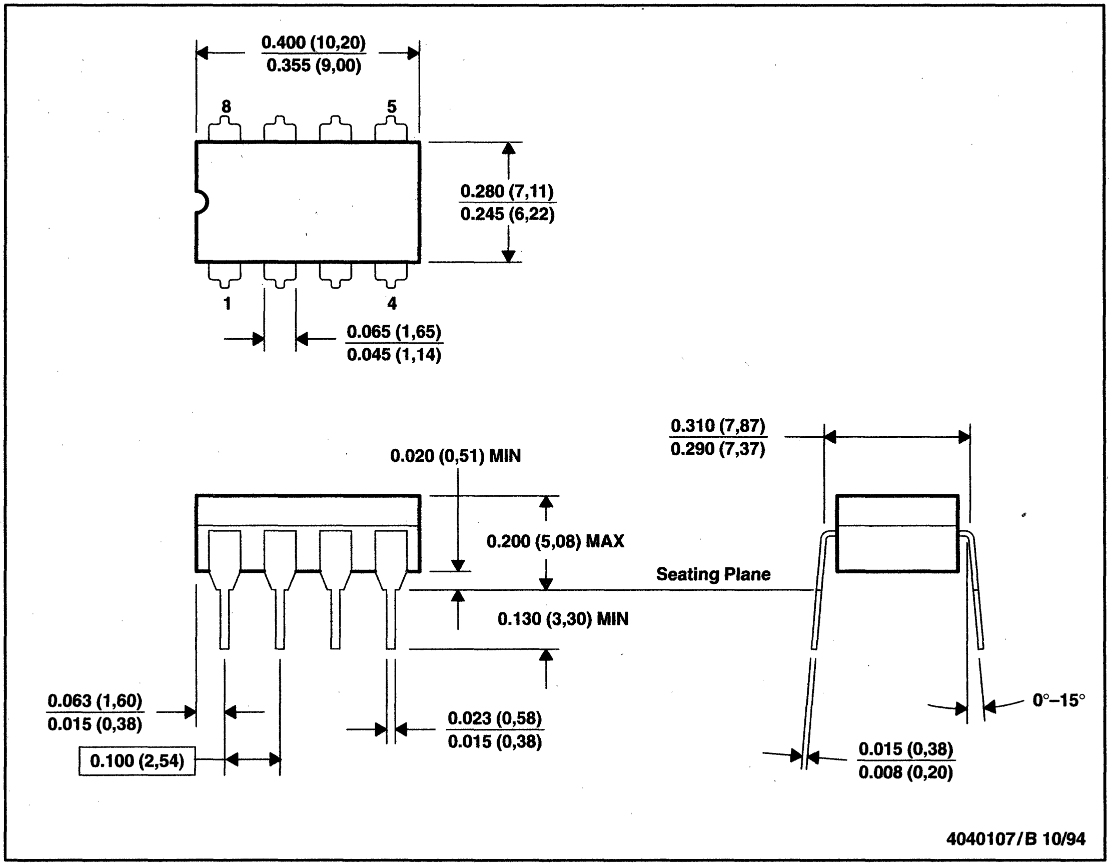
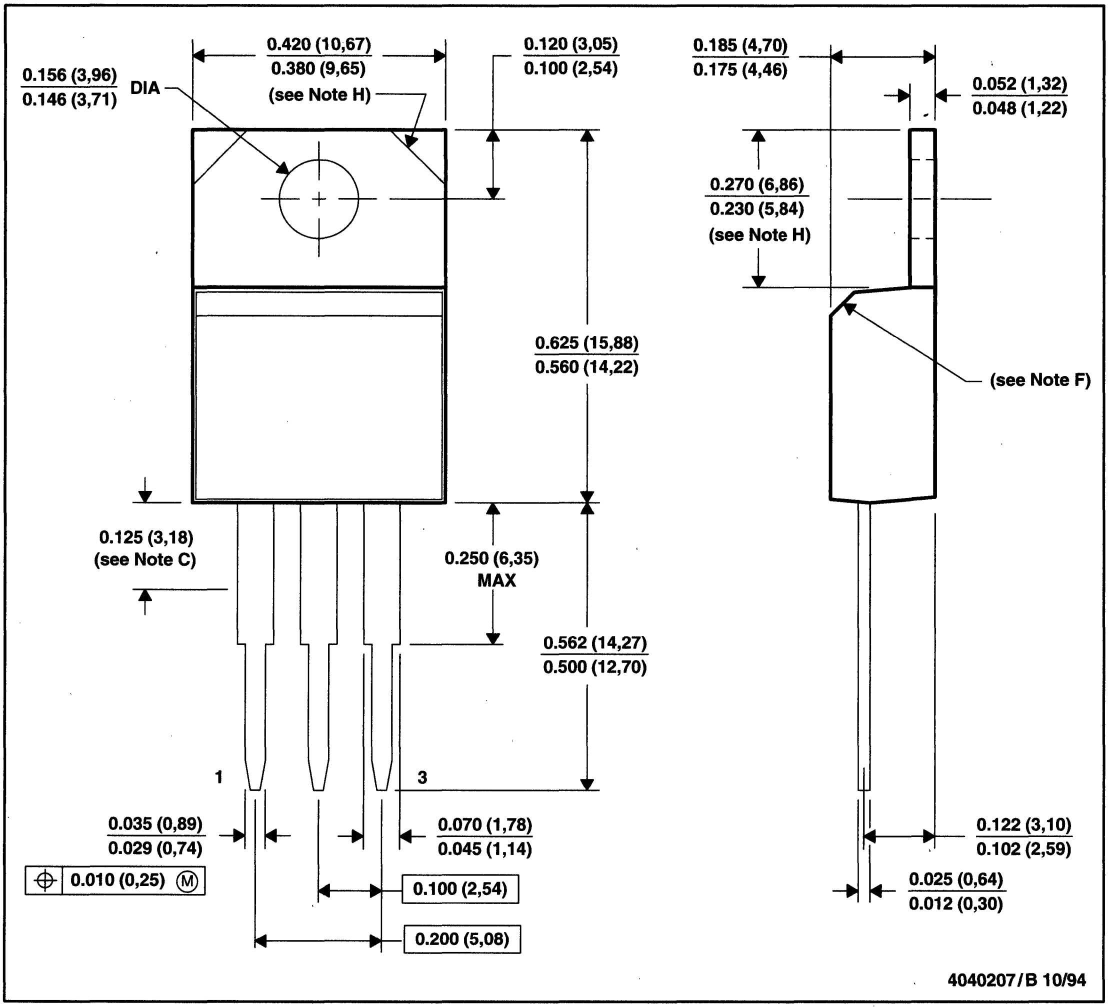
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



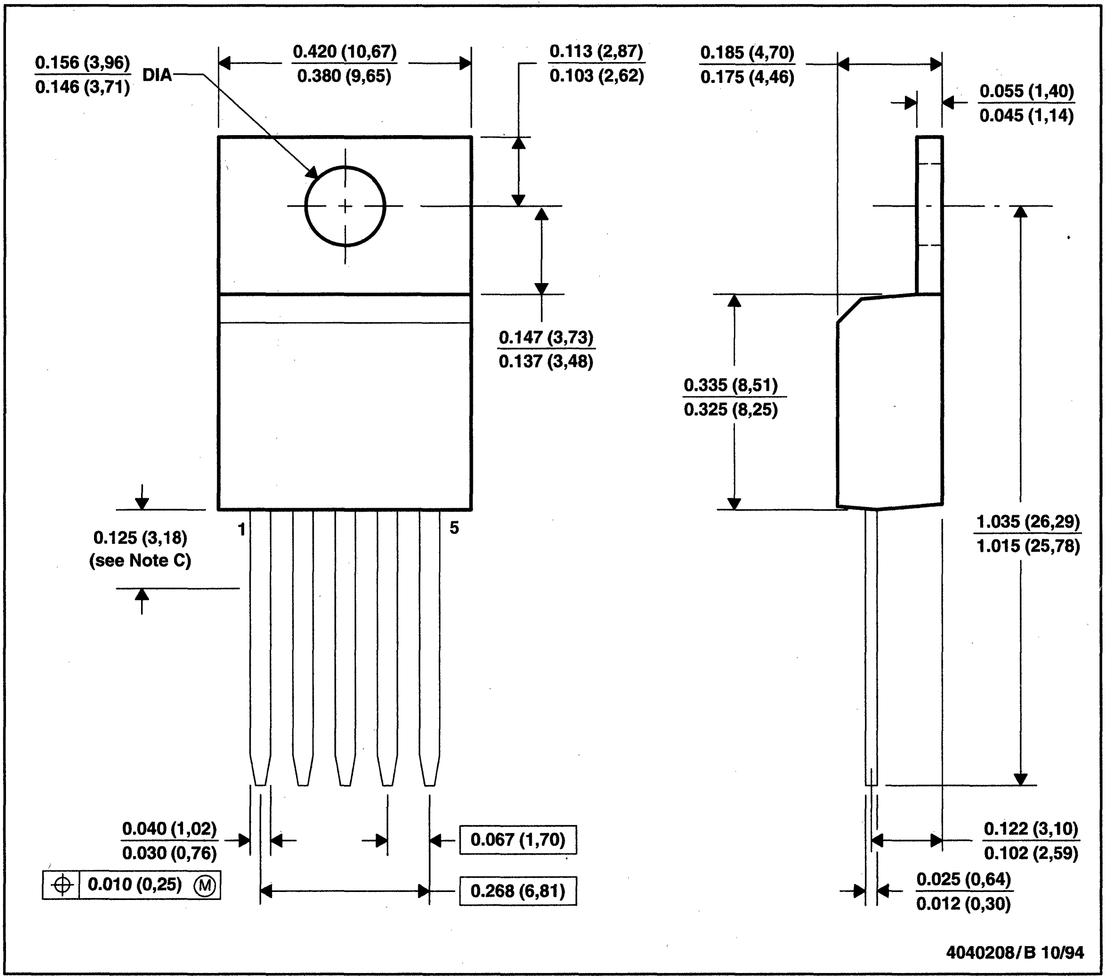
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T8

KC (R-PSFM-T3) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Falls within JEDEC TO-220AB
- H. Tab contour optional within these dimensions

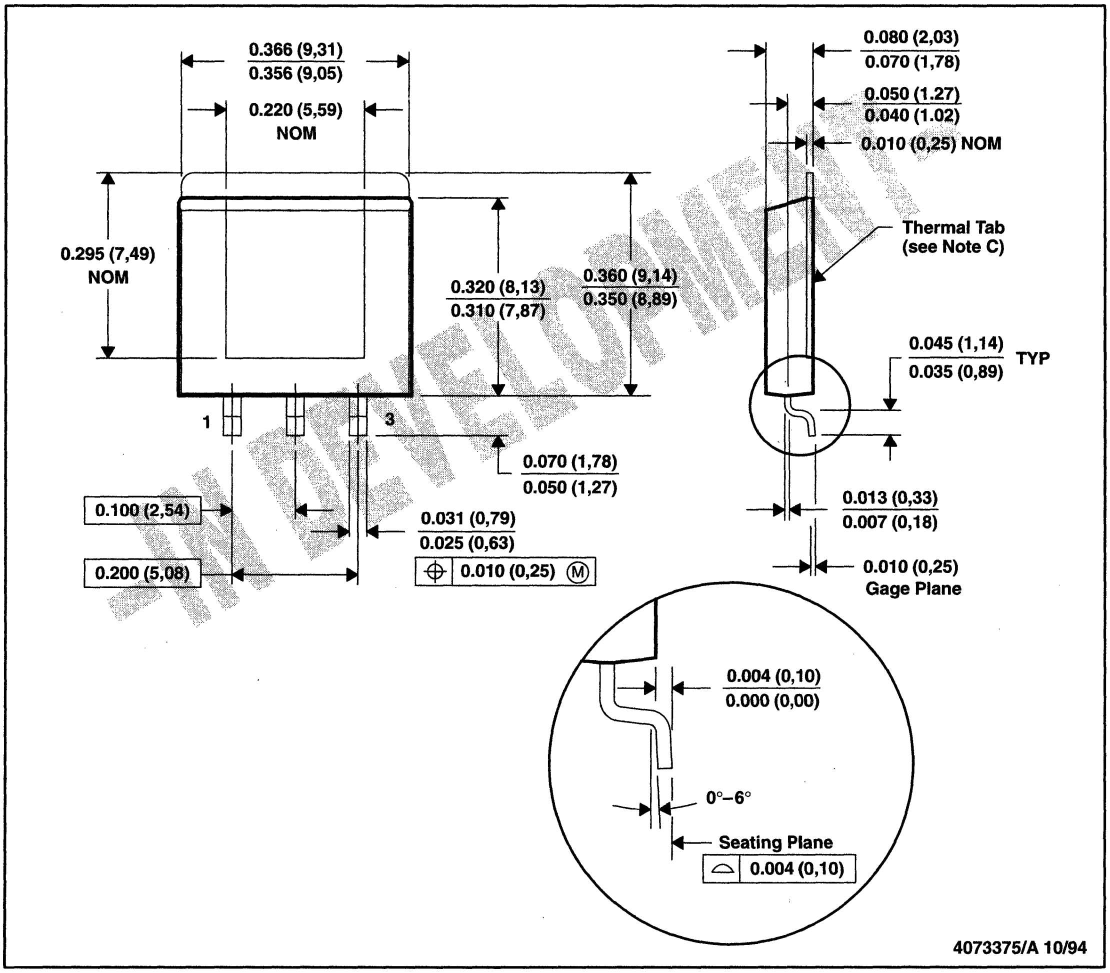
KC (R-PSFM-T5) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.

OCTOBER 1995

KTE (R-PSFM-T3) PLASTIC FLANGE-MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.

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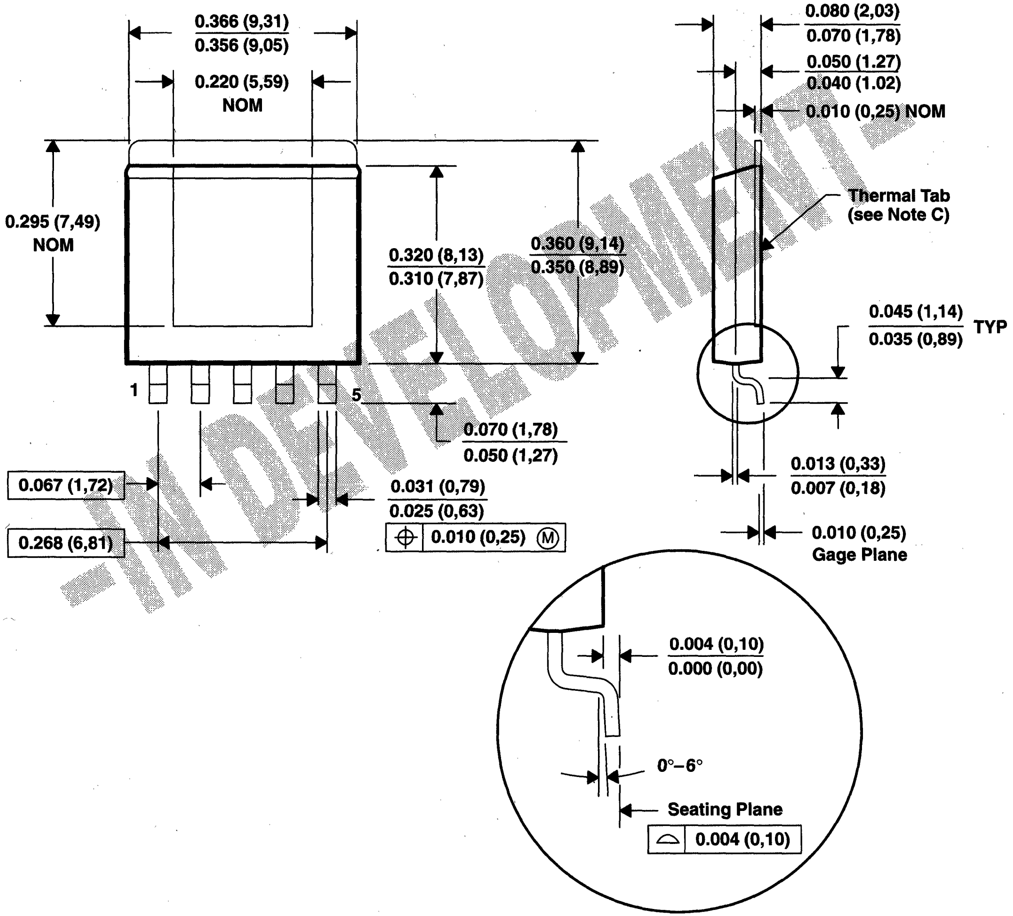
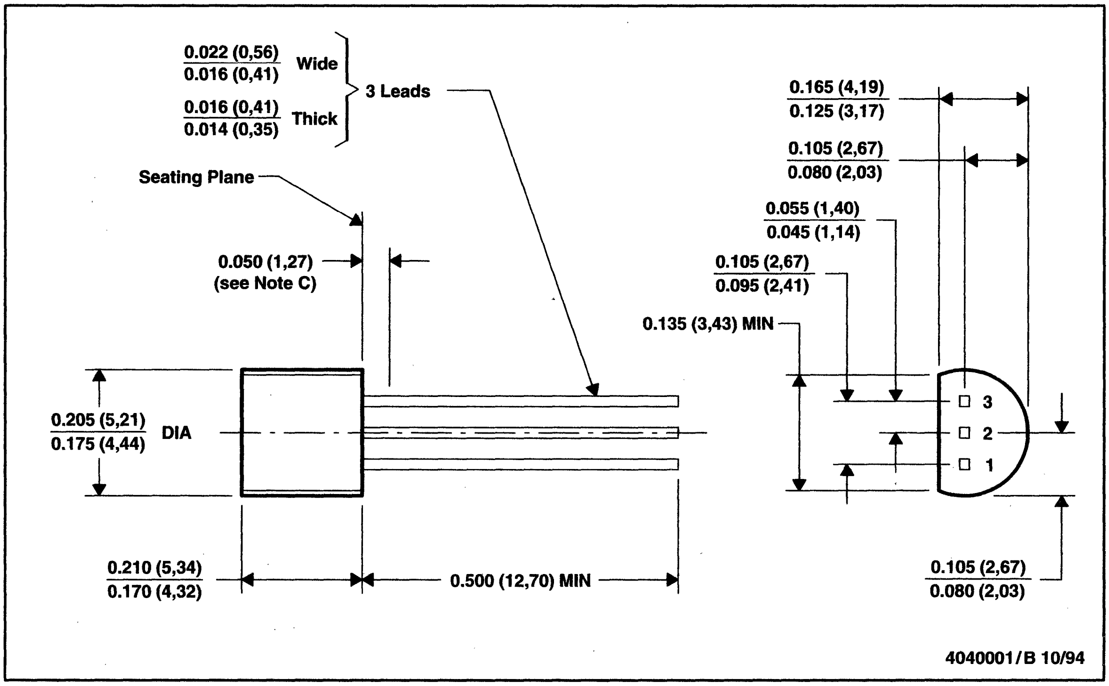
KTG (R-PSFM-G5) PLASTIC FLANGE-MOUNT PACKAGE



4073377/A 10/94

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the thermal tab.

LP (O-PBCY-W3) PLASTIC CYLINDRICAL PACKAGE



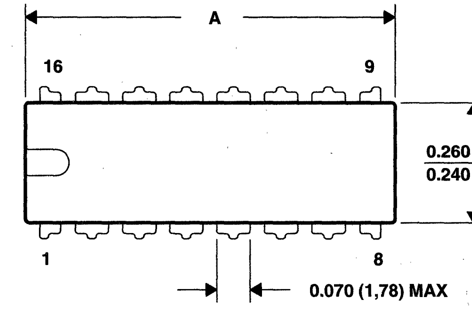
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. Falls within JEDEC TO-226AA (TO-226AA replaces TO-92)

OCTOBER 1995

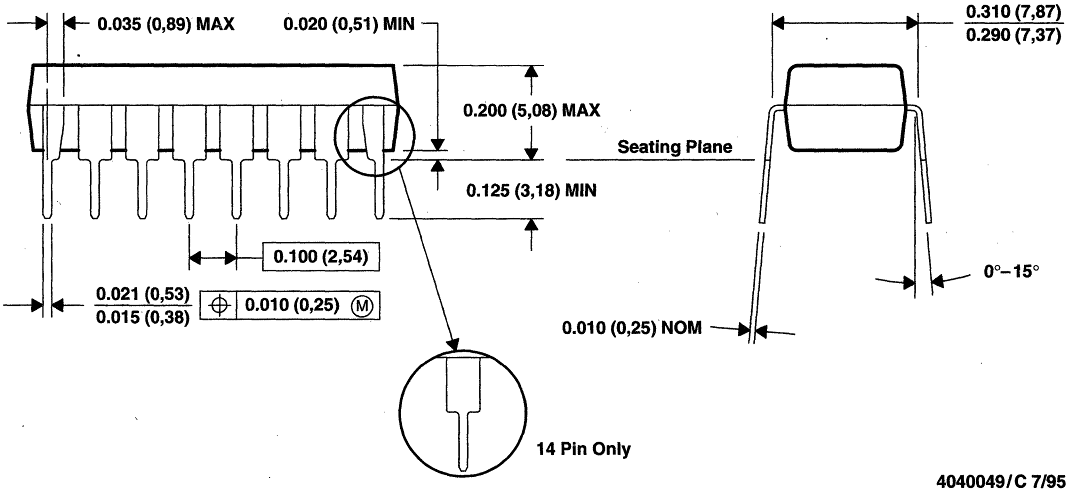
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



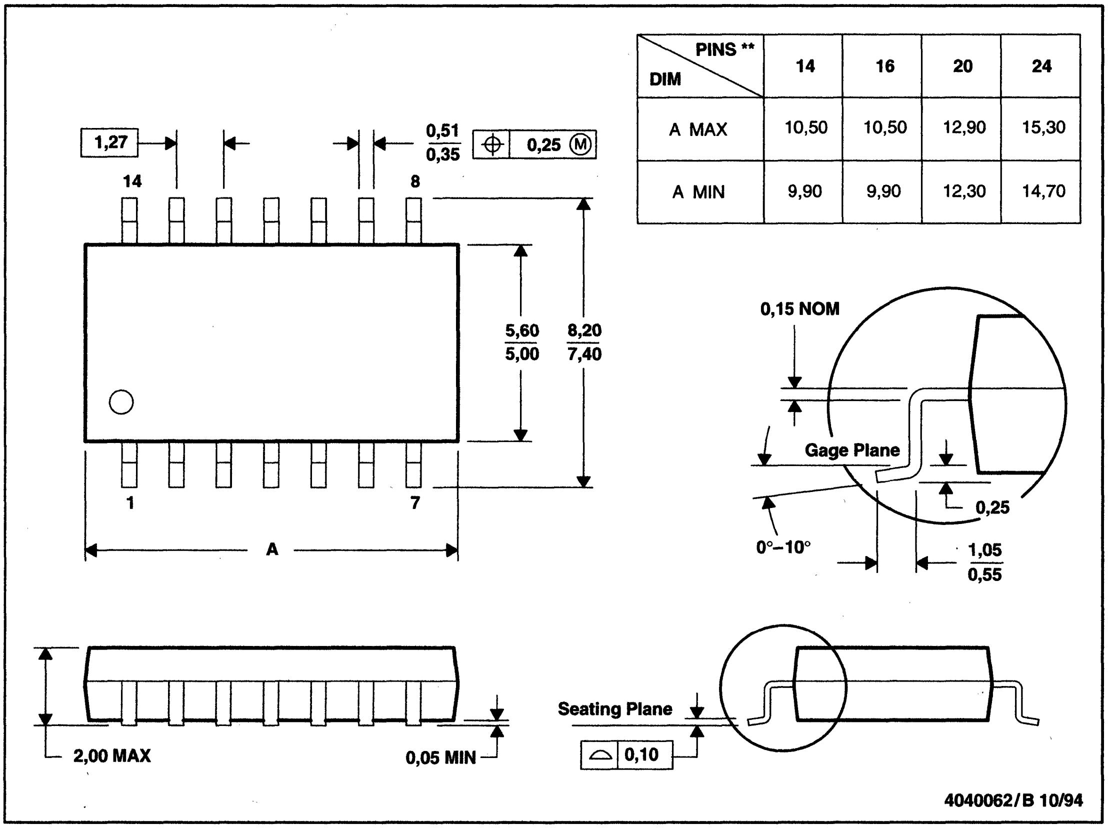
4040049/C 7/95

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

OCTOBER 1995

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

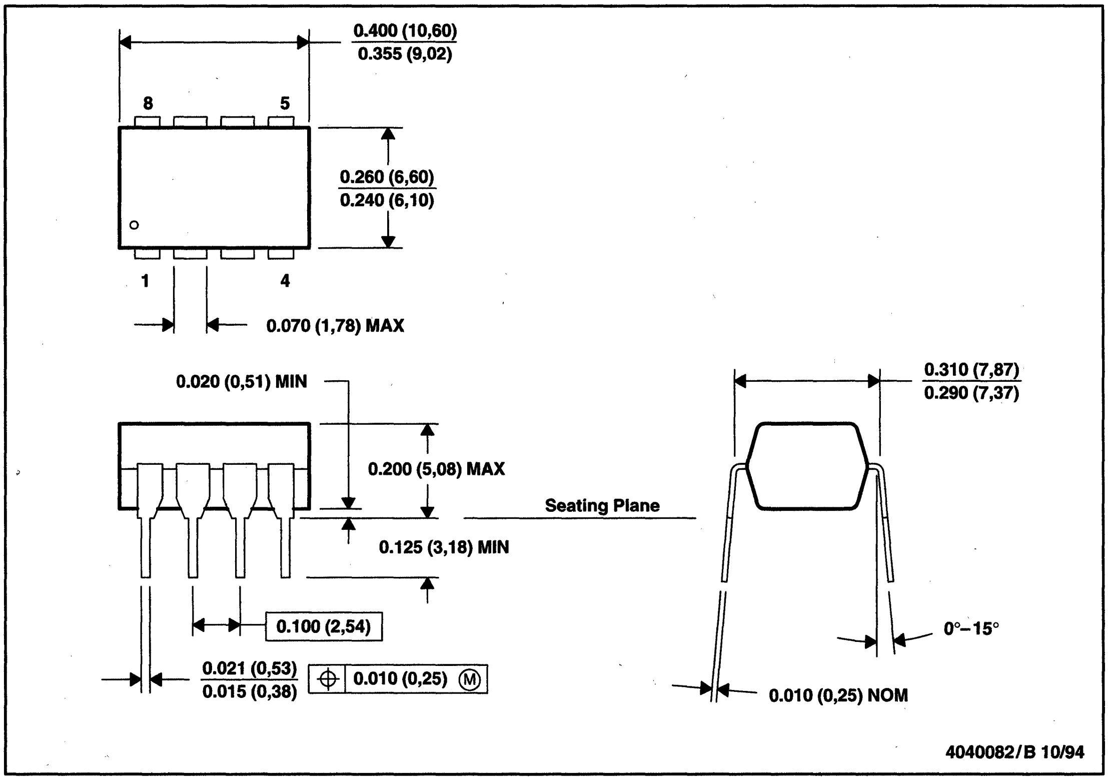
14 PIN SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

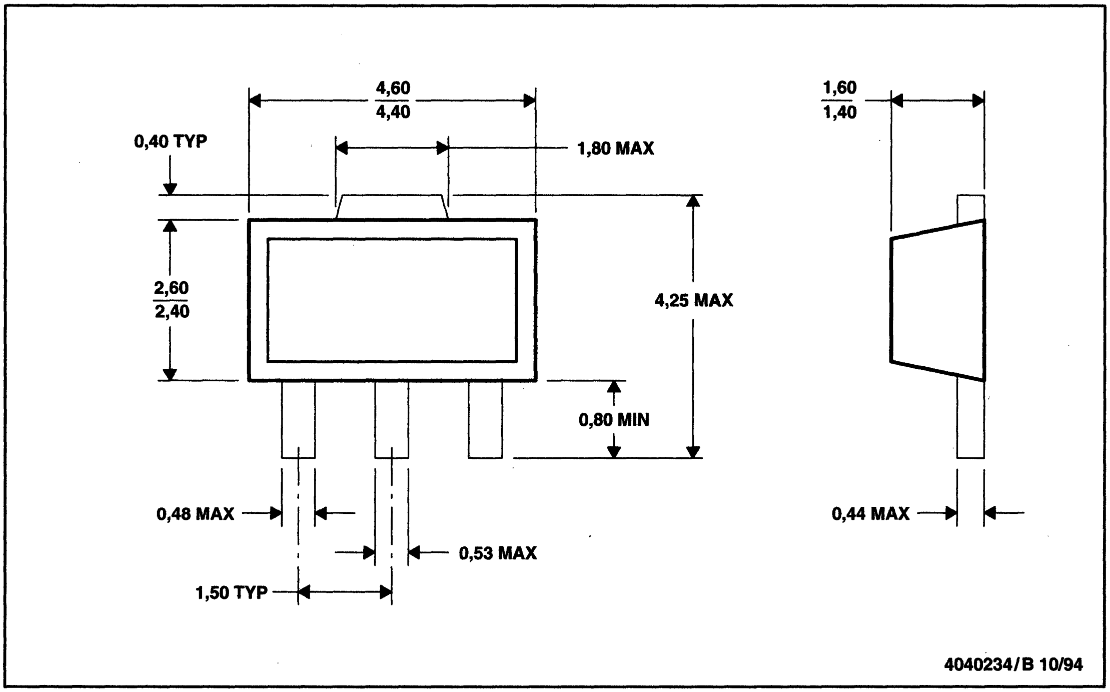
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

PK (R-PSSO-F3) PLASTIC SINGLE-IN-LINE PACKAGE



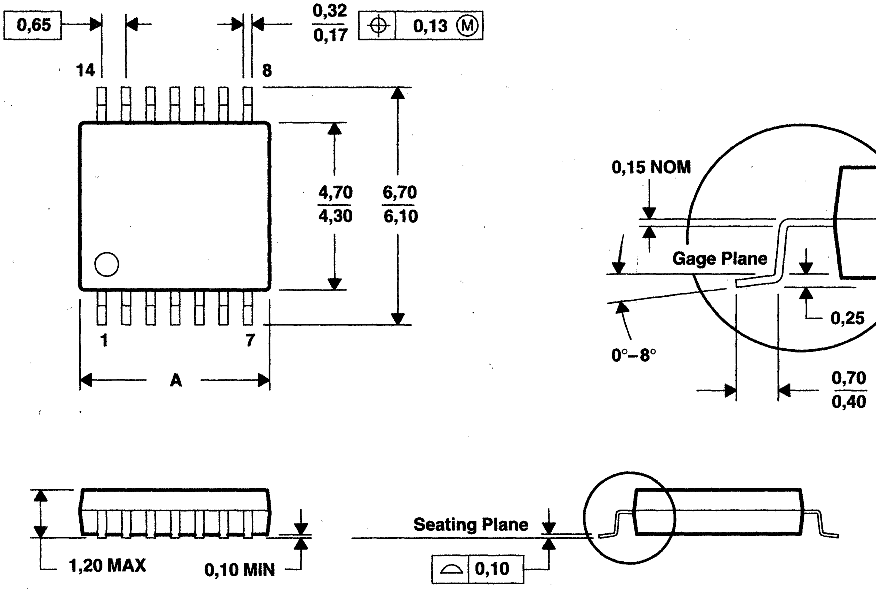
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

MECHANICAL DATA

OCTOBER 1995

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



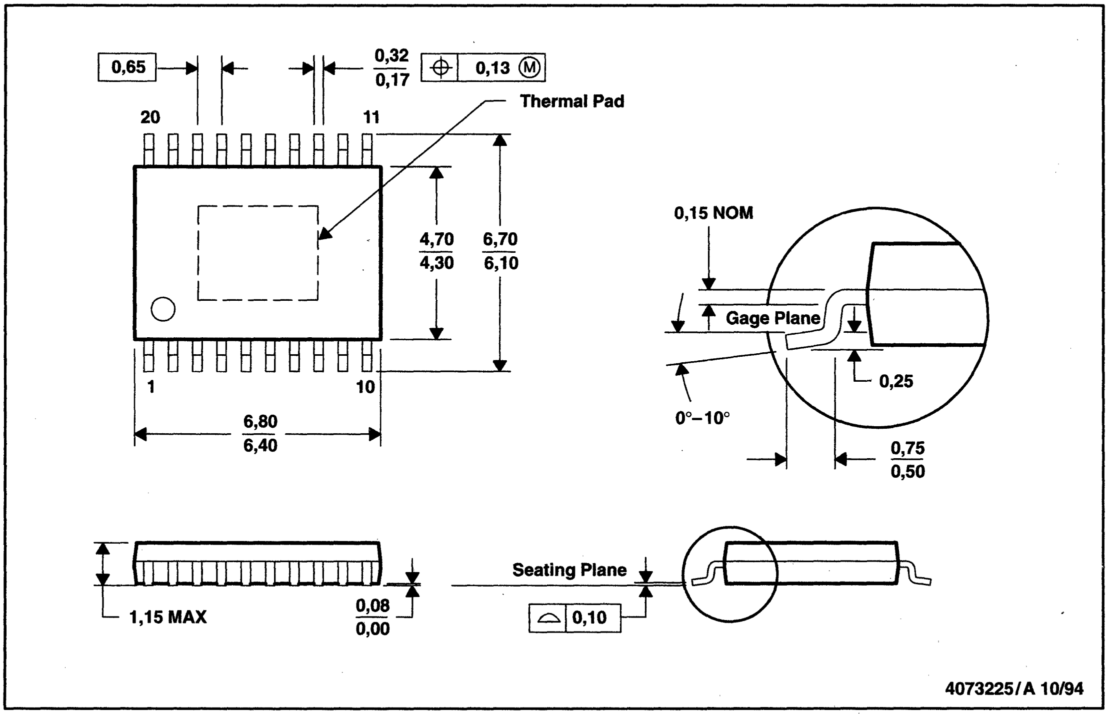
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/B 10/94

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

OCTOBER 1995

PWP (R-PDSO-G20) **PLASTIC SMALL-OUTLINE PACKAGE**

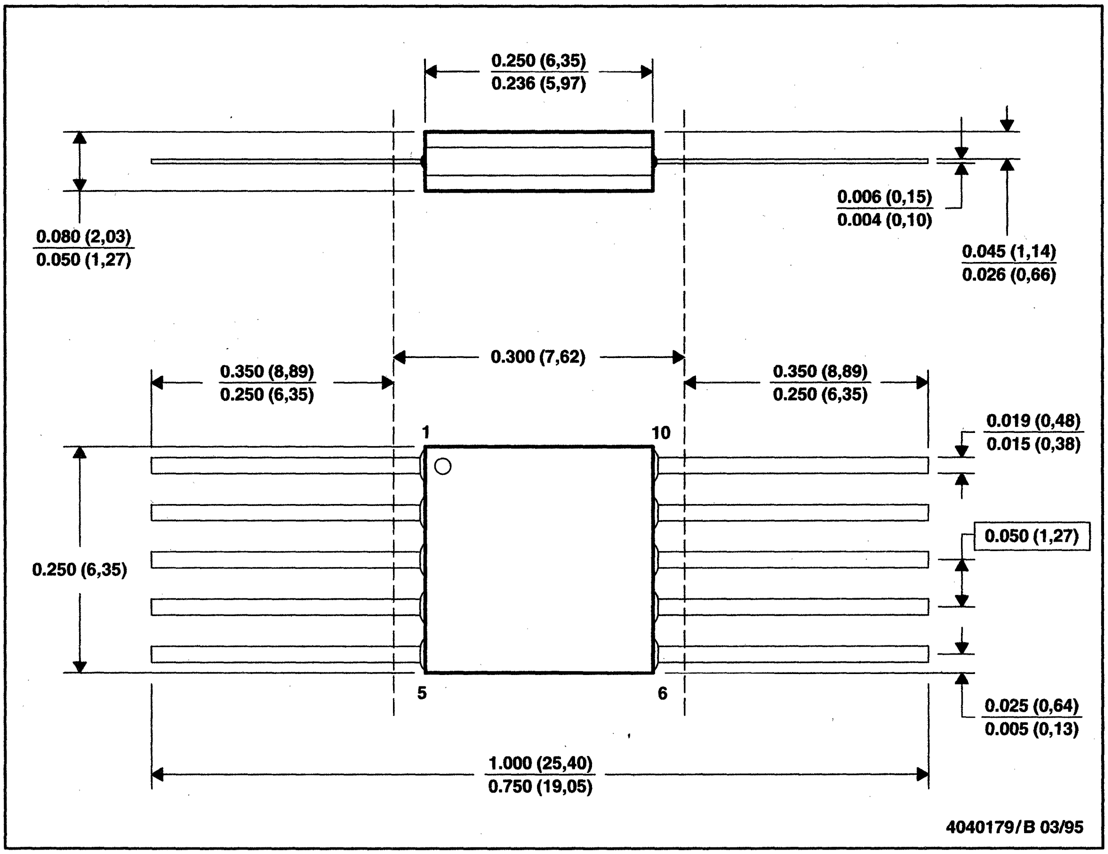


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. The solderable pad is electrically and thermally connected to the backside of the die and leads 1, 2, 9, 10, 11, 12, 19 and 20.

U (S-GDFP-F10) CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

NOTES

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