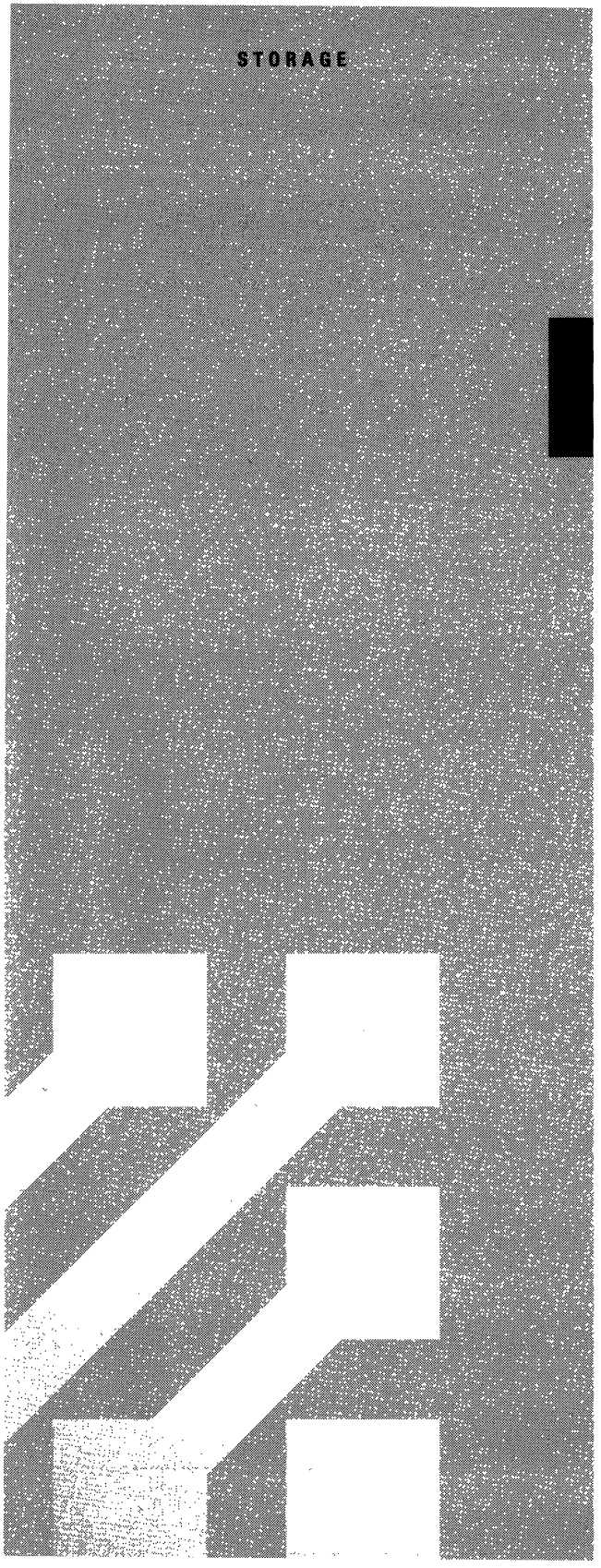
WD10C23

Self-Adjusting

Data Separator



WESTERN DIGITAL

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1.0 INTRODUCTION

The WD10C23 Read/Write Channel is an LSI device implemented in 1.25 micron high-speed CMOS. It is specifically designed to be compatible with the Western Digital WD53C22/ 42C22/ WD50C12 series of Hard Disk Controllers, and with disk drives conforming to the popular ST506/412 interface standard and recent speed-enhanced versions. In addition it will support optical applications when used with the WD60C31A ENDEC.

1.1 Features

- 5-15Mbit/sec data rates with no component changes
- Fixed/variable frequency control for zone bit recording
- Pin selectible hard/soft sector support and 2,7 RLL coding
- Precision internal self-adjusting VCO
  - —compensates for component, temperature, voltage, and aging variations
  - —one sigma phase jitter to within 250 psec at 15 Mbit/sec
- Dual gain charge pump
  - —high gain for faster frequency acquisition
  - —low gain for greater jitter rejection
  - —charge pump balance to within ± 5%
- Dual mode phase frequency detector
  - —phase frequency detection for velocity lock on XTALIN reference and on the data synchronization field , thus eliminating quadrature and harmonic locks
  - —phase only detection (phase lock) while tracking data
  - —phase window centering is precisely controlled to within ±1 nsec
- Frequency independent data detection window optimization
  - —window centering is precisely controlled to within ±1 nsec
  - —window loss controlled to within 1 nsec
  - —"built in" PMA with window shifting from 0 to 100% at ±1 nsec accuracy
  - —adaptive window centering for correction for channel antisymmetry
- Crystal controlled processing of the write data

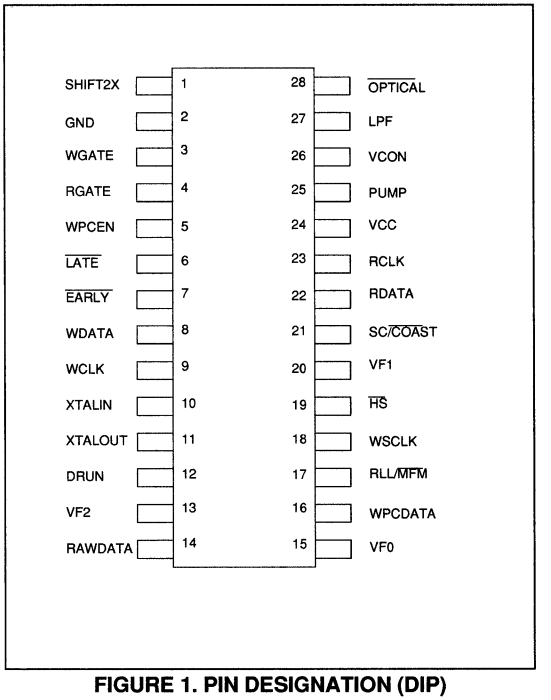

FIGURE 1. PIN DESIGNATION (DIP)

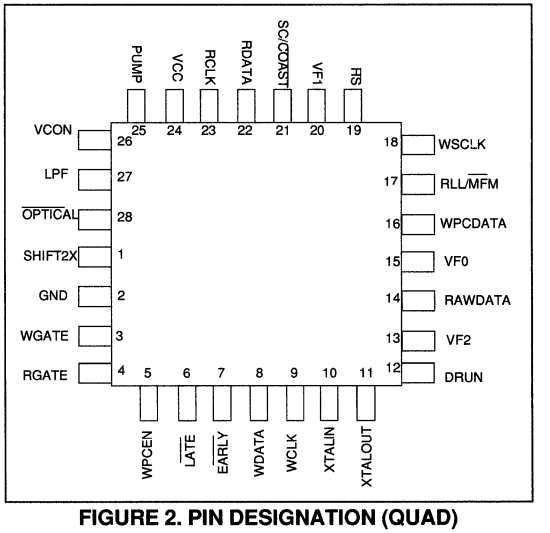

FIGURE 2. PIN DESIGNATION (QUAD)

- Dual level precompensation of ±6.25% and/or ±12.5% of the window, accurate to within ±1 nsec

2.0 DESCRIPTION

The WD10C23 uses a single 5 volt supply and has been designed for 5Mbit/sec MFM encoding, or 5 to 15 Mbit/sec data rates using RLL encoding. Variable frequency applications, or various fixed frequency applications may be accommodated through selection of the VF control bus.

One of the key features of the WD10C23 is the group of internal delay lines, that are automatically set by the XTALIN frequency. These precision elements allow for a high degree of accuracy in the handling of write precompensation, window centering, and window shifting. Further developments in this technology enable the unique implementation of Adaptive Window Shifting/Centering (AWS).

In a typical application, the WD10C23 performs all of the handling of the sensitive read/write signals between a disk controller and data drivers and receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The fundamental purpose of the WD10C23 is to remove these sources of noise, and present a clean digital signal to the controller.

2.1 Zone Bit Recording

The WD10C23 was designed for use in zone bit recording schemes. In these applications, the data rate is varied to create a fixed bit density (flux transitions/inch or FCI) from the outer radius of the media.

To maintain optimum performance as the data rate changes, loop parameters (i.e., gain, bandwidth, etc.) must be modified. This is accomplished through selection of appropriate frequency bands. The WD10C23 accommodates five different bands.

COMP:	5 Mbit/sec MFM and 7.5 Mbit/sec RLL
BAND0:	RLL, variable frequencies ranging from 5 to 7.5 Mbit/sec
BAND1:	RLL, variable frequencies ranging from 7.5 to 10.6 Mbit/sec
BAND2:	RLL, variable frequencies ranging from 10.6 to 15 Mbit/sec
BAND3:	RLL, 15 Mbit/sec

BAND0-3 may be programmed for zone bit recording, or strapped for fixed frequency applications. In these four bands, LPF must be connected to the external filter, and an external resistor placed across PUMP and VCON.

The COMP band allows for backwards compatibility with previous Western Digital data separators through component de-population.

See Table 1 for information to help you select a frequency band that is appropriate for your application.

The Table 1 columns, K_o and K_d, when unbroken, represent regions across which the gains are montonic. Across these boundaries, defined by a change in the state of the VFO/VF1 controls, the gains are re-centered to optimize for the respective frequency bands.

Recording Mode Select	VF1	VF0	RLL	Frequency Band (Data Rate MHz)	Band Name	VCO Gain Ko	Charge Pump Gain ** K_d	Open Loop Gain K_{ol}	Filter Resistors* Pump-VCON LPF†			
									INT‡	EXT	INT	EXT
Fixed Frequency	z	z	0	f=5.0	Comp	K_{om}	Kd2	K_{olm}	3kΩ	∞	∞	∞
			1	f=7.5								
Fixed or Variable Frequency Formats	0	0	1	5.0 ≤ f<7.5	Band0	K_{or} K_{o0} K_{o1}		K_{olr} K_{ol0} K_{ol1}	∞	3kΩ		
	0	1		7.5≤ f≤10.6	Band1						2.8kΩ	
	1	1		10.6< f <15.0	Band2	K_{o2}		K_{ol2}	6kΩ		525Ω	307Ω
	1	0		f=15.0	Band3	K_{o3}	Kd3	K_{ol3}	3.5kΩ		150Ω	

TABLE 1. FREQUENCY BAND SELECTION

*The following information is not intended to represent device specifications, but is indicative of typical values. See the PLL section for actual specifications.

**Charge Pump Gain, and thus, Loop Gain, is reduced by half in phase lock.

†LPF internal resistance is to GROUND, external resistance is to the filter

‡PUMP to VCON internal resistor is shorted during velocity lock

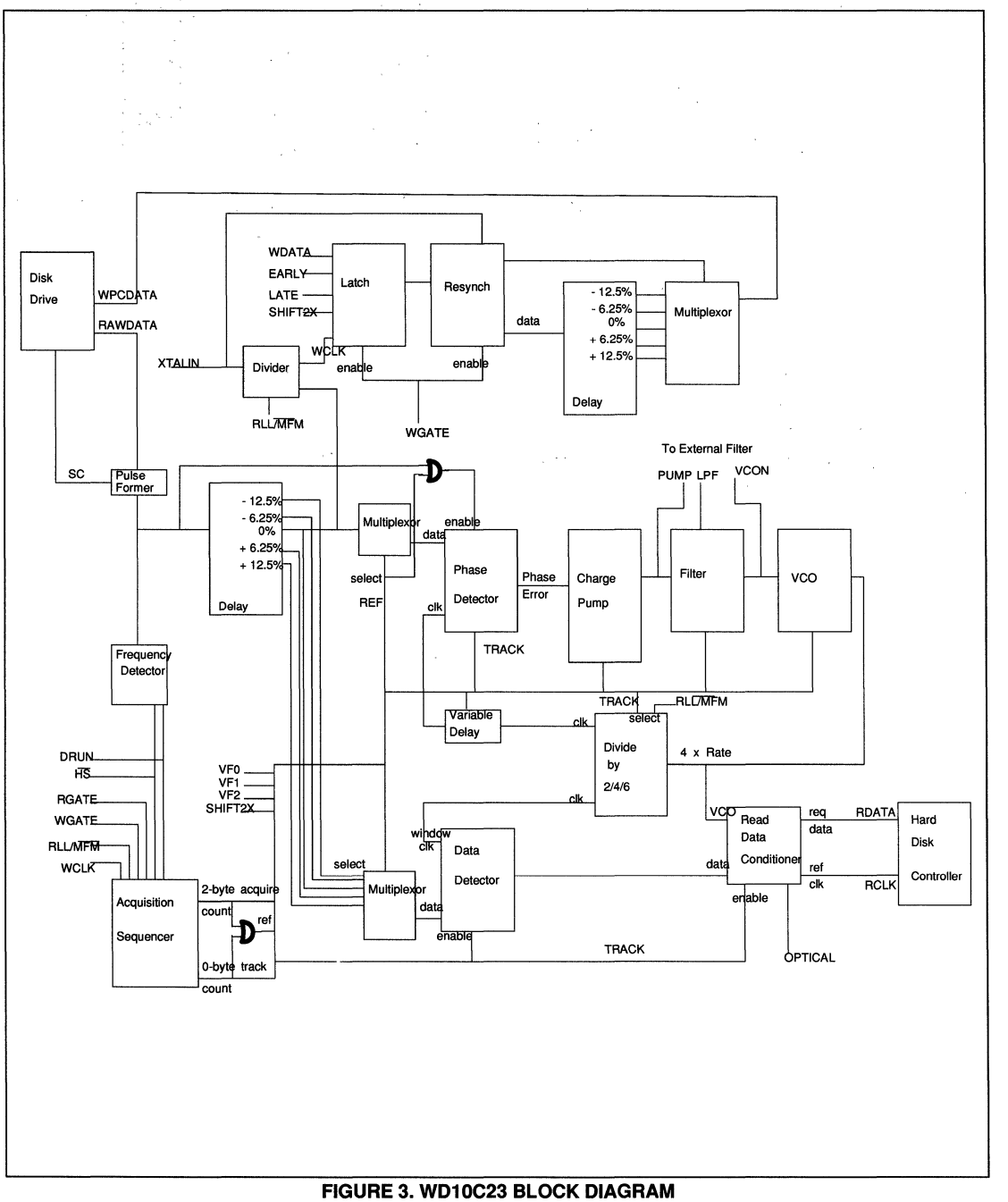

FIGURE 3. WD10C23 BLOCK DIAGRAM

2.2 Read Operations

The WD10C23 performs phase-locked loop data synchronization on read data from the drive. For soft-sector applications, an on-board synch field detector automatically switches the PLL from the stable crystal reference to the read data. Phase-frequency detection (velocity lock) is used at the beginning of the synch field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD10C23 then switches to phase-only detection to complete the phase acquisition before the end of the synch field, and to enable tracking of random read data. The phase jump at the acquisition-to-tracking switchover due to multiplexing, seen in other circuits, is avoided through the use of a zero phase jump design.

When switching to phase detection, the WD10C23 reduces the charge pump gain for better jitter rejection. A precisely centered detector samples the data at twice the underlying data rate to remove the phase jitter. A proprietary technique adjusts the window width, T, to the current data rate, providing greater phase margin. The regenerated signal, along with a fixed-phase synchronous clock, are output for the controller's digital circuits.

2.3 Write Operations

The WD10C23 performs conditioning on write data to the drive. Data from the controller is precisely synchronized with the crystal reference at twice the data frequency, thus minimizing the addition of digital phase jitter on the write data to the drive. If enabled, precompensation is achieved via delay taps available through proprietary CMOS delay line technology. The delay line is servo-controlled to the crystal reference for precision. Synchronized, precompensated write data is thus sent directly to the drive's write circuits.

Precompensation levels are programmable to be either 12.5 or 6.25 percent of the window, defined by the inverse of the crystal frequency. The SHIFT2X input allows dynamic control of early and late precompensation magnitude for more complex precompensation schemes. In addition, SHIFT2X may be programmed using track information for zone bit precompensation schemes.

3.0 EXTERNAL COMPONENTS PARTS LIST

The parts list shown below gives typical component values for 5 Mbit/sec MFM and 5-15 Mbit/sec RLL data rates.

See the diagram on the opposite page for the location of each component.

Contact your local Western Digital sales representative for more information on how to change these values, to accommodate different data rates.

10C23 EXTERNAL COMPONENTS for 5 Mbits/sec (MFM) and 5-15 Mbits/sec (RLL)

PART #	TYPE	VALUE	SPECIFICATIONS
C111	capacitor	4700 pF	cer. , 5%, 50V, COG
C112	capacitor	150 pF	cer. , 5%, 50V, COG
C101	capacitor	47 µF	tan. , 20%,10V
C106	capacitor	0.1 µF	+80-20%, 50V, z5u
L101	----------	3.3 ohm	5%, 1/4 w
R107	resistor	590 ohm	1%, 1/4 w, 100 ppm
R301	resistor	301 ohm	1%, 1/4 w, 100 ppm
R302	resistor	3.01K ohm	1%, 1/4 w, 100 ppm
Y101	crystal	10-15 MHz	.01%, 3 leads
C104	capacitor	68 pF	cer. , 5%, 50V, COG
C105	capacitor	47 pF	cer. , 5%, 50V, COG
Y101	crystal	15-20 MHz	.01%, 3 leads
C104	capacitor	33 pF	cer. , 5%, 50V, COG
C105	capacitor	22 pF	cer. , 5%, 50V, COG
Y101	crystal	20-30 MHz	.01%, 3 leads
C104	capacitor	22 pF	cer. , 5%, 50V, COG
C105	capacitor	10 pF	cer. , 5%, 50V, COG

R302 resistor is left open for compatibility mode.
R301 & R302 resistors are left open for BAND0.

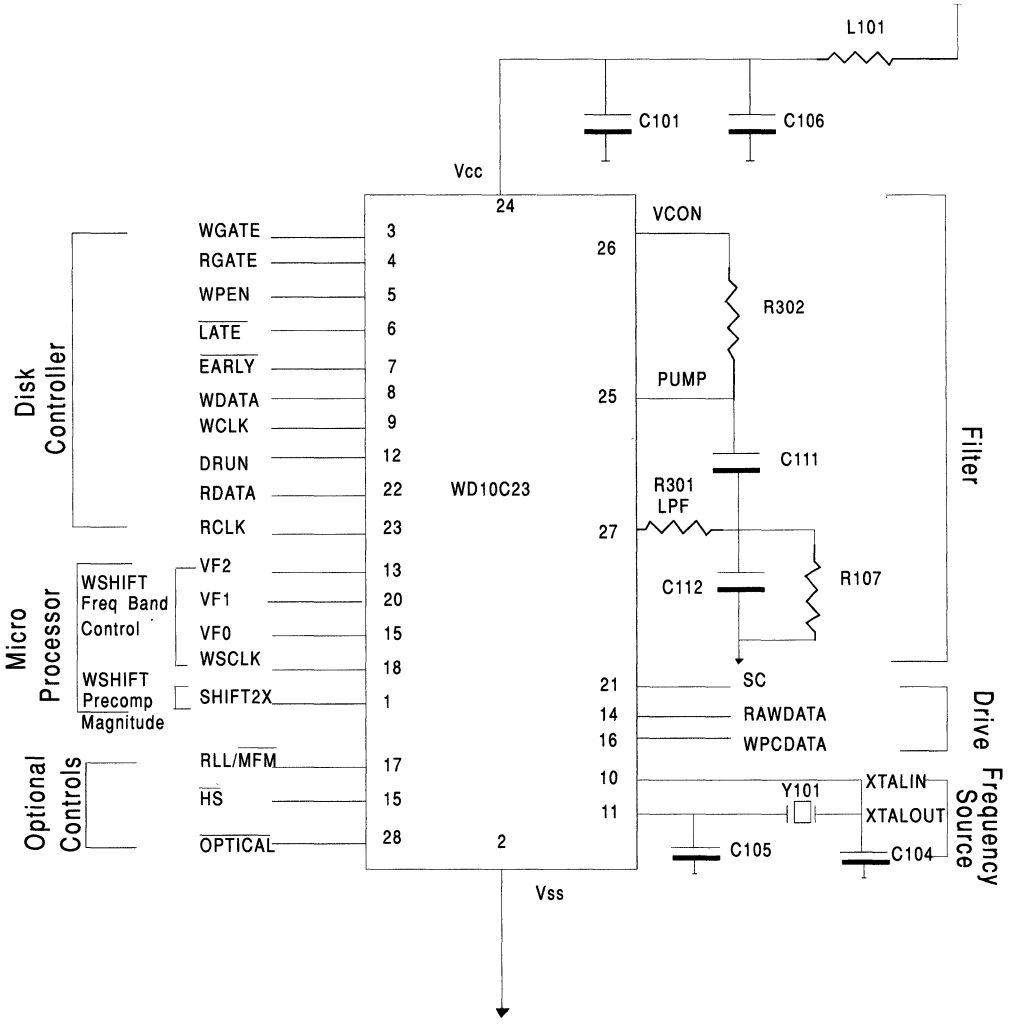

FIGURE 4. EXTERNAL COMPONENTS

4.0 PIN DESCRIPTIONS

Signals have the same pin numbers for both packages.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	SHIFT2X	SHIFT2X	I	Shift two times. When false, selects ±6.25% of the window for write precompensation and window shifting. When true, selects two times that amount or ±12.5 of the window. Internal pullup.
2	GND	GROUND	I	GROUND.
3	WGATE	WRITE GATE	I	Write gate. Set high when recording onto the disk. Write gate takes precedence over read gate.
4	RGATE	READ GATE	I	Read gate. Set high when the Controller intends to read.
5	WPCEN	WRITE PRECOMP ENABLE	I	Write precompensation enable. When high, it enables EARLY, LATE, and SHIFT2X for precompensation.
6	$\overline{\text{LATE}}$	LATE	I	Negative true inputs used to delay write data for write precompensation.
7	$\overline{\text{EARLY}}$	EARLY	I	Negative true inputs used to advance write data for write precompensation. Internal pullup.
8	WDATA	WRITE DATA	I	Write data to be conditioned and sent out through WPCDATA to be written onto the disk.
9	WCLK	WRITE CLOCK	O	Clock signal at one half the XTALIN frequency.
10	XTALIN	XTALIN	I	Input pins for a crystal oscillator circuit. If an external frequency source is desired, XTALIN can be driven and XTALOUT left open.
11	XTALOUT	XTALOUT	O	Output pins for a crystal oscillator circuit.
12	DRUN	DATA RUN	O	The output of a frequency detector connected to RAWDATA. Short, high frequency periods cause it to go high; long, low frequency periods cause it to go low. Used for detecting high frequency synch fields. Not used in hard sector.
13	VF2	VARIABLE FREQUENCY CONTROL	I	Tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes. VF2 is compatible with the WSHIFT pin on the 10C20A/21A/20B/22B when VF0 and VF1 are open.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
14	RAWDATA	RAW DATA	I	Data received from the drive read circuits. Includes an internal pullup resistor to allow tri-state multiplexing of the drives' data receivers.
15	VF0	VARIABLE FREQUENCY	I	Variable frequency tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes.
16	WPCDATA	WRITE PRECOMP DATA	O	Write precompensation data sent to the drive write circuits. Low when WGATE is low.
17	RLL/$\overline{\text{MFM}}$	RLL/$\overline{\text{MFM}}$ SELECT	I	When high, selects RLL (2,7) mode. When low, selects MFM (1,3) mode. Internal pullup.
18	WSCLK	WINDOW SHIFT CLOCK	I	Window shift clock reference. Internal pullup.
19	$\overline{\text{HS}}$	HARD SECTOR	I	When true, disables DRUN qualification on reads. RGATE controls the acquisition sequence to and from data. Internal pullup.
20	VF1	VARIABLE FREQUENCY	I	Variable frequency tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes.
21	SC/$\overline{\text{COAST}}$	SEEK COMPLETE	I	When low, disables RAWDATA and keeps VCO on reference. May be used to coast through defects when tracking. Internal pullup.
22	RDATA	READ DATA	O	Detected and regenerated version of RAWDATA. Jitter has been removed and pulses have been synchronized with RCLK.
23	RCLK	READ CLOCK	O	VCO divided to the data rate. Tracks the base frequency of RAWDATA during a read operation; otherwise tracks the crystal frequency.
24	V_{CC}	POWER SUPPLY	I	+5 Volts. Power supply input.
25	PUMP	PUMP	I/O	Charge pump output to the external filter.
26	VCON	VCO INPUT	I	Input to the external filter.
27	LPF	FILTER OUTPUT	O	Output of the external filter.
28	$\overline{\text{OPTICAL}}$	OPTICAL	I/O	Optical mode select. Used to enable test modes. Internal pullup.

5.0 ARCHITECTURE

The twelve major functions within the WD10C23 are listed below:

- Synchronization Field Detector
- Acquisition Sequencer
- Phase-Locked Loop (PLL)
  - —Phase-Frequency Detector
  - —Charge Pumps
  - —Filter
  - —Voltage Controller Oscillator (VCO)
- Read Data Conditioner
- Read Data Detector
- Phase Margining
- Crystal Oscillator
- Write Data Conditioner
- Delay-Locked Loop (DLL)
- Pulse Former
- Power-on Reset
- Test Modes

5.1 Synchronization Field Detector

The purpose of this circuit is to reliability discriminate between the high frequency of a PLL synchronization field and the lower frequencies immediately preceding it. The criterion used is pulse period discrimination on RAWDATA. If the period between consecutive rising edges of RAWDATA is short with respect to the threshold, then DRUN will go high; if long, then DRUN will go low.The pulses in the synchronization field must have the shortest period in the format (i.e. 3T for 2, 7 RLL; 2T for 1, 3 MFM). The pulses in the field preceding the synchronization field must have a period sufficient to drop DRUN.

In MFM mode, the optimum discrimination threshold is set using an internal delay line. In RLL mode, the threshold is set digitally.

When a synchronization field is detected, DRUN will remain high until address mark detection. At this time, the Synchronization Field Detector is put to sleep. Upon de-assertion of RGATE, the Detector will be awakened.

Although the Synchronization Field Detector is not used in hard sector mode (by either the controller or the internal Acquisition Sequencer), DRUN will still respond to pulse period information on RAWDATA.

5.2 Acquisition Sequencer

The Acquisition Sequencer sends sequencing control signals to the appropriate circuits when the WD10C23 switches between the read, write, and idle modes.

5.2.1 Idle-to-Read Sequencing

The soft sector read sequence begins when the Synchronization Field Detector raises DRUN in response to high frequency data on the RAWDATA input. If DRUN remains high for two NRZ byte times, the Sequencer switches the Phase - Frequency Detector from the crystal reference to the incoming data. The Phase-Frequency Detector is in phase-frequency (velocity lock) mode with the PLL set at high gain.

At the end of six bytes of velocity lock to data, RGATE is polled. If the controller has been issued a read command, RGATE will be true, and the Sequencer will switch the Phase-Frequency Detector to phase lock mode phase lock. The charge pump are set for low gain for improved jitter rejection.

At this time, the Acquisition Sequencer is put to sleep and disables the Synchronization Field Detector. Upon the dropping of RGATE, the Sequencer awakens the Synchronization Field Detector, sets the Phase Detector back to velocity lock, and sets the charge pumps back to high gain.

For hard sector formats, the acquisition sequence is slightly altered. RGATE alone initiates the acquisition sequence data, without qualification of the Synchronization Field Detector. At the end of eight bytes in velocity lock, the sequence is as described above.

5.2.2 Idle-to-Write Sequencing

The write sequencer is initiated by the assertion of WGATE. WGATE disables the Aquisistion Sequencer, which in turn puts the Synchronization Field Detector to sleep. The Phase Detector is forced to remain on the crystal reference for the duration of the write.

5.3 Phase-Locked Loop (PLL)

5.3.1 Phase-Frequency Detector

The Phase-Frequency Detector can be operated in two modes. The velocity lock mode is used for acquisition when the PLL is switched to read data, and is always used when the PLL is following the reference crystal oscillator. Whenever the device is not reading, the PLL is locked to XTALIN.

The second mode, phase lock, is standard phase-only detection. The Acquisition Sequencer switches to this mode when frequency acquisition is essentially complete on data, and phase acquisition is nearly complete as well. Phase-only mode must, of course, be used to lock to the data following the synch field, since that will contain the three frequencies inherent in MFM or the six frequencies inherent in RLL mode.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal will be routed to the pump up or pump down circuitry in the Charge Pump section.

5.3.2 Charge Pumps

This circuit converts the pulse widths received from the Phase-Frequency Detector to proportional amounts of charge into or out of the Filter. The symmetry of the Charge Pumps is continuously determined by the voltage on the VCON. A proprietary technique selects a pump up current which precisely matches that of the pump down at the given filter voltage.

When in phase lock, the gain is reduced by two.

5.3.3 Filter

The Filter converts the current pulses from the Charge Pumps to a voltage output to the VCO.

The Filter has been carefully designed to the specific requirements of damping factor, acquisition time, capture range, and jitter rejection; and within the context of its effect on VCO operation. Roughly speaking, it functions to filter out high frequency signals due to RAWDATA read data jitter, while passing the low frequency signals associated with the more slowly varying underlying frequency of RAWDATA, and handling a step change in input frequency when switching between drive data and reference.

The Filter is internal, with the exception of external components. In variable frequency applications, two additional external resistors are required.

5.3.4 Voltage Controlled Oscillator(VCO)

The VCO consists of an internal charge pump and ring oscillator. Thus, the VCO requires no expensive components, and has no tuning requirements for voltage, temperature, or aging.

The VCO converts the voltage developed by the Filter to a control voltage for the ring oscillator. The non-linear I-V characteristic inherent in most internal VCO designs, is eliminated by a proprietary technique, and loop gain is linearized over a wide frequency band.

The VCO runs at four times the channel rate and is divided down for extremely high precision duty cycles.

5.4 Read Data Conditioner

This circuit synchronizes the output of the Read Data Detector and produces the signals RCLK and RDATA. RCLK is a square wave at either one or two times the data rate selected via the OPTICAL input (see Table 3). During data tracking, the frequency of RCLK mirrors the slowly varying frequency of the raw data from the drive, RAWDATA. RDATA is a regenerated form of RAWDATA, with all jitter removed and positive pulses one window wide. It is synchronous with RCLK. RCLK edges occur nominally in the center of RDATA pulses to allow sufficient setup and hold time for the digital circuits in the controllers that use these signals. For the 2XRCLK, RDATA and RCLK edges are coincident. RDATA is DC low during velocity lock, and is activated by the Acquisition Sequencer approximately at the transition to phase lock.

RCLK will stop for several windows at the transition to phase lock for internal synchronization of the Read Data Detector and Read Data Conditioner.

5.5 Read Data Detector

The Read Data Detector latches the incoming drive data and presents it to the synchronization circuits of the Read Data Conditioner. Window shifting is performed here using one of several techniques described below.

To maximize phase margin, the window at the Read Data Detector is precisely centered and tracks the frequency of the incoming data.

5.6 Phase Margining

Phase margining is performed at the Read Data Detector by shifting the incoming raw read data either early or late with respect to the Read Data Detector's sampling clock or strobe. Window shifting is accomplished in one of two fashions described below, and is summarized in Table 2.

5.6.1 Window Shifting as Percentage of the Window

The first technique is compatible with previous Western Digital data separator designs. Window shifting is achieved by advancing or delaying the raw read data to the Read Data Detector through precision internal delay stages. Shifting is programmable to either ±6.25% or ±12.5% of the window, and is inversely proportional to the crystal frequency.

Window shifting as a percentage of the window applies for fixed frequency as well as variable frequency applications.

5.6.2 Adaptive Window Shifting/Centering (AWS)

This technique uses an external reference clock, WSCLK, to set the timing relationship of the raw read data to the Data Detector strobe. By allowing for a continuous, precision, user controlled strobe placement, the effective detection window may be advanced or delayed as desired. This feature, when used in conjunction with micro-processor interaction at the VF0-2 inputs (see Table 2) may be used to:

- Create an adaptive window centering scheme to offset any asymmetry induced by the read channel electronics
- Provide system self-test in the form of built-in PMA capabilities
- Execute error recovery algorithms

Using AWS, the absolute range of window placement is dictated by the VF0-2 control pins. Once the range, N, has been selected, window placement within that range is proportional to the period of the reference (WSCLK) with a gain of approximately 1/2 to 1/6. Thus, for every 1ns of change on the external source, window shift resolution ranges from 166 ps to 500 ps.

The value of N is the closest value which represents one quarter of the window, T/4, for any given data rate. For each of the twelve ranges, there exists some frequency on WSCLK for which the range is optimum. That is, the window position may be programmed symmetrically about this frequency up to plus or minus one-half window. When this center frequency is equal to the data rate, it is known as the Optimum Center Frequency, denoted f(N). Since "range" is now equal to "window", strobing may be programmed about f(N) up to ±window/2, denoted T/2.

As the data rate varies from f(N), the range set by N may be insuffient to achieve window placement across the full window. However, placement across the full window may be obtained by using a different value of N for early shifting than that for late shifting. Here are some examples.

Example 1:

If the actual data rate is 10.4Mbit/sec, selecting N=12 gives a 10.4Mbit/sec center frequency, $f(12)$. We have selected an Optimum Center Frequency. The window at 10.4Mbit/sec is 48ns. Varying WSCLK from 4.44Mhz to 12.32Mhz will allow window shifting over a range of 24ns to 72ns, or 48ns $\pm$T/2 (Figure 5).

For the partial range of 24ns to just under 48ns, the data is shifted from window center to the late edge of the window, respectively. This is equivalent to window shifting from 0ns to 24ns, or 0ns to +T/2.

For the partial range of just over 48ns to 72ns, the data is shifted into the next window, from that window's early edge to its center, respectively. This is equivelant to window shifting from -24ns to 0ns, or -T/2 ns to 0ns.

In the example, window shifting of $\pm$T/2 was achieved.

If however the actual data rate was 10Mbit/sec, a single value of N would be insufficient (we would not be at an Optimum Center Frequency).

Example 2:

For an actual data rate of 10Mbit/sec the window is 50ns. Again selecting N=12, the range of shifting achieved by varying WSCLK from 4.44Mhz to 12.32Mhz will be 24ns to 72ns, as in the example above (Figure 6).

For the partial range of 25ns to just under 50ns, the data is shifted from window center to the late edge of the window respectively. This is equivelent to window shifting from 0ns to 25ns respectively, or 0ns to +T/2.

For the partial range of just over 50ns to 72ns, the data is shifted into the next window, from that window's early edge to 3ns from its center respectively. This is equivelant to window shifting from -25ns to -3ns respectively, or -window/2 ns to -3ns.

Thus the range provided by N=12 is not sufficient to allow early window shifting over the full half window. If N were selected to be 13, the range would change from 24-72ns, to 26-78ns. Using the same analysis as above, this would allow early window shifting from -24ns to 0ns, and late window shifting of 0ns to 25ns, or 0ns to +T/2.

Thus by using one value of N for the early window shifting, and another value for late, the full range of $\pm$window/2 may be achieved.

Selection of N may be made by looking for the Optimum Center Frequency $f(N)$ which is closest the data rate in Table 2. N may also be determined using the relationships listed after Table 2.

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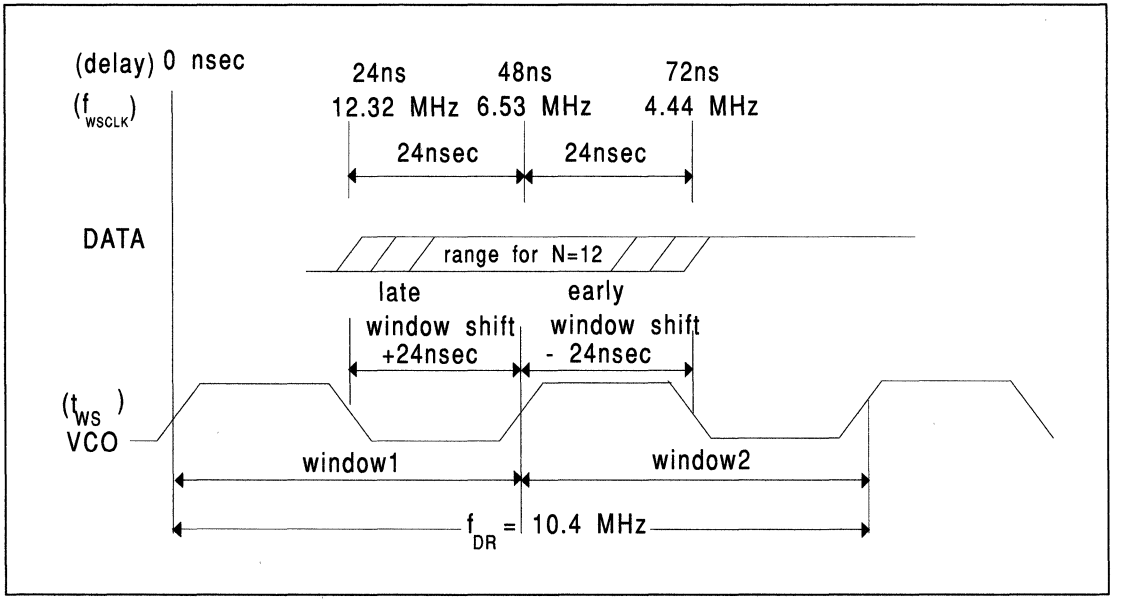

FIGURE 5. AWS OPTIMUM CENTER FREQUENCY

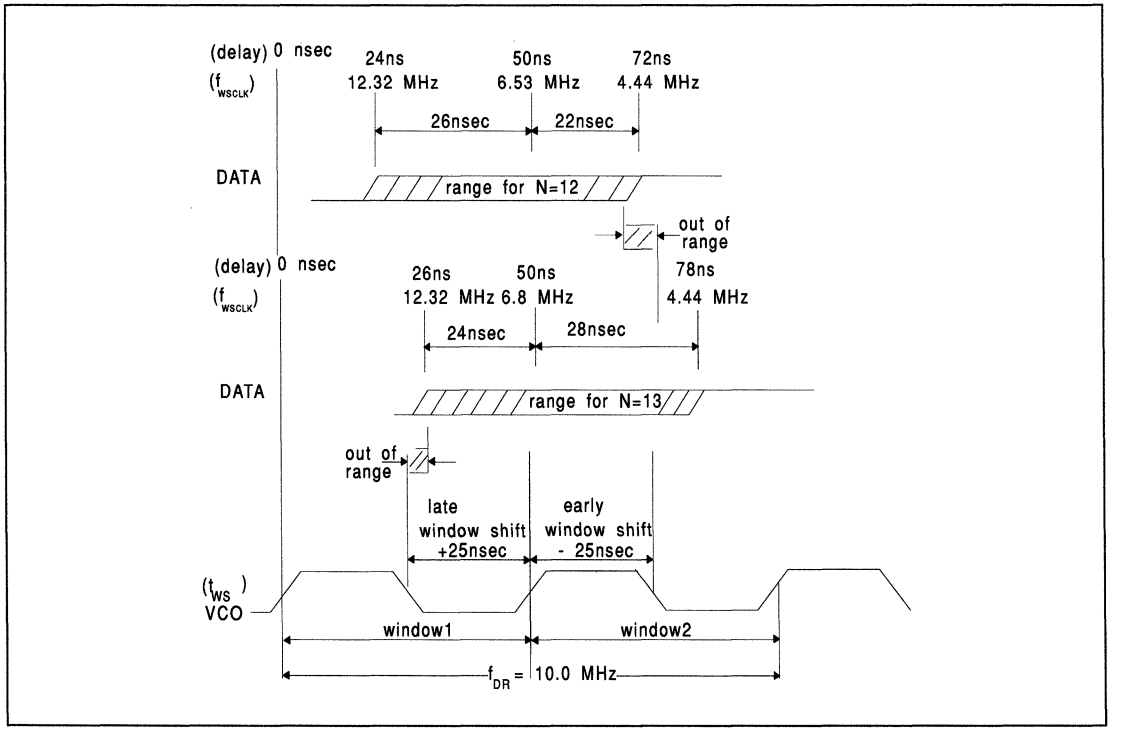

FIGURE 6. AWS NON-OPTIMUM FREQUENCY

Mode Selected	VF2	VF1	VF0	Data Rate (MHz)	Window Shift	Optimum Ctr f(N) MHz	Range N (T/4)
	0	0	z	$7.5 \leq f \leq 10.6$	Ext. Ref	7.4	17
	0	z	0	$7.5 \leq f \leq 10.6$	Ext. Ref	7.8	16
	0	z	1	$7.5 \leq f \leq 10.6$	Ext. Ref	8.3	15
	0	1	z	$7.5 \leq f \leq 10.6$	Ext. Ref	8.9	14
	z	0	z	$7.5 \leq f \leq 10.6$	Ext. Ref	9.6	13
Variable	z	z	0	$7.5 \leq f \leq 10.6$	Ext. Ref	10.4	12
Frequency -	z	z	1	$10.6 < f < 15.0$	Ext. Ref	11.4	11
Adaptive	z	1	z	$10.6 < f < 15.0$	Ext. Ref	12.5	10
Window Shift	1	0	z	$10.6 < f < 15.0$	Ext. Ref	13.9	9
	1	z	0	$15.0 = f$	Ext. Ref	15.6	8
	1	z	1	$15.0 = f$	Ext. Ref	17.8	7
	1	1	z	$15.0 = f$	Ext. Ref	20.8	6
	0	0	0	$5.0 \leq f < 7.5$	EARLY		
	0	0	1	$7.5 \leq f \leq 10.6$	EARLY		
	0	1	1	$10.6 < f < 15.0$	EARLY		
	0	1	0	$15.0 = f$	EARLY		
	z	0	0	$5.0 \leq f < 7.5$	None		
Variable	z	0	1	$7.5 \leq f \leq 10.6$	None		
Frequency -	z	1	1	$10.6 < f < 15.0$	None		
Percentage	z	1	0	$15.0 = f$	None		
Window Shift	1	0	0	$5.0 \leq f < 7.5$	LATE		
	1	0	1	$7.5 \leq f \leq 10.6$	LATE		
	1	1	1	$10.6 < f < 15.0$	LATE		
	1	1	0	$15.0 = f$	LATE		
Compatibility	0	z	z	5.0 MFM	EARLY		
Percentage	z	z	z	or	None		
Window Shift	1	z	z	7.5 RLL	LATE		

TABLE 2. PHASE MARGIN CONTROL

Relationships for Selecting Window Position:

1. t_{ws} = desired window shift in nsec, where $-2N \leq t_{ws} \leq 2N$
2. T_{wsclk} = required WSCLK period in MHz, where $4.44 \text{ MHz} \leq f_{wsclk} \leq 12.32 \text{ MHz}$
3. T_{dr} = data rate in nsec
4. $T_{wsclk}(N, t_{ws}, T_{dr}) = \{ (36/N)\, t_{ws} + [(9/N) T_{dr} + 9.2] \quad (t_{ws} \geq 0 \text{ ns})$
   $\{ (36/N)\, t_{ws} + [(27/N) T_{dr} + 9.2] \quad (t_{ws} \leq 0 \text{ ns})$

5.7 Crystal Oscillator

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. It is used primarily for internal reference when the PLL is not on data, and for accurate generation of the precompensated write data.

When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, with XTALOUT left unconnected.

The oscillator circuit includes a special implementation to better guarantee startup and to startup more quickly. A low value resistor is connected across the gain stage during the internal power-on reset. This quickly charges the external capacitors to the threshold value. As the resistor is disconnected, capacitive coupling induces a transient into the circuit, which helps to quickly achieve oscillation. A high value resistor is always present.

The oscillator should not be connected to any external circuits.WCLK may drive only high impedence MOS inputs. See the DC Electrical Characteristics section for specific limitations.

5.8 Write Data Conditioner

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY, LATE and SHIFT2X on the rising and falling edges of WCLK. They are immediately pipelined into flip-flops that are sampled on one edge of the XTALIN frequency (twice WCLK) to remove all jitter due to differential rise and fall times of WCLK.

When WGATE is active, the synchronized WDATA is channeled through an internal delay line for precompensation. If WPCEN is low, then the nominal delay is selected and passed to the WPCDATA output pin. If WPCEN is high, then the EARLY and LATE signals will select the early or late delays, respectively with SHIFT2X selecting the magnitude of shift. If both EARLY and LATE are inactive, or in the illegal case when they are simultaneously active, the nominal delay will be selected.

The differential delay between the early WPCDATA and nominal WPCDATA defines the amount of early precompensation, and similar, nominal WPCDATA to late WPCDATA defines the amount of late precompensation. The value is nominally 6.25%, or 12.5% with SHIFT2X active.

It should be noted that SHIFT2X may be used for dynamic dual level precompensation, or programmed with track information for zone level precompensation.

Finally, in MFM soft sector formats, the third WPCDATA output pulse on any given write operation is suppressed. This is done to ensure a low frequency interval after the write splice, required for initialization of the Acquisition Sequencer on subsequent reads.

5.9 Delay-Locked Loop (DLL)

This section includes the integrated delay lines and RAWDATA pulse forming logic of the WD10C23.

The Delay-Locked Loop consists of an integrated active delay line, phase detector, charge pump, and internal filter. The DLL has special start-up and monitoring circuitry to prevent harmonic lock and to provide for faster acquisition.

The DLL, when locked to the incoming XTALIN reference, will provide a 360^0 phase shift through its sixteen delay stages. Thus, each delay stage will accurately provide delays of XTALIN period/16. Since the XTALIN period is equal to the window, each delay cell represents $\pm$6.25% window. It is these delay stages which are used for accurate write data precompensation, window centering during reads, and window shifting as a percentage of the window.

5.10 Pulse Former

Pulse forming on RAWDATA is used to provide internal pulses suitable for use by the internal circuitry. In response to input rising edges on RAWDATA, it produces internal positive pulses terminated by a Delay Line tap. Pulse forming makes the WD10C23 extremely insensitive to the normal pulse width modulation seen on the raw read data from the read channel circuits.

5.11 Power-on Reset

This integrated function is used to reliably initialize the flip-flops to a predictable state during the application of V_{CC}. It is also used by the Crystal Oscillator startup circuit and DLL for fast and reliable startup.

5.12 Test Modes

The WD10C23 has several built-in modes for testability. Test modes are activated via one of two sequences.

The primary method of invoking test modes is through the OPTICAL pin. With the appropriate selection of EARLY,LATE, and WPCEN, one of the following tests may be selected:

5.12.1 Optical Mode

This mode allows RCLK to be generated at two times the data rate for compability with the WD60C31A optical ENDEC.

5.12.2 Acquisition Sequencer Mode

This mode passes the CRGATE and PLOCK signals to RDATA and RCLK respectively. CRGATE is a composite read gate signal, activated upon the switchover from reference to raw read data after two bytes of high frequency data have been sensed by the Synchronization Field Detector. PLOCK is asserted just prior to the transition from VLOCK to PLOCK.

5.12.3 Pump Up Mode

This test disables the data input to the Phase Detector, forcing a DC pump down. In this mode, the internal feedback from VCON to PUMP is opened, and the PUMP clamp defeated. With VCON forced to its locked voltage, the PUMP'S source I-V characteristics may be obtained.

5.12.4 Pump Down Mode

This test disables the data input to the Phase Detector, forcing a DC pump down. In this mode, the internal feedback from VCON (VCO control voltage) to PUMP (Charge Pump output) is opened. With VCON forced to its locked voltage, the PUMP's sink I-V characteristics may be obtained.

5.12.5 Phase Detector Mode

This test passes the Phase Detector's phase error signals to the Read Data Conditioner output, RDATA and RCLK. RDATA will represent frequency up, and RCLK frequency down. These signals, when used differentially, can be used to reconstruct the error amplifier envelope. This test may be used in conjunction with Pump Up/Down Tests when forcing D.C. pump up/down.

The second method of envoking tests is through illegal states.

5.12.6 Reset/Synchronization Mode

This mode is envoked by pulling $\overline{\text{EARLY}}$ and LATE low (illegal), and pulling WGATE high. Once in this configuration, the WPCEN pin may be used to generate an internal synchronization/reset pulse. The pulse will begin on the leading edge of WPCEN and end on the falling edge of WPEN.

This test is used to initialize internal logic states which may be otherwise unknown. For instance, WCLK is a divide-by-two of XTALIN, and its phase relationship is not important to system operation. For testablility however, the phase is important.

In this mode WCLK is set high, RCLK is set high, the internal VCO divider, is initialized, the VCO ring oscillator is halted, the Phase Detector is initialized, the Charge Pump is tristated, the Acquisition Sequencer is placed in velocity lock mode, the PUMP to VCON internal resistior is opened, and the PUMP clamp is defeated.

RGATE must not be true on the falling edge of WPEN. See External VCO Test.

5.12.7 Internal/External VCO Modes

The External VCO mode is envoked by pulling EARLY and LATE low (illegal), and pulling RGATE and WGATE high (illegal). WPCEN is now pulsed high for a duration of at least five XTALIN clocks. On the falling edge of WPCEN, an internal clock edge is created. This internal clock edge latches the state of the VCO selector: RGATE high selects External VCO mode; RGATE low selects Internal VCO mode.

This sequence is identical to the Synchronization/Reset Test above. When WPEN is true, this test is executed.

In External VCO mode, the PLL is running open loop with the VCO clock supplied through the OPTICAL input. The external VCO must be four times the data rate.

In External mode, PUMP to VCON internal resistance is open; the PUMP clamp is defeated, and OPTICAL is internally decoded as an active low. This allows OPTICAL to be used as the VCO input, while still allowing test mode selection.

Caution should be used to ensure that a test mode is not inadvertantly selected via the states of EARLY, LATE, WPCEN, RGATE, and WGATE.

EARLY	LATE	WPCEN	OPTICAL†	WGATE	RGATE	TEST MODE
x	x	x	1	x	x	Normal Operation
0	0	1	x	1	x	Reset/Synch Mode
0	0	⎍	x	1	0	Internal VCO Mode
0	0	⎍	x	1	1	External VCO Mode†
0	0	0	0	x	x	Phase Detector Mode
0	0	1	0	0	x	Acquisition Sequencer Mode
0	1	0	0	x	x	Pump Up/Phase Det Mode
0	1	1	0	x	x	Pump Up Mode
1	0	0	0	x	x	Pump Dn/Phase Det Mode
1	0	1	0	x	x	Pump Down Mode
1	1	0	0	x	x	Optical Mode
1	1	1	0	x	x	Normal Operation

TABLE 3. TEST MODE MATRIX

† After latching the external VCO mode of operation, $\overline{\text{OPTICAL}}$ is internally decoded as a logic low to allow for the enabling of the various test modes. Caution should be used to avoid inadvertantly enabling test modes under this condition.

6.0 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	-55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground (except XTALIN):	-0.5 to V_{CC}+0.5 volts
Voltage on XTALIN with respect to ground	-0.1 to V_{CC}+0.5 volts
Supply Voltage with respect to ground	+5.5 volts

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the above.

6.2 Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground.

Operating temperature (TA)	0°C (32°F) to 70°C (158°F)
Power supply voltage (VCC)	+5.0V±.25V

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6.3 Digital Signals

Input Signals:WGATE, RGATE, WPCEN,

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	
V_{IL}	Voltage input low			0.8	V	

Input Signals: SHIFT2X,RAWDATA,RLL/$\overline{MFM}$,WSCLK,$\overline{HS}$, SC/$\overline{COAST}$,$\overline{OPTICAL}$,WDATA,$\overline{EARLY}$,$\overline{LATE}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	
V_{IL}	Voltage input low			0.8	V	

Input Signals: RGATE,WGATE,WPCEN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IN}	Input leakage current	-10		+10	µA	V_{IN}=GND to V_{CC}

Input Signals: SHIFT2X,RAWDATA,RLL/$\overline{MFM}$,WSCLK,$\overline{HS}$,SC/$\overline{COAST}$,$\overline{OPTICAL}$,WDATA,$\overline{EARLY}$, $\overline{LATE}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IH}	Input high current	-0.1			mA	V_{IH}= 2.40 V*
I_{IL}	Input low currrent			-1.0	mA	V_{IL}=0.40V*

* Internal pullup resistor (10Kohm).

Input Signal: VF2, VF1, VF0

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	0.8V_{CC}			V	
V_{IT}	Voltage input 3-st volt	0.4V_{CC}		0.6V_{CC}	V	
V_{IL}	Voltage input low			0.2V_{CC}	V	
I_{IH}	Input high current	0.2		0.7	mA	V_{IH}=4.4 V, *
I_{IL}	Input low current	-0.2		-0.7	mA	V_{IL}=0.6 V, *
I_{IZ}	Input high Z current	-50.0		+50.0	µA	V_{IN} tristated, *, **

* Internal pullup and pulldown resistors (10Kohm). I_{IZ} tristate driver leakage current tolerance 50 µA.

**Allowable leakage of the tristate driver. Leakage greater than this will pull the input level out of the tristate band. This parameter is guaranteed by forcing voltages at the edge of the tristate band and measuring a tolerance greater than or equal to the I_{iz} specification.

Input Signal: VF2, VF1, VF0

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{RISE}	Rise time			25.0	nsec	0.2 V_{CC} to 0.8 V_{CC}; *
t_{FALL}	Fall time			25.0	nsec	0.8 V_{CC} to 0.2 V_{CC}; *

* Internal pullup and pulldown resistors (10Kohm). I_{IZ} tristate driver leakage current tolerance 50 µA.

Input Signal: XTALIN*

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	$f \leq 20.0$ MHz
V_{IL}	Voltage input low			0.8	V	$f \leq 20.0$ MHz
V_{IH}	Voltage input high	3.0			V	$f > 20.0$ MHz
V_{IL}	Voltage input low			0.4	V	$f > 20.0$ MHz

* Externally generated oscillator; XTALOUT open

Power Supply Currents: V_{CC}

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CCA}	5v active current		25	35	mA	V_{CC} = 5.25; *
I_{CCS}	5v static current		6	10	mA	V_{CC} = 5.25; **

* I_{CCA} measured as follows : Highest current draw is at 15 Mbit/sec during a write operation, with WSCLK programmed to 14 MHz and the VF pins programmed to one of the Adaptive Window Shift states. Idle currents will be several mamps lower.

** I_{CCS} measured as follows: During the Reset Test Mode, pull XTALIN high after the required number of XTALIN clocks. Follow by grounding WGATE, RGATE, WPCEN; all other pins floating.

Power Supply Voltage: V_{CC}

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{PRD}	Power reset inactive	4.1			V	*
V_{PRA}	Power reset active			2.6	V	**

* At this level V_{CC} level and above, the power-qualified reset is guaranteed to be inactive.

** At this level V_{CC} level and below, the power-qualified reset is guaranteed to be active.

MOS Outputs:WCLK, RCLK, RDATA, DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-20μA
V_{OL}	Output low volt			0.4	V	I_{OL}=+20μA
t_{RISE}	Rise time			7.0	nsec	0.8 to 2.0 V; *
t_{FALL}	Fall time			4.0	nsec	2.0 to 0.8 V; *

* Specified with a maximum external load of 20 pF; intended for high impedence MOS receivers, whose input threshold requirement is TLL compatible (i.e. 2.0/0.8V V_{IH}/V_{IL})

TTL Outputs:WPCDATA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-400μA
V_{OL}	Output low volt			0.4	V	I_{OL}=+2.0mA
t_{RISE}	Rise time			7.0	nsec	0.8 to 2.0 V; *
t_{FALL}	Fall time			4.0	nsec	2.0 to 0.8 V; **

* Specified with 20 pF/20 kΩ load to V_{SS}; intended for TLL receivers

**Specified with 20 pF load to V_{SS}/2 kΩ load to V_{CC}; intended for TLL receivers

6.4 Analog Signals (Crystal Oscillator)

Input: XTALIN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LKX}	Input leakage currents	-100		+100	nA	$V_{IN}/V_{OUT}=V_{IBIAS}$
V_{IBIAS}	Input bias volt	1.0		1.8	V	XTALOUT floating

Leakage measured after the internal Power-On Reset has timed out.

Output: XTALOUT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{OLS}	Short circuit sink current	4.5		18	mA	V_{CC}=+5; XTALIN=2.5V,XTALOUT=5V
I_{OHS}	Short circuit source current	-1.6		-9.4	mA	V_{CC}=+5; XTALIN,XTALOUT=0
R_{BO}	Operating bias resistance	1.1		5.6	Mohm	*
R_{BS}	Startup bias resistance	8		70	Kohm	**

*Measured after the internal Power Qualified Reset has timed out, R_{BO} is the feedback resistance between XTALIN and XTALOUT. With Vcc=5V, XTALOUT=0V, R_{BO} is modelled as a resistance combination with the measured leakage resistance, $R_{LKX} = V_{IBIAS}/I_{LKX}$. With XTALIN=$V_{IBIAS}$, XTALOUT = 0V, I_{LKX} measured at the XTALIN input is given by $V_{IBIAS}(1/R_{BO} + 1/R_{LKX})$ for leakage to GND, or by $V_{IBIAS}(1/R_{BO} + 1/R_{LKX})-5/R_{LKX}$ for leakage to Vcc. After measuring I_{LKX}, R_{BO} may be computed.

**Measured during the internal Power Qualified Reset, R_{BS} is the internal parallel resistor combination of R_{BO} and an additional resistor activated during Power Qualified Reset. R_{BS} is modelled as a parallel resistance to the measured leakage resistance $R_{LKX} = V_{IBIAS}/I_{LKX}$. To ensure that PQR is active, the supply should be set at 2.5V. At this supply setting, measure V_{IBIAS}. With XTALIN=V_{IBIAS}, XTALOUT = 0V, and Vcc=2.5V, I_{LKX} measured at the XTALIN input is given by $V_{IBIAS}(1/R_{BS} + 1/R_{LKX})$ for leakage to GND, or by $V_{IBIAS}(1/R_{BS} + 1/R_{LKX})-2.5/R_{LKX}$ for leakage to Vcc.

6.5 Phase-Locked Loop

Filter Input/Output: PUMP, VCON

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
I_{LKV}	VCON leakage current			100	nA	VCON=V_{CC}, *
I_{LKP}	PUMP leakage current	-100		100	nA	PUMP =V_{CC}/GND, *
I_{CLP}	PUMP clamp current	4		15	mA	VCON/PUMP=V_{CC}, **
V_{CAP}	PUMP clamp act threshold	2.7		3.9	V	$I_{PUMP} \geq$ 2.5 mA, **
V_{CDP}	PUMP clamp deact thrsh'd	.55		1.15	V	I_{PUMP} < 2.5 mA, **
I_{CLN}	VCON clamp current	1.3		4.5	mA	VCON=GND, **
V_{CLN}	VCON clamp threshold	.5		.95	V	I_{VCON} = -1µA, **
R_{PVC}	Pump-VCON comp res	2.2	3	5	Kohm	†
R_{PV0}	Pump-VCON BAND0 res		∝		ohm	†
R_{PV1}	Pump-VCON BAND1 res		∝		ohm	†
R_{PV2}	Pump-VCON BAND2 res	4.0	6	9.8	Kohm	†
R_{PV3}	Pump-VCON BAND3 res	2.3	3.5	5.6	Kohm	†
R_{PVV}	Pump-VCON Vlock res	531	627	1381	ohm	‡

* High impedence is guaranteed by placing the device in the Reset Test Mode to open the PUMP to the VCON resistor, tristate the Charge Pump, and disable the PUMP clamp. Leakage on VCON is not measured to V_{CC}, as there is a low voltage clamp on this pin.

** The PUMP clamp will activate, pulling PUMP low, when VCON rises above the PUMP clamp activation threshold voltage. The PUMP clamp is latched until VCON falls below the clamp deactivation threshold. The VCON clamp will activate, keeping VCON above ground, when VCON falls below the VCON clamp threshold. Both clamp currents/voltages should be measured after tristating the Charge Pump by disabling the RAWDATA input in phase lock, and selecting BAND0 or BAND1 to open the internal resistance betweeen PUMP and VCON.

† Measured during phase lock, this is the internal filter resistance between PUMP and VCON. The measurement should be made in the correct band with PUMP =1.5 V and VCON = 2.0 V.

‡ Measured during velocity lock, this is the internal filter resistance between PUMP and VCON. The measurement may be made in any band with PUMP = 1.5 V and VCON = 2.0V

Filter Input/Output: LPF

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LKL}	Leakage current	-10		10	µA	*
R_{LPC}	LPF-GND comp res		∝		ohm	**
R_{LP0}	LPF-GND BAND0 res		∝		ohm	**
R_{LP1}	LPF-GND BAND1 res	1.5	2.8	4.8	Kohm	**
R_{LP2}	LPF-GND BAND2 res	300	525	950	ohm	**
R_{LP3}	LPF-GND BAND3 res	75	150	250	ohm	**

* Tristate on LPF is guaranteed by setting VF0/=00 or zz.

** This in the internal filter resistance between LPF and GND. The measurement should be made in the correct band with LPF=2.0 V.

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Charge Pump: PUMP

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
I_{PLP}	Comp/BAND0-2 pmp cur	40		200	µA	phase lock
I_{PLV}	Comp/BAND0-2 pmp cur	80		400	µA	velocity lock
I_{PHP}	BAND3 pump current	80		400	µA	phase lock
I_{PHV}	BAND3 pump current	160		800	µA	velocity lock
R_{PB}	Pump cur symmetry ratio	.95		1.05		I_{up}:I_{down}
R_{KDVP}	Vlock-Plock pmp gain ratio	1.9		2.1		K_D Vlock:Plock
R_{KDH1}	Hi-lo band pump gain ratio	1.9		2.1		K_{D3}:K_{D2}

* Currents are for the measured VCON voltages found at the frequency extremes of the specified frequency bands, and are specified as magnitudes. Pump current is related to VCON approximately by $I \cong \beta (V_{CON} - Vt)^2$.

VCO: VCON

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CON}	VCO N-Channel control volt	.9		2.4	V	*
K_{OM}	Comp VCO gain	150		450	%/V	5Mbit MFM, **
K_{OR}	Comp VCO gain	150		450	%/V	7.5Mbit RLL, **
K_{O0}	BAND0 VCO gain	150		500	%/V	**
K_{O1}	BAND1 VCO gain	50		450	%/V	**
K_{O2}	BAND2 VCO gain	50		450	%/V	**
K_{O3}	BAND3 VCO gain	50		450	%/V	**
K_{OLM}	Comp open loop gain	15		45	%mA/V	MFM, †
K_{OLR}	Comp open loop gain	15		45	%mA/V	RLL, †
K_{OL0}	BAND0 open loop gain	10		45	%mA/V	†
K_{OL1}	BAND1 open loop gain	10		50	%mA/V	†
K_{OL2}	BAND2 open loop gain	10		50	%mA/V	†
K_{OL3}	BAND3 open loop gain	30		79	%mA/V	†

* This is the voltage developed by the filter and charge pump used to drive the internal VCO. The VCON voltage will be within this range for each of the four K_O settings in Table 1.

** The VCO frequency is proportional to the square of the voltage, V_{CON}, on the VCON input. VCO gain is given by % $(\Delta f / f_{AVE})$ $(1/\Delta V_{CON})$, or 4000 $(f2 - f1) / (f2 + f1)$ where $f2$ and $f1$ are the frequencies at $V_{CON} \pm$ 25mV respectively. The gains are specified for the V_{CON}'s found at the frequency extremes of the frequency bands. (i.e., at 5 and 7.5 MHz for BAND0).

† The open loop gain is given as a product of K_O and the average Charge Pump current. Specifically, $K_{O1} = K_O I_{AVE} = 2000\ (f2 - f1)\ (I2+I1)/\ (f2 + f1)$ where I2 and I1 are the Charge Pump currents found at the V_{CON} voltages determine $f2$ and $f1$, respectively.

7.0 TIMING CHARACTERISTICS

The following timings have been, where applicable, expressed in terms of the data rate by T = 1/(2x NRZ data frequency), for data frequencies in the range of 5 to 15 MBit/sec.

Several timings are referenced using a phase relationship of input signals called NULL phases. These phases should be such that there is zero phase error at the Phase Detector and zero net charge transfer on the PUMP pin. When the PLL is acquiring data in velocity lock mode, for a given set of conditions there is one phase of RAWDATA with respect to VCOIN which results in zero net current on PUMP. This phase is called NULLV (denoted ΘV).

The equivalent phase relationship found when the PLL is tracking data in phase detection mode is called NULLP(denoted Θp). When the PLL is tracking the crystal reference, the corresponding NULL, NULLX (denoted Θx), refers to the equivalent phase between XTALIN and the VCO.

All timings are measured with input levels of 2.4V V_{IH} and .4V V_{IL}, Ta = 0 °C to 70 °C; V_{SS} = 0V, V_{CC} = 5 V + 0.25 V. Closed loop PLL timings will be guaranteed to within ±1ns for power supply ripple of no more than 30mV peak to peak.

Transition times are measured at the 2.0 V crossing for high going transitions, and at the 0.8 V crossing for low going. Any deviations from these criteria will be specified.

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7.1 Disk Drive Raw Read Data

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{RDH}	RAWDATA pulse width high	15			nsec	
t_{RCL}	RAWDATA pulse width low	15			nsec	
t_{RDT}	RAWDATA period	T			nsec	MFM mode, *
t_{RDT}	RAWDATA period	2T			nsec	RLL mode, *

* This timing is intended to indicate that two consecutive bit shifts, in a direction such that a minimum interval is created, can be tolerated up to just under T/2ns each without recycle failure in the phase or data detectors.

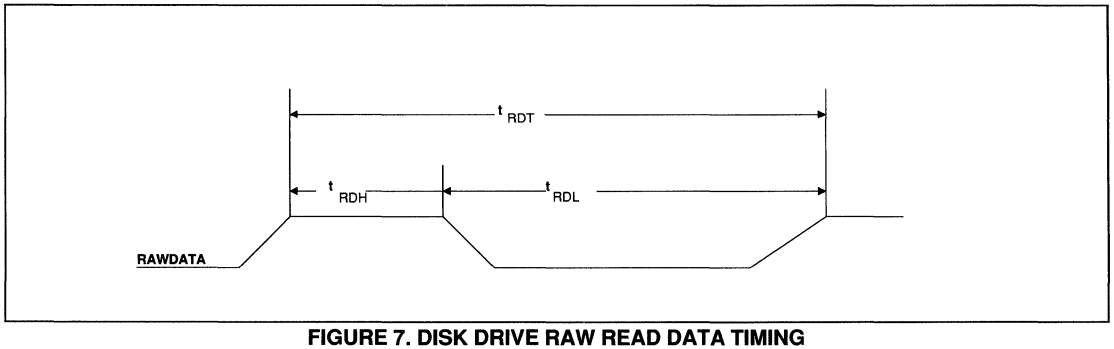

FIGURE 7. DISK DRIVE RAW READ DATA TIMING

7.2 Disk Drive
Raw Read Data Frequency Detector

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DRL}	DRUN low freq threshold	2.50T	2.625T	2.75T	nsec	MFM mode, *
t_{DRH}	DRUN high freq threshold	1.188T	1.313T	1.438T	nsec	MFM mode, *
t_{DR}	DRUN threshold	4T		5T	nsec	RLL mode, **

* DRUN is guaranteed to be high for RAWDATA frequencies greater than t_{DRL} but less that t_{DRH}. For frequencies less than t_{DRL}, DRUN will not remain high, and for those greater than t_{DRH} DRUN behavior is not specified. DRUN low pulse widths will always reflect the pulse periods on RAWDATA for those periods which cause DRUN to drop. Thus the minimum will typically be 2.625T nsec.

** DRUN mInimum low pulse widths will be typically T nsec.

7.3 Read Data Conditioner

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
t_{RDP}	RDATA pulse width		T		nsec	
t_{RCP}	RCLK pulse width		T		nsec	
t_{RCS}	RDATA setup to RCLK	T/2-6.6	T/2	T/2+6.6	nsec	
t_{RCH}	RDATA hold from RCLK	T/2-6.6	T/2	T/2+6.6	nsec	

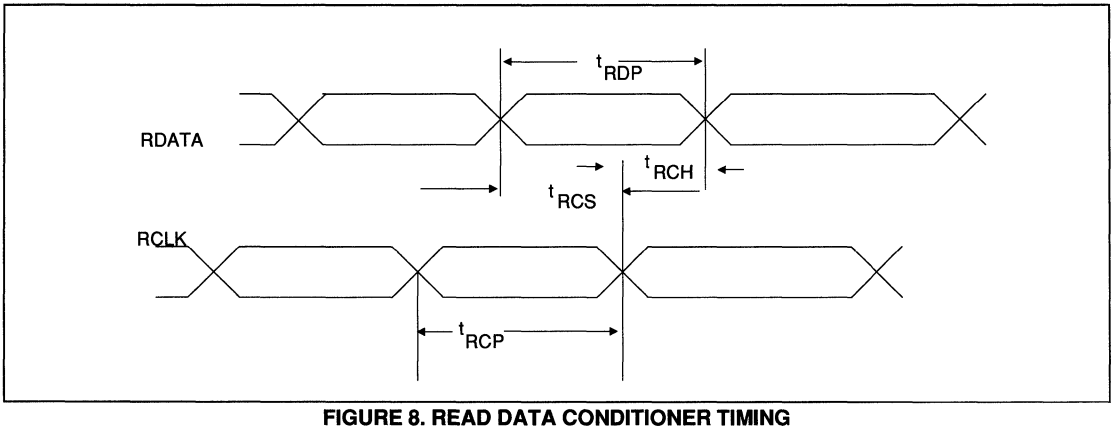

FIGURE 8. READ DATA CONDITIONER TIMING

7.4 Read Data Detector (Percentage Window Shift)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DDW}	Data Detect Window	T-1	T	---	nsec	
t_{DWC}	DD Center Window	x/2-1	x/2	x/2+1	nsec	x = T_{DDW}, *
t_{DWSE1}	DD Window Shift Early 1X	-T/16-1	T/16	-T/16+1	nsec	SHIFT2X=GND
t_{DWSL1}	DD Window Shift Late 1X	T/16-1	T/16	T/16+1	nsec	SHIFT2X=GND
t_{DWSE2}	DD Window Shift Early 2X	-T/8-1	T/8	-T/8+1	nsec	SHIFT2X=V_{CC}
t_{DWS12}	DD Window Shift Late 2X	T/8-1	T/8	T/8+1	nsec	SHIFT2X=V_{CC}

* Window centering, t_{DWC}, is not a function of window loss and is thus correctly specified in terms of t_{DDW}.

7.5 Read Data Detector (Adaptive Window Shift)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{WS}	AWS Accuracy			5	%/Δns	**

** The accuracy is specified as the error in the gain (slope), 36/N, as given by equation 4 from Table 2. The t_{WS} error is determined by multiplying the difference in T_{WSCLK} from 153.2 ns. For example, if the required T_{WSCLK} is 160.2 ns, then the maximum t_{WS} error will be the 0.05x(160.2 -153.2)=350ps. If the required T_{WSCLK} were 150.2 ns, the maximum error would be 0.05x(150.2-153.2)ns=-150ps.

7.6 Phase-Frequency Detector

7.6.1 Phase Lock Mode

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{PDW}	Phase Detect Window		T		nsec	*
t_{PWC}	Phase Centering Window	x/2-1	x/2	x/2+1	nsec	$x=T_{PDW}$, *

* The phase detection window must be equal to T. Any apparent gain or loss in the window must be due to tester inaccuracy and/or statistical error in the measurement. Phase window centering is not a function of window size, and is thus correctly specified in terms of T_{PDW}.

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7.6.2 Velocity Lock Mode (MFM)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VDW}	Velocity Lock Detect Window		4T		nsec	
t_{VWE}	Velocity Lock Early Window		2T		nsec	
t_{VWL}	Velocity Lock Late Window		2T		nsec	

7.6.3 Velocity Lock Mode (RLL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VDW}	Velocity Lock Detect Window		6T		nsec	
t_{VWE}	Velocity Lock Early Window		3T		nsec	
t_{VWL}	Velocity Lock Late Window		3T		nsec	

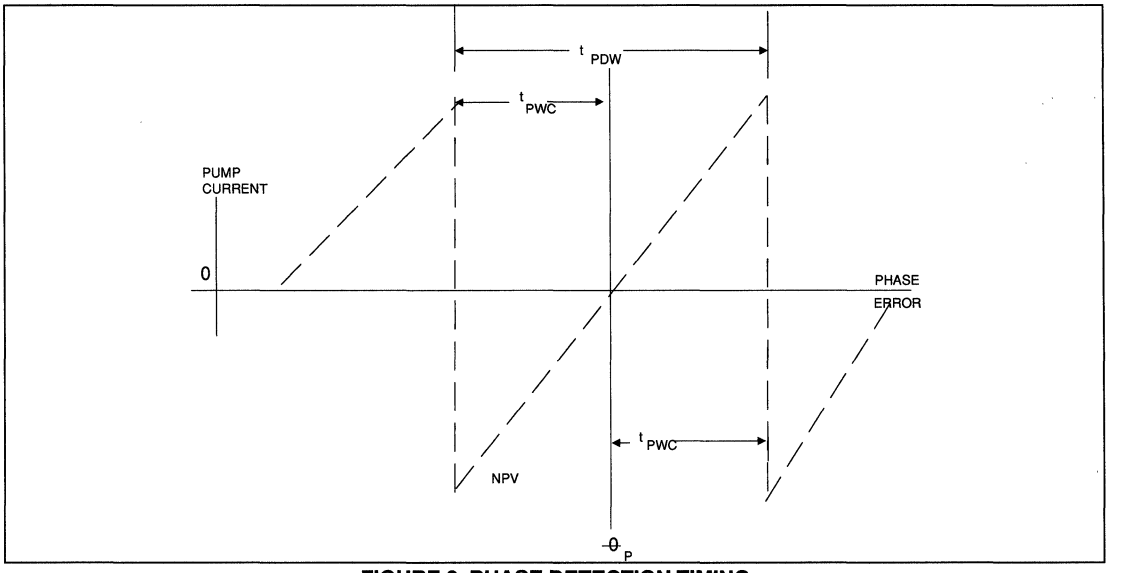

FIGURE 9. PHASE DETECTION TIMING

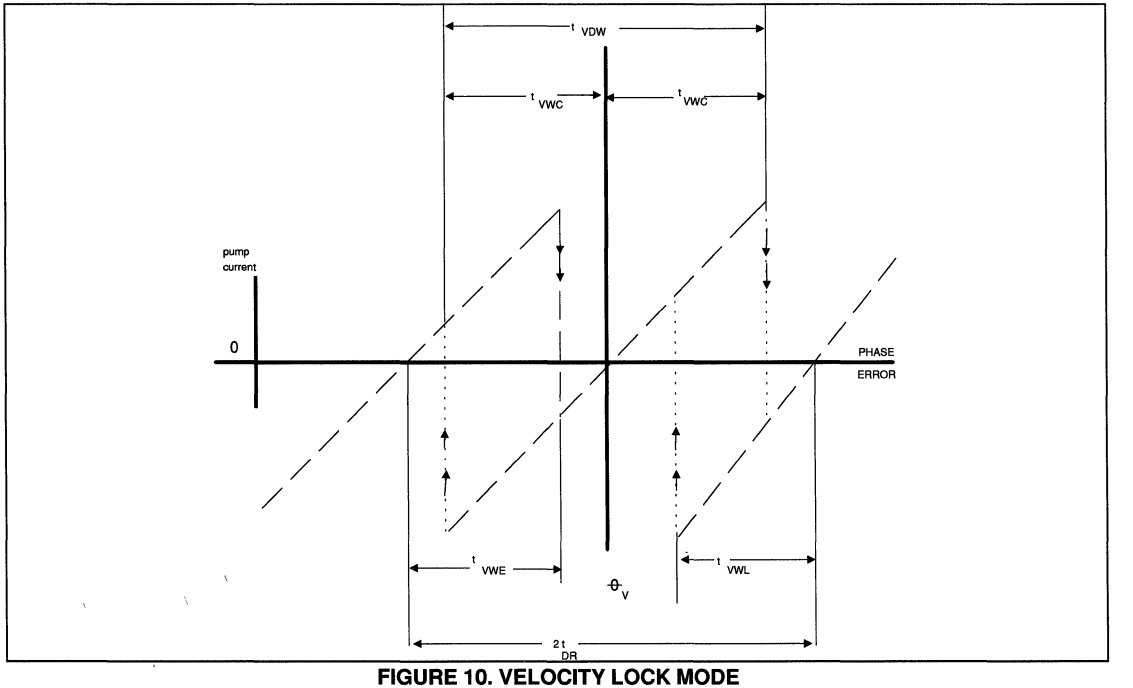

FIGURE 10. VELOCITY LOCK MODE

7.7 Write Data Conditioner

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{WCS}	WD setup to WCLK	8			nsec	*
t_{WCH}	WD hold from WCLCK	3			nsec	*
t_{PCE1}	Early precomp 1X	T/16-1	T/16	T/16+1	nsec	**, SHIFT2X=GND
t_{PCL1}	Late precomp 1X	T/16-1	T/16	T/16+1	nsec	**, SHIFT2X=GND
t_{PCE2}	Early precomp 2X	T/8-1	T/8	T/8+1	nsec	**, SHIFT2X=VCC
t_{PCL2}	Late precomp 2X	T/8-1	T/8	T/8+1	nsec	**, SHIFT2X=VCC
t_{PCP}	WPCDATA high	T-10	T		nsec	***, SHIFT2X=GND
t_{WPD}	WDATA to WPCDATA	.5T		2.75T+50	nsec	

* Timings are for WDATA, $\overline{EARLY}$, $\overline{LATE}$, and SHIFT2X.

** Differential measurement of rising edge of precompensated WPCDATA versus non-precompensated WPCDATA.

*** Measured for early and late precompensated WPCDATA.

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7.8 TTL XTALIN Input Clock, WCLK Output

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{XS}	Crystal startup		1	2	msec	
t_{XP}	XTALIN freq @ TTL levels			20	MHz	40/60% Duty Cycle
t_{WCD}	WCLK duty cycle	45		55	%	*

* WCLK duty cycle is specified for the high phase, at any voltage between 0.8-2.0 V. This guarantees the worst case duty cycle seen at the input of a receiver, whose input threshold is specified to be within this voltage range. See the Output Driver section of the DC Electrical Characteristics above for load limitations.

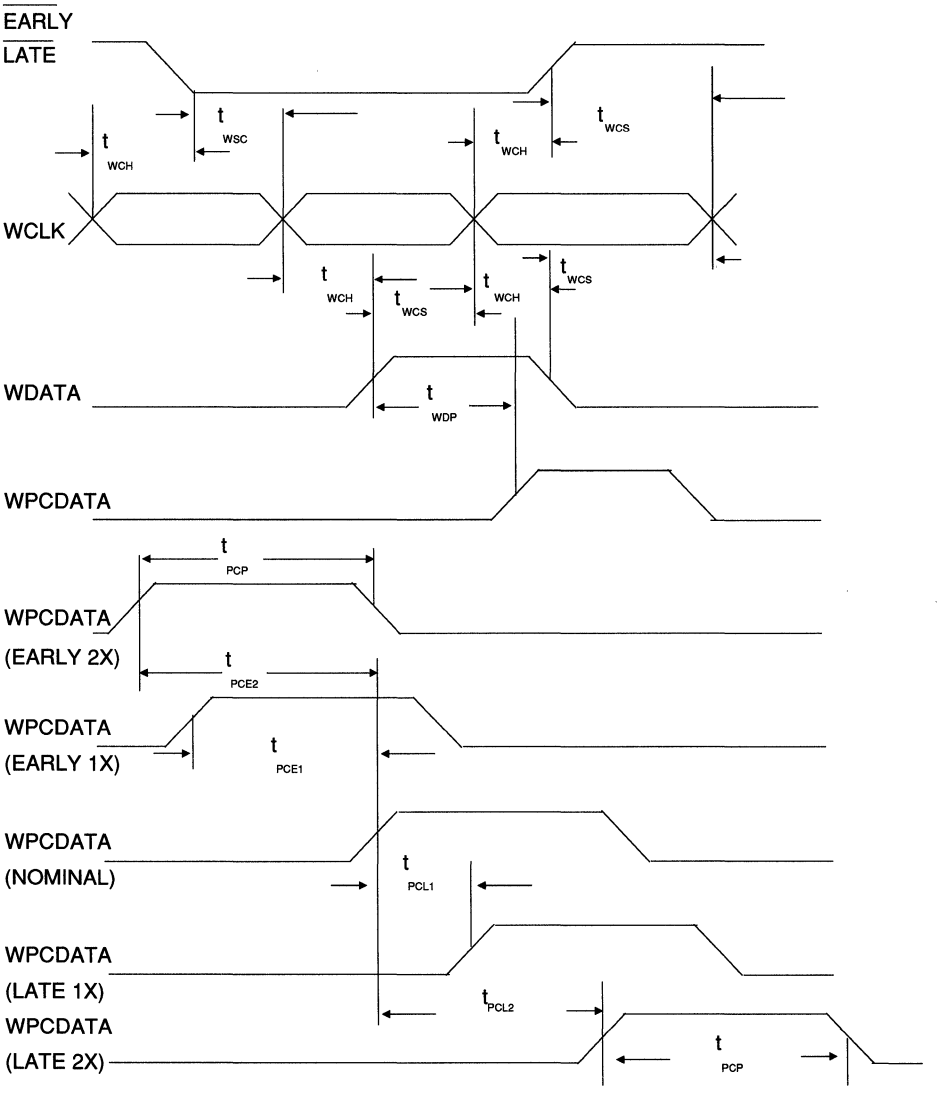


FIGURE 11. WRITE DATA CONDITIONER TIMINGS

7.9 Delay Line

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DRC}	Delay-Locked Loop Time Constant		.4	1.5	msec	*

* This is the time required for the DDL to acquire the XTALIN frequency. It should be used in conjunction with t_{XS} to determine the time from power up to device ready.

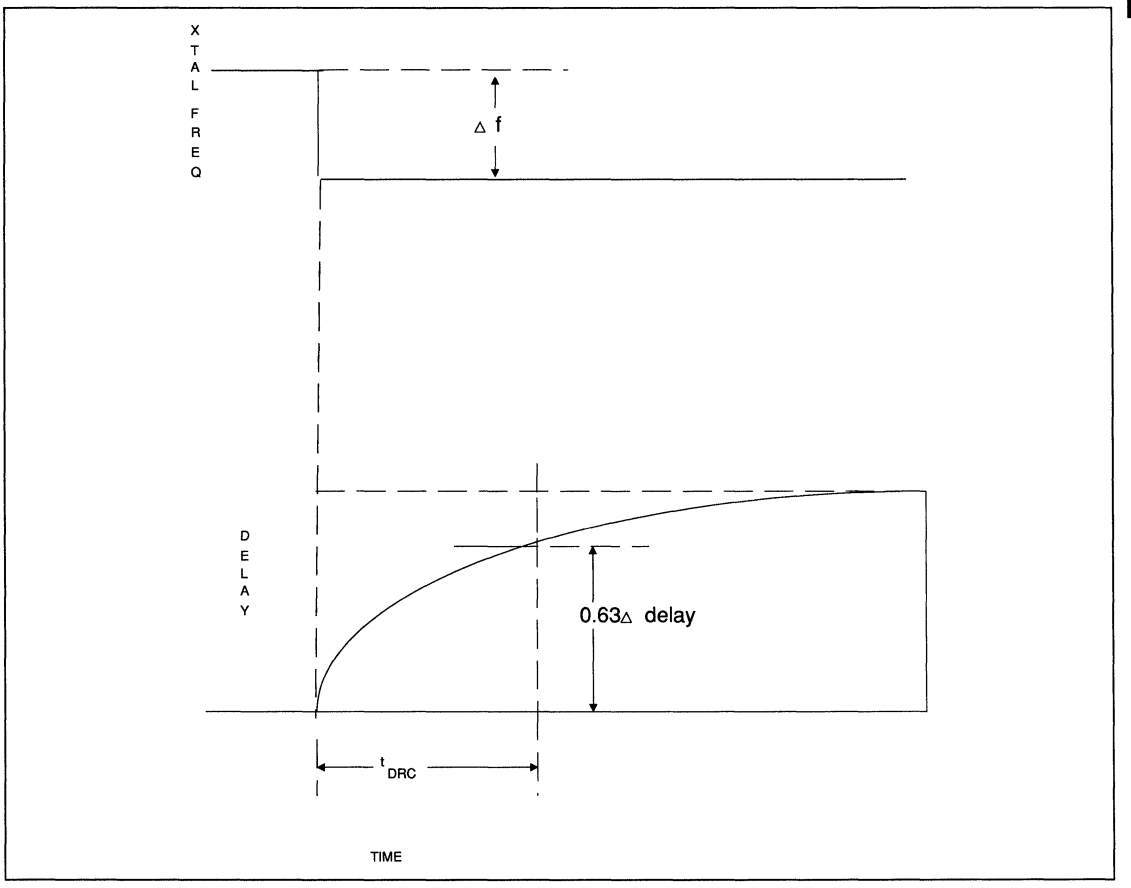
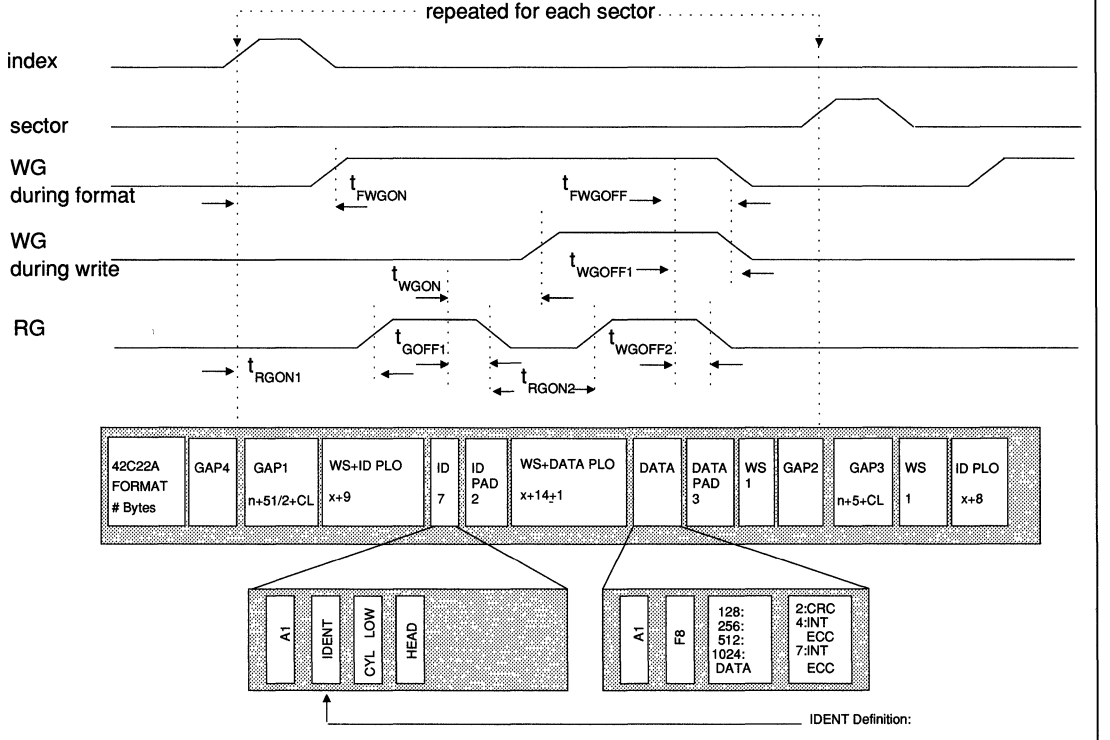


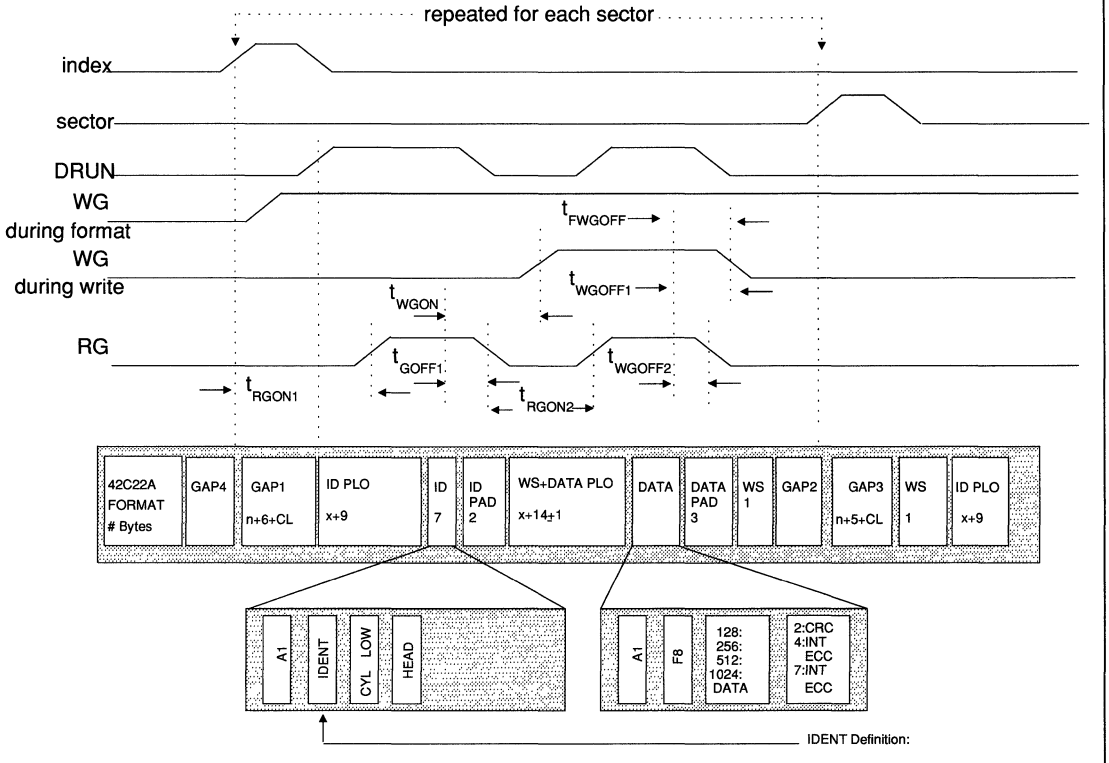
FIGURE 12. DELAY LINE TIMING



NOTES:

1. n=contents of Sector Number Register during Format command.
2. CL=controller latency. 0≤CL≤1 byte times.
3. x=contents of PLO register. ID PLO Length is programmable during Format command. DATA PLO Length is programmable during Write command. Data PLO Length is 11 during Format. Data PLO Length is 12±1 during write if x=0.
4. t_{WGON}=17±1 bit times with respect to RD in.
5. t_{WGOFF1}=28 bit times with respect to WD out.
6. t_{RGOFF1}=9±1 bit times with respect to RD in.
7. t_{RGOFF2}=9±1 bit times with respect to RD in.
8. t_{RGON1}=z+CL byte times with respect to INDEX/SECTOR (SCT). Sector is tied to DRUNSCT always. z=contents of internal GAP register.
9. t_{RGON2}=35±1 bit times with respect to RD in.
10. GAP2= speed tolerance + comined ENDEC delays + other GAP requirements (i.e. SERVO) GAP2 Length= (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad)
11. t_{FWGON}=n+51/2+CL byte times with respect to INDEX/SECTOR. n=contents of Sector Number Register during Format. t_{WGOFF}=20 bit times with respect to WD out.

FIGURE 13. HARD SECTOR FORMAT w/WG PULSE OPTION



NOTES:

1. n=contents of Sector Number Register during Format command.
2. CL=controller latency. 0≤CL≤1 byte times.
3. x=contents of PLO register. ID PLO Length is programmable during Format command.
   DATA PLO Length is programmable during Write command. Data PLO Length is 11 during Format. Data PLO Length is 12±1 during write if x=0.
4. t_{WGON}=17±1 bit times with respect to RD in.
5. t_{WGOFF1}=28 bit times with respect to WD out.
6. t_{RGOFF1}=9±1 bit times with respect to RD in.
7. t_{RGOFF2}=9±1 bit times with respect to RD in.
8. t_{RGON1}=19±1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during Format and DRUN is tied to DRUNSCT during Read and Write.
9. t_{RGON2}=35±1 bit times with respect to RD in.
10. GAP2= speed tolerance + comined ENDEC delays + other GAP requirements (i.e. SERVO)
    GAP2 Length= (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad)

FIGURE 14. HARD SECTOR FORMAT w/ SOFT SECTOR R/W

8.0 PRODUCT COMPATIBILITY

The following is a matrix of the features for each of the data separators from Western Digital's family of devices.

Market Number	**WD10C 20A**	**WD10C 21A**	**WD10C 20B**	**WD10C 22B**	**WD10C 23**
CMOS	3 µSM	3 µSM	3 µSM	3 µSM	1.25 µDM
min ext componts	15	15	14	14	3
ext delay line	√	√			
int delay line			√	√	√
ext VCO	√	√	√	√	
int VCO					√
MFM encoding	√		√	√	√
RLL encoding		√		√	√
5 Mbit	√	√	√	√	√
7.5 Mbit		√		√	√
10 Mbit				√	√
15 Mbit					√
var frequency					√
soft sector	√	√	√	√	√
hard sector					√
write precomp	ext dly	ext dly	± 12.5 %	± 12.5 %	*
window shift	ext dly	ext dly	± 12.5 %	± 12.5 %	**
adapt win centering					√

TABLE 4. PRODUCT COMPATIBILITY FOR DATA SEPARATORS

* ± 12.5 % / ± 6.25 %

** ± WIN / 2