WD83C690

Ethernet LAN Controller

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION AND APPLICATION

The WD83C690 Ethernet LAN Controller (ELC) is a VLSI device designed to interface with networks such as Ethernet, Cheapernet, and StarLAN. Functionally similar to the National DP8390 device, the WD83C690 incorporates an original architecture and provides several new registers (for en-hancements, block address, and test control). The device is implemented in a single-clock, single-phase synchronous design, with the exception of serial portions of the receiver and transmitter. The WD83C690's signal functions, polarity requirements, and timings are compatible with the WD83C583 and WD83C593 bus interface devices.

1.1 FEATURES

- Meets the IEEE 802.3 protocol for networks such as Ethernet, Cheapernet, and StarLAN
- Provides direct memory address (DMA) channel for transferring data between memory and the host
- Implements an original, sophisticated architecture in standard cell technology
- Provides programmable wait states and slot times
- Provides full duplex loopback capability
- Requires single, 5V power supply
- Supports physical, promiscuous, and broadcast address filtering
- Provides efficient, versatile buffer management

1.2 SYSTEM INTERFACE

The WD83C690 is part of a three-device set that implements the complete IEEE 802.3-compatible network node electronics. The WD83C691 Manchester Encoder/Decoder (MED) and the WD83B692 Ethernet Transceiver (ET) comprise the other two devices in the set. The WD83C691 provides the Manchester encoding/decoding functions, while the WD83B692 serves as a coaxial cable line driver/receiver. Figure 1-1 illustrates how the devices interface.

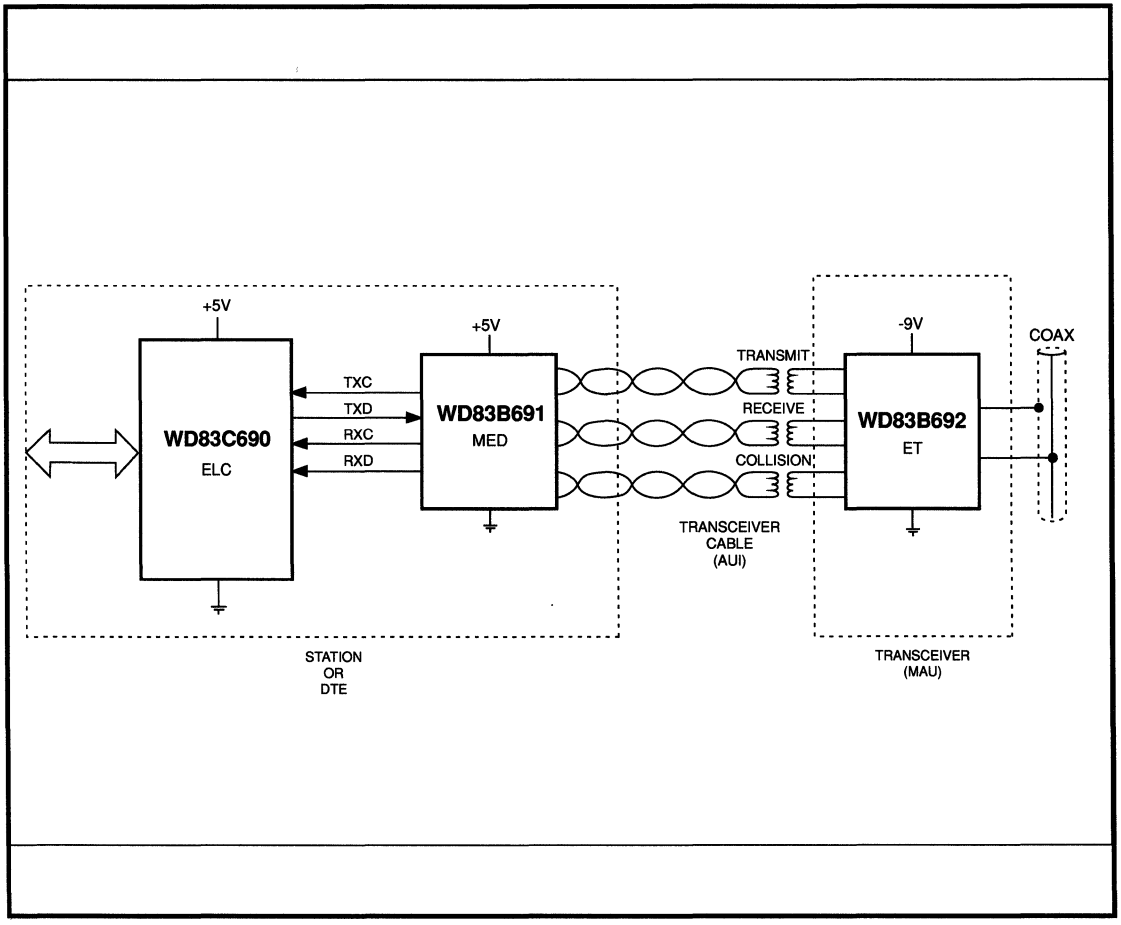

FIGURE 1-1. WD83C690 SYSTEM INTERFACE

2.0 OPERATIONAL DESCRIPTION

This section describes the functional blocks that comprise the Ethernet LAN controller. A general system block diagram is shown in Figure 2.1. Sections 3 and 4 provide more detailed explanations of the receive and transmit functions and memory interface.

2.1 RECEIVE FEEDBACK MULTIPLEXOR

For testing purposes, an internal multiplexor at the network interface end of the receiver permits the loopback of transmitted data, and the use of transmit enable as a carrier sense signal. The multiplexor can be programmed via the transmit configuration register.

2.2 CARRIER SENSING

Carrier sensing is done externally and brought into the WD83C690 through the CRS pin. Received data and clock are brought in through the RXD and RXC pins, respectively, and feed the CRC checker, the octet alignment circuit, and the serial-to-parallel converter.

2.3 CRC CHECKER

The receiver section performs the cyclic redundancy check (CRC) for the incoming serial data. The CRC computation includes the address, data, and CRC fields. It excludes the preamble and SFD.

The CRC polynomial used is AUTODIN II (X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X1 + 1).

2.4 RECEIVE DESERIALIZER

The receive deserializer clocks incoming bits into an eight-bit serial-to-parallel shift register, and, when an octet is complete, loads the parallel data into the receiver "first in, first out" buffer (FIFO). Octet alignment is determined by a synchronization circuit which detects the start of frame delimiter (SFD).

2.5 ADDRESS RECOGNITION LOGIC

The destination address is compared to a 6-byte station address stored in the internal registers, and, if all bytes match (or if promiscuous mode is enabled), the frame is received. When multicast addressing is enabled, only the individual/group bit of the destination address is checked. No filtering of group addresses is done. Broadcast frames are received when the broadcast enable bit is active.

If the address is rejected, the receive FIFO is cleared and none of the frame is stored. If the address is accepted, buffering of the frame begins.

2.6 RECEIVE PROTOCOL FINITE STATE MACHINE (RPFSM)

The Receive Protocol Finite State Machine (RPFSM) determines whether the incoming frame will be saved in memory, and coordinates the operation of all other blocks in the receiver section. This involves generating status information regarding each frame (the information is placed in the receiver status register) and keeping track of the length of the frame via a 16-bit-wide frame length byte counter attached to the state machine. The block is controlled by the receiver configuration register and the START and STOP bits from the command register. The receiver error counters are also under control of this circuit.

2.7 RECEIVER ERROR COUNTERS

There are three error counters in the receiver section: the CRC error counter, the frame alignment error counter, and the missed packet counter. Each counter is eight bits wide and can be incremented up to 255, where it remains until the counter clears (when the register is read or the device reset).

The CRC error counter, under control of the receive protocol finite state machine, is incremented when a received frame's computed CRC does not match the appended CRC.

The frame alignment error counter is advanced when a frame with too many dribble bits and a CRC error at the same time is received.

The missed packet counter is incremented when a frame that would ordinarily be stored in memory was not stored (either because the receiver was operating in monitor mode, or because there was insufficient memory to store the entire frame).

2.8 FIFOS

The transmitter and receiver sections have similar, but independent, 16-byte deep FIFOs. These FIFOs have a programmable threshold level that allows the transmit receive (TR) direct memory access controller (TRDMA) to determine when there is a need to move data between the WD83C690 and memory.

2.9 TRANSMITTER PROTOCOL FINITE STATE MACHINE (TPFSM)

The transmitter protocol finite state machine (TPFSM) coordinates the operation of all blocks that comprise the transmitter section. It decides when to transmit, when to defer transmission, and, in the event of a collision, when to back off and attempt to transmit again. The transmit configuration register controls the operation of this state machine, which updates the transmit status register after each attempt to send a frame.

2.10 TRANSMIT SERIALIZER

The transmit serializer converts the 8-bit parallel data from the transmit FIFO into serial data. Serial data is clocked out of the TXD pin (least significant bit first) by the rising edge of an external clock at the TXC pin.

2.11 TRANSMITTER CRC GENERATOR

Using the same polynomial as the receiver CRC checker, the transmit section generates CRC serially and appends it to each outgoing frame. (CRC is clocked-out most significant bit first.)

2.12 PREAMBLE GENERATOR

The preamble generator block generates a data pattern of alternating "1" and "0" bits.

2.13 JAM GENERATOR

This block generates a pattern of consecutive "1" bits. It drives the TXD pin when a collision is detected.

2.14 SERIAL STREAM MUX

Using the serial stream multiplexor, the TPFSM composes each frame from its constituent parts.

2.15 SYNC-TO-TXC

To ensure minimal output jitter, the transmit data stream is reclocked to the rising edge of TXC prior to driving the pin.

2.16 COLLISION DETECTION LOGIC

Collisions are sensed externally during transmission, then input through the COL pin.

2.17 DMA CONTROLLER

There is an internal direct memory access (DMA) controller, TRDMA, which moves packets between buffer memory and the WD83C690.

The DMA generates 16-bit addresses, supplemented by 8 bits of static address in the high order positions (A16-23). The DMA controller supports memory cycles as short as 200 nsec, which can be slowed down using the MEM-READY pin or by programming a default number of wait states into the configuration register.

2.18 ASSEMBLY AND DISASSEMBLY LATCHES

The TRDMA does all of its transfers as pairs of 8-bit bytes. The assembly and dissassembly latches match the internal 8-bit data path to the external data bus. When interfacing to a 16-bit bus, the assembly latches combine two 8-bit words to form a 16-bit word; when interfacing with an 8-bit bus, they supply the two consecutive bytes of a transfer. The disassembly latches perform the opposite function.

2.19 BUS INTERFACE AND INTERNAL BUS ARBITRATOR

The bus interface unit (BIU) and internal bus arbitrator control access to the WD83C690's internal registers and ensure that the device does not attempt a DMA transfer until it has access to the memory bus. The BIU transfers data from buffer memory to the internal disassembly latches and from the internal assembly latches to buffer memory. It generates the bus request (BREQ), memory strobes (MRD and MWR) and the address strobe (ALE).

To control the initiation of a transfer and insertion of wait states, the BIU observes the bus grant (BGRANT) and memory ready (MEMRDY) signals.

Until BGRANT becomes true, the memory strobes, address outputs, and ALE outputs are tri-stated. Once BGRANT is issued, the host must not drive the address, data, ALE, or memory strobes until BREQ is dropped and BGRANT taken away at the end of the DMA burst. Failure to adhere to this rule will result in contention on the lines and corruption of the data transferred. Refer to the timing diagrams in Appendix D for more details.

When the DMA bursts are complete and BGRANT is negated, the host can access the internal bus. Although BREQ may again become active in response to new DMA needs, the arbitration logic permits access until BGRANT becomes true. The internal arbitrator generates the READY signal to tell the host that the requested I/O access has been made and the internal bus is available.

The host may force the WD83C690 to interrupt a DMA burst by removing the BGRANT signal while BREQ is still active. When this happens, the BIU completes the current byte or word transfer, then relinquishes the bus by dropping BREQ for one clock. The internal bus arbitration unit disables the DMA until BGRANT is again true, at which time, the burst continues where it left off.

2.20 ACCESSING INTERNAL REGISTERS

To access an internal register, the host must assert the chip select (CS) signal and wait until READY is asserted before driving the bus. When the WD83C690 is not involved in a DMA operation, it is not necessary to wait for READY to be asserted prior to driving the address, ALE, and data lines. CS must be maintained throughout the access.

In multiplexed bus applications, ALE latches the register address into the WD83C690. In non-multiplexed bus applications, ALE should be driven high or pulled up during register access to allow the address to flow through the internal transparent latch.

To read from a register, IOR must be asserted by the host (either before or after CS). It is recognized by the internal bus arbitrator (BUSARB) circuit, which enables data flow from the addressed register to the AD00-07 pins. During read operations (which are always done through the AD00-07 pins), AD08-15 are tri-stated. READY indicates when the host can sample data and terminate the read operation.

To write to a register, IOW must be asserted by the host and recognized by the internal BUSARB. When the bus is free for the transfer, READY is asserted and the register address is latched internally. Data is latched into an intermediate transfer latch with the trailing edge of IOW, and, two clocks later, transferred to the destination register.

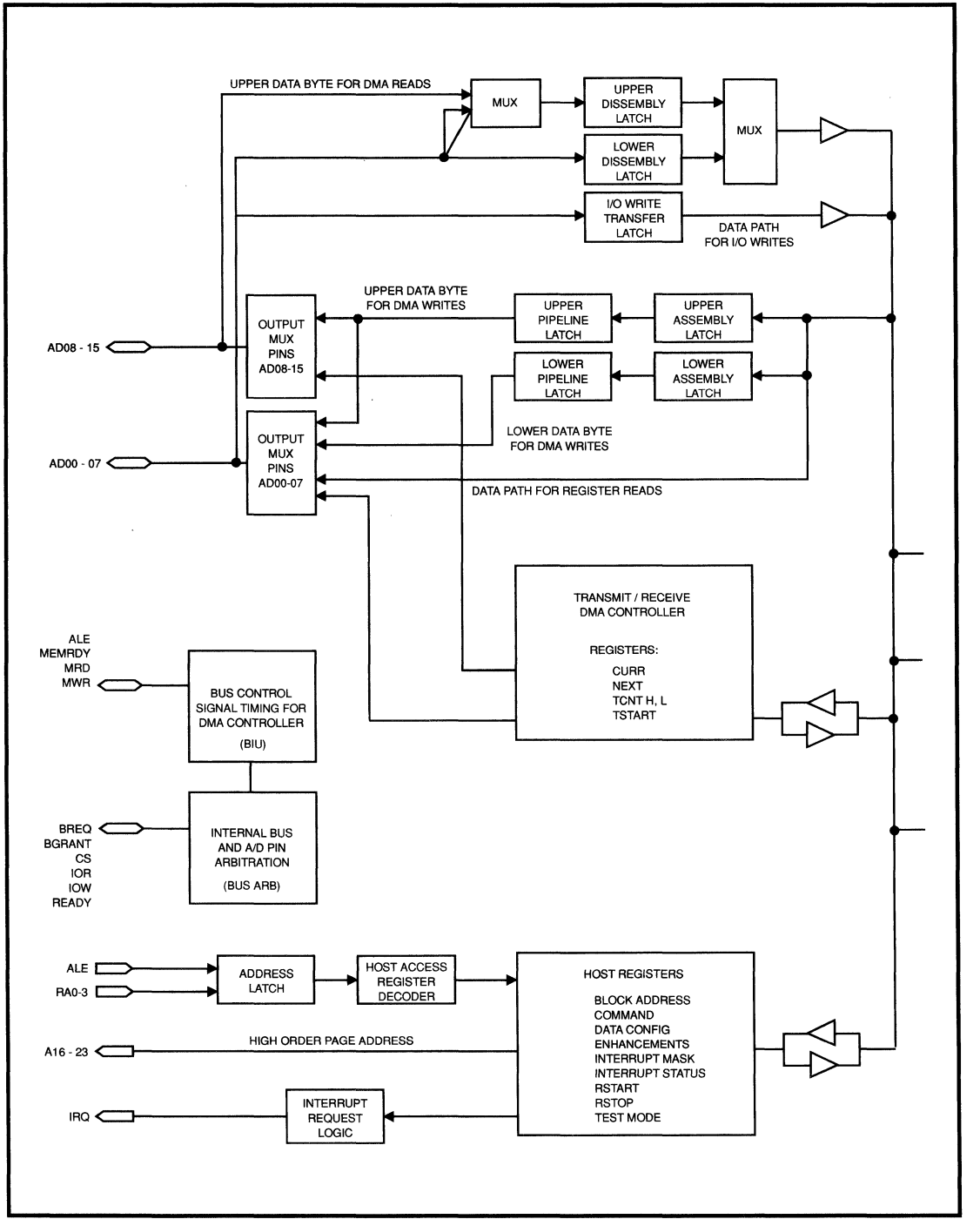

FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM

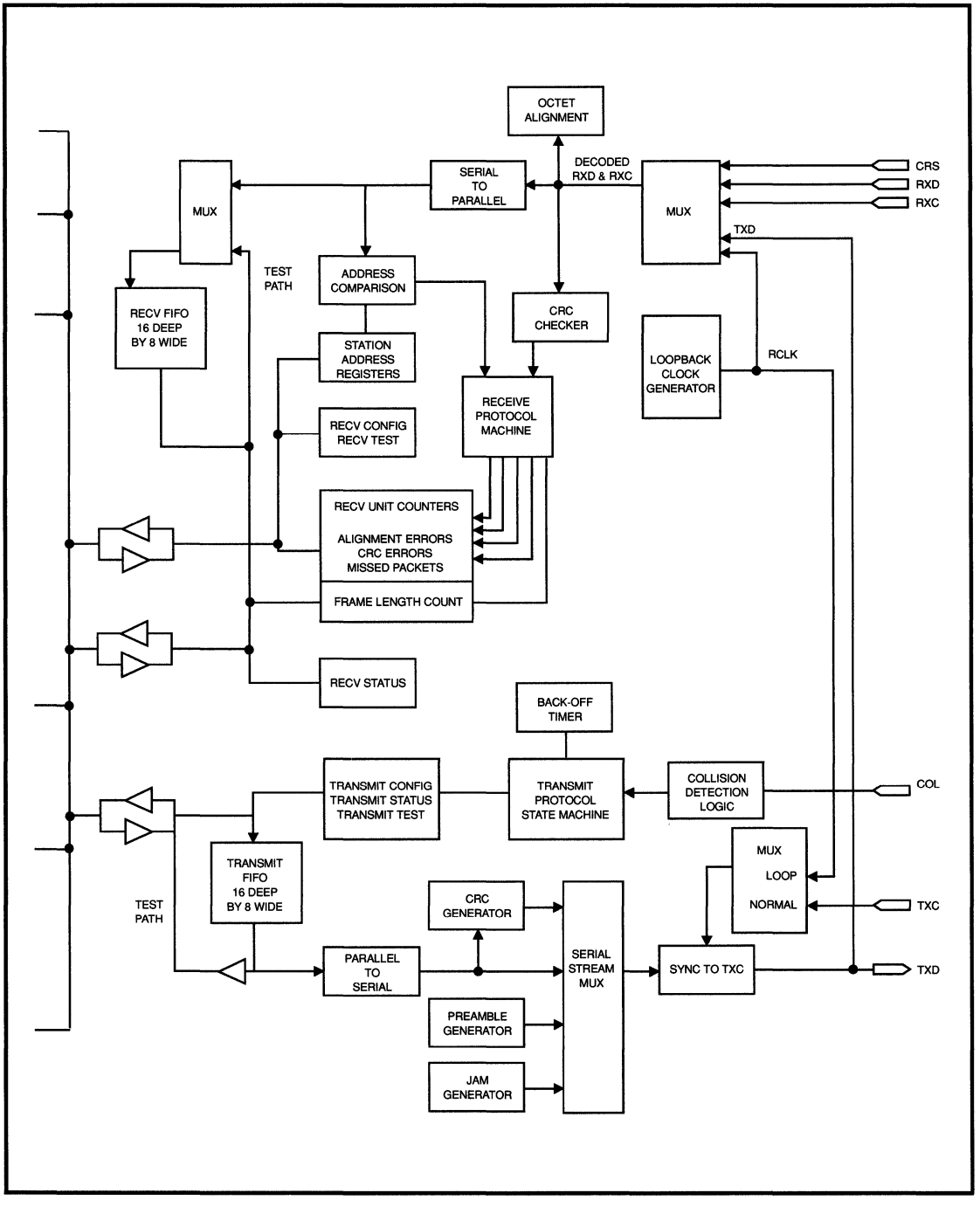

FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM (Continued)

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3.0 OPERATION OF THE SERIAL INTERFACE SECTIONS

When the stop bit in the command register is cleared and the start bit is set, the transmit and receive sections are enabled. This permits the serial interface sections to recognize incoming frames and to act on requests for transmitting frames. Once enabled, the serial interface sections remain enabled until the stop bit is set. Clearing the start bit does not disable the serial interface.

If the stop bit is set while the transmit and receive sections are operational, they will finish handling the current frame, then go to a soft reset condition and ignore incoming frames and requests for transmission. Before the transmitter stops, however, it will complete the retransmission of any colliding packets. When both sections are stopped, the RST bit in the interrupt status register is set (although the DMA controller may remain active), and the receiver status registers are reinitialized.

3.1 RECEIVE FUNCTIONS

This section describes how the receiver section operates.

3.1.1 RECEIVING A FRAME

The preamble field is used to train the external Manchester decoder and to detect carrier. If carrier sense (CRS) is true, the preamble passes through the receive deserializer which discards it while searching for the consecutive "1" bits that mark the start-frame-delimiter (SFD). The deserializer loads the receive FIFO with octets (bytes), beginning with the first bit after SFD.

While the destination address (DA field) is being checked for recognition, the receive DMA is disabled. If the frame is accepted, the DMA is enabled, and when the FIFO fills to the programmed burst level, transfer to memory begins. If the frame's address is not accepted, the receive unit clears out the FIFO and waits for the start of the next frame.

The destination address, source address, and data fields are passed to buffer memory. In some protocols, the first 2 bytes of the data field denote a frame length. These bytes are not interpreted by the WD83C690, but treated as ordinary data.

3.1.2 END OF FRAME

Upon loss of carrier sense, dribble clocks (receive clocks that occur after the loss of carrier) on the RXC pin flush the remainder of the received frame through the deserializer and CRC checker. The CRC of all received octets is computed and compared to the CRC at the end of the frame, and the result is recorded in the receiver status register. The CRC from each received frame is sent to memory with the frame via DMA, and included in the byte count posted in the buffer header.

The deserializer counts the number of bits left over after the last complete octet. If the number is greater than 6, a frame alignment error is reported.

If the receive unit detects errors in the frame, it may abort reception, depending on how the bits, "save errored packets" and "accept runt frames", have been configured. If reception is aborted, the DMA controller stops sending bytes to the buffer, the receive unit clears out the FIFO, the receive status register (RSR) and the interrupt status register (ISR) are updated, and the receive unit waits for the next frame to begin.

For frames that are not accepted, a header is not posted, and the previous contents of the header location remain unchanged. We recommend that the header portions of recycled buffers be cleared out so that they are not subject to misinterpretation during subsequent host processing.

The received packet length must be less than 65,024 bytes, including DA, SA, data, and CRC. In addition, the buffer ring must have enough space for the entire frame and a 4-byte header. Packets larger than the available buffer space cannot be received, regardless of the SEP bit in the RECEIVE CONFIG register. Such frames are posted as ring over-writes and cause the over-write (OVW) interrupt to be set. Receiver interrupts (RXE, PRX) are posted after the frame has been completely posted to memory by DMA. If DMA aborts, these interrupts are not set for the current frame (if set previously, they remain unchanged). Packets shorter than 64 bytes are received only when the "accept runts" bit is enabled.

3.2 TRANSMITTER

This section describes how the transmitter section operates.

3.2.1 INITIALIZATION FOR TRANSMISSION

The host builds packets to be transmitted in buffer memory. These packets must include the DA, SA and data fields. CRC is not read from buffer memory unless CRC generation is disabled. If it is disabled, the user is expected to place the computed CRC in the last four bytes of memory with the bit order reversed so that when clocked out least significant bit first, the CRC is presented to the serial interface most significant bit first.

The transmit start and transmit length (TSTART and TLENGTH) registers must be properly programmed before the TXP bit in the command register is set by the host. Once the TXP bit is set, the transmit unit can request the frame from the TRDMA unit. TXP can be cleared only by the transmitter upon completion of an attempted transmission.

3.2.2 TRANSMISSION PROCESS

TRDMA fills the transmit FIFO with bursts of data until there is no room left for an entire data burst. Burst lengths of 2, 4, or 8 bytes are repeated until they result in a full FIFO. A burst length of 12 bytes stops TRDMA and leaves only 12 bytes in the FIFO. When all bursts are done, TRDMA notifies the transmit unit that the FIFO is ready for transmission to begin.

The transmit unit waits until the media is clear for transmission, then generates 62 bits of preamble and SFD. Following this operation, it pulls bytes out of the transmit FIFO, serializes them, shifts their bits to the TXD pin, and computes the packet's CRC. During this operation, the TRDMA monitors the condition of the FIFO to determine when there is room for other bursts of data. As soon as there is room, additional bursts are performed.

When the DMA has filled the transmit FIFO with the last byte of the packet, it sets a flag. The transmitter continues to pull data out of the FIFO until it becomes empty, which marks the end of the frame. CRC computation stops and the CRC is appended serially to the frame, most significant bit first.

3.2.3 TRANSMIT UNDERRUN

If the FIFO becomes empty before the internal flag is set, a transmit underrun condition results and a transmit error is posted. Transmission of the packet is aborted and an interrupt may be generated.

3.2.4 COLLISIONS

When a collision is reported on the COL pin, the transmitter sends thirty-two "1" bits as a jam signal, terminates transmission, then tries again (up to 16 times).

If there are fewer than 16 retries, the transmitter randomly selects a backoff delay, in slot-time units, from the range, $0 \leq R < 2^K$ (where K is 10 or the number of retries, whichever is less). The transmitter requests retransmission of the frame from memory and delay is initiated. Note: in accord with the 802.3 specifications, the carrier sense is ignored during the last third of the interframe gap.

When retransmitting a frame, the DMA controller clears out the transmit FIFO, loads its pointer to the start of the frame in memory, and waits for the abort signal to subside. The FIFO is then loaded in the same manner as it was initially. If the maximum number of collisions (16) is exceeded, transmission is aborted without further retries or back-off delay.

3.2.5 EXTENSIONS TO THE 802.3 10base5 PROTOCOL

The 802.3 10base5 protocol uses frame lengths between 64 and 4096 bytes, inclusive. The transmitter section can send frames containing more than 16 and fewer than 65,276 bytes in length. The ability to transmit shorter or longer frames may be useful in other variations of the 802.3 protocol.

To support these variations, the slot time is program-selectable (the choices are 256-, 512-, or 1024-bit times).

4.0 MEMORY INTERFACE

As previously noted, the DMA channel generates a 16-bit linear address which can be used with a static 8-bit upper address stored in a page register. This enables the WD83C690's 64-Kbyte address space to be positioned on any 64-Kbyte boundary within the host's 16-Mbyte address space.

4.1 MEMORY ACCESS TIME

Once granted control of the memory bus, the DMA channel can perform memory accesses in as little as 200 nsec. The actual cycle time depends on the number of wait states requested by memory. Wait states add 50 nsec each to the cycle time. For systems in which memory access time is known at design time, a choice of 0, 1, 2, or 3 automatic wait states can be programmed into the enhancement register. Automatic wait states apply to all memory cycles, regardless of the direction in which the data is moving.

Wait states are also inserted when the MEMRDY line is pulled high, even if the automatic wait states have expired.

4.2 DMA BURSTS

To economize on arbitration time, the TRDMA channel collects transfers into bursts of 2 bytes (1 word), 4 bytes (2 words), 8 bytes (4 words), or 12 bytes (6 words). The choices provide a trade-off between bus latency and efficiency. The same burst length applies to transmit and receive operations.

When a data burst is required, the BREQ line requests the memory bus. An external arbitrator drives BGRANT high, enabling the address pin drivers, and a multiplexed address is driven onto the bus. An ALE signal coordinates the external address latches. Data is then either driven out or read in. In byte mode operation, the evenly-addressed byte is always accessed first.

Provided that the BGRANT line remains high, the entire burst proceeds as back-to-back cycles without relinquishing the bus. The DMA controller, however, can be preempted on a word boundary by removing BGRANT. On completion of the present word transfer (or second byte of a paired-byte transfer), the WD83C690 tri-states its address and data drivers and suspends DMA operations. (While DMA is suspended, the device's registers can be accessed.) When BGRANT is asserted again the DMA process picks up where it left off.

Be careful when preempting DMA bursts. If memory is not regained soon enough, FIFO overflow or underrun can result.

4.3 TRANSMIT PACKET BUFFERING

A packet to be transmitted is placed by the host into buffer memory. The packet must include the DA, SA, and data fields. The preamble, SFD, and (normally) CRC are not included in the buffer. If CRC generation is suppressed, the CRC field for the packet is also supplied by the host. The packet is placed in a contiguous block of memory, starting on a 256-byte boundary.

Valid 802.3 packets have at least 48 bytes of data. If data with fewer bytes are to be transmitted on an 802.3 network, it is the host's responsibility to build a packet with pad data included. The WD83C690 can transmit frames of any programmed length, even those which are too short to be valid frames on an 802.3 network.

TRDMA transfers the number of bytes programmed into the transmit frame length high-and low-byte (TCNTH, TCNTL) register pair, starting from the address, TSTART, 00.

4.4 RECEIVE PACKET BUFFERING

All received packets are stored in a circular set of 256-byte buffers. The values written into the receive start and receive stop page registers (RSTART and RSTOP) by the host when the WD83C690 is initialized determine the number and location of the buffers in the ring. RSTART points to the first buffer in the ring, and RSTOP points to the buffer after the last one in the ring.

Each packet received is stored in one or more of these buffers, with a 4-byte header inserted at the start of the first buffer. Figure 4-1 illustrates the format of a received packet in memory.

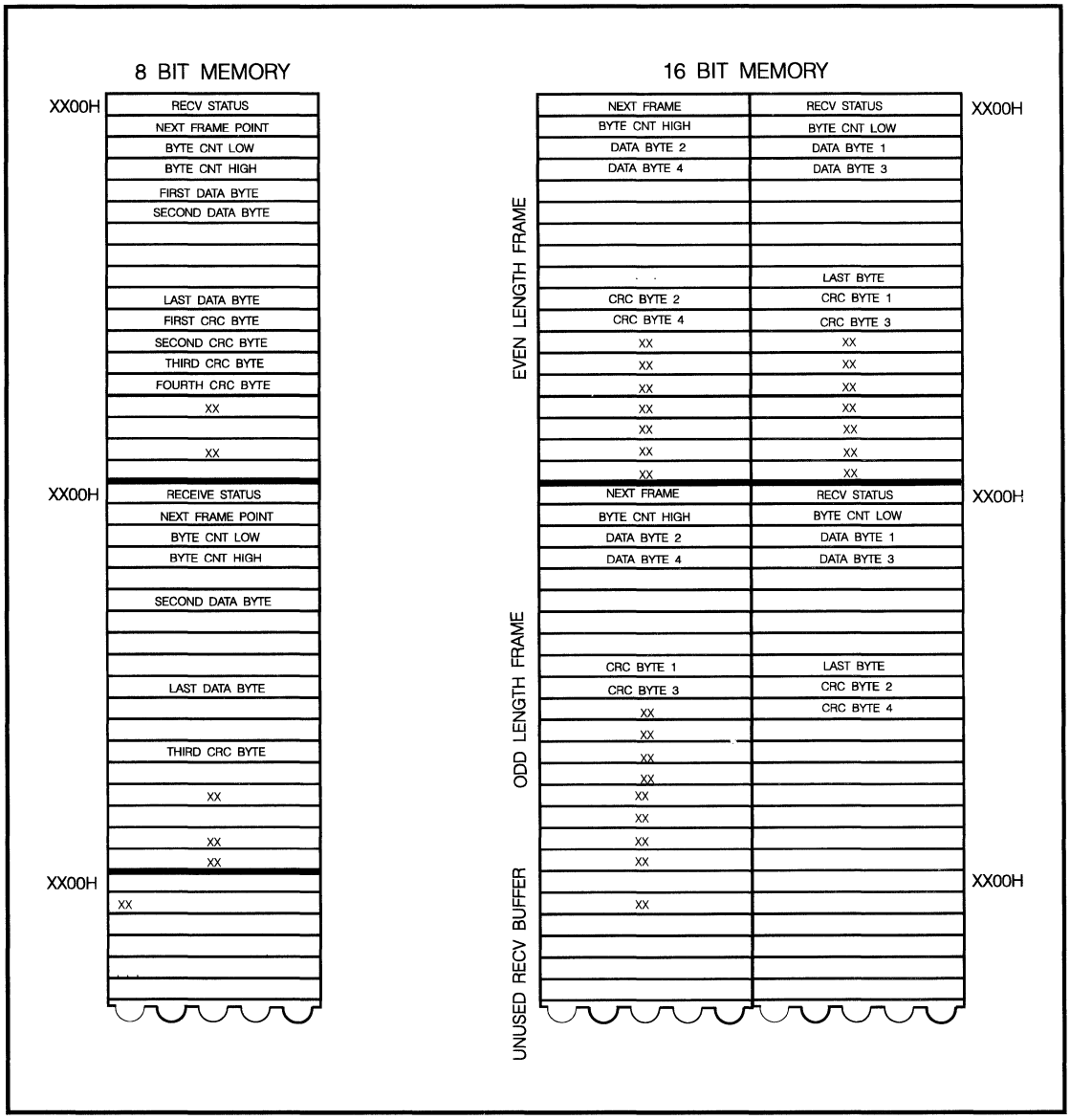

FIGURE 4-1. RECEIVER BUFFER FORMAT

Frames that extend to the buffer pointed to by RSTOP are continued in the buffer pointed to by RSTART. RSTOP can be either greater than RSTART + 1 or less than RSTART. Making RSTOP equal to RSTART or RSTART + 1 leads to unpredictable results. The relationship of these registers to ring placement in memory is illustrated in Figure 4-2.

Up to 254 buffers can be allocated to the ring. The receiver DMA uses as many as required to store a packet. This enables you to configure the device to receive frames nearly as long as 64K bytes, a

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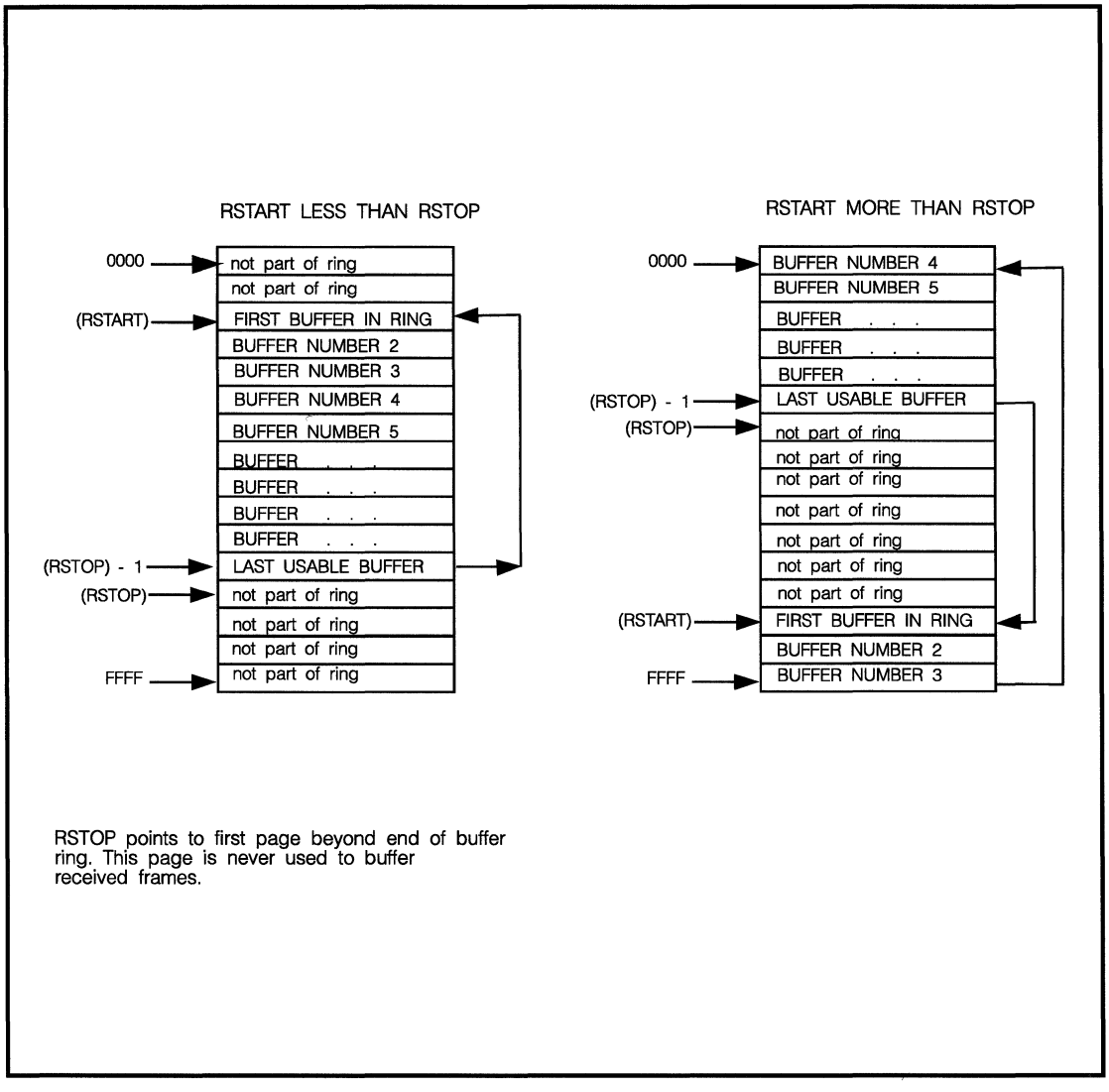

FIGURE 4-2. RECEIVER BUFFER STRUCTURE

feature that may be useful in customized CSMA networks.

The receive DMA uses two additional registers to manage the buffer ring: the current (CURR) page register and the boundary (BOUND) page register. CURR points to the first buffer that is not part of a completely-received packet. When TRDMA is storing a frame, for example, CURR points to the start of the frame being stored. When TRDMA is not storing a frame, CURR points to the first buffer that will be used for the next frame to be received.

The receive boundary page register (BOUND) protects received frames from being overwritten by later frames. It points to the first buffer in the ring that is not to be overwritten. When the receive DMA process attempts to open the buffer pointed to by BOUND, reception is aborted and the overwrite (OVW) flag in the receiver status register is set.

Normally, BOUND is set up to point to the oldest received packet in the ring. The pointer is managed by the host. To discard an unwanted frame, the host simply rewrites BOUND to point to the next packet. To prevent misinterpretation of the discarded packet as a received packet, it is advisable to write zeros into the first word.

CURR is updated by the receive DMA after a frame is received. Conversely, BOUND is updated by host software after data is removed from the ring. When the last frame has been removed from the ring buffer, BOUND has the same value as CURR, and the ring is considered empty by the WD83C690.

The WD83C690 distinguishes between empty, full, and partially-filled buffer rings on the basis of the BOUND and CURR pointer values. Whenever BOUND is not equal to CURR, the buffer ring is assumed to be partially filled, starting with the buffer pointed to by BOUND and ending with the buffer prior to that pointed to by CURR.

When BOUND equals CURR, the ring is full only if CURR was changed by the TRDMA controller more recently than BOUND was changed by the host. When BOUND is changed more recently than CURR, the ring is considered empty.

Note: you can initialize BOUND and CURR to point to any buffer within the ring, for example RSTART. Because RSTOP is outside the ring, the registers should not point to RSTOP. (This would result in the TRDMA storing frames outside the ring in an unpredictable manner.)

Provided the buffer is in the ring, you can give BOUND and CURR the same value. Figure 4-3 illustrates the relationship between pointers in a typical initialized ring. Figure 4-4 shows a ring that has received a few frames (this is its normal condition), and Figure 4-5 shows the same ring after proper removal of the oldest received packet. Figure 4-6 shows a ring that is completely full, and Figure 4-7 shows a ring on the verge of overflow.

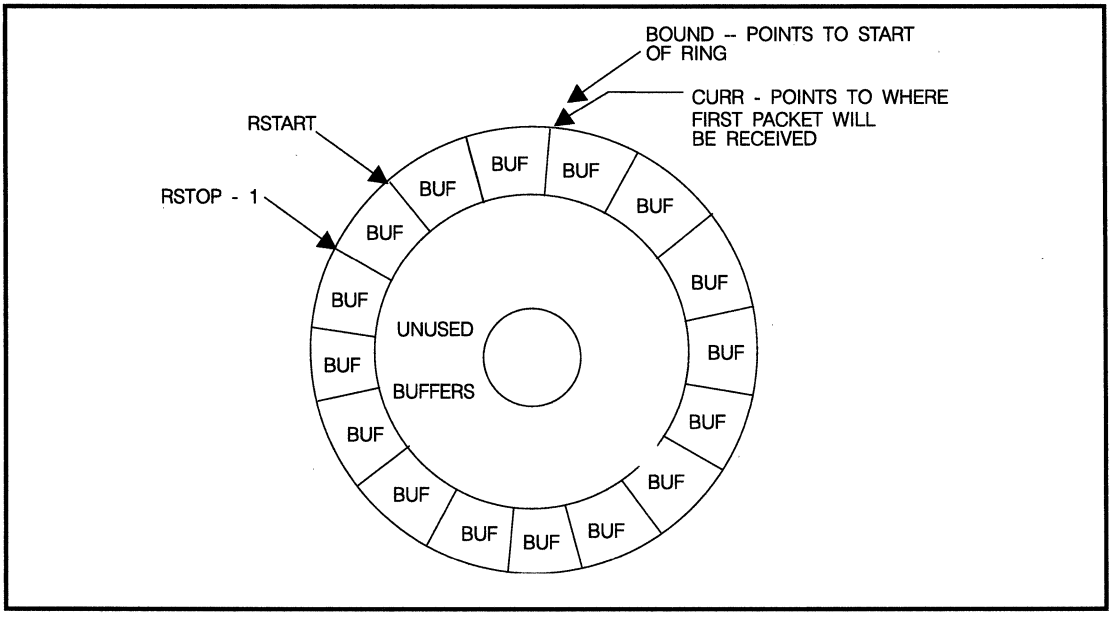

FIGURE 4-3. RECEIVER BUFFER RING,TYPICAL SETUP CONFIGURATION

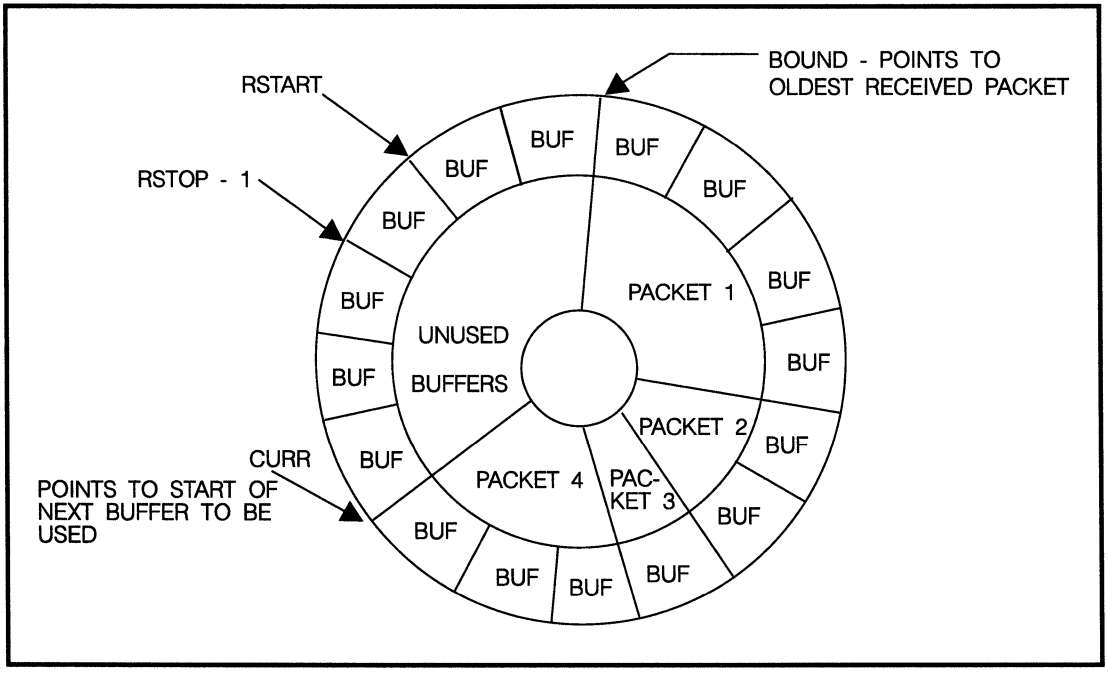

FIGURE 4-4. RECEIVER BUFFER RING, TYPICAL OPERATING CONFIG.

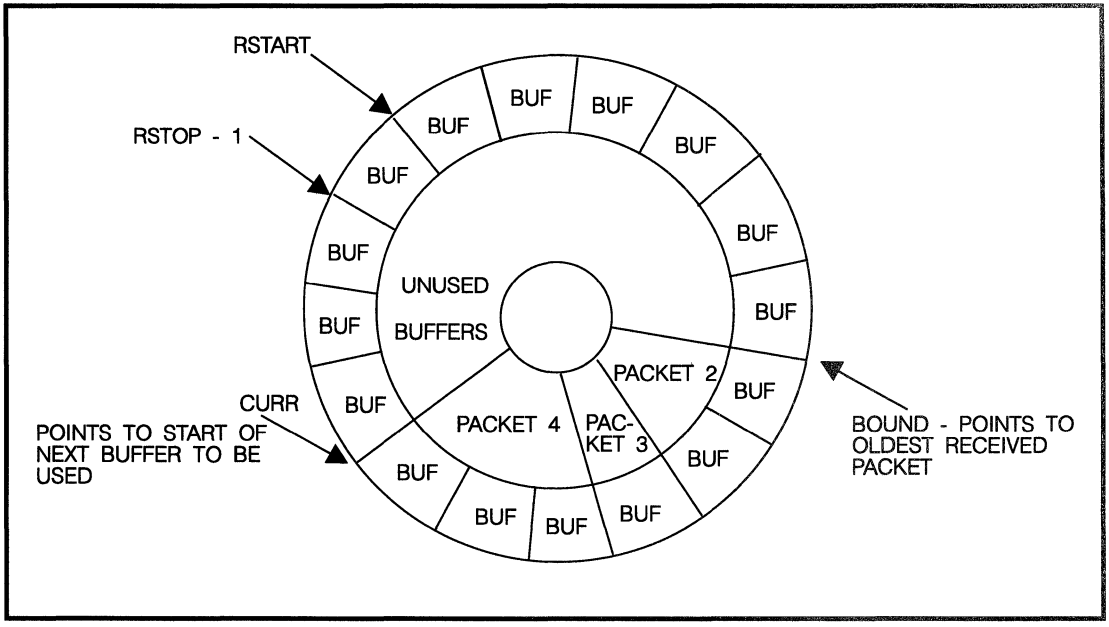

FIGURE 4-5. SAME BUFFER RING, AFTER REMOVING ONE PACKET

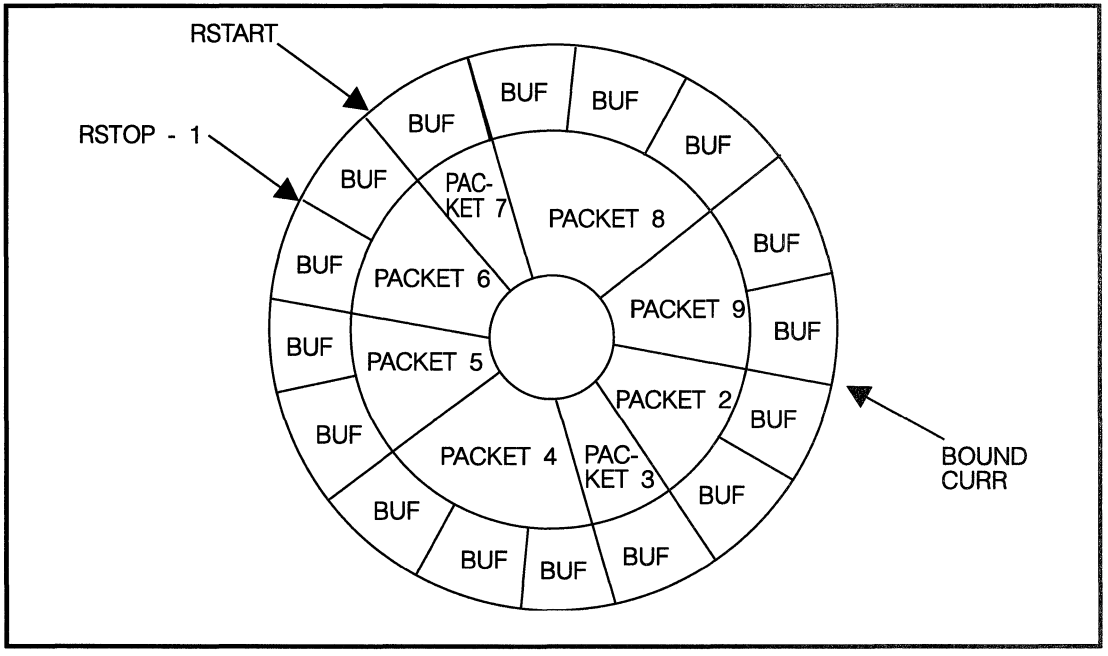

FIGURE 4-6. FULL RECEIVER BUFFER RING, NO OVERFLOW

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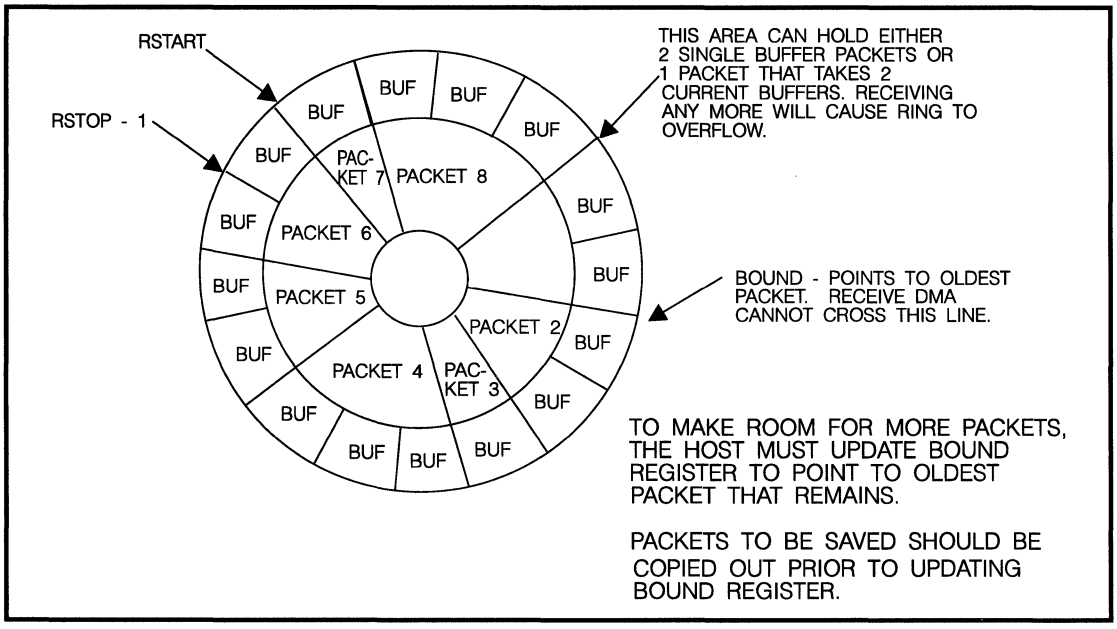

FIGURE 4-7. RECEIVER BUFFER RING VERGING ON OVERFLOW

A.0 APPENDIX A

A.1 HARDWARE CHARACTERISTICS

FEATURE	CHARACTERISTERIC(S)
Package	PLCC-68
Supplies	Single 5V supply
Technology	CMOS
IEEE 802.3 compatibility	Yes
Individual addresses	Filters completely
Group addresses	No filter; only enable/disable
Broadcast address	Enable/disable
Collision detection	External input
Buffer block size	Fixed at 256 bytes
Transmit buffers	One frame, contiguous blocks
Receive buffers	Circular buffer Many frames 65 Kbyte maximum frame size
DMA channel	Transmit/receive 8/16 bit data Full duplex operation Muxed address/data Interruptible bursts Programmable wait states Programmable burst size
Memory addressing	64 Kbyte buffer region within 16 Mbyte address space.
Loopback	Full duplex –allows reception of entire frame.
Clock relationships	Device and transmit clocks must be synchronous. RXC is asynchronous.
Clock frequency	Device clock must be 20 MHz. RXC and TXC may be 1,2, or 10 MHz.

TABLE A-1. SUMMARY OF HARDWARE CHARACTERISTICS

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B.0 APPENDIX B

B.1 REGISTER DESIGNATIONS

REG ADDR	PAGE 0 READ	PAGE 0 WRITE	PAGE 1 READ	PAGE 1 WRITE
0	COMMAND	COMMAND	COMMAND	COMMAND
1	TRINCRL	RSTART	STA0	STA0
2	TRINCRH	RSTOP	STA1	STA1
3	BOUND	BOUND	STA2	STA2
4	TSTAT	TSTART	STA3	STA3
5	COLCNT	TCNTL	STA4	STA4
6	–	TCNTH	STA5	STA5
7	INTSTAT	INTSTAT	CURR	CURR
8	–	–	–	–
9	–	–	–	–
A	–	–	–	–
B	–	–	–	–
C	RSTAT	RCON	–	–
D	ALICNT	*TCON	–	–
E	CRCCNT	*DCON	–	–
F	MPCNT	INTMASK	–	–

TABLE B-1. REGISTER ADDRESSES

*Register contains new or modified bits.

REG ADDR	PAGE 2 READ	PAGE 2 WRITE	PAGE 3 READ	PAGE 3 WRITE
0	COMMAND	COMMAND	COMMAND	COMMAND
1	RSTART	*TRINCRL	*TEST	*TEST
2	RSTOP	*TRINCRH	–	–
3	–	–	–	–
4	TSTART	–	–	–
5	NEXT	NEXT	–	–
6	*BLOCK	*BLOCK	–	–
7	*ENH	*ENH	–	–
8	–	–	–	–
9	–	–	–	–
A	–	–	–	–
B	–	–	–	–
C	RCON	–	–	–
D	*TCON	–	–	–
E	*DCON	–	–	–
F	INTMASK	–	–	–

TABLE B-1. REGISTER ADDRESSES (Continued)

*Register contains new or modified bits.

Name:	**R/W Addr:**
ALICNT	OD/–

Description: This register is the alignment error counter. It is incremented by the receive unit when a packet is received with a frame alignment error. Only packets whose address is accepted are included in the tally. The counter increments to 255, then stops. It clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
BLOCK	26/26

Description: This is a page register for the upper 8 bits of memory address. During each memory/transfer cycle, the contents of this register are driven out onto the A16-A23 pins, which are not multiplexed and need not be latched by the host system.

MSB	7	6	5	4	3	2	1	0
NAME	A23	A22	A21	A20	A19	A18	A17	A16
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
BOUND	03/03

Description: To prevent overflow in the buffer ring, the receive boundary page register points to the oldest used receive buffer. TRDMA compares the contents of this register to the next buffer address when linking together buffers to store a received frame. If the contents match the next buffer address, the TRDMA operation is aborted. Because all buffers are aligned on 256-byte boundaries, only A08–A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
COLCNT	05/–

Description: This register contains the number of collisions detected during attempted transmission of the current (or most recent) packet. It is cleared at the start of transmission. For each collision encountered, the count is incremented. If no collisions are detected, the counter reads zero. If more than 15 collisions occur, the abort bit of TSR is set and the count is reset to zero.

MSB	7	6	5	4	3	2	1	0
NAME	0	0	0	0	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS

Name:	R/W Addr:
COMMAND	x0/x0

Description: The command register is used to initialize the device, start transmissions, and switch pages.

MSB	7	6	5	4	3	2	1	0
NAME	PS1	PS0	CMD.5	CMD.4	CMD.3	TXP	STA	STP
INIT	0	0	1	0	0	0	0	1

Notes:

PS1, PS0 — Page select, a two-bit field.

Bits 5,4,3 — These bits may be read and written to, but they control no hardware in the WD83C690. (They were used for remote DMA control in the National 8390.)

TXP — Transmit packet. Set this bit after loading transmit buffer and control registers to initiate transmission of a packet. The WD83C690 clears this bit upon completion, or abortion, of the transmission. The host can clear the bit by setting TESTMODE in the TEST CONTROL register and writing "0" into COMMAND.TXP. When TESTMODE is not set, writing "0" into COMMAND.TXP is ignored.

STA — Start bit. This bit is set by the user to activate the WD83C690 after power is applied or after the WD83C690 is reset. (Although the user's software should set the other registers prior to bringing the device on line, this is the actual command that allows normal operation of the transmit and receive portions of the device.) Until the register is set, no frames can be sent or received. Once set, this bit may be cleared and the WD83C690 will continue to remain online.

STP — Stop bit. Set this bit to stop the device via the software. The bit takes the device offline from the LAN. Frames partially transmitted or received are completed before reset occurs. ISR.RST is set high when the transmit and receive sections have completed all outstanding operations. No frames will be received until the start bit is set. Receiver status reqs are reinitialized when this command is executed.

Name:	R/W Addr:
CRCCNT	0E/–

Description: This register is the CRC error counter. It is incremented by the receive unit when a packet is received with a CRC error. Only packets whose address is accepted are included in the tally. The counter stops at 255, and clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

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Name:	**R/W Addr:**
CURR	17/17

Description: This register points to the first buffer used to store the current frame. It is used internally by TRDMA to facilitate the storage of buffer header information, and to provide a backup address for recovering buffers in case of a flawed packet. The register should be initialized after the device has been reset and thereafter not altered by the user unless the ring overflows. Note: Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
DCON	2E/0E

Description: The data configuration register defines characteristics of the memory interface.

MSB	7	6	5	4	3	2	1	0
NAME	–	BSIZE1	BSIZE0	–	–	–	–	BUS16
INIT	0	0	0	0	0	0	0	0

Notes:

BSIZE1,0 This two-bit field determines the length of DMA bursts and the FIFO threshold at which they are triggered. As a rule, each FIFO triggers its DMA when there is adequate room for an entire burst to fit in.

TRANS

BSIZE1	BSIZE0	BURST	RECV TRIG LEVEL	TRIG LEVEL
0	0	2 bytes	R≥2	T≤4
0	1	4 bytes	R≥4	T≤12
1	0	8 bytes	R≥8	T≤8
1	1	12 bytes	R≥12	T≤4

Bits 7,4,3,2,1 Not used.

BUS16 "1" tells the WD83C690 to make all DMA transfers 16 bits wide. "0" tells the WD83C690 to make all DMA transfers 8 bits wide.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name: ENH **R/W Addr:** 27/27

Description: This register enables features that are unique to the WD83C690.

MSB	7	6	5	4	3	2	1	0
NAME	WAIT1	WAIT0	–	SLOT1	SLOT0	–	–	—
INIT	0	0	0	0	0	0	1	0

Notes:

WAIT1
WAIT0 This two-bit field defines the default number of wait states the WD83C690 inserts into every DMA cycle.

WAIT1	WAIT0	WAIT STATES
0	0	0
0	1	1
1	0	2
1	1	3

SLOT1,
SLOT0 This two-bit field selects the slot time according to the following table.

SLOT1	SLOT0	SLOT TIME
0	X	512 bit times – Ethernet, StarLAN
1	0	256 bit times
1	1	1024 bit times

Name: INIT MASK **R/W Addr:** 2F/0F

Description: This register is used to selectively mask interrupt sources. Mask bits that are "1" allow the corresponding interrupts to cause an IRQ. Mask bits that are "0" block interrupt sources.

MSB	7	6	5	4	3	2	1	0
NAME	–	XDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

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Name:	**R/W Addr:**
INT STATUS	07/07

Description: This register enables the host to determine the cause of an interrupt and to evaluate pending or masked interrupts (which are visible in this register even though they do not generate an IRQ). Pending interrupts can be cleared by writing "1" into the associated bit of this register. The IRQ signal is active as long as any unmasked interrupt bit remains set.

MSB	7	6	5	4	3	2	1	0
NAME	RST	–	CNT	OVW	TXE	RXE	PTX	PRX
INIT	1	0	0	0	0	0	0	0

RST — Reset status. This bit, which does not generate an interrupt, is set by the WD83C690 when its transmit and receive sections are stopped in response to assertion of the RESET pin or the CMD.STP bit.

BIT 6 — This bit is unused in the WD83C690. It always returns 0 when read.

CNT — The counter overflow bit indicates that the MSB of one or more network error counters has been set.

OVW — The overwrite warning bit is set when the receive DMA attempts to write into the buffer pointed to by the boundary register.

TXE — Transmit error is set when there are excessive collisions, or when FIFO underrun prevents a packet from being transmitted.

RXE — Receive error is set when a packet is received with one or more of the following errors:

- CRC error
- Frame alignment error
- FIFO overrun
- Missed packet (monitor mode)

This interrupt is not posted if DMA abort occurs. (OVW interrupt indicates that condition.) If, however, the interrupt has been previously set, it will not be changed due to OVW.

PTX — Packet transmitted indicates that a packet was successfully transmitted.

PRX — Packet received indicates that a packet was received with no errors. This interrupt is not posted if DMA abort occurs. If previously set, it will not be changed due to OVW.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
MPCNT	0F/–

Description: This register is the missed packet error counter. It is incremented by the receive unit when a packet cannot be received due to a lack of receive buffers, receive FIFO overflow, or because the receiver is in monitor mode. Only packets whose address is accepted are included in the tally. The counter stops at 255, and clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
NEXT	25/25

Description: This is a working register of the TRDMA controller. It holds a pointer to the next buffer to be opened.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
RCON	2C/0C

Description: The receive configuration register defines optional behavior of the receive unit. It controls both address recognition and the acceptance of abnormal packets. These bits can be set independently, although monitor mode takes precedence over the others.

MSB	7	6	5	4	3	2	1	0
NAME	–	–	MON	PROM	GROUP	BROAD	RUNTS	SEP
INIT	0	0	0	0	0	0	0	0

Notes:

MON — When set, this bit enables the receive unit to check addresses and CRC on incoming packets without buffering them to memory. The missed packet counter is incremented for each recognized packet. Under normal operation, this bit is cleared to "0".

PROM — When set to "1", this bit enables promiscuous reception of all frames having individual addresses.

GROUP — Setting this bit enables reception of all frames destined to multicast (group) addresses other than broadcast frames.

BROAD — Setting this bit enables reception of all frames having a broadcast destination address.

RUNTS — Setting this bit enables the WD83C690 to receive frames with fewer than 64 bytes, provided they meet the other requirements of the IEEE 802.3 protocol.

SEP — Setting the saved error packets bit to "1" causes the receive unit to save packets having CRC or frame alignment errors in the buffers.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	**R/W Addr:**
RSTART	21/01

Description: The receive start page register points to the start of the receive buffer ring. Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
RSTAT	0C/–

Description: The receive status register reports the status of the most recently received packet, categorizing any errors detected. At the start of reception, all bits are cleared except DIS.

MSB	7	6	5	4	3	2	1	0
NAME	DFR	DIS	GROUP	MPA	OVER	FAE	CRC	PRX
INIT	0	0	0	0	0	0	0	0

DFR — The deferring bit is set when the interframe gap state machine is deferring. If the transceiver asserts the CD line as a result of jabber, this bit remains set, indicating a jabber condition.

DIS — The receiver disabled bit is set when the receiver is in monitor mode. It is cleared when the receiver leaves monitor mode.

GROUP — This bit is set when the address is a group address (multicast) or broadcast. It is cleared to indicate an individual (physical) address match.

MPA — The missed packet address is set when a packet intended for this station cannot be accepted by the device due to a lack of receive buffers or because the device is in monitor mode. The missed packet counter is also incremented when this occurs.

OVER — The FIFO overrun bit is set when the receiver attempts to write into a FIFO that is already full. This can occur when the TRDMA fails to keep up with the received data.

FAE — A frame alignment error indicates that the incoming packet did not end on a byte boundary and the CRC did not match at the last byte boundary. Frames having 7 dribble bits are reported as alignment errors. The alignment error counter is incremented when this condition occurs.

CRC — When set, this bit indicates that the frame's computed CRC did not correspond to the CRC appended to the end of the frame. This error also causes the CRC counter to be incremented.

PRX — When the packet received intact bit is set to "1, it indicates that a packet was received without error. (This means that CRC, FAE, OVER, and MPA all equal 0.)

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
RSTOP	22/02

Description: Prior to wrapping around to the RSTART buffer, the receive stop page register points to the last receive buffer in the ring. Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
STA 0	11/11
STA 1	12/12
STA 2	13/13
STA 3	14/14
STA 4	15/15
STA 5	16/16

Description: These six registers contain the node's individual station address.

STA0:	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DALSB
STA1:	DA15	DA14	DA13	DA12	DA11	DA10	DA09	DA08
STA2:	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
STA3:	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
STA4:	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
STA5:	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Name:	R/W Addr:
TCNT H	–/06
TCNT L	–/05

Description: Together, the transmit frame length high- and low-byte registers hold the byte count for the frame to be transmitted. The byte count includes the DA, SA and data fields. If CRC generation is inhibited, the count also includes the CRC field in the buffer.

TCNT H:

MSB	7	6	5	4	3	2	1	0
NAME	L15	L14	L13	L12	L11	L10	L09	L08
INIT	0	0	0	0	0	0	0	0

TCNT L:

MSB	7	6	5	4	3	2	1	0
NAME	L7	L6	L5	L4	L3	L2	L1	L0
INIT	0	0	0	0	0	0	0	0

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TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name: TCON — **R/W Addr:** 2D/0D

Description: The transmit configuration register controls loopback options, data rate options, and Manchester codes.

MSB	7	6	5	4	3	2	1	0
NAME	TCON7	TCON6	TCON5	TCON4	TCON3	LB1	LB0	CRCN
INIT	0	0	0	0	0	0	0	0

Notes:

TCON7,6,5,4,3 These bits are writable and readable, but have no function in the WD83C690. They are reserved for future enhancements.

LB1,LB0 This two-bit field is for selecting loopback options.

LB1	LB0	OPERATION
0	0	Normal (no loopback)
0	1	Internal loopback just inside WD83C690 pins
1	0	External loopback with LOOP pin high
1	1	External loopback with LOOP pin low

CRCN Setting this bit inhibits generation of CRC during transmission of the frame. The user is responsible for calculating the frame's CRC and placing it in the buffer so that, when the last 4 bytes of the buffer are shifted out, they form the correct CRC for the frame. Note that the serializer shifts bytes out of LSB first, whereas the CRC shifts bytes out of MSB first.

The operation of the receiver is unaffected by this bit.

Name: TEST — **R/W Addr:** 31/31

Description: This register, which is reserved, enables various internal test modes of the WD83C690, as well as host access to sensitive internal registers. It is important that you do not write to this register.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
TRINCRH	02/22
TRINCRL	01/21

Description: This register pair is the address incrementer for the TRDMA unit. Its value approximates the memory address associated with the next TRDMA operation. The information is approximate because the LSB of the address is not accessible when operating in 8-bit bus mode. Additional uncertainty arises because of an internal one-word-deep address pipeline in the memory data transfer logic.

The address obtained from these registers is usually the address of the lower half of the word just transferred, or the address of the lower half of the word to be transferred next. The word address applies even when the bus is being operated byte-wide.

If these registers are read during the beginning or end of either transmission or reception, meaningless values may be obtained. The incrementer is used for pointer update and length modification calculations during these periods.

TRINCR H:

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	1	1	1	1	1	1	1	1

TRINCR L:

MSB	7	6	5	4	3	2	1	0
NAME	A07	A06	A05	A04	A03	A02	A01	A00
INIT	1	1	1	1	1	1	1	1

Name:	R/W Addr:
TSTART	24/04

Description: The transmit start page register points to the assembled packet to be transmitted. Because all frames are assembled on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	**R/W Addr:**
TSTAT	04/–

Description: The transmit status register reports events that occur on the media while a packet is transmitted. All bits are cleared prior to transmission of a packet and set as needed.

MSB	7	6	5	4	3	2	1	0
NAME	OWC	CDH	UNDER	CRL	ABORT	TWC	NDT	PTX
INIT	0	0	0	0	0	0	0	0

Notes:

OWC	The out-of-window-collision bit is set if a collision is detected more than one slot time after transmission begins. The transmission is not aborted when this occurs.
CDH	This is the collision detect heartbeat bit. It is set when heartbeat is detected.
UNDER	The FIFO underrun bit it set when the transmit unit attempts to read from an empty FIFO prior to receiving the TDONE flag from TRDMA. It means that the FIFO failed to supply enough data for the serializer to maintain the generation of a frame.
CRL	The carrier sense lost bit is set when the carrier is lost while a packet is being transmitted. Carrier sense is monitored from its rising edge at the start of the outgoing frame's echo. Transmission is not aborted upon loss of the carrier, but the event is reported for statistical purposes.
ABORT	This bit is set if the transmission is aborted because of excessive collisions.
TWC	The transmitted-with-collisions bit is set when a transmitted frame collides (at least once) with another frame.
NDT	The non-deferred transmission bit is set when the frame is transmitted successfully without deferring. A deferred transmission can occur only the first time an attempt is made to send a packet. Collisions are not deferred transmissions.
PTX	The packet transmitted bit is set to indicate (1) transmission of a packet without excessive collisions or (2) a FIFO underrun.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

C.0 APPENDIX C

C.1 PIN DESIGNATIONS

Figure C-1 illustrates the 68-pin Ethernet controller.
Table C-1 lists all pin designations.

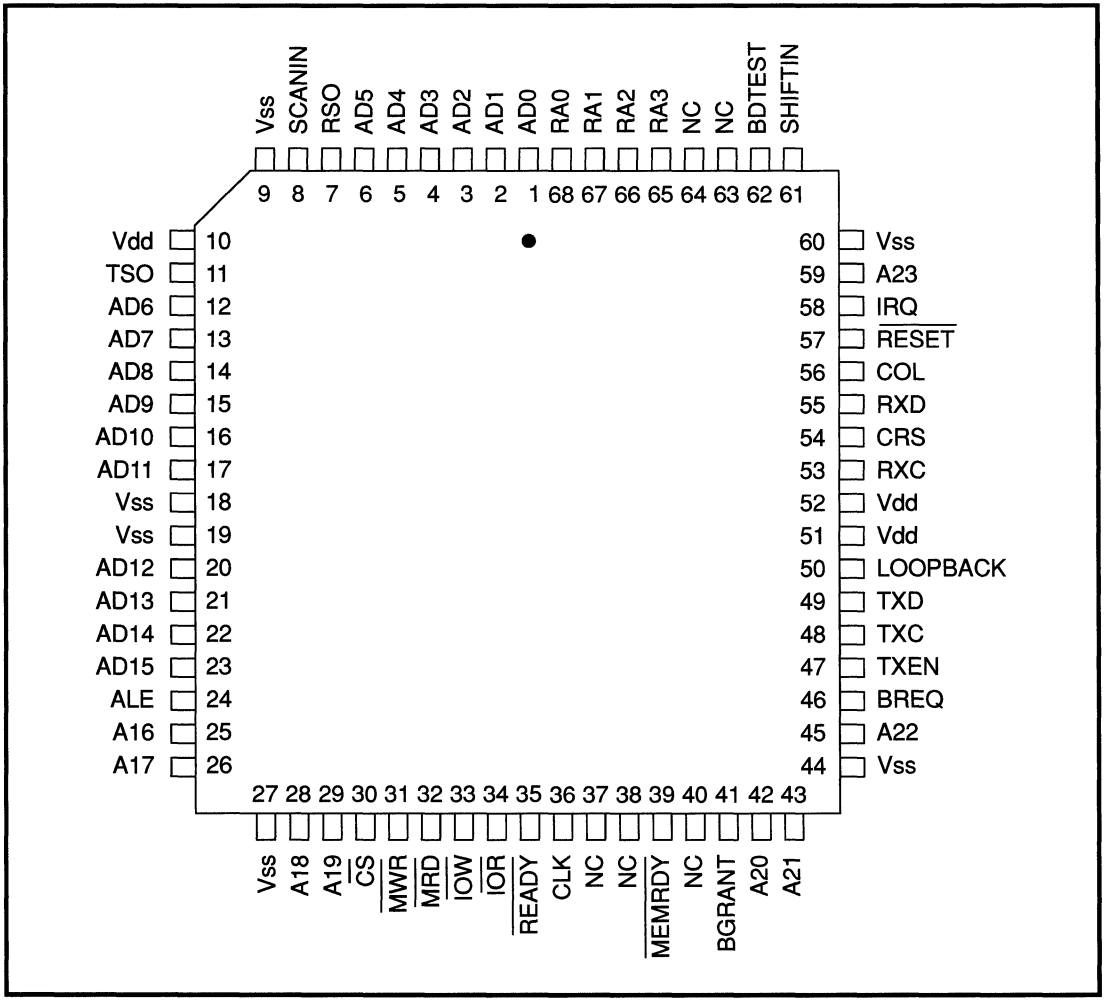

FIGURE C-1. 68-PIN ETHERNET CONTROLLER

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PIN	DIR	NO.	DESCRIPTION
A16 A17 A18 A19 A20 A21 A22 A23	OUT TRI	25 26 28 29 42 43 45 59	Highest address lines. These are used to define the page address for the buffer memory block. In systems having 64 Kbytes or less of local memory, they are unused. The value of these pins is programmed into the BLOCK ADDRESS register.
AD00 AD01 AD02 AD03 AD04 AD05 AD06 AD07 AD08 AD09 AD10 AD11 AD12 AD13 AD14 AD15	BIDIR TRI	01 02 03 04 05 06 12 13 14 15 16 17 20 21 22 23	Multiplexed address/data lines when internal DMA channels are active and granted access to the local memory bus. When bus access is not permitted, AD00 – AD07 become input/output pins for host data bus, and AD08 – AD15 are tri-stated.
ALE	BIDIR TRI	24	Address latch enable goes high when DMA address is driven onto AD00 - AD15. It goes low to latch address externally. When accessed by the host, this pin is an input which serves to transparently latch the RA0-3 address lines internally on the falling edge.
$\overline{\text{BDTEST}}$	IN	62	This pin tri-states the following output pins when pulled low: BREQ, IRQ, LOOPBACK, READY, RSO, TSO, TXD, TXEN. It may also be used to facilitate in-circuit testing of boards. This pin is pulled up by an internal resistor.
BREQ	OUT TRI	46	Bus request (active high). This pin goes high for the WD83C690 to request access to the local memory bus. It stays high throughout the DMA burst.
BGRANT	IN	41	Bus grant (active high). When active, the internal DMA channels drive the AD pins and strobes as needed to perform DMA transfers. When inactive, any ongoing DMA transfers are completed, and the DMA strobe pins tri-state.

TABLE C-1. PIN DESIGNATIONS

PIN	DIR	NO.	DESCRIPTION
CLK	IN	36	Master clock input for the device. Internal operation is timed relative to this clock. In normal operation, the clock must be 20 MHz.
COL	IN	56	Collision detection input (active high). This pin must be pulled low when external circuit detects collision conditions on the network.
CRS	IN	54	Carrier sensed (active high). This pin is driven by an external decoder circuit.
$\overline{CS}$	IN	30	Chip select is active low.
$\overline{IOR}$	IN	34	I/O read (active low). Internal registers can be written to when CS and IOR are active.
$\overline{IOW}$	IN	33	I/O write (active low). Internal registers can be written to when CS and IOW are active.
IRQ	OUT TRI	58	Interrupt request (active high).
LOOP-BACK	OUT TRI	50	Loopback goes high when either of the external loopback modes is programmed in the TRANSMIT CONFIGURATION register.
$\overline{MEMRDY}$	IN	39	Memory ready (active low). Memory ready is negated externally to insert wait states into DMA transfers.
$\overline{MRD}$	OUT TRI	32	Memory read strobe output for the DMA channels (active low).
$\overline{MWR}$	OUT TRI	31	Memory write strobe output for the DMA channels (active low).
RA0 RA1 RA2 RA3	IN	68 67 66 65	Register address 0,1,2,3 (active high). RA0 is the least significant. These lines combine with two bits in the COMMAND register to select an internal WD83C690 register during host I/O access to the device.
$\overline{READY}$	OUT TRI	35	Register access ready (active low) is asserted by the WD83C690 when host access to the internal register is ready.

TABLE C-1. PIN DESIGNATIONS (Continued)

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PIN NAME	DIR	NO.	DESCRIPTION
$\overline{\text{RESET}}$	IN	57	Active low. Asserting this pin forces the WD83C690 to a known (initial) state. The device remains in its initial state until the line is released.
RSO	OUT TRI	7	This pin is the data output for level-sensitive scan testing of the receiver section. The pin should be left open in board applications.
RXC	IN	53	Serial receive clock is active on its rising edge.
RXD	IN	55	Serial receive data (active high) is connected to decoded serial data from the network.
SCANIN	IN	8	This pin is used to gate the level-sensitive scanning clock during testing of the device. This pin must be left open or tied to ground in board applications.
SHIFT-IN	IN	61	This pin serves as data input for level-sensitive scan testing of the device. The pin must be left open or tied to ground in board applications.
TSO	OUT TRI	11	This pin is the data output for level-sensitive scan testing of the transmit section. The pin must be left open in board applications.
TXC	IN	48	Serial transmit clock is active on its rising edge.
TXD	OUT TRI	49	Serial transmit data (active high) is NRZ-encoded.
TXEN	OUT TRI	47	Serial transmitter enable is used to enable the LAN driver during transmission of a frame. This signal is active high.
Vdd (3)		10 51 52	+5 dc power inputs.
Vss (6)		09 18 19 27 44 60	Ground returns for power.

TABLE C-1. PIN DESIGNATIONS (Continued)

D.0 APPENDIX D

D.1 OPERATING CHARACTERISTICS

This appendix describes the dc and ac operating characteristics. Recommended operating conditiions are listed below.

D.2 RECOMMENDED OPERATING CONDITIONS

Minimum Ambient Temperature = 0°C (32°F)
Maximum Ambient Temperature = 85°C (185°F)
Minimum Vdd = 4.75V
Maximum Vdd = 5.25V

D.3 DC PARAMETERS

The input pins have the following parameters:

v_{IL}= 0.8V
i_{IL}= 50µA (except $\overline{BDTEST}$, which is 200 µA)

v_{IH}= 2.0V
i_{IH}= 50µA

AD00 – 15 have the following dc parameters:

v_{OL} = 0.4V
i_{OL}= 1.6 mA

v_{OH}= 2.7V
i_{OH}= 0.1 mA

All other outputs have the following dc parameters:

v_{OL}= 0.4V
i_{OL}= 0.8 mA

v_{OH}= 2.7V
i_{OH} = 0.1 mA

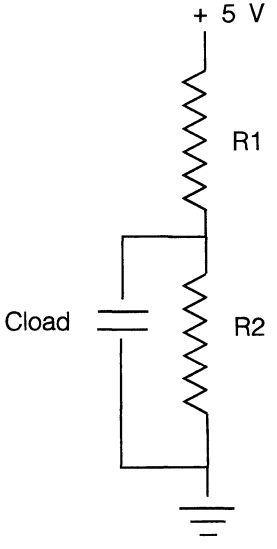
D.4 AC PARAMETERS (TIMING)

The test load for the AD00-15, MRD, and MWR outputs is:

Cload = 60 pF
R1 = 2.64 KOhms
R2 = 2.78 KOhms

The test load for all other outputs is:

Cload = 25 pF
R1 = 5.23 KOhms
R2 = 5.0 KOhms



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REF	FROM	TO	MIN	MAX	NOTES
T01	CLK	ALE	0	40	–
T02	$\overline{CLK}$	$\overline{ALE}$	0	40	–
Tre11	ALE	$\overline{ALE}$	15	–	–
T03	CLK	Valid Address AD00 – AD15	0	35	–
T04	CLK	AD00 — AD15 (– AD07) high impedance	3	45	–
Tre12	ADxx valid	$\overline{ALE}$	8	–	–
T05	$\overline{CLK}$	MRD	3	35	–
T06	CLK	$\overline{MRD}$	0	35	–
T07	CLK	MWR	0	32	–
T08	$\overline{CLK}$	$\overline{MWR}$	3	30	–
T09	$\overline{CLK}$	Valid Data AD00 – AD15	0	45	–
T10	CLK	AD00 – AD15 (– AD07) high impedance	3	45	–
T14	CLK	BREQ	0	35	–
T15	CLK	$\overline{BREQ}$	0	35	–
T16	CLK	A16-23, ALE MRD, MWR low impedance	0	35	–
T17	CLK	A16-23, ALE, MRD, MWR high impedance	0	35	–
T20	CS	READY	100	200	1*
T21	IOR or IOW	READY	50	150	1

TABLE D-1. OUTPUT TIMING

*Refer to Notes on p. 40-40.

REF	FROM	TO	MIN	MAX	NOTES
T22	CLK	READY	0	35	–
T23	CLK after IOR	AD00-07 low impedance	0	45	–
T24	CLK after IOR	Data valid	0	95	2*
T25	$\overline{IOR}$	AD00-07 high impedance	0	45	–
T26	$\overline{IOR}$ and $\overline{IOW}$	$\overline{READY}$	0	45	–
T27	CLK	TXEN or TXD	0	45	–
T28	TXEN	$\overline{TXD}$	1 CLK	1 BT	–
T29	TXC	TXD valid	0	47	–
T30	CLK	$\overline{TXEN}$	0	45	–
T31	COL	First bit of JAM	4 BT	6 BT	–
T32	End of last TXD bit	$\overline{TXEN}$	50	100	–
T33	BDTEST	Outputs high impedance	0	95	–
T34	$\overline{BDTEST}$	Outputs low impedance	0	95	–
T35	CLK	IRQ or $\overline{IRQ}$	0	45	–
T36	CLK	LOOPBACK or $\overline{LOOPBACK}$	0	45	–
T37	CLK	TSO, RSO valid	0	45	–
T38	BREQ	ALE	2	2 CLKS	3
T39	BGRANT	A16-23, ALE, MRD, MWR low impedance	2	2 CLKS	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 40-40.

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REF	FROM	TO	MIN	MAX	NOTES
T40	$\overline{\text{BGRANT}}$ $\overline{\text{BREQ}}$	A16-23, ALE, MRD, MWR high impedance	2	2 CLKS	–
T41	$\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ (last transfer)	$\overline{\text{BREQ}}$	1	4 CLKS	–
T42	ALE	Next ALE in receive DMA burst on 16-bit bus.	7	8 CLKS	4*
T43	ALE	Next ALE in transmit DMA burst on 16-bit bus	5	5 CLKS	4
T50	IOW	$\overline{\text{IOW}}$	100	–	–
T51	RXC	$\overline{\text{RXC}}$	35	–	–
T52	$\overline{\text{RXC}}$	RXC	35	–	–
T53	RXC	RXC – clock period	99	–	–
T54	RXC of first preamble bit	First RXC of SFD (preamble length)	6 BT	–	–
T55	RXC of last data bit	Last RXC prior to CRS (dribble bits)	0 BT	6 BT	–
T56	Last RXC prior to $\overline{\text{CRS}}$	Last RXC (dribble bits)	5 BT	–	–
T57	$\overline{\text{CRS}}$	CRS and Start – of Frame	27 BT	–	8
T58	TXC	$\overline{\text{TXC}}$	35	–	–
T59	$\overline{\text{TXC}}$	TXC	35	–	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 4-40.

REF	FROM	TO	MIN	MAX	NOTES
T60	TXC	TXC – clock period	2 CLKS	20 CLKS	9*
T61	$\overline{CLK}$	TXC, $\overline{TXC}$	0	30	9
T62	$\overline{TXEN}$	COL (heartbeat detect)	0	59 BT	10
T63	COL	$\overline{COL}$ (collision width)	1 BT	–	–
T64	Vdd = 4.75V	$\overline{RESET}$	10 CLKS	–	–
T65	RESET	$\overline{RESET}$	10 CLKS	–	–
T66	CLK	$\overline{CLK}$	23	800	–
T67	$\overline{CLK}$	CLK	23	800	–
T68	CLK	CLK	50	1600	9
T69	ALE	$\overline{ALE}$	15	–	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 4-40.

REF	FROM	TO	MIN	MAX	NOTES
TS01	Data Valid	CLK	15	–	–
TS02	$\overline{\text{MEMRDY}}$ or MEMRDY	CLK #2	15	–	5
TS04	BGRANT, $\overline{\text{BGRANT}}$	CLK	15	–	–
TS05	DMA pins undriven	BGRANT	0	–	–
TS06	TXC	$\overline{\text{CLK}}$	10	–	–
TS07	CS, IOR, IOW	CLK	15	–	6
TS08	RA0-3 valid	CS and (IOR or IOW)	0	–	–
TS09	RA0-3 valid	$\overline{\text{ALE}}$	15	–	–
TS10	Data valid	$\overline{\text{IOW}}$	25	–	–
TS11	CRS or $\overline{\text{CRS}}$	RXC	15	–	–
TS12	RXD valid	RXC	15	–	–
TH01	$\overline{\text{MRD}}$	Data invalid	0	–	–
TH02	CLK #2	MEMRDY, $\overline{\text{MEMRDY}}$	15	–	–
TH03	$\overline{\text{CLK}}$	TXC edge	10	–	–
TH04	$\overline{\text{IOR}}$ and $\overline{\text{IOW}}$	RA0-3 invalid	0	–	7
TH05	$\overline{\text{IOW}}$	Data invalid	10	–	–
TH06	$\overline{\text{ALE}}$	RA0-3 invalid	10	–	–
TH07	RXC	RXD invalid	15	–	–

TABLE D-2. INPUT TIMING SETUP AND HOLD REQUIREMENTS

NOTES

1. These maximum times apply if, when the device is selected, there is no ongoing DMA. When there is ongoing DMA, the maximum times apply after BREQ = 0 and BGRANT = 0.
2. This applies after the first clock for which IOR meets the setup requirement.
3. This is the delay between the time the bus is requested and internal DMA is ready to use the bus. Timing T39 is also satisfied and usually controls when DMA uses the bus.

NOTES (continued):

4. These are the minimum durations of DMA transfers on 16-bit busses. The receive transfer requires 4 cycles, plus wait states, with an interval of 3 or 4 clocks after completion of a 16-bit transfer. The transmit transfer is the same except that the interval after completion is only 1 clock. Because some versions of the device do not have this gap, we recommend that you not use the bus during the interval between the 16-bit transfers.

   There is no interval between 8-bit transfers. They require 4 cycles, plus wait states.

5. This timing must be met to control insertion of wait states.

6. To minimize the delay to READY, this timing needs to be met. Failure to meet this timing may add an extra clock delay to the onset of the READY signal, but does not adversely affect access to the device.

7. This timing applies only when ALE remains high during host access, as is the case with non-multiplexed or externally-latched addresses and data. The addresses must be stable throughout access to the device.

8. This is the time required from the end of one frame to the reception of the SFD delimiter of the next frame. The limiting factor in reception of back-to-back frames is the time required for DMA to post the header of the received frame. This depends on memory speed and on access to the bus. The interval given here is based on memory with two wait states, and the ability to access the bus within 5 clocks after request.

9. Operation of this device in an 802.3 network requires a CLK period of 50 nsec $\pm$ 0.01%. TXC must be generated synchronously from CLK. The TXC period may be 2 CLKS, 10 CLKS, or 20 CLKS.

10. The maximum time is 63 bit times from CRS going low if that does not occur more than 4 bit times prior to TXEN going inactive.

D.5 TIMING DIAGRAMS

Table D-3 lists all timing diagrams. Figures D-1 through D-14 illustrate all timings.

Figure	Title
D-1	Host Access Timing
D-2	16 -Bit Bus, 4-Cycle DMA Read and Write Timing
D-3	16-Bit Bus, 5-Cycle DMA Read and Write Timing
D-4	8-Bit Bus, DMA Read and Write Timing
D-5	Bus Request Timing for Normal DMA Burst
D-6	16-Bit Bus DMA Burst Timing
D-7	DMA Burst Timing – Bus Busy
D-8	8-Bit Bus, Interrupted DMA Burst
D-9	Receiver Serial Timing , Start of Frame
D-10	Receiver Serial Timing , End of Frame
D-11	Transmit Serial Timing , Start of Frame
D-12	Transmit Serial Timing , End of Frame
D-13	Transmit Serial Timing , Collision
D-14	Other Timing

TABLE D-3. LIST OF TIMING DIAGRAMS

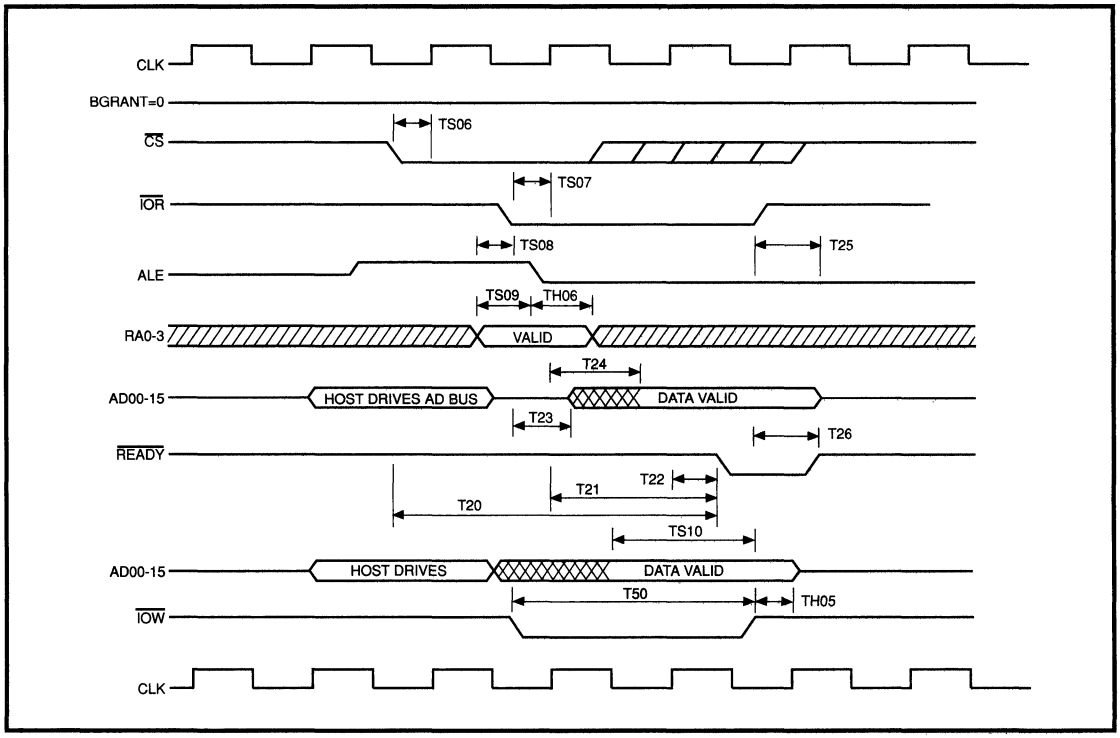

FIGURE D-1. HOST ACCESS TIMING

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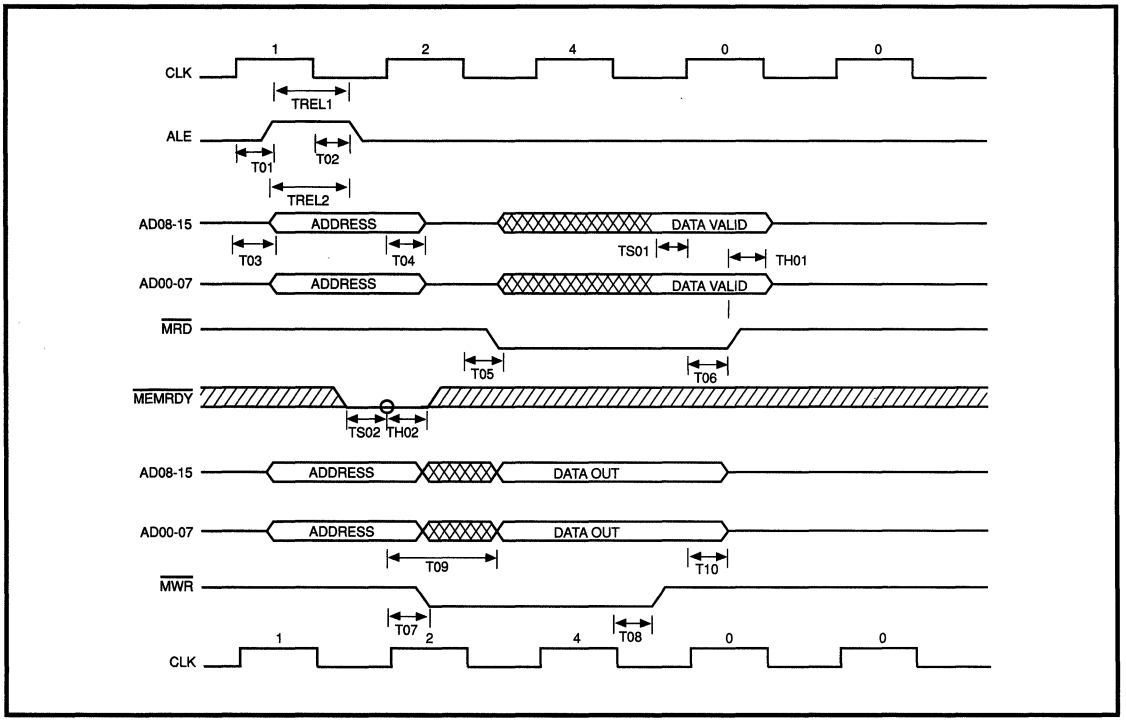

FIGURE D-2. 16-BIT BUS, 4-CYCLE DMA READ AND WRITE TIMING

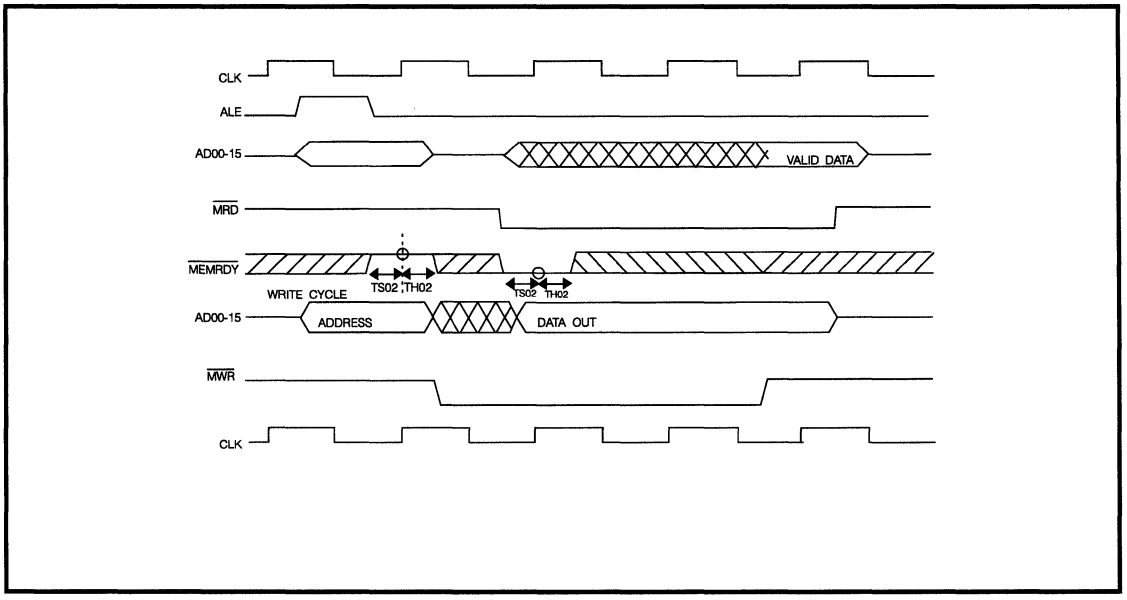

FIGURE D-3. 16-BIT BUS, 5-CYCLE DMA READ AND WRITE TIMING

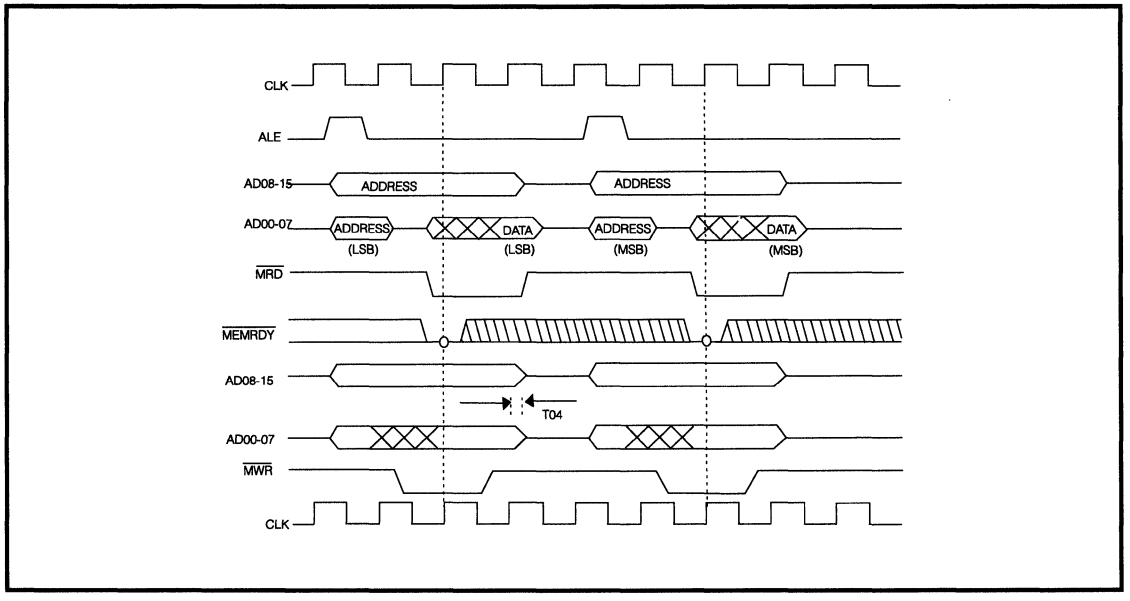

FIGURE D-4. 8-BIT BUS, DMA READ AND WRITE TIMING

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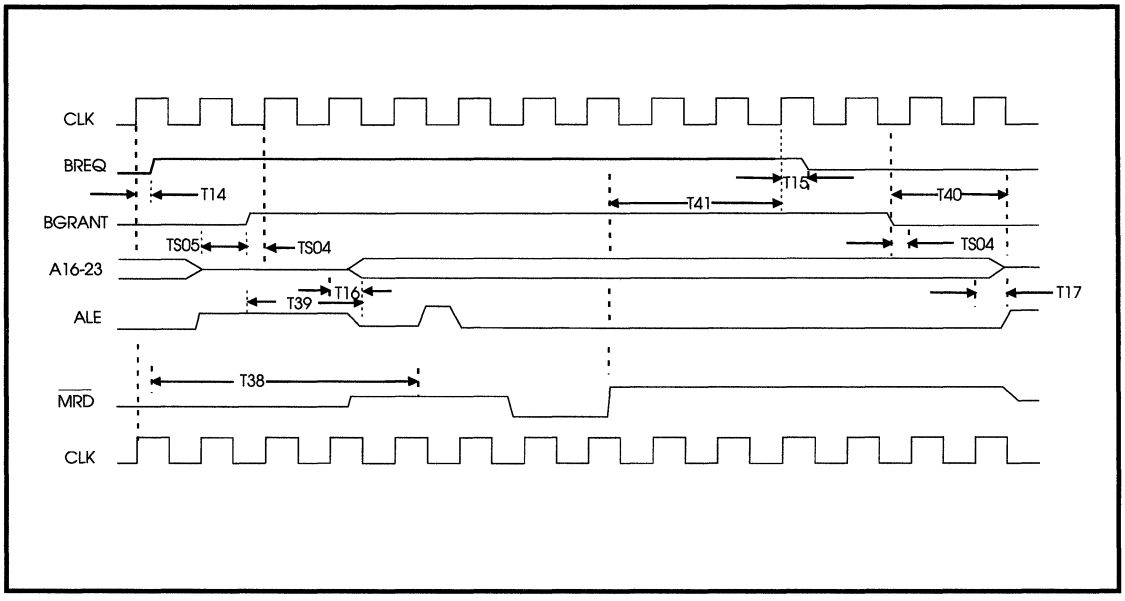

FIGURE D-5. BUS REQUEST TIMING FOR NORMAL DMA BURST

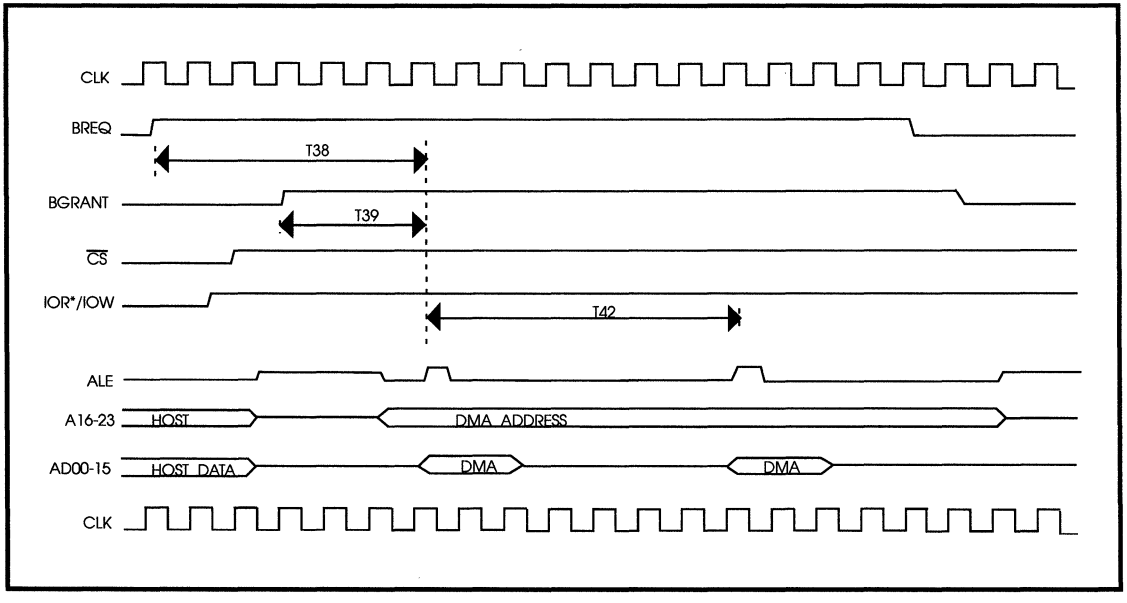

FIGURE D-6. 16-BIT BUS DMA BURST TIMING

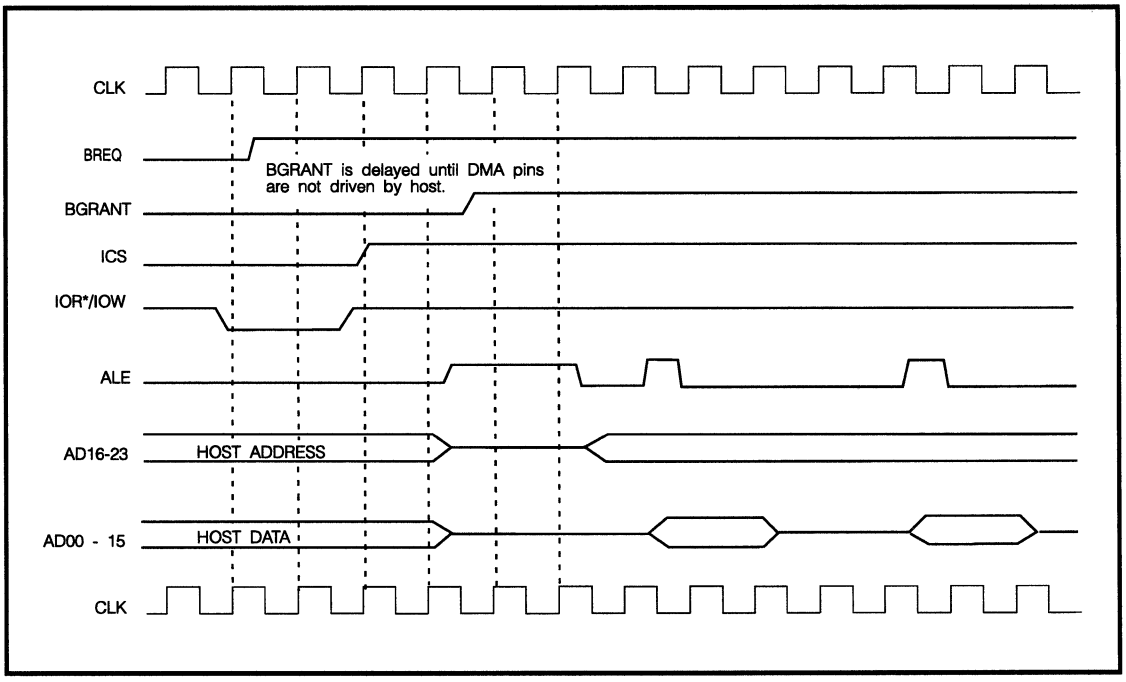

FIGURE D-7. DMA BURST TIMING, BUS BUSY

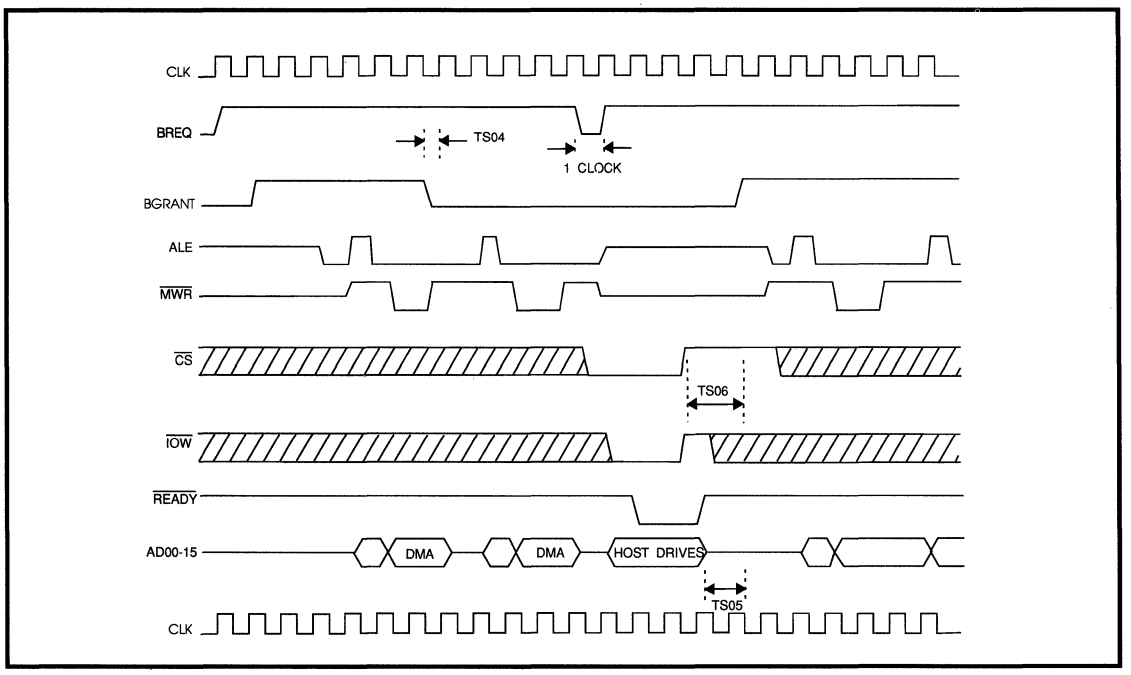

FIGURE D-8. 8-BIT BUS, INTERRUPTED DMA BURST

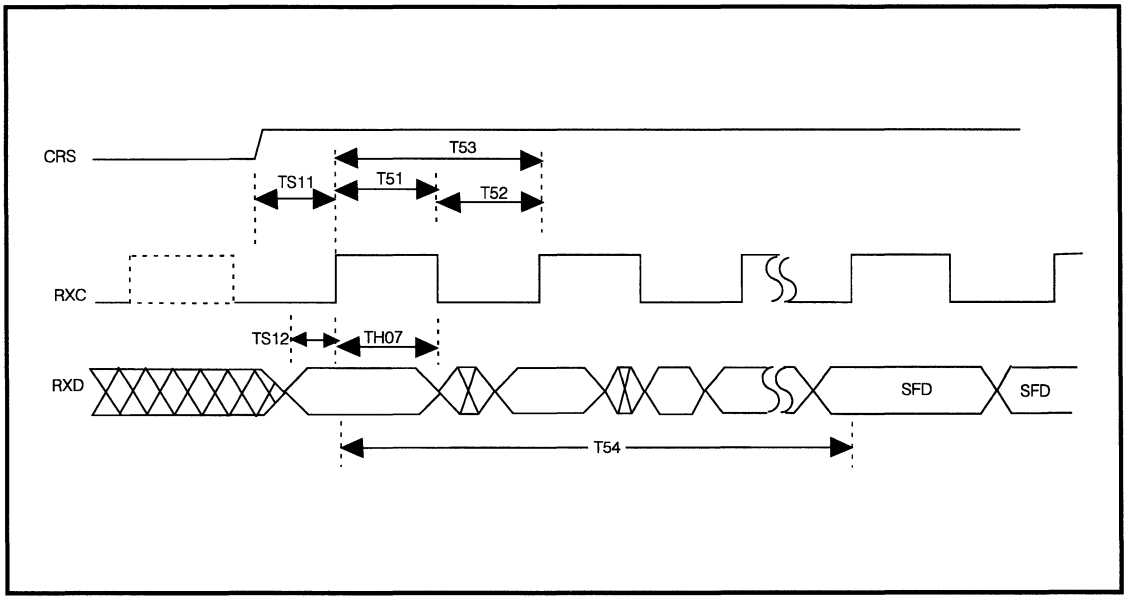

FIGURE D-9. RECEIVER SERIAL TIMING, START OF FRAME RECEPTION

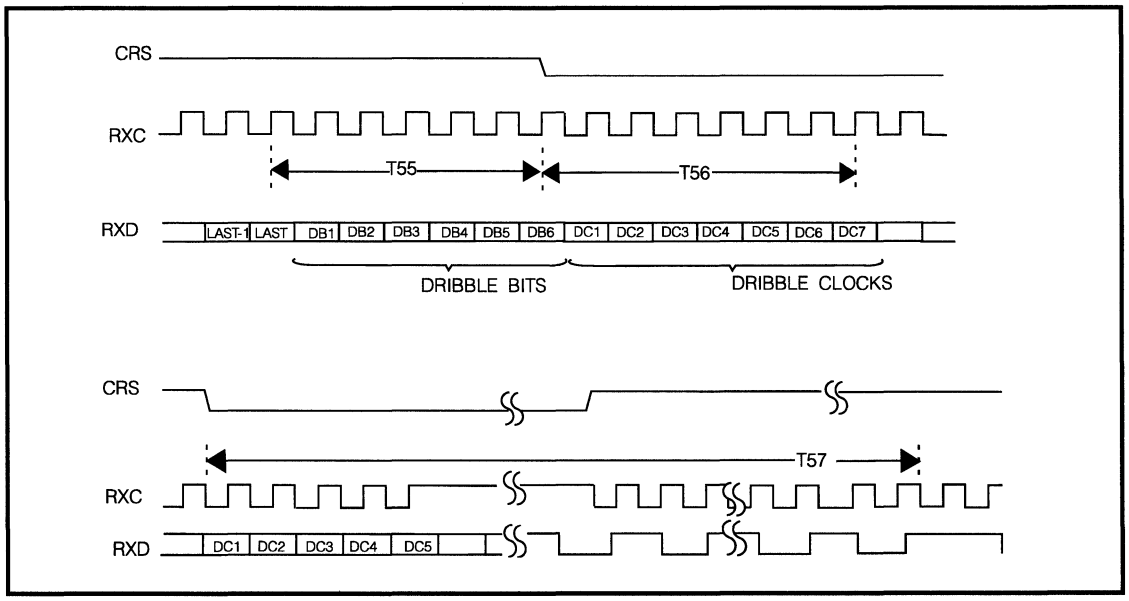

FIGURE D-10. RECEIVER SERIAL TIMING, END OF FRAME

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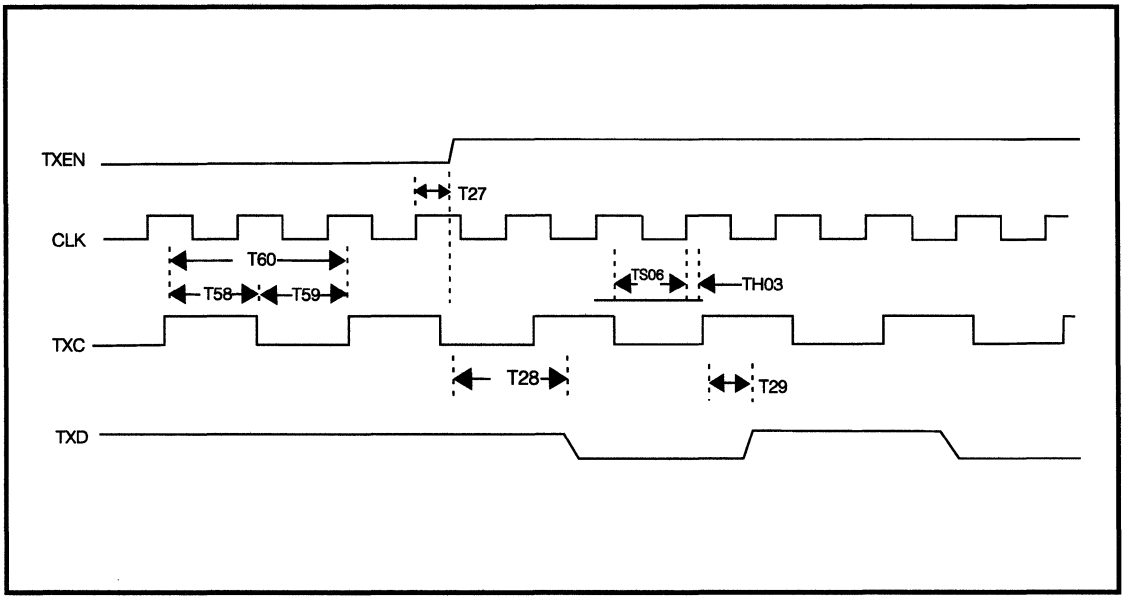

FIGURE D-11. TRANSMIT SERIAL TIMING, START OF FRAME

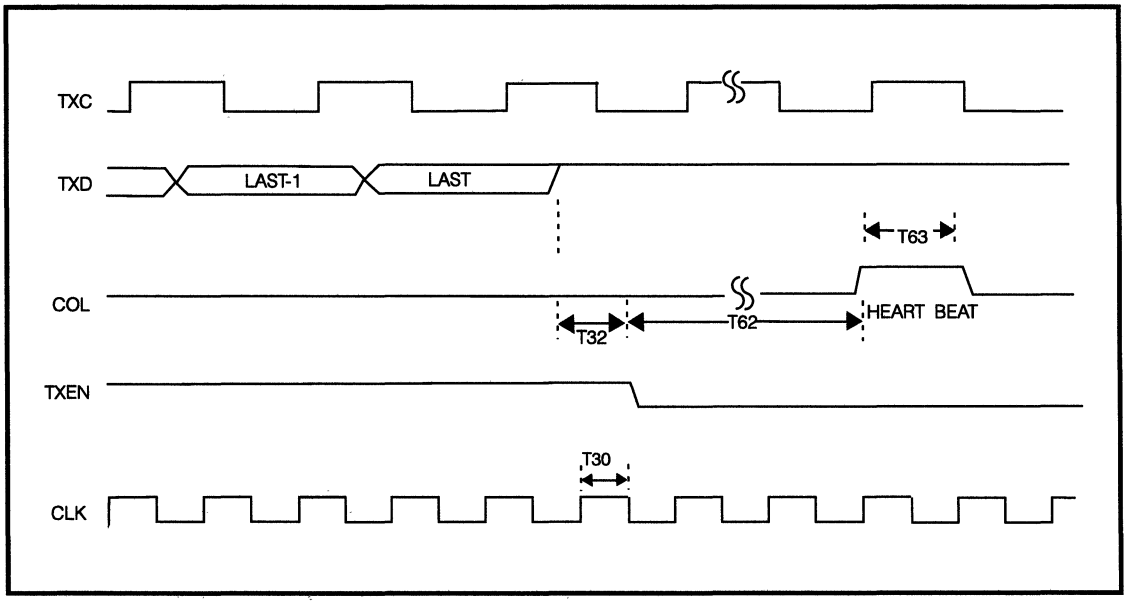

FIGURE D-12. TRANSMIT SERIAL TIMING, END OF FRAME

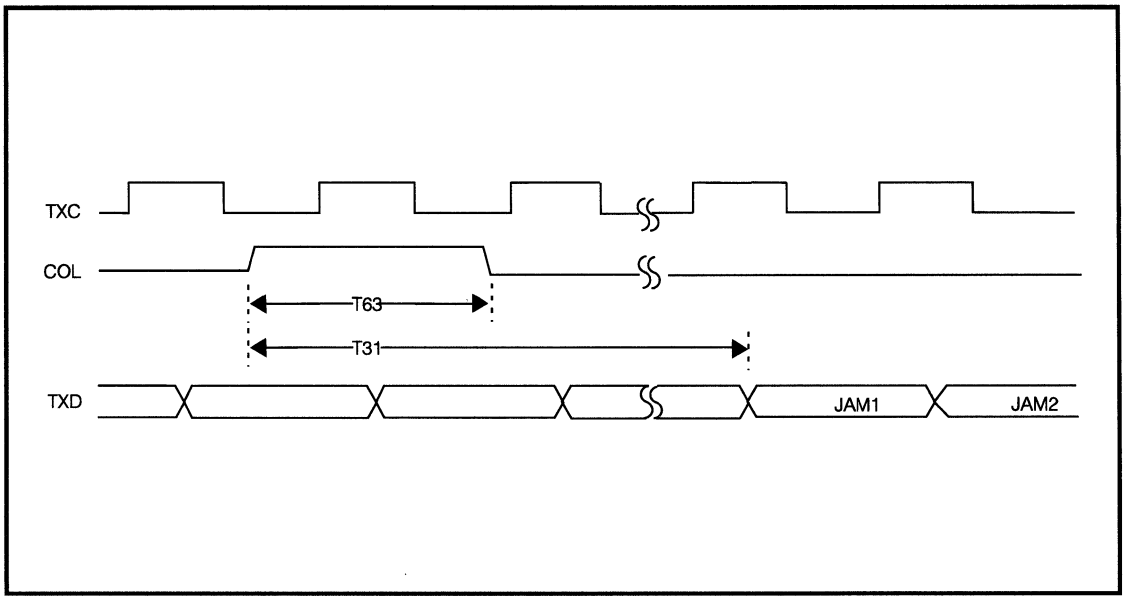

FIGURE D-13. TRANSMIT SERIAL TIMING, COLLISION

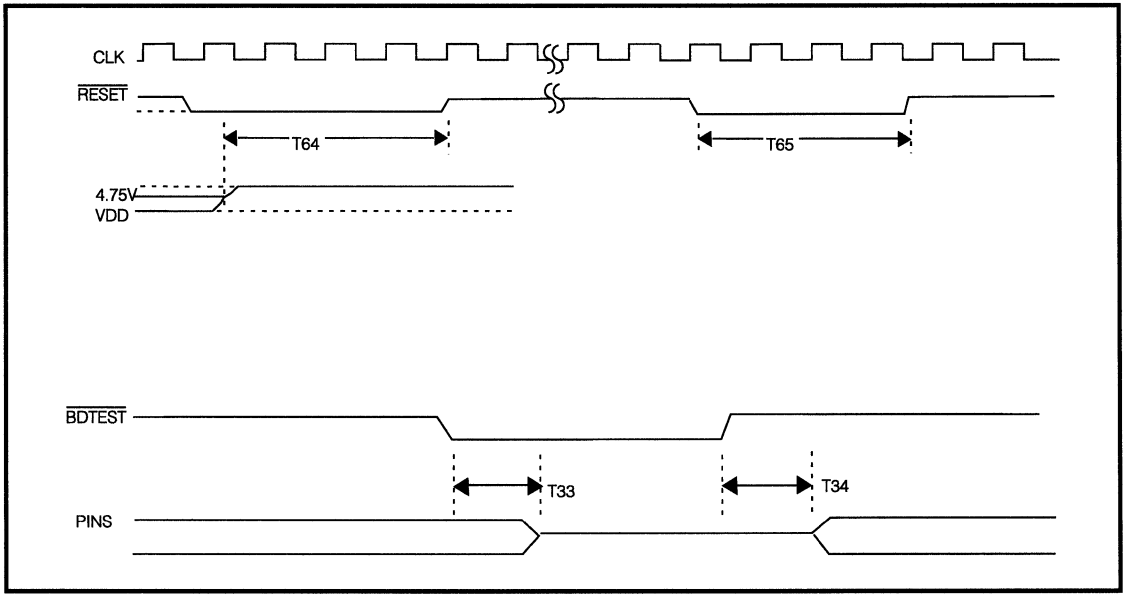

FIGURE D-14. OTHER TIMING

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