WD90C55 VGA LCD Interface

WESTERN DIGITAL

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1.0 INTRODUCTION

The WD90C55 Color Interface Device provides the RGB data exchange interface between the WD90C2x family of VGA/LCD controllers and a variety of LCD color panels. The WD90C55 also acts as a pass-through buffer for LCD monochrome data.

This section provides an introduction to the WD90C55 and a list of features.

1.1 GENERAL DESCRIPTION

The WD90C55 supports laptop computers that use color-LCD type panels. The WD90C55 interfaces with the following VGA laptop controllers:

- WD90C20
- WD90C22
- WD90C20A
- WD90C26
- WD90C26A

With a VGA laptop controller interface, the WD90C55 provides complete support for laptop computers with either monochrome and color LCD displays (refer to Tables 1-1 and 1-2).The WD90C55 drives color LCD panels directly, without requiring additional buffers. Also, it can be used as output buffers to drive mono-LCD panels.

Tables 1-1 and 1-2 show color LCD implementations and number of colors available for each type.

1.2 FEATURES

The major features of the WD90C55 are listed below.

- Direct interface with WD90C20, WD90C22, WD90C20A, WD90C26, and WD9026A VGA Controllers
- Power down mode control to reduce power consumption
- I/O pin mapping to improve board level testability
- 8-bit (2 and 2/3 pixels) STN color LCD interface
- 16-bit (5 and 1/3 pixels) STN color LCD interface
- Timing adjustment for TFT color LCD panel
- 44-pin PQFP package

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CONTROLLER TYPE PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26/ WD90C26A
STN Color LCD	with WD90C55	with WD90C55	with WD90C55	with WD90C55
Hitachi TFT	with WD90C55	with WD90C55	direct	direct
Sharp TFT	N/A	direct	direct	direct

TABLE 1-1 COLOR LCD IMPLEMENTATION

CONTROLLER TYPE PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26/ WD90C26A
STN Color LCD	512	4K or 256K	4K	4K or 256K
TFT Color LCD	512	512	512	512 or 27K

TABLE 1-2 COLOR CAPABILITY

2.0 ARCHITECTURE

The WD90C55 color interface device provides the RGB data exchange interface between the WD90C2x family of VGA/LCD controllers and a variety of color LCD panels, including TFT and STN color panels. It also acts as a pass-through buffer for LCD monochrome data, buffering LCD monochrome data from the WD90C2X family, and passing it, along with control signals, to LCD monochrome panels. These interface functions are supported for the following five modes:

- STN 8-bit Color LCD mode
- STN 16-bit Color LCD mode
- TFT Color LCD for WD90C20
- TFT Color LCD mode for WD90C22
- LCD Monochrome mode

The following additional modes are also provided:

- Pin scan mode
- Output tri-state mode

The WD90C55 turns off any unnecessary logic not selected by SEL[2:0] inputs.

The WD90C55 contains the following eight major functional modules:

- Sequencer
- Data Conversion Control
- Bi-Phase Clock Generator
- Power Down Control
- I/O Pin Mapping Control
- TFT Timing Control Interface
- Color Panel Interface
- Monochrome LCD Interface

Each of these modules is described in the following subsections and are illustrated in the functional block diagram provided in Figure 2-1.

2.1 SEQUENCER - STN INTERFACE

The sequencer provides the key timing control from the WD90C2X controller to the color LCD panel. In STN color-LCD mode, the WD90C2X sends out 6-bits (2-pixels) every shift clock. The shift clock (SCLK) is not free-running but toggling. It toggles only when the video data is valid. WGTCLK line is used to qualify the valid data and to start the state machine in the sequencer.

2.2 DATA CONVERSION CONTROL - STN INTERFACE

Data Conversion Control provides both 6-bit to 8-bit and 6-bit to 16-bit data conversion.

Only one type of color LCD panel is enabled during the operation.

Unused logic is automatically turned off.

2.3 BI-PHASE CLOCK GENERATOR - STN INTERFACE

The Bi-phase Clock Generator is used to generate two-phase clock outputs XUCLK and XLCLK. These outputs are used in the 8-bit STN color LCD interface.

Eight-bit data is latched on the falling edges of XUCLK and XLCLK. Sixteen-bit data is latched on the falling edge of XLCLK.

2.4 POWER DOWN CONTROL

Power Down Control accepts the $\overline{\text{PDOWN}}$ input and generates the control signals to turn off the WD90C55 when the system goes to power down mode.

The power down control signals drive the output data bus low and turn off the output clocks as long as $\overline{\text{PDOWN}}$ remains active.

2.5 I/O PIN MAPPING CONTROL

I/O Pin Mapping Control allows the WD90C55 to enter a test mode where its pins are divided into groups of logically connected input and output pins. When the SEL[2:0] = 000, test mode is enabled.

When in Test mode, each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups.

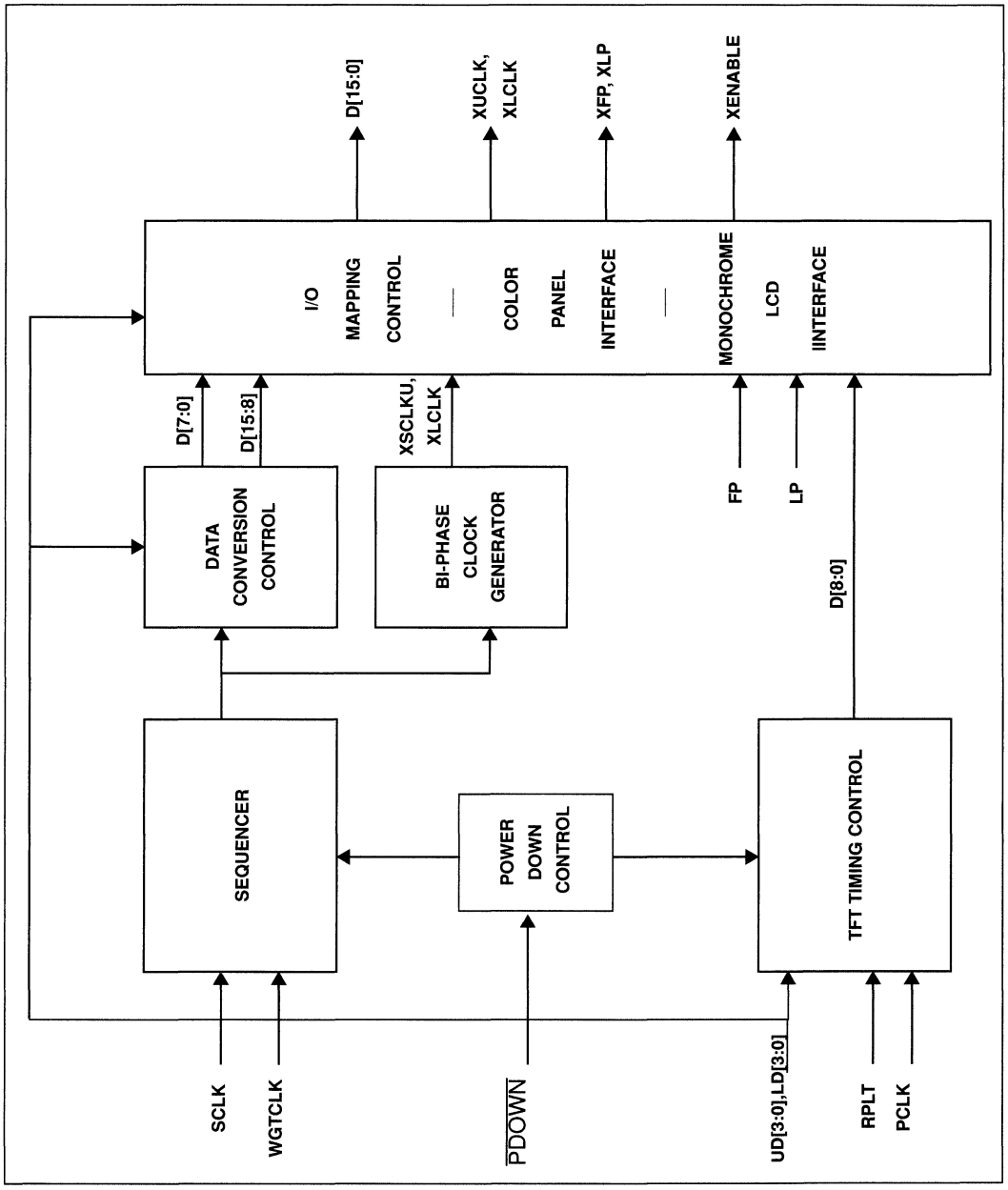

FIGURE 2-1 COLOR LCD FUNCTIONAL BLOCK DIAGRAM

2.6 TFT TIMING CONTROL - TFT INTERFACE

Because the WD90C20 and WD90C22 controllers require different timing, the function of the TFT Timing Control is to adjust the timing to meet the Hitachi TFT Color LCD Panel specification. This adjustment consists of a 7 PCLK delay for the WD90C20 and 2 PCLK delay for the WD90C22.

The WD90C20A, WD90C26, and WD90C26A can drive the Hitachi TFT color LCD directly, without a WD90C55 interface.

Also, the WD90C22, WD90C20A, WD90C26, and WD90C26A can drive the Sharp TFT color LCD panel directly.

2.7 COLOR PANEL INTERFACE

The color panel interface supports multiplexing of data onto the external data bus. The 8-bit STN data are multiplexed onto the external data bus D[7:0], or 16-bit STN data are multiplexed onto external data bus D[15:0].

Nine-bit TFT data R[2:0], G[2:0], and B[2:0] are multiplexed onto D[8:0], and 8-bit monochrome LCD data is multiplexed onto D[7:0].

2.8 MONOCHROME LCD INTERFACE

In Monochrome LCD mode, input data UD[3:0] LD[3:0] and control signals for FP, LP, and SCLK, are multiplexed onto the color interface bus. These input data and control signals are simply buffered and passed through the WD90C55. See Figure 2-2.

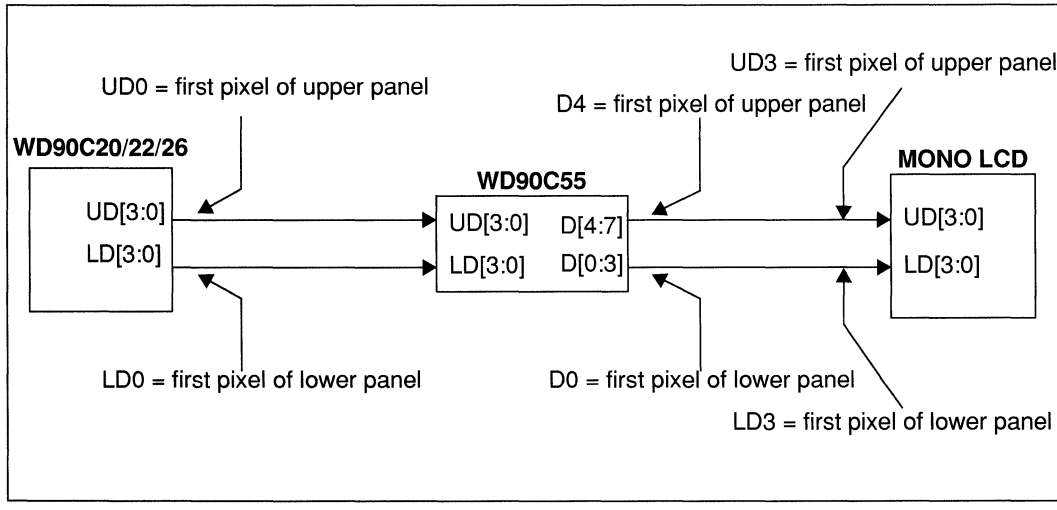

FIGURE 2-2 WD90C55 MONO LCD INTERFACE BLOCK DIAGRAM

3.0 SIGNAL DESCRIPTION

This section contains pin configuration information for the 44-pin WD90C55 devices. Pin assignment tables and pin diagrams are provided.

- Pinout diagram
- Pin Number to Signal list
- Pin/Package Descriptions
- Bus Definition
- LCD Panel Pinout Specification

3.1 WD90C55 PINOUT

This section contains the following information:

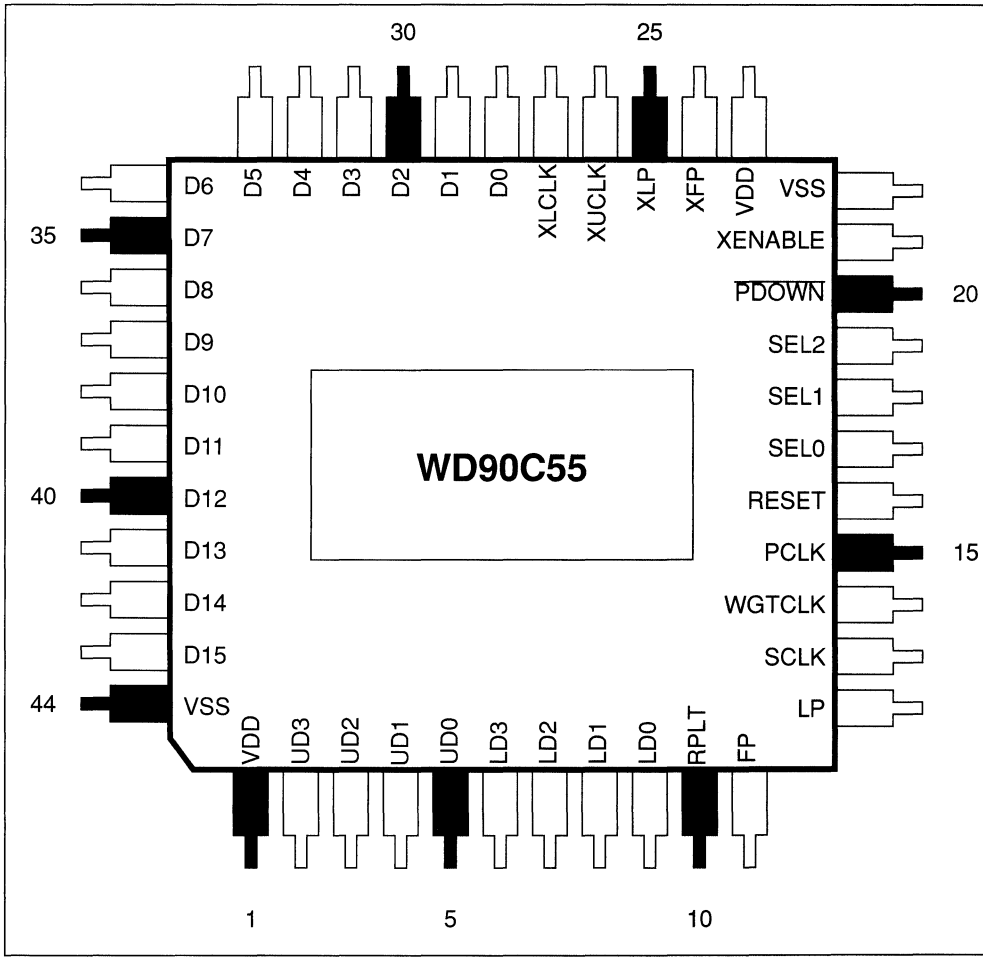

FIGURE 3-1 44-PIN PQFP PACKAGE PINOUT DIAGRAM

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VDD	16	RESET	31	D3
2	UD3	17	SEL0	32	D4
3	UD2	18	SEL1	33	D5
4	UD1	19	SEL2	34	D6
5	UD0	20	$\overline{\text{PDOWN}}$	35	D7
6	LD3	21	XENABLE	36	D8
7	LD2	22	VSS	37	D9
8	LD1	23	VDD	38	D10
9	LD0	24	XFP	39	D11
10	RPLT	25	XLP	40	D12
11	FP	26	XUCLK	41	D13
12	LP	27	XLCLK	42	D14
13	SCLK	28	D0	43	D15
14	WGTCLK	29	D1	44	VSS
15	PCLK	30	D2		

TABLE 3-1 WD90C55 PIN NUMBER TO SIGNAL LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1,22,23,44	VSS, VDD	I	Power
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[0:2]	I	WD90C55 Selection Bus, bit 0 to bit 2
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output

TABLE 3-2 WD90C55 PIN/SIGNAL DESCRIPTIONS

SEL[2:0]	DESCRIPTION
0 0 0	Test Mode 1 I/O pin mapping, ICT test
0 0 1	8-Bit STN Panels (Sharp, Seiko)
0 1 0	16-Bit STN Panels (Sanyo)
1 0 0	Monochrome LCD Panels
1 0 1	Hitachi TFT Color Panel (WD90C20)
1 1 0	Hitachi TFT Color Panel (WD90C22)
1 1 1	Test Mode 2, Output buffer tristate test

TABLE 3-3 WD90C55 BUS SEL[2:0] BUS DEFINITION

NOTE

The WD90C22 controller can drive the Sharp TFT color LCD directly without the WD90C55 device.

WD90C55	MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN (Sanyo/ Matsushita)	9-BIT TFT (Hitachi/ Sharp)
XFP	FP	DIN	YD	FLM	VSYNC
XLP	LP	LP	LP	CL1	HSYNC
XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
FR	FR	UNUSED	UNUSED	M	UNUSED
XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
D8	UNUSED	UNUSED	UNUSED	UD0	B0
D7	UD3	D7	D0	LD7	R2
D6	UD2	D6	D1	LD6	R1
D5	UD1	D5	D2	LD5	R0
D4	UD0	D4	D3	LD4	G2
D3	LD3	D3	D4	LD3	G1
D2	LD2	D2	D5	LD2	G0
D1	LD1	D1	D6	LD1	B2
D0	LD0	D0	D7	LD0	B1

TABLE 3-4 LCD PANEL PINOUT SPECIFICATION

4.0 DC ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0° C to 70° C
Storage temperature	-40° C to 125° C
Voltage on all inputs and outputs with respect to Vss	-0.3 to 7 Volts
Power dissipation	0.85 watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70° C
Power Supply Voltage	4.75 to 5.25 Volts

4.3 SUPPLY PINS

Table 4-1 lists the minimum and maximum supply voltage.

PARAMETER	MIN	MAX	CONDITIONS
VDD	4.75V	5.25V	Pins 1, 23

TABLE 4-1 WD90C55 SUPPLY VOLTAGE

4.4 INPUT PINS

Table 4-2 lists the minimum and maximum DC voltage and current for the following input signal pins:

FP	$\overline{\text{PDOWN}}$	$\overline{\text{SEL[2:0]}}$
LD[3:0]	RESET	UD[3:0]
LP	RPTL	WGTCLK
PCLK	SCLK	

PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC +0.5V	
IIL	-10µA	-10 µA	VIH = VCC, VIL = 0V
IDDS		100 µA	VIN = VCC or VSS, IOH = IOL = 0mA

TABLE 4-2 WD90C55 INPUT PIN PARAMETERS

4.5 OUTPUT PINS

Table 4-3 lists the minimum and maximum DC voltage and current for the following output signal pins:

D[15:0] XENABLE XFP
XLCLK XLP XUCLK

PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6mA
VOH	2.4V		IOH = -6mA
IOZ	-50 µA	50 µA	VOUT = VCC or VSS
C_{out}		100pf	

TABLE 4-3 WD90C55 OUTPUT PIN PARAMETERS

4.6 TYPICAL POWER CONSUMPTION

Table 4-4 lists the typical power consumption for five common display modes:

DISPLAY MODE	DISPLAY ACTIVE		POWERDOWN	
	LOAD	NO LOAD	LOAD	NO LOAD
CRT	17.5	16.57	1.38	.02
8-BIT STN	23.3	19.43	.02	.02
16-BIT STN	27.88	19.13	.02	.02
TFT	24.63	18.06	.04	.04
MONOCHROME	18.68	16.16	.02	.02
NOTE: All values are given in milliamperes (mA).				

TABLE 4-4 WD90C55 TYPICAL POWER CONSUMPTION

5.0 AC OPERATING CHARACTERISTICS

Timing is provided for the following:

- STN Color LCD Mode - Input Timing
- STN Color LCD Mode - 8-bit interface
- STN Color LCD Mode - 16-bit interface
- TFT Color LCD Mode - 9-bit interface
- Mono LCD Mode

ITEM	DESCRIPTION	MIN	MAX
1	Rise/Fall Time (Inputs: PCLK SCLK FP LP WGTCLK		5 ns 10 ns 10 ns 10 ns 10 ns
2	UD[3:1], LD[3:1] setup to ⇓ SCLK	18 ns	
3	UD[3:1], LD[3:1] hold from ⇓ SCLK	18 ns	
4	UD[3:1], LD[3:1] valid from ⇑ WGTCLK	10 ns	
5	UD[3:1], LD[3:1] invalid from ⇓ WGTCLK	-10 ns	
6	SCLK period	62.5 ns (PCLK = 32 MHz)	80 ns (PCLK = 25 MHz)
7	FP ⇑ to LP ⇓ SETUP time	1LP	
8	FP ⇓ to LP ⇓ HOLD time		0

TABLE 5-1 STN COLOR LCD MODE - INPUT TIMING

Refer to the following figure for timing diagram.

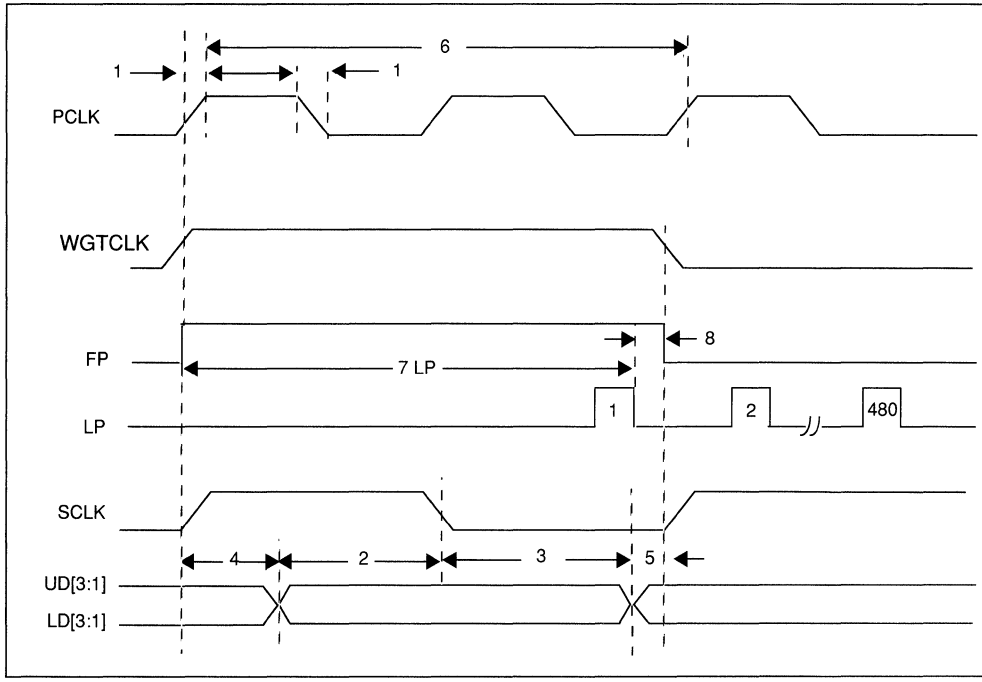

FIGURE 5-1 STN COLOR LCD MODE - INPUT TIMING DIAGRAM

NOTE

$LP = 1/_{PCLK} * 800$

ITEM	DESCRIPTION	MIN	MAX
1	XFP⇓ to XLP⇓ Hold time	24PCLK	32 PCLK
2	XFP ⇑ to XLP ⇑ Setup time		1LP
3	⇑ SCLK to ⇑ XUCLK		240 ns
4	⇑ SCLK to ⇑ XLCLK		345 ns
5	D[7:0] (even byte) setup to XUCLK ⇓ or setup to XLCLK ⇓	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
6	D[7:0] (odd byte) hold from XUCLK⇓ or hold from XLCLK⇓	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
7	XUCLK cycle time	163 ns	218 ns
8	XLCLK cycle time	165 ns	205 ns

TABLE 5-2 STN COLOR LCD MODE - 8-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

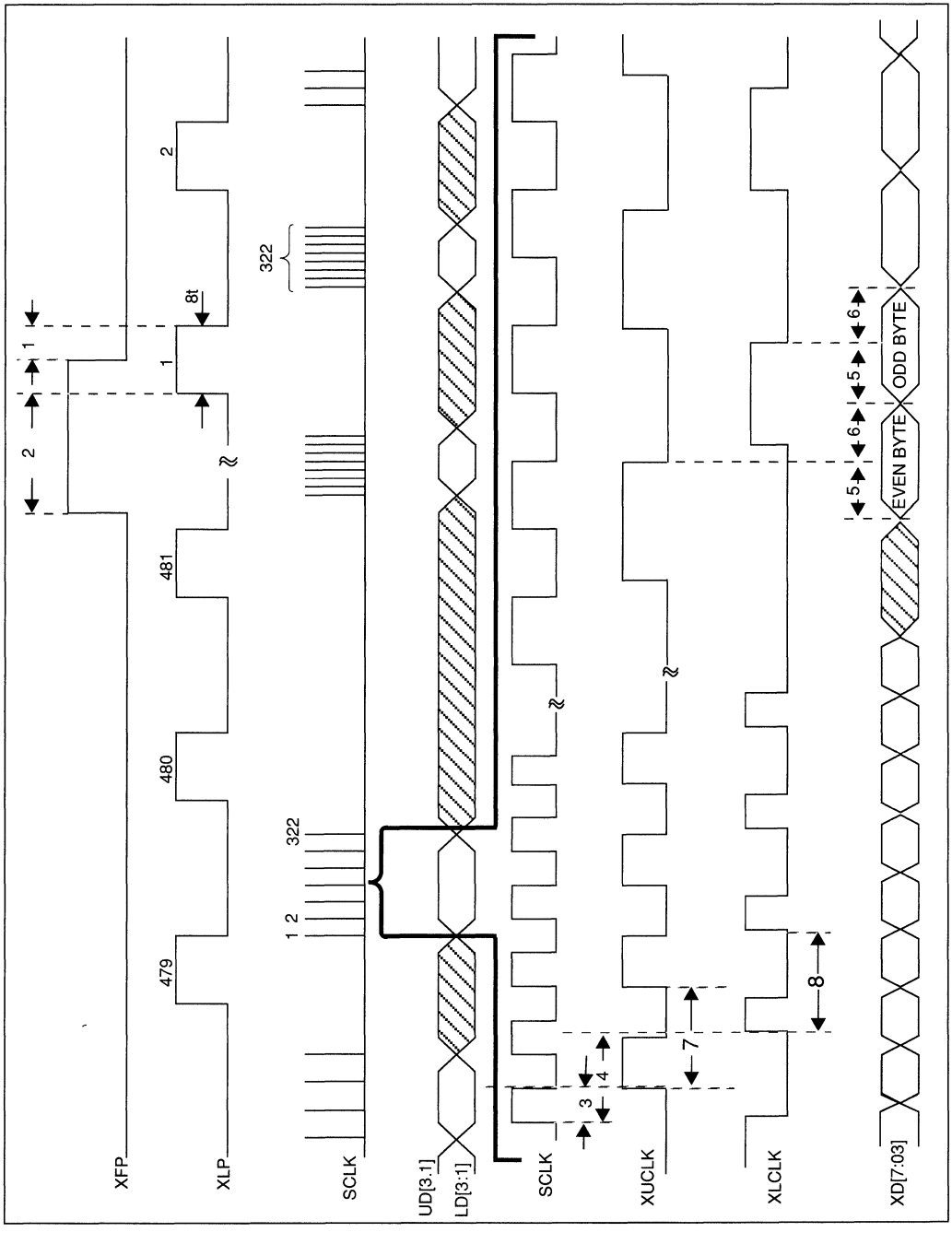

FIGURE 5-2 STN COLOR LCD 8-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	XFP ⇑ to XLP ⇑ Hold time	24PCLK	32 PCLK
2	XFP⇓ to XLP⇓ Setup time		1LP
3	D[15:0] setup to XLCLK ⇓	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	
4	D[15:0] hold to XLCLK ⇑	30 @ t=32MHz 35 @ t=28MHz 40 @ t=25MHz	

TABLE 5-3 STN COLOR LCD MODE - 16-BIT INTERFACE

Refer to the figure on the next page for timing diagram.

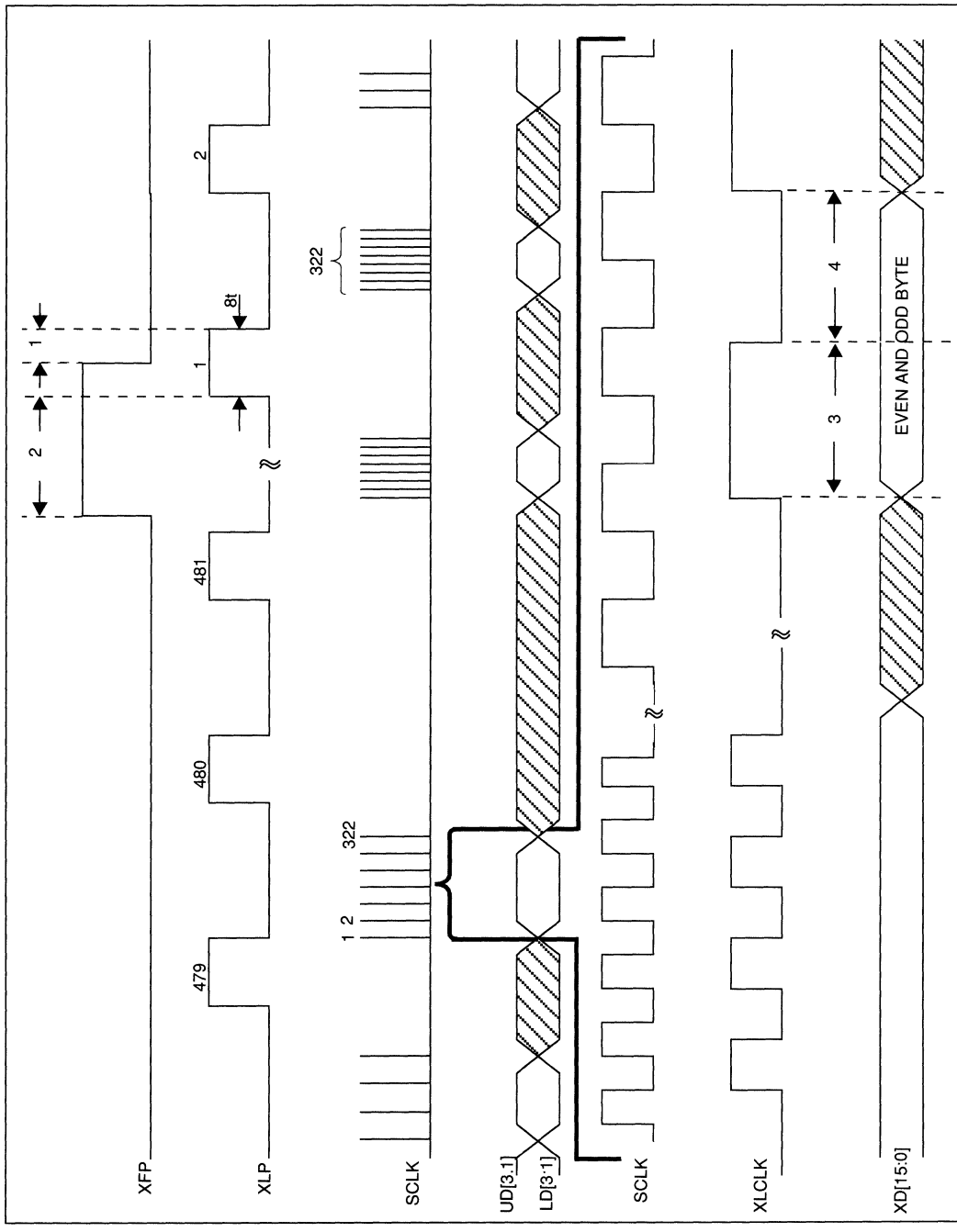

FIGURE 5-3 STN COLOR LCD 16-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	Data IN [8:0] setup to PCLK ⇓	10 ns	
2	Data IN [8:0] hold from PCLK⇓	10 ns	
3	D[8:0] setup to XUCLK ⇓(WD90C22) PCLK=25MHz	10 ns	
4	D[8:0] hold from XUCLK ⇓(WD90C22) PCLK=25MHz	10 ns	
5	D[8:0] setup to XUCLK ⇓ (WD90C20) PCLK=25MHz	10 ns	
6	D[8:0] hold from XUCLK ⇓ (WD90C20) PCLK=25MHz	10 ns	

TABLE 5-4 TFT COLOR LCD MODE - 9-BIT INTERFACE

Refer to the following figure for timing diagram.

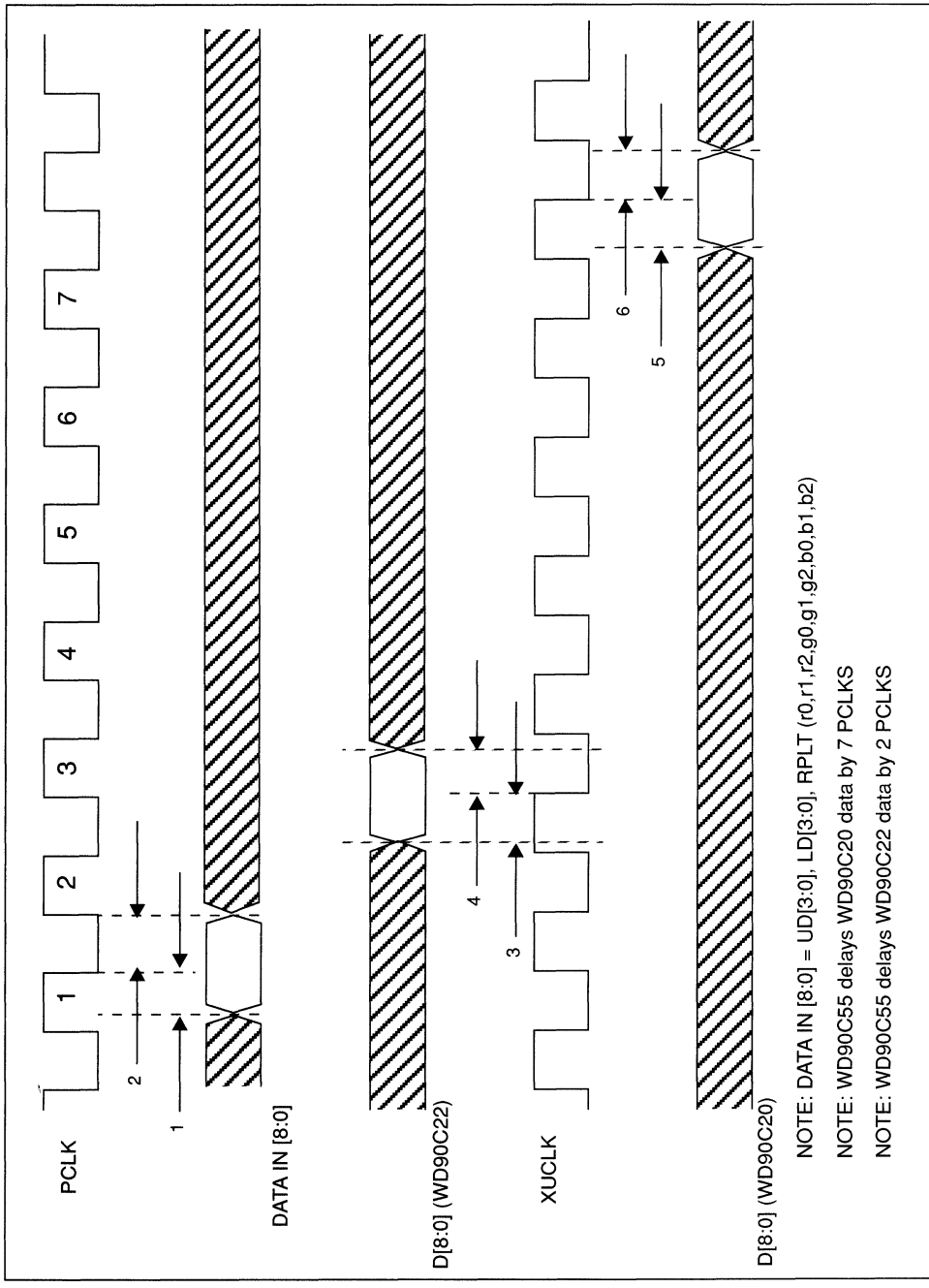

FIGURE 5-4 TFT COLOR LCD 9-BIT INTERFACE MODE TIMING DIAGRAM

6.0 IMPLEMENTATION

This section provides block diagrams of the WD90C55 device in each of the following implementations:

- WD90C20 Implementation
- WD90C20A Implementation
- WD90C22 Implementation
- WD90C26 and WD90C26A Implementation

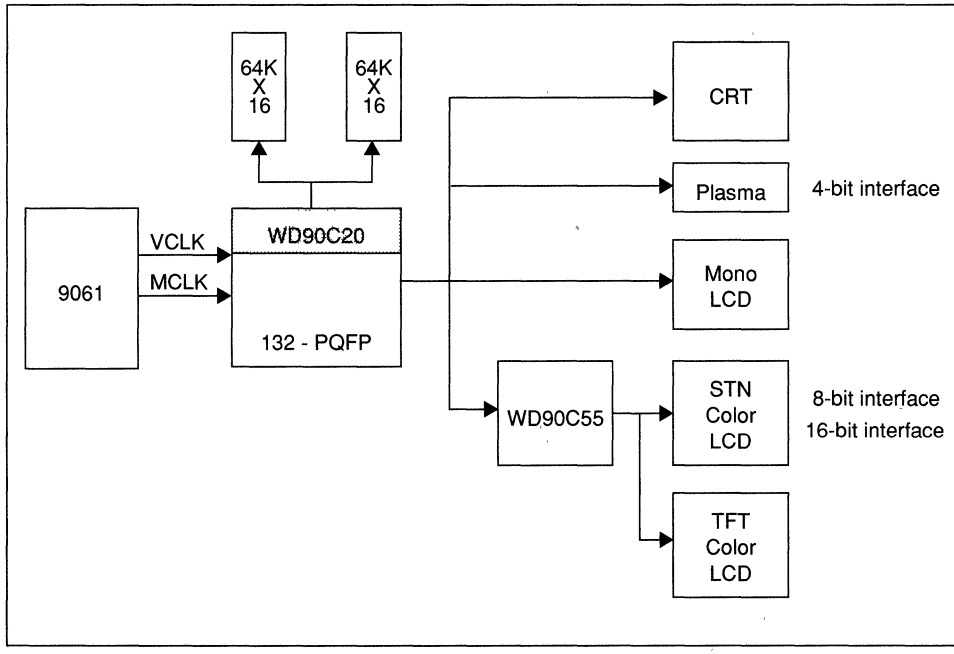

FIGURE 6-1 WD90C55 WITH WD90C20 IMPLEMENTATION

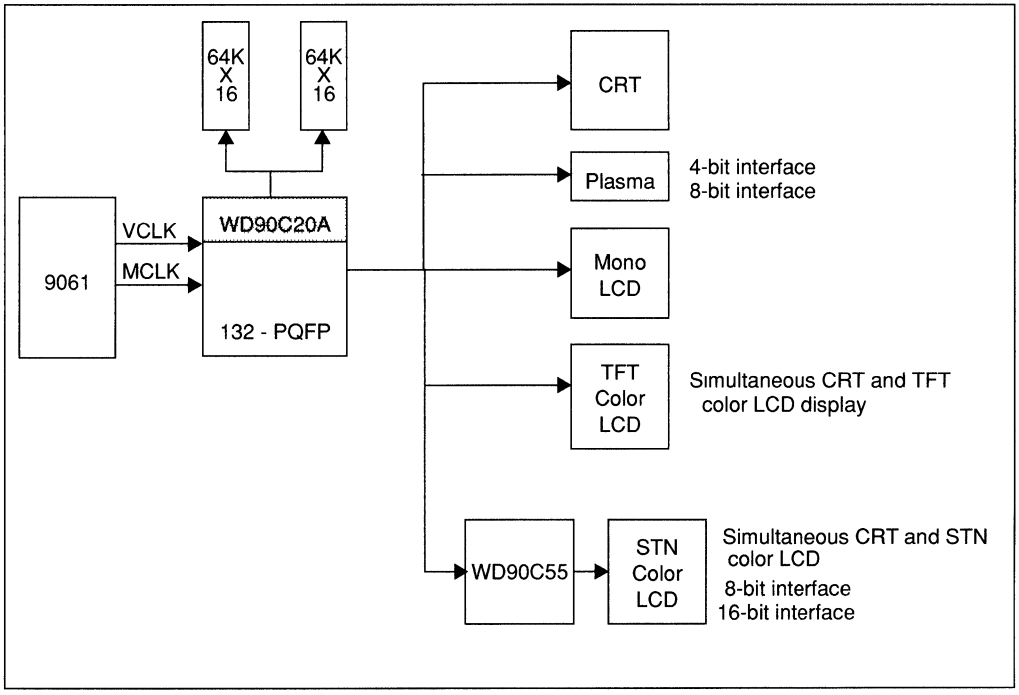

FIGURE 6-2 WD90C55 WITH WD90C20A IMPLEMENTATION

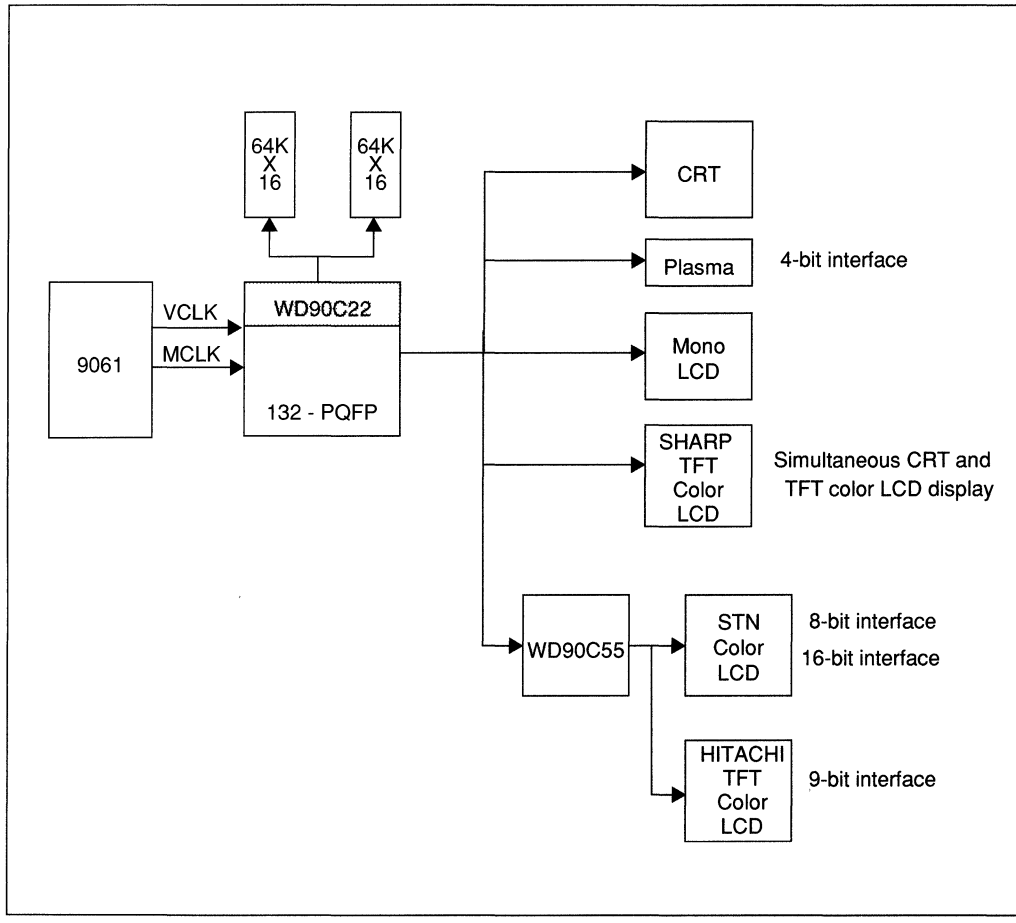

FIGURE 6-3 WD90C55 WITH WD90C22 IMPLEMENTATION

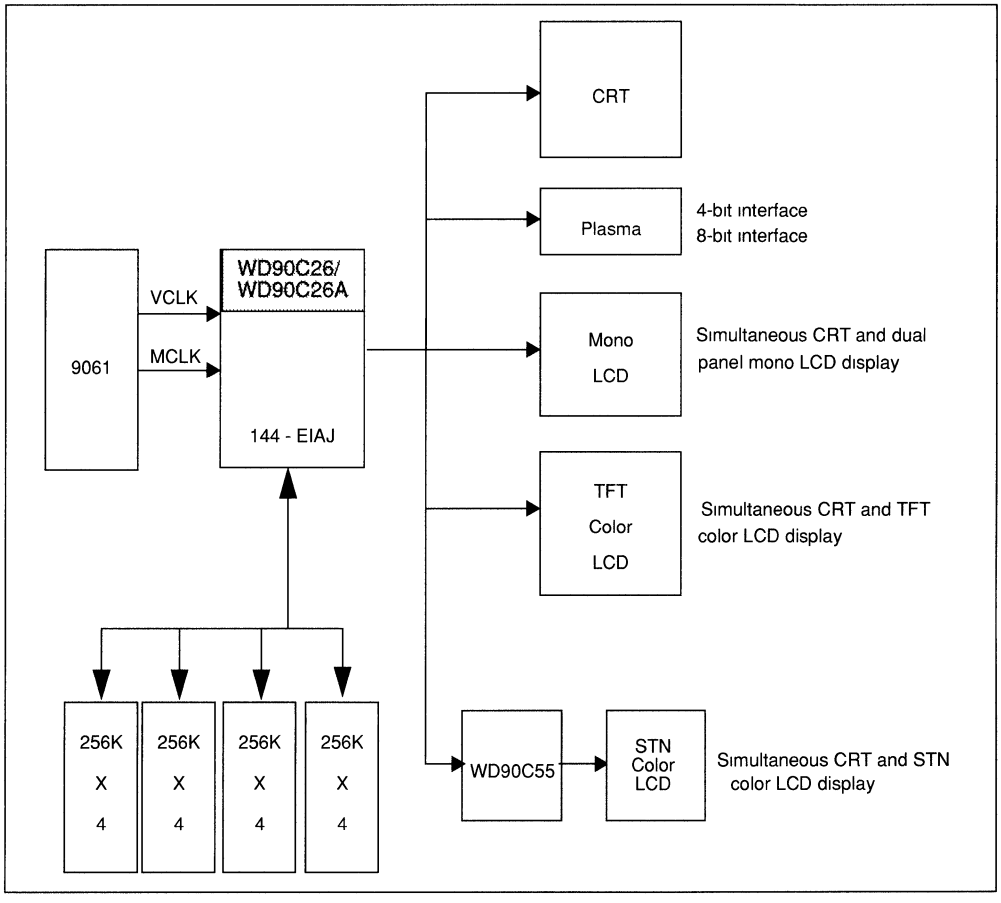

FIGURE 6-4 WD90C55 WITH WD90C26/WD90C26A IMPLEMENTATION

7.0 MECHANICAL SPECIFICATIONS

Figure 8-1 contains the mechanical specifications for WD90C55 44-pin PQFP package.

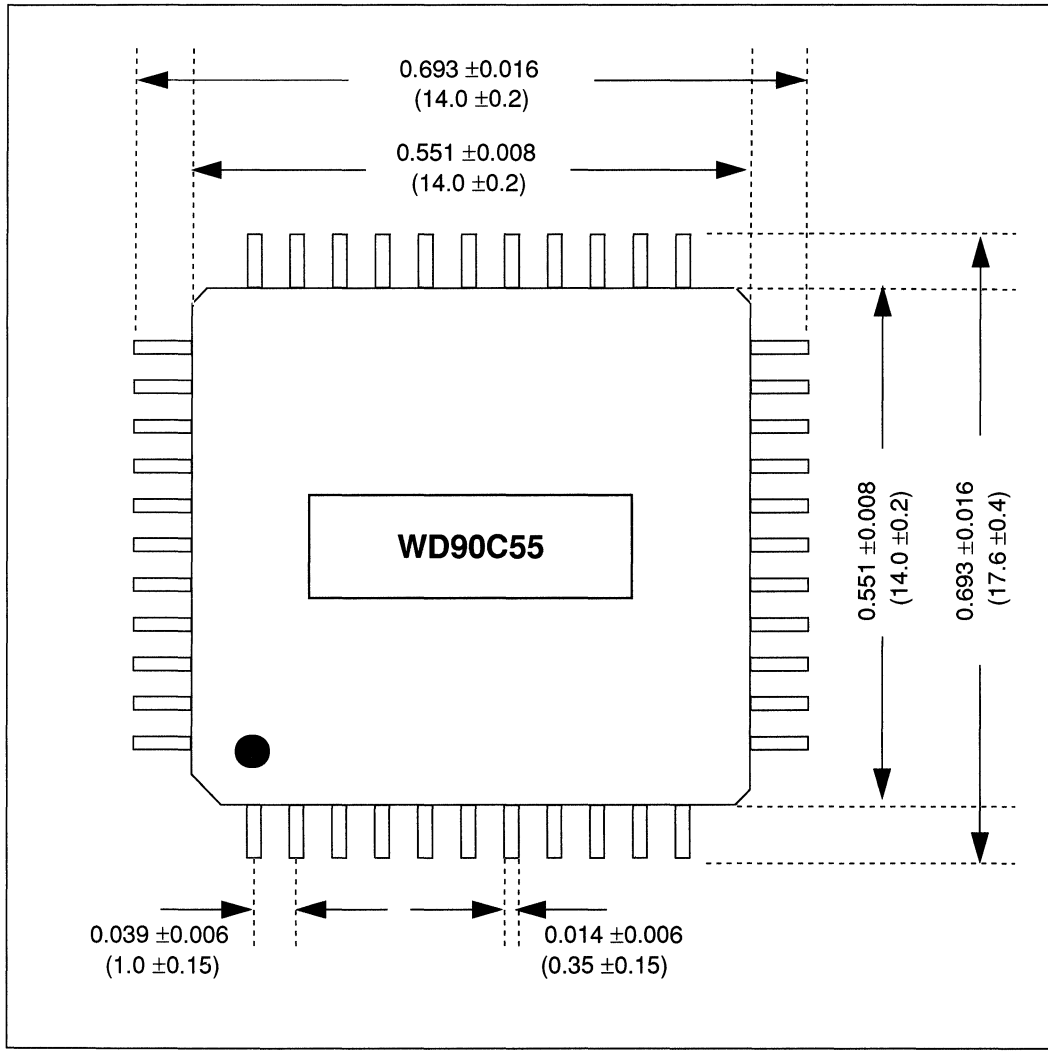

FIGURE 7-1 44-PIN LAYOUT MECHANICAL SPECIFICATION