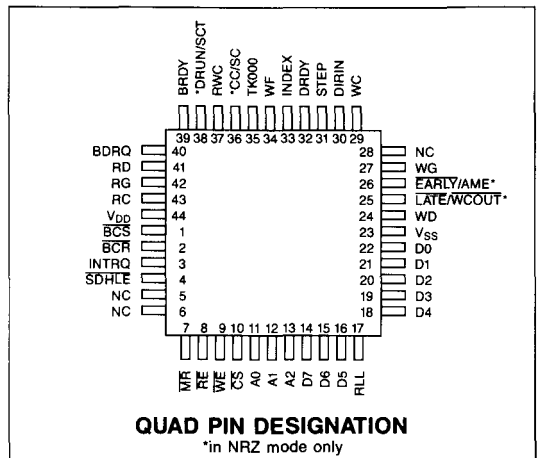# WD50C12
Winchester Disk
Controller

FEATURES

- Software selectable MFM, NRZ, or RLL disk data format
- Software selectable Soft Sector or Hard Sector mode
- Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC for MFM and NRZ
- Supports 1:1 interleave and data transfer rate up to 15Mb/s for NRZ mode
- Supports 1:1 interleave and data transfer rate up to 10Mb/s for MFM and RLL mode
- Software selectable default sector lengths of 128, 256, 512, and 1024.
- User programmable sector size up to 2048 bytes
- Can automatically correct errors when sector buffer is used
- Software programmable 5 or 11 bit error correction span when 32 bit ECC is selected
- Software programmable 11 or 22 bit error correction span when 56 bit ECC is selected
- Compatible with most microprocessors through 8 bit data bus

- Integration of features previously contained in the WD1010/2010/5010A/5011A/50C20A
- Software selectable retry algorithms
- Software selectable 3 bit or 4 bit head number field
- Low Power CMOS design
- Compatible with WD5011A-10

QUAD PIN DESIGNATION
*in NRZ mode only

DESCRIPTION

The WD50C12 (5012) integrates the function of the WD5010A-10, WD5011A-10, and some WD50C20A-10 hard disk controller functions in a single CMOS device. This single chip disk controller is designed for use with ST506-type Winchester disk drives, ST412-type Winchester disk drives, and hard and soft sectored serial mode ESDI drives. The WD50C12 is designed to be software compatible with the WD5011A-10.

The MFM, NRZ, and RLL disk data formats are software selectable. The WD50C12 defaults to the soft sector RLL disk data format with 56 bit ECC.

The controller will read or write disk data at up to a 10 megabit per second rate for RLL and MFM encoding in ST506 mode, and will run up to 15 megabit per second for NRZ encoding in ESDI mode.

The RLL implementation is a (2,7,2,4,3) code, based on the IBM 3370 code. The only difference lies in the assignments of the code words to the 7 different data streams possible. Error propagation is limited to 4 bits.

When programmed in the NRZ mode, the WD50C12 qualifies NRZ disk data using the Sector / Address Mark Detect signal, and also modifies the Read Gate and Write Gate signals to meet ESDI specifications. In this same mode the length of PLO sync and Gap fields are software programmable.

The WD50C12 disk controller requires only a single supply at +5 volts. It is designed to operate with an external sector buffer memory or with an external DMA controller. Data bytes are transferred to or from the buffer every 800ns (average) with a 10Mb/s drive. The buffer consists of a RAM and 8 bit resettable counter. The disk controller generates counter control signals to minimize external gating. Buffer to processor transfers may be made via programmed I/O or via DMA. The controller also generates handshake signals to control DMA operation for multiple sector transfers.

WESTERN DIGITAL

†

PIN DESCRIPTION

The following inputs and outputs are TTL compatible. Outputs are capable of driving one TTL unit load. Table 1 describes the pin designations for the processor interface. Table 2 describes the pin designations for the buffer interface. Table 3 describes the pin designations for the drive interface.

TABLE 1. PROCESSOR INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
14-16 18-22	D0 to D7	Data 0 to 7	I/O	Tristate bi-directional 8 bit data bus. Commands, status, and data to/from buffer memory are transferred over this bus. D7 is MSB.
8	$\overline{RE}$	$\overline{READ\ ENABLE}$	I/O	Tristate bidirectional line. Used as input in conjunction with $\overline{CS}$ to read controller task register file. Used as output when reading data from buffer memory to controller.
9	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I/O	Tristate bidirectional line. Used as input in conjunction with $\overline{CS}$ to write command or task information into controller task register file. Used as output when writing data from controller to buffer memory.
11-13	A2,A1,A0	ADDRESS 0 TO 2	I	Address inputs used to select register from task register file. A2 is MSB.
10	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Chip select input must be active when reading or writing into controller task register file.
3	INTRQ	INTERUPT REQUEST	O	Interrupt request is an active high output set when a command terminates and reset when the status register is read, or when command register is written.
7	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	Master reset input will initialize the controller state and clear status flags when activated.
4	$\overline{SDHLE}$	$\overline{SDH\ LATCH\ ENABLE}$	O	This output is low when the SDH register has been selected and is being written by the host.
44	V_{DD}	+5 volt	I	Digital +5 volts.
23	V_{SS}	GROUND	I	Digital Ground.

TABLE 2. BUFFER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	O	Buffer chip select output is active when the controller is transferring data to or from buffer memory. $\overline{BCS}$ is also used to control bus switching.
39	BRDY	BUFFER READY	I	Buffer ready input is used to signal the controller that the buffer memory is ready for controller data transfers. It is activated when the buffer is full for write or format, or when the buffer is empty for read.
2	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	O	Buffer counter reset output is used to reset the address counter when the buffer memory is implemented with a counter and static RAM. This output is not used when the buffer memory is implemented with a FIFO memory.
40	BDRQ	BUFFER DATA REQUEST	O	Buffer data request output is used to initiate DMA transfers to/from buffer memory.

Pin descriptions change depending on whether the drive interface is using RLL and MFM encoding in ST506 mode or using NRZ encoding in ESDI mode. **See the note at end of this table.**

TABLE 3. DRIVE INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
27†	WG	WRITE GATE	O	Write gate is an output that is active when write data is valid; enables head write current. This signal is deactivated when write fault (WF) is detected.
31*	STEP	STEP PULSE	O	Step pulse output.
30*	DIRIN	DIRECTION IN	O	Step direction output; direction is inward (cylinder number increasing) for DIRIN = '1'.
32†	DRDY	DRIVE READY	I	Receipt of deactivated DRDY will halt all read, write or stepping commands.
34†	WF	WRITE FAULT	I	Receipt of WF will halt all read, write, or stepping commands.
35*	TK000	TRACK ZERO	I	Used to verify proper cylinder location when executing a restore command.
33†	INDEX	INDEX PULSE	I	Used for timing when formatting. Also used for counting retries. Rising edge triggered.
37*	RWC	REDUCE WRITE	O	Reduced write current output; this signal indicates to the drive that a reduced write current is to be used.
36*	SC	SEEK COMPLETE	I	When active this indicates drive stepping has settled.
36**	CC	COMMAND COMPLETE	I	When active this indicates drive has completed requested command.
24†	WD	WRITE DATA	O	RLL/MFM/NRZ write data is shifted out at rate determined by write clock. Write data should be synchronized by a D-flip flop clock at twice the data rate. WD has an active pullup and pulldown output. The output can sink 6.0mA.
29†	WC	WRITE CLOCK	O	Write clock frequency at bit rate.
26*	$\overline{\text{EARLY}}$ /	$\overline{\text{EARLY}}$ /		$\overline{\text{EARLY}}$, along with $\overline{\text{LATE}}$, is used to indicate the delay value for precompensation. The output is valid when write gate (WG) is active.
26**	AME	ADDRESS MARK ENABLE		When NRZ disk data format is selected this output becomes AME and is connected to the Address Mark Enable input of the ESDI drive. It is used to control writing of the address mark and PLO field.
				$\overline{\text{EARLY}}$/AME has active pullup and pulldown output. The output can sink 6.0mA.
25*	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	O	$\overline{\text{LATE}}$ (along with $\overline{\text{EARLY}}$) is used to indicate the delay value for precompensation. This output is valid when write gate (WG) is active.
25**	$\overline{\text{WCOUT}}$	$\overline{\text{WRITE CLOCK OUT}}$		When NRZ encoding in ESDI mode is selected, this output becomes $\overline{\text{WCOUT}}$. $\overline{\text{WCOUT}}$ is the WC input in inverted and is connected to the WC input of the ESDI drive.
				$\overline{\text{LATE}}$ has active pullup and pulldown output. The output can sink 6.0mA.

TABLE 3. DRIVE INTERFACE PIN DESCRIPTION (Continued)

| PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
41†	RD	READ DATA	I	Single ended input which receives RLL/MFM/NRZ data from the drive. Binary data and clock are internally separated from the RLL and MFM encoded data in ST506 mode.
43†	RC	READ CLOCK	I	Typically generated from an oscillator phase-locked to read data.
42†	RG	READ GATE	O	This signal is inactive until a search is started for an address mark.
38 *	DRUN /	DATA RUN INPUT	I	In MFM or RLL mode, this input is DRUN and indicates a sequence of '0's in RLL or a sequence of '0's or '1's in MFM.
38 * *	SCT	SECTOR PULSE	I	In NRZ mode, this input becomes SCT (DRUN will be generated internally). SCT is connected to the Sector/Address Mark Found output of the ESDI drive. It signals the start of a sector on the drive.
17 *	RLL	RLL DISK DATA	O	This pin is high when RLL disk data format has been selected. This pin is low when MFM or NRZ disk data format has been selected.

* RLL and MFM encoding in ST506 mode.
* * NRZ encoding in ESDI mode.
† Both RLL and MFM encoding in ST506 mode and NRZ encoding in ESDI mode.
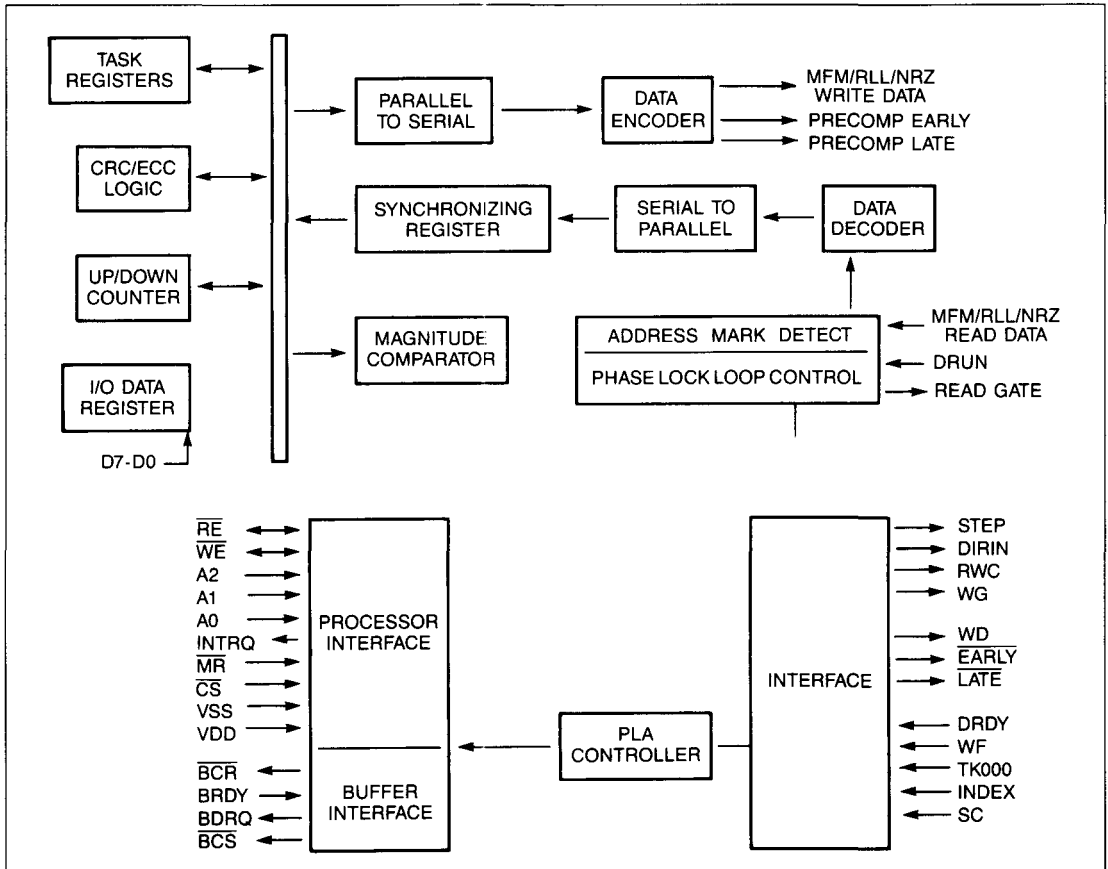
FIGURE 1. WD50C12 BLOCK DIAGRAM
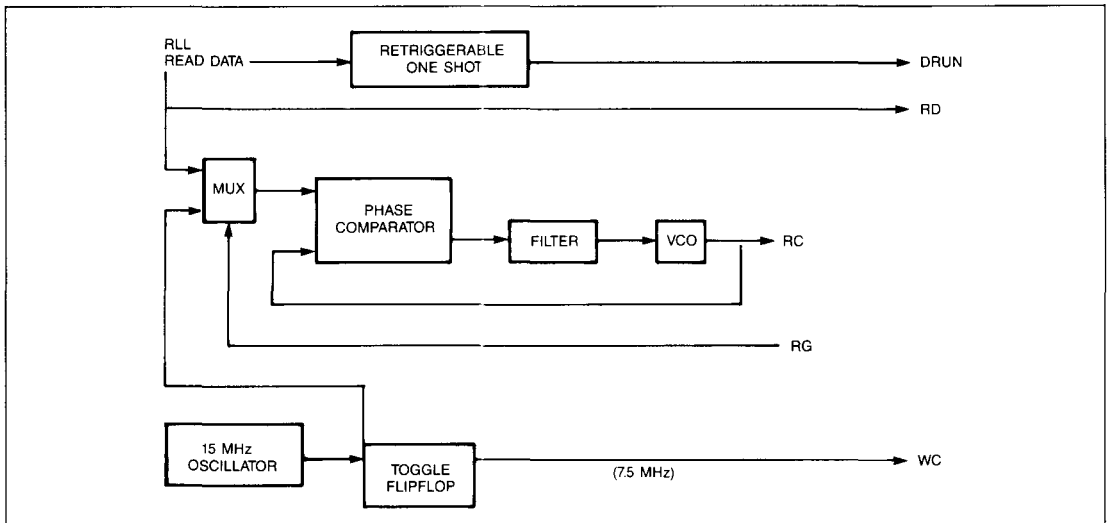
FIGURE 2. PHASE LOCK LOOP CONTROL BLOCK DIAGRAM FOR 7.5MHz RC/WC

ARCHITECTURE

The controller is composed of the following major sections: PLA Control, CRC/ECC Logic, MFM/RLL/NRZ Decoding, Address Mark Detector, Buffer and DMA Control and Task File. The controller is designed to operate with 2 clock inputs: RC and WC. These clocks come from the data separator. The PLA controller, processor interface, and buffer control sections use the write clock input. The read clock input is used for MFM, RLL, or NRZ decoding and will be 10MHz for a 10 Mbit/sec data rate. The write clock input is used for MFM, RLL, or NRZ encoding. It will be at a frequency of 10 MHz for a 10 Mbit/sec data rate.

Programmable Logic Array (PLA) Controller

The PLA Controller interprets read, write, etc. commands; its operation is synchronized with the WC input. The PLA controller is started when a command is written into the command register. It generates control signals and operates in a handshake mode when communicating with the RLL and MFM decoding block in ST506 mode. The RLL and MFM decoding block in ST506 mode uses the RC input which may be asynchronous to WC.

Magnitude Comparator

An 11 bit magnitude comparator is used for calculation of drive step direction and number of step pulses between present cylinder position and desired position. A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

CRC/ECC Generator and Checker

The CRC mode of operation, defined by the SDH (Sector Size, Head, drive select) Register (Bit 7 = 0), provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it. (Bit 7 of the SDH register will not implement CRC mode for data fields when RLL mode is selected.)

The CRC/ECC generator computes and checks the cyclic redundancy check characters appended to the ID and data fields written on the disk. The CRC polynomial used is,

$$X^{16} + X^{12} + X^5 + 1.$$

The CRC register is preset to all ones before computation starts.

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by setting bit 4 of the Error Register. If the failure is in the data field, bit 6 of the Error Register is set.

A 32 bit or 56 bit ECC polynomial may be selected instead of the CRC polynomial for the data field. The CRC/ECC selection is controlled by bit 7 of the SDH register when the controller is in MFM or NRZ modes. CRC is selected when bit 7 of the SDH register is 0 in MFM or NRZ modes. ECC is selected when bit 7 of the SDH register is 1 in MFM or NRZ modes, and the polynomial chosen (32 or 56 bit) depends on the value of bit 2 in the set parameter command. However, when RLL mode is selected, the default becomes 56 bit ECC and the CRC or 32 bit ECC options are not usable.

The ECC mode of operation (SDH 7 = 1) is only applicable to the data field. This feature built into the WD50C12 provides the user with the ability to detect and correct errors in the data field automatically.

The following is a summary of the parameters considered when ECC is used:

1. SDH Register bit 7.
2. Read Command bit 0 (T).
3. Read and Write Command bit 1 (L).
4. Compute Correction Command.
5. Set Parameter Command.
6. Error correction successful, bit 2 of the Status Register.
7. Error occured, bit 0 of the Status register.
8. Uncorrectable error, bit 6 of the Error Register.

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode, for MFM and NRZ only.

The T bit (bit 0) within the Read Command controls whether or not error correction is attempted.

When T = 0 and an error is detected, the WD50C12 tries up to 10 times to correct the error. If successful, bit 2 of the Status Register is set. The Host can interrogate the Status Register and detect that a problem existed, but was corrected. When the error is uncorrectable, the error bit (bit 0) of the status register is set, and bit 6 of the Error Register is set. The Host can read the data, even though errors exist.

When T = 1, and an error is detected, no attempt is made to correct it and bit 0 of the Status Register and bit 6 of the Error Register are set. The user now has two choices:

1. Ignore the error and make no attempt to correct it.
2. Use the Compute Correction Command to determine the pattern and location of the error, and correct it within the user's program.

When implementing the Compute Correction Command, use it before executing commands that alter the content of the ECC Register. The Read, Write, Scan, and Format commands can alter the syndrome and make correction impossible. If the Compution Correction Command determines that the error is uncorrectable, then the error bits in the Status Register and Error Register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The 32-bit ECC polynomial is,

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$$

and is the same one used in the WD1002 Winchester controller board. The 32-bit ECC polynomial has an 11 bit maximum single burst correction span. The reverse 32-bit ECC polynomial is,

$$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1.$$

The non-detection probability for the 32-bit ECC polynomial is,

$$2.3 \ (E-10), r = 516 \times 8, b = 5$$

and the miscorrection probability is,

$$1.57 \ (E-5), r = 516 \times 8, b = 5$$

The 56-bit ECC polynomial is,

$$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^8 + 1.$$

The 56-bit ECC polynomial has a 22 bit maximum single burst correction span.

The reverse 56-bit ECC polynomial is,

$$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1.$$

The non-detection probability for the 56-bit ECC polynomial is,

$$1.39 \ (E-17), r = 519 \times 8, b = 11$$

and the miscorrection probability is,

$$5.84 \ (E-11), r = 519 \times 8, b = 11$$

For auto correction the external data buffer must be implemented with a static RAM and counter, not a FIFO memory.

The Set Parameter Command selects the number of bits in the correction span, through the use of bit 0.

Read and Write Commands, with the L bit (bit 1) equal to one, are referred to as Read Long and Write Long Commands. With these commands, no ECC or CRC characters are generated or checked by the WD50C12. In effect the 4 or 7 ECC bytes are handled as an additional 4 or 7 bytes of data which pass through the data buffer. With proper use of the Write, Read Long, Write Long, and Read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

For CRC/ECC calculations, the CRC/ECC register is initialized to all 1's. For CRC/ECC purposes only, the Address Mark byte has a value of 'A1' and is included in the CRC/ECC calculations.

RLL and MFM Encoding/Decoding in ST506 Mode

The RLL and MFM encoding in ST506 mode data section receives 8 bit parallel data and generates RLL and MFM encoded write data in ST506 mode. This section operates with a write clock having a frequency of the desired bit rate. The write clock need not be synchronized to read clock (RC).

Data bytes are written to the drive MSB first.

The MFM decoding section generates 8 bit binary data from MFM data once an address mark has been detected.

The RLL decoding section generates 8 bit parallel data from the RLL data once an address mark has been detected. The RLL coding rules are given below.

RLL CODE RULES

NRZ Data		RLL Code Word Output							
First Bit	Last Bit	First Bit							Last Bit
1 1	X X	1	0	0	0	X	X	X	X
1 0	X X	0	1	0	0	X	X	X	X
0 1	1 X	0	0	1	0	0	0	X	X
0 1	0 X	0	0	0	1	0	0	X	X
0 0	0 X	1	0	0	1	0	0	X	X
0 0	1 1	0	0	0	0	1	0	0	0
0 0	1 0	0	0	1	0	0	1	0	0

When NRZ mode is selected, the MFM/RLL encode and decode logic is bypassed. NRZ read data is clocked in on the rising edge of Read Clock and NRZ write data is clocked out on the rising edge of Write Clock.

Address Mark Detector

An address mark is a unique 2 byte code placed at the beginning of each ID field or data field. A series of zero bytes always precedes each address mark. The address mark detector section begins searching for an address mark when synchronization has been lost and after a series of zero bytes is detected. The detection of an address mark establishes resynchronization; coding of the second byte of the address mark specifies the type of field.

The address mark is composed of a 2 byte sequence; the first byte is used for resynchronization and the second byte specifies ID or data field. For the MFM mode the first byte is an A1 (hex) byte with missing clock (data = A1, clock = 0A). The second byte is encoded with normal MFM rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In RLL mode the first byte is a unique code which violates normal RLL coding rules but does not violate the 2,7 timing rule. The second byte is encoded with normal RLL rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field. The RLL address mark pattern is 1000 0000 1001 0000 (8090 hex).

In NRZ mode, an NRZ 'A1' byte establishes byte synchronization. When the WD50C12 is used to control an ESDI (NRZ) drive, the Sector Pulse (Address

Mark Found) signal will qualify Read Data to prevent false address mark detection.

Host Interface

The primary interface between the Host processor and the WD50C12 is an 8-bit bi-directional bus. This bus is used to transmit and receive data for both the WD50C12 and the Sector Buffer. The Sector Buffer consists of either a FIFO memory, or a static RAM and counter. Since the WD50C12 makes the bus active when accessing the Sector Buffer, a tranceiver must be used to isolate the Host during this time. Figure 3 illustrates a typical interface with a Sector Buffer, implemented with a RAM memory. Whenever the WD50C12 is not using the Sector Buffer, it gives control of the Sector Buffer and data bus to the Host by de-asserting its output term, $\overline{BCS}$. This de-selects the Sector Buffer and switches the data bus transceivers.

When the Host wants to access the Sector Buffer it produces an address of zero (A0 thru A2 $\neq$ 0). A decoder recognizing A0 thru A2 $\neq$ 0 asserts a $\overline{BCS}$ of its own. The Host then asserts $\overline{WE}$ or $\overline{RE}$ for the counter, at the leading edge, the location within the Sector Buffer addressed by the counter is accessed, at the trailing edge the counter advances to the next count. The decoder asserts $\overline{CS}$ to the WD50C12 any time the address does not equal zero (A0 thru A2 $\neq$ 0).

During Write Sector commands the Host sets up data in the Task File and issues the command. The WD50C12 asserts $\overline{BCR}$ to zero the counter. It then generates a BDRQ status to inform the Host it can load the Sector Buffer with the data to be written.

When the counter reaches its maximum count, BRDY is asserted by the carry out of the counter, informing the WD50C12 that the Sector Buffer is full. (BRDY is asserted with a rising edge and is ignored if asserted before the WD50C12 asserts $\overline{BCR}$.) $\overline{BCS}$ is then asserted, disconnecting the Host through the transceivers, and $\overline{RE}$ and $\overline{WE}$ become outputs from the WD50C12 to allow access to the Sector Buffer. When the WD50C12 is done using the Sector Buffer, it deasserts $\overline{BCS}$. This allows the Host to access the local bus.

The Read Sector Command operates in a similar manner, except that the Sector Buffer is loaded by the WD50C12 instead of the Host.

When the BDRQ is used, it can either be connected to a DMA controller or used for programmed I/O. In either case it signals that the WD50C12 is ready to receive or transmit data. DRQ status bit (if used) must be polled by the Host; therefore, it is limited to programmed I/O.

When INTRQ is asserted, the Host is signaled that a command has terminated (either a normal termination or an aborted command). In the case of the Read Command, INTRQ can be programmed by bit 3 to be asserted upon termination as the other commands, or at the same time BDRQ is asserted, if m = 0 or for the last sector, if m = 1. In either case, INTRQ remains asserted until the Host reads the Status Register to determine the result of the termination, or writes a new command into the Command Register.

The WD50C12 asserts $\overline{SDHLE}$ to the Host whenever writing to the SHD register. Thus the same information can be stored in an external register for decoding.
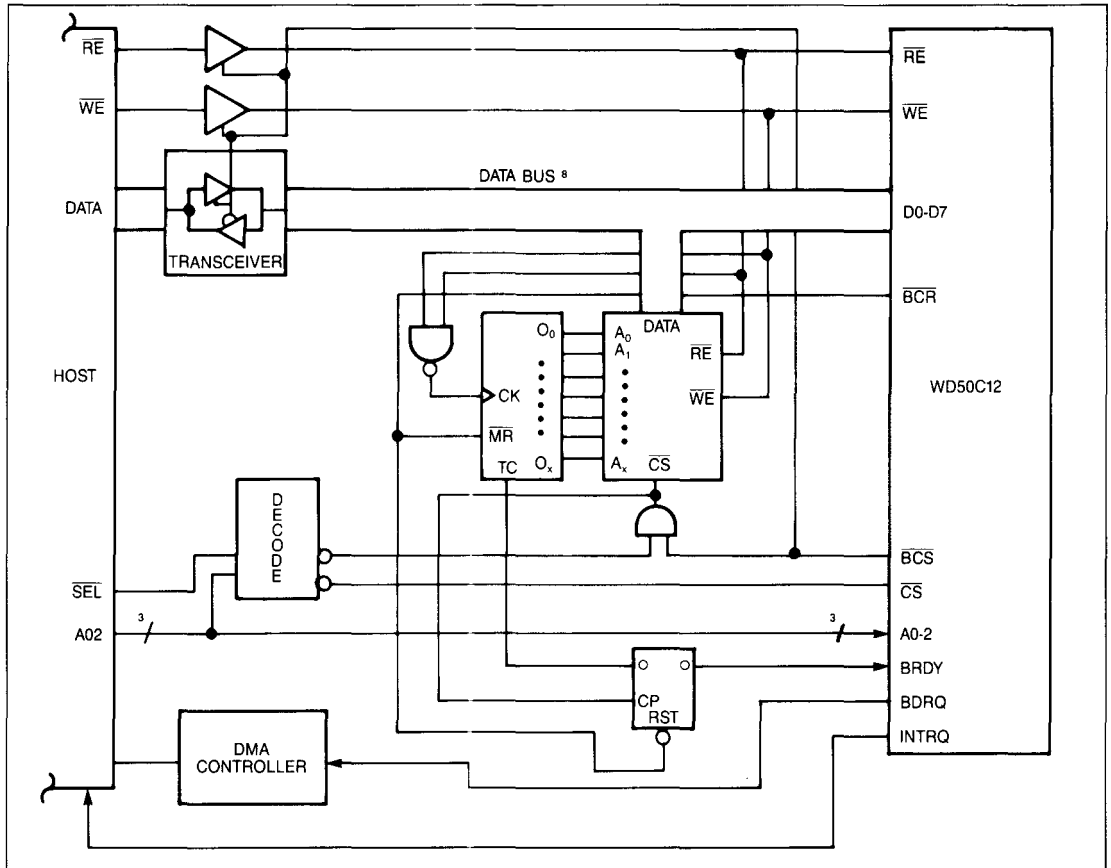
FIGURE 3. HOST INTERFACE

Drive Interface

The drive side of the WD50C12 controller requires three sections of external logic. These are interface buffers, data separator, and write precompensation. Figure 4 illustrates the drive interface.

The control lines are buffered, single-ended, and resistor terminated at TTL levels. The data lines to and from the drive also require buffering, and are terminated with RS-422 drivers. The interface specifications for the drive can be found in the manufacturer's manual. The WD50C12 supplies TTL compatible signals, and interfaces with most driver devices.

When writing to the SDH Register, the Head and Drive select signals are latched externally by the latch enable signal $\overline{SDHLE}$.

The data recovery circuits consist of a phase lock loop, data separator, and associated components. The WD50C12 interacts with the data separator through DRUN and RG. Data read from the drive is presented to the RD input of the WD50C12, the reference

multiplexor, and a retriggerable one shot. The RG is de-asserted when the WD50C12 is not inspecting data and the PLL stays locked to the reference clock.

The Write Precompensation circuitry is designed to reduce the shift in the data caused by the effect one bit has over another. The Write precompensation logic is divided into two areas: RWC and $\overline{Early}$ or $\overline{Late}$ writing of the bits.

RWC is controlled by the Write Precomp/PLO Length/ Gap Length Register in the Task File. This register is written into by the Host. When a cylinder is called for that is equal to, or greater than the content of this register, the write current will be reduced, thus lessening the effect one bit can have on another.

Shift may also be caused by the bit pattern. With certain combinations of ones and zeros some of the bits can drift far enough apart to become difficult to read without error. This phenomenon can be miminized by using EARLY and LATE as described under MFM Encoder.
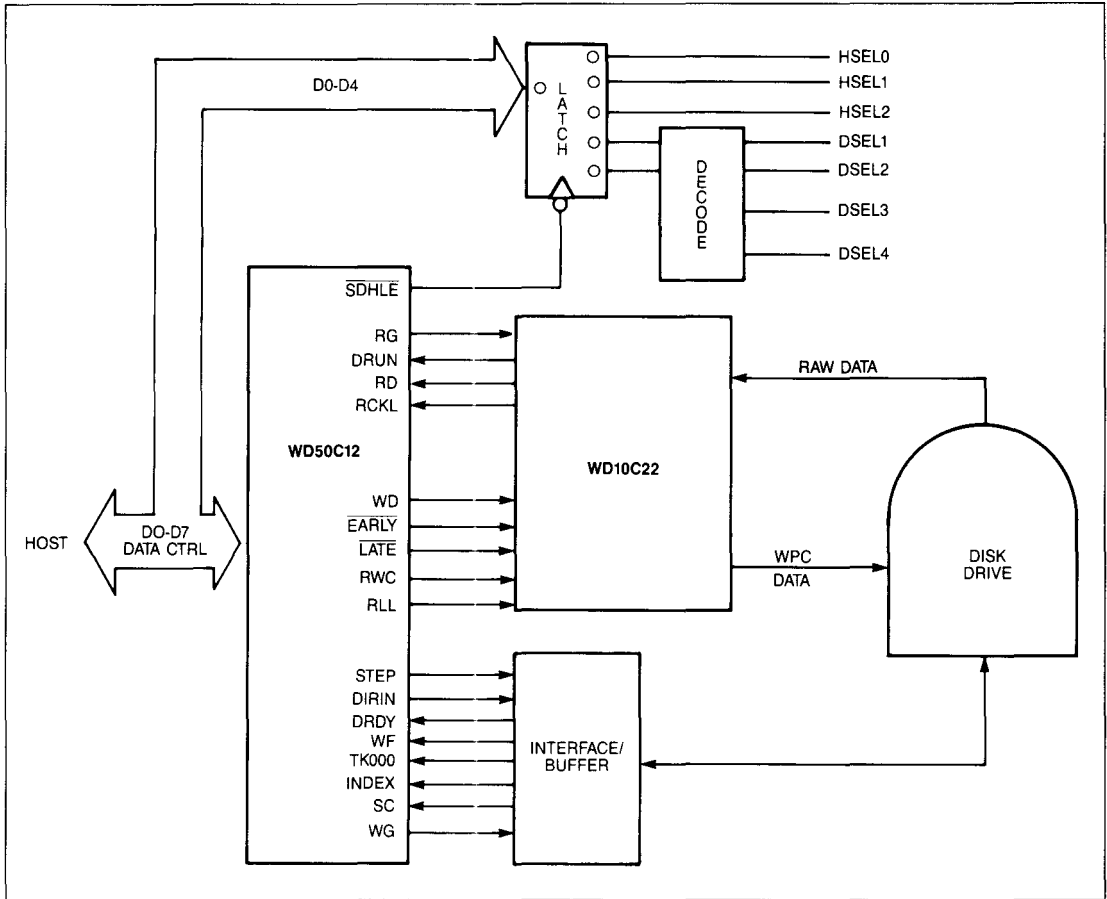
FIGURE 4. DRIVE INTERFACE BLOCK DIAGRAM

Controller to Data Separator Interface

The read interface section generates Read Gate from signals sent by the PLA controller and by the DRUN input. The block diagram of a phase lock loop circuit compatible with the WD50C12 controller is shown in Figure 2. In this system, raw read data from the drive is presented to the RD input.

Read Gate is inactive when the controller is not inspecting read data. The phase lock loop uses the write lock as a reference at this time. When a read command is started and a search begins for an address mark, the DRUN input is examined. Since each address mark should be preceded by approximately 12 bytes of zeros, when a sequence of zeros is detected by the activation of DRUN, Read Gate is activated and read data is examined until either an address mark is detected or a non-zero byte which is not an address mark is detected.

When an address mark is detected, and it is preceded by at least 8 bytes of zeroes, read gate is held high and the ID or data field can be read. After reading the ID field, the sector transfer is performed. The address mark stays active for ID and data fields and deactivates for write splice areas.

If a non-zero non-address mark byte is detected, read gate is dropped for at least 2 byte times, allowing the phase lock loop to resynchronize with the write clock, before inspecting DRUN input again.

If the ID bytes do not match, or an address mark is not preceded by 8 bytes of zeroes with 6 coming after RG on, RG is lowered and DRUN is inspected again for a sequence of zeros. The above control sequence is detailed in a flow chart shown in Figure 6.

The WD50C12 Winchester disk controller is specifically designed to be compatible with the WD10C22B Read/Write Channel LSI device. When the

WD50C12 is used with the WD10C22B, excess noise is removed and a clean digital read signal is available to the controller.

The write precompensation circuitry in the controller to drive interface is designed to reduce the effect one bit has on another.

The write precompensation logic consists of two parts: RWC and shifting of the bits as they are written. The RWC (reduced write current) is controlled by the Write Precomp/PLO Length/Gap Length Register (register 1, write). For any cylinder greater than that specified by this register the write current will be reduced by having the RWC output go high.

The shifting of the data bits is controlled by the $\overline{EARLY}$ and $\overline{LATE}$ outputs. These two outputs should be used to delay the output as follows:

$\overline{EARLY}$	$\overline{LATE}$	Delay
0	1	no delay
1	1	one unit delay
1	0	two units delay

The $\overline{EARLY}$ and $\overline{LATE}$ outputs are generated according to the following rules.

For RLL:

RLL Coded Data Pattern									
Preceding Bits				Comp. Bit	Following Bits				Precomp
0	1	0	0	1	0	0	0	1	None
0	1	0	0	1	0	0	0	0	EARLY
X	0	0	0	1	0	0	0	X	None
1	0	0	0	1	0	0	1	0	None
0	0	0	0	1	0	0	1	0	LATE
0	1	0	0	1	0	0	1	0	None

For MFM:

MFM Coding - NRZ Data Pattern									
Preceding Bits				Comp. Bit	Following Bits				Precomp
X	X	X	1	1	0	X	X	X	EARLY
X	X	X	0	1	1	X	X	X	LATE
X	X	0	0	0	1	X	X	X	EARLY
X	X	1	0	0	0	X	X	X	LATE

* Note: The rules for RLL refer to the encoded bit stream. The rules for MFM refer to the NRZ data prior to being encoded.
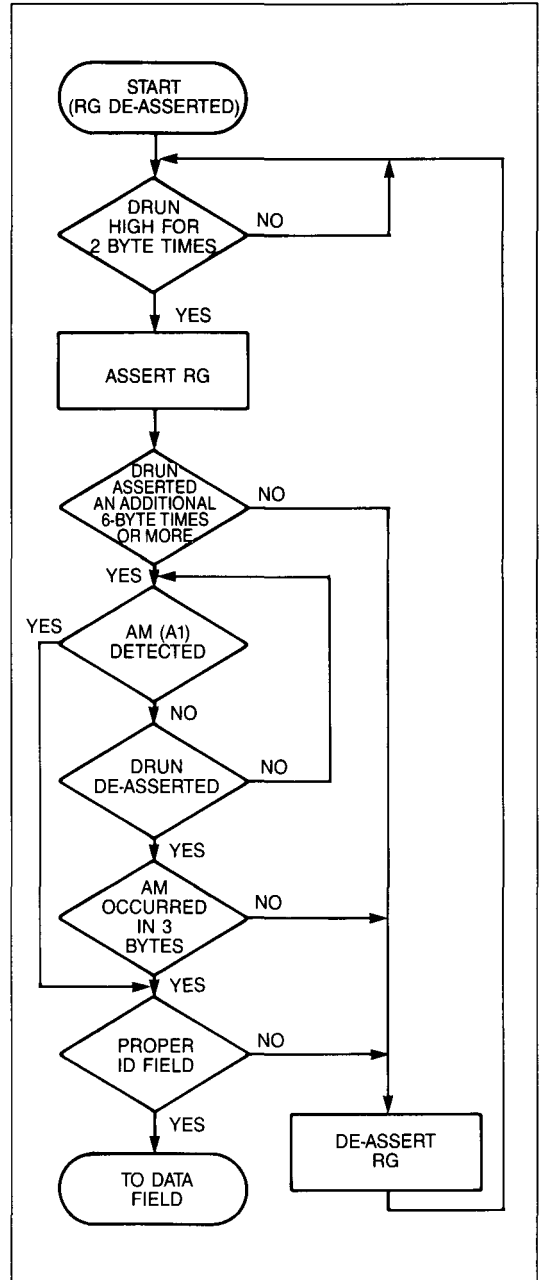
FIGURE 5. PLL CONTROL SEQUENCE FOR ID FIELD
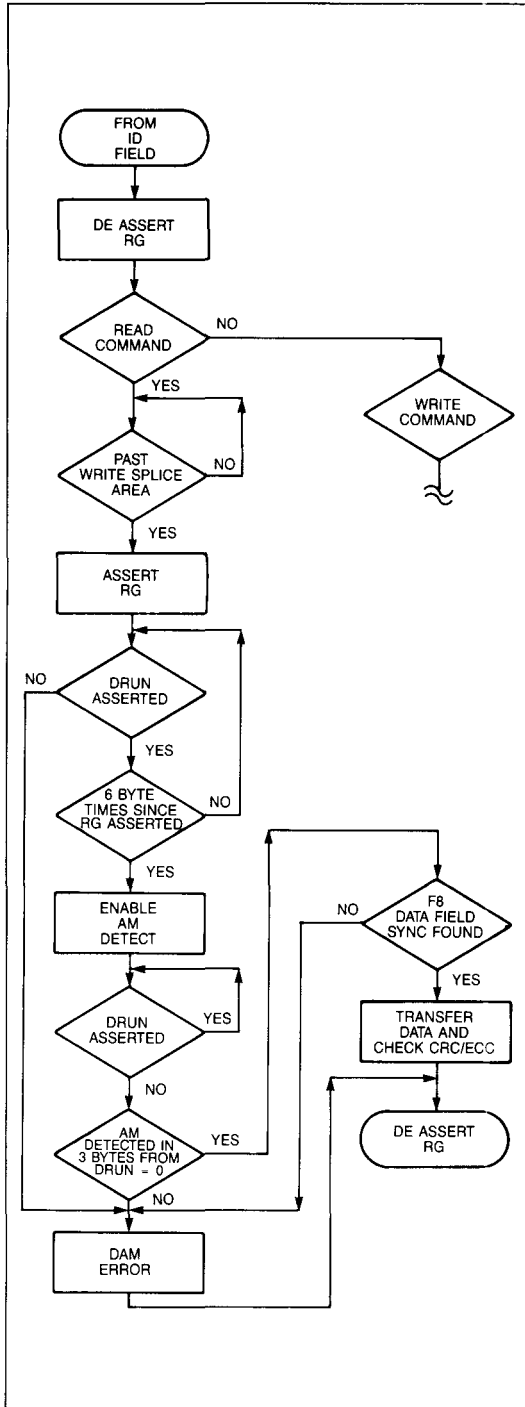
FIGURE 6. PLL CONTROL SEQUENCE FOR DATA FIELD

TASK FILE

The task file is a set of registers which contain the command, status, track, sector and other task information. Nine registers are accessed via A2 to A0.

Register selection is as follows:

ADDRESS			TASK FILE	
A2	A1	A0	Read	Write
0	0	0	BUS TRI-STATED	BUS TRISTATED
0	0	1	Error Flags	Write Precomp/ PLO/Gap
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Number Low	Cylinder Number Low
1	0	1	Cylinder Number High	Cylinder Number High
1	1	0	SDH	SDH
1	1	1	Status	Command

The status and error registers are read-only, the command and write precomp track registers are write only, and the remaining registers are read/write. The registers are described below.

ERROR REGISTER (A2, A1, A0 = 1, READ)

The error register is read-only and contains the specific error status pertaining to a command. This register is written by the local microcontroller. The meaning of the status register bits are as follows:

Bit	7	6	5	4	3	2	1	0
	BB	CRC/ECC	0	ID	0	AC	TK	DM

BIT 7 — Bad Block

A bad block address mark has been detected when trying to read or write that sector. The data field will not be read or written.

BIT 6 — CRC/ECC Data Field Error

A CRC error in the data field has been detected when in CRC mode. If retries were not disabled, the data was re-read automatically for 10 disk revolutions and each time a CRC error has been found. In ECC mode, data errors were detected and the data re-read for 10 disk revolutions; each time, the auto-correction process failed to correct the data. If retries were disabled, the data was not re-read. In ECC mode, no attempt to correct the data was made. The data contained in the buffer can be read but contains errors.

BIT 5 — Reserved

Not used, forced to zero.

BIT 4 — ID Not Found

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For a

Scan ID command, this bit is set after 10 index pulses if the retry disable bit is not set, otherwise this bit is set after 2 index pulses if no ID field was found. For Read and Write Sector commands with the retry disable bit set, this bit indicates that after 10 index pulses, an auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set, then no matching ID field was found after 2 index pulses; no auto-scan or auto-seek is performed.

BIT 3 — Reserved

Not used, forced to zero.

BIT 2 — Aborted Command

Set if command was started and one of the following conditions occurred:

1. Drive not ready
2. Write fault
3. Illegal command code.

BIT 1 — TK000 Error

Occurs in restore command when TK000 pin not active after 2047 steps.

BIT 0 — Data Address Mark Not Found

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for Read Sector commands only.

WRITE PRECOMP/PLO LENGTH/GAP LENGTH REGISTER (A2, A1, A0 = 1, write)

Bit	7	6	5	4	3	2	1	0
	(RWC)/(PLO)/GAP CONTROL							

The Write Precomp/PLO Length/Gap Length Register has three different uses:

1. To control the RWC (reduced write current) pin. The Write Precomp/PLO Length/Gap Length Register may contain any value from 0 to 255. The RWC pin is high when the Cylinder Register is greater than or equal to four times the Write Precomp/PLO Length/Gap Length Register value; the RWC ST506 mode switching point may thus be at track 0, 4, 8, ... 1020. If the Write Precomp/PLO Length/Gap Length Register value is 255, the RWC pin is always forced low.

2. To determine ID PLO lengths for ESDI mode. The content of the Precomp/PLO Length/Gap Length Register is used to extend the ID PLO beyond normal length if the B Option is selected on the FORMAT COMMAND. The value of the ID PLO will be the Precomp value + 11 Bytes in ESDI mode.

3. To determine the length of the data PLO field during Write commands in ESDI mode.

4. To load a value into an internal Gap register. During the Auxilliary Set Parameter command the contents in the lower six bits of the Write Precomp/PLO Length/Gap Length Register are loaded into this internal Gap register. In hard sector ESDI (NRZ) mode this internal Gap register is used during Scan ID, Read, and Write commands to control the delay between the Index or Sector pulse and the rising edge of Read Gate. The Write Precomp/PLO Length/Gap Length Register is loaded with the desired value for the internal Gap register prior to issuing the Auxilliary Set Parameter command.

SECTOR COUNTS (A2, A1, A0 = 2)

Bit	7	6	5	4	3	2	1	0
	NUMBER OF SECTORS							

The sector count register is used in read sector, write sector and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count is decremented and the sector number is incremented after each sector transfer to or from the buffer.

SECTOR NUMBER (A2, A1, A0 = 3)

Bit	7	6	5	4	3	2	1	0
	SECTOR NUMBER							

The sector number register holds the number of the desired sector. The sector number can range from 0 to 255. During Format commands the Sector Number Register is used to control the Gap1 and Gap3 lengths. The sector number holds the number of gap bytes minus three for Format.

CYLINDER NUMBER REGISTERS

The Cylinder number may range in value from 0 to 2047. This register has two different uses:

1. When a seek is performed, the Cylinder number register is compared to an internal present position cylinder register to determine the direction and number of steps. The present position cylinder register is updated after the execution of the seek operation of a Restore, Seek, Read, Format, or Write command. The present position cylinder register is initialized by either Restore or Scan ID command. For Read Sector, Write Sector, Format, and Seek commands, if the drive number has been changed since the last command then an automatic Scan ID command is performed before seeking.

2. During an auxilliary set parameter command cylinder number register is used to specify the desired sector size if a non-standard sector size is desired. The content of the cylinder high/low is stored in the sector size register. However, the actual sector size will be Sector size register + 1.

Cylinder Number Low (A2, A1, A0 = 4)

This register holds the 8 least significant bits of the desired cylinder number or the 8 least significant bits of the desired sector size.

Bit	7	6	5	4	3	2	1	0
	LS BYTE OF CYLINDER NUMBER							

Cylinder Number High (A2, A1, A0 = 5)

This register holds the three most significant bits of the desired cylinder number or the three most significant bits of the desired sector size.

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	X	3 MS BITS OF CYLINDER NUMBER		

SDH REGISTER (A2, A1, A0 = 6)

SDH Register in 3-Bit Head Mode

When the 3 bit head select field size is selected, the default after a master reset, the SDH register is coded as follows:

SDH Register

Bit	7	6	5	4	3	2	1	0
	CRC/ ECC	Sector Size		Drive Number		Head Number		

BIT 7 — ECC/CRC Select

This bit is set for data field ECC mode. It is reset for data field CRC mode. In RLL mode this bit is ignored. RLL mode always uses 7-byte ECC. The CRC/ECC flag bit is not written onto the disk at format time; the Bad Block flag is written on the disk in its place.

BIT 6 and BIT 5 — Sector Size

Bits 6 and 5 contain sector size bits. These bits are written onto the disk at format time. The sector size is dependent on the sector size bits and the data interface mode (MFM, RLL, or NRZ).

The possible sector sizes and their selection codes are:

Bit 6	Bit 5	Sector Size
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field
1	1	128 byte data field

The sector sizes can be optionally specified to be any value between 100 and 2048 bytes by using the auxilliary set parameter command.

BIT 4 and BIT 3 — Drive Number

Bits 4 and 3 specify Drive Number. Since there are no Drive Select outputs from the WD50C12, these bits must be externally decoded and latched to perform the select function. These bits are not recorded on the disk.

BIT 2, BIT 1, and BIT 0 — Head Number

Bit 2, 1 and 0 specify Head number. Again, head selects do not exist as outputs of the WD50C12 and must be externally latched. However, the WD50C12 uses these bits for format purposes and ID field compares. These bits are written on the disk at format time.

The SDH byte written in the ID field during a format command is not the same as the SDH register. The SDH format byte is shown below.

SDH ID Field Format Byte (3-bit Head Mode)

Bit	7	6	5	4	3	2	1	0
	Bad Block	Sector Size		0	0	Head Number		

SDH Register in 4-BIT Head Mode

When the 4 bit head select field size is selected the SDH register is coded as follows:

Bit	7	6	5	4	3	2	1	0
	CRC/ ECC	Sector Size		Drive Number	Head Number			

BIT 7 — ECC/CRC Select

See SDH Register in 3-Bit Head Mode.

BIT 6 and BIT 5 — Sector Size

See SDH Register in 3-Bit Head Mode.

BIT 4 — Drive Number

Bit 4 specifies the Drive Number. See SDH Register in 3-Bit Head Mode for Bits 3 and 4.

BIT 3, BIT 2, BIT 1, and BIT 0 — Head Number

Bits 3, 2, 1 and 0 specify Head number. See SDH Register in 3-Bit Head Mode for Bits 2,1,0.

The SDH byte written in the ID field during a format command is not the same as the SDH register. The SDH format byte is shown below.

SDH ID Field Format Byte (4-bit Head Mode)

Bit	7	6	5	4	3	2	1	0
	Bad Block	Sector Size		0	Head Number			

STATUS REGISTER (A2 thru A0 = 7, read)

The status register is read-only and reflects the status of the controller as well as the status of certain drive control lines.

If Busy (bit 7) is set then no other bits in the status register are valid. If Command In Progress (bit 1) is set then no other register reads are valid. The status register contents are returned instead.

The description of the status register bits follows:

Bit	7	6	5	4	3	2	1	0
	BSY	RDY	WF	SC	DRQ	DWC	CIP	ERR

BIT 7 — Busy

This bit is active (=1) when the controller is accessing the disk. BUSY is activated by the start of a command (writing into command register). It is deactivated at end of all commands except read sector. For read sector, BUSY is deactivated when a sector of data has been transferred to the buffer and data is available to the host.

BIT 6 — Drive Ready

This bit reflects the status of the DRDY. Any command will be aborted if DRDY is low.

BIT 5 — Write Fault

This bit reflects the state of the WF pin. Any command will be aborted if WF is high.

BIT 4 — Seek Complete

This bit reflects the state of the SC pin. This bit is latched after an aborted command error.

BIT 3 — Data Request

This bit reflects the state of the BDRQ pin. When active this bit indicates that a buffer data transfer is desired.

The data request flag is used for programmed I/O while the BDRQ pin is used for DMA controlled I/O.

BIT 2 — Data Was Corrected

This bit indicates that an error in the data field was detected and corrected. The buffer contains corrected data.

BIT 1 — Command In Progress

This bit indicates that a command is in progress and no new commands should be issued.

BIT 0 — Error

This bit indicates that a non-recoverable error has occurred. The error register will describe the error condition when this bit is active.

Drive ready, seek complete and write fault bits reflect the state of their associated input pins. The states of these status register bits are latched at the end of the command and are unlatched after the first status register read. When a command is in progress, Drive Not Ready or Write Fault conditions will be latched if the condition exists for at least 8 write clocks.

Reading the status register results in INTRQ being reset.

COMMAND REGISTER (A2 thru A0 = 7, write)

The command to be executed is written into this register. All other task information should be loaded into the task register file before loading the command register. Writing this register will set BUSY and CIP and will cause the controller to start executing the desired command. Writing this register will reset INTRQ.

Bit	7	6	5	4	3	2	1	0
				COMMAND				

COMMAND SUMMARY

The command codes are as follows:

COMMAND	(MSB) 7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0**
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	N	0	1	0	I	M	L	T
Read Next Data	N	1	1	0	I	0	L	1
Write Sector	N	0	1	1	0	M	L	T
Scan ID	0	1	0	0	0	0	0	T
Format	N	1	0	1	0	A*	B*	F*
Compute Correction	0	0	0	0	1	0	0	C
Set Parameter	Z	0	0	0	0	E	H	S
Aux. Set Parameter	1	0	0	0	1	D	K	U

* - These option bits should be zero (0) when RLL mode is selected.
** - If step rate is odd, 2 Index pulses trigger level sensing of SC.
** - If step rate is even, 10 Index pulses trigger level sensing of SC.

Stepping Rate Field R3 - R0∗∗∗

R3 R2 R1 R0		Step Time
0000	:	17.2 μs (microsec)
0001	:	0.25 ms (millisec)
0010	:	0.5 ms
0011	:	0.75 ms
0100	:	1.0 ms
0101	:	1.3 ms
0110	:	1.5 ms
0111	:	1.8 ms

∗∗∗ step rates are WC dependent.

Step rates and pulse widths are WC dependent. For slow step rates, pulse widths are 4 μs, and for fast step rates, pulse widths are 800 ns (for a 10 MHz WC). These values change to 8 μs and 1.6 μs, respectively, when WC is 5 MHz.

I - Interrrupt Control

I = 0 : Interrupt only occurs when BDRQ becomes active.

I = 1 : Interrupt occurs at end of command (after buffer has been read by host).

M - Multiple Sector Flag

M = 0 : Single sector read or write. The sector count is ignored.

M = 1 : Multiple sector read or write. Used for 1:1 interleave.

T - Retry Flag

T = 0 : Enable retries.

T = 1 : Disable retries.

L - Long Mode

L = 0 : Normal mode, selected ECC or CRC functions are performed.

L = 1 : Sector is extended by 4 or 7 bytes (depending on Set Parameter command). No ECC is generated or checked. ECC bytes passed externally.

N - Automatic Scan

N = 0 : Enable automatic ID scan on drive number change and enable implied seeks.

N = 1 : Disable automatic ID scan on drive number change and disable implied seeks. The cylinder number register is assumed to hold the current cylinder position. This option is used for serial mode ESDI.

B - Sync Field Length

B = 0 : ID PLO sync field length is fixed at 14.5 bytes.

B = 1 : ID PLO sync field length is programmable. The PLO Length Register specifies the desired PLO field length.

10MHz clock

R3 R2 R1 R0		Step Time
1000	:	2.0 ms
1001	:	2.3 ms
1010	:	2.5 ms
1011	:	2.8 ms
1100	:	3.0 ms
1101	:	3.3 ms (millisec)
1110	:	1.6 μs (microsec)
1111	:	8.0 μs (microsec)

A - Pad and Gap Value Control

A = 0 : ID CRC pad bytes are '00' if MFM or NRZ mode is selected. ID CRC pad bytes are '33' if RLL mode is selected.

A = 1 : ID CRC pad bytes are 'AA'. GAP1/GAP3 bytes are 'AA' if G = B = 0 or F = 0. See table below for more details.

F - Gap Value Control

F = 0 : GAP1/GAP3 bytes are '4E' if MFM or NRZ data interface GAP1/GAP3 bytes are '33' if RLL data interface.

F = 1 : GAP1 bytes are '00' and GAP3 bytes are 'FF' if G = 1. GAP1/GAP3 bytes are '00' if B = 1.

GAP1/GAP3 TABLE:

A	B	F	GAP1	GAP3	PAD
x	1	1	00	00	00
1	x	0	AA	AA	AA
1	0	1	AA	AA	AA
0	0	1	4E	4E MFM or NRZ	00
0	0	1	33	33 RLL	33
0	x	0	4E	4E MFM or NRZ	00
0	x	0	33	33 RLL	33

S - Error Correction Span

S = 0 : Error correction span = 5 bits if 4 byte ECC, 11 bits if 7 byte ECC.

S = 1 : Error correction span = 11 bits if 4 byte ECC, 22 bits if 7 byte ECC.

E - ECC Length/Sector Extension

E = 0 : Sector extension for read long / write long is 4 bytes. ECC generator/checker is 4 bytes. This bit is ignored if RLL is selected.

E = 1 : Sector extension for read long / write long is 7 bytes. ECC generator/checker is 7 bytes. This bit is ignored if RLL is selected.

H - SDH Register

H = 0 : SDH register is programmed for 2 drive select bits and 3 head select bits.

H = 1 : SDH register is programmed for 1 drive select bit and 4 head select bits.

C - Error Pattern (For Compute Correction Command)

C = 0 : Transfer 3 error pattern bytes.

C = 1 : Transfer 4 error pattern bytes. This bit is ignored if 7 byte ECC is selected.

Z - Data Mode Select 1

Z = 0 : MFM or RLL mode.

Z = 1 : NRZ mode if option bit K = 1.

K - Data Mode Select 2

K = 0 : Data interface is RLL. When this option is selected then the NRZ option is disabled. This is the default after a master reset.

K = 1 : Data interface is either MFM or NRZ.

Z	K	Mode
0	0	RLL
0	1	MFM
1	0	RLL
1	1	NRZ

U - Sector Size Select

U = 0 : Use the standard sector sizes as defined under the SDH register description.

U = 1 : Select user defined sector size. The sector size must be put into the cylinder registers prior to issuing an Auxilliary Set Parameter command.

D - Hard or Soft Sector Select

D = 0 : For operation with soft sector drives.

D = 1 : For operation with hard sector drives.

OPTION SUMMARY TABLE:

MODE	MODE CONTROL			OPTIONS											
	Z	D	K	I	M	T	L	A	B	F	S	E	H	C	U
RLL soft sector	.	0	0	x	x	x	x	0	0	0	x	*	x	*	x
RLL hard sector	.	1	0	x	x	x	x	0	x	0	x	*	x	*	x
MFM soft sector	0	0	1	x	x	x	x	x	0	0	x	x	x	x	x
MFM hard sector	0	1	1	x	x	x	x	x	x	0	x	x	x	x	x
NRZ soft sector	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x
NRZ hard sector	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x

. - Don't care, could be 0 or 1.
x - These options are supported.
* - These options have no affect.
0 - These options should be set to 0.

RESTORE COMMAND

The Restore command positions the read/write heads over track zero. The Host issues the Restore Command after the drive is turned on.

The SC (seek complete) determines the stepping rate. The WD50C12 issues a Step pulse and then waits for the leading edge of the seek complete before starting another step. If the leading edge of the SC is not observed within 2 or 10 revolutions (index pulses) the WD50C12 switches to sensing the level of SC. If after 2047 stepping pulses TK000 is not asserted, the WD50C12 sets the Track Zero error bit, asserts INTRQ and terminates the operation. An interrupt also occurs if WRITE FAULT is asserted or DRDY is de-asserted during execution.

The stepping rate field is stored in an internal register for future use by commands with implied seeks.

The Restore step rate is controlled by seek complete and is not affected by the R3 R2 R1 R0 rate. However, the R0 bit does control the Index time out to level sensing for the Restore command. When R0 is equal to 0, 10 Index Pulses then level sense. When R0 is equal to 1, 2 Index Pulses then sense level.
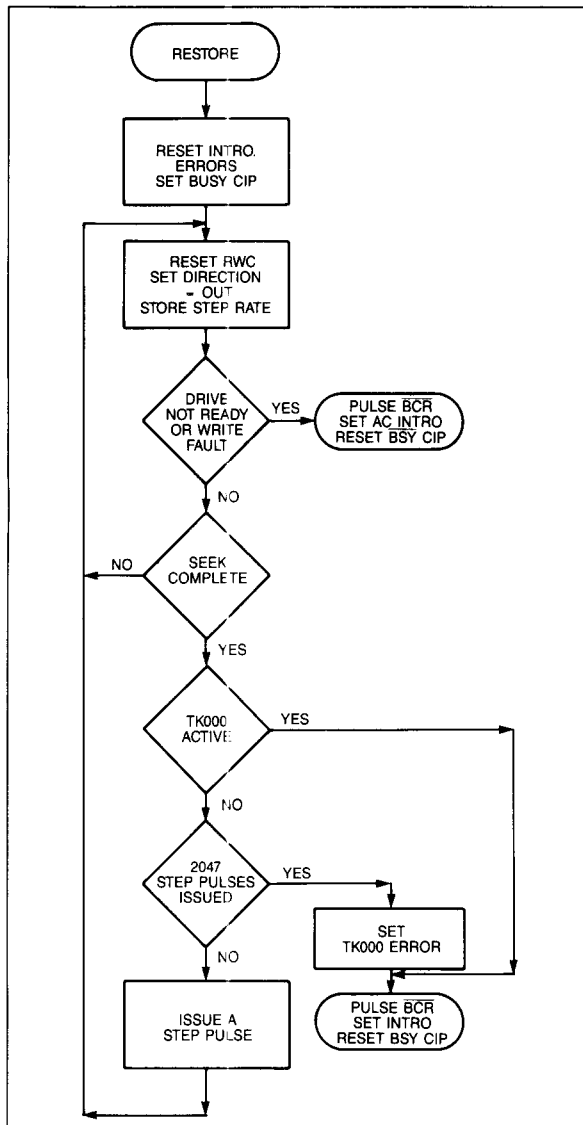
FIGURE 7. RESTORE COMMAND

SEEK COMMAND

The Seek Command goes to the track number specified in the task register file at the step rate specified by R3 R2 R1 R0. The controller keeps the present cylinder position for the current drive, but does not wait for seek complete (SC) at the end of the command. This allows overlapped seeks with the ST412 drive in RLL format and ST506 drive in MFM format.

If an implied seek is performed on a Read, Write, or Format command, the stepping rate for all but the last

step is controlled by R3 through R0 of the seek command. On the last step the seek continues until the leading edge of the seek complete is detected.

This signal is rising edge activated after the WD50C12 generates a step pulse. It is level sensed, if no step pulses are generated.

It also becomes level sensed if a rising edge of SC is not received within 2 or 10 disk revolutions after a step pulse. The 2 or 10 revolutions are dependent on the Retry mode.
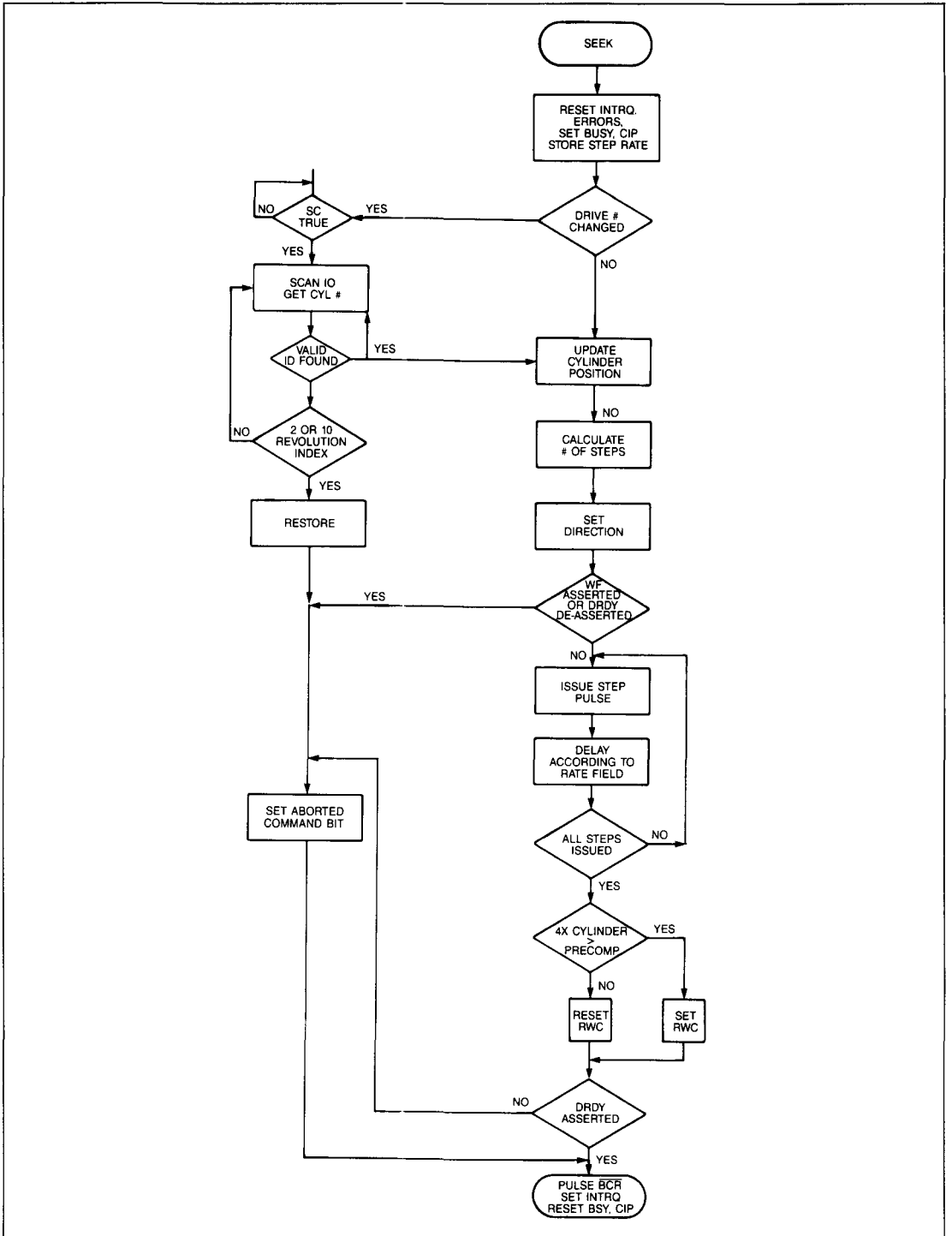
FIGURE 8. SEEK COMMAND

READ SECTOR

The Read Sector command transfers one or more sectors of data from the disk to the sector buffer. Upon receipt of this command, the WD50C12 compares the cylinder number in the Task File with the Present Cylinder Position Register. From this, the direction and number of steps required for the seek are calculated.

If the WD50C12 detects that the drive number has changed since the last Read command and if the N bit is 0, then an implied seek is performed.

If an implied seek is performed, the stepping rate for all but the last step is controlled by R3 through R0 of the last seek or restore command. On the last step the seek continues until the controller detects the leading edge of the seek complete (SC).

After the WD50C12 senses SC, it searches for an ID field with the specified cylinder, head, sector size, and CRC. When Retry is enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error after ten attempts, and auto-scan and auto-seek are done, then ten more tries are made before setting the ID Not Found Error. When Retry is disabled (T = 1) only two attemps are made before setting the ID Not Found Error, and no Auto-scan or auto-seek operations are done.

When the Data Address Mark is found the WD50C12 is ready to transfer data to the Sector Buffer. After the disk has filled the sector buffer, the WD50C12 asserts BDRQ and DRQ and then checks the I flag. If the flag is 0, INTRQ is asserted, signaling the Host to read the contents of the Sector Buffer. If the flag is 1, INTRQ occurs after the Host has read the Sector Buffer and terminates the command.

An optional M flag can be set for multiple sector transfers. When M = 0, then the sector specified in the sector number register is read. When M = 1, then multiple records are read. If the sector count register = 0, then 256 sectors are read at the desired track. If I = 0, then an interrupt occurs at the activation of BDRQ. If I = 1, then an interrupt occurs at the end of the command.

When M = 0 and T = 0, ID searches are retried for 10 index pulses, then an auto-scan and auto seek is done, then retried for 10 more index pulses. Data CRC errors and uncorrectable ECC errors will be retried for up to 10 index pulses. When T = 1, ID searches are retried for 2 index pulses, and no data CRC errors or uncorrectable ECC errors will be retried.

When L = 0, then normal CRC or ECC read commands are performed. When L = 1, then the CRC or ECC check bytes are not computed but instead, the CRC or ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 4 or 7 bytes. If ECC and retry modes have been selected and a data field error occurs, the WD50C12 (5012) will attempt to correct the data held in the sector buffer. If the error was uncorrectable, the sector will be re-read and a correction will be attempted again to a maximum of 10 times.

If after reading the correct ID field, the Data Address mark is not found a DAM error is set.

A bad block mark in the ID field sets the error bit and the data field is not read. If a bad block mark is found in an ID field during a multiple sector transfer, the command terminates.

WF and DRDY are monitored throughout the command. If WF becomes asserted, or DRDY de-asserted, the command terminates and the AC error flag is set. For a description of the error checking procedure on the data field see the explanation under the CRC and ECC Generator Checker. Both the Read and Write commands feature simulated completion to ease programming. BDRQ, DRQ, and INTRQ are generated in a normal manner upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.

When M = 0 (Single Sector Read)
(1)   Host: Sets up parameters; issues Read Sector command
(2)   50C12: Finds sector specified; asserts BCR and BCS, Sector Buffer data transfer via WE
(3)   50C12: Asserts BCR de-asserts BCS
(4)   50C12: Asserts BDRQ and DRQ flag
(5)   50C12: If 1 bit = 0, then (8)
(6)   Host: Reads contents of Sector Buffer (asserts RE)
(7)   50C12: Waits for BRDY then assert INTRQ; End
(8)   50C12: Asserts INTRQ
(9)   Host: Reads contents of Sector Buffer (asserts RE); End.

When M = 1 (Multiple Sector Read)
(1)   Host: Sets up parameters; issues Read Sector command
(2)   50C12: Finds sector specified; asserts BCR and BCS, Sector Buffer data transfer via WE
(3)   50C12: Asserts BCR de-asserts BCS
(4)   50C12: Asserts BDRQ and DRQ flag
(5)   Host: Reads contents of Sector Buffer (asserts RE)
(6)   Sector: Indicates data has been transferred by
      Buffer: asserting BRDY
(7)   50C12: Decrements sector count/increments sector number; go to (9), if sector count =0
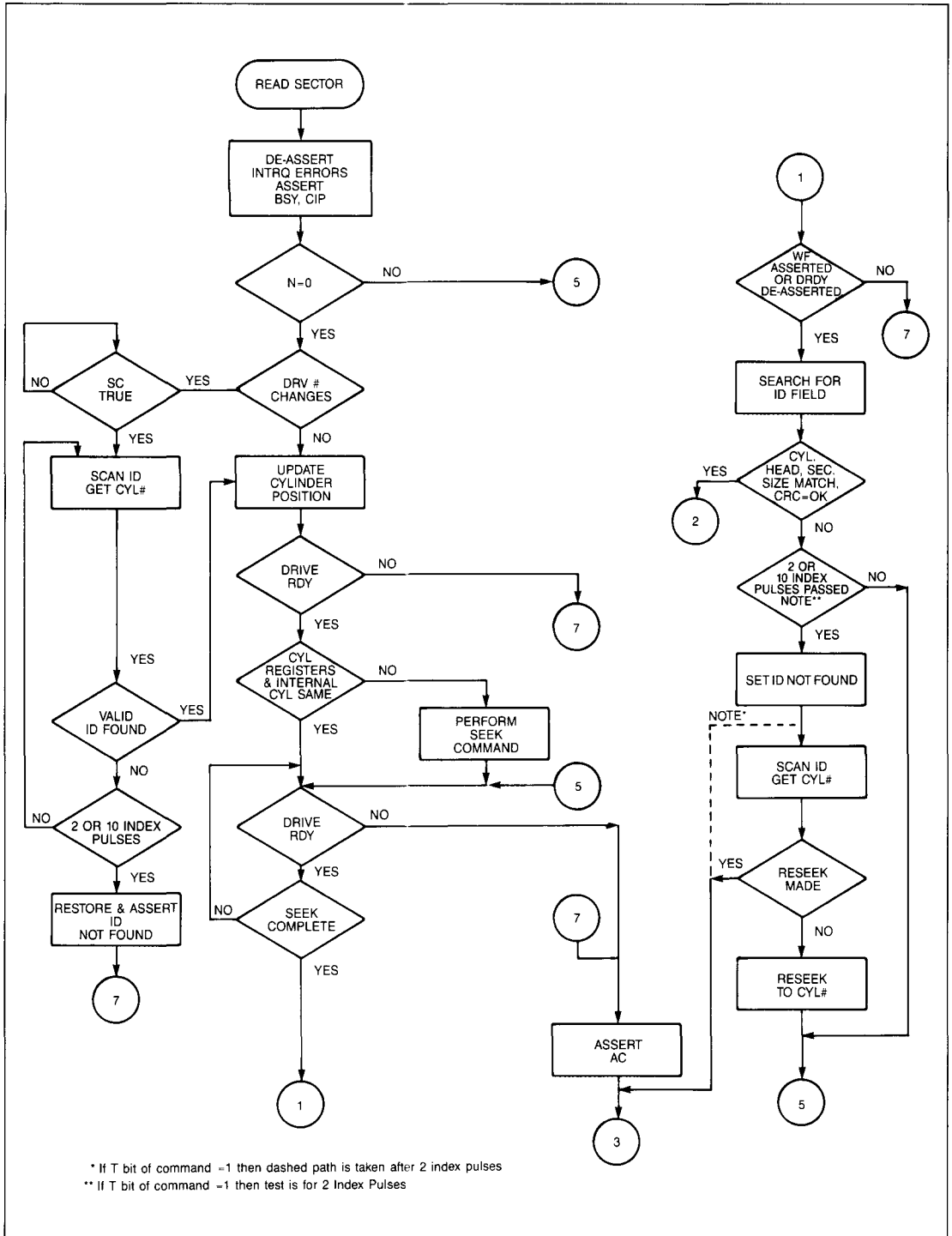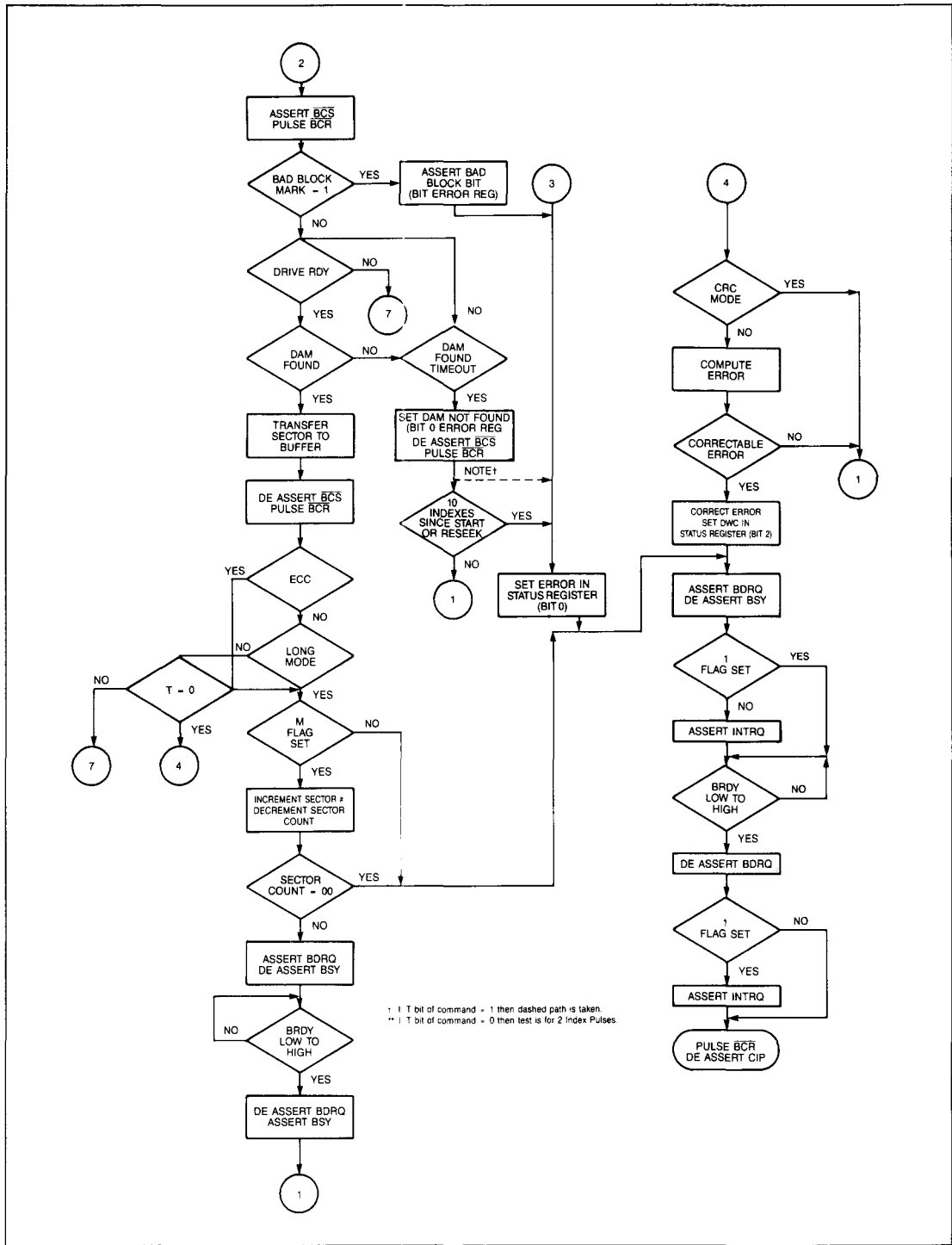(8)   50C12 Host: Go to step (2)
(9)   50C12: Asserts INTRQ; End

READ SECTOR

DE-ASSERT
INTRQ ERRORS
ASSERT
BSY, CIP

N=0 — NO → 5

YES

SC TRUE — YES → DRV # CHANGES

NO ← SC TRUE

YES

SCAN ID
GET CYL#

UPDATE
CYLINDER
POSITION

DRV # CHANGES — NO → UPDATE CYLINDER POSITION

DRIVE RDY — NO → 7

YES

CYL
REGISTERS
& INTERNAL
CYL SAME — NO → PERFORM SEEK COMMAND → 5

YES

VALID ID FOUND — YES → UPDATE CYLINDER POSITION

YES

NO

2 OR 10 INDEX PULSES — NO

YES

RESTORE & ASSERT ID NOT FOUND

7

DRIVE RDY — NO → 7

YES

SEEK COMPLETE

NO

YES

1

ASSERT AC → 3

1

WF ASSERTED OR DRDY DE-ASSERTED — NO → 7

YES

SEARCH FOR ID FIELD

CYL, HEAD, SEC, SIZE MATCH, CRC=OK — YES → 2

NO

2 OR 10 INDEX PULSES PASSED NOTE** — NO

YES

SET ID NOT FOUND

NOTE*

SCAN ID GET CYL#

RESEEK MADE — YES

NO

RESEEK TO CYL#

5

* If T bit of command =1 then dashed path is taken after 2 index pulses
** If T bit of command =1 then test is for 2 Index Pulses

FIGURE 9. READ COMMAND

21

FIGURE 9A. READ COMMAND (Continued)

READ NEXT DATA

The Read Next Data command finds the next data field and places it in a buffer. If the WD50C12 detects that the drive number has changed since the last Read command and if the N bit is 0, then an auto-scan ID is performed and step pulses are issued to update the present cylinder position.

The I flag controls interrupts the flow either at BDRQ or the end of the command. If I = 0, it interrupt at activation of BDRQ, but if I = 1, the interrupt occurs at end of command.

All searches for a data field are retried for 2 index pulses, but if a data ECC error is detected there are no retries.

If after reading the correct ID field, the Data Address mark is not found a DAM error is set.

The L flag controls the ECC check bytes. If L = 0, then the data field is read and ECC is checked. If L = 1, then the ECC check bytes are not computed; instead, the ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 7 bytes.
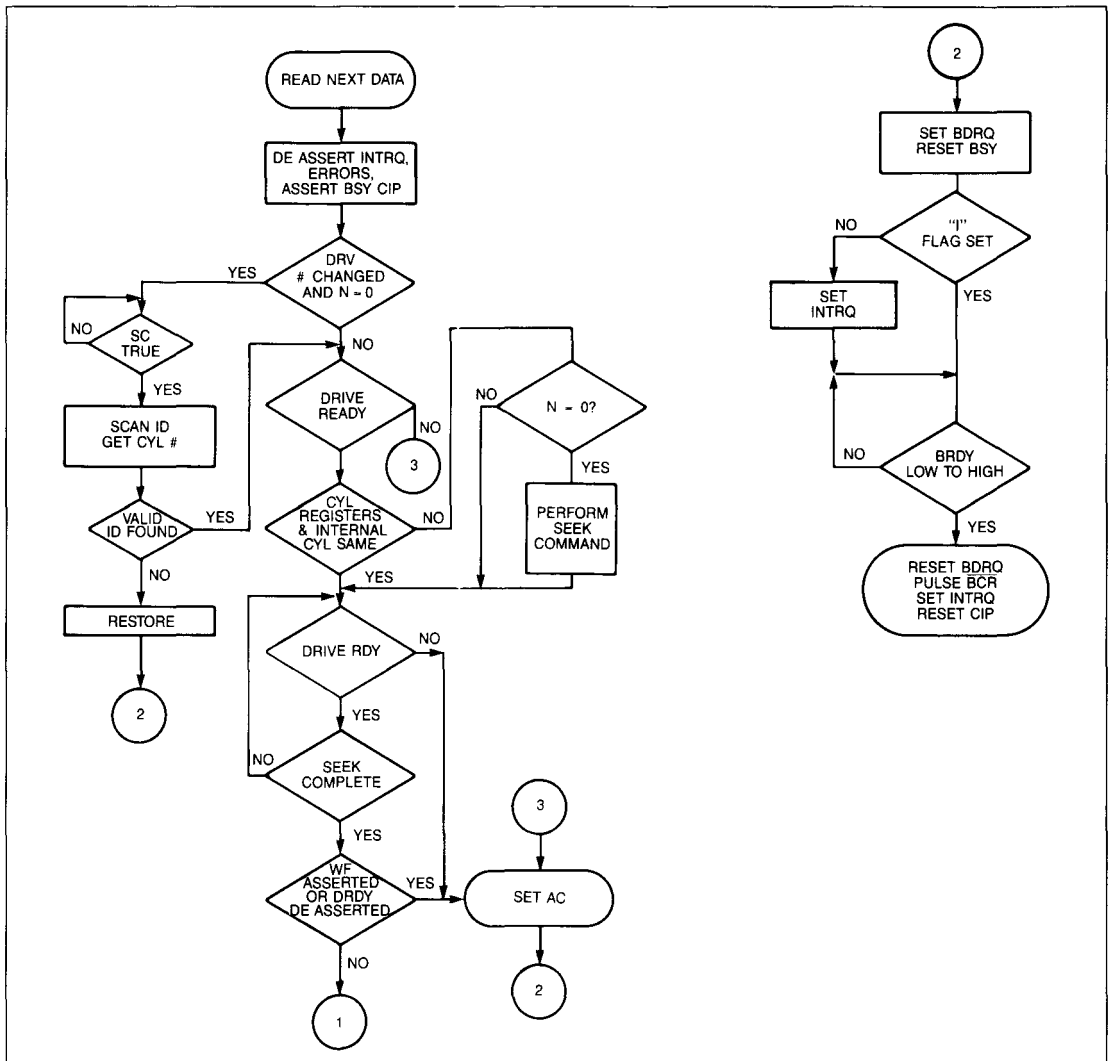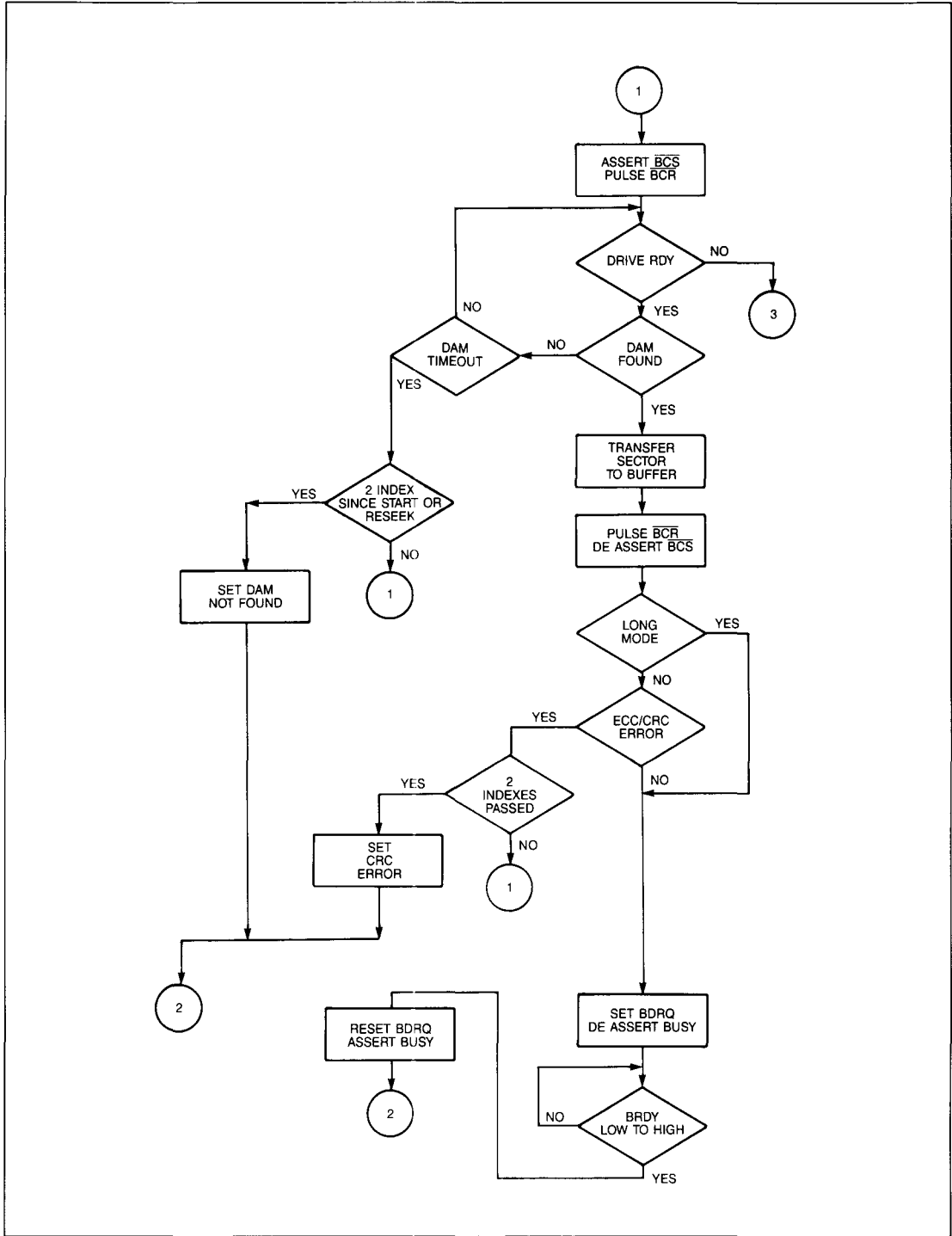

FIGURE 10. READ NEXT DATA COMMAND

FIGURE 10A. READ NEXT DATA COMMAND (Continued)

WRITE SECTOR

The Write Sector Command is used to write one or more sectors of data from the Sector Buffer to the disk. Upon receipt of this command, the WD50C12 compares the cylinder number in the Task File with the present position cylinder number. From this, the direction and number of steps required for the seek are calculated. As stated in the Seek Command, if an implied seek is performed when N = 0, the stepping rate is controlled by R3 through R0 of the previous seek command. After the last step the WD50C12 waits until the leading edge of the Seek Complete is received.

If the WD50C12 detects that the drive number has changed since the last Write command and if the N bit is 0, then an implied seek is done.

After the WD50C12 senses SC, BDRQ, and DRQ signals are asserted and the Host fills the Sector Buffer. When BDRY is asserted the controller searches for an ID field with the specified cylinder, head, sector size, and CRC. If the ID is not found and retry is enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error after ten attempts, an auto-scan and auto-seek are done. Then ten more tries are made before setting the ID Not Found Error. When Retry is disabled (T = 1) only two attemps are made before setting the ID Not Found Error, and no Auto-scan or auto-seek operations are done.

When the correct ID field is found the WD50C12 is ready to transfer data, WG is asserted and data is written to the disk.

The M flag controls multiple sector write operations. When the BRDY pin is activated, data is written from the buffer to the disk. The total number of sectors in the sector count register are written if M = 1. If M = 0, the sector count is ignored and only one sector is written. The data field PLO sync field is nominally 12 bytes long but will be extended as long as the Seek Complete line is low after the first 12 bytes of PLO sync field are written. For NRZ mode the PLO will be extended by the PLO value in register 1 (Precomp/PLO Length/Gap Length).

The T flag controls retries and the L flag controls CRC and ECC retries. If T = 0, ID searches are retried for 10 index pulses, then auto-scan and auto-seek are done, then retried for 10 more index pulses. If T = 1, ID searches are retried for 2 index pulses only. If L = 0, then normal ECC write sector commands are performed. If L = 1, then the ECC check bytes are not computed and written to the disk but instead, 4 or 7 additional bytes are read from the buffer and written to the disk immediately after the data field.

A bad block mark in the ID field sets the error bit and the data field is not written. If a bad block mark is found in an ID field during a multiple sector transfer, the command terminates.

The Write Data begins pulsing within 1.5 bit times of Write Gate (WG) going high for MFM and within 2 bit times of WG going high for RLL.

SUMMARY OF A WRITE SECTOR OPERATION

(1) Host: Sets up parameters; issues Write Sector command
(2) 50C12: Asserts BDRQ and DRQ
(3) Host: Loads sector buffer with data (asserts WE)
(4) 50C12: Waits for leading edge of BRDY
(5) 50C12: Finds specified ID field, writes to sector
(6) 50C12: If M = 0, asserts INTRQ; End
(7) 50C12: Increments sector number/decrements sector count
(8) 50C12: If sector count = 0, asserts INTRQ; End
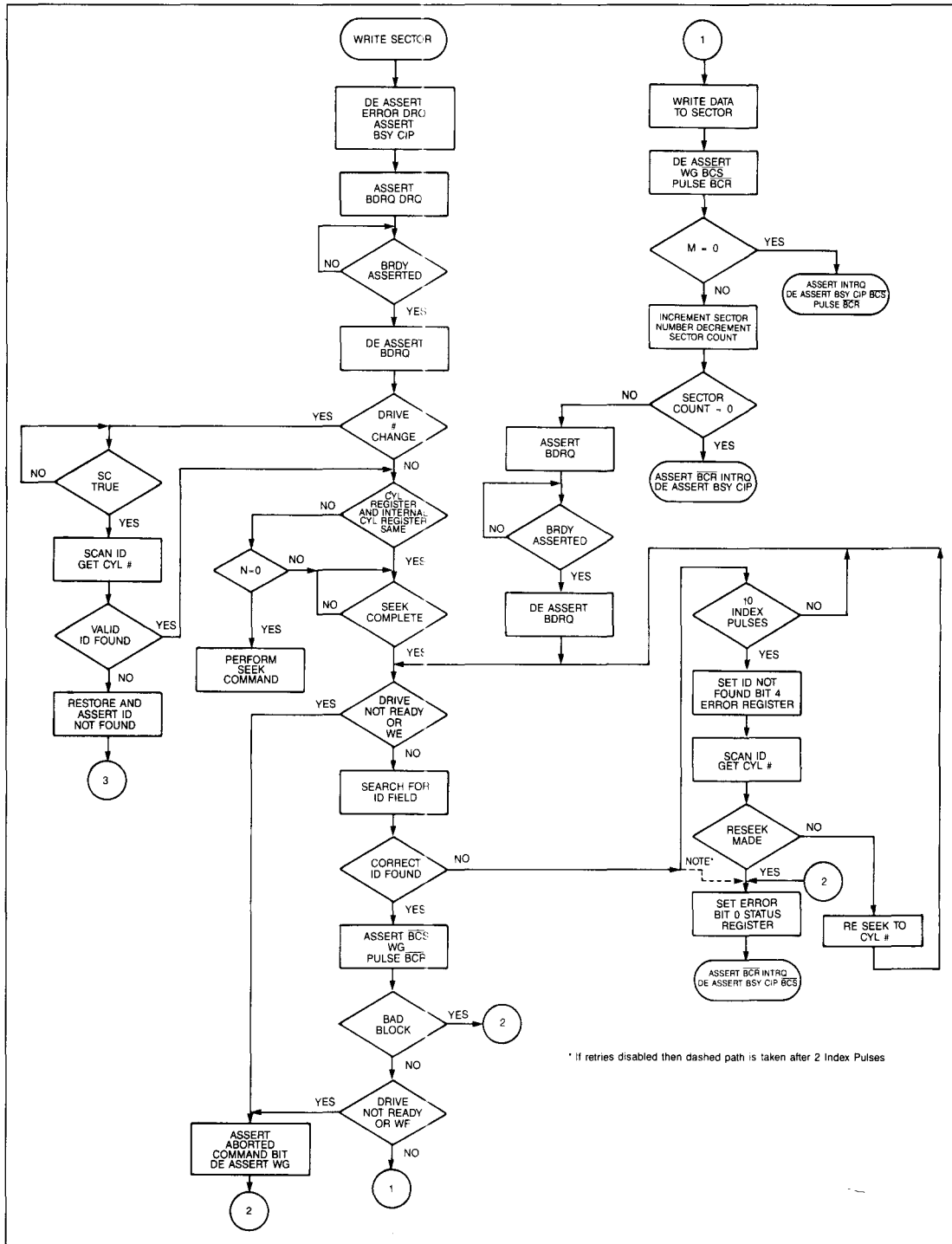(9) 50C12: Go to step 2

FIGURE 11. WRITE COMMAND

SCAN ID

The Scan ID command updates the head, sector size, sector number, and cylinder registers.

When the next ID field of the present track is encountered, cylinder number, sector size, head number and sector number are loaded into the respective registers. When auto-scan ID is done (if drive number changed or for retry procedure), only the internal cylinder position register is changed.

A bad block mark in the ID field sets the error bit. If the correct ID field is not found, an ID not found error is set.
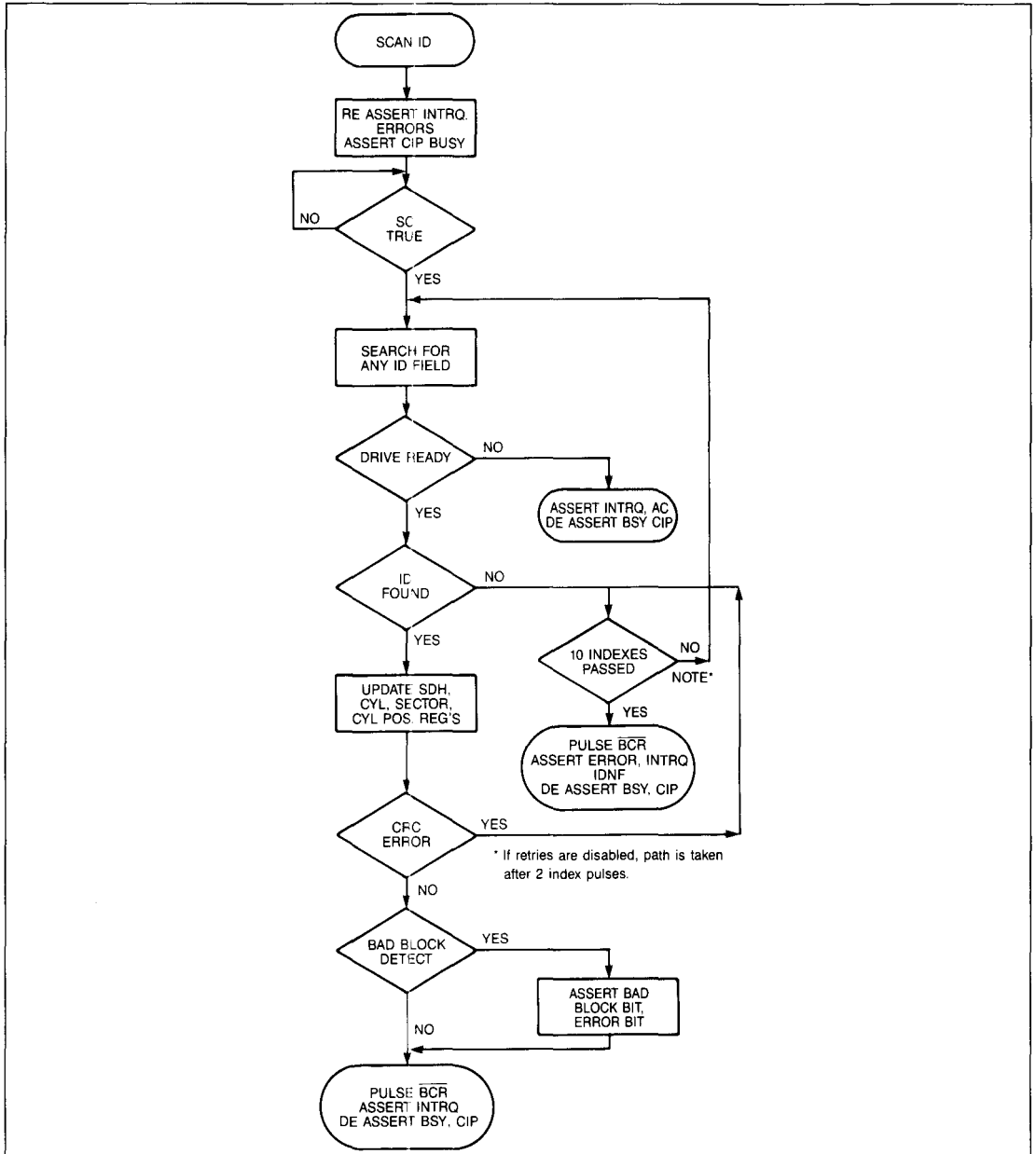

FIGURE 12. SCAN ID COMMAND

FORMAT

The Format command formats one track using the Task File and buffer memory.

During this command parameters (cylinder, head, and sector size) are taken from the Task File. Good block/bad block marks and sector numbers are taken from buffer memory. Table 4 shows the contents of the Sector Buffer for a 32 sector track format with an interleave of two.

The total number of sectors formatted is specified by the sector count register. The length of GAP1 and GAP3 minus three is loaded into the sector number register.

GAP1/GAP3 LENGTH = 'SECTOR NUMBER REGISTER' + 3

After the Task File has been loaded with the desired format parameters and the command register has been loaded with the write format command, the block marks and sector addresses are loaded into the buffer. When the BRDY pin is activated, the specified number of sectors are written. The block marks and sector numbers are read from the buffer prior to each sector as needed. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command. If the drive number has changed since the last command, an automatic ID scan is performed if the N bit is 0. An automatic seek is performed if the N bit is 0.

A = 1 and soft sector mode is selected, then ID PAD = 'AA' and, in MFM or NRZ mode, GAP3 = 'AA'. If A = 0 then ID PAD = '00' for MFM or NRZ and ID PAD = '33' for RLL.

If B = 1 the PLO field is programmable and is determined by the Precomp/PLO Length/Gap Length register. If B = F = 1 then GAP3 = '00'. This is not available in RLL format.

F = 0 and soft sector mode is selected then Gap 1 and Gap 3 bytes are '4E' for MFM or NRZ and '33' for RLL. If F = 0 and hard sector mode is selected then Gap 1 and Gap 3 bytes are '00'. If F = G = 1 and NRZ encoding in ESDI mode or hard sector mode is selected, the Gap 1 byte is '00' and the Gap 3 bytes are 'FF'. If F = B = 1 and NRZ encoding in ESDI mode or hard sector mode is selected, Gap 1 and Gap 3 bytes are '00'.

The gap length written on disk is 3 bytes longer than gap value specified in sector number register. The specified gap value must be greater than or equal to 2 (actual gap must be 5 bytes or more).

In hard sector mode Write Gate (WG) is turned on and off within 1.5 bit times after Index. In soft sector mode WG is turned on and off within 5 bit times after Index.

In RLL soft sector mode, Write Data (WD) will begin pulsing 1 bit time after WG goes high. In MFM soft sector mode, WD will begin pulsing immediately upon WG going high. In hard sector mode, WD will begin pulsing within 2.5 bit times of WG going high for MFM and within 4 bit times of WG going high for RLL.

When WF is asserted or DRDY is de-asserted the command terminates and an AC error is asserted.
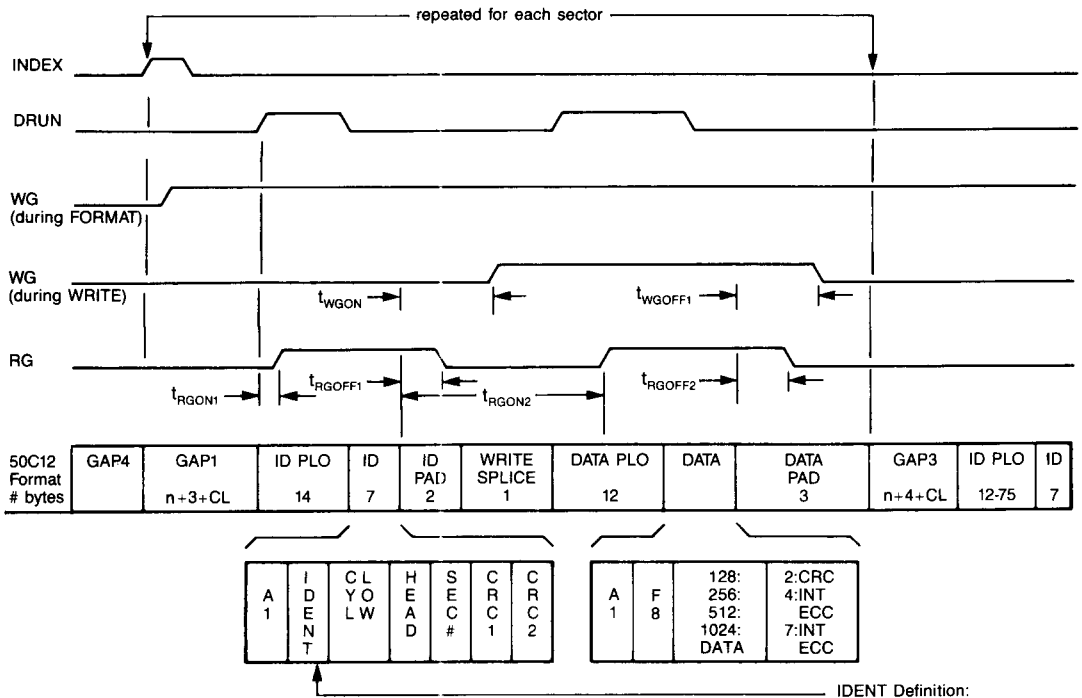
The SC signal is level sensed when used to signal gap extension during a Format command.

SC is used in the Format command to indicate gap extension, for soft sectored MFM modes and CC (Command Complete) for soft sectored ESDI modes.

TABLE 4. INTERLEAVE TABLE

ADDR	DATA							
	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
				.				
F0	FF	FF	FF	FF	FF	FF	FF	FF

SOFT SECTOR MFM/RLL TRACK FORMAT

────────────────── repeated for each sector ──────────────────

INDEX

DRUN

WG
(during FORMAT)

WG
(during WRITE) t_{WGON} →| |← t_{WGOFF1} →| |←

RG t_{RGON1} →| |← t_{RGOFF1} |← t_{RGON2} t_{RGOFF2} →| |←

50C12 Format # bytes	GAP4	GAP1	ID PLO	ID	ID PAD	WRITE SPLICE	DATA PLO	DATA	DATA PAD	GAP3	ID PLO	ID
		n+3+CL	14	7	2	1	12		3	n+4+CL	12-75	7

A 1	I D E N T	C L Y O L W	H E A D	S E C #	C R C 1	C R C 2

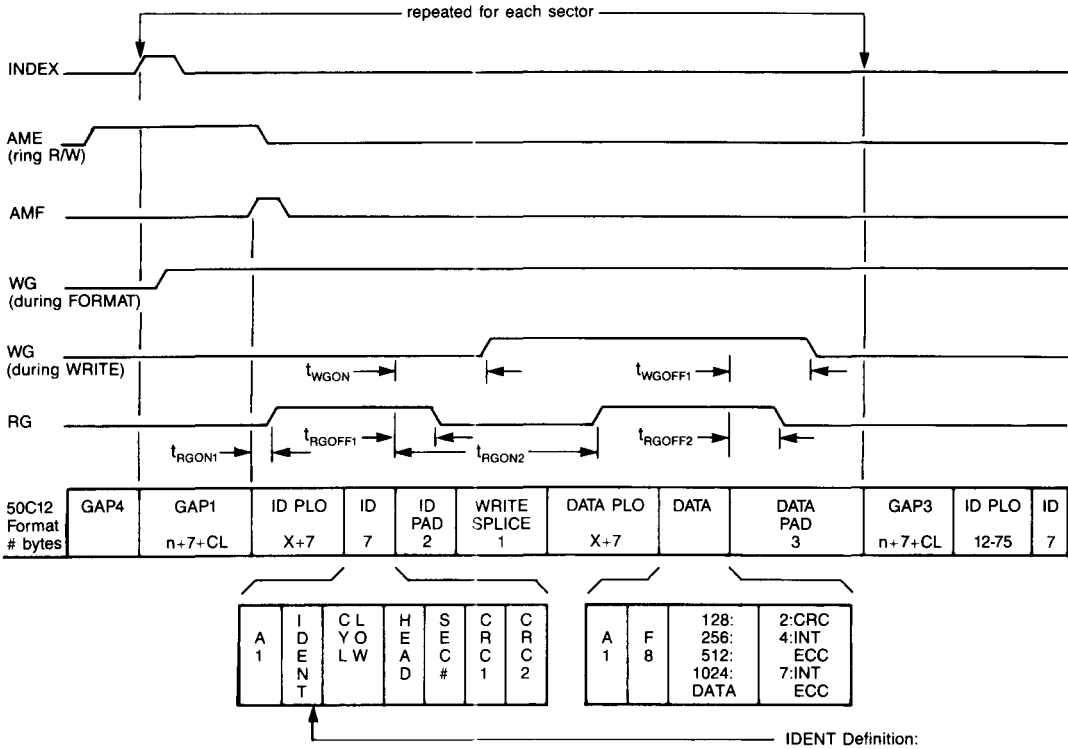| A 1	F 8	128: 256: 512: 1024: DATA	2:CRC 4:INT ECC 7:INT ECC

IDENT Definition:

NOTES:

1. n = contents of Sector Number Register during Format Command.
2. CL = controller latency. $\frac{1}{2} \leq CL \leq 1\frac{1}{2}$ byte times.
3. t_{WGON} = 18 ± 2 bit times with respect to RD in.
4. t_{WGOFF1} = 20 ± 2 bit times with respect to WD out.
5. t_{RGOFF1} = 10 ± 2 bit times with respect to RD in.
6. t_{RGOFF2} = 19 ± 2 bit times with respect to RD in.
7. t_{RGON1} = 20 ± 2 bit times with respect to DRUN.
8. t_{RGON2} = 36 ± 2 bit times with respect to RD in.
9. set B = 0 on Format Command.

FE = Cylinders 0-255
FF = Cylinders 256-511
FC = Cylinders 512-767
FD = Cylinders 768-1023
F6 = Cylinders 1024-1279
F7 = Cylinders 1280-1535
F4 = Cylinders 1526-1791
F5 = Cylinders 1792-2047

FIGURE 13. FORMAT

SOFT SECTOR NRZ TRACK FORMAT

50C12 Format # bytes	GAP4	GAP1	ID PLO	ID	ID PAD	WRITE SPLICE	DATA PLO	DATA	DATA PAD	GAP3	ID PLO	ID
		n+7+CL	X+7	7	2	1	X+7		3	n+7+CL	12-75	7

ID: A1 | IDENT | CLYOLW | HEAD | SEC # | CRC1 | CRC2

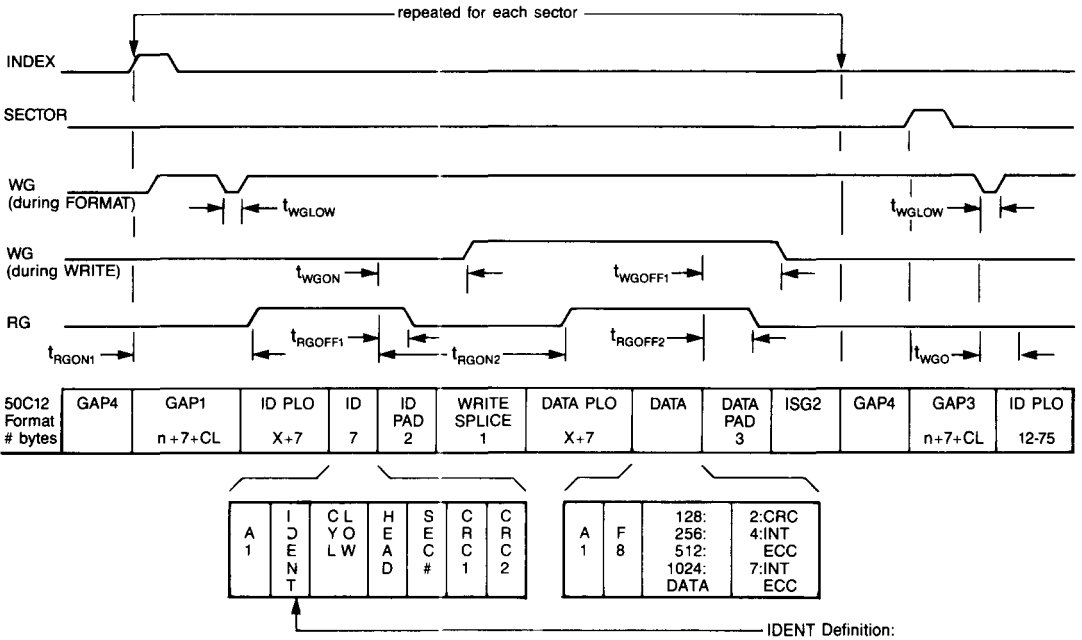DATA: A1 | F8 | 128: 256: 512: 1024: DATA | 2:CRC 4:INT ECC 7:INT ECC

IDENT Definition:

NOTES:

1. n = contents of Sector Number Register during Format Command.
2. CL = controller latency. $\frac{1}{2} \leq CL \leq 1\frac{1}{2}$ byte times.
3. ID PLO Length is programmable during Format Command. (With B Option)
   DATA PLO Length is programmable during Write Command.
4. t_{WGON} = 18 ± 2 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 20 ± 2 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 10 ± 2 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 19 ± 2 bit times with respect to NRZRD in.
8. t_{RGON1} = 4 ± 2 bit times with respect to AMF.
9. t_{RGON2} = 36 ± 2 bit times with respect to NRZRD in.
10. X = contents of PLO register.
11. PLO is abbreviation for the Write Precomp/PLO Length/Gap Length Register.

FE = Cylinders 0-255
FF = Cylinders 256-511
FC = Cylinders 512-767
FD = Cylinders 768-1023
F6 = Cylinders 1024-1279
F7 = Cylinders 1280-1535
F4 = Cylinders 1536-1791
F5 = Cylinders 1792-2047

FIGURE 13A. FORMAT

HARD SECTOR NRZ TRACK FORMAT

50C12 Format # bytes	GAP4	GAP1	ID PLO	ID	ID PAD	WRITE SPLICE	DATA PLO	DATA	DATA PAD	ISG2	GAP4	GAP3	ID PLO
		n+7+CL	X+7	7	2	1	X+7		3			n+7+CL	12-75

IDENT Definition:

A 1	I D E N T	C L Y O L W	H E A D	S E C #	C R C 1	C R C 2

A 1	F 8	128: 256: 512: 1024: DATA	2:CRC 4:INT ECC 7:INT ECC

NOTES:

1. n = contents of Sector Number Register during Format Command.
2. CL = controller latency. $\frac{1}{2} \leq CL \leq 1\frac{1}{2}$ byte times.
3. ID PLO Length is programmable during Format Command. (with B Option)
   DATA PLO Length is programmable during Write Command.
4. t_{WGON} = 18 ± 2 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 20 ± 2 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 10 ± 2 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 19 ± 2 bit times with respect to NRZRD in.
8. t_{RGON1} = x + CL byte times with respect to INDEX/SECTOR.
   x = contents of internal Gap Register.
9. t_{RGON2} = 36 ± 2 bit times with respect to NRZRD in.
10. t_{WGLOW} = 2 bit times. t_{WGOFF2} = 8 bit times. Both timings with respect to NRZWD out.
11. ISG2 = Intersector Gap 2 = SPEED TOLERANCE + COMBINED ENDEC DELAYS.
12. x = contents of PLO register.
13. PLO is abbreviation for the Write Precomp/PLO Length/Gap Length Register.

FE = Cylinders 0-255
FF = Cylinders 256-511
FC = Cylinders 512-767
FD = Cylinders 768-1023
F6 = Cylinders 1024-1279
F7 = Cylinders 1280-1535
F4 = Cylinders 1536-1791
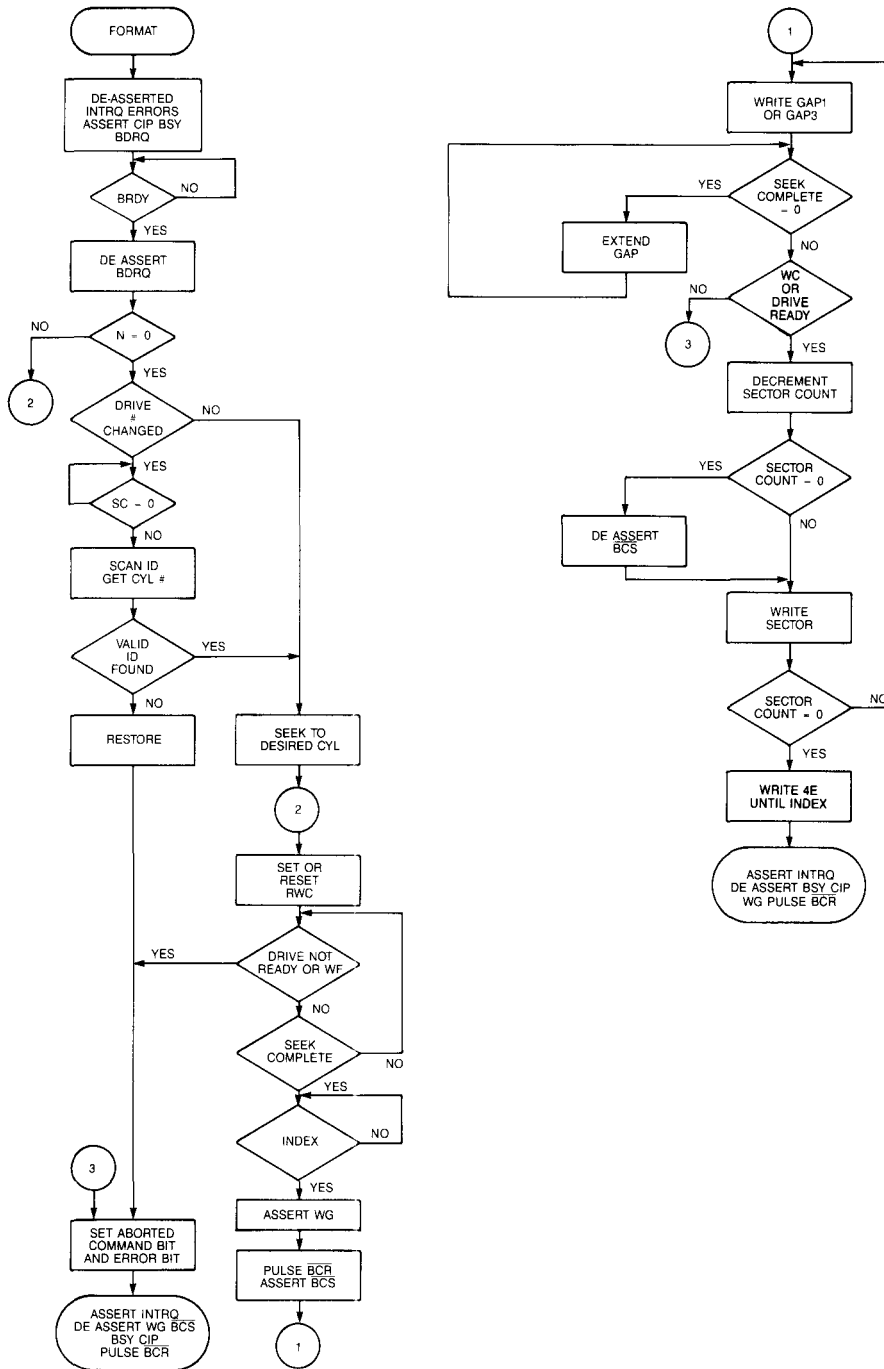F5 = Cylinders 1792-2047

FIGURE 13B. FORMAT

FORMAT

DE-ASSERTED
INTRQ ERRORS
ASSERT CIP BSY
BDRQ

BRDY — NO

YES

DE ASSERT
BDRQ

N = 0 — NO → 2

YES

DRIVE # CHANGED — NO

YES

SC = 0

NO

SCAN ID
GET CYL #

VALID ID FOUND — YES

NO

RESTORE

SEEK TO
DESIRED CYL

2

SET OR
RESET
RWC

DRIVE NOT
READY OR WF — YES

NO

SEEK
COMPLETE — NO

YES

INDEX — NO

YES

ASSERT WG

PULSE BCR
ASSERT BCS

1

3

SET ABORTED
COMMAND BIT
AND ERROR BIT

ASSERT INTRQ
DE ASSERT WG BCS
BSY CIP
PULSE BCR

1

WRITE GAP1
OR GAP3

SEEK
COMPLETE
= 0 — YES

EXTEND
GAP

NO

WC
OR
DRIVE
READY — NO → 3

YES

DECREMENT
SECTOR COUNT

SECTOR
COUNT = 0 — YES

DE ASSERT
BCS

NO

WRITE
SECTOR

SECTOR
COUNT = 0 — NO

YES

WRITE 4E
UNTIL INDEX

ASSERT INTRQ
DE ASSERT BSY CIP
WG PULSE BCR

FIGURE 14. FORMAT COMMAND

COMPUTE CORRECTION

This computes the pattern and location of a single burst error, but does not correct it. The Host, using the data provided by the WD50C12, performs the correction. The Compute Correction Command follows a data field ECC error when the command initiating the read operation specifies no Retry (T = 1).

The compute correction command first writes the syndrome bytes, four for 4 byte ECC or seven for 7 byte ECC from the ECC Register to the buffer. The WD50C12 then processes the syndrome bytes to compute the error pattern and error location and then writes the pattern and location to the buffer. If C = 0 and 4 byte ECC is selected then three error pattern bytes are written into the buffer. If C = 1 or 7 byte ECC is selected then four error pattern bytes are written into the buffer. The error pattern bytes are automatically byte aligned.

The error pattern and error location bytes are not valid when the error is uncorrectable. An uncorrectable error is indicated by bits set in the status and error register.

The buffer contents contain the following:

SYNDROME BYTE (MSB)
SYNDROME BYTE
SYNDROME BYTE
SYNDROME BYTE (LSB for 4 byte ECC)
If C = 1 or 7 byte ECC is selected then the buffer will contain three more syndrome bytes.
SYNDROME BYTE
SYNDROME BYTE
SYNDROME BYTE (LSB for 7 byte ECC)
BYTE OFFSET (MSB)
BYTE OFFSET (LSB)
ERROR PATTERN (MSB)
ERROR PATTERN
ERROR PATTERN

If C = 1 or 7 byte ECC is selected then the buffer contains one more error pattern byte:

ERROR PATTERN (LSB)

If the byte offset is 0 then the first data byte of the sector should be exclusive OR'ed with the first error pattern byte (MSB), the second data byte exclusive OR'ed with the second error pattern byte, and the third data byte with the last error pattern byte (LSB).

The WD50C12 defaults to 11 bit correction span after master reset (seven byte ECC). If four byte ECC is selected using the Set Parameter command the default is a 5 bit correction span.
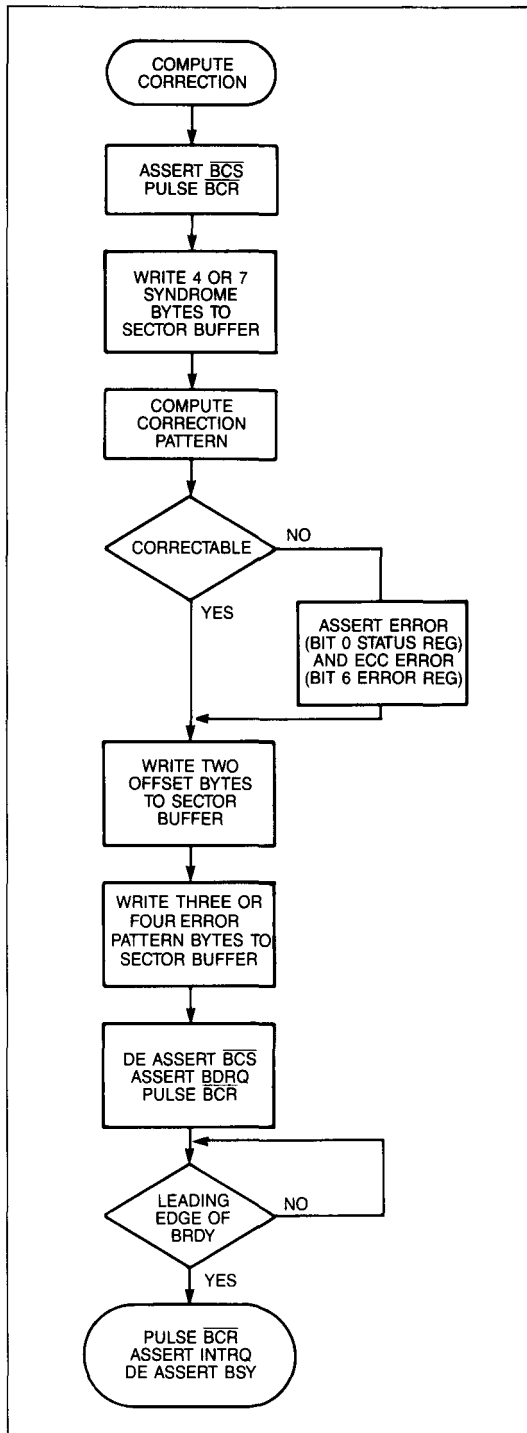

FIGURE 15. COMPUTE CORRECTION COMAND

SET PARAMETER

The Set Parameter command selects various parameters by setting several bits. These are explained below.

The E bit selects either 4 byte or 7 byte sector extension for long mode or internally generated ECC. A 7 byte sector extension and 7 byte ECC are the defaults following a master reset. If E is 0 and MFM or NRZ mode is selected then a 4 byte sector extension and 4 byte ECC or 2 byte CRC are selected depending on the MSB of SDH register; if E is 1 then a 7 byte sector extension and 7 byte ECC are selected.** RLL mode always uses a 7 byte ECC.

The H bit selects either 2 drive select bits and 3 head select bits in the SDH register or 1 drive select bit and 4 head select bits in the SDH register. The default following a master reset is 2 drive select and 3 head select bits.

The S bit selects among a 5, 11, or 22 bit correction span for the error correction process. In 4 byte ECC mode, if S = 0 then a 5 bit correction span is selected and if S = 1 then an 11 bit correction span is selected. In 7 byte ECC mode, if S = 0 then an 11 bit correction span is selected and if S = 1 then a 22 bit correction span is selected. The S bit is set to zero following a master reset.

The Z bit selects MFM or NRZ mode. If Z is 0 and K is 1 (K being a bit in the Auxilliary Set Parameter command) then MFM coding is selected. If Z is 1 and K is 1 then NRZ coding is selected. Otherwise, RLL coding is selected. The WD50C12 defaults to RLL mode following a master reset.

The Set Parameter command contains no error flags.

**Note: To use CRC mode, set E to zero.

AUXILLIARY SET PARAMETER

The Auxilliary Set Parameter command loads an internal GAP register with the contents of the Write Precomp/PLO Length/Gap Length Register.

In hard sector NRZ encoding in ESDI mode this internal Gap register is used during Scan ID, Read, and Write commands to control the delay between the Index or Sector pulse and the rising edge of Read Gate. The Write Precomp/PLO Length/Gap Length Register is loaded with the desired value for the internal Gap register prior to issuing the Auxilliary Set Parameter command.

The K bit selects the data interface mode. When K = 0, RLL mode is selected. If K = 1 then the interface is either MFM or NRZ depending on the set parameter command, bit Z. The default is RLL mode following a master reset.

The U bit selects the sector size options. When U = 0 the sector sizes are 128, 256, 512, and 1024. If U = 1 then the sector size is defined by the user. The cylinder registers are loaded with the desired sector size prior to issuing the Auxilliary Set Parameter command. The maximum sector size is 2048 bytes.

The D bit selects between hard and soft sector disk format. When D = 0 soft sector format is selected. If D = 1 then hard sector is selected. The default is soft sector after a master reset.

The Auxilliary Set Parameter command contains no error flags.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) .... +5.25V
Max Voltage on any pin with respect to V_{SS} .... −0.5V to +0.5V
Operating Temperature .... 0°C (32°F) to 70°C (158°F)
Storage Temperature .... 55°C (−67°F) to 125°C (257°F)

NOTE: Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating characteristics.

DC Operating Characteristics T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OZ}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		.8	V	
V_{OH}	Output High Voltage	2.4		V	I_O = −100μA
V_{OL}	Output Low Voltage		.4	V	I_O = 1.6mA
I_{CC}	Supply Current		20	mA	All outputs open
T_{RS}	Rise Time (Pins 21-23)		20	nS	10% to 90%
V_{OL}	Output Low Voltage		.45	V	I_O = 6.0mA
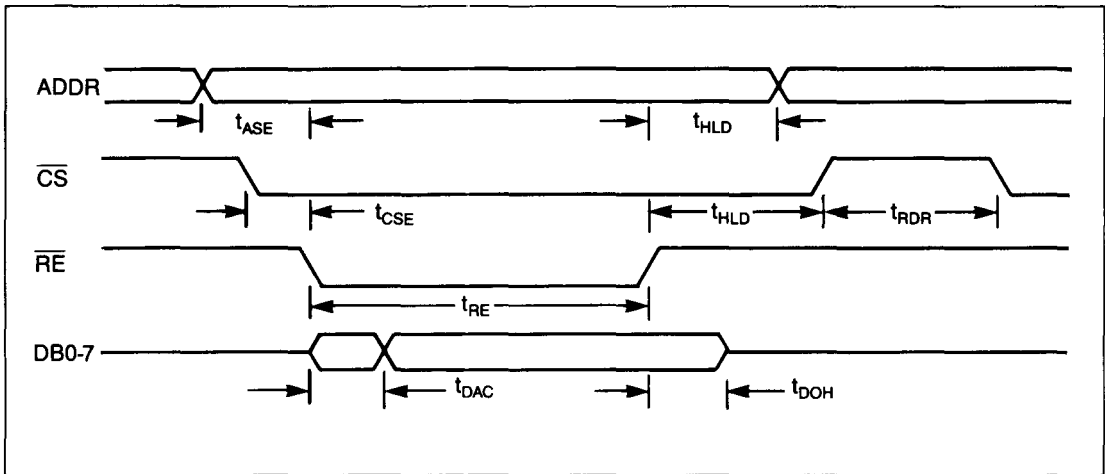
FIGURE 16. AC TIMING CHARACTERISTICS

HOST READ TIMING WD50C12   WC = 10MHz

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{RE}$	100		nS	
t_{CSE}	$\overline{CS}$ Setup to $\overline{RE}$	0		nS	
t_{DAC}	Data Valid from $\overline{RE}$		180	nS	
t_{RE}	Read Enable Pulse Width	.20	10	μS	
t_{DOH}	Data Hold from $\overline{RE}$	60	200	nS	
t_{HLD}	Address $\overline{CS}$ Hold from $\overline{RE}$	0		nS	
t_{RDR}	Read Recovery Time	300		nS	
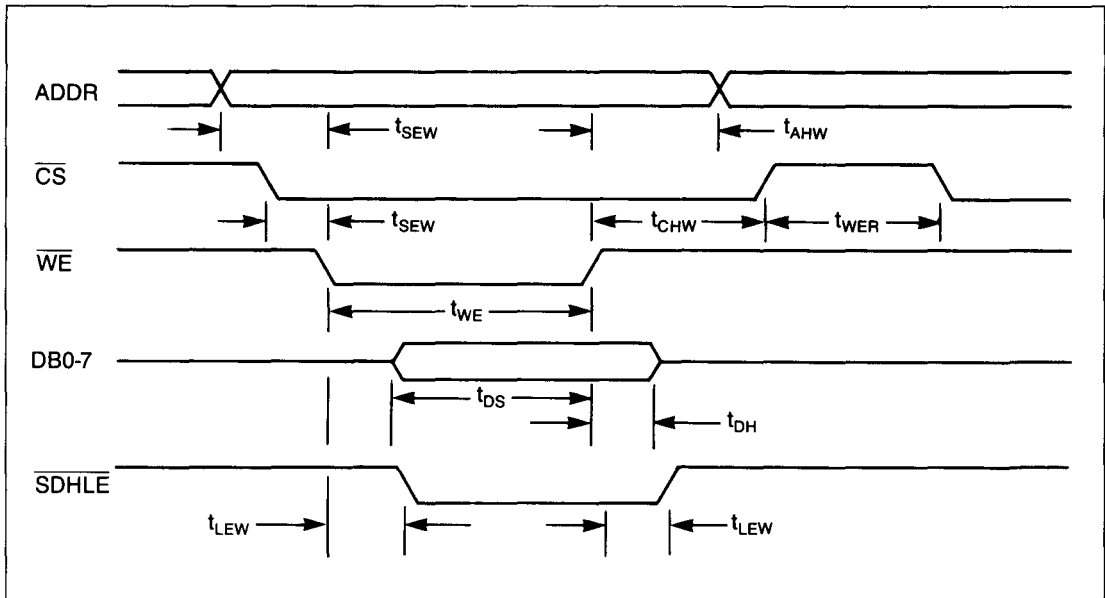
FIGURE 17. HOST WRITE TIMING WD50C12   WC = 10MHz

HOST WRITE TIMING   WC = 10MHZ

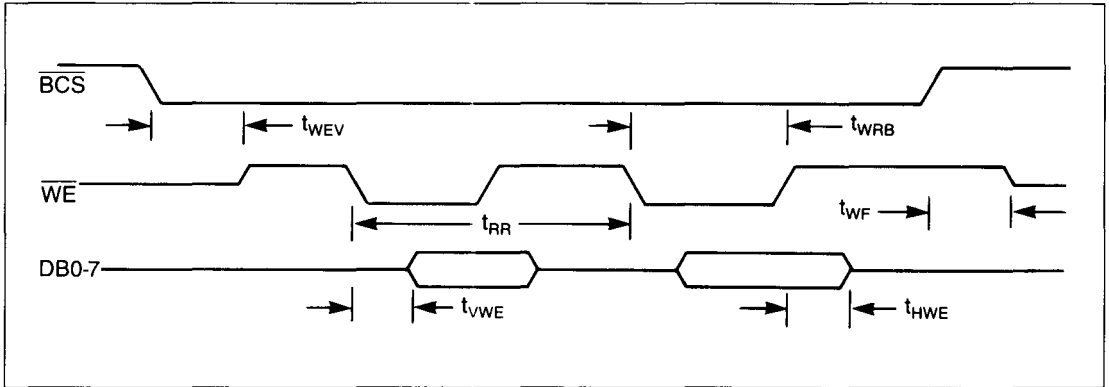| SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{SEW}	Address $\overline{CS}$ Setup to $\overline{WE}$	0	10	μS	
t_{DS}	Data Setup to $\overline{WE}$	.2	10	μS	
t_{WE}	Write Enable Pulse Width	.2	10	μS	
t_{DH}	Data Hold from $\overline{WE}$	10		nS	
t_{AHW}	Address Hold from $\overline{WE}$	10		nS	
t_{CHW}	$\overline{CS}$ Hold from $\overline{WE}$	0		nS	
t_{WER}	Write Recovery Time	1.0		μS	
t_{LEW}	$\overline{SDHLE}$ Propagation Delay	10	100	nS	

FIGURE 18. BUFFER WRITE TIMING (READ SECTOR CMD) WD50C12

BUFFER WRITE TIMING (READ SECTOR CMD) WD50C12

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	0		100	ns	
t_{WRB}	$\overline{WE}$ Output Pulse Width	*	2	**	WC	See note
t_{VWE}	Data Valid from $\overline{WE}$			100	ns	
t_{THWE}	Data Hold from $\overline{WE}$	60		200	ns	
t_{RR}	$\overline{WE}$ Repetition Rate	6	8	10	WC	See note
t_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	0		100	ns	
t_{WC}	WC period	—	—	—	—	Function of WC

Note:

   t_{WRB} and t_{RR} are dependent upon the WC

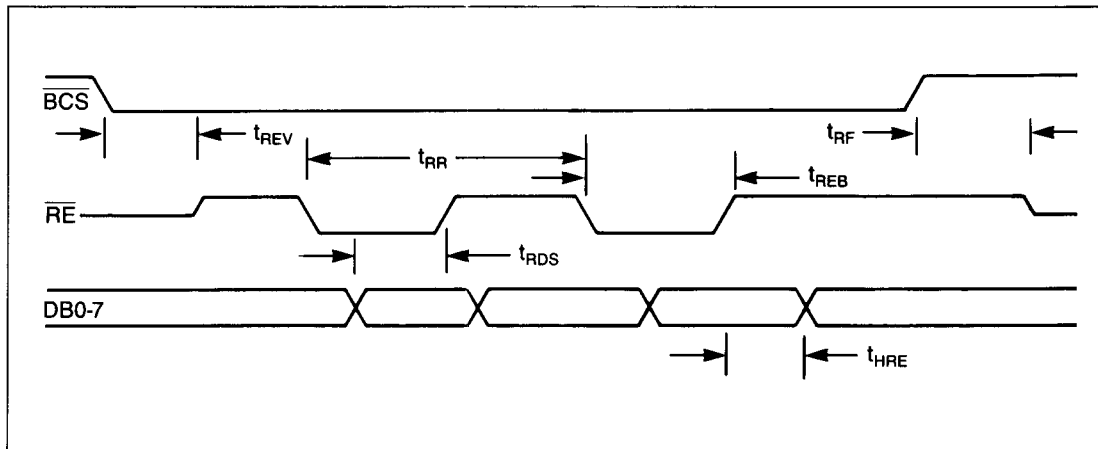* t_{WRB} min is $2t_{WC} - .25$ns

**t_{WRB} max is $2t_{WC} + .25$ns

FIGURE 19. BUFFER READ TIMING (WRITE SECTOR CMD) WD50C12

BUFFER READ TIMING (WRITE SECTOR CMD) WD50C12

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	0		100	nS	
t_{REB}	$\overline{RE}$ Output Pulse Width	*	2	**	t_{WC}	See note
t_{RDS}	Data Setup to $\overline{RE}$	100			nS	
t_{HRE}	Data Hold from $\overline{RE}$	0			nS	
t_{RR}	$\overline{RE}$ Repetition Rate	6	8	10	t_{WC}	See note
t_{RF}	$\overline{RE}$ Float from $\overline{BCS}$	0		100	nS	
t_{WC}	WC period	—	—	—	—	Function of WC

Note:

t_{WRB} and t_{RR} are dependent upon the WC

* t_{WRB} min is $2t_{WC} - .25ns$

** t_{WRB} max is $2t_{WC} + .25ns$

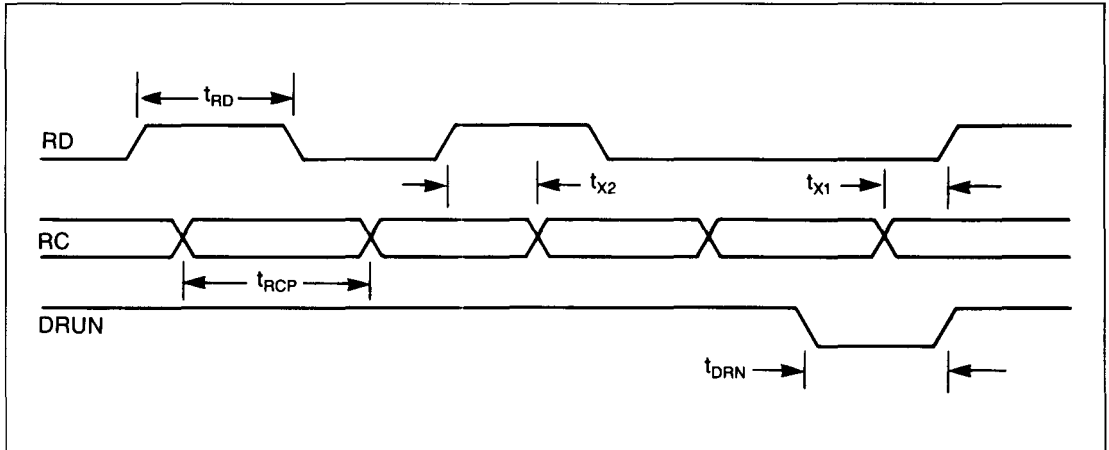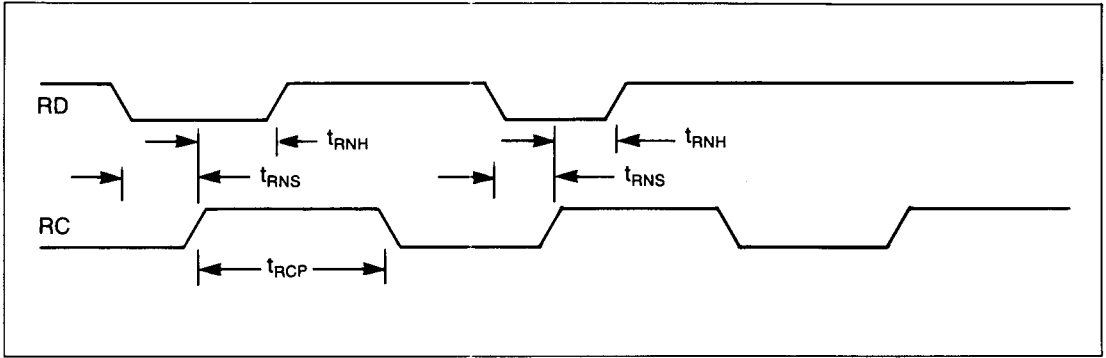**FIGURE 20. READ DATA TIMING - MFM MODE WD50C12   WC = 10MHz**

READ DATA TIMING - MFM MODE WD50C12   WC = 10MHz

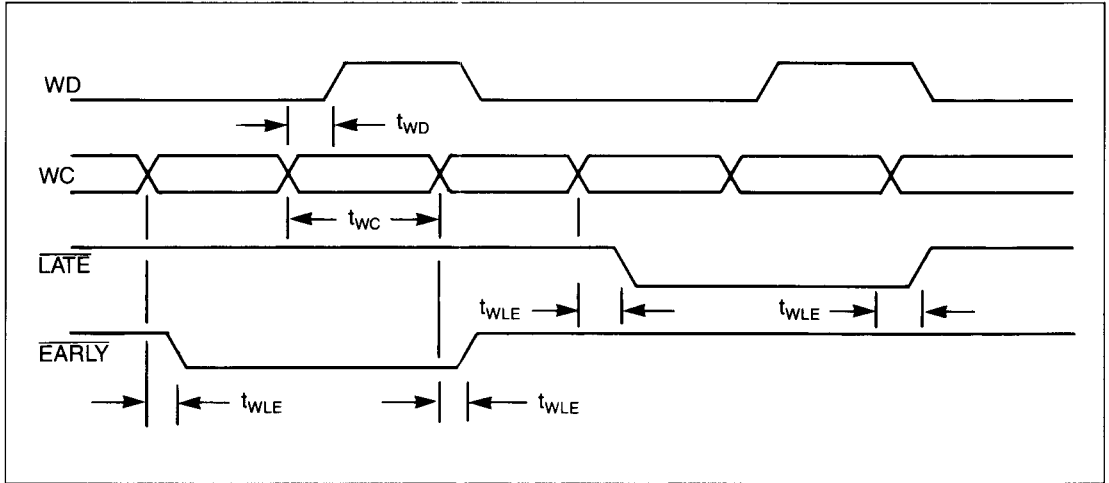| SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RCP}	RC Pulse Width	45		500	nS	
t_{x1}	RC Transition to Next Leading RD	10			nS	
t_{x2}	Leading RD to Next RC Transition	20			nS	
t_{RD}	Read Data Pulse Width	30		500	nS	
t_{DRN}	DRUN Pulse Width Low	25			nS	
t_{RCF}	RC Frequency	1		11.1	MHz	

FIGURE 21. READ DATA TIMING - NRZ MODE WD50C12   WC = 15MHz

READ DATA TIMING - NRZ MODE WD50C12   WC = 15 MHz

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RCP}	RC Pulse Width	30		500	nS	
t_{RNS}	RD Setup	10			nS	
t_{RNH}	RD Hold	10			nS	
t_{RCF}	RC Frequency	1		16.0	MHz	

FIGURE 22. WRITE DATA TIMING - MFM MODE WD50C12   WC = 10MHz

WRITE DATA TIMING - MFM MODE WD50C12   WC = 10MHz

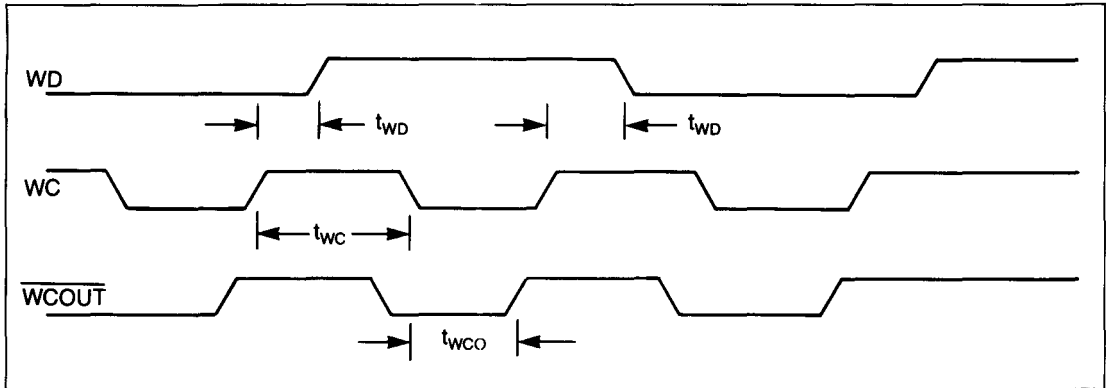| SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WC}	WC Pulse Width	45		500	nS	
t_{WD}	WD Propagation Delay	5		35	nS	
t_{WLE}	$\overline{EARLY}/\overline{LATE}$ Propagation Delay	5		35	nS	
t_{WCF}	WC Frequency	1		11.1	MHz	

FIGURE 23. WRITE DATA TIMING - NRZ MODE WD50C12   WC = 15MHz

WRITE DATA TIMING - NRZ MODE WD50C12   WC = 15MHz

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WC}	WC Pulse Width	30		500	nS	
t_{WD}	WD Propagation Delay	5		35	nS	
t_{WCF}	WC Frequency	1		16.0	MHz	
t_{WCO}	$\overline{WCOUT}$ Prop Delay	5		35	ns	

MISCELLANEOUS TIMING WD50C12

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RO}	BDRQ Reset from BRDY	20		200	nS	
t_{BDW}	BDRQ Pulse Width	150			nS	
t_{BCR}	$\overline{BCR}$ Pulse Width	7	8	9	WC	PERIODS
t_{STP}	Step Pulse Width	7	8	42	WC	Fast rates
t_{IDX}	Index Pulse Width	500			nS	
t_{IWG}	Index to Write Gate	2		7	WC	RLL
	Index to Write Gate	5		10	WC	MFM
	Index to Write Gate	2		4	WC	NRZ
t_{MR}	Master Reset Pulse W.	24			WC	PERIODS
t_{BRY}	Buffer Ready Pulse W.	150			nS	
f_{RCWC}	Difference of RC freq from WC freq	−15%		+15%		
t_{MRB}	$\overline{MR}$ Trailing to $\overline{BCR}$	0	.8	1.6	μS	
t_{MRW}	$\overline{MR}$ Trailing to Host Register Write	2.4			μS	

ADDITIONAL TIMINGS

GAP3 $= 2 \times M \times S + K$

   M = motor speed variation (e.g. .03 for $\pm 3\%$)
   S = sector length in bytes
   K = 10 for an interleave factor of 1
   K = 0 for any other interleave factor

NOTES

NOTES

NOTES

NOTES

Western Digital
2445 McCabe Way
Irvine, California 92714
(800) 847-6181   (714) 863-0102
FAX 714-660-4909   TLX 910-595-1139

WESTERN DIGITAL

WD1739 3/88 5M
79-000213

009584