Winbond

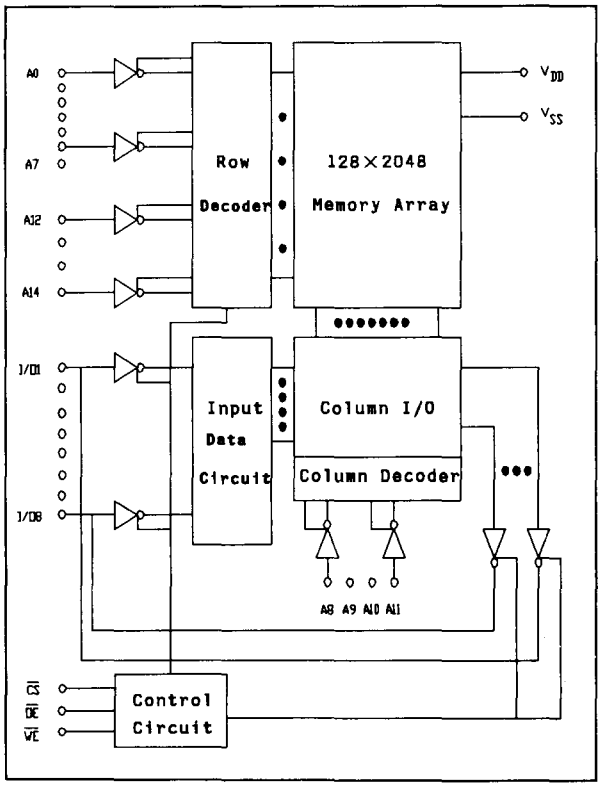
W24256A

32K X 8 HIGH SPEED CMOS STATIC RAM

FEATURES

- High speed access time: 20/25 nS (max.)
- Low power consumption:
  Active: 400mW (typ.)
  Standby: 10 μW(typ.) (L-version)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Battery back up operation capability (L-version)
- Data retention voltage: 2V (min.) (L-version)
- Available packages: 28-pin SOJ, or skinny DIP

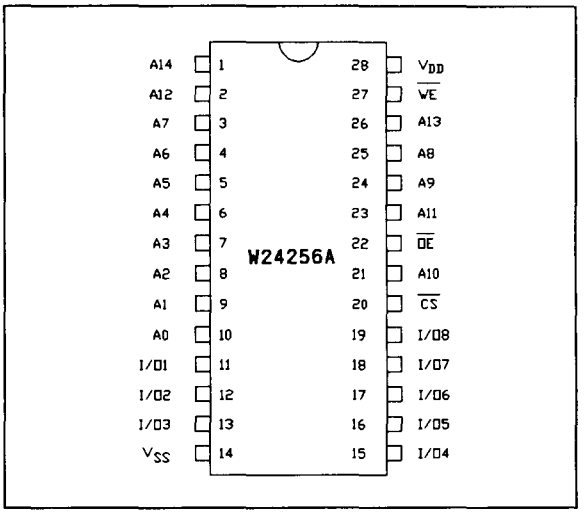
BLOCK DIAGRAM



GENERAL DESCRIPTION

The W24256A is a very high speed, low power CMOS static RAM organized as 32768×8 bits and operates on a single 5-Volt power supply. It is manufactured using Winbond's high performance CMOS technology.

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground

November 1991

DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Inputs/Outputs to V_{SS} Potential	-0.5 to V_{DD}+0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 - I/O8	V_{DD} Current
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		- 0.5	-	+ 0.8	V
Input High Voltage	V_{IH}	-		+ 2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN}= V_{SS} to V_{DD}		- 10	-	+ 10	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 10	-	+ 10	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0mA CYCLE = MIN, DUTY = 100%		-	-	200	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}		-	-	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{DD} -0.2V	L	-	2	100	μA
			S	-	-	2000	μA

Note: Typical characteristics are at V_{DD}=5V, Ta=25℃.

CAPACITANCE

(V_{DD}=5V, Ta=25℃, f=1MHz)

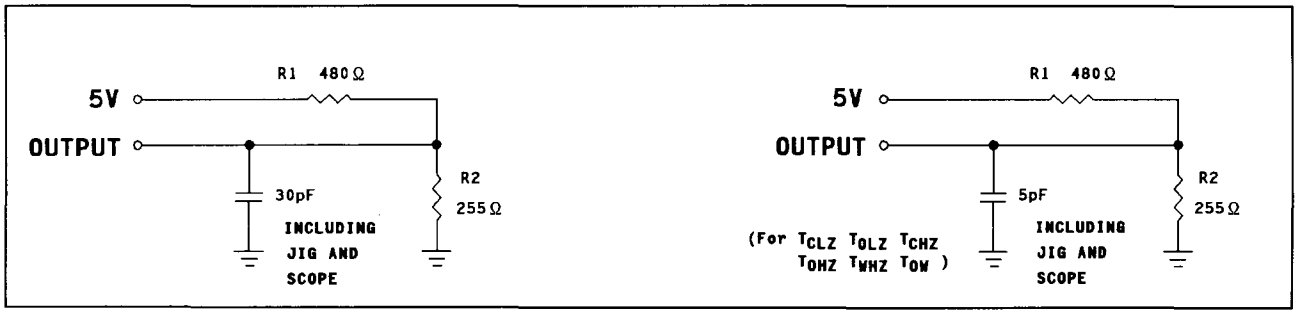
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}=0V	10	pF

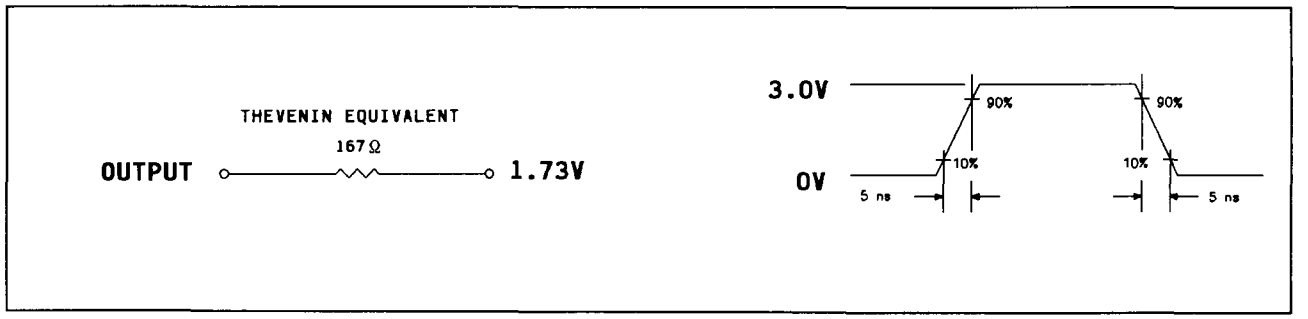
Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L=30pF, I_{OH}/I_{OL}=-4mA/8mA

AC TEST LOADS AND WAVEFORMS





AC CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	W24256A-20		W24256A-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	20	-	25	-	nS
Address Access Time	T_{AA}	-	20	-	25	nS
Chip Select Access Time	T_{ACS}	-	20	-	25	nS
Output Enable to Output Valid	T_{AOE}	-	10	-	12	nS
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	10	-	12	nS
Output Disable to Output in High Z	T_{OHZ}*	-	10	-	12	nS
Output Hold from Address Change	T_{OH}	3	-	3	-	nS

Note: * These parameters are sampled but not 100% tested.

(2) WRITE CYCLE

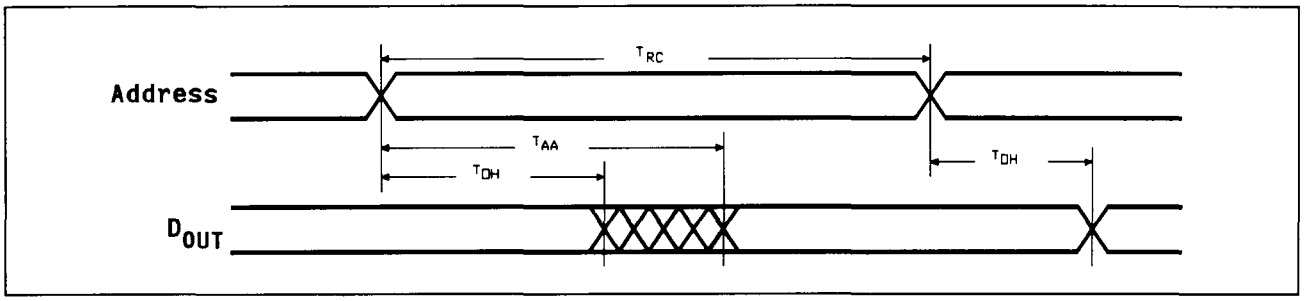
PARAMETER		SYMBOL	W24256A-20		W24256A-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	20	-	25	-	nS
Chip Selection to End of Write		T_{CW}	15	-	20	-	nS
Address Valid to End of Write		T_{AW}	15	-	20	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	12	-	15	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	10	-	12	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	10	-	12	nS
Output Disable to Output in High Z		T_{OHZ}*	-	10	-	12	nS
Output Active from End of Write		T_{OW}	2	-	2	-	nS

Note: * These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

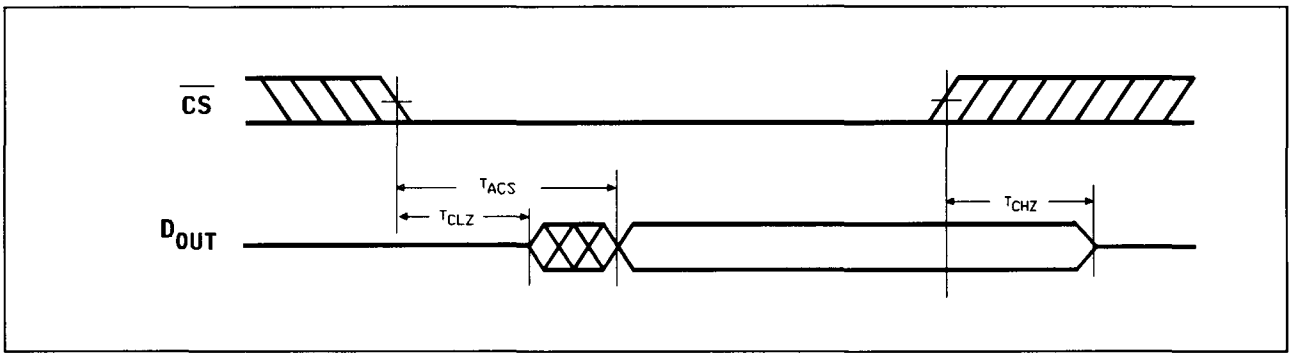
READ CYCLE 1

(Address Controlled)



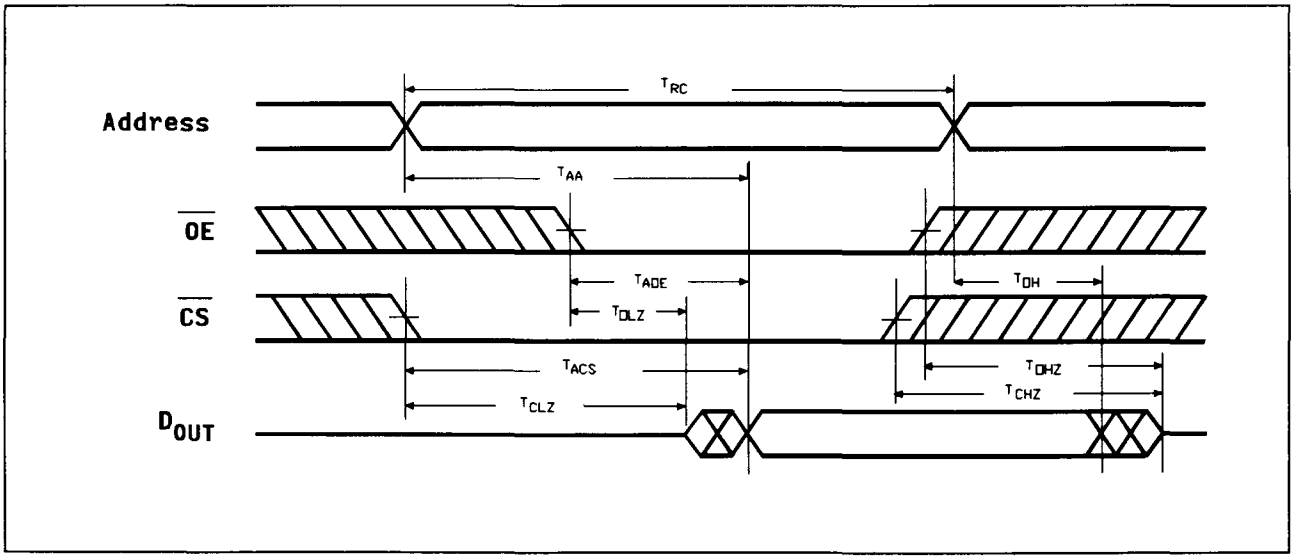
READ CYCLE 2

(Chip Select Controlled)



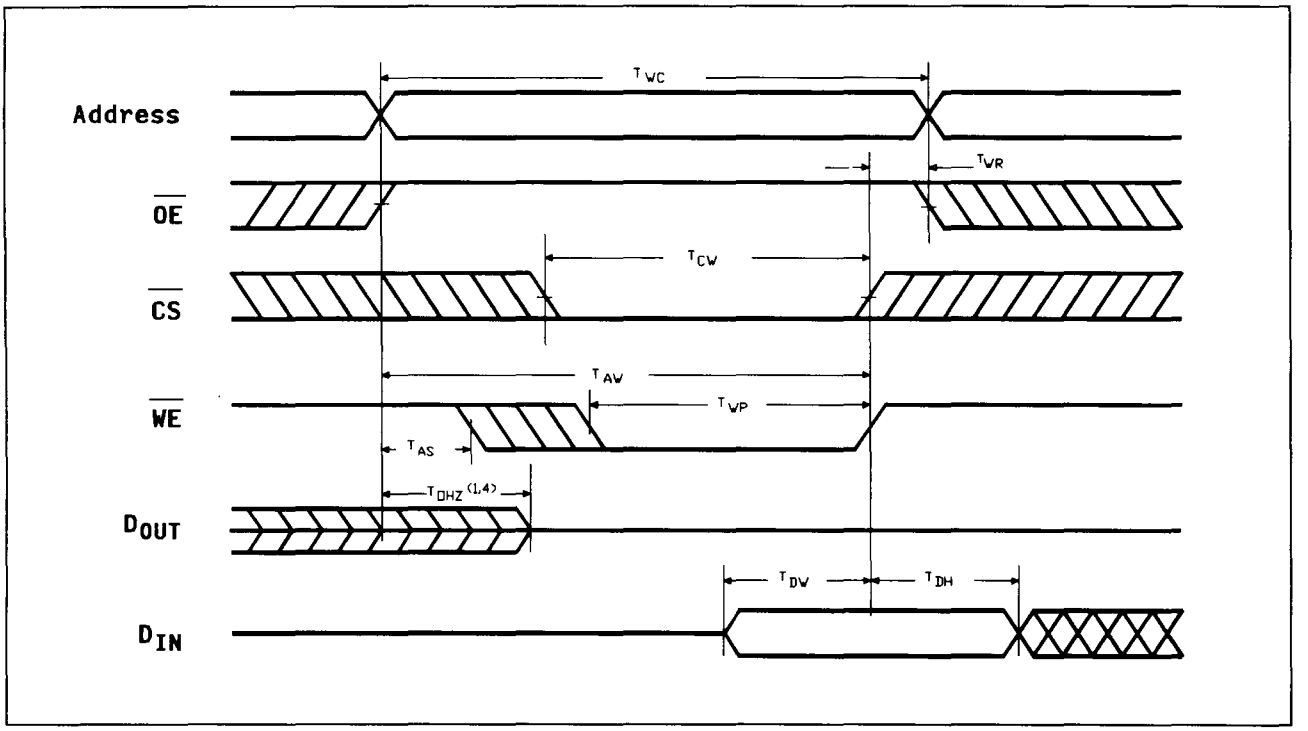
READ CYCLE 3

(Output Enable Controlled)



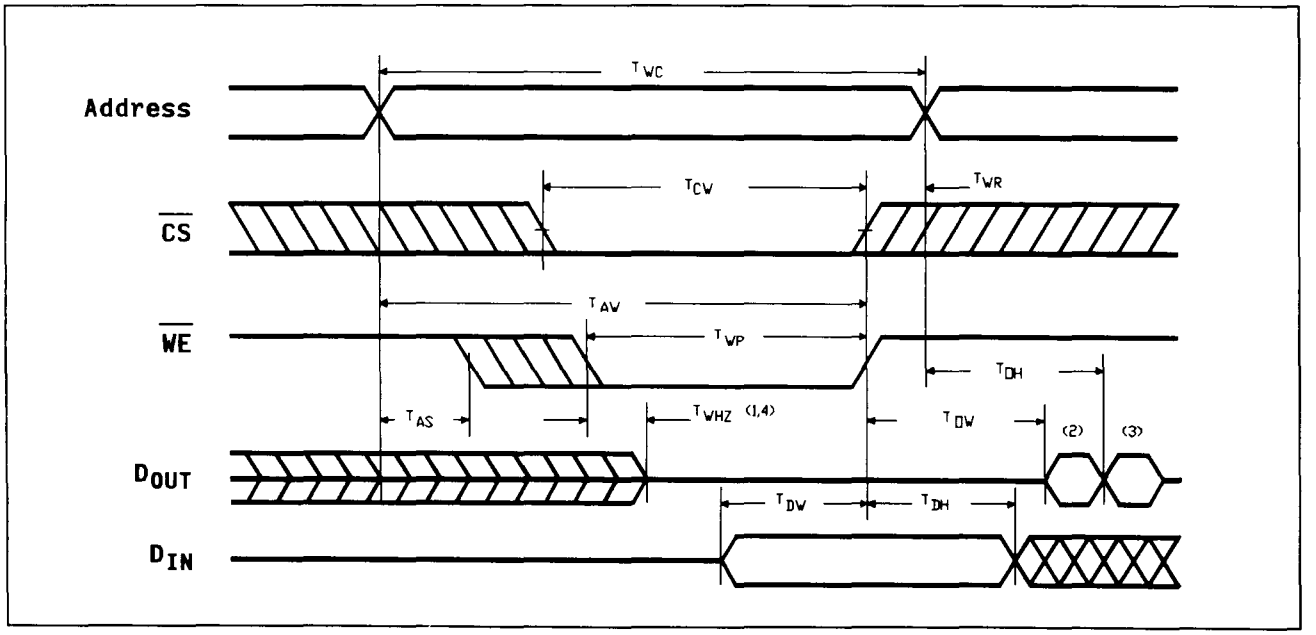
WRITE CYCLE 1

($\overline{OE}$ Clock)



WRITE CYCLE 2

($\overline{OE}$=V_{IL} Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} is the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500mV from steady state with C_L=5pF. This parameter is guaranteed but not 100% tested.

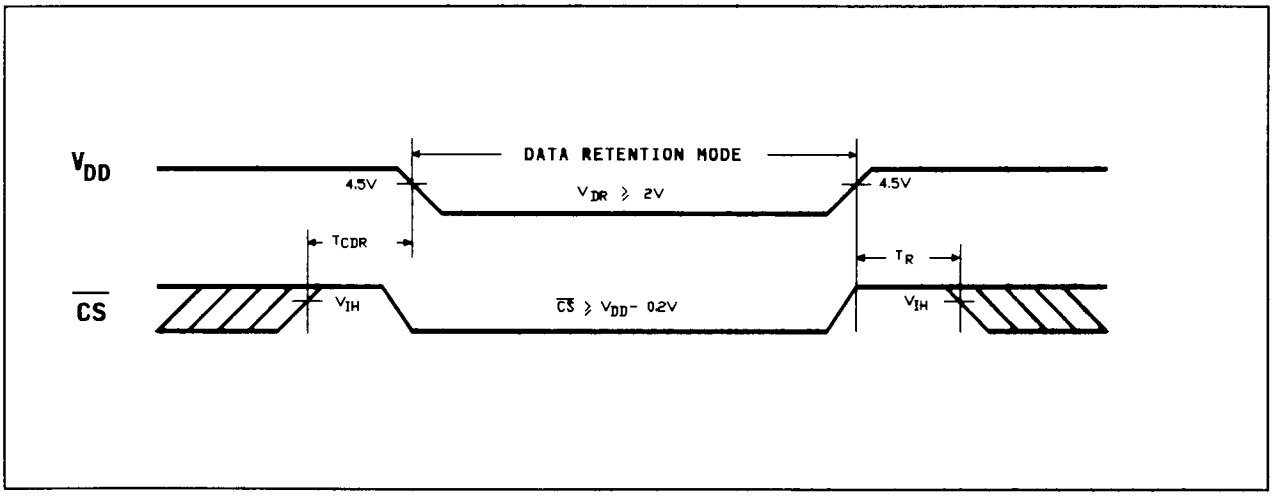
DATA RETENTION CHARACTERISTICS

(Ta=0 to 70℃, Guaranteed Only for L-Version)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{DD}$ - 0.2V	2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS} \geqq V_{DD}$ - 0.2V V_{DD} = 3V	-	-	100	μA
Chip Deselect to Data Retention Time	T_{CDR}	See Retention Waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC} *	-	-	nS

Note:* T_{RC}=Read Cycle Time

DATA RETENTION WAVEFORM



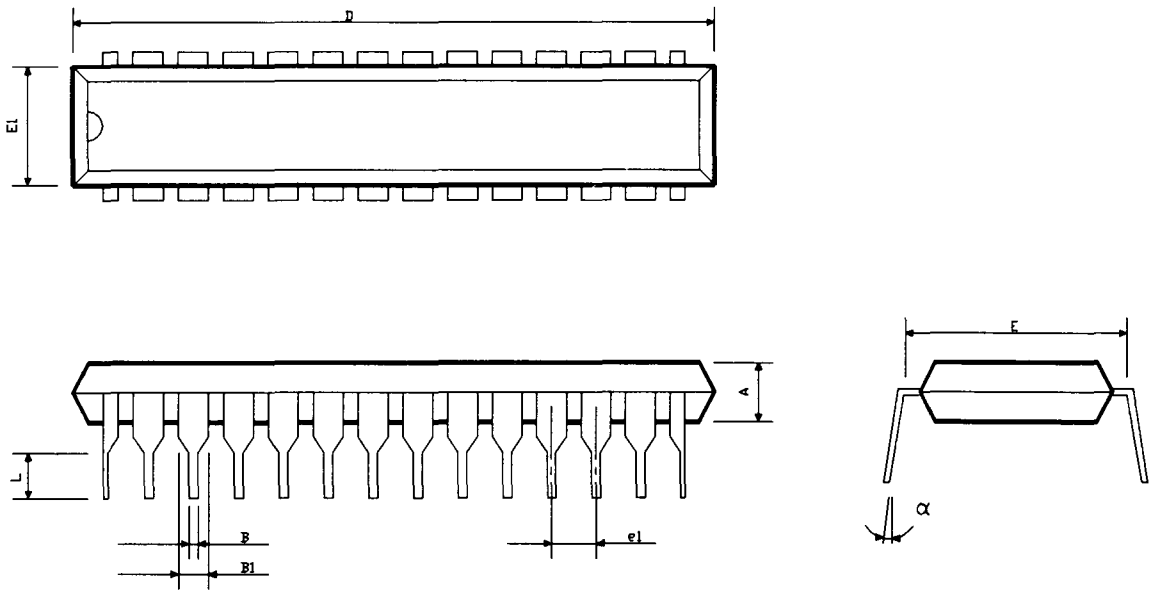
ORDERING INFORMATION

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package	Remark
W24256AJ-20	20	200	5	300mil SOJ	
W24256AJ-20L	20	200	0.1	300mil SOJ	Low Power
W24256AJ-25	25	180	5	300mil SOJ	
W24256AJ-25L	25	180	0.1	300mil SOJ	Low Power
W24256AJ-35	35	160	5	300mil SOJ	
W24256AJ-35L	35	160	0.1	300mil SOJ	Low Power
W24256AK-20	20	200	5	300mil Skinny	
W24256AK-20L	20	200	0.1	300mil Skinny	Low Power
W24256AK-25	25	180	5	300mil Skinny	
W24256AK-25L	25	180	0.1	300mil Skinny	Low Power
W24256AK-35	35	160	5	300mil Skinny	
W24256AK-35L	35	160	0.1	300mil Skinny	Low Power

Notes:

1. Winbond Electronics Corp. reserves the right to make design improvements and other changes to its products without notice.
2. Purchasers are responsible for performing appropriate quality assurance testing or products used in applications where personal injury might result from device failure.

28 LEAD P-DIP SKINNY



Symbol	Dimensions in inch	Dimensions in mm
A	0.130 ± 0.010	3.302 ± 0.254
B	0.018 ± 0.004	0.457 ± 0.102
B1	0.060 ± 0.004	1.524 ± 0.102
D	1.390 ± 0.010	35.306 ± 0.254
E	0.310 ± 0.010	7.874 ± 0.254
E1	0.290 ± 0.010	7.366 ± 0.254
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.135 ± 0.010	3.429 ± 0.254
α	0° ~ 15°	0° ~ 15°

Winbond

Winbond
Electronics Corp.

CORPORATE HEADQUARTERS:
No. 2, R&D Rd. VI,
Science-Based Industrial Park.
Hsin chu, Taiwan, R.O.C.
TEL: (035)770066
FAX: 886-35-774527

SALES OFFICE:
11 Fl, No. 673, Min Sheng E. Rd,
Taipei, Taiwan, R.O.C.
TEL: (02)7190505
TLX: 16485 WINTPE
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Room 305, 3/F, 17 Wang Hoi Road
Shun Fat Industrial Bldg. Kowloon Bay
Kowloon, Hong Kong
TEL: 7516023-7
FAX: 7552064

Winbond Electronics (North America) Corp.
3350, Scott Blvd., Bldg. #20
Santa Clara, CA 95054 U.S.A.
TEL: (408) 982-0381
FAX: (408) 982-9231

Winbond Europe
Leuvensesteenweg 613
B-1930 Zaventem, Belgium
TEL: (32) (2) 7592910
FAX: (32) (2) 7592964
TLX: 20370 BC.Zav.B.

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