To all our customers

We are pleased to inform you that National Semiconductor Corporation's Advanced PC (APC) Division joined Winbond Electronics Corporation on May 5th 2005. As a result, in this document "National Semiconductor Corporation" and "National" should be understood as "Winbond Electronics Corporation" and "Winbond", respectively.

Continuity
There is no change to this datasheet as a result of offering the device as a Winbond product.

For more information see our website:
    http://www.winbond.com

or contact APC Customer Support:
    APC.Support@winbond.com

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National
Semiconductor

PC87391, PC87392, PC87393, PC87393F
100-Pin LPC SuperI/O Devices for Portable Applications

General Description

National Semiconductor's PC8739x family of LPC SuperI/O devices is targeted for a wide range of portable applications. PC99 and ACPI compliant, the PC8739x family features an X-Bus Extension for read and write operations over the X-Bus, a full IEEE 1284 Parallel Port with a Parallel Port Multiplexer (PPM) for external Floppy Disk Drive (FDD) support, a Musical Instrument Digital Interface (MIDI) port, and a Game port. Like all National LPC SuperI/O devices, the PC8739x offers a single-chip solution to the most commonly used PC I/O peripherals.

The PC8739x family also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serializer for Parallel IRQs and an enhanced WATCH-DOG™ timer.

The following features apply to the PC87393F. The feature lists for other PC8739x devices may differ. See the table on page 3 for a list of features for each device.

Outstanding Features

- X-Bus Extension for read and write operations
- LPC bus interface, based on Intel's *LPC Interface Specification* Rev. 1.01, February 1999 (supports $\overline{\text{CLKRUN}}$ and $\overline{\text{LPCPD}}$ signals) and Intel FWH transactions
- PC99 and ACPI compliant
- Serial IRQ support (15 options)
- Interrupt Serializer (four Parallel IRQs to Serial IRQ)
- PPM for external FDD signal support
- MIDI interface compatible with MPU-401 UART mode
- Game port inputs for up to two joysticks
- Protection features, including GPIO lock and pin configuration lock
- 32 GPIO ports (16 standard, 16 with Assert IRQ/$\overline{\text{SMI}}$)
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 100-pin TQFP Package

Block Diagram

PC87393 / PC87393F
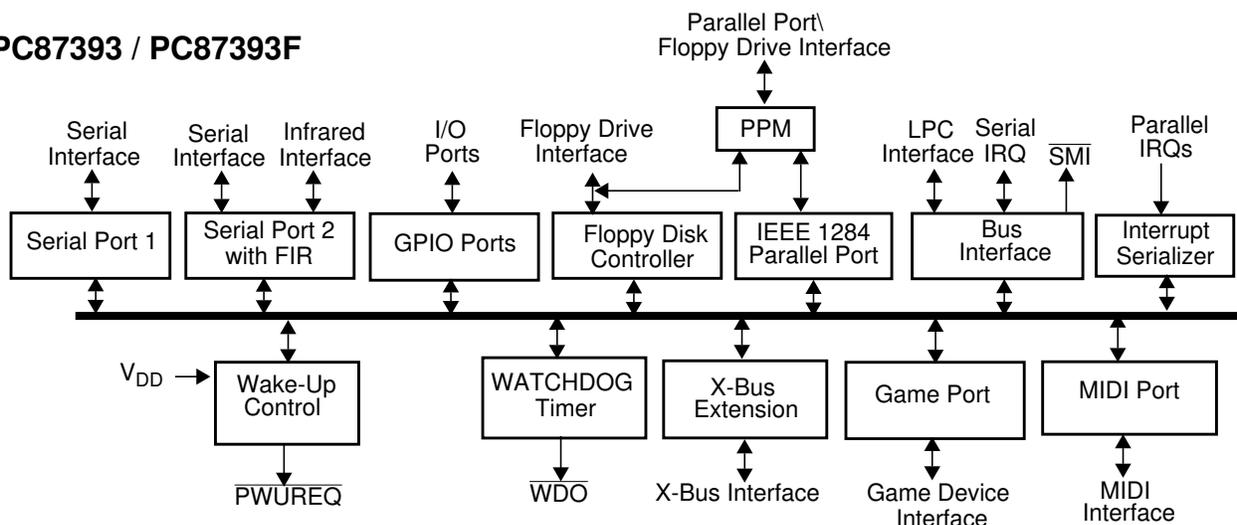
Features

- LPC System Interface
  - Synchronous cycles, up to 33 MHz bus clock
  - 8-bit I/O cycles
  - Up to four 8-bit DMA channels
  - $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support
  - Implements PCI mobile design guide recommendation (*PCI Mobile Design Guide 1.1, Dec. 18, 1998)*
  - Memory and FWH transaction support

- Interrupt Serializer
  - Four Parallel IRQs to Serial IRQ

- Musical Instrument Digital Interface (MIDI) Port
  - Compatible with MPU-401 UART mode
  - 16-byte Receive and Transmit FIFOs
  - Loopback mode support

- Game Port
  - Compatible with the Legacy Game Port definition
  - Full digital implementation
  - Supports up to two analog joysticks

- X-Bus Extension
  - Supports read and write operations
  - 8-bit data bus
  - Up to 28-bit address bus supports up to 256MB data
  - Two chip select pins
  - Interrupt routing via PIRQ pins
  - Supports BIOS flash devices

- PC99 and ACPI Compliant
  - PnP Configuration Register structure
  - Flexible resource allocation for all logical devices
    - ❏ Relocatable base address
    - ❏ Fifteen IRQ routing options
    - ❏ Four optional 8-bit DMA channels (where applicable)

- Clock Sources
  - 32.768 KHz, 14.318 MHz or 48 MHz clock input
  - LPC clock, up to 33 MHz

- Power Supply
  - 3.3V supply operation
  - All pins are 5V tolerant
  - All pins are back-drive protected, except LPC bus pins

- Wake-Up Control
  - Optional routing of IRQ to power-up event

- 32 General-Purpose I/O (GPIO) Ports
  - Sixteen standard, with Assert IRQ/$\overline{\text{SMI}}$ for 16 ports
  - Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - Programmable option for internal pull-up resistor on each input pin
  - Output lock option

- Input debounce mechanism

- Floppy Disk Controller (FDC)
  - Programmable write protect
  - FM and MFM mode support
  - Enhanced mode command for three-mode Floppy Disk Drive (FDD) support
  - Perpendicular recording drive support for 2.88 MB
  - Burst and non-burst modes
  - Full support for IBM Tape Drive register (TDR) implementation of AT and PS/2 drive types
  - 16-byte data FIFO
  - Error-free handling of data overrun and underrun
  - Software compatible with the PC8477, which contains a superset of the FDC functions in the µDP8473, the NEC µPD765A and the N82077
  - High-performance, digital separator
  - Standard 5.25" and 3.5" FDD support
  - Supports up to four floppy disk drives
  - Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
  - Supports external drive via parallel port pins

- IEEE 1284 compliant Parallel Port
  - ECP, including Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - EPP support as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages, even if the device is in power-down
  - Parallel Port Multiplexer (PPM) to support additional external FDC signals on parallel port pins for FDD use

- Serial Port 1 (SP1)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud

- Serial Port 2 with Fast Infrared (SP2 with FIR)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
  - FIR IrDA 1.1 compliant
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - DMA support – one or two channels
  - PnP dongle support

Features (Continued)

- WATCHDOG Timer
  - Times out the system based on user-programmable time-out period
  - System power-down capability for power saving
  - User-defined trigger events to restart WATCHDOG
  - Optional routing of WATCHDOG output on IRQ and/or SMI lines

- Strap Configuration
  - Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - Test strap to force the device into test mode (reserved for National Semiconductor use)
  - X-Bus straps (XCNF2-0) define the functionality of the X-Bus at reset

Device-specific Information

The following table shows the main features for each device in the PC87393 family.

Function[1]	PC87391	PC87392	PC87393	PC87393F
LPC System Interface	✔	✔	✔	✔
Interrupt Serializer	✔	✔	✔	✔
Musical Instrument Digital Interface (MIDI) Port	✘	✘	✔	✔
Game Port	✘	✘	✔	✔
X-Bus Extension	✘	✘	✔	✔
FWH Emulation	✘	✘	✘	✔
PC99 and ACPI Compliant	✔	✔	✔	✔
Wake-Up Control	✔	✔	✔	✔
General-Purpose I/O (GPIO) Ports	✘	✔	✔	✔
Floppy Disk Controller (FDC)	✔	✔	✔	✔
IEEE 1284 compliant Parallel Port	✔	✔	✔	✔
Serial Port 1 (SP1)	✔	✔	✔	✔
Serial Port 2 with Fast Infrared (SP2 with FIR)	✔	✔	✔	✔
WATCHDOG Timer	✔	✔	✔	✔

1. This datasheet contains notes that are device-specific. These notes can be found by searching for the specific device number.

Features (Continued)

The following set of device-specific Block Diagrams show the modules for each device in the PC87393 family.

PC87391
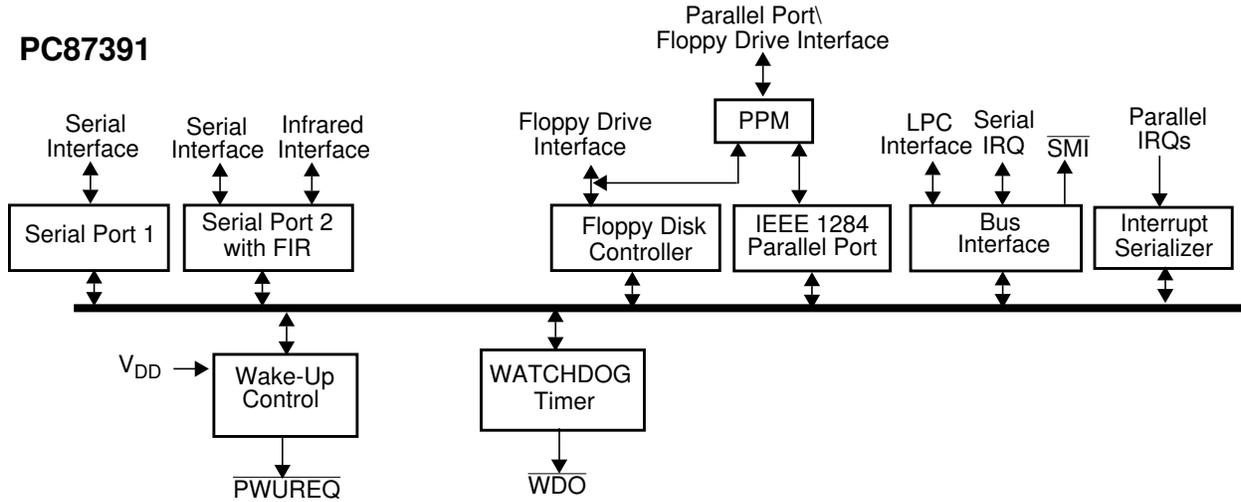
PC87392

PC87393 / PC87393F

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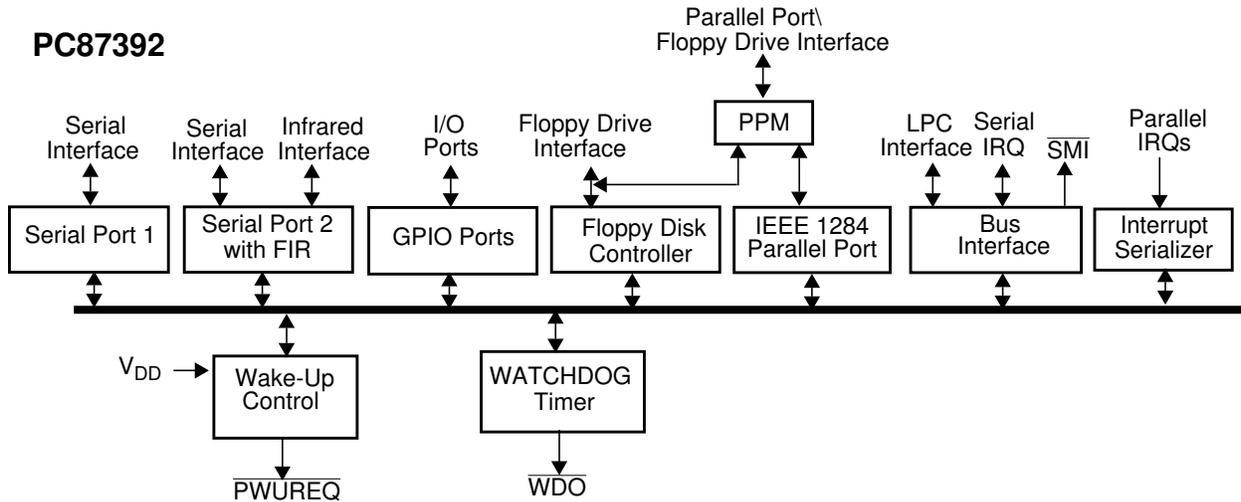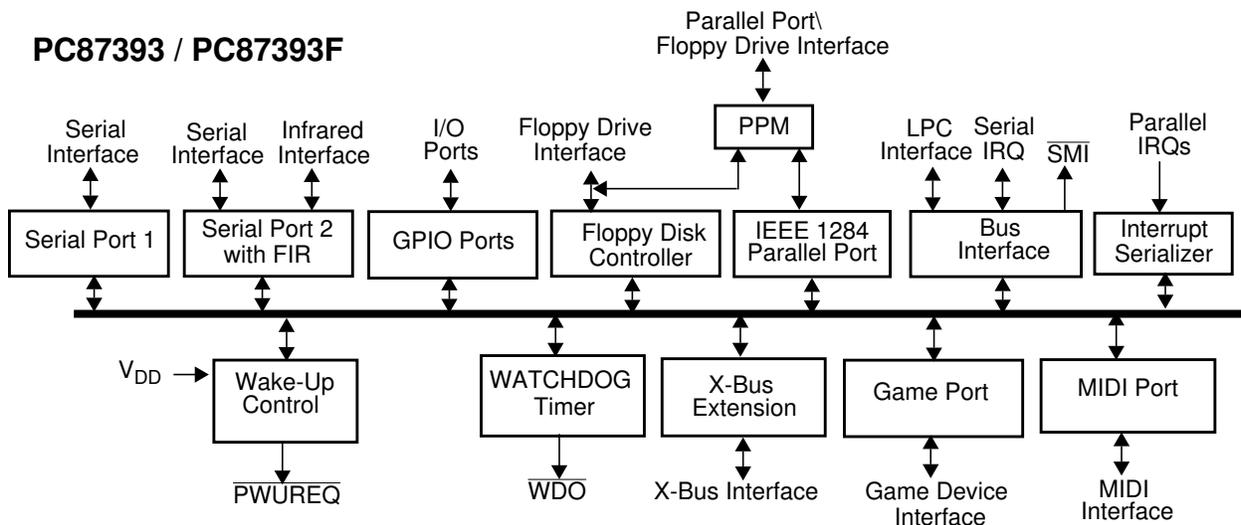# Table of Contents (Continued)

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1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAMS

Top pins (left to right, 75–51):
$\overline{DSR2}$, $\overline{DCD2}$, $\overline{MTR1}$/DRATE0, $\overline{DR1}$, IRSL2/$\overline{DR1}$, IRTX, IRRX1, IRRX2_IRSL0, IRSL1, IRSL3/PWUREQ, NC, VSS, VDD, $\overline{RI1}$, $\overline{DTR1}$_BOUT1/BADDR, $\overline{CTS1}$, SOUT1/XCNF0, $\overline{RTS1}$/TEST, SIN1, $\overline{DSR1}$, $\overline{DCD1}$, STB_$\overline{WRITE}$, $\overline{AFD}$_$\overline{DSTRB}$/DENSEL/DRATE1, PD0/$\overline{INDEX}$, ERR/HDSEL

Pin numbers top: 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51

Left pins:
- 76 SIN2
- 77 $\overline{RTS2}$
- 78 SOUT2
- 79 $\overline{CTS2}$
- 80 $\overline{DTR2}$_BOUT2
- 81 $\overline{RI2}$
- 82 NC
- 83 NC
- 84 $\overline{MTR1}$
- 85 NC
- 86 NC
- 87 NC
- 88 VDD
- 89 VSS
- 90 (XCNF2) NC
- 91 NC
- 92 NC
- 93 NC
- 94 NC
- 95 NC
- 96 NC
- 97 NC
- 98 NC
- 99 NC
- 100 NC

Center: **PC87391-VJG**

Right pins:
- 50 PD1/$\overline{TRK0}$
- 49 $\overline{INIT}$/$\overline{DIR}$
- 48 PD2/$\overline{WP}$
- 47 $\overline{SLIN}$_$\overline{ASTRB}$/$\overline{STEP}$
- 46 PD3/$\overline{RDATA}$
- 45 PD4/$\overline{DSKCHG}$
- 44 PD5/MSEN0
- 43 PD6/DRATE0
- 42 PD7/MSEN1
- 41 $\overline{ACK}$/$\overline{DR1}$
- 40 BUSY_$\overline{WAIT}$/$\overline{MTR1}$
- 39 VDD
- 38 VSS
- 37 PE/$\overline{WDATA}$
- 36 SLCT/$\overline{WGATE}$
- 35 PNF
- 34 DRATE0/IRSL2
- 33 DENSEL
- 32 $\overline{INDEX}$
- 31 $\overline{MTR0}$
- 30 $\overline{DR0}$
- 29 $\overline{DIR}$
- 28 $\overline{STEP}$
- 27 $\overline{WDATA}$
- 26 $\overline{WGATE}$

Pin numbers bottom: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

Bottom pins (left to right):
NC, NC, NC, (XCNF1) NC, $\overline{WDO}$, $\overline{CLKRUN}$, LPCPD, LCLK, $\overline{LRESET}$, SERIRQ, $\overline{LDRQ}$, $\overline{LFRAME}$, VSS, VDD, LAD0, LAD1, LAD2, LAD3, $\overline{SMI}$, CLKIN, $\overline{DSKCHG}$, HDSEL, $\overline{RDATA}$, $\overline{WP}$, $\overline{TRK0}$

NC - Not Connected (these pins should be left unconnected)

Thin Quad Flatpack (TQFP), JEDEC
Order Number PC87391-VJG
See NS Package Number VLJ100A

1.0 Signal/Pin Connection and Description (Continued)

Top pins (75–51):
GPIO16/$\overline{DSR2}$ (75), DCD2/GPIO17 (74), MTR1/DRATE0 (73), DR1/GPIO25 (72), GPIO37/IRSL2/$\overline{DR1}$ (71), IRTX (70), IRRX1 (69), IRRX2_IRSL0 (68), IRSL1 (67), IRSL3/PWUREQ (66), NC (65), VSS (64), VDD (63), RI1 (62), DTR1_BOUT1/BADDR (61), $\overline{CTS1}$ (60), SOUT1/XCNF0 (59), RTS1/TEST (58), SIN1 (57), $\overline{DSR1}$ (56), $\overline{DCD1}$ (55), STB_WRITE (54), AFD_DSTRB/DENSEL/DRATE1 (53), PD0/$\overline{INDEX}$ (52), ERR/HDSEL (51)

Left pins (76–100):
- GPIO15/SIN2 — 76
- GPIO14/$\overline{RTS2}$ — 77
- GPIO13/SOUT2 — 78
- GPIO12/$\overline{CTS2}$ — 79
- GPIO11/$\overline{DTR2}$_BOUT2 — 80
- GPIO10/$\overline{RI2}$ — 81
- GPIO33 — 82
- GPIO32 — 83
- GPIO31/$\overline{MTR1}$ — 84
- GPIO30 — 85
- GPIO27 — 86
- GPIO26 — 87
- VDD — 88
- VSS — 89
- (XCNF2) NC — 90
- GPIO24 — 91
- GPIO23 — 92
- GPIO22 — 93
- GPIO21 — 94
- GPIO20 — 95
- GPIO07 — 96
- GPIO06 — 97
- GPIO05 — 98
- GPIO04 — 99
- GPIO03 — 100

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Right pins (50–26):
- 50 — PD1/$\overline{TRK0}$
- 49 — $\overline{INIT}$/$\overline{DIR}$
- 48 — PD2/$\overline{WP}$
- 47 — $\overline{SLIN\_ASTRB}$/$\overline{STEP}$
- 46 — PD3/$\overline{RDATA}$
- 45 — PD4/$\overline{DSKCHG}$
- 44 — PD5/MSEN0
- 43 — PD6/DRATE0
- 42 — PD7/MSEN1
- 41 — $\overline{ACK}$/$\overline{DR1}$
- 40 — BUSY_$\overline{WAIT}$/$\overline{MTR1}$
- 39 — VDD
- 38 — VSS
- 37 — PE/$\overline{WDATA}$
- 36 — SLCT/$\overline{WGATE}$
- 35 — PNF
- 34 — DRATE0/IRSL2
- 33 — DENSEL
- 32 — $\overline{INDEX}$
- 31 — $\overline{MTR0}$
- 30 — $\overline{DR0}$
- 29 — $\overline{DIR}$
- 28 — $\overline{STEP}$
- 27 — $\overline{WDATA}$
- 26 — $\overline{WGATE}$

Bottom pins (1–25):
GPIO02 (1), GPIO01 (2), GPIO00 (3), (XCNF1) NC (4), GPIO34/$\overline{WDO}$ (5), GPIO36/$\overline{CLKRUN}$ (6), LPCPD (7), LCLK (8), $\overline{LRESET}$ (9), SERIRQ (10), $\overline{LDRQ}$ (11), $\overline{LFRAME}$ (12), VSS (13), VDD (14), LAD0 (15), LAD1 (16), LAD2 (17), LAD3 (18), GPIO35/$\overline{SMI}$ (19), CLKIN (20), $\overline{DSKCHG}$ (21), $\overline{HDSEL}$ (22), $\overline{RDATA}$ (23), $\overline{WP}$ (24), $\overline{TRK0}$ (25)

NC - Not Connected (these pins should be left unconnected)

Thin Quad Flatpack (TQFP), JEDEC
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1.0 Signal/Pin Connection and Description (Continued)

Top pin labels (pins 75–51):
- 75 XA18/GPIO16/JOYBBTN0/DSR2
- 74 XA19/DCD2/JOYABTN0/GPIO17
- 73 XCS1/MTR1/DRATE0/XIOWR
- 72 XCS0/DR1/XRDY/GPIO25
- 71 GPIO37/IRSL2/DR1/XIORD
- 70 IRTX
- 69 IRRX1
- 68 IRRX2_IRSL0
- 67 IRSL1
- 66 IRSL3/PWUREQ
- 65 NC
- 64 VSS
- 63 VDD
- 62 RI1
- 61 DTR1_BOUT1/BADDR
- 60 CTS1
- 59 SOUT1/XCNF0
- 58 RTS1/TEST
- 57 SIN1
- 56 DSR1
- 55 DCD1
- 54 STB_WRITE
- 53 AFD_DSTRB/DENSEL/DRATE1
- 52 PD0/INDEX
- 51 ERR/HDSEL

Left pin labels (pins 76–100):
- 76 GPIO15/JOYAX/SIN2/XA17
- 77 GPIO14/JOYBX/RTS2/XA16
- 78 GPIO13/JOYBY/SOUT2/XA15
- 79 GPIO12/JOYAY/CTS2/XA14
- 80 GPIO11/JOYBBTN1/DTR2_BOUT2/XA13
- 81 GPIO10/JOYABTN1/RI2/XA12
- 82 GPIO33/XIOWR/MDTX/XA11
- 83 GPIO32/XIORD/MDRX/XA10
- 84 GPIO31/MTR1/PIRQD/XA9
- 85 GPIO30/PIRQC/XA8
- 86 GPIO27/PIRQB/XA7
- 87 GPIO26/PIRQA/XSTB2/XA6
- 88 VDD
- 89 VSS
- 90 XSTB1/XCNF2/XA5
- 91 GPIO24/XSTB0/XA4
- 92 GPIO23/XA3
- 93 GPIO22/XA2
- 94 GPIO21/XA1
- 95 GPIO20/XA0
- 96 GPIO07/JOYABTN0/XD7
- 97 GPIO06/JOYBBTN0/XD6
- 98 GPIO05/JOYAX/XD5
- 99 GPIO04/JOYBX/XD4
- 100 GPIO03/JOYBY/XD3

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Right pin labels (pins 50–26):
- 50 PD1/TRK0
- 49 INIT/DIR
- 48 PD2/WP
- 47 SLIN_ASTRB/STEP
- 46 PD3/RDATA
- 45 PD4/DSKCHG
- 44 PD5/MSEN0
- 43 PD6/DRATE0
- 42 PD7/MSEN1
- 41 ACK/DR1
- 40 BUSY_WAIT/MTR1
- 39 VDD
- 38 VSS
- 37 PE/WDATA
- 36 SLCT/WGATE
- 35 PNF/XRDY
- 34 DRATE0/IRSL2
- 33 DENSEL
- 32 INDEX
- 31 MTR0
- 30 DR0
- 29 DIR
- 28 STEP
- 27 WDATA
- 26 WGATE

Bottom pin labels (pins 1–25):
- 1 GPIO02/JOYAY/XD2
- 2 GPIO01/JOYBBTN1/XD1
- 3 GPIO00/JOYABTN1/XD0
- 4 XCNF1/XWR
- 5 GPIO34/WDO/XRD
- 6 GPIO36/CLKRUN
- 7 LPCPD
- 8 LCLK
- 9 LRESET
- 10 SERIRQ
- 11 LDRQ
- 12 LFRAME
- 13 VSS
- 14 VDD
- 15 LAD0
- 16 LAD1
- 17 LAD2
- 18 LAD3
- 19 GPIO35/SMI
- 20 CLKIN
- 21 DSKCHG
- 22 HDSEL
- 23 RDATA
- 24 WP
- 25 TRK0

NC - Not Connected (these pins should be left unconnected)

**Thin Quad Flatpack (TQFP), JEDEC
Order Number PC87393-VJG
See NS Package Number VJG100A**

1.0 Signal/Pin Connection and Description (Continued)

Top side pins (left to right, pins 75–51):

- 75 — XA18/GPIO16/JOYBBTN0/$\overline{DSR2}$
- 74 — XA19/$\overline{DCD2}$/JOYABTN0/GPIO17
- 73 — $\overline{XCS1}$/MTR1/DRATE0/$\overline{XIOWR}$
- 72 — $\overline{XCS0}$/$\overline{DR1}$/XRDY/GPIO25
- 71 — GPIO37/IRSL2/$\overline{DR1}$/$\overline{XIORD}$
- 70 — IRTX
- 69 — IRRX1
- 68 — IRRX2_IRSL0
- 67 — IRSL1
- 66 — IRSL3/PWUREQ
- 65 — NC
- 64 — VSS
- 63 — VDD
- 62 — $\overline{RI1}$
- 61 — $\overline{DTR1}$_BOUT1/BADDR
- 60 — $\overline{CTS1}$
- 59 — SOUT1/XCNF0
- 58 — RTS1/TEST
- 57 — SIN1
- 56 — $\overline{DSR1}$
- 55 — $\overline{DCD1}$
- 54 — STB_WRITE
- 53 — AFD_$\overline{DSTRB}$/DENSEL/DRATE1
- 52 — PD0/$\overline{INDEX}$
- 51 — ERR/HDSEL

Left side pins (top to bottom, pins 76–100):

- 76 — GPIO15/JOYAX/SIN2/XA17
- 77 — GPIO14/JOYBX/$\overline{RTS2}$/XA16
- 78 — GPIO13/JOYBY/SOUT2/XA15
- 79 — GPIO12/JOYAY/$\overline{CTS2}$/XA14
- 80 — GPIO11/JOYBBTN1/$\overline{DTR2}$_BOUT2/XA13
- 81 — GPIO10/JOYABTN1/$\overline{RI2}$/XA12
- 82 — GPIO33/$\overline{XIOWR}$/MDTX/XA11
- 83 — GPIO32/$\overline{XIORD}$/MDRX/XA10
- 84 — GPIO31/$\overline{MTR1}$/PIRQD/XA9
- 85 — GPIO30/PIRQC/XA8
- 86 — GPIO27/PIRQB/XA7
- 87 — GPIO26/PIRQA/$\overline{XSTB2}$/XA6
- 88 — VDD
- 89 — VSS
- 90 — $\overline{XSTB1}$/XCNF2/XA5
- 91 — GPIO24/$\overline{XSTB0}$/XA4
- 92 — GPIO23/XA3
- 93 — GPIO22/XA2
- 94 — GPIO21/XA1
- 95 — GPIO20/XA0
- 96 — GPIO07/JOYABTN0/XD7
- 97 — GPIO06/JOYBBTN0/XD6
- 98 — GPIO05/JOYAX/XD5
- 99 — GPIO04/JOYBX/XD4
- 100 — GPIO03/JOYBY/XD3

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Right side pins (top to bottom, pins 50–26):

- 50 — PD1/$\overline{TRK0}$
- 49 — $\overline{INIT}$/DIR
- 48 — PD2/$\overline{WP}$
- 47 — $\overline{SLIN}$_ASTRB/STEP
- 46 — PD3/$\overline{RDATA}$
- 45 — PD4/$\overline{DSKCHG}$
- 44 — PD5/MSEN0
- 43 — PD6/DRATE0
- 42 — PD7/MSEN1
- 41 — $\overline{ACK}$/$\overline{DR1}$
- 40 — BUSY_WAIT/$\overline{MTR1}$
- 39 — VDD
- 38 — VSS
- 37 — PE/$\overline{WDATA}$
- 36 — SLCT/$\overline{WGATE}$
- 35 — PNF/XRDY
- 34 — DRATE0/IRSL2
- 33 — DENSEL
- 32 — $\overline{INDEX}$
- 31 — $\overline{MTR0}$
- 30 — $\overline{DR0}$
- 29 — $\overline{DIR}$
- 28 — $\overline{STEP}$
- 27 — $\overline{WDATA}$
- 26 — $\overline{WGATE}$

Bottom side pins (left to right, pins 1–25):

- 1 — GPIO02/JOYAY/XD2
- 2 — GPIO01/JOYBBTN1/XD1
- 3 — GPIO00/JOYABTN1/XD0
- 4 — XCNF1/$\overline{XWR}$
- 5 — GPIO34/$\overline{WDO}$/$\overline{XRD}$
- 6 — GPIO36/CLKRUN
- 7 — LPCPD
- 8 — LCLK
- 9 — $\overline{LRESET}$
- 10 — SERIRQ
- 11 — $\overline{LDRQ}$
- 12 — $\overline{LFRAME}$
- 13 — VSS
- 14 — VDD
- 15 — LAD0
- 16 — LAD1
- 17 — LAD2
- 18 — LAD3
- 19 — GPIO35/$\overline{SMI}$
- 20 — CLKIN
- 21 — $\overline{DSKCHG}$
- 22 — HDSEL
- 23 — RDATA
- 24 — WP
- 25 — $\overline{TRK0}$

NC - Not Connected (these pins should be left unconnected)

Thin Quad Flatpack (TQFP), JEDEC
Order Number PC87393-VJG
See NS Package Number VJG100A

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics are denoted by a buffer type symbol, described briefly below and in further detail in Section 9.2. The pin multiplexing information refers to three different types of multiplexing:

- Multiplexed, denoted by a slash (/) between pins in the diagram in Section 1.1. Pins are shared between two different functions. Each function is associated with different board connectivity, a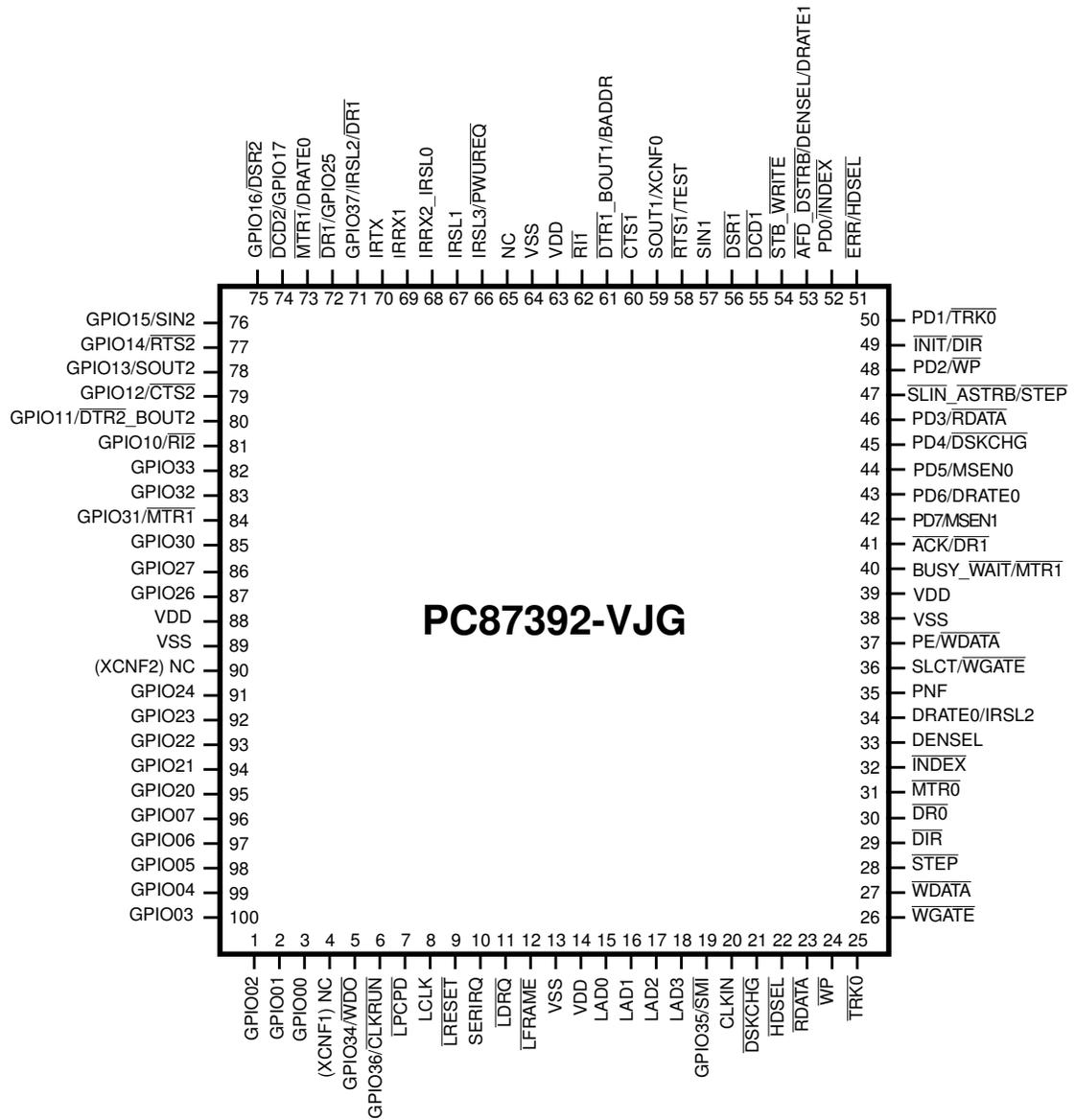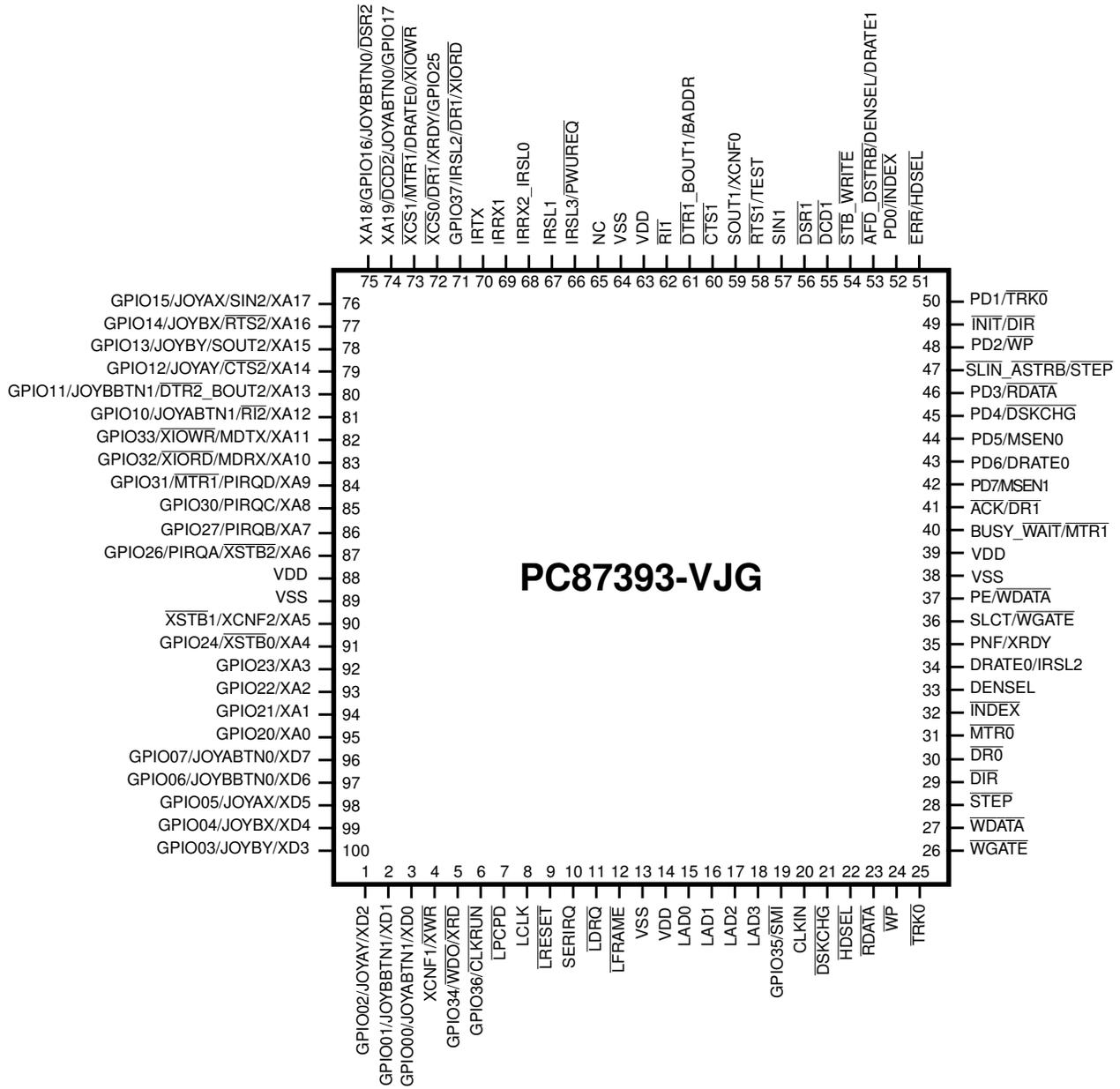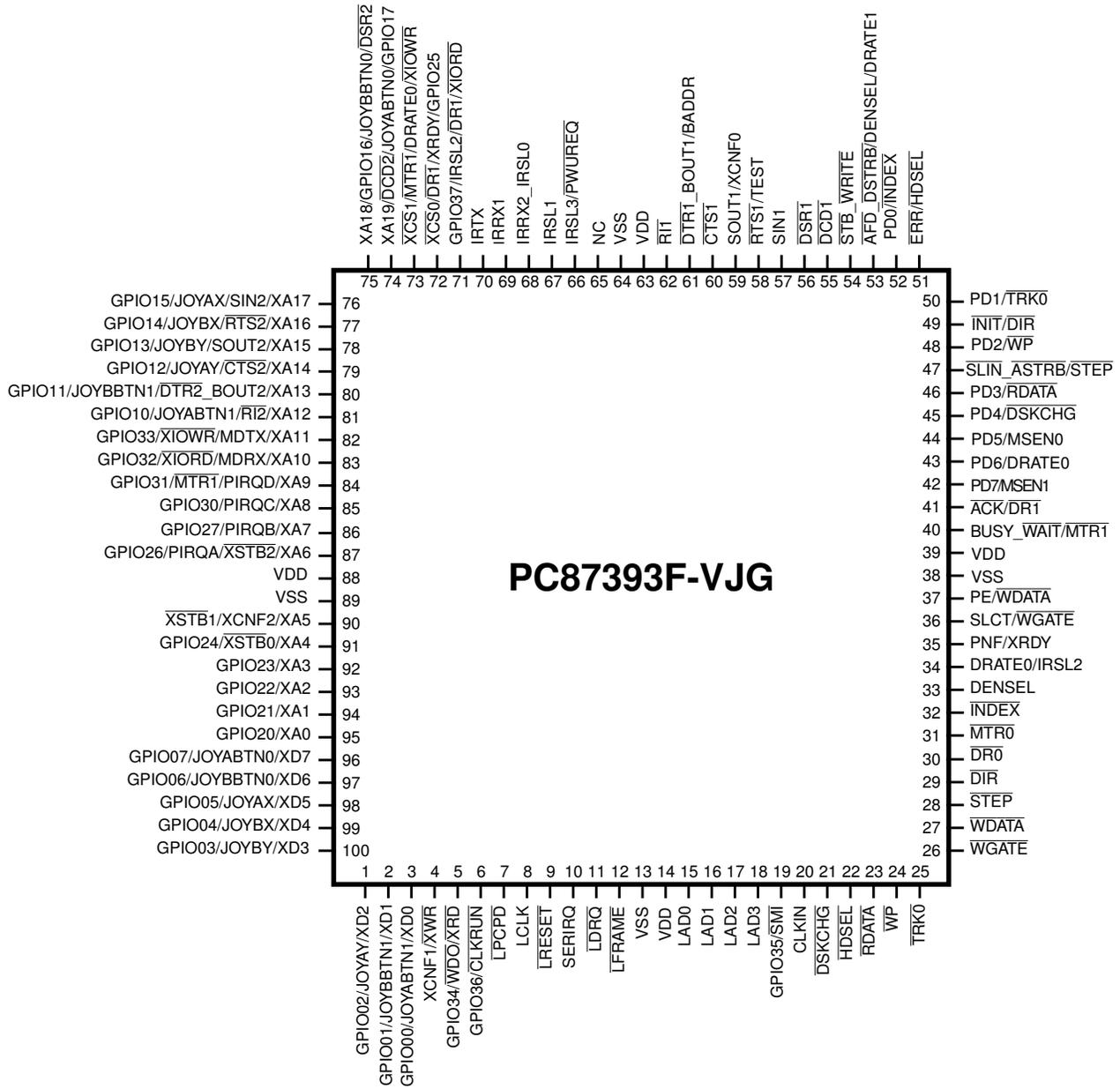nd normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS upon power-up, in order to comply with the board implementation.

- Multiple Mode, denoted by an underscore (_) between pins in the diagram in Section 1.1. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection may be controlled by the device driver, through the registers of the functional block, and do not require a special BIOS setup upon power-up. These pins are not considered multiplexed pins from the SuperI/O configuration perspective. The mode selection method (registers and bits) as well as the signal specification in each mode, are described within the functional description of the relevant functional block.

- Parallel Port Multiplexer, denoted by a slash (/) between pins in the diagram in Section 1.1. Parallel Port pins can be used to support external Floppy Disk Controller signals when the PPM is enabled and bit 7 of the SuperI/O Configuration 5 register (SIOCF5) is cleared. See Table 3 for a summary of all PPM options.

Table 1. Buffer Types

Symbol	Description
IN_C	Input, CMOS compatible
IN_{PCI}	Input, PCI 3.3V
IN_{STRP}	Input, Strap pin with weak pull-down during strap time
IN_T	Input, TTL compatible
IN_{TS}	Input, TTL compatible with Schmidt Trigger
O_{PCI}	Output, PCI 3.3V
$O_{p/n}$	Output, push-pull buffer that is capable of sourcing p mA and sinking n mA
OD_n	Output, open-drain output buffer that is capable of sinking n mA
PWR	Power pin
GND	Ground pin

1.3 PIN MULTIPLEXING

Table 2 groups all multiplexed PC8739x pins in their associated functional blocks, and provides links to the relevant configuration registers and bit values for selecting multiplexed options.

Table 2. Pin Multiplexing Configuration

Functional Block	Signal	Functional Block	Signal	Functional Block	Signal	Functional Block	Signal	Config Section
GPIO	GPIO00	X-Bus	XD0	Game Port	JOYABTN1			2.10.3
GPIO	GPIO01	X-Bus	XD1	Game Port	JOYBBTN1			2.10.3
GPIO	GPIO02	X-Bus	XD2	Game Port	JOYAY			2.10.3
GPIO	GPIO03	X-Bus	XD3	Game Port	JOYBY			2.10.3
GPIO	GPIO04	X-Bus	XD4	Game Port	JOYBX			2.10.3
GPIO	GPIO05	X-Bus	XD5	Game Port	JOYAX			2.10.3
GPIO	GPIO06	X-Bus	XD6	Game Port	JOYBBTN0			2.10.3

1.0 Signal/Pin Connection and Description (Continued)

Functional Block	Signal	Functional Block	Signal	Functional Block	Signal	Functional Block	Signal	Config Section
GPIO	GPIO07	X-Bus	XD7	Game Port	JOYABTN0			2.10.3
GPIO	GPIO10	X-Bus	XA12	Serial Port	$\overline{RI2}$	Game Port	JOYABTN1	2.10.3
GPIO	GPIO11	X-Bus	XA13	Serial Port	$\overline{DTR2\_BOUT2}$	Game Port	JOYBBTN1	2.10.3
GPIO	GPIO12	X-Bus	XA14	Serial Port	$\overline{CTS2}$	Game Port	JOYAY	2.10.3
GPIO	GPIO13	X-Bus	XA15	Serial Port	SOUT2	Game Port	JOYBY	2.10.3
GPIO	GPIO14	X-Bus	XA16	Serial Port	$\overline{RTS2}$	Game Port	JOYBX	2.10.3
GPIO	GPIO15	X-Bus	XA17	Serial Port	SIN2	Game Port	JOYAX	2.10.3
GPIO	GPIO16	X-Bus	XA18	Serial Port	$\overline{DSR2}$	Game Port	JOYBBTN0	2.10.3
GPIO	GPIO17	X-Bus	XA19	Serial Port	$\overline{DCD2}$	Game Port	JOYABTN0	2.10.3
GPIO	GPIO20	X-Bus	XA0					2.10.3
GPIO	GPIO21	X-Bus	XA1					2.10.3
GPIO	GPIO22	X-Bus	XA2					2.10.3
GPIO	GPIO23	X-Bus	XA3					2.10.3
GPIO	GPIO24	X-Bus	XA4	X-Bus	$\overline{XSTB0}$			2.10.3
GPIO	GPIO25	X-Bus	$\overline{XCS0}$	X-Bus	XRDY	FDC	$\overline{DR1}$	2.10.5
GPIO	GPIO26	X-Bus	XA6	X-Bus	PIRQA	X-Bus	$\overline{XSTB2}$	2.10.3
GPIO	GPIO27	X-Bus	XA7	X-Bus	PIRQB			2.10.4
GPIO	GPIO30	X-Bus	XA8	X-Bus	PIRQC			2.10.4
GPIO	GPIO31	X-Bus	XA9	X-Bus	PIRQD	FDC	$\overline{MTR1}$	2.10.4
GPIO	GPIO32	X-Bus	XA10	MIDI Port	MDRX	X-Bus	$\overline{XIORD}$	2.10.4
GPIO	GPIO33	X-Bus	XA11	MIDI Port	MDTX	X-Bus	$\overline{XIOWR}$	2.10.4
GPIO	GPIO34	X-Bus	$\overline{XRD}$	WATCHDOG	$\overline{WDO}$			2.10.5
GPIO	GPIO35	LPC Bus	$\overline{SMI}$					2.10.5
GPIO	GPIO36	LPC Bus	$\overline{CLKRUN}$					2.10.5
GPIO	GPIO37	FDC	$\overline{DR1}$	FIR	IRSL2	X-Bus	$\overline{XIORD}$	2.10.6
X-Bus	$\overline{XCS1}$	FDC	$\overline{MTR1}$	FDC	DRATE0	X-Bus	$\overline{XIOWR}$	2.10.5
Wake-Up Control	$\overline{PWUREQ}$	FIR	IRSL3					2.10.11
FDC	DRATE0	FIR	IRSL2					2.10.6
Serial Port	DTR1_BOUT1	Strap	BADDR					
Serial Port	SOUT1	Strap	XCNF0					
Serial Port	RTS1	Strap	TEST					
X-Bus	$\overline{XWR}$	Strap	XCNF1					
Parallel Port	PNF	X-Bus	XRDY					2.10.6

1.0 Signal/Pin Connection and Description (Continued)

1.4 PARALLEL PORT MULTIPLEXER (PPM)

The Floppy Disk Controller (FDC) signals in Table 3 are directed to the associated Parallel Port (PP) pins either when the PNF signal is low and bits 6-5 of the SuperI/O Configuration 5 register (SIOCF5) are set to 01, or when the PNF signal is high and bits 6-5 are set to 10.

Table 3. FDC Signals on Parallel Port Pins

Parallel Port Pin	FDC Signal
PD0	$\overline{\text{INDEX}}$
PD1	$\overline{\text{TRK0}}$
PD2	$\overline{\text{WP}}$
PD3	$\overline{\text{RDATA}}$
PD4	$\overline{\text{DSKCHG}}$
PD5	MSEN0
PD6	DRATE0
PD7	MSEN1
$\overline{\text{SLIN\_ASTRB}}$	$\overline{\text{STEP}}$
$\overline{\text{AFD\_DSTRB}}$	DENSEL/DRATE1
INIT	$\overline{\text{DIR}}$
$\overline{\text{ACK}}$	$\overline{\text{DR1}}$
$\overline{\text{ERR}}$	$\overline{\text{HDSEL}}$
SLCT	$\overline{\text{WGATE}}$
PE	$\overline{\text{WDATA}}$
BUSY_WAIT	$\overline{\text{MTR1}}$

1.0 Signal/Pin Connection and Description (Continued)

1.0 Signal/Pin Connection and Description (Continued)

1.5 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all the signals used in the PC8739x family. Some members of the PC8739x family implement a subset of these signals. Refer to the table on page 3 to identify the functions relevant to a specific device.

1.5.1 Bus Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD3-0	18-15	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**LPC Address-Data.** Multiplexed command, address bi-directional data and cycle status.
LCLK	8	I	IN_{PCI}	V_{DD}	**LPC Clock**. Same 33 MHz clock as the PCI clock.
$\overline{LDRQ}$	11	O	O_{PCI}	V_{DD}	**LPC DMA Request**. Encoded DMA request for LPC interface.
$\overline{LFRAME}$	12	I	IN_{PCI}	V_{DD}	**LPC Frame**. Low pulse indicates the beginning of new LPC cycle or termination of a broken cycle.
$\overline{LRESET}$	9	I	IN_{PCI}	V_{DD}	**LPC Reset.** Practically the PCI system reset.
SERIRQ	10	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{SMI}$	19	OD	OD_{12}	V_{DD}	**System Management Interrupt**
$\overline{LPCPD}$	7	I	IN_{PCI}	V_{DD}	**Power Down.** Indicates that power is going to be shut on the LPC interface.
$\overline{CLKRUN}$	6	I/OD	IN_{PCI}/OD_{12}	V_{DD}	**Clock Run.** Indicates that LCLK is going to be stopped, and requests full-speed LCK (same as PCI $\overline{CLKRUN}$).

1.5.2 Clock

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CLKIN	20	I	IN_T	V_{DD}	**Clock In.** Active clock input signal of 32.768 KHz, 14.318 MHz or 48 MHz.

1.5.3 Infrared (IR)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
IRRX1	69	I	IN_{TS}	V_{DD}	**IR Receive 1.** Primary input to receive serial data from the IR transceiver. Monitored during power-off for wake-up event detection.
IRRX2_IRSL0	68	I/O	$IN_{TS}/O_{3/6}$	V_{DD}	**IRRX2 - IR Receive 2.** Auxiliary IR receiver input to support a second transceiver. Monitored during power-off for wake-up event detection.
IRSL1	67	I/O	$IN_T/O_{3/6}$	V_{DD}	**IRSL3-0 IR Select**. Outputs are used to control the IR transceivers. Input for PnP identification of plug-in IR transceiver (dongle).
IRSL2	71, 34	I/O	$IN_T/O_{3/6}$	V_{DD}	
IRSL3	66	I	IN_T	V_{DD}	After reset, the dual function IRSLX pins wake up in input mode. After the ID is read by the IR driver, these pins can be put into output mode. The output mode is controlled by Serial Port 2.
IRTX	70	O	$O_{6/12}$	V_{DD}	**IR Transmit.** IR serial output data.

1.0 Signal/Pin Connection and Description (Continued)

1.5.4 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	33, 53	O	$O_{2/12}$	V_{DD}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected.
$\overline{DIR}$	29, 49	O	$OD_{12}, O_{2/12}$	V_{DD}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation.
$\overline{DR1}$ $\overline{DR0}$	41, 71, 72 30	O	$OD_{12}, O_{2/12}$	V_{DD}	**Drive Select.** Decoded output signals in 2-drive mode, or encoded signals in 4-drive mode. Controlled by bits 1 and 0 of the Digital Output register (DOR).
DRATE0	34, 73	O	$O_{3/6}$	V_{DD}	**Data Rate 0.** Reflects the value of bit 0 of the Configuration Control register (CCR) or the Data Rate Select register (DSR), whichever was written to last.
DRATE1	53	O	$O_{3/6}$	V_{DD}	**Data Rate 1.** Reflects the value of bit 1 of the Configuration Control register (CCR) or the Data Rate Select register (DSR), whichever was written to last. Available on the PPM pins only.
$\overline{DSKCHG}$	21, 45	I	IN_T	V_{DD}	**Disk Change.** Indicates if the drive door has been opened.
$\overline{HDSEL}$	22, 51	O	$OD_{12}, O_{2/12}$	V_{DD}	**Head Select.** Determines which side of the FDD is accessed. Active low selects side 1, inactive selects side 0.
$\overline{INDEX}$	32, 52	I	IN_T	V_{DD}	**Index.** Indicates the beginning of an FDD track.
MSEN1, 0	42, 44	I	IN_T	V_{DD}	**Automatic Media Sense.** Identifies the media type of the floppy disk in drive 1 and 0, if the drive supports this protocol.
$\overline{MTR1}$ $\overline{MTR0}$	84, 73, 40 31	O	$OD_{12}, O_{2/12}$	V_{DD}	**Motor Select.** Active low, motor enable lines for drive 1 and 0, controlled by bits D7-4 of the Digital Output register (DOR). MTR0 is used to decode DR1 and DR0 in 4-drive mode.
$\overline{RDATA}$	23, 46	I	IN_T	V_{DD}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{STEP}$	28, 47	O	$OD_{12}, O_{2/12}$	V_{DD}	**Step.** Issues pulses to the FDD at a software programmable rate to move the head during a seek operation.
$\overline{TRK0}$	25, 50	I	IN_T	V_{DD}	**Track 0.** Indicates to the controller that the head of the selected FDD is at track 0.
$\overline{WDATA}$	27, 37	O	$OD_{12}, O_{2/12}$	V_{DD}	**Write Data**. Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.
$\overline{WGATE}$	26, 36	O	$OD_{12}, O_{2/12}$	V_{DD}	**Write Gate.** Enables the write circuitry of the selected FDD. WGATE is designed to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
$\overline{WP}$	24, 48	I	IN_T	V_{DD}	**Write Protected.** Indicates that the disk in the selected drive is write protected.

1.0 Signal/Pin Connection and Description (Continued)

1.5.5   Game Port (PC87393 and PC87393F)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
JOYAX	98, 76	I/O	IN_{TS}/OD_{12}	V_{DD}	**Joystick A X-Axis.** Indicates X-axis position of joystick .
JOYAY	1, 79	I/O	IN_{TS}/OD_{12}	V_{DD}	**Joystick A Y-Axis.** Indicates Y-axis position of joystick A
JOYABTN0	96, 74	I	IN_{TS}	V_{DD}	**Joystick A Button 0.** Indicates button 0 status of joystick A
JOYABTN1	3, 81	I	IN_{TS}	V_{DD}	**Joystick A Button 1.** Indicates button 1 status of joystick A
JOYBX	99, 77	I/O	IN_{TS}/OD_{12}	V_{DD}	**Joystick B X-Axis.** Indicates X-axis position of joystick B
JOYBY	100, 78	I/O	IN_{TS}/OD_{12}	V_{DD}	**Joystick BY-Axis.** Indicates Y-axis position of joystick B
JOYBBTN0	97, 75	I	IN_{TS}	V_{DD}	**Joystick B Button 0.** Indicates button 0 status of joystick B
JOYBBTN1	2, 80	I	IN_{TS}	V_{DD}	**Joystick B Button 1.** Indicates button 1 status of joystick B

1.5.6   General-Purpose Input/Output (GPIO) Ports (PC87392, PC87393 and PC87393F)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
GPIO00-07	3, 2, 1, 100, 99, 98, 97, 96	I/O	$IN_{TS}/$ $OD_6, O_{3/6}$	V_{DD}	**General-Purpose I/O Port 0, bits 0-7.** Each pin is configured independently as input or I/O, with or without static pull-up, and with either open-drain or totem-pole output type. The port support interrupt assertion and each pin can be enabled or masked as an interrupt source.
GPIO10-17	81, 80, 79, 78, 77, 76, 75, 74	I/O	$IN_{TS}/$ $OD_6, O_{3/6}$	V_{DD}	**General-Purpose I/O Port 1, bits 0-7.** Same as Port 0.
GPIO20-27	95, 94, 93, 92, 91, 72, 87, 86	I/O	$IN_{TS}/$ $OD_6, O_{3/6}$	V_{DD}	**General-Purpose I/O Port 2, bits 0-7.** Same as Port 0, without interrupt support.
GPIO30-37	85, 84, 83, 82, 5, 19, 6, 71	I/O	$IN_{TS}/$ $OD_6, O_{3/6}$	V_{DD}	**General-Purpose I/O Port 3, bits 0-7.** Same as Port 0, without interrupt support.

1.5.7   Musical Instrument Digital Interface (MIDI) Port (PC87393 and PC87393F)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
MDTX	82	O	$O_{3/6}$	V_{DD}	**MIDI Transmit.** MIDI serial data output
MDRX	83	I	IN_{TS}	V_{DD}	**MIDI Receive**. MIDI serial data input

1.0 Signal/Pin Connection and Description (Continued)

1.5.8 Parallel Port

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{ACK}$	41	I	IN_T	V_{DD}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the Parallel Port.
AFD_DSTRB	53	O	OD_{14}, $O_{14/14}$	V_{DD}	**AFD - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. **DSTRB - Data Strobe (EPP).** Active low, used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_WAIT	40	I	IN_T	V_{DD}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the Parallel Port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	51	I	IN_T	V_{DD}	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	49	O	OD_{14}, $O_{14/14}$	V_{DD}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. Use an external 4.7 KΩ pull-up resistor.
PD7-3, PD2, PD1 PD0	42-46, 48, 50, 52	I/O	IN_T $O_{14/14}$	V_{DD}	**Parallel Port Data.** Transfer data to and from the peripheral data bus and the appropriate Parallel Port data register. These signals have a high current drive capability.
PE	37	I	IN_T	V_{DD}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	36	I	IN_T	V_{DD}	**Select.** Set active high by the printer when the printer is selected.
SLIN_ASTRB	47	O	OD_{14}, $O_{14/14}$	V_{DD}	**SLIN - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Uses an external 4.7 KΩ pull-up resistor. **ASTRB - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).
STB_WRITE	54	O	OD_{14}, $O_{14/14}$	V_{DD}	**STB - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. **WRITE - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{WRITE}$ becomes inactive (high).
PNF	35	I	IN_T	V_{DD}	**Printer Not Floppy.** This signal selects the internal logical device that is connected to the PPM pins. For details on setting PNF polarity, see Section 2.10.6.

1.5.9 Power and Ground

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
V_{DD}	14, 39, 63, 88	I	PWR	-	**Main 3.3V Power Supply**
V_{SS}	13, 38, 64, 89	I	GND	-	**Ground**

1.0 Signal/Pin Connection and Description (Continued)

1.5.10   Serial Port 1 and Serial Port 2 (SP1 and SP2)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{CTS1}$ $\overline{CTS2}$	60 79	I	IN$_{TS}$	V$_{DD}$	**Clear to Send.** When low, indicate that the modem or other data transfer device is ready to exchange data.
$\overline{DCD1}$ $\overline{DCD2}$	55 74	I	IN$_{TS}$	V$_{DD}$	**Data Carrier Detected.** When low, indicate that the modem or other data transfer device has detected the data carrier.
$\overline{DSR1}$ $\overline{DSR2}$	56 75	I	IN$_{TS}$	V$_{DD}$	**Data Set Ready.** When low, indicate that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{DTR1\_}$ $\overline{BOUT1}$ $\overline{DTR2\_}$ $\overline{BOUT2}$	61 80	O	O$_{3/6}$	V$_{DD}$	**Data Terminal Ready.** When low, indicate to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{DTR}$ function and set these signals to inactive high. Loopback operation holds them inactive. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 register is set. $\overline{DTR1}\_BOUT1$ is used also as BADDR.
$\overline{RI1}$ $\overline{RI2}$	62 81	I	IN$_{TS}$	V$_{DD}$	**Ring Indicator.** When low, indicate that a telephone ring signal has been received by the modem. They are monitored during power-off for wake-up event detection.
$\overline{RTS1}$ $\overline{RTS2}$	58 77	O	O$_{3/6}$	V$_{DD}$	**Request to Send.** When low, indicate to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive. $\overline{RTS1}$ is used also as TEST.
SIN1 SIN2	57 76	I	IN$_{TS}$	V$_{DD}$	**Serial Input.** Receive composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT1 SOUT2	59 78	O	O$_{3/6}$	V$_{DD}$	**Serial Output.** Send composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.

1.0 Signal/Pin Connection and Description (Continued)

1.5.11 Strap Configuration

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
BADDR	61	I	IN_{STRP}	V_{DD}	**Base Address.** Sampled at Reset to determine the base address of the configuration Index-Data register pair, as follows. No pull-up resistor: 2Eh-2Fh 10K external pull-up resistor: 4Eh-4Fh
TEST	58	I	IN_{STRP}	V_{DD}	**Test.** Forces the device into test mode if an external pull-up resistor is connected. Otherwise, the pin is pulled to '0' (zero) by the internal resistor.
XCNF2-0	90, 4, 59	I	IN_{STRP}	V_{DD}	**X-Bus Reset Configuration Mode.** Forces the X-Bus transaction to be in one of the following modes: no BIOS, normal or latch. For details, see Chapter 7. **Pins** **2 1 0 Functionality** x 0 0 No BIOS[1] x 0 1 Normal Mode, XRDY disabled 0 1 0 Latch Mode, XA12-19, XRDY enabled 1 1 0 Latch Mode, GPIO10-17, XRDY enabled 0 1 1 Latch Mode, XA12-19, XRDY disabled 1 1 1 Latch Mode, GPIO10-17, XRDY disabled Pulled to 0 by internal resistor, or set to 1 by external 10K pull-up resistor.

1.   In the **PC87391 and PC87392,** the XCNFi signals must be set to this value. This is value is guaranteed by the internal pull-down resistors, as long as the pins are not connected, or the load is small enough.

1.5.12 Wake-Up Control

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
PWUREQ	66	O	OD_6	V_{DD}	**Power-Up Request.** Active (low) level indicates that wake-up event has occurred, and causes the chipset to turn the power supply on, or to exit its current sleep state.

1.5.13 WATCHDOG Timer

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{WDO}$	5	O	OD_6, $O_{3/6}$	V_{DD}	**WATCHDOG Out.** Low level indicates that the WATCHDOG Timer has reached its time-out period without being retriggered. The output type and an optional pull-up are configurable.

1.5.14 X-Bus Extension (PC87393 and PC87393F)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{XRD}$	5	O	$O_{3/6}$	V_{DD}	**Read.** Active (low) level indicates read cycle on the X-Bus Extension.
$\overline{XWR}$	4	O	$O_{3/6}$	V_{DD}	**Write.** Active (low) level indicates write cycle on the X-Bus Extension.
$\overline{XIORD}$	83, 71	O	$O_{3/6}$	V_{DD}	**I/O Read.** Active (low) level indicates I/O read cycle on the X-Bus Extension. This signal is for devices that require separate read/write inputs for memory and I/O.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{\text{XIOWR}}$	82, 73	O	$O_{3/6}$	V_{DD}	**I/O Write.** Active (low) level indicates I/O write cycle on the X-Bus Extension. This signal is for devices that require separate read/write inputs for memory and I/O.
XD7-0	96, 97, 98, 99, 100, 1, 2, 3	I/O	$IN_{TS}/O_{3/6}$	V_{DD}	**Data Bus**
XA19-0	74-95	O	$O_{3/6}$	V_{DD}	**Address Bus**
$\overline{\text{XCS}}$1-0	73, 72	O	$O_{3/6}$	V_{DD}	**Chip Select.** These signals control the selection of up to two chips residing on the X-Bus Extension.
$\overline{\text{XSTB}}$2-0	87, 90, 91	O	$O_{3/6}$	V_{DD}	**Assert Strobe.** These signals control the selection of up to three external latch devices for X-Bus Latched Address Mode transactions.
XRDY	72, 35	I	IN_{TS}	V_{DD}	**I/O Ready.** This signal indicates to the PC87393 to extend the access cycles.
PIRQA-D	87-84	I	IN_{TS}	V_{DD}	**Parallel Interrupt.** Convert parallel interrupts into serial interrupts by means of the Interrupt Serializer (The interrupt number associated with each signal is a part of the system configuration.)

1.6 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 4 can optionally support internal pull-up (PU) and/or pull-down (PD) resistors. See Section 9.3 for the values of each resistor type.

Table 4. Internal Pull-Up and Pull-Down Resistors

Signal	Pin/s	Type	Comments
Game Port (GMP) (PC87393 and PC87393F)			
JOYABTN0		PU_{25}	Programmable
JOYABTN1		PU_{25}	Programmable
JOYBBTN0		PU_{25}	Programmable
JOYBBTN1		PU_{25}	Programmable
General-Purpose Input/Output (GPIO) Ports (PC87392, PC87393 and PC87393F)			
GPIO00-07		PU_{25}	Programmable
GPIO10-17		PU_{25}	Programmable
GPIO20-27		PU_{25}	Programmable
GPIO30-37		PU_{25}	Programmable
Musical Instrument Digital Interface (MIDI) Port (PC87393 and PC87393F)			
MDRX		PU_{25}	Programmable
Strap Configuration			
BADDR		PD_{40}	Strap
TEST		PD_{15}	Strap

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin/s	Type	Comments
XCNF0		PD_{40}	Strap
XCNF1		PD_{40}	Strap
XCNF2		PD_{40}	Strap
Parallel Port			
$\overline{ACK}$		PU_{220}	
$\overline{AFD\_DSTRB}$		PU_{220}	
BUSY_WAIT		PD_{120}	
$\overline{ERR}$		PU_{220}	
$\overline{INIT}$		PU_{220}	
PE		$PU_{220}/$ PD_{120}	Programmable
SLCT		PD_{120}	
$\overline{SLIN\_ASTRB}$		PU_{220}	
$\overline{STB\_WRITE}$		PU_{220}	
WATCHDOG Timer (WDT)			
$\overline{WDO}$		PU_{30}	Programmable

2.0   Device Architecture and Configuration

The PC8739x SuperI/O device comprises a collection of legacy and proprietary functional blocks. Each functional block is described in a separate chapter in this document. However, some parameters in the implementation of each functional block may vary per SuperI/O device. This chapter describes the PC8739x structure and provides all logical device specific information, including special implementation of generic blocks, system interface and device configuration.

2.1   OVERVIEW

The PC8739x consists of 9 logical devices, the host interface, and a central set of configuration registers, all built around a central, internal bus. The internal bus is similar to an 8-bit ISA bus protocol. See Figure 1, which illustrates the blocks and related logic.

The system interface serves as a bridge between the external LPC interface and the internal bus. It supports 8-bit Read and Write transactions for I/O, memory, DMA, and FWH, as defined in Intel's *LPC Interface Specification, Revision 1.01*.

The central configuration register set is ACPI compliant and supports a PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel and Microsoft. All system resources assigned to the functional blocks (I/O address space, DMA channels and IRQ lines) are configured in, and managed by, the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals.

2.2   CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is comprised of a set of banked registers which are accessed via a pair of specialized registers.

2.2.1   The Index-Data Register Pair

Access to the SuperI/O configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset, according to the state of the hardware strapping option on the BADDR pin. Table 5 shows the selected base addresses as a function of BADDR.
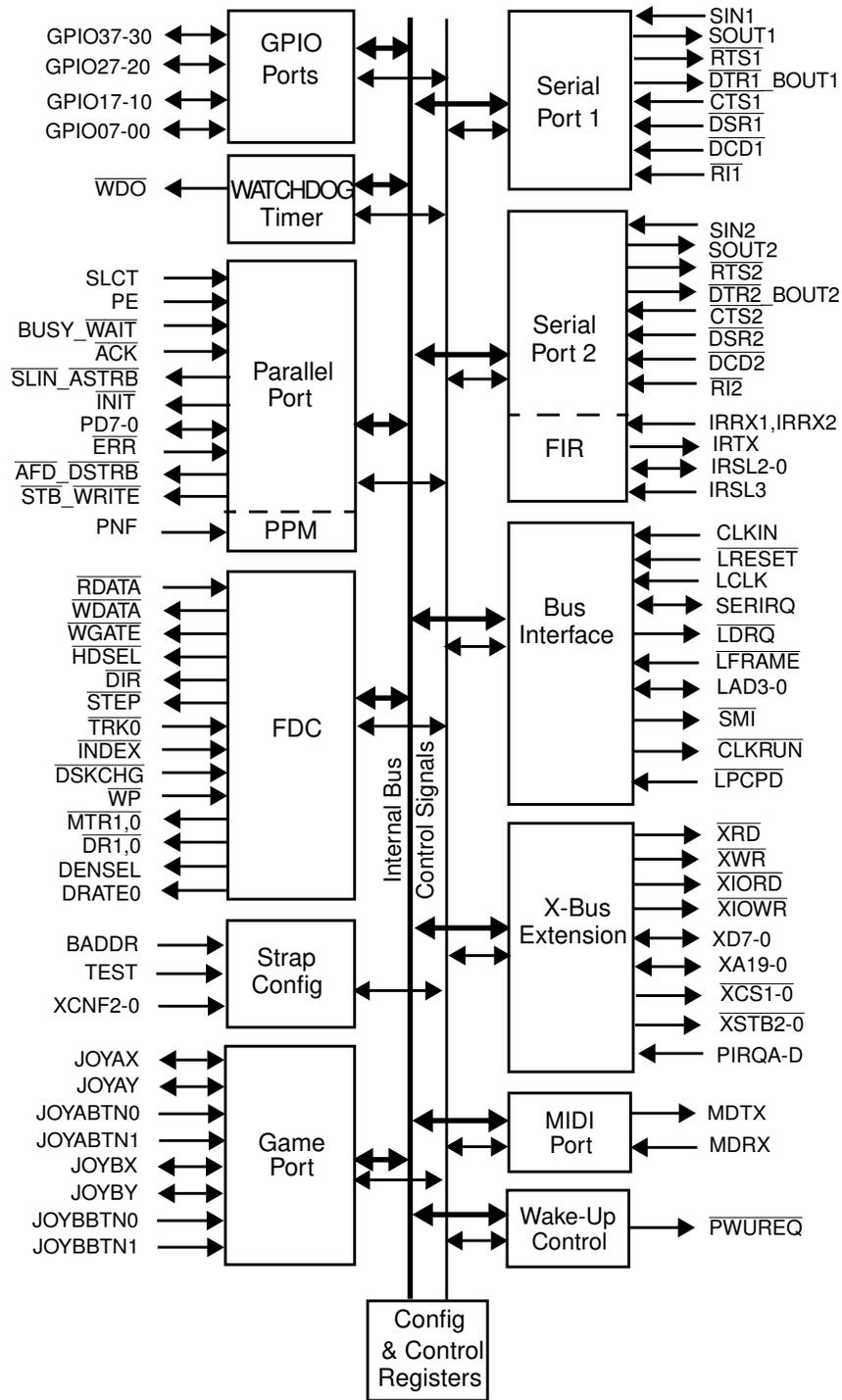
Table 5. BADDR Strapping Options

BADDR	I/O Address	
	Index Register	**Data Register**
0	2Eh	2Fh
1	4Eh	4Fh

The Index register is an 8-bit read/write register located at the selected base address (Base+0). It is used as a pointer to the configuration register file, and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit register (Base+1) used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

2.0 Device Architecture and Configuration (Continued)

Left side signals	Block	
GPIO37-30	GPIO Ports	
GPIO27-20		
GPIO17-10		
GPIO07-00		

WDO — WATCHDOG Timer

Parallel Port:
- SLCT
- PE
- BUSY_WAIT
- ACK
- SLIN_ASTRB
- INIT
- PD7-0
- ERR
- AFD_DSTRB
- STB_WRITE
- PNF — PPM

FDC:
- RDATA
- WDATA
- WGATE
- HDSEL
- DIR
- STEP
- TRK0
- INDEX
- DSKCHG
- WP
- MTR1,0
- DR1,0
- DENSEL
- DRATE0

Strap Config:
- BADDR
- TEST
- XCNF2-0

Game Port:
- JOYAX
- JOYAY
- JOYABTN0
- JOYABTN1
- JOYBX
- JOYBY
- JOYBBTN0
- JOYBBTN1

Internal Bus / Control Signals

Serial Port 1:
- SIN1
- SOUT1
- RTS1
- DTR1_BOUT1
- CTS1
- DSR1
- DCD1
- RI1

Serial Port 2 / FIR:
- SIN2
- SOUT2
- RTS2
- DTR2_BOUT2
- CTS2
- DSR2
- DCD2
- RI2
- IRRX1,IRRX2
- IRTX
- IRSL2-0
- IRSL3

Bus Interface:
- CLKIN
- LRESET
- LCLK
- SERIRQ
- LDRQ
- LFRAME
- LAD3-0
- SMI
- CLKRUN
- LPCPD

X-Bus Extension:
- XRD
- XWR
- XIORD
- XIOWR
- XD7-0
- XA19-0
- XCS1-0
- XSTB2-0
- PIRQA-D

MIDI Port:
- MDTX
- MDRX

Wake-Up Control:
- PWUREQ

Config & Control Registers

Note: Not all members of the PC8739x family contain all these blocks. For device-specific information, see the Block Diagrams on Page 4.

Figure 1. PC8739x Detailed Block Diagram

2.0 Device Architecture and Configuration (Continued)

2.2.2   Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 6 shows the LDN values of the PC8739x functional blocks. Any value not listed is reserved.

Figure 2 shows the structure of the standard configuration register file. The SuperI/O control and configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over 9 banks for 9 logical devices. Therefore, accessing a specific register in a specific bank is performed by two dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher physically accesses the logical device configuration registers currently pointed to by the Index register, within the logical device currently selected by the LDN register.
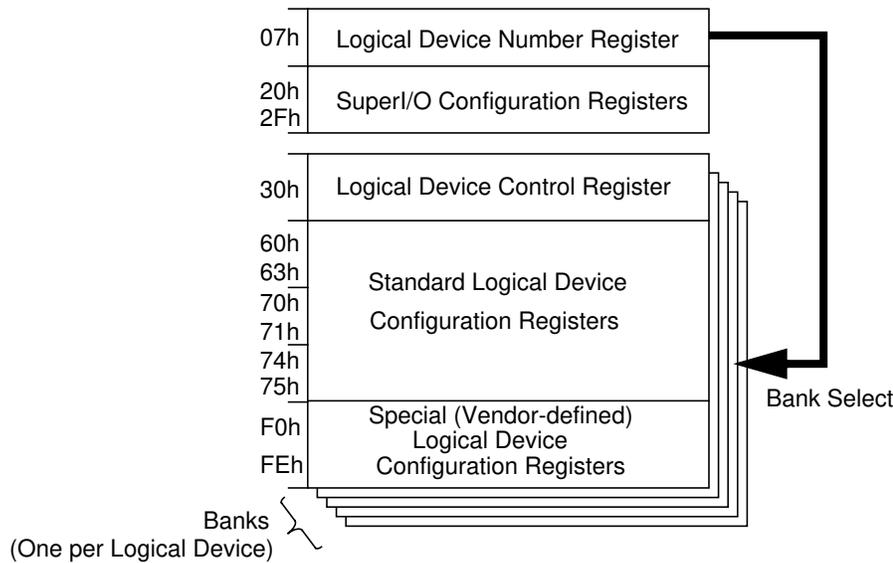
Figure 2. Structure of Standard Configuration Register File

Table 6. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 with IR (SP2)
03h	Serial Port 1 (SP1)
07h	General-Purpose I/O (GPIO) Ports (PC87392, PC87393 and PC87393F only)
0Ah	WATCHDOG Timer (WDT)
0Bh	Game Port (GMP) (PC87393 and PC87393F only)
0Ch	Musical Instrument Digital Interface (MIDI) Port (PC87393 and PC87393F only)
0Fh	X-Bus Extension (PC87393 and PC87393F only)

Write accesses to unimplemented registers (i.e. accessing the Data register while the Index register points to a non-existing register), are ignored and read returns 00h on all addresses, except for 74h and 75h (DMA configuration registers) which returns 04h (indicating no DMA channel is active). The configuration registers are accessible immediately after reset.

2.0 Device Architecture and Configuration (Continued)

2.2.3   Standard Logical Device Configuration Register Definitions

In the registers below, any undefined bit is reserved. Unless otherwise noted, the following definitions also hold true:

- All registers are read/write.

- All reserved bits return 0 on reads, except where noted otherwise. To prevent unpredictable results, do not modify these bits. Use read-modify-write to prevent the values of reserved bits from being changed during write.

- Write only registers should not use read-modify-write during updates.

Table 7. Standard Control Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 6 for valid numbers. All other values are reserved.
20h - 2Fh	SuperI/O Configuration	SuperI/O configuration registers and ID registers

Table 8. Logical Device Activate Register

Index	Register Name	Description

30h	Activate	Bit 0 - Logical device activation control
		    0: Disabled
		    1: Enabled
		Bits 7-1 - Reserved

Note: When the X-Bus Extension is disabled, access to its registers (not the PnP registers) is disabled, but all bridging functions continue to operate according to its register settings.

Table 9. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits (15-8) Descriptor 0	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits (7-0) Descriptor 0	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 0.

2.0 Device Architecture and Configuration (Continued)

Table 10. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number and Wake-Up on IRQ Enable	Indicates selected interrupt number. Bits 7-5 - Reserved. Bit 4 - Enables wake-up on the IRQ of the logical device. When enabled, IRQ assertion triggers a wake-up event. 0: Disabled (default) 1: Enabled Bits 3–0 select the interrupt number. A value of 1 selects IRQL1. A value of 15 selects IRQL15. IRQL0 is not a valid interrupt selection and represents no interrupt selection.
71h	Interrupt Request Type Select	Indicates the type and level of the interrupt request number selected in the previous register. If a logical device supports only one type of interrupt, this register is read only. Bits 7–2 - Reserved. Bit 0 - Type of interrupt request selected in the previous register. 0: Edge 1: Level Bit 1 - Level of the interrupt request selected in the previous register. 0: Low polarity 1: High polarity

Table 11. DMA Configuration Registers

Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 - The first DMA channel in case of using more than one DMA channel). Bits 7-3 - Reserved. Bits 2-0 select the DMA channel for DMA 0. The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 - The second DMA channel in case of using more than one DMA channel). Bits 7-3 - Reserved. Bits 2-0 select the DMA channel for DMA 1. The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.

Table 12. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FEh	Logical Device Configuration	Special (vendor-defined) configuration options

2.0 Device Architecture and Configuration (Continued)

2.2.4   Standard Configuration Registers

Index	Register Name
07h	Logical Device Number
20h	SuperI/O ID
21h	SuperI/O Configuration 1
22h	SuperI/O Configuration 2
23h	SuperI/O Configuration 3
24h	SuperI/O Configuration 4
25h	SuperI/O Configuration 5
26h	SuperI/O Configuration 6
27h	SuperI/O Revision ID
28h	SuperI/O Configuration 8
29h	SuperI/O Configuration 9
2Ah	SuperI/O Configuration A
2Bh - 2Eh	Reserved exclusively for National use
30h	Logical Device Control (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h - F9h	Device Specific Logical Device Configuration 1 to 10

SuperI/O Control and Configuration Registers

Logical Device Control and Configuration Registers - one per Logical Device (some are optional)

Figure 3. Configuration Register Map

SuperI/O Control and Configuration Registers

The SuperI/O configuration registers at indexes 20h and 27h are mainly used for part identification, global power management and the selection of pin multiplexing options. For details, see Section 2.10.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See functional block descriptions in the following sections.

Control

The only implemented control register for each logical device is the Activate register at index 30h. Bit 0 of the Activate register controls the activation of the associated functional block. Activation enables access to the functional block's registers, and attaches its system resources, which are unassigned as long as it is not activated. Other effects may apply, on a function-specific basis (such as clock enable and active pinout signaling).

Standard Configuration

The standard configuration registers manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60-61h, holding the first 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at index 62-63h is used for logical devices with more than one

2.0 Device Architecture and Configuration (Continued)

continuous register set. Interrupt Number and Wake-Up on IRQ Enable (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

Special Configuration

The vendor-defined registers, starting at index F0h, control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection, and non-standard extensions to generic functions.

2.2.5   Default Configuration Setup

The default configuration setup of the PC8739x can include two reset types, described below. See specific register descriptions for the bits affected by each reset type.

- **Software Reset**

  This reset is enabled by bit 1 of the SIOCF1 register, which resets all logical devices. A software reset also resets most bits in the SuperI/O control and configuration registers (see Section 2.10 for the bits not affected). This reset does not affect register bits that are locked for write access.

- **Hardware Reset**

  This reset is activated by the assertion of the $\overline{\text{LRESET}}$ input. It resets all logical devices. It also resets all SuperI/O control and configuration registers.

In event of a hardware reset, the PC8739x wakes up with the following default configuration setup:

— The configuration base address is 2Eh or 4Eh, according to the BADDR strap pin value, as shown in Table 5.

— All logical devices are disabled, with the exception of the X-Bus which remains functional but whose registers cannot be accessed.

— All multiplexed GPIO pins are configured according to the strap pins. When configured as GPIO, they have an internal static pull-up (default direction is input) except GPIO36.

In event of either a hardware or a software reset, the PC8739x wakes up with the following default configuration setup:

— The legacy devices are assigned with their legacy system resource allocation.

— The National proprietary functions are not assigned with any default resources and the default values of their base addresses are all 00h.

2.2.6   Power States

The following terminology is used in this document to describe the various possible power states:

- **Power On**
  V_{DD} is active.

- **Power Off**
  V_{DD} is inactive.

2.2.7   Address Decoding

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded within the functional block to determine the offset of the accessed register, within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore the lower bits of the base address register are forced to 0 (read only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base address of the FDC, Serial Port 1, Serial Port 2 with FIR are limited to the I/O address range of 00h to 7FXh only (bits 11-15 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of the non-legacy logical devices, including the GMP, MIDI and X-Bus, are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 10 in the Parallel Port). For more details, see the description of the base address register for each logical device.

The X-Bus extension serves as a bridge from the LPC to the X-Bus. For module control and security function registers, the 16-bit base address is applied through the configuration address space. The lower 4 address bits are decoded within the X-Bus for accessing each register. The address ranges in the LPC I/O space, LPC memory space and FWH memory space that are bridged to the X-Bus are defined in the SuperI/O configuration section for the X-Bus bridge. The number of address bits used for this decoding varies according to the specified zones and their sizes. See Section 2.19.2 and Section 2.19.3 for details of the address range specifications.

2.0 Device Architecture and Configuration (Continued)

2.3 THE CLOCK MULTIPLIER

The source of all internal clocks in the chip is either an external 48 MHz clock on the CLKIN pin, or the on-chip clock multiplier. The clock multiplier is fed by applying a clock source at one of two frequencies on the CLKIN pin: 32.768 KHz or 14.31818 MHz. The clock multiplier generates two internal clocks, 24 MHz and 48 MHz. These clocks are needed for all the modules in the PC8739x with the exception of the X-Bus module. After power-up or reset, the clock (clock multiplier or external clock) is disabled.

2.3.1 Functionality

The on-chip clock multiplier starts working when it is enabled by bit 2 of the SIOCF9 register, index 29h, i.e., when its value changes from 0 to 1 (only for source clocks 32.768 KHz or 14.31818 MHz). This bit can also disable the clock multiplier and its output clock after the multiplier is enabled. Once enabled, the output clock is frozen to a steady logic level until the multiplier provides a stable output clock that meets all requirements. Then the clock starts toggling.

On power-up when V_{DD} is applied, the chip wakes up with the on-chip clock multiplier disabled. The input and output clocks of the clock multiplier may toggle regardless of the state of the Master Reset (MR) pin. The clock multiplier waits for a toggling input clock.

Bit 3 of the SIOCF9 register, a read only bit, is the Valid Clock Multiplier status bit. While stabilizing, the output clock is frozen to a steady logic level, and the status bit is cleared to 0 to indicate a frozen clock. When the clock multiplier is stable, the output clock starts toggling and the status bit is set to 1. It tells the software when the clock multiplier is ready. The software should poll this status bit until it is set (1), and only then activate (enable) the FDC, Parallel Port, UARTs and infrared interface. When the multiplier is enabled for the first time after power-up, more time is required until this status bit is set to 1.

The clock multiplier and its output clock do not consume power when they are disabled.

2.3.2 Chip Power-Up

To ensure proper operation, proceed as follows after power-up:

1. Set bits 2, 1 and 0 of the Clock Control Configuration register (SIOCF9) at index 29h according to the clock source used (even if the external clock is the default frequency setting). See Table 13. Bits 2, 1 and 0 may be written in a single write cycle. From this point on, bits 1 and 0 of the SIOCF9 register are read only. The value of the clock source cannot be changed, except by a total power-down and power-up cycle. However, the clock can be disabled at any time.

Table 13. Clock Multiplier Encoding Options

External Source on CLKIN Pin	SIOCF9 Register (Index 29h)			
	Valid Clock Multiplier Status	Clock Enable	Chip Clock Source	
	Bit 3	Bit 2	Bit 1	Bit 0
External 48 MHz clock	Always 1	1	0	0
32.768 KHz clock multiplier	0 = Frozen 1 = Stable	1	0	1
14.31818 MHz clock multiplier		1	1	0
No clock	0	0	10, 01, 00	

2. Enable the clock.

If the clock source is 32.768 kHz or 14.31818 MHz:

— Poll bit 3 of the SIOCF9 register while the clock multiplier is stabilizing.

— When bit 3 of SIOCF9 is set to 1, go to step 3.

3. Enable any module in the chip, as needed.

2.3.3 Disabling the Clock

Before disabling the clock multiplier (by clearing bit 2 of SIOCF9 Register) or the external clock (for 48 MHz), make sure that all PC8739x modules are disabled. This is done by polling bit 4 of the SIOCF9 register (Module Enable Status) for 0.

2.3.4 Specifications

Wake-up time is 33 msec (maximum). This is measured from valid V_{DD} toggling of the input clock and multiplier enabled until the clock is stable. Tolerance (long term deviation) of the multiplier output clock, relative to the input clock, is ±110 ppm. Total tolerance is therefore ± (input clock tolerance + 110 ppm). Cycle by cycle variance is 0.4 nsec (maximum).

2.0 Device Architecture and Configuration (Continued)

2.4 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request (PIRQ) signals received from external devices, via the PIRQn (n can be A, B, C or D) pins and from internal IRQ sources, into serial interrupt request data transmitted over the SERIRQ bus. This enables the integration of devices that support only parallel IRQs in a system which supports only serial IRQs.

PIRQ signals that enter the device or internal IRQs are fed into an IRQ Mapping, Enable, and Polarity Control block. This block maps them to their associated IRQ slots. The IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and transmitted over the SERIRQ bus.

The PIRQn input value is routed to the Interrupt Serializer as the IRQ value to be driven onto IRQ slot n.

The same slot cannot be shared among different interrupt sources in this device.

When a transition is sensed on an IRQ source, the new value of the IRQ source is transmitted over the SERIRQ bus during the corresponding IRQ slot. For example, when a transition on PIRQA is sensed, the new value of PIRQA is transmitted during slot n of the SERIRQ bus.

Figure 4 shows the mechanism for both interrupt serialization and wake-up.
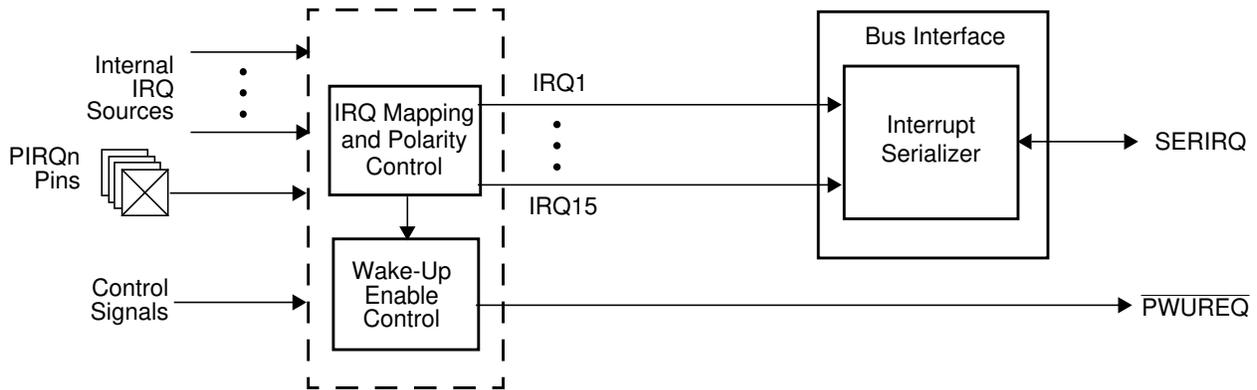
Figure 4. Interrupt Serialization and Wake-Up Mechanism

2.5 WAKE-UP CONTROL

The Wake-Up Control module receives the parallel interrupt request (PIRQn) signals from external devices and the IRQ signals from internal sources. It generates the $\overline{PWUREQ}$ system wake-up signal. All mapped IRQ signals, both internal and external, enter the Wake-Up Enable Control block. If one of them becomes active and is enabled for wake-up, an active $\overline{PWUREQ}$ signal is generated.

2.6 THE PARALLEL PORT MULTIPLEXER (PPM)

The Parallel Port Multiplexer (PPM) allows connection of an external Floppy Disk Drive (FDD) through the Parallel Port connector (25-pin DIN) instead of, or in addition to, the internal FDD on the normal FDC header. This is done by turning the Parallel Port pins into an additional set of FDC pins, while isolating them from Parallel Port functionality (see Section 1.4 for a signal multiplexing description).

A printer, or any other parallel device, may be exchanged with an external FDD without turning the system off. The PPM logic automatically detects whether a parallel device or the FDD is connected, and routes the Parallel Port pins to either the Parallel Port or the FDC functional blocks accordingly. See Figure 5.

To enable PPM mode, set bits 6-5 (Pin 35 Function Select) of the SIOCF5 register to the values that represent the desired configuration (see Section 2.10.6). The control of the connection, after enabling PPM mode, is done by bit SIOCF5[7] (PNF status) of this register as follows:

- PNF status = 1, PPM is inactive and the Parallel Port pins are assigned Parallel Port functionality

- PNF status = 0, PPM is active and the Parallel Port pins are assigned FDC functionality.

The value of bit SIOCF5[7] is determine by the PNF pin signal and the PNF polarity setting (bits SIOCF5[6:5]).

When PPM mode is disabled (both bits 6-5 of the SIOCF5 register = 0), the Parallel Port pins are assigned Parallel Port functionality, regardless of the value of PNF.

The internal FDD on the normal FDC pins, and the external FDD on the Parallel Port pins can be assigned as Drive A and Drive B, respectively, or the drive assignment can be switched between them.

2.0 Device Architecture and Configuration (Continued)

The Parallel Port pins function as an FDD interface for either drive 1 or drive 3. See Figure 5 for the internal routing between the PPM and FDC, and the Parallel Port and FDC pin-sets when PPM mode is active. The FDC output signals are driven simultaneously both on the normal FDC pins and on the corresponding Parallel Port pins. The FDC inputs are received from the FDC pins when either drive 0 or drive 2 is selected, and from the corresponding Parallel Port pins when either drive 1 or drive 3 is selected.

The Parallel Port output signals are isolated from the Parallel Port pins. The Parallel Port input signals, as reflected by the STR register, assume one of two possible values ([$\overline{BUSY}$, PE, SLCT, $\overline{ACK}$] = 1001 or 1111), indicating that nothing is connected to the Parallel Port. The default values are controlled by bit 2 of the Parallel Port Configuration register (see Section 2.12.3 for details).

PPM is in power save mode when PPM is active and the PPM power save mode bit is enabled.See Section 2.6.1 for details.
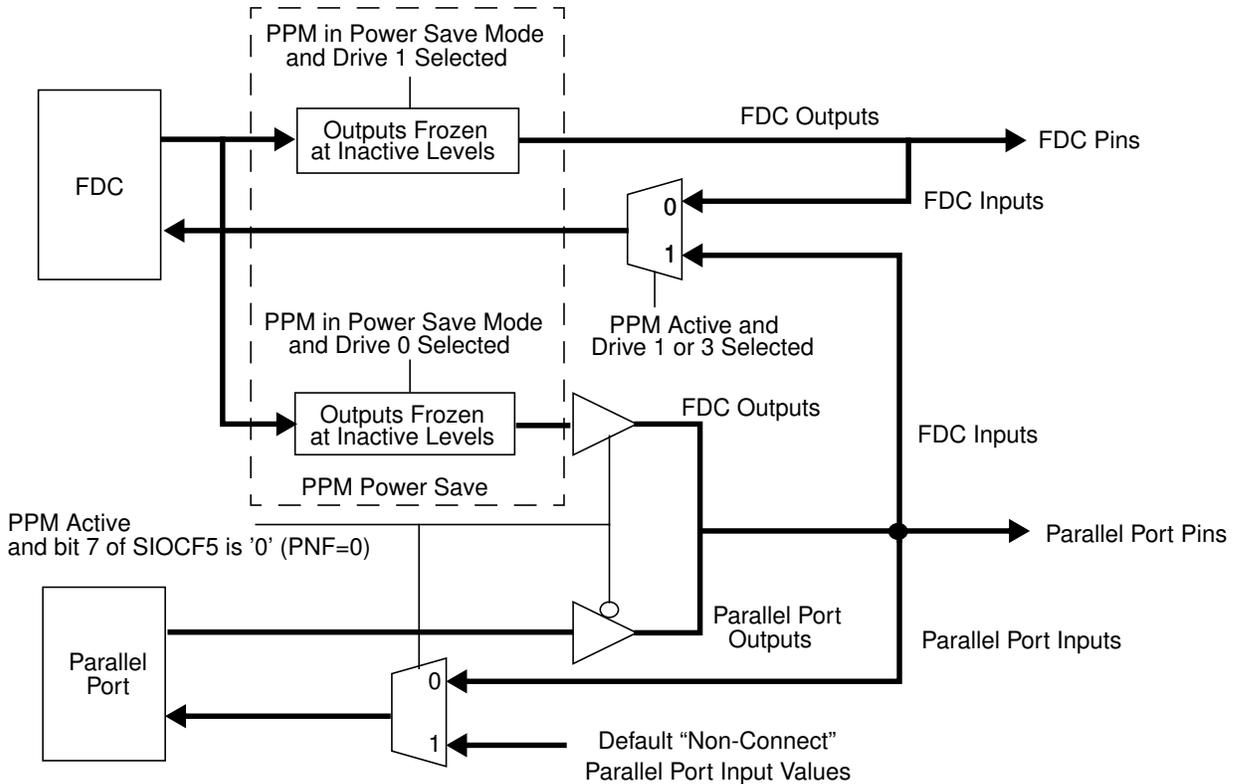
Figure 5. PPM Routing

2.6.1   PPM Power Save Mode

PPM power save mode helps avoid the additional power consumption associated with driving two sets of FDD outputs by limiting the activity to the selected drive only. PPM power save mode is enabled by bit 2 of the SIOCF5 register, and is in effect only when the PPM is active. Assuming that the internal FDD (on the normal FDC pins) is drive 0, while the external FDD (on the Parallel Port pins) is drive 1, the outputs of the non-selected drive do not toggle, but rather are frozen at their inactive levels. Table 14 shows the behavior of the FDC outputs on both the FDC and Parallel Port pins when the PPM is active and PPM power save mode is enabled.

Table 14. FDC Output Status in PPM Power Save Mode

$\overline{DR0}$ Signal	$\overline{DR1}$ Signal	FDC Outputs	
		FDC Pins	**Parallel Port Pins**
0	1	Functional	Frozen at inactive levels
1	0	Frozen at inactive levels	Functional
1	1	Functional	Functional

2.0 Device Architecture and Configuration (Continued)

2.7 PROTECTION

The PC8739x provides features to protect the PC at software levels. It can be locked to protect configuration bits or alteration of the device hardware configuration, as well as internal GPIO settings and several types of configuration settings.

All protection mechanisms can be used optionally.

2.7.1 Pin Configuration Lock

To lock the pin configuration of the PC8739x in order to prevent unwanted changes to hardware configuration, set bit 7 of the SIOCF1 register to 1. This causes all function select configuration bits to become read only bits. This bit can only be cleared by a hardware reset.

2.7.2 GPIO Pin Function Lock

The PC8739x is capable of locking the attributes of each GPIO pin. The following attributes can be locked:

- Output enable
- Output type
- Static pull-up
- Driven data.

GPIO pins are locked per pin by setting the Lock bit in the appropriate GPIO Pin Configuration register. When the Lock bit is set, the configuration of the associated GPIO pin can be cleared only by a hardware reset.

2.8 LPC INTERFACE

2.8.1 LPC Transactions Supported

The PC8739x LPC interface can respond to the following LPC transactions as part of the standard SuperI/O implementation:

- — I/O read and write cycles
- — 8-bit DMA read and write cycles
- — DMA request cycles.

In addition, the X-Bus bridge uses the following transaction:

- — 8-bit memory read and write (PC87393 and PC87393F only)
- — 8-bit FWH read and write (PC87393F only)

LPC transactions conform with Intel's *LPC Interface Specification*, Revision 1.00.

The LPC-FWH read and write cycles are similar to memory read and write cycles. The specifications of these cycles are listed below. The Address, Data, TAR and SYNC cycles are as specified for LPC memory read and write cycles. The START and ID fields are similar to the equivalent cycle in LPC memory read and write cycles but differ in the data placed on the LAD signals (see details in the cycle description).

FWH Read Cycle (PC87393F only)

1. START: 1101   (0xD)
2. ID field: FWH ID nibble (compared with bits 7-4 of X-Bus Memory Configuration Register, Section 2.19.8)
3. Address: 8 address nibbles (MS nibble first; see usage below)
4. TAR (two cycles)
5. SYNC
6. DATA: 2 data nibbles (LS nibble first; D3-D0, D7-D4)
7. TAR (two cycles)

FWH Write Cycle (PC87393F only)

1. START: 1110 (0xE)
2. ID field: FWH ID nibble (compared with bits 7-4 of X-Bus Memory Configuration Register, Section 2.19.8)
3. Address: 8 address nibbles (MS nibble first; see usage below)
4. DATA: 2 data nibbles (LS nibble first; D3-D0, D7-D4)
5. TAR (two cycles)
6. SYNC
7. TAR (two cycles)

The ID field is compared with bits 7-4 of the X-Bus Memory Configuration register, described in Section 2.19.8. If the two match, the PC8739x continues handling the transaction; if not, the current LPC-FWH transaction is ignored.

2.0 Device Architecture and Configuration (Continued)

LPC-FWH Address Translation: The address field in the LPC-FWH transaction is constructed of eight nibbles. The first seven nibbles correspond to the first LS seven address nibbles (A27-A0), as follows: the first incoming nibble corresponds to addresses A27 - A24, the second to A23 - A20, and so forth until the seventh nibble, which corresponds to A3 - A0. Incoming nibble eight is ignored. The MS bits of the 32-bit addresses are '1111' (A31 - A28).

2.8.2 $\overline{\text{CLKRUN}}$ Functionality

The PC8739x supports the $\overline{\text{CLKRUN}}$ I/O signal, whose use is highly recommended in portable systems. This signal is implemented according to the specification in *PCI Mobile Design Guide*, Revision 1.1, December 18, 1998. The PC8739x supports operation with both a slow and stopped clock in ACPI state S0 (the system is active but is not being accessed). The PC8739x drives the $\overline{\text{CLKRUN}}$ signal low to force the LPC bus clock into full speed operation in the following cases:

- An IRQ is pending internally, waiting to be sent through the serial IRQ.

- A DMA request or abort is pending internally, waiting to be sent through the serial DMA.

Note: When the $\overline{\text{CLKRUN}}$ signal is not in use, the PC8739x assumes valid clock on the CLKIN pin.

2.8.3 $\overline{\text{LPCPD}}$ Functionality

The PC8739x supports the $\overline{\text{LPCPD}}$ input. This signal is used in case the V_{DD} chip supply is not shared by all residents of the LPC bus. The $\overline{\text{LPCPD}}$ signal conforms with Intel's *LPC Interface Specification*, Revision 1.00. Note that if the PC8739x power supply exists while $\overline{\text{LPCPD}}$ is active, it is not mandatory to reset the PC8739x when $\overline{\text{LPCPD}}$ is de-asserted.

2.9 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write

- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.

- W = Write

- RO = Read Only

- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

2.10 SUPERI/O CONFIGURATION REGISTERS

This section describes the SuperI/O configuration and ID registers (those registers with first level indexes in the range of 20h - 2Eh). See Table 15 for a summary and directory of these registers.

Note: Set the configuration registers to enable functions or signals that are relevant to the specific device. The values of fields that select functions, or signals, that are excluded from a specific device are treated as reserved and should not be selected.

Table 15. SuperI/O Configuration Registers

Index	Mnemonic	Register Name	Power Well	Type	Section
20h	SID	SuperI/O ID	V_{DD}	RO	2.10.1
21h	SIOCF1	SuperI/O Configuration 1	V_{DD}	R/W	2.10.2
22h	SIOCF2	SuperI/O Configuration 2	V_{DD}	R/W	2.10.3
23h	SIOCF3	SuperI/O Configuration 3	V_{DD}	R/W	2.10.4
24h	SIOCF4	SuperI/O Configuration 4	V_{DD}	R/W	2.10.5
25h	SIOCF5	SuperI/O Configuration 5	V_{DD}	R/W	2.10.6
26h	SIOCF6	SuperI/O Configuration 6	V_{DD}	R/W	2.10.7
27h	SRID	SuperI/O Revision ID	V_{DD}	RO	2.10.8
28h	SIOCF8	SuperI/O Configuration 8	V_{DD}	R/W	2.10.9
29h	SIOCF9	SuperI/O Configuration 9	V_{DD}	R/W	2.10.10
2Ah	SIOCFA	SuperI/O Configuration A	V_{DD}	R/W	2.10.11
2Bh - 2Fh	Reserved exclusively for National use				

2.0 Device Architecture and Configuration (Continued)

2.10.1 SuperI/O ID Register (SID)

This register contains the identity number of the chip. Members of the PC8739x family are identified by the value EAh.

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Chip ID							
Reset	EAh							

2.10.2 SuperI/O Configuration 1 Register (SIOCF1)

Location: Index 21h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	Pin Function Select Lock	Reserved	Number of DMA Wait States		Number of I/O Wait States		Software Reset	Global Device Enable
Reset	0	0	0	1	0	0	0	1

Bit	Description
7	**Pin Function Select Lock**. This bit determines if the bits that select pin functions (located in the SIOCF1, 2, 3, 4, 5, 8 and A registers) are read only or read/write. When set to 1, this bit can only be cleared by a hardware reset. 0: Bits are R/W 1: Bits are RO.
6	**Reserved**
5-4	**Number of DMA Wait States.** These are R/W bits. **Bits Number** **5 4** 0 0 Reserved 0 1 Two (default) 1 0 Six 1 1 Twelve
3-2	**Number of I/O Wait States.** These are R/W bits. **Bits Number** **3 2** 0 0 Zero (default) 0 1 Two 1 0 Six 1 1 Twelve
1	**Software Reset**. Read always returns 0. This is a R/W bit. 0: Ignored (default) 1: Resets all the logical devices that are affected by hardware reset (with the exception of Lock bits)
0	**Global Device Enable.** This bit controls the function enable of all the PC8739x logical devices, except X-Bus . With the exception of X-Bus, it allows all logical devices to be disabled simultaneously by writing to a single bit. This is a R/W bit. 0: All logical devices in the PC8739x are disabled (except X-Bus) 1: Each logical device is enabled according to its Activate register (Index 30h) (default)

2.0 Device Architecture and Configuration (Continued)

2.10.3 SuperI/O Configuration 2 Register (SIOCF2)

Location: Index 22h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pin 87 Function Select**		**Pins 95-90 Function Select**		**Pins 81-74 Function Select**		**Pins 3-1 and 100-96 Function Select**	
Reset	Strap		Strap		Strap		Strap	

Bit	Description
7-6	**Pin 87 Function Select** **Bits Function** **7 6** 0 0 GPIO26 (default for all XCNF2-0 values, except x01) 0 1 XA6 (default when XCNF2-0 is x01) 1 0 $\overline{\text{PIRQA}}$ 1 1 $\overline{\text{XSTB2}}$
5-4	**Pins 95-90 Function Select** **Bits Function** **5 4** 0 0 GPIO20-24, $\overline{\text{XSTB1}}$ (default when XCNF2-0 is x00) 0 1 XA5-0 (default when XCNF2-0 is x01) 1 0 XA3-0, $\overline{\text{XSTB0}}$, $\overline{\text{XSTB1}}$ (default for all XCNF2-0 values, except x00 and x01) 1 1 Reserved
3-2	**Pins 81-74 Function Select[1]** **Bits Function** **3 2** 0 0 GPIO10-17 (default when XCNF2-0 is x00, 110 or 111) 0 1 XA12-19 (default when XCNF2-0 is x01, 010 or 011) 1 0 JOYABTN1, JOYBBTN1, JOYAY, JOYBY, JOYAX, JOYBX, JOYABTN0, JOYBBTN0 1 1 $\overline{\text{RI2}}$, $\overline{\text{DTR2}}$_BOUT2, $\overline{\text{CTS2}}$, SOUT2, $\overline{\text{RTS2}}$, SIN2, $\overline{\text{DSR2}}$, $\overline{\text{DCD2}}$
1-0	**Pins 3-1 and 100-96 Function Select** **Bits Function** **1 0** 0 0 GPIO00-07 (default when XCNF2-0 is x00) 0 1 XD0-7 (default for all XCNF2-0 values, except x00) 1 0 JOYABTN1, JOYBBTN1, JOYAY, JOYBY, JOYAX, JOYBX, JOYABTN0, JOYBBTN0 1 1 Reserved

1.   In the PC87391, these pins are pulled up after reset by an internal pull-up resistor. Software should set this field to 11 to enable the UART 2 function.

2.0 Device Architecture and Configuration (Continued)

2.10.4 SuperI/O Configuration 3 Register (SIOCF3)

Location: Index 23h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pins 83 and 82 Function Select**		**Pin 84 Function Select**		**Pin 85 Function Select**		**Pin 86 Function Select1**	
Reset	Strap		Strap		Strap		Strap	

Bit	Description
7-6	**Pins 83 and 82 Function Select** **Bits** **Function** **7 6** 0 0 GPIO32-33 (default for all XCNF2-0 values except x01) 0 1 XA10-11 (default when XCNF2-0 is x01) 1 0 MDRX, MDTX 1 1 $\overline{\text{XIORD}}$, $\overline{\text{XIOWR}}$
5-4	**Pin 84 Function Select**[1] **Bits** **Function** **5 4** 0 0 GPIO31 (default for all XCNF2-0 values except x01) 0 1 XA9 (default when XCNF2-0 is x01) 1 0 PIRQD 1 1 MTR1 (signal output is floated when PPM mode is enabled)
3-2	**Pin 85 Function Select** **Bits** **Function** **3 2** 0 0 GPIO30 (default for all XCNF2-0 values except x01) 0 1 XA8 (default when XCNF2-0 is x01) 1 0 PIRQC 1 1 Reserved
1-0	**Pin 86 Function Select** **Bits** **Function** **1 0** 0 0 GPIO27 (default for all XCNF2-0 values except x01 0 1 XA7 (default when XCNF2-0 is x01) 1 0 PIRQB 1 1 Reserved

1. In the PC87391, this pin is pulled up after reset by an internal pull-up resistor. Software should set this field to 11 to enable the FDC function.

2.0 Device Architecture and Configuration (Continued)

2.10.5 SuperI/O Configuration 4 Register (SIOCF4)

Location: Index 24h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pin 5 Function Select**		**Pin 19 Function Select**	**Pin 73 Function Select**		**Pin 72 Function Select**		**Pin 6 Function Select**
Reset	Strap		0	0	1	Strap		0

Bit	Description
7-6	**Pin 5 Function Select**[1] **Bits** **Function** **7 6** 0 0 GPIO34 (default when XCNF2-0 is x00) 0 1 $\overline{XRD}$ (default for all XCNF2-0 values except x00) 1 0 $\overline{WDO}$ 1 1 Reserved
5	**Pin 19 Function Select**[1] 0: GPIO35 (default) 1: $\overline{SMI}$
4-3	**Pin 73 Function Select**[1] **Bits** **Function** **4 3** 0 0 $\overline{XIOWR}$ 0 1 $\overline{XCS1}$ (default) 1 0 $\overline{MTR1}$ (signal output is inactive, 1, when PPM mode is enabled) 1 1 DRATE0
2-1	**Pin 72 Function Select**[1] **Bits** **Function** **2 1** 0 0 GPIO25 (default when XCNF2-0 is x00) 0 1 $\overline{XCS0}$ (default for all XCNF2-0 values except x00, 010 and 110) 1 0 XRDY (default when XCNF2-0 is 010 or 110) 1 1 $\overline{DR1}$ (signal output is inactive, 1, when PPM mode is enabled)
0	**Pin 6 Function Select**[1] 0: GPIO36 (default) 1: $\overline{CLKRUN}$

1. In the PC87391, this pin is pulled up after reset by an internal pull-up resistor. Software should set this field as appropriate to enable the required Legacy function.

2.0 Device Architecture and Configuration (Continued)

2.10.6 SuperI/O Configuration 5 Register (SIOCF5)

Location: Index 25h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	PNF Status	Pin 35 Function Select		$\overline{\text{SMI}}$ to IRQ2 Enable	Pin 34 Function Select	PPM Power Save Enable	Pin 71 Function Select	
Reset	1	0	0	0	0	0	0	0

Bit	Description
7	**PNF Status.** This bit describes the status of the PNF signal, which determines if Parallel Port of external FDD signals are selected by PPM mode. This is a RO bit. 0: Floppy Disk 1: Parallel Port (default)
6-5	**Pin 35 Function Select.** These are R/W bits. **Bits** **Function** **6 5** 0 0 PPM disabled (default) 0 1 PNF signal selected as active low (high selects printer, low selects floppy) 1 0 PNF signal selected as active high (low selects printer, high selects floppy) 1 1 XRDY signal selected
4	**$\overline{\text{SMI}}$ to IRQ2 Enable.** This is a R/W bit. 0: Disabled (default) 1: Enabled
3	**Pin 34 Function Select.** This is a R/W bit. 0: DRATE0 (default) 1: IRSL2
2	**PPM Power Save Enable** 0: Disabled (default). 1: When PPM is active and PNF is 0 (bit 7 of this register), the FDC output pins and the Parallel Port output pins are masked when the corresponding drive is not used.
1-0	**Pin 71 Function Select.**[1] This is a R/W bit. **Bits** **Function** **1 0** 0 0 GPIO37 (default) 0 1 $\overline{\text{DR1}}$ 1 0 IRSL2 1 1 $\overline{\text{XIORD}}$

1. In the PC87391, this pin is pulled up after reset by an internal pull-up resistor. Software should set this field as appropriate to enable the required Legacy function.

2.0 Device Architecture and Configuration (Continued)

2.10.7   SuperI/O Configuration 6 Register (SIOCF6)

Write access to this register can be inhibited by setting bit 7. Activation of each logical device (bits 0-4) is also affected by bit 0 of the logical device Activate register, index 30h and bit 0 of the SIOCF1 register.

Location: Index 26h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	SIOCF6 Software Lock	General-Purpose Scratch		Reserved	Serial Port 1 Disable	Serial Port 2 Disable	Parallel Port Disable	FDC Disable
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SIOCF6 Software Lock.** When this bit is set to 1 by software, it can be cleared only by hardware reset. 0: Write access to bits 0-6 of this register enabled (default) 1: Bits 6-0 of this register are RO
6-5	**General-Purpose Scratch**
4	**Reserved**
3	**Serial Port 1 Disable** 0: Enabled (default) 1: Disabled
2	**Serial Port 2 Disable** 0: Enabled (default) 1: Disabled
1	**Parallel Port Disable** 0: Enabled (default) 1: Disabled
0	**FDC Disable** 0: Enabled (default) 1: Disabled

2.10.8   SuperI/O Revision ID Register (SRID)

This register contains the ID number of the specific family member (Chip ID) and the chip revision number (Chip Rev). The Chip Rev field identity number the chip revision.

Location: Index 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Chip ID			Chip Rev				
Reset	0	0	0	X	X	X	X	X

Bit	Description
7-5	**Chip ID.**
4-0	**Chip Rev.** These bits identify the device revision.

2.0 Device Architecture and Configuration (Continued)

2.10.9 SuperI/O Configuration 8 Register (SIOCF8)

Location: Index 28h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved						GPIO to $\overline{\text{SMI}}$ Enable	$\overline{\text{WDO}}$ to $\overline{\text{SMI}}$ Enable
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved**
1	**GPIO to $\overline{\text{SMI}}$ Enable**[1] 0: Disabled (default) 1: Enabled
0	**$\overline{\text{WDO}}$ to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled

1. PC87392, PC87393 and PC87393F only.

2.0 Device Architecture and Configuration (Continued)

2.10.10 SuperI/O Configuration 9 Register (SIOCF9)

Location: Index 29h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	Reserved			Module Enable Status	Valid Multiplier Clock Status	Clock Enable	SuperI/O Chip Clock Source	
Reset	0	0		0	0	0	1	0

Bit	Description
7-5	**Reserved**
4	**Module Enable Status.** This bit defines the status of all the PC8739x modules with exception of the X-Bus. This bit is read only. 0: All modules disabled 1: At least one module enabled
3	**Valid Multiplier Clock Status.** This bit is read only. 0: On-chip clock frozen 1: On-chip clock stable and toggling
2	**Clock Enable.** This bit enables the 48 and 24 MHz clock to the SuperI/O modules. When the SuperI/O chip clock source is set to 48 MHz, this bit enables the path from the input CLKIN pin. When the clock source is set to 32.768 KHz or 14.31818 MHz, this bit enables the clock multiplier.This is a read/write bit that is reset by hardware reset only. 0: Clock disabled (default) 1: Clock enabled
1-0	**SuperI/O Chip Clock Source.** These bits define the clock source for the SuperI/O chip that is fed via the CLKIN pin. On power-up (only), these bits are read or write and assume their default value. Once they are written, they become read only bits. **Bits Function** **1 0** 0 0 Clock source is 48 MHz 0 1 Clock source is the on-chip clock multiplier fed by 32.768 KHz 1 0 Clock source is the on-chip clock multiplier fed by 14.31818 MHz (default) 1 1 Reserved

2.0 Device Architecture and Configuration (Continued)

2.10.11 SuperI/O Configuration A Register (SIOCFA)

Location: Index 2Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Pin 53 PPM FDC Function Select	Pin 66 Function Select		Reserved				
Reset	0	0	1	1	0	1	1	1

Bit	Description
7	**Pin 53 PPM FDC Function Select.** This bit defines which of the following two FDC signals will appear on the PPM. 0: DENSEL (default) 1: DRATE1
6-5	**Pin 66 Function Select** **Bits Function** **6 5** 0 0 Reserved 0 1 PWUREQ (default) 1 0 Reserved 1 1 IRSL3
4-0	**Reserved**

2.0 Device Architecture and Configuration (Continued)

2.11 FLOPPY DISK CONTROLLER (FDC) CONFIGURATION

2.11.1 General Description

The generic FDC is a standard FDC with a digital data separator, and is DP8473 and N82077 software compatible. The PC8739x FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including:

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode

- A logic 1 is returned for all floating (TRI-STATE) FDC register bits upon LPC I/O read cycles.

Exceptions to standard FDC support include:

- Automatic media sense is supported by MSEN1-0 pins only on FDC signals routed to the PPM functional block (on the Parallel Port)

- DRATE1 is supported only on FDC signals routed to the PPM functional block (on the Parallel Port).

Table 16 lists the FDC functional block registers.

Table 16. FDC Registers

Offset[1]	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W
06h		N/A	X
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

1. From the 8-byte aligned FDC base address.

2.11.2 Logical Device 0 (FDC) Configuration

Table 17 lists the configuration registers which affect the FDC. Only the last two registers (F0h and F1h) are described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 17. FDC Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 0 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB register. Bits 2 and 0 (for A2 and A0) are read only, 00b.	R/W	F2h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	03h
74h	DMA Channel Select	R/W	02h
75h	Report no second DMA assignment	RO	04h
F0h	FDC Configuration register	R/W	24h
F1h	Drive ID register	R/W	00h

2.0 Device Architecture and Configuration (Continued)

2.11.3 FDC Configuration Register

This register is reset by hardware to 24h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Four-Drive Encode Enable	TDR Register Mode	DENSEL Polarity Control	FDC 2Mbps Enable	Write Protect	PC-AT or PS/2 Drive Mode Select	Reserved	TRI-STATE Control
Reset	0	0	1	0	0	1	0	0

Bit	Description
7	**Four-Drive Encode Enable** 0: Two floppy drives are directly controlled by $\overline{DR1\text{-}0}$, $\overline{MTR1\text{-}0}$. 1: Four floppy drives are controlled with the aid of an external decoder.
6	**TDR Register Mode** 0: PC-AT compatible drive mode; i.e., bits 7-2 of the TDR are 111111b (default) 1: Enhanced drive mode
5	**DENSEL Polarity Control** 0: Active low for 500 Kbps, or 1 or 2 Mbps data rates 1: Active high for 500 Kbps, or 1 or 2 Mbps data rates (default)
4	**FDC 2Mbps Enable.** This bit is set only when a 2Mbps drive is used. 0: 2Mbps disabled and the FDC clock is 24 MHz (default) 1: 2Mbps enabled and the FDC clock is 48 MHz
3	**Write Protect.** This bit allows forcing of write protect functionality by software. When set, writes to the floppy disk drive are disabled. This effect is identical to $\overline{WP}$ when it is active. 0: Write protected according to $\overline{WP}$ signal (default) 1: Write protected regardless of value of $\overline{WP}$ signal
2	**PC-AT or PS/2 Drive Mode Select** 0: PS/2 drive mode 1: PC-AT drive mode (default)
1	**Reserved**
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

2.11.4 Drive ID Register

This read/write register is reset by hardware to 00h. This register controls bits 5 and 4 of the TDR register in the Enhanced mode.

Location: Index F1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Drive 1 ID		Drive 0 ID	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-2	**Drive 1 ID.** When drive 1 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.
1-0	**Drive 0 ID.** When drive 0 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.

Usage Hints: Some BIOS implementations support automatic media sense FDDs, in which case bit 5 of the TDR register in the Enhanced mode is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID register should be set to 1 respectively (to indicate non-valid media sense) when the corresponding drive is selected and the Drive ID bit is reflected on bit 5 of the TDR register in the Enhanced mode.

2.0 Device Architecture and Configuration (Continued)

2.12 PARALLEL PORT CONFIGURATION

2.12.1 General Description

The PC8739x Parallel Port supports all IEEE1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of this registers (at offsets 403h, 404h and 405h) are used only in the Extended ECP mode.

- A group of four registers, used only in the Extended ECP mode, accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. See Tables 18 and 19 for a listing of all registers, their offset addresses, and the associated modes.

Table 18. Parallel Port Registers at First Level Offset

Offset	Mnemonic	Mode(s)	Type	Register Name
00h	DATAR	0,1	R/W	Data
	AFIFO	3	W	ECP FIFO (Address)
	DTR	4	R/W	Data (for EPP)
01h	DSR	0,1,2,3	RO	Status
	STR	4	RO	Status (for EPP)
02h	DCR	0,1,2,3	R/W	Control
	CTR	4	R/W	Control (for EPP)
03h	ADDR	4	R/W	EPP Address
04h	DATA0	4	R/W	EPP Data Port 0
05h	DATA1	4	R/W	EPP Data Port 1
06h	DATA2	4	R/W	EPP Data Port 2
07h	DATA3	4	R/W	EPP Data Port 3
400h	CFIFO	2	W	PP Data FIFO
	DFIFO	3	R/W	ECP Data FIFO
	TFIFO	6	R/W	Test FIFO
	CNFGA	7	RO	Configuration A
401h	CNFGB	7	RO	Configuration B
402h	ECR	0,1,2,3	R/W	Extended Control
403h	EIR[1]	0,1,2,3	R/W	Extended Index
404h	EDR[1]	0,1,2,3	R/W	Extended Data
405h	EAR[1]	0,1,2,3	R/W	Extended Auxiliary Status

1. These registers are extended to the standard IEEE1284 registers. They are accessible only when enabled by bit 4 of the Parallel Port Configuration register (see Section 2.12.3).

2.0 Device Architecture and Configuration (Continued)

Table 19. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Type	Register Name
00h	Control0	R/W	Extended Control 0
02h	Control2	R/W	Extended Control 1
04h	Control4	R/W	Extended Control 4
05h	PP Confg0	R/W	Configuration 0

2.12.2 Logical Device 1 (PP) Configuration

Table 20 lists the configuration registers which affect the Parallel Port. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 20. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b. Bit 2 (for A10) should be 0b.	R/W	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read only, 00b. For ECP Mode 4 (EPP) or when using the Extended registers, bit 2 (A2) should also be 0b.	R/W	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	07h
71h	Interrupt Type Bits 7-2 are read only. Bit 1 is a read/write bit. Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended Mode and cleared (edge interrupt) in all other modes.	R/W	02h
74h	DMA Channel Select	R/W	04h
75h	Report no second DMA assignment	RO	04h
F0h	Parallel Port Configuration register	R/W	F2h

2.0 Device Architecture and Configuration (Continued)

2.12.3 Parallel Port Configuration Register

This register is reset by hardware to F2h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Parallel Port Mode Select			Extended Register Access	Reserved	PP Reflect-ed Input Signals	Power Mode Control	TRI-STATE Control
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select** 000: SPP Compatible mode. PD7-0 are always output signals. 001: SPP Extended mode. PD7-0 direction is controlled by software. 010: EPP 1.7 mode 011: EPP 1.9 mode 100: ECP mode (IEEE1284 register set), with no support for EPP mode. 101: Reserved 110: Reserved 111: ECP mode (IEEE1284 register set), with EPP mode selectable as mode 4. Selection of EPP 1.7 or 1.9 in ECP mode 4 is controlled by bit 4 of the Control2 configuration register of the parallel port at offset 02h.
4	**Extended Register Access** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored). 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports run-time configuration within the Parallel Port address space.
3	**Reserved**
2	**PP Reflected Input Signals.** When the parallel port input signal is disconnected by the PPM, the input signals reflected by the STR register assume one of the following values: 0: $\overline{BUSY}$ = 1, PE = 0, SLCT = 0, $\overline{ACK}$ = 1 (default) 1: $\overline{BUSY}$ = 1, PE = 1, SLCT = 1, $\overline{ACK}$ = 1.
1	**Power Mode Control.** When the logical device is active: 0: Parallel port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

2.13 SERIAL PORT 2 CONFIGURATION

2.13.1 General Description

Serial Port 2 includes IR functionality as described in the Serial Port 2 with IR chapter.

2.13.2 Logical Device 2 (SP2) Configuration

Table 21 lists the configuration registers which affect the Serial Port 2. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 21. Serial Port 2 Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 2 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	DMA Channel Select 0 (RX_DMA)	R/W	04h
75h	DMA Channel Select 1 (TX_DMA)	R/W	04h
F0h	Serial Port 2 Configuration register	R/W	02h

2.0 Device Architecture and Configuration (Continued)

2.13.3 Serial Port 2 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Bank Select Enable	Reserved				Busy Indicator	Power Mode Control	TRI-STATE Control
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default). 1: Enables bank switching for Serial Port 2.
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 2 clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained (unlike Active bit in index 30 that also prevents access to Serial Port 2 registers). 1: Normal power mode Serial Port 2 clock enabled. Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control**. When enabled and the device is inactive, the logical device output pins are in TRI-STATE. One exception is the IRTX pin, which is driven to 0 when Serial Port 2 is inactive and is not affected by this bit. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

2.14 SERIAL PORT 1 CONFIGURATION

2.14.1 Logical Device 3 (SP1) Configuration

Table 22 lists the configuration registers which affect the Serial Port 2. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 22. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 3 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	Report no DMA Assignment	RO	04h
75h	Report no DMA Assignment	RO	04h
F0h	Serial Port 1 Configuration register	R/W	02h

2.14.2 Serial Port 1 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Bank Select Enable	Reserved				Busy Indicator	Power Mode Control	TRI-STATE Control
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 1. 0: Disabled (default). 1: Enabled
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 1 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 1 clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained (unlike Active bit in Index 30 that also prevents access to Serial Port 1 registers). 1: Normal power mode Serial Port 1 clock enabled. Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control**. When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

2.15 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

This section applies to the PC87392, PC87393 and PC87393F only.

2.15.1 General Description

The GPIO functional block includes 32 pins, arranged in four 8-bit ports (ports 0, 1, 2 and 3). All pins in ports 0 and 1 are I/O, and have full event detection capability, enabling them to trigger the assertion of IRQ and $\overline{SMI}$ signals. Pins in ports 2 and 3 are I/O, but none of them has event detection capability. The twelve runtime registers associated with the four ports are arranged in the GPIO address space as shown in Table 23. The GPIO base address is 16-byte aligned. Address bits 3-0 are used to indicate the register offset.

Table 23. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Type
00h	GPDO0	GPIO Data Out 0	0	R/W
01h	GPDI0	GPIO Data In 0		RO
02h	GPEVEN0	GPIO Event Enable 0		R/W
03h	GPEVST0	GPIO Event Status 0		R/W1C
04h	GPDO1	GPIO Data Out 1	1	R/W
05h	GPDI1	GPIO Data In 1		RO
06h	GPEVEN1	GPIO Event Enable 1		R/W
07h	GPEVST1	GPIO Event Status 1		R/W1C
08h	GPDO2	Data Out 2	2	R/W
09h	GPDI2	Data In 2		RO
0Ah	GPDO3	Data Out 3	3	R/W
0Bh	GPDI3	Data In 3		RO

2.15.2 Implementation

The standard GPIO port with event detection capability (such as ports 0 and 1) has four runtime registers. Each pin is associated with a GPIO Pin Configuration register that includes seven configuration bits. Ports 2 and 3 are non-standard ports that do not support event detection, and therefore differ from the generic model as follows:

- They each have two runtime registers for basic functionality: GPDO2/3 and GPDI2/3. Event detection registers GPEVEN2/3 and GPEVST2/3 are not available.

- Only bits 3-0 are implemented in the GPIO Pin Configuration registers of ports 2 and 3. Bits 6-4, associated with the event detection functionality, are reserved.

2.0 Device Architecture and Configuration (Continued)

2.15.3 Logical Device 7 (GPIO) Configuration

Table 24 lists the configuration registers which affect the GPIO. Only the last three registers (F0h - F2h) are described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 24. GPIO Configuration Register

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 7 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 3-0 (for A3-0) are read only, 0000b.	R/W	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	GPIO Pin Select register	R/W	00h
F1h	GPIO Pin Configuration register	R/W	44h
F2h	GPIO Pin Event Routing register	R/W	01h

Figure 6 shows the organization of these registers.
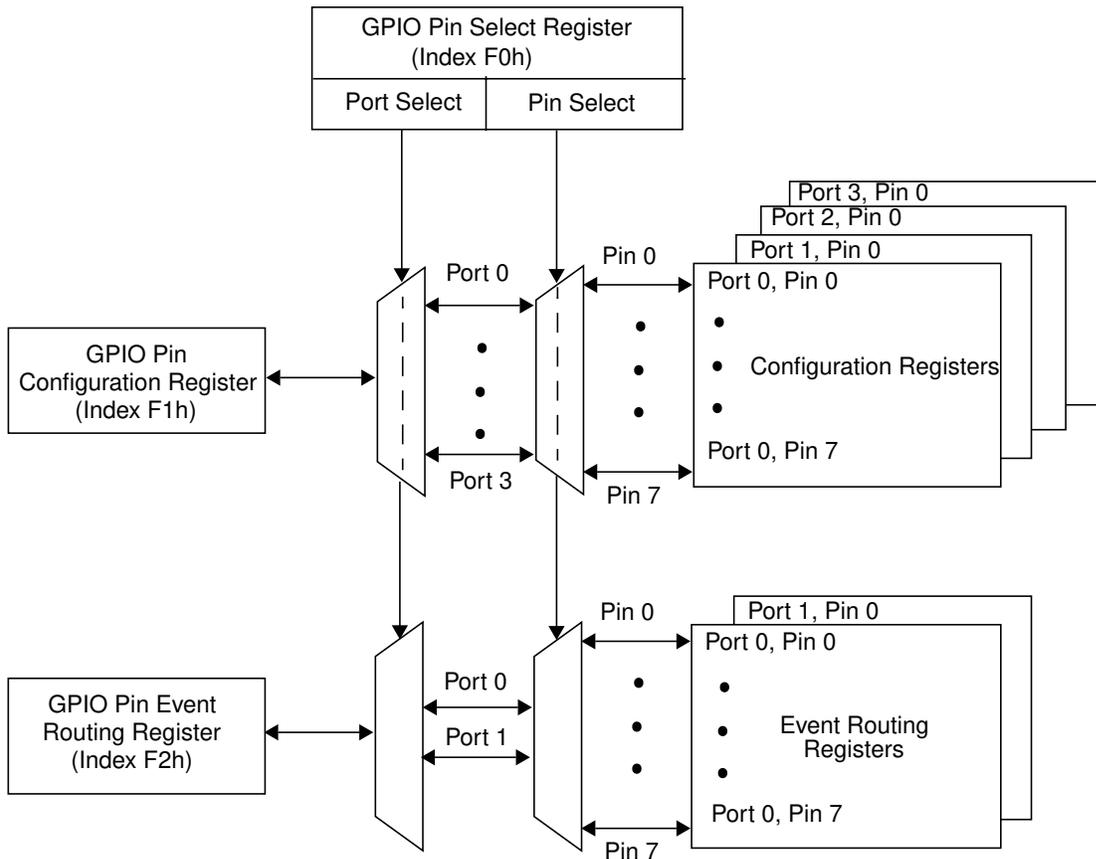
Figure 6. Organization of GPIO Pin Registers

2.0 Device Architecture and Configuration (Continued)

2.15.4 GPIO Pin Select Register

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO Pin Configuration register). It is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved		Port Select		Reserved	Pin Select		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved**
5-4	**Port Select.** These bits select the GPIO port to be configured: 00: Port 0 (default) 01, 10, 11: Binary value of port numbers 1-3 respectively. All other values are reserved.
3	**Reserved**
2-0	**Pin Select.** These bits select the GPIO pin to be configured in the selected port: 000, 001,... 111: Binary value of the pin number, 0, 1,... 7 respectively (default=0)

2.0 Device Architecture and Configuration (Continued)

2.15.5 GPIO Pin Configuration Register

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. All the GPIO Pin registers that are accessed via this register have a common bit structure, as shown below. This register is reset by hardware to 44h, except for ports 2 and 3, that are reset to 04h, and GPIO36 which resets to 00h.

Location: Index F1h
Type: R/W

Ports: 0 and 1 (with event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Event Debounce Enable	Event Polarity	Event Type	Lock	Pull-Up Control	Output Type	Output Enable
Reset	0	1	0	0	0	1	0	0

Ports 2 and 3 (without event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Lock	Pull-Up Control	Output Type	Output Enable
Reset	0	0	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**Event Debounce Enable.** (Ports 0 and 1 with event detection capability). Enables transferring the signal only after a predetermined debouncing period of time. 0: Disabled 1: Enabled (default) **Reserved.** (Ports 2 and 3). Always 0.
5	**Event Polarity.** (Ports 0 and 1 with event detection capability). This bit defines the polarity of the signal that issues an interrupt from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input **Reserved.** (Ports 2 and 3). Always 0.
4	**Event Type.** (Ports 0 and 1 with event detection capability). This bit defines the type of the signal that issues an interrupt from the corresponding GPIO pin (edge or level). 0: Edge input (default) 1: Level input **Reserved.** (Ports 2 and 3). Always 0.
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1 (bit 7 of SuperI/O Configuration 1 register, SIOCF1). 0: No effect (default) 1: Direction, output type, pull-up and output value locked

2.0 Device Architecture and Configuration (Continued)

Bit	Description
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals. 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on the input path. 0: TRI-STATE (default) 1: Output enabled

2.15.6 GPIO Event Routing Register

This register enables the routing of the GPIO event to IRQ and/or $\overline{\text{SMI}}$ signals. It is implemented only for ports 0,1 which have event detection capability. This register is reset by hardware to 00h.

Location: Index F2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved						Enable $\overline{\text{SMI}}$ Routing	Enable IRQ Routing
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-2	**Reserved**
1	**Enable $\overline{\text{SMI}}$ Routing** 0: Disabled (default) 1: Enabled
0	**Enable IRQ Routing** 0: Disabled 1: Enabled (default)

2.0 Device Architecture and Configuration (Continued)

2.16 WATCHDOG TIMER (WDT) CONFIGURATION

2.16.1 Logical Device 10 (WDT) Configuration

Table 25 lists the configuration registers which affect the WATCHDOG Timer. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 25. WDT Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 1 and 0 (for A1 and A0) are read only, 00b.	R/W	00h
70h	Interrupt Number (for routing the $\overline{WDO}$ signal) and Wake-Up on IRQ Enable register.	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	WATCHDOG Timer Configuration register	R/W	02h

2.16.2 WATCHDOG Timer Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Output Type	Internal Pull-Up Enable	Power Mode Control	TRI-STATE Control
Reset	0	0	0	0	0	0	1	0

Bit	Description
7-4	**Reserved**
3	**Output Type.** This bit controls the buffer type (open-drain or push-pull) of the $\overline{WDO}$ pin. 0: Open-drain (default) 1: Push-pull
2	**Internal Pull-Up Enable.** This bit controls the internal pull-up resistor on the $\overline{WDO}$ pin. 0: Disabled (default) 1: Enabled
1	**Power Mode Control** 0: Low power mode: WATCHDOG Timer clock disabled. $\overline{WDO}$ output signal is set to 1. Registers are accessible and maintained (unlike Active bit in Index 30h that also prevents access to WATCHDOG Timer registers). 1: Normal power mode: WATCHDOG Timer clock enabled. WATCHDOG Timer is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

2.17 GAME PORT (GMP) CONFIGURATION

This section applies to the PC87393 and PC87393F only.

2.17.1 Logical Device 11 (GMP) Configuration

Table 26 lists the configuration registers which affect the Game Port. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 26. GMP Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	00h
60h	Base Address MSB register	R/W	02h
61h	Base Address LSB register.	R/W	01h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	Game Port Configuration register	R/W	00h

2.17.2 Game Port Configuration Register

This register is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name			Reserved		GMP Enhanced Mode Enable	Internal Pull-Up Enable	Reserved	TRI-STATE Control
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**GMP Enhanced Mode Enable.** See Usage Hints below. 0: Disabled (default) 1: Enabled
2	**Internal Pull-Up Enable.** When the GMP functions are selected, this bit controls the internal pull-up resistor on pins 96 (GPIO07/JOYABTN0), 3 (GPIO00/JOYABTN1), 97 (GPIO06/JOYBBTN0) and 2 (GPIO01/JOYBBTN1) or pins 74 (GPIO17/JOYABTN0), 81 (GPIO10/JOYABTN1), 75 (GPIO16/JOYBBTN0), 80 (GPIO11/JOYBBTN1). 0: Disabled (default) 1: Enabled
1	**Reserved**
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.0 Device Architecture and Configuration (Continued)

Usage Hints: To operate GMP enhanced features, make sure to locate its base address within the LPC Wide Generic address range.

When bit 3 of the GMP configuration register is set to 0 (default), the GMP operates in Legacy mode. In this mode, only the Game Port Legacy Status (GMPLST) register of the GMP is accessible, and is mapped to the base address of the GMP. For example, if GMP configuration bit 3 is set to 0 and the base address is programmed to 203h, the GMPLST register is mapped to address 203h, and is the only user-accessible GMP register.

The GMP is also forced to operate in Legacy mode if the programmed base address is not 16-byte aligned; i.e. bits 3-0 of the base address are not all 0's.

When bit 3 of the GMP register is set to 1 and the programmed GMP base address is 16-byte aligned; i.e., bits 3-0 of the base address are all 0's, the GMP can be operated in Enhanced mode. In this condtion, all the registers listed in the GMP chapter are accessible.

2.0 Device Architecture and Configuration (Continued)

2.18 MIDI PORT (MIDI) CONFIGURATION

This section applies to the PC87393 and PC87393F only.

2.18.1 Logical Device 12 (MIDI) Configuration

Table 26 lists the configuration registers which affect the MIDI Port. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 27. MIDI Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	00h
60h	Base Address MSB register	R/W	03h
61h	Base Address LSB register. Bit 0 (for A0) is read only, 0b.	Varies per bit	30h
70h	Interrupt Number and wake-up on IRQ enable.	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	MIDI Port Configuration register	R/W	00h

2.18.2 MIDI Port Configuration Register

This register is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				MIDI Enhanced Mode Enable	Internal Pull-Up Enable	Reserved	TRI-STATE Control
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**MIDI Enhanced Mode Enable.** See Usage Hints below. 0: Disabled (default) 1: Enabled
2	**Internal Pull-Up Enable.** This bit controls the internal pull-up resistor on pin 83 (GPIO32/MDRX). 0: Disabled (default) 1: Enabled
1	**Reserved**
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

Usage Hints: To operate MIDI enhanced features, make sure to locate its base address within the LPC Wide Generic address range.

When bit 3 of the MIDI configuration register is set to 0 (default), the MIDI operates in Legacy mode. In this mode, only the MIDI IN, MIDI OUT, MIDI Status and MIDI Command registers of the MIDI are user-accessible.

When bit 3 of the MIDI configuration register is set to 1, the MIDI is operated in Enhanced mode. In this condition, all the registers listed in the MIDI chapter are accessible.

2.0 Device Architecture and Configuration (Continued)

2.19 X-BUS CONFIGURATION

This section applies to the PC87393 and PC87393F only. FWH-related descriptions apply to the PC87393F only.

2.19.1 Logical Device 15 (X-Bus) Configuration

Table 28 lists the configuration registers that affect the X-Bus functional block. The X-Bus base address registers point to the X-Bus registers described in the X-Bus chapter. The memory space to which the X-Bus responds is defined by the configuration registers in the following sections. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 28. X-Bus Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 3-0 (for A3-A0) are read only, 0000b.	Varies per bit	00h
70h	Interrupt Number and wake-up on IRQ enable.	RO	00h
71h	Interrupt Type.	RO	00h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	X-Bus I/O Configuration register	R/W	00h
F1h	X-Bus I/O Base Address High Byte register	R/W	00h
F2h	X-Bus I/O Base Address Low Byte register	R/W	00h
F3h	X-Bus I/O Size Configuration register	R/W	00h
F4h	X-Bus Memory Configuration register	R/W	00h
F5h	X-Bus Memory Base Address High Byte register	R/W	00h
F6h	X-Bus Memory Base Address Low Byte register	R/W	00h
F7h	X-Bus Memory Size Configuration register	R/W	00h
F8h	X-Bus PIRQA and PIRQB Mapping register	R/W	00h
F9h	X-Bus PIRQC and PIRQD Mapping register	R/W	00h

2.19.2 X-Bus I/O Range Programming

LPC I/O transactions can be forwarded to the PC8739x X-Bus. The X-Bus I/O configuration registers define the map of addresses to be forwarded. The PC8739x provides five, individually enabled I/O zones. Each zone generates an internal select signal that is sent to the X-Bus functional block. The mapping of the internal select signals to the PC8739x $\overline{XCS0\text{-}1}$ signals is controlled by the X-Bus. See Section 7.3 for further details.

The supported I/O zones are:

- Keyboard controller (KBC) - legacy 60h, 64h addresses and an alternate location

- Power Management & Embedded Controller (PM) - legacy 62h, 66h and an alternate location

- Real Time Clock (RTC) - legacy 70h, 71h and two alternate locations

- User-Defined I/O Zone (UDIZ) - specified using the zone size (2^n where n is 1 through 8) and start address (must be aligned with the block size)

- Debug Port Address Enable (TST) - This zone is for debug use only.

These decoded I/O zones are determined by the following four registers: X-Bus I/O Configuration, X-Bus I/O Zone Base Address High and Low Byte, and X-Bus I/O Size Configuration. When a zone (e.g. KBC, PM or RTC) is enabled but is not associated with any select signal in the X-Bus interface, a value of 00h is read and data written is ignored.

2.0 Device Architecture and Configuration (Continued)

2.19.3 X-Bus Memory Range Programming

LPC memory transactions and/or LPC-FWH transactions can be forwarded to the PC8739x X-Bus. The X-Bus Memory Configuration register defines the address space to which the PC8739x responds. The XCNF2-0 strap inputs impact the default setting of the X-Bus Memory Configuration register enable boot process from memories connected on the X-Bus. Two memory areas may be individually enabled: a user-defined zone, and BIOS memory (BIOS-LPC and/or BIOS-FWH spaces).

To enable BIOS support, set the XCNF2-0 strap inputs to select any of the BIOS modes (see Section 1.5.11 for details). The PC8739x responds to LPC memory read and write transactions to/from the BIOS address spaces, shown in Table 29, as long as BIOS LPC Enable (bit 0) of the X-Bus Memory Configuration register is set.

Table 29. BIOS-LPC Memory Space Definition

Memory Address Range	Description
000E 0000h - 000E FFFFh	Extended BIOS Range (Legacy) Only when Extended BIOS Enable bit in X-Bus Memory Range Configuration register is set
000F 0000h - 000F FFFFh	BIOS Range (Legacy)
FFC0 0000h - FFFFF FFFh	386 mode BIOS Range. This is the upper 4 Mbyte of the memory space

The PC8739x responds to LPC-FWH read and write transactions from/to the high memory address range ('386' mode BIOS range), shown in Table 29, as long as BIOS FWH Enable (bit 3) of the X-Bus Memory Configuration register is set.

Table 30. BIOS-FWH Memory Space Definition

Memory Address Range	Description
FFC0 0000h - FFFFF FFFh	386 mode BIOS Range. This is the upper 4 Mbyte of the memory space

Upon reset in BIOS enabled mode (XCNF≠000), the BIOS LPC Enable bit is set and the BIOS FWH Enable bit is set. The PC8739x automatically detects the type of host boot protocol in use via the first completed BIOS read operation after reset. If the first read is an LPC memory read, the BIOS FWH Enable bit is cleared. If the first read is an LPC-FWH read, the BIOS LPC Enable bit is cleared. Any other LPC or LPC-FWH transactions are ignored. The bits are cleared only by the first read operation, allowing software to enable response to these address ranges by setting the bit. Figure 7 illustrates this behavior.
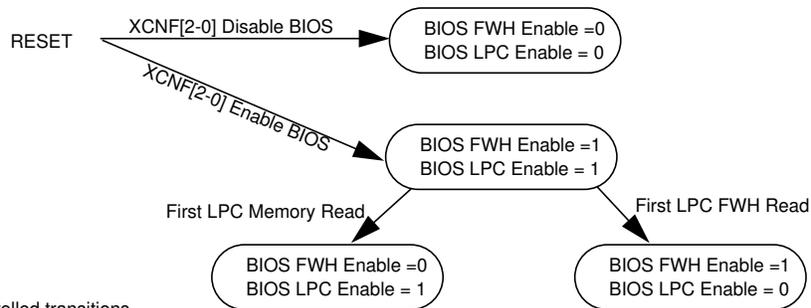
Figure 7. BIOS Mapping Enable Scheme

The User-Defined Memory Zone (UDMZ) is specified via a 32-bit start address. This address is formed by 8 bits of the X-Bus Memory Base Address Low Byte register, 8 bits of the X-Bus Memory Base Address HIgh Byte register and 16 least significant bits of 0. The size of the window is specified through the X-Bus Memory Size Configuration register. The zone base address must be aligned to the block size.

The address used for the X-Bus transaction is the 28 least significant bits of the address bus. In read transactions, the data read from the X-Bus is passed to the LPC bus. In write transactions, the data from the LPC is passed to the X-Bus.

2.19.4 X-Bus I/O Configuration Register

This register is reset by hardware to 00h.

Location: Index F0h

2.0 Device Architecture and Configuration (Continued)

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**User-Defined I/O Zone Enable**	**TST Address Enable**	**RTC Address Enable**		**PM Address Enable**		**KBC Address Enable**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**User-Defined I/O Zone Enable.** This bit enables the mapping of the User-Defined I/O zone to the X-Bus space. The zone base address and size are defined by the X-Bus I/O Base Address High Byte register, X-Bus I/O Base Address Low Byte register and the X-Bus I/O Size Configuration register. 0: Disabled (default) 1: Enabled
6	**TST (Debug Port) Address Enable**. When set, enables the mapping of I/O address 80h to the X-Bus space. 0: Disabled (default) 1: Enabled
5-4	**RTC Address Enable.** This bit controls the mapping of the RTC I/O address to the X-Bus space. **Bits Mapping (hex)** **5 4** 0 0 Disabled (default) 0 1 70, 71 1 0 370, 371 1 1 70, 71, 72, 73
3-2	**PM Address Enable.** This bit controls the mapping of the PM I/O address to the X-Bus space. **Bits Mapping (hex)** **3 2** 0 0 Disabled (default) 0 1 62, 66 1 0 362, 366 1 1 Reserved
1-0	**KBC Address Enable.** This bit controls the mapping of the KBC I/O address to the X-Bus space. **Bits Mapping (hex)** **1 0** 0 0 Disabled (default) 0 1 60, 64 1 0 360, 364 1 1 Reserved

2.0 Device Architecture and Configuration (Continued)

2.19.5 X-Bus I/O Base Address High Byte Register

This register describes the high byte for the user-defined I/O zone mapped to the X-Bus. This register is reset by hardware to 00h.

Location: Index F1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	User-Defined Zone Address High							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**User-Defined Zone Address High.** Defines the higher 8 bits of the user-defined I/O block base address. The base address should be aligned on the selected block size.

2.19.6 X-Bus I/O Base Address Low Byte Register

This register describes the low byte for the user-defined I/O zone mapped to the X-Bus. This register is reset by hardware to 00h.

Location: Index F2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	User-Defined Zone Address Low							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**User-Defined Zone Address Low.** Defines the lower 8 bits of the user-defined I/O block base address. The base address should be aligned on the selected block size.

2.19.7 X-Bus I/O Size Configuration Register

This register defines the size of the user-defined I/O zone mapped to the X-Bus. This register is reset by hardware to 00h.

Location: Index F3h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				User-Defined I/O Zone Size			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-0	**User-Defined I/O Zone Size.** Defines the size in bytes of the zone window. The size is defined as a power of two using the equation: NumOfBytes = 2^n(User-Defined I/O Zone size). The zone must always be aligned to the window size (i.e., for a 128 byte window, the 7 LSBs of the address are zero). **Bits Size (Bytes)** **3 2 1 0** 0 0 0 0 1 (default) **. . .** 1 0 0 0 256 Other Reserved

2.0 Device Architecture and Configuration (Continued)

2.19.8 X-Bus Memory Configuration Register

This register is reset by hardware to 00h.

Location: Index F4h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	BIOS FWH ID				BIOS FWH Enable	User-Defined Memory Space Enable	BIOS Extended Space Enable	BIOS LPC Enable
Reset	0	0	0	0	Depends on strap setting.			

Bit	Description
7-4	**BIOS FWH ID.** The identification nibble that is part of a FWH transaction (see Section 2.8.1 for details), which identifies the device addressed.
3	**BIOS FWH Enable.** When set, enables PC8739x response to LPC-FWH transactions to the BIOS-FWH space, if the BIOS FWH ID matches the ID of the transaction.. The reset value of this register is defined by the XCNF2-0 configuration inputs. The value of this bit is later updated, based on the detected host BIOS scheme, see Section 2.19.3 for details. 0: Disabled (default when XCNF disable BIOS configuration) 1: Enabled (default when XCNF enable BIOS configuration)
2	**User-Defined Memory Space Enable.** When set, enables the PC8739x to respond to LPC memory read and write accesses in the user-defined memory area range. The base address and size of the user-defined range is specified by X-Bus Memory Base Address High and Low Byte registers and the X-Bus Memory Size Configuration register. 0: Disabled (default) 1: Enabled
1	**BIOS Extended Space Enable.** Expands the BIOS address space to which the PC8739x responds to include the Extended BIOS address range. 0: Disabled (default) 1: Enabled
0	**BIOS LPC Enable.** Enables the PC8739x to respond to LPC memory accesses to the BIOS-LPC space. The reset value of this register is defined by the XCNF2-0 configuration inputs. The value of this bit is later updated, based on the detected host BIOS scheme (see Section 2.19.3 for details). 0: Disabled (default when XCNF disable BIOS configuration) 1: Enabled (default when XCNF enable BIOS configuration)

2.19.9 X-Bus Memory Base Address High Byte Register

This register describes the high byte for the user-defined memory zone mapped to the X-Bus (decoded as bits 31 to 24 of the 32-bit address range, bits 15-0 are 0). This register is reset by hardware to 00h.

Location: Index F5h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	User-Defined Memory Zone Address High							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**User-Defined Memory Zone Address High.** Defines the higher 8 bits of the user-defined memory block base address. The base address should be aligned on the selected block size.

2.0 Device Architecture and Configuration (Continued)

2.19.10 X-Bus Memory Base Address Low Byte Register

This register describes the low byte for the user-defined memory zone mapped to the X-Bus (decoded as bits 23 to 16 of the 32-bit address range; bits 15 to 0 are 0). This register is reset by hardware to 00h.

Location: Index F6h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	User-Defined Memory Zone Address Low
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**User-Defined Memory Zone Address Low.** Defines the lower 8 bits of the user-defined memory block base address. The base address should be aligned on the selected block size.

2.19.11 X-Bus Memory Size Configuration Register

This register defines the size of the user-defined memory zone mapped to the X-Bus. This register is reset by hardware to 00h.

Location: Index F7h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	\multicolumn{4}{c}{Reserved}	\multicolumn{4}{c}{User-Defined Memory Zone Size}
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-0	**User-Defined Memory Zone Size.** Defines the size in bytes of the zone window. The size is defined as a power of two using the equation: NumOfBytes = 2^n(User-Defined Memory Zone size+16). The zone must always be aligned to the window size (i.e., for a 128 Kbyte window, the 17 LSBs of the address should be zero. **Bits Size (Bytes)** **3 2 1 0** 0 0 0 0 64K (default) **. . .** 1 0 0 0 16M Other Reserved

2.0 Device Architecture and Configuration (Continued)

2.19.12 X-Bus PIRQA and PIRQB Mapping Register

This set of registers defines the mapping of the PIRQA and PIRQB signals.

Location: Index F8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	PIRQB Mapping				PIRQA Mapping			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**PIRQB Mapping.** Defines to which host IRQ the PIRQB input is routed. **Bits Function** **3 2 1 0** 0 0 0 0 IRQ Disabled (default) 0 0 0 1 IRQ1 **. . .** 1 1 1 1 IRQ 15
3-0	**PIRQA Mapping.** Defines to which host IRQ the PIRQA input is routed. **Bits Function** **3 2 1 0** 0 0 0 0 IRQ Disabled (default) 0 0 0 1 IRQ1 **. . .** 1 1 1 1 IRQ 15

2.19.13 X-Bus PIRQC and PIRQD Mapping Register

This set of registers defines the mapping of the PIRQC and PIRQD signals.

Location: Index F9h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	PIRQD Mapping				PIRQC Mapping			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**PIRQD Mapping.** Defines to which host IRQ the PIRQD input is routed. **Bits Function** **3 2 1 0** 0 0 0 0 IRQ Disabled (default) 0 0 0 1 IRQ1 **. . .** 1 1 1 1 IRQ 15
3-0	**PIRQC Mapping.** Defines to which host IRQ the PIRQC input is routed. **Bits Function** **3 2 1 0** 0 0 0 0 IRQ Disabled (default) 0 0 0 1 IRQ1 **. . .** 1 1 1 1 IRQ 15

3.0 General-Purpose Input/Output (GPIO) Port

Note: This section applies to the PC87392, PC87393 and PC87393F only.

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For the device specific implementation, see the *Device Architecture and Configuration* chapter.

3.1 OVERVIEW

The GPIO port is an 8-bit port, which is based on eight pins. It features:

- Software capability to manipulate and read pin levels

- Controllable system notification by several means based on the pin level or level transition

- Ability to capture and manipulate events and their associated status

- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers, mapped in the Device Configuration space. These registers are used to statically set up the logical behavior of each pin. There are two 8-bit register for each GPIO pin.

- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device IO space (which is determined by the base address registers in the GPIO Device Configuration). They are used to manipulate and/or read the pin values, and to control and handle system notification. Each runtime register corresponds to the 8-pin port, such that bit n in each one of the four registers is associated with GPIOXn pin, where X is the port number.

Each GPIO pin is associated with ten configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 8.

The functionality of the GPIO port is divided into basic functionality that includes the manipulation and reading of the GPIO pins, and enhanced functionality. The basic functionality is described in Section 3.2. The enhanced functionality which includes the event detection and system notification is described in Section 3.3.
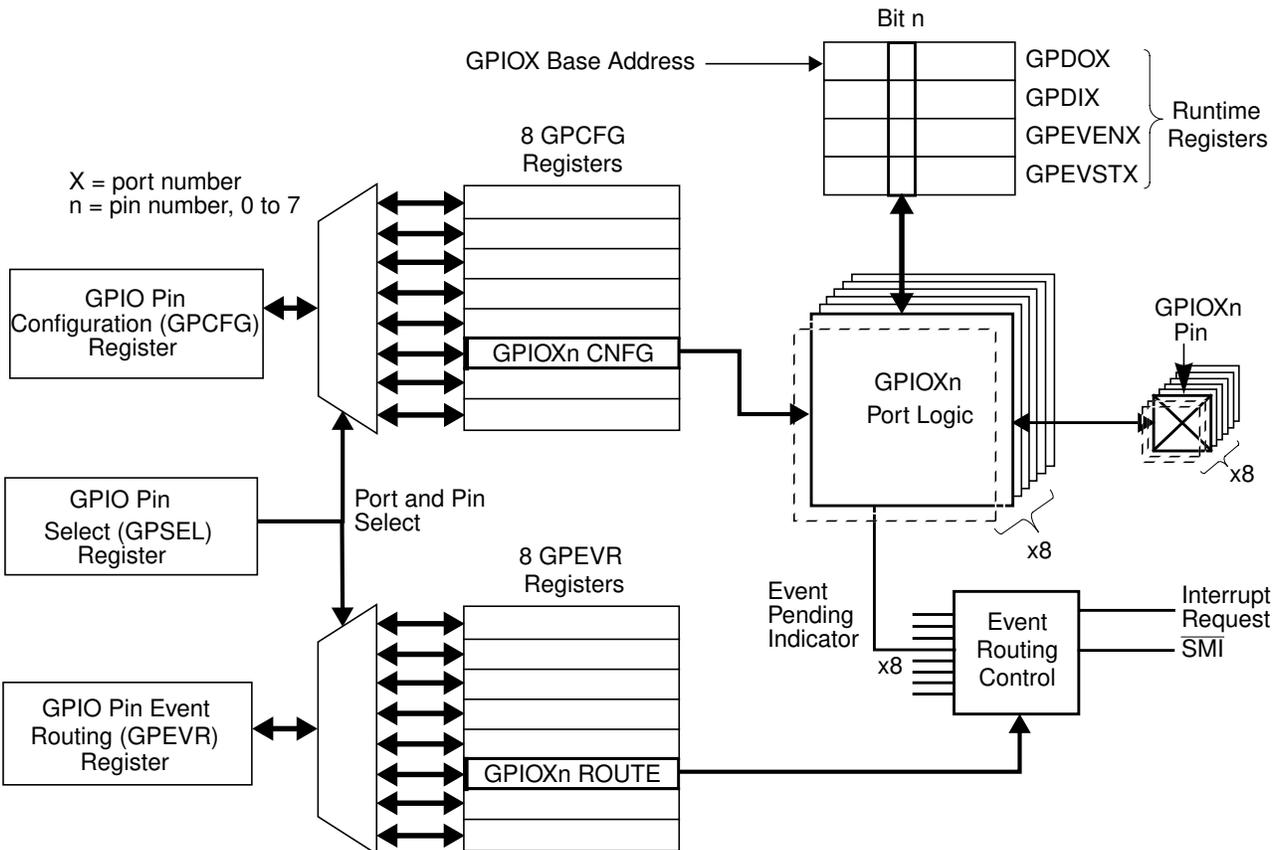
Figure 8. GPIO Port Architecture

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI. The configuration and operation of a single pin GPIOXn (pin n in port X) is shown in Figure 9.
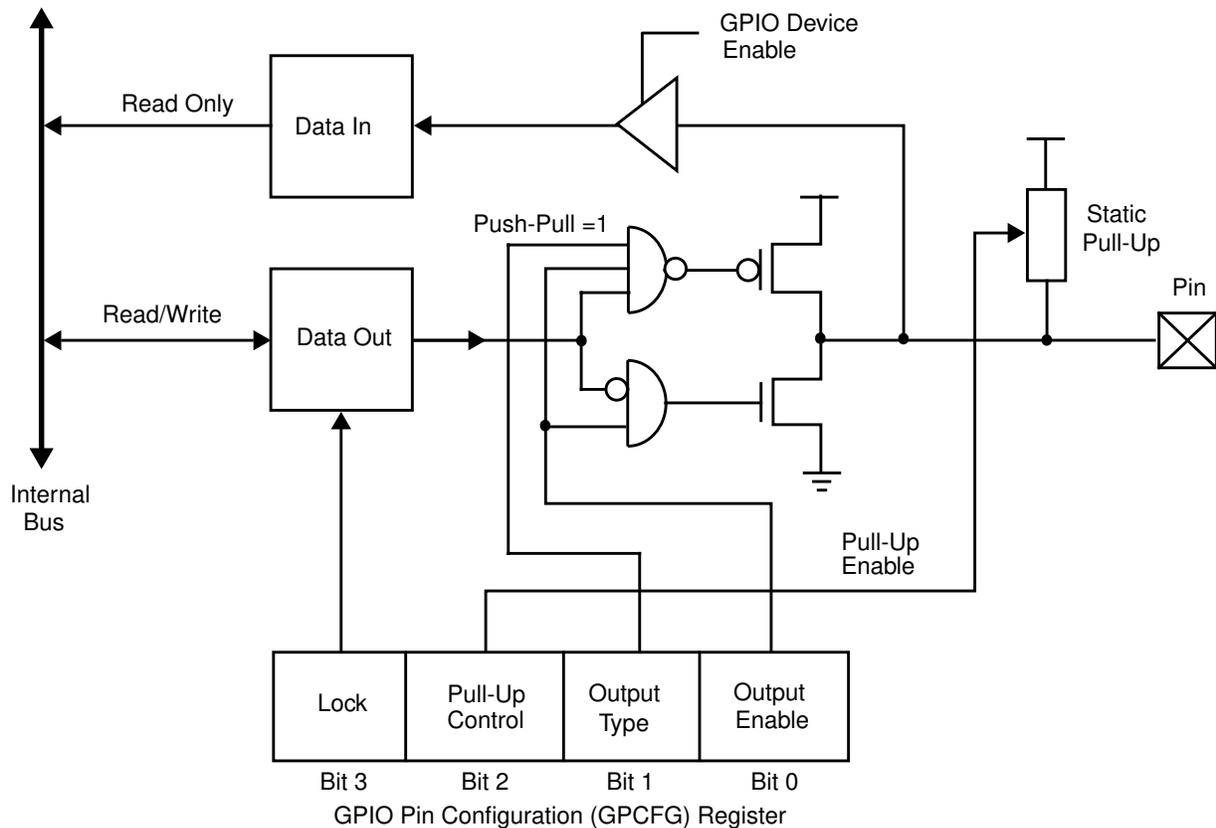
Figure 9. GPIO Basic Functionality

3.2.1 Configuration Options

The GPCFG register controls the following basic configuration options:

- Port Direction - Controlled by the Output Enable bit (bit 0)

- Output Type - Push-pull vs. open-drain. It is controlled by Output Buffer Type (bit 1) by enabling/disabling the pull-up portion of the output buffer.

- Weak Static Pull-Up - May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2).

- Pin Lock - GPIO pin may be locked to prevent any changes in the output value and/or the output characteristics. The lock is controlled by Lock (bit 3). It disables writes to the GPDO register bits, and to bits 0-3 of the GPCFG register (Including the Lock bit itself). Once locked, it can be released by hardware reset only.

3.2.2 Operation

The value that is written to the GPDO register is driven to the pin, if the output is enabled. Reading from the GPDO register returns its contents, regardless of the pin value or the port configuration. The GPDI register is a read-only register. Reading from the GPDI register returns the pin value, regardless of what is driving it (the port itself, configured as an output port, or the external device when the port is configured as an input port). Writing to this register is ignored.

Activation of the GPIO port is controlled by external device specific configuration bit (or a combination of bits). When the port is inactive, access to GPDI and GPDO registers is disabled, and the inputs are blocked. However, there is no change in the port configuration and in the GPDO value, and hence there is no effect on the outputs of the pins.

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port supports system notification based on event detection. This functionality is based on six configuration bits and a bit slice of runtime registers GPEVEN and GPEVST. The configuration and operation of the event detection capability is shown in Figure 10. The operation of system notification is illustrated in Figure 11.
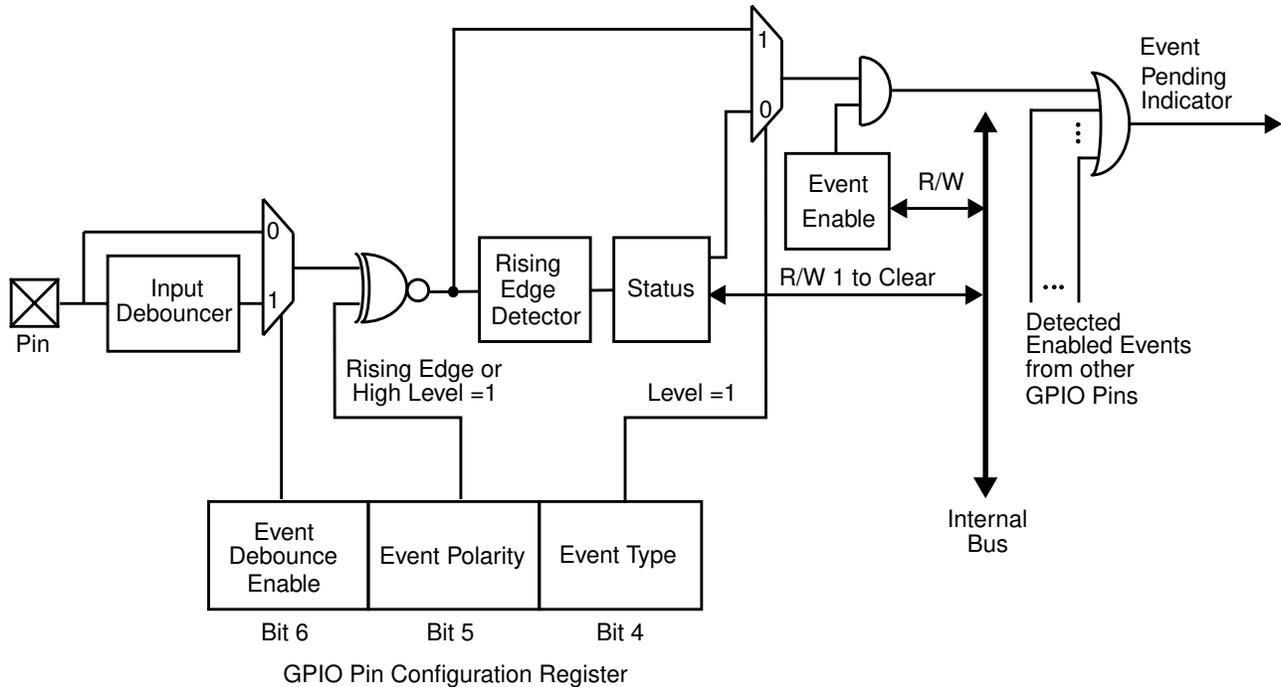
Figure 10. Event Detection

3.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification upon predetermined behavior of the source pin. The GPCFG register determines the event detection trigger type for the system notification.

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected upon a source pin transition either from high to low or low to high. A level event may be detected when the source pin is in active level. The trigger type is determined by Event Type (bit 4 of the GPCFG register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of the GPCFG register).

Event Debounce Enable

The input signal can be debounced for about 15 msec before entering the detector. The signal state is transferred to the detector only after a debouncing period during which the signal has no transitions, to ensure that the signal is stable. The debouncer adds 15 msec delay to both assertion and de-assertion of the event pending indicator. Therefore, when working with a level event and system notification by either $\overline{SMI}$ or IRQ, it is recommended to disable the debounce if the delay in the $\overline{SMI}$/IRQ de-assertion is not acceptable. The debounce is controlled by Event Debounce Enable (bit 6 of the GPCFG register).

3.3.2 System Notification

System notification on GPIO-triggered events is by means of assertion of one or more of the following output pins:

- Interrupt Request (via the device's Bus Interface)
- System Management Interrupt ($\overline{SMI}$, via the device's Bus Interface)

The system notification for each GPIO pin is controlled by the corresponding bits in the GPEVEN and GPEVR registers. System notification by a GPIO pin is enabled if the corresponding bit of the GPEVEN register is set to 1. The corresponding bits in the GPEVR register select which means of system notification the detected event is routed to. The event routing mechanism is described in Figure 11.

3.0 General-Purpose Input/Output (GPIO) Port (Continued)
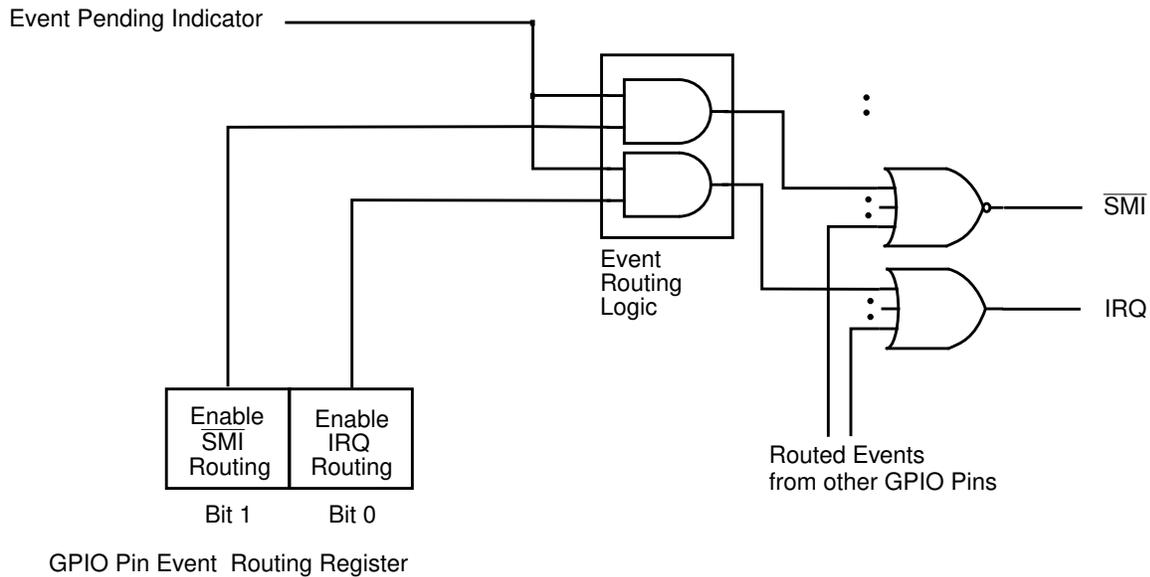
Figure 11. GPIO Event Routing Mechanism

The GPEVST register is a general-purpose edge detector which may be used to reflect the event source pending status for edge-triggered events.

The term *active edge* refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit of the GPEVST register is set by hardware whenever an active edge is detected, regardless of any other bit settings. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if the corresponding bit of the GPEVEN register is set and either:

- The Event Type is level and the pin is in active level, or
- The Event Type is edge and the corresponding bit of the GPEVST register is set.

The target means of system notification is asserted if at least one GPIO pin is in event pending state.

The selection of the target means of system notification is determined by the GPEVR register. If IRQ is selected as one of the means for the system notification, the specific IRQ line is determined by the IRQ selection procedure of the device configuration. The assertion of any means of system notification is blocked when the GPIO functional block is deactivated.

If the output of a GPIO pin is enabled, it may be put in event pending state by the software when writing to the GPDO register.

An pending edge event may be cleared by clearing the corresponding GPEVST bit. However, a level event source may not be released by software (except for disabling the source), as long as the pin is in active level. When level event is used, it is recommended to disable the input debouncer.

Upon de-activation of the GPIO port, the GPEVST register is cleared and access to both the GPEVST and GPEVEN registers is disabled. All system notification means including the target IRQ line are detached from the GPIO and de-asserted.

Before enabling any system notification, it is recommended to set the desired event configuration, and then verify that the status registers are cleared.

3.4 GPIO PORT REGISTERS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.4.1 GPIO Pin Configuration (GPCFG) Register

This is a group of eight identical configuration registers, each of which is associated with one GPIO pin. The entire set is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register that functions as an index register, and the specific GPCFG register that reflects the configuration of the currently selected pin. For details on the GPSEL register, refer to the *Device Architecture and Configuration* chapter.

Bits 4-6 are applicable only for the enhanced GPIO port with event detection support. In the basic port, these bits are reserved, return 0 on read and have no effect on port functionality.

Location: Device specific

Type: R/W (bit 3 is set only)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Event Debounce Enable	Event Polarity	Event Type	Lock	Pull-Up Control	Output Type	Output Enable
Reset	0	1	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**Event Debounce Enable** 0: Disabled 1: Enabled (default)
5	**Event Polarity.** This bit defines the polarity of the signal that causes a detection of an event from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input
4	**Event Type.** This bit defines the signal type that causes detection of an event from the corresponding GPIO pin. 0: Edge input (default) 1: Level input
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1. (Refer to the *Device Architecture and Configuration* chapter.) 0: No effect (default) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on input. 0: TRI-STATE (default) 1: Output enabled

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.4.2 GPIO Pin Event Routing (GPEVR) Register

This is a group of eight identical configuration registers, each of which is associated with one GPIO pin. The entire set is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register that functions as an index register, and the specific GPER register that reflects the routing configuration of the currently selected pin. For details on the GPSEL register, refer to the *Device Architecture and Configuration* chapter.

This set of registers is applicable only for the enhanced GPIO port with event detection support. In the basic port this register set is reserved, returns 0 on read and has no effect on port functionality.

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved						GPIO Event to $\overline{\text{SMI}}$ Enable	GPIO Event to IRQ Enable
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-2	**Reserved**
1	**GPIO Event to $\overline{\text{SMI}}$ Enable.** This bit is used to enable/disable the routing of the corresponding detected GPIO event to $\overline{\text{SMI}}$. 0: Disabled (default) 1: Enabled
0	**GPIO Event to IRQ Enable.** This bit is used to enable/disable the routing of the corresponding detected GPIO event to IRQ. 0: Disabled 1: Enabled (default)

3.4.3 GPIO Port Runtime Register Map

Offset	Mnemonic	Register Name	Type	Section
Device specific [1]	GPDO	GPIO Data Out	R/W	3.4.4
Device specific [1]	GPDI	GPIO Data In	RO	3.4.5
Device specific [1]	GPEVEN	GPIO Event Enable	R/W	3.4.6
Device specific [1]	GPEVST	GPIO Event Status	R/W1C	3.4.7

1. The location of this register is defined in the *Device Architecture and Configuration* chapter in Section 2.15.1.

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.4.4 GPIO Data Out Register (GPDO)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Data Out							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7	
6	
5	**Data Out.** Bits 7-0 correspond to pins 7-0 respectively. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the
4	bit is locked by the GPCFG register Lock bit. Reading the bit returns its value, regardless of the pin value and configuration.
3	0: Corresponding pin driven to low when output enabled
2	1: Corresponding pin driven or released to high (according to buffer type and static pull-up selection) when
1	output enabled
0	

3.4.5 GPIO Data In Register (GPDI)

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Data In							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7	
6	
5	**Data In.** Bits 7-0 correspond to pins 7-0 respectively. Reading each bit returns the value of the corresponding
4	GPIO pin, regardless of the pin configuration and the GPDO register value. Write is ignored.
3	0: Corresponding pin level low
2	1: Corresponding pin level high
1	
0	

3.0 General-Purpose Input/Output (GPIO) Port (Continued)

3.4.6 GPIO Event Enable Register (GPEVEN)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Event Enable							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	
6	
5	**Event Enable.** Bits 7-0 correspond to pins 7-0 respectively. Each bit enables system notification triggering by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in the GPEVST register.
4	0: IRQ generation by corresponding GPIO pin masked
3	1: IRQ generation by corresponding GPIO pin enabled
2	
1	
0	

3.4.7 GPIO Event Status Register (GPEVST)

Location: Device specific

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	Status							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	
6	
5	**Status.** Bits 7-0 correspond to pins 7-0 respectively. Each bit is an edge detector that is set to 1 by the hardware upon detection of an active edge (i.e. edge that matches the IRQ Polarity bit) on the corresponding GPIO pin. This edge detection is independent of the Event Type or the Event Enable bit in the GPEVEN register. However, the bit may reflect the event status for enabled, edge-trigger event sources. Writing 1 to the Status bit clears it to 0.
4	
3	0: No active edge detected since last cleared
2	1: Active edge detected
1	
0	

4.0   WATCHDOG Timer (WDT)

4.1   OVERVIEW

The WATCHDOG Timer prompts the system via SMI or interrupt when no system activity is detected on a predefined selection of system events for a predefined period of time (1 to 255 minutes).

The WATCHDOG Timer monitors two maskable system events: the interrupt request lines of the two serial ports (UART1 and UART2). The system prompt is performed by asserting a special-purpose output pin ($\overline{WDO}$), which can be attached to external SMI. Alternatively, this indication can be routed to any arbitrary IRQ line and is also available on a status bit that can be read by the host.

This chapter describes the generic WATCHDOG Timer functional block. A device may include a different implementation. For device specific implementation, see the *Device Architecture and Configuration* chapter.

4.2   FUNCTIONAL DESCRIPTION

The WATCHDOG Timer consists of an 8-bit counter and three registers: Timeout register (WDTO), Mask register (WDMSK) and Status register (WDST). The counter is an 8-bit down counter that is clocked every minute and is used for the timeout period countdown. The WDTO register holds the programmable timeout, which is the period of inactivity after which the WATCHDOG Timer prompts the system (1 to 255 minutes). The WDMSK register determines which system events are enabled as WATCHDOG Timer trigger events to restart the countdown. The WDST register holds the WATCHDOG Timer status bit that reflects the value of the $\overline{WDO}$ pin and indicates that the timeout period has expired.

Figure 12 shows the functionality of the WATCHDOG Timer.

Upon reset, the Timeout register (WDTO) is initialized to zero, the timer is deactivated, the $\overline{WDO}$ is inactive (high) and all trigger events are masked.

Upon writing to the WDTO register, the timer is activated while the counter is loaded with the timeout value and starts counting down every minute. If a trigger event (unmasked system event) occurs before the counter has expired (reached zero), the counter is reloaded with the timeout period (from WDTO register) and restarts the countdown. If no trigger event occurs before the timeout period expires, the counter reaches zero and stops counting. Consequently, the $\overline{WDO}$ pin is asserted (pulled low) and the $\overline{WDO}$ Status bit is cleared to 0.~

Writing to the WDTO register de-asserts the $\overline{WDO}$ output (released high) and sets the $\overline{WDO}$ Status bit to 1. If a non-zero value is written, a new countdown starts as described above. If 00h is written, the timer is deactivated.

To summarize, the $\overline{WDO}$ output is de-asserted (high) and the Status bit is set to 1 (inactive) upon:

- Reset
- Activating the WATCHDOG Timer or
- Writing to the WDTO register.

The $\overline{WDO}$ output is asserted (low) and the $\overline{WDO}$ status is set to zero (active) when the counter reaches zero.

When an IRQ is assigned to the WATCHDOG Timer (through the WATCHDOG Timer device configuration), the selected IRQ level is active as long as the $\overline{WDO}$ status bit is low (active).
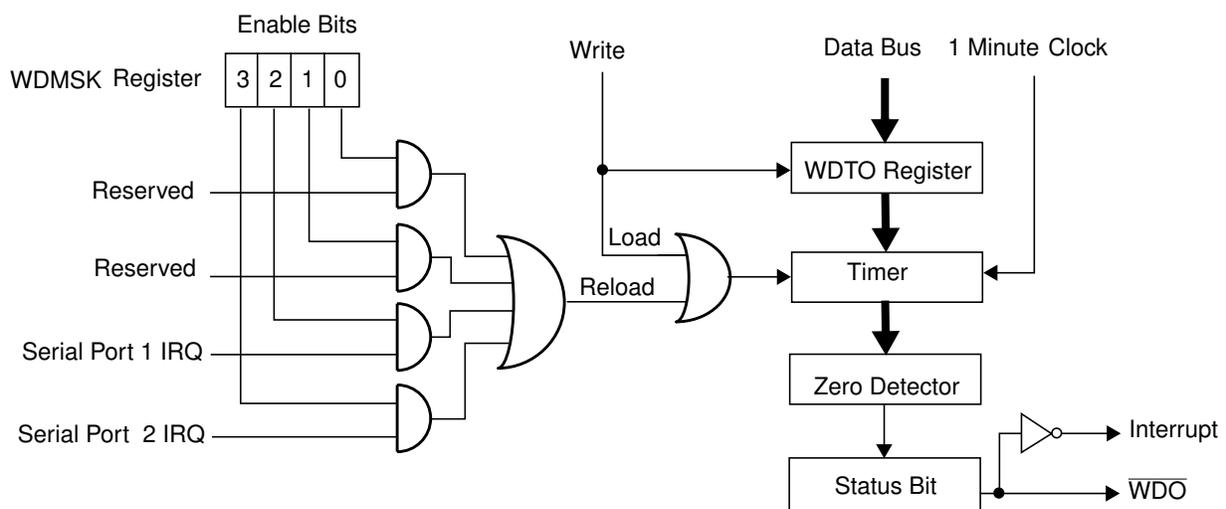
Figure 12. WATCHDOG Timer Functional Diagram

4.0 WATCHDOG Timer (WDT) (Continued)

4.3 WATCHDOG TIMER REGISTERS

The WATCHDOG Timer registers at offsets 00h-02h relative to the WATCHDOG base address, are shown in the following register map. The base address is defined by designated registers in the WATCHDOG Timer device configuration register set.

The following abbreviations are used to indicate the Register Type:

R/W   = Read/Write

R   = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.

W   = Write

RO   = Read Only

R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

4.3.1   WATCHDOG Timer Register Map

Offset	Mnemonic	Register Name	Type	Section
00h	WDTO	WATCHDOG Timeout	R/W	4.3.2
01h	WDMSK	WATCHDOG Mask	R/W	4.3.3
02h	WDST	WATCHDOG Status	RO	4.3.4
03h		Reserved		

4.3.2   WATCHDOG Timeout Register (WDTO)

This register holds the programmable timeout period, between 1 and 255 minutes. Writing to this register de-asserts the $\overline{WDO}$ output and sets the $\overline{WDO}$ status bit to 1 (inactive). Additionally, writing to this register is interpreted as a command for starting or stopping the WATCHDOG Timer, according to the data written. If a non-zero value is written, the timer is activated (countdown starts). If a non-zero value is written when the counter is running, the timer is immediately reloaded with the new value and starts counting down from the new value. If 00h is written, the timer and its outputs are de-activated.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Programmed Timeout Period							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Programmed Timeout Period.** These bits hold the binary value of the timeout period in minutes (1 to 255). A value of 00h halts the counter and forces the outputs to inactive levels. A device reset clears the register to 00h. 00h: Timer and $\overline{WDO}$ outputs inactive 01h-FFh: Programmed timeout period (in minutes)

4.0 WATCHDOG Timer (WDT) (Continued)

4.3.3 WATCHDOG Mask Register (WDMSK)

This register is used to determine which system events (IRQ) are enabled as WATCHDOG Timer trigger events. An enabled IRQ event becomes a trigger event that causes the timer to reload the WDTO and restart the countdown.

This register enables or masks the trigger events that restart the WATCHDOG timer.

Location: Offset 01h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Serial Port 2 IRQ Trigger Enable	Serial Port 1 IRQ Trigger Enable	Reserved	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**Serial Port 2 IRQ Trigger Enable.** This bit enables the IRQ assigned to Serial Port 2 to trigger WATCHDOG Timer reloading. 0: Serial Port 2 IRQ not a trigger event 1: An active Serial Port 2 IRQ enabled as a trigger event
2	**Serial Port 1 IRQ Trigger Enable.** This bit enables the IRQ assigned to Serial Port 1 to trigger WATCHDOG Timer reloading. 0: Serial Port 1 IRQ not a trigger event 1: An active Serial Port 1 IRQ enabled as a trigger event
1-0	**Reserved**

4.0 WATCHDOG Timer (WDT) (Continued)

4.3.4   WATCHDOG Status Register (WDST)

This register holds the WATCHDOG Timer status, which reflects the value of the $\overline{\text{WDO}}$ pin and indicates that the timeout period has expired.

On reset or on WATCHDOG Timer activation, this register is initialized to 01h.

Location: Offset 02h
Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Reserved							$\overline{\text{WDO}}$ Value
Reset	0	0	0	0	0	0	0	1
Required	0							

Bit	Description
7-1	**Reserved**
0	**$\overline{\text{WDO}}$ Value.** This bit reflects the value of the $\overline{\text{WDO}}$ signal (even if $\overline{\text{WDO}}$ is not configured for output). 0: $\overline{\text{WDO}}$ active 1: $\overline{\text{WDO}}$ inactive (default)

4.4   WATCHDOG TIMER REGISTER BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	WDTO	Programmed Timeout Period							
01h	WDMSK	Reserved				Serial Port 2 IRQ Trigger Enable	Serial Port 1 IRQ Trigger Enable	Reserved	
02h	WDST	Reserved							$\overline{\text{WDO}}$ Value

5.0 Game Port (GMP)

Note: This section applies to the PC87393 and PC87393F only.

5.1 OVERVIEW

This chapter describes a generic Game Port. For the implementation used in this device, see the *Device Architecture and Configuration* chapter.

The Game Port monitors the interface of up to two game devices, and provides data that can be used to determine the exact momentary status of these game devices.

A game device is an instrument used for giving commands to a PC, usually to control a game executed on that PC. A Joystick is a commonly used game device. These commands are given by the game device in a passive manner, by indicating several status parameters that can be captured by the system via the Game Port.

The status of a game device includes the following parameters:

- Button status (pressed/released) of up to two buttons per game device
- Horizontal (X-axis) position indicated by the game device
- Vertical (Y-axis) position indicated by the game device.

Figure 13 shows the basic system configuration of the Game Port.
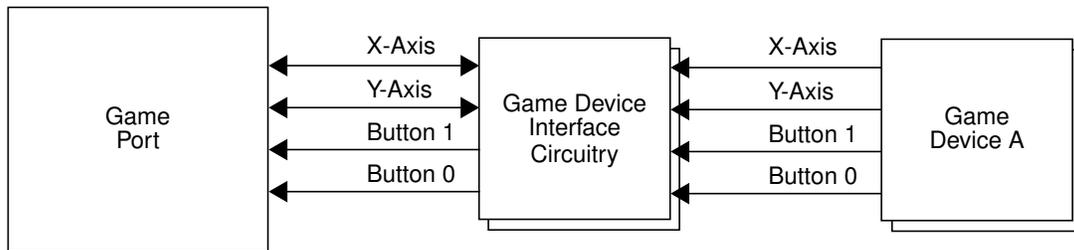
Figure 13. Game Port System Configuration

5.2 FUNCTIONAL DESCRIPTION

5.2.1 Game Device Axis Position Indication

A typical game device has the following interface pins:

- an X-axis position indicator
- a Y-axis position indicator
- one or two button status indicator(s).

The X and Y axis indicators are fed into the Game Port via pins JOYnX and JOYnY, respectively, where 'n' indicates the game device number. The status indicators of buttons 0 and 1 are fed into the Game Port via JOYnBTN0,1, respectively.

The X and Y axis position indication mechanism of each game device includes external components, as seen in Figure 14. Such a mechanism is implemented per game device axis line.
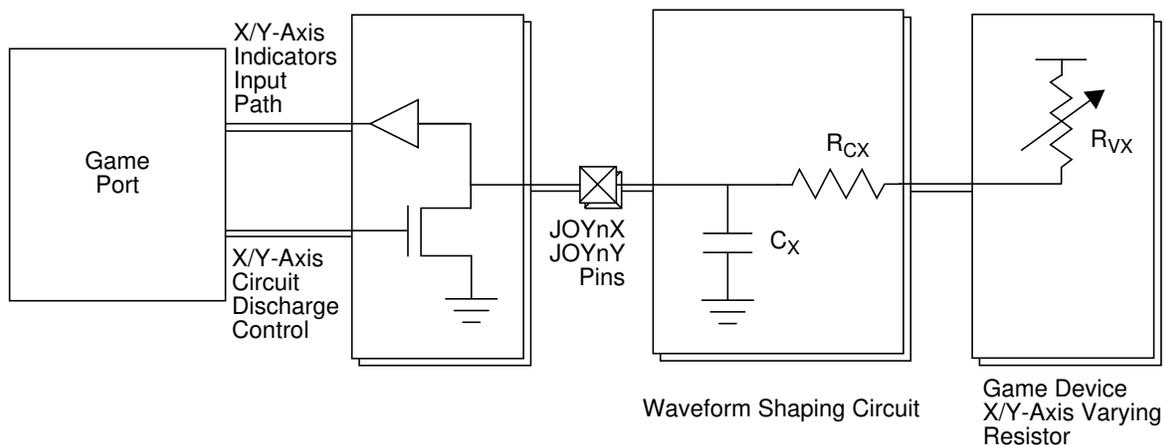
Figure 14. Game Device Axis Position Indication Mechanism

5.0 Game Port (GMP) (Continued)

The varying resistors R_{VX} and R_{VY} are usually implemented in the game device. Their resistance values are determined directly by the horizontal and vertical positions, respectively, indicated by the game device. The waveform shaping circuits are usually implemented outside the game device using constant resistors ($R_{CX/Y}$) and constant capacitors ($C_{X/Y}$). Together with $R_{VX/Y}$, these components implement two R-C structures, the varying parameters of which are used to determine the exact momentary position indicated by the game device.

When the Game Port is enabled and not in the midst of a game device position reading process, it drives the JOYnX,Y pins low. In this state, the capacitors $C_{X/Y}$ are completely discharged.

5.2.2   Capturing the Position

The process of capturing the position indicated by the game device is initiated by a command given to the Game Port to release the JOYnX,Y lines, thus allowing the capacitors $C_{X/Y}$ to be charged. This command is given by performing a write access to offset 1 from the Game Port base address, which is the offset of the Game Port Legacy Status Register (GMPLST, see Section 5.3.3). Once JOYnX,Y pins are released, $R_{CX/Y}$ and $R_{VX/Y}$ start charging $C_{X/Y}$, and the voltage level of the JOYnX,Y pins increases until it reaches V_{IH}. This process is described in Figure 15.
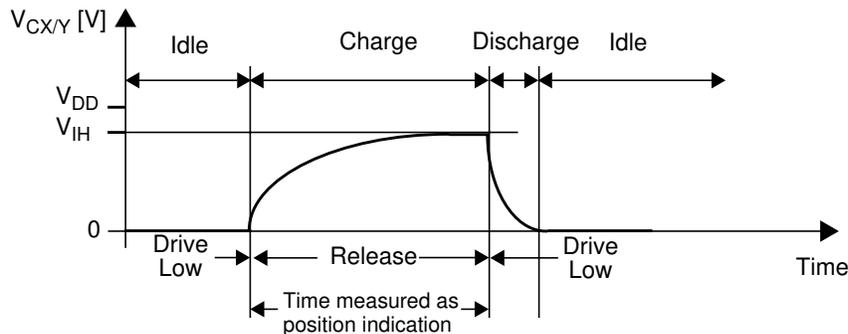
Figure 15. Position Reading Process Waveform (not drawn to scale)

The vertical and horizontal positions indicated by the game device are determined by measuring the time it takes for the voltage level on the JOYnX,Y pins to reach the level of logic 1. Since the charging time is determined by the resistance values of $R_{VX/Y}$, measuring this time actually indicates the resistance values of $R_{VX/Y}$, and therefore also reflects the position indicated by the game device.

Once an axis pin is sensed as logic 1, the axis circuit discharge control is activated in order to discharge $C_{X/Y}$. This causes the corresponding axis pin to be driven low for approximately 1.5 µsec. After that, this axis line is held low until another position reading process is initiated.

During the charge time and the 1.5 µsec discharge time which follows, the corresponding axis line does not respond to any reading process initiation. This prevents software from disturbing the position reading process and makes the position reading processes of all axis lines independent of each other.

5.2.3   Button Status Indication

The button(s) status indication mechanism is described in Figure 16. Although this figure shows an active-low button ($R_{BU0} \gg R_{BD0}$), the polarity of the button can be either high or low, assuming that the Game Port software is aware of the button's polarity.

Game Device Button Status Circuit
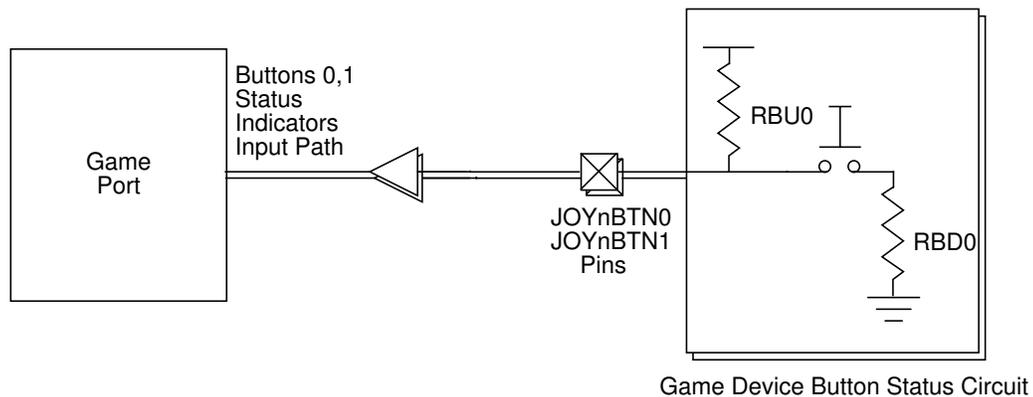
Figure 16. Game Device Button Status Indication Mechanism

5.0 Game Port (GMP) (Continued)

A simple push-button mechanism is usually used to implement the game device buttons. The status of each button is sensed by the Game Port via the JOYnBTN0,1 pins as either high or low, and reflected by the GMPLST register. It is the responsibility of the software to determine the actual status of the buttons according to their polarity, which depends on the specific implementation of the system and the game device.

5.2.4   Operation Modes

The Game Port can be used to monitor the position and button status indicators in one of the following operation modes:

- Legacy mode
- Enhanced mode.

Legacy Mode

Legacy mode is enabled when bit 0 of the GMPCTL register is set to 0, which is its default state.

In this mode, the game device indicators are monitored by polling their momentary status via the Game Port Legacy Status register (GMPLST, see Section 5.3.3).

The process of reading the position status of the game device(s) is initiated by performing a write access to offset 1 in the Game Port address space. This write access causes the Game Port to release the JOYnX,Y pins. When a JOYnX,Y pin is released, the corresponding bit in the GMPLST register is set to 1. To capture the position indicated by the game device, the software must poll the GMPLST register and measure the time it takes for the JOYnX,Y to go high. This measurement should be performed by measuring the time during which an axis bit is 1.

Reading the status of the buttons of the game device is done by polling the GMPLST register and looking for changes in the bits reflecting the status of the JOYnBTN0,1 pins.

No debounce of the input signals is performed by the Game Port in Legacy mode. It is the responsibility of the software to implement such debounce, if necessary.

Enhanced Mode

Enhanced mode is enabled when bit 0 of the GMPCTL register is set to 1.

In Enhanced mode, the Game Port hardware monitors the status indicators of the game device(s), and provides processed data that can be easily used by software to determine the complete status of the game device.

The process of reading the position status of the game device(s) is initiated as in Legacy mode. However, in Enhanced mode the Game Port hardware measures the $C_{X/Y}$ charging time using four 16-bit up-counters. Each one of the four axis status lines (two lines per game device) has a dedicated counter.

Once the Game Port releases the JOYnX,Y to go high, each one of the counters starts counting until its associated axis status line reaches the voltage level of logic 1.

When a position counter of a game device stops counting, its associated Position Counter Ready bit in the GMPXST register is set. In this case, the software must wait until the counters associated with the game device are ready, and then read their values. The least significant byte of a position counter should be read first. The full, 16-bit count value should be calculated as follows:

$$X/Y \text{ Position Count} = GMPnX/YL + (GMPnX/YH * 256)$$

> where:
> GMPnX/YL indicates the low byte of the position counter of device n (either X or Y axis)
>
> GMPnY/HL indicates the high byte of the position counter of device n (either X or Y axis)

The software must calibrate itself according to the actual count values acquired when the game device was set to indicate its extreme horizontal and vertical positions.

If a position counter has reached the full count of FFFFh, this counter has overflowed; i.e., it has reached its full count before the corresponding axis indicator has reached the level of logic 1. In such a case, the software must decide what to do.

The Game Port supports the following clock frequencies for operating the position counters:

- 1 MHz clock (default)
- 500 KHz clock.

The clock frequency for the position counter of each game device is configured via the GMPCTL register and should be set by the software to match the physical components of the external game device interface circuitry. The desired position of the counter frequency should be set before initiating a position status reading process.

Reading the status of the buttons of the game device(s) is performed as in Legacy mode. In addition, an optional debouncer of 16 msec is implemented on each button status input. The debouncers are disabled by default and may be enabled by software via the GMPCTL register.

5.0 Game Port (GMP) (Continued)

5.2.5   Operation Control

When the Game Port is operated in Legacy mode, it can only be operated by polling (see Section 5.2.4, *Legacy Mode*).

When the Game Port is operated in Enhanced mode, both kinds of status reading operations (position and button) can be performed using polling or interrupt controlled operation.

If polling controlled operation is preferred, the software should poll either the GMPLST register for the direct status of the buttons as in Legacy mode, or the GMPXST register which provides indications regarding button events detected by hardware. The GMPXST register should also be polled for the status of the position counters. When the status is ready, the counter values can be read. These values reflect the positions indicated by the game device.

If interrupt controlled operation is preferred, the software should first define the events on which an interrupt request is to be issued. This is done by writing the required values to the GMPEPOL (see Section 5.3.14) and GMPIEN (see Section 5.3.5) registers. The GMPEPOL register defines the events on which the buttons cause an interrupt request to be issued. These events are all edge-triggered. The GMPIEN register determines what events are physically routed to the interrupt request assigned to the Game Port. An independent interrupt enable bit is implemented in the GMPIEN register for each one of the four buttons and two position counters of the two supported game devices.

5.3 GAME PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write

- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.

- W = Write

- RO = Read Only

- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

5.3.1   Game Port Register Map

The following table lists the Game Port registers. for the Game Port register bitmap, see Section 5.4.

Offset	Mnemonic	Register Name	Type	Section
00h	GMPCTL	Game Port Control	R/W	5.3.2
01h	GMPLST	Game Port Legacy Status	RO	5.3.3
02h	GMPXST	Game Port Extended Status	R/W1C	5.3.4
03h	GMPIEN	Game Port Interrupt Enable	R/W	5.3.5
04h	GMPAXL	Game Device A X Position Low Byte	RO	5.3.6
05h	GMPAXH	Game Device A X Position High Byte	RO	5.3.7
06h	GMPAYL	Game Device A Y Position Low Byte	RO	5.3.8
07h	GMPAYH	Game Device A Y Position High Byte	RO	5.3.9
08h	GMPBXL	Game Device B X Position Low Byte	RO	5.3.10
09h	GMPBXH	Game Device B X Position High Byte	RO	5.3.11
0Ah	GMPBYL	Game Device B Y Position Low Byte	RO	5.3.12
0Bh	GMPBYH	Game Device B Y Position High Byte	RO	5.3.13
0Ch	GMPEPOL	Game Port Event Polarity	R/W	5.3.14

5.0 Game Port (GMP) (Continued)

5.3.2   Game Port Control Register (GMPCTL)

This register affects the functionality of the Game Port only when operated in Enhanced mode (bit 0 of this register is set to 1). Bits 1,2 and 4-7 affect Game Port functionality, as described in the table below.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Device B Button 1 Debounce Enable	Device B Button 0 Debounce Enable	Device A Button 1 Debounce Enable	Device A Button 0 Debounce Enable	Reserved	Device B Pre-Scale Enable	Device A Pre-Scale Enable	GMP Enhanced Mode Enable
Reset	0	0	0	0	0	0	0	0
Required					0			

Bit	Description
7	**Device B Button 1 Debounce Enable.** When set to 1, enables a 16 ms input debouncer on Device B Button 1 status input. 0: Disabled (default) 1: Enabled
6	**Device B Button 0 Debounce Enable.** Same as bit 7, but for Device B Button 0. 0: Disabled (default) 1: Enabled
5	**Device A Button 1 Debounce Enable.** Same as bit 7, but for Device A Button 1. 0: Disabled (default) 1: Enabled
4	**Device A Button 0 Debounce Enable.** Same as bit 7, but for Device A Button 0. 0: Disabled (default) 1: Enabled
3	**Reserved**
2	**Device B Pre-Scale Enable.** This bit determines the clock frequency used by Device B position counters. 0: 1 MHz (default) 1: 500 KHz
1	**Device A Pre-Scale Enable.** This bit determines the clock frequency used by Device A position counters. 0: 1 MHz (default) 1: 500 KHz
0	**GMP Enhanced Mode Enable** 0: Disabled (default) 1: Enabled

5.0 Game Port (GMP) (Continued)

5.3.3 Game Port Legacy Status Register (GMPLST)

This register is functional in all Game Port operation modes. Reading this register returns the status and the state of Device A and B button and Axis pins, as defined in the table below. Writing to the offset of this register initiates a game device position reading process by forcing a low pulse to be driven on the axis pins in Legacy and Enhanced modes, and by initializing all position counters in Enhanced mode.

Location: Offset 01h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device B Button 1 Pin Status	Device B Button 0 Pin Status	Device A Button 1 Pin Status	Device A Button 0 Pin Status	Device B Y-Axis Pin Status	Device B X-Axis Pin Status	Device A Y-Axis Pin Status	Device A X-Axis Pin Status
Reset	X	X	X	X	X	X	X	X

Bit	Description
7	**Device B Button 1 Pin Status.** This bit directly reflects the status of Device B Button 1 input pin. 0: Low 1: High
6	**Device B Button 0 Pin Status.** This bit directly reflects the status of Device B Button 0 input pin. 0: Low 1: High
5	**Device A Button 1 Pin Status.** This bit directly reflects the status of Device A Button 1 input pin. 0: Low 1: High
4	**Device A Button 0 Pin Status.** This bit directly reflects the status of Device A Button 0 input pin. 0: Low 1: High
3	**Device B Y-Axis Pin Status.** This bit reflects the state of Device B Y-axis input pin. 0: JOYBY pin is driven low 1: JOYBY pin is released for charging
2	**Device B X-Axis Pin Status.** This bit reflects the state of Device B X-axis input pin. 0: JOYBX pin is driven lowr 1: JOYBX pin is released for charging
1	**Device A Y-Axis Pin Status.** This bit reflects the state of Device A Y-axis input pin. 0: JOYAY pin is driven low 1: JOYAY pin is released for charging
0	**Device A X-Axis Pin Status.** This bit reflects the status of Device A X-axis input pin. 0: JOYAX pin is driven low 1: JOYAX pin is released for charging

5.0 Game Port (GMP) (Continued)

5.3.4   Game Port Extended Status Register (GMPXST)

This register indicates which of the corresponding game device interface events have occurred. Writing 1 to a bit clears it. Reading a position counter clears the corresponding Counter Ready bit. Writing to a bit 0 has no effect.

This register is functional only in Enhanced mode.

Location: Offset 02h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	Device B Button 1 Event Status	Device B Button 0 Event Status	Device A Button 1 Event Status	Device A Button 0 Event Status	Device B Y-Position Counter Ready	Device B X-Position Counter Ready	Device A Y-Position Counter Ready	Device A X-Position Counter Ready
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Device B Button 1 Event Status.** When set to 1, it indicates that a Device B Button 1 event has occurred. The event itself is defined by the GMPEPOL register, see Section 5.3.14. 0: Event not active (default) 1: Event active
6	**Device B Button 0 Event Status.** When set to 1, it indicates that a Device B Button 0 event has occurred. The event itself is defined by the GMPEPOL register, see Section 5.3.14. 0: Event not active (default) 1: Event active
5	**Device A Button 1 Event Status.** When set to 1, it indicates that a Device A Button 1 event has occurred. The event itself is defined by the GMPEPOL register, see Section 5.3.14. 0: Event not active (default) 1: Event active
4	**Device A Button 0 Event Status.** When set to 1, it indicates that a Device A Button 0 event has occurred. The event itself is defined by the GMPEPOL register, see Section 5.3.14. 0: Event not active (default) 1: Event active
3	**Device B Y-Position Counter Ready.** When set to 1, it indicates that the value of the Y-position counter of Device B can now be read. 0: Event not active (default) 1: Event active
2	**Device B X-Position Counter Ready.** When set to 1, it indicates that value of the X-position counter of Device B can now be read. 0: Event not active (default) 1: Event active
1	**Device A X-Position Counter Ready.** When set to 1, it indicates that the value of the Y-position counter of Device A can now be read. 0: Event not active (default) 1: Event active
0	**Device A X-Position Counter Ready.** When set to 1, it indicates that the value of the X-position counter of Device A can now be read. 0: Event not active (default) 1: Event active

5.0 Game Port (GMP) (Continued)

5.3.5 Game Port Interrupt Enable Register (GMPIEN)

This register defines the conditions on which the Game Port asserts its interrupt request signal.

This register is functional only in Enhanced mode.

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Device B Button 1 IRQ Enable	Device B Button 0 IRQ Enable	Device A Button 1 IRQ Enable	Device A Button 0 IRQ Enable	Reserved	Position IRQ Event Definition	Device B Position IRQ Enable	Device A Position IRQ Enable
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Device B Button 1 IRQ Enable.** When set to 1, the Game Port issues an interrupt request in response to an event triggered by Button 1 of Device B. When set to 0, Button 1 of Device B cannot cause interrupt requests to be issued. 0: Disabled (default) 1: Enabled
6	**Device B Button 0 IRQ Enable.** Same as bit 7 of this register, but for Device B Button 0. 0: Disabled (default) 1: Enabled
5	**Device A Button 1 IRQ Enable.** Same as bit 7 of this register, but for Device A Button 1. 0: Disabled (default) 1: Enabled
4	**Device A Button 0 IRQ Enable.** Same as bit 7 of this register, but for Device A Button 0. 0: Disabled (default) 1: Enabled
3	**Reserved**
2	**Position IRQ Event Definition** Defines the event on which the position IRQ is asserted for both game devices. 0: Both X-Position Counter and Y-Position Counter are ready 1: Either X-Position Counter or Y-Position Counter is ready
1	**Device B Position IRQ Enable.** When set to 1, the Game Port issues an interrupt request when the position reading of Device B is completed and the position counters can be read. When set to 0, no interrupt request is issued in response to any change in the status of Device B position counters. 0: Disabled (default) 1: Enabled
0	**Device A Position IRQ Enable.** Same as bit 2 of this register, but for Device A. 0: Disabled (default) 1: Enabled

5.0 Game Port (GMP) (Continued)

5.3.6 Game Device A X-Axis Position Low Byte (GMPAXL)

Reading this register returns the value of the low byte of the X-axis position counter of game Device A. Before reading this register verify that bit 0 of GMPXST (Device A Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 04h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device A X-Axis Position Counter Low Byte							
Reset	0	0	0	0	0	0	0	0

5.3.7 Game Device A X-Axis Position High Byte (GMPAXH)

Reading this register returns the value of the high byte of the X-axis position counter of game Device A. Read this register after reading the GMPAXL register, and verifying that bit 0 of GMPXST (Device A Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 05h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device A X-Axis Position Counter High Byte							
Reset	0	0	0	0	0	0	0	0

5.3.8 Game Device A Y-Axis Position Low Byte (GMPAYL)

Reading this register returns the value of the low byte of the Y-axis position counter of game Device A. Before reading this register verify that bit 1 of GMPXST (Device A Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 06h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device A Y-Axis Position Counter Low Byte							
Reset	0	0	0	0	0	0	0	0

5.3.9 Game Device A Y-Axis Position High Byte (GMPAYH)

Reading this register returns the value of the high byte of the Y-axis position counter of game Device A. Read this register after reading the GMPAYL register and verifying that bit 1 of GMPXST (Device A Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 07h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device A Y-Axis Position Counter High Byte							
Reset	0	0	0	0	0	0	0	0

5.0 Game Port (GMP) (Continued)

5.3.10 Game Device B X-Axis Position Low Byte (GMPBXL)

Reading this register returns the value of the low byte of the X-axis position counter of game Device B. Before reading this register verify that bit 2 of GMPXST (Device B Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 08h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device B X-Axis Position Counter Low Byte							
Reset	0	0	0	0	0	0	0	0

5.3.11 Game Device B X-Axis Position High Byte (GMPBXH)

Reading this register returns the value of the high byte of the X-axis position counter of game Device B. Before reading this register verify that bit 2 of GMPXST (Device B Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location: Offset 09h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device B X-Axis Position Counter High Byte							
Reset	0	0	0	0	0	0	0	0

5.3.12 Game Device B Y-Axis Position Low Byte (GMPBYL)

Reading this register returns the value of the low byte of the Y-axis position counter of game Device B. Before reading this register verify that bit 3 of GMPXST (Device B Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location:Offset 0Ah

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device B Y-Axis Position Counter Low Byte							
Reset	0	0	0	0	0	0	0	0

5.3.13 Game Device B Y-Axis Position High Byte (GMPBYH)

Reading this register returns the value of the high byte of the Y-axis position counter of game Device B. Before reading this register verify that bit 3 of GMPXST (Device B Position Counter Ready) is set to 1. Writing to the offset of this register is ignored.

This register is functional only in Enhanced mode.

Location:Offset 0Bh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	Device B Y-Axis Position Counter High Byte							
Reset	0	0	0	0	0	0	0	0

5.0 Game Port (GMP) (Continued)

5.3.14 Game Port Event Polarity Register (GMPEPOL)

This register defines the polarity of button events on which the Game Port issues an interrupt request.

This register is functional only in Enhanced mode.

Location: Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Device B Button 1 Event Polarity**		**Device B Button 0 Event Polarity**		**Device A Button 1 Event Polarity**		**Device A Button 0 Event Polarity**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Device B Button 1 Event Polarity.** This bit defines the event polarity on which Device B Button 1 issues an interrupt request. **Bits** **7 6 Number** 0 0 None (default) 0 1 Rising edge 1 0 Falling edge 1 1 Rising and falling edge
5-4	**Device B Button 0 Event Polarity.** Same as bits 7-6 of this register, but for Device B Button 0. **Bits** **5 4 Number** 0 0 None (default) 0 1 Rising edge 1 0 Falling edge 1 1 Rising and falling edge
3-2	**Device A Button 1 Event Polarity.** Same as bits 7-6 of this register, but for Device A Button 1. **Bits** **3 2 Number** 0 0 None (default) 0 1 Rising edge 1 0 Falling edge 1 1 Rising and falling edge
1-0	**Device A Button 0 Event Polarity.** Same as bits 7-6 of this register, but for Device A Button 0. **Bits** **1 0 Number** 0 0 None (default) 0 1 Rising edge 1 0 Falling edge 1 1 Rising and falling edge

5.0 Game Port (GMP) (Continued)

5.4 GAME PORT BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	GMPCTL	Device B Button 1 Debounce Enable	Device B Button 0 Debounce Enable	Device A Button 1 Debounce Enable	Device A Button 0 Debounce Enable	Reserved	Device B Pre-Scale Enable	Device A Pre-Scale Enable	GMP Enhanced Mode Enable
01h	GMPLST	Device B Button 1 Pin Status	Device B Button 0 Pin Status	Device A Button 1 Pin Status	Device A Button 0 Pin Status	Device B Y-Axis Pin Status	Device B X-Axis Pin Status	Device A Y-Axis Pin Status	Device A X-Axis Pin Status
02h	GMPXST	Device B Button 1 Event Status	Device B Button 0 Event Status	Device A Button 1 Event Status	Device A Button 0 Event Status	Device B Y-Position Counter Ready	Device B X-Position Counter Ready	Device A Y-Position Counter Ready	Device A X-Position Counter Ready
03h	GMPIEN	Device B Button 1 IRQ Enable	Device B Button 0 IRQ Enable	Device A Button 1 IRQ Enable	Device A Button 0 IRQ Enable	Reserved	Position IRQ Event Definition	Device B Position IRQ Enable	Device A Position IRQ Enable
04h	GMPAXL	Device A X-Axis Position Counter Low Byte							
05h	GMPAXH	Device A X-Axis Position Counter High Byte							
06h	GMPAYL	Device A Y-Axis Position Counter Low Byte							
07h	GMPAYH	Device A Y-Axis Position Counter High Byte							
08h	GMPBXL	Device B X-Axis Position Counter Low Byte							
09h	GMPBXH	Device B X-Axis Position Counter High Byte							
0Ah	GMPBYL	Device B Y-Axis Position Counter Low Byte							
0Bh	GMPBYH	Device B Y-Axis Position Counter High Byte							
0Ch	GMPEPOL	Device B Button 1 Event Polarity		Device B Button 0 Event Polarity		Device A Button 1 Event Polarity		Device A Button 0 Event Polarity	

6.0   Musical Instrument Digital Interface (MIDI) Port

Note: This section applies to the PC87393 and PC87393F only.

6.1   OVERVIEW

This chapter describes a generic MIDI Port. For the implementation used in this device, see the *Device Architecture and Configuration* chapter.

The MIDI Port is an asynchronous receiver/transmitter that uses a two-wire, bi-directional, relatively slow communication channel to transmit and receive data bytes to or from MIDI-compliant devices, according to a predefined communication protocol. The MIDI Port is compatible with MPU-401 UART mode.

The MIDI was originally defined to establish a standard interface between computers and digital musical instruments such as synthesizers, and has become the de facto standard for this purpose. However, the MIDI is also commonly used for other purposes, such as communicating with advanced game devices.

The MIDI Port serves as a communication pipe between software and a MIDI device. The software and the MIDI device must interpret the data they exchange, and act accordingly.

The MIDI Port supports the following two feature types:

- Legacy (MPU-401)

- Enhanced.

Legacy. These include all features supported by MPU-401 UART mode. They can all be operated via the Legacy I/O address space of 2 bytes, traditionally allocated for the MIDI Port.

Enhanced. These features extend the capabilities of the MIDI Port. They can only be operated if the MIDI is allocated with an address space of at least 3 bytes.

The basic system configuration of the MIDI Port consists of the port itself, a single pull-up resistor for the MDRX pin, and a MIDI compliant device. This system configuration is shown in Figure 17. The purpose of the pull-up resistor is to make sure that the MIDI Port senses an inactive (high) MIDI receive signal in the absence of a MIDI device.
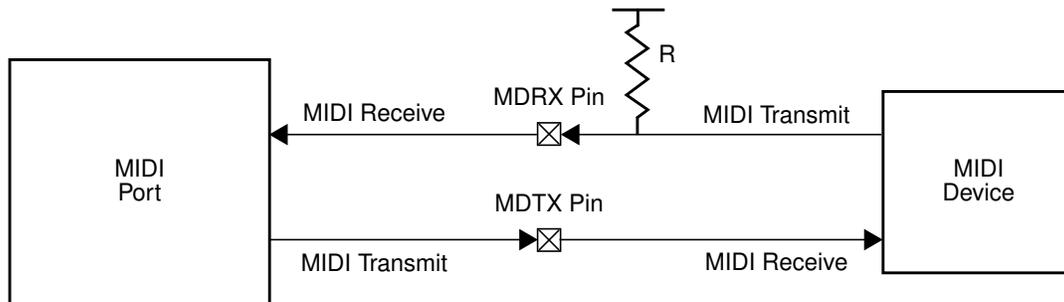
Figure 17. MIDI System Configuration

6.2   FUNCTIONAL DESCRIPTION

The MIDI Port consists of five major functional blocks:

- Internal Bus Interface Unit

- Port Control and Status Registers

- Data Buffers and FIFOs

- MIDI Communication Engine

- MIDI Signals Routing Control Logic.

See Figure 18 for a block diagram of the MIDI Port.

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)
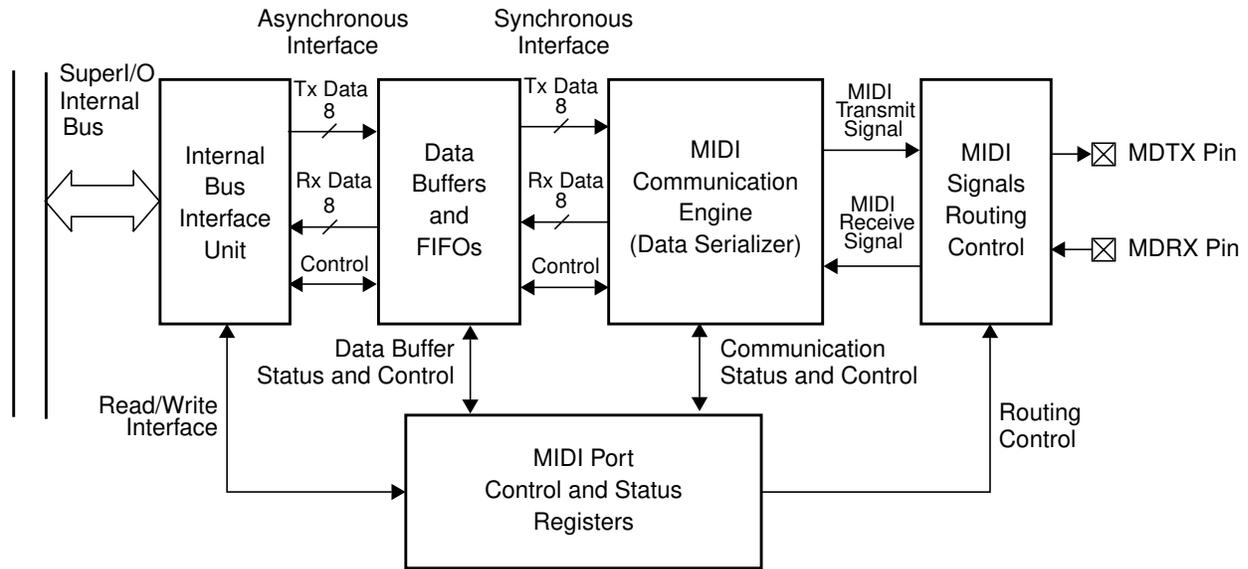
Figure 18. MIDI Port Block Diagram

6.2.1 Internal Bus Interface Unit

The Internal Bus Interface Unit handles all read and write transactions between the host and the registers of the MIDI Port. It also controls the MIDI Port interrupt request logic (see Section 6.2.8).

6.2.2 Port Control and Status Registers

A Control register (MCNTL, see Section 6.3.6) and a Status register (MSTAT, see Section 6.3.4) allow the user to control the operation of the MIDI, and provide status information regarding its various functional units. A Command register (MCOM, see Section 6.3.5) allows the user to control the operation mode of the MIDI Port by serving as a port via which the host can issue commands to the MIDI. A MIDI Port command is defined as a write access to the MIDI Command register. The meaning of each command is determined by the data byte written during this write access.

6.2.3 Data Buffers and FIFOs

The Data Buffers and FIFOs function as a mechanism for synchronizing between the Internal Bus Interface Unit and the MIDI Communication Engine. This synchronization allows each of these units to handle its own tasks without having to pause to send/receive data to/from the other unit. Synchronization also bridges the gap in the data transfer rate between these two units. Data transfer rate matching is done when the FIFOs of the MIDI Port are enabled. It allows the MIDI Port to interface a bus at a relatively high data transfer rate, while maintaining communication with a MIDI device over a communication channel that supports a relatively low data transfer rate.

6.2.4 MIDI Communication Engine

The MIDI Communication Engine handles the serializing of outgoing data and the de-serializing of incoming data transferred between the MIDI Port and the MIDI device. During transmit (serial data transfer from the MIDI Port to the MIDI device), the Communication Engine receives data bytes from the output data buffer or FIFO, serializes them into a stream of data bits, and transmits them as a sequence of high and low pulses over the MDTX pin according to the MIDI communication protocol. During receive (serial data transfer from the MIDI device to the MIDI Port), the Communication Engine receives a sequence of high and low pulses via the MDRX pin, converts them into a stream of data bits and de-serializes them into data bytes that it sends to the input data buffer or FIFO.

Both transmit and receive are performed at a fixed serial data rate of 31.25 Kbits per second. The serial data format is also fixed, and consists of 1 Start bit, 8 Data bits and 1 Stop bit. See the waveform illustrating a MIDI byte transfer in Figure 19.

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)
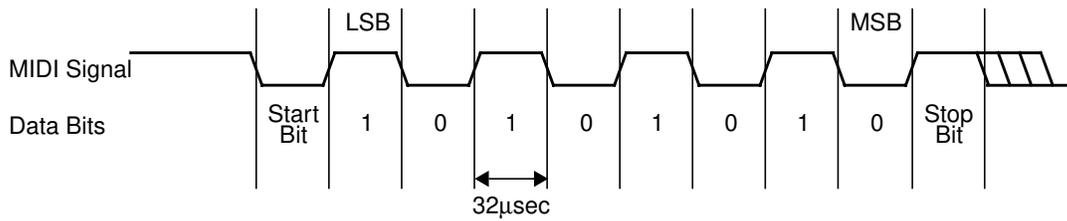
Figure 19. MIDI Byte Transfer Waveform

6.2.5   MIDI Signals Routing Control Logic

The MIDI Signals Routing Control Logic controls the various routing options available for the MIDI transmit and receive signals. It is controlled by the MIDI Control register (MCNTL, see Section 6.3.6). These routing options are not part of the Legacy definition of the MIDI Port.

6.2.6   Operation Modes

The MIDI Port can be operated in one of the following modes:

- Pass-Thru (Non-UART) Mode (default)
- UART Mode.

Pass-Thru (Non-UART) Mode

After a hardware reset, the MIDI Port is in Pass-Thru mode.

In this mode, transmission is disabled by default, and all writes to the MIDI Data Out register (MDO, see Section 6.3.3) are ignored. Transmission in this mode may be enabled by setting bit 4 of the MIDI Control register (MCNTL, see Section 6.3.6).

Receive in Pass-Thru mode is enabled, and a 16-byte Receive FIFO is available. Reading the MIDI Data In register (MDI, see Section 6.3.2) in this mode returns the oldest data stored in the Receive FIFO. If serial data is received while the Receive FIFO is full with data that has not yet been read, the last received data is lost, thus maintaining the data that was previously stored in the Receive Buffer.

When in Pass-Thru mode, the MIDI Port responds to commands issued by the host, as follows:

- 3Fh puts the MIDI Port in UART mode. Also, in response to this command, the MIDI Port puts an acknowledge byte of FEh in the Receive Buffer.
- A0h-A7h or ABh causes the MIDI Port to put an acknowledge byte of FEh followed by a data byte of 00h in the Receive Buffer.
- ACh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 15h, in the Receive Buffer.
- ADh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 01h, in the Receive Buffer.
- AFh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 64h, in the Receive Buffer.
- FFh resets the MIDI Port to its initial state, including all the bits of the MSTAT register. In response, the MIDI Port puts an acknowledge of FEh in the Receive Buffer. This command is usually referred to as the MIDI Reset Command.
- The MIDI Port responds to all other commands by putting an acknowledge byte of FEh in the Receive Buffer.

Putting the acknowledge byte of FEh is equivalent to receiving a data byte. Therefore, once an acknowledge byte is put in the Receive Buffer, it causes the Receive Buffer Empty status flag (see Section 6.2.7) to be cleared, which may also cause a MIDI Port interrupt request to be issued.

When the Receive FIFO is disabled, switching from Pass-Thru mode to UART mode causes data stored in the Receive Buffer to be lost. After switching to UART mode, the MIDI Port is blocked for receive until the acknowledge byte is read from the Receive Buffer.

If a command is issued to the MIDI Port while the MIDI Communication Engine is in the middle of a byte transfer (the Start bit has been transmitted or received), the execution of the command and the response are postponed until the ongoing byte transfer is completed.

After each MIDI Port operation in Pass-Thru mode, the MIDI Status register (MSTAT, see Section 6.3.4) is updated accordingly.

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

UART Mode

Entering UART mode is done by software, by giving the MIDI Port command of 3Fh. Once in UART mode, both transmit and receive are enabled. In addition, the two 16-byte Receive and Transmit FIFOs are automatically enabled.

In UART mode, data written to the MDO register is placed in the Transmit FIFO, from which it is taken by the MIDI Communication Engine and transmitted via the MDTX pin to the MIDI device. Likewise, whenever the Transmit FIFO is not empty, the next byte is taken out by the Communication Engine and transmitted via the MDTX pin to the MIDI device.

Whenever serial data is received by the Communication Engine via the MDRX pin, it is de-serialized and put in the Receive FIFO. Reading the MDI register returns the next byte in the Receive FIFO. The MDI register should not be read while the Receive FIFO is empty. If serial data is received while the Receive FIFO is full, this data is lost and not stored in the Receive FIFO, thus keeping the data that was previously stored in the Receive FIFO.

When in UART mode, the MIDI Port responds to commands given by the host as follows:

- A command of FFh returns the MIDI Port to Pass-Thru mode, and resets it to its initial state.

- All other commands, issued while the MIDI Port is in UART mode, are ignored.

When switching from UART mode to Pass-Thru mode, any data previously stored in the Receive FIFO is lost, unless the FIFO is enabled for Pass-Thru mode.

As in Pass-Thru mode, if a command is issued to the MIDI Port while the MIDI Communication Engine is in the middle of a byte transfer, the execution of the command and the response are postponed until the ongoing byte transfer is completed.

The MIDI commands supported by the MIDI Port and their respective responses are listed in Table 31.

After each MIDI Port operation in UART mode, the MSTAT register is updated accordingly.

Table 31. MIDI Commands Supported by the MIDI Port

Command	MIDI Port Response	
	Pass-Thru Mode	**UART Mode**
3Fh	Enter UART mode FEh (Acknowledge)	Ignored
A0h-A7h, ABh	FEh (Acknowledge) 00h	Ignored
ACh	FEh (Acknowledge) 15h	Ignored
ADh	FEh (Acknowledge) 01h	Ignored
AFh	FEh (Acknowledge) 64h	Ignored
FFh	MIDI Port Reset FEh (Acknowledge)	Enter Pass-Thru Mode MIDI Port Reset
Others	FEh (Acknowledge)	Ignored

6.2.7   MIDI Port Status Flags

The status of the various functional units of the MIDI Port is reflected by the MSTAT register. This register is functional in both Pass-Thru and UART modes. Some of the status indications provided by the MSTAT register are not included in the Legacy definition of the MIDI Port. These indications can be ignored, if not required by the software.

The following status flags are included in the Legacy definition of the MIDI Port:

- Receive Buffer Empty

- Transmit Buffer Full

The Receive Buffer Empty flag is reflected by bit 7 of the MSTAT register. The Transmit Buffer Full flag is reflected by bit 6 of the MSTAT register. When operating in UART mode, these bits reflect the status of the Receive and Transmit FIFOs.

The Receive Buffer Empty status flag is cleared to 0 also when an acknowledge byte is put by the MIDI Port itself following a MIDI command.

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

The values of these bits are set by the MIDI Port hardware and are not affected by reading the MSTAT register.

The following status indications are provided by the MIDI Port, although they are not included in the Legacy definition of the MIDI Port:

- Receive FIFO Full
- Transmit FIFO Empty
- Receive Overrun Error
- MIDI Port Operation Mode

The Receive FIFO Full and Transmit FIFO Empty status flags are reflected by MSTAT register bits 5 and 2, respectively. These bits are updated only when the MIDI Port operates in UART mode or when in Pass-Thru mode with the Receive FIFO enabled. Otherwise, these bits are constantly cleared. The values of these bits are set by the MIDI Port hardware and are not affected by reading the MSTAT register.

The Receive Overrun Error flag indicates that serial data has been received by the MIDI Communication Engine while the Receive Buffer of FIFO was full. This flag is reflected by bit 3 of the MSTAT register. It is updated in both Pass-Thru and UART modes. When a Receive Overrun Event occurs, the data in the Receive Buffer/FIFO is kept and all incoming data is lost. Incoming data will keep getting lost until there is room in the Receive Buffer/FIFO to accept it. The Receive Overrun Error status flag is cleared when the MSTAT register is read.

The MIDI Port Operation Mode flag indicates whether the MIDI Port currently operates in Pass-Thru or UART mode. This status flag is reflected by bit 4 of the MSTAT register. It can be used by software to keep track of the currently selected MIDI Port operation mode.

6.2.8   MIDI Port Interrupts

The MIDI Port supports interrupt assertion in both Pass-Thru and UART modes, in response to one of the following events, or both:

- Receive Data Ready
- Transmit Buffer Empty

The Receive Data Ready event refers to the case in which there is data to be read in the Receive Buffer/FIFO. An interrupt request is asserted by the MIDI Port to indicate a Receive Data Ready event in one of the following cases:

- The MIDI Port is in Pass-Thru mode, and the Receive Buffer contains a data or acknowledge byte which has not been read yet. In this case, the interrupt request is deasserted once the Receive Buffer is read.

- The MIDI Port is in UART mode, and the Receive FIFO contains eight, or more, data bytes which have not been read yet, or it is in Pass-Thru mode with the Receive FIFO enabled. In this case, the interrupt request is deasserted once the Receive FIFO level drops below eight bytes.

- The MIDI Port is in UART mode, the Receive FIFO contains less than eight data bytes which have not been read yet, and no data was received by the Communication Engine, the MIDI Port is in Pass-Thru mode with the Receive FIFO enabled, or a read occurs from the Receive FIFO during a timeout period of approximately 1.28 msec (the time it takes to transfer 4 bytes over the MIDI communication channel). In this case, the interrupt request is deasserted when either new data is received by the Communication Engine, or data is read from the Receive FIFO.

The Transmit Buffer Empty event refers to the case in which the Transmit Buffer/FIFO of the MIDI Port can still accept data to transmit. An interrupt request is asserted by the MIDI Port to indicate a Transmit Buffer Empty event in one of the following cases:

- The MIDI Port is in Pass-Thru mode, and the Transmit Buffer is empty. In this case, the interrupt request is deasserted once a byte is written to the Transmit Buffer.

- The MIDI Port is in UART mode, and the Transmit FIFO is empty. In this case, the interrupt request is deasserted once the Transmit FIFO is filled with at least 3 bytes.

After hardware reset, interrupts are asserted by the MIDI Port only in response to a Receive Data Ready event. Interrupt assertion in response to Transmit Buffer Empty events can be enabled by setting writing 1 to bit 1 of the MCNTL register. Interrupt assertion in response to Receive Data Ready events can be disabled by writing 0 to bit 3 of the MCNTL register.

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

6.2.9 Enhanced MIDI Port Features

The MIDI Port supports the following modes/operations, which are not part of the Legacy definition of the MIDI Port:

- Transmit in Pass-Thru
- Loopback mode
- MIDI Thru
- MDTX pin masking

Transmit in Pass-Thru. When the MIDI Port is operated in Pass-Thru mode, transmit is disabled by default. To enable it, write 1 to bit 4 of the MCNTL register.

Loopback Mode. The MIDI serial data transmit signal is routed internally to the MIDI serial data receive signal. This causes all the data transmitted by the MIDI Port to also be received. Loopback mode can be used as a mode for testing the MIDI Port or its software. To enable it, write 1 to bit 7 of the MCNTL register.

MIDI Thru. The MIDI serial data receive signal is routed internally to the MIDI serial data transmit signal. This causes any incoming stream of pulses received via the MDRX pin to be driven immediately on the MDTX pin. This feature allows the MIDI Port to be connected as a link in a chain of several MIDI devices. In parallel to routing the MIDI receive signal to the MIDI transmit signals, the incoming serial data is also received by the MIDI Port itself. To enable it, write 1 to bit 6 of the MCNTL register.

MDTX Pin Masking. MDTX pin masking forces this pin to remain at a high level. This causes all transmit processes to occur without physically driving the serial data via the MDTX pin. Writing 1 to bit 2 of the MCNTL register enables MDTX pin masking.

The above three features are handled by the MIDI Signals Routing Control Logic, which is illustrated in Figure 20.
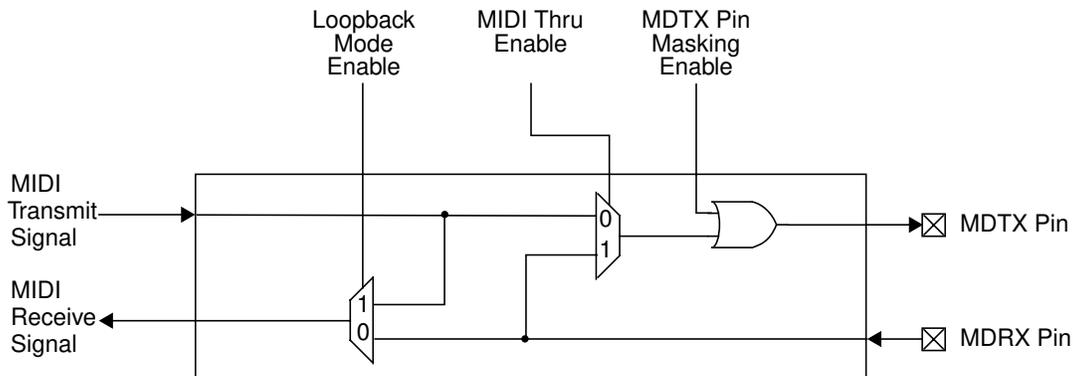
Figure 20. MIDI Signals Routing Control Logic

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

6.3 MIDI PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write

- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.

- W = Write

- RO = Read Only

- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

6.3.1 MIDI Port Register Map

The following table lists the MIDI Port registers. For the MIDI Port register bitmap, see Section 6.4.

Offset	Mnemonic	Register Name	Type	Section
00h	MDI	MIDI Data In	R	6.3.2
00h	MDO	MIDI Data Out	W	6.3.3
01h	MSTAT	MIDI Status	R	6.3.4
01h	MCOM	MIDI Command	W	6.3.5
02h	MCNTL	MIDI Control	R/W	6.3.6

6.3.2 MIDI Data In Register (MDI)

This read register is used for reading data received by the MIDI Port, and status information returned by the MIDI Port in response to a previously issued command. When the FIFOs of the MIDI Port are enabled, reading from this offset returns the next byte taken out of the Receive FIFO.

Location: Offset 00h

Type: R

Bit	7	6	5	4	3	2	1	0
Name	Data In							
Reset	X	X	X	X	X	X	X	X

6.3.3 MIDI Data Out Register (MDO)

This write register is used for writing data to be transmitted by the MIDI Port. When the FIFOs of the MIDI Port are enabled, writing to this offset puts the data byte into the Transmit FIFO.

Location: Offset 00h

Type: W

Bit	7	6	5	4	3	2	1	0
Name	Data Out							
Reset	X	X	X	X	X	X	X	X

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

6.3.4 MIDI Status Register (MSTAT)

This read register provides status information regarding the functional blocks of the MIDI Port.

Location: Offset 01h

Type: R

Bit	7	6	5	4	3	2	1	0
Name	Rx Buffer Empty	Tx Buffer Full	Rx FIFO Full	MIDI Port Operation Mode	Rx Overrun Error	Tx FIFO Not Empty	Reserved	
Reset	1	0	0	0	0	0	0	0

Bit	Description
7	**Rx Buffer Empty.** When set to 1, it indicates that the Receive Buffer in Pass-Thru mode, or the FIFO in UART mode, is empty. When set to 0, it indicates that the Receive Buffer or FIFO contain data that can be read via the MDI register. 0: Not empty 1: Empty (default)
6	**Tx Buffer Full.** When set to 1, it indicates that the Transmit Buffer or FIFO cannot accept any more data. When set to 0, it indicates that the Transmit Buffer or FIFO can accept more data written to the MDO register. 0: Not full (default) 1: Full
5	**Rx FIFO Full.** When set to 1, it indicates that the Receive FIFO cannot accept any more received data bytes. When set to 0, it indicates that the Receive FIFO can accept more received data bytes. This bit is forced to 0 when the FIFOs are disabled. 0: Not full or disabled (default) 1: Full
4	**MIDI Port Operation Mode.** When set to 1, it indicates that the MIDI Port is currently operating in UART mode. When set to 0, it indicates that the MIDI Port is currently operating in Pass-Thru (non-UART) mode. 0: Pass-Thru mode (default) 1: UART mode
3	**Rx Overrun Error.** This bit is cleared to 0 when the MSTAT register is read. An overrun error is defined as the state in which one or more data bytes have been received by the MIDI Port while the Receive Buffer, or FIFO, was full. 0: No overrun error (default) 1: Overrun error
2	**Tx FIFO Not Empty.** This bit is forced to 0 when the FIFOs are disabled. 0: Empty or disabled (default) 1: Not empty
1-0	**Reserved**

6.3.5 MIDI Command Register (MCOM)

This write register is a port via which commands are issued by the host to the MIDI Port.

Location: Offset 01h

Type: W

Bit	7	6	5	4	3	2	1	0
Name	Command Byte							
Reset	X	X	X	X	X	X	X	X

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

6.3.6 MIDI Control Register (MCNTL)

This register controls enhanced MIDI functions.

Location: Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Loopback Mode Enable	MIDI Thru Enable	Reserved	Pass-Thru Transmit Enable	Rx Data Ready Interrupt Enable	MDTX Pin Masking Enable	Tx Buffer Empty Interrupt Enable	Rx FIFO Enable for Pass-Thru Mode
Reset	0	0	0	0	1	0	0	1
Required			0					

Bit	Description
7	**Loopback Mode Enable**. When enabled, the MIDI receive signal is internally connected to the MIDI transmit signal. 0: Disabled (default) 1: Enabled
6	**MIDI Thru Enable**. When enabled, the MDRX pin is internally connected to the MDTX pin, which then reflects the MIDI receive signal. When disabled, the MDTX pin is driven with data coming from the MIDI Port transmit engine. 0: Disabled (default) 1: Enabled
5	**Reserved.** Must be 0.
4	**Pass-Thru Transmit Enable.** When enabled, data is transmitted in Pass-Thru (non-UART) mode. 0: Disabled (default) 1: Enabled
3	**Rx Data Ready Interrupt Enable.** When enabled, an interrupt request is asserted in response to a Receive Data Ready event. 0: Disabled 1: Enabled (default)
2	**MDTX Pin Masking Enable.** When enabled, the MDTX pin is constantly driven high by the MIDI Port. When disabled, MDTX serves as the MIDI Port transmit line. 0: Disabled (default) 1: Enabled
1	**Tx Buffer Empty Interrupt Enable.** When enabled, an interrupt request is asserted in response to a Transmit Buffer Empty event. 0: Disabled (default) 1: Enabled
0	**Rx FIFO Enable for Pass-Thru Mode**. When this bit is set to 1, the Receive FIFO is enabled in Pass-Thru mode. This bit is ignored in UART mode. 0: Disabled 1: Enabled (default)

6.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

6.4 MIDI PORT BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	MDI	Data In							
00h	MDO	Data Out							
01h	MSTAT	Rx Buffer Empty	Tx Buffer Full	Rx Buffer Full	MIDI Port Operation Mode	Rx Overrun Error	Tx FIFO Empty	Reserved	
01h	MCOM	Command Byte							
02h	MCNTL	Loopback Mode Enable	MIDI Thru Enable	Reserved	Pass-Thru Transmit Enable	Rx Data Ready Interrupt Enable	MDTX Pin Masking Enable	Tx Buffer Empty Interrupt Enable	Rx FIFO Enable for Pass-Thru Mode

7.0 X-Bus Extension

Notes: **This section applies to the PC87393 and PC87393F only.**
            FWH-related descriptions apply to the PC87393F only.

7.1 OVERVIEW

The PC8739x provides an X-Bus extension to the LPC bus to enable the ISA-like interface to external 8-bit peripherals. Decode logic, described in the *Device Architecture and Configuration* chapter, defines the addresses for which the X-Bus generates transactions. These transactions may be in the I/O address space and the memory address space or in the FWH memory address space. Using the X-Bus interface, the PC8739x serves as a bridge for such transactions into the X-Bus. Figure 21 is a schematics block diagram of the X-Bus bridging function. For details on the decoder functions, see the *Device Architecture and Configuration* chapter. All other functions are described in detail in this chapter.
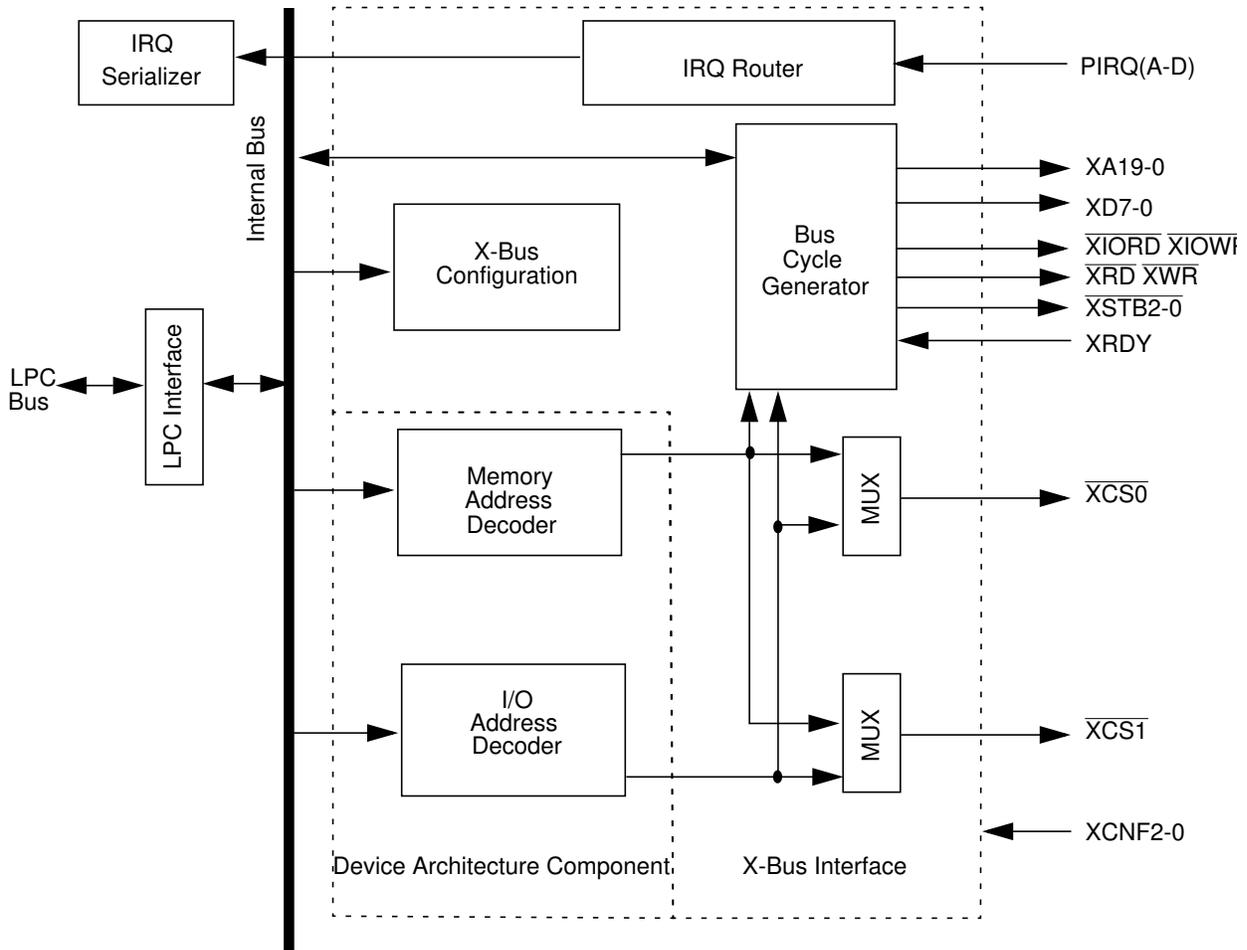
Figure 21. X-Bus Block Diagram

7.2 IRQ ROUTING

The PC8739x supports up to four IRQ inputs, PIRQA through PIRQD. These pins may be used to support legacy devices that are connected on the X-Bus. The PC8739x enables any of these interrupts to be routed to any one of fifteen host IRQs. The IRQ inputs are mapped by X-Bus PIRQA-D Mapping registers at F8h and F9h. XIRQCA through XIRQCD registers enable the user to define the interrupt as active high or low, and to route it to a wake-up event.

7.3 X-BUS TRANSACTIONS

The X-Bus extension supports 8-bit I/O or memory read/write cycles.

The zone mapping of the chip select signals determines how X-Bus read and write cycles correspond to memory and I/O bus cycles. The zone mapping to a select signal, $\overline{XCS1\text{-}0}$, must be enabled regardless of whether the I/O device is using the chip select signal. Signal mapping to a pin may be disabled when the select signal is not required for an off-chip interface.

7.0 X-Bus Extension (Continued)

The X-Bus interface outputs the address in one of two modes:

- Normal Address mode - A pin is assigned for each address line, and a non-multiplexed address data bus is used.

- Latched Address mode - The number of pins used for outputting the address is reduced. The address lines are multiplexed with the data bus. External latches should be used to enable the memory or I/O device access to the multiplexed address signals. When the memory configuration uses more than 1 Mbyte of memory, this mode must be used to generate address signals 20 through 27.

X-Bus access timing is driven by an internal version of the LPC clock (i.e., it has the same frequency but may have some phase delay), referred to in this section simply as "the clock". The transactions are described in reference to the clock, and the AC specifications are relative to it. This provides an easy way for calculating the timing for the system design. However, the system interface is optimized for an asynchronous interface. For hints on how to use it, refer to the usage hints in Section 7.5.

7.3.1 Programmable I/O Range Chip Select

The PC8739x has two chip select signals, $\overline{XCS1\text{-}0}$, to indicate X-Bus accesses. The PC8739x X-Bus functional block enables flexible association of these chip selects with I/O and memory address ranges in the LPC address space. The Chip Select Mapping field of the X-Bus Zone Configuration registers defines to which of the decoded address ranges the respective $\overline{XCS}$ signal responds. In addition, the X-Bus Configuration register enables specifying the access time for the respective select signal via bits that control the fixed wait cycles and variable wait cycles, using the XRDY input.

If the chip select signal setting results in a conflict in which both selects are configured for the same transaction, $\overline{XCS0}$ has priority. $\overline{XCS1}$ remains inactive and its Configuration register setting is ignored. For zones that are not associated with one of the chip select signals, the X-Bus does not respond to LPC transactions.

7.3.2 LPC and FWH Address to X-Bus Address Translation

The BIOS memory on the LPC bus can occupy one of three regions in the memory space (specified in Table 29 and Table 31). Address translation between the LPC bus address and the X-Bus is performed as follows:

I/O Transactions. The 16-bit address of the LPC bus is padded with zeroes (bits 16 through 27) to create the 28-bit input address to the X-Bus functional block.

Memory Transactions. The 32-bit address received from the LPC bus is used to decode the different zones described in Section 2.19. The address is then translated to the X-Bus address using the following rules:

- User-Defined Zone (UDZ) and 386 Mode-Compatible BIOS Range (LPC or LPC-FWH) - The 28 least significant bits of the LPC address are used as the X-Bus input address. Figure 22 illustrates the mapping for this zone. (Note: See Section 2.8.1 for the way addresses are built for FWH transactions.)

- Legacy and Extended Legacy BIOS Range - The 17 least significant bits (A16-0) of the LPC address are routed as the 17 least significant signals address lines of the X-Bus (XA16-0). The upper 11 X-Bus address lines are driven to 1. This shifts the addresses to the end of the X-Bus memory space (see Figure 23).
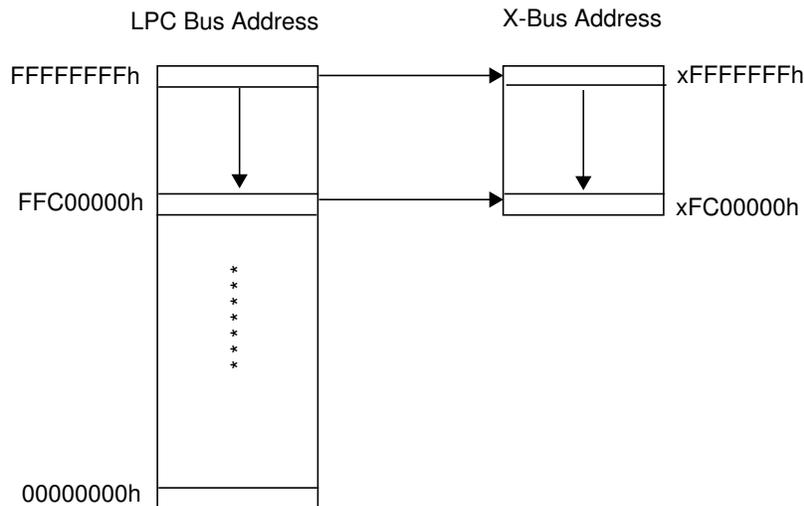
Figure 22. LPC to X-Bus Address Translation: 386 Mode-Compatible BIOS Range

7.0 X-Bus Extension (Continued)

```
        LPC Bus Address                                    X-Bus Address

FFFFFFFFh  ┌──────────┐                          ┌──────────┐  xFFFFFFFh
           │          │                          │          │
000FFFFFFh ├──────────┤                          │          │
           │  Legacy  │                          │          │
           │  BIOS    │                          │          │
000F0000h  ├──────────┤                          └──────────┘  xFFE0000h
000EFFFFh  ├──────────┤
           │ Extended │
           │ Legacy   │
           │ BIOS     │
000E0000h  ├──────────┤
           │    *     │
           │    *     │
           │    *     │
           │    *     │
           │    *     │
00000000h  └──────────┘
```
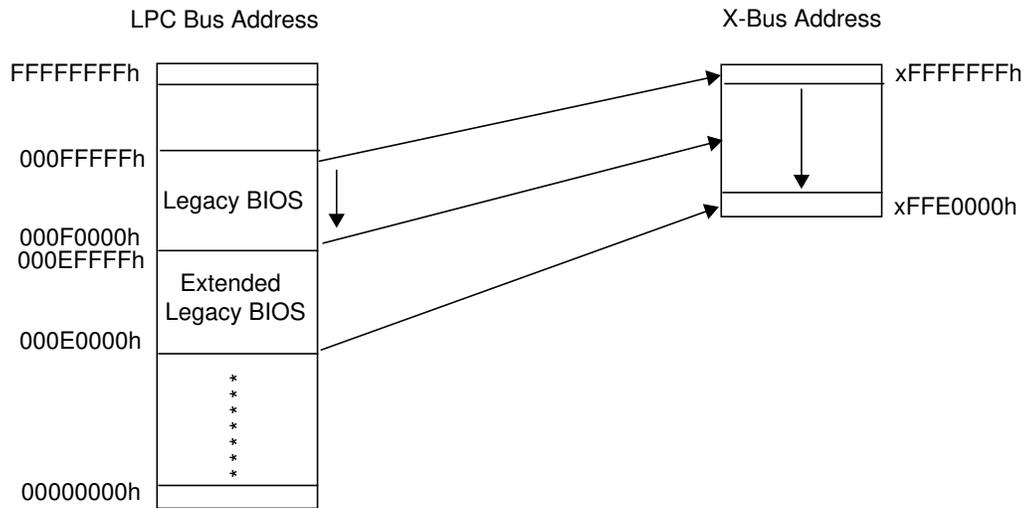
Figure 23. LPC to X-Bus Address Translation: Legacy and Extended Legacy BIOS Ranges

7.3.3   Extended Read/Write Signal Mode

This mode is essential for devices that have separate read and write signals for memory transactions and for I/O transactions. While in this mode, the PC8739x routes I/O read and write signals to $\overline{XIORD}$ and $\overline{XIOWR}$ pins, and memory or FWH read and write signals to $\overline{XRD}$ and $\overline{XWR}$.

If the PC8739x is set to wake-up with the X-Bus signals configured to output pins (using strap pins XCNF2-0), the extended mode is disabled, and must be re-enabled by the user.

7.3.4   Indirect Memory Read and Write Transaction

I/O mapped registers may be used through an LPC I/O transaction to perform an X-Bus memory transaction. This mechanism uses the following X-Bus module registers:

- Four Indirect Memory Address registers, XIMA3-XIMA0, representing address bits 31 to 0

- One Indirect Memory Data register (XIMD), representing data bits 7 to 0

- Two enable bits, one for each Select Configuration register, XZCNF0[5] and XZCNF1[5].

Following a write to the XIMD register, a memory write cycle appears on the X-Bus using the addresses and data from the XIMA3-XIMA0 and XIMD registers. Following a read from the XIMD register, a memory read cycle appears on the X-Bus using the addresses from these same registers. The returned data from the X-Bus cycle is used to finish the LPC I/O read cycle from XIMD register.

The read or write cycles appear only if one of the Indirect Memory Cycle Enable bits (XZCNF0[5] or XZCNF1[5]) is set. If both of these bits are set, select 1 is ignored and the transaction takes place according to select 0 settings. All X-Bus cycle configurations are the same as defined in the X-Bus Select Configuration registers (XZCNF0 and XZCNF1).

7.3.5   Normal Address Mode X-Bus Transactions

The read and write transactions in Normal address mode are similar to those used in the X-Bus or ISA bus. At least two idle cycles are inserted at the end of each X-Bus transaction cycle (there may be more idle cycles due to the LPC transactions).

Once a read cycle on the LPC falls within the range of any of the enabled decoded address ranges of the X-Bus functional block, a read cycle begins. A read cycle (Figure 24) starts by outputting the address signals on address signals XA19-0 on the rising edge of the clock. During this time, the PC8739x does not drive the data bus signals XD7-0. One LPC clock cycle later, a chip select signal $\overline{XCS1}$ or $\overline{0}$ is asserted, based on the address accessed and the select signal mapping. Three clock cycles later, on the next rising edge of the clock, the $\overline{XRD}$ signal is asserted (set to 0) indicating that this is a read cycle and enabling the device being accessed to drive the data bus within 16 clock cycles plus the internally programmed wait state period. If XRDY use is enabled for this zone, XRDY input value is then checked on the rising edge of the clock, and the transaction is extended until XRDY is detected to be high. Four clock cycles later, the input data XD7-0 is sampled on the rising edge of the clock. One LPC clock cycle later, $\overline{XRD}$ is de-asserted (set to 1) and one clock cycle later, the transaction is completed by de-asserting $\overline{XCS1-0}$. The address is retained for the duration of two more cycles, after which the address lines change their values to 0.

7.0 X-Bus Extension (Continued)

Once a write cycle on the LPC falls within the range of any of the enabled decoded address ranges of the X-Bus functional block, a write cycle begins. A write cycle (Figure 25) starts by outputting the address signals on address signals XA19-0, and the data signals on data pins XD7-0, on the rising edge of the clock. One LPC clock cycle later, a chip select signals $\overline{XCS1}$ or $\overline{0}$ is asserted, based on the address accessed and the select signal mapping. Three clock cycles later, on the next rising edge of the clock, the $\overline{XWR}$ signal is asserted (set to 0) indicating that this is a write cycle and enabling the device to be written for 16 clock cycles plus the internally programmed wait state period. If XRDY use is enabled for this zone, XRDY input value is then checked on the rising edge of the clock, and the transaction is extended until XRDY is detected to be high. Five LPC clock cycles later, $\overline{XWR}$ is de-asserted (set to 1) and one clock cycle later, the transaction is completed by de-asserting $\overline{XCS1\text{-}0}$. Two clock cycle later, the address lines change their values to 0.

Insert 12+"Programmed Wait States" of 33 MHz clocks here.
All non-clock signals remain the same during this inserted time.
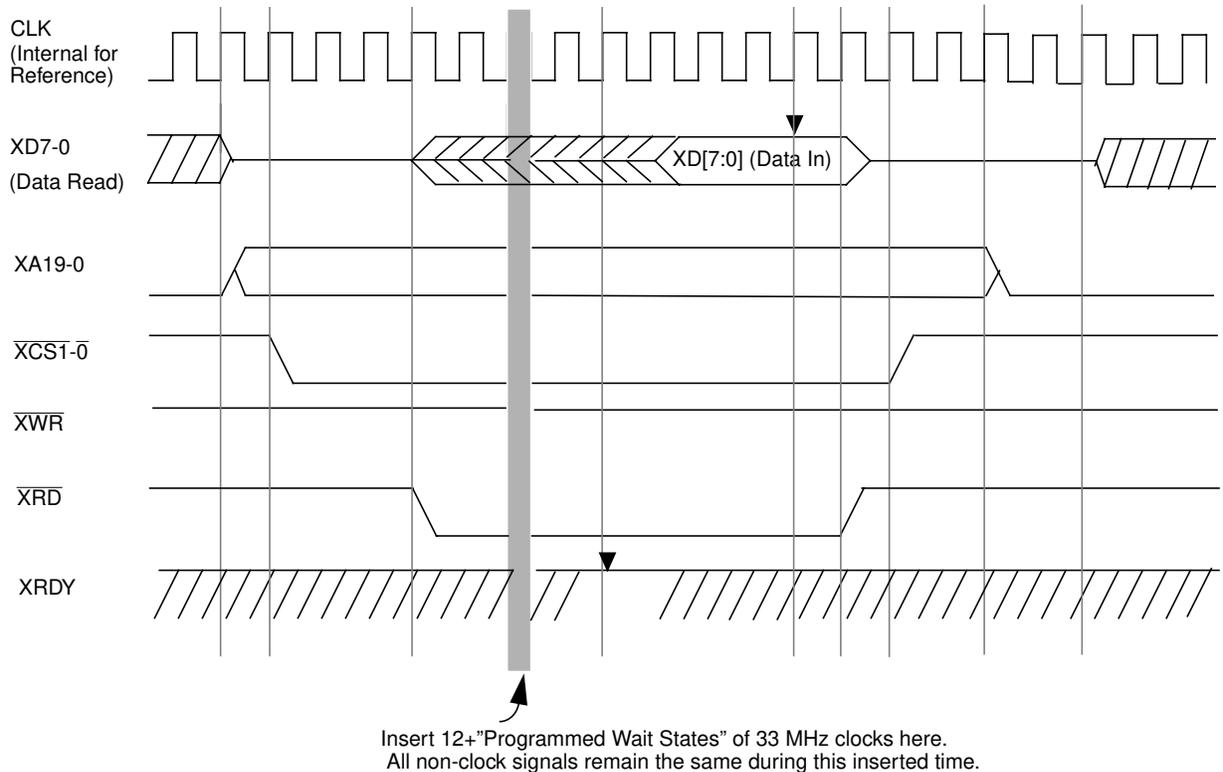
Figure 24. Read Access Cycle - Normal Address Mode

7.0 X-Bus Extension (Continued)

Insert 12+"Programmed Wait States" of 33 MHz clocks here.
All non-clock signals remain the same during this inserted time.
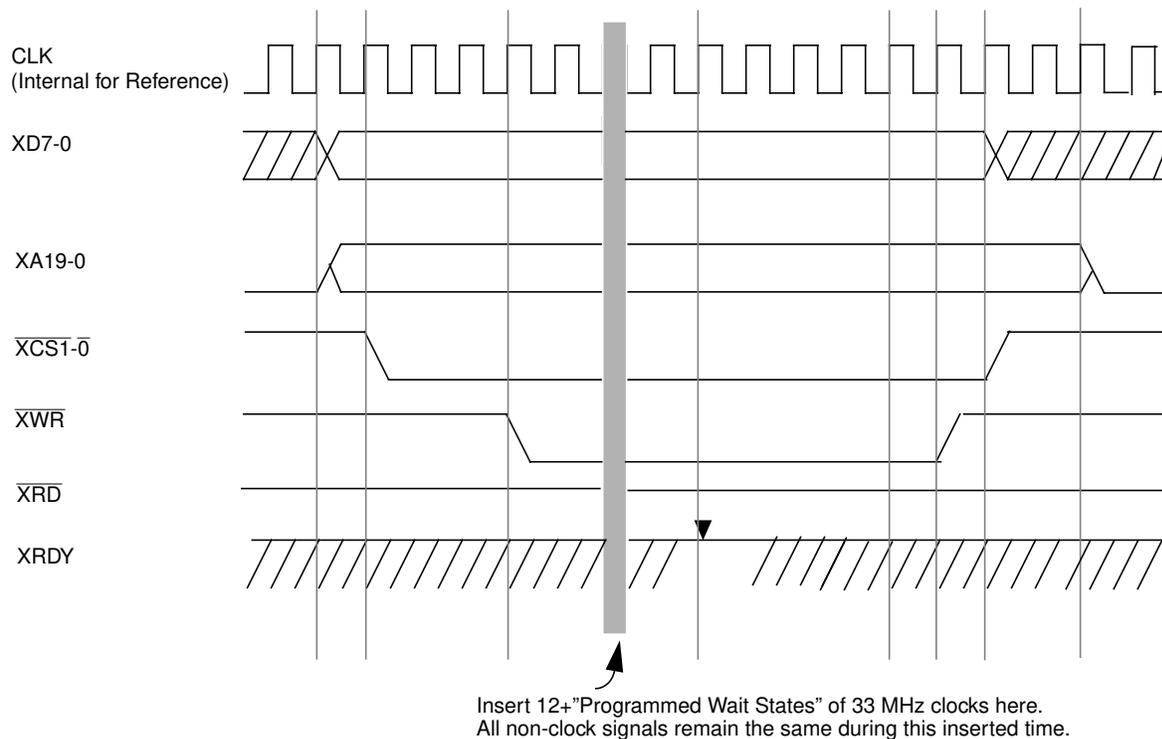
Figure 25. Write Access Cycle - Normal Address Mode

7.3.6 Latched Address Mode X-Bus Transactions

The read and write transactions in Latched address mode are similar to those used in Normal address mode, except for how the addresses are placed on the X-Bus. In this mode, address signals 27-0 are output using the XA signals and via multiplexing over the data bus (XD7-0). Latch control signals $\overline{XSTB2\text{-}0}$ help a system capture these signals. The $\overline{XSTB2\text{-}0}$ signals are placed as long as the address signal are valid (until the end of a transaction).

Once a read cycle on the LPC falls within the range of any of the enabled X-Bus decoded address ranges, a read cycle begins. A read cycle starts by outputting the lower twenty address signals on address signals XA19-0, and address signals 27-20 on data signals XD7-0, on the rising edge of the clock. Two clock cycles later, a strobe signal ($\overline{XSTB2}$) is asserted to latch the information on an external latch. Two clock cycles later, a second set of address signals, 19-12, is placed on data pins XD7-0. These may be latched using the strobe signal $\overline{XSTRB1}$ output two cycles later on the rising edge of the clock. Two clock cycles later, the last group of address signals, 11-4, is output on data signals XD7-0. The $\overline{XSTRB0}$ output two cycles later, on the rising edge of the clock, may be used to latch this part of the address. Two cycles later on the rising edge of the clock, the PC8739x stops driving the data bus. At this point, all addresses are available either on the address outputs of the PC8739x (XA19-0) or in one of the three latches. The system may require only part of these addresses, depending on the size of the address memory or peripheral space. One clock cycle later, a chip select signal $\overline{XCS1}$ or $\overline{0}$ is asserted, based on the address accessed and the select signal mapping. From this point, the read continues as described for the Normal address mode. $\overline{XSTRB2\text{-}0}$ are deasserted when the address becomes invalid.

Once a write cycle on the LPC falls within the range of any of the enabled decoded address ranges of the X-Bus functional block, a read cycle is started. A write cycle starts by outputting the lower twenty address signals on address signals XA19-0] and address signals 27- 20 on data signals XD7-0, on the rising edge of the clock. Two clock cycles later, a strobe signal ($\overline{XSTB2}$) is asserted to latch the information on an external latch. Two clock cycles later, a second set of address signals, 19-12, is placed on data pins XD7-0. These may be latched using the strobe signal $\overline{XSTRB1}$ output two cycles later on the rising edge of the clock. Two clock cycles later, the last group of address signals, 11-4, is output on the data signals XD7-0. The $\overline{XSTRB0}$ output, two cycles later on the rising edge of the clock, may be used to latch this part of the address. Two cycles later on the rising edge of the clock, the PC8739x outputs the data signals on data pins XD7-0 on the rising edge of the clock. At this point, all the address is available either on the address outputs of the PC8739x (XA[19:0]) or in one of the three latches. The system may require only part of these addresses, depending on the size of the address memory or peripheral space. One clock cycle later, chip select signal $\overline{XCS1}$ or $\overline{0}$ is asserted, based on the address accessed and the select signal mapping. From this point, the write continues as described for the Normal address mode. $\overline{XSTRB2\text{-}0}$ are deasserted when the address becomes invalid.

7.0 X-Bus Extension (Continued)

CLK
(Internal for Reference)

XD7-0

XSTB2

XSTB1

XSTB0

XA19-0
(Some May Not be
Available Due to Multiplexing)

XA27-0
(Externally Available Address)

XCS

XRD

XWR

XRDY

Transaction Continues as for Normal Address Mode Read
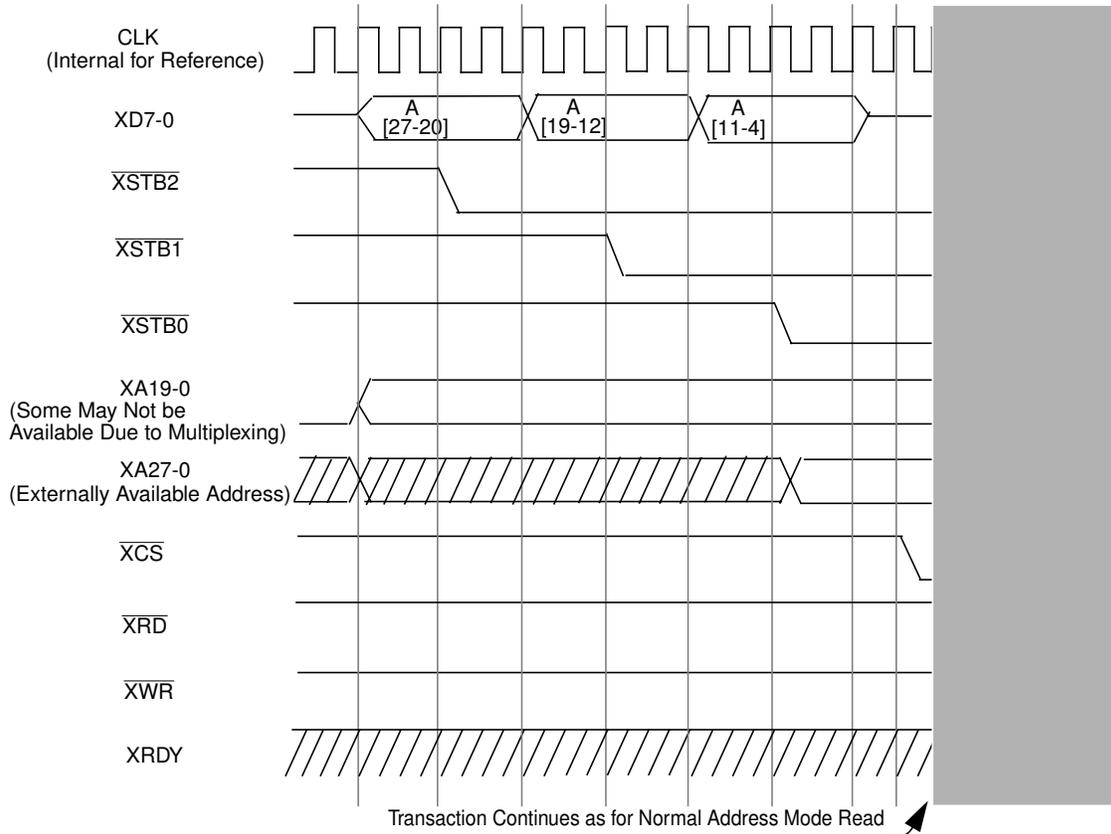
Figure 26. X-Bus Read Access Cycle - Latched Address Mode

CLK
(Internal for Reference)

XD7-0

XSTB2

XSTB1

XSTB0

XA19-0
(Some May Not be
Available Due to Multiplexing)

A27-0
(Externally Available Address)

XCS

XRD

XWR

XRDY

Transaction Continues as for Normal Address Mode Write
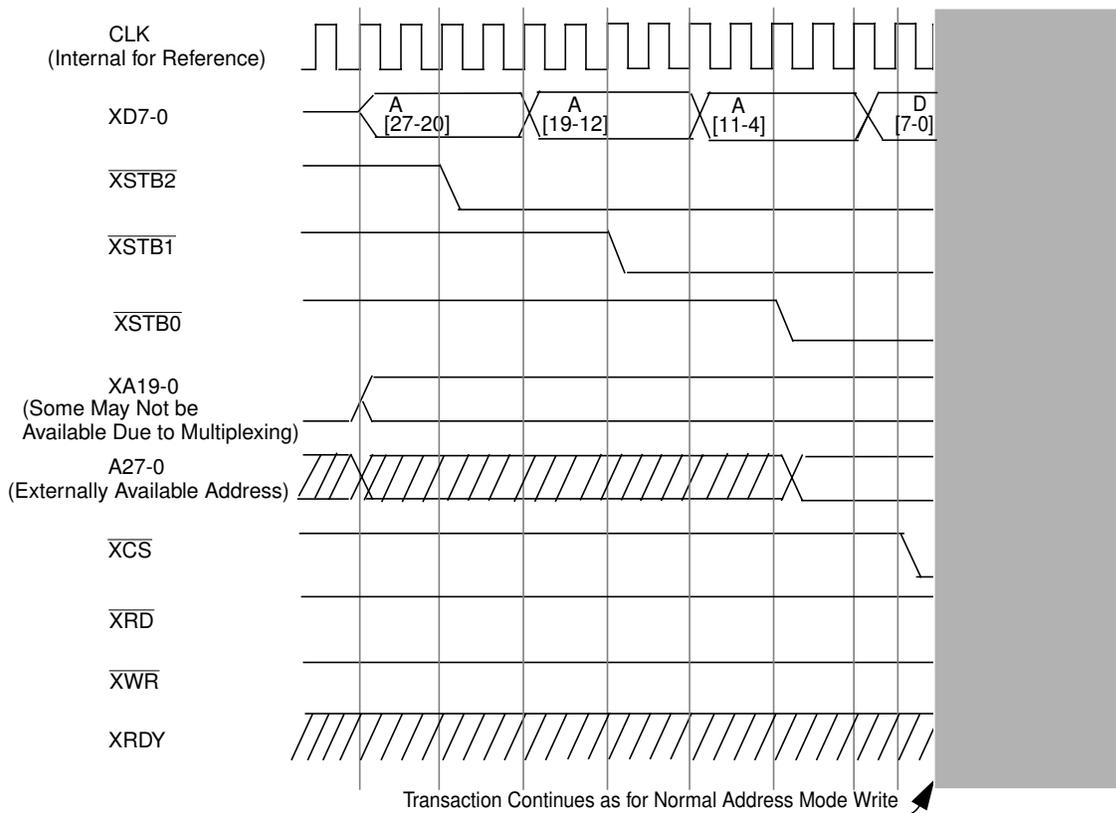
Figure 27. X-Bus Write Access Cycle - Latched Address Mode

7.0 X-Bus Extension (Continued)

7.4 X-BUS CONFIGURATION REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write

- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.

- W = Write

- RO = Read Only

- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

7.4.1 X-Bus Register Map

The following table lists the X-Bus registers.

Offset	Mnemonic	Register Name	Type	Section
00h	XBCNF	X-Bus Configuration	R/W	7.4.2
01h	XZCNF0	X-Bus Select 0 Configuration	R/W	7.4.3
02h	XZCNF1	X-Bus Select 1 Configuration	R/W	7.4.4
03h	Reserved exclusively for National use			
04h	XIRQCA	X-Bus IRQ A Configuration	R/W	7.4.5
05h	XIRQCB	X-Bus IRQ B Configuration	R/W	7.4.5
06h	XIRQCC	X-Bus IRQ C Configuration	R/W	7.4.5
07h	XIRQCD	X-Bus IRQ D Configuration	R/W	7.4.5
08h	XIMA0	X-Bus Indirect Memory Address Register 0	R/W	7.4.6
09h	XIMA1	X-Bus Indirect Memory Address Register 1	R/W	7.4.7
0Ah	XIMA2	X-Bus Indirect Memory Address Register 2	R/W	7.4.8
0Bh	XIMA3	X-Bus Indirect Memory Address Register 3	R/W	7.4.9
0Ch	XIMD	X-Bus Indirect Memory Data Register	R/W	7.4.10

7.4.2 X-Bus Configuration Register (XBCNF)

This register affects the functionality mode of the X-Bus.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved						R/W Extended Mode Enable	Latch Address Mode Enable
Reset	0	0	0	0	0	0	0	Strap

7.0 X-Bus Extension (Continued)

Bit	Description
7-2	**Reserved**
1	**Read/Write Extended Mode Enable.** When set to 1, enables the separation of the I/O read and write transactions from pins XRD & XWR to pins XIORD & XIOWR, leaving the memory and FWH transactions to be routed to XRD and XWR. 0: Disabled (default) 1: Enabled
0	**Latch Address Mode Enabled.** When set to 1, enables three phases of addresses to be latched on the data pins. Reset value of this bit is set by the XCNF2-0 strap inputs. See Section 1.5.11 for the definition of this setting. 0: Disabled 1: Enabled

7.0 X-Bus Extension (Continued)

7.0 X-Bus Extension (Continued)

7.4.3 X-Bus Select 0 Configuration Register (XZCNF0)

This register affects the mapping of modules associated with Chip Select 0, $\overline{XCS0}$.

Location: Offset 01h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	XRDY Enable	Wait States Enable	Indirect Memory Cycle Enable	Select 0 Mapping				
Reset	Strap	1	0	Strap				

Bit	Description
7	**XRDY Enable**. Enables the use of XRDY input for devices mapped to $\overline{XCS0}$. Reset value of this bit is defined by the XCNF2-0 strap inputs. 0: Disabled (default for all XCNF2-0 values, except 010 or 110) 1: Enabled (default if XCNF2-0 is set to 010 or 110)
6	**Wait States Enable** 0: Wait states disabled 1: 8 clock cycles of wait enabled (default)
5	**Indirect Memory Cycle Enable**. Enable indirect memory access mechanism to generate memory transaction on $\overline{XCS0}$. 0: Disabled (default) 1: Enabled
4-0	**Select 0 Mapping** UDIZ = User-Defined I/O Zone - = $\overline{XCS0}$ does not respond to this zone decode + = $\overline{XCS0}$ responds to this zone decode and is influenced by its setting

Bits 4 3 2 1 0	KBC	PM	RTC	TST	UDIZ	BIOS	MEM	
0 0 0 0 0	-	-	-	-	-	-	-	(default if XCNF2-0 No BIOS mode is set)
0 0 0 0 1	-	-	-	-	-	+	-	(default if XCNF2-0 selects any of the BIOS modes)
0 0 0 1 0	+	-	-	-	-	+	-	
0 0 0 1 1	+	+	-	-	-	+	-	
0 0 1 0 0	+	+	+	-	-	+	-	
0 0 1 0 1	+	+	+	+	-	+	-	
0 0 1 1 0	-	-	-	-	+	+	-	
0 0 1 1 1	+	+	+	-	+	+	-	
0 1 0 0 0	+	+	+	+	+	+	-	
0 1 0 0 1	+	-	-	-	-	-	-	
0 1 0 1 0	+	-	-	-	+	-	-	
0 1 0 1 1	+	+	-	-	-	-	-	
0 1 1 0 0	+	+	+	-	-	-	-	
0 1 1 0 1	+	+	+	+	-	-	-	
0 1 1 1 0	-	-	-	-	+	-	-	
0 1 1 1 1	+	+	+	+	+	-	-	
1 0 0 0 0	+	+	+	+	+	-	+	
1 0 0 0 1	+	-	-	-	-	-	+	
1 0 0 1 0	-	-	-	-	-	-	+	
1 0 0 1 1	+	+	-	-	-	-	+	
1 0 1 0 0	+	+	+	-	-	-	+	
1 0 1 0 1	+	+	+	+	-	-	+	
1 0 1 1 0	-	-	-	-	+	-	+	
1 0 1 1 1	+	+	+	+	+	+	+	
Others	Reserved							

7.0 X-Bus Extension (Continued)

7.4.4 X-Bus Select 1 Configuration Register (XZCNF1)

This register affects the mapping of modules associated with Chip Select 1, $\overline{XCS1}$.

Location: Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	XRDY Enable	Wait States Enable	Indirect Memory Cycle Enable	Select 1 Mapping				
Reset	0	1	0	0	0	0	0	0

Bit	Description
7	**XRDY Enable**. Enables the use of XRDY input for devices mapped to $\overline{XCS1}$. 0: Disabled (default) 1: Enabled
6	**Wait States Enable** 0: Wait states disabled 1: 8 clock cycles of wait enabled (default)
5	**Indirect Memory Cycle Enable**. Enable indirect memory access mechanism to generate memory transaction on $\overline{XCS1}$. 0: Disabled (default) 1: Enabled
4-0	**Select 1 Mapping** UDIZ = User-Defined I/O Zone - = $\overline{XCS1}$ does not respond to this zone decode + = $\overline{XCS1}$ responds to this zone decode and is influenced by its setting

```
Bits                    Function
4 3 2 1 0  KBC  PM  RTC  TST  UDIZ  BIOS  MEM

0 0 0 0 0   -    -    -    -    -     -    - (default)
0 0 0 0 1   -    -    -    -    -     +    -
0 0 0 1 0   +    -    -    -    -     +    -
0 0 0 1 1   +    +    -    -    -     +    -
0 0 1 0 0   +    +    +    -    -     +    -
0 0 1 0 1   +    +    +    +    -     +    -
0 0 1 1 0   -    -    -    -    +     +    -
0 0 1 1 1   +    +    +    -    +     +    -
0 1 0 0 0   +    +    +    +    +     +    -
0 1 0 0 1   +    -    -    -    -     -    -
0 1 0 1 0   +    -    -    -    +     -    -
0 1 0 1 1   +    +    -    -    -     -    -
0 1 1 0 0   +    +    +    -    -     -    -
0 1 1 0 1   +    +    +    +    -     -    -
0 1 1 1 0   -    -    -    -    +     -    -
0 1 1 1 1   +    +    +    +    +     -    -
1 0 0 0 0   +    +    +    +    +     -    +
1 0 0 0 1   +    -    -    -    -     -    +
1 0 0 1 0   -    -    -    -    -     -    +
1 0 0 1 1   +    +    -    -    -     -    +
1 0 1 0 0   +    +    +    -    -     -    +
1 0 1 0 1   +    +    +    +    -     -    +
1 0 1 1 0   -    -    -    -    +     -    +
1 0 1 1 1   +    +    +    +    +     +    +
 Others        Reserved
```

7.0 X-Bus Extension (Continued)

7.4.5 X-Bus PIRQx Input Registers (XIRQCA to XIRQCD)

This set of four registers defines the mapping of the four PIRQ signals. Each registers is associated with one of the four PIRQ inputs, as follows:

Location: Offset 04h (XIRQCA)

Location: Offset 05h (XIRQCB)

Location: Offset 06h (XIRQCC)

Location: Offset 07h (XIRQCD)

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	Reserved				PIRQ Polarity Inversion	PIRQ Enable	PIRQ Polarity	$\overline{\text{PWUREQ}}$ Enable
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**PIRQ Polarity Inversion.** This bit controls the polarity of the IRQ signal sent through the IRQ Serializer (see Table 32). This bit is reset to '0'.
2	**PIRQ Enable.** When this bit is set, it enables the interrupt. Ignored when the IRQ is mapped to zero (see Section 2.2.3). 0: Disabled (default). 1: Enabled.
1	**PIRQ Polarity.** This bit specifies the active level of the incoming IRQ signal. 0: Active low (default). 1: Active high.
0	**Power-Up Request Enable.** An IRQ event is routed to the $\overline{\text{PWUREQ}}$ output. 0: Disabled (default). 1: Enabled.

Table 32. IRQ Polarity Control

PIRQ Polarity Inversion	PIRQ Polarity	Serial IRQ Polarity
0	0	PIRQx
0	1	$\overline{\text{PIRQx}}$
1	0	PIRQx
1	1	$\overline{\text{PIRQx}}$

7.0 X-Bus Extension (Continued)

Figure 28. Functional Illustration of X-Bus PIRQx Input Registers

7.4.6   X-Bus Indirect Memory Address Register 0 (XIMA0)

This register describes the addresses 7-0 for read or write transaction to the memory.

Location: Offset 08h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	X-Bus Indirect Memory Address 7-0							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory Address 7-0**

7.4.7   X-Bus Indirect Memory Address Register 1 (XIMA1)

This register describes the addresses 15-8 for read or write transaction to the memory.

Location: Offset 09h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	X-Bus Indirect Memory Address 15-8							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory Address 15-8**

7.0 X-Bus Extension (Continued)

7.4.8   X-Bus Indirect Memory Address Register 2 (XIMA2)

This register describes the addresses 23-16 for read or write transaction to the memory.

Location: Offset 0Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	X-Bus Indirect Memory Address 23-16							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	X-Bus Indirect Memory Address 23-16

7.4.9   X-Bus Indirect Memory Address Register 3 (XIMA3)

This register describes the addresses 31-24 for read or write transaction to the memory.

Location: Offset 0Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	X-Bus Indirect Memory Address 31-24							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	X-Bus Indirect Memory Address 31-24

7.4.10   X-Bus Indirect Memory Data Register (XIMD)

This register describes data bits 7-0 for read or write transaction to the memory.

Location: Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	X-Bus Indirect Memory Data 7-0							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	X-Bus Indirect Memory Data 7-0

7.5   USAGE HINTS

1. To use the PC8739x with the National Semiconductor PC87570 Keyboard and Power Management Controller, connect the X-Bus as follows:

PC8739x Signals	PC87570 Signals
XRD	HMEMRD
XWR	HMEMWR
XIORD	HIOR
XIOWR	HIOW
XD7-0	HD7-0

7.0 X-Bus Extension (Continued)

XA3-0	HA3-0
XD7-0	HA11-4
XA18-12	HA18-12
XSTB0	FXASTB
XRDY	HIOCHRDY
PIRQA-D	IRQ11, IRQ8, IRQ12, and IRQ1 respectively
GND	HMEMCS

If any of the functions multiplexed on XA18-12 (Game Port or Serial Port 2) are needed, use an external latch for these signals.

Use the XRDY signal that is enabled upon reset. Either of the XIORD and XIOWR signals may be used. Set proper system configuration before accessing a PC87570 or any I/O device with separate read and write signals for I/O and memory transactions.

2. Bear in mind the following system design hints for asynchronous X-Bus use:

● The chip select signal should be used as a qualifier with the address when partial address decoding is in use for multiple device access control.

● In read cycles, the system may drive the data until the read signal XRD is de-asserted to guarantee the proper PC8739x sampling.

● In write cycles, use either the falling or rising edge of the write control signal (XWR) to latch the data in the device.

3. Address multiplexing on XDT7-0 and the $\overline{\text{XSTB2-0}}$ is designed for glueless interface with off-chip latch components. See the example using 74HCT373 latches in Figure 29.
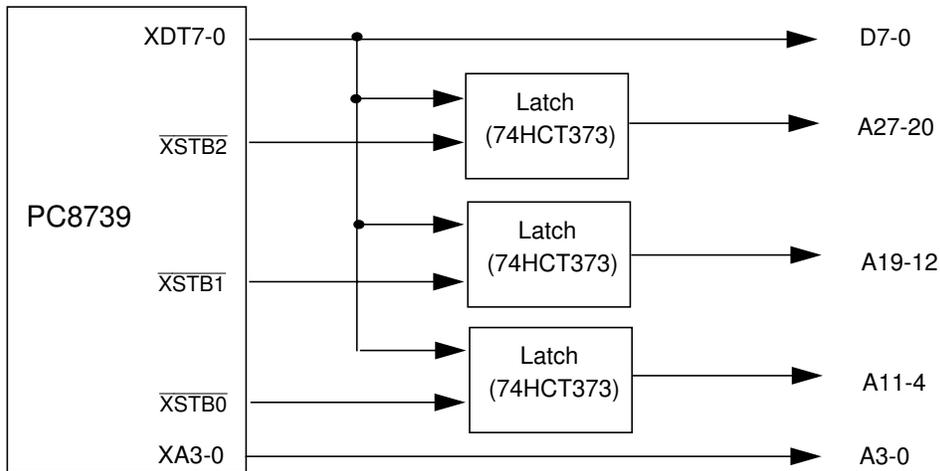
Figure 29. Latched Mode X-Bus Transactions External Logic

7.0 X-Bus Extension (Continued)

7.6 X-BUS EXTENSION BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	XBCNF	Reserved						R/W Extended Mode Enable	Latch Address Mode Enable
01h	XZCNF0	XRDY Enable	Wait States Enable	Reserved	Select 0 Mapping				
02h	XZCNF1	XRDY Enable	Wait States Enable	Reserved	Select 1 Mapping				
03h	Reserved								
04h	XIRQCA	Reserved				PIRQ Polarity Inversion	PIRQ Enable	PIRQ Polarity	$\overline{PWUREQ}$ Enable
05h	XIRQCB	Reserved				PIRQ Polarity Inversion	PIRQ Enable	PIRQ Polarity	$\overline{PWUREQ}$ Enable
06h	XIRQCC	Reserved				PIRQ Polarity Inversion	PIRQ Enable	PIRQ Polarity	$\overline{PWUREQ}$ Enable
07h	XIRQCD	Reserved				PIRQ Polarity Inversion	PIRQ Enable	PIRQ Polarity	$\overline{PWUREQ}$ Enable
08h	XIMA0	X-Bus Indirect Memory Address 7-0							
09h	XIMA1	X-Bus Indirect Memory Address 15-8							
0Ah	XIMA2	X-Bus Indirect Memory Address 23-16							
0Bh	XIMA3	X-Bus Indirect Memory Address 31-24							
0Ch	XIMD	X-Bus Indirect Memory Data 7-0							

8.0 Legacy Functional Blocks

This chapter briefly describes the following blocks that provide legacy device functions:

- Floppy Disk Controller (FDC)
- Parallel Port
- Serial Port 1 (SP1), UART Functionality for both Serial Port 1 and Serial Port 2
- Serial Port 2 (SP2), Infrared Functionality

The description of each Legacy block includes the sections listed below. For details on the general implementation of each legacy block, see the *SuperI/O Legacy Functional Blocks* datasheet.

- General Description
- Register Map table(s)
- Bitmap table(s).

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

8.1 FLOPPY DISK CONTROLLER (FDC)

8.1.1 General Description

The generic FDC is a standard FDC with a digital data separator, and is DP8473 and N82077 software compatible.

The FDC is implemented in this device as follows:

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode
- Automatic media sense is supported by MSEN1-0 pins only on FDC signals routed to the PPM functional block (on the Parallel Port).
- DRATE1 is not supported.
- A logic 1 is returned for all floating (TRI-STATE) FDC register bits upon LPC I/O read cycles.

8.1.2 FDC Register Map

Offset	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
04h	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W
06h		Reserved	
07h	DIR	Digital Input	R
07h	CCR	Configuration Control	W

8.0 Legacy Functional Blocks (Continued)

8.1.3 FDC Bitmap Summary

The FDC supports two system operation modes: PC-AT mode and PS/2 mode (MicroChannel systems). Unless specifically indicated otherwise, all fields in all registers are valid in both drive modes.

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	SRA[1]	IRQ Pending	Reserved	Step	$\overline{TRK0}$	Head Select	$\overline{INDEX}$	$\overline{WP}$	Head Direction
01h	SRB[1]	Reserved		Drive Select 0 Status	$\overline{WDATA}$	$\overline{RDATA}$	$\overline{WGATE}$	$\overline{MTR1}$	$\overline{MTR0}$
02h	DOR	Motor Enable 3	Motor Enable 2	Motor Enable 1	Motor Enable 0	DMAEN	Reset Controller	Drive Select	
03h	TDR	Reserved						Tape Drive Select 1,0	
	TDR[2]	Reserved		Drive ID Information		Logical Drive Exchange		Tape Drive Select 1,0	
04h	MSR	RQM	Data I/O Direction	Non-DMA Execution	Command in Progress	Drive 3 Busy	Drive 2 Busy	Drive 1 Busy	Drive 0 Busy
	DSR	Software Reset	Low Power	Reserved	Precompensation Delay Select			Data Transfer Rate Select	
05h	FIFO	Data Bits							
07h	DIR[3]	$\overline{DSKCHG}$	Reserved						
	DIR[1]	$\overline{DSKCHG}$	Reserved				DRATE 1,0 Status		High Density
07h	CCR	Reserved						DRATE1,0	

1. Applicable only in PS/2 Mode
2. Applicable only in Enhanced TDR Mode
3. Applicable only in PC-AT Compatible Mode

8.0 Legacy Functional Blocks (Continued)

8.2 PARALLEL PORT

8.2.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

8.2.2 Parallel Port Register Map

The Parallel Port functional block register maps are grouped according to first and second level offsets. EPP and second level offset registers are available only when base address is 8-byte aligned.

Table 33. Parallel Port Register Map for First Level Offset

First Level Offset	Mnemonic	Register Name	Modes (ECR Bits) 7 6 5	Type
000h	DATAR	PP Data	0 0 0 0 0 1	R/W
000h	AFIFO	ECP Address FIFO	0 1 1	W
001h	DSR	Status	All Modes	RO
002h	DCR	Control	All Modes	R/W
003h	ADDR	EPP Address	1 0 0	R/W
004h	DATA0	EPP Data Port 0	1 0 0	R/W
005h	DATA1	EPP Data Port 1	1 0 0	R/W
006h	DATA2	EPP Data Port 2	1 0 0	R/W
007h	DATA3	EPP Data Port 3	1 0 0	R/W
400h	CFIFO	PP Data FIFO	0 1 0	W
400h	DFIFO	ECP Data FIFO	0 1 1	R/W
400h	TFIFO	Test FIFO	1 1 0	R/W
400h	CNFGA	Configuration A	1 1 1	RO
401h	CNFGB	Configuration B	1 1 1	RO
402h	ECR	Extended Control	All Modes	R/W
403h	EIR	Extended Index	All Modes	R/W
404h	EDR	Extended Data	All Modes	R/W
405h	EAR	Extended Auxiliary Status	All Modes	R/W

Table 34. Parallel Port Register Map for Second Level Offset

Second Level Offset	Register Name	Type
00h	Control0	R/W
02h	Control2	R/W
04h	Control4	R/W
05h	PP Confg0	R/W

8.0 Legacy Functional Blocks (Continued)

8.2.3   Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 35. Parallel Port Bitmap Summary for First Level Offset

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
000h	DATAR	Data Bits							
	AFIFO	Address Bits							
001h	DSR	Printer Status	$\overline{ACK}$ Status	PE Status	SLCT Status	$\overline{ERR}$ Status	Reserved		EPP Time-out Status
002h	DCR	Reserved		Direction Control	Interrupt Enable	PP Input Control	Printer Initialization Control	Automatic Line Feed Control	Data Strobe Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	Interrupt Request Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	ECP Mode Control			ECP Interrupt Mask	ECP DMA Enable	ECP Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved				Second Level Offset			
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

8.0 Legacy Functional Blocks (Continued)

Table 36. Parallel Port Bitmap Summary for Second Level Offset

Register		Bits							
Second Level Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	Control0	Reserved		DCR Register Live	Freeze Bit	Reserved			EPP Time-out Interrupt Mask
02h	Control2	SPP Com-patibility	Channel Address Enable	Reserved	Revision 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	ECP IRQ Channel Number			PE Internal Pull-up or Pull-down	ECP DMA Channel Number	

8.0 Legacy Functional Blocks (Continued)

8.3 UART FUNCTIONALITY (SP1 AND SP2)

8.3.1 General Description

Both SP1 and SP2 provide UART functionality. The generic SP1 and SP2 support serial data communication with remote peripheral device or modem using a wired interface. The functional blocks can function as a standard 16450, 16550, or as an Extended UART.

8.3.2 UART Mode Register Bank Overview

Four register banks, each containing eight registers, control UART operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 30.
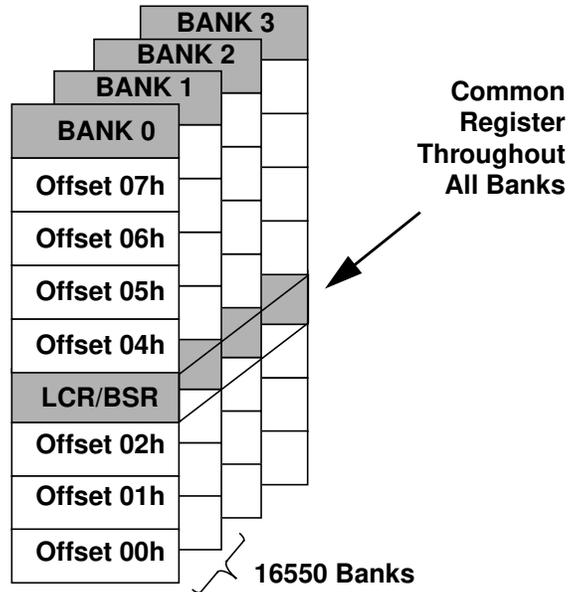
Figure 30. UART Mode Register Bank Architecture

8.0 Legacy Functional Blocks (Continued)

8.3.3 SP1 and SP2 Register Maps for UART Functionality

Table 37. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data Port	RO
00h	TXD	Transmitter Data Port	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification (Read Cycles)	RO
	FCR	FIFO Control (Write Cycles)	W
03h	LCR[1]	Line Control	R/W
	BSR[1]	Bank Select	
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	RO
06h	MSR	Modem Status	RO
07h	SPR/ASCR	Scratchpad/Auxiliary Status and Control	R/W

1. When bit 7 of this Register is set to 1, bits 6-0 of BSR select the bank, as shown in Table 38.

Table 38. Bank Selection Encoding

BSR Bits								Bank Selected	Functionality
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	0	
1	0	x	x	x	x	x	x	1	
1	1	x	x	x	x	1	x	1	UART + IR (SP1 + SP2)
1	1	x	x	x	x	x	1	1	
1	1	1	0	0	0	0	0	2	
1	1	1	0	0	1	0	0	3	
1	1	1	0	1	0	0	0	4	
1	1	1	0	1	1	0	0	5	IR Only (SP2)
1	1	1	1	0	0	0	0	6	
1	1	1	1	0	1	0	0	7	

Table 39. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor Port (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor Port (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Line Control/Bank Select	R/W
04h - 07h		Reserved	

8.0 Legacy Functional Blocks (Continued)

Table 40. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor Port (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor Port (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	R/W
07h	RXFLV	RX_FIFO Level	R/W

Table 41. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Revision ID	RO
01h	SH_LCR	Shadow of LCR (Read Only)	RO
02h	SH_FCR	Shadow of FIFO Control (Read Only)	RO
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h		Reserved	

8.0 Legacy Functional Blocks (Continued)

8.3.4 SP1 and SP2 Bitmap Summary for UART Functionality

Table 42. Bank 0 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	RXD	Receiver Data Bits							
	TXD	Transmitter Data Bits							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	Reserved		TXEMP_IE	Reserved[3]/ DMA_IE[4]	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1	FEN0	Reserved		RXFT	IPR1	IPR0	IPF
	EIR[2]	Reserved		TXEMP_EV	Reserved[3]/ DMA_EV[4]	MS_EV	LS_EV or TXHLT_EV	TXLDL_EV	RXHDL_EV
	FCR	RXFTH1	RXFTH0	TXFTH1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR[5]	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
	BSR[5]	BKSE	Bank Select						
04h	MCR[1]	Reserved			LOOP	ISEN or DCDLP	RILP	RTS	DTR
	MCR[2]	Reserved				TX_DFR	Reserved	RTS	DTR
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR [2]	Reserved	TXUR[4]	RXACT [4]	RXWDG [4]	Reserved	S_OET [4]	Reserved	RXF_TOUT

1. Non-Extended Mode
2. Extended Mode
3. In SP1 only
4. In SP2 only
5. When bit 7 of this register is set to 1, bits 6-0 of BSR select the bank, as shown in Table 38.

8.0 Legacy Functional Blocks (Continued)

Table 43. Bank 1 Bitmap

Offset	Mnemonic	7	6	5	4	3	2	1	0
	Register	**Bits**							
00h	LBGD(L)	Legacy Baud Generator Divisor (Least Significant Bits)							
01h	LBGD(H)	Legacy Baud Generator Divisor (Most Significant Bits)							
02h		Reserved							
03h	LCR/BSR	Same as Bank 0							
04h-07h		Reserved							

Table 44. Bank 2 Bitmap

Offset	Mnemonic	7	6	5	4	3	2	1	0
	Register	**Bits**							
00h	BGD(L)	Baud Generator Divisor Low (Least Significant Bits)							
01h	BGD(H)	Baud Generator Divisor High (Most Significant Bits)							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	LCR/BSR	Same as Bank 0							
04h	EXCR2	LOCK	Reserved	PRESL1	PRESL0	Reserved			
05h	Reserved								
06h	TXFLV	Reserved			TFL4	TFL3	TFL2	TFL1	TFL0
07h	RXFLV	Reserved			RFL4	RFL3	RFL2	RFL1	RFL0

Table 45. Bank 3 Bitmap

Offset	Mnemonic	7	6	5	4	3	2	1	0
	Register	**Bits**							
00h	MRID	Module ID (MID 7-4)				Revision ID(RID 3-0)			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
02h	SH_FCR	RXFTH1	RXFTH0	TXFHT1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR/BSR	Same as Bank 0							
04h-07h		Reserved							

8.0 Legacy Functional Blocks (Continued)

8.4 IR FUNCTIONALITY (SP2)

8.4.1 General Description

This section describes the IR support registers of Serial Port 2 (SP2). The UART support registers for both SP1 and SP2 are described in Section 8.3.

The IR functional block provides advanced, versatile serial communications features with IR capabilities.

SP2 supports also two DMA channels; the functional block can use either one or both of them. One channel is required for IR-based applications, since IR communication works in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex UART based applications.

8.4.2 IR Mode Register Bank Overview

Eight register banks, each containing eight registers, control SP2 operation. Banks 0-3 are used to control both UART and IR modes of operation; banks 4-7 are used to control and configure the IR modes of operation only. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 31.
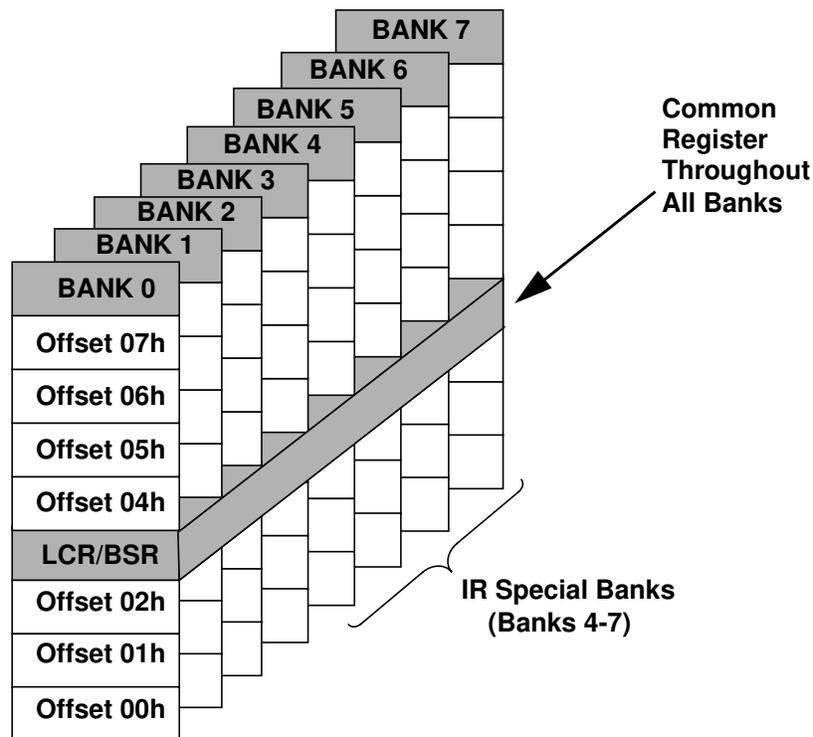
Figure 31. SP2 Register Bank Architecture

8.0 Legacy Functional Blocks (Continued)

8.4.3   SP2 Register Map for IR Functionality

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Table 46. Bank 4 Register Map

Offset	Mnemonic	Register Name	Type
00h-01h		Reserved	
02h	IRCR1	IR Control 1	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h - 07h		Reserved	

Table 47. Bank 5 Register Map

Offset	Mnemonic	Register Name	Type
00h-02h		Reserved	
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	IRCR2	IR Control 2	R/W
05h - 07h	Reserved		

Table 48. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRCR3	IR Control 3	R/W
01h		Reserved	
02h	SIR_PW	SIR Pulse Width Control ($\leq$ 115 Kbps)	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h		Reserved	

Table 49. Bank 7 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRRXDC	IR Receiver Demodulator Control	RO
01h	IRTXMC	IR Transmitter Modulator Control	RO
02h	RCCFG	CEIR Configuration	RO
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	IRCFG1	IR Interface Configuration 1	R/W
05h		Reserved	
06h	IRCFG3	IR Interface Configuration 3	R/W
07h	IRCFG4	IR Interface Configuration 4	R/W

8.0 Legacy Functional Blocks (Continued)

8.4.4 SP2 Bitmap Summary for IR Functionality

Table 50. Bank 4 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h-01h		Reserved							
02h	EIR	Reserved				IR_SL1	IR_SL0	Reserved	
03h	LCR/BSR	Same as Bank 0							
04h-07h		Reserved							

Table 51. Bank 5 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h-02h		Reserved							
03h	LCR/BSR	Same as Bank 0							
04h	IRCR2	Reserved			AUX_IRRX	Reserved		IRMSSL	IR_FDPLX
05h-07h		Reserved							

Table 52. Bank 6 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	IRCR3	SHDM_DS	SHMD_DS	Reserved					
01h		Reserved							
02h	SIR_PW	Reserved				SPW (3-0)			
03h	LCR/BSR	Same as Bank 0							
04h-07h		Reserved							

8.0 Legacy Functional Blocks (Continued)

Table 53. Bank 7 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	IRRXDC	DBW (2-0)			DFR (4-0)					
01h	IRTXMC	MCPW (2-0)			MCFR (4-0)					
02h	RCCFG	R_LEN	T_OV	RXHSC	RCDM_DS	Reserved	TXHSC	RC_MND1	RC_MMD0
03h	LCR/BSR	Same as Bank 0								
04h	IRCFG1	STRV_MS	SIRC (2-0)			IRID3	IRIC (2-0)			
05h		Reserved								
06h	IRCFG3	Reserved	RCH (2-0)			Reserved	RCLC (2-0)			
07h	IRCFG4	AMCFG	Reserved	IRSL0_DS	RXINV	IRSL21_DS	Reserved			

9.0 Device Characteristics

9.1 GENERAL DC ELECTRICAL CHARACTERISTICS

9.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
T_A	Operating Temperature	0		+70	°C

9.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		−0.5	+6.5	V
V_I	Input Voltage		−0.5	$V_{DD} + 0.5$	V
V_O	Output Voltage		−0.5	$V_{DD} + 0.5$	V
T_{STG}	Storage Temperature		−65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	$C_{ZAP} = 100$ pF $R_{ZAP} = 1.5$ KΩ[1]	2000		V

1. Value based on test complying with RAI-5-048-RA human body model ESD testing.

9.1.3 Capacitance

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance	5	8	12	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

$T_A = 25°C$, f = 1 MHz

9.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{CC}	V_{DD} Average Main Supply Current	$V_{IL} = 0.5$ V, $V_{IH} = 2.4$ V No Load	32	50	mA
I_{CCLP}	V_{DD} Quiescent Main Supply Current in Low Power Mode	$V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$ No Load	1.3	1.7	mA

9.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in the *Signal/Pin Connection and Description* chapter. The characteristics describe the general I/O buffer types defined in Table 1. For exceptions, refer to Section 9.2.9. The DC characteristics of the system interface meet the PCI2.1 3.3V DC signaling.

9.0 Device Characteristics (Continued)

9.2.1 Input, CMOS Compatible

Symbol: IN_C

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.7 V_{DD}	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.3 V_{DD}	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		50	nA
		$V_{IN} = V_{SS}$		−50	nA

1. Not tested. Guaranteed by design.

9.2.2 Input, PCI 3.3V

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		$0.5V_{DD}$	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{DD}$	V
I_{IL}[1]	Input Leakage Current	$0 < V_{in} < V_{DD}$		±10	μA

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with TRI-STATE outputs.

9.2.3 Input, Strap Pin

Symbol: IN_{STRP}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		$0.6V_{DD}$[1]	5.5[1]	V
V_{IL}	Input Low Voltage		-0.5[1]	$0.5V_{DD}$[1]	V
R_{IH}	Input High Resistance	During Reset: $V_{IN} = 0.6V_{DD}$	16.5		KΩ
R_{IL}	Input Low Resistance	During Reset: $V_{IN} = 0.4V_{DD}$		20	KΩ

1. Not tested. Guaranteed by design.

9.2.4 Input, TTL Compatible

Symbol: IN_T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
		$V_{IN} = V_{SS}$		−10	μA

1. Not tested. Guaranteed by design.

9.0 Device Characteristics (Continued)

9.2.5 Input, TTL Compatible with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5^1	V
V_{IL}	Input Low Voltage		-0.5 [1]	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
		$V_{IN} = V_{SS}$		-10	μA
V_H	Input Hysteresis		250		mV

1. Not tested. Guaranteed by design.

9.2.6 Output, PCI 3.3V

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{out} = -500$ μA	$0.9V_{DD}$		V
V_{OL}	Output Low Voltage	$I_{out} = 1500$ μA		$0.1 V_{DD}$	V

9.2.7 Output, Totem-Pole Buffer

Symbol: $O_{p/n}$

Output, Totem-Pole buffer that is capable of sourcing p mA and sinking n mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -p$ mA	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

9.2.8 Output, Open-Drain Buffer

Symbol: OD_n

Output, Open-Drain output buffer, capable of sinking n mA. Output from these signals is open-drain and cannot be forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

9.2.9 Exceptions

1. All pins are back-drive protected, except for the output pins with PCI Buffer Type.

2. The following pins have a PU_{220} internal pull-up resistor and therefore have input leakage current to V_{DD}: $\overline{ACK}$, $\overline{AFD\_DSTRB}$, $\overline{ERR}$, $\overline{INIT}$, PE, $SLIN\_ASTRB$, $\overline{STB\_WRITE}$.

3. The following pins have a PU_{25} internal pull-up resistor and therefore have input leakage current to V_{DD}: GPIO40-47, GPIO30-37, GPIO20-27, GPIO10-17, GPIO00-07.

4. The following pins have a PD_{120} internal pull-down resistor and therefore have input leakage current to GND: BUSY_$\overline{WAIT}$, PE, SLCT.

5. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 Register is 0) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.

9.0 Device Characteristics (Continued)

6. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 Register is set to 1) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.

7. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.

8. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.

9.3   INTERNAL RESISTORS

9.3.1   Pull-Up Resistor

Symbol: PU_{nn}.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
R_{PU}	Pull-up equivalent resistance	$V_{PIN} = V_{DD} = 3.3V$	*nn*-30%	*nn*	*nn*+30%	KΩ

9.3.2   Pull-Down Resistor

Symbol: PD_{nn}.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
R_{PD}	Pull-down equivalent resistance	$V_{PIN} = 0V$, $V_{DD} = 3.3V$	*nn*-30%	*nn*	*nn*+30%	KΩ

9.0 Device Characteristics (Continued)

9.4 AC ELECTRICAL CHARACTERISTICS

9.4.1 AC Test Conditions

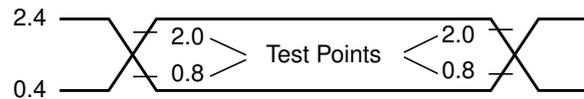**Load Circuit** (Notes 1, 2, 3)
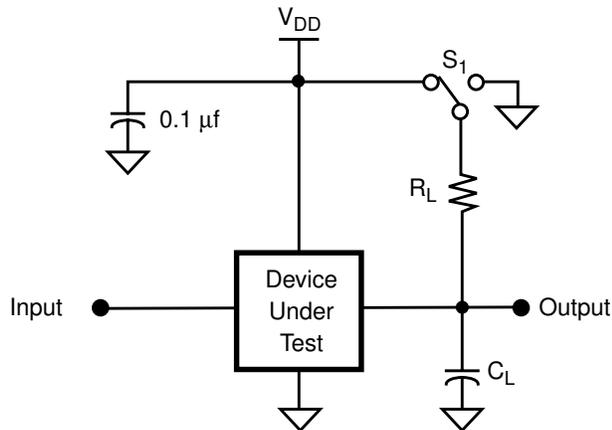
AC Testing Input, Output Waveform

**Figure 32. AC Test Conditions, T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ±10%**

Notes:

1. C_L = 100 pF for all output pins (except O_{PCI});
   C_L = 50 pF for O_{PCI} output pins;
   These values include both jig and oscilloscope capacitance.

2. S_1 = Open for push-pull output pins.
   S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements.
   S_1 = GND for high impedance to active high and active high to high impedance measurements.
   R_L = 1.0KΩ for μP interface pins.

3. For the FDC open-drive interface pins, S_1 = V_{DD} and R_L = 150Ω.

9.4.2 Clock Timing

Symbol	Parameter	48 MHz		Unit
		Min	Max	
t_{CH}	Clock High Pulse Width[1]	8.4		ns
t_{CL}	Clock Low Pulse Width[1]	8.4		ns
t_{CP}	Clock Period [1] [2]	20	21.5	ns

1. Not tested. Guaranteed by design.
2. For the 14.31818 MHz clock, required tolerance is 200 ppm (max).
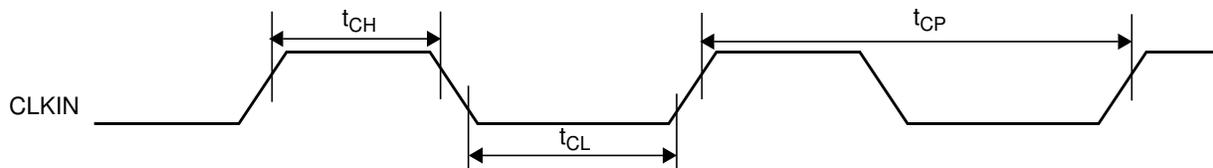
9.0 Device Characteristics (Continued)

9.4.3 LCLK and $\overline{\text{LRESET}}$

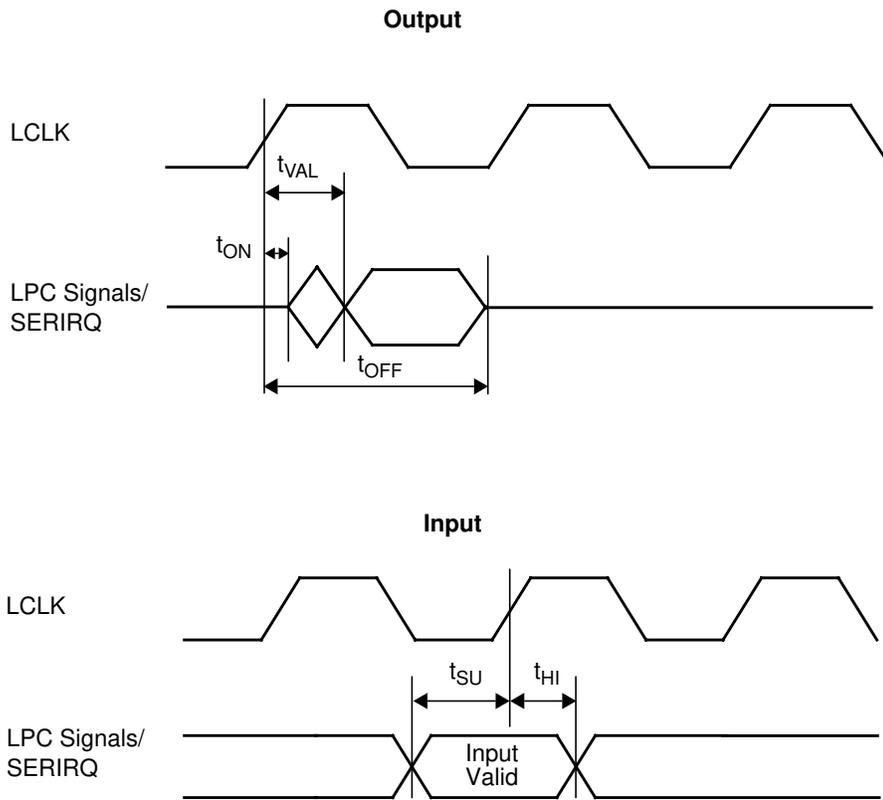| Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	LCLK Cycle Time	30		ns
t_{HIGH}	LCLK High Time	11		ns
t_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate[2]	1	4	V/ns
-	$\overline{\text{LRESET}}$ Slew Rate[3]	50		mV/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain "clean" (monotonic) and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering as shown below.
3. The minimum $\overline{\text{LRESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal, and ensures that system noise cannot render an otherwise a monotonic signal to appear to bounce in the switching range.

3.3 V Clock
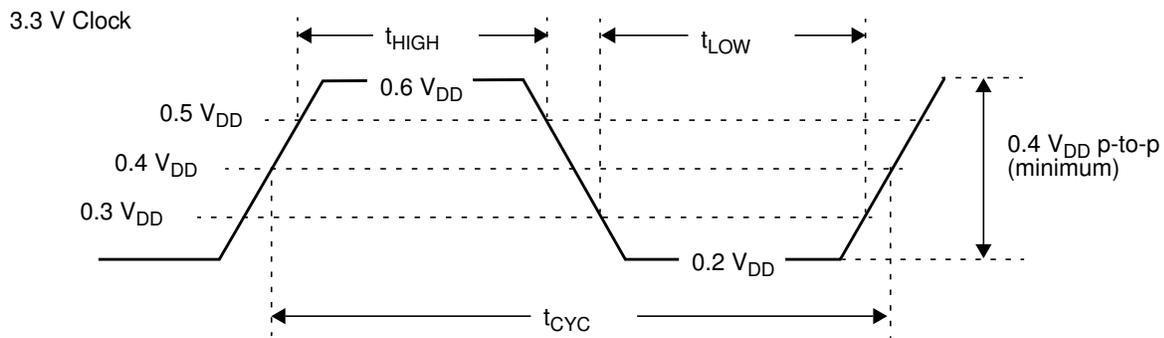
9.0 Device Characteristics (Continued)

9.4.4 LPC and SERIRQ Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Output	Output Valid Delay	After RE CLK		11	ns
t_{ON}	Output	Float to Active Delay	After RE CLK	2		ns
t_{OFF}	Output	Active to Float Delay	After RE CLK		28	ns
t_{SU}	Input	Input Setup Time	Before RE CLK	7		ns
t_{HI}	Input	Input Hold Time	After RE CLK	0		ns

Output

LCLK

t_{VAL}

t_{ON}

LPC Signals/
SERIRQ

t_{OFF}

Input

LCLK

t_{SU} t_{HI}

LPC Signals/
SERIRQ

Input
Valid

9.0 Device Characteristics (Continued)

9.4.5 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

| Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	$t_{BTN} - 25$ [1]	$t_{BTN} + 25$	ns
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	ns
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 25$ [2]	$t_{CWN} + 25$	ns
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 25$ [3]	$t_{CPN} + 25$	ns
		Receiver	t_{MMIN} [4]	t_{MMAX} [4]	ns
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(^3/_{16}) \times t_{BTN} - 15$ [1]	$(^3/_{16}) \times t_{BTN} + 15$ [1]	ns
		Transmitter, Fixed	1.48	1.78	µs
		Receiver	1		µs
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter. % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

1. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers

2. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits 7-5) of the IRTXMC registerand the TXHSC bit (bit 2) of the RCCFG register

3. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFR field (bits 4-0) of the IRTXMC registerand the TXHSC bit (bit 2) of the RCCFG register.

4. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of the IRRXDC register and the setting of the RXHSC bit (bit 5) of the RCCFG register
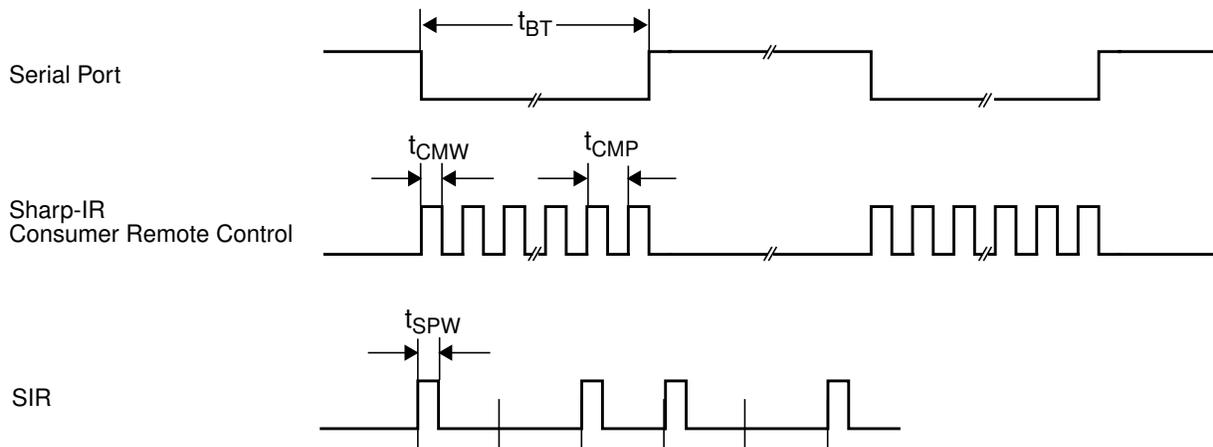
9.0 Device Characteristics (Continued)

9.4.6 Modem Control Timing

Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI2,1}$ Low Time	10		ns
t_H	$\overline{RI2,1}$ High Time	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns
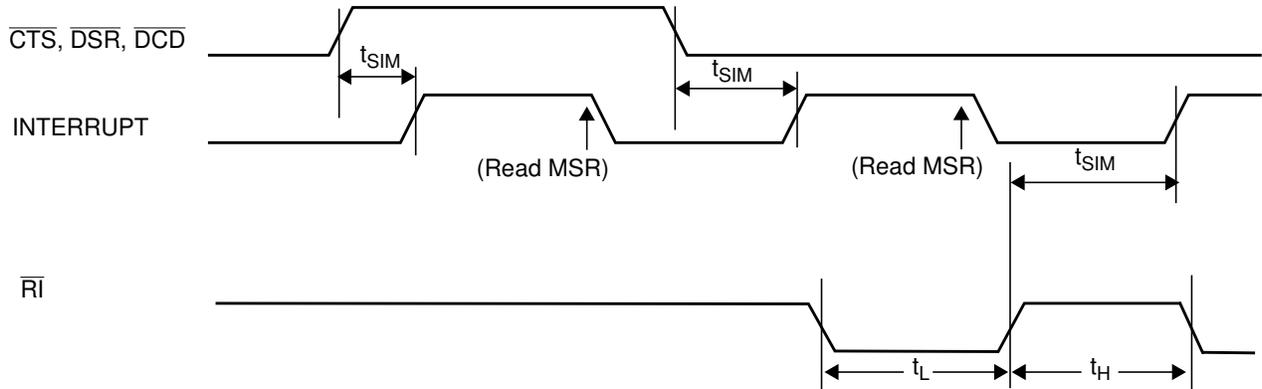
9.4.7 FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[1]	100		µs
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[1]	100		µs
t_{WDW}	Write Data Pulse Width	See t_{DRP} t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.
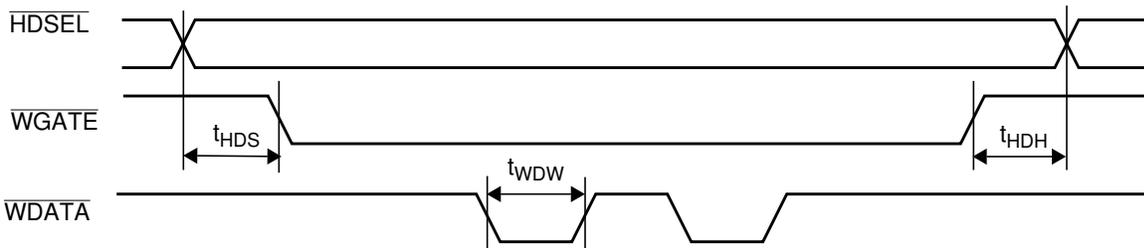
t_{DRP} t_{ICP} t_{WDW} Values

| Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	ns

1. t_{CP} is the clock period defined in the *Clock Timing* section of this chapter.

9.0 Device Characteristics (Continued)

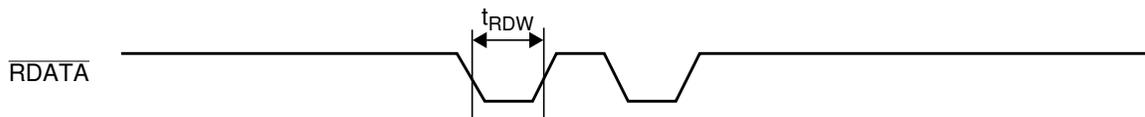### 9.4.8 FDC Drive Control Timing

Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[1]	6		μs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active High Pulse Width[1]	8		μs
t_{STR}	$\overline{STEP}$ Rate Time[1]	0.5		ms

1. Not tested. Guaranteed by design.
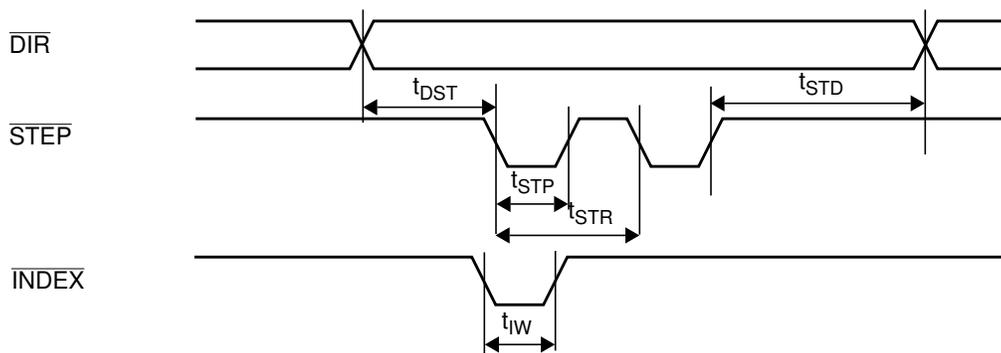
9.4.9 FDC Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns

9.0 Device Characteristics (Continued)

9.4.10 Standard Parallel Port Timing

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{PDH}	Port Data Hold	These times are system dependent and are therefore not tested.	500		ns
t_{PDS}	Port Data Setup	These times are system dependent and are therefore not tested.	500		ns
t_{SW}	Strobe Width	These times are system dependent and are therefore not tested.	500		ns

Typical Data Exchange
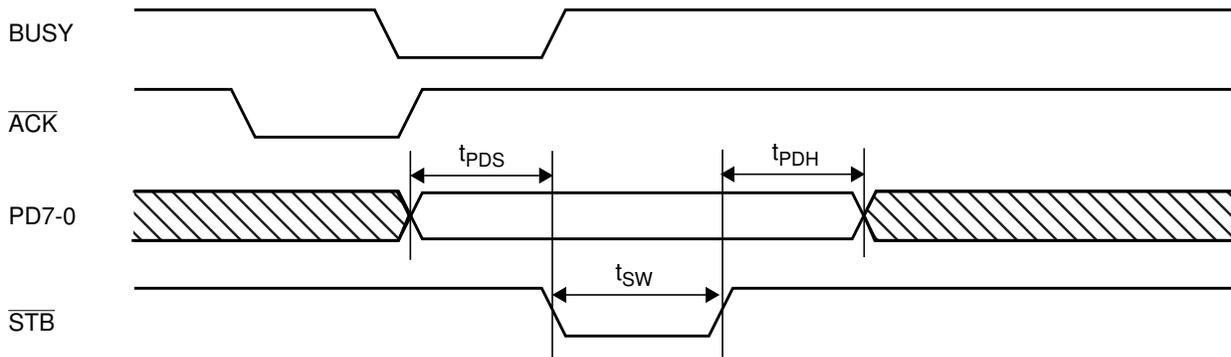
9.4.11 Enhanced Parallel Port Timing

| Symbol	Parameter	Min	Max	EPP 1.7	EPP 1.9	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	2		✔	✔	ns
t_{WPDH}	PD7-0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7-0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7-0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7-0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns
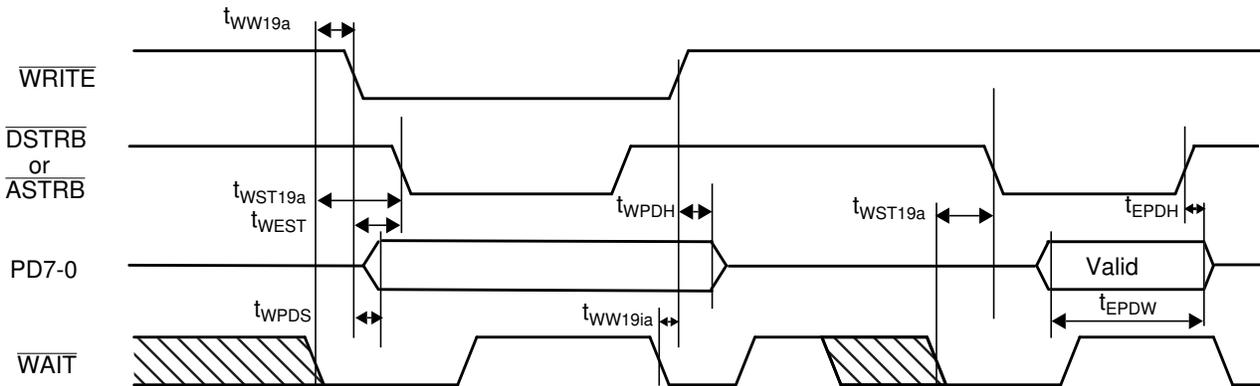
9.0 Device Characteristics (Continued)

9.4.12 Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Active	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		ns
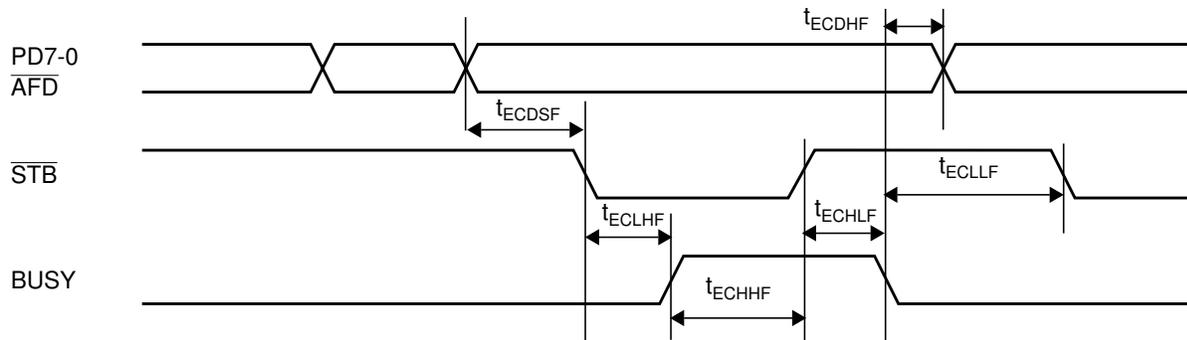
Reverse Mode

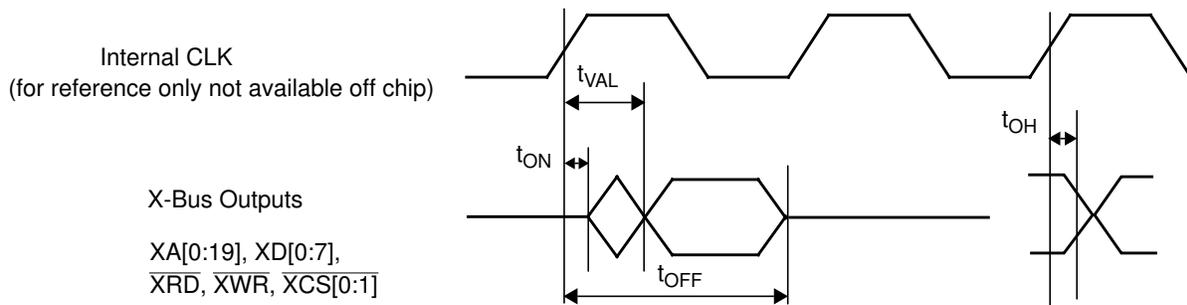| Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		ns
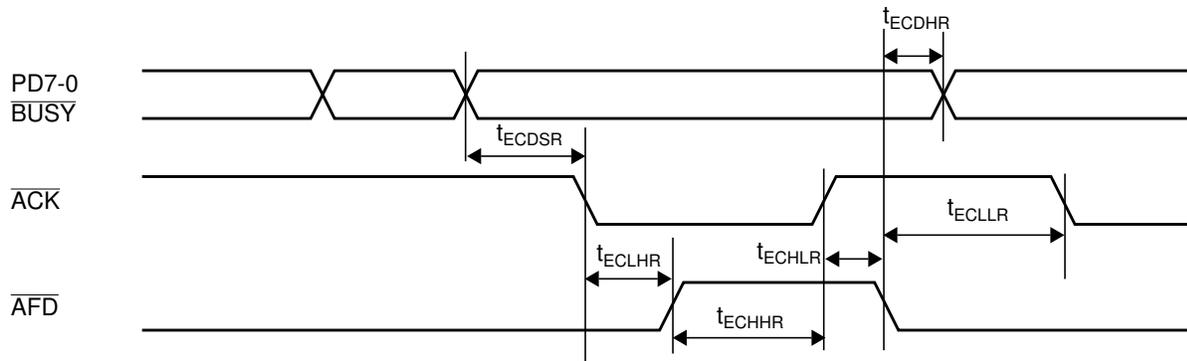
9.0 Device Characteristics (Continued)

9.4.13   X-Bus Signals (PC87393 and PC87393F only)

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Output	Output Valid Delay	After RE CLK		20	ns
t_{ON}	Output	Float to Active Delay	After RE CLK	0		ns
t_{OH}	Output	Output Hold time	After RE CLK	0		ns
t_{OFF}	Output	Active to Float Delay	After RE CLK		30	ns
t_{SU}	Input	Input Setup Time	Before RE CLK	15		ns
t_{HI}	Input	Input Hold Time	After RE CLK	0		ns

Output

Internal CLK
(for reference only not available off chip)

t_{VAL}

t_{OH}

t_{ON}

X-Bus Outputs

XA[0:19], XD[0:7],
$\overline{XRD}$, $\overline{XWR}$, $\overline{XCS[0:1]}$

t_{OFF}

Input

Internal CLK
(for reference only not available off chip)

t_{SU} t_{HI}

XD[0:7]
XRDY

Input
Valid

PC87391, PC87392, PC87393, PC87393F 100-Pin LPC SuperI/O Devices for Portable Applications
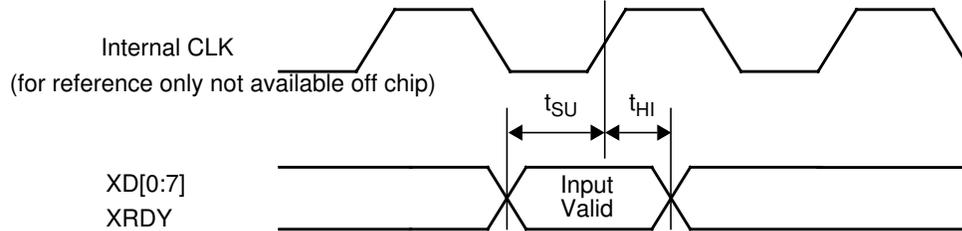
Physical Dimensions

All dimensions are in millimeters.

16.0 ± 0.2 TYP

75   51   OPTIONAL

76   50

100   26

PIN #1
IDENT.

1   0.5 TYP   25

0.22 ± 0.05 TYP

SEE DETAIL A

1.40 ± 0.05

□ 14.00 ± 0.1

0.09 ± 0.20 TYP

(1.0)

11°−13° TOP AND BOTTOM

0° MIN

R0.08 MIN

R0.08−0.20

0.25
GAGE PLANE

1.6 MAX

0.08

0° − 7°

SEATING PLANE

0.05−0.15

0.60 ± 0.15

0.20 MIN

DETAIL A
TYPICAL, SCALE: 20X
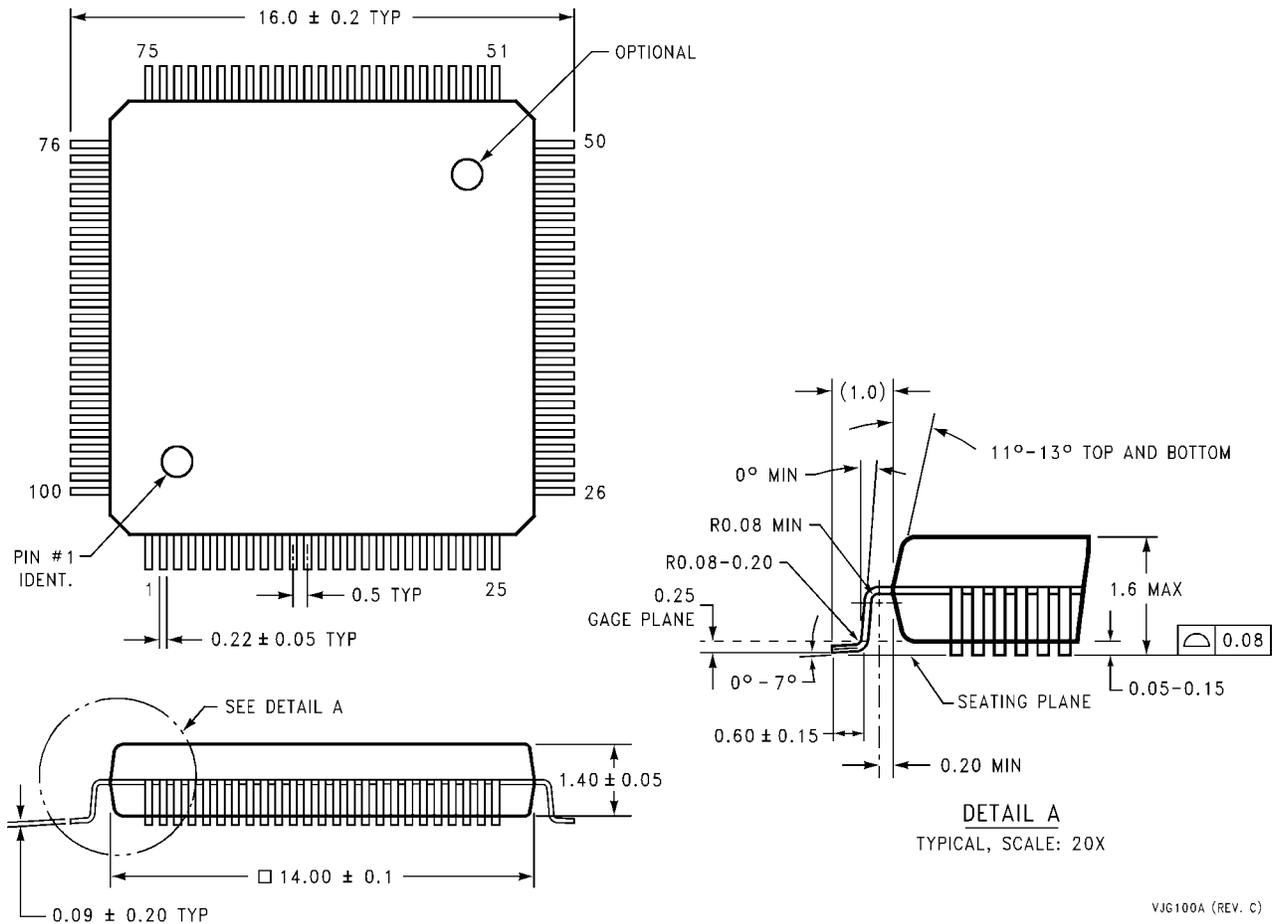
VJG100A (REV. C)

Thin Quad Flatpack (TQFP), JEDEC
Order Number PC8739x-VJG
NS Package Number VJG100A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.