# Bipolar LSI takes a new direction with integrated injection logic

## Using conventional processes, simplified gate structure of $I^2L$ boosts yields and density, while reducing power consumption a thousandfold; the low-cost technique is applicable to both analog and digital circuits

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☐ Integrated injection logic, the new approach to bipolar chip design, is catching the imagination of logic designers throughout the world with its high-density capability and its performance that features either nanosecond delay or microwatt power dissipation. Conceived almost simultaneously by Dutch and German researchers at Philips Gloeilampenfabrieken, Eindhoven, and IBM Deutschland, Boeblingen, $I^2L$ quickly spread to the United States and Japan, where it's become the best bet for the realization of truly high-performance bipolar LSI circuitry.

Ultimate source of all the excitement is $I^2L$'s elegant gate layout, from which the space- and power-consuming current sources and load resistors of transistor-transistor logic are noticeably absent. As a result of this simplicity, up to 3,000 gates or 10,000 bits of memory can be packed into a single high-yield chip. Moreover, the speed-power product can drop, at low power, to an astonishing 0.13 picojoule, 1,000 times better than today's TTL circuits.

Thus, while operating at speeds almost as fast as TTL, thousands of gates will dissipate no more power than today's 100-gate devices. Or, where speed isn't essential, as in watch circuits, $I^2L$ chips will offer microwatt dissipation while providing direct high-current drive capability for light-emitting-diode displays.

To top it off, this revisionary bipolar logic is extremely versatile. $I^2L$ enables designers to put both digital and analog circuits on the same chip and, because it uses conventional bipolar processes, is low-cost and can be applied to the full range of microcircuit applications. Among these are single-chip digital data processors, large-scale integrated logic arrays, watch chips, digital voltmeter circuits, high-frequency counters, digital tuners, read-only memories, shift registers, converters of all kinds, control logic for complex calculators, frequency dividers for electronic organs, and linear circuits for radio and television. Although not presently at Philips, commercial production of 8- and 16-bit microprocessors and high-frequency watch circuits is beginning. Touch control circuits for radio and TV tuning and circuits for telephone tone-dialing systems are also on the way [*Electronics*, July 11, p. 25].

Injection logic reduces a gate to a single complementary transistor pair. A vertical npn transistor with multiple collectors operates as an inverter, a lateral pnp transistor serves both as current source and load, and no ohmic resistors are required for either the source or load function. In contrast, a typical TTL gate is constructed out of six or eight transistors as well as source and load components.

When the $I^2L$ gate is laid out on silicon, both circuit elements can be merged and fitted into the area of a single transistor, in the process eliminating completely the space-consuming necessity of device isolation. Structural complexity almost vanishes, being reduced to that of a single planar transistor.

This, plus the absence of resistors and current sources, accounts for injection logic's greatly increased circuit density, which, as Table 1 shows, can be up to 100 times greater than that of TTL chips. As Table 1 also shows, an $I^2L$ gate is somewhat slower than a TTL gate, but in most applications this is more than compensated for by its far lower speed-power product.

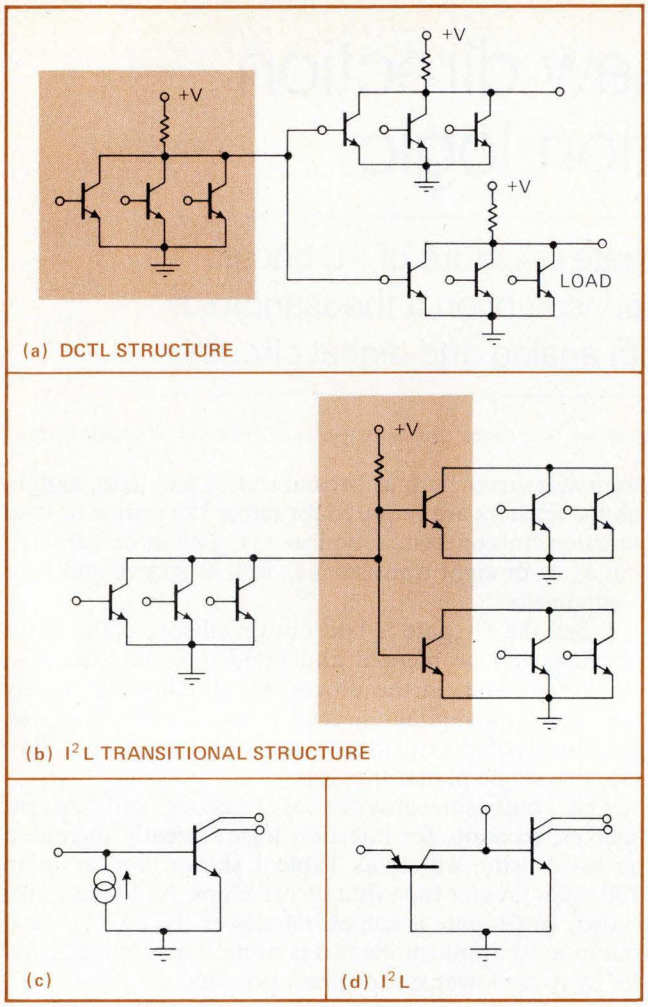
### Origin of the $I^2L$ gate

Injection logic derives its layout from the old direct-coupled transistor logic (DCTL) structure shown in Fig. 1a. The circuit between the dashed lines consists of a number of transistors in parallel. Clearly, when one or more of them are on, they act as a short circuit, and no current is supplied to the load gates. Conversely, when they are all in the off state, current moves to the bases of the transistors in the load gates.

If the two transistors that have their bases connected

**TABLE 1: COMPARISON OF TYPICAL $I^2L$ AND TTL PROPERTIES**

| | $I^2L$ | TTL |
|---|---|---|
| Packing density (7-μm mask details) | 120 – 200 gates/mm² | 20 gates/mm² |
| Speed-power product | 0.1 – 0.7 pJ/gate | 100 pJ/gate |
| Minimum delay | 30 ns | 10 ns |
| Supply voltage | 1 – 15 V | 3 – 73 V |
| Logic voltage swing | 0.6 V | 5 V |
| Current range (per gate) | 1 nA – 1 mA | 2 mA |




**1. Starting point.** Direct-coupled transistor logic (DCTL) can be converted into integrated injection logic ($I^2L$) if the transistors with connected bases (a) are placed in a common region (b) and finally replaced by a multi-collector npn transistor (c). The resistor in (b) is replaced by a current source as in (d)—a pnp transistor where the collector is common to the emitter of the npn transistor.

in Fig. 1a are placed in a common region, the result is the circuit between the dashed lines in Fig. 1b.

Next, the resistor in Fig. 1b is replaced by an active current source (to be described later), and transistors with connected bases are replaced by a multi-collector transistor—an easy thing to do because all the DCTL transistors have a common emitter that is connected to ground. This basic $I^2L$ configuration is presented in Fig. 1c.

The simple pnp transistor shown in Fig. 1d can serve as the current source, by injecting minority carriers into the emitter region of the npn transistor. (Alternatively, injection could be done by a light source for electro-optical applications.)

In any case, it is readily seen that the base of the npn transistor is common to the collector of the current source, while the base of the pnp current source is common to the emitter of the npn transistor. The emitter of the pnp, common for all gates, is called the injector. On silicon the entire gate takes up the room of a single multi-emitter transistor.

The original DCTL structure had its faults. Referring again to the structure in Fig. 1a, consider the case where all transistors between the dashed lines are in the off state and current is supplied to the bases of the load transistors. Because of the differences that process variations during normal production runs and temperature differences during operation cause in the emitter-base junction voltages, not all bases will receive the same current. For example, a transistor operating at a higher temperature will receive more current than one operating at a lower temperature.

Fortunately, this condition, known as current hogging, does not arise in $I^2L$ structures because the different bases and emitters are now combined in the single multi-collector transistor and are formed by the diffusion step. What's more, the hogging of input currents by high fan-in gates—another type of current hogging in DCTL—is negligible in $I^2L$ gates because of the inherently high inverse current gain of the upside-down npn transistors.

## Building an $I^2L$ circuit

Figure 2 shows the cross section of a typical circuit that combines $I^2L$ gates with conventionally isolated transistors. Fabrication of this circuit starts with a p-type substrate containing discrete $n^+$ buried layers. The buried layer in the $I^2L$ part of the circuit acts as a common emitter for the npn transistors, while in conventional TTL or emitter-coupled logic they act as the collector for the isolated structures.

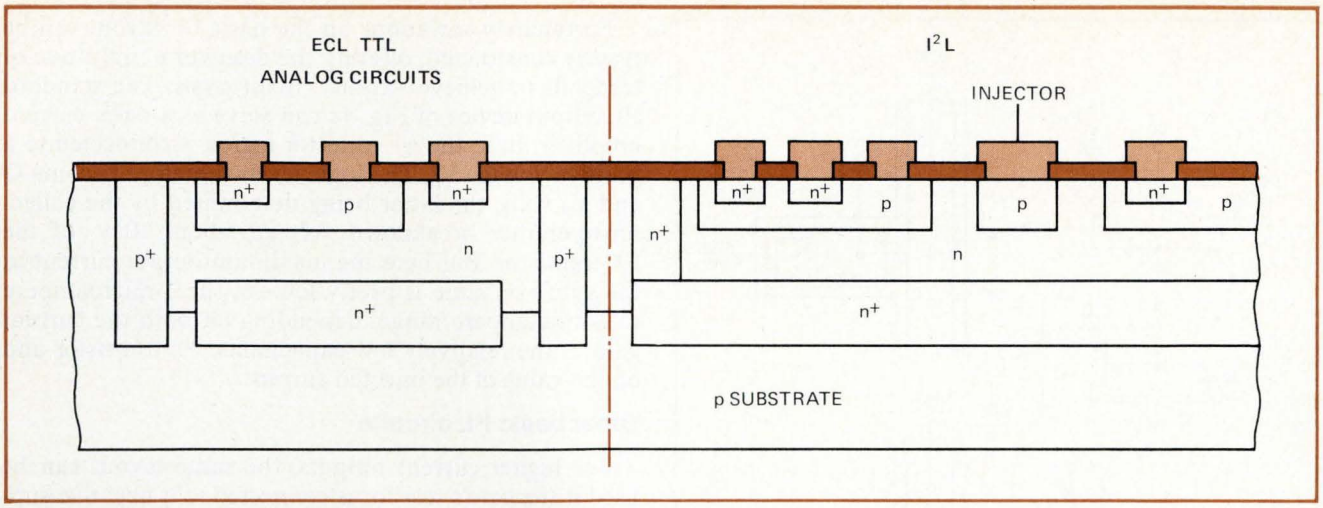
After the n-type epitaxial layer has been grown, a deep $p^+$ diffusion is performed to isolate the conventional components, while in the $I^2L$ part the gates are isolated from each other by a deep $n^+$ diffusion. A p-type diffusion is then carried out to form all base regions and emitters of the lateral pnp transistors (the injectors of the $I^2L$ gate). Next, a shallow $n^+$ diffusion forms both the collectors in the $I^2L$ part of the circuit and the emitter and the collector contact regions for the conventional transistor structures. Two additional mask steps are needed for the contact holes and metalization.

In all, only seven masks are needed to manufacture both conventional isolated and $I^2L$ transistors on the same chip. No extra processing is required. Most important, any standard bipolar process can be used to build the circuit elements—with one limitation: gold doping may not be used on the conventional transistors to boost their speed and reduce their loading effects because it would decrease the inverse current gain of the $I^2L$ transistors.

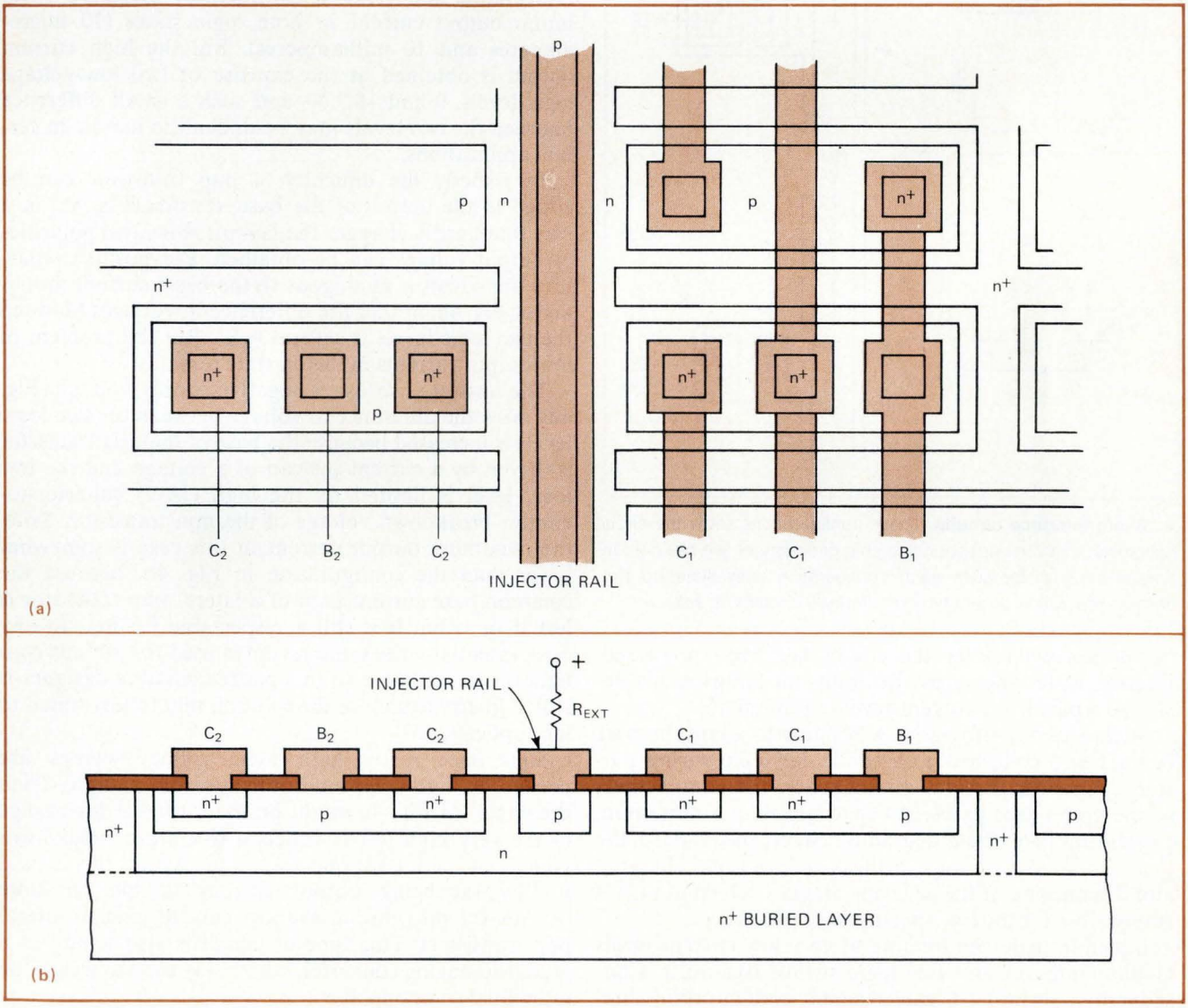
## It's flexible

From the top view and cross sections of some typical $I^2L$ gates, (Fig. 3), it is apparent that the $n^+$ buried layer acts as a common emitter region for the multi-collector npn transistors, and a long narrow p-type area (the injector) acts as the emitter of the pnp transistor. The gates are situated on both sides of the injector.

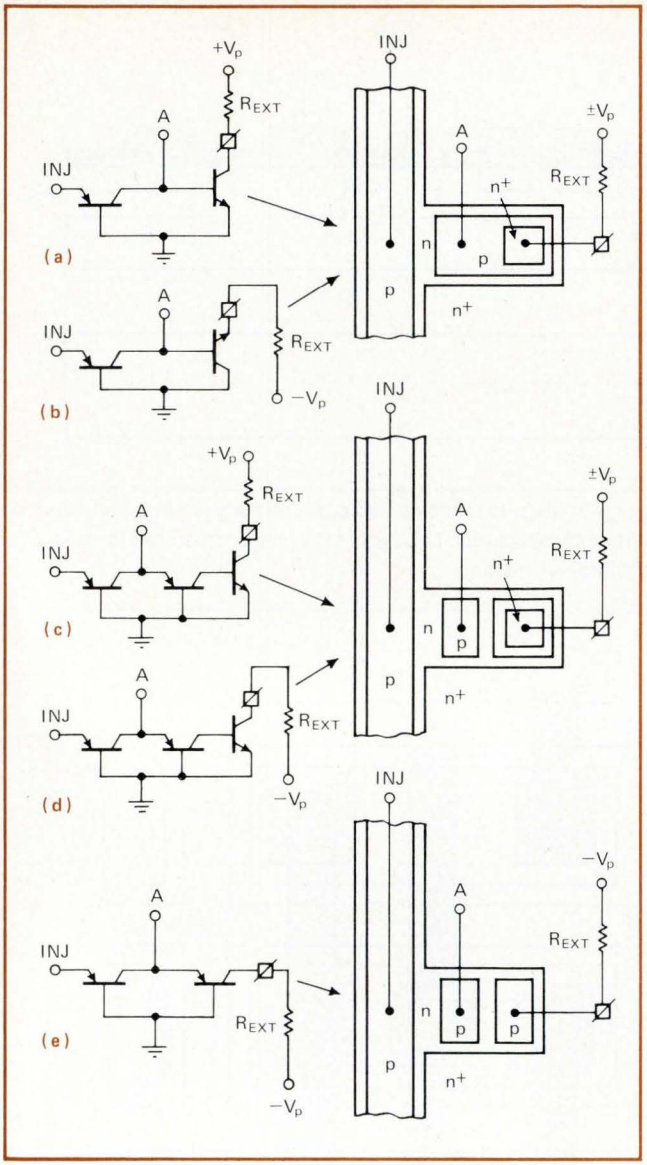
This layout guarantees that the total current, supplied over an external resistor to the injector rail, is divided equally among the gates. And since only one external resistor controls the current, the level of this current can




**2. Good combination.** An inherent advantage of the bipolar I²L technique is its ability to combine with conventionally isolated transistors on one chip. On the right are the I²L gates, on the left the conventional npn transitor structures. This part of the chip can be used to make TTL, ECL or analog circuits or any combination, any of which altogether need only seven masks.




**3. Construction.** Gates of an I²L chip (a) are situated on both sides of an injector rail, which forms the emitter of the lateral pnp current source transistor. A heavily doped n+ isolation region increases the current amplification factor of the npn transistor and kills the parasitic effects of the pnp transistors between two adjacent gates. In (b) are shown the space-saving features of I²L.




**4. Basic interface circuits.** These configurations show the circuit schematic and the corresponding chip geometry of five basic I²L interface circuits. Because each configuration uses standard processes, realization of any type of interface circuitry is easy.

be chosen even after the circuit has been processed, offering a designer great flexibility in tailoring his design to a particular current-level requirement.

Such a layout also allows a designer to adapt the base contact and collectors to a particular logic wiring pattern. Moreover, besides saving space, the compactness of the gate keeps parasitic capacitances to a minimum, preventing them from degrading circuit speed. Also, the gate's small logic voltage swings result in rapid charging and discharging of the cell capacitances, which in turn is responsible for the low speed-power product.

Injection logic can operate at very low current levels (1 nanoampere) and low logic swings (0.6 volt). Consequently, several I²L gate element configurations and interface circuits are necessary, if they are to be used along with conventional TTL and analog circuits that require higher currents and voltages.

Fortunately variations on the basic I²L layout can be readily constructed, offering the designer a multitude of tradeoffs to achieve various circuit goals. The standard I²L output device of Fig. 4a can serve as a basic current amplifier. In it, the $n^+$ collector region is connected to a positive voltage $V_p$. The logic levels therefore become O and $V_p$ volts, the latter being determined by the collector-to-emitter breakdown voltage—about 10 V—of the I²L transistor. But here the maximum output current in the gate's on state is pretty low—in the 1-microampere to 1-milliampere range, depending on both the current gain of the relatively low-capacitance I²L transistor and on the value of the injected current.

### Other basic I²L circuits

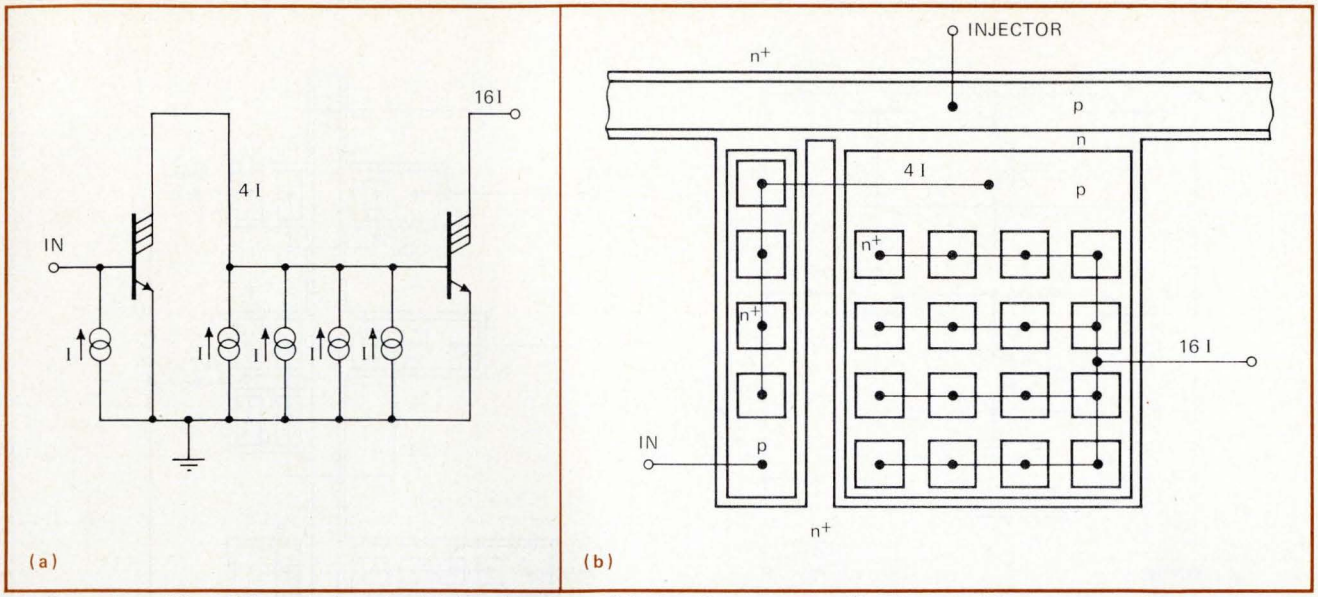
For higher current outputs, the same layout can be used if the gate's resistor is connected to a negative supply voltage (Fig. 4b). Now the $n^+$ area acts as an emitter and makes the transistor behave as an emitter follower. In this case a much higher current gain in the transistor is available and yields a considerably increased maximum output current in both logic states (10 microamperes and 10 milliamperes). But the high current output is obtained at the expense of two low-voltage logic levels, 0 and −0.7 V—and such a small difference between the two levels may be difficult to handle in certain applications.

To remedy the difficulty, a pnp transistor can be added to the output of the basic circuits (Fig. 4c) in a way that hardly changes the layout. Now, two polarities of output voltage can be obtained. For positive polarities the circuit is analogous to the basic current amplifier of Fig. 4a, in that the difference in voltages between the two logic levels is several volts. But the problem of low output currents in the on state remains.

The answer is to use a negative supply voltage (Fig. 4d). Now the difference in voltage between the two logic levels is increased because the base of the npn transistor is driven by a current instead of a voltage and the low logic level is limited by the high (10-V) collector-to-emitter breakdown voltage of the npn transistor. True, the maximum output current in this case is somewhat lower than the configuration in Fig. 4b, because the common base current gain of a lateral pnp transistor is less than 1, but it is still a respectable 0.5 mA. In any case, essentially the same layout is used for all four configurations, so that even in a packed circuit a designer is still at liberty to choose the solution that is best suited to his application.

Sometimes really high logic voltage swings are needed, in high noise environments, for example. Then the circuit of Fig. 4e might be used, to take advantage of the very high (40-V) collector-to-emitter breakdown voltage of the lateral pnp transistor. Again, this is paid for by sacrificing output current in the on state (0.1 μA–0.1 mA) due to the low current gain of lateral pnp transistors. This type of circuit is also handy in a digital-to-analog converter, where it is used to weigh the individual components.

The design of the current amplifier in Fig. 5 evolves straightforwardly from the simple configuration of Fig. 4a. In this circuit, since the current output capability in




**5. Current amplifier.** This equivalent circuit (a) and the layout (b) of an I²L current amplifier show a minimum current sink capability of 16. This can be doubled by using two stages. The four current sources in parallel are realized by making the total injecting area in the second stage four times larger than in the first stage. Subsequent stages are developed similarly.

the gate's on state is linearly proportional over a large range to the $n^+$ collector area, current amplification can be obtained by cascading I²L gates and taking care to increase the collector area at each step.

The current gain in this I²L amplifier can be determined by noting that each collector is guaranteed to sink a current equal to its base current, so that the minimum current gain of the npn transistor $h_{FE} = 1$. To provide noise margin, $h_{FE}$ typically should be 2. Thus in Fig. 5b, the minimum current sink capability is 16, and typically 32, obtained in two stages.

## A digital-to-analog converter

A digital-to-analog converter, shown schematically in Fig. 6a, can be built with I²L techniques by combining the basic current amplifier (transistors $S_1$ to $S_4$) with the lateral pnp interface output configuration of Fig. 4e. Now, if the input of $S_1$ is high, then the current I delivered by the lateral pnp transistor $P_1$ is short-circuited by $S_1$. In that case no current flows in the collector of the output transistor $T_1$. On the other hand, if input A of $S_1$ is low, it draws no current but instead allows a collector-current $\alpha$I to flow in $T_1$, where $\alpha$ is the common base-current gain factor of $T_1$.

This is the first amplification stage of the converter. Each successive stage contains twice as many elements as its predecessor, and any number of the stages can be cascaded to achieve the desired converter resolution—four stages for a 4-bit device, six stages for a 6-bit device, and so on.

The layout of a 4-bit d-a converter is shown in Fig. 6b, where an I²L transistor is used for $S_1$ and where the proper signal summing is achieved by doubling the number of transistors in each succeeding stage. On silicon this means putting two transistors of the $P_1$ type in parallel for a sum of $P_2$, putting two $T_1$s in parallel for a sum of $T_2$, and so on. As a result, transistor $S_2$ of Fig. 6a must now be able to sink 2I, a requirement that can be realized by simply doubling its collector area.

In the same way 4I and 8I current values can be realized in succeeding stages, and, depending on the logic levels of the four input terminals A, B, C, and D, a current from 0 to 15 $\alpha$I is available at the output terminal. High-resolution accuracy can be obtained because the circuit is built up from a number of identical transistors—to realize the second, third and fourth stage, the right number of transistors is simply put in parallel.

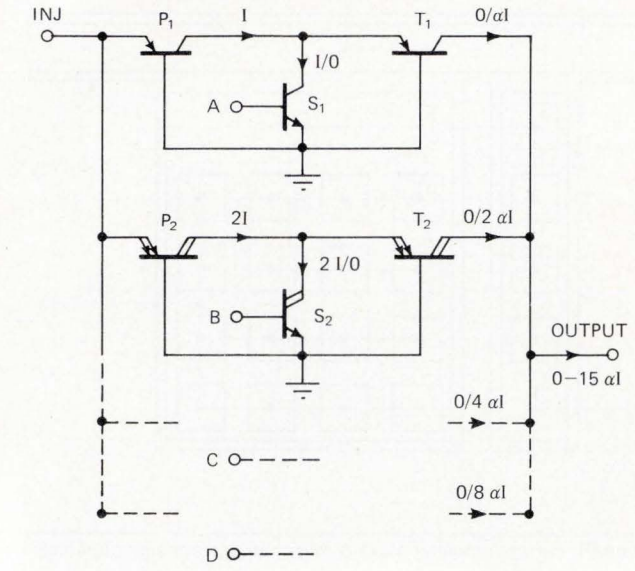
## TTL compatibility

For the many applications where I²L circuits must be combined with TTL circuits on the same chip, compatibility between the logic elements must be assured. That is to say, the switching threshold point and current levels of the two logic families must be made compatible.

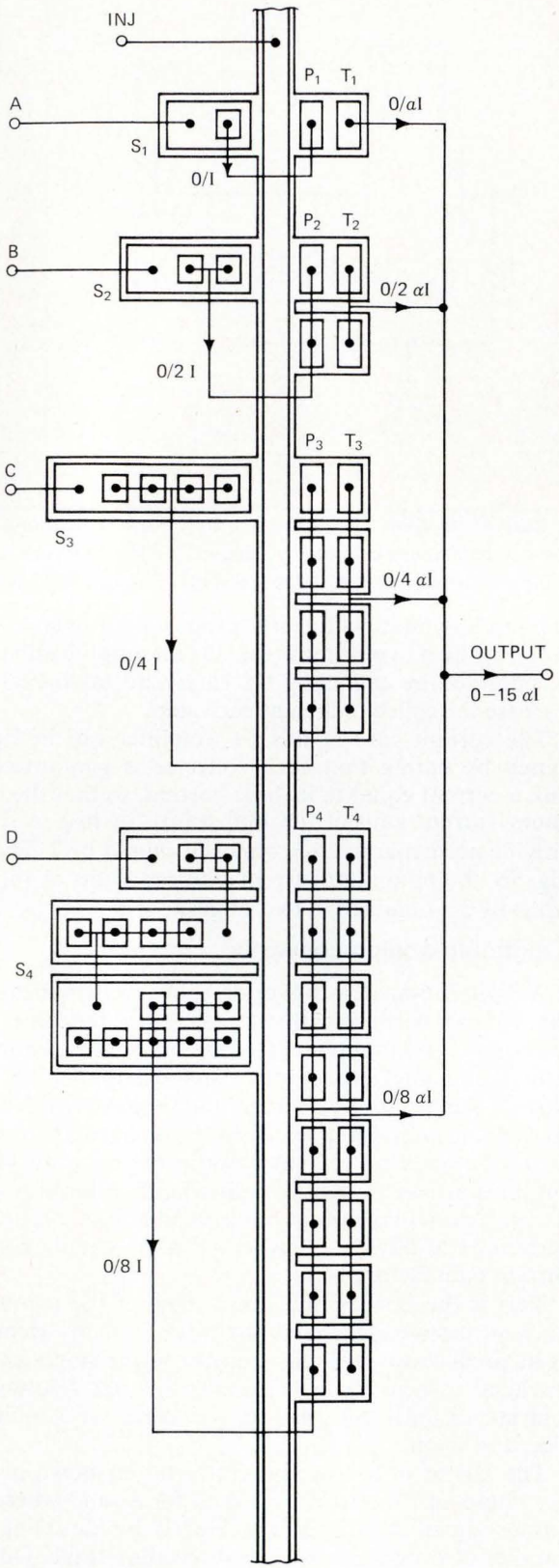
Generally a TTL load current is 1.9 mA per fanout for a low logic condition and 20 $\mu$A or less for its high condition. Since an I²L gate, on the other hand, works at a current level between 1 and 20 $\mu$A per gate, two types of interface circuits are necessary—one at the gate inputs as an interface from TTL to I²L, and one at the gate output as an interface from I²L to TTL.

The electrical diagram of the input condition is shown in Fig. 7a. For the situation where the TTL gate is at its low logic level, the realization of the proper interface condition follows automatically because a normal TTL imput current will flow if appropriate resistor values are chosen. For the high logic TTL condition, however, care must be taken that the inverse current gain of I²L transistor $T_1$ does not affect the input current of the TTL transistor.

In normal TTL fabrication, this is achieved with a gold diffusion in the transistor base to diminish the loading effect of a high inverse current gain. But on a chip containing I²L gates, the I²L inverse current gain has to be high for proper gate operation. The way round this dilemma is to short-circuit the collector-base junc-




(a)




(b)

**6. Digital-to-analog conversion.** Schematic of the first and second stage of a 4-bit d-a converter shows that by putting the right number of $P_1$, $T_1$ and $S_1$ structures in parallel any number of bits can be realized. In the schematic layout of a 4-bit d-a converter (b), the transistors $P_2$, $P_3$ and $P_4$ are built up by putting several $P_1$ structures in parallel. The same is done for $T_2$, $T_3$ and $T_4$.

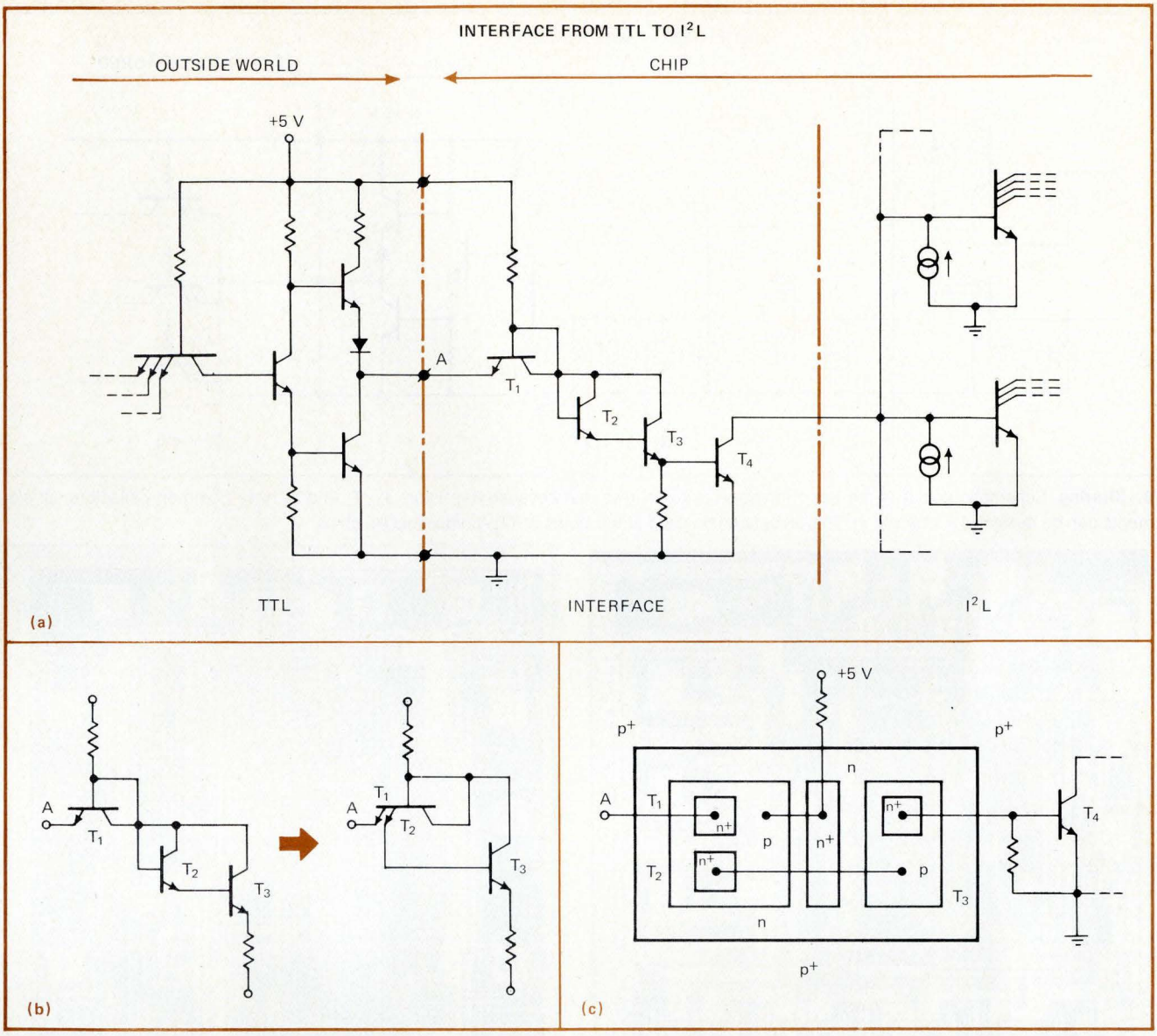
tion of transistor $T_1$ in the interface circuit and add an extra diode $T_2$ to make the input threshold voltage again equal to the required TTL threshold level.

The corrected transistors $T_1$, $T_2$, and $T_3$ are redrawn in Fig. 7b. Since $T_1$ and $T_2$ have a common base and collector, they are drawn as a multi-emitter structure with the base-collector junction short-circuited. One emitter serves as the input of the interface circuit, the other connects to the base of $T_3$. And because $T_3$ has a common collector with $T_1$ and $T_2$, all three can be located on one isolated island, as shown in Fig. 7c.

As for transistor $T_4$, its emitter is connected to ground giving the designer the freedom of building it as a conventional isolated transistor or as an inverted $I^2L$ transistor without current source. The choice depends on the number of fanouts desired. For use as a clock or a reset line, say, the normal high-gain version is preferable. For a few fanouts the $I^2L$ transistor type can be used.

Figure 8 shows the circuit for interfacing $I^2L$ to TTL. Here the problem of linking the low $I^2L$ current level of 1 to 10 μA per gate to the much larger TTL current of 1.9 mA is solved in two steps. The first step is the current amplifier, as realized in Fig. 5b and here serving as a first input buffer. The second step is an output stage of isolated transistors that exploit the high $I^2L$ forward-current amplification factor to boost the current into the TTL input range. The layout of this current amplifier depends on the current level of $I^2L$ and on the number of TTL fanouts required.

Today's technology requires the circuit designer to use two chips to build a low-level digital logic array and




**7. Interfacing.** The basic interface circuit (a) from TTL to I²L has three buffer transistors $T_1$, $T_2$, and $T_3$. To go from I²L to TTL in (b), $T_1$ and $T_2$ form a current amplifier. On silicon, $T_1$ and $T_2$ can be realized with a multi-emitter structure (e).

the necessary power output circuits. The I²L approach lets him do both on the same chip. An example is an 8-bit shift register with latches and power output circuits (Fig. 9), built as a driver stage for alphanumerical display systems. The I²L section of the chip is on the left near the chip's center. It is laid out so that the gates are on either side of an injector rail that's covered with aluminum to maintain a uniform current distribution.

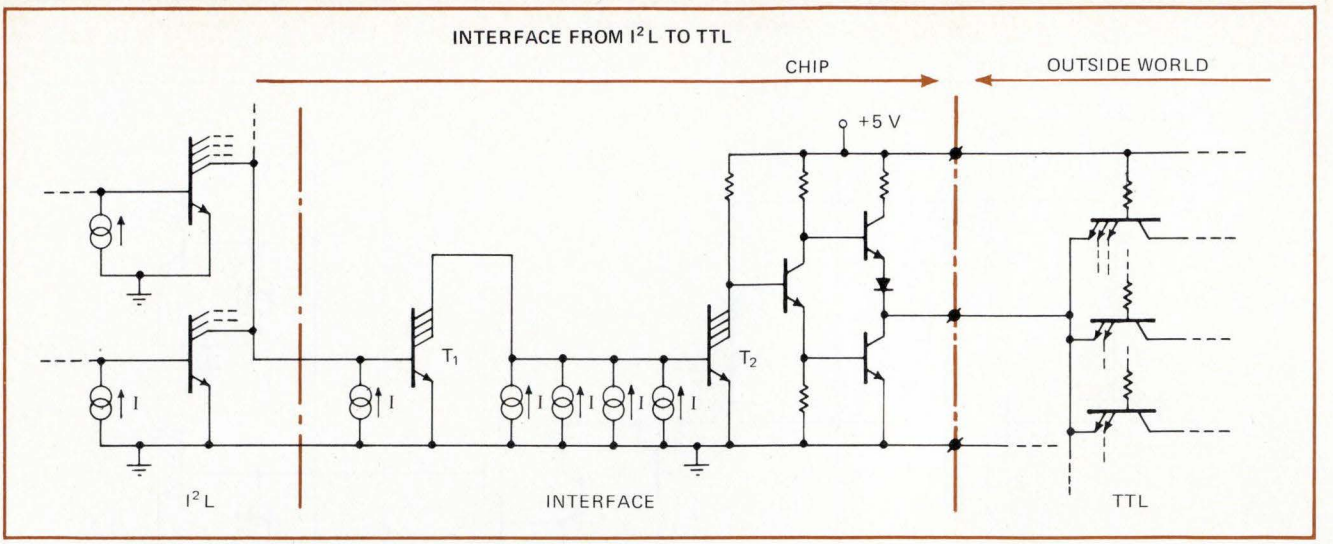
The inputs to the I²L circuits, located at the top of the chip, are made TTL-compatible with the interface circuit of Fig. 7c. At the right and bottom part of the chip are the eight power-output circuits of an open collector type, supplying an output current of typically 100 mA—an example of how low-power I²L gates (10 μA) can be combined with high-drive power output circuits (100 mA) on one chip. Some typical data on the 8-bit power shift register is summarized in Table 2.

The details of the I²L region are discernible on the shift-register chip, where the gates on both sides of the injector rail and current amplifiers are clearly evident. The required power up-conversion is done by interconnecting several collector regions. It takes two stages, the first stage forming a part of the I²L gate of the subsequent stage to save space.

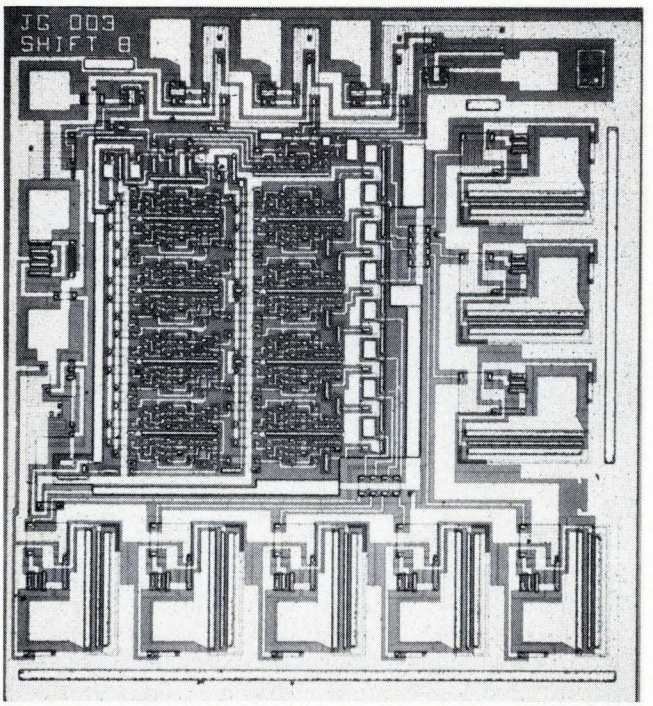
## A motor speed control chip

Another circuit combining I²L and analog circuits on one chip is the motor speed control chip of Fig. 10 where revolutions of the motor are sensed by a photodiode that delivers input pulse data to the chip. There, a 9-bit counter counts these pulses. The four most significant bits of the counter output control first-order motor power. The five least significant bits are stored in latches which drive a 5-bit d-a converter. The output of this converter is amplified, and the amplified signal in turn controls the fine range of power supplied to the motor.

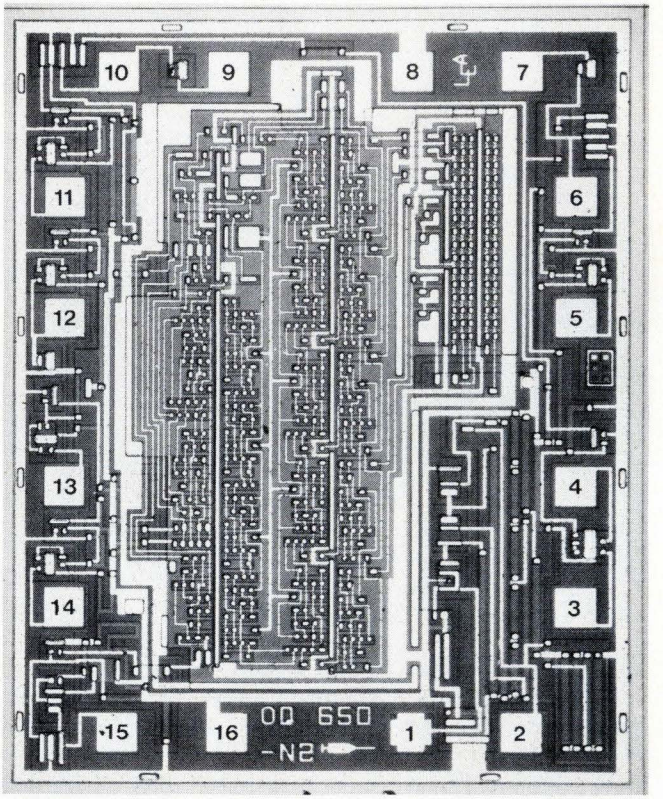
Again, the I²L gates are located in the center of the chip, on both sides of two injector bars laid out from top




**8. Sharing.** Schematic layout of the basic interface circuit shows that because transistors $T_1$, $T_2$ and $T_3$ have common collectors, all elements can be designed in one island. This layout can be used at the inputs of TTL-compatible I²L chips.




**9. Implementation.** Microphotograph of 8-bit power shift-register chip (a) shows the I²L gates at the center and the power output stages at the bottom and right, between the bonding pads.




**10. At the controls.** Microphotograph of motor speed control circuit has I²L elements in the center as well as TTL input interface circuits between the bonding pads on the left.

to bottom. The inputs (bonding pads 5, 11, 12, 13 and 14, for instance) have been made TTL-compatible, again with the interface circuit of Fig. 7c.

In this respect, it's interesting to note that the interface circuits can also be used to realize logic functions. If the input transistor $T_1$ in the basic interface circuit (Fig. 7a) has a multi-emitter structure, then the normal AND function of the input signals is obtained.

This principle has been applied in the motor control chip on inputs 3 and 4. One output is a TTL totem-pole (bonding pad 15), while the motor outputs, forward and reverse (bonding pads 10 and 6 respectively), are open-collector-type structures with a current sink capability greater than 20 mA and a saturation voltage less than 300 mV. The data is tabulated in Table 3.

Note that the 5-bit d-a converter has 1 + 2 + 4 + 8 + 16 equal current sources. In addition, 16 other equal current sources work with an on-chip operational amplifier to control the injector current. The voltage drop over the injector bars could result in nonuniform current distributions, and care has been taken to minimize it so that the output of the d-a converter shows no discontinuities. □