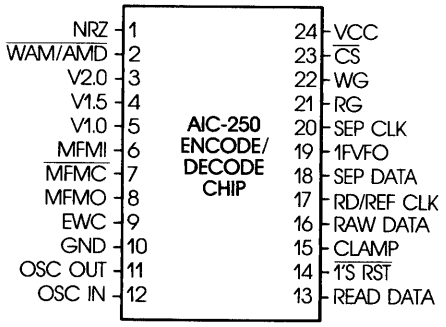
Encoder/Decoder

PRELIMINARY

- **Full NRZ to/from MFM Encode and Decode**
- **500 KHz to 5 MHz Bit Rates**
- **Address Mark Generation and Detection**
- **Write Precompensation without External Delay Lines**
- **Minimum Passive Support Components**
- **Minimum Board Space Requirements**
- **Locks onto Preamble within First 2 Bytes**
- **Single +5V Power Supply**



DESCRIPTION

The Adaptec AIC-250 Encode/Decode Chip is a 24 pin custom LSI device which provides an efficient data interface between NRZ data and MFM recorded disk drives with a minimum of external support. Together with the AIC-100 and AIC-300 these 3 chips are the core of a Winchester disk controller.

This chip performs all the functions necessary to convert NRZ data to and from MFM compensated data. An external variable frequency oscillator is also necessary to convert from MFM to NRZ data. The AIC-250 also incorporates address mark generation and detection logic. This feature includes VFO sync field circuitry which enables the VFO data lock-on and performs address mark search and detection. This ENDEC (Encode/Decode) device also includes the ability to delete a clock pulse in an outgoing MFM data stream, thereby generating address marks when formatting the drives.

Write precompensation circuitry in the AIC-250 enables a controller to compensate for the tighter bit spacing on high density inner tracks. All delay functions are contained within the package itself. The components required external to AIC-250 are the crystal and its passive components; a passive network to determine early, on-time and late data bits; any clocking and pulse shaping circuitry; and phase locked loop.

The AIC-250 is designed to operate at bit rates from 500 KHz to 5 MHz, covering a wide range of MFM floppy and Winchester disk drives currently available. The chip is capable of supporting several drive interfaces including but not limited to the ST506/412.

AIC-250 PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME AND FUNCTION
NRZ	1	IN/OUT	NRZ READ/WRITE DATA: Non-return to zero data between AIC-250 and AIC-100. It connects to pin of same name on Adaptec AIC-100 Winchester controller. This pin is an output when RG is active.
$\overline{\text{WAM/AMD}}$	2	IN/OUT	WRITE ADDRESS MARK/ADDRESS MARK DETECT: A pulse is input when write gate is active and an address mark is to be written. When read gate is active, a latched output is used for address mark detect. Connected to pin of same name on Adaptec AIC-100.
V2.0	3	IN	VOLTAGE = 2.0: An input voltage reference point used on the MFM ramp to derive the late write precompensation point.
V1.5	4	IN	VOLTAGE = 1.5: An input voltage reference point used in a similar manner as V2.0, above, to derive the on-time write precomp point.
V1.0	5	IN	VOLTAGE = 1.0: Same as above, except used to derive the early write precomp point.
MFMI	6	IN	MFM IN: The input for the RC ramp which is derived through external logic providing an RC time constant, driven by a 7438.
$\overline{\text{MFMC}}$	7	OUT	MFM WRITE DATA: Compensated MFM Write Data that is sent to the drive. Compensation is enabled by the EWC input.
MFMO	8	OUT	MFM OUT: Used to drive the 7438 which is used to drive the external RC time constant for MFMI.
EWC	9	IN	ENABLE WRITE PRECOMP: Used when the drive requires write precompensation on. When this pin is high during RG, the VFO Sync field search is disabled. This mode is used in hard sectored applications.
GND	10		GROUND.
−OSC OUT	11	OUT	OSCILLATOR OUTPUT.
−OSC IN	12	IN	OSCILLATOR INPUT.
READ DATA	13	IN	READ DATA: This is the MFM input read stream from the disk. Note: pulse shaping is recommended, between the drive interface and AIC-250.
1's $\overline{\text{RESET}}$	14	IN	1's RESET: Resets the counter to detect 16 zeros after Read Gate is valid.
CLAMP	15	OUT	CLAMP: Output to external VFO which occurs after count of 16 zeros is reached and raw data source is switched from 2FOSC to the read data stream. This is a two to three bit wide pulse.
RAW DATA	16	OUT	RAW DATA: The raw data stream to be output to the external VFO. Source for this output is either the OSC IN or READ DATA.
RD/REF	17	OUT	READ REFERENCE CLOCK: Output to the AIC-100 Winchester controller which is sourced from the VFO oscillator during Read Gate active. Otherwise sourced from the write oscillator.
SEP DATA	18	IN	SEPARATED DATA: This is the data input from the external data/clock separator.
1FVFO	19	IN	1FVFO: This is a fundamental VFO input from the external data/clock separator.

AIC-250 PIN DESCRIPTION (Continued)

SYMBOL	PIN	TYPE	NAME AND FUNCTION
SEP CLK	20	IN	SEPARATED CLOCK: This is the clock input from the external data/clock separator.
RG	21	IN	READ GATE: An input generated by the AIC-100, which signals the phase lock loop to lock onto the read data stream coming from the drive.
WG	22	IN	WRITE GATE: An input generated by the AIC-100, which is used to gate the write data stream to the drive interface.
$\overline{CS}$	23	IN	CHIP SELECT: Is used to select the AIC-250. In most applications, this pin may be tied to ground.
V_{CC}	24		+5 Volts.

FUNCTIONAL DESCRIPTION

The AIC-250 Encode/Decode Chip has three major areas of logic:

1. Data encode/precompensation circuitry.
2. The sync field search circuitry and counter.
3. Address mark detect and data decode circuitry.

The functional block diagram is shown in Figure 1. The data encode/precomp circuitry is used during a disk write operation (NRZ to MFM conversion), and the sync field search circuitry, address mark detect and data decode circuitry are used during a disk read operation (MFM to NRZ conversion). These two operations are discussed below.

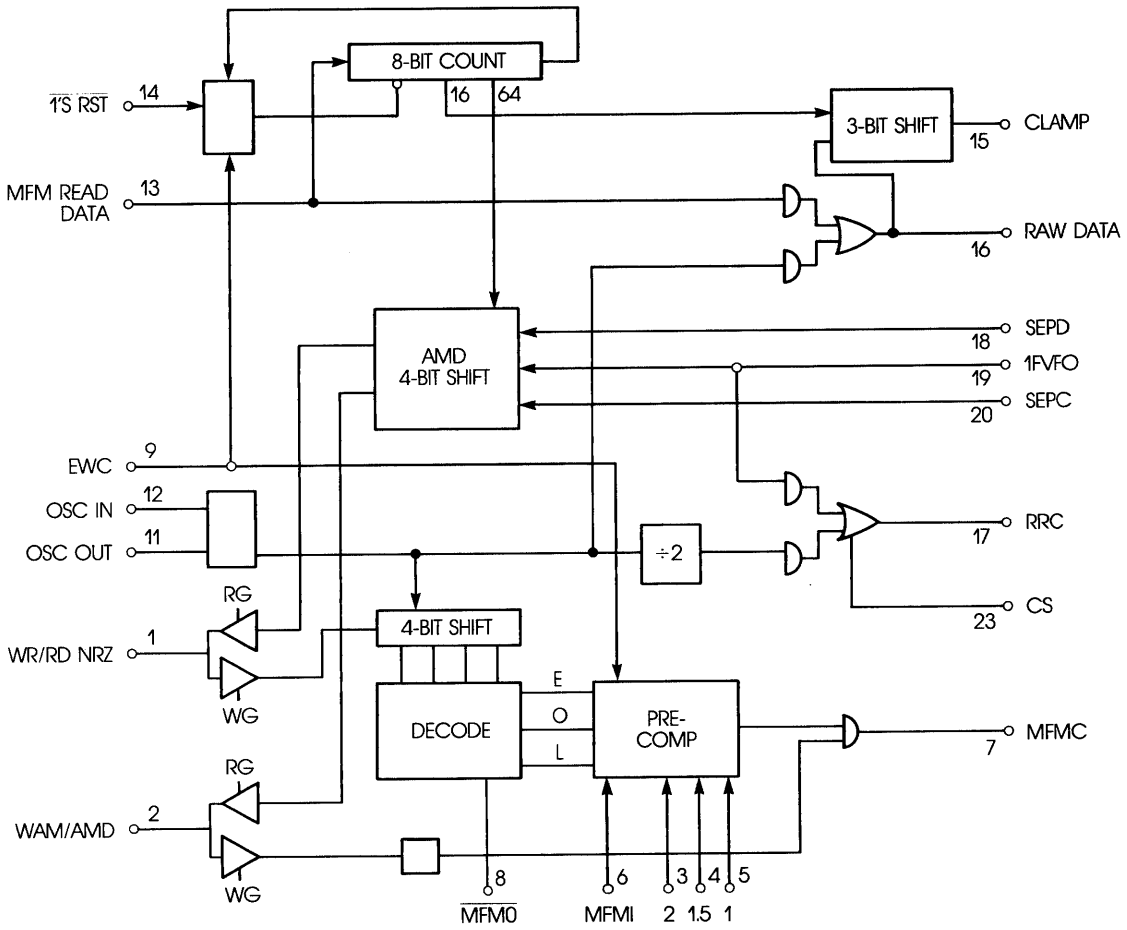


FIGURE 1. ENDEC BLOCK DIAGRAM

Write Disk Operation

WRITE DATA: During a write operation, the AIC-250 chip converts NRZ format data to MFM format. In addition to this, the chip also appends address marks, to define the start of the ID field and the data fields. The AIC-250 chip also has the necessary circuitry for write precompensation.

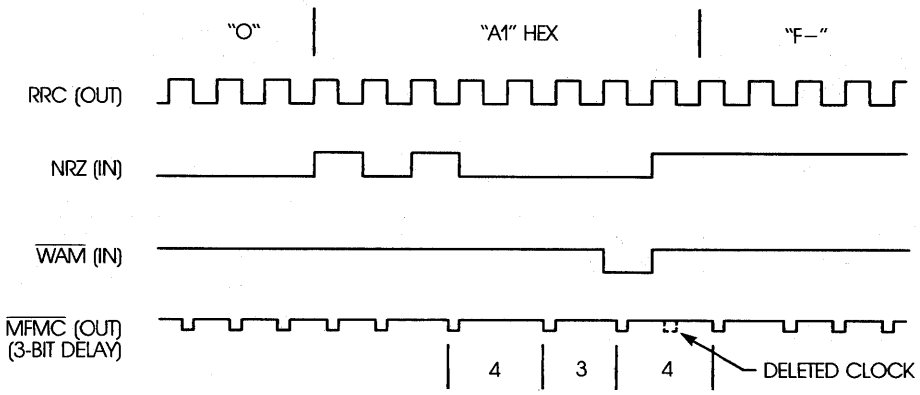
The AIC-250 chip receives serial NRZ data (typically from the AIC-100 Winchester disk control chip). This data is clocked and latched such that the bit cell boundaries are defined. During a format operation, the chip receives serial data which includes gaps, sync fields, address marks, data and ECC fields. During a write operation the chip receives only the data and ECC fields.

The serial bit stream received by the AIC-250 chip are optimized for a disk controller, in that it consists of clocked data of high and low levels. However, since it is not convenient or efficient to write to the disk both data and clock, a self clocking MFM code is used. MFM coding is more efficient than FM for use on a disk drive. MFM is self clocking and encodes data patterns on bit cell boundaries as well as within cells. When decoded later, data and clock information can be separated to again define bit cell boundaries and data.

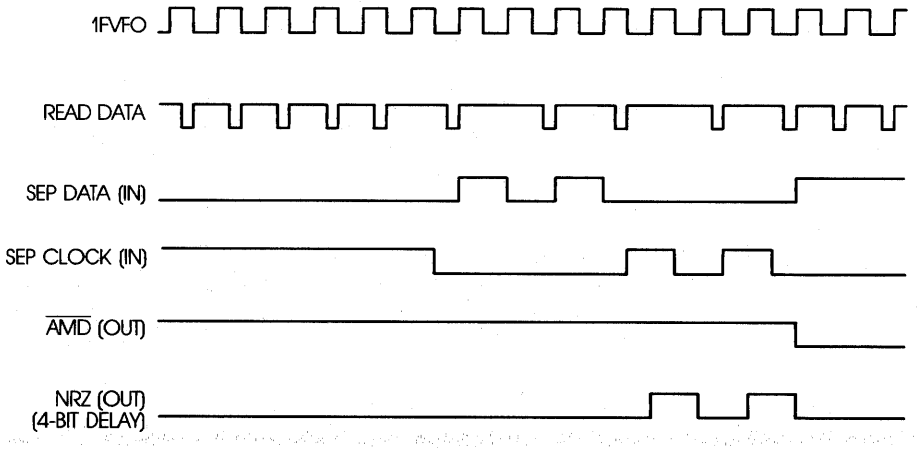
When the MFM data is written to the disk drive, certain reference points must be defined in order to recover data later. These reference points are called address marks. The AIC-250 inserts these address marks into the data pattern it receives from AIC-100. These address marks are unique illegal data patterns, so as to not confuse them with valid address, data, gap, sync or ECC fields.

The address mark is created in the serial data stream by gating the WAM (Write Address Mark) signal with the MFM data pattern. WAM blocks one pulse in the A1 pattern to produce a "434" pattern. Later when read, this 434 pattern defines the beginning of ID address mark. Conversely, this pattern appears in the data address mark. The above reference timing diagrams show the NRZ data and MFM data during address mark generation and detection.

WRITE ADDRESS MARK TIMING



ADDRESS MARK DETECT TIMING



WRITE PRECOMPENSATION: Write precompensation is a method of reducing the occurance of bit shift caused by specific data patterns, when many bits are positioned closely together (for example, on the inner cylinders of the disk drive). These bit shifts can cause read timing errors. A write precompensation circuit usually consists of a delay line with several taps at different time delays. Certain data patterns will cause bit (peak) shift. The circuit recognizes these patterns and adds or subtracts time to each bit when required, to minimize bit shift.

Write precompensation is accomplished by the AIC-250 without the need of an expensive external delay line. The output "MFMO" drives a 7438 inverter whose output in turn drives an external RC ramp generator. This ramp is input on "MFMI." Internal to the AIC-250 are three high speed voltage comparators with references set at 1.0, 1.5 and 2.0 volts by external resistors. As the ramp voltage on "MFMI" passes through these three reference points, early, ontime and late delays are generated and the appropriate pulse is output on the "MFMC" pin (WRITE DATA).

Read Disk Operation

During a read operation, the AIC-250 chip works in conjunction with external VFO circuitry, to convert MFM data to NRZ data. The VFO circuitry can also be referred to as a data separator. A block overview of the data separator is shown in Figure 2.

The two signals that interface to the VFO are "RAW DATA" and "CLAMP." The raw data input to the VFO is the signal that the VFO is required to track. When "READ GATE" is off, the raw data output of the AIC-250 is "2FOSC." The purpose is simply to provide an input to the VFO that will keep the VFO pumped to nominal disk data rates.

When "READ GATE" is turned on, a sequence of events must occur for a successful transition from "2FOSC" feeding the VFO to "READ DATA" feeding the VFO. The sequence is as follows.

1. After RG is on, the counter must count 16 zeros in a row. Any time a one is detected externally, a "ONE'S RESET" input will occur to restart the counter. The "ONE'S RESET" input will be a minimum of 40 ns in width, and is typically implemented with a retriggerable one-shot of 1.25 × bit cell duration.

2. When count 16 is reached, a latch is set that will switch the "RAW DATA" source from "2FOSC" to "READ DATA" and generate a "CLAMP" output. The "CLAMP" signal is guaranteed to be at least 2 data periods in length and its trailing edge will follow the "RAW DATA" output by not more than 15 ns or precede it by no more than 10 ns.

3. With "READ DATA" feeding the VFO, the counter will continue for 48 more counts to a maximum of 64. During this period, if a "ONE'S RESET" occurs, the counter will be reset, a "CLAMP" signal will occur, and the "RAW DATA" source will be switched back to "2FOSC." If "ONE'S RESET" does not occur, a latch will be set that allows for the detection of an address mark and disallows any further "ONE'S RESET" from effecting the counter. This latch will also switch the "RD/REF CLOCK" output source from the divided "2FOSC" to "1FVFO." There are no timing constraints for this switch to occur and a glitch will be output on the RD/REF clock at this point.

4. The counter continues to run while the AM detector is looking for an address mark. If the counter

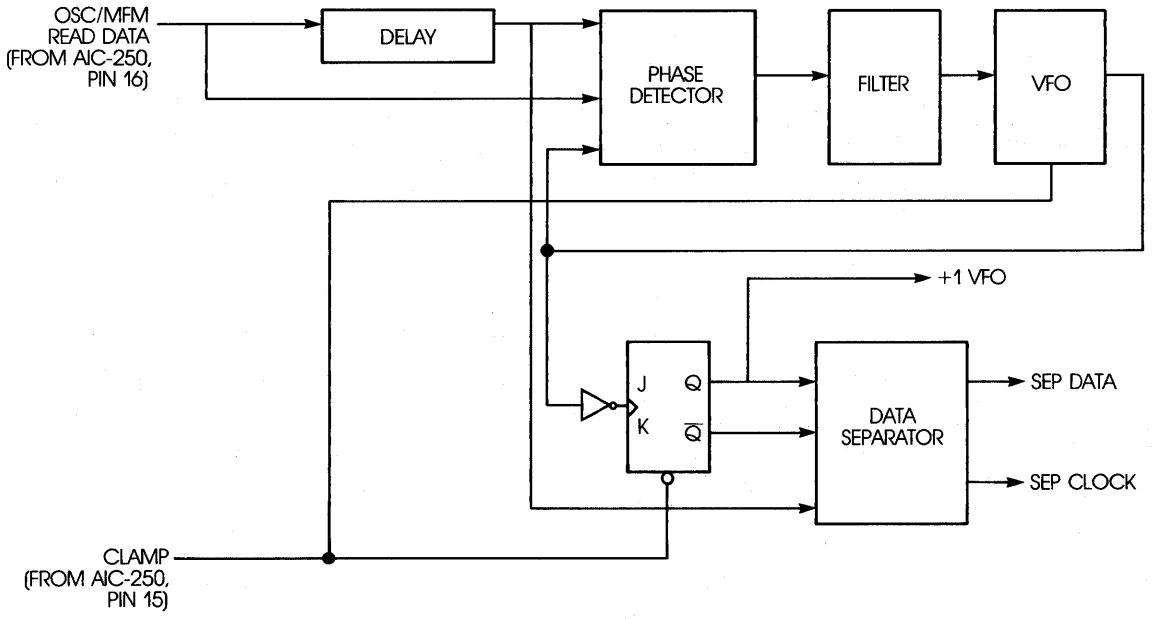


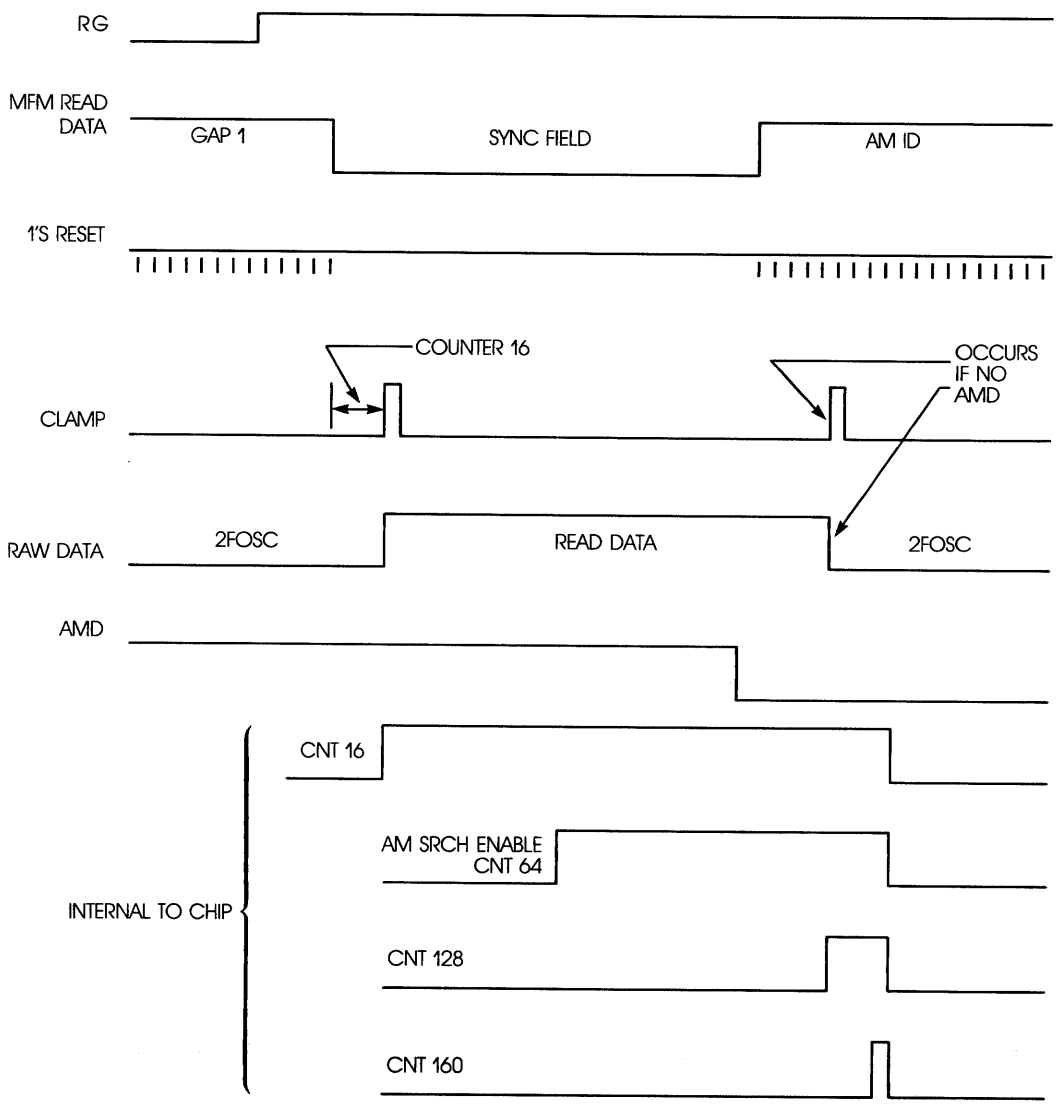
FIGURE 2. VFO BLOCK OVERVIEW

reaches count 128 without an AM detected, the count 16 latch will be reset, causing a "CLAMP" signal to be generated and "2FOSC" to be output to the VFO. Also, the search AM latch will be reset, disabling the AM detector and switching the source for the "RD/REF CLOCK" output. The VFO will be input with "2FOSC" for 4 byte times and the sequence will begin again at Step 1.

If an address mark is found, the "AMD" latch will be set and its output will appear on the "WAM/AMD" pin. The AMD latch being set will disable any further contributions to the sequence by the counter, allowing the data field to be read.

5. At any time "RG" may be turned off, resetting the counter and causing a "CLAMP" signal to be generated and the "RAW DATA" source changed to "2FOSC."

A reference timing diagram is shown below.



The external data separator takes the RAW DATA input, and outputs separate clock and data. A read reference clock signal at the data transfer rate is provided by VFO circuitry. The ENDEC chip uses these inputs to generate NRZ data, which is fed to the AIC-100 disk controller chip, along with the read reference clock.

The chip simplifies ST412 interface Winchester disk controller design, due to the fact that it needs very few external passive components. A typical configuration of the ENDEC for a 5MHz data rate is shown in Figure 3.

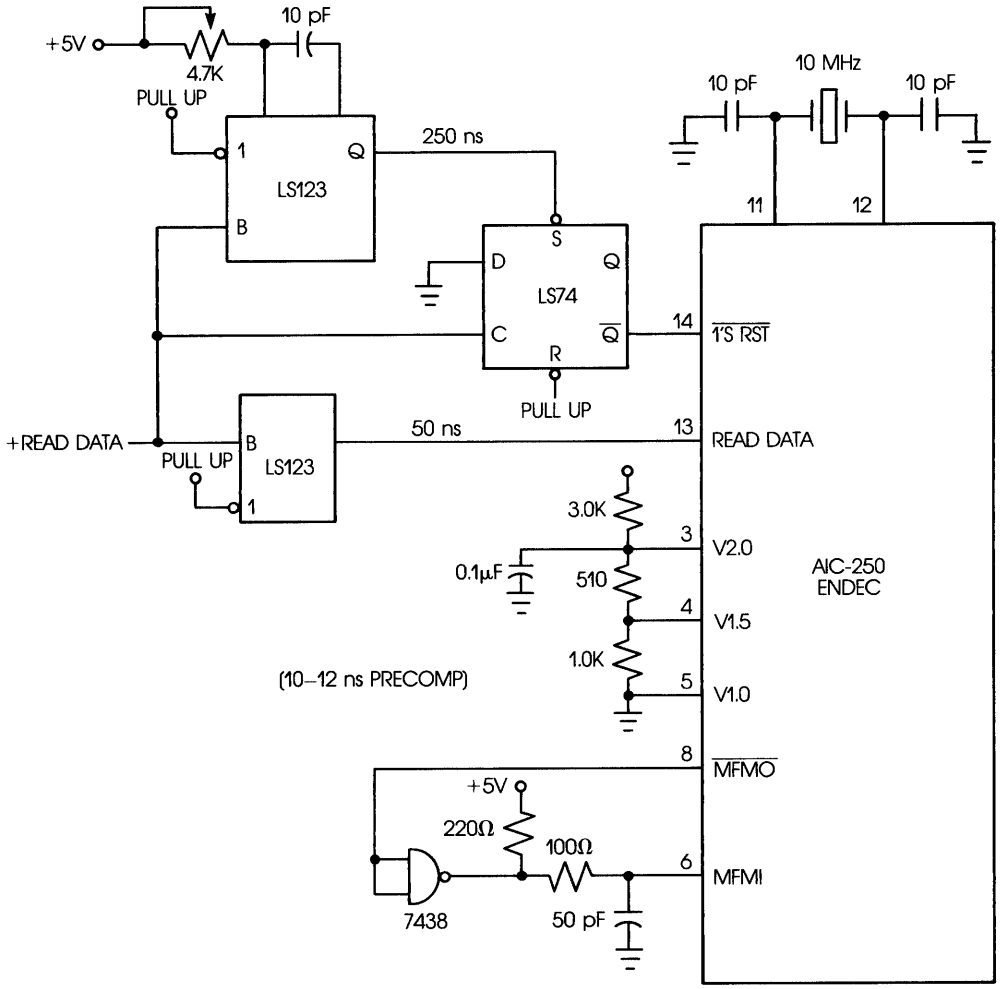


FIGURE 3. EXTERNAL COMPONENT REQUIREMENTS AT 5 MHz DATA

ABSOLUTE MAXIMUM RATINGS

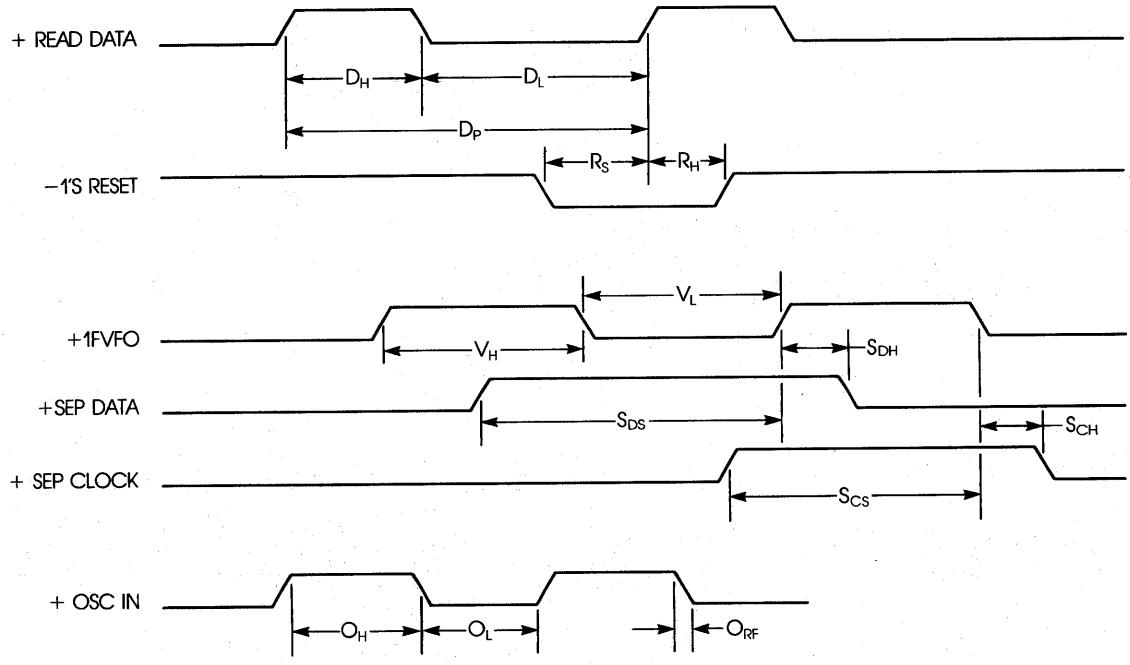
Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 to 7 volts
Power Dissipation ..... 0.14 watt
Power Supply Voltage ..... 4.75 to 5.25 volts

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

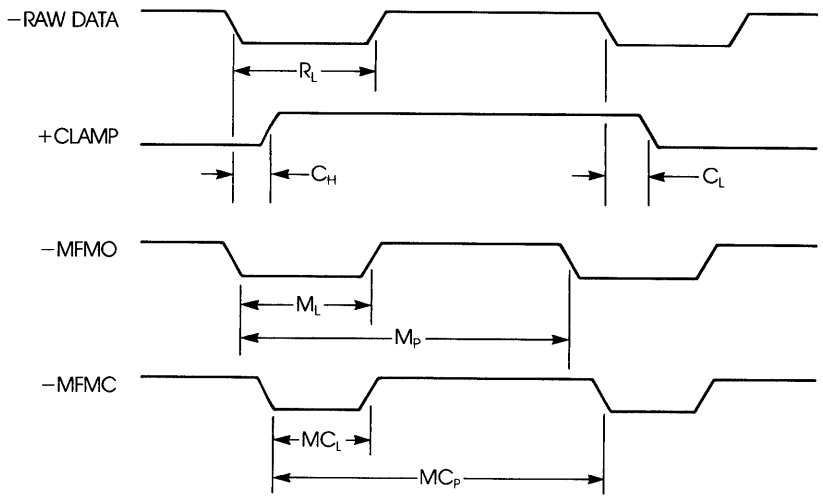
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage (All Except OSC)		0.4	V	
V_{IL}	Input Low Voltage (OSC)		0.8	V	
V_{IH}	Input High Voltage (All Except OSC)	2.4		V	
V_{IH}	Input High Voltage (OSC)	3.0		V	
V_{OL}	Output Low Voltage (All Except OSC, RD/REF, NRZ and WAM/AMD)		0.4	V	I_{OL} = 2 mA
V_{OL}	Output Low Voltage (OSC, RD/REF, NRZ and WAM/AMD)		0.3	V	I_{OL} = 0.8 mA
V_{OH}	Output High Voltage (All Except OSC, RD/REF, NRZ and WAM/AMD)	2.4		V	I_{OH} = −400 µA
V_{OH}	Output High Voltage (OSC, RD/REF, NRZ and WAM/AMD)	3.0		V	I_{OH} = −400 µA
I_{CC}	Supply Current		25	mA	
I_{IL}	Input Leakage	−10	10	µA	$0 < V_{IN} < V_{CC}$

AIC-250 INPUT TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
D_H	Read Data High	45		ns
D_L	Read Data Low	40		ns
D_P	Read Data Period	120	4000	ns
R_S	One's Reset ↓ to Read Data ↑	35		ns
R_H	Read Data ↑ to One's Reset ↑	20		ns
V_H	1FVFO High	60		ns
V_L	1FVFO Low	60		ns
S_{DS}	Sep Data Setup to 1FVFO ↑	70		ns
S_{DH}	Sep Data Hold	10		ns
S_{CS}	Sep Clock Setup to 1FVFO ↓	70		ns
S_{CH}	Sep Clock Hold	10		ns
O_H	OSC in High	40		ns
O_L	OSC in Low	40		ns
O_{RF}	OSC in Rise or Fall		8	ns
Chip Select Read Gate Write Gate Enable Write Comp	These four inputs are control inputs that have no critical timing requirements and are responded to within 2 full clock periods.			

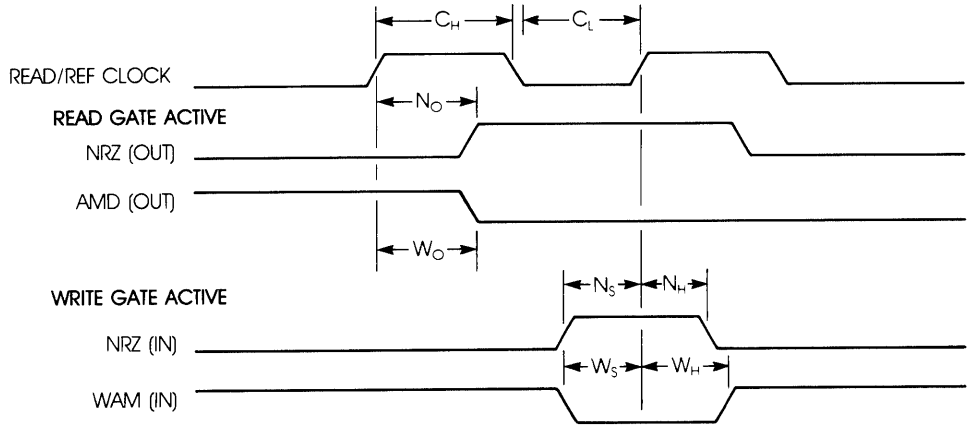
AIC-250 OUTPUT TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
R_L	Raw Data Active Low	27		ns
C_H	Raw Data ↓ to Clamp ↑		11	ns*
C_L	Raw Data ↓ to Clamp ↑		14	ns*
M_L	MFM Out Low	55		ns
M_P	MFM Out Period	120		ns
MC_L	MFMC Low with Compensation	20		ns
MC_P	MFMC Period without Delay	120		ns

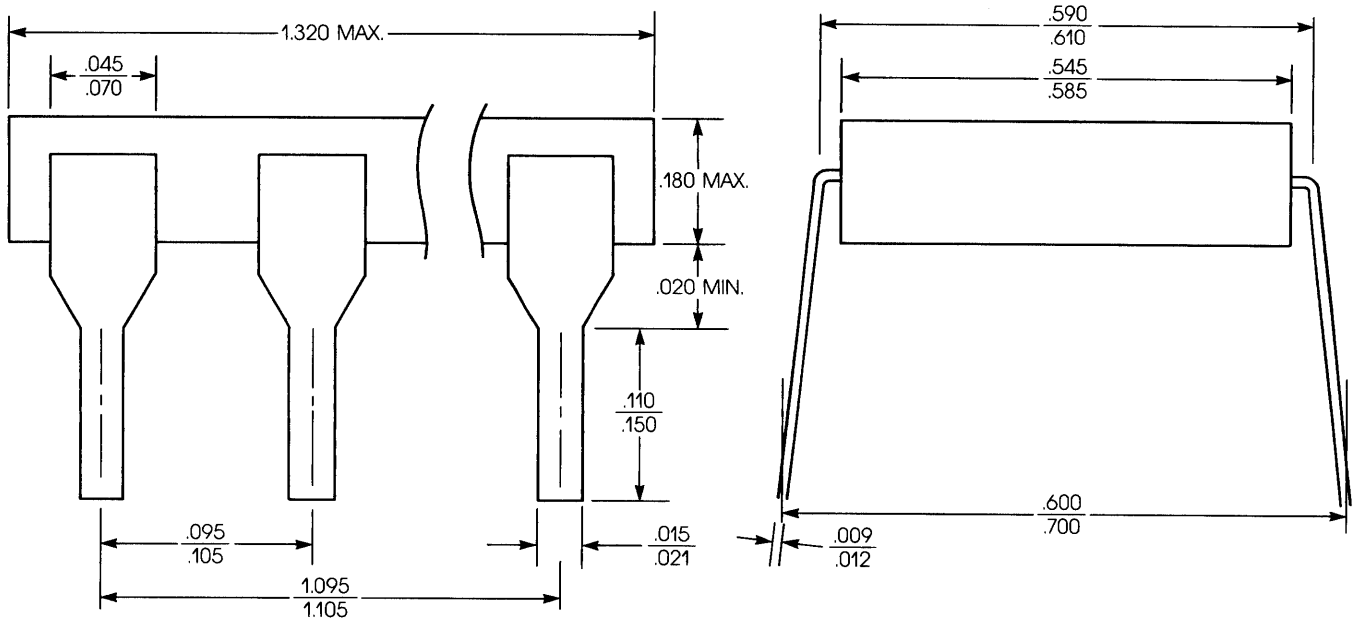
*Raw data and clamp have equivalent loading.

AIC-250 BI-DIRECTIONAL TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
C_H	Read/Ref Clock High	56		ns
C_L	Read/Ref Clock Low	56		ns
N_O	Read/Ref ↑ to NRZ Out Valid	10	95	ns
W_O	Read/Ref ↑ to WAM Out Valid	10	95	ns
N_S	NRZ in Set-up to Read/Ref ↑	40		ns
N_H	Read/Ref ↑ to NRZ in Hold	10		ns
W_S	WAM in Set-up to Read/Ref ↑	40		ns
W_H	Read/Ref ↑ to WAM in Hold	10		ns

PACKAGING INFORMATION



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